

P264: MXM-II, G3, 256MB, 128-bit, 4/8Mx32DDR LVDS, DVI_A, DVI_B, TV_OUT, VGA

HISTORY:


A00: INITIAL VERSION -
600-10264-00xx-000

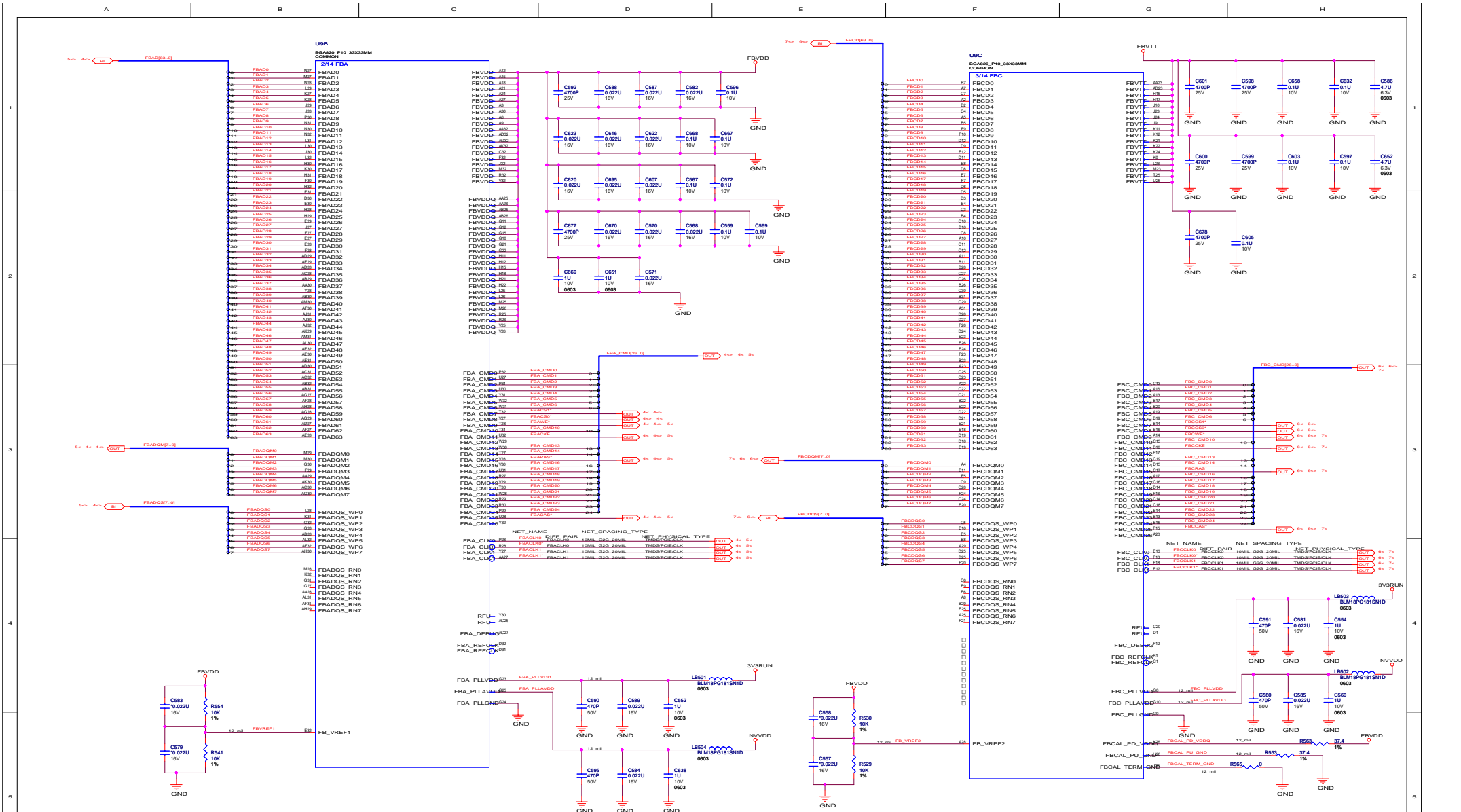
3/18/04 - Stated P264 from P263 design

| REV | VARIANT | NVPN | ASSEMBLY |
|-----|-------------|--------------------|--|
| B | BASE | 600-10264-xxxx-vvv | BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES |
| 1 | SKU000 | 600-10264-0000-000 | 600-10264-0000-000 (128bit) DDR1 8Mx32 144BGA, LVDS + DVI_A/DVI_B + TV_OUT + |
| 2 | SKU001 | 600-10264-0001-000 | 600-10264-0001-000 (128bit) DDR1 8Mx32 144BGA, LVDS + DVI_A/DVI_B + TV_OUT + |
| 3 | SKU002 | 600-10264-0002-000 | 600-10264-0002-000 (128bit) DDR1 4Mx32 144BGA, LVDS + DVI_A/DVI_B + TV_OUT + |
| 4 | <UNDEFINED> | <UNDEFINED> | <UNDEFINED> |
| 5 | <UNDEFINED> | <UNDEFINED> | <UNDEFINED> |
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PAGE: 2000 (2000 of 2000) details

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PAGE 2/28

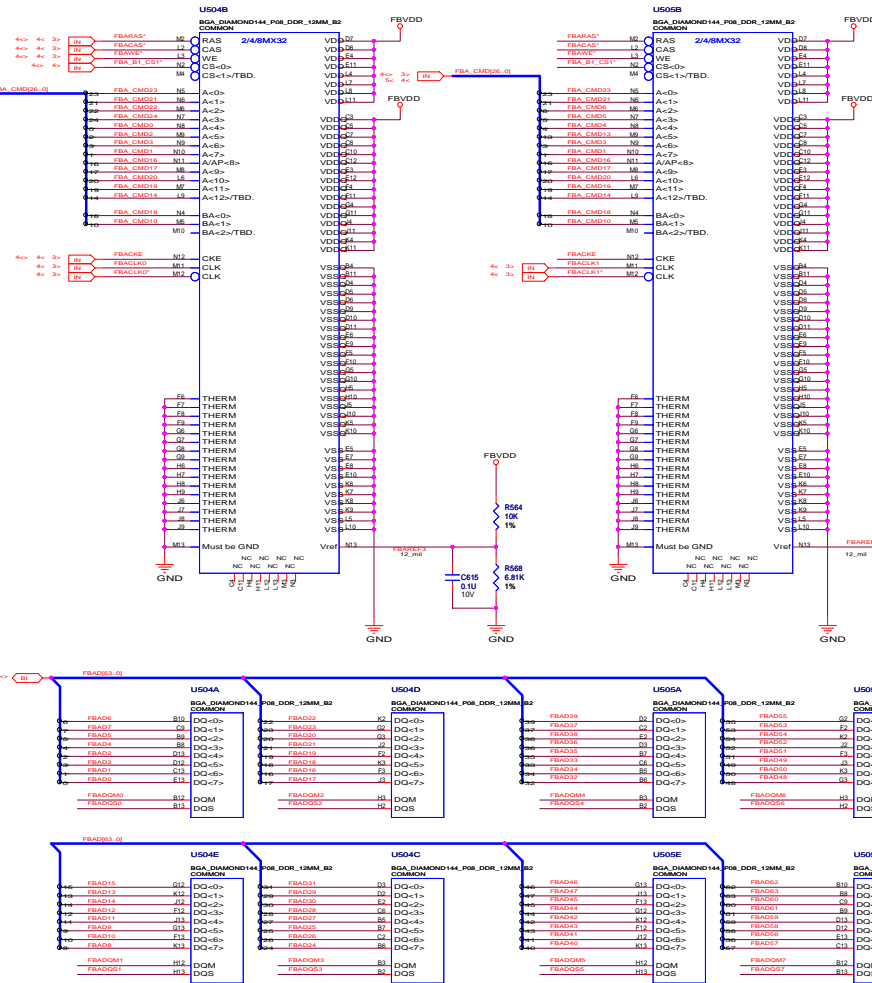
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MEMORY 128/256MB, 8Mx32DDR, PARTITION A, BANK 1

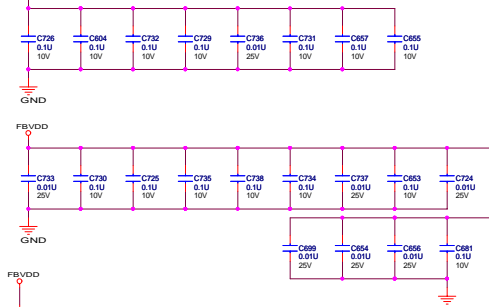
PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

need to hook up bank 1 signal



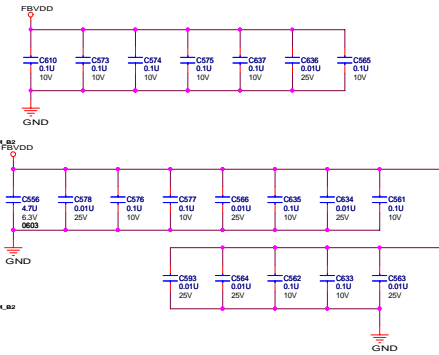
Decoupling for left MEMORY

Place around the MEM



Decoupling for right MEMORY

Place around the MEM

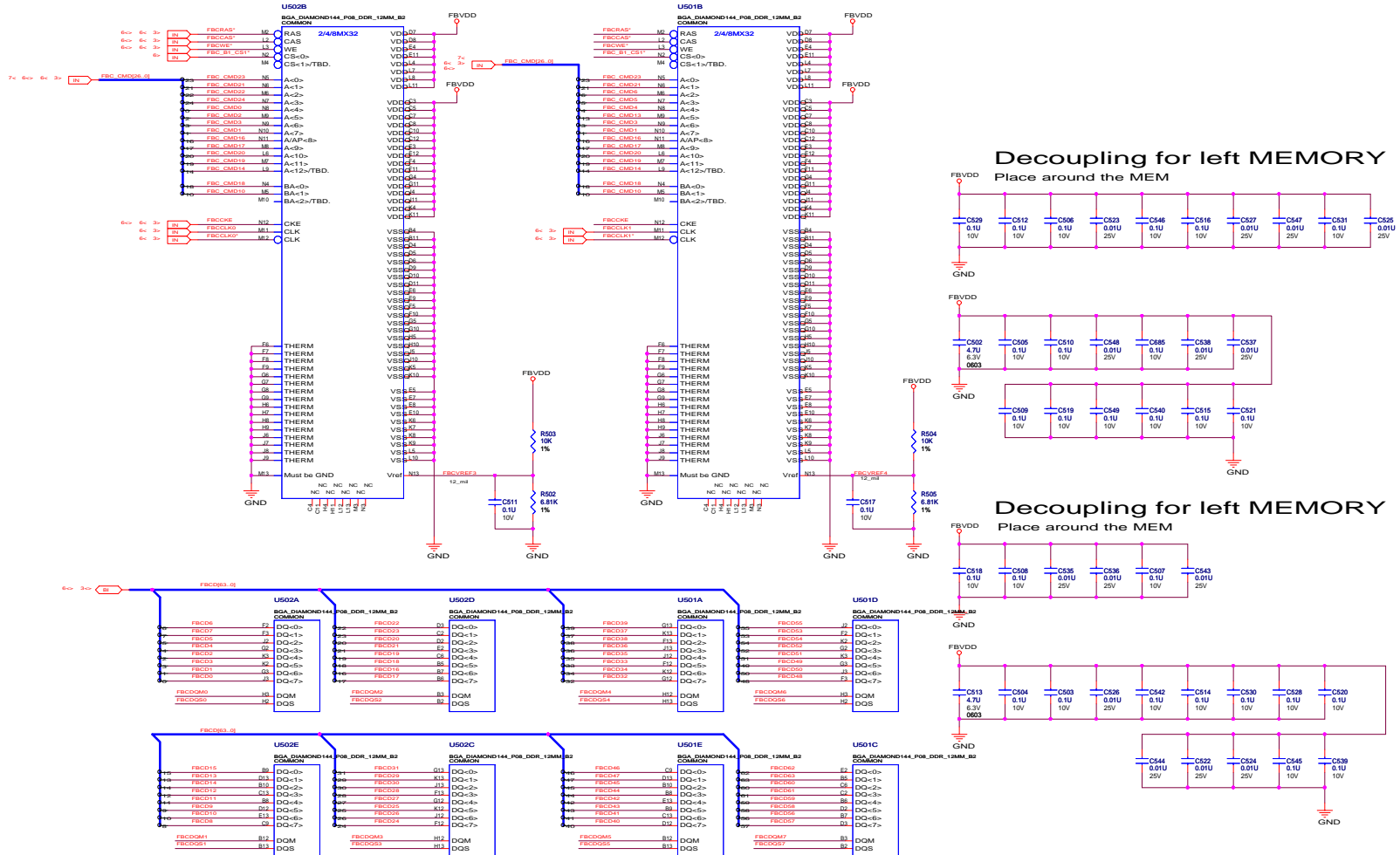


ASSEMBLY PAGE 2/21
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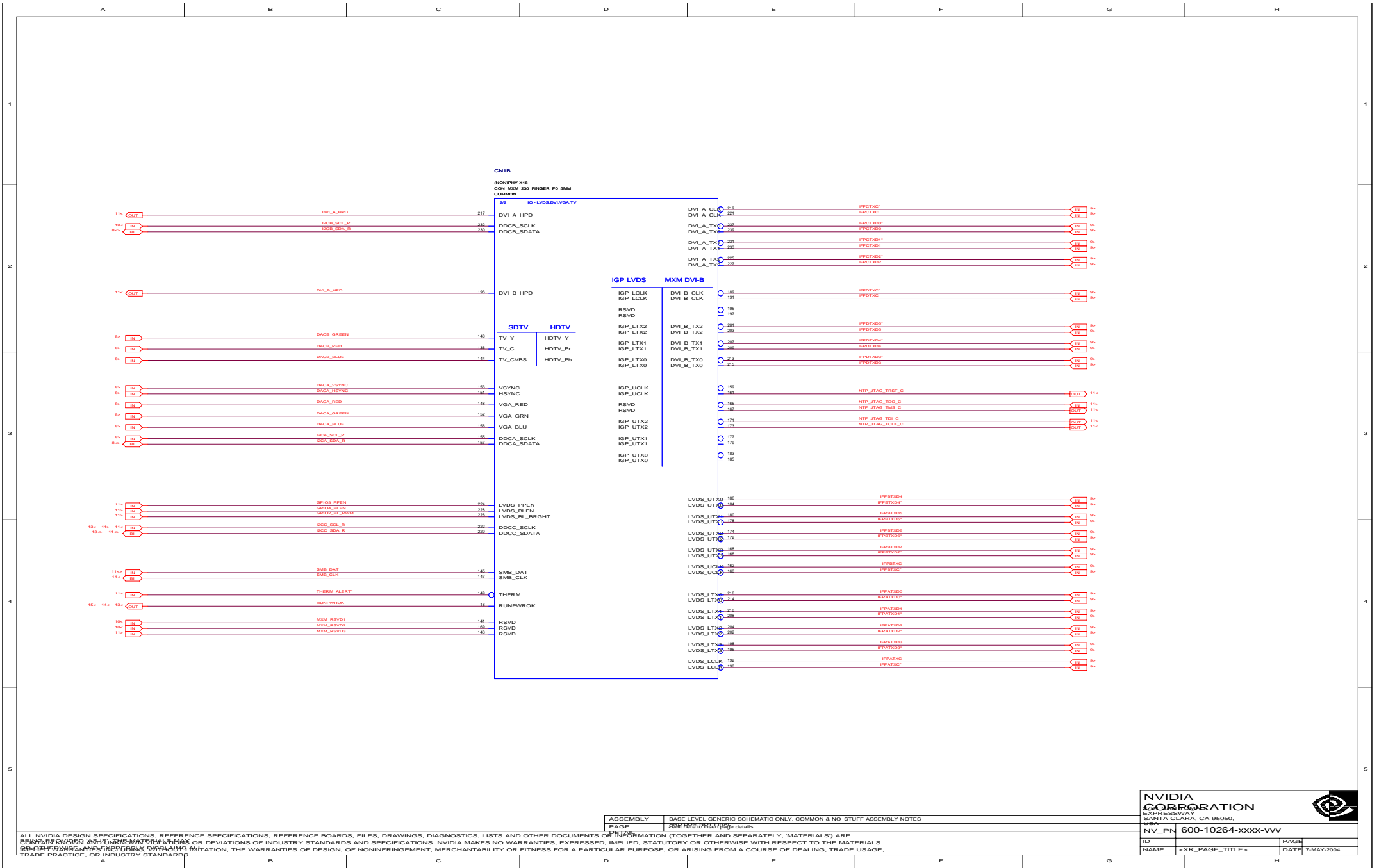
MEMORY 128/256MB, 8Mx32DDR, PARTITION C, BANK 1

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



Decoupling for left MEMORY
Place around the MEM

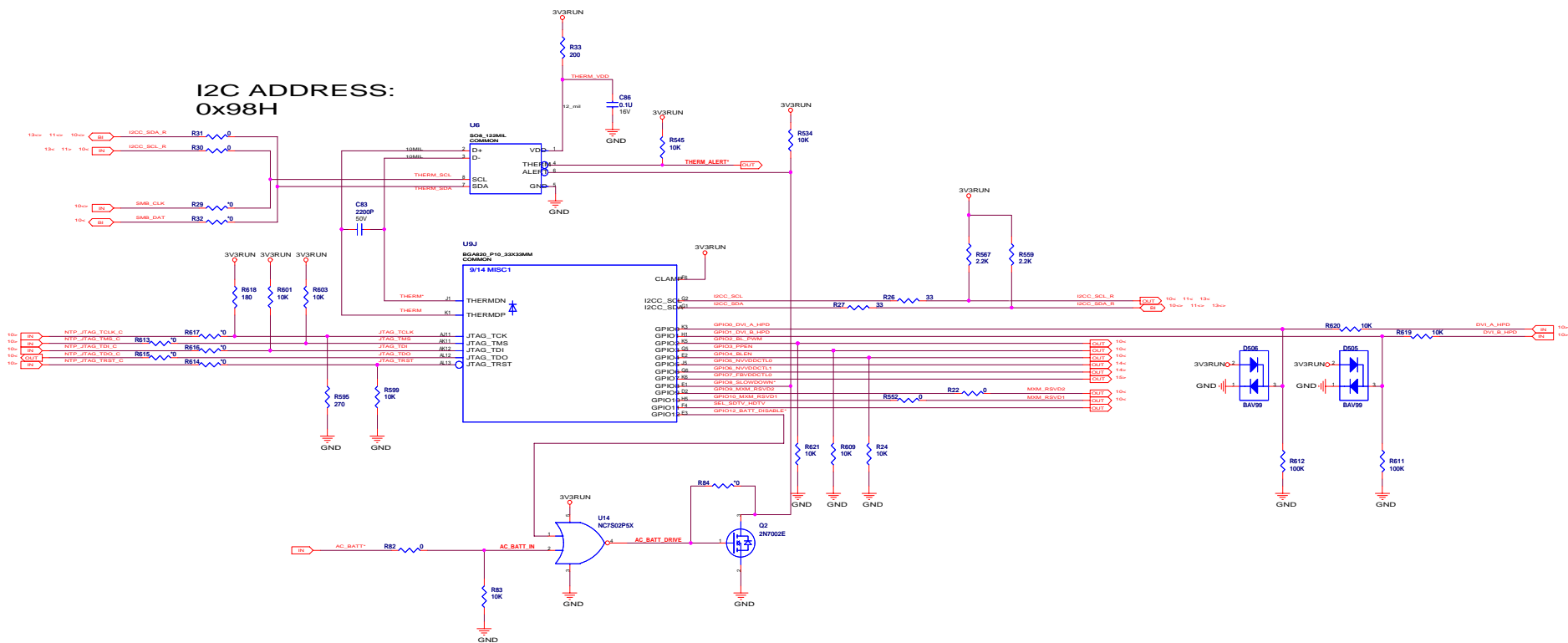
Decoupling for left MEMORY
Place around the MEM



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 PAGE: 2/21 (Total 21 pages)

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| ID | PAGE |
| NAME | DATE |
| <CON_PAGE_NUM> | 7-MAY-2004 |
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ASSEMBLY PAGE 1 OF 1

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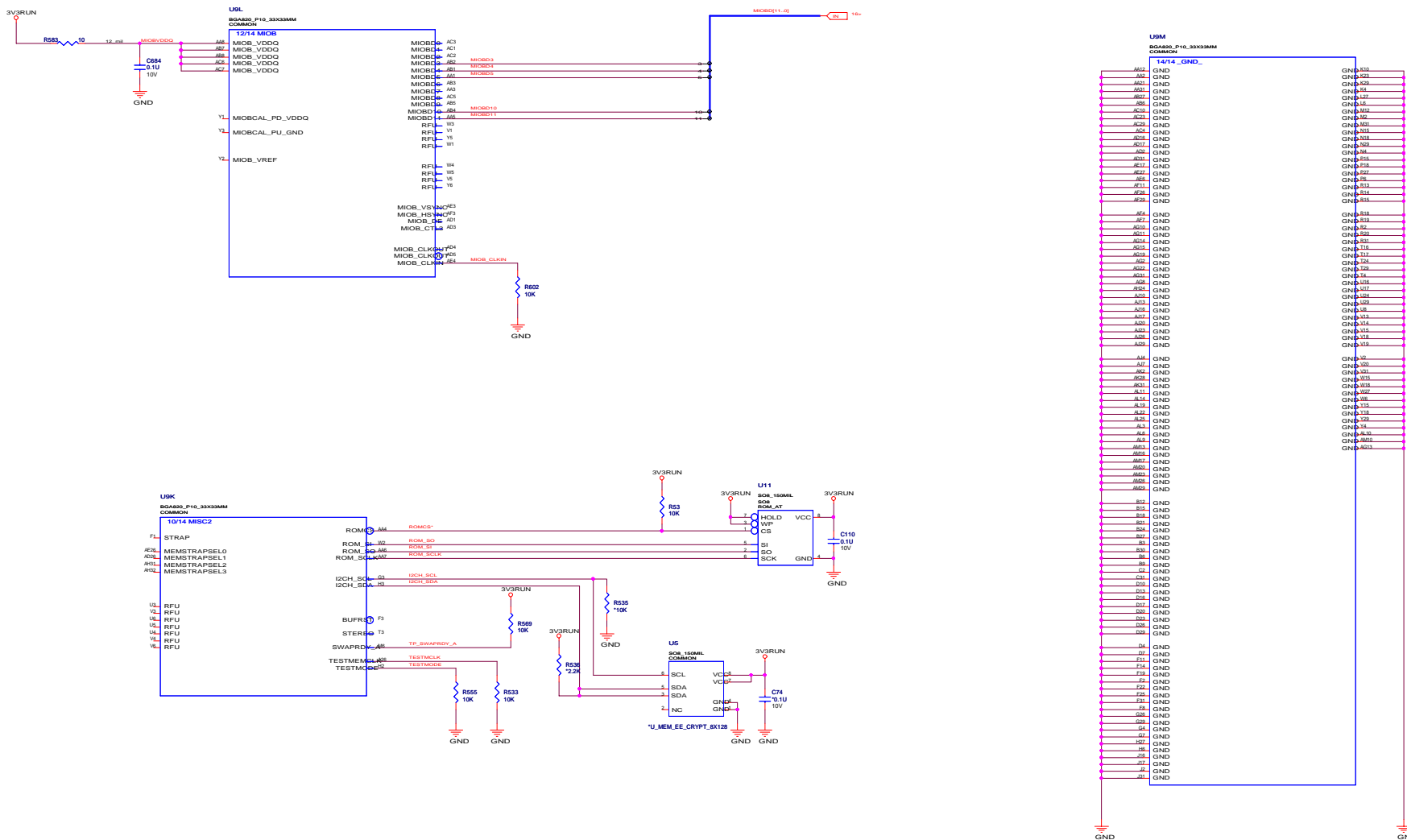
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DESCRIPTION

1 7-MAY-2004

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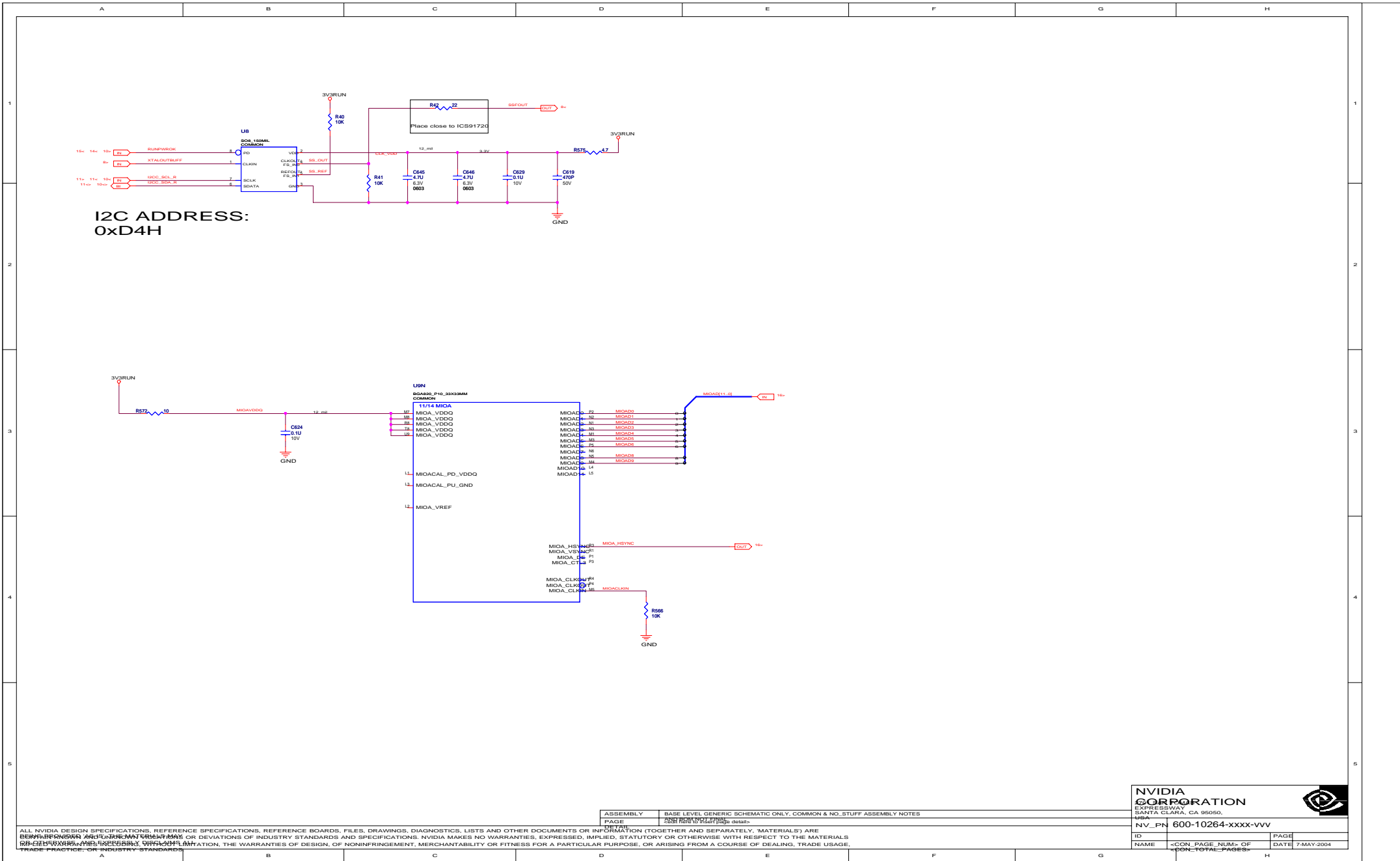
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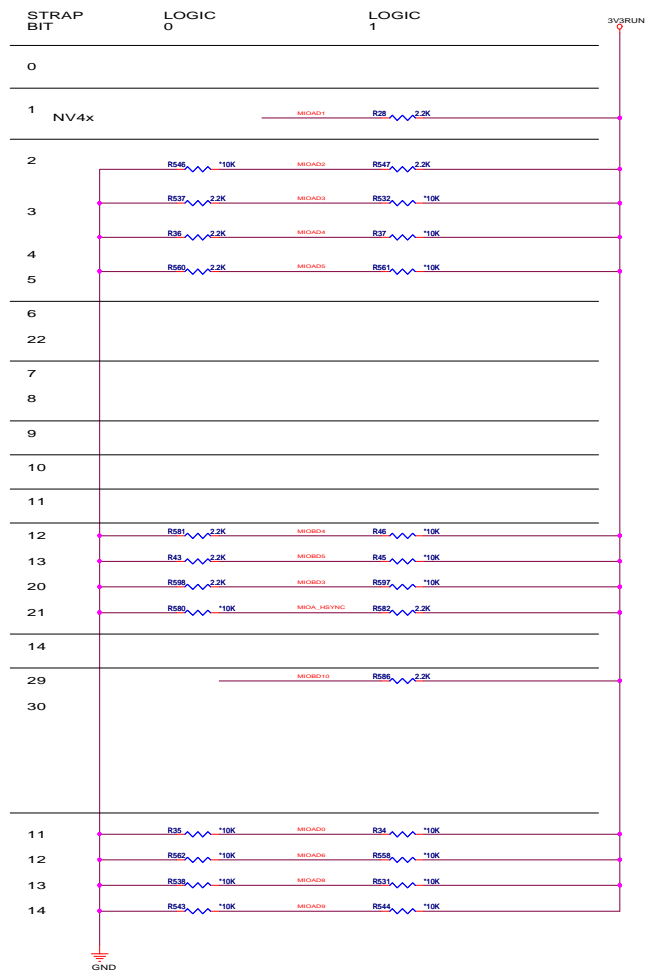
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12k OUT MIC0BD[11_0]

12k OUT MIC0AD[11_0]

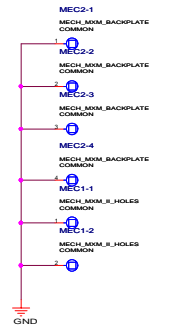


REG: NV_STRAP_0

| | | |
|---------------|--|---------|
| PCI_AD_SWAP | 0: REVERSED | |
| | 1: NORMAL | DEFAULT |
| SUB_VENDOR | 0: SYSTEM BIOS | |
| | 1: ADAPTER BIOS | DEFAULT |
| RAM_CFG_0 | RAM_CFG[3:0] | |
| | MS_0001: 8Mx32 DDR SDRAM, DQS PER 8 BITS, Monolithic | |
| | MS_0011: 8Mx32 DDR SDRAM, DQS PER 8 BITS, Stacked | |
| | MS_0110: 4Mx32 DDR SDRAM, DQS PER 8 BITS, Monolithic | |
| RAM_CFG_1 | | |
| RAM_CFG_2 | | |
| RAM_CFG_3 | | |
| CRYSTAL_0 | MS_00: 13.5MHz | |
| | MS_01: 14.318MHz | |
| | MS_10: 27MHz | DEFAULT |
| | MS_11: RESERVED | |
| TV_MODE_0 | MS_00: SECAM | |
| | MS_01: NTSC | DEFAULT |
| | MS_10: PAL | |
| | MS_11: VGA | |
| AGPBx/4x | 0: 8x | DEFAULT |
| | 1: 4x | |
| AGP_SIDEBAND | 0: ENABLE | DEFAULT |
| | 1: DISABLE | |
| AGP_FASTWRITE | 0: ENABLE | DEFAULT |
| | 1: DISABLE | |
| PCI_DEVID_0 | MS_0100: NV34M | |
| | MS_0110: NV18M | |
| | MS_0111: NV18MPRO | DEFAULT |
| | MS_1010: NV31M | |
| | MS_1011: NV31MPRO | |
| | MS_1100: NV31GLM | |
| | MS_1101: NV33M | |
| | MS_1110: NV31GLMPRO | |
| BUS_TYPE | 0: PCI | DEFAULT |
| | 1: AGP | |
| ROM_TYPE_0 | MS_00: PARALLEL | |
| | MS_01: SERIAL AT25F | |
| | MS_10: SERIAL SST45VF | DEFAULT |
| | MS_11: RESERVED | |

REG: NV_STRAP_1

| | |
|------------------------|--|
| PEX_PLL_EN_TERM100 | |
| 3GIO_PADCFG_LUT_ADR[0] | |
| 3GIO_PADCFG_LUT_ADR[1] | |
| 3GIO_PADCFG_LUT_ADR[2] | |



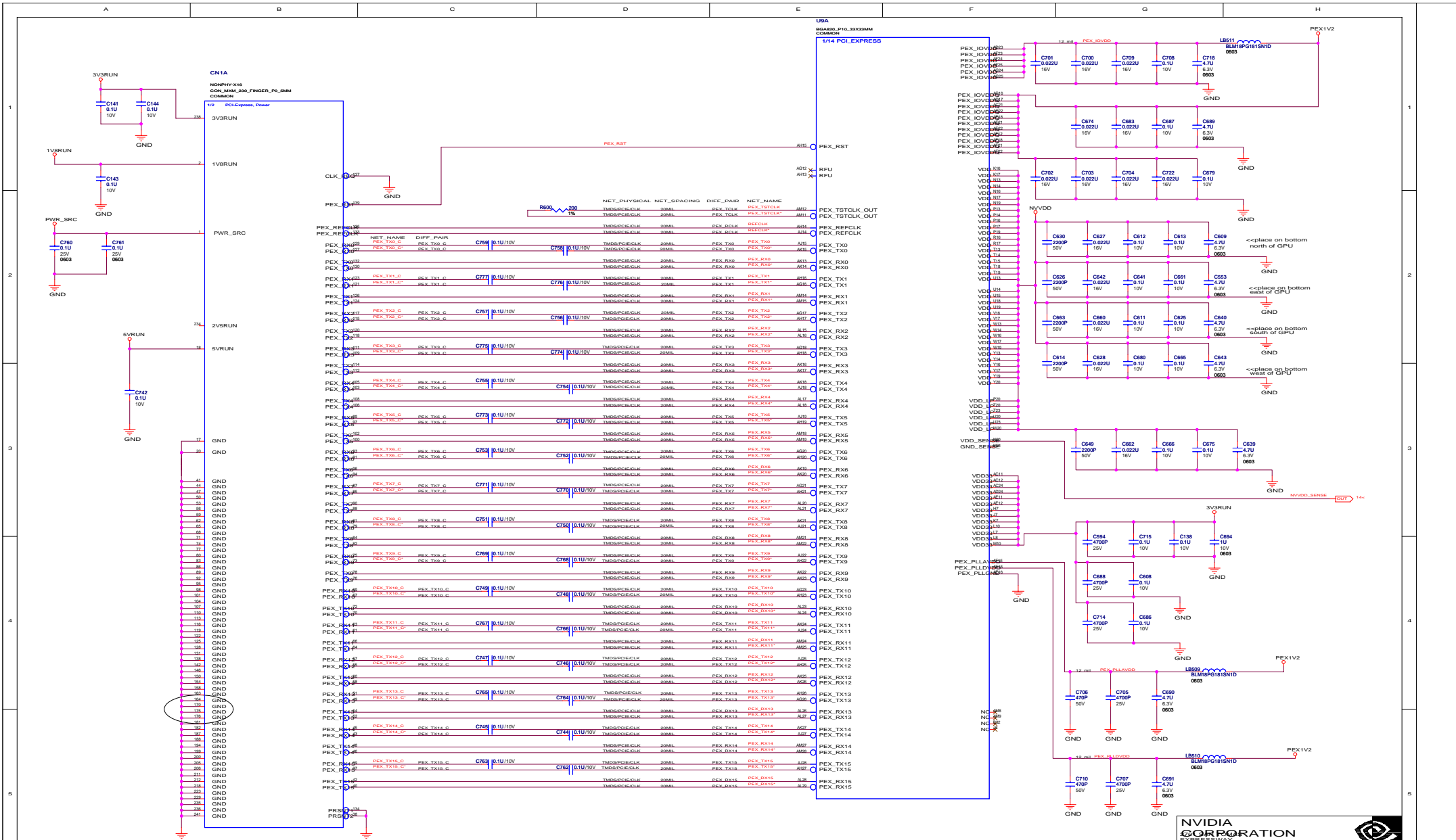
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| NAME | DATE |
| <CON_PAGE_NUM> OF | 7-MAY-2004 |
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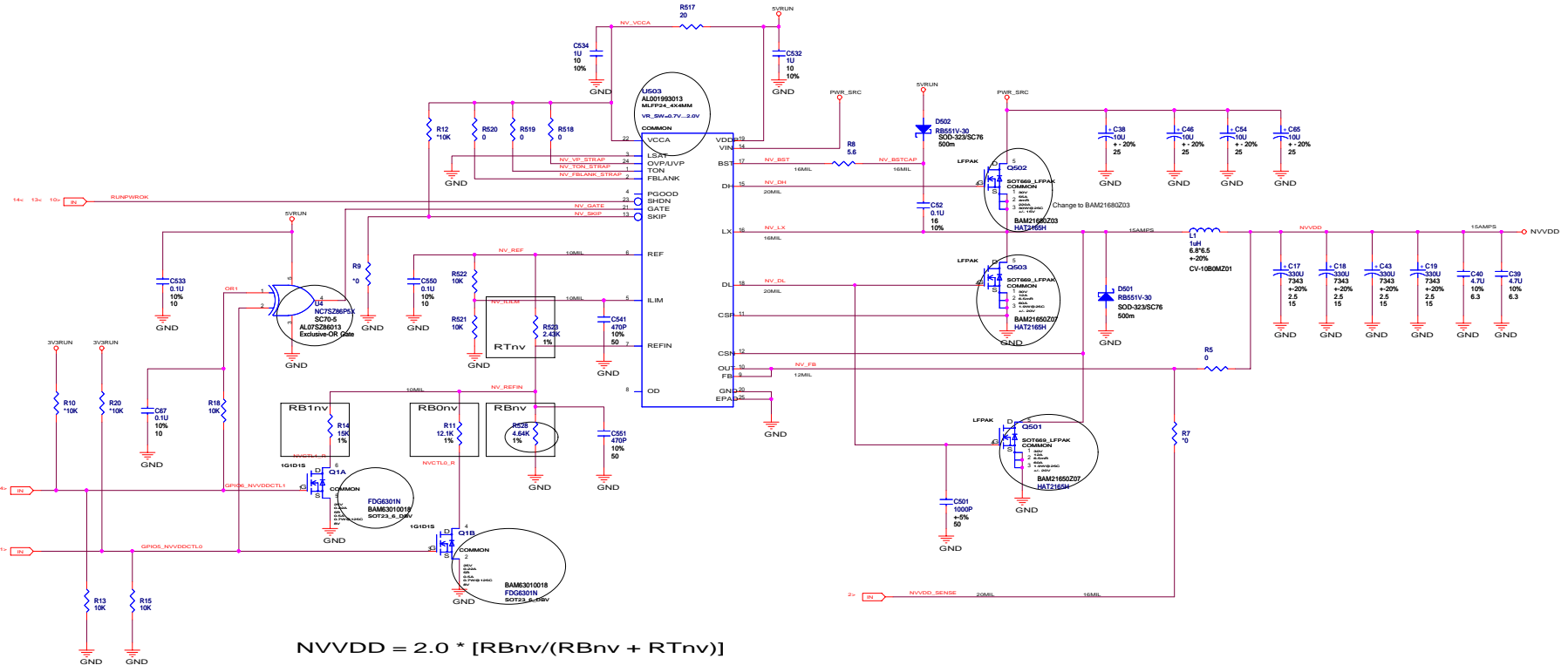
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| PAGE | 2/28 |



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| NET | MIN_LINE_WIDTH | VOLTAGE |
|---------|----------------|---------|
| SVRLUN | 10MIL | 5V |
| SV3RLUN | 10MIL | 3.3V |
| FBVDD | 12MIL | 2.5V |
| FBVDDG | 12MIL | 2.5V |
| NV_VDD | 12MIL | 1.2V |
| PWR_SRC | 18MIL | 22V |



$$NV_VDD = 2.0 * [RBnv / (RBnv + RTnv)]$$

| NV_VDD | RTnv | RBnv | GPIO0 | GPIO1 |
|--------|-------|-----------------|-------|-------|
| 1.02V | 3.09K | 4.75K(15.4K)28K | High | High |
| 1.08V | 3.09K | 4.75K(15.4K) | High | Low |
| 1.13V | 3.09K | 4.75K(28K) | Low | High |
| 1.21V | 3.09K | 4.75K | Low | Low |

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