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23	LVDS	SA	65	SYS Power(+1 8V)	SA
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Project Code & Schematics Subject: M960&M970 L Model

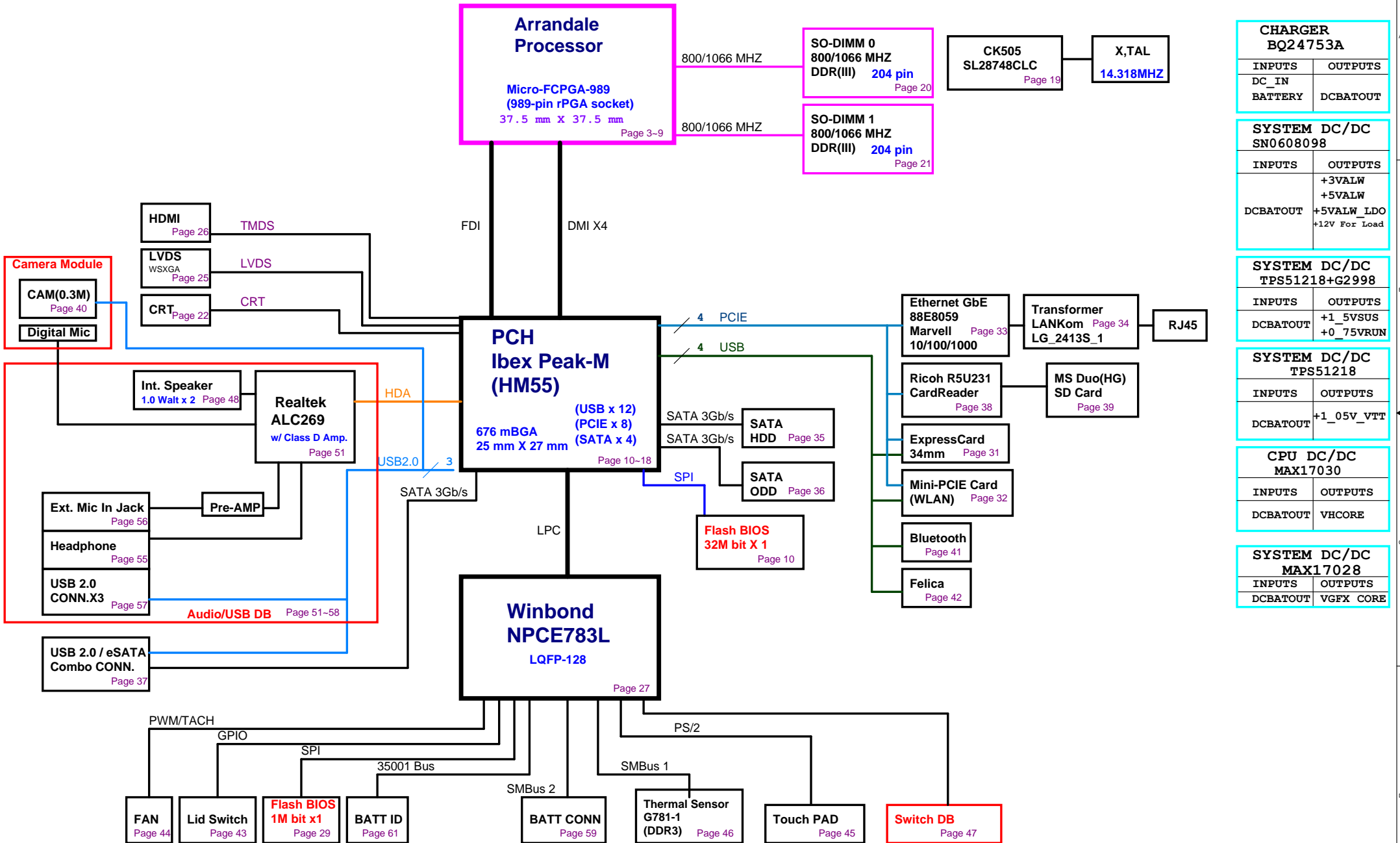
PCB P/N:

- 1P-0099J00-60SB (IRIS MB)
- 1P-1099J00-60SB (IRIS AUDIO)
- 1P-1099J01-60SB (IRIS PWR)
- 1P-0099500-60SB (HANNSTAR MB)
- 1P-1099500-60SB (HANNSTAR Audio)
- 1P-1099501-60SB (HANNSTAR PWR)

P. Leader	Check by	Design by

FOXCONN			HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title Index Page			
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M960&M970 L Model Calpella Platform UMA Graphic



CHARGER
BQ24753A

INPUTS	OUTPUTS
DC_IN	DCBATOUT
BATTERY	

SYSTEM DC/DC
SN0608098

INPUTS	OUTPUTS
DCBATOUT	+3VALW
	+5VALW
	+5VALW_LDO
	+12V For Load

SYSTEM DC/DC
TPS51218+G2998

INPUTS	OUTPUTS
DCBATOUT	+1_5VSUS
	+0_75VRUN

SYSTEM DC/DC
TPS51218

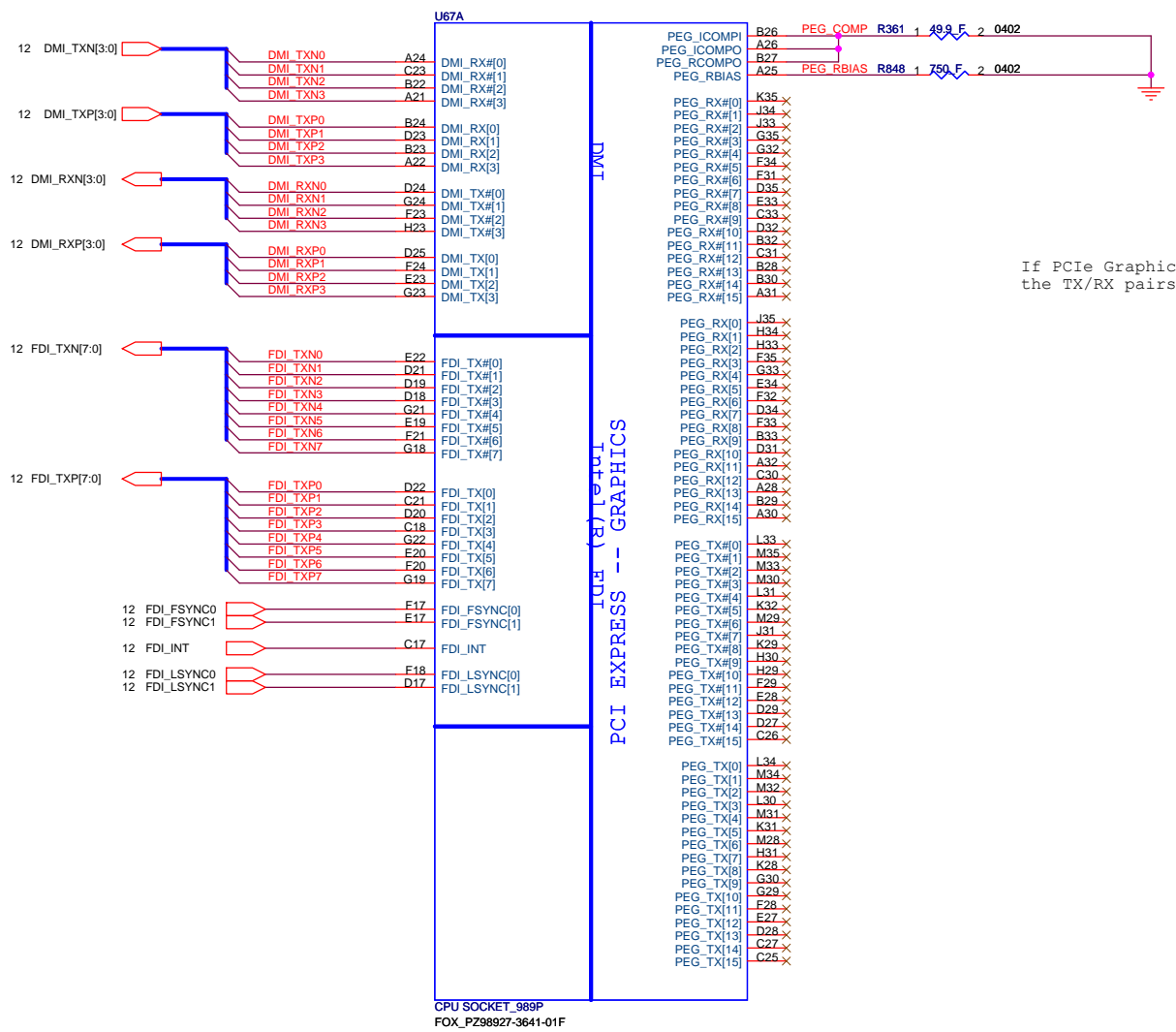
INPUTS	OUTPUTS
DCBATOUT	+1_05V_VTT

CPU DC/DC
MAX17030

INPUTS	OUTPUTS
DCBATOUT	VH CORE

SYSTEM DC/DC
MAX17028

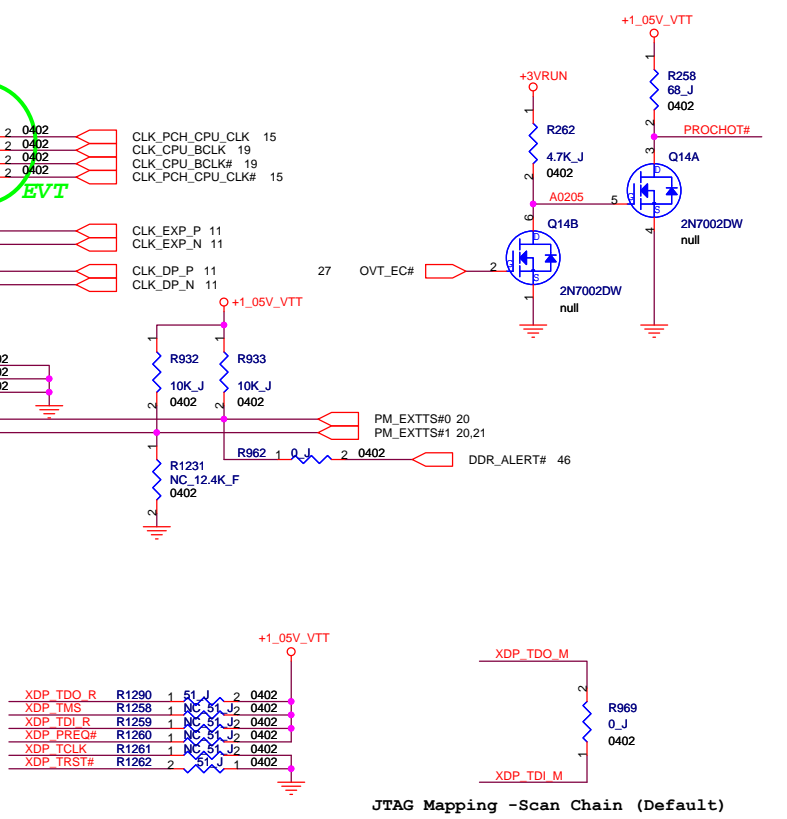
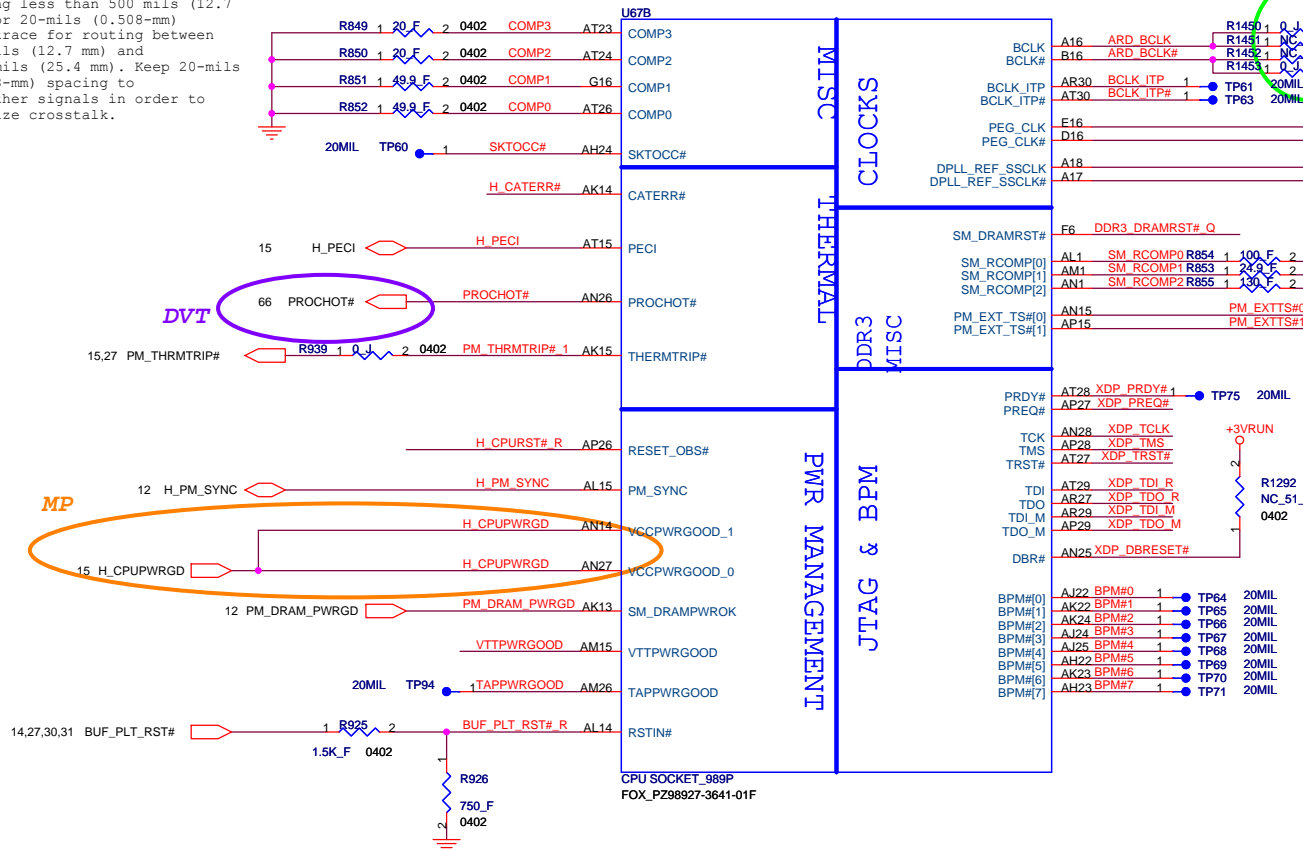
INPUTS	OUTPUTS
DCBATOUT	VGFX CORE



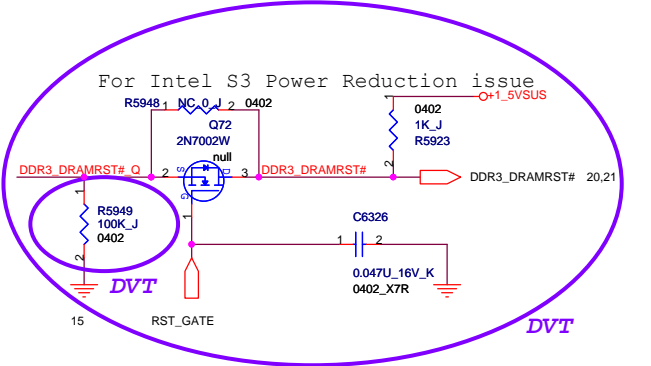
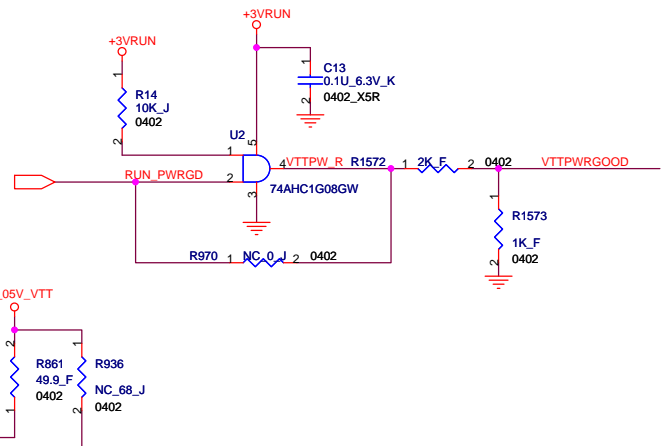
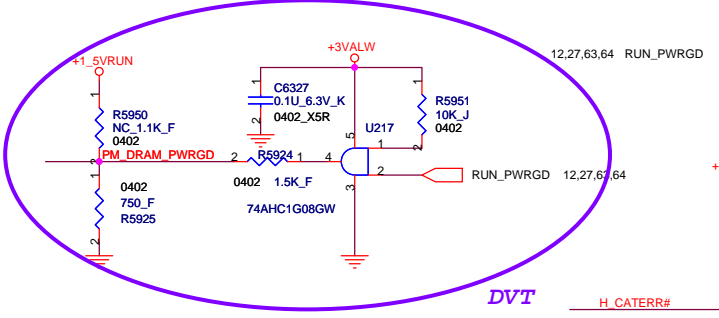
If PCIe Graphics is not implemented,
the TX/RX pairs can be left as No Connect.

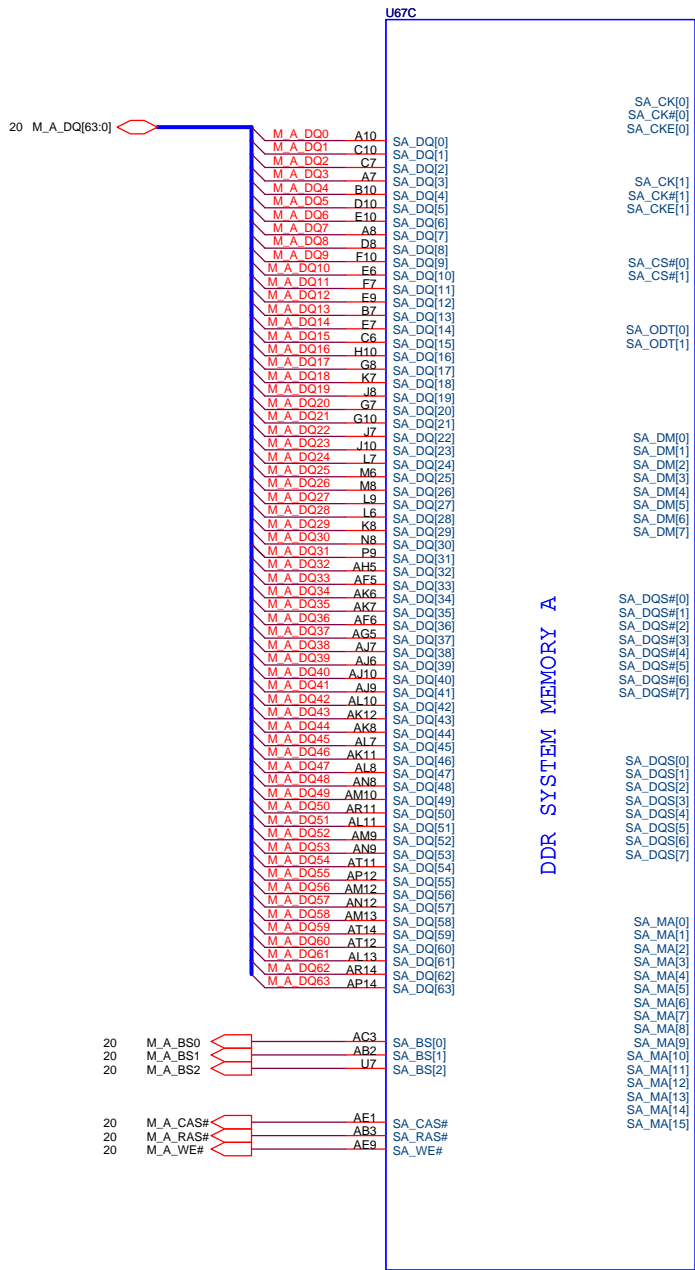
CPU SOCKET_989P
FOX_PZ98927-3641-01F

Layout Note:
 Comp0,1 connect with Zo=49.9 ohm,
 Comp2,3 connect with Zo=20 ohm,
 In order to minimize resistance,
 use thick traces to route all
 COMP signals, use 10-mils
 (0.254-mm) wide trace for
 routing less than 500 mils (12.7
 mm), or 20-mils (0.508-mm)
 wide trace for routing between
 500 mils (12.7 mm) and
 1000 mils (25.4 mm). Keep 20-mils
 (0.508-mm) spacing to
 any other signals in order to
 minimize crosstalk.



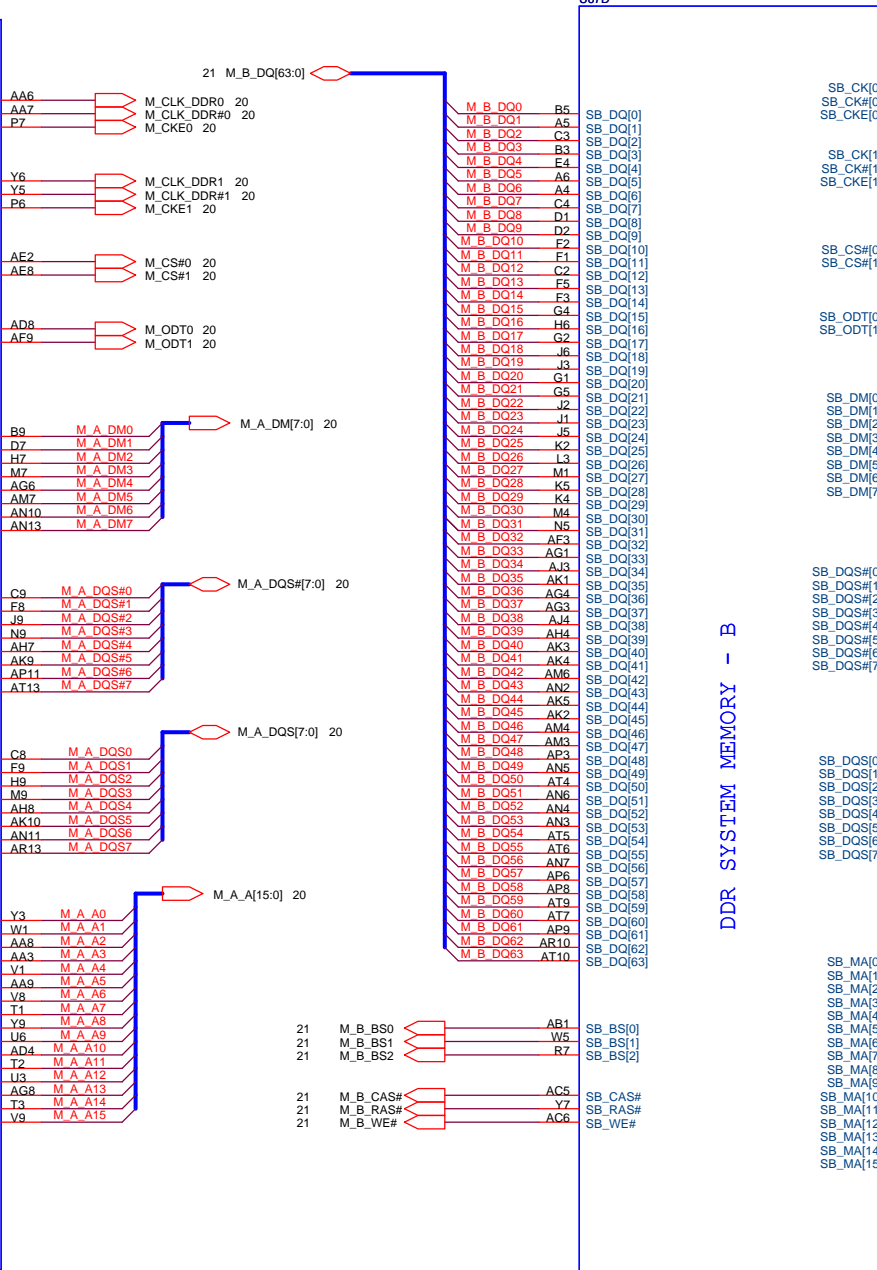
For Intel S3 Power Reduction issue





DDR SYSTEM MEMORY A

CPU SOCKET_989P
FOX_PZ98927-3641-01F



DDR SYSTEM MEMORY - B

CPU SOCKET_989P
FOX_PZ98927-3641-01F

FOXCONN HON HAI Precision Ind. Co., Ltd.
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Title: **ARD (DDR3)**

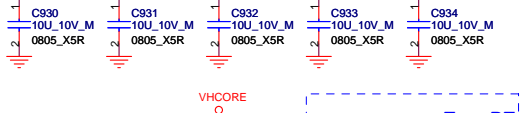
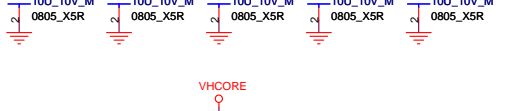
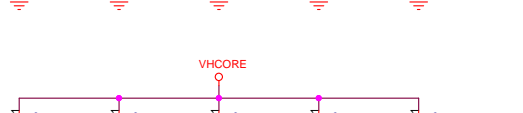
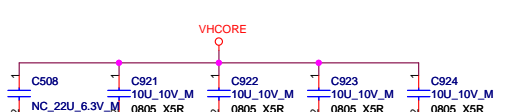
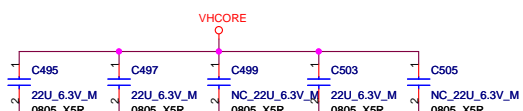
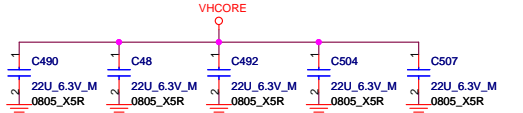
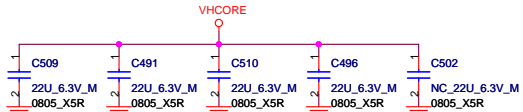
Size: A3
Document Number: **M960&M970 L Model**

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48A (SV)



For RE Noise

- VHOCORE
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AC25 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

1.1V RAIL POWER

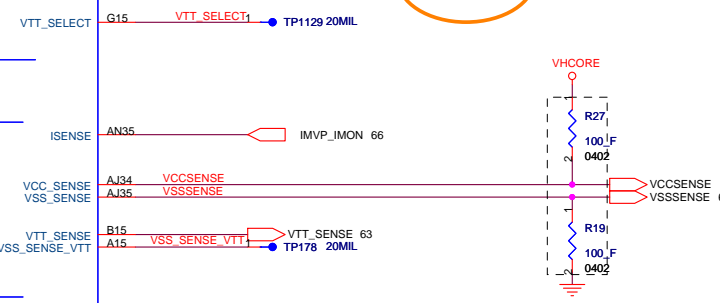
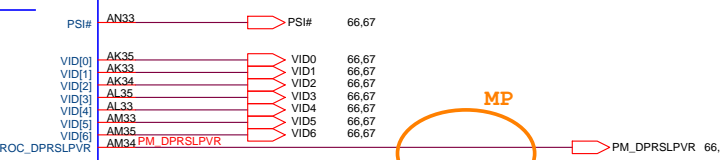
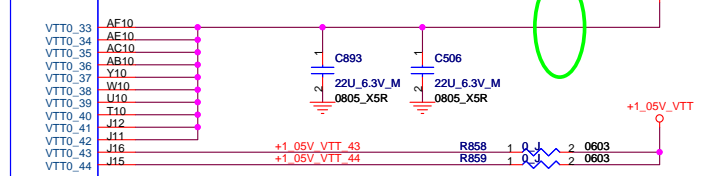
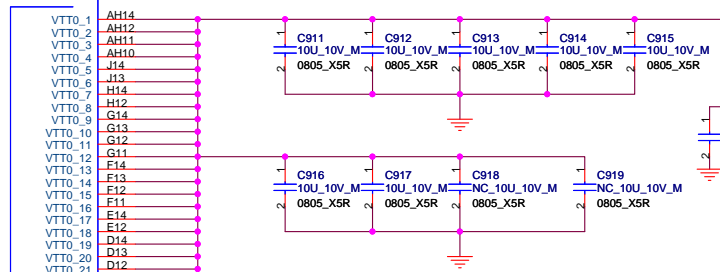
CPU CORE SUPPLY

CPU VIDS

SENSE LINES

CPU SOCKET_989P
FOX_P298927-3641-01F

18A (SV) (VTT)



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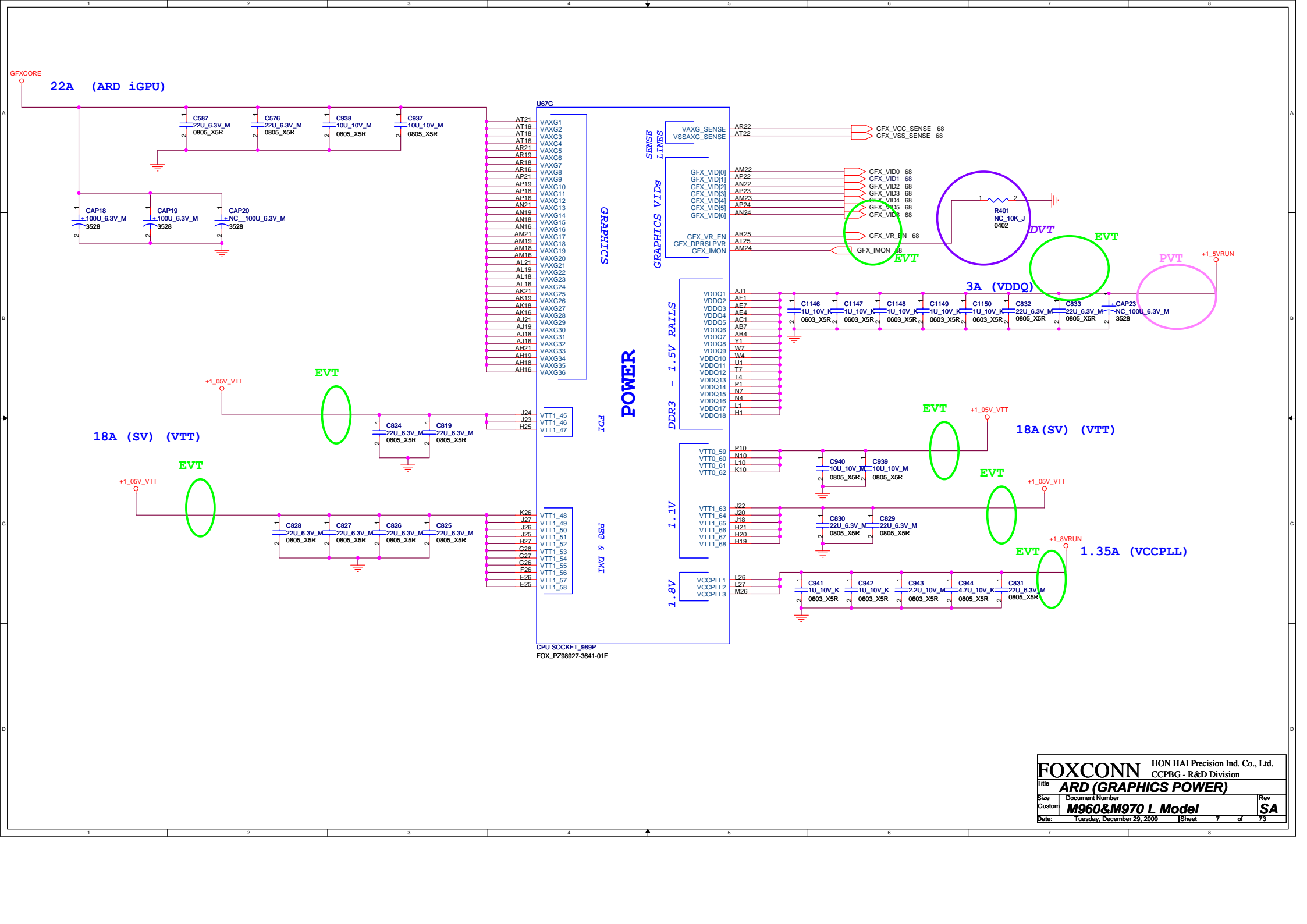
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Size: Document Number

Custom: **M960&M970 L Model**

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22A (ARD iGPU)

18A (SV) (VTT)

3A (VDDQ)

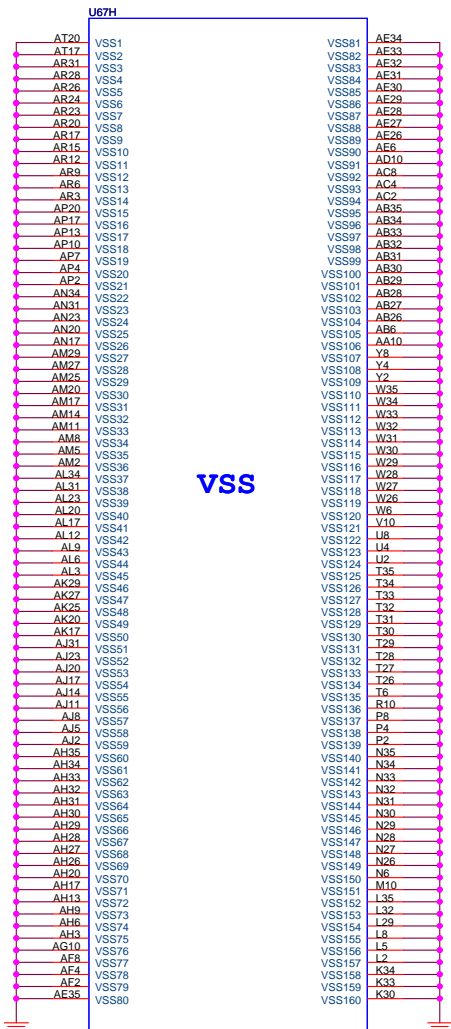
18A (SV) (VTT)

1.35A (VCCPLL)

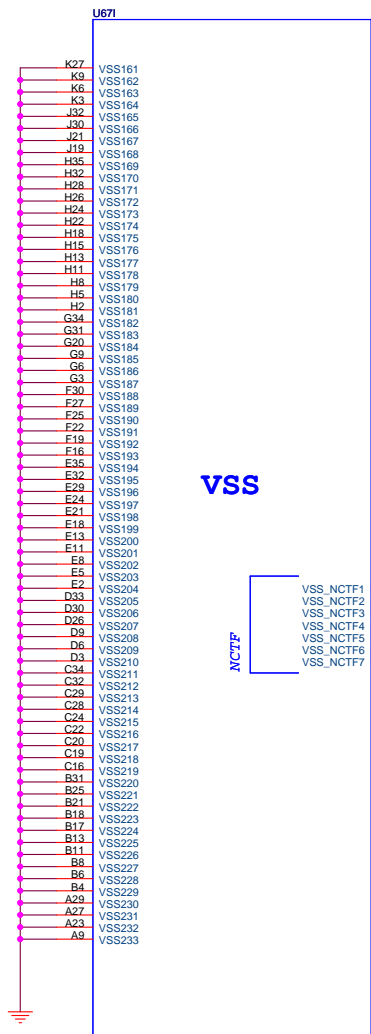
U67G

GPU SOCKET_089P
FOX_P298927-3641-01F

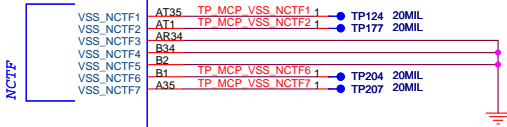
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title ARD (GRAPHICS POWER)			
Size	Document Number		Rev
Custom	M960&M970 L Model		SA
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CPU SOCKET_989P
FOX_PZ98927-3641-01F

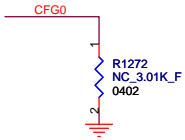


CPU SOCKET_989P
FOX_PZ98927-3641-01F

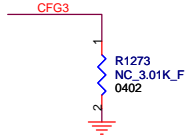


PCI Express Configuration Select
 CFG0 1 : Single PEG
 0 : Bifurcation enable

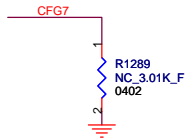
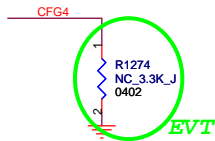
3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
 The Clarksfield EDS V011 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.



CFG3 PCI Express Static Lane Reversal
 CFG3 1 : Normal Operation
 0 : Lane Numbers Reversed
 15 -> 0 , 14 -> 1 , ...

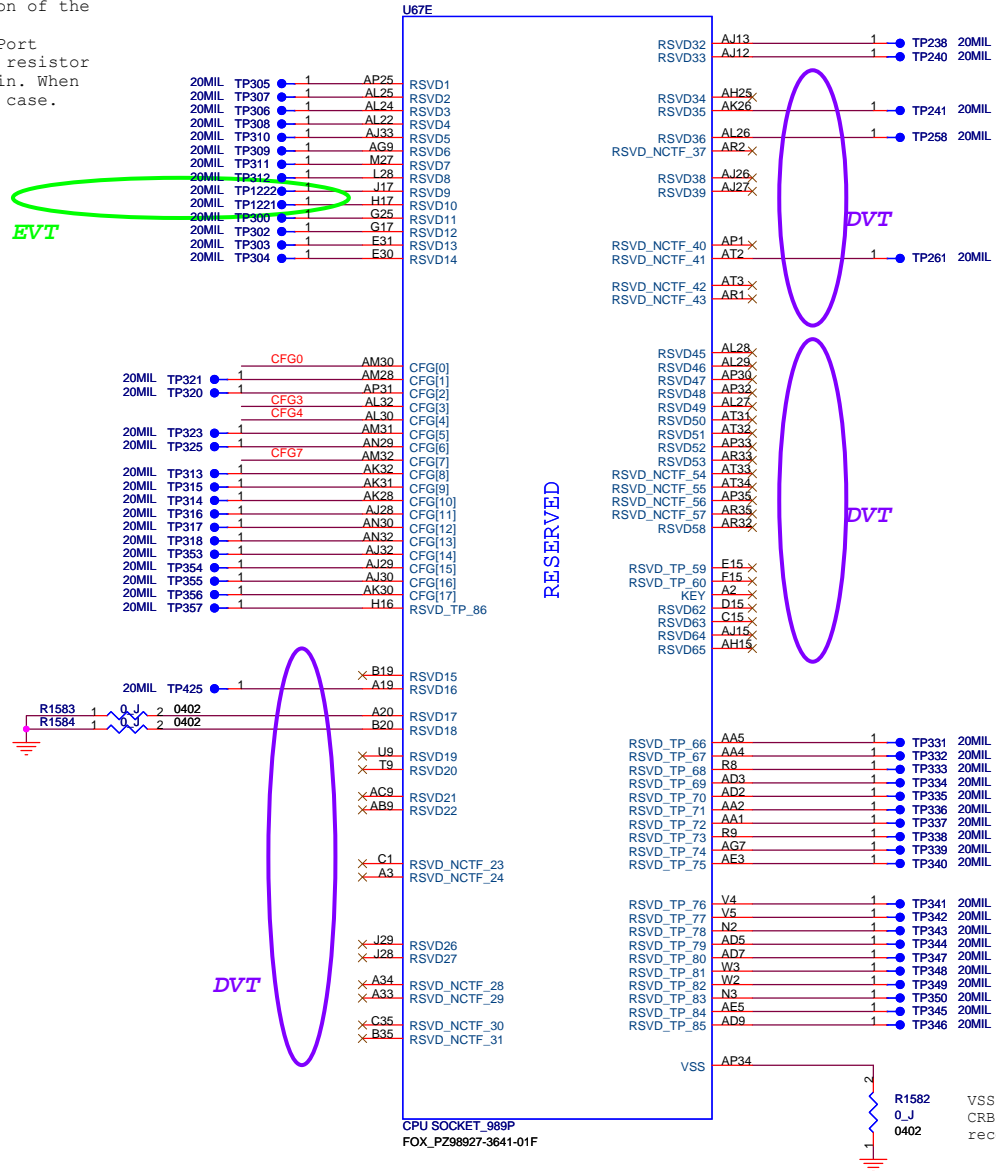


CFG4 Display Port Presence
 CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
 0 : Enable ; An external Display Port device is connected to the Embedded Display Port

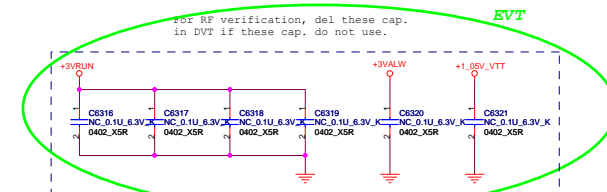
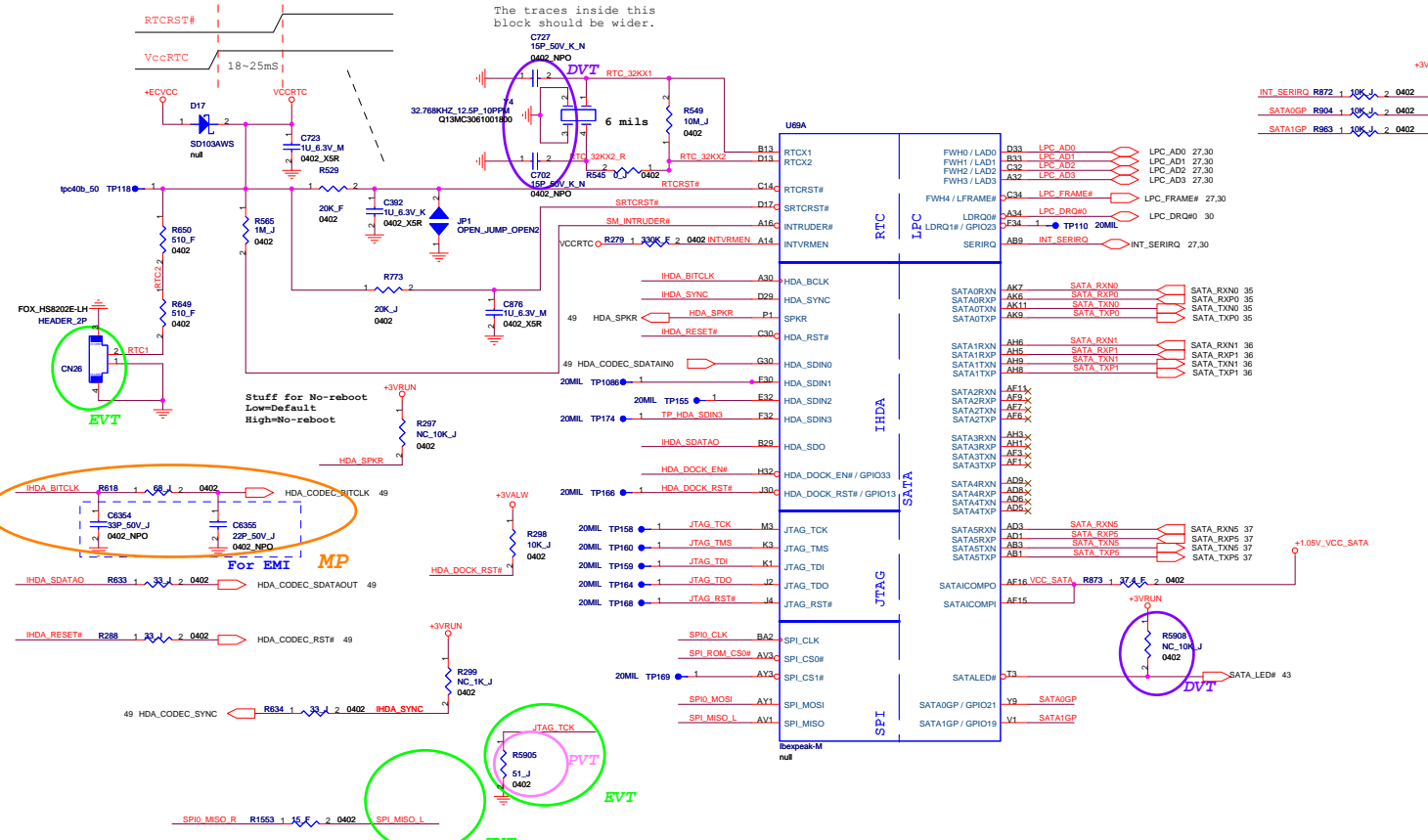


2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

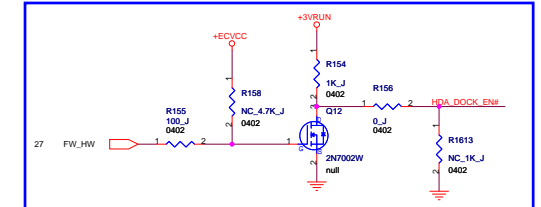
Intel has determined that the workaround (3.01k pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



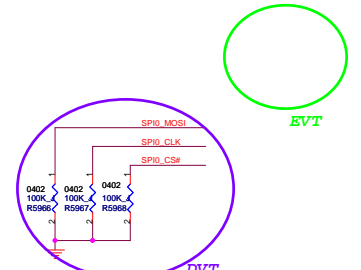
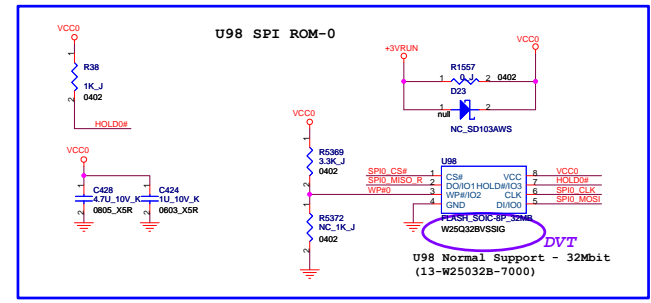
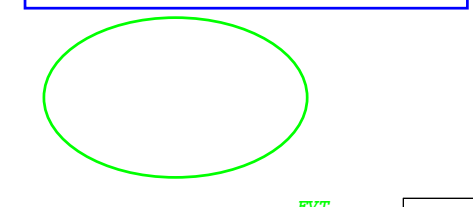
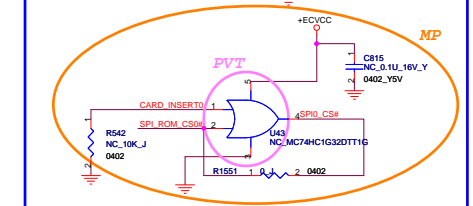
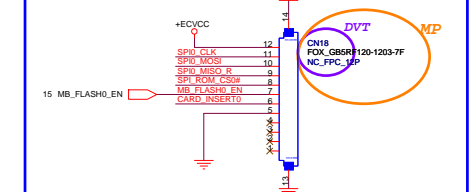
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND



[HDA_DOCK_EN#/GPIO33]
Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) - Security measure defined in the Flash Descriptor will be enabled

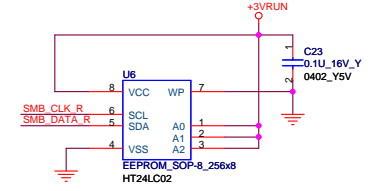
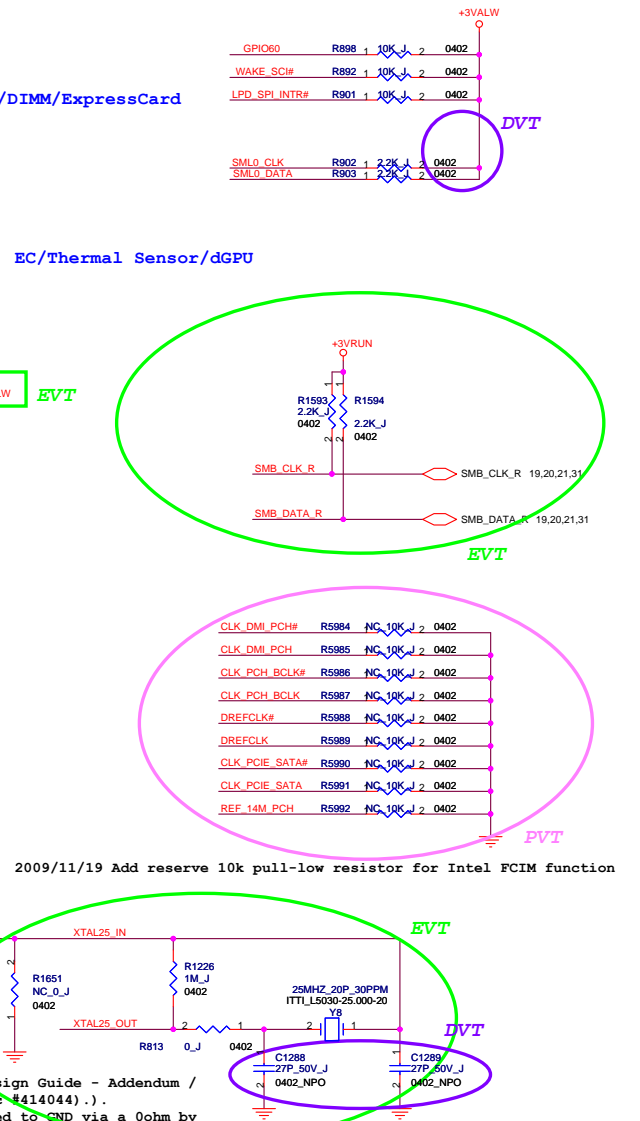
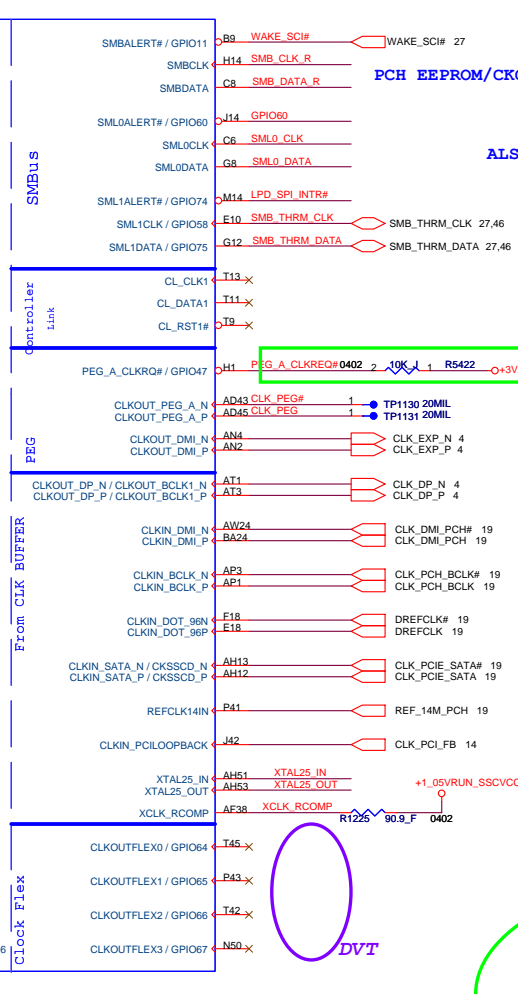
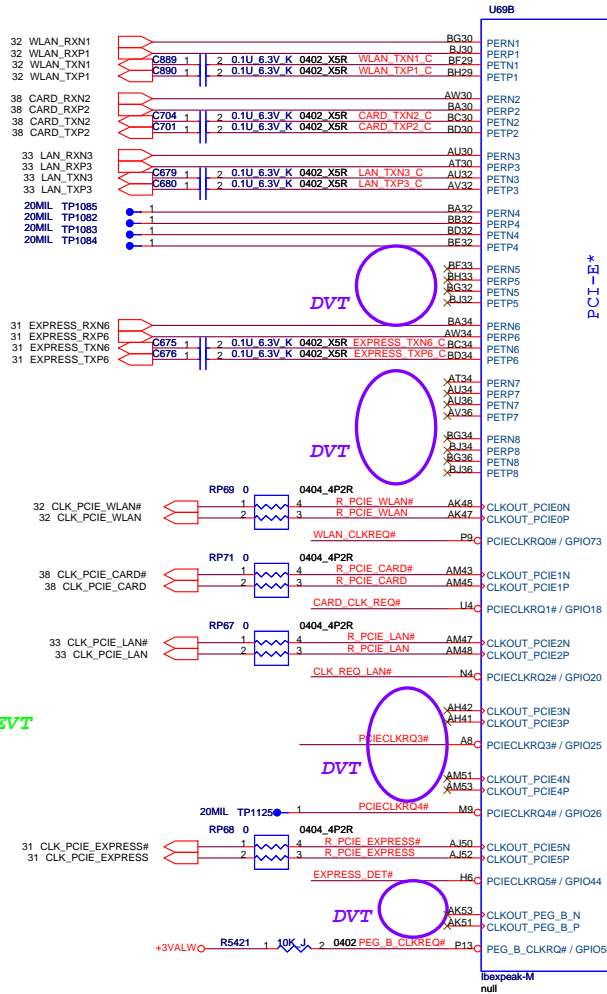
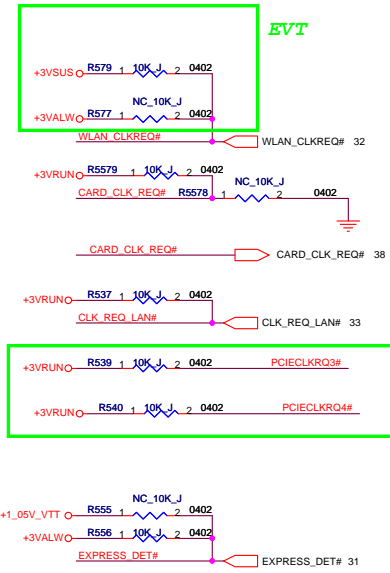


EXTERNAL SPI0 ROM INTERFACE (FOR U98)



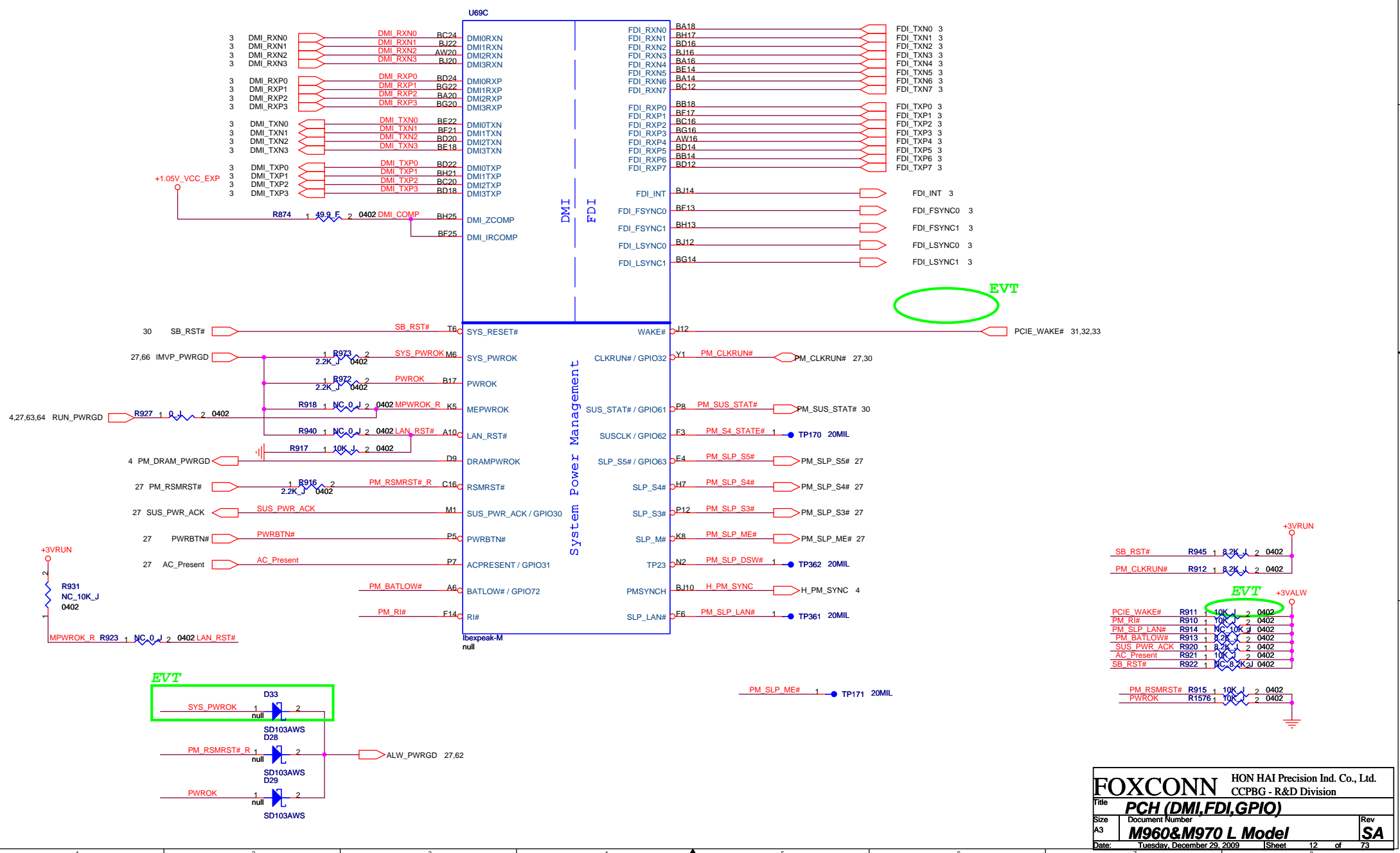
PCI-E Port Table

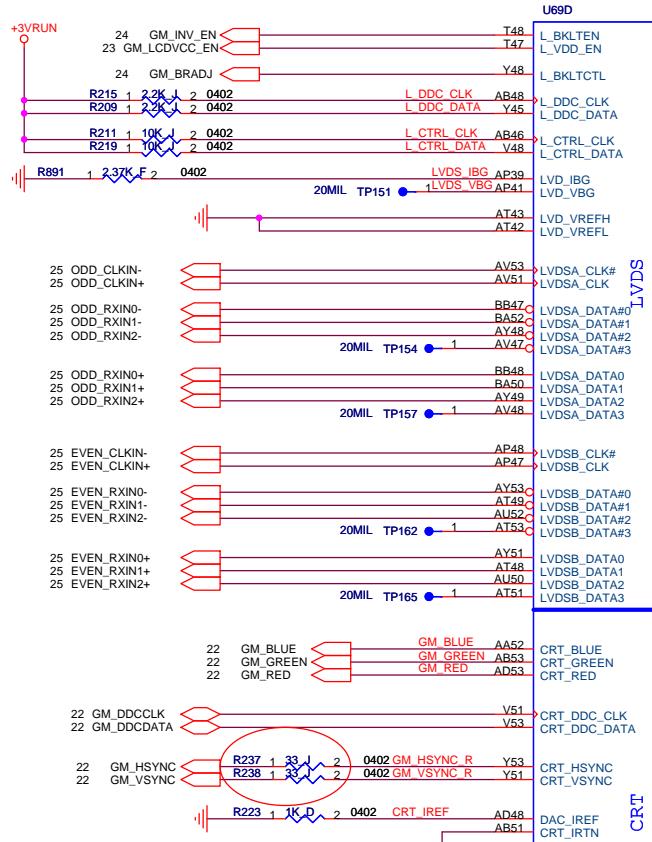
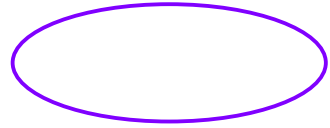
Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCI-E)
Port7	NC
Port8	NC



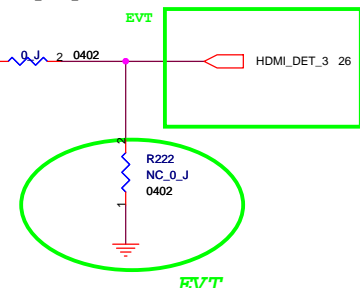
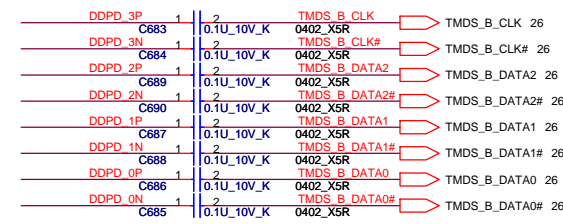
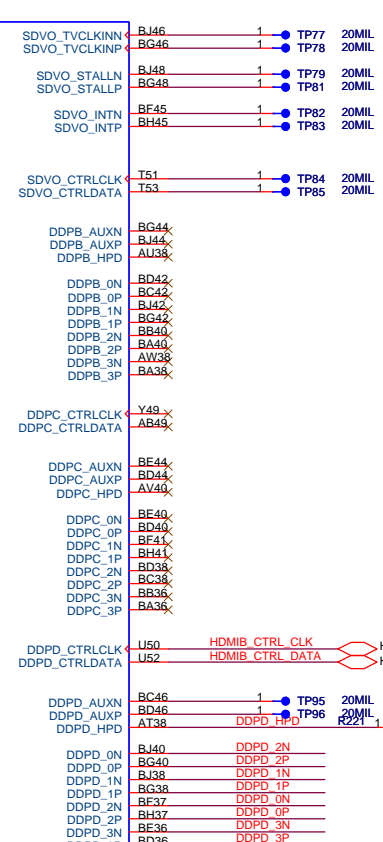
Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044).
 XTAL_IN should be pulled to GND via a 0ohm by default.
 This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

For Disable Arrandale Graphic
 In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
 FDI_TX_[7:0] and FDI_TX#_[7:0] can be left floating on the Arrandale. The
 GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
 signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



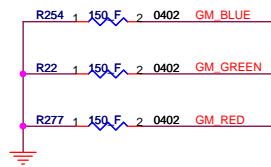


Digital Display Interface

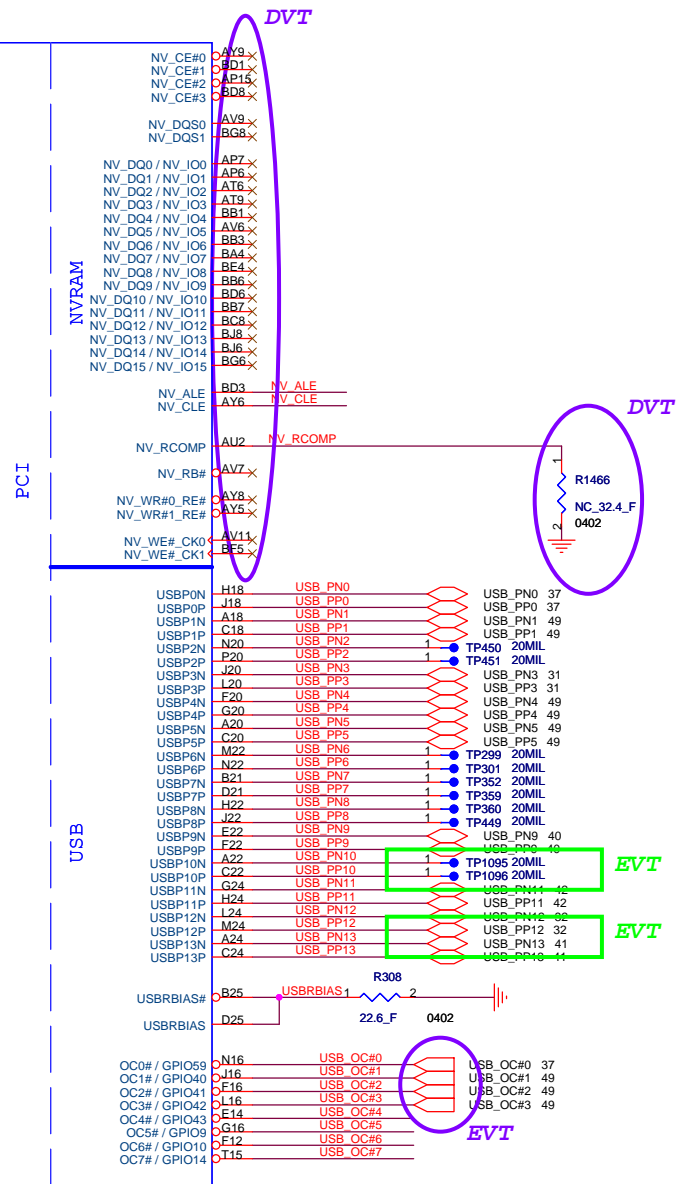
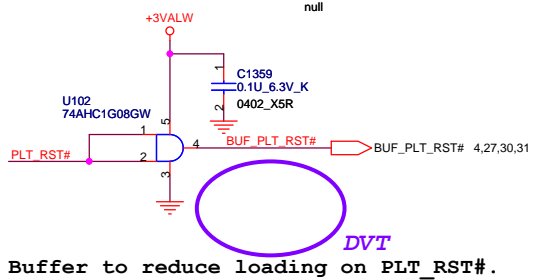
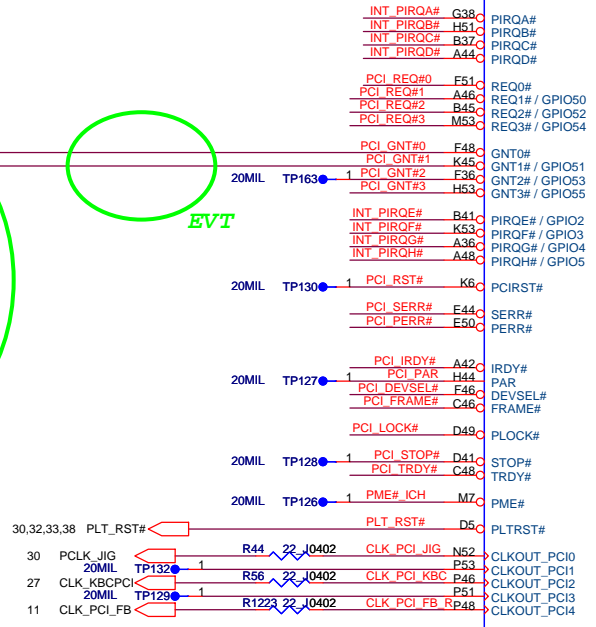
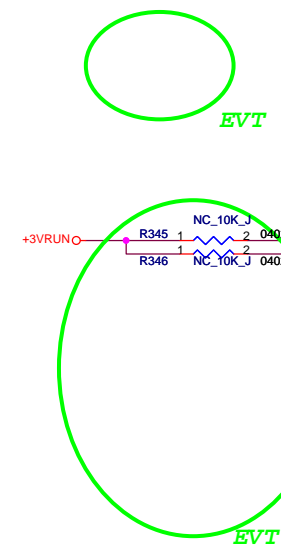
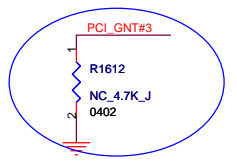
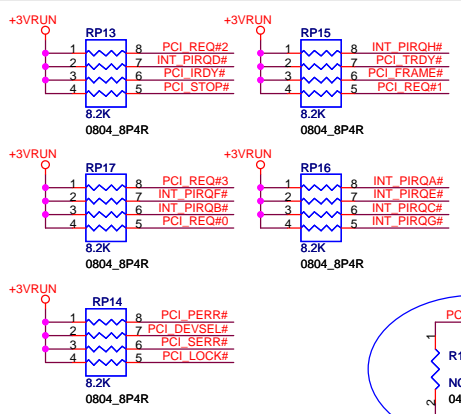


Calpella Platform - Design Guide - Addendum / Update - Rev. 1.52 (Doc #414044)..

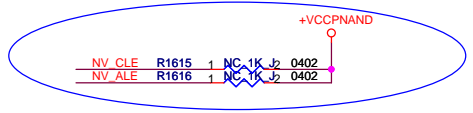
ibexpeak-M
null



Place resistor close to PCH (U69).

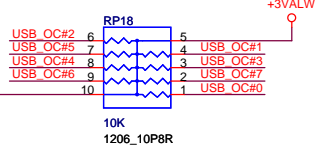


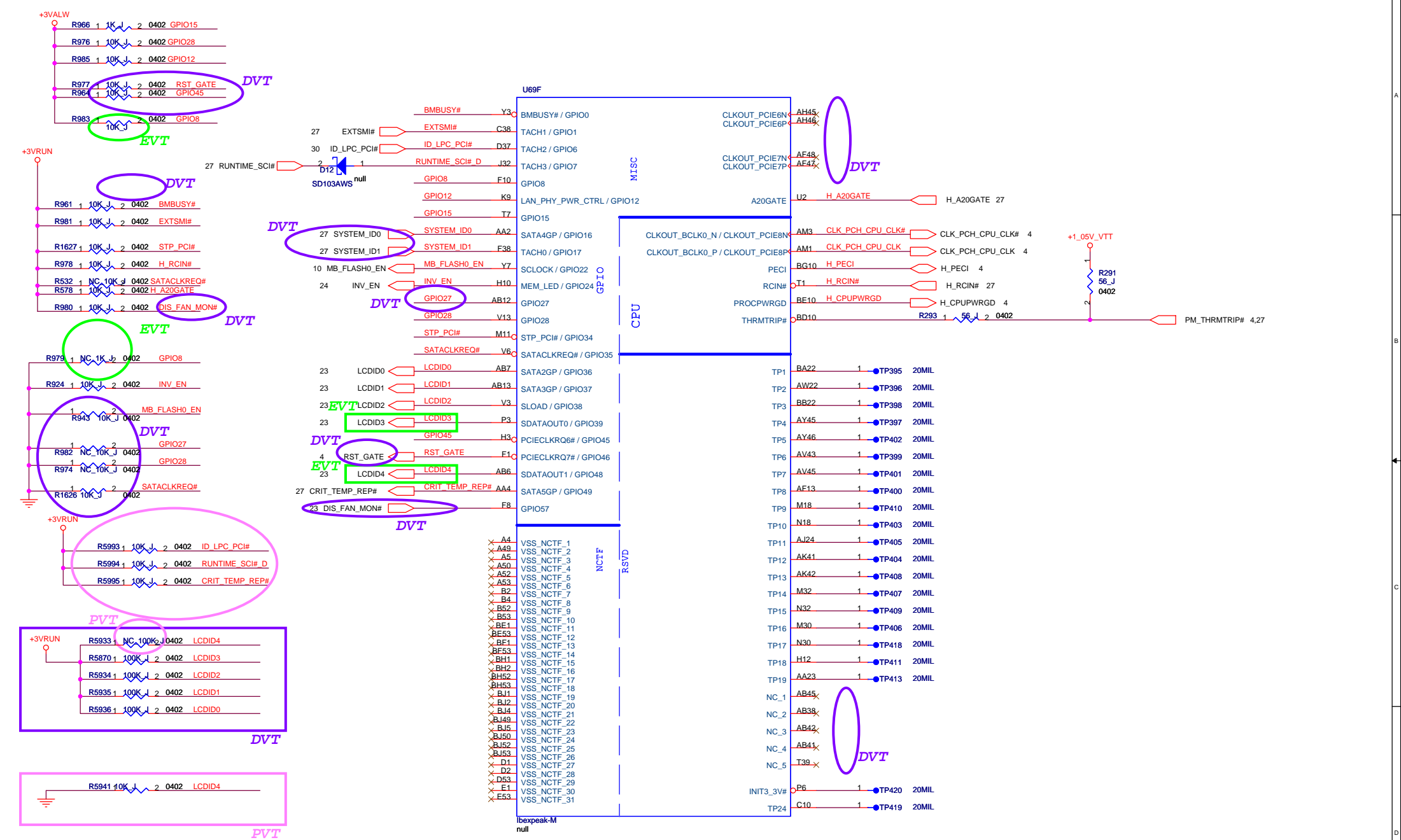
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW
NV_CLE	Set to Vcc when HIGH



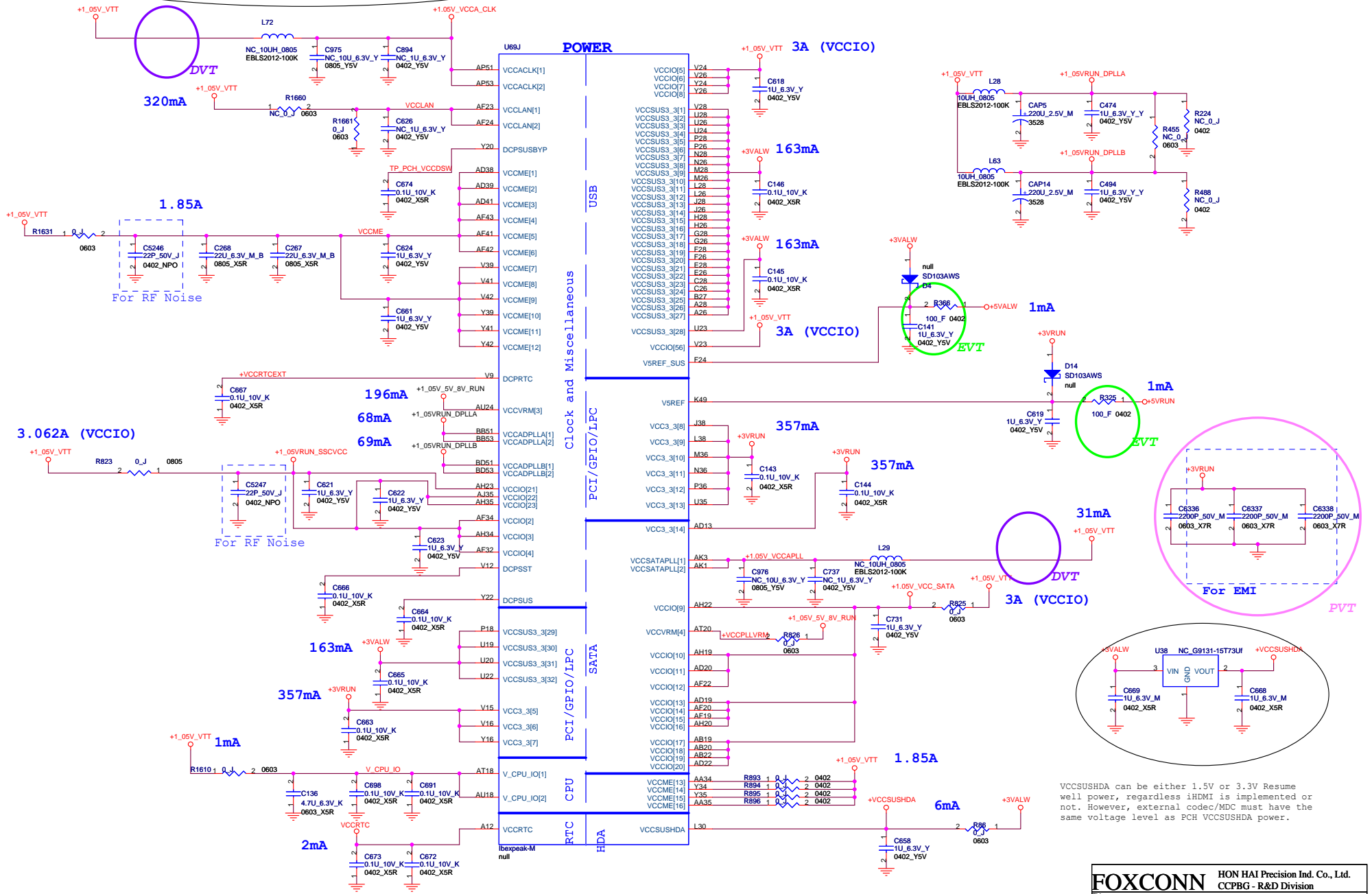
Danbury Technology
Disabled when Low
Enabled when High

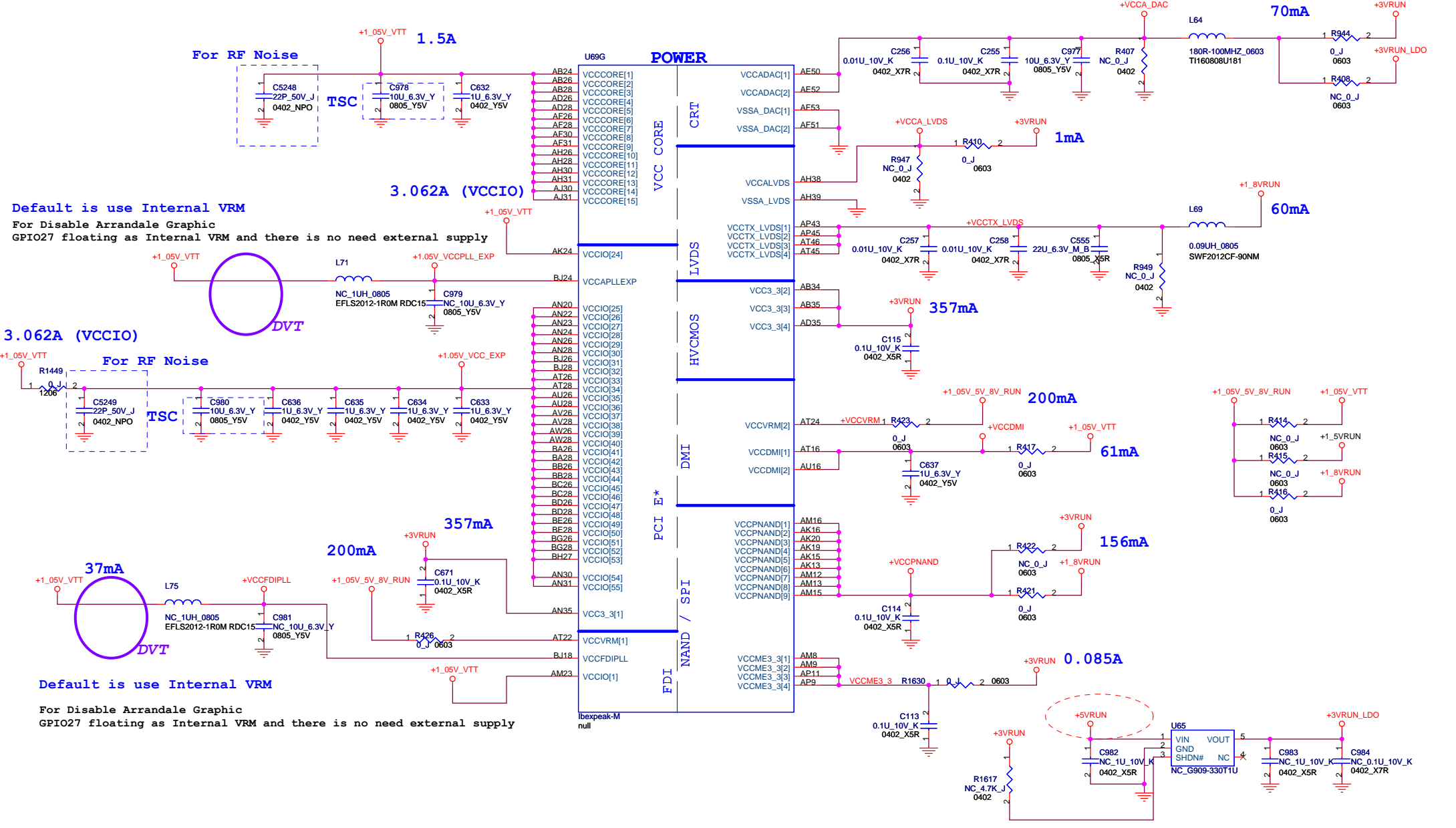
USB PORT	Function
PORT-0	eSATA
PORT-1	External Port-2
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-3
PORT-5	External Port-1
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	
PORT-11	Felica
PORT-12	WLAN
PORT-13	Bluetooth





Default is use Internal VRM
For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



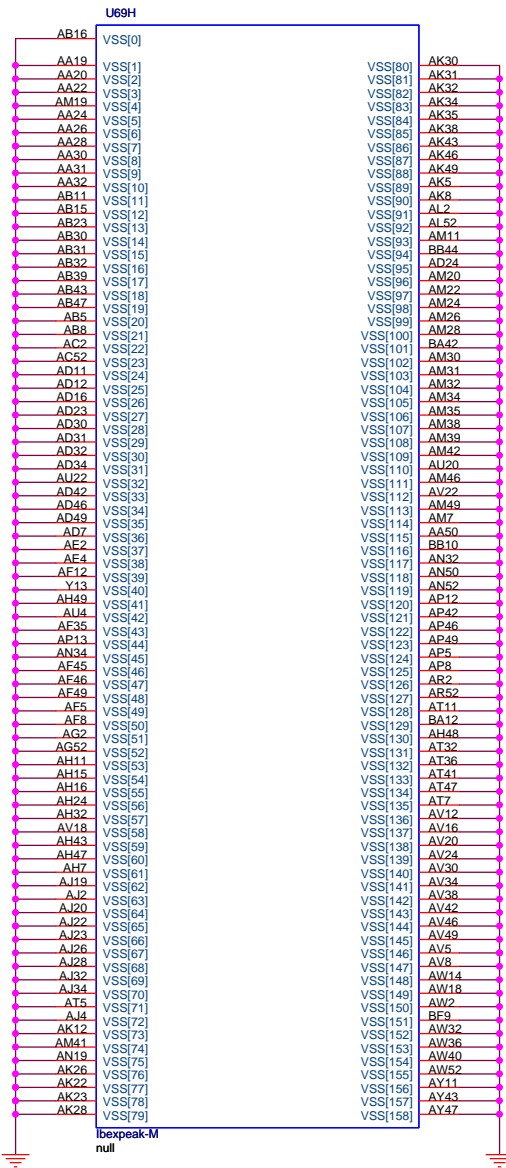
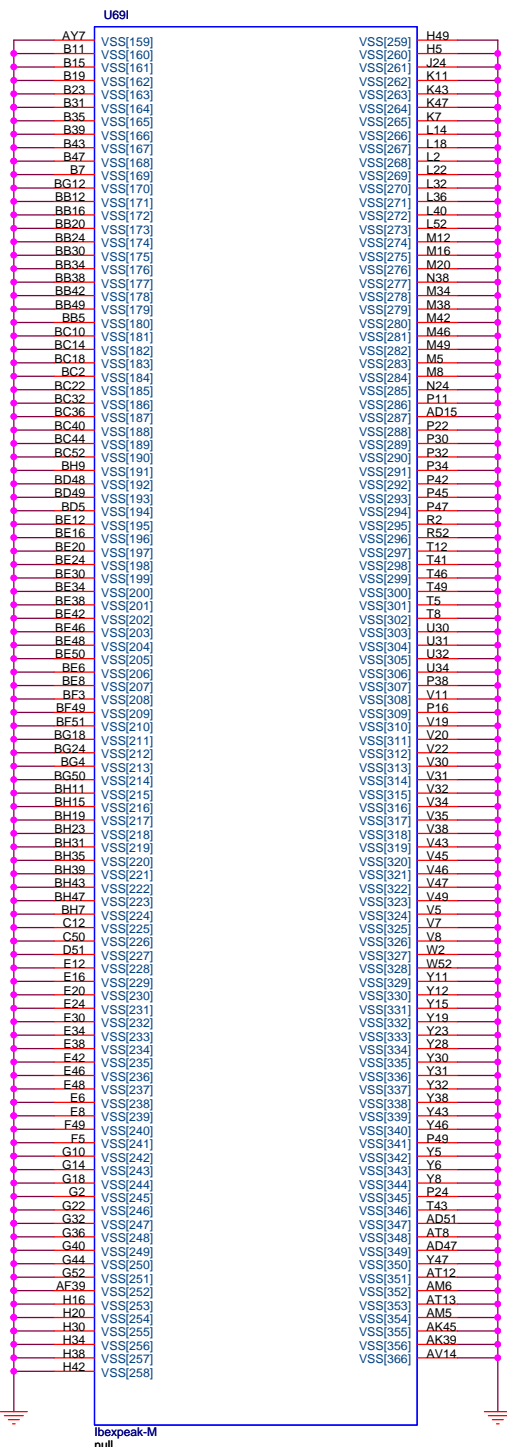


Default is use Internal VRM
 For Disable Arrandale Graphic
 GPIO27 floating as Internal VRM and there is no need external supply

3.062A (VCCIO)
 For RF Noise

37mA
 For RF Noise

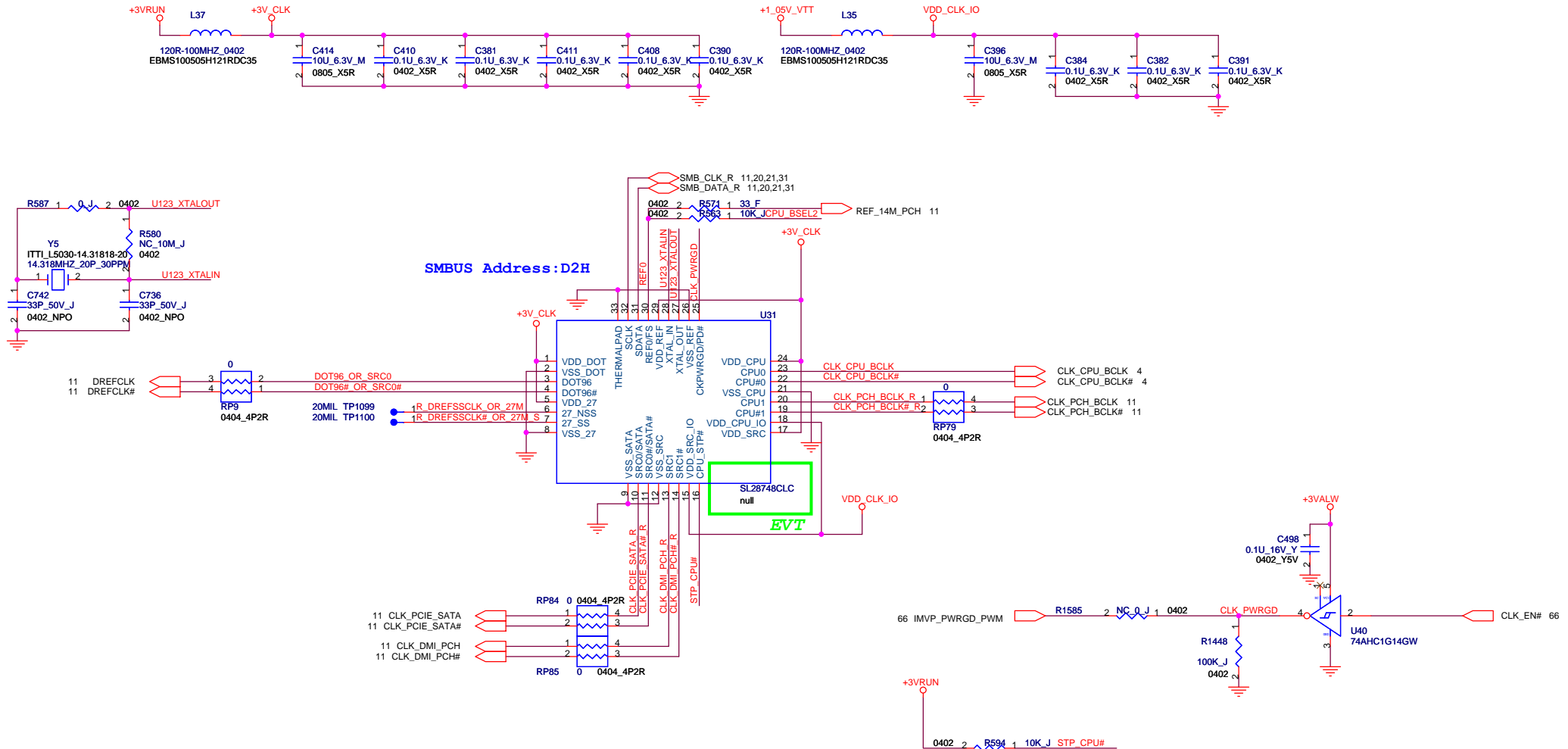
Default is use Internal VRM
 For Disable Arrandale Graphic
 GPIO27 floating as Internal VRM and there is no need external supply



ibexpeak-M
null

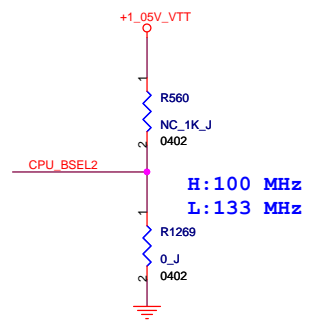
ibexpeak-M
null

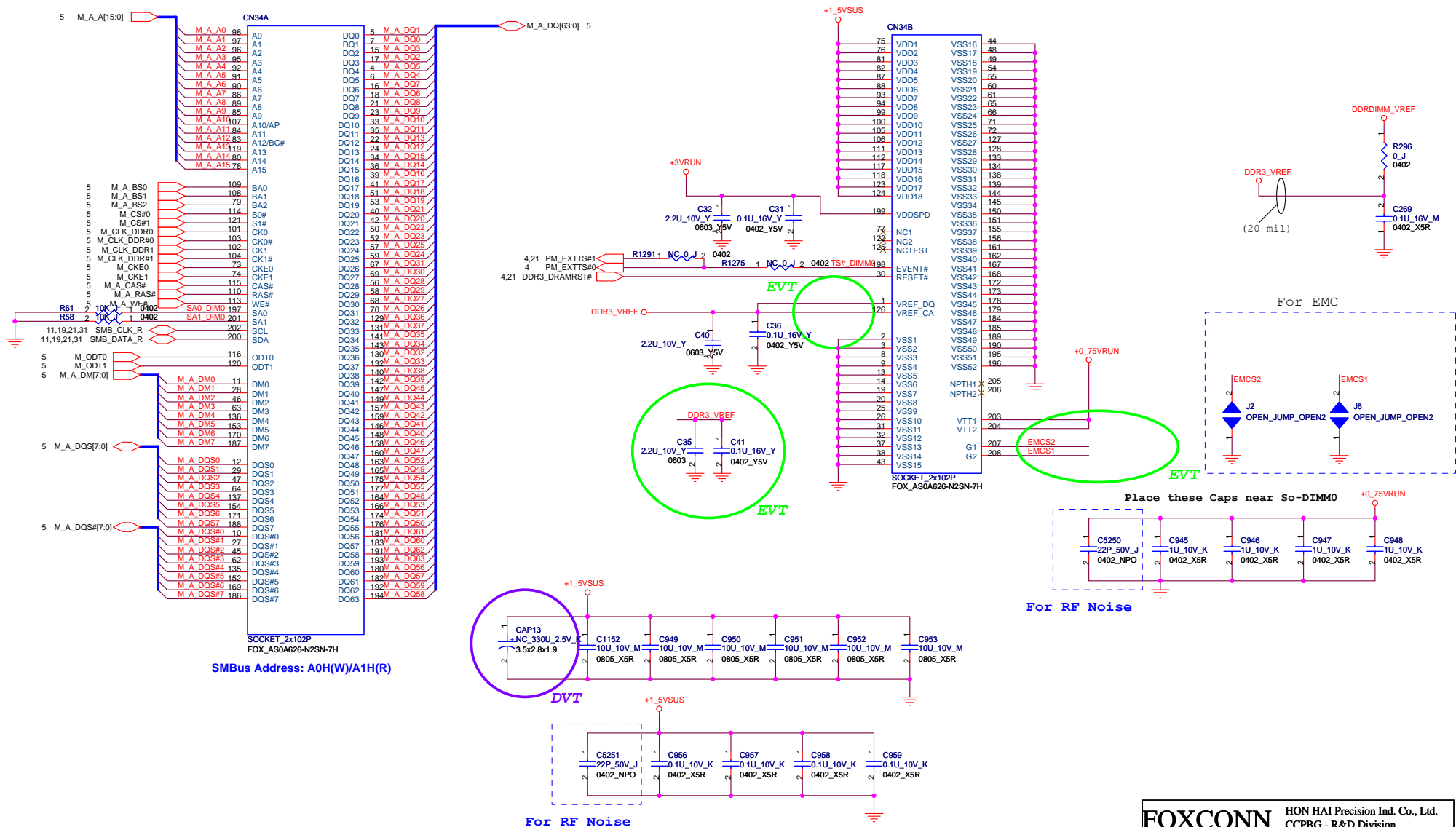
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	PCH (VSS)		Rev
Size	Document Number		
A3	M960&M970 L Model	SA	
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Frequency Select Pin (FS)

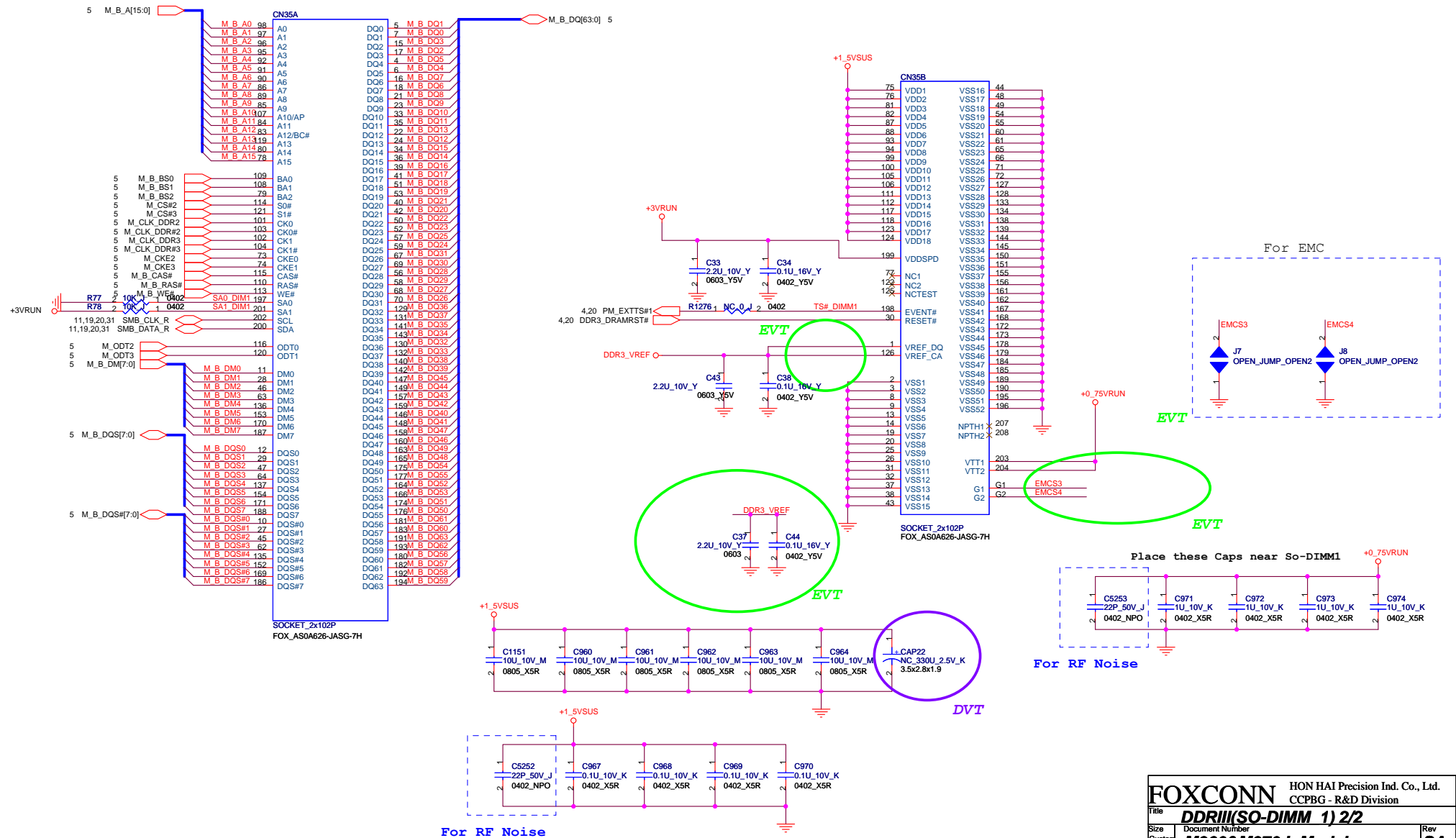
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

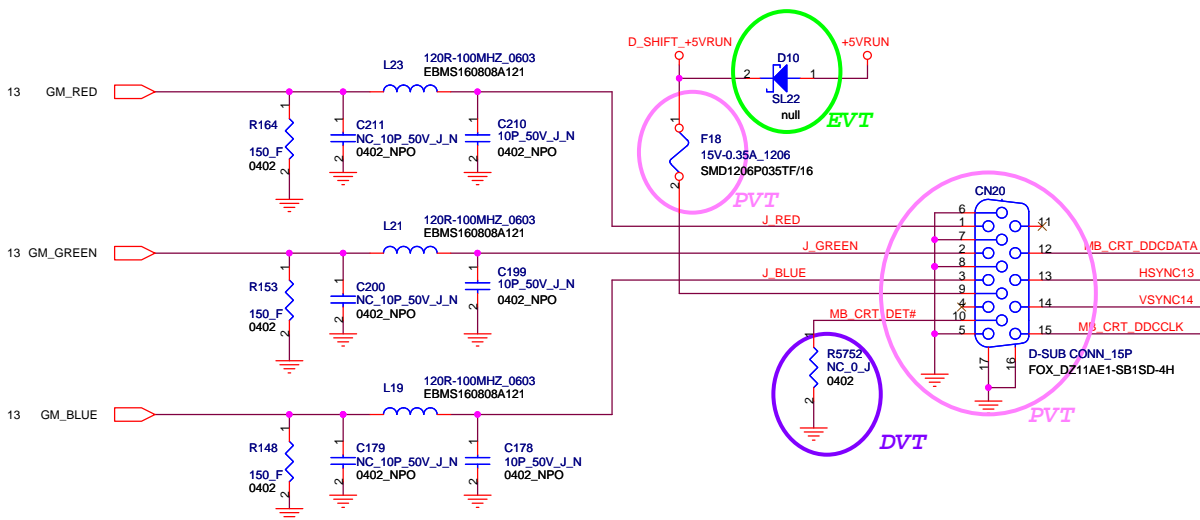
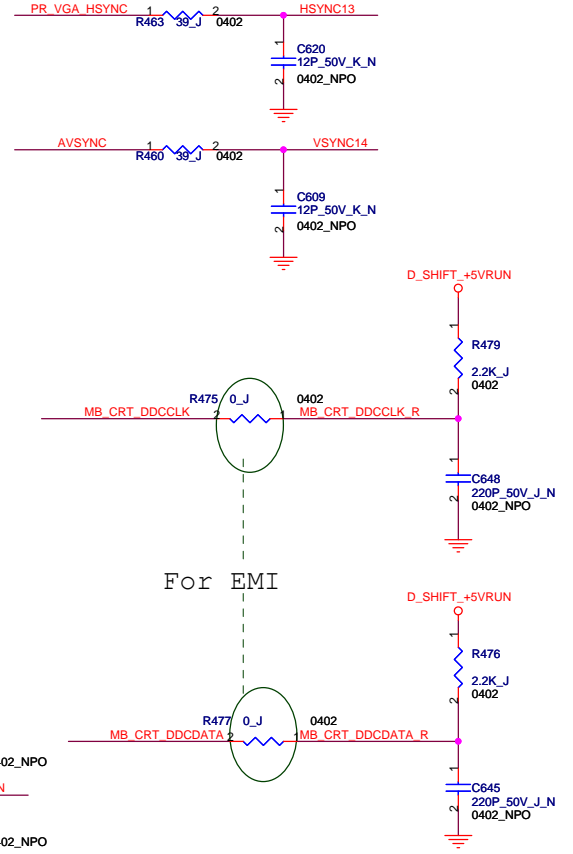
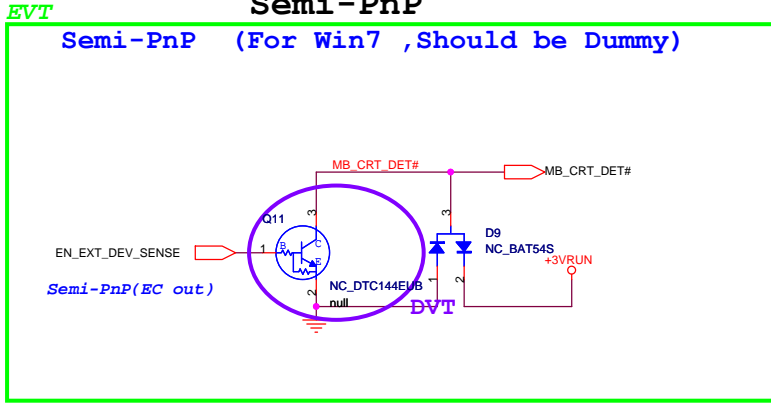
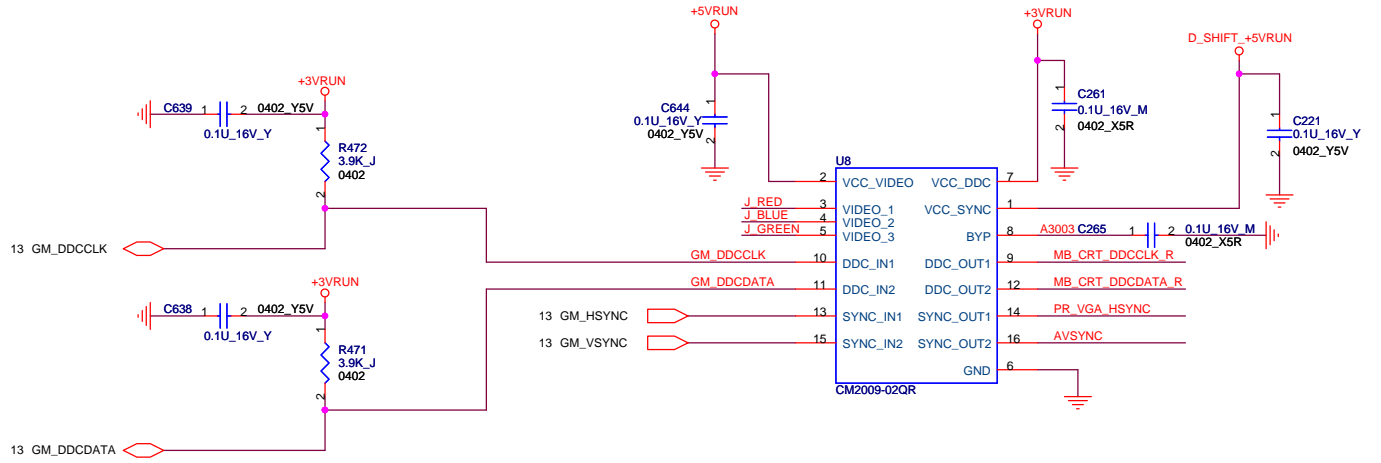




SMBus Address: A0H(W)/A1H(R)

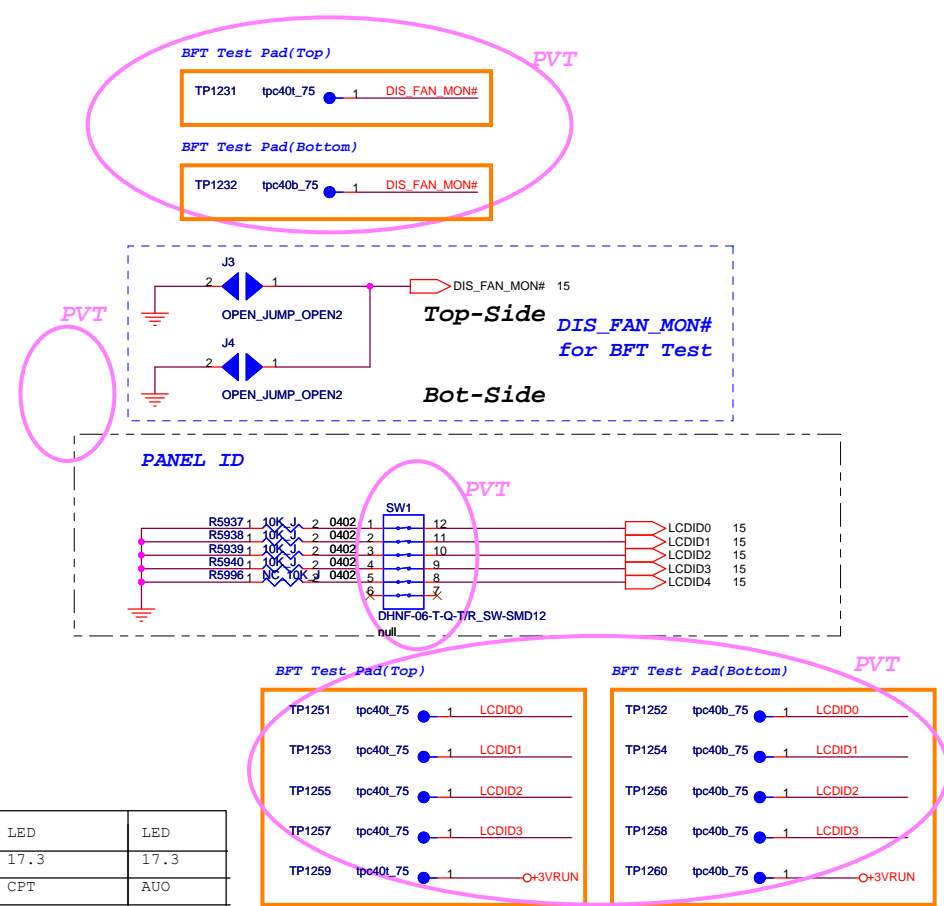
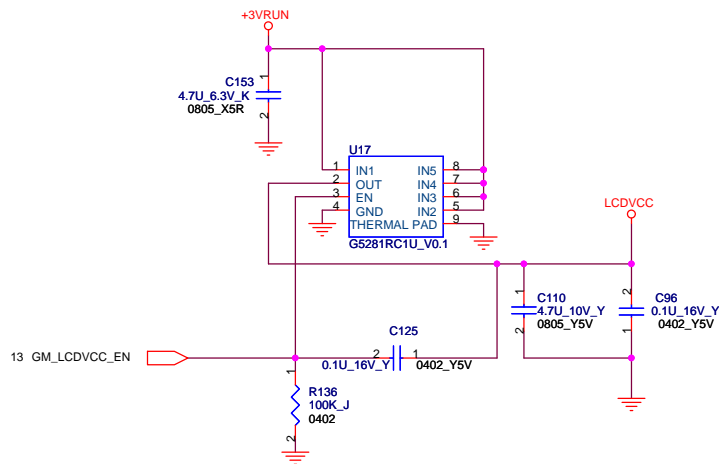
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DDRIII(SO-DIMM 0) 1/2			
Size	Document Number		Rev
Custom	M960&M970 L Model		SA
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CRT CONNECTOR

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Title CRT			
Size	Document Number	Rev	
A3	M960&M970 L Model	SA	
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PANEL ID

Type		LED	LED	LED	LED	1	1	1	LED	LED	LED
Size	14	14	14	14	14	15.5	15.5	15.5	15.5	17.3	17.3
Vendor	No LCD	AUO	Samsung	LGD	AUO	LGD	CPT	Samsung	LGD	CPT	AUO
Model Name		B140XW02	LTN140AT08	LP140WH2	B140RW02	LP156WH1	CLAA156WA01A	LTN156AT01	LP156WF1	CLAA173UA01A	B173HW01
Panel ID [4.3.2.1.0]	00000	00001	00010	00011	00100	00110	00111	01000	01001	01011	01100

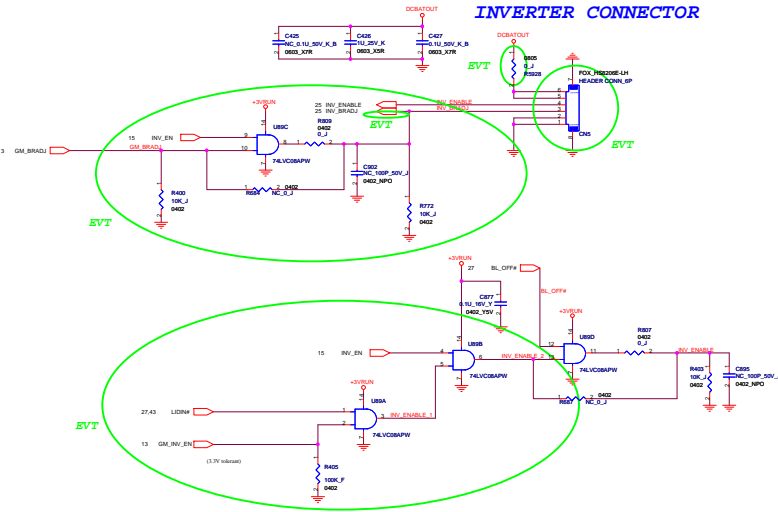
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

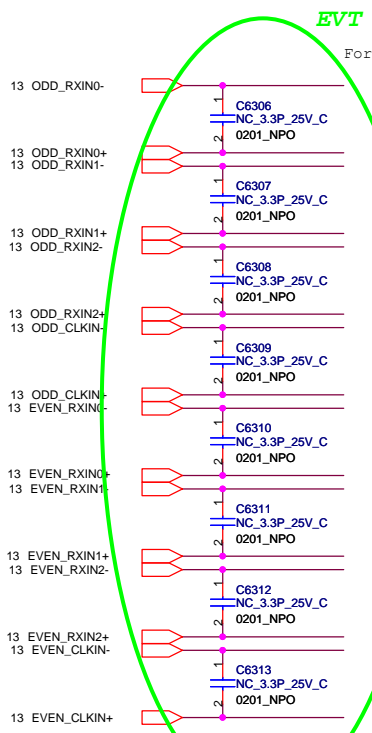
Title: **LVDS**

Size: A3 Document Number: **M960&M970 L Model** Rev: **SA**

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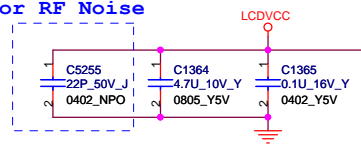
INVERTER CONNECTOR



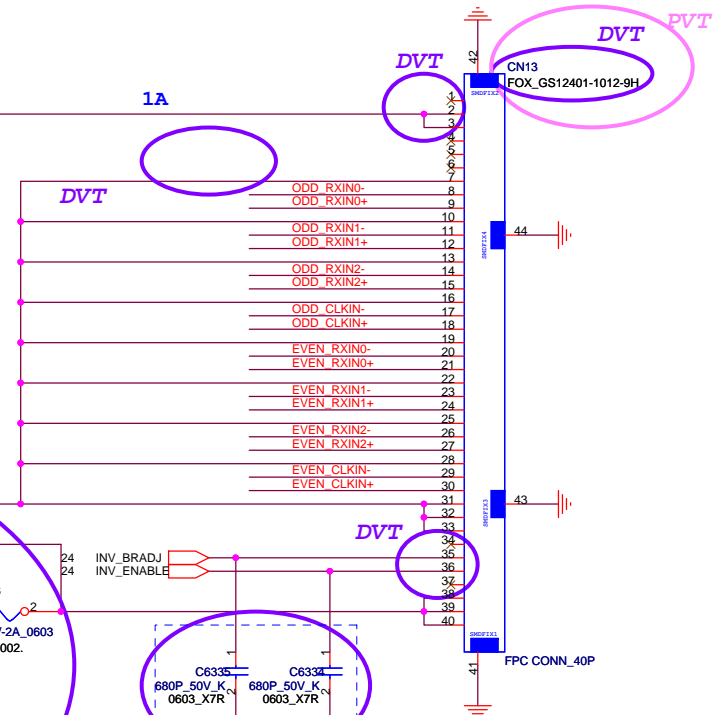
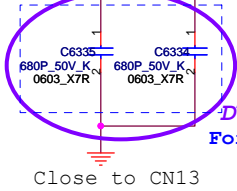
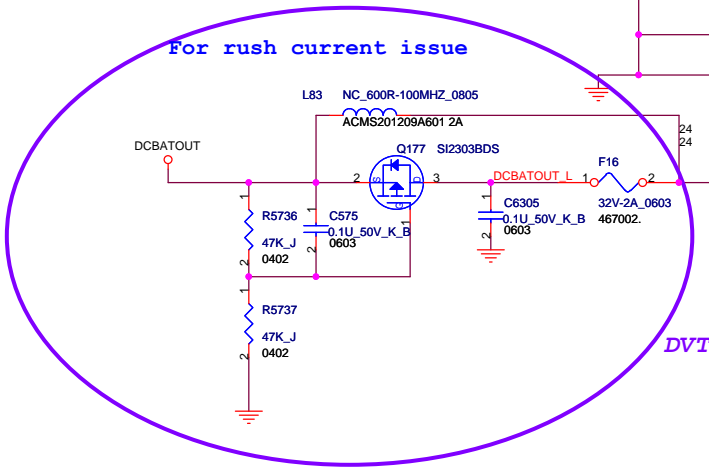


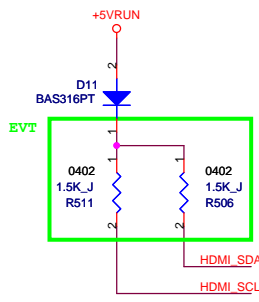
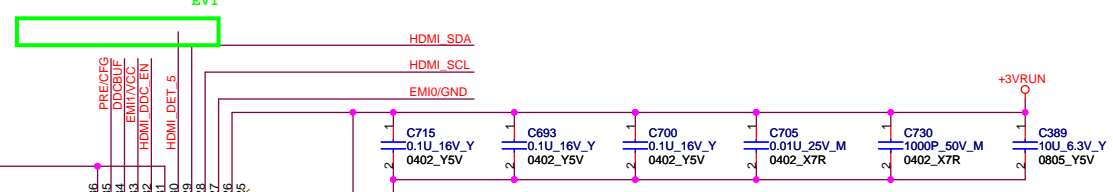
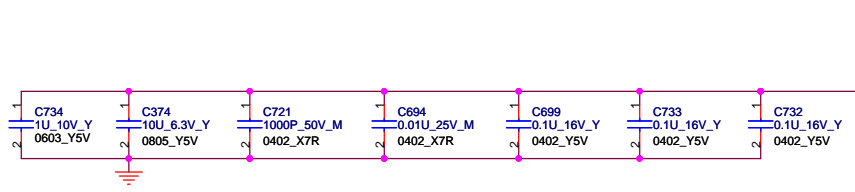
LVDS CONNECTOR

For RF Noise

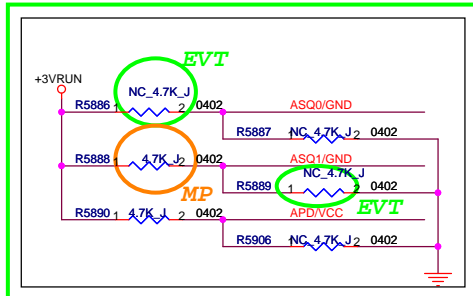
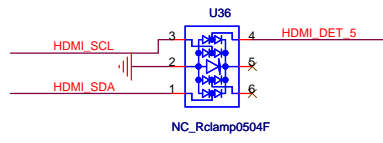
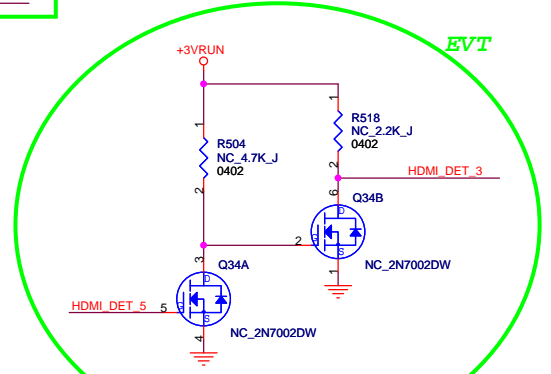
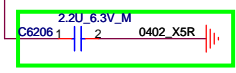
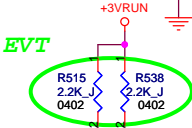
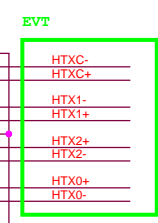
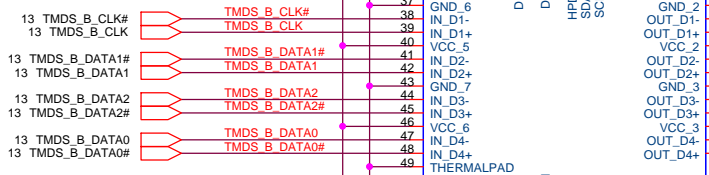
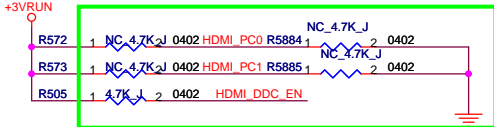


For rush current issue

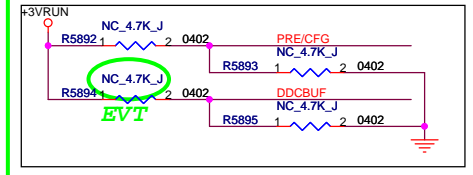




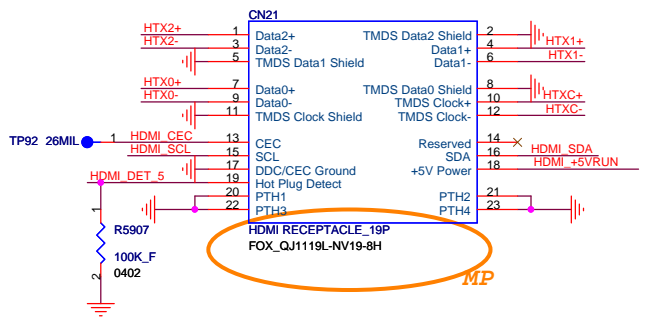
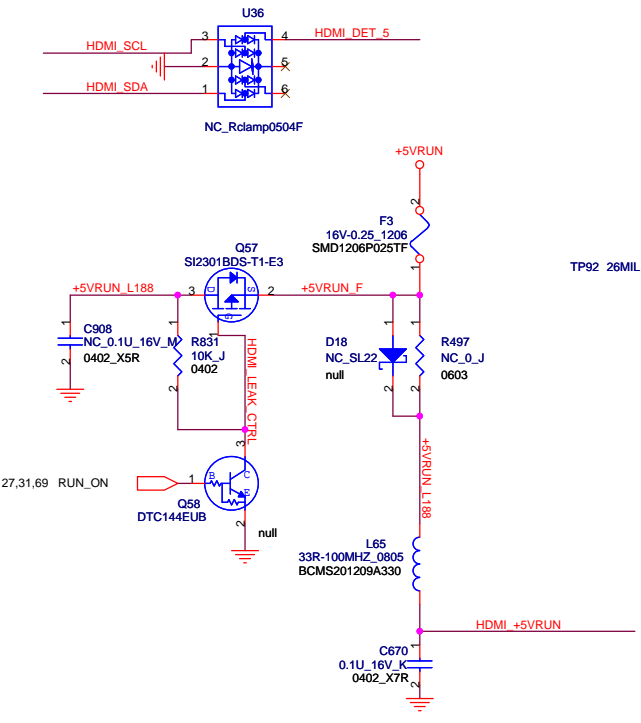
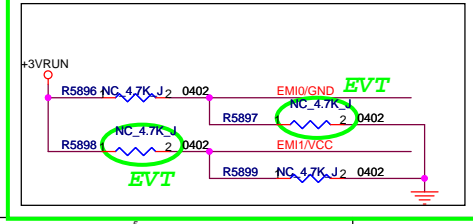
(TMSD inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB

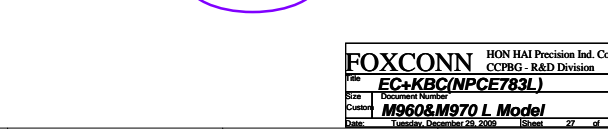
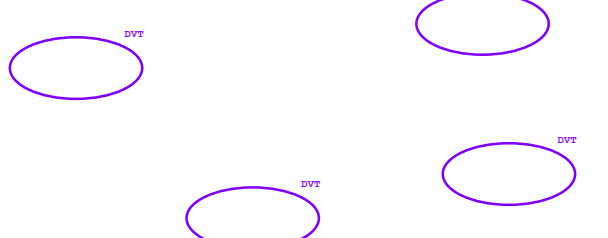
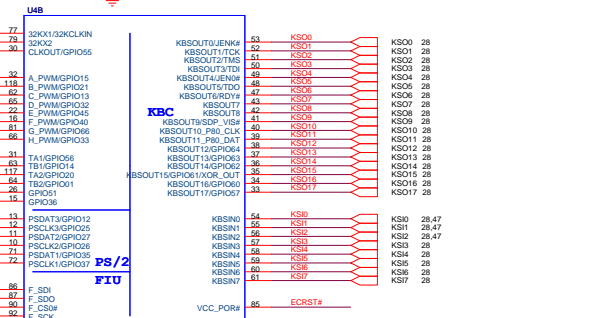
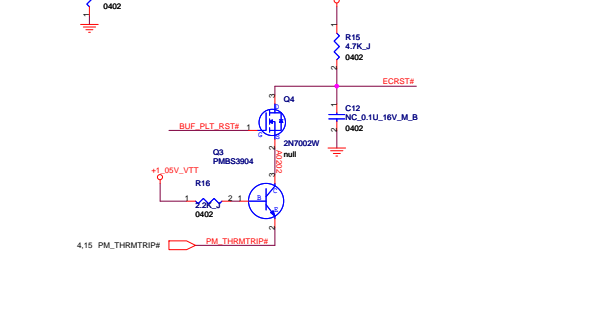
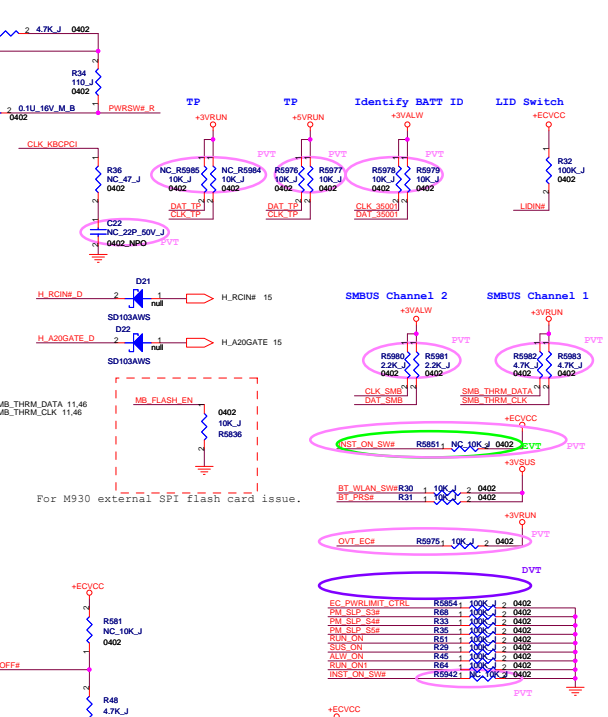
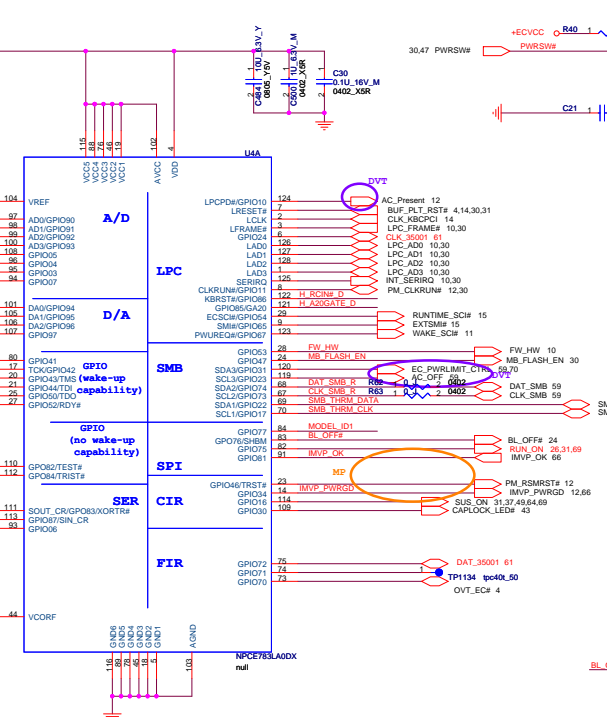


For Automatic power down



For EMI reduction



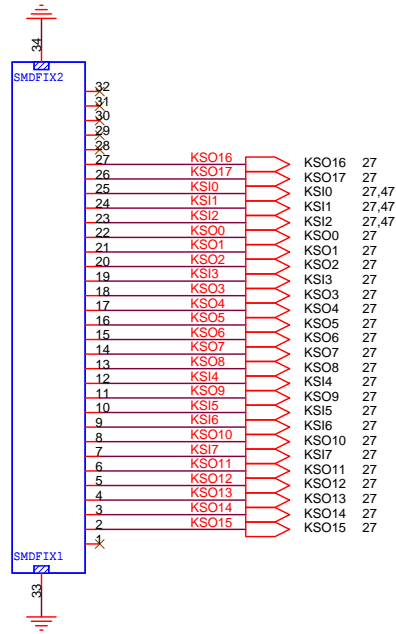


ID1 (gSPU)	ID0	SKU
0	0	L
0	1	Reserved
1	0	M
1	1	H

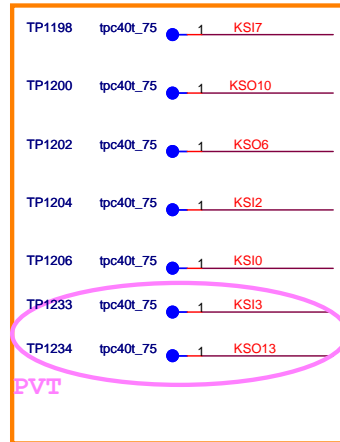
ID3	ID2	ID1	ID0	SKU
0	0	0	0	M960
0	1	0	0	M970
1	0	0	0	M980

KBC Conn

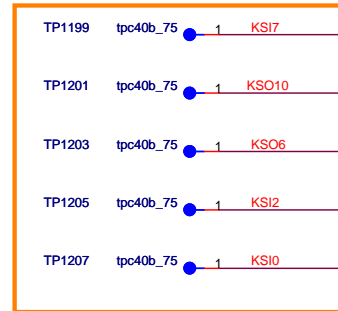
CN38
FPC CONN_32P
FOX_GB1SH320-1280-7H



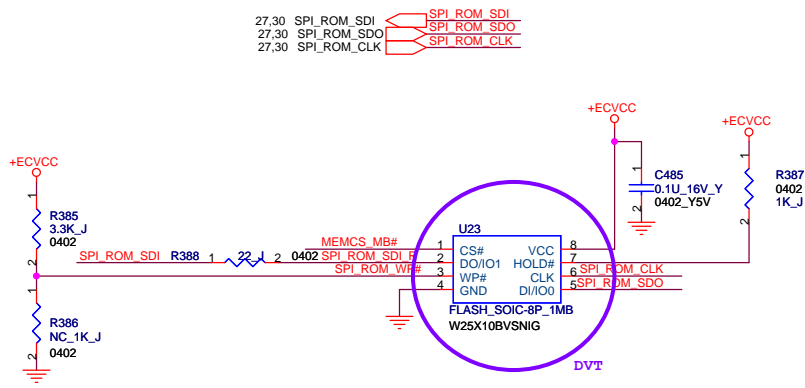
BFT Test Pad(Top)



BFT Test Pad(Bottom)

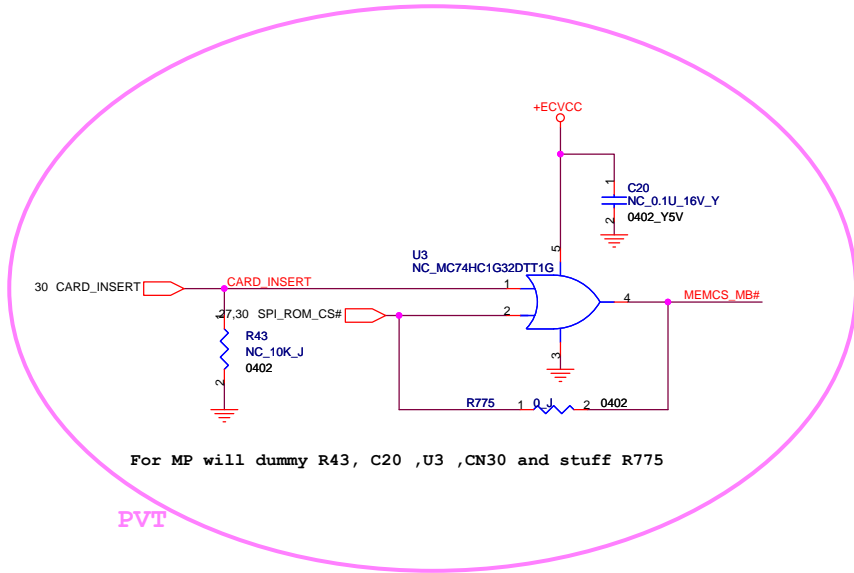


FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title KB Connector			
Size	Document Number		Rev
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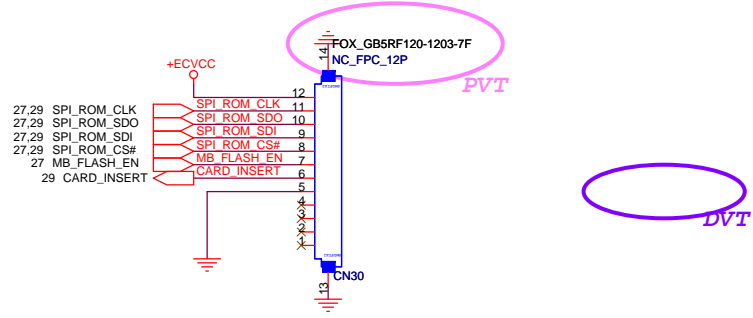
27.30 SPI_ROM_SDI < SPI_ROM_SDI
 27.30 SPI_ROM_SDO < SPI_ROM_SDO
 27.30 SPI_ROM_CLK < SPI_ROM_CLK

SPI ROM (EC Firmware) (1Mb)

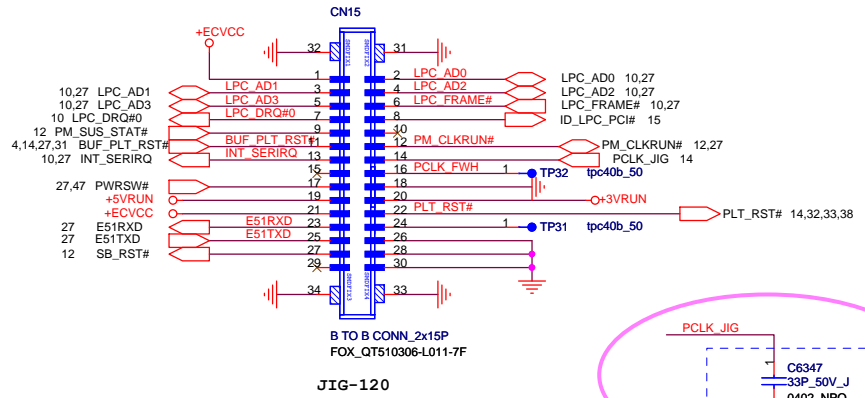


For MP will dummy R43, C20, U3, CN30 and stuff R775

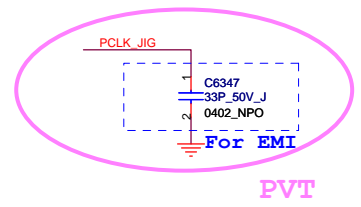
PVT



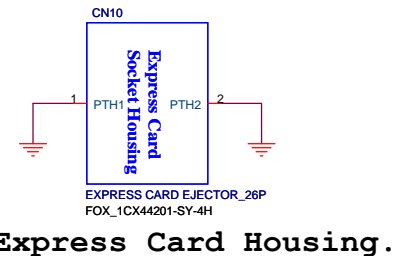
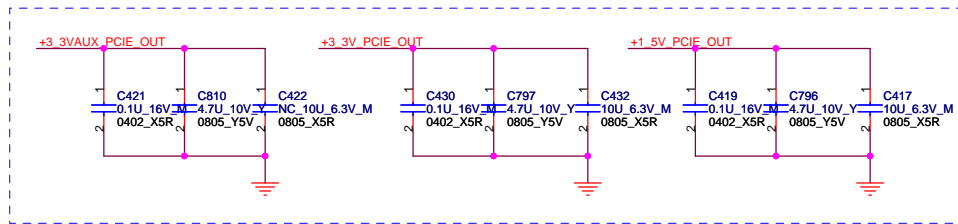
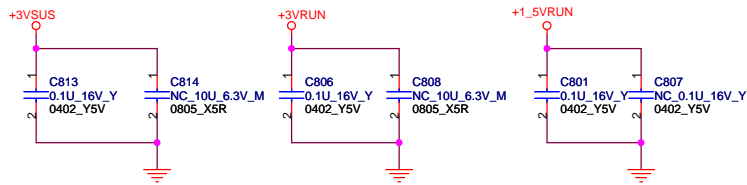
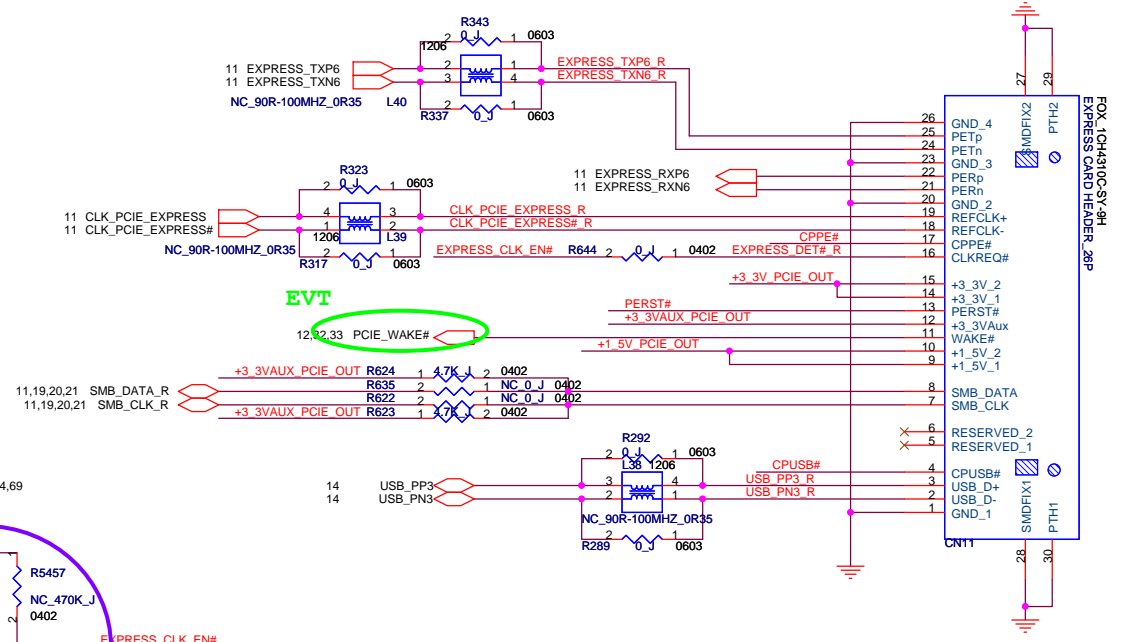
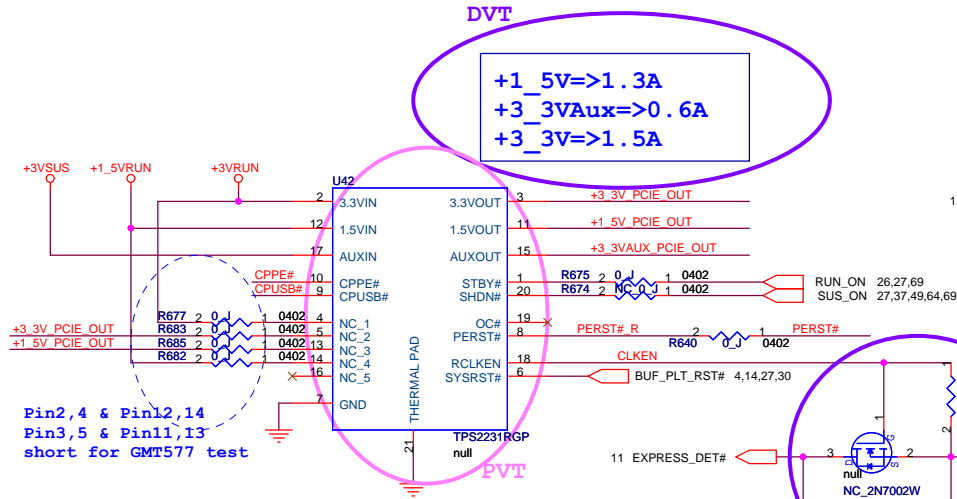
EXTERNAL SPI ROM INTERFACE (EC)

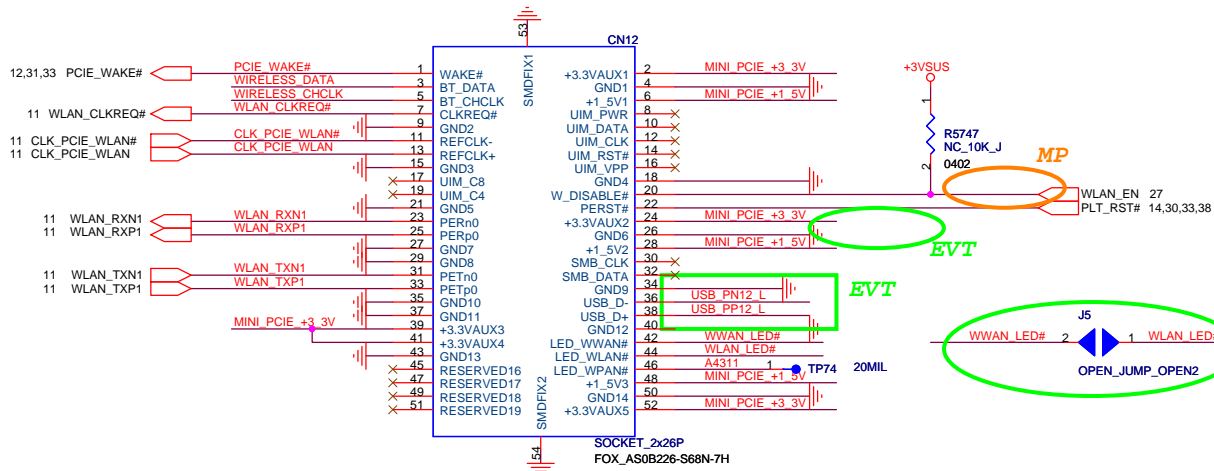


B TO B CONN_2x15P
FOX_QT510306-L011-7F
JIG-120

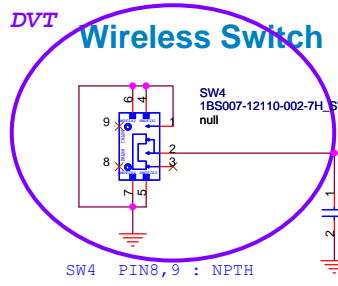
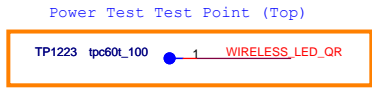
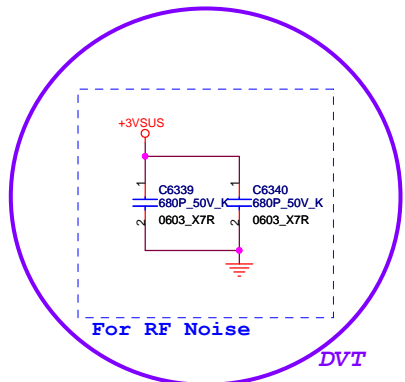


PVT

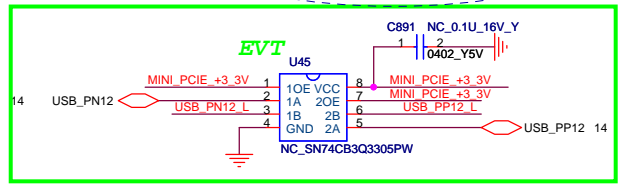
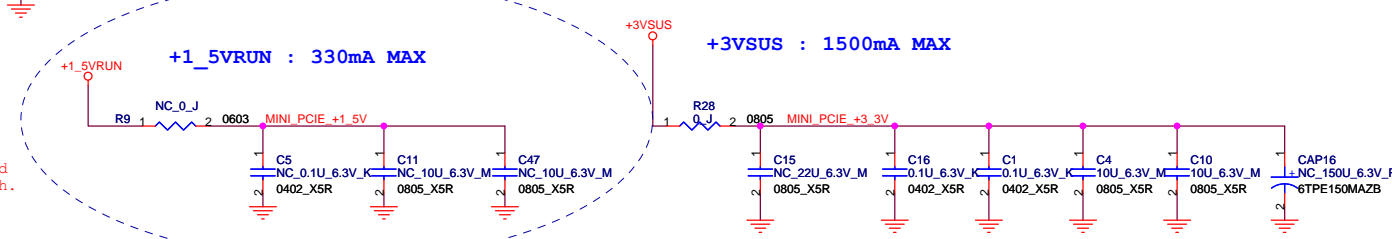
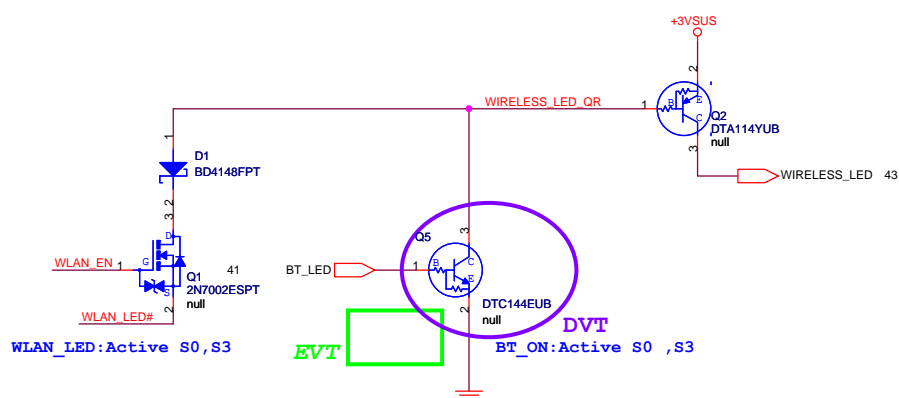
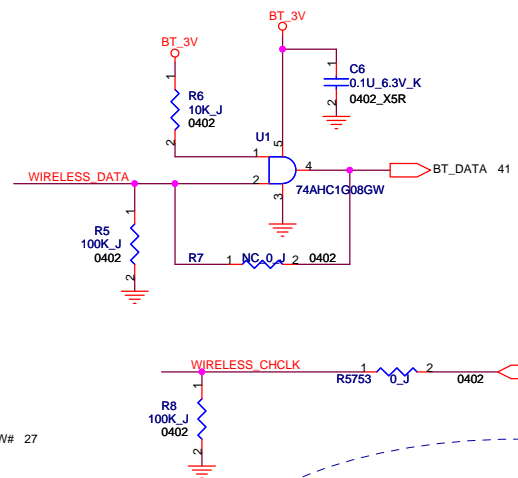




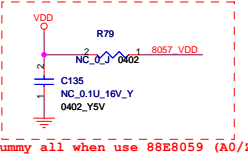
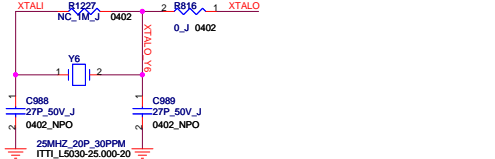
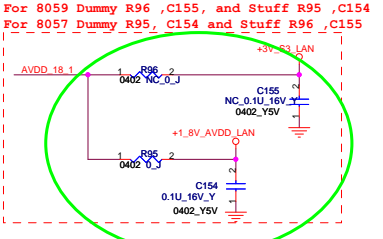
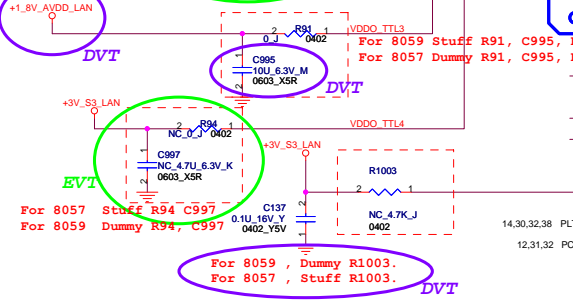
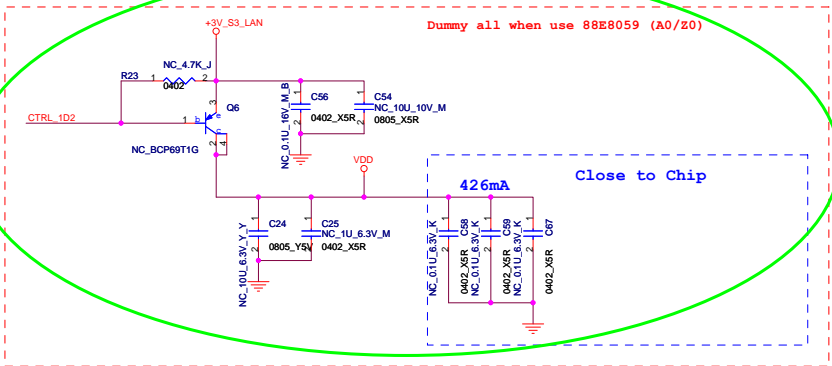
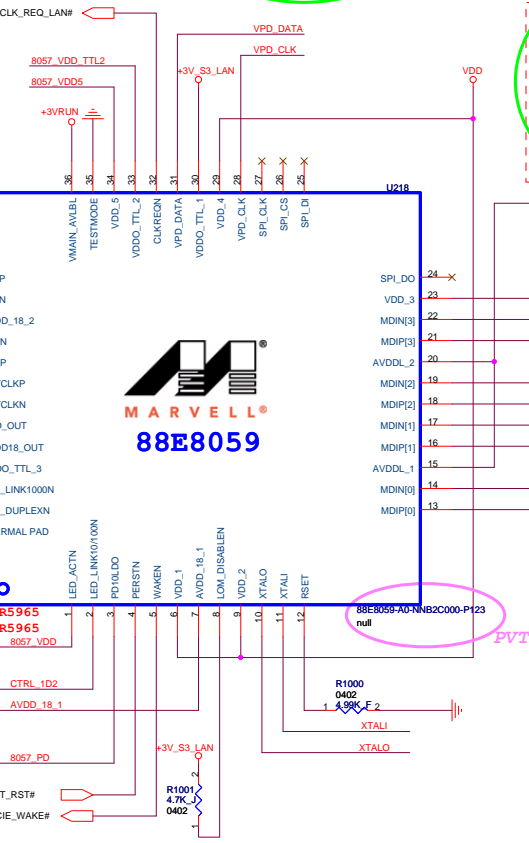
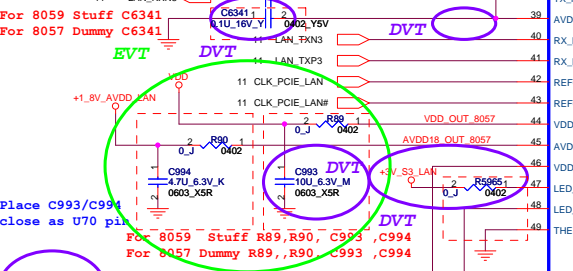
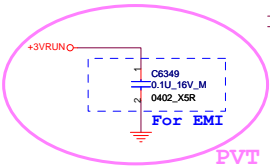
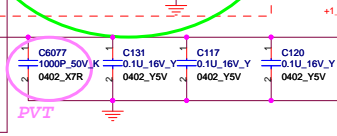
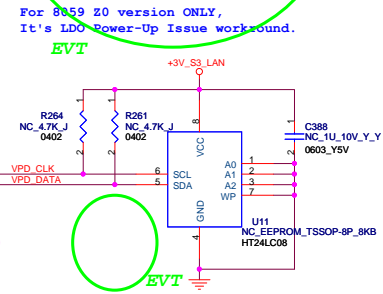
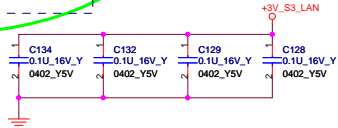
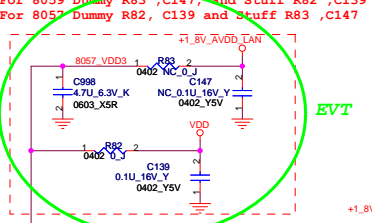
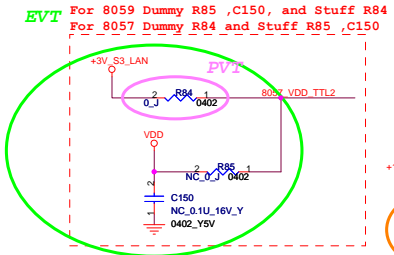
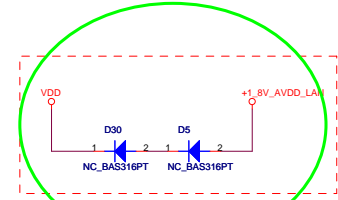
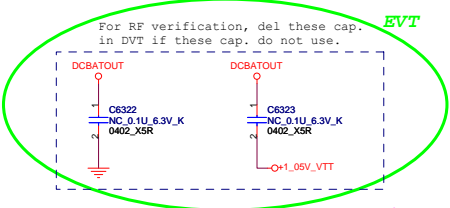
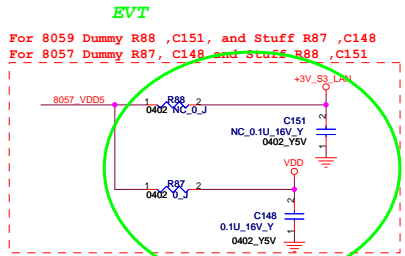
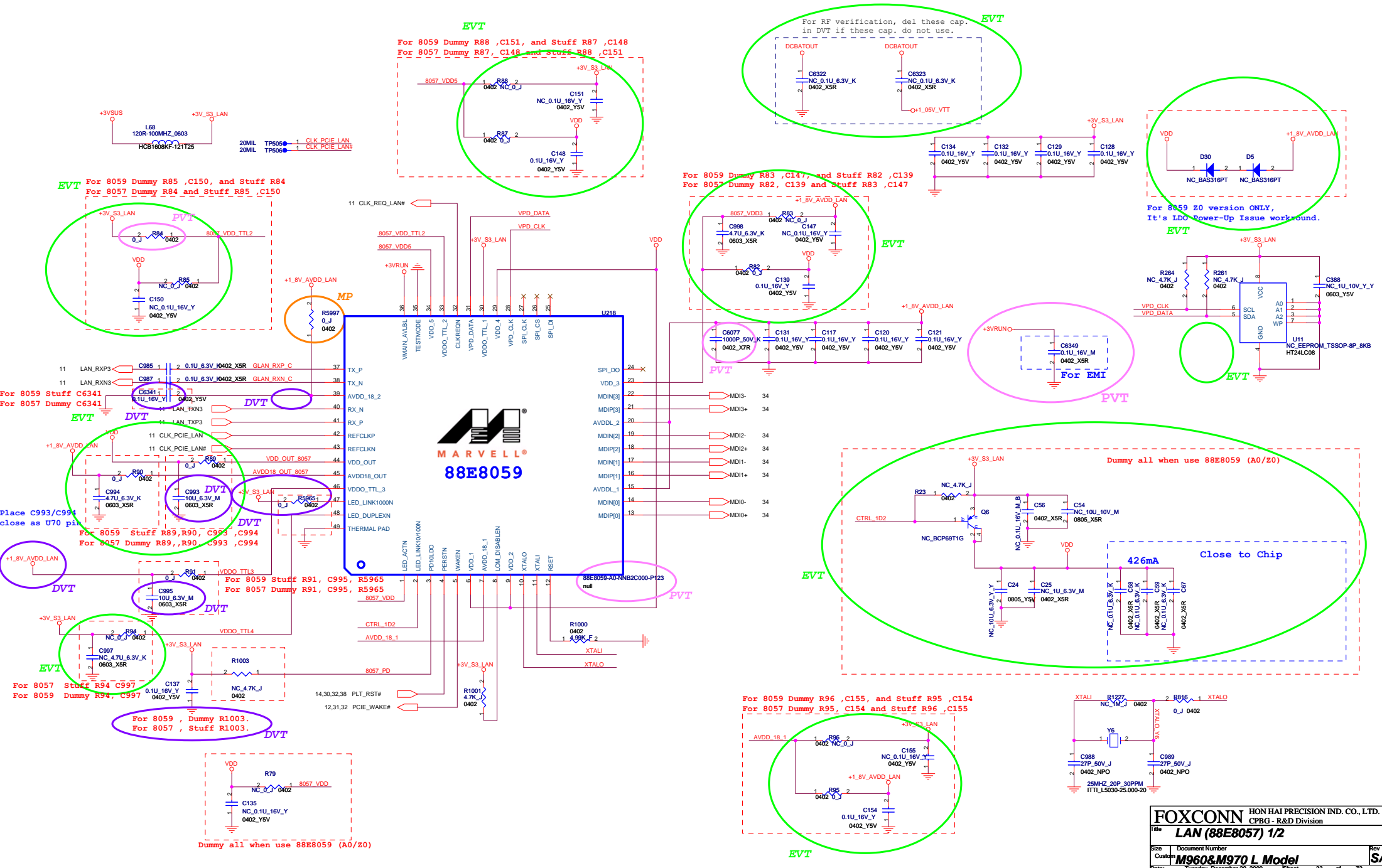
Half Size Mini Card

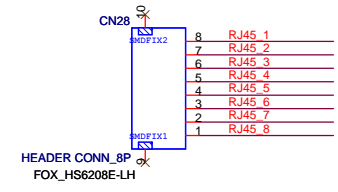
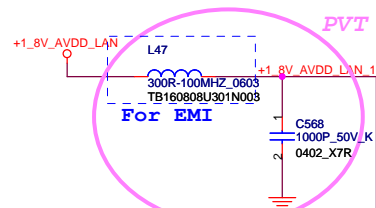


This is a reserved circuit. According to RF comment, this circuit could be deleted if Layout space is not enough.

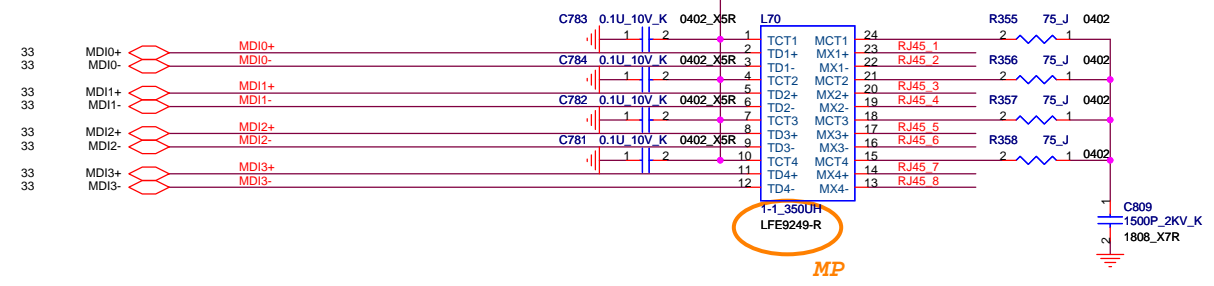


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Mini-PCIE Card (WLAN)		
Size	Document Number		
A3	M960&M970 L Model		
Date:	Tuesday, December 29, 2009	Sheet	32 of 73
Rev	SA		





RJ45

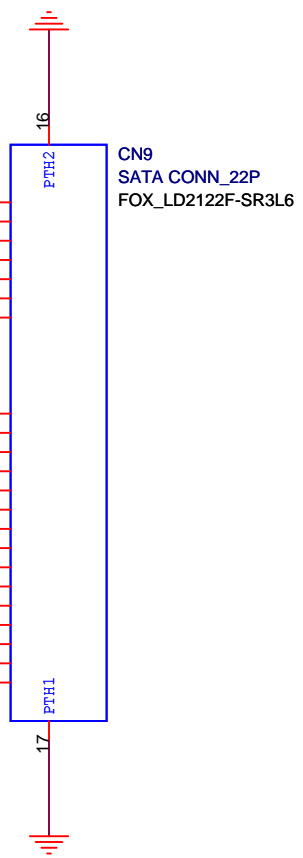
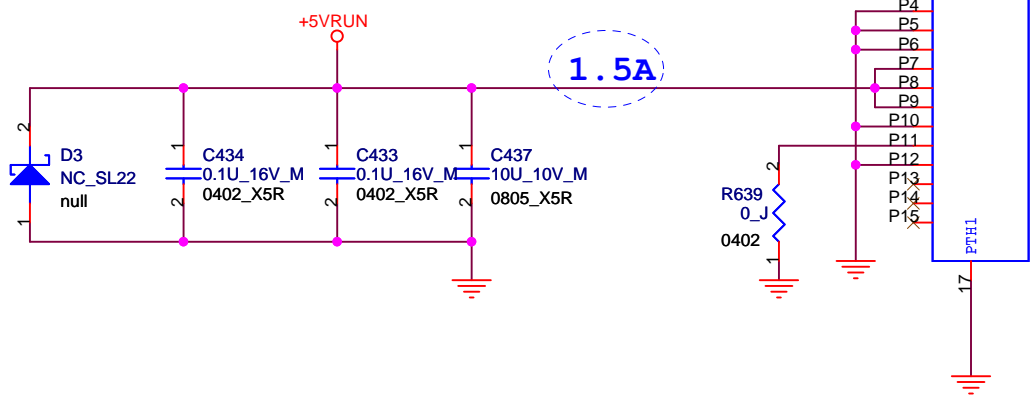
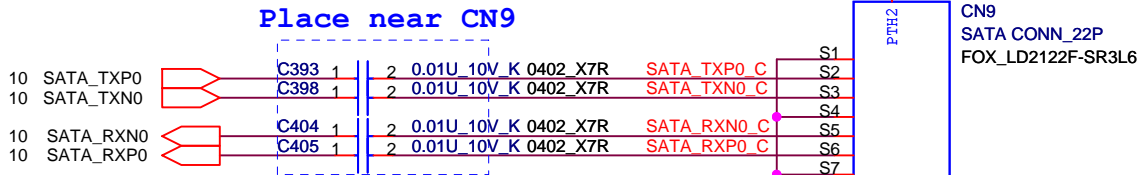


BFT Test Point(TOP)

TP1166	tpc40t_75	1	RJ45_8	TP1174	tpc40t_75	1	RJ45_4
TP1168	tpc40t_75	1	RJ45_7	TP1176	tpc40t_75	1	RJ45_3
TP1170	tpc40t_75	1	RJ45_6	TP1178	tpc40t_75	1	RJ45_2
TP1172	tpc40t_75	1	RJ45_5	TP1180	tpc40t_75	1	RJ45_1

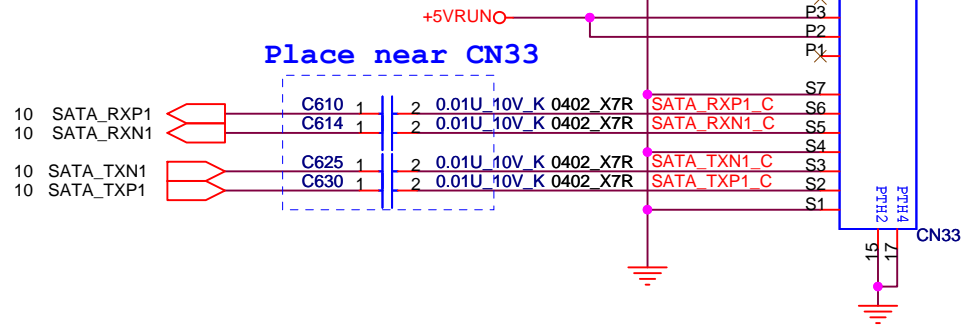
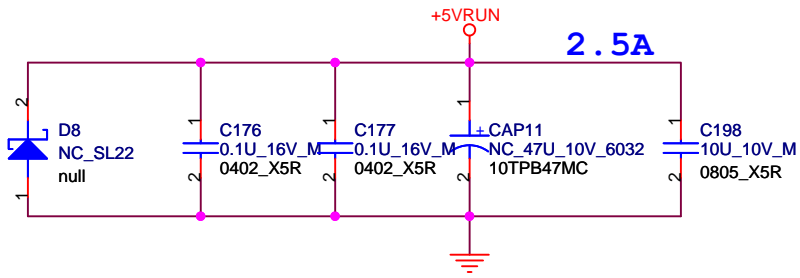
BFT Test Point(Bottom)

TP1167	tpc40b_75	1	RJ45_8	TP1175	tpc40b_75	1	RJ45_4
TP1169	tpc40b_75	1	RJ45_7	TP1177	tpc40b_75	1	RJ45_3
TP1171	tpc40b_75	1	RJ45_6	TP1179	tpc40b_75	1	RJ45_2
TP1173	tpc40b_75	1	RJ45_5	TP1181	tpc40b_75	1	RJ45_1



SATA HDD CONN

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title SATA HDD			
Size A4	Document Number M960&M970 L Model		Rev SA
Date:	Tuesday, December 29, 2009	Sheet 35	of 73

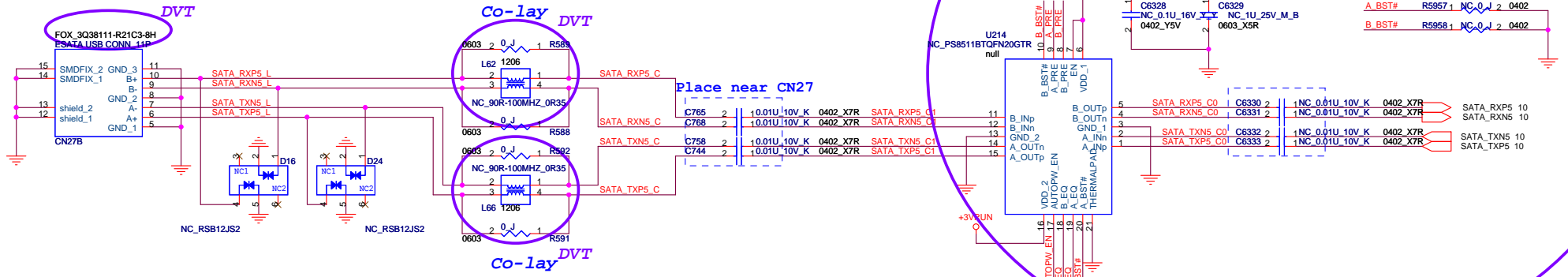
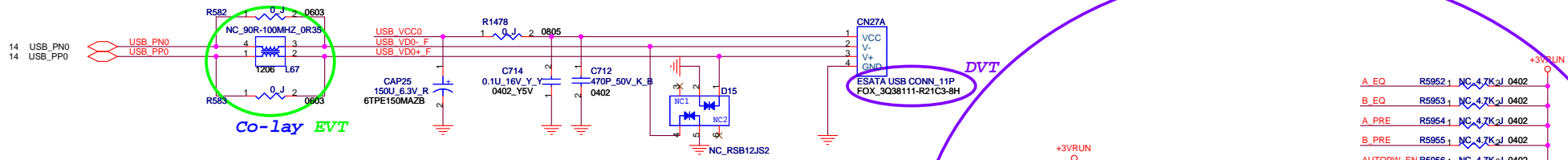
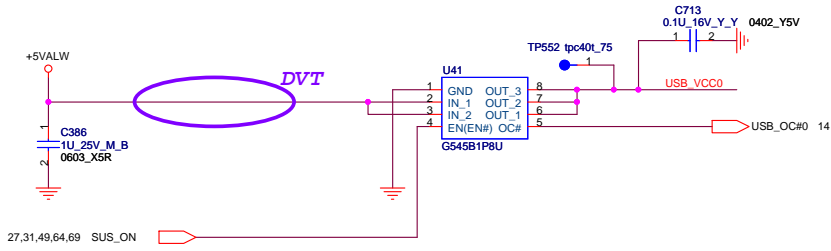


Place near CN33

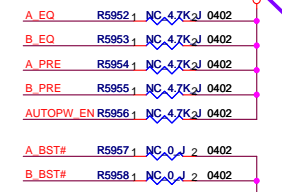
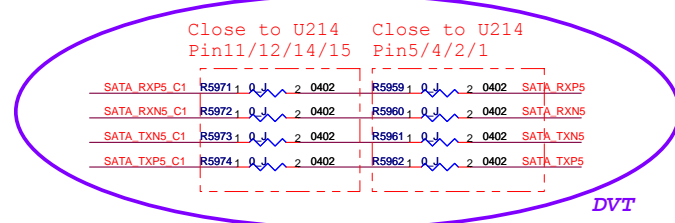
SATA ODD CONN

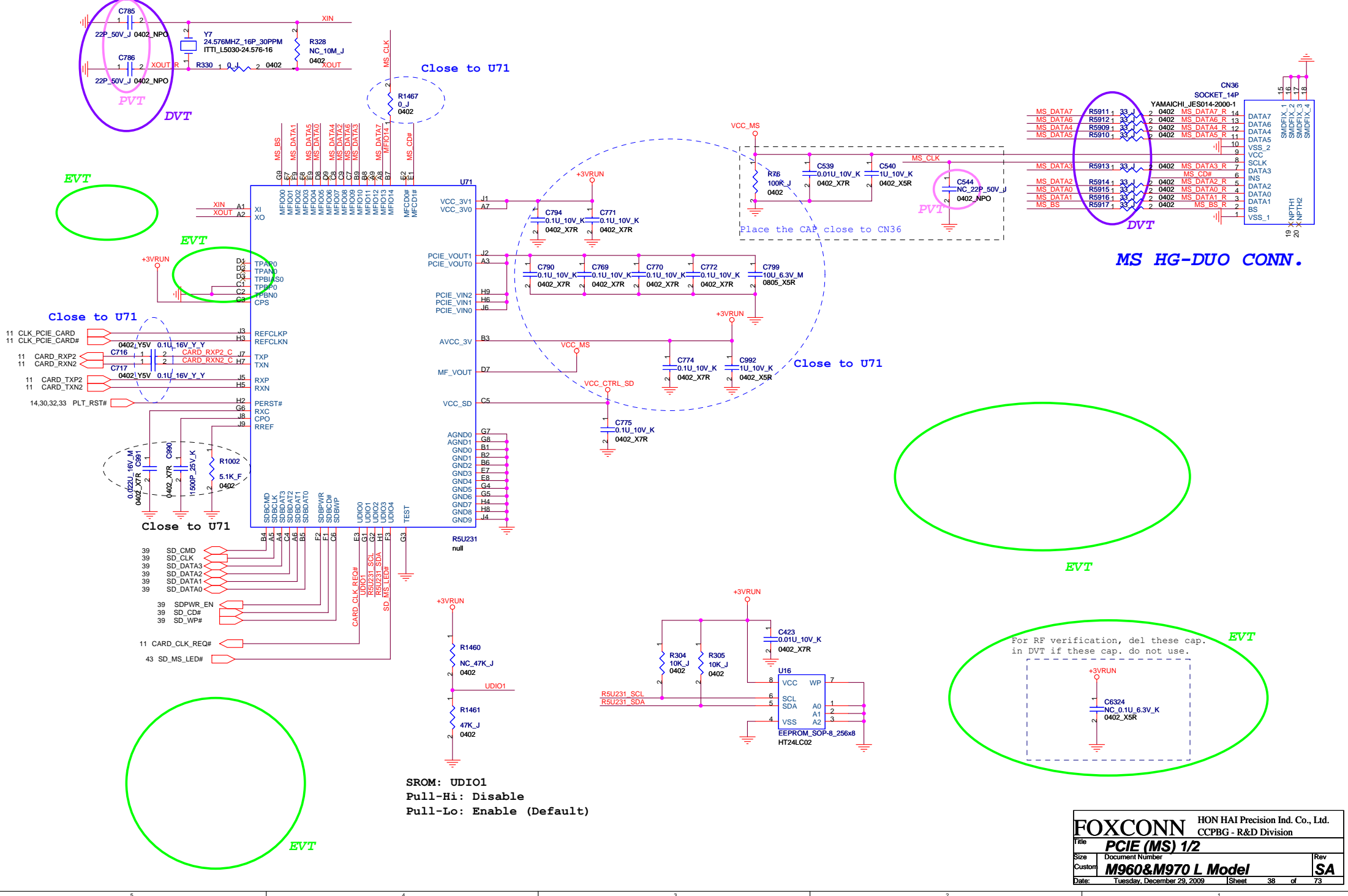
DVT

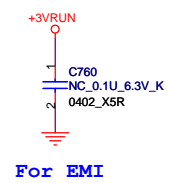
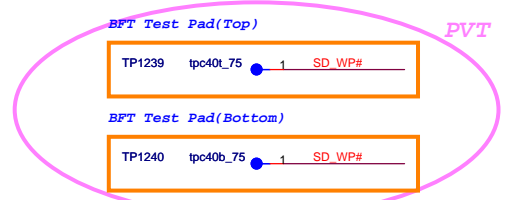
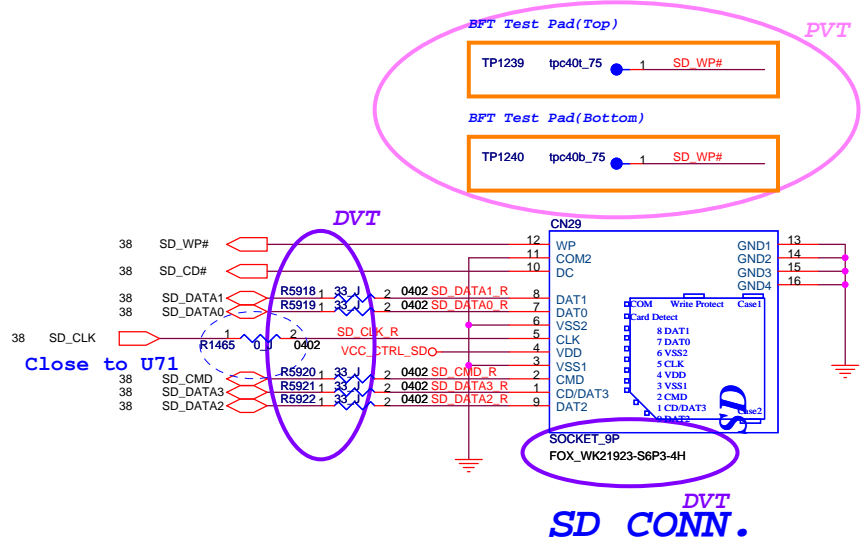
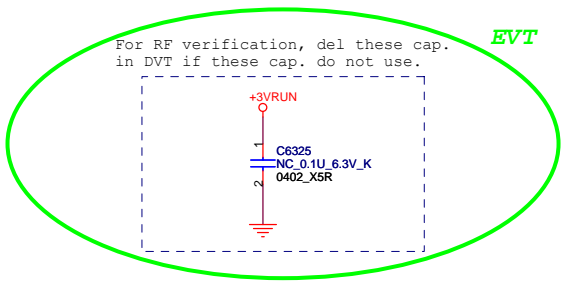
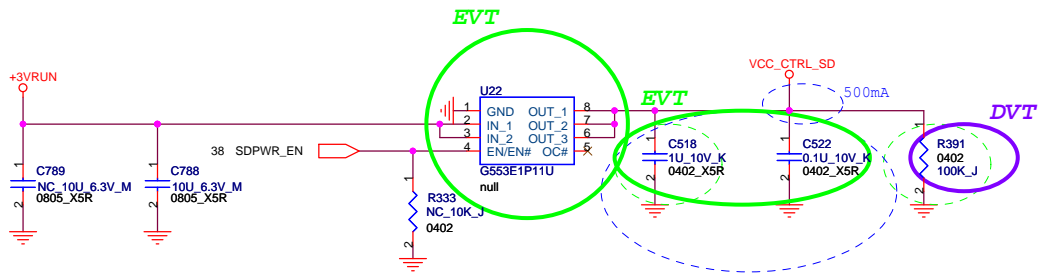
DVT
FOX LN21131-D40L-9H
SLIMLINE SATA_13P



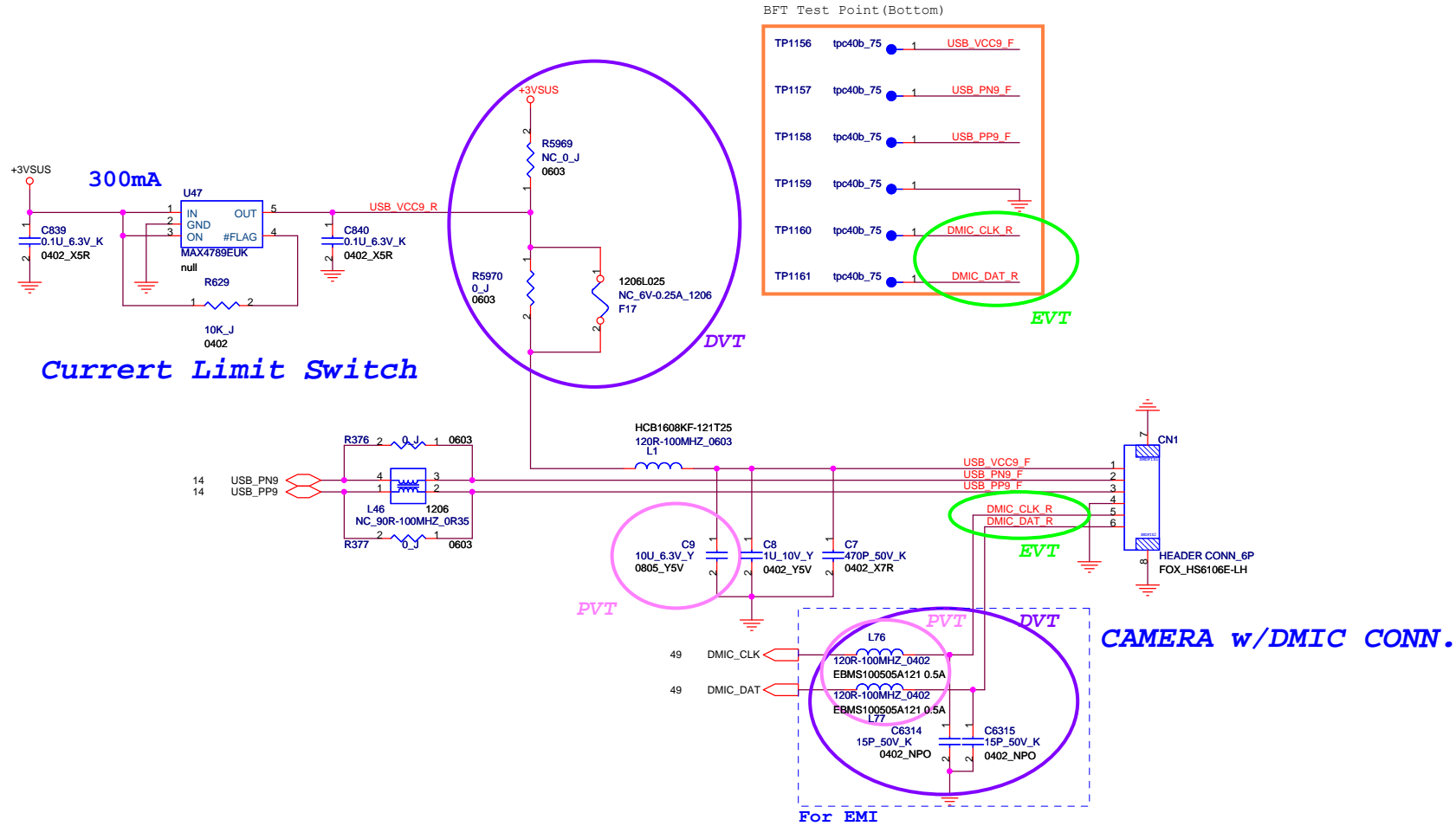
USB + eSATA on MB

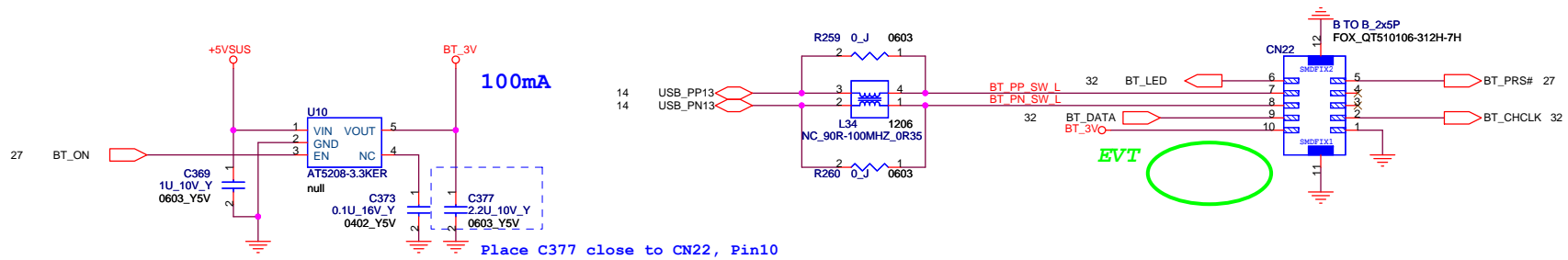






FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title PCIE (SD) 2/2		CCPBG - R&D Division	
Size	Document Number	Rev	
Custom	M960&M970 L Model	SA	
Date:	Tuesday, December 29, 2009	Sheet	39 of 73





Bluetooth CONN.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Bluetooth Connector			
Size	Document Number	Rev	
Custom	M960&M970 L Model	SA	
Date:	Tuesday, December 29, 2009	Sheet	41 of 73

Current Limit Switch

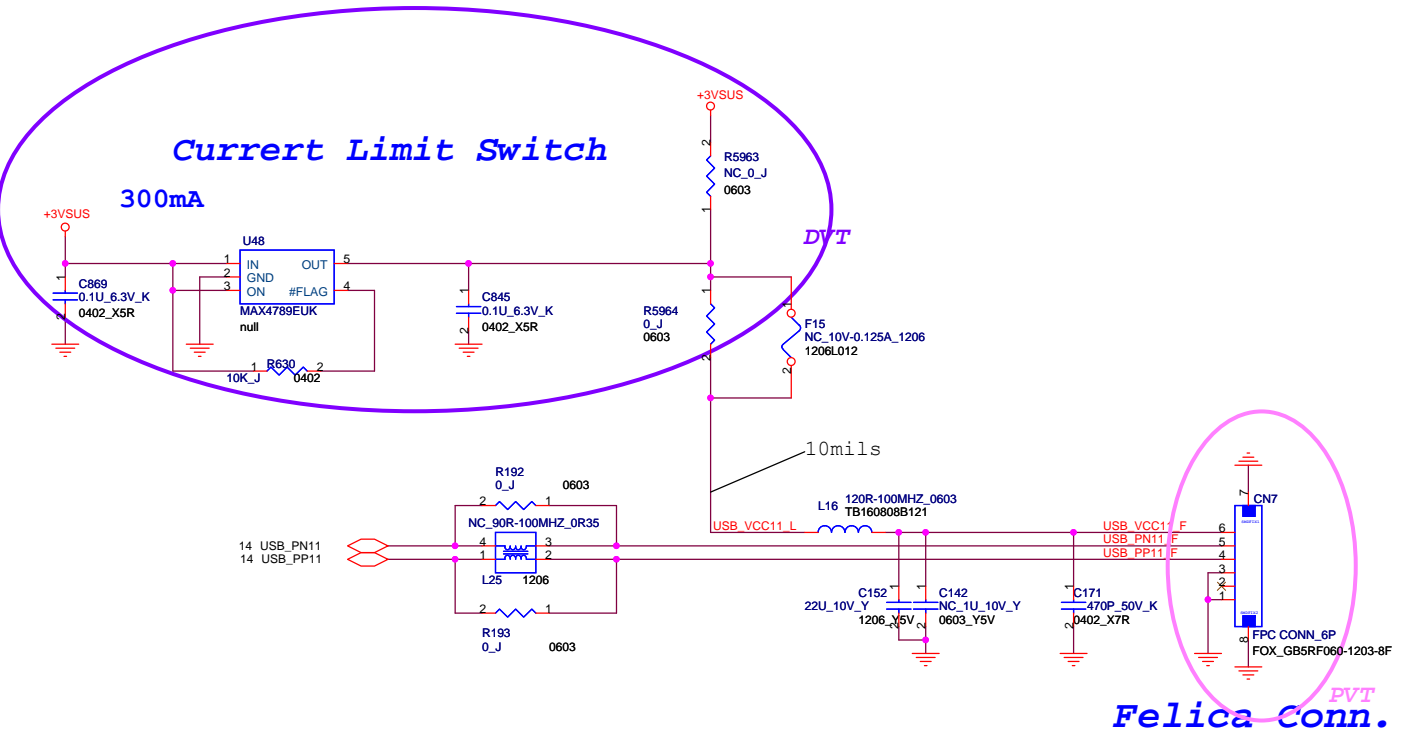
300mA

DVT

Felica Conn.

PVT

Felica Vdd Spec. (3.15V to 3.45V)



Power Test Test Point (Top)

Power Test Test Point (Top)

Power Test Test Point (Top)

BFT Test Point (Top) PVT

TP1227 tpc60t_100 1 WIRELESS_LED_TP

TP1224 tpc60t_100 1 CHARGE_LED
TP1228 tpc60t_100 1 CHARGE_LED_TP

TP1225 tpc60t_100 1 SATA_LED#
TP1229 tpc60t_100 1 SATA_LED#_TP

TP1226 tpc60b_100 1 SD_MS_LED#
TP1230 tpc60b_100 1 SD_MS_LED#_TP

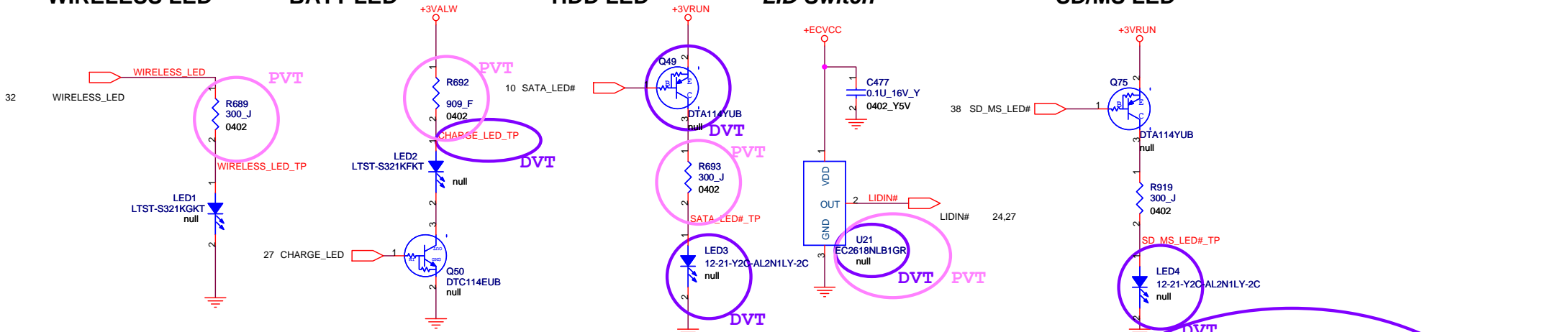
WIRELESS LED

BATT LED

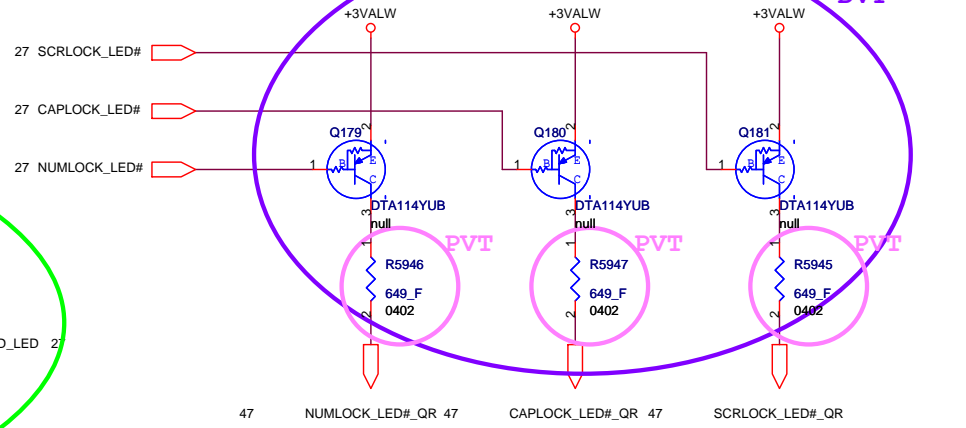
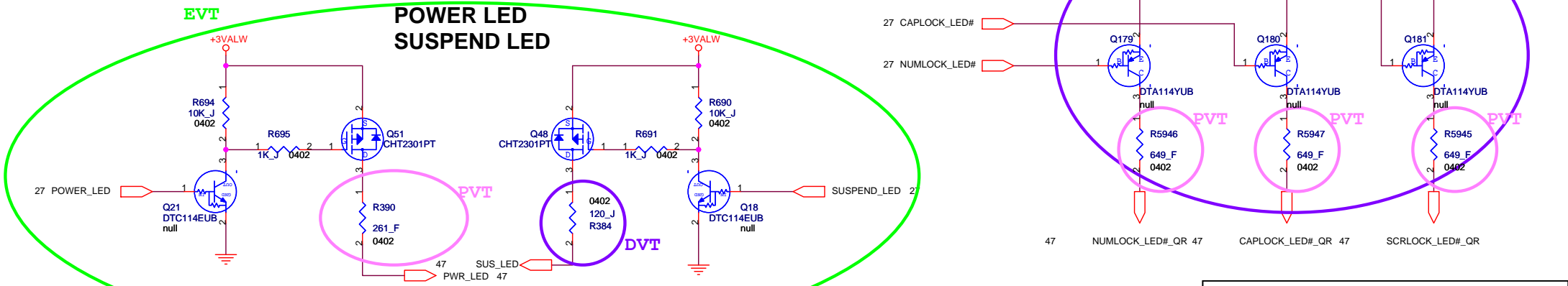
HDD LED

LID Switch

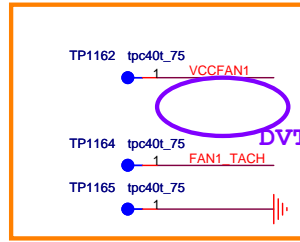
SD/MS LED



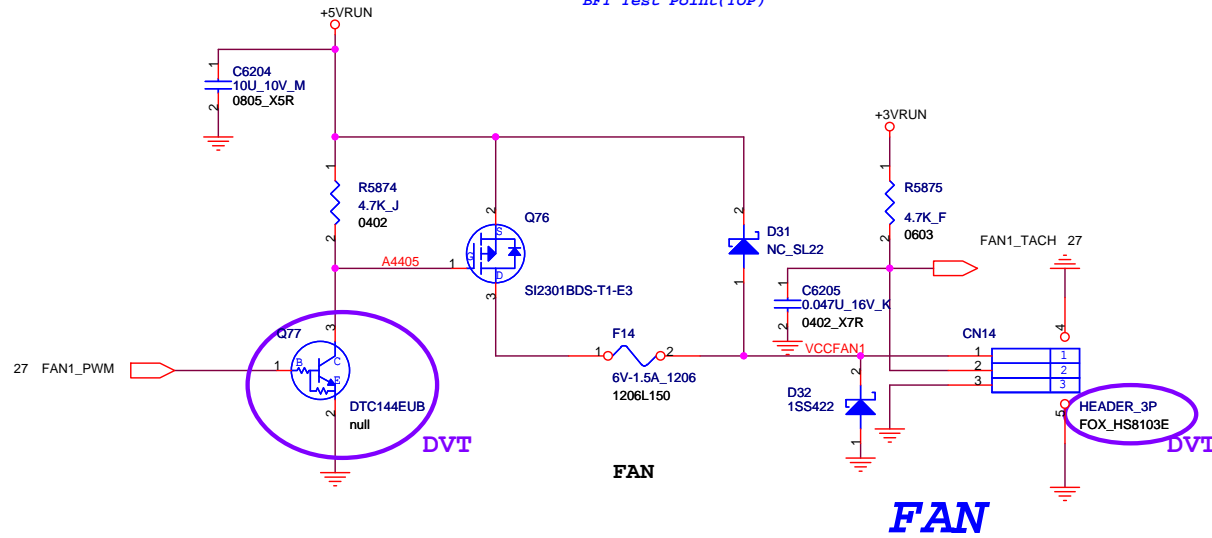
POWER LED SUSPEND LED



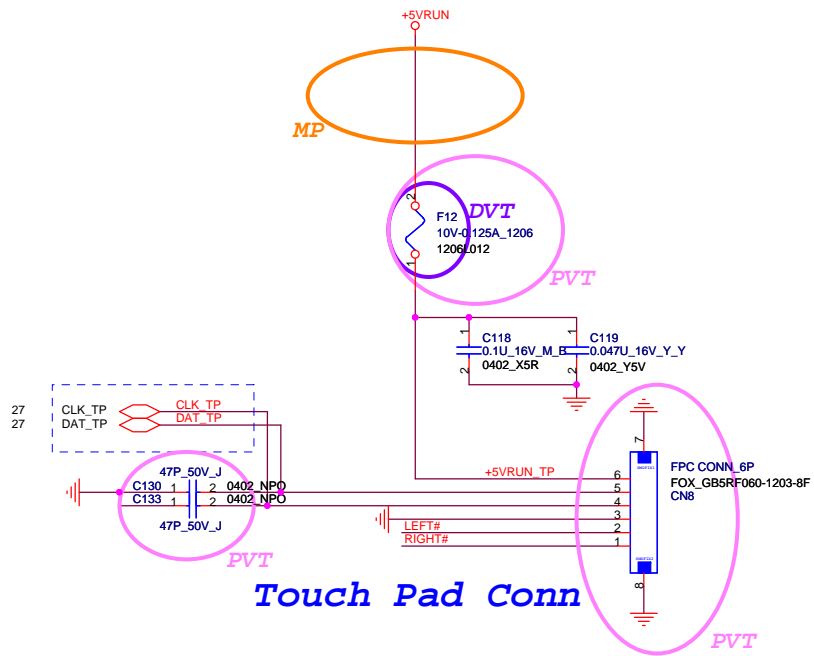
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Status LED & LID			
Size	Document Number		Rev
B	M960&M970 L Model		SA
Date:	Tuesday, December 29, 2009	Sheet	43 of 73



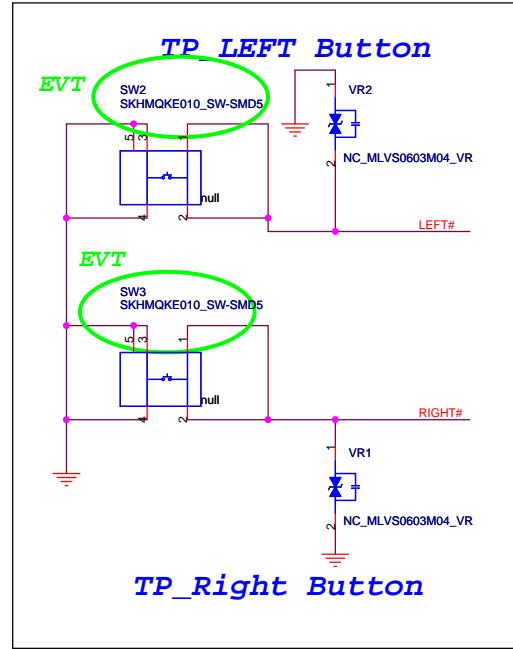
BFT Test Point(TOP)



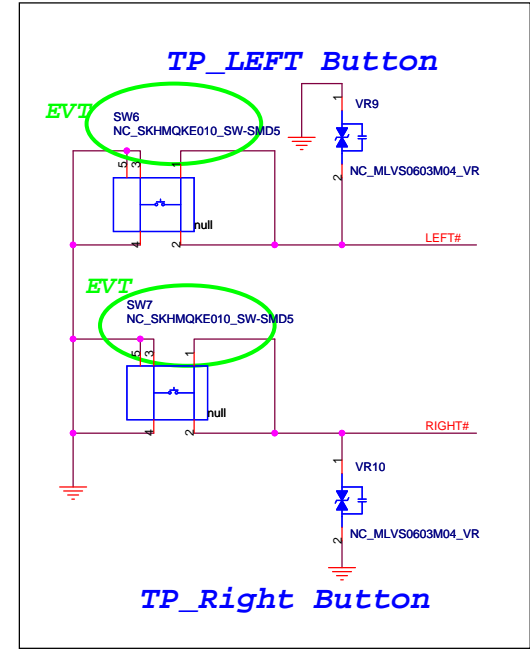
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN		
Size	Document Number		Rev
B	M960&M970 L Model		SA
Date:	Tuesday, December 29, 2009	Sheet	44 of 73



Touch Pad Conn



For M960 Only

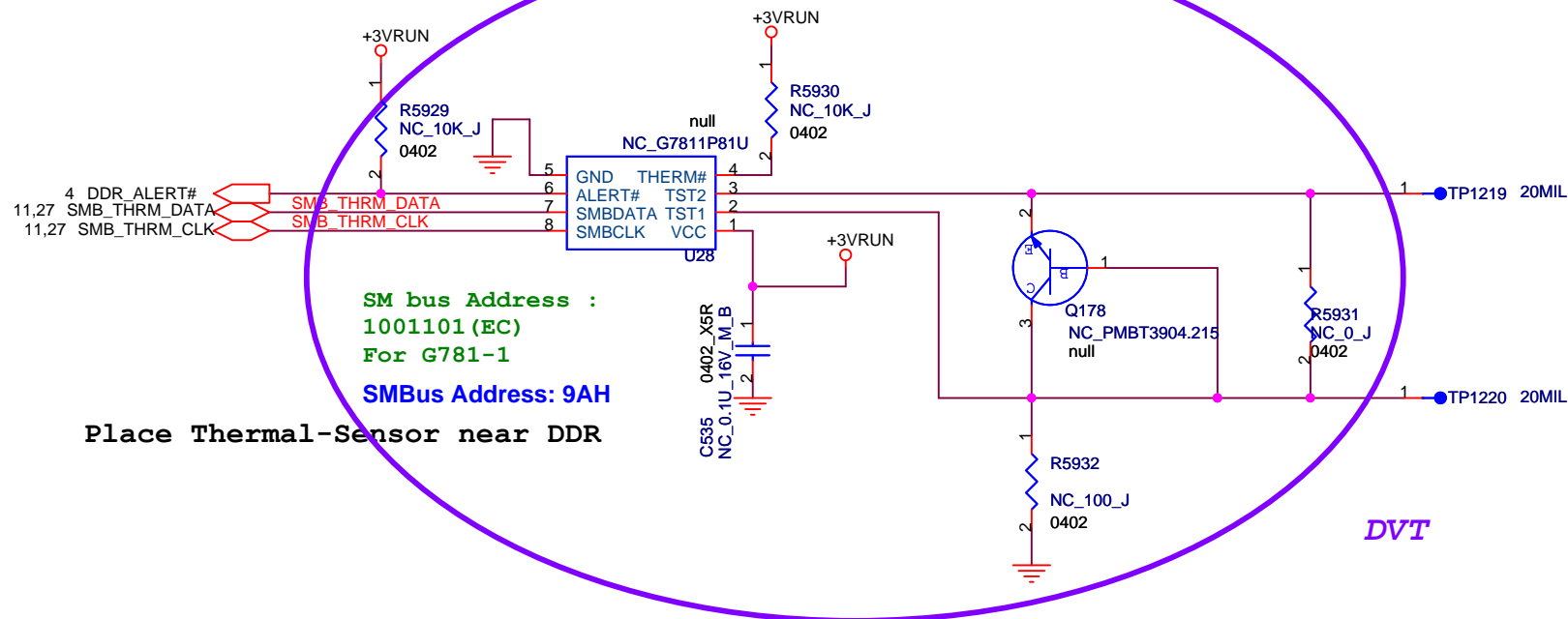


For M970 Only

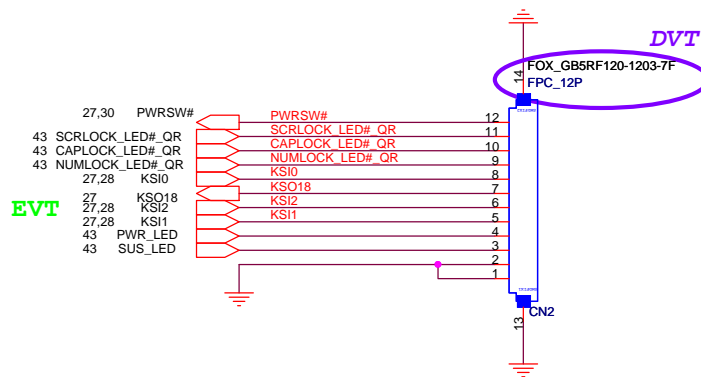
M960/M970 T/P Control Table

	SW2	SW3	SW6	SW7				
M960	Stuff	Stuff	Dummy	Dummy				
M970	Dummy	Dummy	Stuff	Stuff				

DDR Thermal SENSOR G781-1

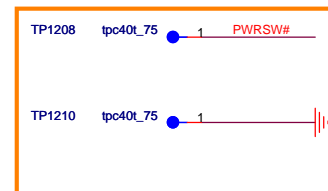


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Thermal Sensor & Protection			
Size A4	Document Number M960&M970 L Model	Rev SA	
Date: Tuesday, December 29, 2009	Sheet 46	of	73

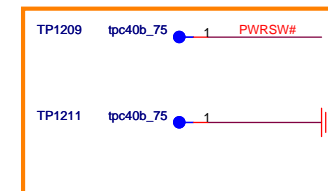


Switch DB Conn.

BFT Test Pad(Top)

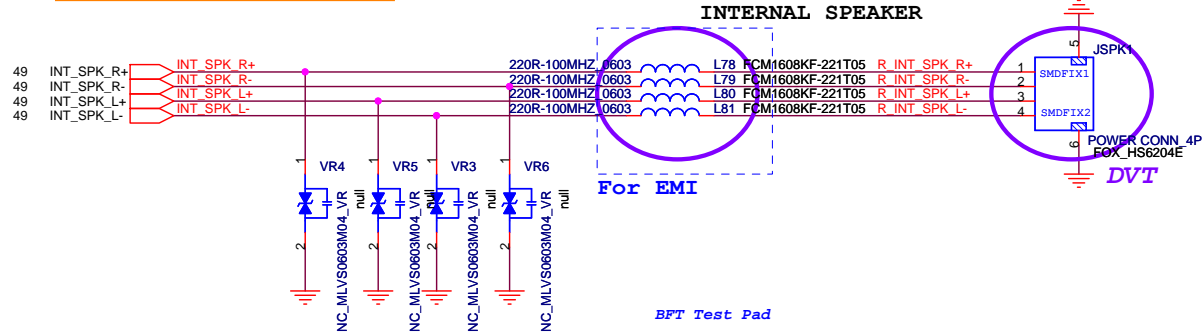


BFT Test Pad(Bottom)

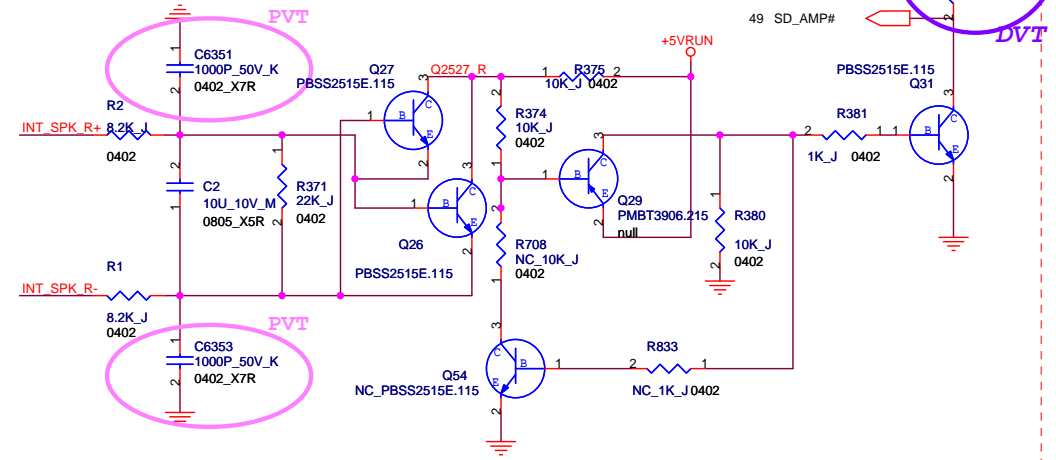
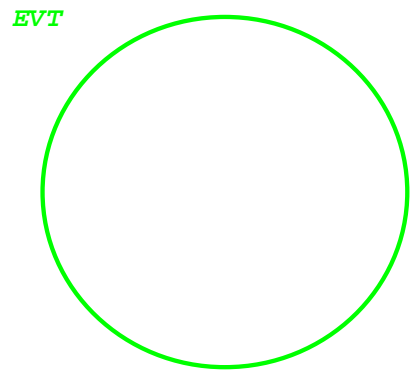
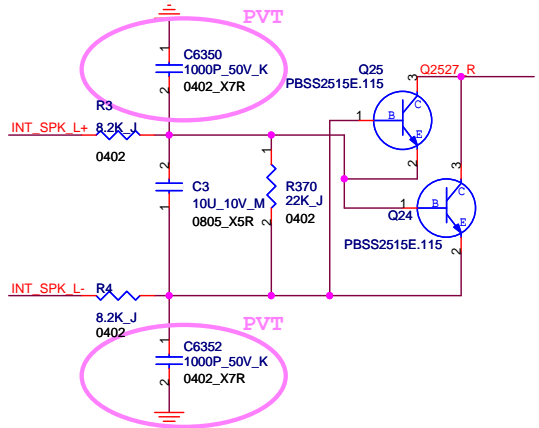


BFT Test Pad(Bottom)

TP1194	tpc40b_75	1	R_INT_SPK_R-
TP1195	tpc40b_75	1	R_INT_SPK_R+
TP1196	tpc40b_75	1	R_INT_SPK_L-
TP1197	tpc40b_75	1	R_INT_SPK_L+

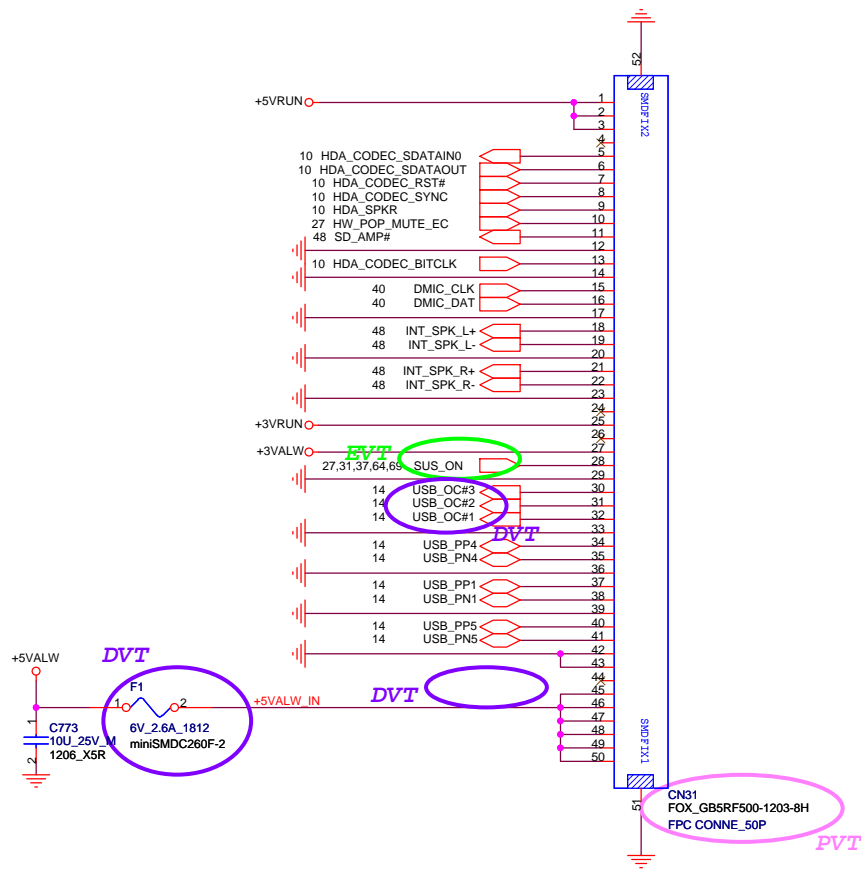


If use ALC275 Codec, for Shut-down Codec Amp. power (PVDD1 and PVDD2)

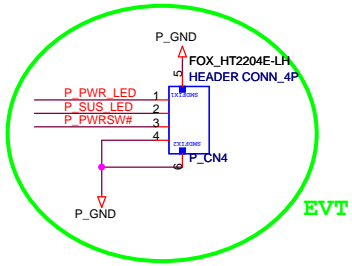


For Mor request, add the speaker cable short protection circuit

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	AUDIO SPEAKER CONNECTOR		
Size	Document Number		Rev
B	M960&M970 L Model		SA
Date:	Tuesday, December 29, 2009	Sheet	48 of 73

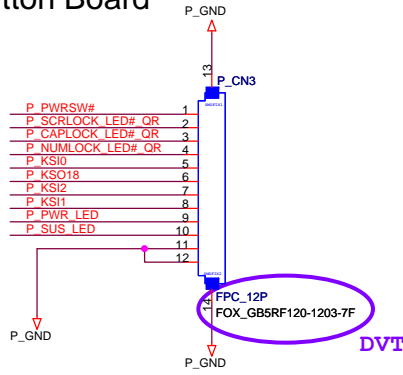


POWER BUTTON



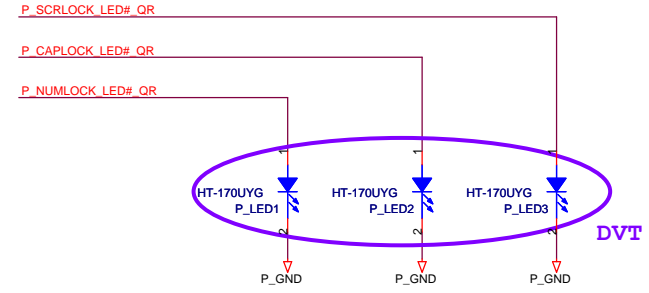
EVT

Power Button Board

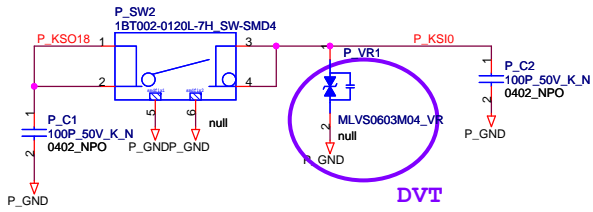


DVT

NUM LOCK LED CAP LED SCROLL LOCK LED



DVT

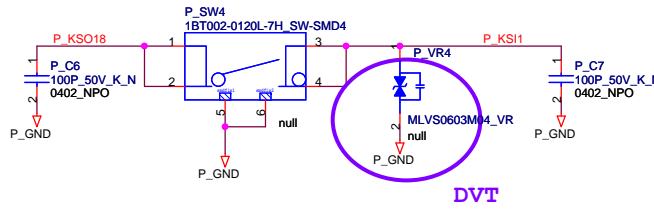


DVT

Assist

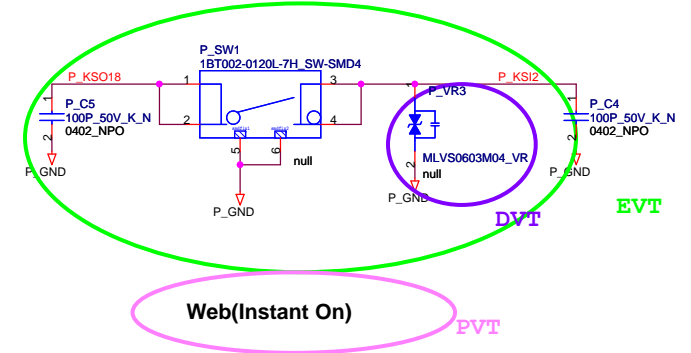
EVT

PVT



DVT

VAIO



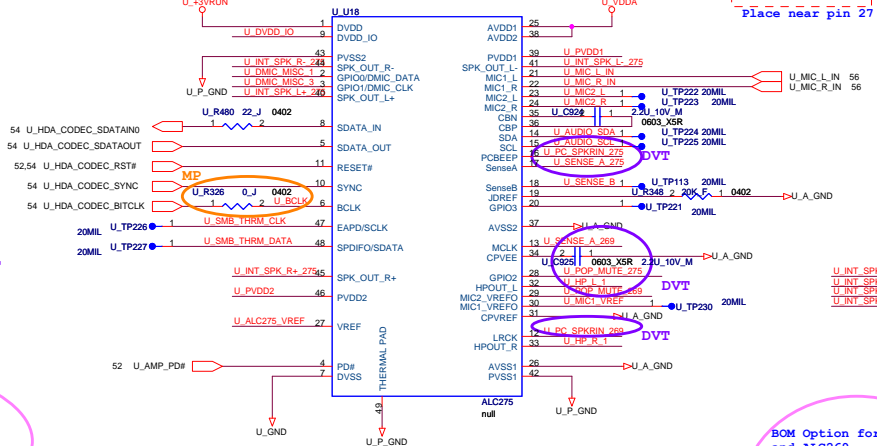
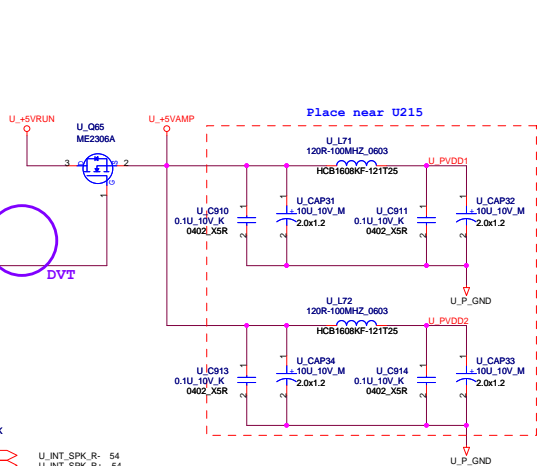
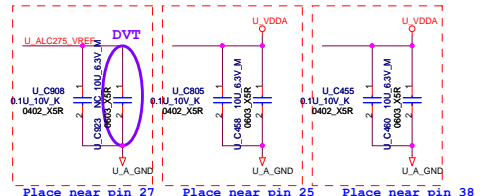
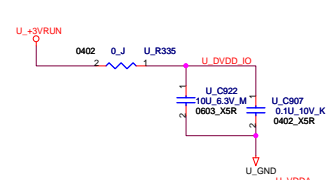
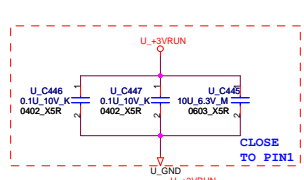
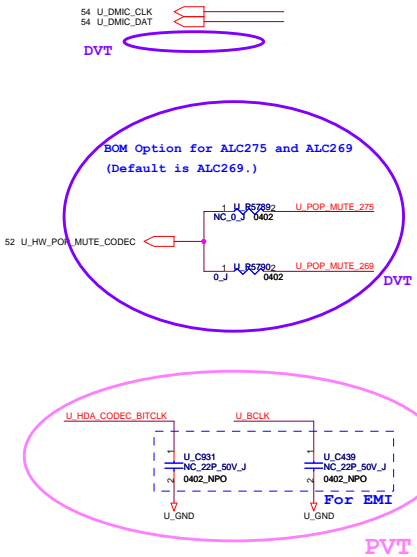
DVT

Web(Instant On)

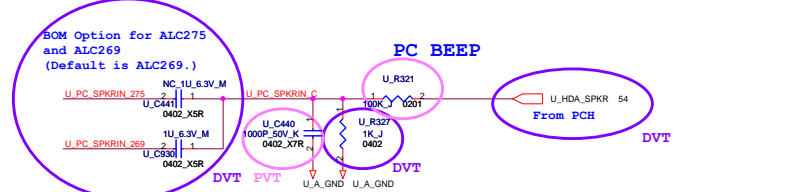
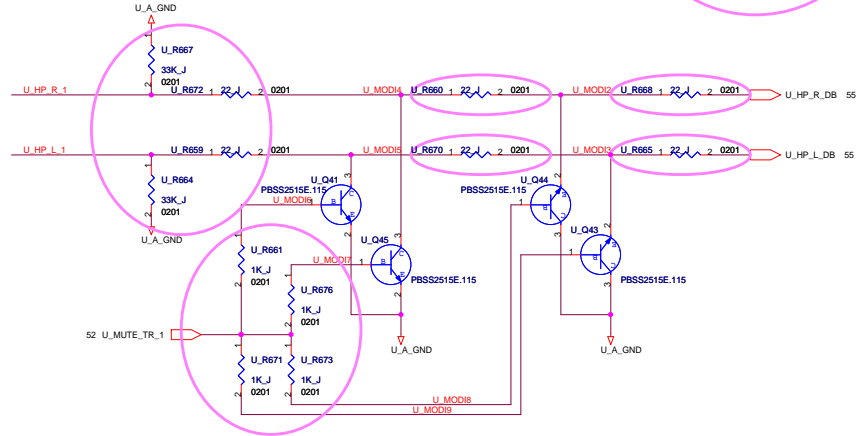
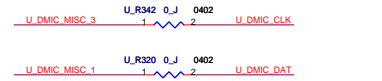
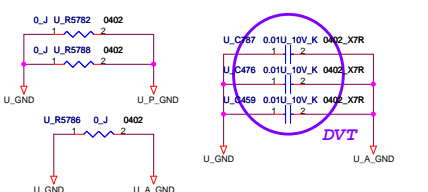
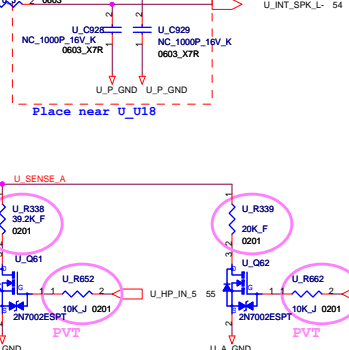
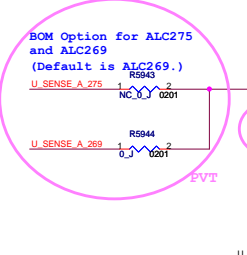
PVT

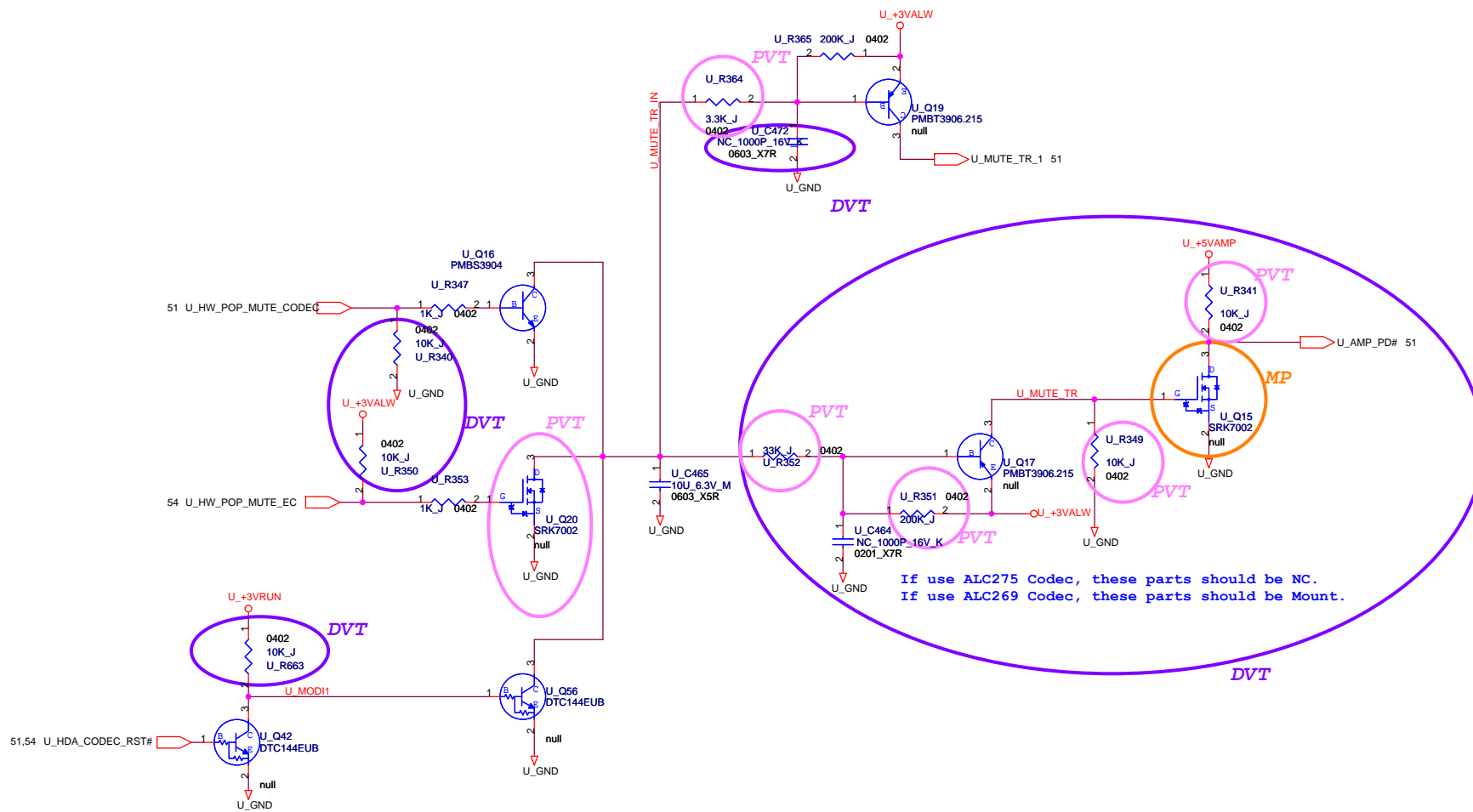
EVT

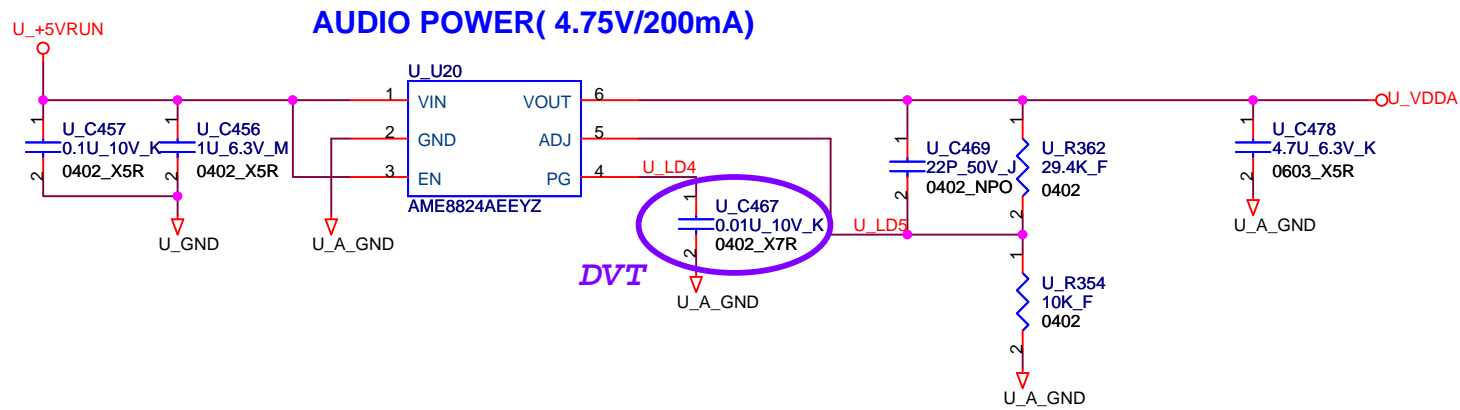
DVDD_IO can be either 1.5V or 3.3V. Resume low power, regardless of HDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHD power.



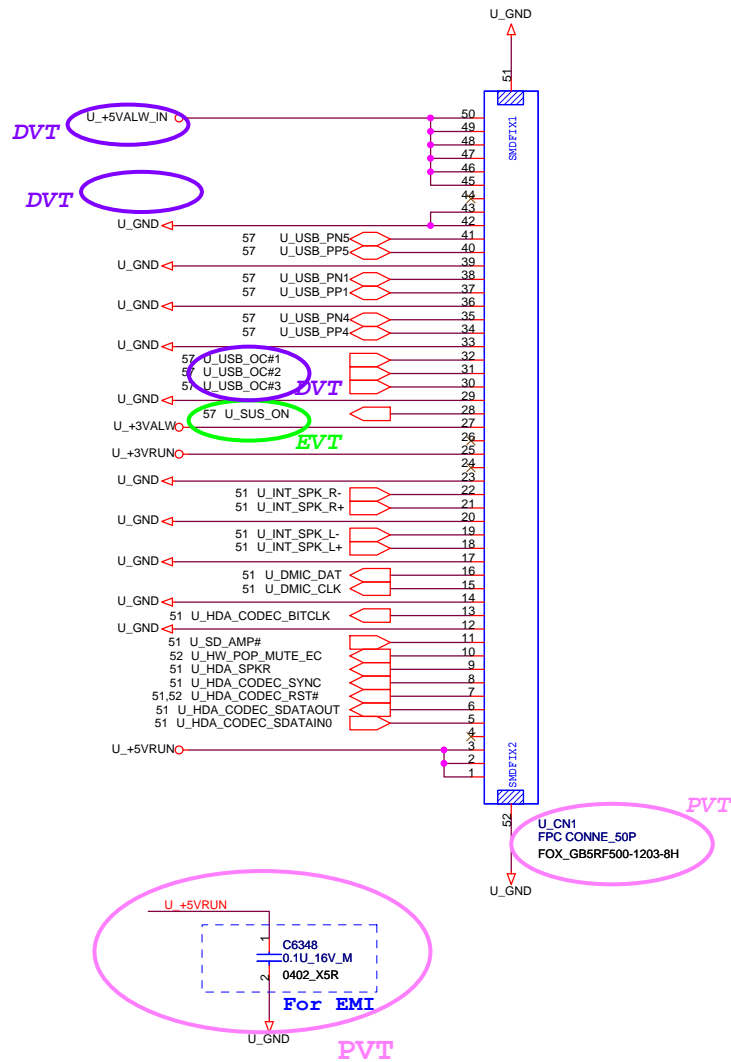
<<Attention>>
For power on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note:
1. If you want the system make warning signal after power on, please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before.)

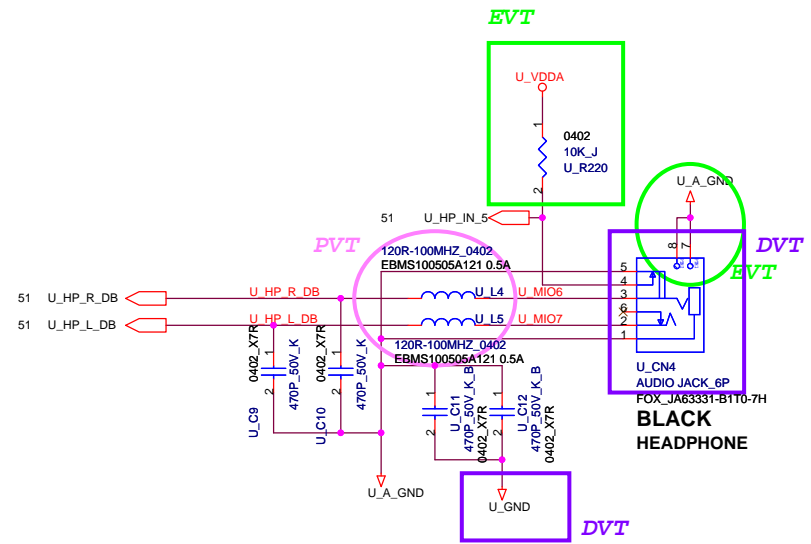


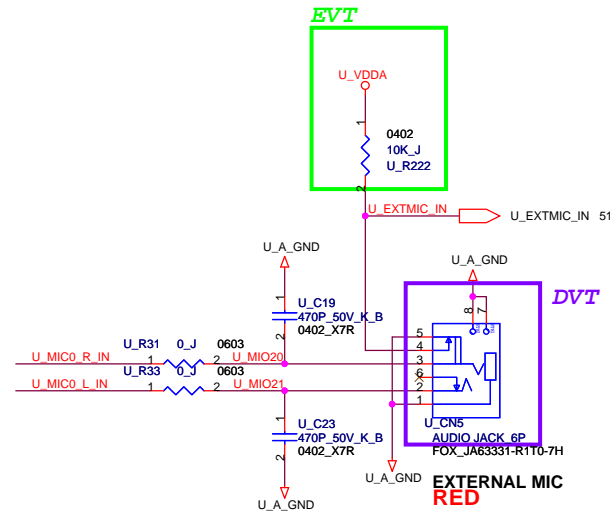
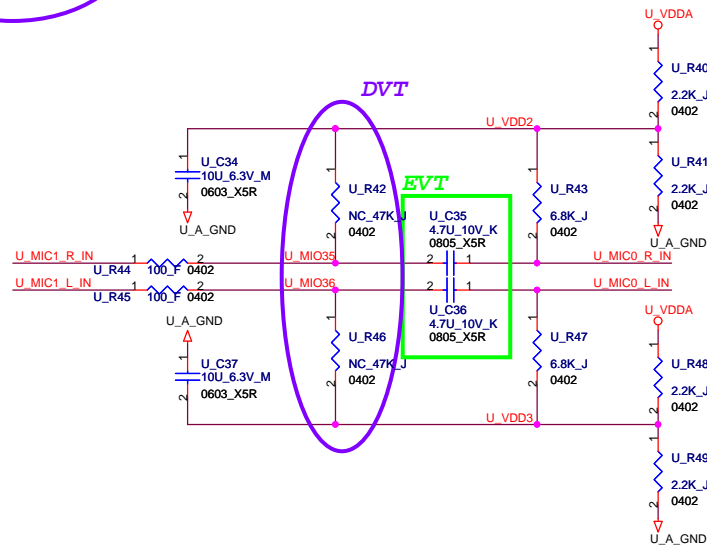
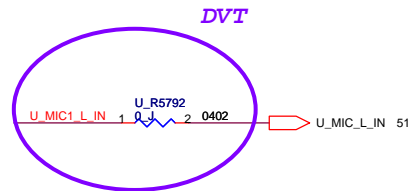
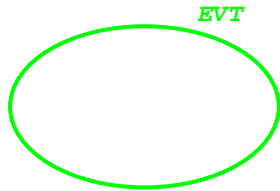
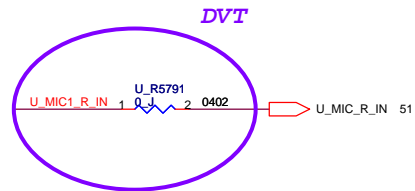
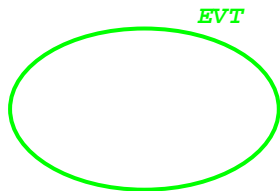


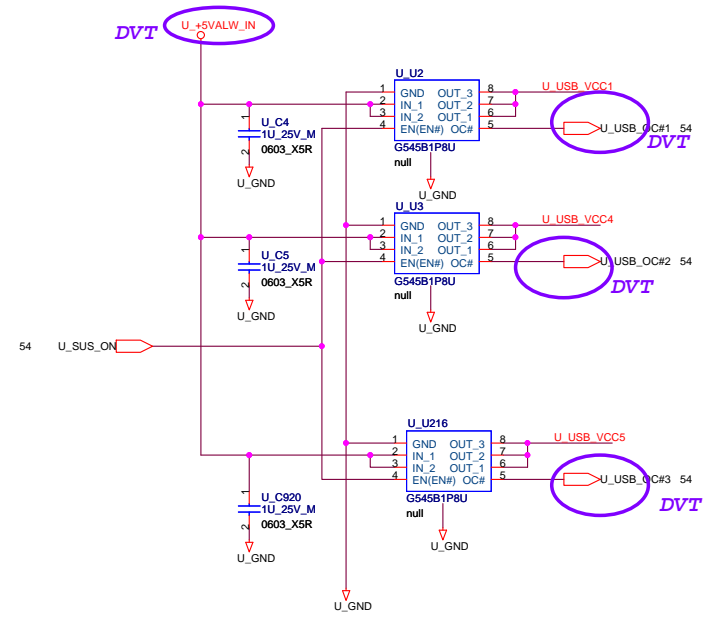
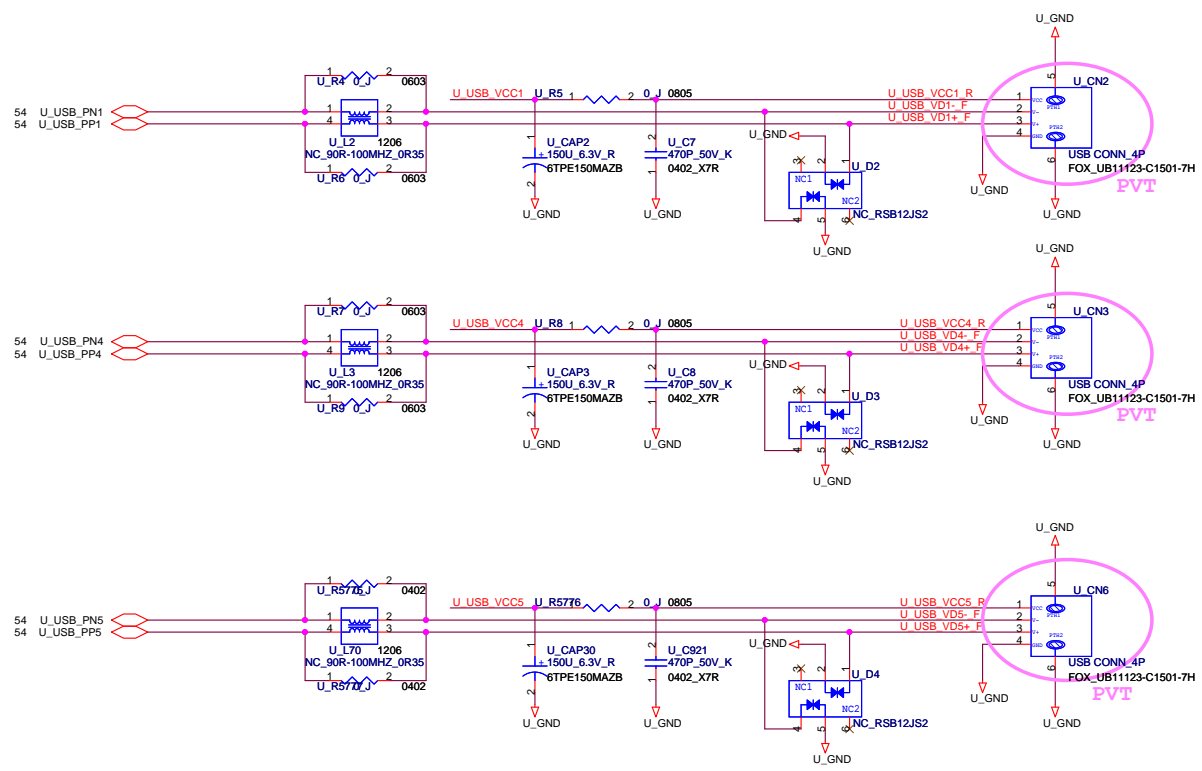


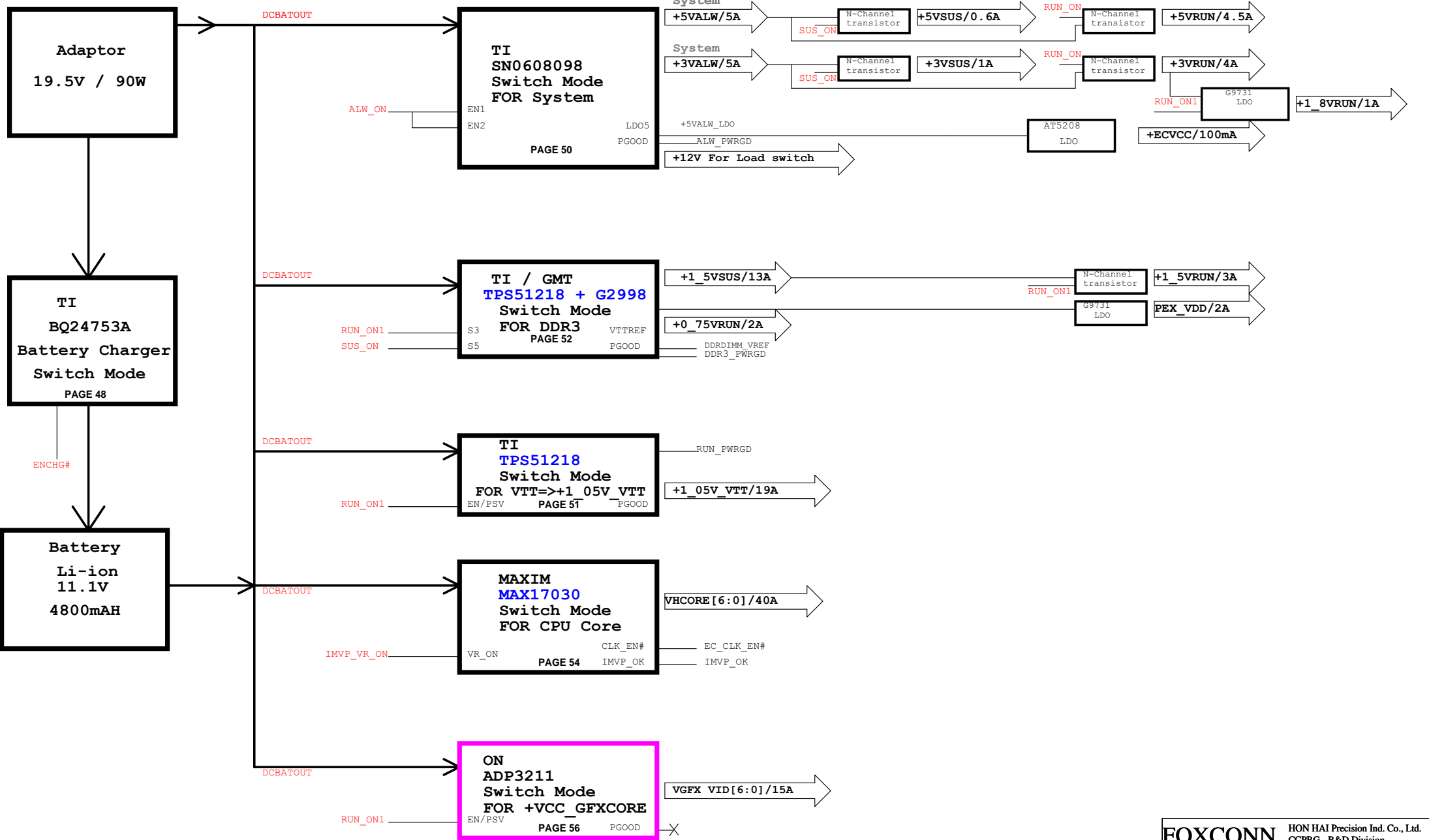
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title AUDIO POWER			
Size	Document Number		Rev
A4	M960&M970 L Model		SA
Date:	Thursday, December 24, 2009	Sheet	53 of 73





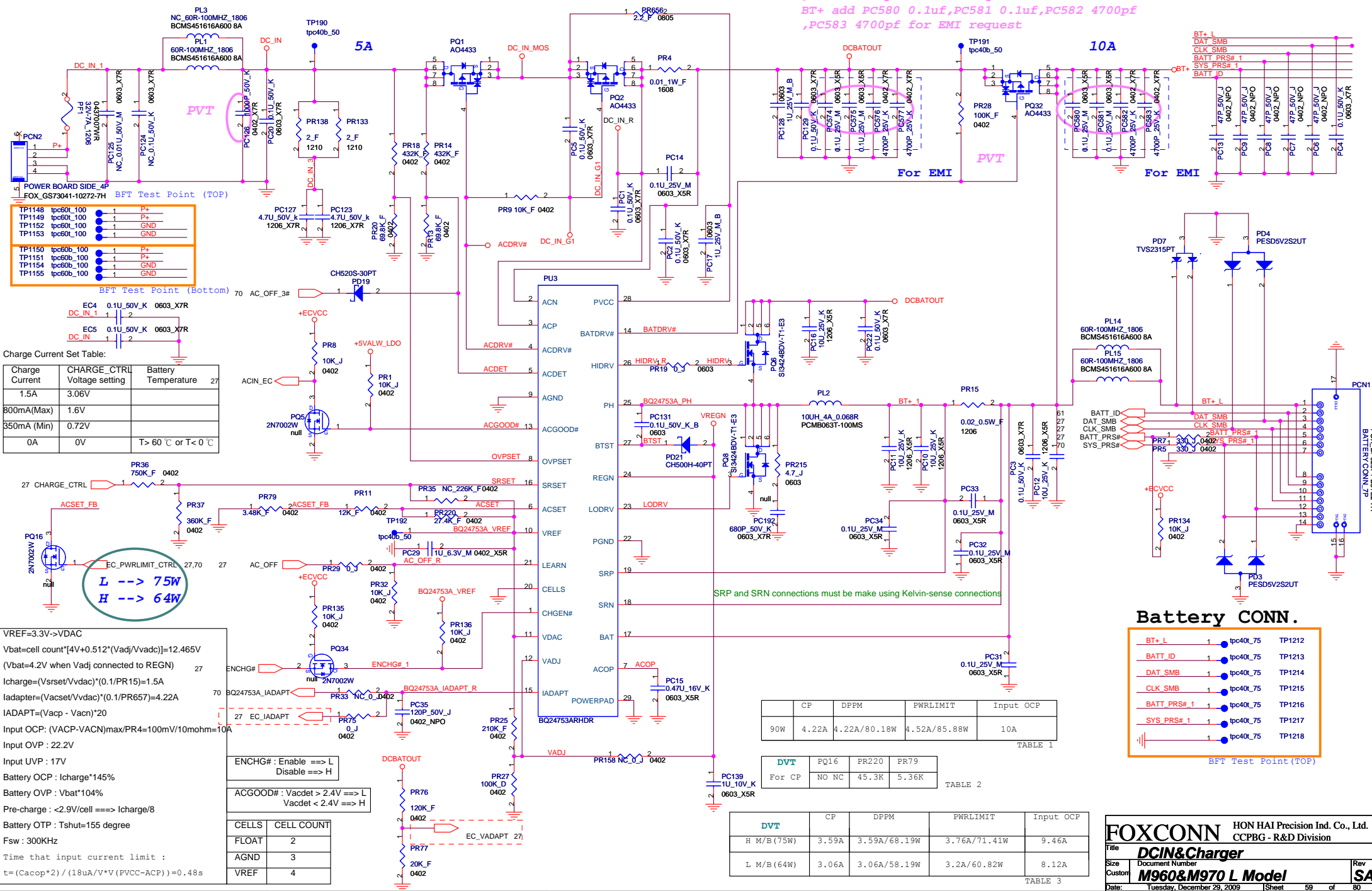






ACP and ACN connections must be make using Kelvin-sense connections

09/11/21 Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf
 ,PC577 4700pf for EMI request
 BT+ add PC580 0.1uf,PC581 0.1uf,PC582 4700pf
 ,PC583 4700pf for EMI request



BFT Test Point (TOP)

TP1148	tpc60L_100	1	P+
TP1149	tpc60L_100	1	P+
TP1152	tpc60L_100	1	GND
TP1153	tpc60L_100	1	GND
TP1150	tpc60L_100	1	P+
TP1151	tpc60L_100	1	P+
TP1154	tpc60L_100	1	GND
TP1155	tpc60L_100	1	GND

BFT Test Point (Bottom)

TP1148	tpc60L_100	1	P+
TP1149	tpc60L_100	1	P+
TP1152	tpc60L_100	1	GND
TP1153	tpc60L_100	1	GND
TP1150	tpc60L_100	1	P+
TP1151	tpc60L_100	1	P+
TP1154	tpc60L_100	1	GND
TP1155	tpc60L_100	1	GND

Charge Current Set Table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
800mA(Max)	1.6V	
350mA (Min)	0.72V	
0A	0V	T > 60 °C or T < 0 °C

L ---> 75W
H ---> 64W

VREF=3.3V->VDAC
 $V_{bat} = cell\ count * [4V + 0.512 * (V_{adj} / V_{vdac})] = 12.465V$
 (Vbat=4.2V when Vadj connected to REGN)
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR15) = 1.5A$
 $I_{adapter} = (V_{vacset} / V_{vdac}) * (0.1 / PR657) = 4.22A$
 $I_{ADAPT} = (V_{vacp} - V_{vacn}) * 20$
 Input OCP: $(V_{ACP} - V_{ACN}) / max(PR4) = 100mV / 10mohm = 10A$
 Input OVP: 22.2V
 Input UVP: 17V
 Battery OCP: $I_{charge} * 145\%$
 Battery OVP: $V_{bat} * 104\%$
 Pre-charge: $< 2.9V / cell ==> I_{charge} / 8$
 Battery OTP: $T_{shut} = 155\ degree$
 Fsw: 300KHz
 Time that input current limit :
 $t = (C_{acop} * 2) / (18uA / V * (PVCC - ACP)) = 0.48s$

ENCHG# : Enable ==> L
 Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
 Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

CP	DPPM	PWRLIMIT	Input OCP	
90W	4.22A	4.22A/80.18W	4.52A/85.88W	10A

TABLE 1

DVT	PQ16	PR220	PR79
For CP	NO NC	45.3K	5.36K

TABLE 2

DVT	CP	DPPM	PWRLIMIT	Input OCP
H M/B (75W)	3.59A	3.59A/68.19W	3.76A/71.41W	9.46A
L M/B (64W)	3.06A	3.06A/58.19W	3.2A/60.82W	8.12A

TABLE 3

Battery CONN.

BT+ L	1	tpc40L_75	TP1212
BATT_ID	1	tpc40L_75	TP1213
DAT_SMB	1	tpc40L_75	TP1214
CLK_SMB	1	tpc40L_75	TP1215
BATT_PRS#_1	1	tpc40L_75	TP1216
SYS_PRS#_1	1	tpc40L_75	TP1217
	1	tpc40L_75	TP1218

BFT Test Point (TOP)

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **DCIN&Charger**
 Size: Document Number
 Custom: **M960&M970 L Model**
 Date: Tuesday, December 29, 2019 | Sheet 59 of 80

Rev: **SA**

5

4

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D

D

C

C

B

B

A

A

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title		DISCHARGE CIRCUIT	
Size	Document Number	Rev	
A	M960&M970 L Model	SA	
Date:	Thursday, December 24, 2009	Sheet	60 of 80

5

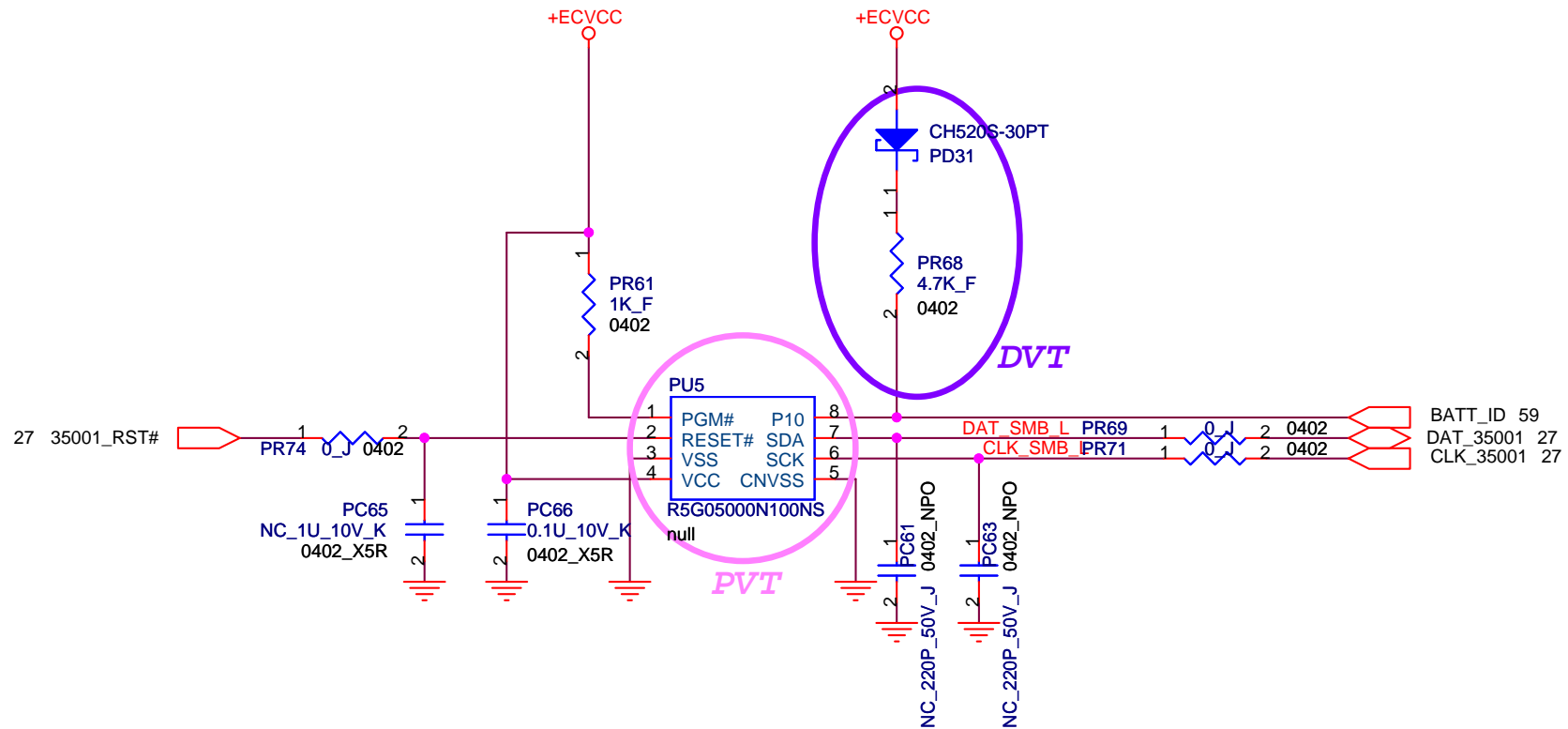
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3

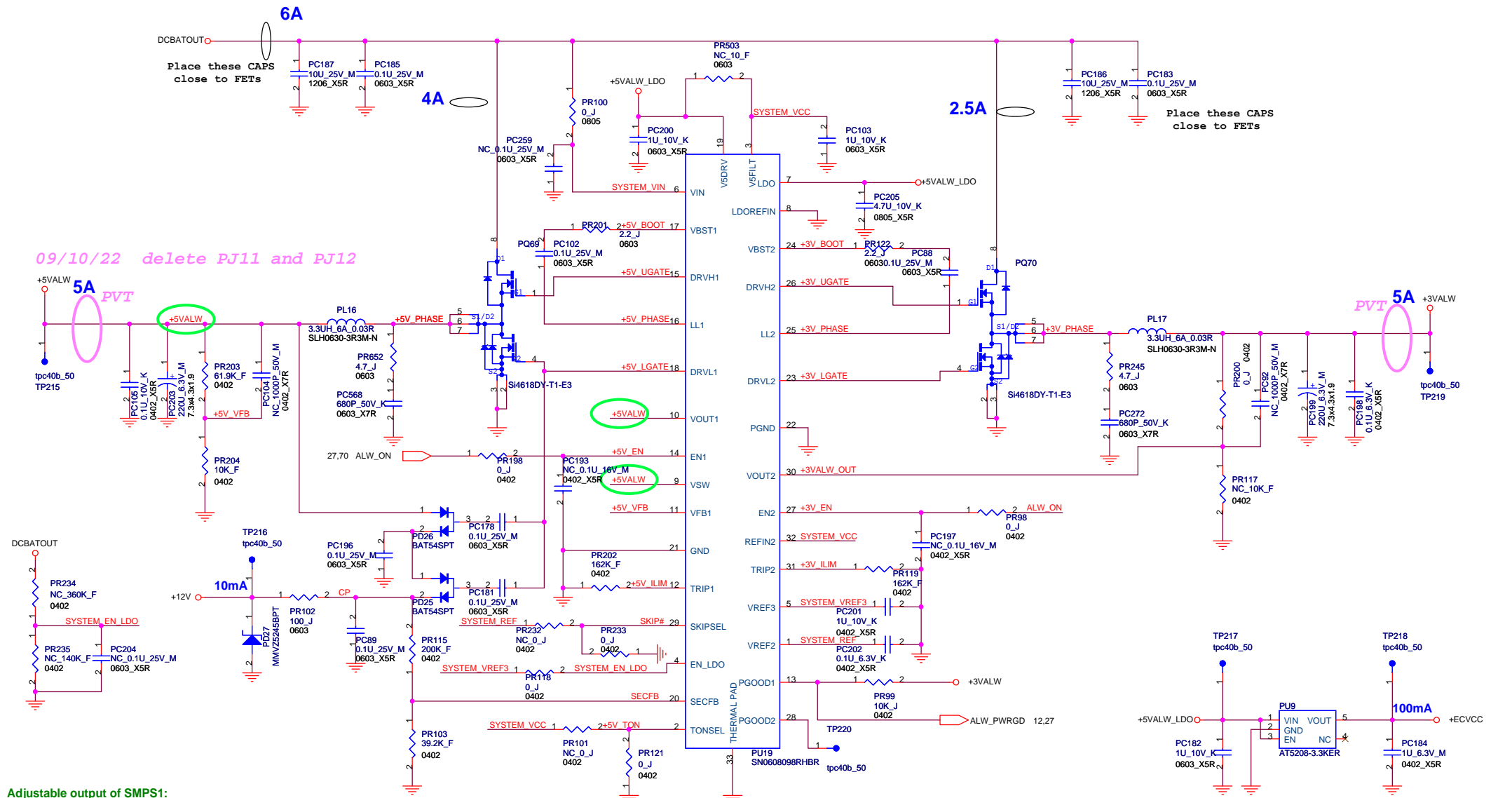
2

1

9/8 Add PD31 and change PR68 to 4.7K for MOR request.



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Identify IC			
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Adjustable output of SMPS1:
 Vout1 = 5.05V
 PR204 = 10K, PR203 = P204 x (Vout1 / 0.7V - 1) = 61.9Kohm

Second Feedback :
 Vout_sec = 12V, PR103 = 20Kohm
 PR115 = PR103 x (Vout_sec / 2V - 1) = 100Kohm

$$L = VOUT (VIN - VOUT) / (VIN * f * LIR * ILOAD (MAX))$$

$$Rocp = (Iocp - Iripple / 2) * (10 * Rds (on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) * VFB1$$

Current limit resistor for SMPS1 :
 Ivalley_5 = 5.775A, Rcs_5 = Rds1 = 10.8mohm
 PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

Current limit resistor for SMPS2 :
 Ivalley_3 = 5.525A, Rcs_3 = Rds2 = 10.8mohm
 PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

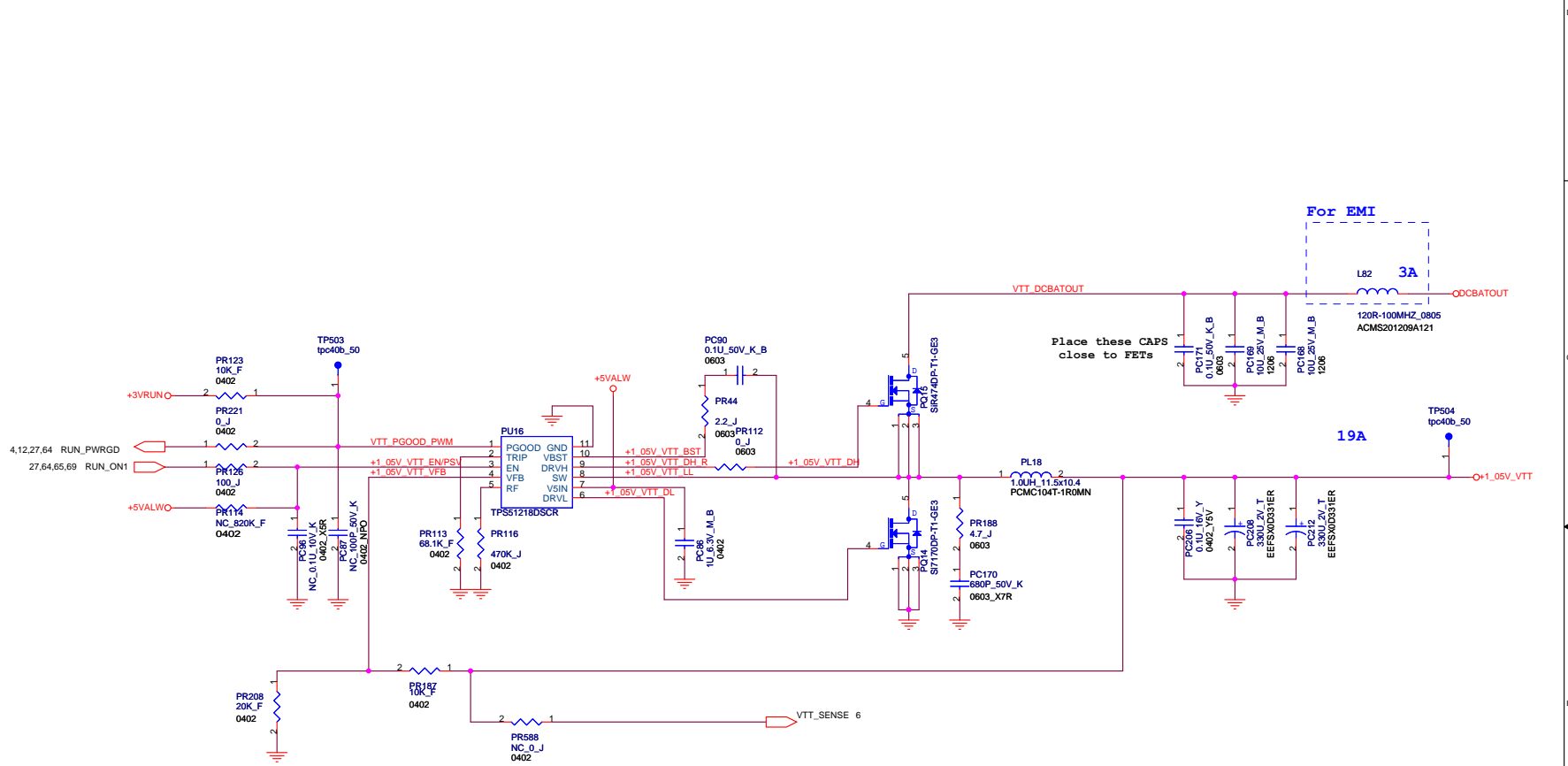
SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **SYS Power (+3 3V/+5V)**

Size: Document Number
 A3: **M960&M970 L Model** Rev: **SA**

Date: Tuesday, December 29, 2009 Sheet: 62 of 80

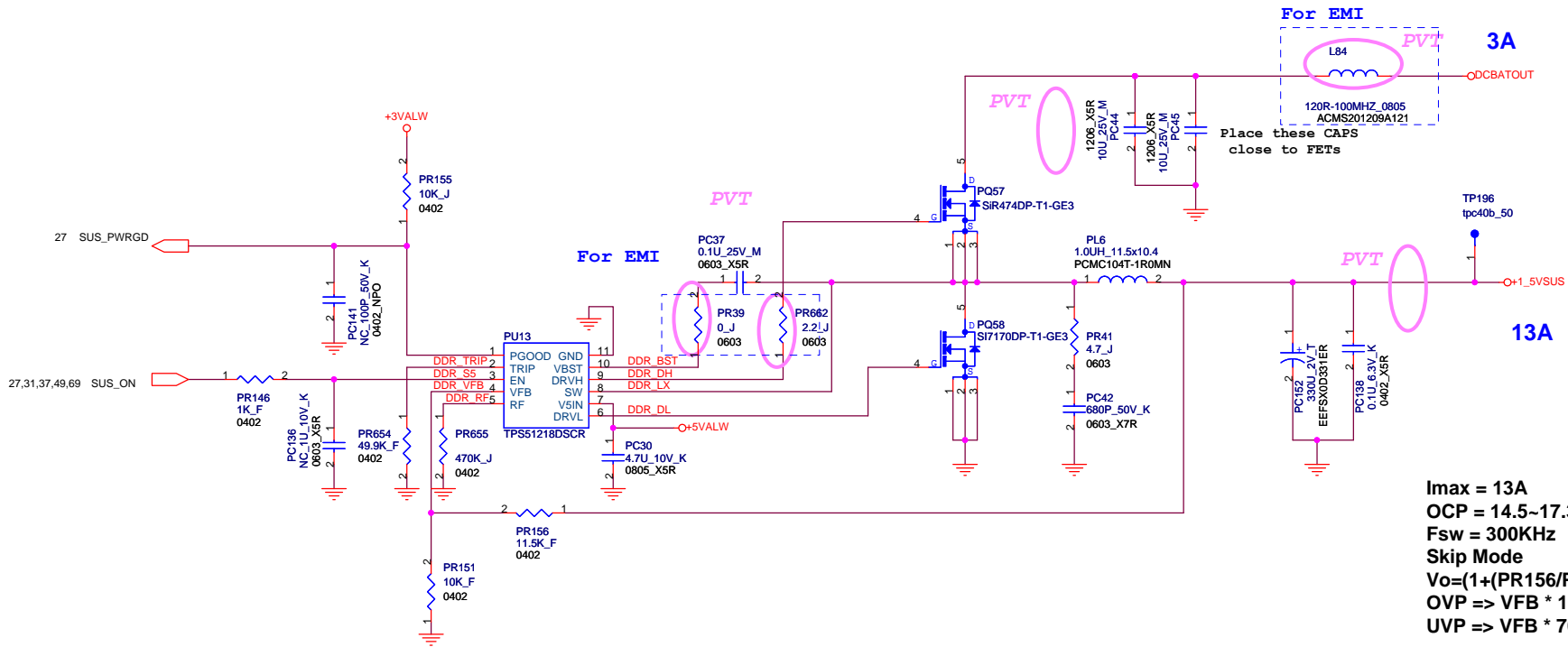


I_{max} = 19A
F_{sw} = 390KHz
Skip Mode
 $V_o = (1 + (PR187/PR208)) * 0.704 = 1.05V$
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

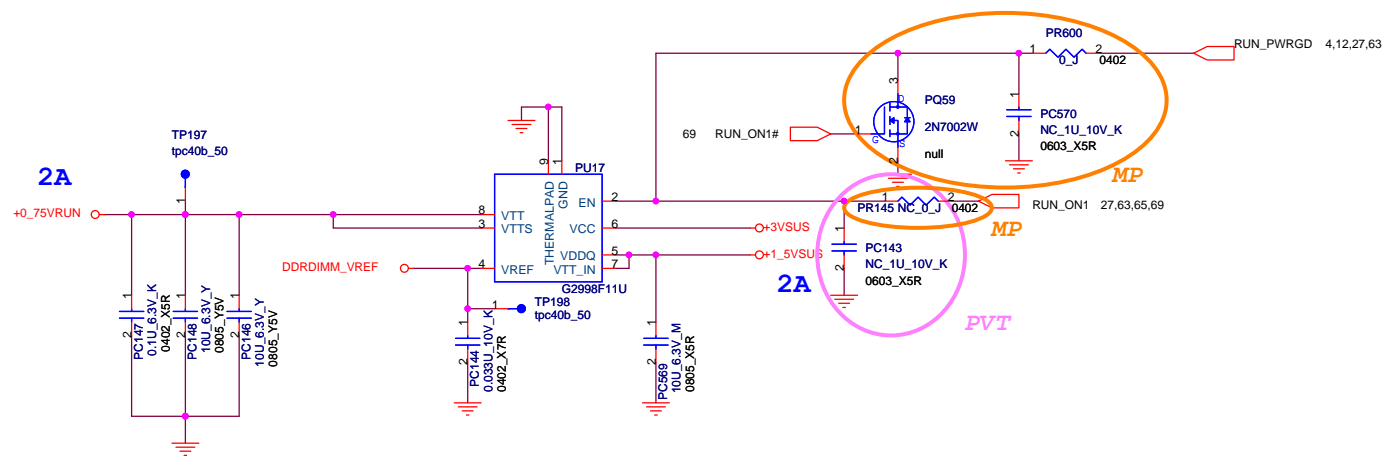
For EMI
 L82 3A
 120R-100MHZ_0805
 ACMS201209A121
 Place these CAPS close to FETs

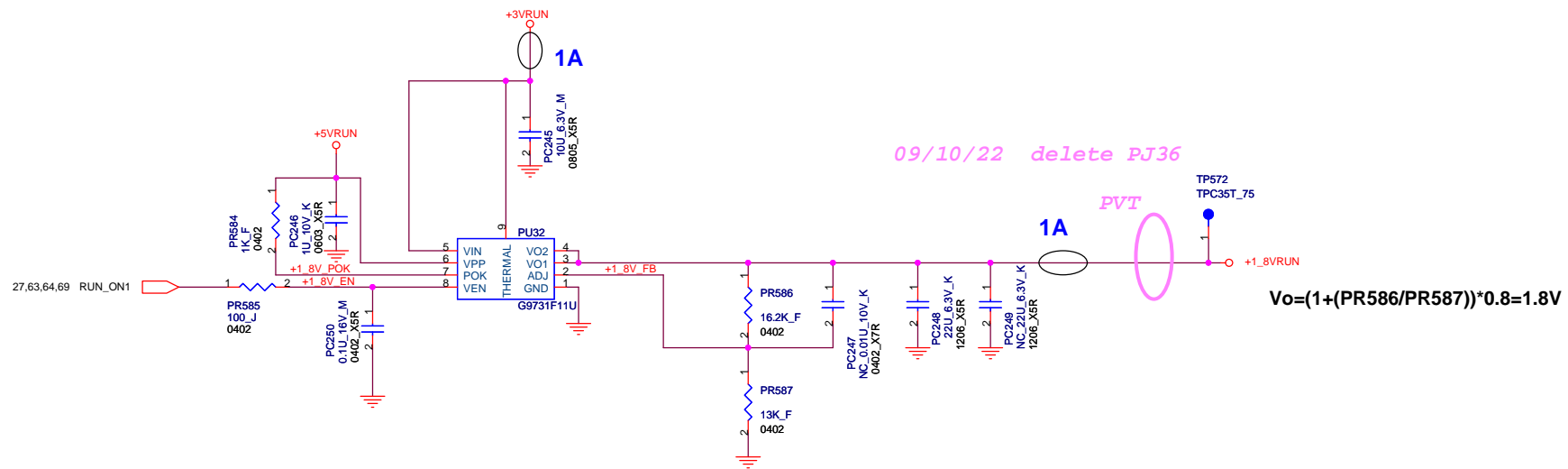
19A



Imax = 13A
OCP = 14.5~17.32A
Fsw = 300KHz
Skip Mode
 $V_o = (1 + (PR156/PR151)) * 0.704 = 1.514V$
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz





09/11/21 change PC151 and PC156 from NC to no NC for EMI request

Placement TOP and BOTTOM Overlapped

Place these CAPS close to FETs

4A

OCBATOUT

40A

OVHCORE

Placement TOP and BOTTOM Overlapped

Place these CAPS close to FETs

4A

DCBATOUT

PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI

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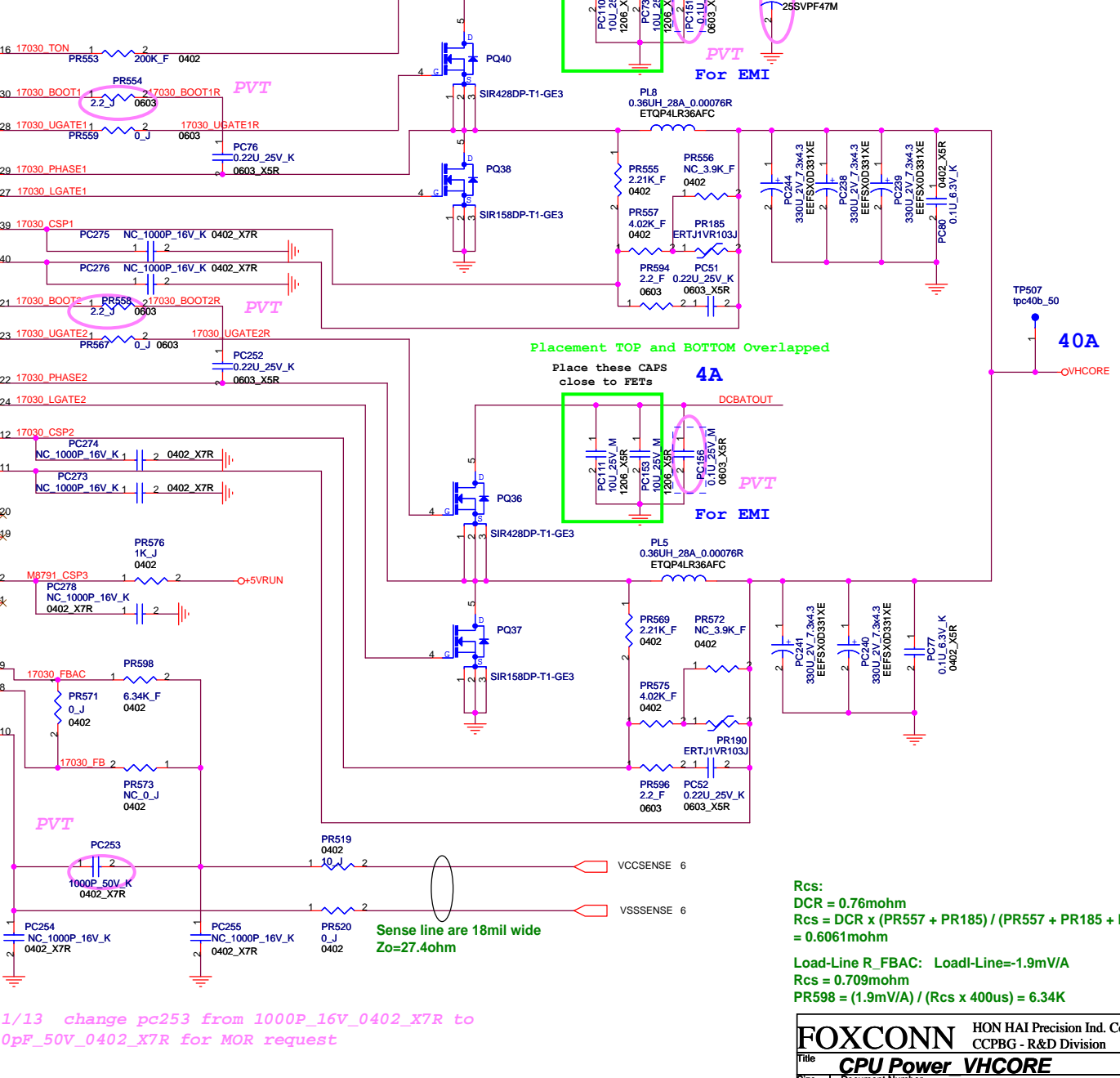
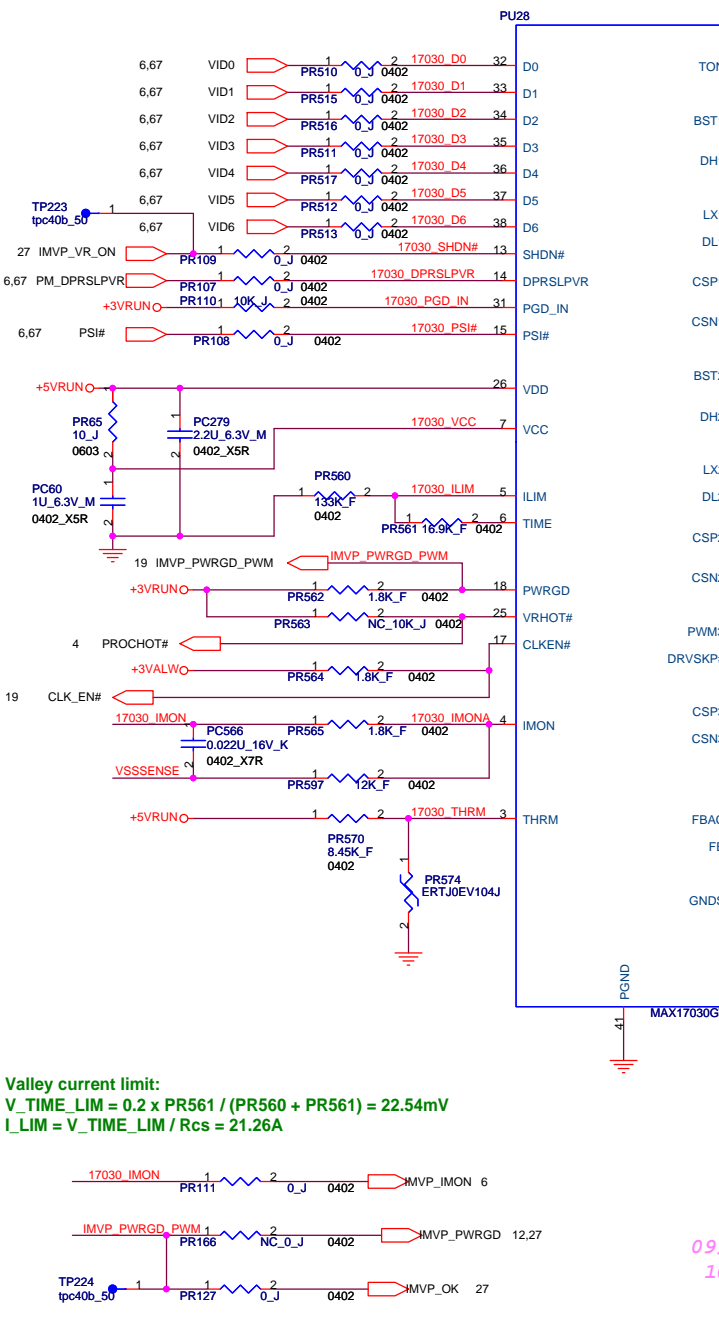
PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI

PVT For EMI



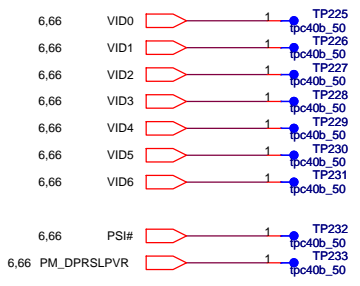
Valley current limit:
 $V_TIME_LIM = 0.2 \times PR561 / (PR560 + PR561) = 22.54mV$
 $I_LIM = V_TIME_LIM / Rcs = 21.26A$

Sense line are 18mil wide
 $Z_o = 27.4ohm$

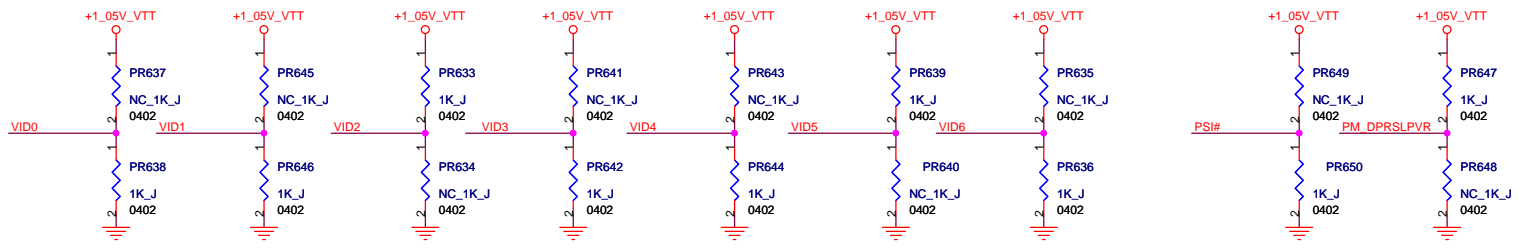
Rcs:
 $DCR = 0.76mohm$
 $Rcs = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.6061mohm$
 Load-Line R_FBAC: Load-Line=1.9mV/A
 $Rcs = 0.709mohm$
 $PR598 = (1.9mV/A) / (Rcs \times 400us) = 6.34K$

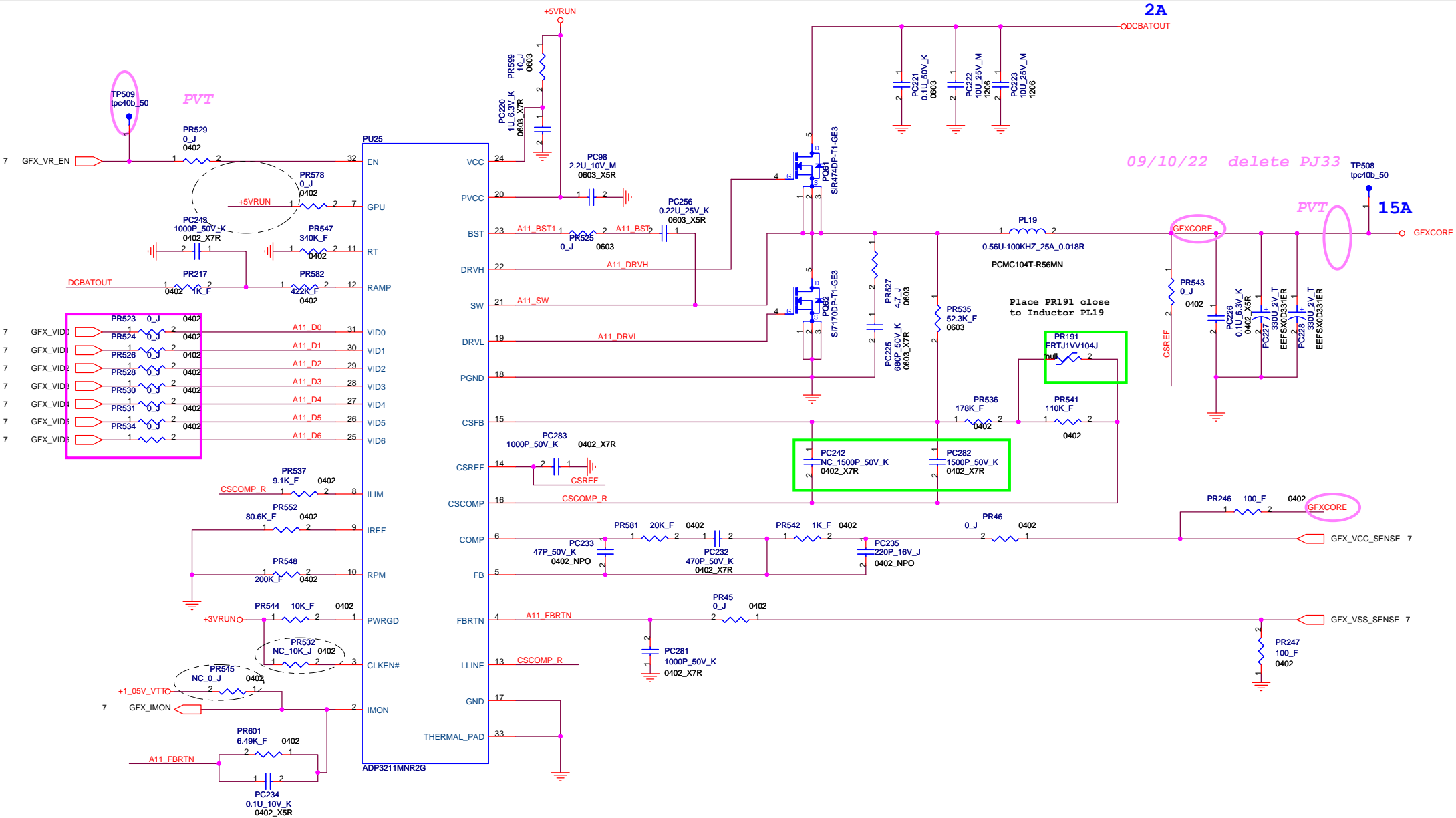
09/11/13 change pc253 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CPU Power VHCORE	
Size	Document Number	Rev	
A3	M960&M970 L Model	SA	
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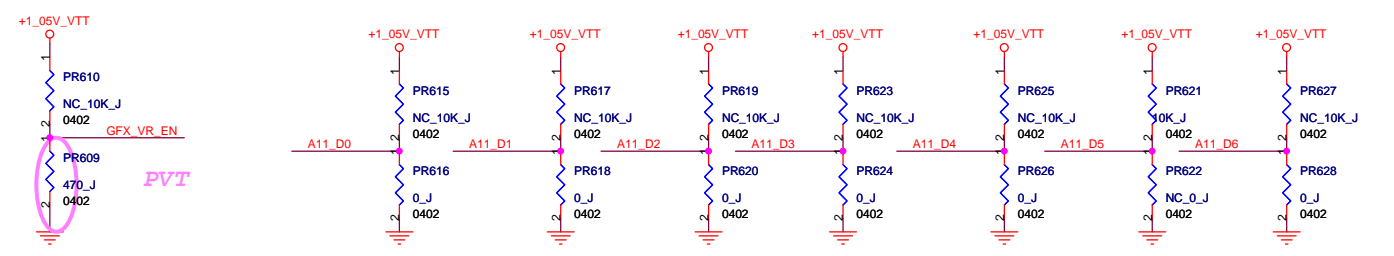
Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1



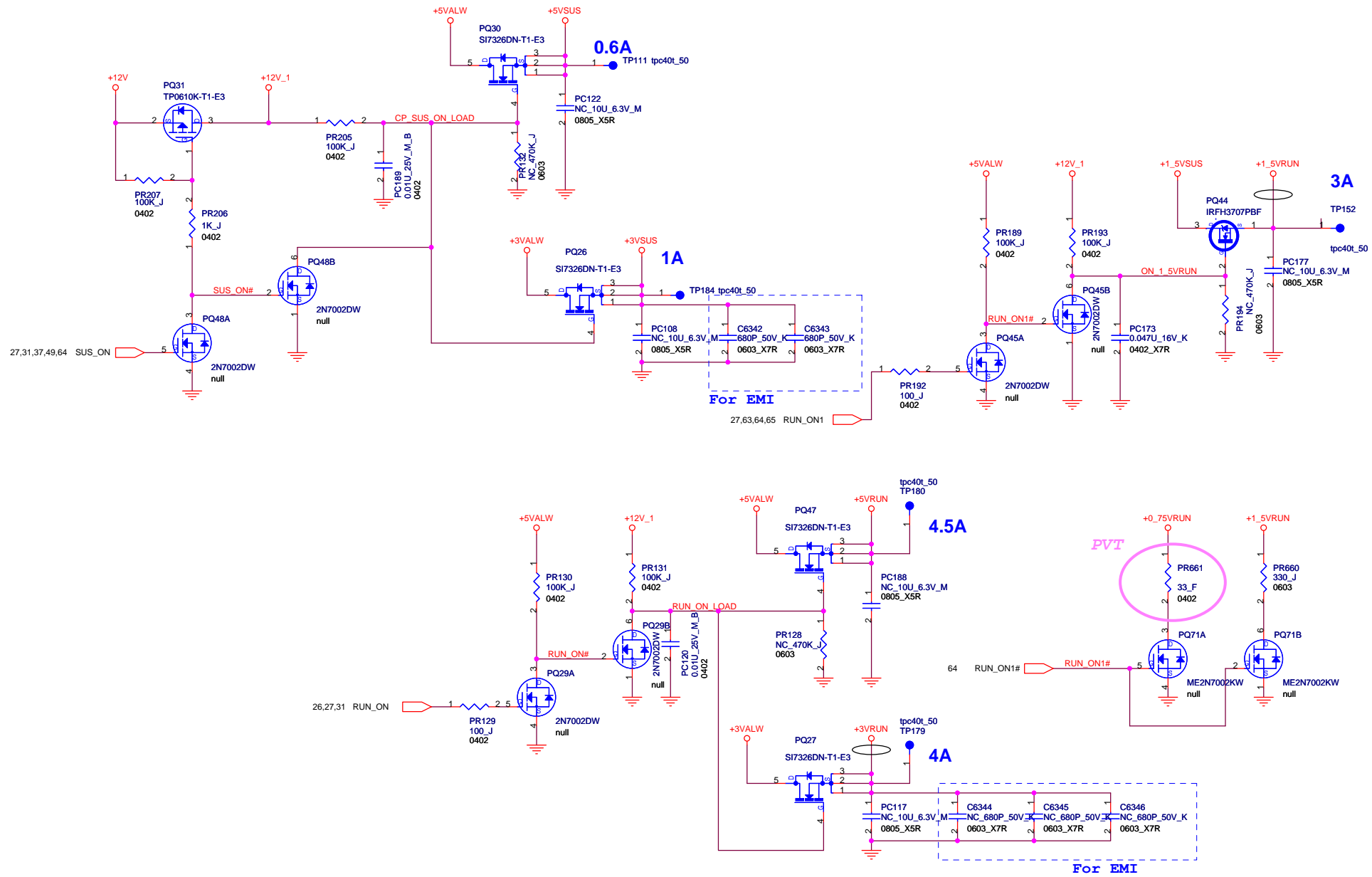


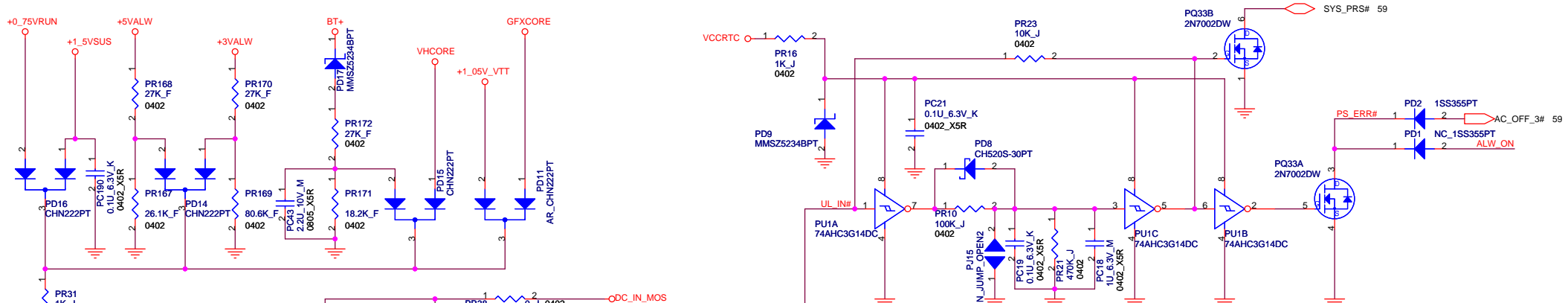
09/11/26 change PR609 to 470ohm for MOR request

Default value of VID [6:0] = [0100000]



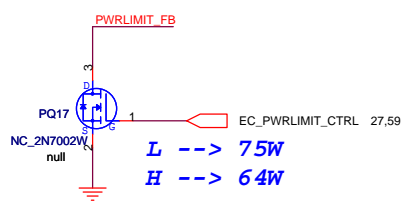
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
VGFX Power GFXCORE	
Title M960&M970 L Model	Rev SA
Size A3	Document Number M960&M970 L Model
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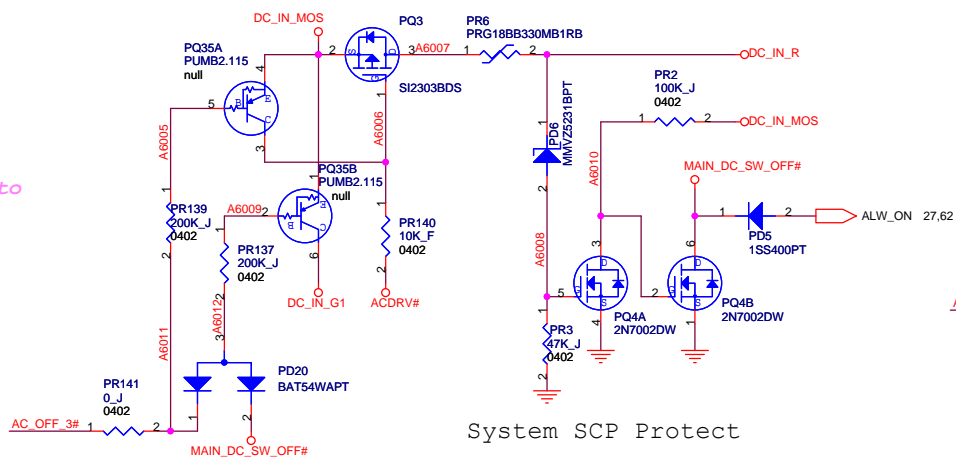


PJ15 Near the DDR socket door

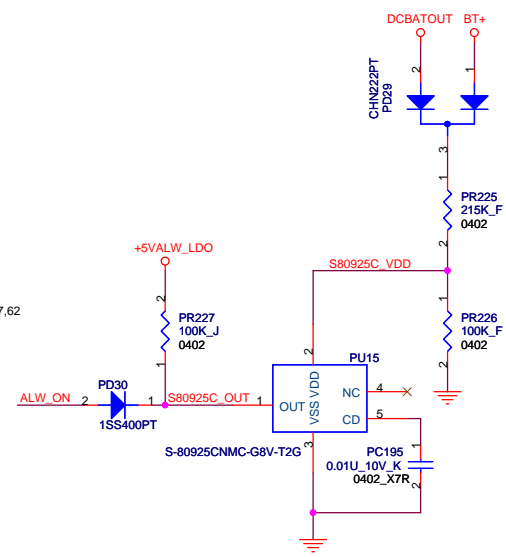
PVT
 System OVP protect
 09/11/13 change pc41 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request



L --> 75W
 H --> 64W



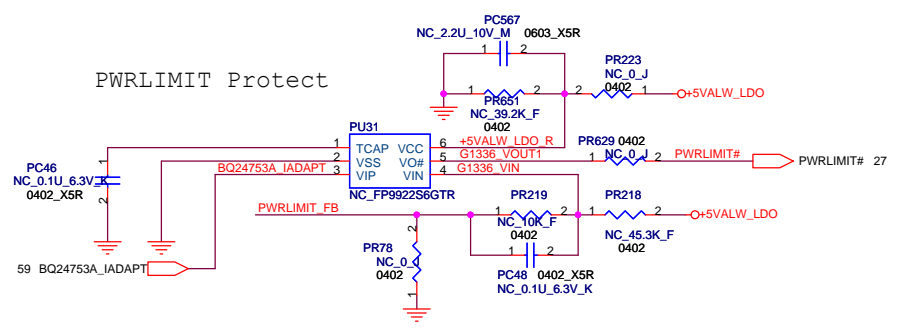
System SCP Protect



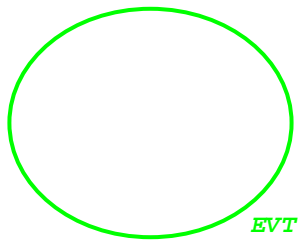
Battery UVP Protect

DVT	PQ18	PR219	PR79
For Power limit	NO NC	68.1K	2.05K

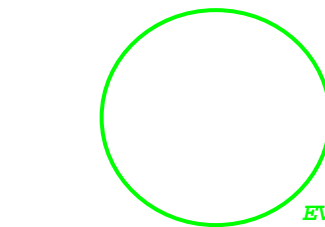
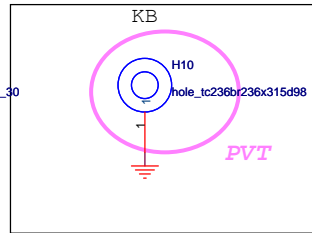
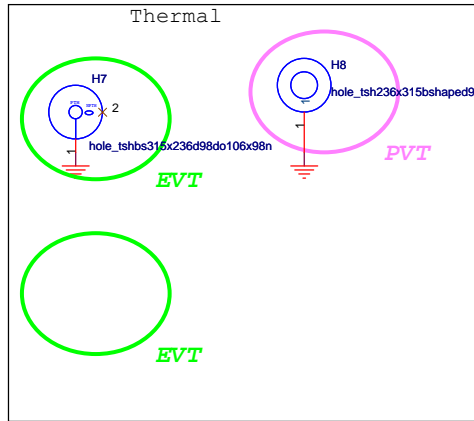
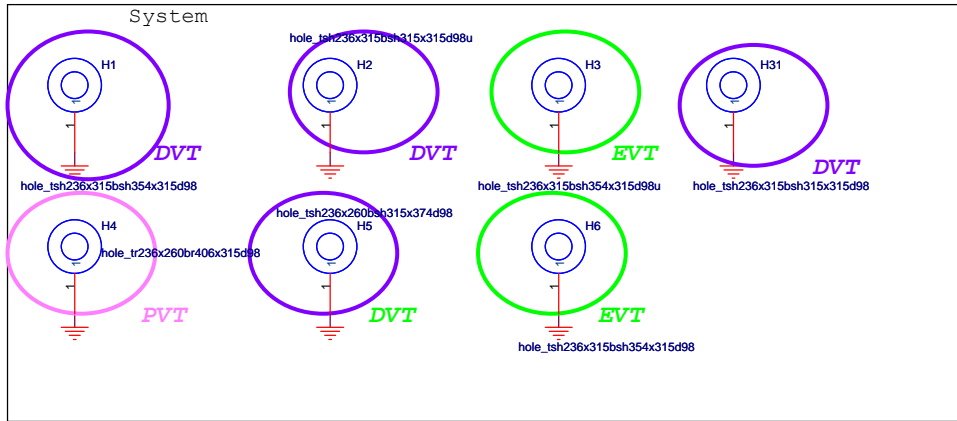
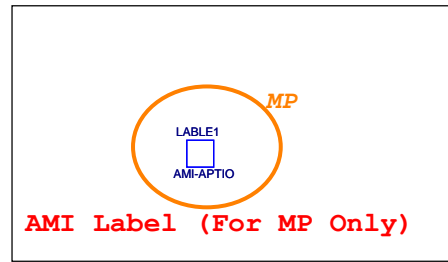
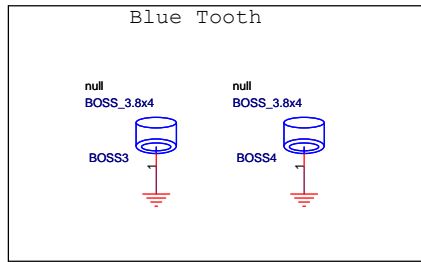
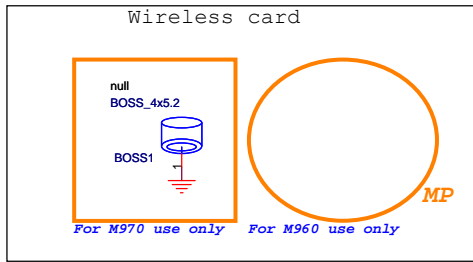
DVT	PWRLIMIT
H M/B (75W)	3.76A/71.41W
L M/B (64W)	3.2A/60.82W



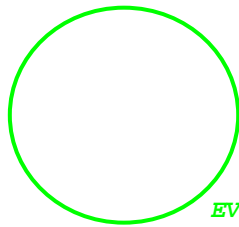
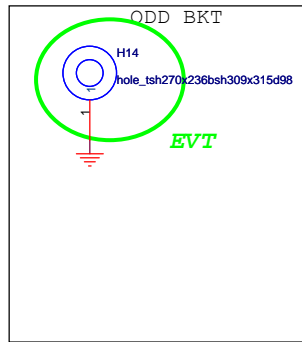
PWRLIMIT Protect



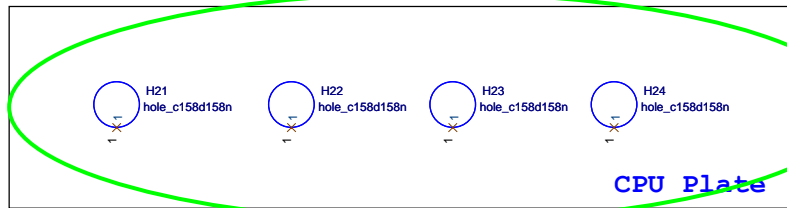
EVT



EVT

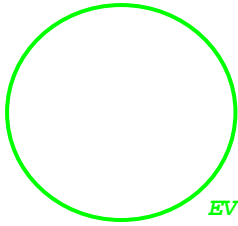


EVT

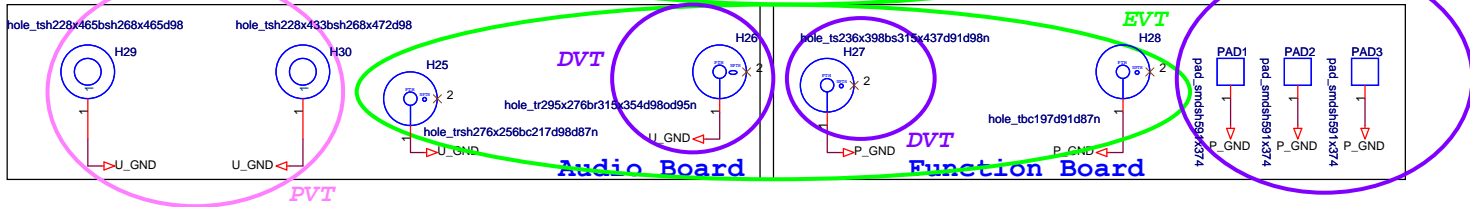


CPU Plate

EVT



EVT



Audio Board

Function Board

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	HOLE		
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M960/M970 EVT

(2009/06/22)

P.23 [CRT]Change D10 from S24 to SSM24PT for same as M930.

(2009/06/23)

- P.61 [DCIN & Charger]Add test points TP1148~TP1155 for BFT test.
- P.41 [Camera Connector]Add test points TP1156~TP1161 for BFT test.
- P.45 [FAN]Add test points TP1162~TP1165 for BFT test.
- P.47 [LAN]Add test points TP1166~TP1181 for BFT test.
- P.31 [Debug Port]Add test points TP1186~TP1193 for BFT test.
- P.49 [AUDIO Speaker Conn]Add test points TP1194~TP1197 for BFT test.
- P.29 [KB Connector]Add test points TP1198~TP1207 for BFT test.
- P.48 [SWITCH DB Conn.]Add test points TP1208~TP1211 for BFT test.
- P.61 [DCIN&Charger]Add test points TP1212~TP1218 for BFT test.
- P.29 [KB Connector]Del CN4 because M960 and M970 KB connectors are decided to co-use.
- P.55 [AUDIO Speaker AMP]Del this page because AMP is combined with ALC275
- P.51 [PCIE (MS&iLINK)]Change the net name from "SDMS_VCC" to "VCC_MS" because this net is for MS power only.
- P.13 [PCH (LVDS,DDI)]Del R1571 because it is a over-design part.
- P.27 [HDMI]Del R507,R508,R568,R569,RP53,RP77 for redundant design.
- P.23 [CRT]Add Semi-PNP schematic
- P.27 [HDMI]Del R567,R504 and change Q34 to 2N7002EPT for PS8101 and PS8171 co-lay.
- P.27 [HDMI]Change R515,R538 from 3.9K to 1.5K for PS8101 and PS8171 co-lay.
- P.27 [HDMI]Del R496 for PS8101 and PS8171 co-lay.
- P.13 [PCH (LVDS,DDI)]Del Q72,R1578,R1577
- P.27 [HDMI]Change R511,R506 from 2.2K to 1.5K for PS8101 and PS8171 co-lay.
- P.25 [Inverter Connector]Del R400 because it is useless.
- P.27 [HDMI]Add R5884~R5899,C6206 for PS8101 and PS8171 co-lay.

P.23 [CRT]NC R5752 for Semi-PNP schematic.

(2009/06/24)

- P.23 [CRT]Del U9,R767,C279 for Semi-PNP.
- P.23 [CRT]Change net name "VGA_CRT_DET#" to MB_CRT_DET# for Semi-PNP.
- P.23 [CRT]Stuff R5752 for Semi-PNP schematic.
- P.27 [HDMI]Change R572,R573,R505,R5884,R5885 from 2.2K_J to 4.7K_J for PS8171 only design.
- P.27 [HDMI]NC R572,R573,R5884,R5885 for PS8171 only design.
- P.27 [HDMI]Del R570 for PS8171 only design.
- P.27 [HDMI]Del RP53 for PS8171 only design.
- P.27 [HDMI]Stuff R5886,R5890,R5889 for PS8171 only design.
- P.27 [HDMI]Stuff R5894 for PS8171 only design.
- P.10 [PCH (HDA,JTAG,SAT)]Del R302 for redundant design.
- P.27 [HDMI]Stuff R5897,R5898 for PS8171 only design.
- P.27 [HDMI]Del R481,R482,R484,R485,R486,R490,R491,R493,L56,L59,L61,L73 for PS8171 only design.
- P.27 [HDMI]Del R518,Q34 for PS8171 only design.
- P.27 [HDMI]Add R5900 on HDMI_DET_5 and connect it to GND for Intel recommend.
- P.43 [Felica Connector]Del F13,R5873,R5872 because the F13 related circuit is out of Felica spec.
- P.43 [Felica Connector]Stuff C869,U48,R630,C845 because F14 related circuit is out of Felica spec.
- P.60 [DCIN&CHARGE]Change DC-IN current form 8A to 5A.
- P.60 [DCIN&CHARGE]Change PD7 from SMD15C to TVS2315PT.
- P.62 [Identify ID]Change PC61 from 1uF 10V_k to 220Pf_50v_J,then NC PC61.
- P.64 [VTT&PCH Power(+1_05V)]Change PR116 from 100k to 470k.
- P.65 [DDR3 Power(+1_5V/+0_75V)]Change PR655 from 100k to 470k.
- P.67 [CPU Power_VHCORE]Delete PC67,PC155.
- P.70 [Other plane power]Change PQ29,PQ45,PQ48: from 2N7002DW to 2N7002SPT.
- P.71 [OVP protection]Change PC41 from 0.01uF to 1000Pf.
- P.07 [ARD (GRAPHICS POWER)]Del R5811 and connect a off page to GFX_VR_EN.
- P.25 [Inverter Connector]Add and NC R400 on GM_BRADJ to GND for Intel recommend.

(2009/06/25)

- P.33 [Mini-PCIE Card (WLAN)]Add R5901 on WLAN_EN for RF VEDS test.
- P.51 [SWITCH (Botton & KB LED)*]Change P_VR1,P_VR2,P_VR3,P_VR4,P_VR5 for EMC team request.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Del SPR1,J1.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Connect CN34 207 Pin to GND.
- P.21 [DDRIII(SO-DIMM_0) 2/2]Connect CN35 G2 Pin to GND.
- P.07 [ARD (GRAPHICS POWER)]Connector a pull-low resistor "R401" to GFX_DPRSPLVVR.
- P.34 [LAN (88E8057) 1/2]Del R1462 for Marvell comment.
- P.34 [LAN (88E8057) 1/2]NC C997,R94 for Marvell comment.
- P.07 [ARD (GRAPHICS POWER)]NC R401 and del GFX_DPRSPLVVR off-page.
- P.25 [Inverter Connector]Add U89C,R809,R684,C902,R772 for MOR's request.
- P.25 [Inverter Connector]Change the off-page from "BL_OFF#" to "INV_EN" for MOR's request.
- P.25 [Inverter Connector]Add U89A,U89B,C877,R687 for MOR's request.
- P.25 [Inverter Connector]Add an off-page of BL_OFF# on U89D for MOR's request.
- P.13 [PCH (LVDS,DDI)]Connect AT38 of U69 to HDMI_DET_5 for MOR's request.
- P.10 [PCH (HDA,JTAG,SAT)]Add R5905 to let JTAG_TCK pull down for MOR's request.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Add R539,R540 to let PCIECLKRQ3#,PCIECLKRQ4# to pull high to +3VRUN for MOR's request.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Add R579 to connect WLAN_CLKREQ# to +3VSUS for MOR's request.
- P.11 [PCH (PCI-E,SMBUS,CLK)]NC R577 for MOR's request.
- P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth function from port 13 to port10 to meet Freedom Project Product Specifications.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del GPIO39 related circuit because this pin is for LCDID3
- P.39 [PCIE (MS&iLINK) 1/2]Delete i-Link function from Freedom_specV0.6.

(2009/06/26)

- P.19 [CLOCK GEN]Change U31 from SL28748ALC to SL28748CLC.
- P.14 [PCH (PCI,USB,NVRAM)]Del USB_PN12,USB_PP12 off-page and add TP365,TP452 on the same ports.
- P.33 [Mini-PCIE Card (WLAN)]Del U45,C891 for disable WIMAX function
- P.33 [Mini-PCIE Card (WLAN)]NC 36pin,38pin of CN12 for disable WIMAX function
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add an off-page "LCDID4" on GPIO48 and change the net name to LCDID4 for LCDID[4:0].
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del R5902 for LCDID[4:0].
- P.51 [SWITCH (Botton & KB LED)*]Del "VAIO" button from Freedom Project Product Specifications V0.6.
- P.51 [SWITCH (Botton & KB LED)*]Change the names "Web" and "Display Off" to "Instant On" and "VAIO" from Freedom Project Specifications V0.6.
- P.39 [PCIE (MS&iLINK) 1/2]Connect TPB+/- to GND and NC TPAP0/TPAN0/TPBIAS0 to disable i-Link function for Realtek comment.
- P.39 [PCIE (MS&iLINK) 1/2]Add R1468 and NC it to disable i-Link function for Realtek comment.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Add a +3VALW pull-high resistor R5422 on PEG_A_CLKREQ# pin for MOR's request.
- P.12 [PCH (DMI,FDI,GPIO)]Connect SYS_PWROK line to ALW_PWRGD through D33 for MOR's request.
- P.32 [Express Card]Add R5457 between the gate and the source of Q38 for MOR's request.
- P.56 [AUDIO (Head Phone Jack)*]Add U_R220 pull-high to U_VDDA on U_HP_IN_5 for Realtek comment.
- P.56 [AUDIO (Head Phone Jack)*]Change U_GND ground to U_A_GND for Realtek comment.
- P.57 [AUDIO (Ext MIC Jack)*]Add U_R222 pull-high to U_VDDA on U_EXTMIC_IN for Realtek comment.

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(2009/06/26)

- P.57 [AUDIO (Ext MIC Jack)*]Change U_C35/U_C36 to 4.7u X5R for Realtek comment.
- P.27 [HDMI]Change HDMI Repeater from PS8101 to PS8171 for MOR's request.
- P.72 [HOLE & AMI LABEL]Add H1~H20 for ME request.

(2009/06/29)

- P.25 [Inverter Connector]Change the net name "GM_BRADJ" of CN5 Pin4 to INV_BRADJ.
- P.26 [LVDS Connector]Change the net name "GM_BRADJ" to INV_BRADJ.
- P.56 [AUDIO (Head Phone Jack)*]Change U_A_GND which is connected to U_C11 pin2 to U_GND.
- P.38 [DCIN&Charger]Change PCN1 connector to BP91071-B51E3-7H for ME request.
- P.38 [eSATA Combo Conn.]Change CN27 connector to 3Q38111-R21C3-8H for ME request.
- P.46 [Touch Pad]Change SW2/SW3/SW6/SW7 to 19-SKRPABE-1000 for ME request.
- P.22 [Braidwood Connector]Change NC39 to 1N-0078002-F1G0 for ME request.
- P.27 [HDMI]NC R5886,R5889,R5894,R5897,R5898 for PS8171 vendor's comment.
- P.39 [PCIE (MS&iLINK) 1/2]Del R1468 and connect XOUT to U71 A2 for Ricoh's comment.
- P.16 [PCH (POWER) 1/2]Change R366,R325 to 100 ohm for Intel'comment.
- P.16 [PCH (POWER) 1/2]Change C141 to 1U for Intel'comment.
- P.27 [HDMI]Change R515 to 2.2K for Intel's comment.
- P.09 [ARD (RESERVED)]Change R1274 to 3.3K for Intel's comment.

(2009/06/30)

- P.68 [CPU Power_VID]Stuff PR638,PR646 for Power request.
- P.68 [CPU Power_VID]NC PR637,PR645 for Power request.
- P.33 [Mini-PCIE Card (WLAN)]Del R824 for MOR's request.
- P.12 [PCH (DMI,FDI,GPIO)]Change R911 to 10K for MOR's request.
- P.42 [Bluetooth Connector]Del C378 for MOR's request.
- P.33 [Mini-PCIE Card (WLAN)]NC CN12 15pin and del R18 for RF request.
- P.44 [Status LED & LID]Add LED6/LED7/LED8/LED9 for M970 only.
- P.33 [Mini-PCIE Card (WLAN)]Add R17 and NC it for MOR's request.

(2009/07/01)

- P.72 [HOLE & AMI LABEL]Del BOSS9,BOSS10 for ME request.
- P.72 [HOLE & AMI LABEL]Add CPU hole H21,H22,H23,H24 for CPU socket.
- P.38 [eSATA Combo Conn.]Del eSATA repeater schematic (U214,C766,C776,C759,C745,R5754,R5835,R5756,R5755,R5757,R5758,R5759,C718,C387) for over-design.
- P.10 [PCH (HDA,JTAG,SAT)]Del U27,U28,C817,C838,R5371,R1555,R1556 because this part is for SW reserve design.
- P.10 [PCH (HDA,JTAG,SAT)]Change SPI_CLK_SW/SPI_MOSI_SW/SPI_MISO_SW to SPI_CLK_L/SPI_MOSI_L/SPI_MISO_L for modifying the SW reserve design.
- P.13 [PCH (LVDS,DDI)]Add two connection L_DDC_CLK/L_DDC_DATA to CN13 5/6 pin for SW request to add EDID function.

(2009/07/02)

- P.26 [LVDS Connector]Connect CN13 Pin1 to LCDVCC for LCD power supply.
- P.26 [LVDS Connector]Connect CN13 Pin34 to GND for LCD power supply.
- P.39 [PCIE (MS&iLINK) 1/2]NC R820/C868/R817/C865/R818/C864 because SD_CD#/SD_WP#/MS_CD# has an internal pull-up resistor and the debouching circuit.
- P.24 [LVDS]Update Panel ID and related information.

(2009/07/03)

- P.10 [PCH (HDA,JTAG,SAT)]Del TP119/TP123/TP133/TP136/TP137/TP138 and R442 because this is SW reserve design.
- P.14 [PCH (PCI,USB,NVRAM)]Del Q39/Q37/R5456/SW5/R300 for changing GNT1#/GNT0# control method.
- P.14 [PCH (PCI,USB,NVRAM)]Add R345/R346 pull-high to +3VRUN for controlling GNT1#/GNT0#.
- P.14 [PCH (PCI,USB,NVRAM)]Change R344/R392/R345/R346 to 10K ohm.
- P.33 [Mini-PCIE Card (WLAN)]Del R17 and change the net name "MINI_PCIE_+3_3V_R" to "MINI_PCIE_+3_3V" to del RF reserve circuit.
- P.58 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 to 2N-0004009-MKG0 for ME request.
- P.27 [HDMI]Reverse Q34A/Q34B/R504/R518 and connect HDMI_DET_3 to AT38 of U69 for MOR's request.
- P.22 [Braidwood Connector]Del CN39 and its related schematic for disabling Braidwood function.
- P.22 [Braidwood Connector]Del Page.22 and change page number 23~74 to 22~73.
- P.51 [AUDIO (CODEC)*]Change U_R5774 to 100K ohm and change the power source on it from U_VDDA to U_+12V because Gate voltage of U_Q55 is too low.
- P.54 [AUDIO (AUDIO & USB Conn)*]Move U_SUS_ON to U_CN1 Pin22 and add U_+12V on Pin7.
- P.49 [AUDIO/USB DB Conn.]Move SUS_ON to CN31 Pin29 and add +12V on Pin44.
- P.25 [LVDS Connector]Add Q177/Q178/R5736/R5737/C575 and change L98 for rush current issue.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add a NC resistor R979 to let GPIO8 pull-low to GND.
- P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth USB port to port13.
- P.14 [PCH (PCI,USB,NVRAM)]Change USB External Port-1 to USB port5 and eSATA change to port0.
- P.26 [HDMI]Change R538 to 2.2k in order to equal to R515.

(2009/07/04)

- P.32 [Mini-PCIE Card (WLAN)]Restore U45,C891 for WIMAX function.
- P.32 [Mini-PCIE Card (WLAN)]Connect 36pin,38pin of CN12 to USB_PN12_L/USB_PP12_L for WIMAX function.
- P.32 [Mini-PCIE Card (WLAN)]Add J5 to connect Pin42 and Pin44 of CN12 for MOR's request.

(2009/07/06)

- P.11 [PCH (PCI-E,SMBUS,CLK)]Stuff Y8,C1288,C1289,R1226,R813 for M930 HDMI complication test issue.
- P.11 [PCH (PCI-E,SMBUS,CLK)]NC R1651 for M930 HDMI complication test issue.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Stuff R979 and NC R983 for M930 HDMI complication test issue.

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(2009/07/07)

- P.41 [Bluetooth Connector]Add C378 pull-low to GND refer to M930.
- P.43 [Status LED & LID]Del POWER/SUSPEND LED and its related circuit for ID changing.
- P.13 [PCH (LVDS,DDI)]Add R222 pull-low resistor connect to HDMI_DET_3 for MOR's comment.
- P.12 [PCH (DMI,FDI,GPIO)]Change R973 to 2.2K ohm for MOR's requirement.
- P.25 [LVDS Connector]Add Q177 and related RC for protecting rush current.
- P.48 [AUDIO Speaker Conn]Del Q28/Q30/Q53 and connect Q25 and Q27 because short protection circuit can marge L channel and R channel.
- P.04 [ARD (CLK,MISC,JTAG)]Add Q72 for Intel S3 Power Reduction issue.
- P.59 [DCIN&Charger]Delete PR17.
- P.62 [SYS Power (+3_3V/+5V)]Delete close_jump GP2.
- P.64 [DDR3 Power(+1_5V/+0_75V)]Change 1.5VSUS full load from 12A to 13A.
- P.64 [DDR3 Power(+1_5V/+0_75V)]Change PR654 from 46.4k to 49.9k.
- P.68 [VGFX Power_GFXCORE]Delete PR195.
- P.69 [Others power plane]Change 1.5VVRUN full load form 6A to 3A.
- P.69 [Others power plane]Add 1.5VVRUN discharge circuit (add PR660 330ohm,PQ71 2N7002EPT).
- P.13 [PCH (LVDS,DDI)]Del L_DDC_CLK/L_DDC_DATA off-page for disabling EDID.

(2009/07/08)

- P.43 [Status LED & LID]Add Q18/Q21/Q48/Q51/R384/R390/R690/R691/R694/R695 for POWER/SUSPEND LED location changing.
- P.41 [Bluetooth Connector]Del C378 because C377 has the same function.
- P.27 [EC+KBC(NPCE783L)]Add SYSTEM_ID3 (R5891/R5900) for SKU control.
- P.25 [LVDS Connector]NC CN13 Pin3 because EDID is disabled.
- P.43 [Status LED & LID]Change Q18/Q21/Q50 to DTC114EUB for MOR's request.
- P.50 [SWITCH (Botton & KB LED)*]Del P_SW3 and add P_CN4 for POWER/SUSPEND LED location changing.
- P.07 [ARD (GRAPHICS POWER)]Change VDDQ power source from +1_5VSUS to +1_5VVRUN for Intel S3 Power Reduction issue.
- P.47 [SWITCH DB Conn.]Change CN2 to 14pin type for POWER/SUSPEND LED location changing.
- P.50 [SWITCH (Botton & KB LED)*]Change P_CN3 to 14pin type for POWER/SUSPEND LED location changing.
- P.38 [PCIE (MS&iLINK) 1/2]Change CN36 type for ME request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Set GPIO27 as RST_GATE for Intel S3 Power Reduction issue.
- P.62 [SYS Power (+3_3V/+5V)]Change NC PR118 to NO NC PR118 and NC PR234,PR235.
- P.68 [VGFX Power_GFXCORE]Change NC PC281 to NO NC PC281.
- P.70 [OVP protection]Delete reserved Power limit circuit (delete PU2,PU11,PD22 ,PR22,PR24,PR142,PR143,PR149,PR153,PR159,PR213,PR214,PC26,PC27,PC28).
- P.70 [OVP protection]Change PR218 from 37k to 45.3k.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Del R1590/R1591/R1592/Q73/Q74 and rename SMB_DATA_SB/SMB_CLK_SB to SMB_DATA_R/SMB_CLK_R refer to M930.
- P.10 [PCH (HDA,JTAG,SAT)]Del R1552/R1554 and rename SPI_CLK_L/SPI_MOSI_L to SPI0_CLK/SPI0_MOSI for redundant design.
- P.10 [PCH (HDA,JTAG,SAT)]Add R5908 on SATA_LED# which is pull-high to +3VVRUN for Intel comment.
- P.04 [ARD (CLK,MISC,JTAG)]NC R1451/R1452 and stuff R1450/R1453 refer to M930.
- P.39 [PCIE (SD) 2/2]Change CN29 type for ME request.
- P.45 [Touch Pad]Change SW2/SW3/SW6/SW7 type for ME request.

(2009/07/09)

- P.55 [AUDIO (Head Phone Jack)*]Change Pin7/Pin8 of U_CN4 to U_A_GND for Layout request.
- P.07 [ARD (GRAPHICS POWER)]Add a Open-Jump PJ43 between +1_5VVRUN to VDDQ.
- P.06 [ARD (POWER)]Del R856/R857 for MOR's request.
- P.07 [ARD&CFD (GRAPHICS POWER)]Del R864/R866/R868/R869/R871 for MOR's request.
- P.38 [PCIE (MS&iLINK) 1/2]Add damping resistors (R5909~R5917) on each MS signal.
- P.39 [PCIE (SD) 2/2]Change C518/C522 to X5R type for MOR's request.
- P.39 [PCIE (SD) 2/2]Add damping resistors (R5918~R5922) on each SD signal for MOR's request.
- P.39 [PCIE (SD) 2/2]Change C767 to 10pF for MOR's request.
- P.56 [Status LED & LID]Del LED7/LED8/LED10 for ME request.
- P.25 [LVDS Connector]Add NC Cap. (C6306~C6313) between each LVDS differential lane.
- P.33 [LAN (88E8057) 1/2]Modify R94/R97/C997 description.
- P.33 [LAN (88E8057) 1/2]Change all resistors and caps to 88E8059 setting.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R979 to 1k ohm for Intel suggestion.
- P.71 [HOLE & AMI LABEL]Add H25/H26/H27/H28 for ME request.
- P.22 [CRT]Change CN20 type for ME request.
- P.57 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 type for ME request.
- P.71 [HOLE & AMI LABEL]Del H11/H12/H13/H15/H16/H17/H18/H19/H20 for ME request.
- P.31 [Express Card]Rename PCIE_EXPRESS_WAKE# to PCIE_WAKE# to del reserve design.
- P.12 [PCH (DMI,FDI,GPIO)]Del R290 and PCIE_EXPRESS_WAKE# off-page to del reserve design.
- P.59 [DCIN&Charger]Renamed resistor PR657 to PR4.
- P.68 [VGFX Power_GFXCORE]Change NC PR523,NC PR523,NC PR526,NC PR528,NC PR530 ,NC PR531,NC PR534 to No NC.
- P.69 [Others power plane]Add 0.75V_RUN discharge circuit (add PR661 330ohm).
- P.69 [Others power plane]Change PQ71 from 2N7002EPT to ME2N7002KW.
- P.04 [ARD (CLK,MISC,JTAG)]Del the description of RST_GATE and add a 1k ohm resistor R5923 between +1_5VSUS and DDR3_DRAMRST#.
- P.04 [ARD (CLK,MISC,JTAG)]Add R5924/R5925/U217 for Intel S3 Power Reduction issue.
- P.04 [ARD (CLK,MISC,JTAG)]Del R928/R929 and related description for Intel S3 Power Reduction issue.
- P.40 [Camera Connector]Add R5926/R5927/C6314/C6315 For EMI verification.
- P.24 [Inverter Connector]Add R5928 For EMI verification.

(2009/07/10)

- P.37 [eSATA Combo Conn.]Swap L66/L67 for layout request.
- P.46 [Thermal Sensor]Change thermal sensor to G781-1 for SW request.
- P.50 [SWITCH (Botton & KB LED)*]Change the description "Instant On" to "Web(Instant On) for SW request"
- P.38 [PCIE (MS&iLINK) 1/2]Del R820/C868/R817/C865/R818/C864 for Ricoh's FAE suggest.
- P.38 [PCIE (MS&iLINK) 1/2]Add description of C794/C771/C774/C992 for Ricoh's FAE suggest.
- P.38 [PCIE (MS&iLINK) 1/2]Add description of C790/C769/C770/C772/C799 for Ricoh's FAE suggest.
- P.38 [PCIE (MS&iLINK) 1/2]Add description of C716/C717 for Ricoh's FAE suggest.
- P.26 [HDMI]Connect Q57 D/S to +5VVRUN_L188/+5VVRUN_F.
- P.25 [LVDS Connector]Connect Q144 D/S to DCBATOUT_L/DCBATOUT.
- P.27 [EC+KBC(NPCE783L)]Change net name "KB_PRESENCE#" to "INST_ON_SW#" for SW request.
- P.59 [DCIN&Charger]Delete NC PR12.
- P.59 [DCIN&Charger]Change charge voltage form 12.48V to 12.465V for MOR request (change PR25 form 200k F to 210K F, change PR27 from 100K F to 100K D).
- P.61 [Identify IC]Change PC66 from 0.1u_16v_0402_Y5V to 0.1u_10v_0402_X5R.
- P.61 [Identify IC]Change NC PC65 1u_10v_0603_X5R to NC PC65 1u_10v_0402_X5R.
- P.66 [CPU Power_VHOCORE]Change PC112 from 100U_25V_M_Φ6.3*7.7mm to 68uF_25V_M_Φ6.3*5.8mm.

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- P.24 [Inverter Connector]Reverse CN5.
- P.50 [SWITCH (Botton & KB LED)*]Reverse P_CN3.
- P.25 [LVDS Connector]Add description on the circuit for inrush current issue of M870.
- P.22 [CRT]Change F2 type for PUR request.
- P.51 [AUDIO (CODEC)*]Change U_C459/U_C476/U_C787 type for PUR request.
- P.07 [ARD (GRAPHICS POWER)]Add net name "+1_5VRUN_J".
- P.14 [PCH (PCI,USB,NVRAM)]Del R344/R392 and the description about Boot-BIOS for SW request.
- P.40 [Camera Connector]Add net name DMIC_CLK_R/DMIC_DAT_R and connect TP1160/TP1161 to the new net for TE request.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Reconnect SPR2/J2 to CN34 and CN35 for EMC request.
- P.10 [PCH (HDA,JTAG,SAT)]Reverse CN26.
- P.26 [HDMI]Change CN21 type for ME request.
- P.48 [AUDIO Speaker Conn]Swap JSPK1 for ME request.

(2009/07/13)

- P.39 [PCIE (SD) 2/2]Change U22 to G553E1P11U to meet MOR's request for SD.
- P.45 [Touch Pad]Reverse CN8 for ME request.
- P.50 [SWITCH (Botton & KB LED)*]NC P_VR2 for EMC reserve.
- P.38 [PCIE (MS) 1/2]Del all i-Link related description.
- P.24 [Inverter Connector]Reverse CN5.
- P.71 [HOLE & AMI LABEL]Change H2/H3/H4/H5/H6/H7/H10/H14 type for ME request.
- P.26 [HDMI]Swap U37 for Layout request.
- P.59 [DCIN&Charger]Delete EC3 and C907.
- P.66 [CPU Power_VHOCORE]Change PC566 from 0.1U_6.3V_K to 0.1U_16V_K (HH PN:1C-2B20104-K300).
- P.68 [VGFX Power_GFXCORE]Change PC98 from 2.2U_6.3V_K to 2.2U_10V_M (HH PN:1C-2B30225-M201).
- P.70 [OVP protection]Change PQ3 from IRLML5103TRPbF to SI2303BDS.
- P.04 [ARD (CLK,MISC,JTAG)]Change U217 SUS_PWRGD to RUN_PWRGD.
- P.71 [HOLE & AMI LABEL]Del H9 for ME request.
- P.04 [ARD (CLK,MISC,JTAG)]Change R5924/R5925 to 1.5K/750 ohm for intel's comment.
- P.69 [Others power plane]Change PR661 from 330ohm to 33ohm.

(2009/07/14)

- P.25 [LVDS Connector]Swap Pin1 CN13 to Pin3 CN13 for cable design.
- P.71 [HOLE & AMI LABEL]Change H4/H5/H7 footprint for ME request.
- P.59 [DCIN&Charger]NC PR76 and PR77.
- P.66 [CPU Power_VHOCORE]Change PR555 and PR569 from 2.7K to 2.21K.
- P.66 [CPU Power_VHOCORE]NC PC260 ,NC PC261.
- P.27 [EC+KBC(NPCE783L)]Pull-high INST_ON_SW# to +ECVCC for SW request.
- P.64 [DDR3 Power(+1_5V/+0_75V)]Add PQ59(2N7002EPT)/PR600(100K)/PC570(1U_10V_K), then NC PQ59/PR600/PC570.
- P.10 [PCH (HDA,JTAG,SAT)]Add C6316/C6317/C6318/C6319/C6320/C6321 for EMC reserve.
- P.33 [LAN (88E8057) 1/2]Add C6322/C6323 for EMC reserve.
- P.39 [PCIE (SD) 2/2]Add C6325 for EMC reserve.
- P.38 [PCIE (MS) 1/2]Add C6324 for EMC reserve.

(2009/07/15)

- P.36 [SATA CD-ROM]NC CN37 for ME request.
- P.10 [PCH (HDA,JTAG,SAT)]Connect C6321 to +1_05V_VTT for EMC request.
- p.66 [CPU Power_VHOCORE]change PC112 from NOCHICON to Panasonic.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Del SPR2 for EMC request.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Del EMCS1/EMCS2 off-page and add J6 for EMC request.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Rename EMCS1/EMCS2 to EMCS3/EMCS4 and add J7/J8 for EMC request.
- P.68 [VGFX Power_GFXCORE]change PC242 and PC282 form 1C-2B20152-M000 to 1C-2B20152-K600.

- P.09 [ARD (RESERVED)]Del RP83/DQ_VREF off-page and add two test point to CPU for Intel's comment.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Del C35/C41/R1283 and DQ_VREF0 off-page for Intel's comment.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Del C37/C44/R1284 and DQ_VREF1 off-page for Intel's comment.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
- P.83 [HOLE & AMI LABEL]Add H29/H30/PAD1/PAD2/PAD3 for EMC request.
- P.71 [HOLE & AMI LABEL]Change H28/H25 type for ME request.

(2009/07/16)

- P.71 [HOLE & AMI LABEL]Change PAD1/PAD2/PAD3 for CIS request.
- P.68 [VGFX Power_GFXCORE]change PR191 vendor numbler form NT731JTTD104J3800J to ERTJ1VV104J.
- P.20 [DDRIII(SO-DIMM_0) 1/2]Restore C35/C41 for MOR's request.
- P.21 [DDRIII(SO-DIMM_1) 2/2]Restore C37/C44 for MOR's request.

(2009/07/17)

- P.66 [CPU Power_VHOCORE]Change PR565 from 10k to 1.8k, change PC566 from 0.1u to 0.022u.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Mount R983 and NC R979 for Intel suggestion.

(2009/07/21)

- p.1~76 [Page Data]Update all page data.

(2009/07/24)

- P.72 [Braidwood Connector]Add CN39 and its related schematic for layout estimation.
- P.14 [PCH (PCI,USB,NVRAM)]Add Braidwood related schematic for layout estimation.

(2009/07/30)

- P.72 [Braidwood Connector]Del CN39 and its related schematic for layout estimation.
- P.66 [CPU Power_VHOCORE]Delete PJ42
- P.68 [VGFX Power_GFXCORE]Delete PJ38.

(2009/08/13)

- P.27 [EC+KBC(NPCE783L)]Del R5852 for OVT_EC# double pull-high.
- P.48 [AUDIO Speaker Conn]Change JSPK1 to 1N-0004003-M1T0 for ME request.
- P.54 [AUDIO (AUDIO & USB Conn)*]Reverse U_CN1 for moving U_CN1 from TOP to BOT side.
- P.55 [AUDIO (Head Phone Jack)*]Changen U_CN4 to 2N-000600N-FKG0.
- P.56 [AUDIO (Ext MIC Jack)*]Change U_CN5 to 2N-000600C-FRG0.
- P.57 [AUDIO (USB)*]Change U_USB_OC#1/2/3 to U_USB_OC#0/2.
- P.54 [AUDIO (AUDIO & USB Conn)*]NC U_USB_OC#3_and_Change U_USB_OC#1/2 to U_USB_OC#0/2.
- P.49 [AUDIO(USB DB Conn.)]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
- P.14 [PCH (PCI,USB,NVRAM)]Del off-page USB_OC#1/3.
- P.04 [ARD (CLK,MISC,JTAG)]Change Q72 to 17-2N7002W-0000 for PUR request.
- P.66 [CPU Power_VHOCORE]Delete NC_PC260, NC_PC261.

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(2009/08/18)

- P.22 [CRT]Change F2 to 0.35A.
- P.83 [HOLE & AMI LABEL]Add H31 and change H1/H27/PAD1/PAD2/PAD3 for ME request.
- P.37 [eSATA Combo]Swap CN27B.
- P.31 [Express Card]Change R5457 to 470K and add NC R686 for MOR request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change RST_GATE from GPIO27 to GPIO46 , Stuff R982, NC R977.
- P.34 [LAN (Transformer) 2/2]Change L70 for cost down.
- P.51 [AUDIO (CODEC)*]Change U_U215.
- P.43 [Status LED & LID]Change U21 to 15-EC2648B-0000 for cost down.
- P.59 [DCIN&Charger] Change PQ5, PQ16, PQ34 to 17-2N7002W-0000 for materials shortage.
- P.64 [DDR3 Power(+1.5V/+0.75V)] Change PQ59 to 17-2N7002W-0000 for materials shortage.
- P.70 [OVP protection] Change PQ9, PQ17 to 17-2N7002W-0000 for materials shortage.
- P.69 [Others power plane] Change PQ29, PQ45, PQ48 to 17-2N7002D-W001 for materials shortage.
- P.69 [Others power plane] Change PQ72A to PQ71A.
- P.83 [HOLE & AMI LABEL]Change H29/H30 for ME request.

(2009/08/24)

- P.57 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 for ME request.
- P.48 [AUDIO Speaker Conn]Change JSPK1 for ME request.
- P.22 [CRT]Change CN20 for ME request.
- P.37 [eSATA Combo Conn.]Reverse L62/L66 for Layout request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R977 from NC to Stuff and change R982 from Stuff to NC.

(2009/08/25)

- P.71 [HOLE & AMI LABEL]Change H26 for ME request.

(2009/08/27)

- P.71 [HOLE & AMI LABEL]Change H30 for ME request.

(2009/08/31)

- P.59 [DCIN&Charger]Change PCN1 to BP92071-B81E2-7H for ME request.
- P.36 [SATA HDD]Change CN33 to LN21131-D40L-9H for ME request.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add R5933/R5934/R5935/R5936 and change R5870 to 100K to pull-high LCDID for PE request.
- P.23 [LVDS]Add R5937/R5938/R5939/R5940/R5941/R5942 to pull-low LCDID for PE request.

(2009/09/01)

- P.44 [FAN]Del TP1163.
- P.51 [AUDIO (CODEC)*]Add ALC269 co-lay schematic and del U_TP229, U_TP231, U_TP228.
- P.14 [PCH (PCI,USB,NVRAM)]Del R1575 for redundant design (double pull-low).
- P.52 [AUDIO (MUTE)*]Add ALC265 co-lay schematic.
- P.10 [PCH (HDA,JTAG,SAT)]NC R5908 for redundant design (double pull-high).
- P.62 [SYS Power (+3.3V/+5V)]Move TP215 from +5VALW_PWM to +5VALW for power test.
- P.62 [SYS Power (+3.3V/+5V)]Move TP219 from +3VALW_PWM to +3VALW for power test.
- P.63 [SYS Power(+1.05V_VTT)]Add TP504 for +1.05V_VTT power test.
- P.66 [CPU Power_VHCORE]Add TP507, TP223, TP224 for VHCORE power test.
- P.67 [CPU Power_VID]Add TP225~ TP233 for power test.
- P.68 [VGFX Power_GFXCORE]Add TP508 for GFXCORE power test.

(2009/09/03)

- P.43 [Status LED & LID]Move R390/R384 to Drain side of Q51/Q48 for MOR comment.
- P.25 [LVDS Connector]Change CN13 to M870 type (1N-0040000-FWGO).
- P.47 [SWITCH DB Conn.]Change CN2 to 12pin type (1N-0012002-F0T0).
- P.50 [SWITCH (Botton & KB LED)*]Change P_CN3 to 12pin type (1N-0012002-F0T0).
- P.50 [SWITCH (Botton & KB LED)*]Move NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit to MB for MOR comment.
- P.43 [Status LED & LID]Add NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit for MOR comment.
- P.09 [ARD (RESERVED)]Del test points for MOR comment.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Del test points for MOR comment.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del test points for MOR comment.
- Test Points[TP109/TP193/TP181/TP208/TP209/TP211/TP210/TP212/T213/TP214/TP235/TP236/TP265/TP266/TP237/TP239/TP327/TP328/TP329/TP256/TP257/TP259/TP260/TP262/TP263/TP264/TP284/TP287/TP288/TP289/TP290/TP291/TP292/TP293/TP294/TP295/TP296/TP297/TP298/TP425/TP1116/TP1117/TP1118/TP1119/TP140/TP147/TP148/TP149/TP148/TP145/TP144/TP134TP1120/TP1121/TP1122/TP1123/TP1124/TP188/TP183/TP88/TP91/TP93/TP101/TP412/TP416/TP415/TP417/TP414/TP421/TP422/TP423/TP424]
- P.09 [ARD (RESERVED)]Del RP87 for MOR and Intel comment.
- P.43 [Status LED & LID]Add LED test points TP1223/TP1224/TP1225/TP1226/TP1227/TP1228/TP1229/TP1230.
- P.10 [PCH (HDA,JTAG,SAT)]Change U98 to W25Q32BVSSIG.
- P.51 [AUDIO (CODEC)*]Del U_U7 and U_C155 for Realtek suggestion.
- P.16 [PCH (POWER) 1/2]Del R897, R989 for MOR comment.
- P.17 [PCH (POWER) 2/2]Del R428, R958 for MOR comment.
- P.04 [ARD (CLK,MISC,JTAG)]Add R5950, C6327, R5951, R5949, R5948, C6326 for Intel S3 issue.

(2009/09/08)

- P.51 [AUDIO (CODEC)*]Change U_R327 to 1K.
- P.59 [DCIN&Charger]NC PR33 for costdown.
- P.70 [OVP protection]PR167 change to 26.1K, PR169 change to 80.6K , PR171 change to 18.2K for OVP Adjust
- P.70 [OVP protection]Use SW PWRLIMIT function replaced HW PWRLIMIT circuit for costdown. (NC PU31, PC567, PR223, PR629, PR219, PR218, PR78, PC46.)
- P.50 [SWITCH (Botton & KB LED)*]Change P_VR1/P_VR2/P_VR3/P_VR4 to 19-MLVS060-5000.
- P.27 [EC+KBC (NPCE783L)]Change C27/C26 to 15p for Crystal vendor comment.
- P.10 [PCH (HDA,JTAG,SAT)]Change C727/C702 to 15p for Crystal vendor comment.
- P.38 [PCIE (MS) 1/2]Change C785/C786 to 22p for Crystal vendor comment.
- P.11 [PCH (PCI-E,SMBUS,CLK)]Change C1288/C1289 to 27p for Crystal vendor comment.
- P.43 [Status LED & LID]Change TP1228 to connect to R692 pin2.
- P.37 [eSATA Combo Conn.]Add eSATA reperator schematic and NC it.
- P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to GB5RF120-1203-7F for Halgen Free.
- P.30 [Debug Port]Change CN30 to GB5RF120-1203-7F for Halgen Free.
- P.42 [Felica Connector]Add Felica power supply schematic as Pokerman type for MOR request.
- P.14 [PCH (PCI,USB,NVRAM)]Change USB_OC# signal to EVT type for MOR request.
- P.29 [SPI Flash ROM]Change U23 to W25X10BVSNIIG for SW comment.
- P.51 [AUDIO (CODEC)*]Move U_R5774 to P.48 and rename to R5774.
- P.49 [AUDIO/USB DB Conn.]NC +12V and add a +5VALW pin for USB VEVS test.
- P.54 [AUDIO (AUDIO & USB Conn)*]NC U_+12V and add a U_+5VALW pin for USB VEVS test.
- P.49 [AUDIO/USB DB Conn.]Change CN31 to 1N-0050004-F0T0 for ME request.
- P.54 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 to 1N-0050004-F0T0 for ME request.
- P.33 [LAN (88E8057) 1/2]Add R5965/R5966/R5967 for 88E8057/88E8059 co-lay.
- P.49 [AUDIO/USB DB Conn.]Change CN31 Pin 43 to GND.
- P.54 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 Pin 43 to GND.

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- P.43 [Status LED & LID]Change Q49/Q179/Q180/Q181 to 17-DTA114Y-UB00 for PUR suggest.
- P.32 [Mini-PCIE Card (WLAN)]Change Q5 to 17-DTC144E-UB00 for PUR suggest.
- P.22 [CRT]Change Q11 to 17-DTC144E-UB00 for PUR suggest.
- P.44 [FAN]Change Q77 to 17-DTC144E-UB00 for PUR suggest.
- P.59 [DCIN&Charger]Change TP1148,TP1149,TP1150,TP1151 from DC_IN_1 to P+ for power test.
- P.59 [DCIN&Charger]Change PQ16,PR76,PR77 from NC to mount for EC PWRLIMIT function.
- P.59 [DCIN&Charger]Change PR79 from 0 to 3.48K, change PR11 from 20K to 12K for EC PWRLIMIT function.
- P.61 [Identify IC]Add PD31 and change PR68 from 10K to 4.7K for MOR side request.
- P.69 [Others power plan]Delete TP189,TP203 for power test.

(2009/09/09)

- P.30 [Debug Port]Del TP1186~TP1193.
- P.25 [LVDS Connector]Add L_DDC_CLK/L_DDC_DATA for EDID function.
- P.13 [PCH (LVDS,DDI)]Add L_DDC_CLK/L_DDC_DATA for EDID function.
- P.62 [SYS Power (+3_3V/+5V)]Change PR652,PR245 from NC to mount 4.7ohm. Change PC568,PC272 from NC to mount 680pF for EMI suggest.
- P.63 [SYS Power(+1_05V_VTT)]Change PR188 from NC to mount 4.7ohm, Change PC170 from NC to 680pF for EMI suggest.
- P.64 [DDR3 Power(+1_5V/+0_75V)]Change PR41 from NC to mount 4.7ohm, Change PC42 from NC to mount 680pF for EMI suggest.
- P.68 [VGFX Power_GFXCORE]Change PR527 from NC to mount 4.7ohm, Change PC225 from NC to mount 680pF for EMI suggest.
- P.40 [Camera Connector]Del R5926/R5927 and add L76/L77 for EMC request for DMIC noise.
- P.40 [Camera Connector]Mount C6314/C6315 for EMC request for DMIC noise.
- P.48 [AUDIO Speaker Conn]Del RR5876, R5877, R5878, R5879 and Add L78, L79, L80, L81 for EMC request to filtrate SPK noise.
- P.25 [LVDS Connector]Add C6334/C6335 for EMC request for 150MHz powerbase issue.
- P.42 [Felica Connector]Change Felica power supply from +5VSUS to +3VSUS.
- P.39 [PCIE (SD) 2/2]Change R391 to 100K for MOR request.
- P.31 [Express Card]NC Q38, R5457 and mount R686 for MOR comment.

(2009/09/10)

- P.25 [LVDS Connector]Add CN13 Pin40 for EDID function.
- P.32 [Mini-PCIE Card (WLAN)]Add C6339/C6340 for EMI request.
- P.16 [PCH (POWER) 1/2]Add C6336/C6337/C6338 for EMI request.
- P.50 [SWITCH (Botton & KB LED)*]Change P_LED1/P_LED2/P_LED3 to HT-170UYG.
- P.63 [VTT&PCH Power(+1_05V)]Del PJ22 and add L82 for EMI request for 150MHz powerbase issue.
- P.69 [Others power plane]Add C6342/C6343 on +3VSUS for EMI request.
- P.69 [Others power plane]Add C6344/C6345/C6346 on +3VRUN for EMI request.
- P.33 [LAN (88E8059) 1/2]Del R97 and add C6341 for Marvell FAE request.
- P.33 [LAN (88E8059) 1/2]Del R5966, R5967 for Marvell FAE request.
- P.45 [LAN (88E8059) 1/2]Change C993 to 10u for Marvell FAE request.
- P.31 [Express Card]Correct Express Card SPEC.
- P.46 [Thermal Sensor]NC U28 and related schematic for MOR request.
- P.36 [SATA CD-ROM]Del CN37 for MOR request.
- P.49 [AUDIO/USB DB Conn.]Add F1 for MOR comment.
- P.54 [AUDIO (AUDIO & USB Conn)*]rename U_+5VALW to U_+5VALW_IN for MOR comment.
- P.57 [AUDIO (USB)*]Del U_F1 and rename U_+5VALW to U_+5VALW_IN for MOR comment.
- P.71 [HOLE & AMI LABEL]Del BOSS2 for MOR request.
- P.51 [AUDIO (CODEC)*]Change U_R321 to 100K for MOR request.
- P.52 [AUDIO (MUTE)*]NC U_C472 for MOR comment.
- P.56 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
- P.56 [AUDIO (Ext MIC Jack)*]Del U_C26, U_C31 and add U_R5791, U_R5792 for MOR comment.
- P.56 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
- P.63 [AUDIO (CODEC)*]NC U_C923.
- P.55 [AUDIO (Head Phone Jack)*]Change U_GND to U_A_GND for Realtek FAE suggest.

P.25 [LVDS Connector]NC CN13 Pin7.

(2009/09/11)

- P.59 [DCIN&Charger]Change PR15 to RLM12FTSR020 for PUR request.
- P.59 [DCIN&Charger]Change PF1 to 0437007.WR for PUR request.
- P.25 [LVDS Connector]Change CN13 for Halgen-free.
- P.48 [AUDIO Speaker Conn]Swap JSPK1 for layout concern.
- P.32 [Mini-PCIE Card (WLAN)]Change SW4 to 1BS007-12110-002-7H for ME request.
- P.43 [Status LED & LID]Change LED3/LED4 vendor to Everlight.
- P.55 [AUDIO (Head Phone Jack)*]Change U_A_GND to U_GND for Realtek FAE suggest.
- P.51 [PCIE (SD) 2/2]Change CN29 to WK21923-S6P3-4H for ME request.
- P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to No Halgen-free.
- P.30 [Debug Port]Change CN30 to No Halgen-free.
- P.50 [SWITCH (Botton & KB LED)*]Change P_CN3 to No Halgen-free.
- P.47 [SWITCH DB Conn.]Change CN2 to No Halgen-free.
- P.44 [FAN]Change CN14 to No Halgen-free.
- P.48 [AUDIO Speaker Conn]Change JSPK1 to No Halgen-free.
- P.71 [HOLE & AMI LABEL]Change H2/H4/H5 for ME request.
- P.27 [EC+KBC (NPCE783L)]NC U216 Pin8 and del R575.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect DIS_FAN_MON# to U69F GPIO57 and pull-high to +3VRUN.
- P.27 [EC+KBC (NPCE783L)]NC U4A Pin20 and add SYSTEM_ID1 off-page.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID1 to U69F GPIO17 and del R965.
- P.27 [EC+KBC (NPCE783L)]NC U4A Pin27 and add SYSTEM_ID0 off-page.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID0 to U69F GPIO16 and NC RP19 Pin7.
- P.27 [EC+KBC (NPCE783L)]NC U216 Pin9.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect PM_SLP_ME# to U4B GPIO26.
- P.27 [EC+KBC (NPCE783L)]Del R5853 and connect INST_ON_SW# to GPIO12.
- P.27 [EC+KBC (NPCE783L)]NC U216 Pin3 and connect WLAN_EN to U4A Pin20.
- P.27 [EC+KBC (NPCE783L)]NC U216 Pin4 and connect BT_ON to U4A Pin27.
- P.27 [EC+KBC (NPCE783L)]NC U216 Pin5/Pin6 and connect AC_OFF/EC_PWRLIMIT_CTRL to U4A Pin19/Pin120.
- P.27 [EC+KBC (NPCE783L)]Del R5855/R5856/C6201/C6202.
- P.27 [EC+KBC (NPCE783L)]Connect AC Present to U4A Pin124.
- P.27 [EC+KBC (NPCE783L)]Del U216/R5857/C6203.
- P.22 [CRT]Del F2 for MOR comment.
- P.51 [AUDIO (CODEC)*]Del U_R5773/U_Q64/U_R5771/U_R5783/U_U215/U_R5784 for MOR comment.
- P.51 [AUDIO (CODEC)*]Move U_AMP_PD# to U_U18 Pin4.
- P.52 [AUDIO (MUTE)*]Mount U_R352/U_R351/U_Q17/U_R349/U_Q15/U_R341 for MOR comment.
- P.22 [CRT]NC R5752 for no need of semi-PNP function.

(2009/09/12)

- P.01 [Index page]Update information.
- P.02 [BLOCK DIAGRAM]Update information.
- P.10 [PCH (HDA,JTAG,SAT)]Update SPI ROM information.
- P.37 [eSATA Combo Conn.]Del F10 for no need.
- P.25 [LVDS Connector]Add F16/L83 to follow M870.
- P.10 [PCH (HDA,JTAG,SAT)]Add 100K pull-low resistors R5966/R5867/R5968 on SPI0_MOSI/SPI0_CLK/SPI0_CS# for Intel EDS request.
- P.07 [ARD (GRAPHICS POWER)]Change R401 to 1R-0000103-J200.
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R943/R974/R982/R1626 to 1R-0000103-J200.
- P.52 [AUDIO (MUTE)*]Change U_R340/U_R350/U_R663 to 1R-0000103-J200.
- P.51 [AUDIO (CODEC)*]Change U_R652/U_R662 to 1R-0000103-J200.
- P.40 [Camera Connector]Add R5969/F17 for adding fuse solution.
- P.25 [LVDS Connector]NC CN13 Pin1/Pin5/Pin6 for del EDID function.
- P.13 [PCH (LVDS,DDI)]Del L_DDC_CLK/L_DDC_DATA for del EDID function.
- P.20 [DDRIII (SO-DIMM_0) 1/2]NC CAP13 for no need.
- P.21 [DDRIII (SO-DIMM_1) 2/2]NC CAP22 for no need.
- P.37 [eSATA Combo Conn.]Swap L62/L66 for layout request.

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- P.51 [AUDIO (CODEC)*]Change the setting to ALC269 (NC: U_C441/R5943/U_R5789, Stuff U_C930/R5944/U_R5790).
- P.59 [DCIN&Charger]Change PL3 to NC for costdown.
- P.63 [VTT&PCH Power(+1_05V)]Change PR44 from 0ohm to 2.2ohm for vendor suggest.
- P.64 [DDR3 Power (+1_5V/+0_75V)]Change PR39 from 0ohm to 2.2ohm for vendor suggest.

- P.45 [Touch Pad]Del F12 for no need.
- P.23 [LVDS]Update Panel ID information.
- P.51 [AUDIO (CODEC)*]Change U_C787/U_C476/U_C459 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.65 [SYS Power(+1_8V)]Change PC247 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.53 [AUDIO (Power)*]Change U_C467 to 1C-2B20103-K200 for MOR comment to use the same kind of Capacitor.
- P.38 [PCIE (MS) 1/2]Change R5911/R5912/R5909/R5910/R5913/R5914/R5915/R5916/R5917 to 33ohm for correcting SI test fail.
- P.39 [PCIE (SD) 2/2]Change R5918/R5919/R5920/R5921/R5922 to 33ohm for correcting SI test fail.

(2009/09/13)

- P.22 [CRT]Change CN20 to DZ11A91-SB281-4H for different package.
- P.56 [AUDIO (Ext MIC Jack)*]Change U_CN5 to JA63331-R1T0-7H for ME request.

(2009/09/14)

- P.63 [VTT&PCH Power(+1_05V)]Del PJ23 for layout space lack.
- P.33 [LAN (88E8059) 1/2]Change C995 to 10uF for Marvell comment.
- P.62 [SYS Power (+3_3V/+5V)] Change PR122/PR201 to 2.2 ohm for RF noise.
- P.66 [CPU Power VHCORE] Change PR563 to NC, change PU28 pin25 connect to PROCHOT# for design change.
- P.04 [ARD (CLK,MISC,JTAG)]Add off-page PROCHOT#.
- P.42 [Felica Connector]NC R5963/F15, stuff C869/U48/R630/C845/R5964 for Felica fuse solution fail.
- P.37 [eSATA Combo Conn.]Add R5971/R5972/R5973/R5974 to reduce the trace length on U214 for vendor request.

(2009/09/15)

- P.11 [PCH (PCI-E,SMBUS,CLK)]Make R902/R903 from +3VRUN pull-high to +3VALW pull-high for Intel recommendation.
- P.26 [HDMI]Change CN21 to DF03-577-1931.

(2009/09/16)

- P.14 [PCH (PCI,USB,NVRAM)]NC R1466 for Intel Braidwood disable guideline.

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(2009/11/4)

- P.07 [ARD (GRAPHICS POWER)] Delete PJ43 for redundant design of EVT & DVT
- P.22 [CRT] Add F18 for current limit by MOR comment
- P.62 [SYS Power (+3_3V/+5V)] Delete PJ11 and PJ12 for redundant design of EVT & DVT
- P.64 [DDR3 Power(+1_5V/+0_75V)] Delete PJ26 and PJ27 for redundant design of EVT & DVT
- P.65 [SYS Power(+1_8V)] Delete PJ36 for redundant design of EVT & DVT
- P.66 [CPU Power VHCORE] Change PC112 from 68u_25V to OS_Con cap 47u_25V
- P.68 [VGFX Power GFXCORE] Delete PJ33 for redundant design of EVT & DVT

(2009/11/12)

- P.27 [EC+KBC (NPCE783L)] Add R5975 on OVT_EC# for GPIO70 need pull high
- P.50 [SWITCH (Botton & KB LED)*] Exchange function name for Assist & Web button
- P.23 [LVDS] No mount R5942 to cancell Instant_On function by MOR request
- P.27 [EC+KBC (NPCE783L)] No mount R5851 to cancell Instant_On function by MOR request
- P.43 [Status LED & LID] R689 change resistor value to 300 Ohm, R692 change resistor value to 909 Ohm, R693 change value to 300 Ohm, R5945~R5947 change resistor value to 392 Ohm for LED brightness by MOR request
- P.25 [LVDS Connector] Change CN13 to 1N-004000E-FKG0 for better L6 process
- P.28 [KB Connector] Add TP1233,TP1234 for BFT test
- P.23 [LVDS] Add TP1231,TP1232 for BFT test
- P.39 [PCIE(SD) 2/2] Add TP1235,TP1236 for BFT test
- P.45 [Touch Pad] Add TP1241~TP1246 for BFT test
- P.42 [Felica Connector] Add TP1237~TP1240 for BFT test

(2009/11/16)

- P.59 [DCIN&Charger] change pc126 from 1000P_50V_0603_X7R to 1000pF_50V_0402_X7R for MOR request
- P.66 [CPU Power VHCORE] change pc253 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request
- P.70 [OVP protection] change pc41 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request
- P.61 [Identify IC] Update PU5 schematic symbol
- P.10 [PCH (HDA,JTAG,SAT)] Update U43 schematic symbol
- P.61 [Identify IC] Update PU5 schematic symbol
- P.40 [Camera Connector] L76,L77 change to Bead,MAX ECHO,EBMS100505A121 0.5A, 120ohm/100MHz,25%,0402(1005mm) by MOR request
- P.55 [Audio (Head Phone Jack)*] U_L4,U_L5 change to Bead, MAX ECHO, EBMS100505A121 0.5A,120ohm/100MHz,25%,0402(1005mm) by MOR request
- P.33 [LAN (88E8059) 1/2] C6077 change to SMD,MLCC,X7R,1000pF,50V,10%,0402 by MOR request
- P.51 [AUDIO (CODEC)*] U_C440 change to SMD,MLCC,X7R,1000pF,50V,10%,0402 by MOR request
- P.34 [LAN (Transformer) 2/2] C568 change to SMD,MLCC,X7R,1000pF,50V,10%,0402 by MOR request
- P.45 [Touch Pad] C130,C133 change to SMD,MLCC,NPO,47pF,50V,5%,0402 by MOR request
- P.27 [EC+KBC (NPCE783L)] C22 change to SMD,MLCC,NPO,22pF,50V,5%,0402 by MOR request
- P.38 [PCIE (MS) 1/2] C544,C785,C786 change to SMD,MLCC,NPO,22pF,50V,5%,0402 by MOR request
- P.51 [AUDIO (CODEC)*] U_C439 change to SMD,MLCC,NPO,22pF,50V,5%,0402 by MOR request
- P.52 [AUDIO (MUTE)*] U_R351 change to SMD,RES,200K,1/16W,5%,0402 by MOR request
- P.52 [AUDIO (MUTE)*] U_R352 change to SMD,RES,33K,1/16W,5%,0402 by MOR request
- P.52 [AUDIO (MUTE)*] U_R341,U_R349, change to SMD,RES,10K,1/16W,5%,0402 by MOR request
- P.10 [PCH (HDA,JTAG,SAT)] R5905, change to SMD,RES,51ohm,1/16W,5%,0402 by MOR request
- P.27 [EC+KBC (NPCE783L)] RP1,RP20,RP90 change to SMD,RES,10K,1/16W,5%,0402 and locations are R5984,R5985 & R5976~R5979 by MOR request

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(2009/11/16)

- P.27 [EC+KBC(NPCE783L)] RP21, change to SMD,RES,2.2K,1/16W,5%,0402 and locations are R5982,R5983 by MOR request
- P.27 [EC+KBC(NPCE783L)] RP22, change to SMD,RES,4.7K,1/16W,5%,0402 and locations are R5980,R5981 by MOR request
- P.31 [Express Card] Update U42 Schematic symbol
- P.43 [Status LED & LID] Change TP1224~TP1230 to TOP for BFT test

(2009/11/17)

- P.71 [HOLE & AMI LABEL] Add BOSS2 for M960 wireless card use only
- P.32 [Mini-PCIE Card (WLAN)] Add TP1235~TP1238 on BT_WLAN_SW# & GND for BFT test
- P.33 [LAN (88E8059) 1/2] LAN chip 88E8059 change packing method to tapping for better L6 process
- P.23 [LVDS] SW1 change from 12-pin to 8-pin panel ID SW
- P.15 [PCH (GPIO,VSS_NCTF,RSVD)] NC_R5933 & move R5941 from P.23 to P.15
- P.27 [EC+KBC(NPCE783L)] Move R5942 from P.23 to P.27

(2009/11/18)

- P.45 [Touch Pad] Add F12 for cable short test fail
- P.23 [LVDS] Add test point from TP1251~TP1260 for panel ID switch BFT test
- P.43 [Status LED & LID] Change U21 to E-CMOS EC2618NLB1GR for distance can't meet MOR spec

(2009/11/19)

- P.11 [PCH (PCI-E,SMBUS,CLK)] Reserve R5984~R5992 for Intel FCIM function
- P.64 [DDR3 Power(+1_5V/+0_75V)] Add L84 (3A/120ohm/100MHz,25%,0805) and PR662 2.2ohm, change PR39 from 2.2ohm to 0ohm for EMI request
- P.66 [CPU Power_VHOCORE] Change PR554 and PR558 from 0ohm to 2.2ohm for EMI request
- P.68 [VGFX Power_GFXCORE] Add test point TP509 for low MB GFXCORE voltage SMT power test request

(2009/11/20)

- P.15 [PCH]Change R5941 to mount for Panel ID setting requirement
- P.52 [Audio(Mute)]Change U_R364 from 33kohm to 3.3kohm for satisfy hFE under 100 as MOR's suggestion.
- P.33 [LAN]Change R84 from 4.7kohm to 0ohm for vendor modification

(2009/11/21)

- P.57 [Audio (USB)*]Change the footprint of U_CN2,U_CN3,U_CN6 as SMT suggestion.
- P.30 [Debug Port]Add C6347 for EMI request.
- P.16 [PCH(POWER)]Change C6336,C6337,C6338 from 680p to 2200p and change to mount for EMI request.
- P.54 [AUDIO]Add C6348 for EMI request.
- P.33 [LAN]Add C6349 for EMI request.
- P.34 [LAN]Change L47 from 100R to 300R for EMI request.
- P.59 [DCIN&Charger]: Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf , PC577 4700pf for EMI request, BT+ add PC580 0.1uf,PC581 0.1uf,PC582 4700pf ,PC583 4700pf for EMI request
- P.66 [CPU Power_VHOCORE]:change PC151 and PC156 from NC to mount 0.1uf for EMI request

(2009/11/22)

- P.48 [Audio]Add C6350~C6353 for speaker noise issue.
- P.10 [PCH]Add C6354,C6355 and NC them, reserve for EMI request.
- P.51 [AUDIO]NC U_C439 and add U_C931(NC) for EMI request.
- P.43 [LED]Change R5945,R5946,R5947 from 392ohm to 649ohm and R390 from 120ohm to 261ohm as QA&ME request.
- P.51 [Audio]Change U_R668,U_R665,U_R660,U_R670,U_R672,U_R659(22ohm) from 0402 to 0201 for implement ME solution and layout space is not enough. And change U_R667,U_R664(33kohm), and R5943(NC),R5944(0ohm), and U_R339(20kohm), and U_R338(39.2kohm), and U_R652,U_662(10kohm) from 0402 to 0201 for implement ME solution and layout space is not enough.

(2009/11/22)

- P.64 [DDR3 Power]Delete PC40 for layout space concern.

(2009/11/23)

- P.69 [Other power plane]Change PR661 from 0603 to 0402 for MOR request to cost down.
- P.15 [PCH]Delete RP19 and add R5993,R5994,R5995 for MOR request to cost down.
- P.40 [Camera]Change C9 from 1C-2Y70106-Y001 to 1C-2Y70106-Y000 for MOR request to cost down.
- P.52 [Audio]Change U_Q20 form 2N7002W to SRK7002 for ESD issue.
- P.71 [HOLE]Change H30,H29,H8,H10,H4 hole size as ME's request.
- P.22 [CRT]Change CN20 from FOX_DZ11A91-SB281-4H to FOX_DZ11AE1-SB1SD-4H as ME's request.
- P.49 [Audio/USB DB CONN]Change CN31 from FOX_GB5RF500-1203-7H to FOX_GB5RF500-1203-8H for ME's request.
- P.54 [Audio (Audio/USB CONN)*]Change U_CN1 from FOX_GB5RF500-1203-7H to FOX_GB5RF500-1203-8H as ME's request.
- P.42 [Felica]Change CN7 from FOX_GB5RF060-1203-7H to FOX_GB5RF060-1203-8F as ME's request.
- P.45 [TouchPad]Change CN8 from FOX_GB5RF060-1203-7H to FOX_GB5RF060-1203-8F as ME's request.
- P.10 [PCH]Change C6354 from 0.1uF to 33pF(mount) and R618 from 33ohm to 47ohm as EMC request.
- P.51 [Audio]Change U_R661,U_R671,U_R676,U_673,U_R321 from 0402 to 0201 for layout space concern.

(2009/11/24)

- P.23 [LVDS]Change SW1 from DHNF-04-T-Q-T-R_SW-SMD8P to DHNF-06-T-Q-T/R_SW-SMD12 for shortage issue.

(2009/11/28)

- P.16 [PCH]Change C6336,C6337,C6338 from 1C-2B30222-K000 to 1C-2B30222-M000 for PUR's suggestion.
- P.34 [LAN]Change L47 from 1L-BACMS16-0809 to 1L-BTB1608-080D for PUR's suggestion.
- P.30 [Debug Port]NC CN30 for EMC solution.
- P.29 [SPI Flash ROM]NC U3,R43,C20 and mount R775 for EMC solution.
- P.68 [VGFX Power_GFXCORE]:change PR609 to 470ohm for Intel (#3622146 A Voltage Spike on Graphics Core Rail (Vaxg) to 1.5V seen during System shutdown) request.

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(2009/12/22)

- P.26 [HDMI] Mount R5888 to fix HDMI issue by MOR request
- P.64 [DDR3 Power(+1_5V/+0_75V)] Mount PQ59, change PR600 resistor to 0 Ohm & no mount PR145 to change the enable signal to RUN_PWRGD by MOR request.
- P.26 [HDMI] Change CN21 symbol from 2N-0019007-MKGO to 2N-0019003-MKGO to improve factory process

(2009/12/23)

- P.71 [HOLE & AMI LABEL] Mount AMI label for AMI certificate
- P.10 [PCH (HDA,JTAG,SAT)] No mount CN18, U43, C815, R542 & Mount R1551 for needless in MP
- P.52 [AUDIO (MUTE)*] Change U_Q15 with ESD protection for factory ESD issue

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(2009/12/24)

- P.71 [HOLE & AMI LABEL]Delete BOSS2 for needless from ME's request
- P.34 [LAN(Transformer)]Change L70 from LANKOM to DELTA for LANKOM transformer issue in PVT
- P.33 [LAN]Add R5997 reserve for 8057 solution
- P.04 [ARD]Delete R937,R930 for MOR's request
- P.06 [ARD]Delete R860 for MOR's request
- P.27 [EC]Delete R39,R46 for MOR's request
- P.32 [Mini-PCIE Card]Delete R5901 for MOR's request
- P.45 [Touch Pad]Delete R5869,R5868 for MOR's request

(2009/12/28)

- P.10 [PCH]Change R618 from 47ohm to 68ohm and Change C6355 from NC_0.1uF to mount 22pF for EMC audio FFC issue
- P.51 [Audio]Change U_R326 from 22ohm to 0ohm for EMC audio FFC issue

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