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PCB P/N: 1P-0065102-80SA - FUBAI  
 1P-0065201-80SA - NANYA  
 1P-0065503-80SA - HANNSTAR

Project Code & Schematics Subject: MS60-L Main Board

P. Leader	Check by	Design by

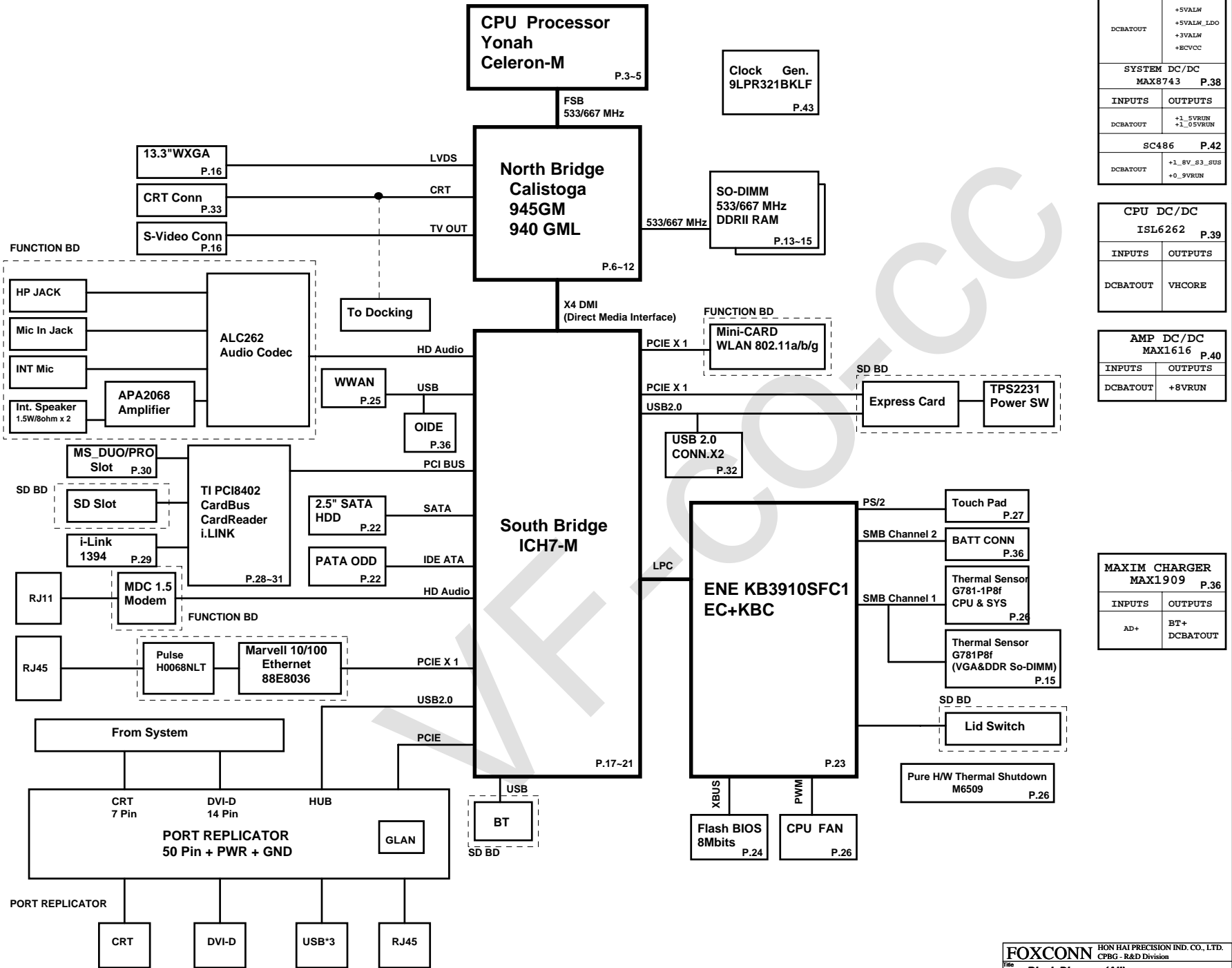
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
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# MS60 (CALISTOGA GM Block Diagram)



SYSTEM DC/DC MAX8734 P.37	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC
SYSTEM DC/DC MAX8743 P.38	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN
SC486 P.42	
DCBATOUT	+1_8V_83_SUS +0_9VRUN

CPU DC/DC ISL6262 P.39	
INPUTS	OUTPUTS
DCBATOUT	VHORE

AMP DC/DC MAX1616 P.40	
INPUTS	OUTPUTS
DCBATOUT	+8VRUN

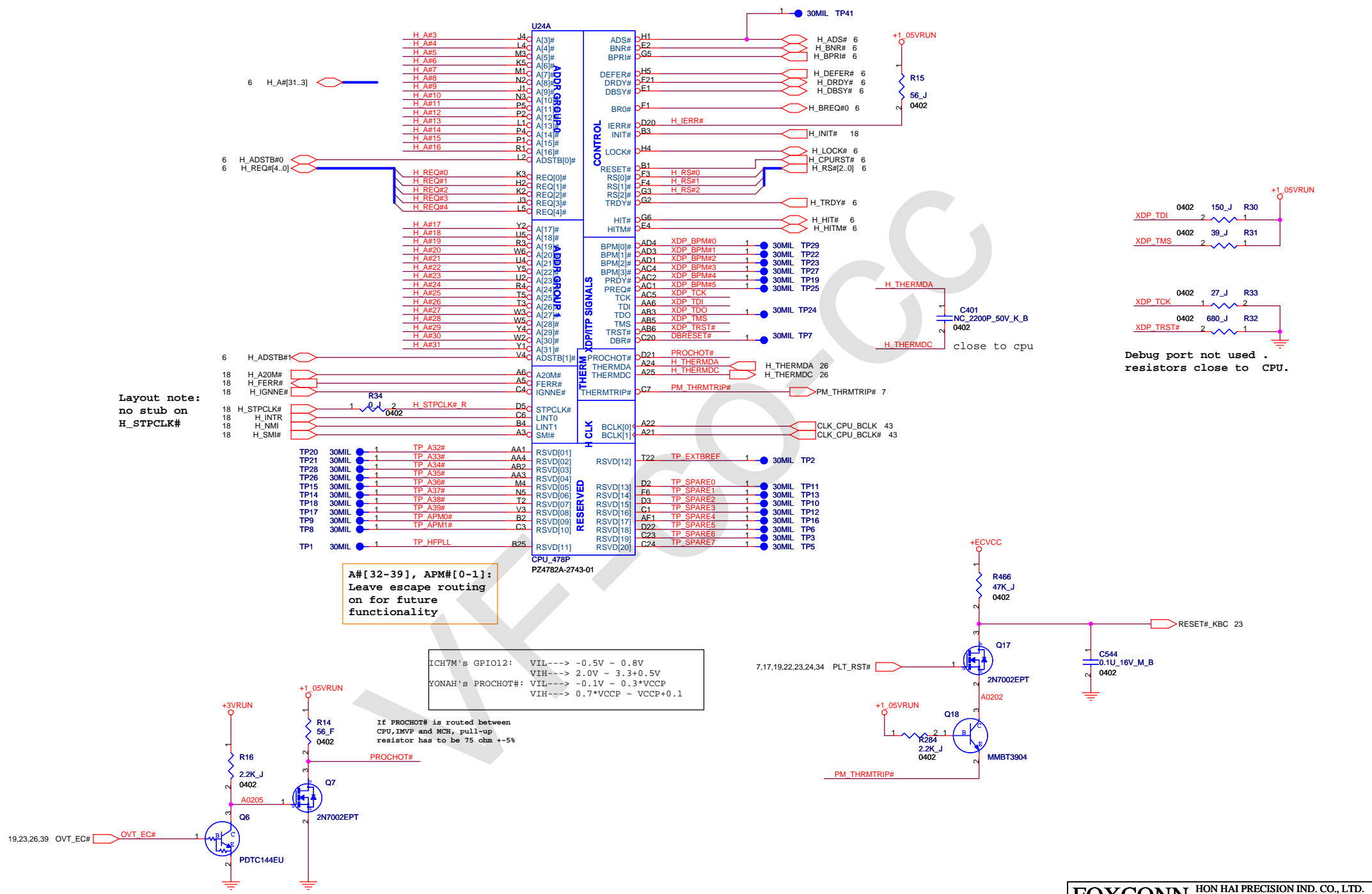
MAXIM CHARGER MAX1909 P.36	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

Layout note:  
no stub on  
H\_STPCLK#

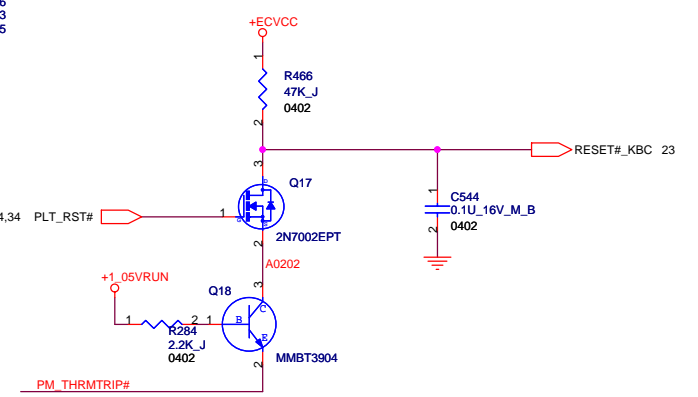
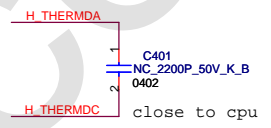
A#[32-39], APM#[0-1]:  
Leave escape routing  
on for future  
functionality

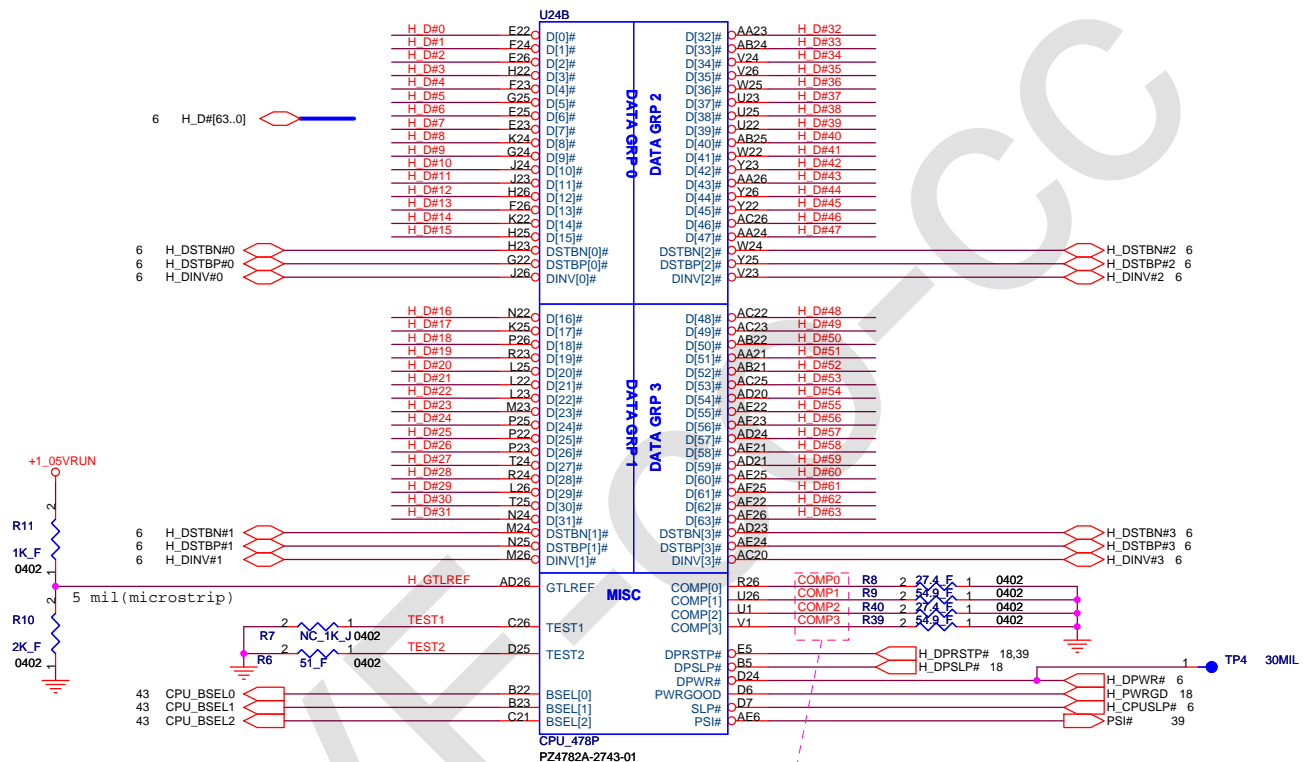
ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V  
VIH----> 2.0V ~ 3.3+0.5V  
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3\*VCCP  
VIH----> 0.7\*VCCP ~ VCCP+0.1

If PROCHOT# is routed between  
CPU,IMVP and MCH, pull-up  
resistor has to be 75 ohm +-5%



Debug port not used.  
resistors close to CPU.





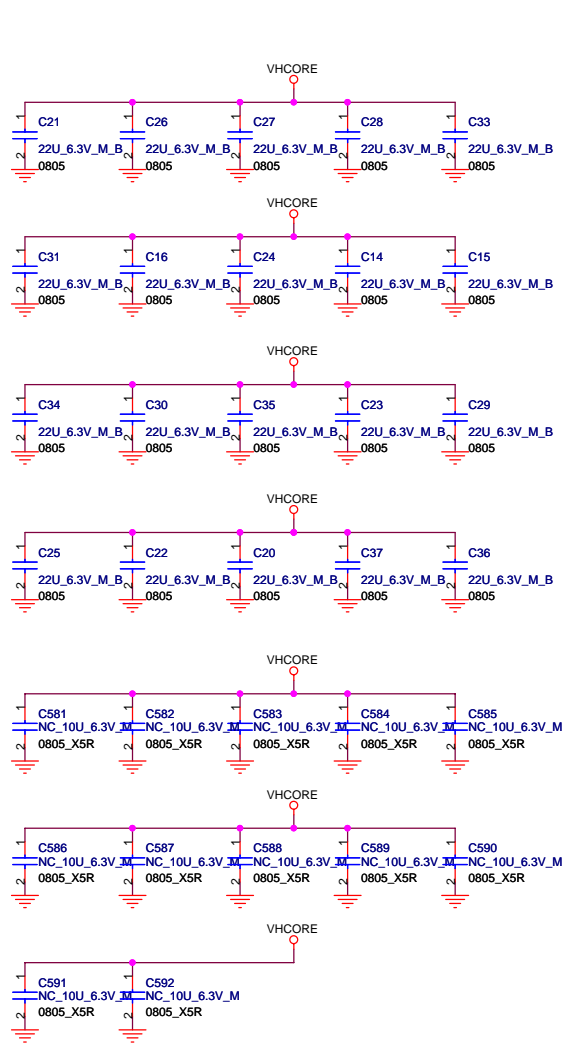
Place close to CPU

Layout Note:  
Z<sub>0</sub>=55 ohm, 0.5"  
max for GTLREF.

**FSB Frequency Table:**

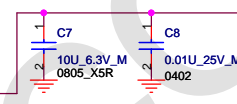
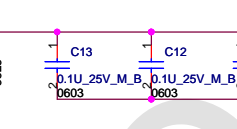
BSEL[2:0]	Freq.(MHz)
LLL	Reserve
LLH	133
LHL	Reserve
LHH	166

Layout Note:  
Comp0,2 connect with Z<sub>0</sub>=27.4 ohm, make trace length shorter then 0.5".  
Comp1,3 connect with Z<sub>0</sub>=55 ohm, make trace length shorter then 0.5".



U24C		U24D	
A7	VCC[001]	A4	VSS[001]
A9	VCC[002]	A8	VSS[002]
A10	VCC[003]	A11	VSS[003]
A12	VCC[004]	A14	VSS[004]
A13	VCC[005]	A16	VSS[005]
A15	VCC[006]	A19	VSS[006]
A17	VCC[007]	A23	VSS[007]
A18	VCC[008]	A26	VSS[008]
A20	VCC[009]	B6	VSS[009]
A21	VCC[010]	B8	VSS[010]
B1	VCC[011]	B11	VSS[011]
B10	VCC[012]	B13	VSS[012]
B12	VCC[013]	B16	VSS[013]
B14	VCC[014]	B19	VSS[014]
B15	VCC[015]	B21	VSS[015]
B17	VCC[016]	B24	VSS[016]
B18	VCC[017]	C5	VSS[017]
B20	VCC[018]	C8	VSS[018]
C9	VCC[019]	C11	VSS[019]
C10	VCC[020]	C14	VSS[020]
C12	VCC[021]	C16	VSS[021]
C13	VCC[022]	C19	VSS[022]
C15	VCC[023]	C22	VSS[023]
C17	VCC[024]	C25	VSS[024]
C18	VCC[025]	D1	VSS[025]
D9	VCC[026]	D11	VSS[026]
D10	VCC[027]	D4	VSS[027]
D12	VCC[028]	D8	VSS[028]
D14	VCC[029]	D11	VSS[029]
D15	VCC[030]	D16	VSS[030]
D17	VCC[031]	D19	VSS[031]
D18	VCC[032]	D23	VSS[032]
E7	VCC[033]	D26	VSS[033]
E9	VCC[034]	E3	VSS[034]
E10	VCC[035]	E6	VSS[035]
E12	VCC[036]	E8	VSS[036]
E13	VCC[037]	E11	VSS[037]
E15	VCC[038]	E14	VSS[038]
E17	VCC[039]	E16	VSS[039]
E18	VCC[040]	E19	VSS[040]
E20	VCC[041]	E21	VSS[041]
F7	VCC[042]	E24	VSS[042]
F10	VCC[043]	F8	VSS[043]
F12	VCC[044]	F11	VSS[044]
F14	VCC[045]	F13	VSS[045]
F15	VCC[046]	F16	VSS[046]
F17	VCC[047]	F19	VSS[047]
F18	VCC[048]	F22	VSS[048]
F20	VCC[049]	F25	VSS[049]
AA7	VCC[050]	G1	VSS[050]
AA9	VCC[051]	G4	VSS[051]
AA10	VCC[052]	G1	VSS[052]
AA12	VCC[053]	G4	VSS[053]
AA13	VCC[054]	G23	VSS[054]
AA15	VCC[055]	G26	VSS[055]
AA17	VCC[056]	H3	VSS[056]
AA18	VCC[057]	H6	VSS[057]
AA20	VCC[058]	H21	VSS[058]
AB9	VCC[059]	H24	VSS[059]
AC10	VCC[060]	H24	VSS[060]
AB10	VCC[061]	J5	VSS[061]
AB12	VCC[062]	J5	VSS[062]
AB14	VCC[063]	J25	VSS[063]
AB15	VCC[064]	K1	VSS[064]
AB17	VCC[065]	K4	VSS[065]
AB18	VCC[066]	K23	VSS[066]
	VCC[067]	K26	VSS[067]
		L3	VSS[068]
		L6	VSS[069]
		L21	VSS[070]
		L24	VSS[071]
		M2	VSS[072]
		M5	VSS[073]
		M22	VSS[074]
		M25	VSS[075]
		N1	VSS[076]
		N4	VSS[077]
		N23	VSS[078]
		N26	VSS[079]
		P3	VSS[080]
			VSS[081]
			VSS[082]
			VSS[083]
			VSS[084]
			VSS[085]
			VSS[086]
			VSS[087]
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			VSS[157]
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			VSS[159]
			VSS[160]
			VSS[161]
			VSS[162]

CPU\_VCCA---->130mA  
 CPU\_VCCP----->2.5A  
 CPU\_VCC----->36A for Yona  
 44A for Merom



maximum current is 130mA for CPU\_VCCA in Merom  
 and 600A/us slew rate for CPU\_VCCA

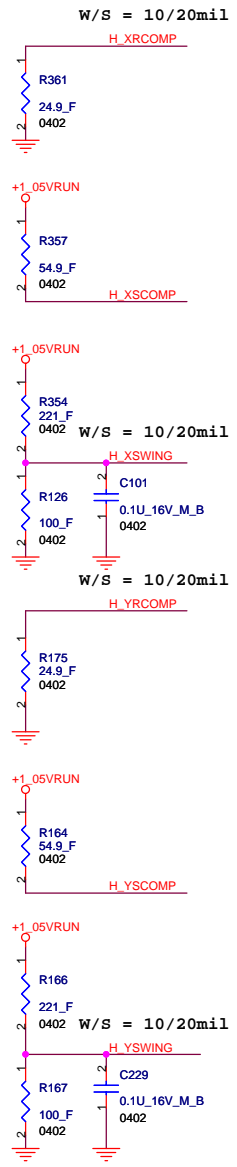
Same Length

Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.  
 width=18 mil  
 spacing=7 mil

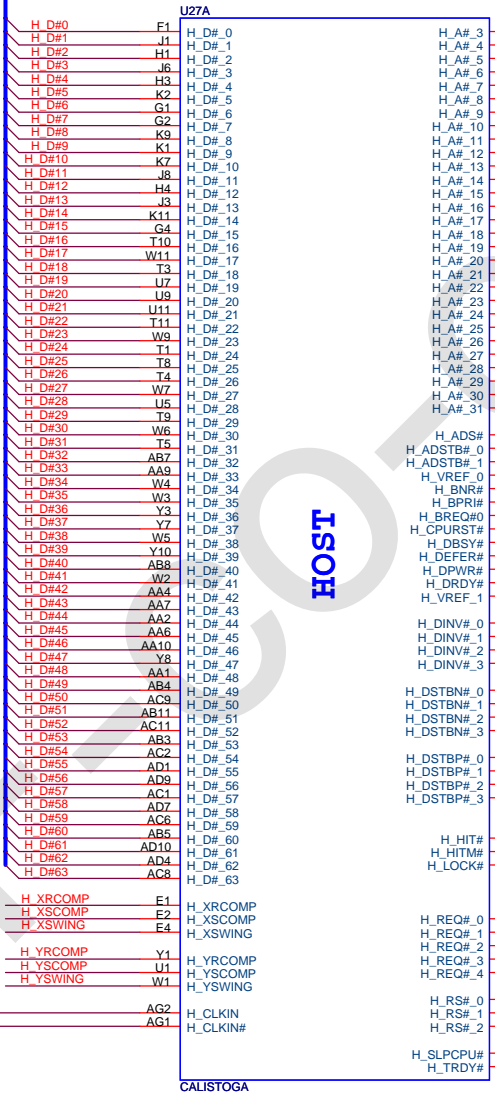
+1.05VRUN  
 100 mil

+1.5VRUN  
 20 mil

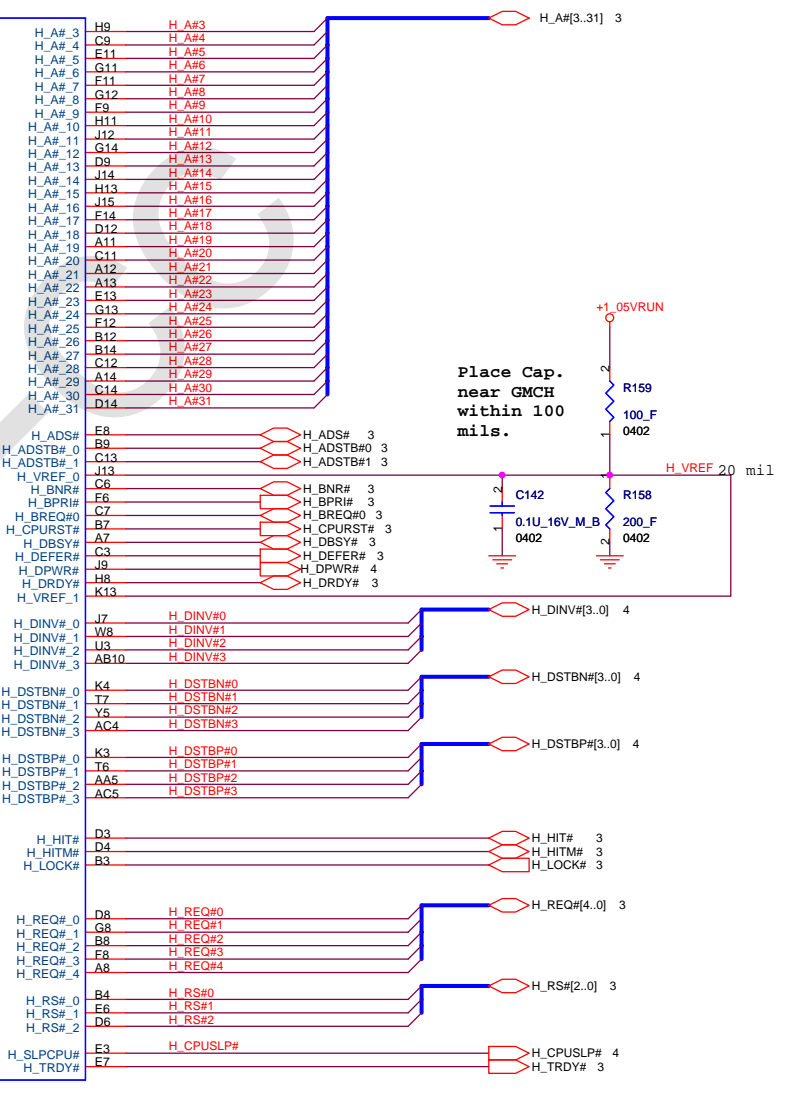
U24D		P6	
A4	VSS[001]	P6	VSS[082]
A8	VSS[002]	P21	VSS[083]
A11	VSS[003]	P24	VSS[084]
A14	VSS[004]	R2	VSS[085]
A16	VSS[005]	R5	VSS[086]
A19	VSS[006]	R22	VSS[087]
A23	VSS[007]	R25	VSS[088]
A26	VSS[008]	T1	VSS[089]
B6	VSS[009]	T4	VSS[090]
B8	VSS[010]	T23	VSS[091]
B11	VSS[011]	T26	VSS[092]
B13	VSS[012]	U3	VSS[093]
B16	VSS[013]	U6	VSS[094]
B19	VSS[014]	U21	VSS[095]
B21	VSS[015]	U24	VSS[096]
B24	VSS[016]	U2	VSS[097]
C5	VSS[017]	V5	VSS[098]
C8	VSS[018]	V22	VSS[099]
C11	VSS[019]	V25	VSS[100]
C14	VSS[020]	W1	VSS[101]
C16	VSS[021]	W4	VSS[102]
C19	VSS[022]	W23	VSS[103]
C22	VSS[023]	W26	VSS[104]
C25	VSS[024]	Y6	VSS[105]
D1	VSS[025]	Y21	VSS[106]
D11	VSS[026]	Y24	VSS[107]
D4	VSS[027]	Y24	VSS[108]
D8	VSS[028]	AA2	VSS[109]
D11	VSS[029]	AA5	VSS[110]
D16	VSS[030]	AA9	VSS[111]
D19	VSS[031]	AA11	VSS[112]
D23	VSS[032]	AA16	VSS[113]
D26	VSS[033]	AA19	VSS[114]
E3	VSS[034]	AA22	VSS[115]
E6	VSS[035]	AA25	VSS[116]
E8	VSS[036]	AA25	VSS[117]
E11	VSS[037]	AB4	VSS[118]
E14	VSS[038]	AB8	VSS[119]
E16	VSS[039]	AB11	VSS[120]
E19	VSS[040]	AB13	VSS[121]
E21	VSS[041]	AB16	VSS[122]
E24	VSS[042]	AB19	VSS[123]
F8	VSS[043]	AB23	VSS[124]
F11	VSS[044]	AC3	VSS[125]
F13	VSS[045]	AC6	VSS[126]
F16	VSS[046]	AC8	VSS[127]
F19	VSS[047]	AC11	VSS[128]
F22	VSS[048]	AC14	VSS[129]
F25	VSS[049]	AC16	VSS[130]
G1	VSS[050]	AC19	VSS[131]
G4	VSS[051]	AC21	VSS[132]
G1	VSS[052]	AC21	VSS[133]
G4	VSS[053]	AC24	VSS[134]
G23	VSS[054]	AD2	VSS[135]
G26	VSS[055]	AD5	VSS[136]
H3	VSS[056]	AD8	VSS[137]
H6	VSS[057]	AD11	VSS[138]
H21	VSS[058]	AD13	VSS[139]
H24	VSS[059]	AD16	VSS[140]
H24	VSS[060]	AD19	VSS[141]
J5	VSS[061]	AD22	VSS[142]
J5	VSS[062]	AD25	VSS[143]
J25	VSS[063]	AE1	VSS[144]
K1	VSS[064]	AE4	VSS[145]
K4	VSS[065]	AE8	VSS[146]
K23	VSS[066]	AE11	VSS[147]
K26	VSS[067]	AE14	VSS[148]
L3	VSS[068]	AE19	VSS[149]
L6	VSS[069]	AE23	VSS[150]
L21	VSS[070]	AE26	VSS[151]
L24	VSS[071]	AE3	VSS[152]
M2	VSS[072]	AE6	VSS[153]
M5	VSS[073]	AE8	VSS[154]
M22	VSS[074]	AE11	VSS[155]
M25	VSS[075]	AE14	VSS[156]
N1	VSS[076]	AE19	VSS[157]
N4	VSS[077]	AE23	VSS[158]
N23	VSS[078]	AE26	VSS[159]
N26	VSS[079]	AF1	VSS[160]
P3	VSS[080]	AF19	VSS[161]
	VSS[081]	AF21	VSS[162]
		AF24	VSS[162]



4 H\_D#[63..0] H\_D#[63..0]



HOST



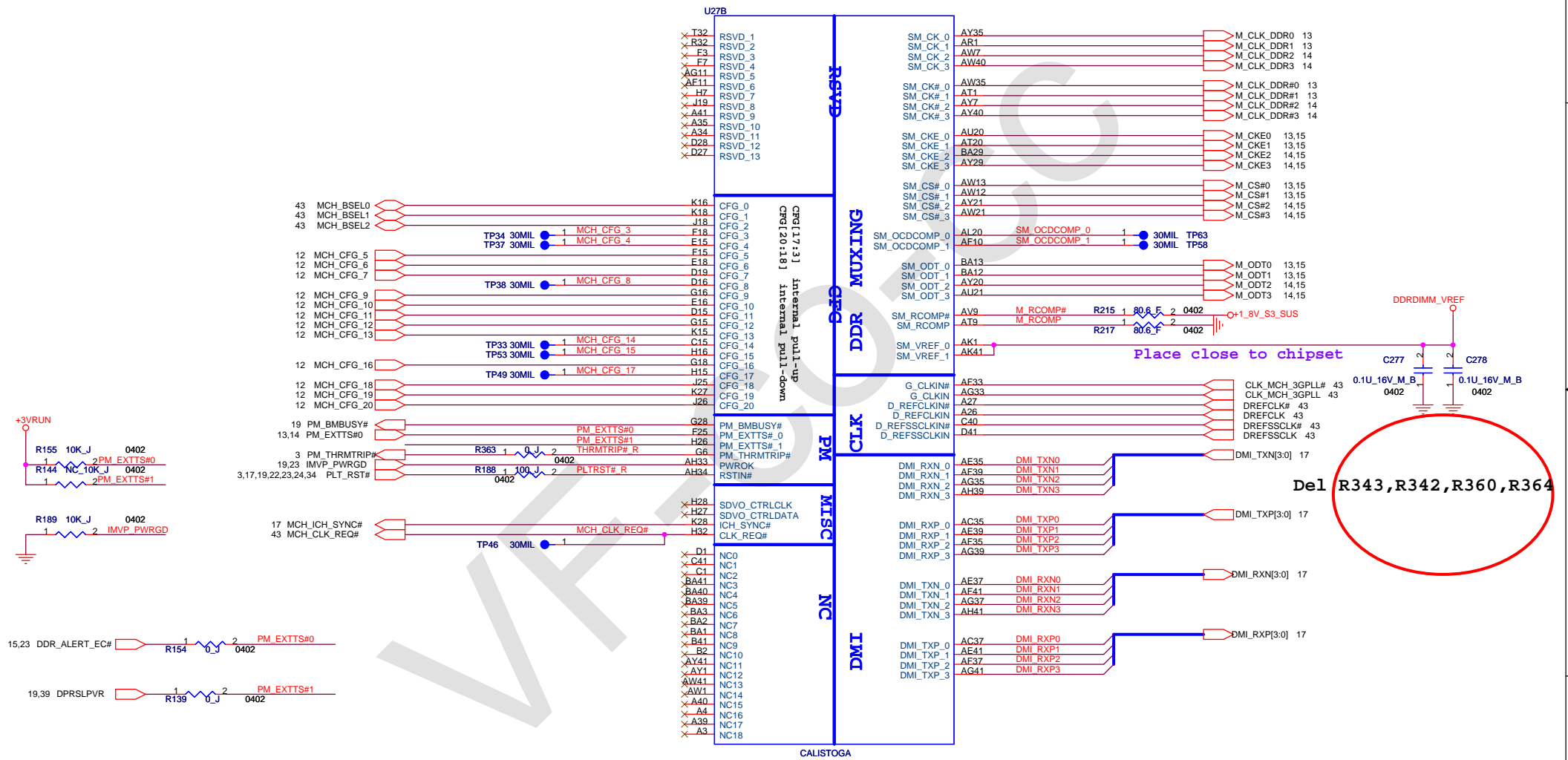
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PM	Q988CPM	12-0G88CPM-0000
GML	940GML-QK60-A3	12-940GML0-A300

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CPBG - R&D Division

Title: **CALISTOHA (HOST)**

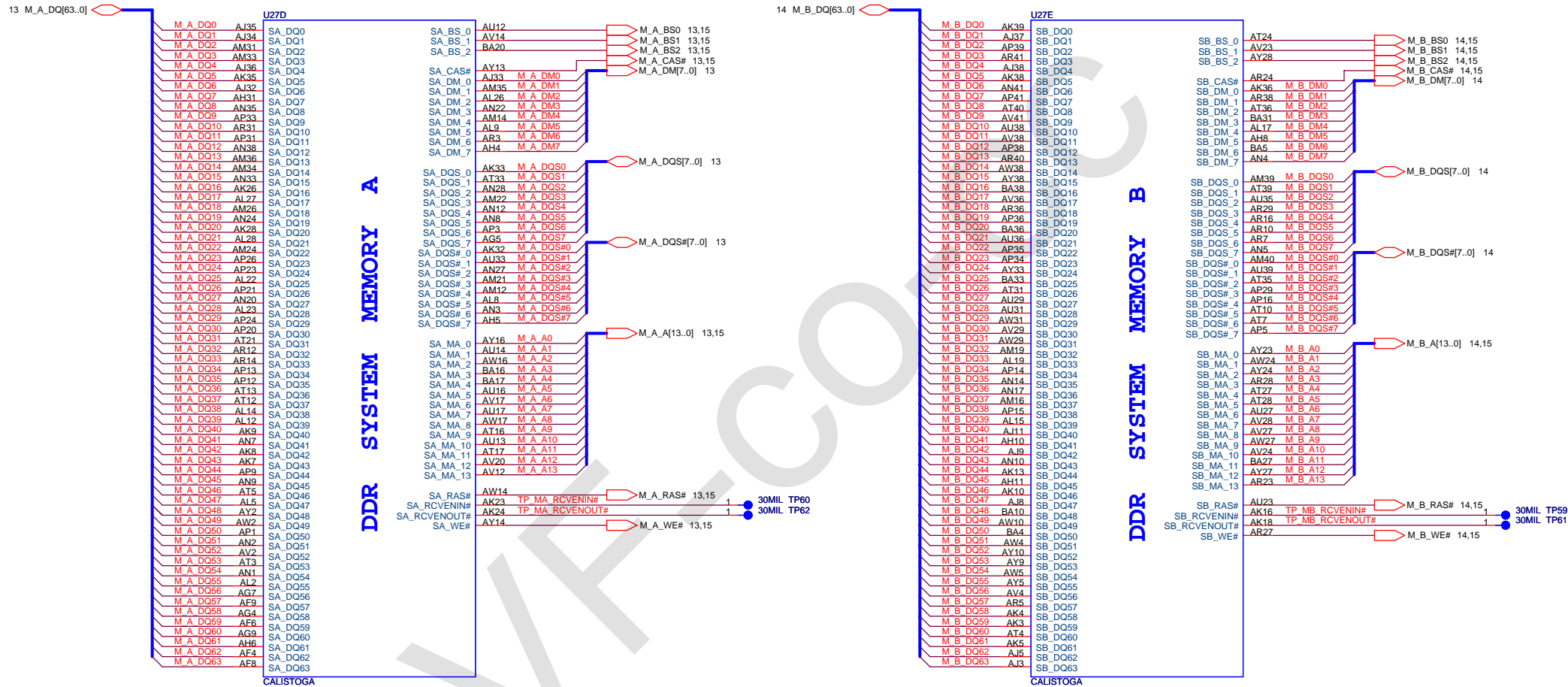
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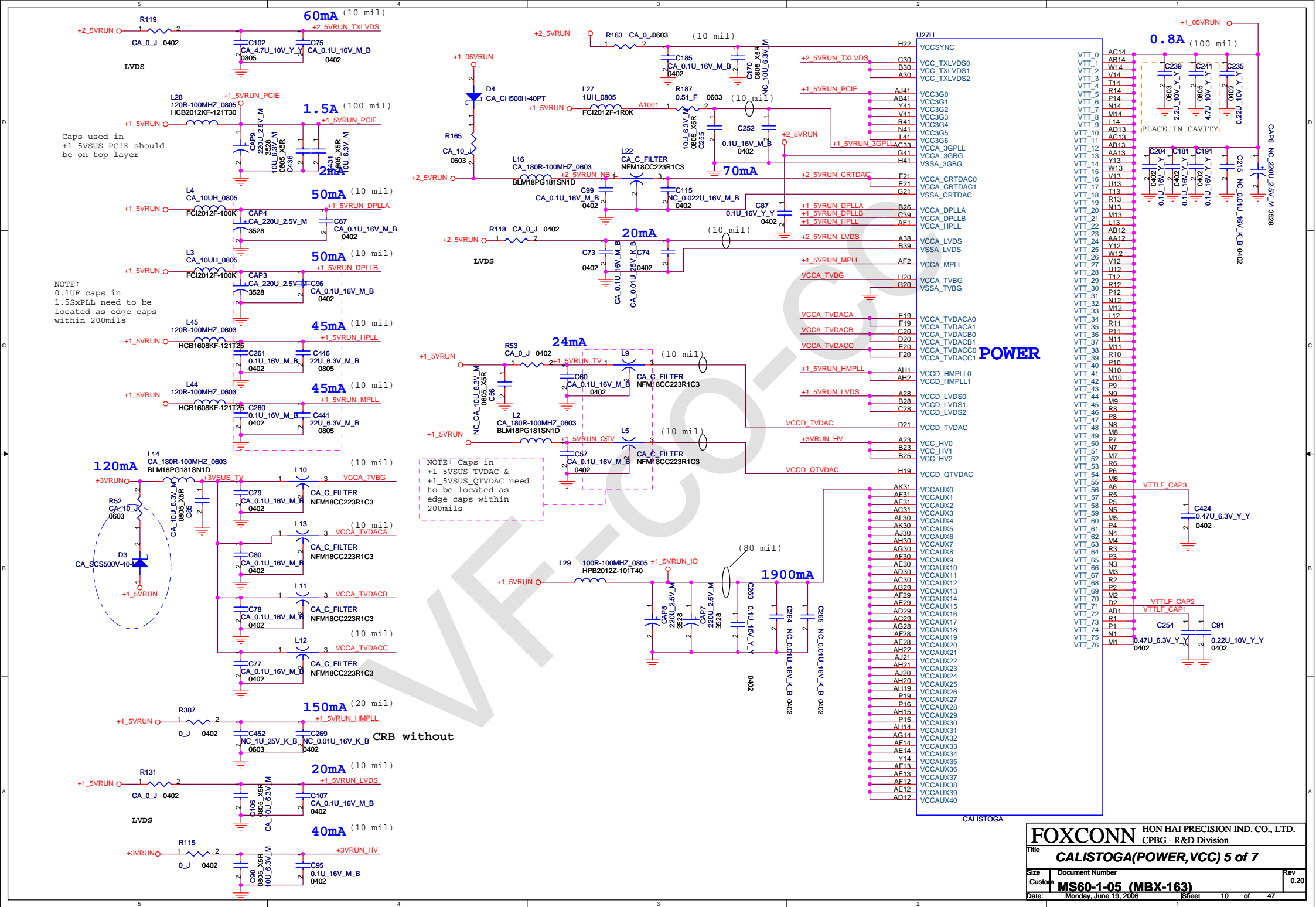
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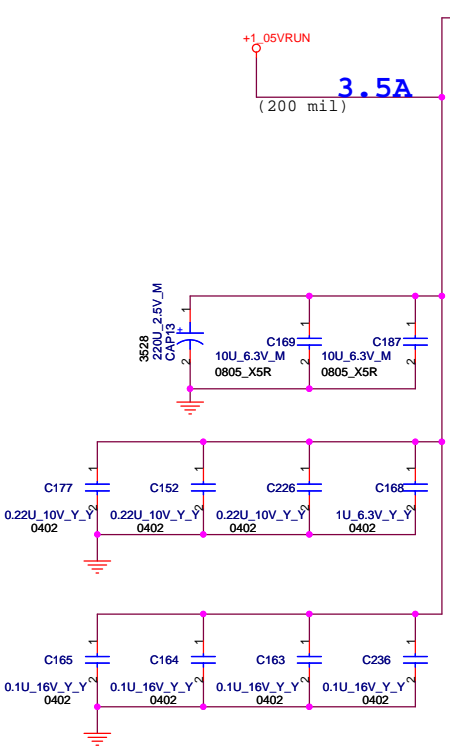


Caps used in +1\_5VSUS\_PCIE should be on top layer

NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200mils

NOTE: Caps in +1\_5VSUS\_TVDAC & +1\_5VSUS\_QTVAC need to be located as edge caps within 200mils

<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
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<b>CALISTOGA(POWER,VCC) 5 of 7</b>			
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Custom	<b>MS60-1-05 (MBX-163)</b>		0.20
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Pin	Signal	Pin	Signal
AA33	VCC_0	AU41	VCCSM LF4
W33	VCC_1	AT41	VCCSM LF5
P33	VCC_2	AM41	
N33	VCC_3	AL40	
L33	VCC_4	BA34	
J33	VCC_5	AY34	
AA32	VCC_6	AW34	
Y32	VCC_7	AV34	
W32	VCC_8	AU34	
V32	VCC_9	AT34	
P32	VCC_10	AR34	
N32	VCC_11	BA30	
M32	VCC_12	AY30	
L32	VCC_13	AW30	
J32	VCC_14	AV30	
AA31	VCC_15	AU30	
W31	VCC_16	AT30	
V31	VCC_17	AR30	
T31	VCC_18	BA30	
R31	VCC_19	AY30	
P31	VCC_20	AW30	
N31	VCC_21	AV30	
M31	VCC_22	AU30	
AA30	VCC_23	AT30	
Y30	VCC_24	AR30	
W30	VCC_25	BA29	
V30	VCC_26	AY29	
U30	VCC_27	AW29	
T30	VCC_28	AV29	
R30	VCC_29	AU29	
P30	VCC_30	AT29	
N30	VCC_31	AR29	
M30	VCC_32	BA29	
L30	VCC_33	AY29	
AA29	VCC_34	AW29	
Y29	VCC_35	AV29	
W29	VCC_36	AU29	
V29	VCC_37	AT29	
U29	VCC_38	AR29	
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V28	VCC_46	BA29	
U28	VCC_47	AY29	
T28	VCC_48	AW29	
R28	VCC_49	AV29	
P28	VCC_50	AU29	
N28	VCC_51	AT29	
M28	VCC_52	AR29	
L28	VCC_53	BA29	
P27	VCC_54	AY29	
N27	VCC_55	AW29	
M27	VCC_56	AV29	
L27	VCC_57	AU29	
P26	VCC_58	AT29	
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L26	VCC_60	BA29	
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M25	VCC_62	AW29	
L25	VCC_63	AV29	
P24	VCC_64	AU29	
N24	VCC_65	AT29	
M24	VCC_66	AR29	
AA23	VCC_67	BA29	
Y23	VCC_68	AY29	
P23	VCC_69	AW29	
N23	VCC_70	AV29	
M23	VCC_71	AU29	
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AC22	VCC_73	AR29	
AB22	VCC_74	BA29	
Y22	VCC_75	AY29	
W22	VCC_76	AW29	
P22	VCC_77	AV29	
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	VCC_110	AW29	
	VCC_110	AV29	
	VCC_110	AU29	

7 MCH\_CFG\_5 ← 1 ● 30MIL TP45

MCH\_CFG\_5  
Low = DMIX2  
High = DMIX4

7 MCH\_CFG\_6 ← 1 ● 30MIL TP40

MCH\_CFG\_6  
Low = Moby Dick  
High = Calistoga  
DDR2 select (default high)

7 MCH\_CFG\_7 ← 1 ● 30MIL TP36

MCH\_CFG\_7 (CPU Strap)  
Low = RSVD  
High = Mobile Yonah processor

7 MCH\_CFG\_9 ← 1 ● 30MIL TP35

MCH\_CFG\_9 (PCIe Graphics Lane)  
Low = Reverse Lane operation  
High = Normal operation

For layout convenience

7 MCH\_CFG\_10 ← 1 ● 30MIL TP35

MCH\_CFG\_10 (HOST PLL VCC SELECT)  
Low = RESERVED  
High = MOBILITY

7 MCH\_CFG\_11 ← 1 ● 30MIL TP35

MCH\_CFG\_11 (PSB 4x CLK ENABLE)  
Low = Reserved  
High = Calistoga

7 MCH\_CFG\_12 ← 1 ● 30MIL TP47

7 MCH\_CFG\_13 ← 1 ● 30MIL TP55

MCH\_CFG\_[13:12] (XOR/ALLZ)  
00=Partial Clock Gating Disable  
01=XOR Mode Enable  
10=All-Z Mode Enable  
11=Normal Operation(Default)

7 MCH\_CFG\_16 ← 1 ● 30MIL TP44

MCH\_CFG\_16 (FSB Dynamic ODT)  
Low = Dynamic ODT Disabled  
High = Dynamic ODT Enable

MCH\_CFG\_18 (VCC\_CORE Select)  
Low = 1.05V(default)  
High = 1.5V

MCH\_CFG\_19 (DMI LANE REVERSAL)  
Low = Normal(default)  
High = LANES REVERSED

MCH\_CFG\_20 (PCIe Backward Interoperability mode)  
Low = Only SDVO or PCIe x1 is operational (defaults)  
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

Layout Noe:  
Location of all MCH\_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

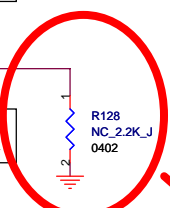
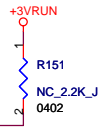
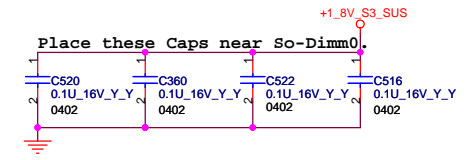
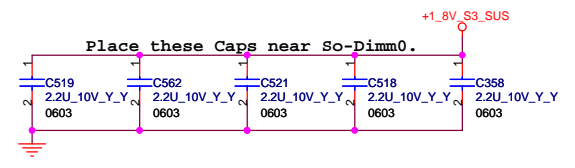
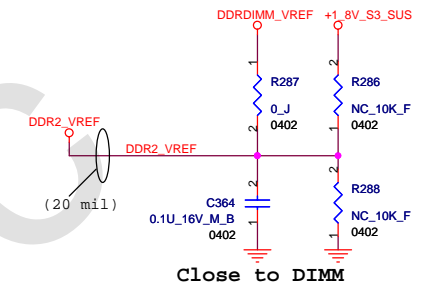
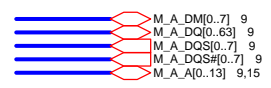
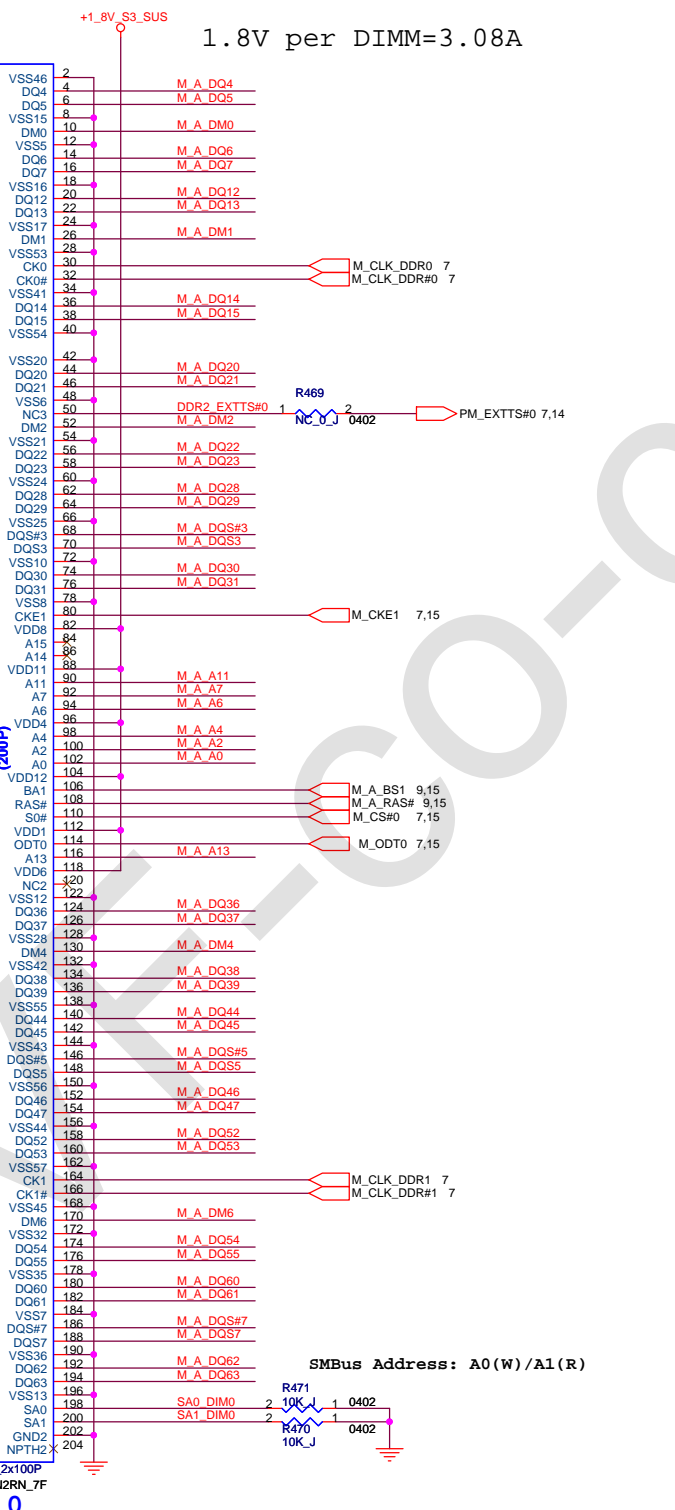
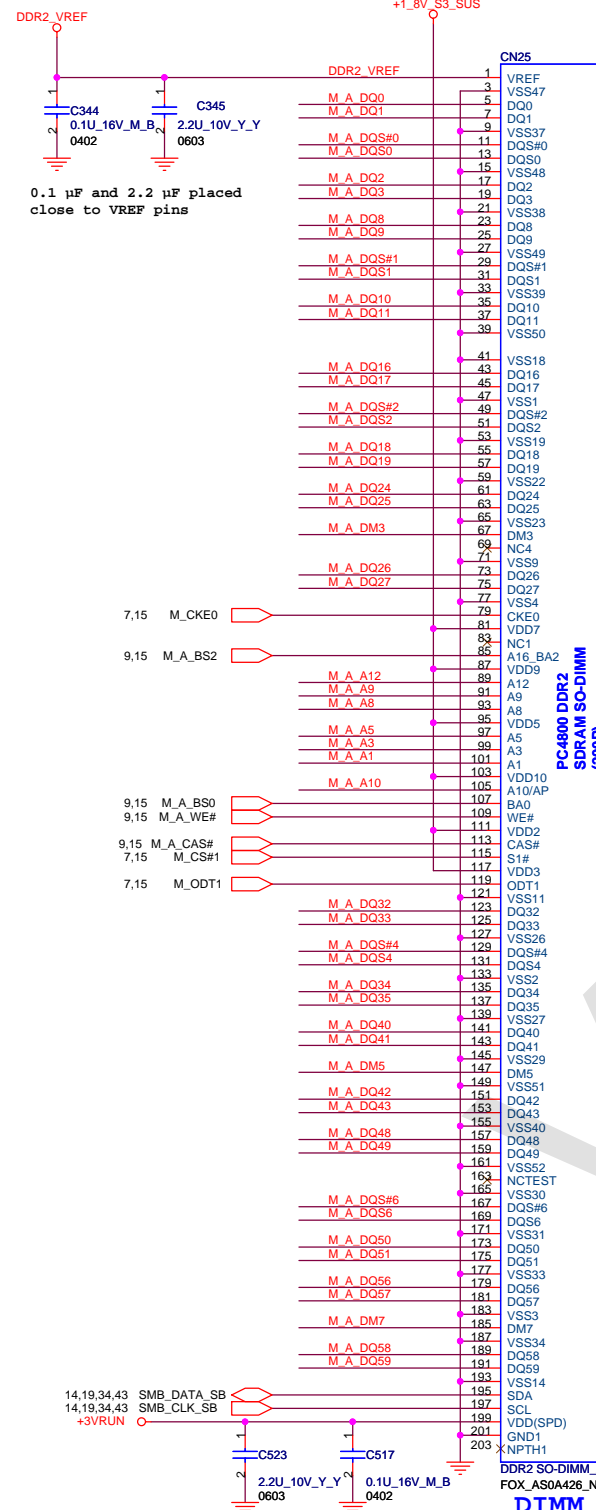


Table listing VSS pins for U271, including pin numbers (e.g., AC41, AA41, W41) and their corresponding VSS identifiers (e.g., VSS\_0, VSS\_1, VSS\_2).

Table listing VSS pins for U27J, including pin numbers (e.g., AT23, AN23, AM23) and their corresponding VSS identifiers (e.g., VSS\_180, VSS\_181, VSS\_182).

Header information for FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division. Title: CALISTOGA(VSS) 7 of 7. Document Number: MS60-1-05 (MBX-163). Date: Monday, June 19, 2006. Sheet 12 of 47. Rev 0.20.

1.8V per DIMM=3.08A

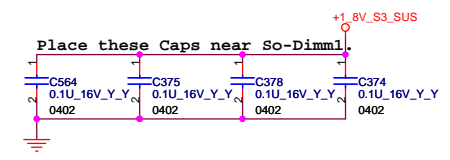
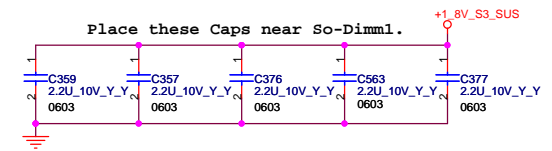
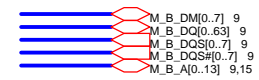
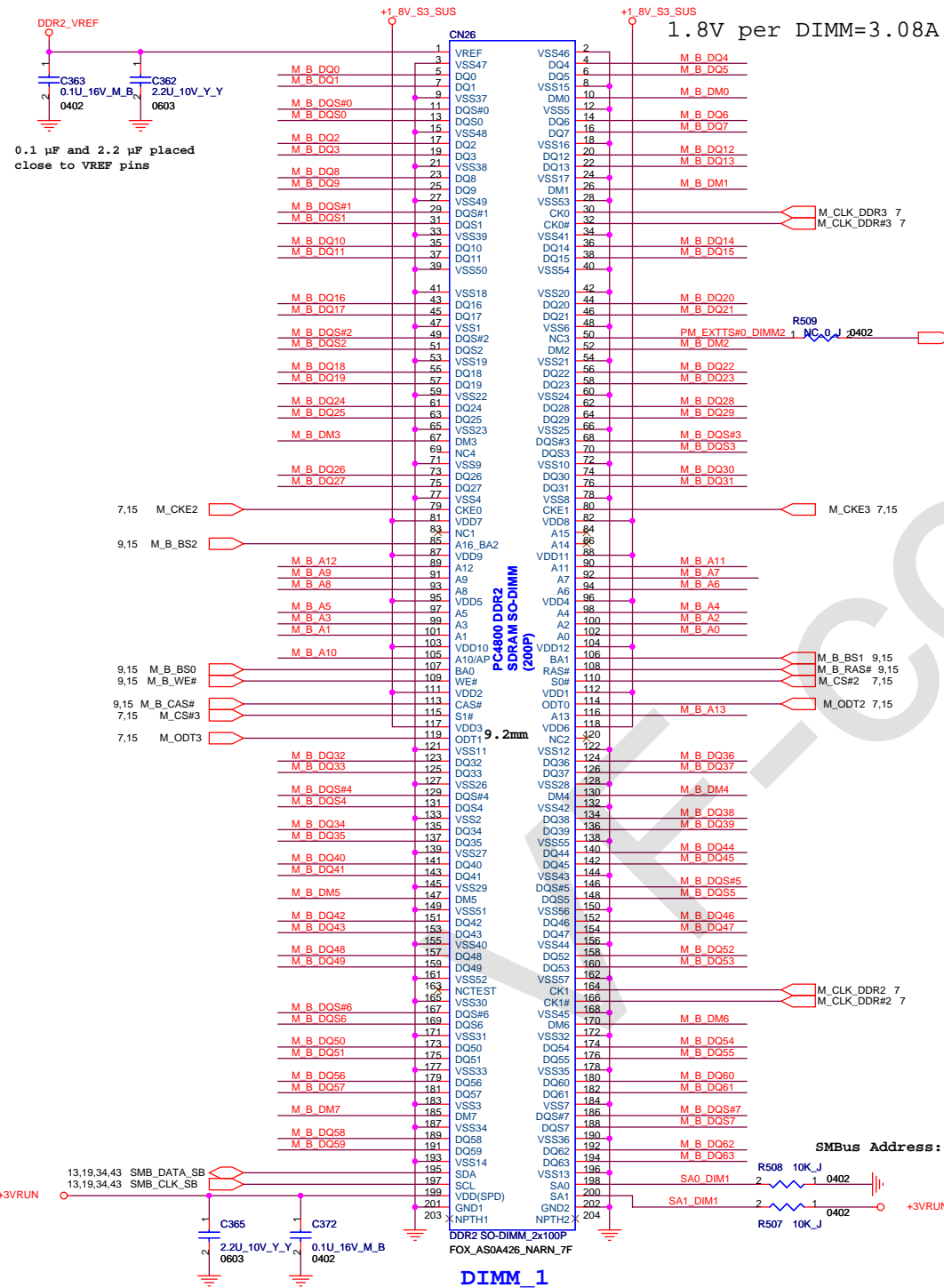


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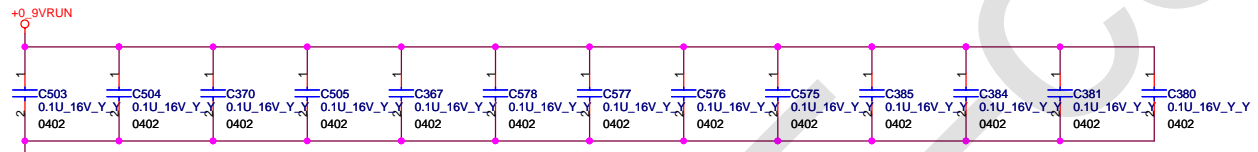
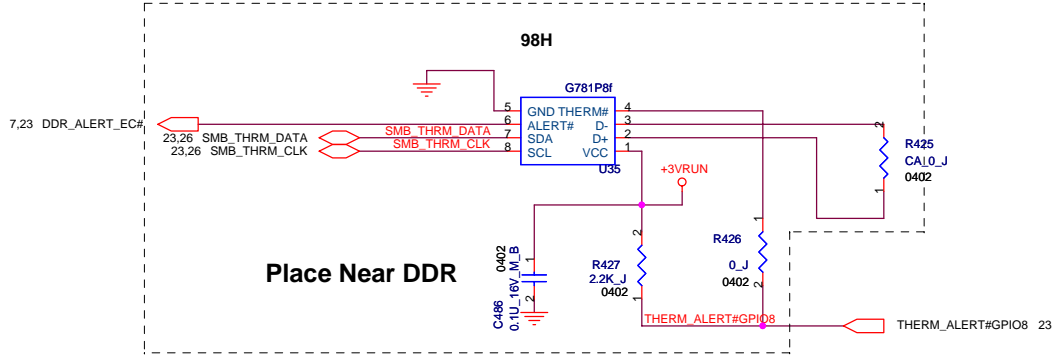
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Size A3 Document Number **MS60-1-05 (MBX-163)** Rev 0.20

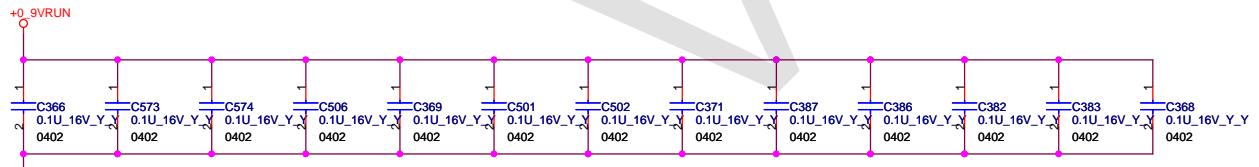
Date: Monday, June 19, 2006 Sheet 13 of 47



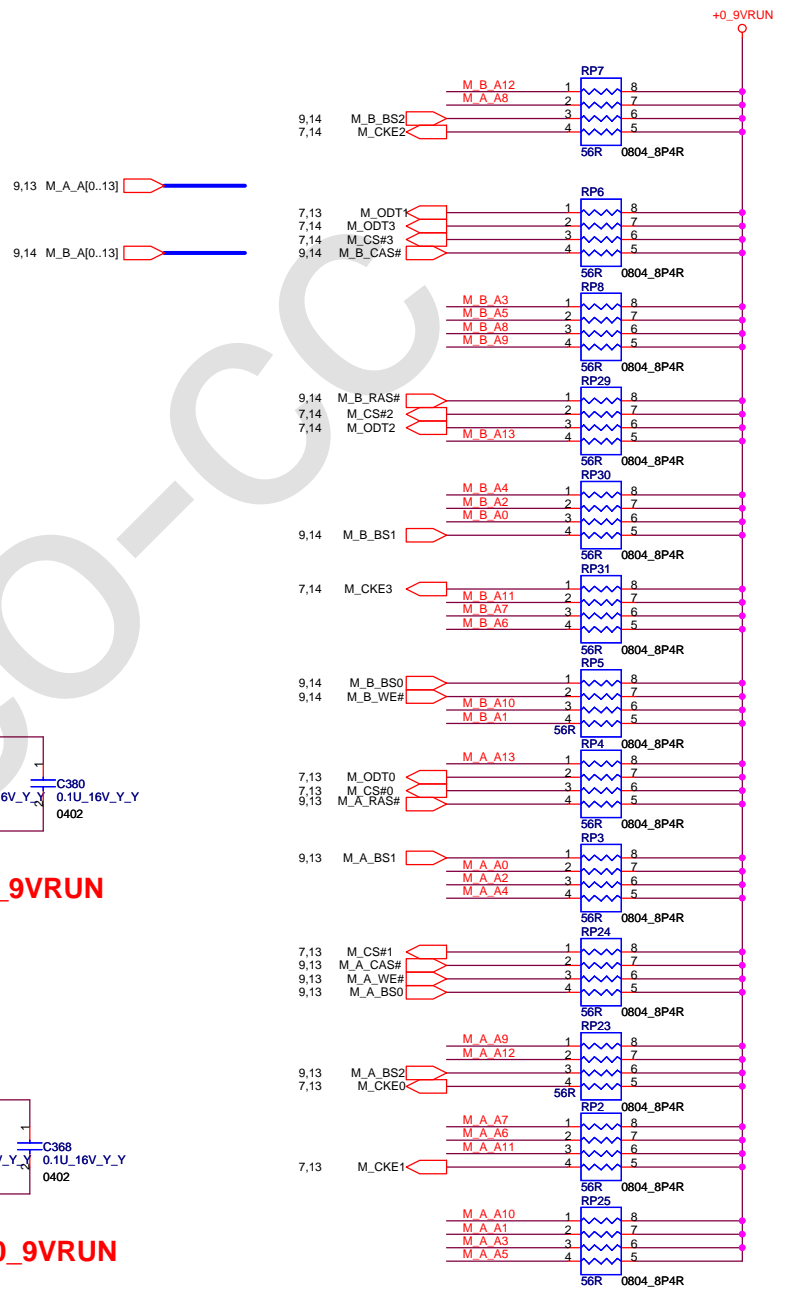
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CPBG - R&D Division		
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Size	Document Number	Rev
Custom	<b>MS60-1-05 (MBX-163)</b>	0.20
Date:	Monday, June 19, 2006	Sheet 14 of 47



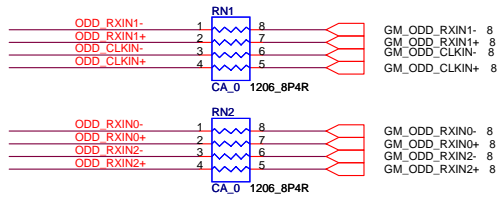
**Layout note: Place 1 cap close to every 1 R-pack terminated to +0\_9VRUN**



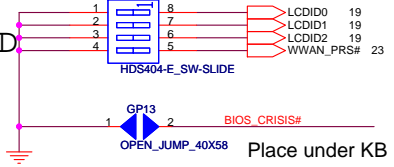
**Layout note: Place 1 cap close to every 1 R-pack terminated to +0\_9VRUN**



### LVDS

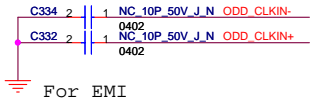


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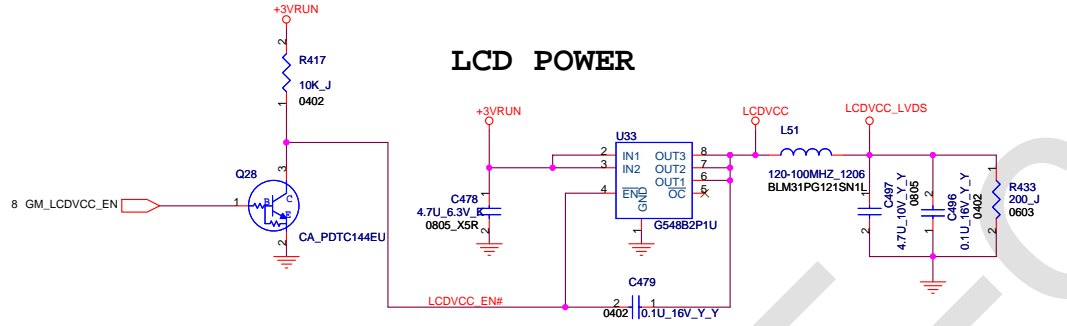


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

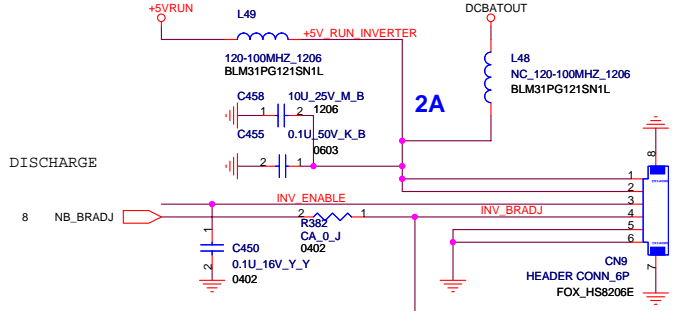
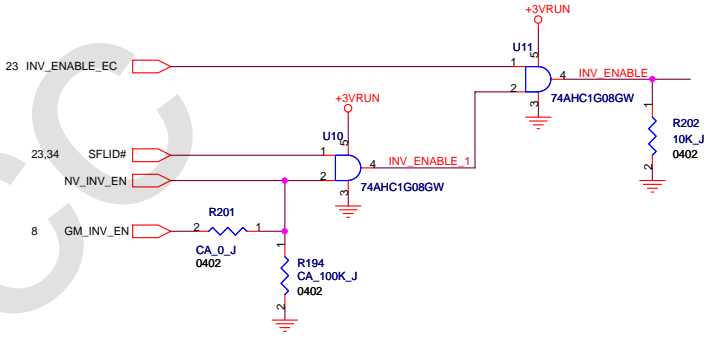
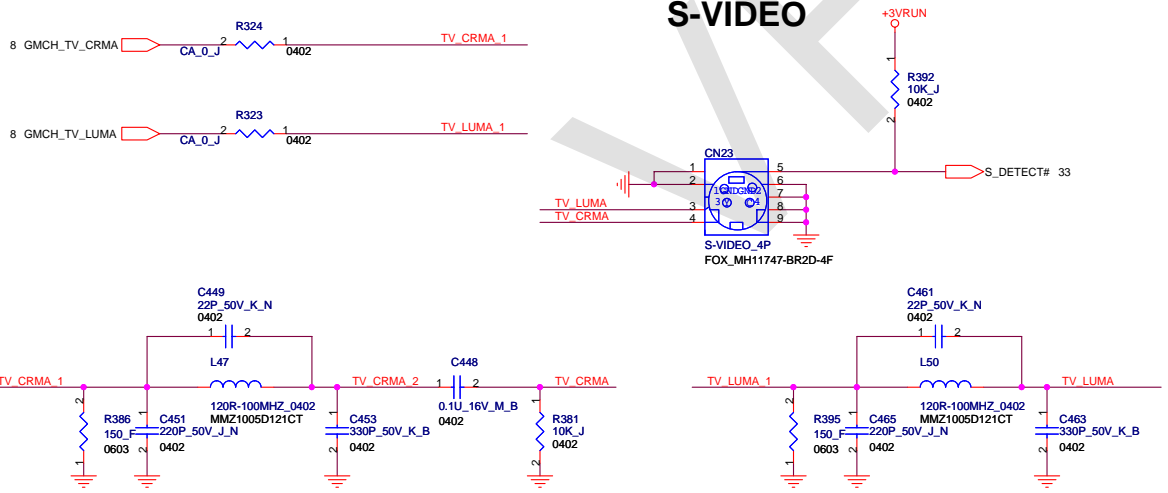
### LVDS CONNECTOR



### LCD POWER



### S-VIDEO



### INVERTER CONNECTOR

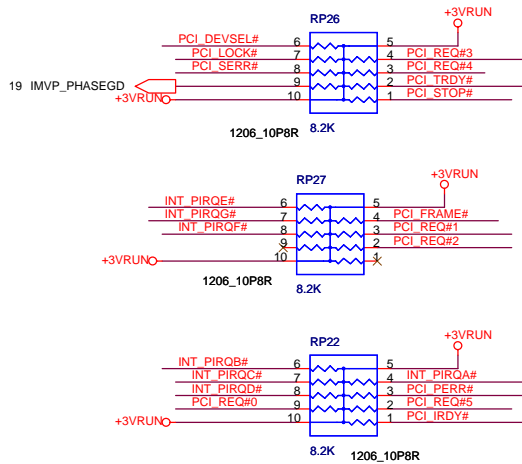
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title: **LVDS / S\_VIDEO**

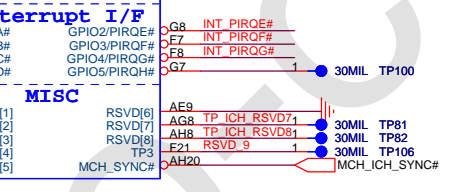
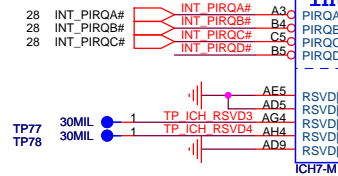
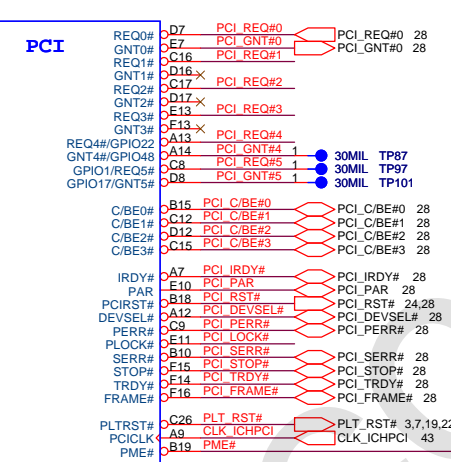
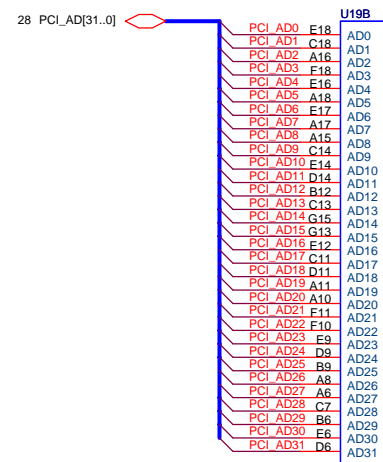
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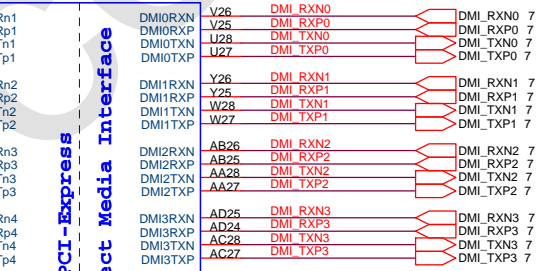
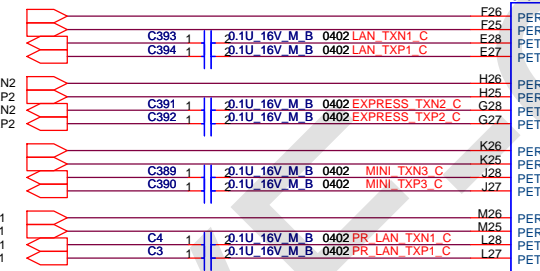


PCI Pullups

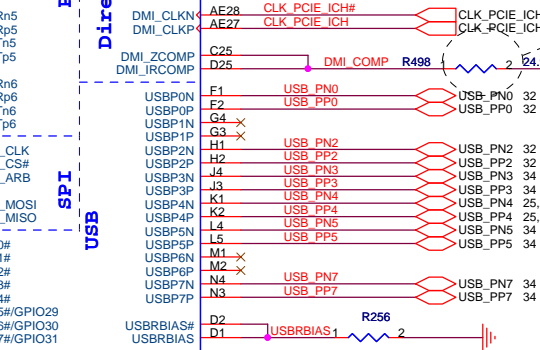
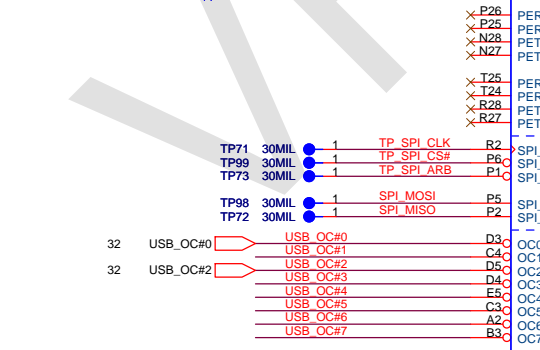
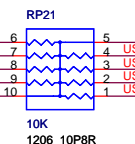


Test leakage voltage in BB

- 34 LAN\_RXN1
- 34 LAN\_RXP1
- 34 LAN\_TXN1
- 34 LAN\_TXP1
- 34 EXPRESS\_RXN2
- 34 EXPRESS\_RXP2
- 34 EXPRESS\_TXN2
- 34 EXPRESS\_TXP2
- 34 MINI\_RXN3
- 34 MINI\_RXP3
- 34 MINI\_TXN3
- 34 MINI\_TXP3
- 34 PR\_LAN\_RXN1
- 34 PR\_LAN\_RXP1
- 34 PR\_LAN\_TXN1
- 34 PR\_LAN\_TXP1

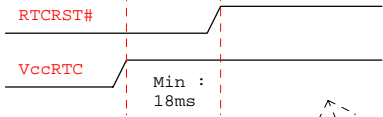


Place within 500 mils of ICH

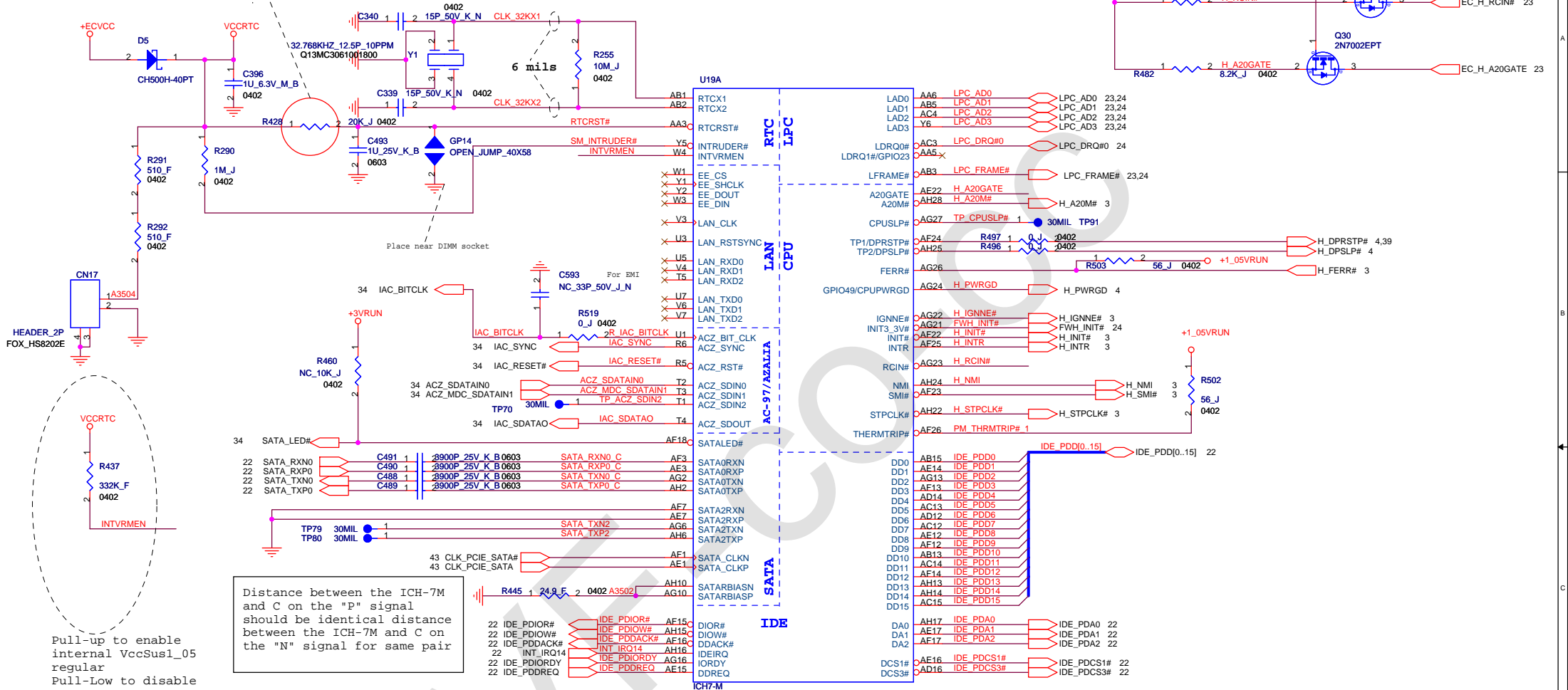


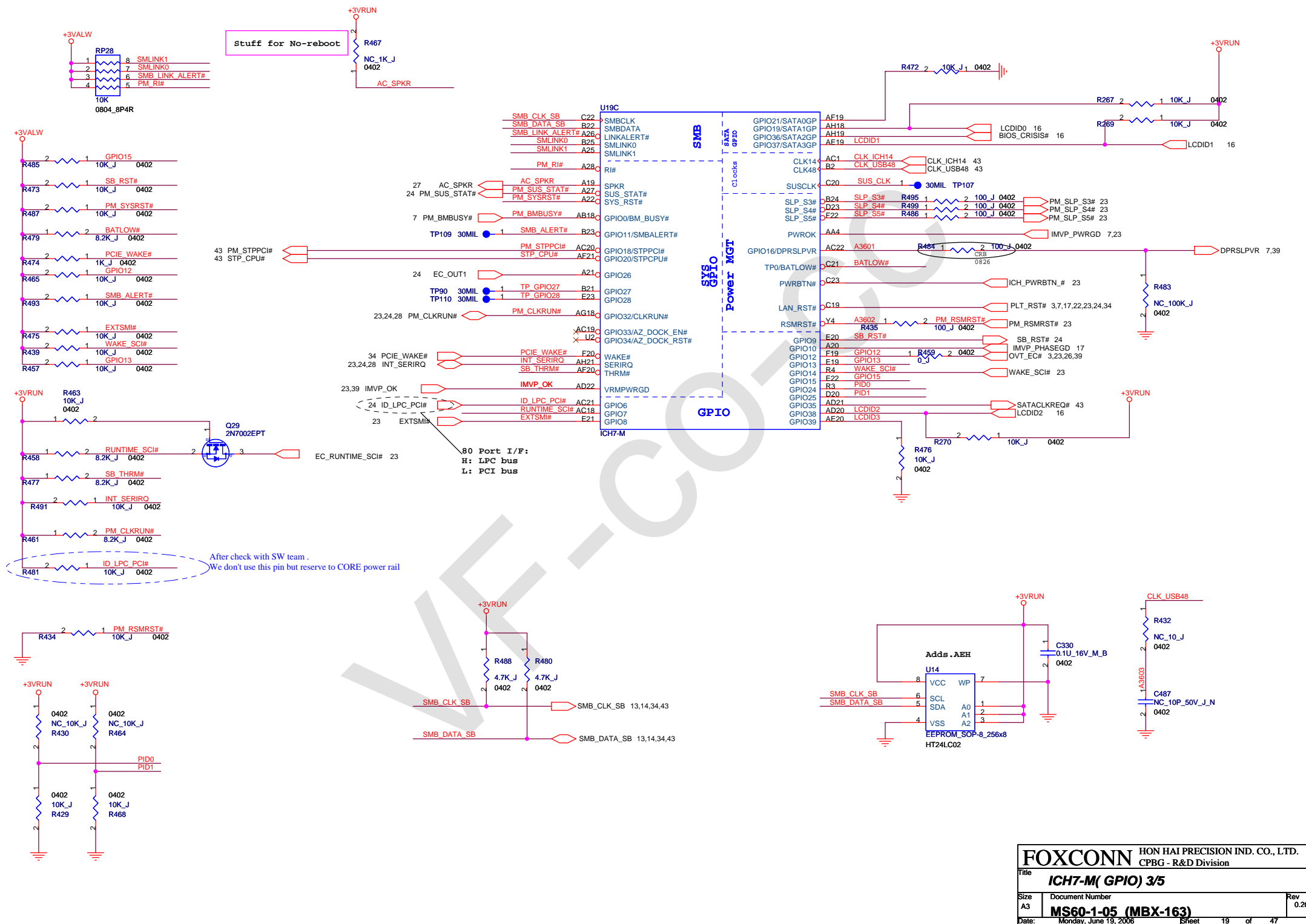
Place within 500 mils of ICH and don't routing next to high speed signals

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 CPBG - R&D Division  
 Title: **ICH7-M( PCI/DMI/USB/PCIE ) 1/5**  
 Size: A3 Document Number: **MS60-1-05 (MBX-163)** Rev: 0.20  
 Date: Monday, June 19, 2006 Sheet 17 of 47



The traces inside this block should be wider.  
No digital signals routed under XTAL







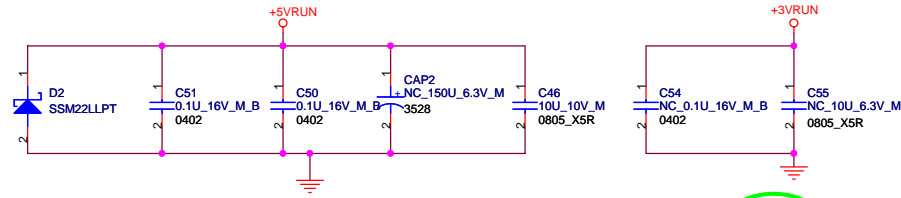
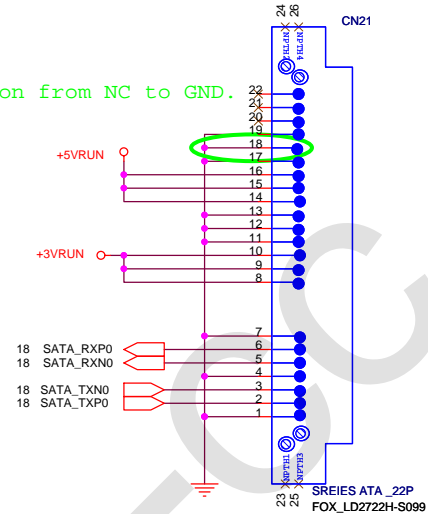
U19E			P28
A4	VSS[1]	VSS[98]	R1
A23	VSS[2]	VSS[99]	R11
B1	VSS[3]	VSS[100]	R12
B8	VSS[4]	VSS[101]	R13
B11	VSS[5]	VSS[102]	R14
B14	VSS[6]	VSS[103]	R15
B17	VSS[7]	VSS[104]	R16
B20	VSS[8]	VSS[105]	R17
B26	VSS[9]	VSS[106]	R18
B28	VSS[10]	VSS[107]	T6
C2	VSS[11]	VSS[108]	T12
C6	VSS[12]	VSS[109]	T13
C27	VSS[13]	VSS[110]	T14
D10	VSS[14]	VSS[111]	T15
D13	VSS[15]	VSS[112]	T16
D18	VSS[16]	VSS[113]	T17
D21	VSS[17]	VSS[114]	U4
D24	VSS[18]	VSS[115]	U12
E1	VSS[19]	VSS[116]	U13
E2	VSS[20]	VSS[117]	U14
F4	VSS[21]	VSS[118]	U15
F8	VSS[22]	VSS[119]	U16
F15	VSS[23]	VSS[120]	U17
F3	VSS[24]	VSS[121]	U24
F4	VSS[25]	VSS[122]	U25
F5	VSS[26]	VSS[123]	U26
F12	VSS[27]	VSS[124]	V2
F27	VSS[28]	VSS[125]	V13
F28	VSS[29]	VSS[126]	V15
G1	VSS[30]	VSS[127]	V24
G2	VSS[31]	VSS[128]	V27
G5	VSS[32]	VSS[129]	V28
G6	VSS[33]	VSS[130]	W6
G9	VSS[34]	VSS[131]	W24
G14	VSS[35]	VSS[132]	W25
G18	VSS[36]	VSS[133]	W26
G21	VSS[37]	VSS[134]	Y3
G24	VSS[38]	VSS[135]	Y24
G25	VSS[39]	VSS[136]	Y27
G26	VSS[40]	VSS[137]	Y28
H3	VSS[41]	VSS[138]	AA1
H4	VSS[42]	VSS[139]	AA24
H5	VSS[43]	VSS[140]	AA25
H24	VSS[44]	VSS[141]	AA26
H27	VSS[45]	VSS[142]	AB4
H28	VSS[46]	VSS[143]	AB6
J1	VSS[47]	VSS[144]	AB11
J2	VSS[48]	VSS[145]	AB14
J5	VSS[49]	VSS[146]	AB16
J24	VSS[50]	VSS[147]	AB19
J25	VSS[51]	VSS[148]	AB21
J26	VSS[52]	VSS[149]	AB24
K24	VSS[53]	VSS[150]	AB27
K27	VSS[54]	VSS[151]	AB28
K28	VSS[55]	VSS[152]	AC2
L13	VSS[56]	VSS[153]	AC5
L15	VSS[57]	VSS[154]	AC9
L24	VSS[58]	VSS[155]	AC11
L25	VSS[59]	VSS[156]	AD1
L26	VSS[60]	VSS[157]	AD3
M3	VSS[61]	VSS[158]	AD4
M4	VSS[62]	VSS[159]	AD7
M5	VSS[63]	VSS[160]	AD8
M12	VSS[64]	VSS[161]	AD11
M13	VSS[65]	VSS[162]	AD15
M14	VSS[66]	VSS[163]	AD19
M15	VSS[67]	VSS[164]	AD23
M16	VSS[68]	VSS[165]	AE2
M17	VSS[69]	VSS[166]	AE4
M24	VSS[70]	VSS[167]	AE8
M27	VSS[71]	VSS[168]	AE11
M28	VSS[72]	VSS[169]	AE13
N1	VSS[73]	VSS[170]	AE18
N2	VSS[74]	VSS[171]	AE21
N5	VSS[75]	VSS[172]	AE24
N6	VSS[76]	VSS[173]	AE25
N11	VSS[77]	VSS[174]	AF2
N12	VSS[78]	VSS[175]	AF4
N13	VSS[79]	VSS[176]	AF8
N14	VSS[80]	VSS[177]	AF11
N15	VSS[81]	VSS[178]	AF27
N16	VSS[82]	VSS[179]	AF28
N17	VSS[83]	VSS[180]	AG1
N18	VSS[84]	VSS[181]	AG3
N24	VSS[85]	VSS[182]	AG7
N25	VSS[86]	VSS[183]	AG11
N26	VSS[87]	VSS[184]	AG14
P3	VSS[88]	VSS[185]	AG17
P4	VSS[89]	VSS[186]	AG20
P12	VSS[90]	VSS[187]	AG25
P13	VSS[91]	VSS[188]	AH1
P14	VSS[92]	VSS[189]	AH3
P15	VSS[93]	VSS[190]	AH7
P16	VSS[94]	VSS[191]	AH12
P17	VSS[95]	VSS[192]	AH23
P24	VSS[96]	VSS[193]	AH27
P27	VSS[97]	VSS[194]	

ICH7-M

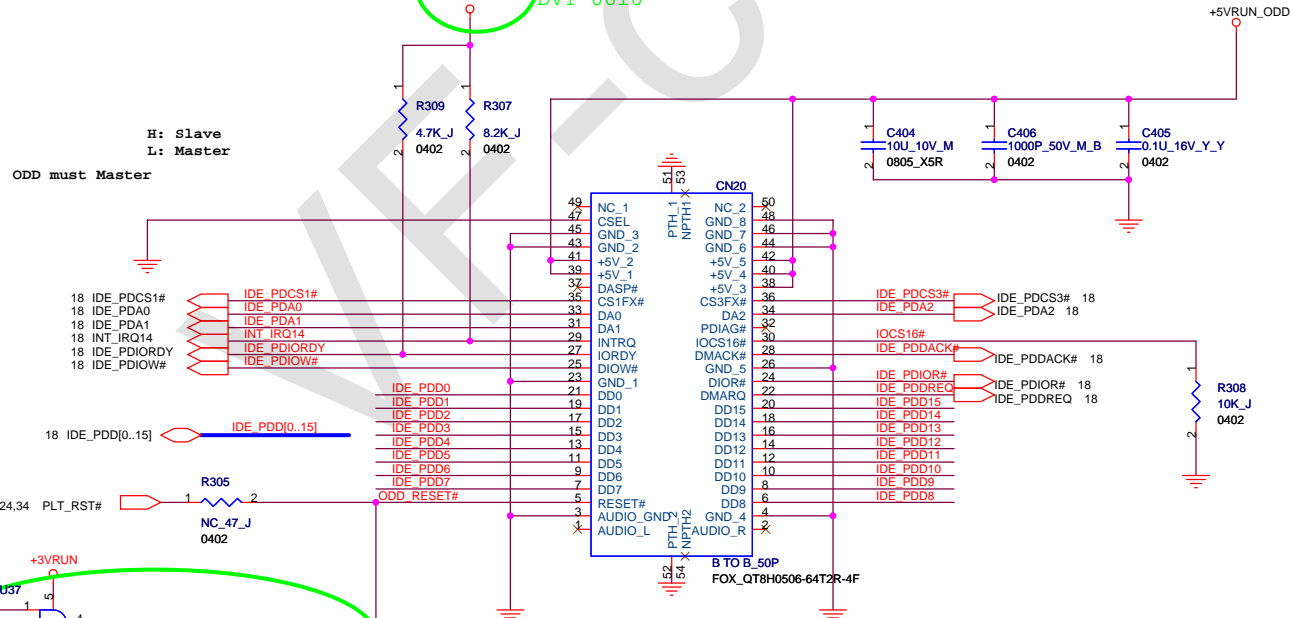
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		CPBG - R&D Division	
Title			
<b>ICH7-M( GND) 5/5</b>			
Size	Document Number		Rev
A3	<b>MS60-1-05 (MBX-163)</b>		0.20
Date:	Monday, June 19, 2006	Sheet	21 of 47

# SATA HDD CONN

CN21's pin18 change connection from NC to GND.  
DVT 0616



+3VRUN\_ODD Change from +3VRUN to +3VRUN\_ODD  
DVT 0616



# CD-ROM CONN

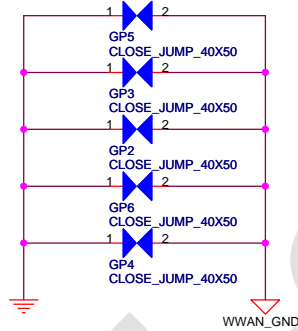
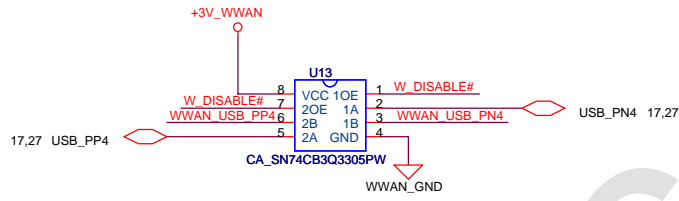
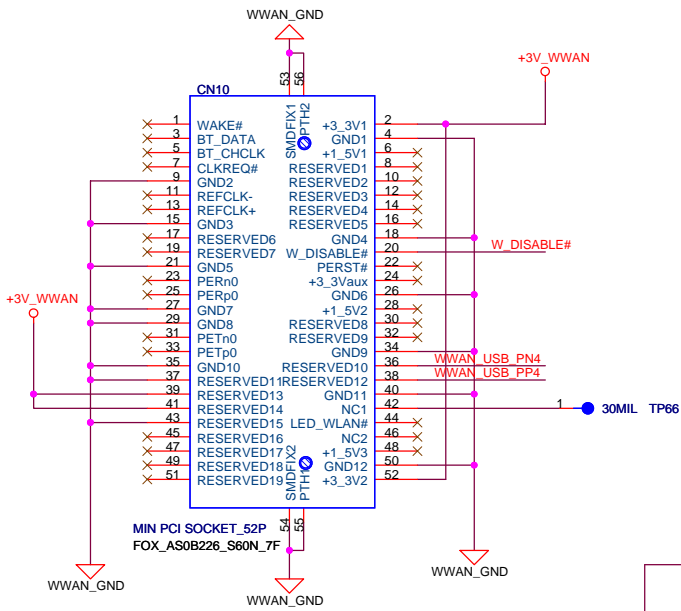
Del R516, R517, C580  
DVT 0615

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title <b>SATA HDD/CD-ROM</b>		
Size A3	Document Number <b>MS60-1-05 (MBX-163)</b>	Rev 0.20
Date: Monday, June 19, 2006	Sheet 22	of 47



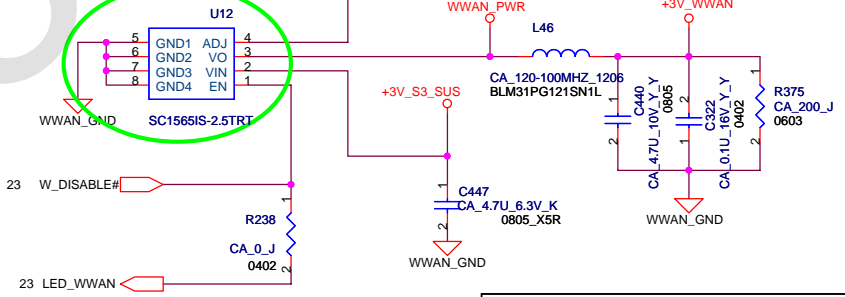






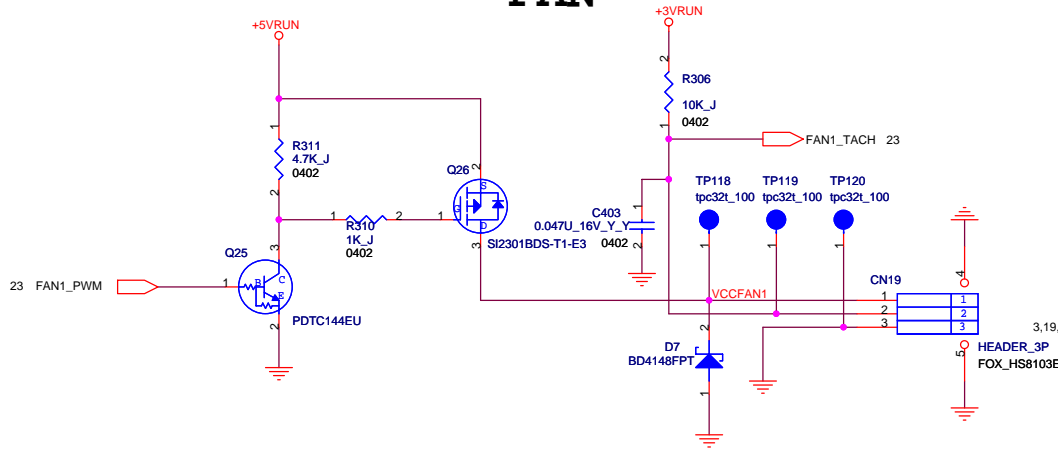
# WWAN POWER

U12 change to SC1565IS-2.5TRT  
DVT 0617

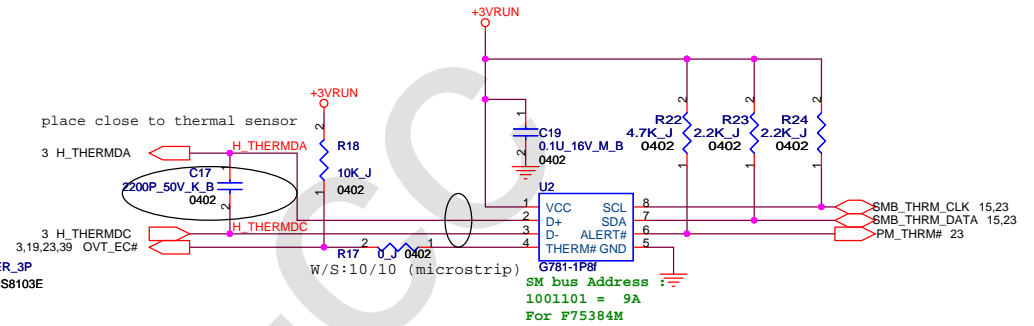


<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title: <b>WWAN</b>			
Size: Custom	Document Number: <b>MS60-1-05 (MBX-163)</b>		Rev: 0.20
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## FAN

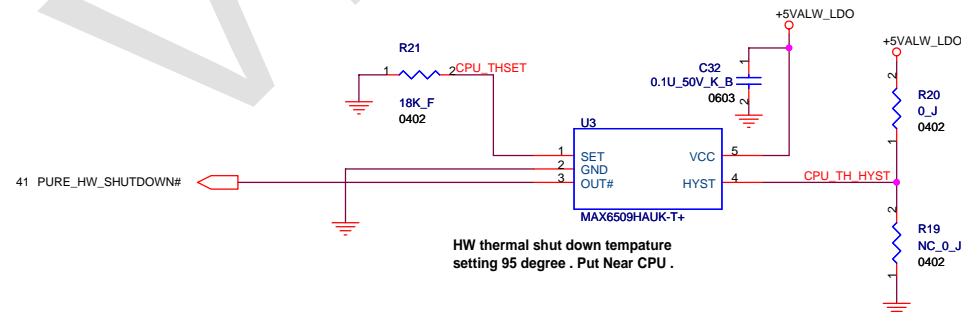


## CPU SENSOR

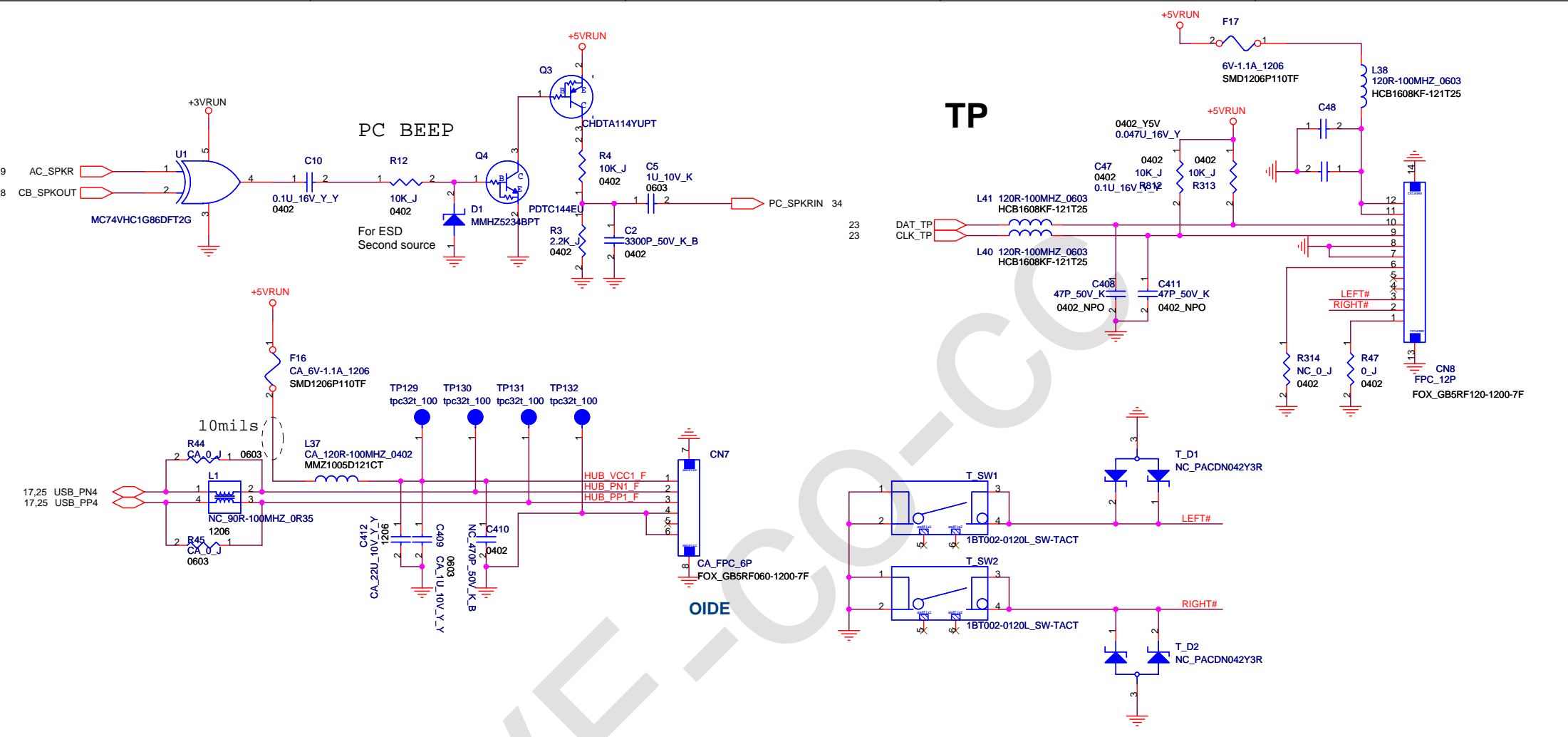


Place Thermal-Sensor near CPU & GMCH.

## HW THERMAL PROTECTION

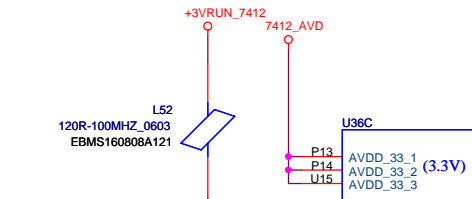


HW thermal shut down temperature setting 95 degree . Put Near CPU .



<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title <b>OIDE/TP</b>		
Size Custom	Document Number <b>MS60-1-05 (MBX-163)</b>	Rev 0.20
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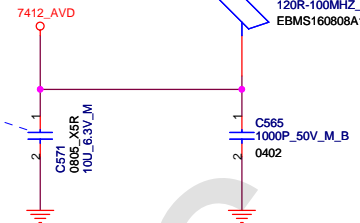


Close to IC

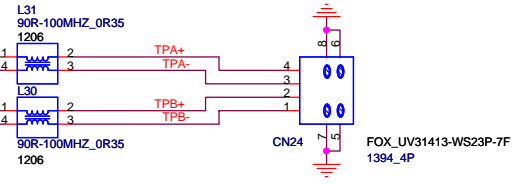
This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

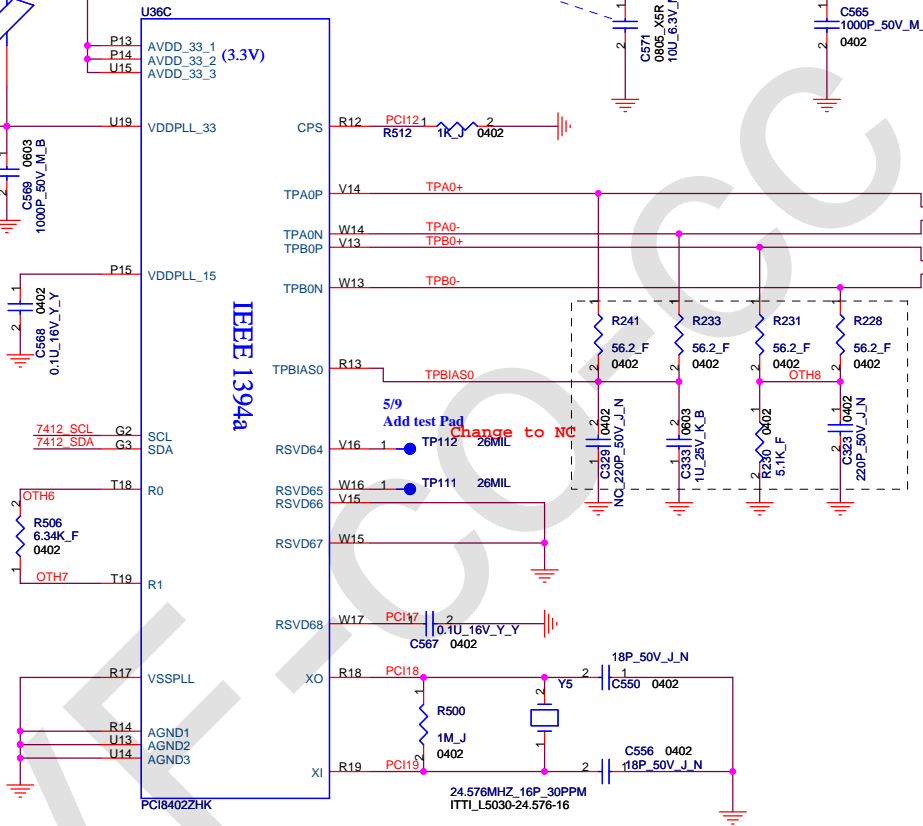
This array must be placed close to AVDD (Pin P13,P14,U15) They must be tied to a low-impedance GND.



iLink CONN.

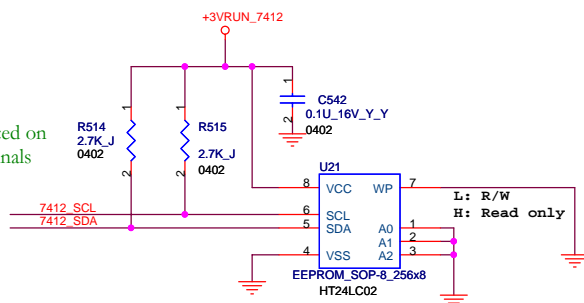


Place near PCI8402

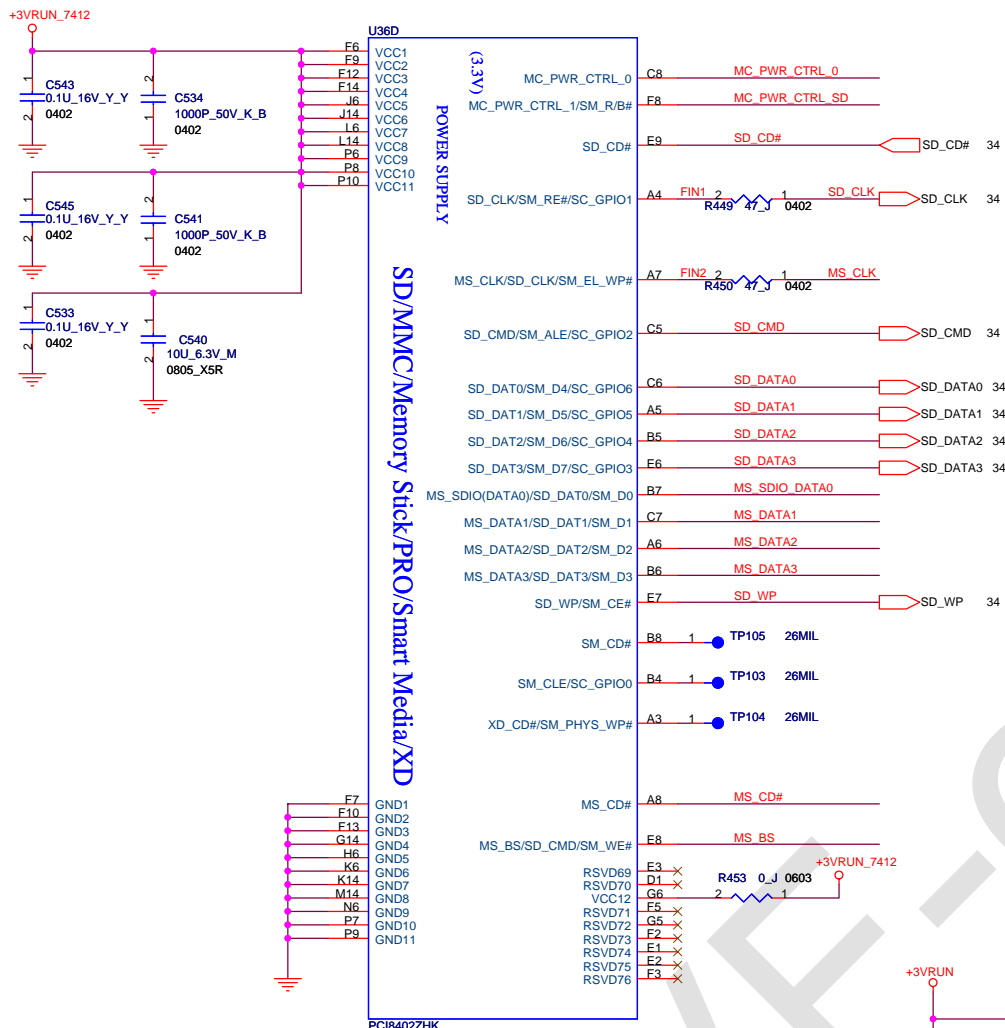


5/9 Add test Pad Change to NC

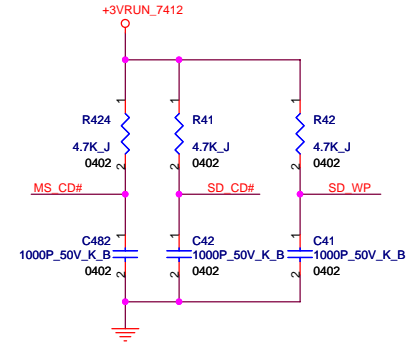
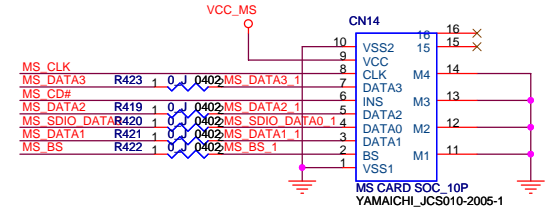
Resistors should be placed on the SCL and SDA terminals



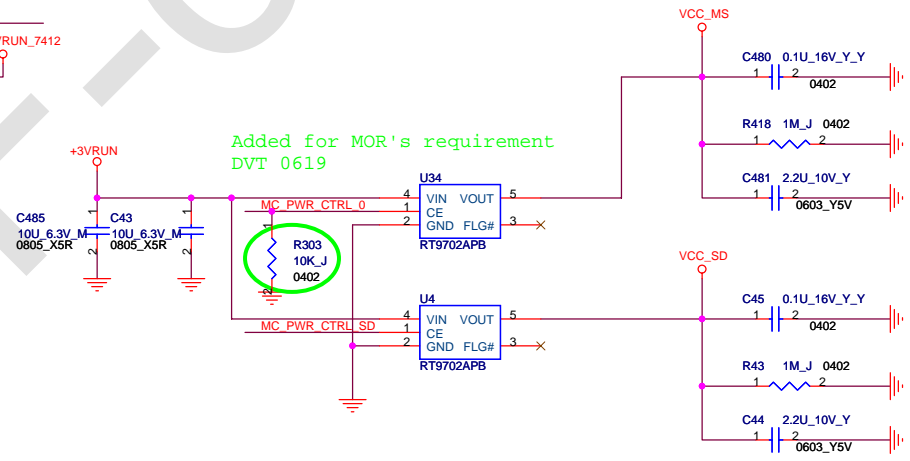
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	<b>PCI ( I LINK )</b>	
Size	Document Number	Rev
A3	<b>MS60-1-05 (MBX-163)</b>	0.20
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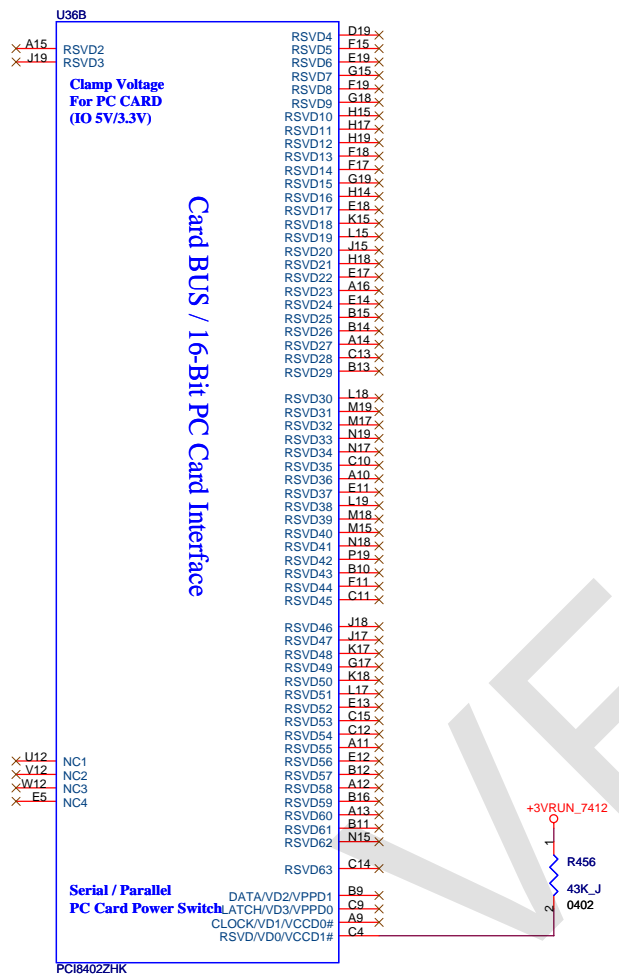


# MS Duo / Pro



Added for MOR's requirement  
DVT 0619



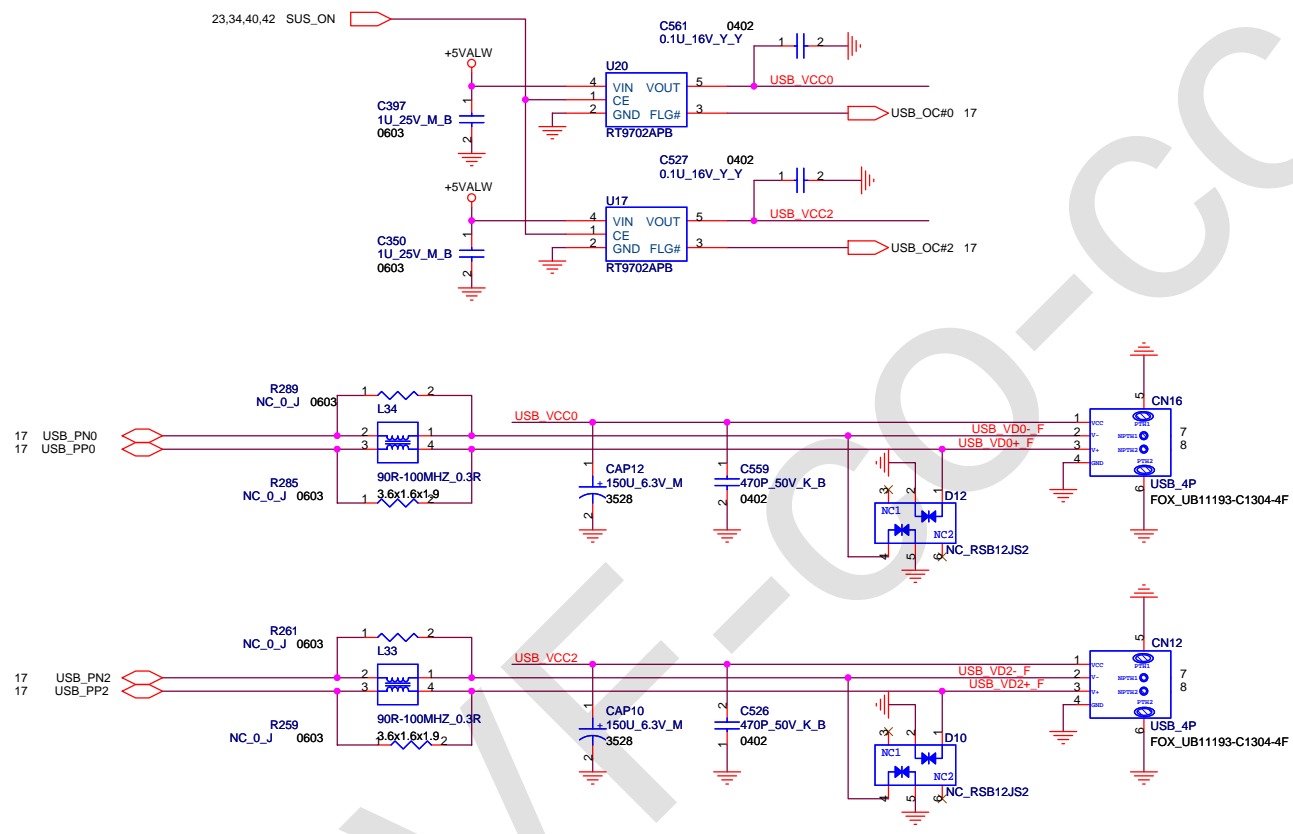


X A15  
X J19

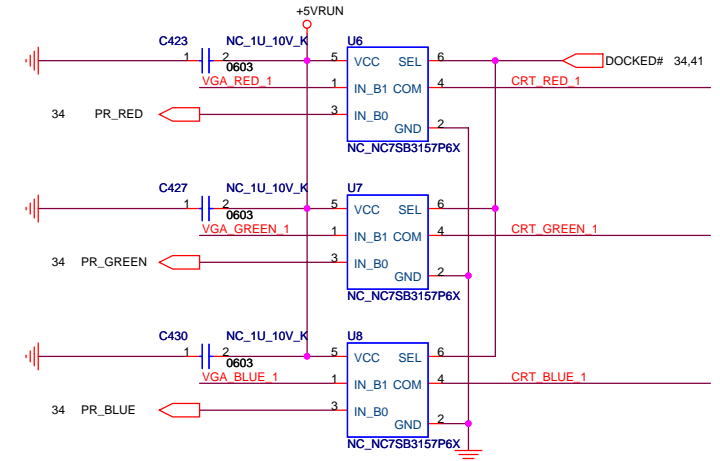
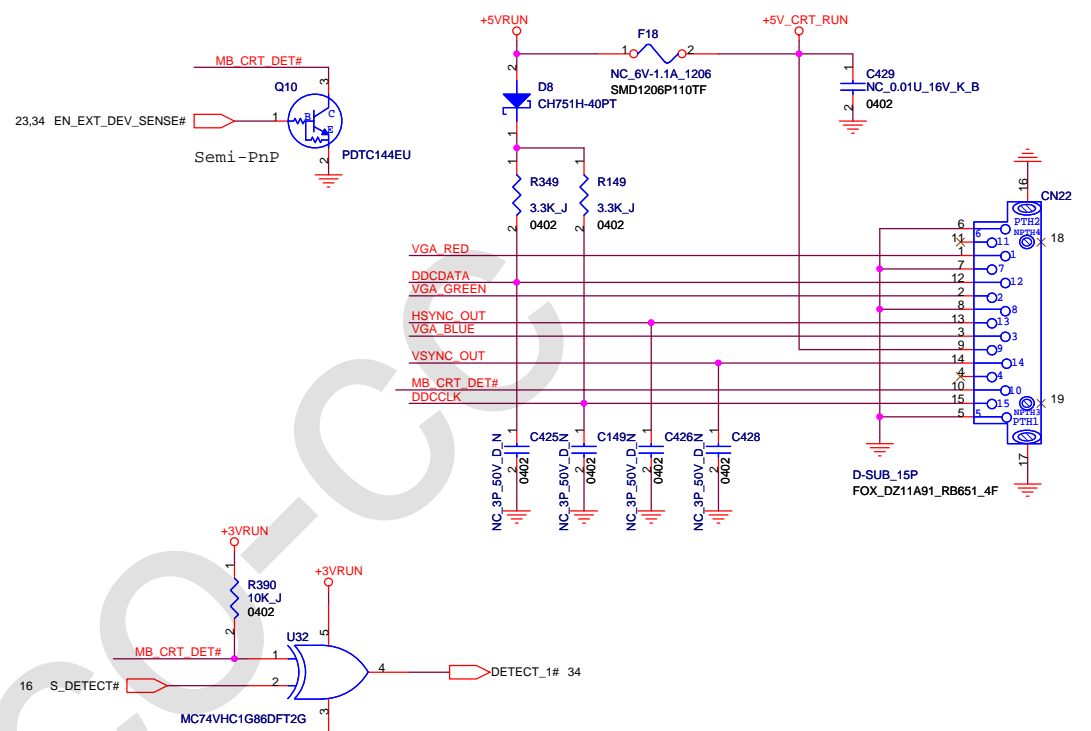
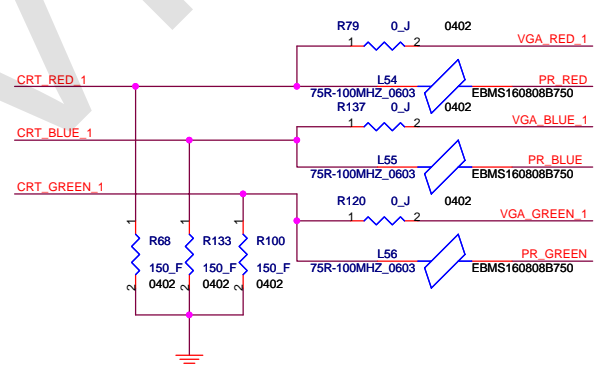
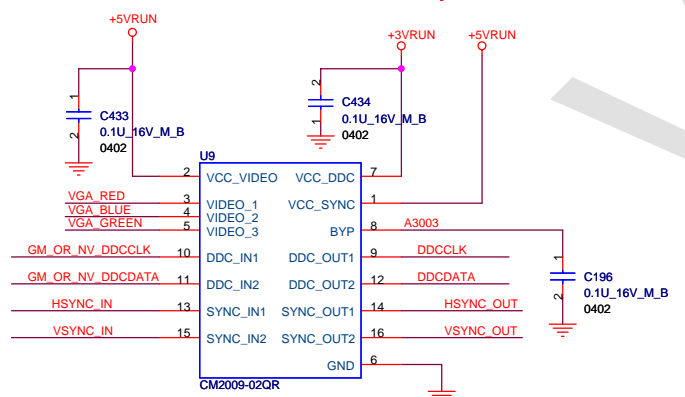
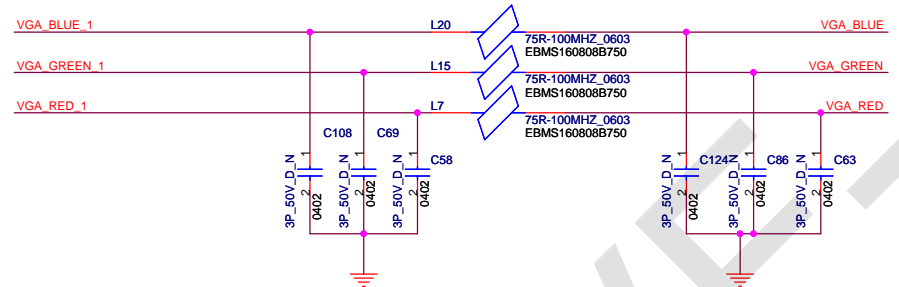
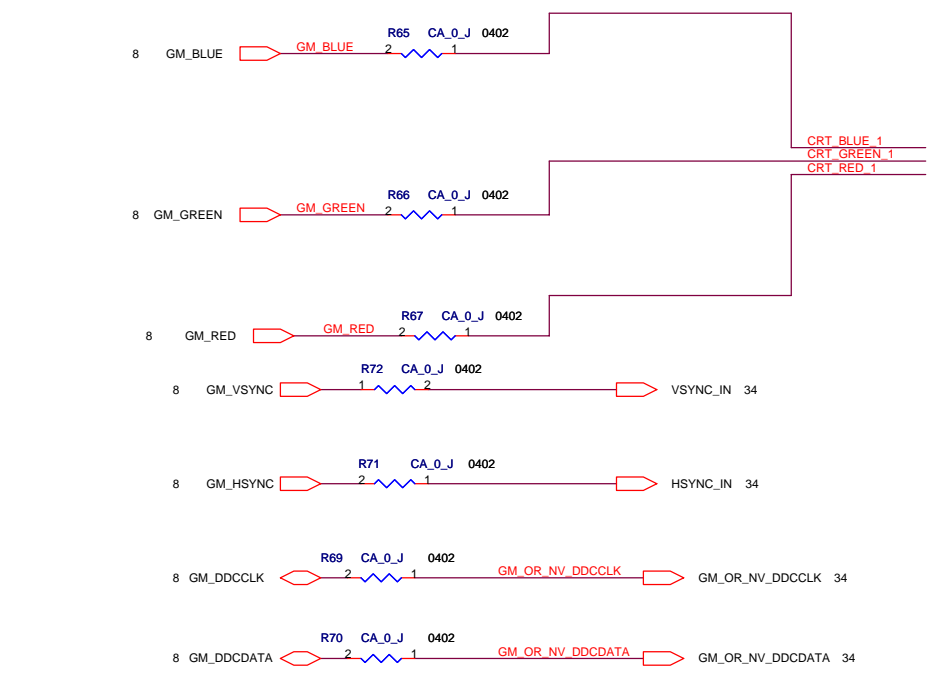
X U12  
X V12  
X W12  
X E5

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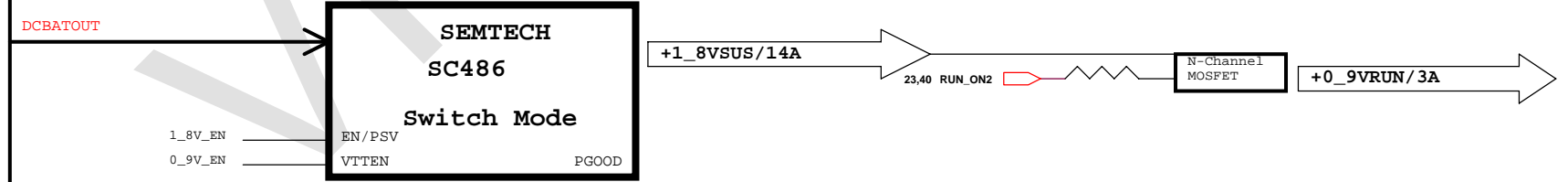
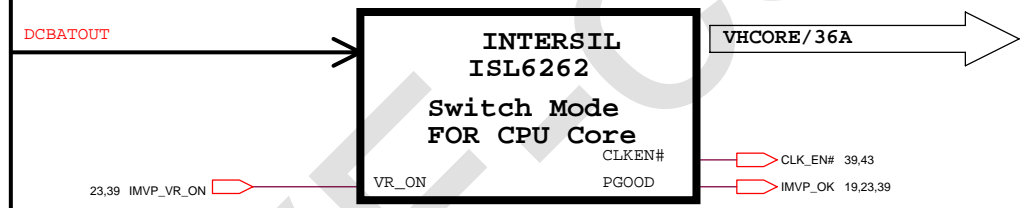
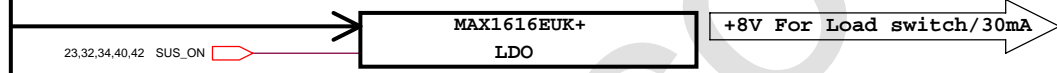
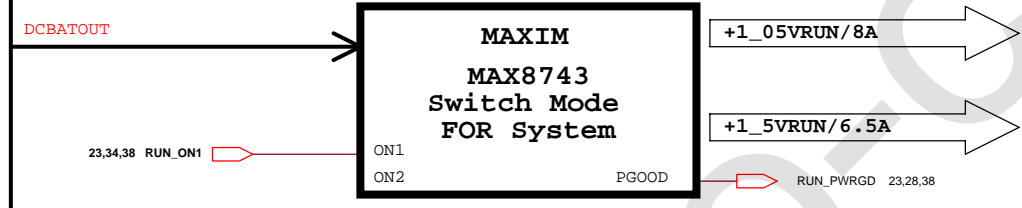
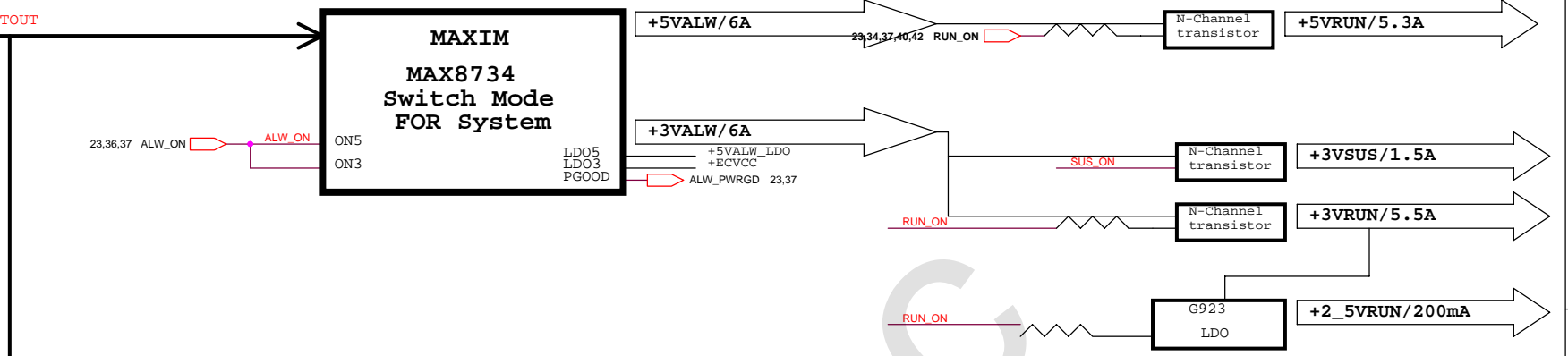
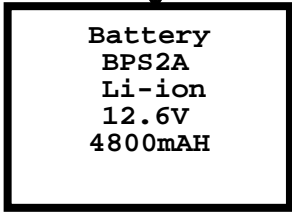
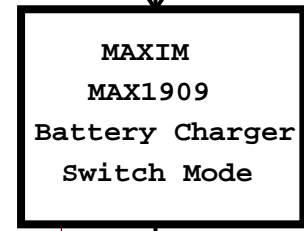
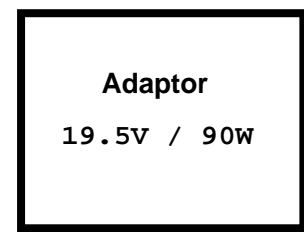
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- C4

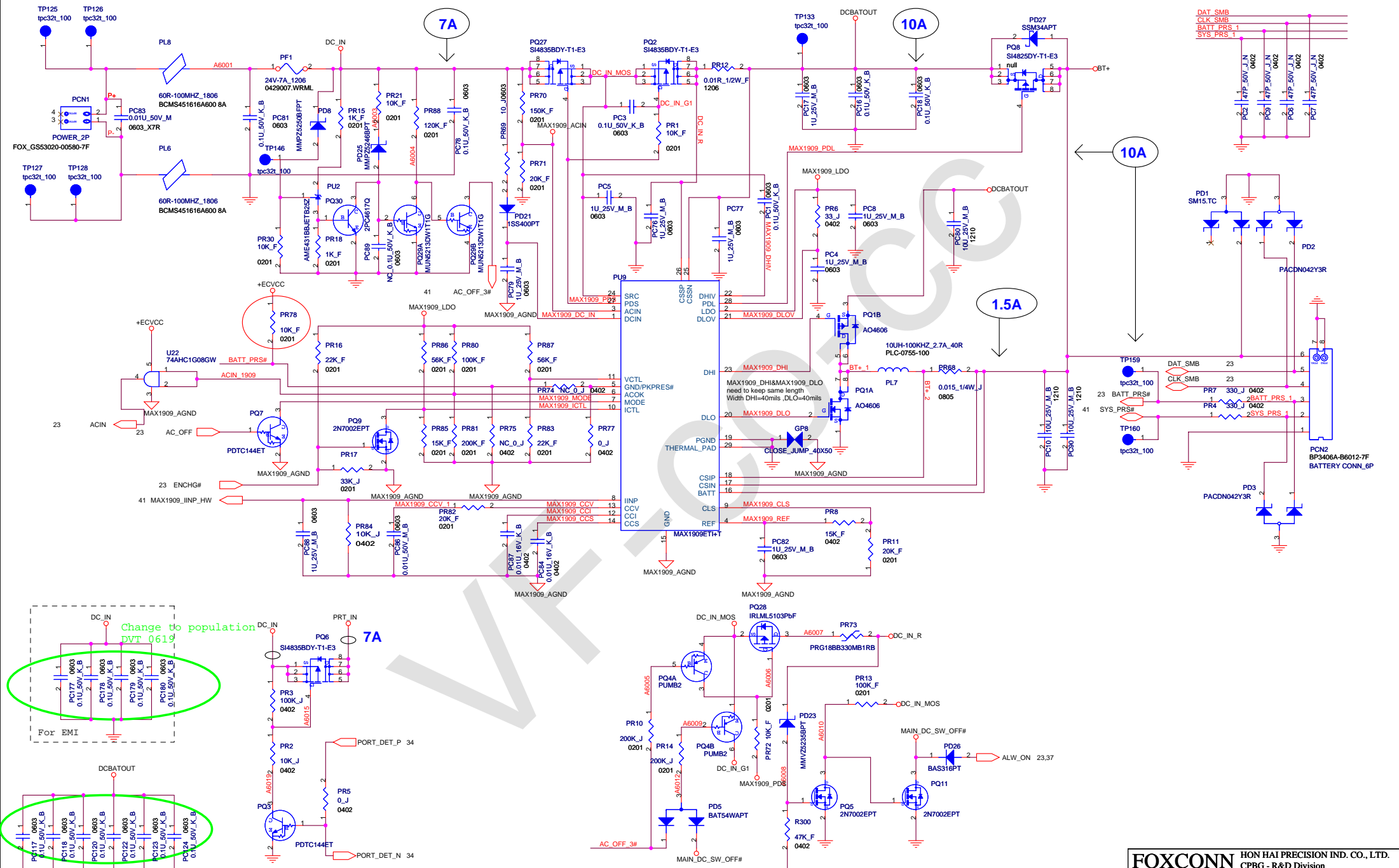












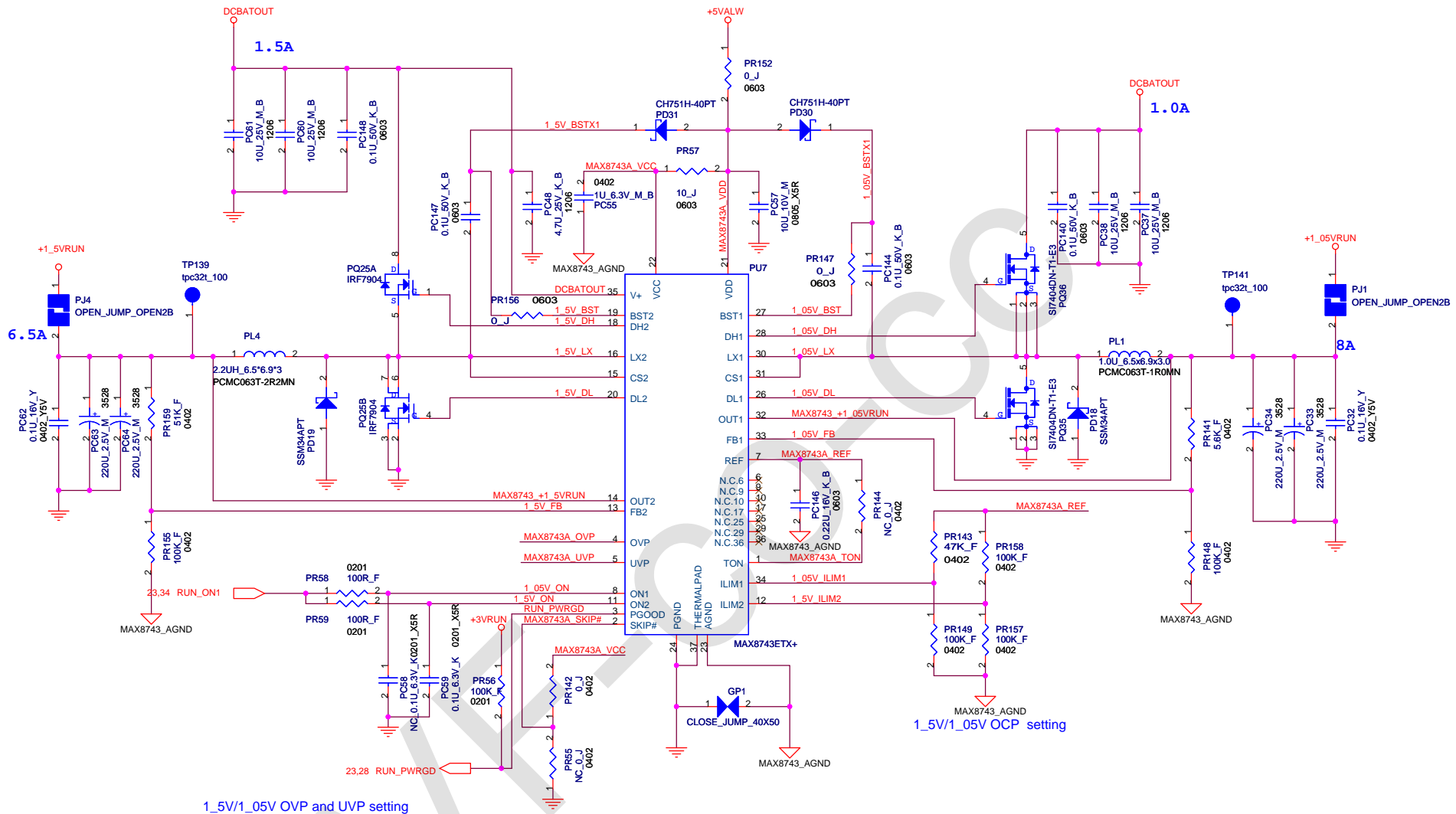
Change to population  
DWT 0619

For EMI

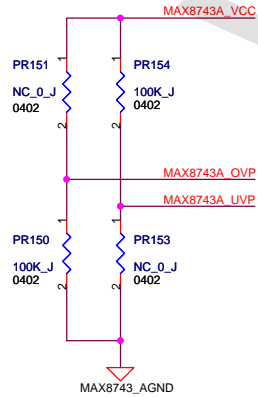
Added for EMI  
DWT 0619

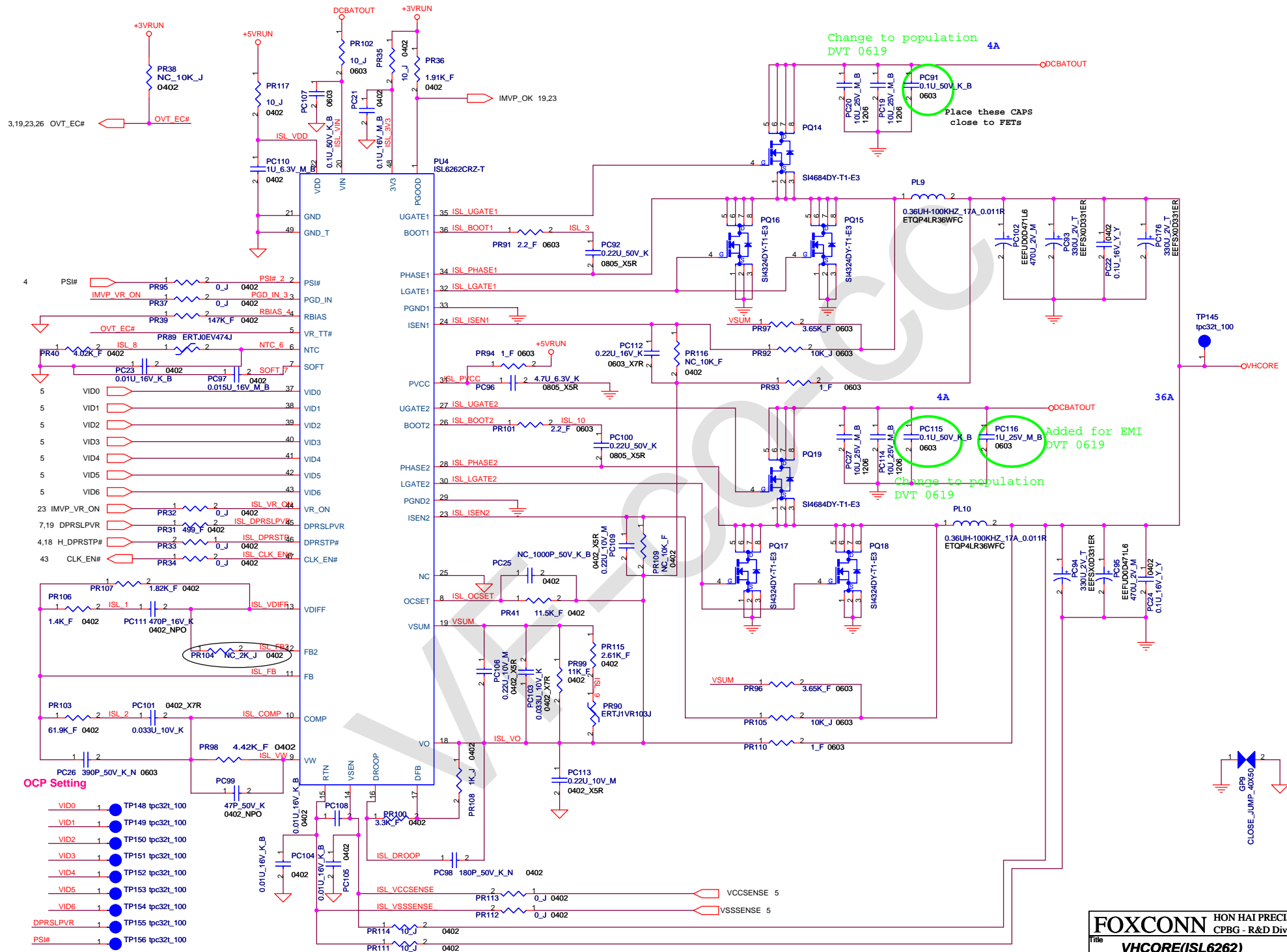
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			CPBG - R&D Division		
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Size	Document Number				Rev
Custom	<b>MS60-1-05 (MBX-163)</b>				020
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1.5V/1.05V OVP and UVP setting



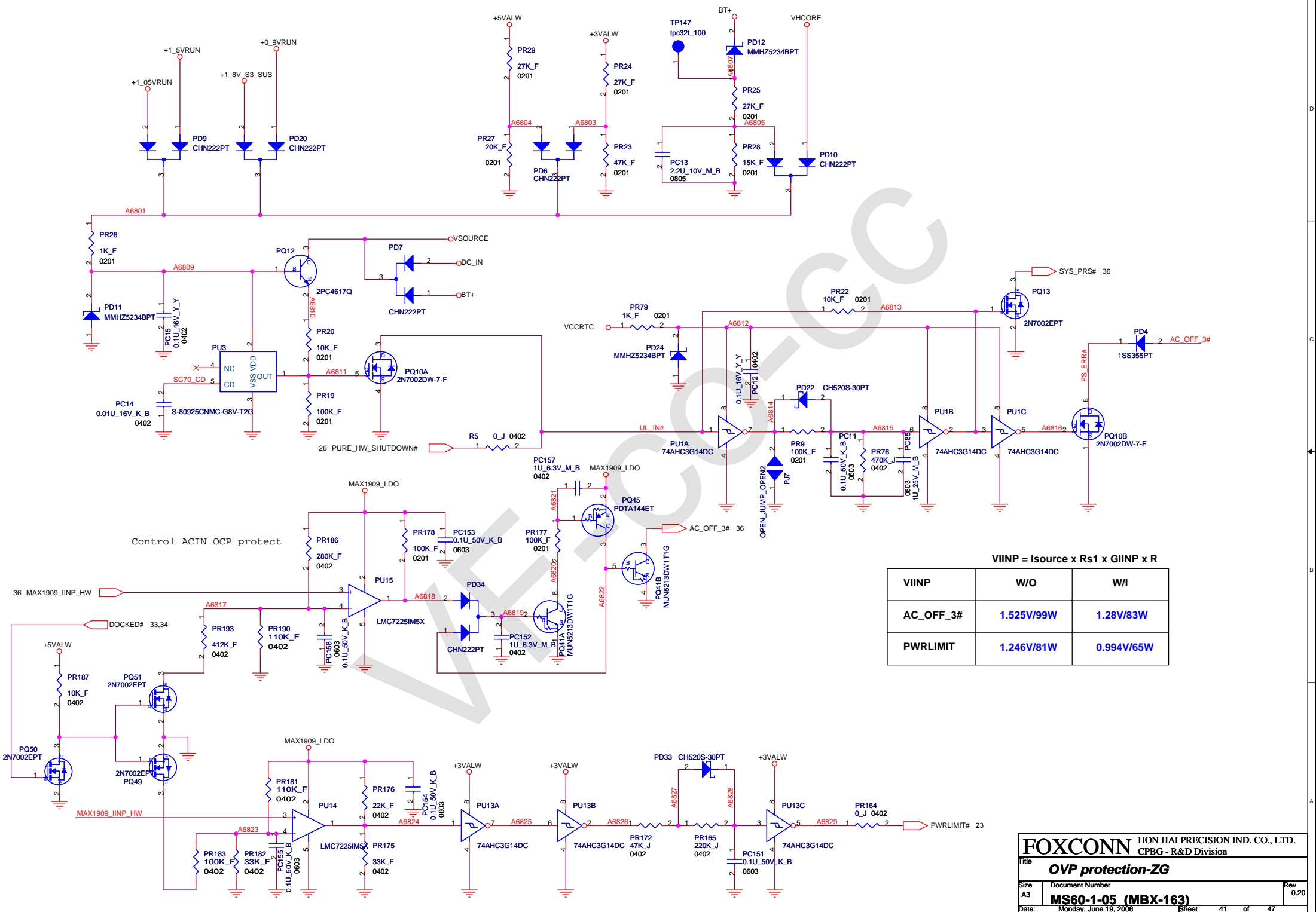


**OCP Setting**

VID0	TP148	tpc32t_100
VID1	TP149	tpc32t_100
VID2	TP150	tpc32t_100
VID3	TP151	tpc32t_100
VID4	TP152	tpc32t_100
VID5	TP153	tpc32t_100
VID6	TP154	tpc32t_100
DPRSPLVR	TP155	tpc32t_100
PSI#	TP156	tpc32t_100
IMVP_VR_ON	TP157	tpc32t_100
H_DPRSTP#	TP158	tpc32t_100







Control ACIN OCP protect

$$VIINP = I_{source} \times R_{s1} \times GIINP \times R$$

VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.246V/81W	0.994V/65W

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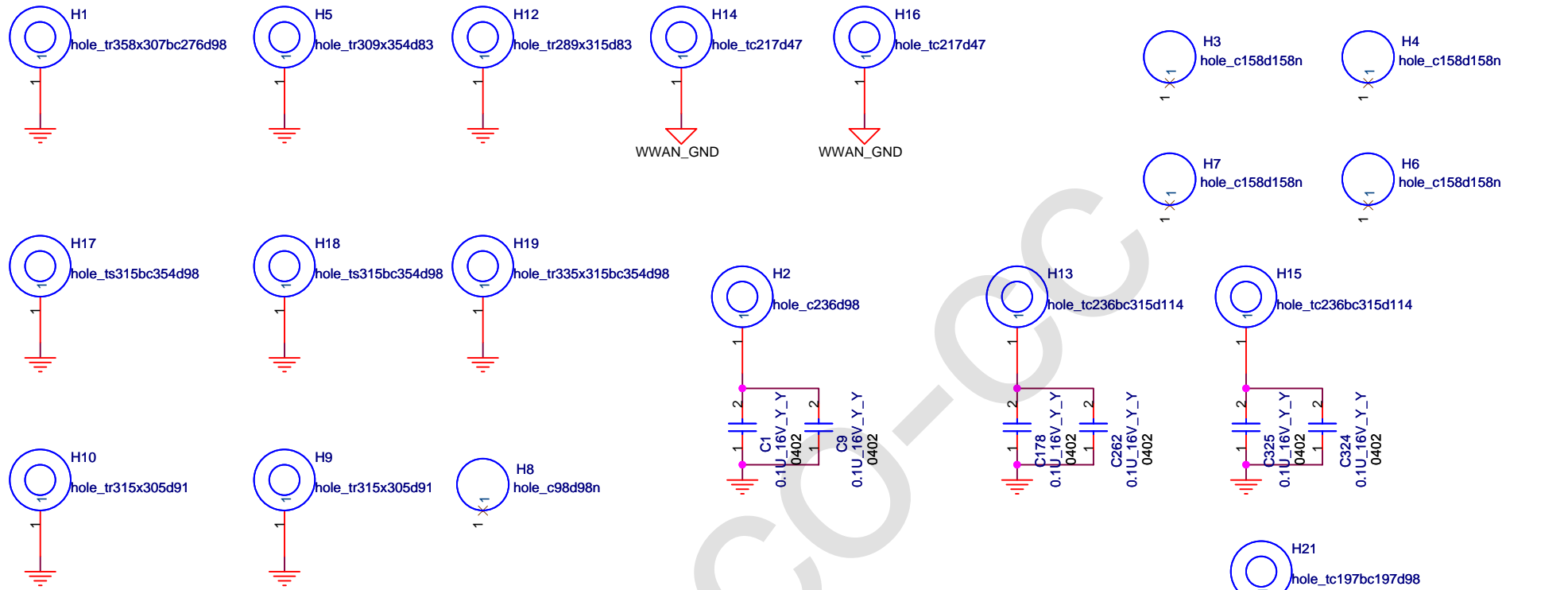
Title: **OVP protection-ZG**

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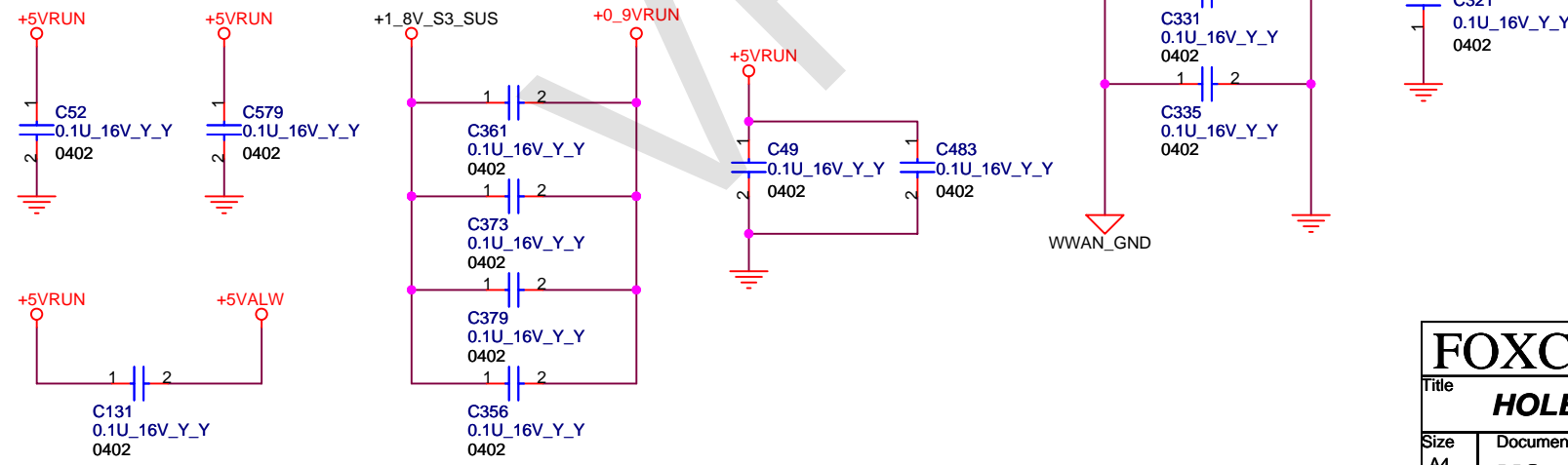
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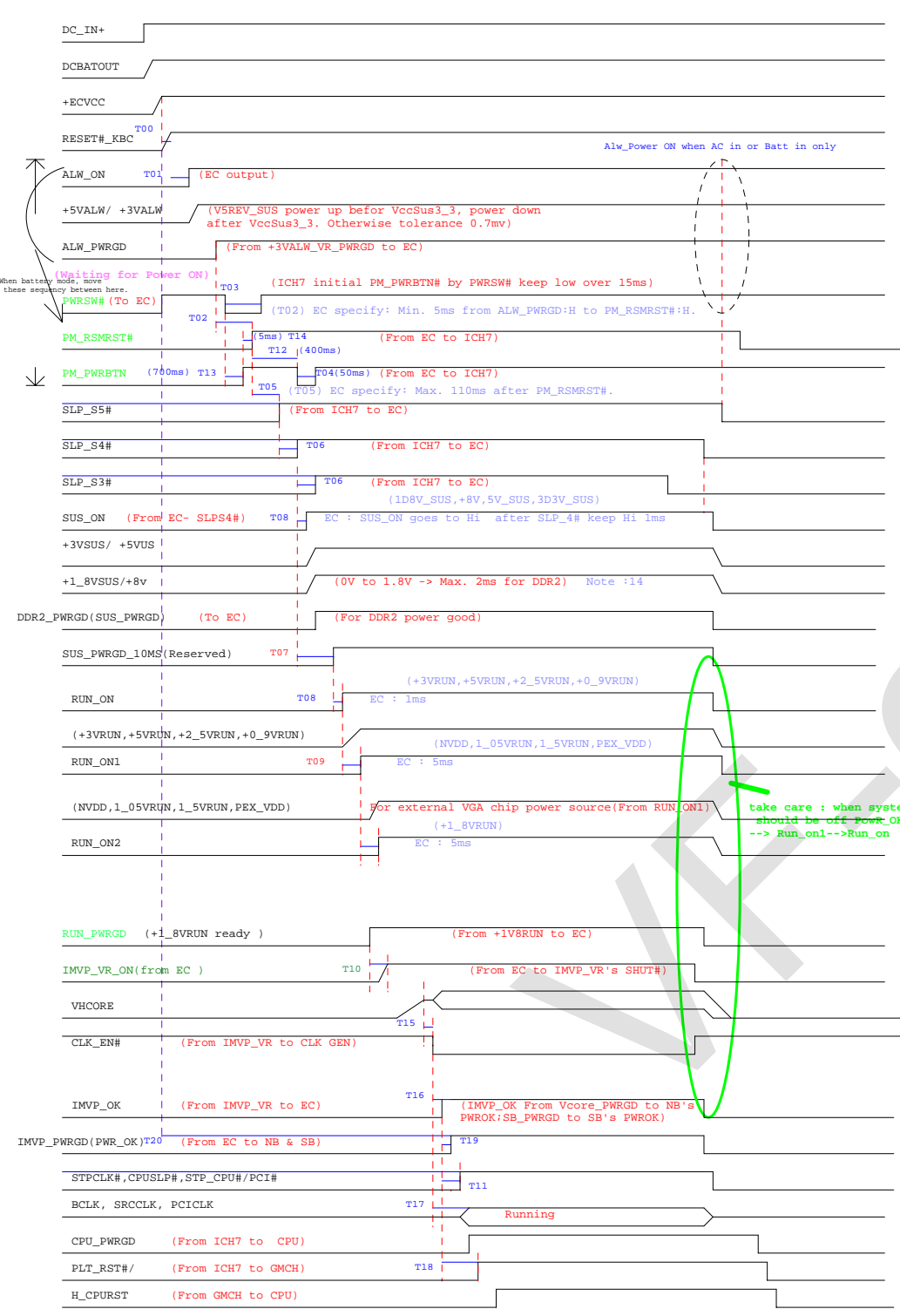
**FOR EMI**



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Title <b>HOLE</b>		
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# MS60 Power On Sequence Timing

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Modified date : 2/14/2006

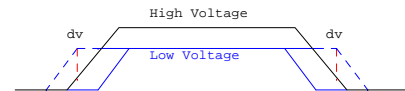


**NOTE :** ( EC KB3910 Min. response time is 1ms)

- T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
- T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)  
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, We measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
- T02 : ALM\_PWRGD#H to PM\_RSMRST#H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
- T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP\_S5# active High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing)
- T06(Please reference Intel 16971 Page 301 of t234 timing)
- T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms )
- T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
- T09 : For MS01 current SPEC
- T10 :Please refer to Intel 16971 Page 300 of t214 timing
- T11 :Please refer to Intel 16971 Page 303 of t216 timing
- T12 : PM\_RSMRST# ACTIVE HIGH TO PM\_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms+Please reference Intel 16971 Page 301of t232 timing)
- T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- IMVP\_OK is same with SB\_PWRGD(reserved And Gate with SYS\_PWRGD)
- In G7X power sequence :3VRUN-->NVDD,PEX\_VDD-->1\_8VRUN
- T15 : Please refer to MAX8771 datasheet
- T16: Please refer to MAX8771 datasheet
- T17 : Please refer to Intel CK410(14690) page 53
- T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- T20 : From ECRST# L->H to IMVP\_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

**Remark :** (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV) SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF\_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2.5VRUN -> GMCH\_VCC(1.05V), dt:0.7mV
- +1\_5VRUN -> +GMCH(1.05V), dt:0.7mV
- +3.3VRUN -> +2\_5VRUN, dt:0.3mV
- +3\_3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3\_3VRUN -> +1\_5VRUN(TV), dt:0.7mV



R/C delay (47k/0.1uF)

T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns-2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Min. 110ms	1 - 2 RTCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	

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**Power Sequence**

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<1>2006/3/28 remove U36.SW no need to program for present application.

<2>2006/3/28 Change PR5 from 13K to common parts 10KOhm.

<3>2006/3/29 Change USB CONN. CN16 & CN40 for ID requirement.  
P/N : FOX\_UB11193-C1301-4F

<4>2006/3/29 Change ODD CONN. CN21 for ID requirement.  
P/N : FOXCONN\_QT8H0506\_64T2R\_4F

<5>2006/3/29 Change PC359,PC360 to 10uF  
P/N : 1C-2B70106-M100

<6>2006/3/29 update new HDD CONN CN24.  
P/N : 2N-0022002-F0G0

<7>2006/3/29 update new DC-IN CONN PCN1.  
P/N : FOX\_GS53020-00580-7F

<8>2006/3/29 update new BTY CONN PCN2.  
P/N : FOXCONN\_BP34063\_B6012\_7F

<9>2006/3/30 U18.U19.U21.R277.R300.R315change to NC according to Customer's feedback.

<10>2006/3/30 R269,R273,R276,R286,R287,R300 change to Populate according to Customer's feedback.

<11>2006/3/30 New add INV\_ENABLE\_EC logic dur to BIOS Code merge issue.add new component :  
U53.U54 P/N : 14-74AHC1G-0800  
R762 P/N : 1R-0000103-J200  
R763 P/N : 1R-0000000-J200  
R764 P/N : 1R-0000104-J200  
Delete R176.R177

<12>2006/3/31 Add C20,C21,C22,C31,C33,C68 for EMI slution.  
P/N : 1C-2Y20104-Y000

<13>2006/3/31 Add R5 for Customer feedback.  
P/N : 1R-0000000-J200

<14>2006/3/31 Dummy R482,R483 for Customer feedback.

<15>2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component :  
U55.U56 P/N : 15-RT9702A-0000  
C521.C522 P/N : 1C-2Y20104-Y000  
R569.R573 P/N : 1R-0000105-J200  
C870.C871 P/N : 1C-2Y30225-Y000  
C535.C751 P/N : 1C-2B70106-M100  
Deleted Component :  
Q12.Q13.Q20.Q21.C535.C527.C521.C751.C753.C752.R486.R476.R568.R569

<16>2006/3/31 CN2 Pin11 change to +3V\_S3\_SUS for Customer feedback.

<17>2006/4/3 CN20.CN32.CN33 Pin assignment modified due to Customer's concern.

<18>2006/4/3 CN31.CN32.CN33 CN34 Connector change.  
P/N : GB11261\_1051\_7F

<19>2006/4/3 L17 & L19 updated according to Customer feedback  
P/N : 1L-DCS0603-1000

<20>2006/4/4 Add PWR\_MIZER circuit.  
U6J GPIO10 with new signal "NV\_PWR\_MIZER"  
new Components added and modified as below :  
10K Ohm -- R130.R766 -- P/N : 1R-0000103-J200  
7.5K Ohm -- R765.R767.R768.R769.R770 -- P/N : 1R-0000752-F200  
4.3K Ohm -- R128 -- P/N : 1R-0000432-F200  
2N7002EPT -- Q54.Q55.Q56.Q57.Q58 -- P/N : 17-2N7002E-PT00

<21>2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.

<22>2006/4/4 D6.D7.D8 change to Q59.Q60.Q61  
P/N : 17-2N7002E-PT00

<23>2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate.  
P/N : 1R-0000121-J200

<24>2006/4/4 new add Q62 for WLAN LED Logic  
P/N : 17-2N7002E-PT00

<25>2006/4/4 NC F1 and C859 according to customer's feedback.

<26>2006/4/4 delete R482.R483 according to customer's feedback.

<27>2006/4/6 add H3 ~ H20

<28>2006/4/6 Update BTY Connector PCN2 for ME requirement.  
P/N : 2N-0006001-MKX0

<29>2006/4/6 R278.R289.R270 change to 75Ohm and circuit modified as customer's feedback.  
P/N : 1R-0000750-F200

<30>2006/4/6 R543 change to 75Ohm as customer's feedback.  
P/N : 1R-0000750-F300

<31>2006/4/6 R553 change to 75Ohm as customer's feedback.  
P/N : 1R-0000750-J200

<32>2006/4/6 R99.R94.R97.R109.R67.R64.R65.R75 change to NC as customer's feedback.  
and R66.R69.R98.R101 change to 120Ohm.  
P/N : 1R-0000121-J200

<33>2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.

<34>2006/4/6 CN31 Pin1.2 change to +3V\_S3\_SUS as customer's feedback.

<35>2006/4/6 add 1A Fuse F4.F5.F9.F11.F15.F17.F18.F19  
P/N : 1M-F32V1A0-F000

<36>2006/4/6 add 0.5A Fuse F2.F3.F6.F7.F8.F10.F12.F13.F14.F16.F18  
P/N : 1M-F32V0A5-F000

<37>2006/4/6 add C872 according to MS20 lesson learn.  
P/N : 1C-2B20102-M000

<38>2006/4/6 CN34 Pin23.24 change to +3VRUN.

<39>2006/4/6 add C71.C74.C87 for EMI.  
P/N : 1C-2Y20104-Y000

<40>2006/4/6 add C89.C188.C199.C208.C213.C214  
P/N : 1C-2Y20104-Y000

<40>2006/4/7 add C215.C216.C217.C218.C219 for EMI solution.  
P/N : 1C-2Y20104-Y000

<41>2006/4/7 R118.R119.R351 change to populate as customer's feedback.

<42>2006/4/7 Y1.C104.C107.C492.C497.C501.R433.R434.R427.R428.R429.R430.R132.  
R133.R134.R136.R117 change to NC as customer's feedback.

<43>2006/4/7 R439.R443 change to 0 Ohm as customer's feedback.  
P/N : 1R-0000000-J200

<44>2006/4/7 update Net name EN\_EXT\_DEV\_SENSE# as customer's feedback.

<45>2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component :  
PQ183 P/N : 17-2N7002D-W000  
PR115 P/N : 1R-0000101-J200  
PR103,PR114 P/N : 1R-0000104-F100  
PC87 P/N : 1C-2B20103-M000  
PQ38 P/N : 17-S14800B-DY00  
PC76 P/N : 1C-2B70106-M200

<46>2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component :  
PR273 P/N : 1R-0000103-F200  
PR773 P/N : 1R-0004992-F200  
PQ20 P/N : 17-2N7002E-PT00  
PR774 P/N : 1R-0000102-J200  
PC873 P/N : 1C-2Y20105-Y000

<47>2006/4/10 add H21-H24.

<48>2006/4/10 Rename Schematic Part referene.  
new version since 4/11

<49>2006/4/11 change R68.R133.R100  
P/N : 1R-0000151-F200

<50>2006/4/11 PR111.PR114 change to NC according to PWR team's suggestion in EVT.

<51>2006/4/11 Modify ODD reset circuit as customer's feedback.  
Add U37 P/N : 15-MAX809S-0000  
Add R516 P/N : 1R-0000104-J200  
NC R305

<52>2006/4/11 Remove C257 for EMI comment.

<53>2006/4/11 add ODD Reset RC.  
Add R517 P/N : 1R-0000103-J200  
Add C580 P/N : 1C-2Y20104-Y000

<54>2006/4/14 change R197.R198.R199.R200 to 60.4Ohm  
P/N : 1R-000604X-F200

<55>2006/4/14 add R518 for 0Ohm  
P/N : 1R-0000000-J200

<56>2006/4/14 CN7.C409.C412.L37.F16.R44.R45 change to CA from NV to fit configuration.

<57>2006/4/27 PR111.PR114 change to Populate from NC according to PWR team's suggestion in EVT.  
P/N : 1R-0000100-J200

### MS60-L change list base on MS60-H

<58>2006/5/02 Del all NV\_ components for L-model only.

<59>2006/5/03 Remove +1\_8VRUN discharge circuit.Delete PR169,PQ44. Add PQ54 P/N:17-2N7002E-PT00

<60>2006/5/03 LED2 pin2,pin3 swap for Power LED color opposite issue

<61>2006/5/03 Change CAP93,CAP94 to NEC,TEPSGV0E337M9-12R,330uF,2.5V  
P/N:1C-31T0337-MX00  
Add CAP95 P/N:1C-31T0337-MX00

<62>2006/5/04 F1,F2,F3,F4,F5,F6,F7,F8,F9,F10,F11,F12,F13,F14,F15,F16,F17,F19 change to fuse,1.1A PTC type  
P/N:1M-F06V1A1-F000

<63>2006/5/05 follow M/E change to exchange PCN1 pin1 & pin2 connection.Layout change placement form top side to bottom side.

<64>2006/5/05 Add GP14,GP15 open jump for repair conveniently

<65>2006/5/05 Add C581,C582,C583,C584,C585,C586,C587,C588,C589,C590,C591,C592 for 22uF\_0805\_6.3V shortage.

<66>2006/5/08 As to M/E assemble issue, we will need rotat 180degree about T/P module.So that R47 change to stuff

<67>2006/05/09 Rename CAP93,CAP94,CAP95 to PC93,PC94,PC176.And change component to Panasonic,EEFSX0D331ER,330uF,2V  
P/N:1C-42T0337-MX00

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<68>2006/05/09 PC54,PC58,PC59,PC139 change to X5R,0.1uF,6.3V,10%,0201 for X7R,0.1uF,10V,0201 shortage  
P/N:1C-2B10104-K100

<69>2006/05/11 L33,L34 pin swap .D12 & D10 change to TOP side for layout conveniently

<70>2006/05/12 PR198 change to 5.6k/0402\_1% to modify 1.8V OCP seting value.  
P/N:1R-0000562-F200

<71>2006/05/12 CN23 change to 'FOX\_MH11747-BR2D-4F' for ME requirement.  
P/N:2N-000400N-FKGO

<72>2006/05/12 CN3,CN8 change to 'FOX\_GB5RF120-1200-7F' for ME requirement.  
P/N:1N-0012001-F0T0

<73>2006/05/12 CN7 change to 'FFOXCONN\_GB5RF060\_1200\_7F' for ME requirement.  
P/N:1N-0006000-F0T0

<74>2006/05/12 CN12,CN16 change to 'FOXCONN\_UB11193\_C1304\_4F' for ME requirement.  
P/N:1N-0004000-FEG0

<75>2006/05/12 CN9 change to 'FOXCONN\_HS8206E' for ME requirement.  
P/N:1N-0006001-M1T0

<76>2006/05/16 Due to ripple noise issue.PC74,PC175 change to 'Panasonic,EEFSX0D331ER'  
.Del PC75 for power requirement.  
P/N:1C-42T0337-MX00

<77>2006/05/17 Add PQ55,PQ56,PR200,PR201,PR202,PR203 for power discharge.  
P/N:17-2N7002D-W000  
P/N:1R-0000331-J300  
P/N:1R-0000104-F100  
P/N:1R-0000101-J200

<78>2006/05/17 U24 change to 'FOXCONN\_P24782A\_2743\_01' for ME requirement.  
P/N:1N-1478002-0000

<79>2006/05/18 PC67 change to 10pF 0402,and need to mount for power requirement.  
P/N:1C-2N20100-J000

<80>2006/05/18 CN12,CN16 change footprint to 'FOXCONN\_UB11193\_C1304\_4F\_HM' for DFM.

<81>2006/05/18 Add R519,R520,C593,C594 on 'IAC\_BITCLK' signal for EMI requirement.  
P/N:1R-0000000-J200  
P/N:1C-2N20330-J000

<82>2006/05/18 H13,H15 footprint change to ' hole\_tc236bc315d114' for ME requirement.  
P/N:1X-HOLE000-0232

<83>2006/05/19 CN25 need change to P/N:1N-1200007-0000. CN26 need change to P/N:1N-1200008-0000. Because P/N:1N-120000C-0000 & P/N:1N-120000D-0000 part number are not available.

<84>2006/05/19 Add PC177,PC178,PC179,PC180 on DC\_IN trace for EMI requirement.  
P/N:1C-2B30104-K000

<85>2006/05/22 Del R89,R140,R127.Add L54,L55,L56 (0 ohm change to bead) for EMI requirement.  
P/N:1L-BEBMS16-0801

<86>2006/05/30 change R517 from 10Kohm to 0ohm for solving the ODD issue.  
P/N:1R-0000000-J200

**DVT change list**

<87>2006/06/15 Delete R264.R271 for Debug BD LED.

<88>2006/06/15 Del reset IC form ODD portion.Del R516,R517,C580. Change U37 to 74AHC1G08GW and connect GPIO\_ODD\_RST# form KBC for ODD reset.

<89>2006/06/15 Add R521 1k ohm and change R244 connection form 'ALW\_ON' to 'ALW\_ON\_1' for customer's requirement.  
P/N : 1R-0000102-J200

<90>2006/06/16 PORT\_DET# change from EC's pin81 to EC's pin176 for noise decreasing.

<91>2006/6/16 remove RP13 and replace with R519/R520 for WLAN issue improving.  
P/N : 1R-0000220-F200

<92>2006/6/16 Add one GPIO signal 'VISTA\_SUPPORT#' that is connected form EC's pin99 to CN1's pin17 to support Vista OS.

<93>2006/6/16 Add PQ57,PC181 for ODD power plane.  
P/N:17-S12304B-DS00  
P/N:1C-2B70106-M200

<94>2006/6/16 (HDD connector)CN21's pin18 change connection from NC to GND for the starting timing improvement.

<95>2006/6/17 Change PQ52 from SI7392DP to IRF807Z and change PQ53 from SI7336ADP to IRF8113 for power requirement.  
P/N:17-1RF7807-2000  
P/N:17-1RF8113-0000

<96>2006/6/17 PR198 change from 5.6K ohm to 7.32K ohm to modify OCP setting value.  
P/N:1R- 0007321-F200

<97>2006/6/17 U12 change from G961-18ADJEU to SC1565IS-2.5TRT for WWAN voltage drop improvement.  
P/N:15-SC15651-0000

<98>2006/6/19 pc117,pc179,pc178,pc180,pc115,pc91 change to populate for EMI requirement.

<99>2006/6/19 Add C595 at PRT\_IN power trace for EMI requirement.  
P/N:1C-2B30104-K000

<100>2006/6/19 Add PC116,PC117,PC118,PC120,PC122,PC123,PC124 at DCBATOUT power trace for EMI requirement.  
P/N:1C-2B30105-M000  
P/N:1C-2B30104-K000

<101>2006/6/19 Add R303 10K pulldown at U34's pin1 to avoid start abnormally for customer's requirement.  
P/N:1R-0000103-J200

<102>2006/6/19 PC171 change to NC\_ condition for power requirement.

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