

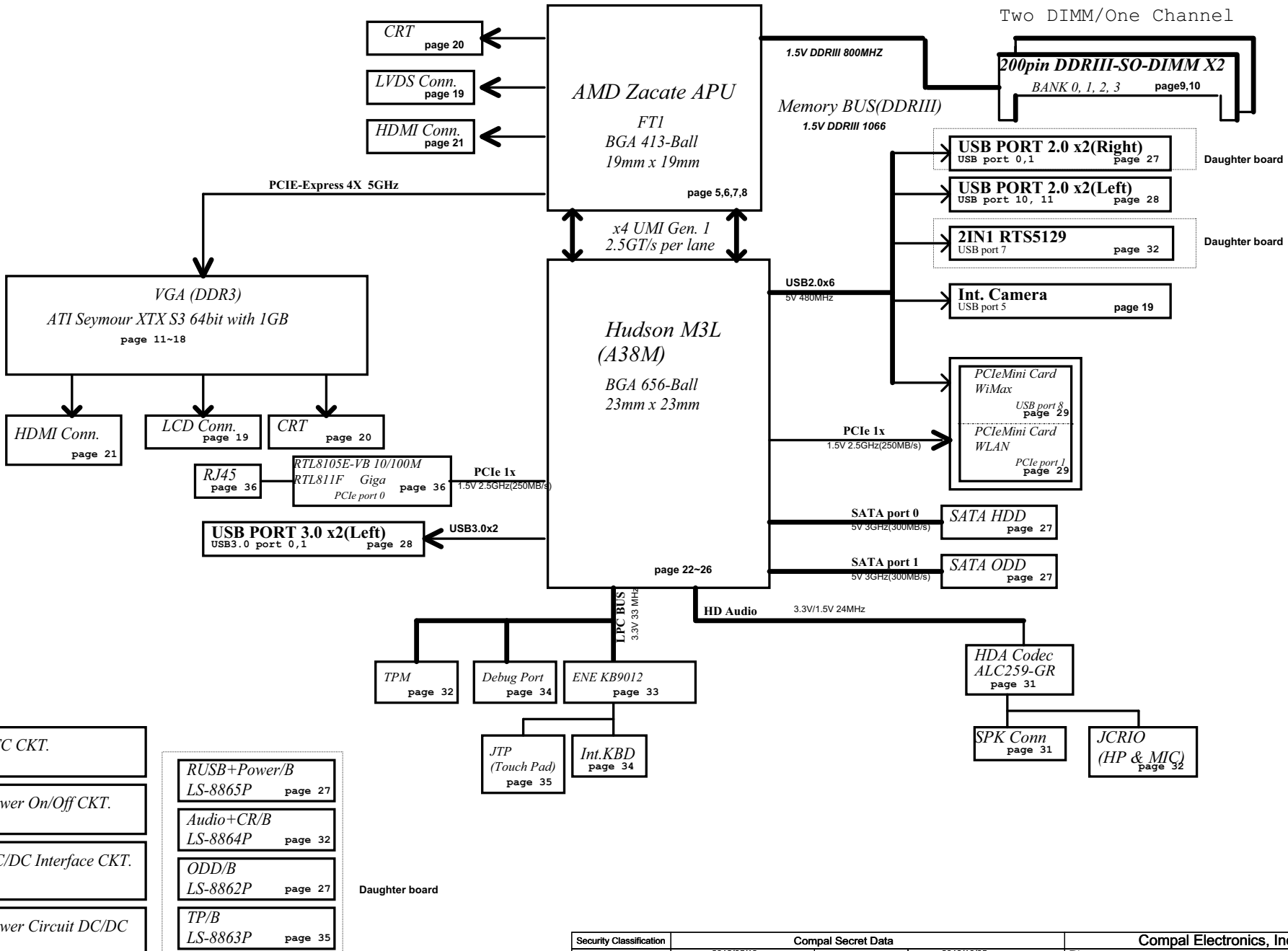
VBLE4 / VBLE5

Eureka

LA-8868P REV 1.0 Schematic

**AMD Brazos 2.0 / Zacate APU / Hudson-M3L FCH
2012-07-12 Rev 1.0**

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			4019K4	B
			Date: Saturday, September 07, 2013	Sheet 1 of 47



- RTC CKT.
- Power On/Off CKT.
- DC/DC Interface CKT.
- Power Circuit DC/DC

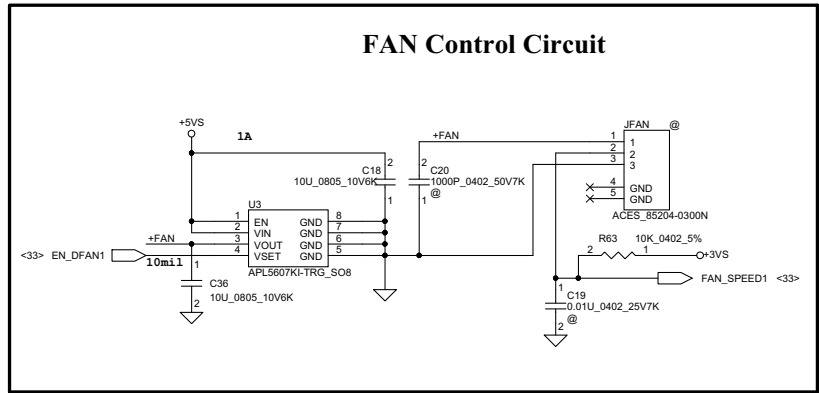
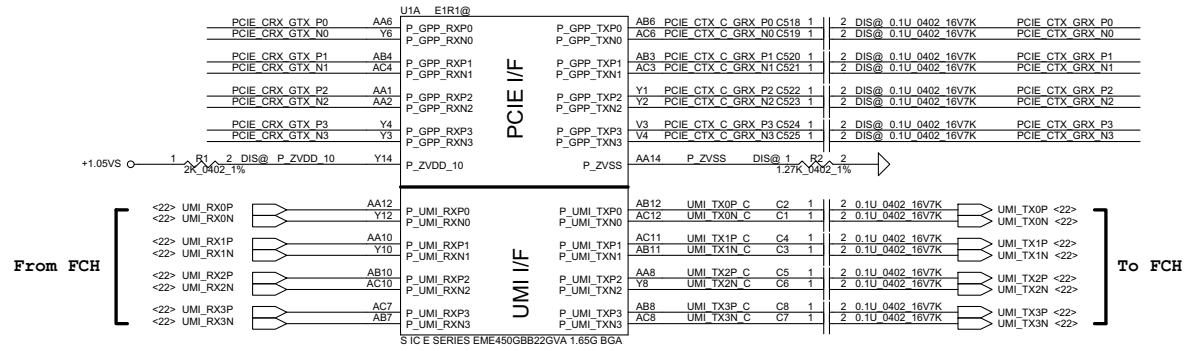
- RUSB+Power/B LS-8865P page 27
- Audio+CR/B LS-8864P page 32
- ODD/B LS-8862P page 27
- TP/B LS-8863P page 35

Daughter board

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				4019K4
				Date: Saturday, September 07, 2013
				Sheet 2 of 47

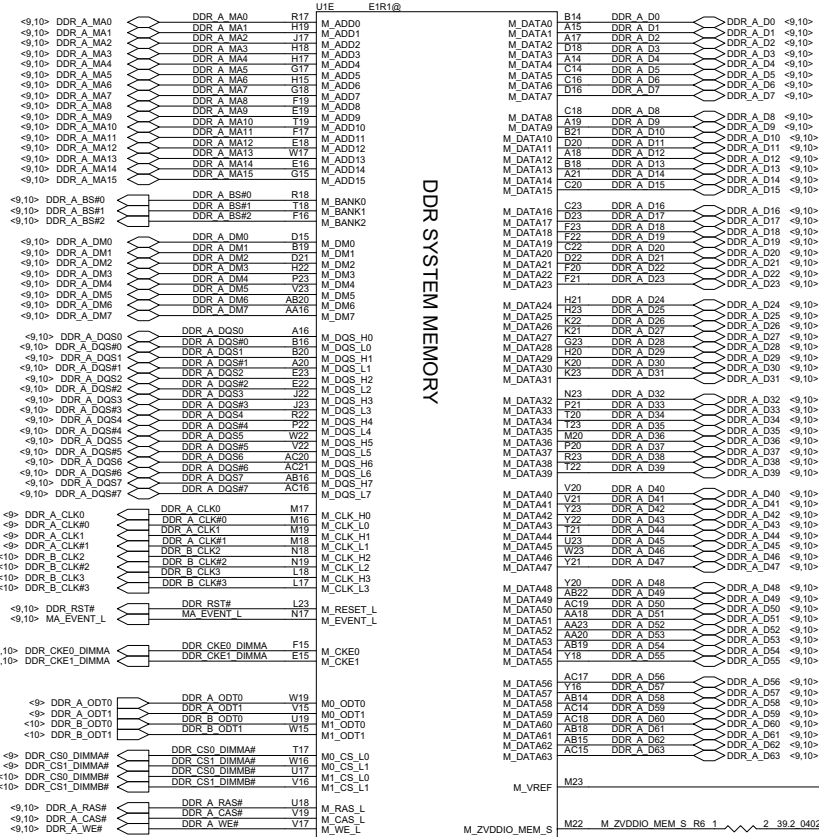
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<11> PCIE_CTX_GRX_P[3..0] ← PCIE_CTX_GRX_P[3..0]
 <11> PCIE_CTX_GRX_N[3..0] ← PCIE_CTX_GRX_N[3..0]
 <11> PCIE_CRX_GTX_P[3..0] → PCIE_CRX_GTX_P[3..0]
 <11> PCIE_CRX_GTX_N[3..0] → PCIE_CRX_GTX_N[3..0]

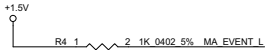


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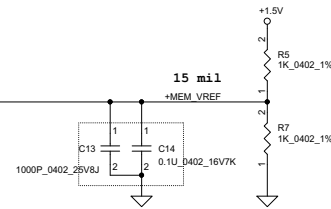
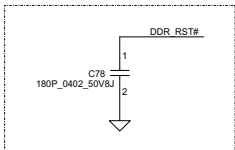
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Document Number	4019K4		Rev	B	
Date:	Saturday, September 07, 2013		Sheet	5 of 47	



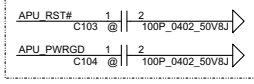
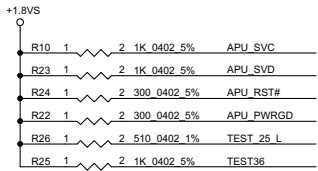
SIC E SERIES EME450GBB22GVA 1.650 BGA



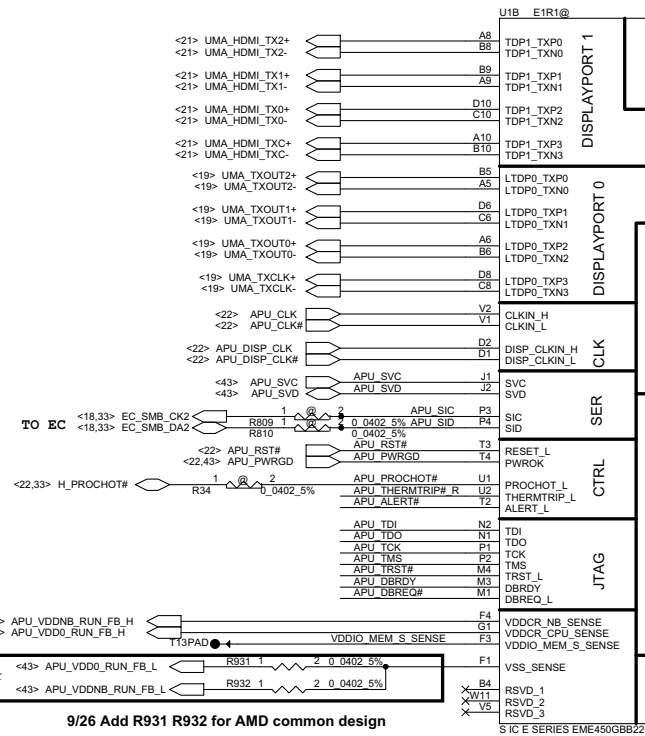
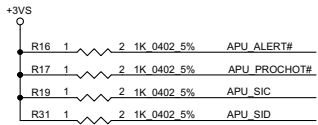
8/6 Add C78 for ESD request



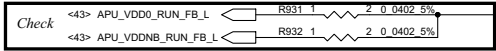
Close to CPU within 1"



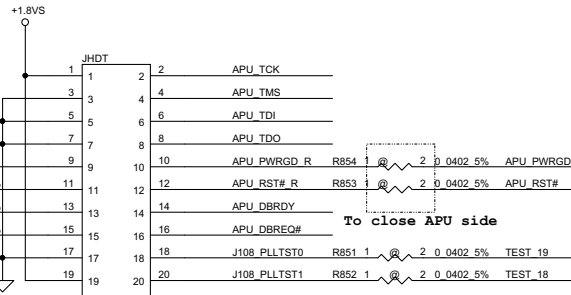
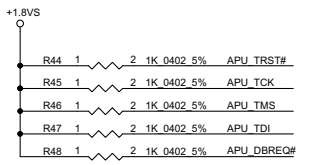
12/13 For debug if layout cross mote



9/26 Add R931 R932 for AMD common design

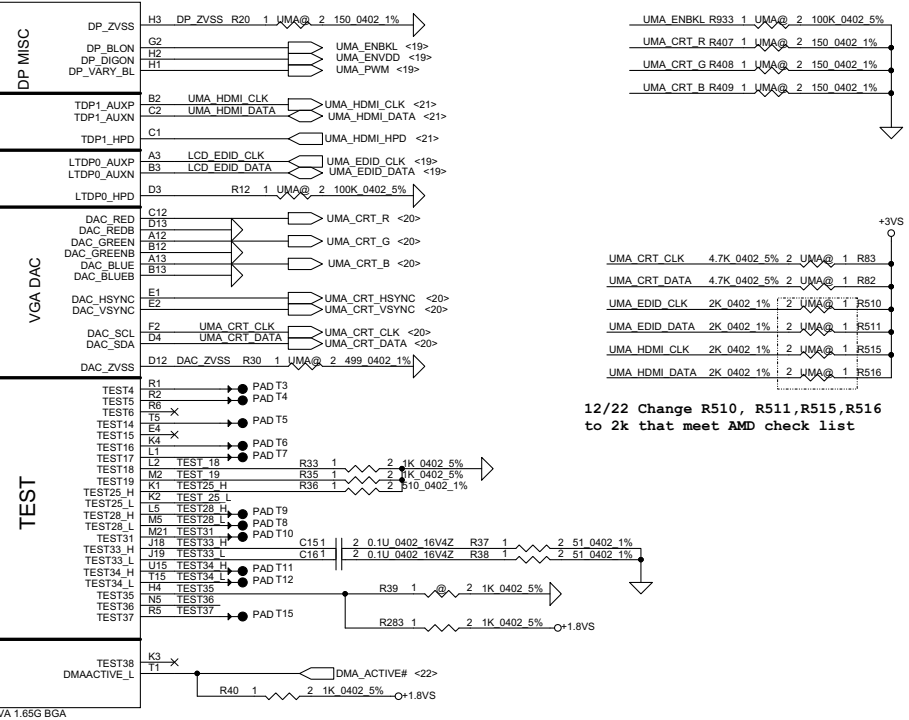


AMD HDT Debug Conn

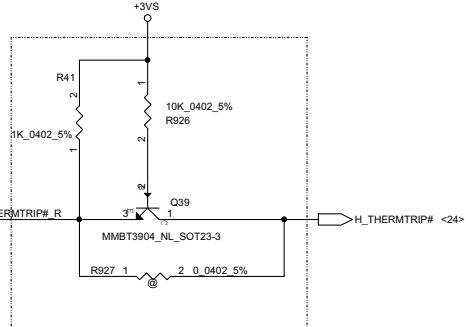


SAMTE_ASP-136446-07-B

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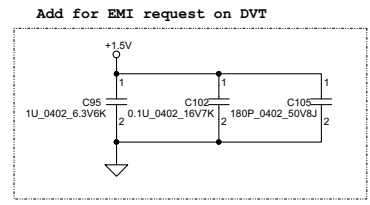
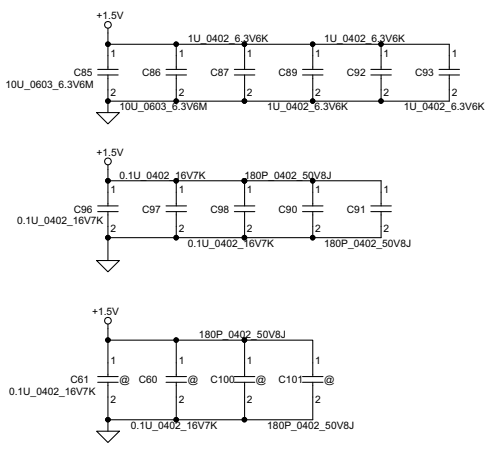
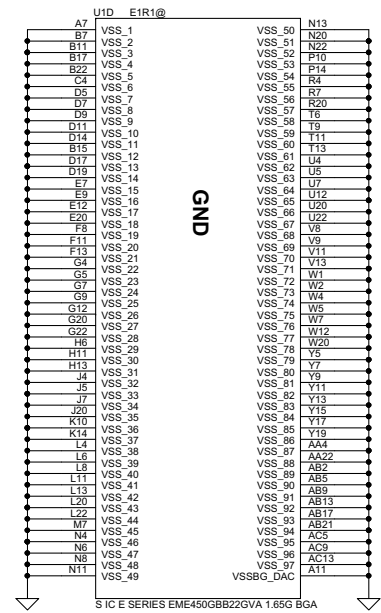
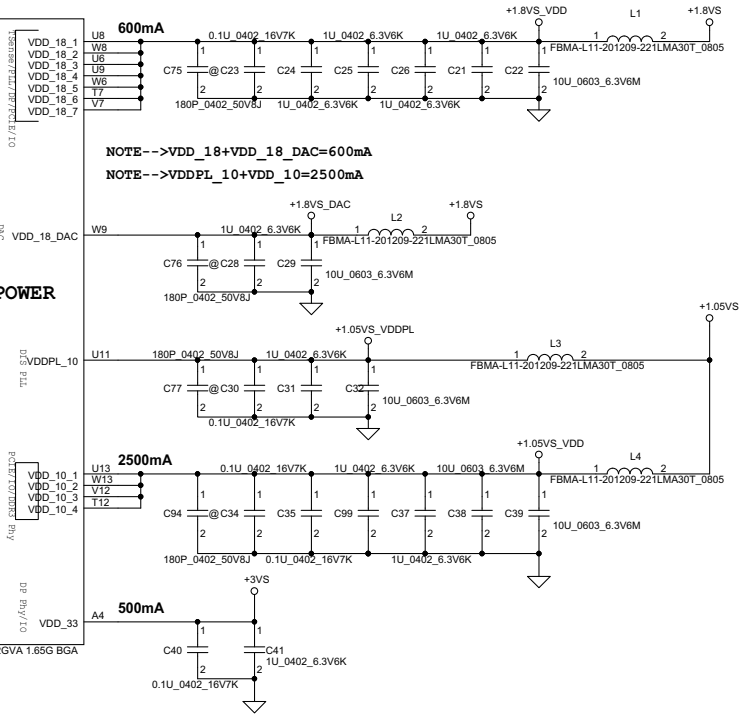
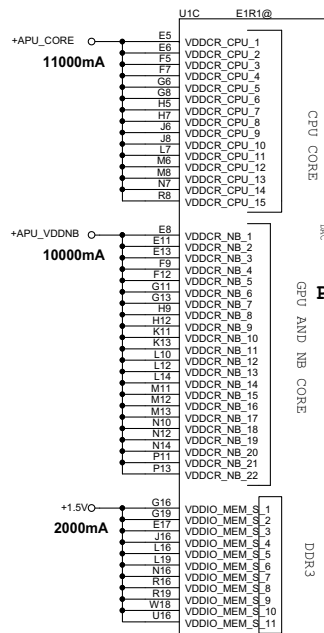


12/22 Change R510, R511, R515, R516 to 2k that meet AMD check list



12/22 PCH side has internal pull up +3VLAW_PCH, so need to level shift

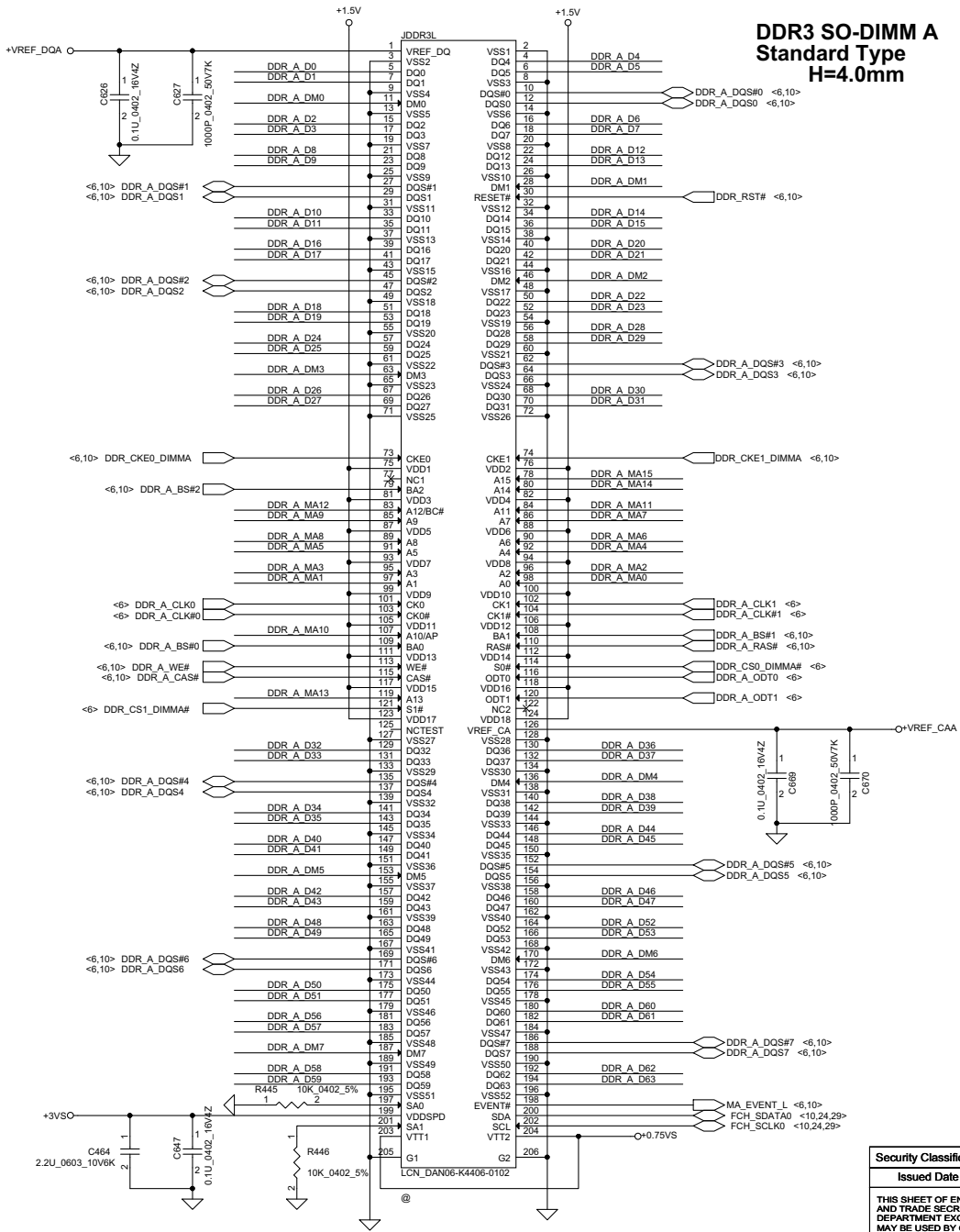
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Document Number	4019K4	Rev	B	Date	Saturday, September 07, 2013
Sheet	7	of	47		



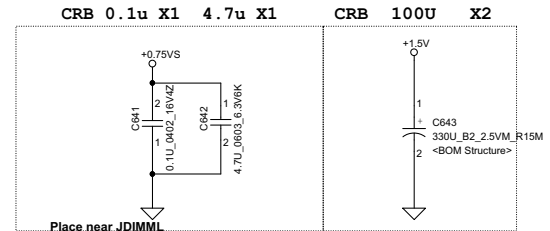
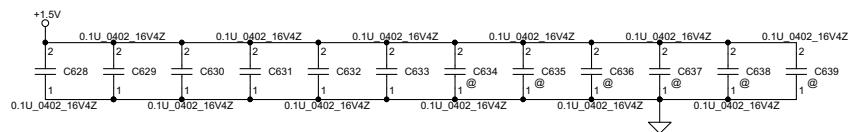
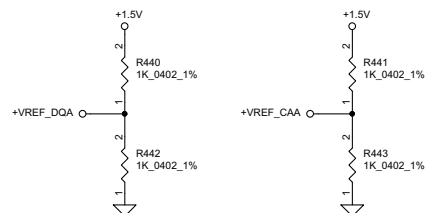
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Date:	Saturday, September 07, 2013	Sheet	8	of	47

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DDR3 SO-DIMM A Standard Type H=4.0mm

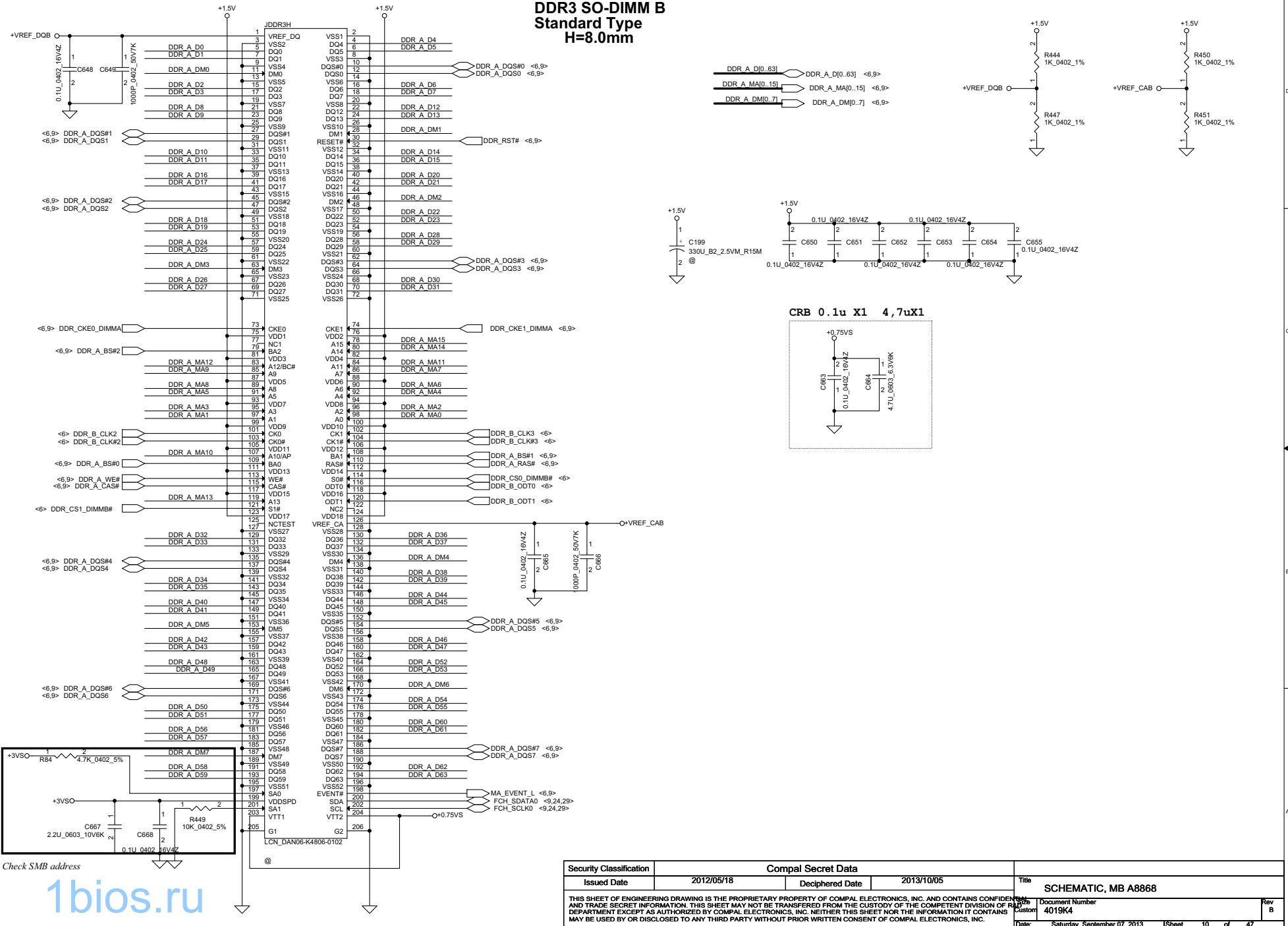


DDR_A D[0..63] → DDR_A_D[0..63] <6,10>
 DDR_A MA[0..15] → DDR_A_MA[0..15] <6,10>
 DDR_A DM[0..7] → DDR_A_DM[0..7] <6,10>



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Date:	Saturday, September 07, 2013	Sheet	9 of 47

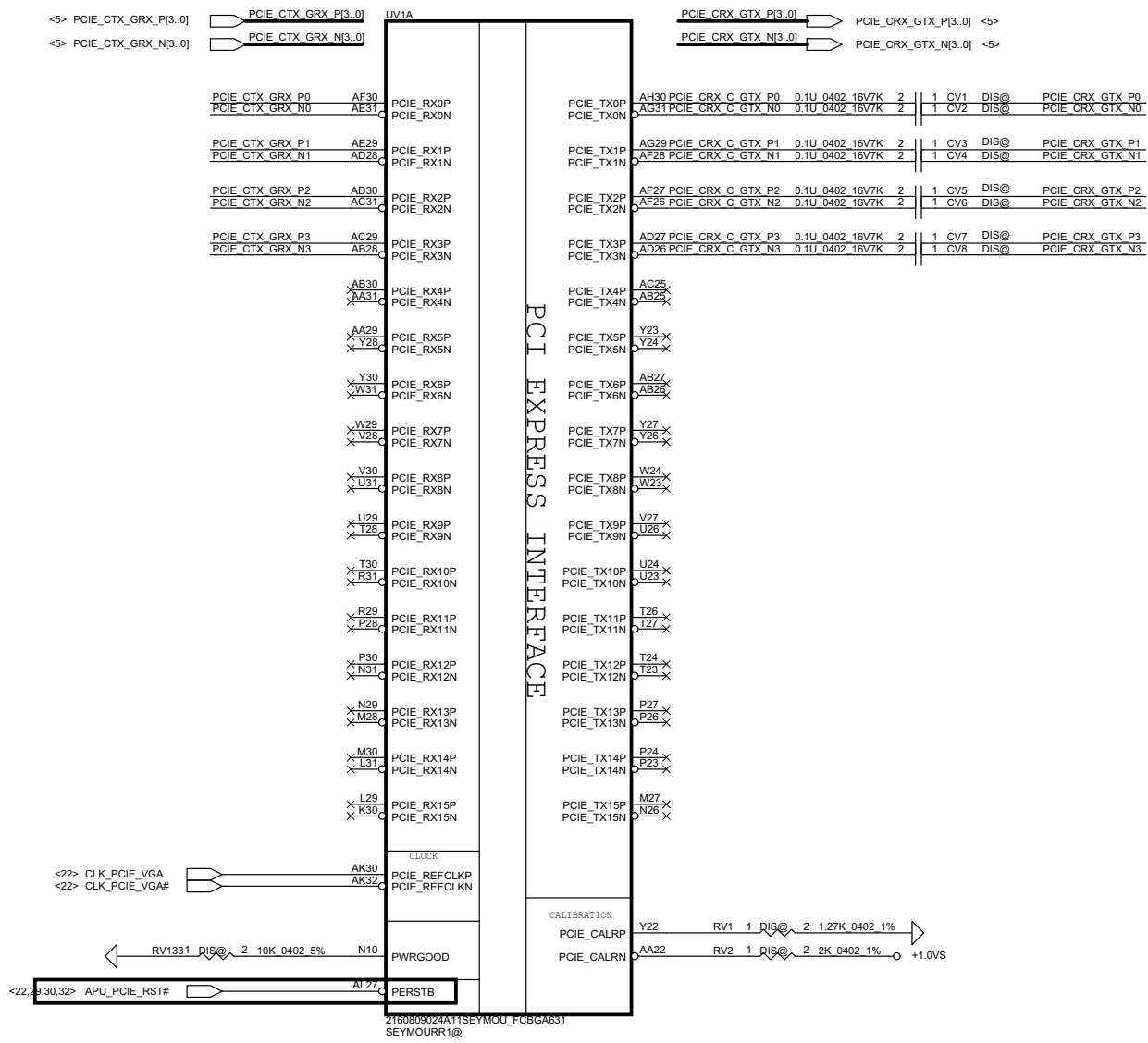
DDR3 SO-DIMM B Standard Type H=8.0mm



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Date:	Saturday, September 07, 2013	Sheet	10 of 47	Rev B

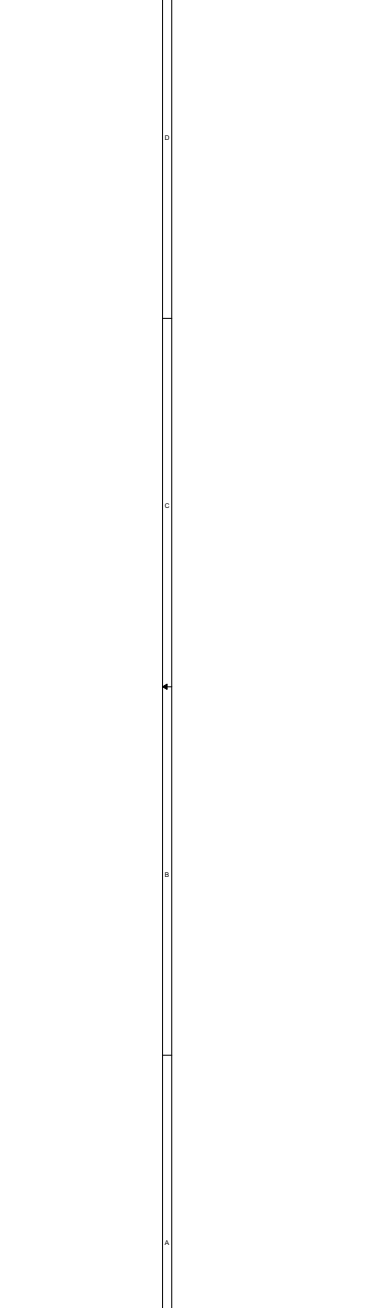
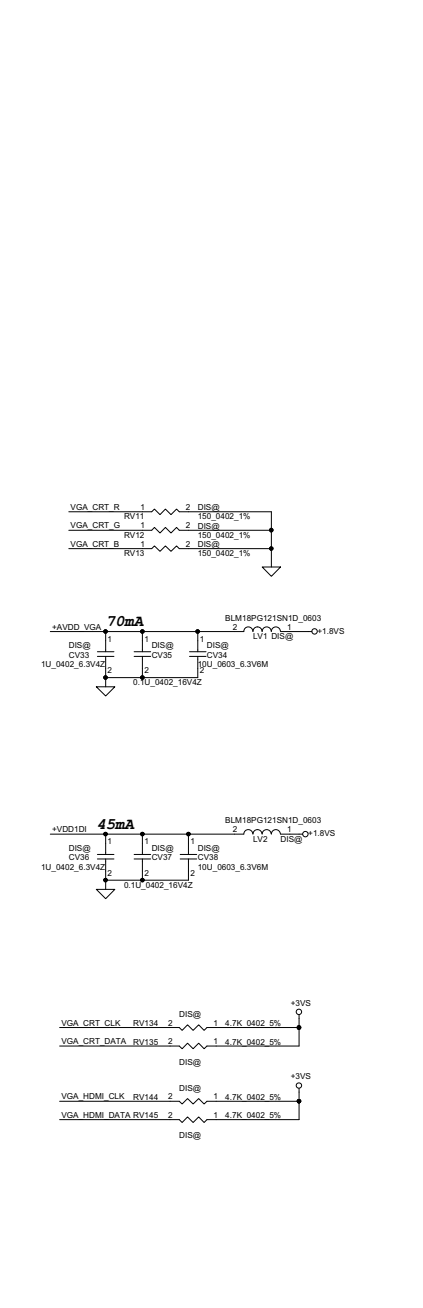
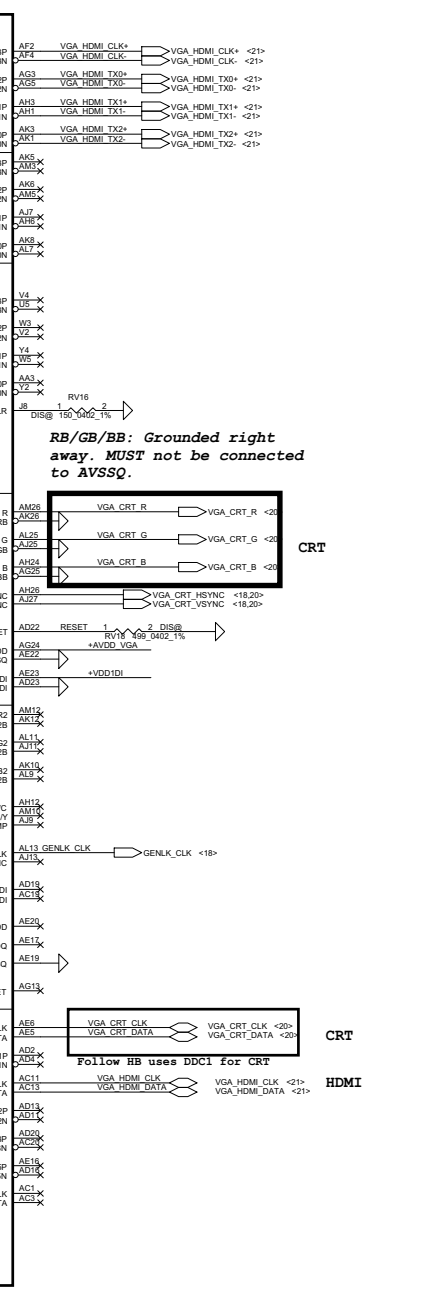
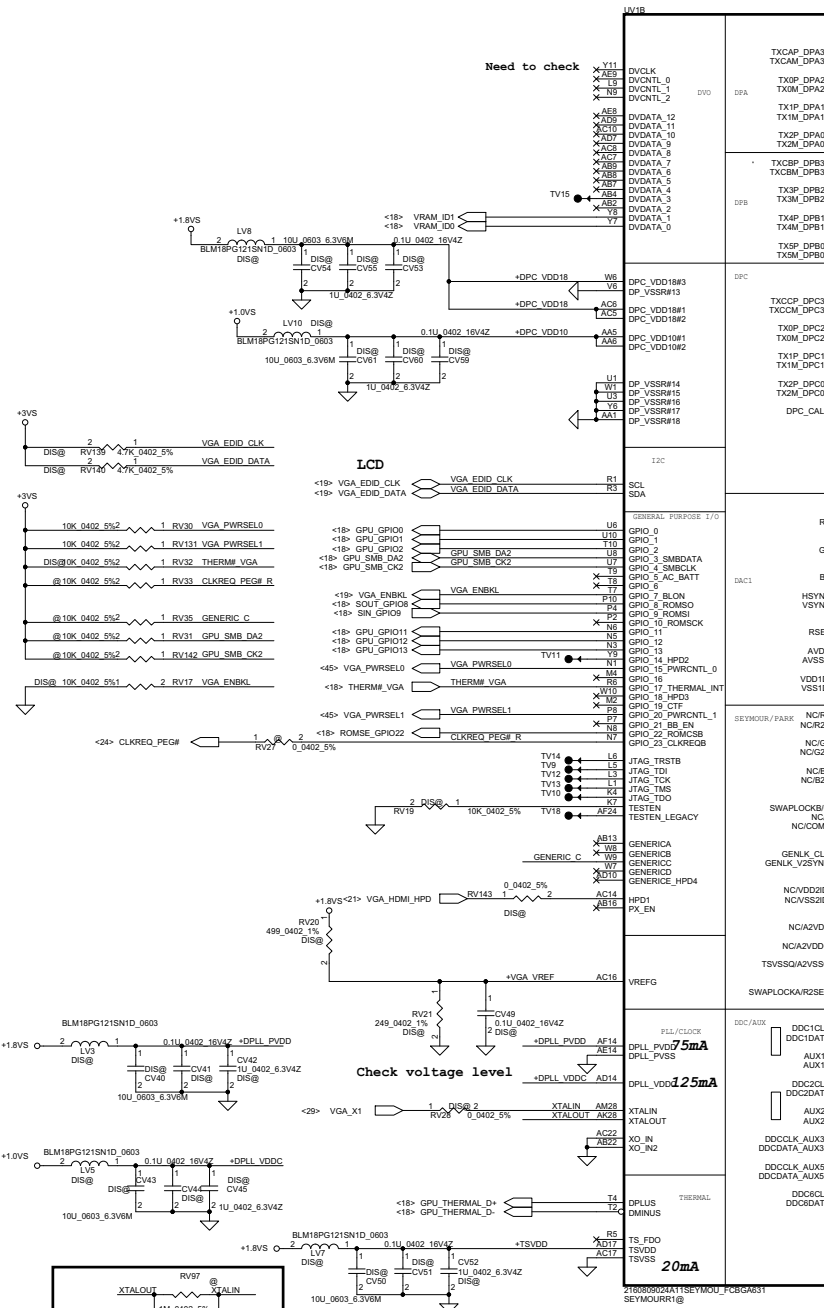
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Check SMB address

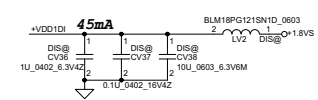
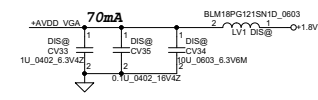
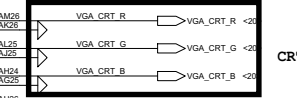


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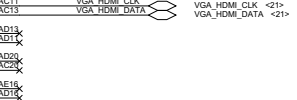
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				4019K4	
Date: Saturday, September 07, 2013				Sheet	11 of 47



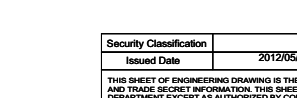
RB/CB/BB: Grounded right away. MUST not be connected to AVSSQ.



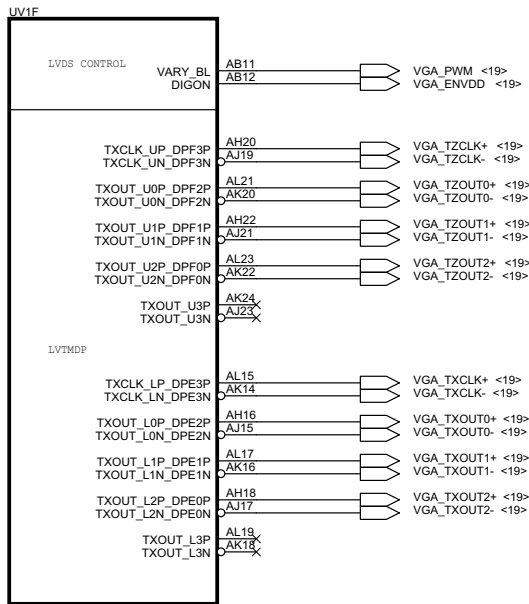
Follow HB uses DDC1 for CRT



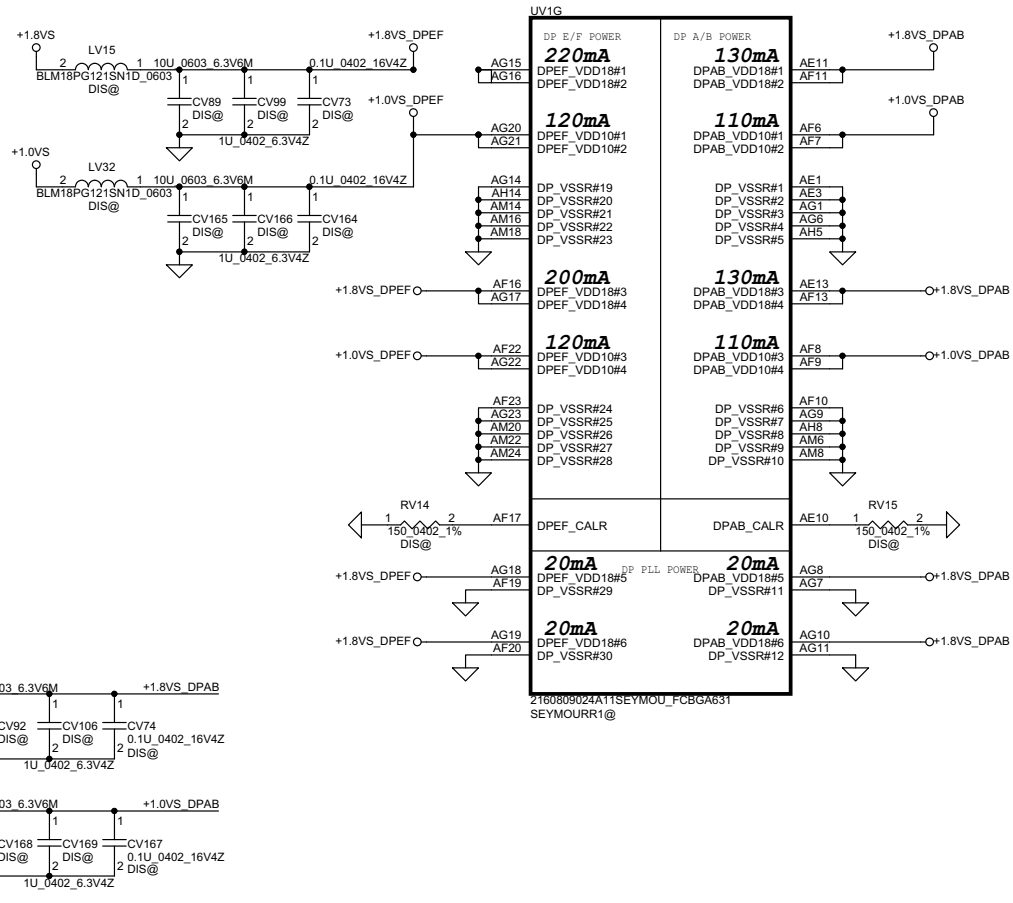
20mA



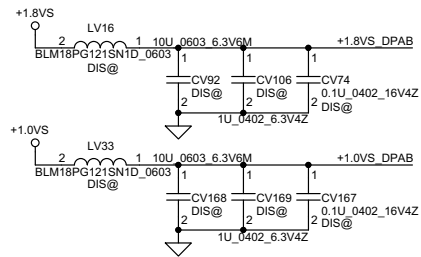
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Rev	B		Document Number	4019K4	
Date	Saturday, September 07, 2013		Sheet	12 of 47	



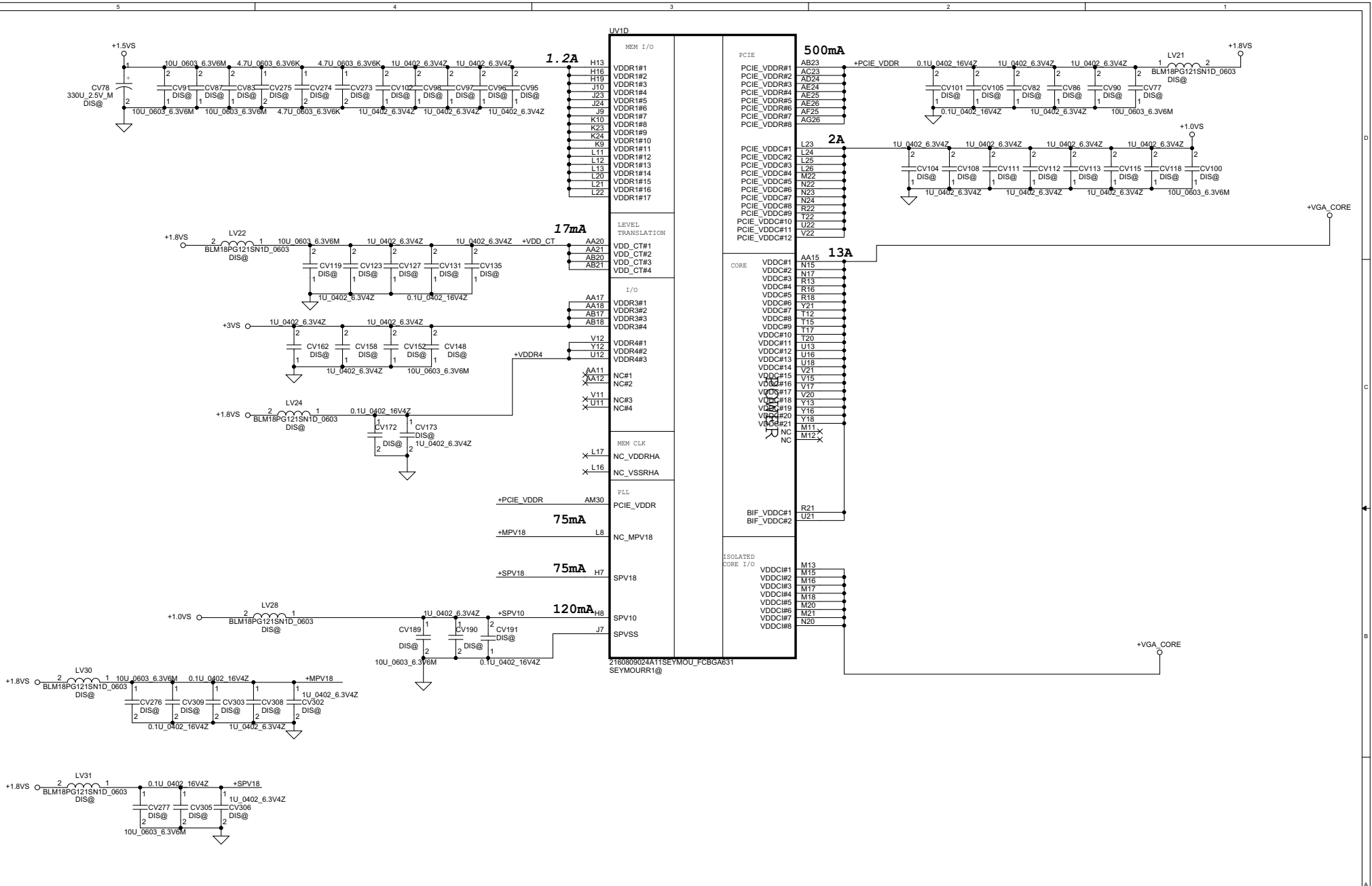
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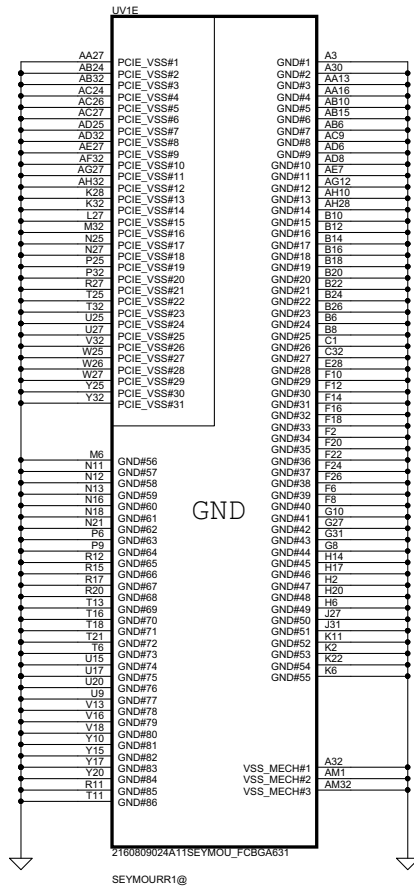
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Date:	Saturday, September 07, 2013	Sheet	13	of 47

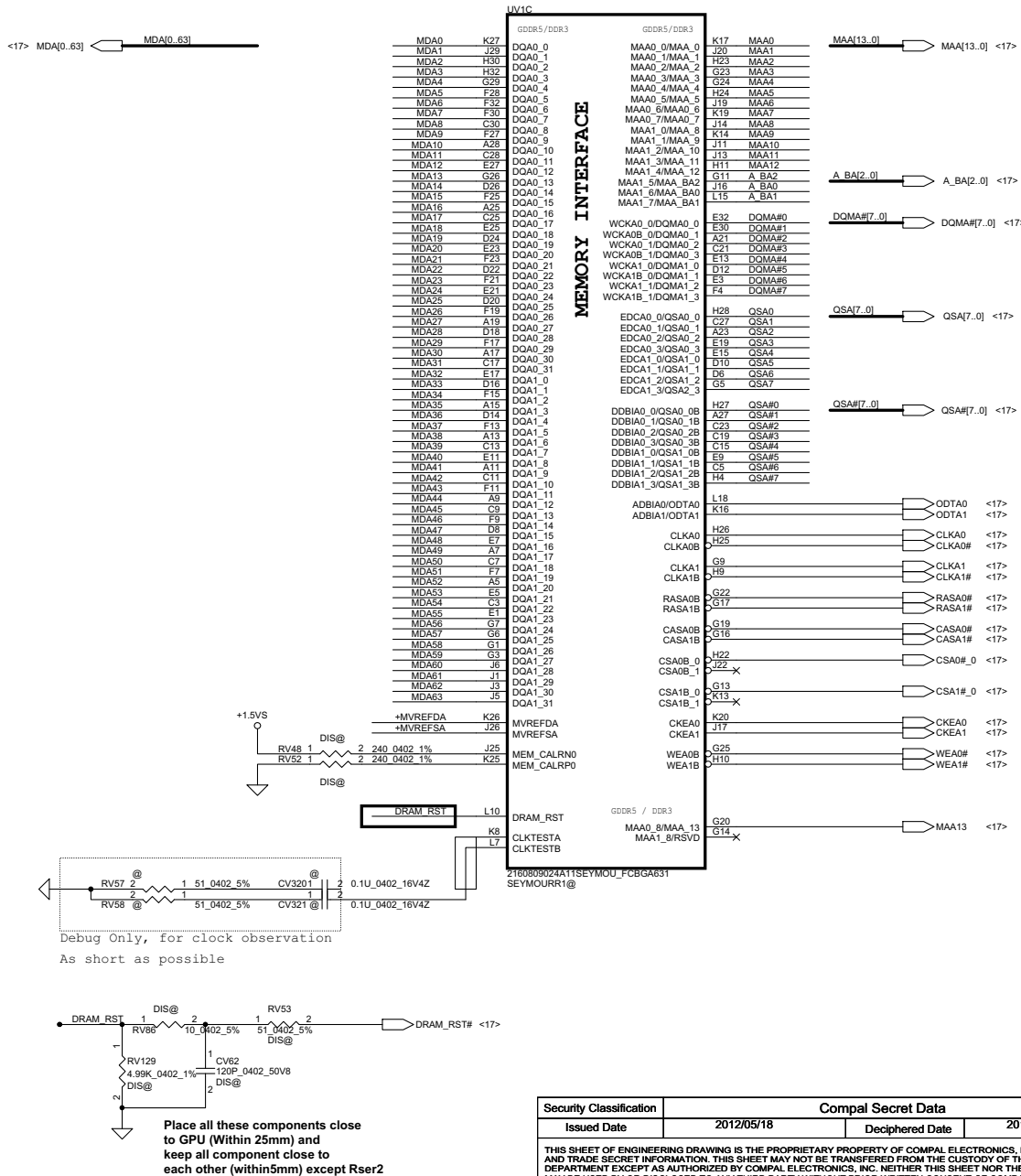


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				Date: Saturday, September 07, 2013 Sheet 14 of 47	



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				4019K4
Date:				Rev
Saturday, September 07, 2013				B
Sheet				15 of 47

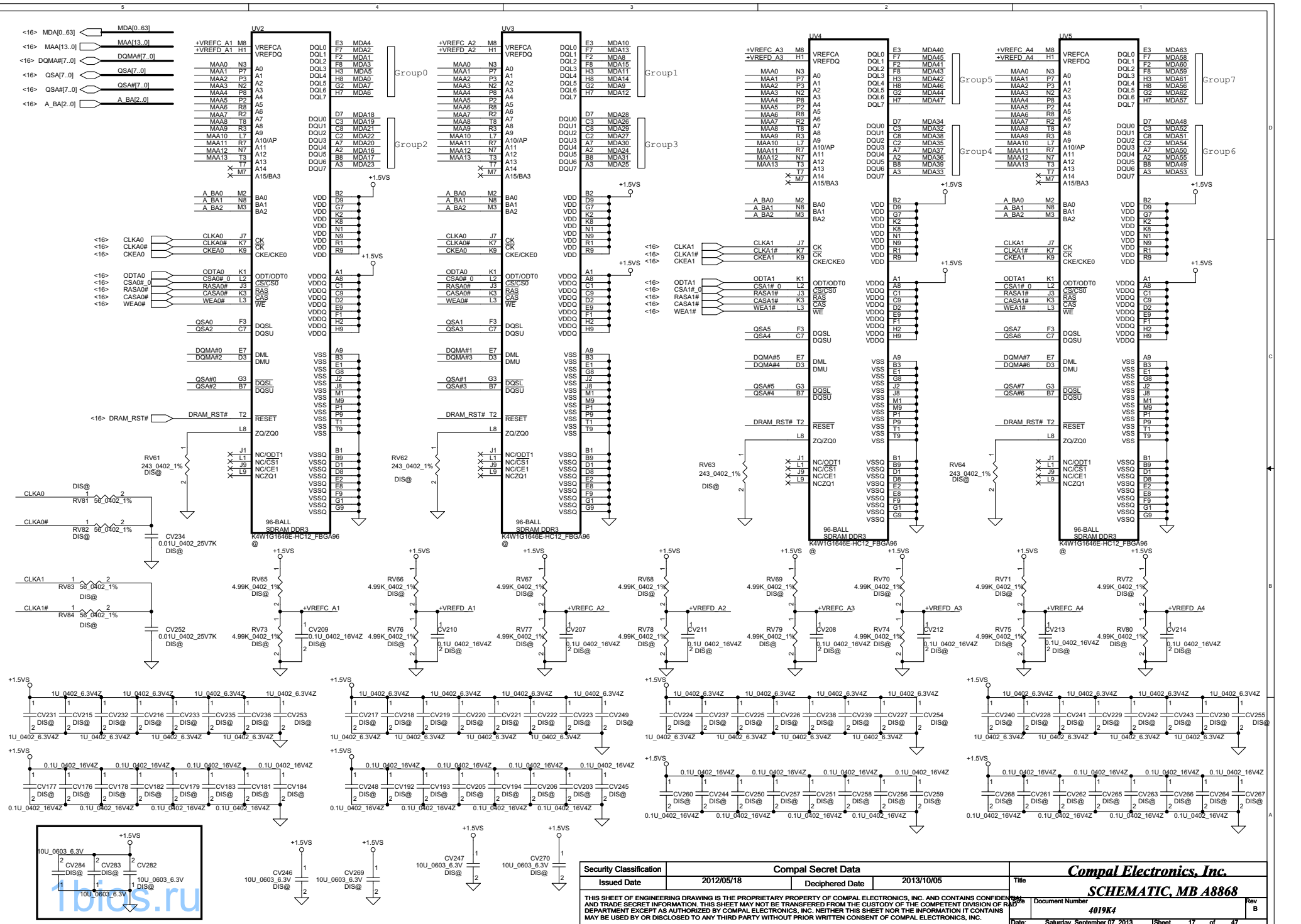


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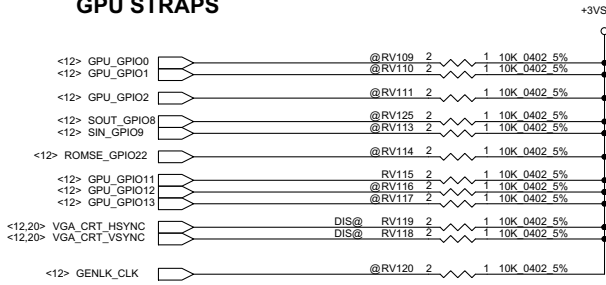
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Title	SCHEMATIC, MB A8868
Document Number	4019K4
Date	Saturday, September 07, 2013
Sheet	16 of 47

Rev B



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Date:	Saturday, September 07, 2013	Sheet	17	of 47

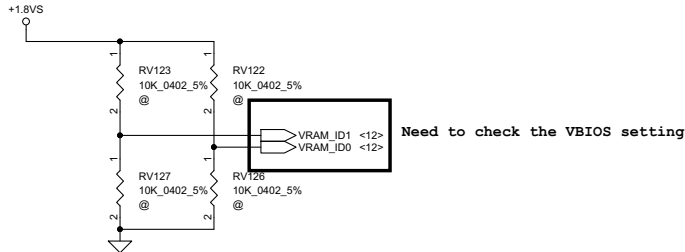
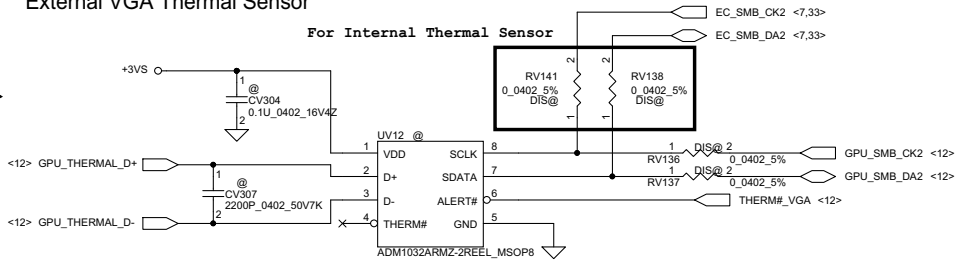
GPU STRAPS



GPU by the system BIOS		GPU by VBIOS	
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)	
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]	
0 0 0	128MB	1 0 0	
0 0 1	256MB	(M25P05A)	
0 1 0	64MB		

External VGA Thermal Sensor

For Internal Thermal Sensor



Need to check the VBIOS setting

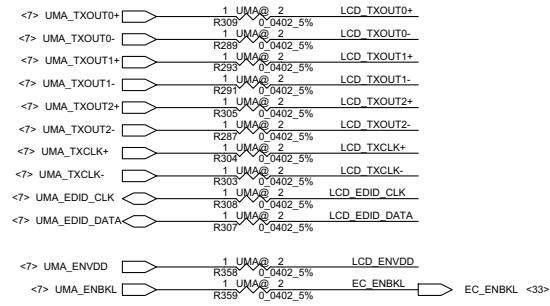
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

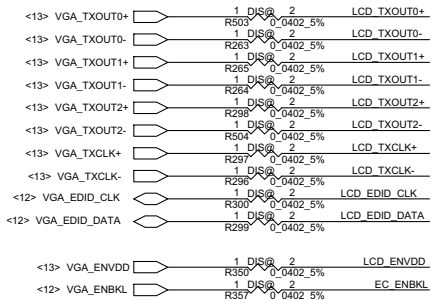
Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
RESERVED	GENLK_CLK	GENLK_CLK		0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 1,0
VRAM_ID[1:0]	DVIDATA (1,0)	Seymour-S3	512M 64Mx16 (x4)	SAM K4W1G1646G-BC11	SA00004GS00	1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC11	SA000047Q00	1 1

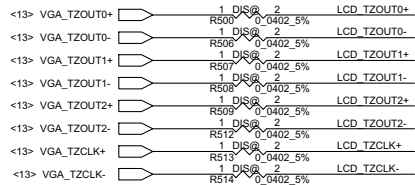
UMA



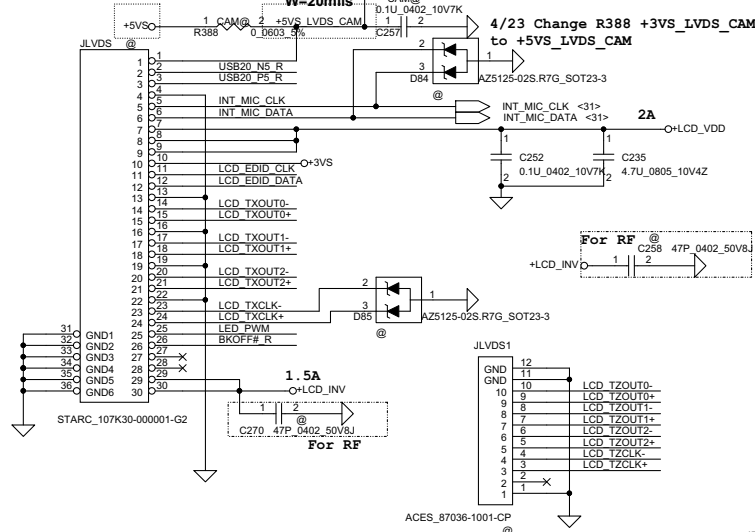
DISCRETE



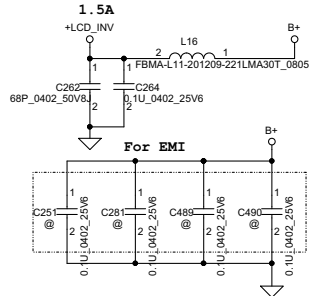
Close to LVDS Connector



4/23 Change R388 +3VS to +5VS

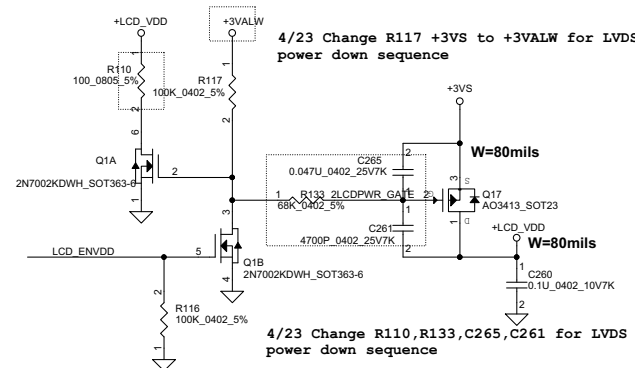


1.5A
LCD_INV

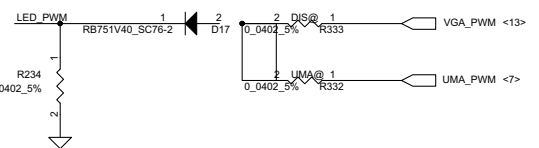
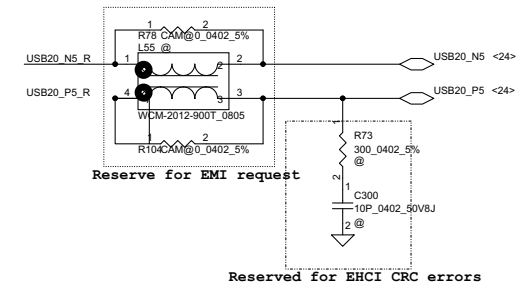


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4/23 Change R117 +3VS to +3VALW for LVDS power down sequence



4/23 Change R110, R133, C265, C261 for LVDS power down sequence

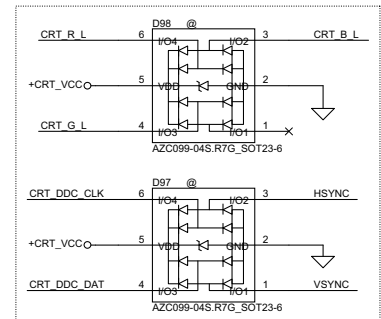
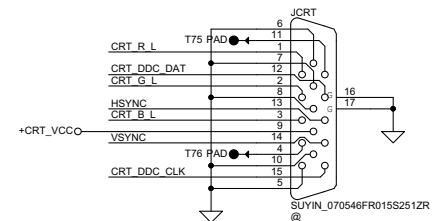
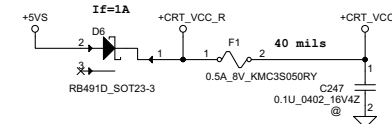


Reserve for LVDS panel

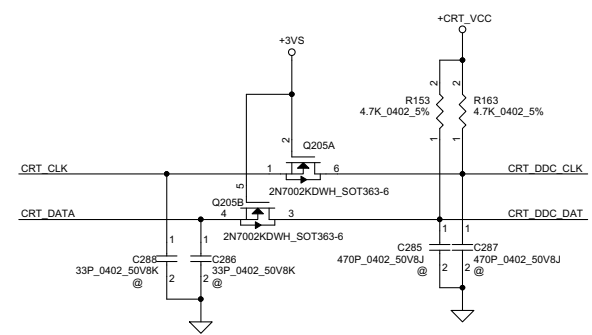
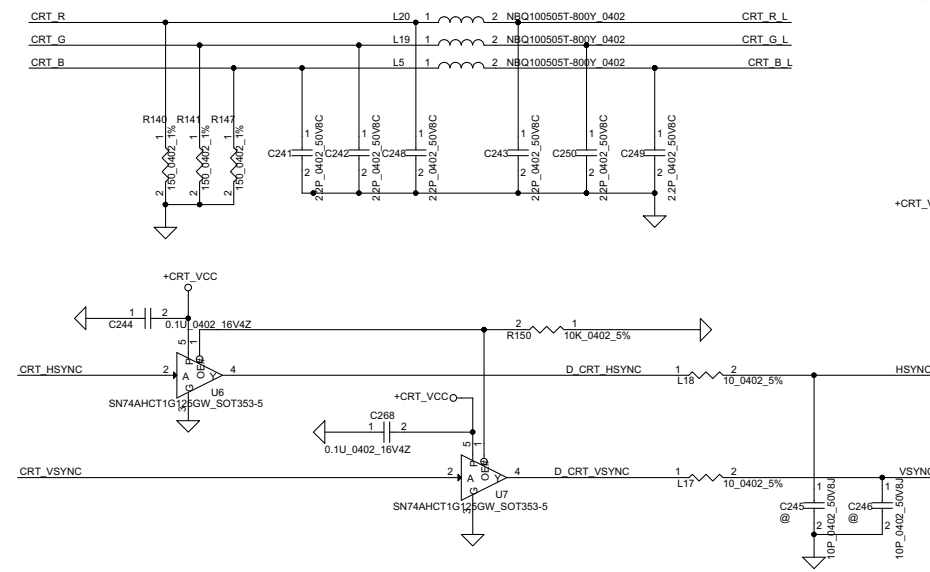
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Date: Saturday, September 07, 2013				Sheet	19	of	47

CRT CONNECTOR

Remove D3~D5 on DVT



Reserve ESD for CRT connector on DVT



UMA

<7> UMA_CRT_R	1 UMA @ 2	CRT_R
	R221 0.0402_5%	
<7> UMA_CRT_G	1 UMA @ 2	CRT_G
	R222 0.0402_5%	
<7> UMA_CRT_B	1 UMA @ 2	CRT_B
	R223 0.0402_5%	
<7> UMA_CRT_HSYNC	1 UMA @ 2	CRT_HSYNC
	R224 0.0402_5%	
<7> UMA_CRT_VSYNC	1 UMA @ 2	CRT_VSYNC
	R235 0.0402_5%	
<7> UMA_CRT_CLK	1 UMA @ 2	CRT_CLK
	R238 0.0402_5%	
<7> UMA_CRT_DATA	1 UMA @ 2	CRT_DATA
	R285 0.0402_5%	

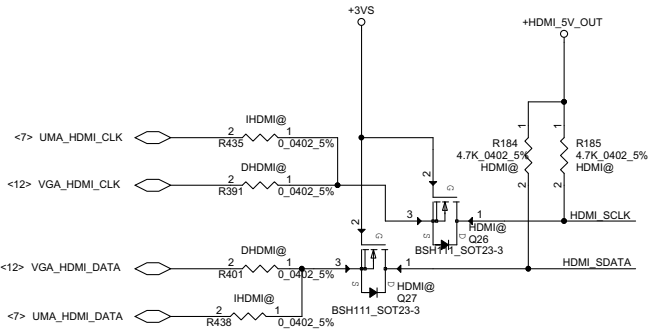
Close to CRT Connector

DISCRETE

<12> VGA_CRT_R	1 DIS @ 2	CRT_R
	R232 0.0402_5%	
<12> VGA_CRT_G	1 DIS @ 2	CRT_G
	R233 0.0402_5%	
<12> VGA_CRT_B	1 DIS @ 2	CRT_B
	R229 0.0402_5%	
<12,18> VGA_CRT_HSYNC	1 DIS @ 2	CRT_HSYNC
	R230 0.0402_5%	
<12,18> VGA_CRT_VSYNC	1 DIS @ 2	CRT_VSYNC
	R231 0.0402_5%	
<12> VGA_CRT_CLK	1 DIS @ 2	CRT_CLK
	R225 0.0402_5%	
<12> VGA_CRT_DATA	1 DIS @ 2	CRT_DATA
	R226 0.0402_5%	

Close to CRT Connector

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<p>Date: Saturday, September 07, 2013</p>				<p>Sheet 20 of 47</p>

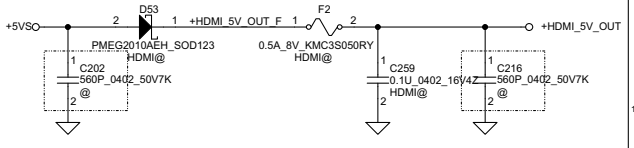
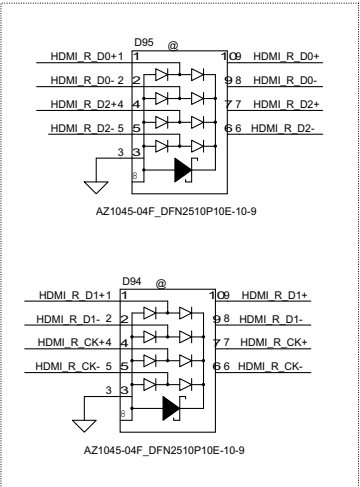
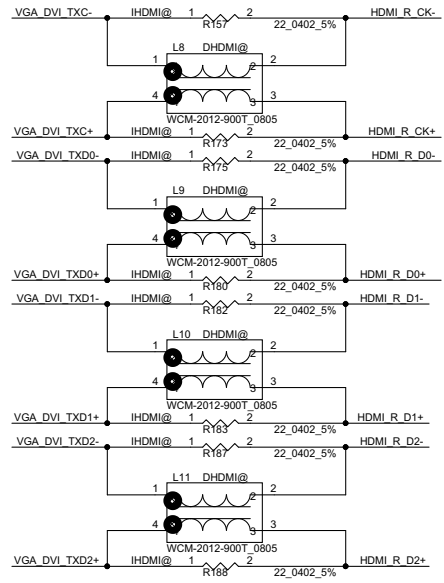
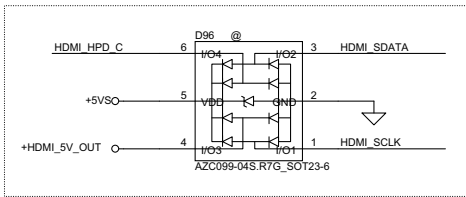


DISCRETE

<12> VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC+
<12> VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC-
<12> VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0+
<12> VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0-
<12> VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1+
<12> VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1-
<12> VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2+
<12> VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2-

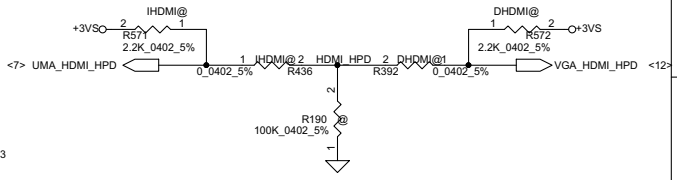
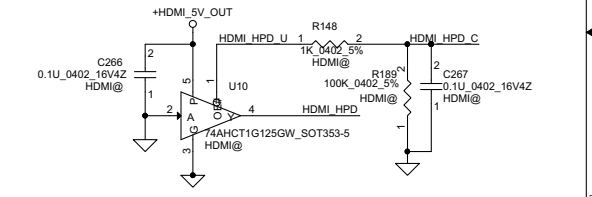
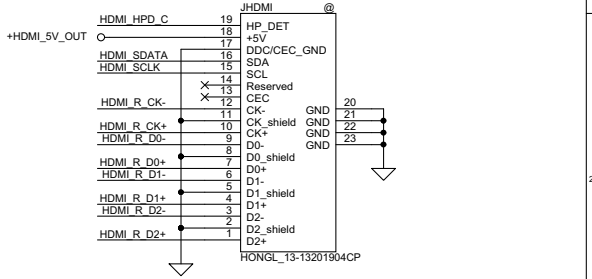
UMA

<7> UMA_HDMI_TXC+	C838	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	C837	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	C843	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	C844	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	C841	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	C842	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	C839	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	C840	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2-

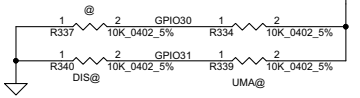
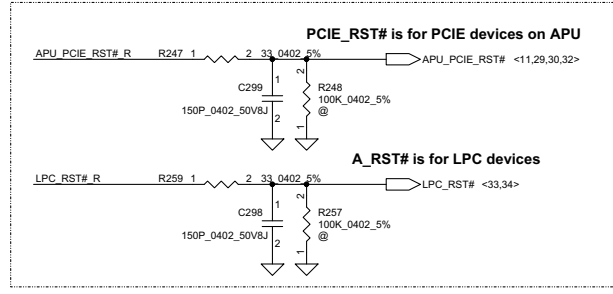
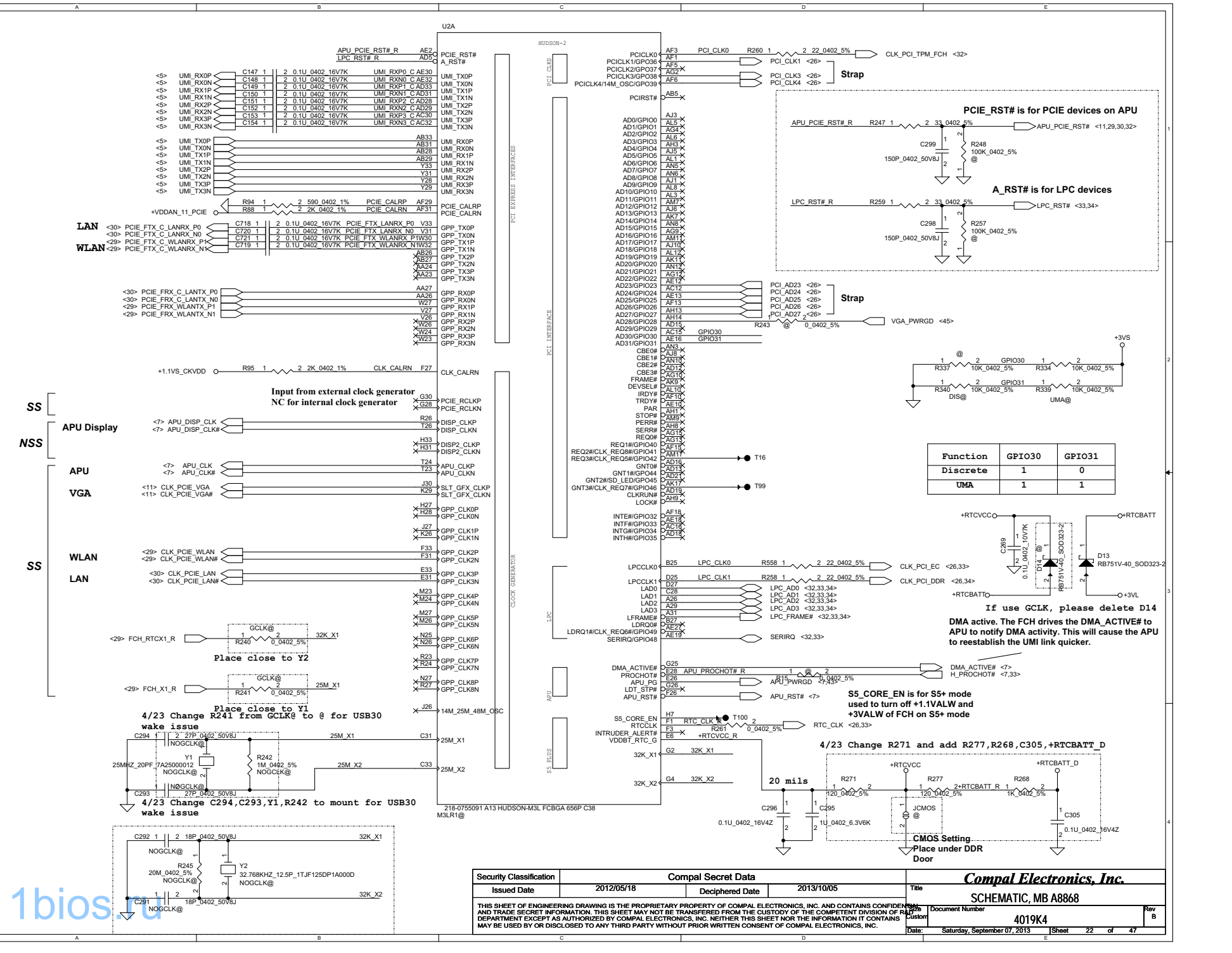


4/23 Add C202 and C216 for EMI request

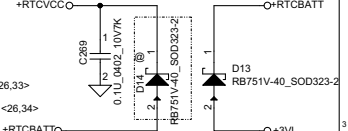
HDMI Connector



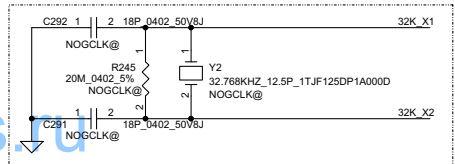
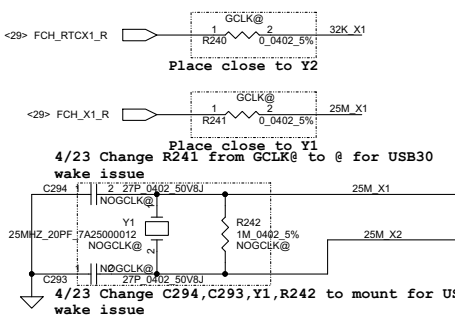
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				Document Number	4019K4
				Date:	Saturday, September 07, 2013
				Sheet	21 of 47



Function	GPIO30	GPIO31
Discrete	1	0
UMA	1	1



If use GCLK, please delete D14 DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

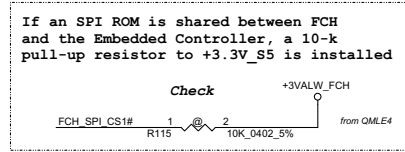


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						Rev B
Date: Saturday, September 07, 2013						Sheet 22 of 47

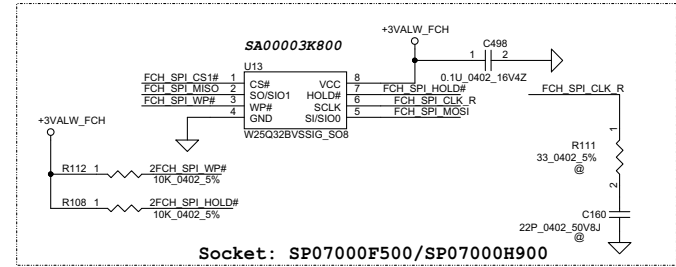
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HDMI_EN# (Internal 8.2K PU)

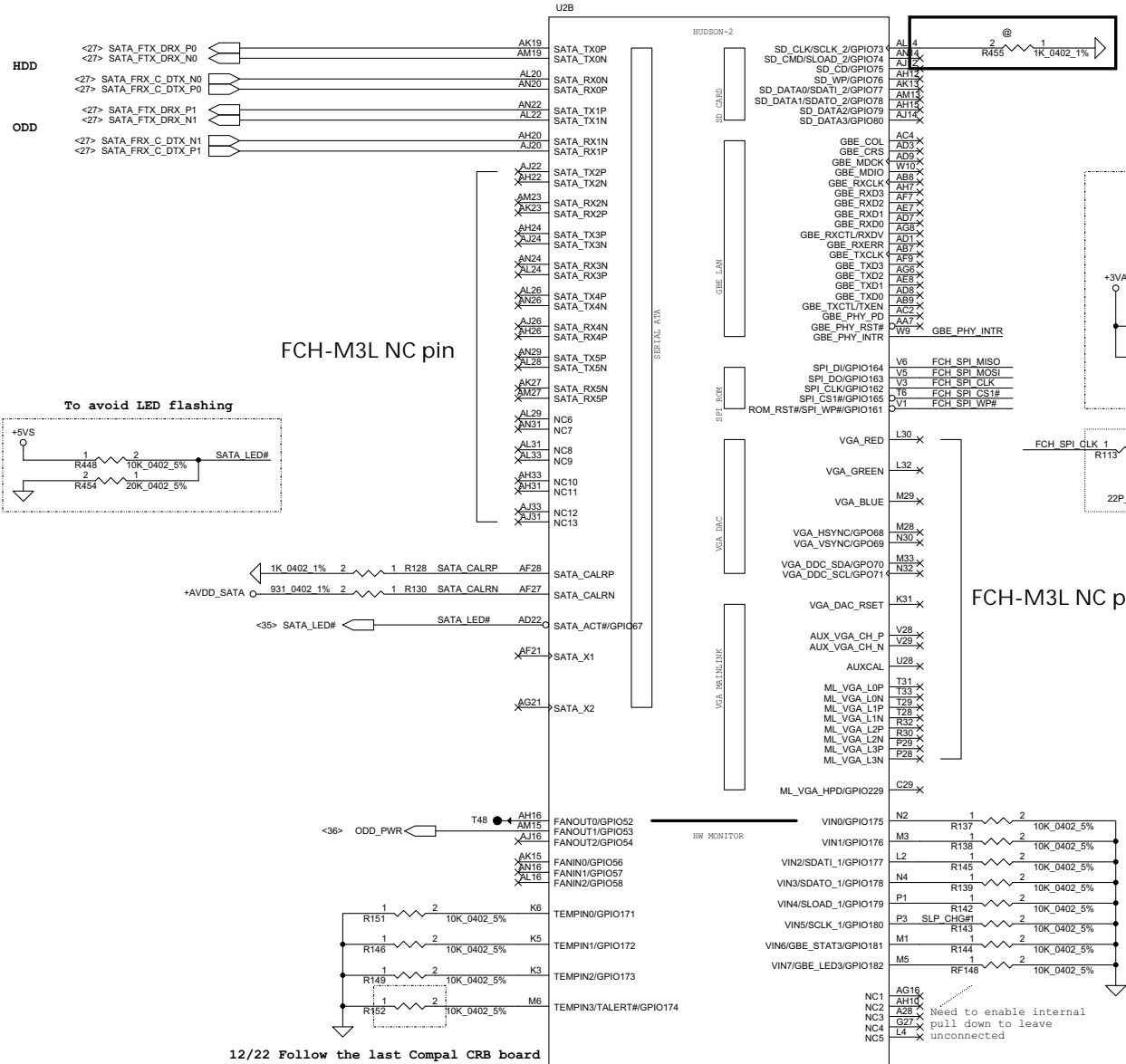
HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU



4MB SPI ROM & Non-shared ROM



5/17 Add R113 and reserve C161 for EMI request



FCH-M3L NC pin

FCH-M3L NC pin

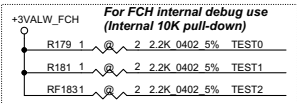
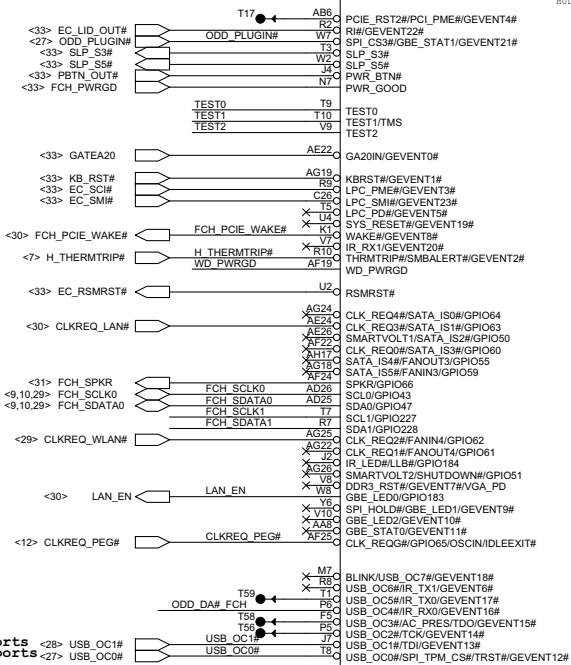
12/22 Follow the last Compal CRB board

218-0755091 A13 HUDSON-M3L FC8GA 656P C38

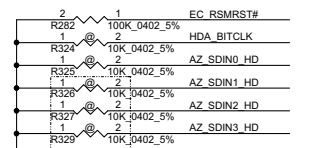
M3LR1@

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Date: Saturday, September 07, 2013				Rev B
Sheet 23 of 47				

PCIE_RST2 : Reset PCIE device on Hudson 3

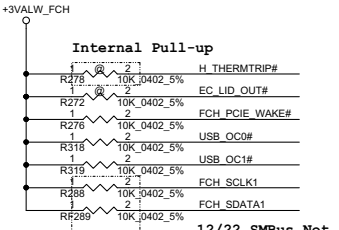


SM Bus 0-->S0 PWR domain==> SO-DIMM, WLAN
SM Bus 1-->S5 PWR domain==> no use

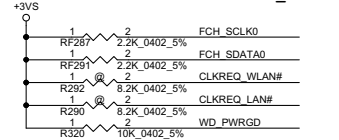


12/22 Reserve R326,R327,R329 but AMD have internal pull down

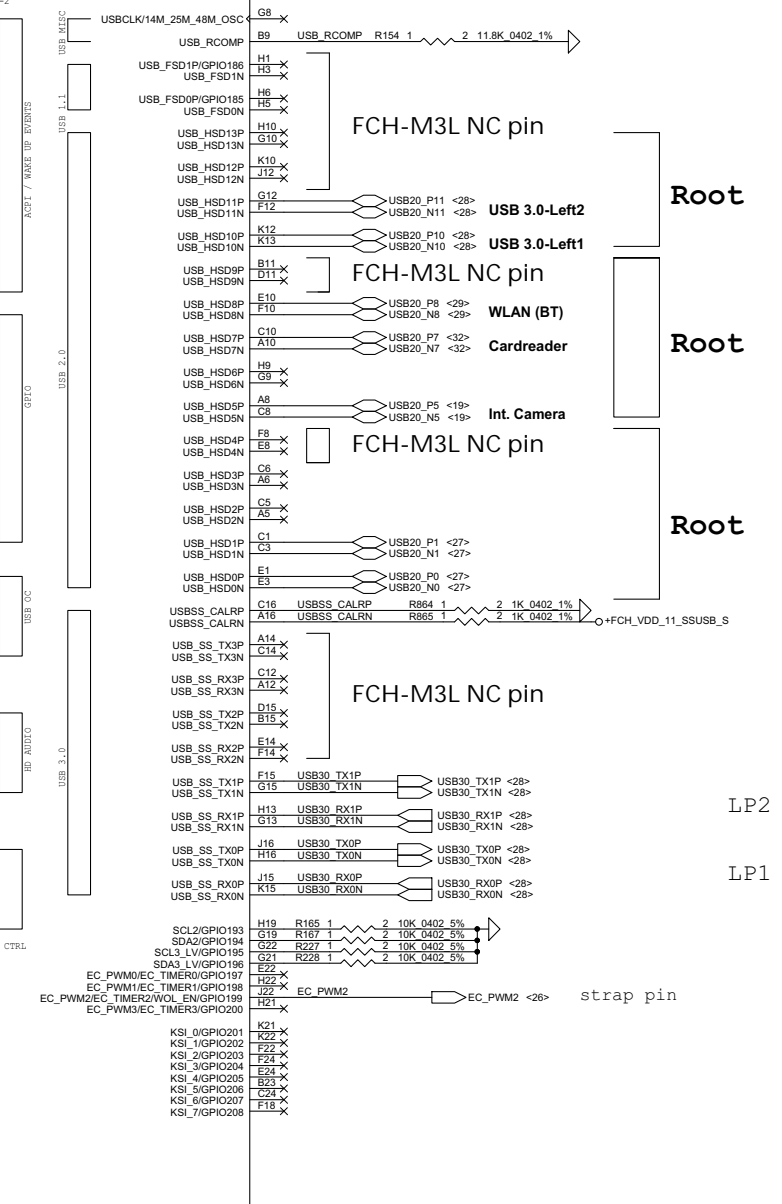
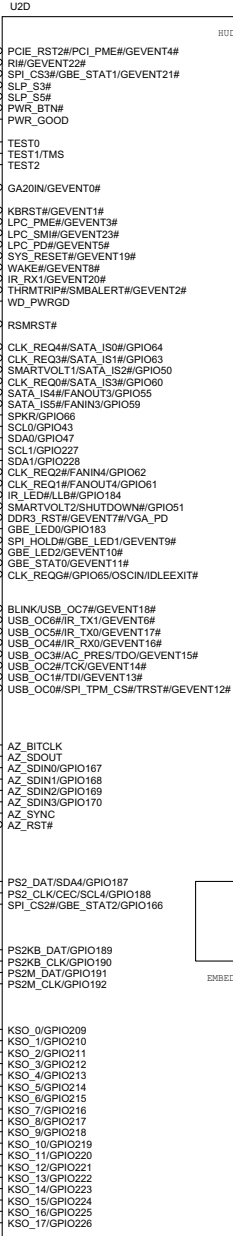
USB_OC1# is for left USB3.0 ports <28> USB_OC#
USB_OC0# is for right USB2.0 ports <27> USB_OC0#



12/22 SMBus Not Implemented use 10k pull up to +3VALW_FCH



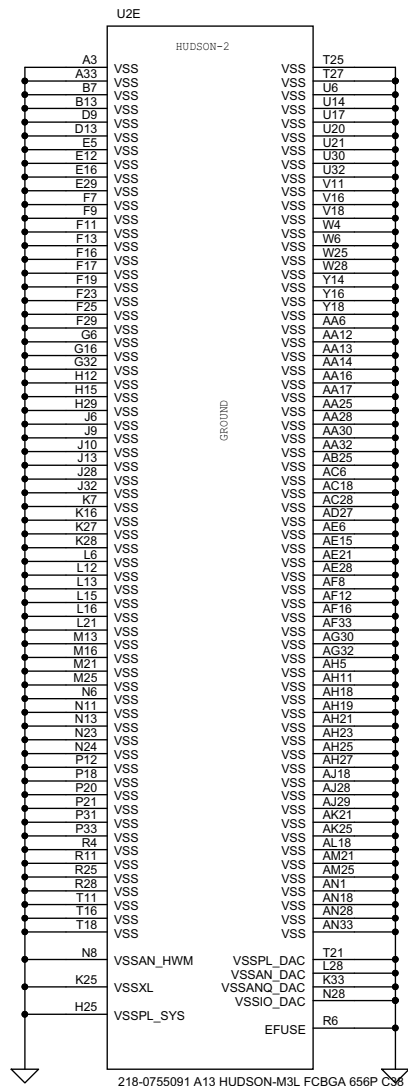
Place R425 and C363 close to FCH for ESD



218-0755091 A13 HUDSON-M3L FCBGA 656P C38

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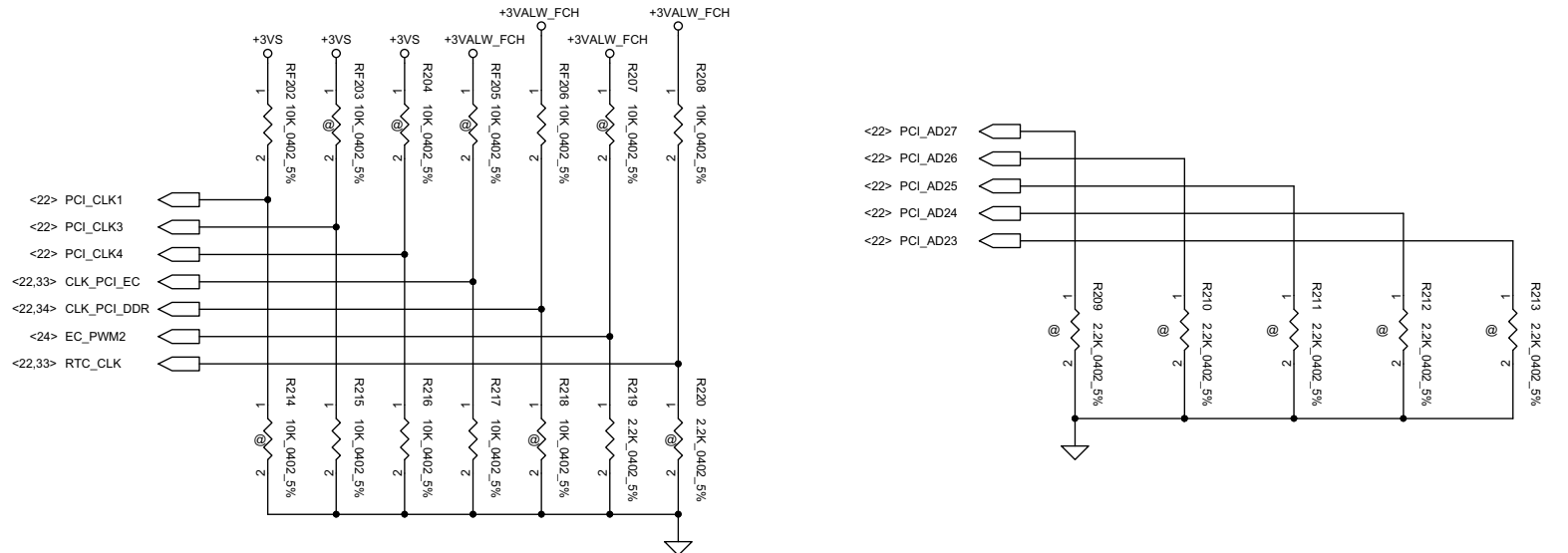
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

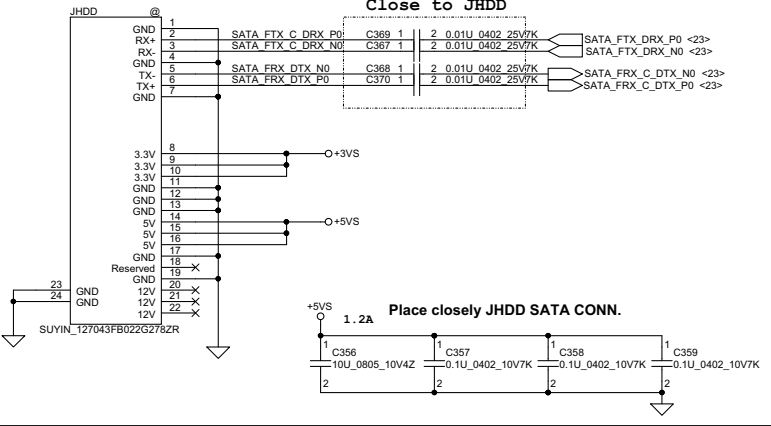


218-0755091 A13 HUDSON-M3L FCBGA 656P C36

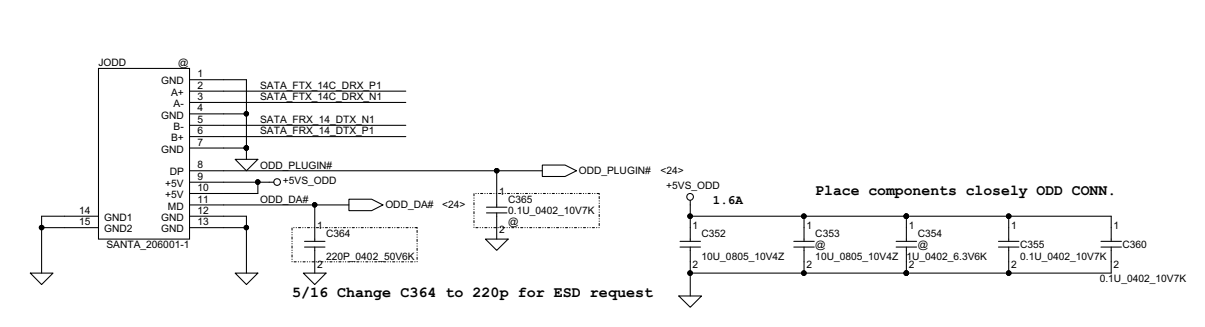
M3LR1@

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Date:	Saturday, September 07, 2013	Sheet	26	of 47

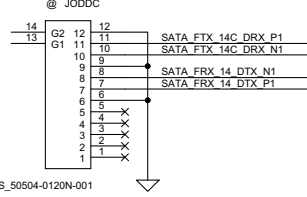
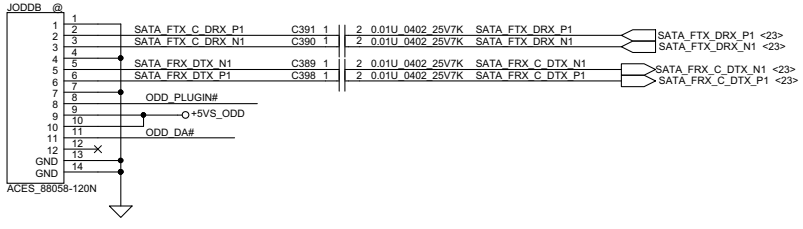
SATA HDD Conn.



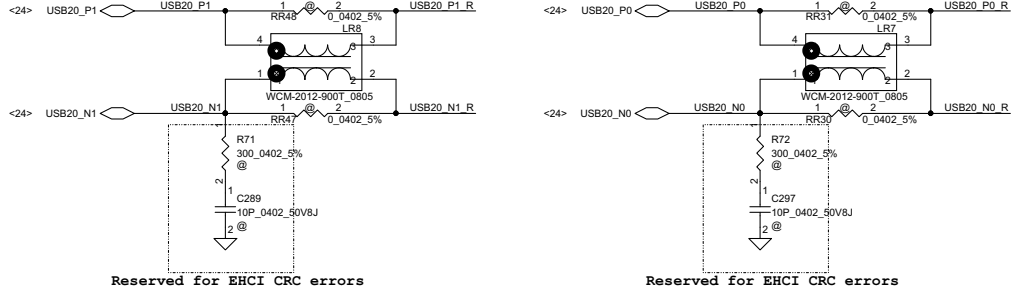
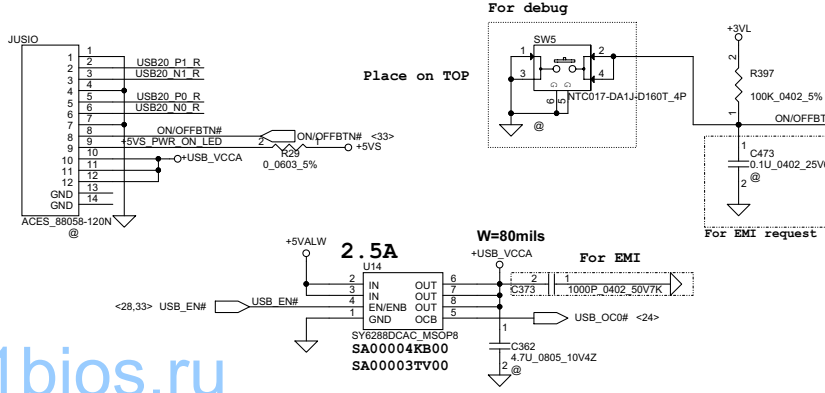
SATA ODD Conn (for 14")



SATA ODD Conn (for 15")

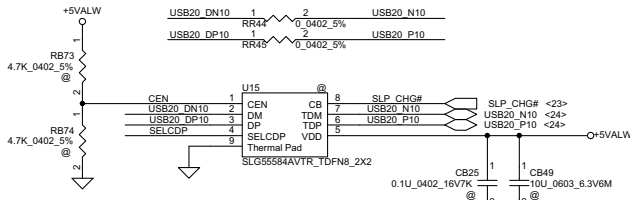


Power Button & RUSB connector

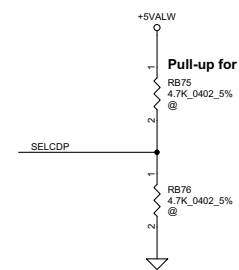


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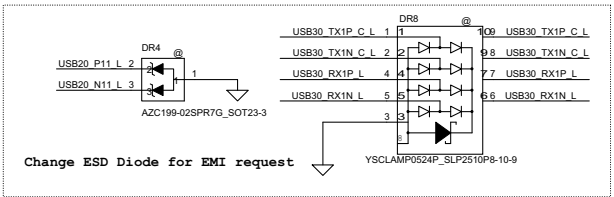
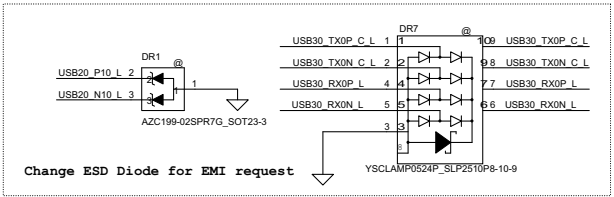
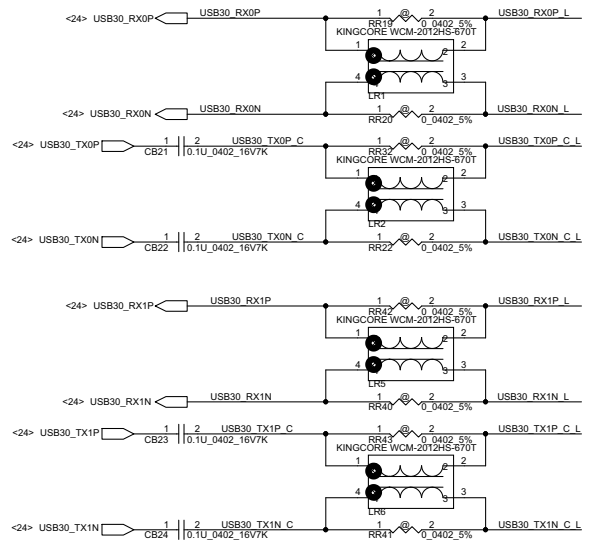
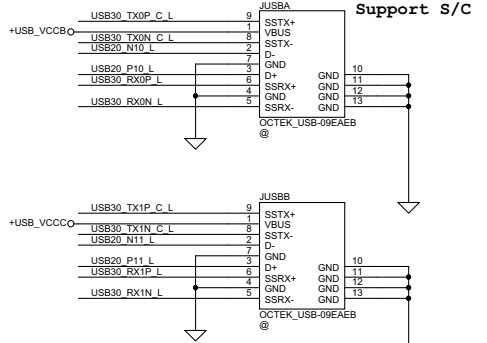
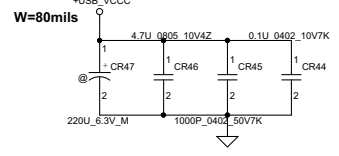
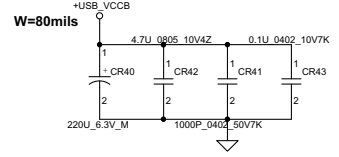
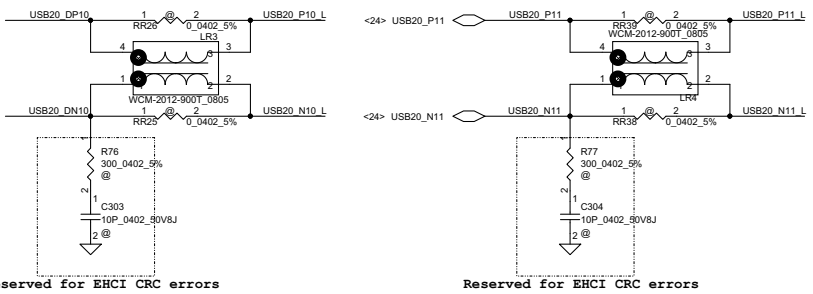
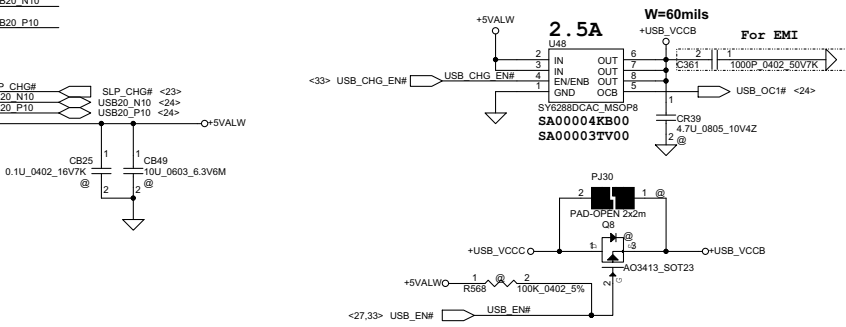
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				4019K4
				Rev B
Date: Saturday, September 07, 2013				Sheet 27 of 47



Pull-up for SLGC55584AV

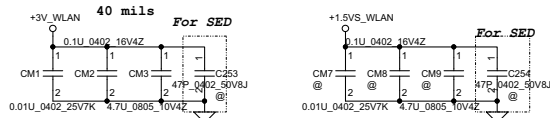


SLP_CHG#	SELCDP	Function
0	X	DCP autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only

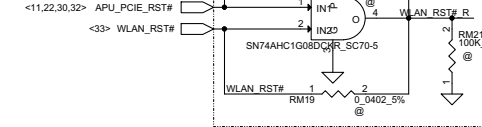


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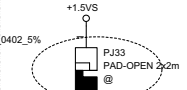
Slot 1 Half PCIe Mini Card-WLAN



Add WLAN_RST# on DVT



4/23 Add RM20 and change UM5, RM21 to @

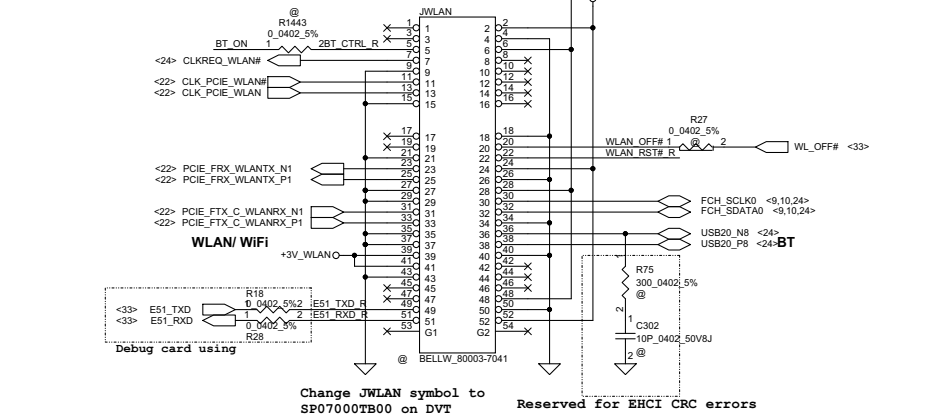


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

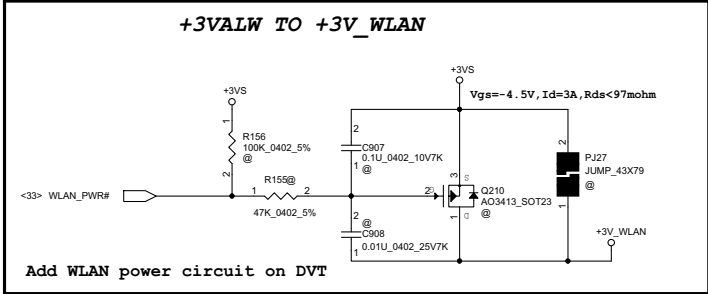
<33> BT_ON E51_RXD R

For isolate BT_CTRL and Compal Debug Card.



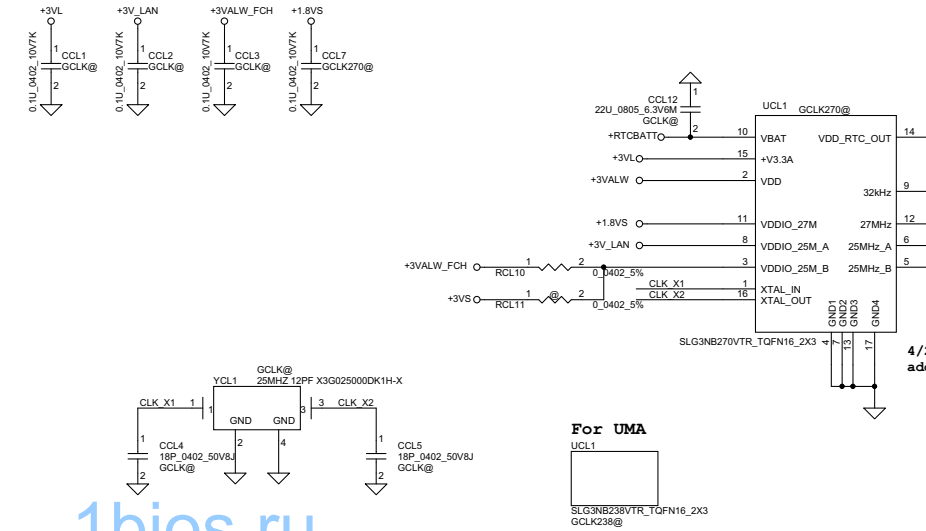
Change JWLAN symbol to SP07000TB00 on DVT

Reserved for EHCI CRC errors



4/23 Change R156, R155, C907, C908, Q210 to @

Green Clock Generator

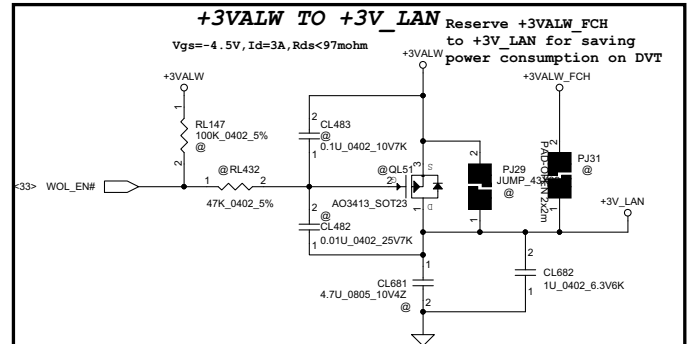
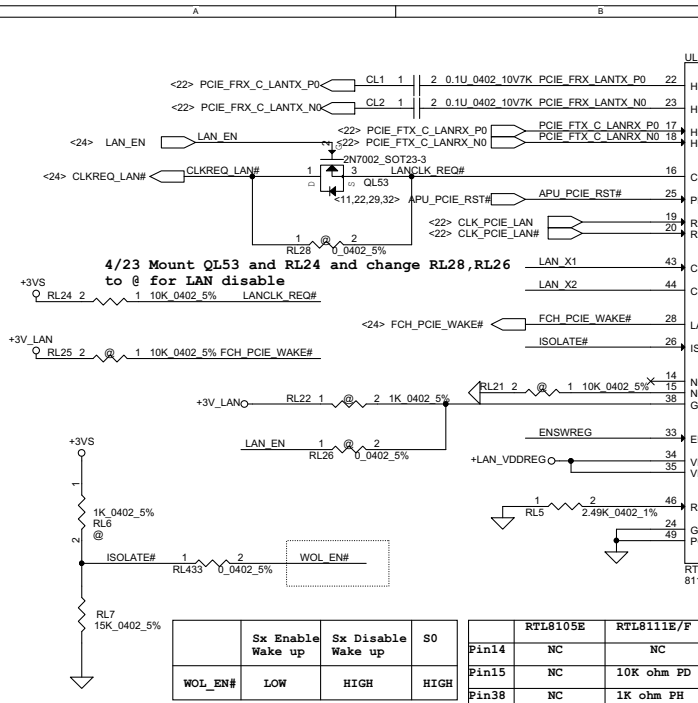


4/23 Change UCL1.2 to +3VALW, UCL1.14 to +RTVCVCC_D and add RCL10, RCL11 for USB30 wake issue

Reserved for Swing Level adjustment (Close GCLK side)

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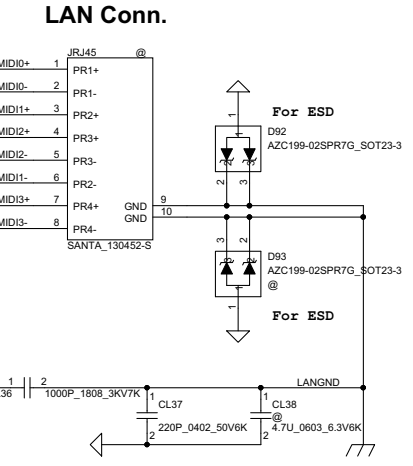
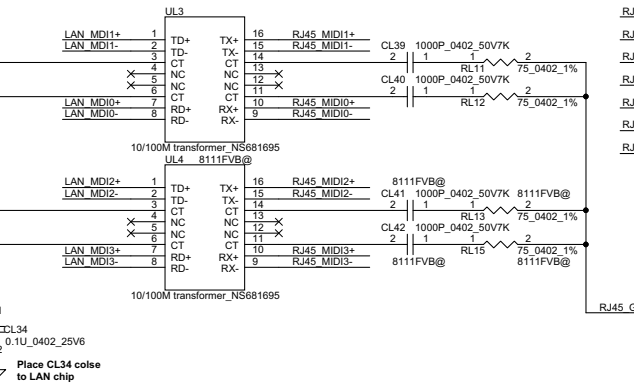
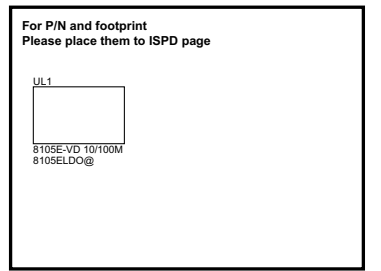
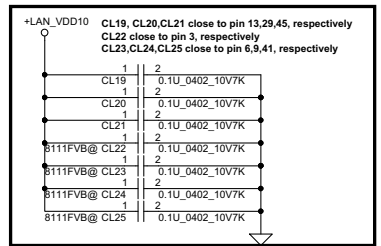
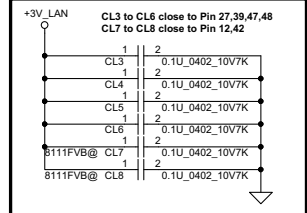
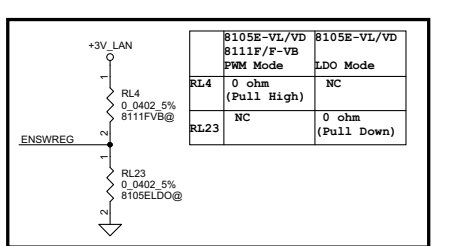
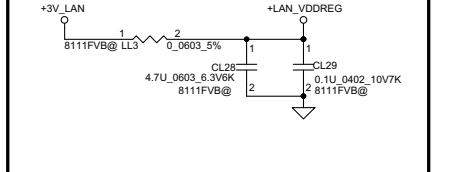
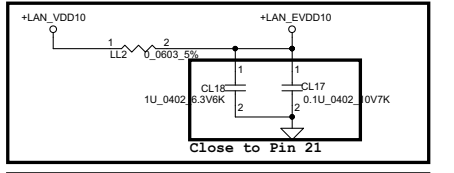
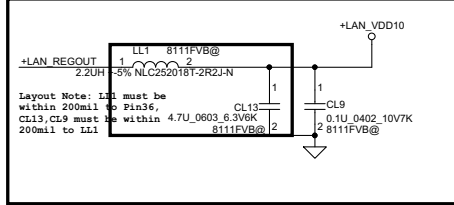
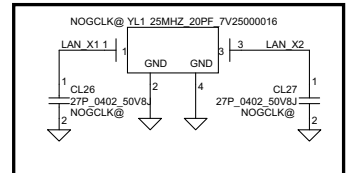
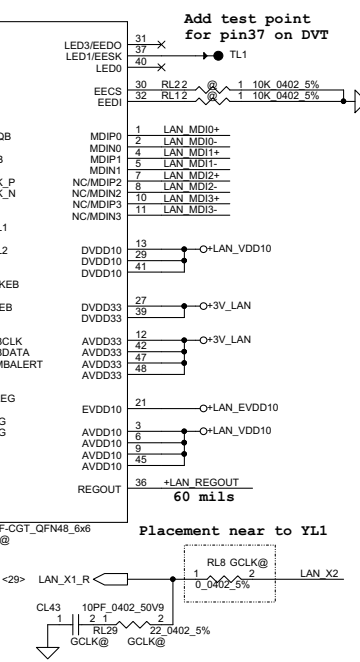
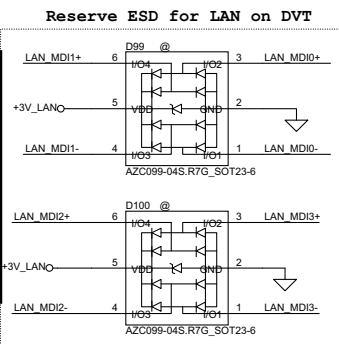
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Size	Document Number	Rev	B	
	4019K4			
Date:	Saturday, September 07, 2013	Sheet	29	of 47



+3V_LAN rising time (10%~90%) need > 1ms and < 100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



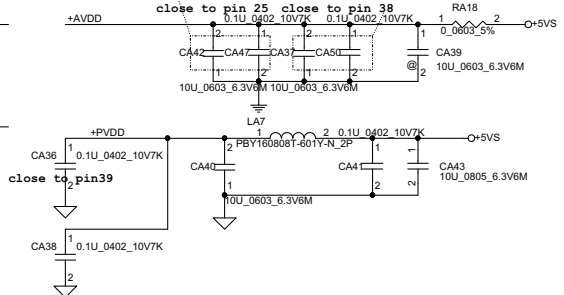
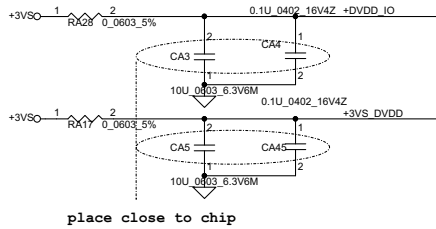
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Document Number	4019K4
Date:	Saturday, September 07, 2013
Sheet	30 of 47

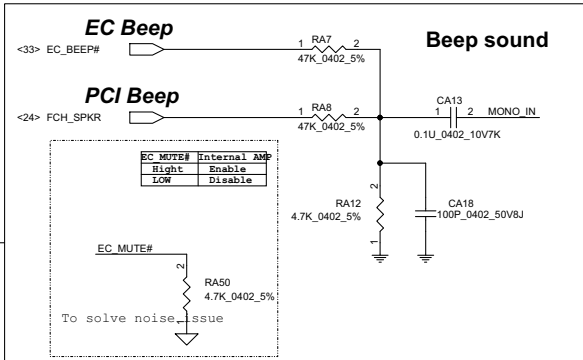
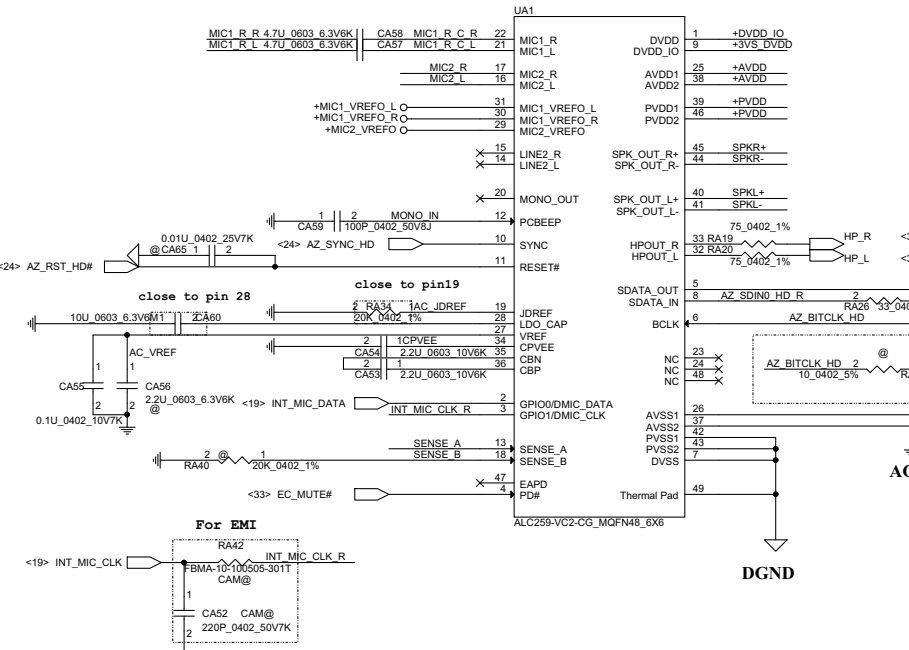
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35mA for 3.3V level

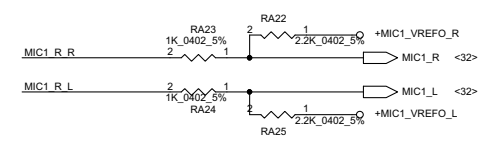


place close to chip

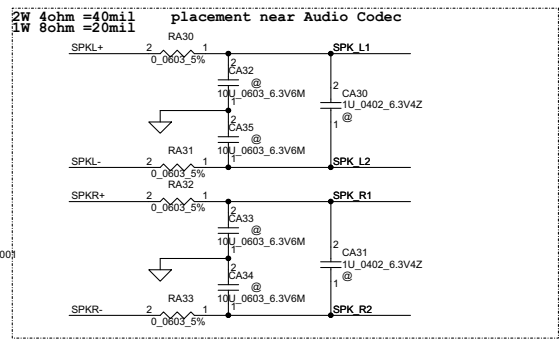
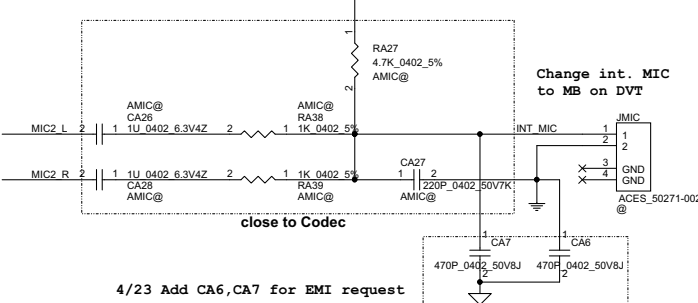
For EMI please place near codec



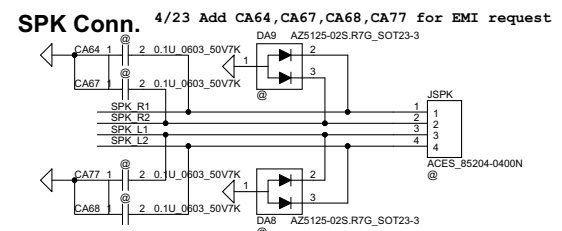
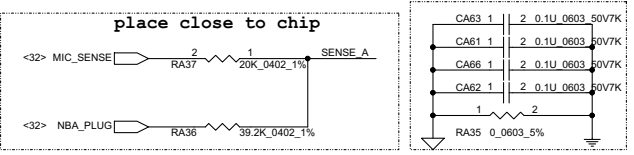
Ext.MIC/LINE IN JACK



Analog MIC

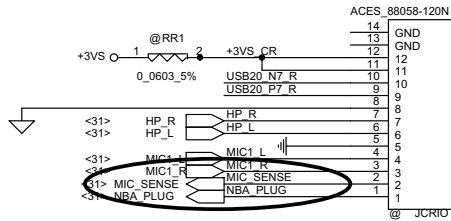


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	

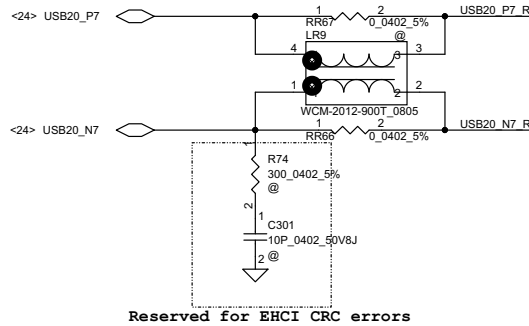


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Date:	Saturday, September 07, 2013	Sheet	31	of 47

CardReader Conn.

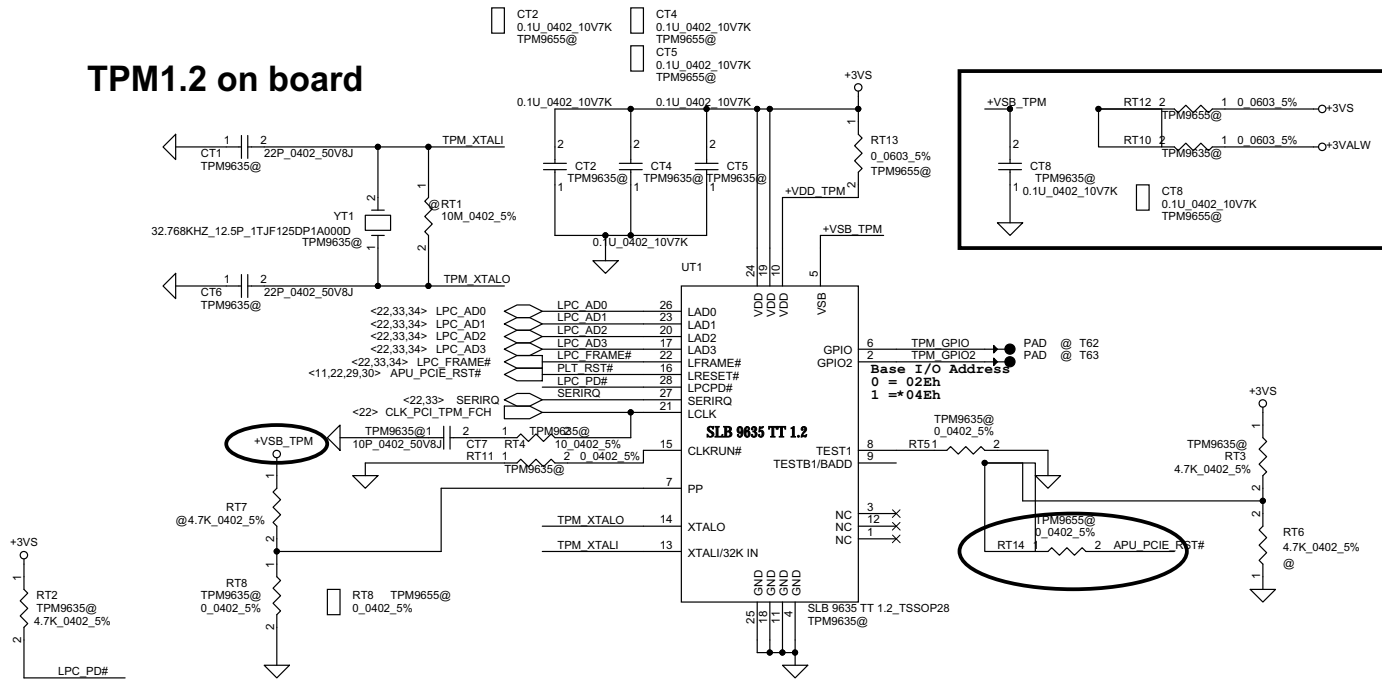


Update JCRI0 pin definition on DVT



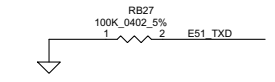
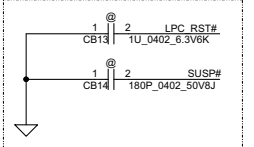
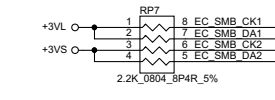
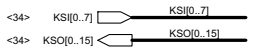
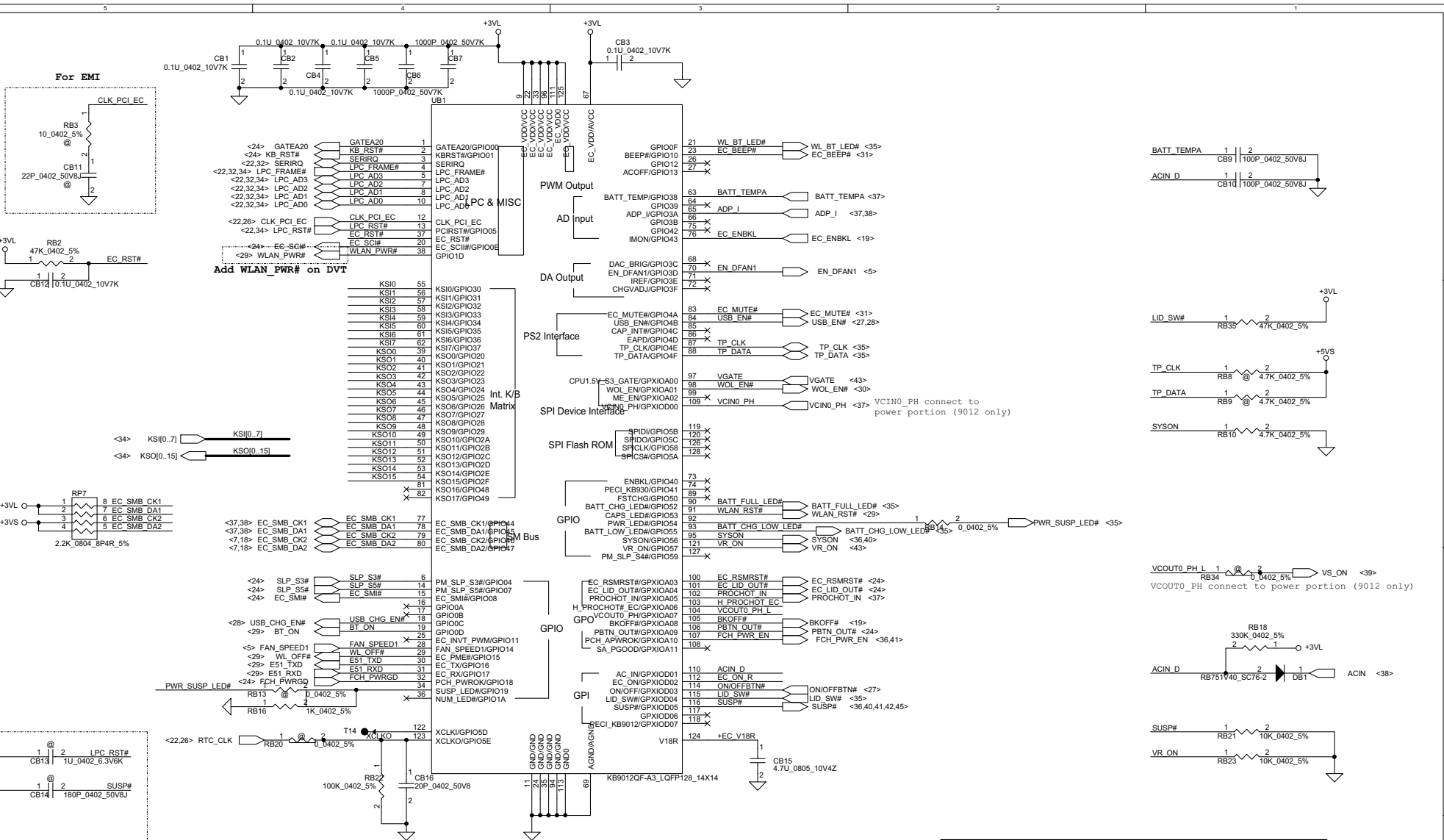
Reserved for EHCI CRC errors

TPM1.2 on board



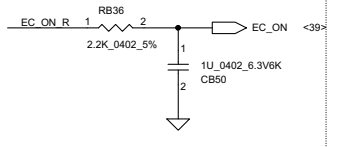
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				4019K4	B
Date: Saturday, September 07, 2013				Sheet	32 of 47

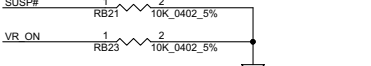
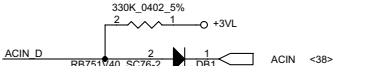
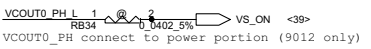
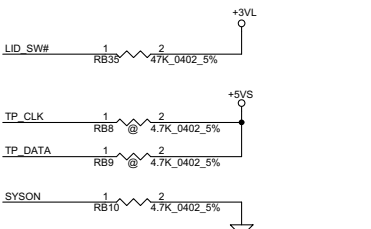
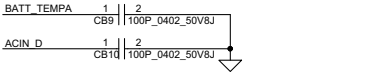
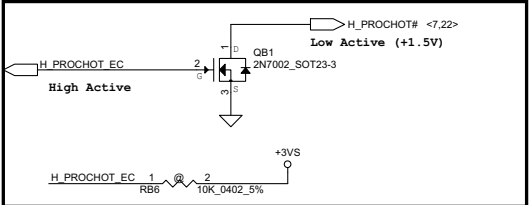


Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



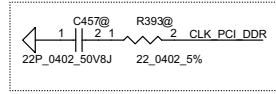
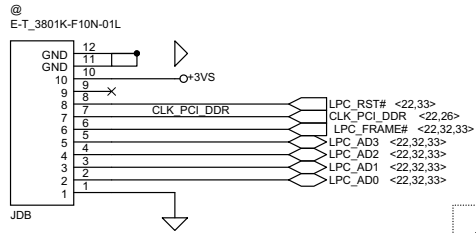
For KB9012 EC_ON low pulse work around



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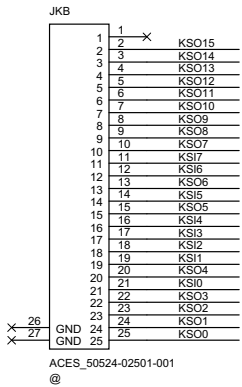
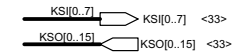
LPC Debug Port

Place the PAD under DDR DIMM.



For EMI

KEYBOARD CONN.



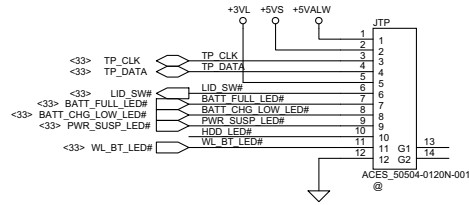
For EMI

Close to JKB

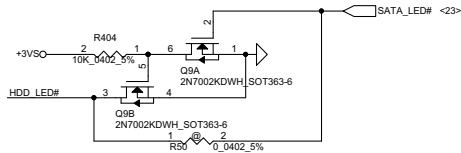
Signal	Pin 1	Pin 2
KSO2	C404	100P_0402_50V8J
KSO1	C405	100P_0402_50V8J
KSO0	C406	100P_0402_50V8J
KSO4	C407	100P_0402_50V8J
KSO3	C408	100P_0402_50V8J
KSO5	C409	100P_0402_50V8J
KSO14	C410	100P_0402_50V8J
KSO6	C411	100P_0402_50V8J
KSO7	C412	100P_0402_50V8J
KSO13	C413	100P_0402_50V8J
KSO8	C415	100P_0402_50V8J
KSO9	C416	100P_0402_50V8J
KSO10	C417	100P_0402_50V8J
KSO11	C418	100P_0402_50V8J
KSO12	C419	100P_0402_50V8J
KSO15	C420	100P_0402_50V8J
KSI7	C421	100P_0402_50V8J
KSI2	C422	100P_0402_50V8J
KSI3	C423	100P_0402_50V8J
KSI4	C424	100P_0402_50V8J
KSI0	C425	100P_0402_50V8J
KSI5	C427	100P_0402_50V8J
KSI6	C429	100P_0402_50V8J
KSI1	C431	100P_0402_50V8J

Touchpad Connector

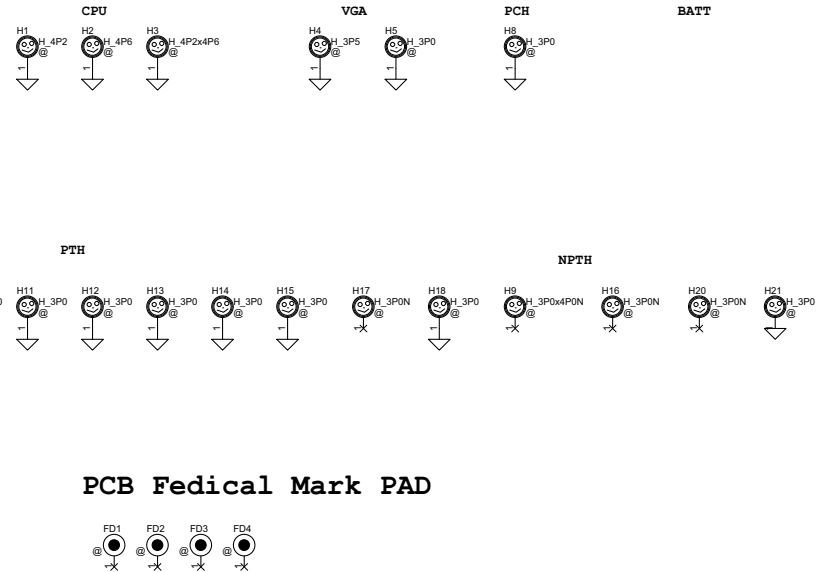
(Reserve 7 pins for LED & Win8 TP)



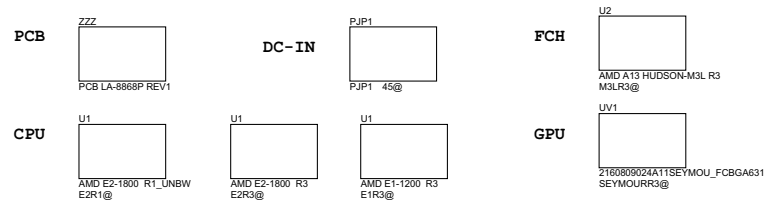
HDD LED



Screw Hole

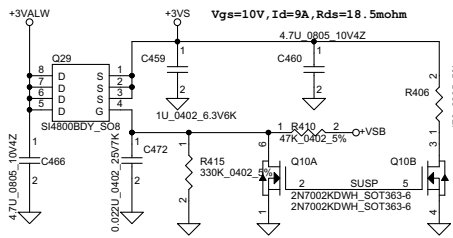


ISPD

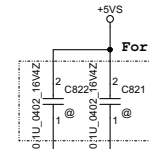
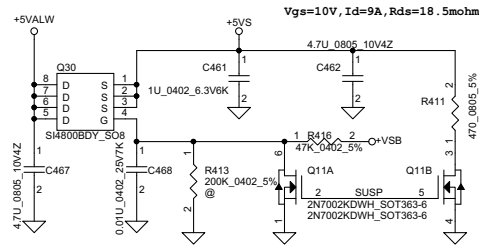


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Size	Document Number	Date	Sheet	Rev
	4019K4	Saturday, September 07, 2013	35 of 47	B

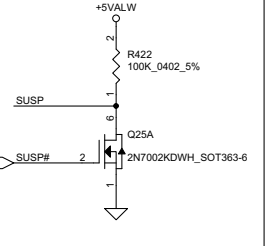
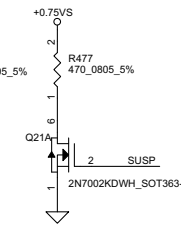
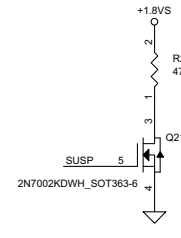
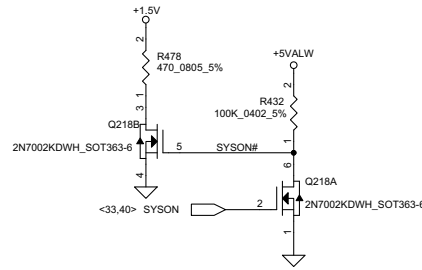
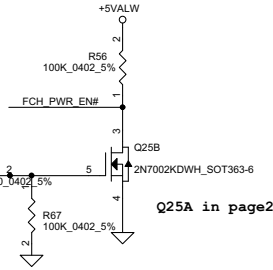
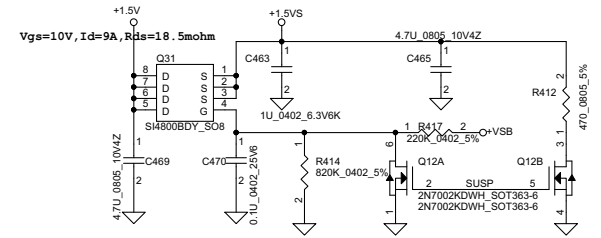
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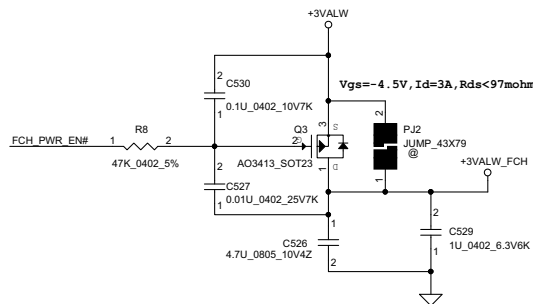
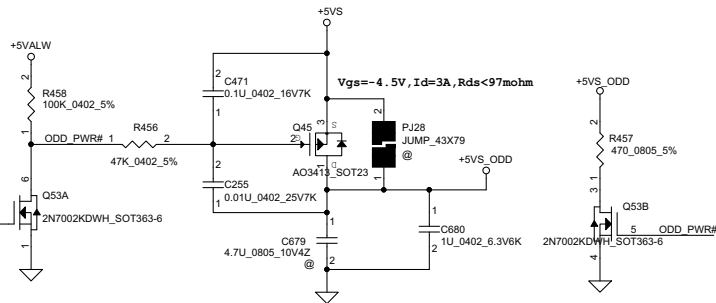
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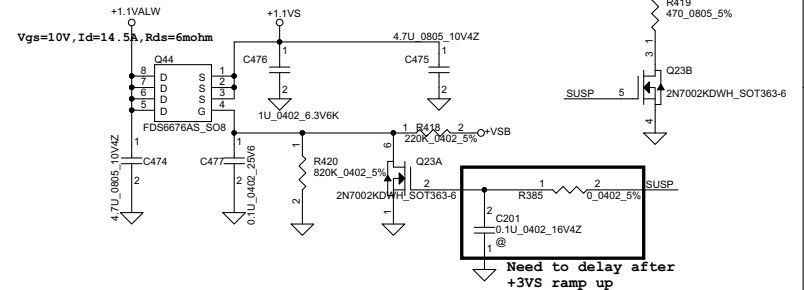
+1.5V to +1.5VS



+5VS TO +5VS_ODD

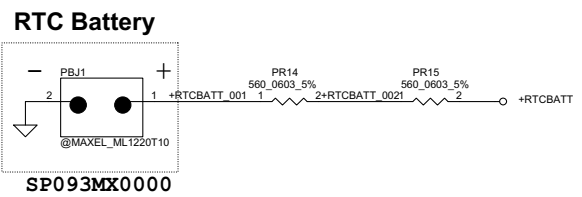
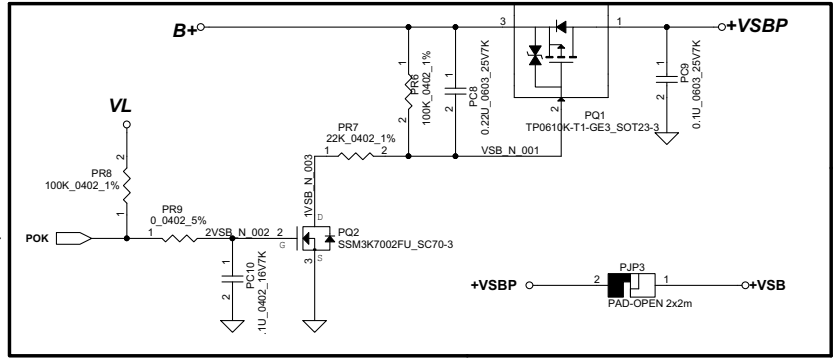
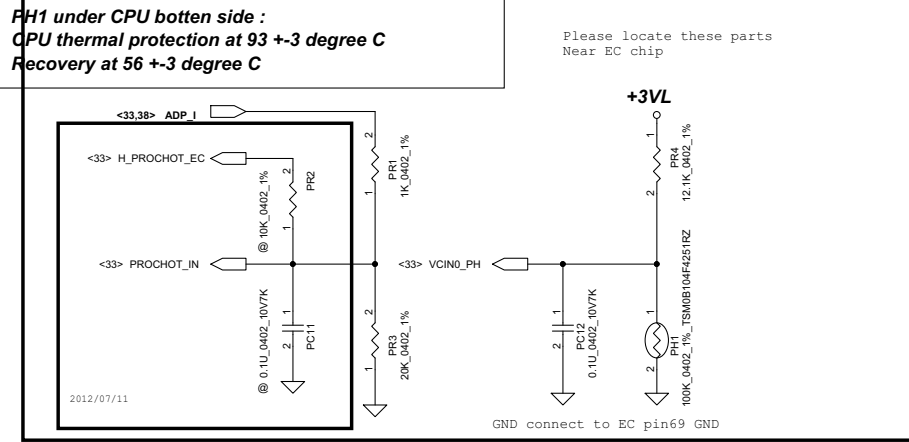
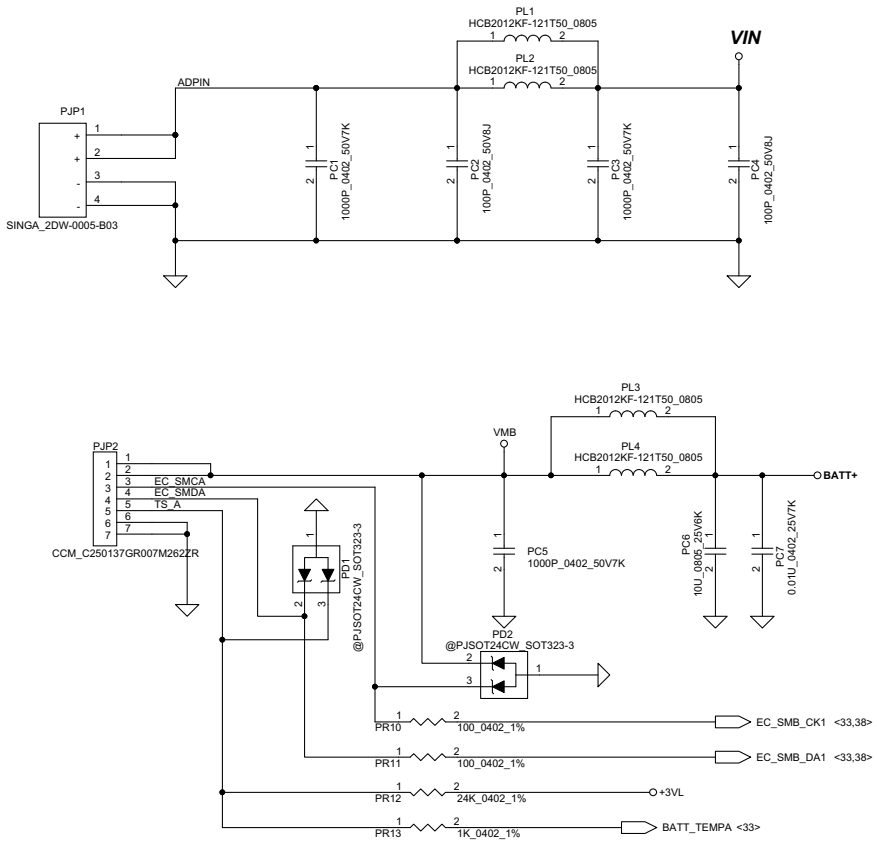


+1.1VALW to +1.1VS



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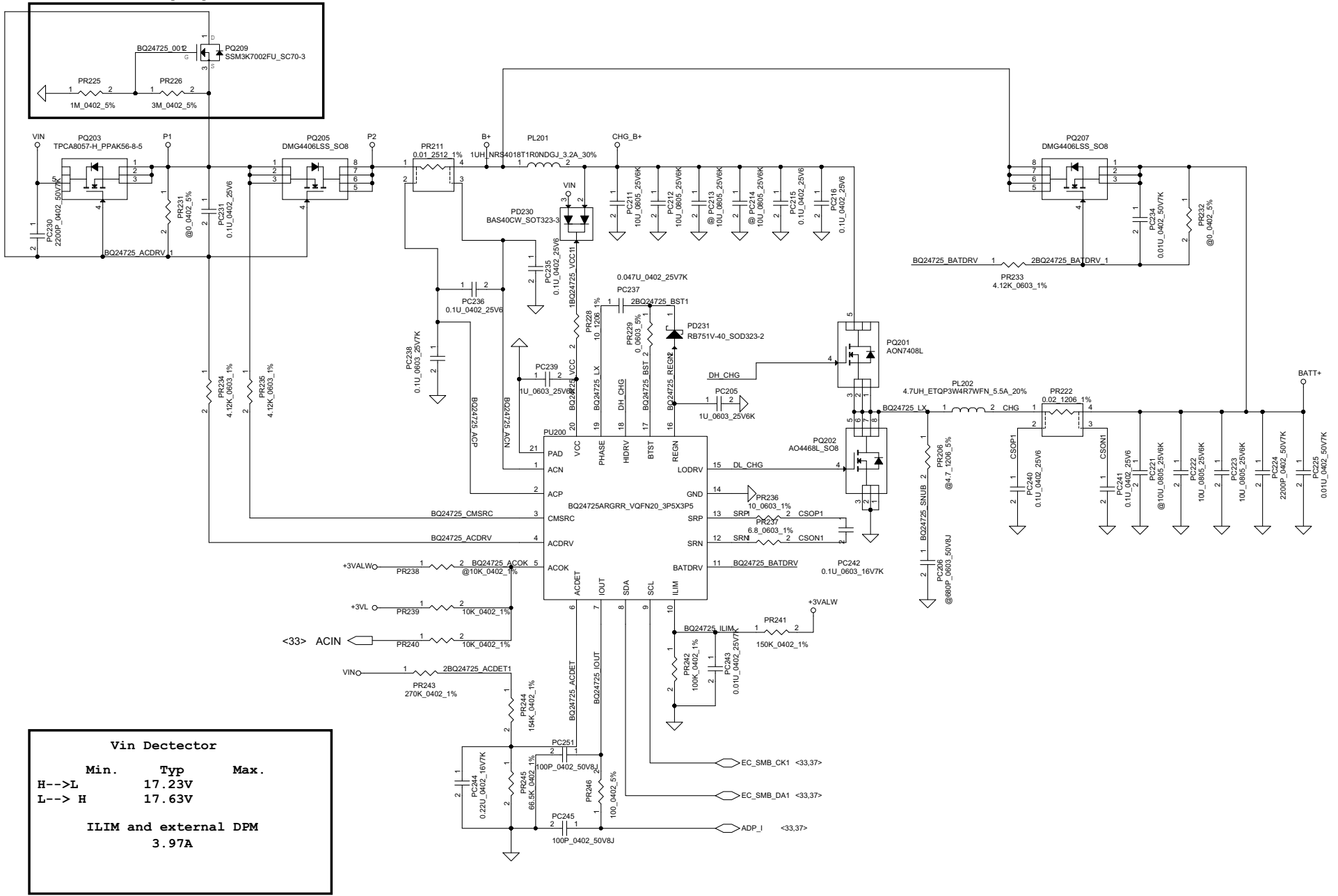
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Date:	Saturday, September 07, 2013	Sheet	36	of	47



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				SAMSUNG
Date: Saturday, September 07, 2013				Sheet 37 of 47

for reverse input protection



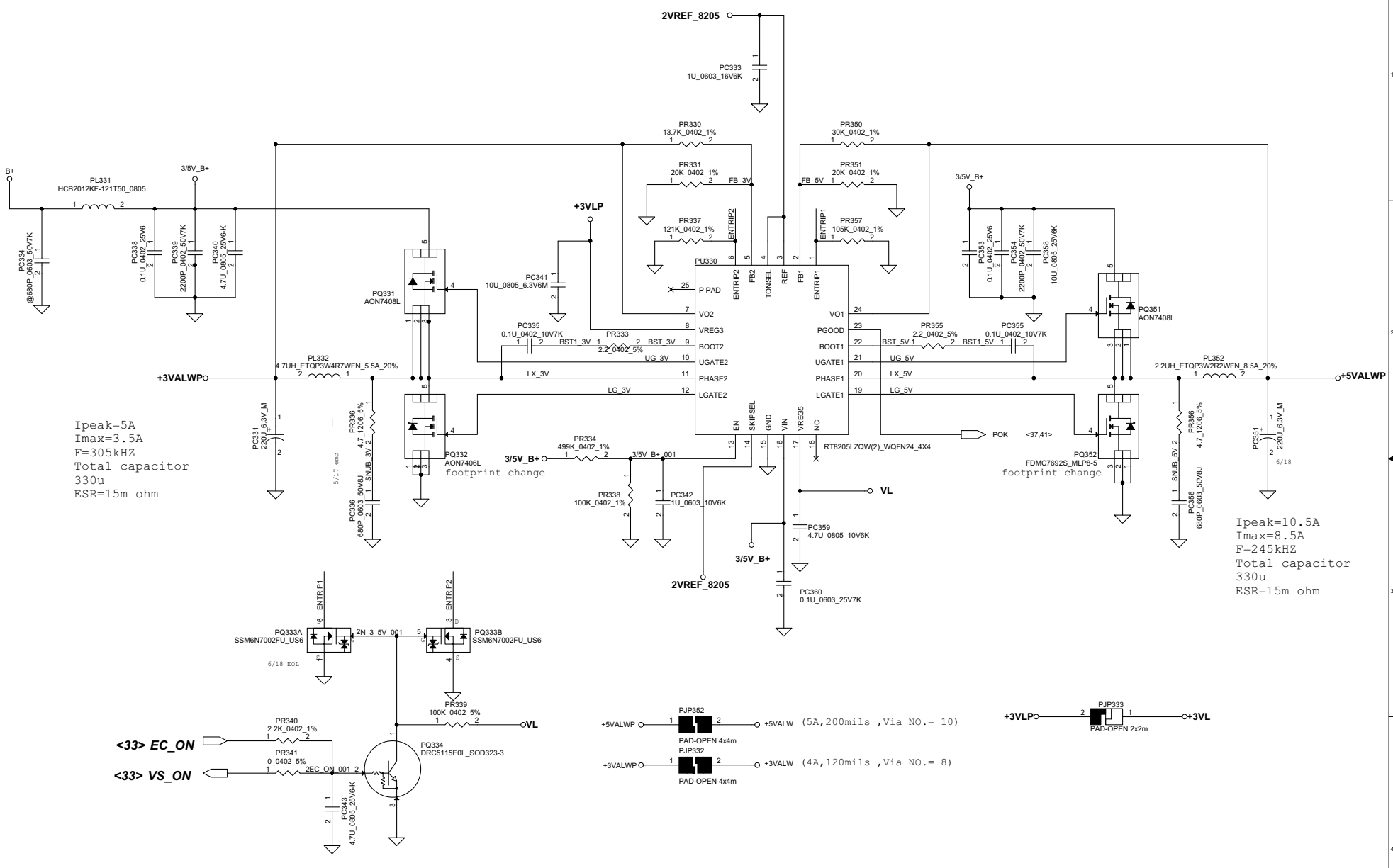
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				SAMSUNG
				Rev B
Date:	Saturday, September 07, 2013	Sheet	38	of 47

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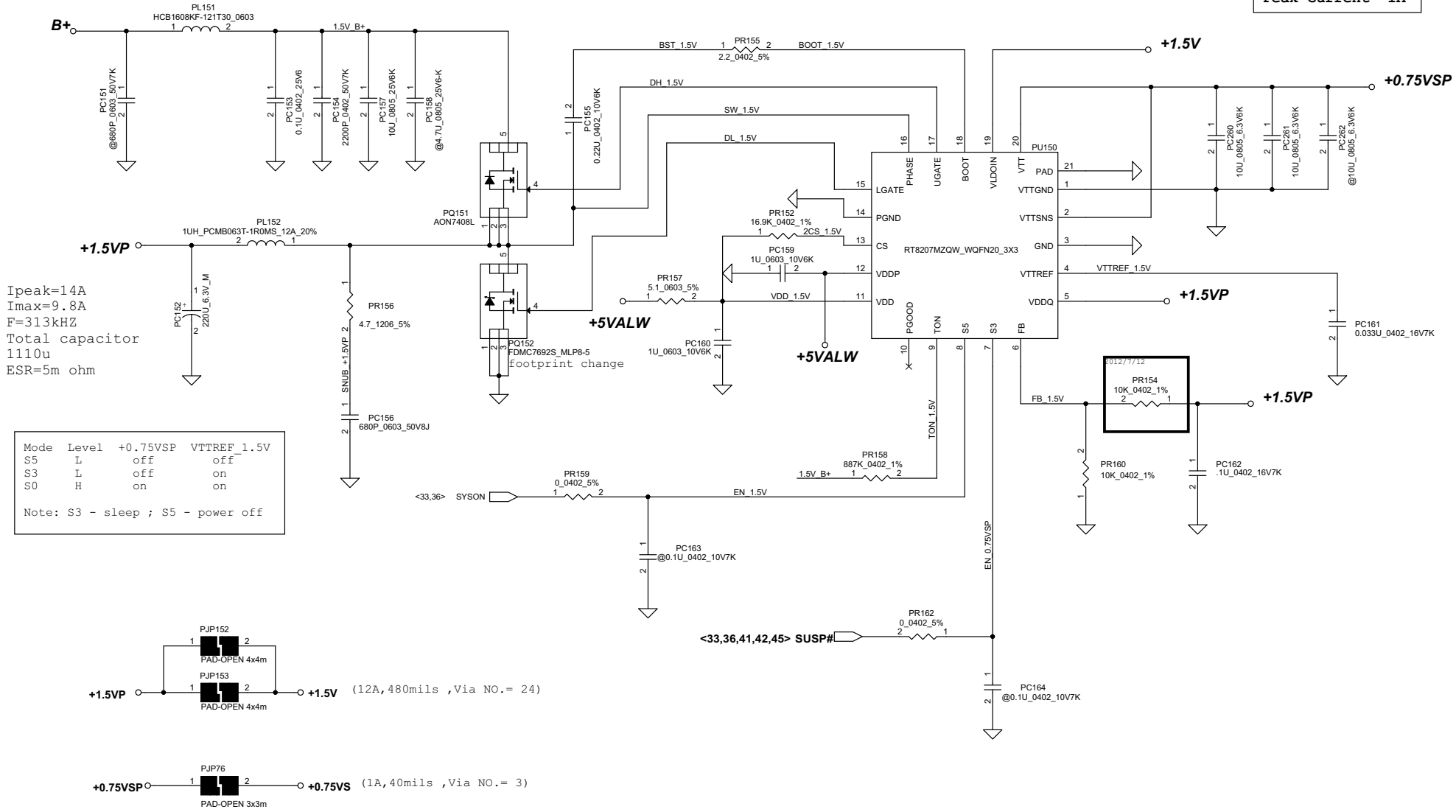
I_{peak}=5A
 I_{max}=3.5A
 F=305kHz
 Total capacitor
 330u
 ESR=15m ohm

I_{peak}=10.5A
 I_{max}=8.5A
 F=245kHz
 Total capacitor
 330u
 ESR=15m ohm



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Doc No	4019K4	Doc Name	4019K4	Rev	B
Date	Saturday, September 07, 2013	Sheet	39	of 47	

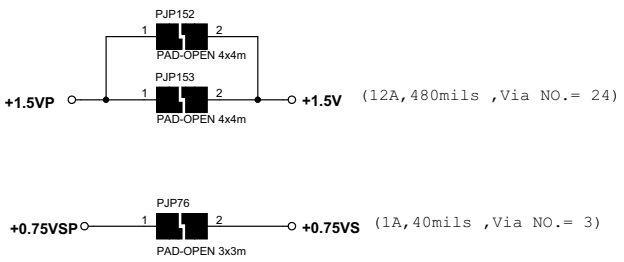
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Ipeak=14A
Imax=9.8A
F=313kHz
Total capacitor
1110u
ESR=5m ohm

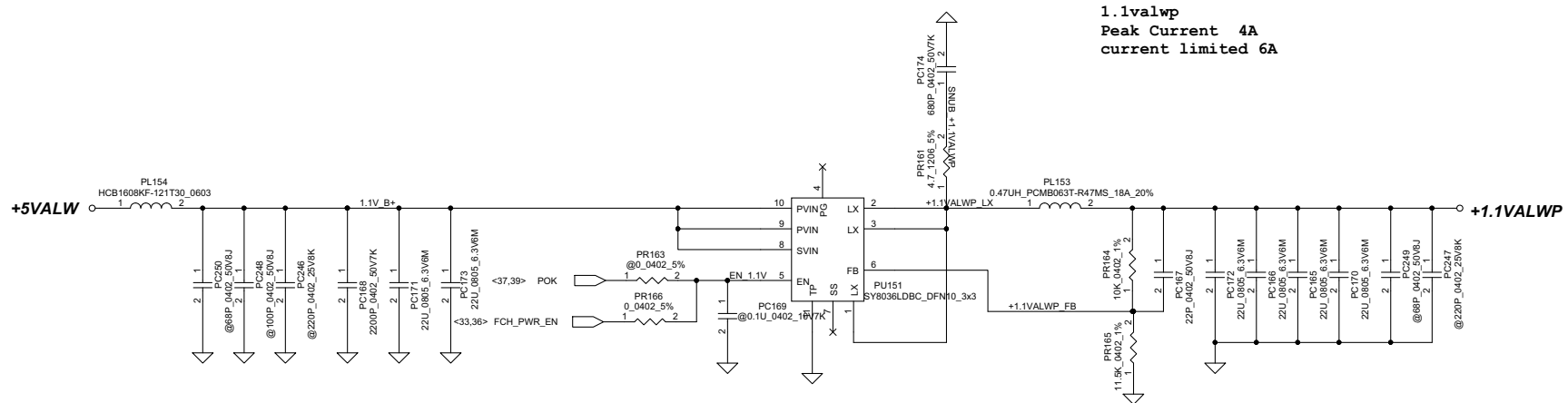
Mode	Level	+0.75VSP	VTTREF 1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

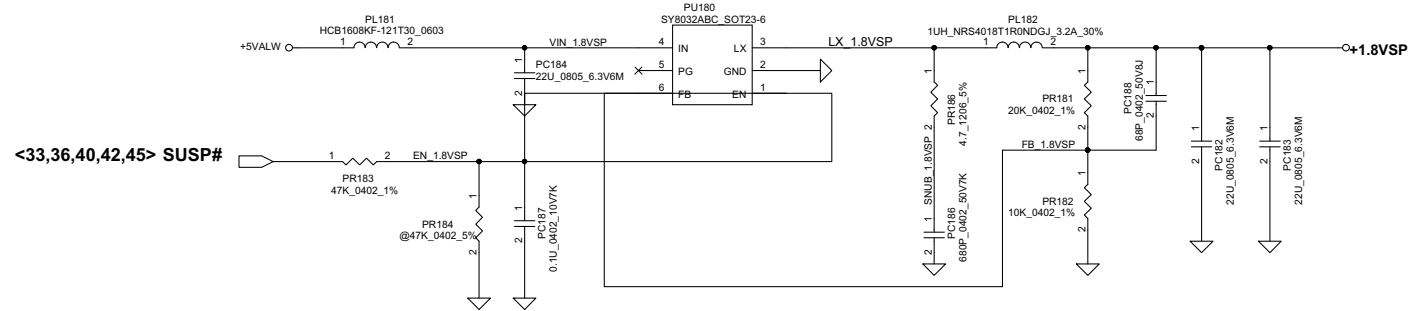
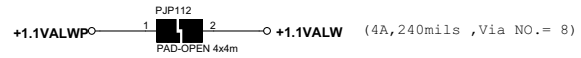


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Date:	Saturday, September 07, 2013	Sheet	40 of 47	Rev B

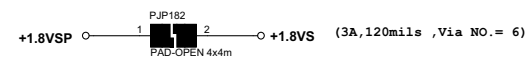
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1.1valwp
Peak Current 4A
current limited 6A

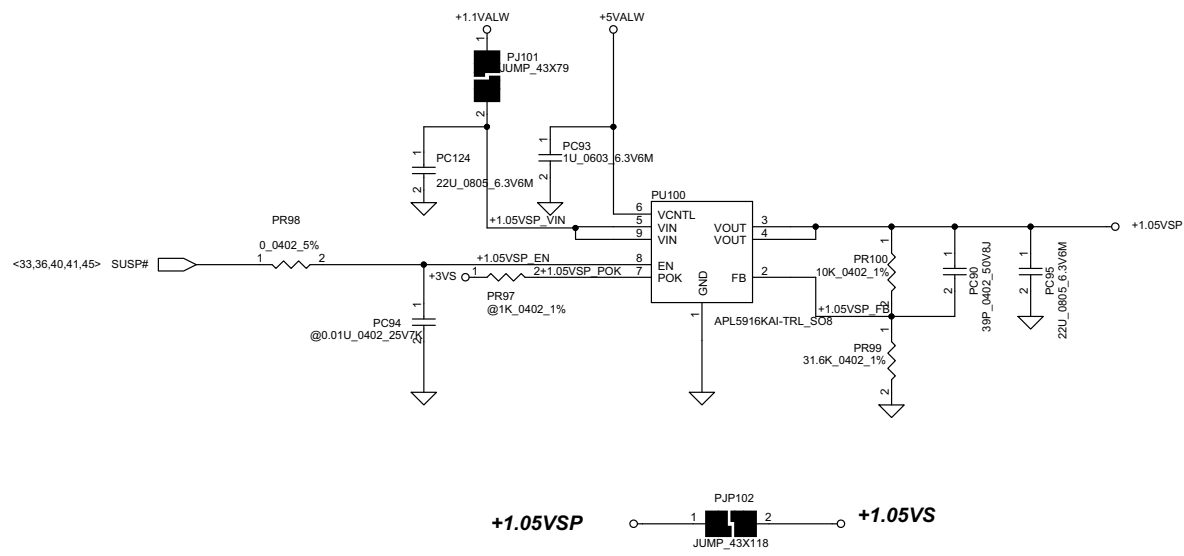


<33,36,40,42,45> SUSP#



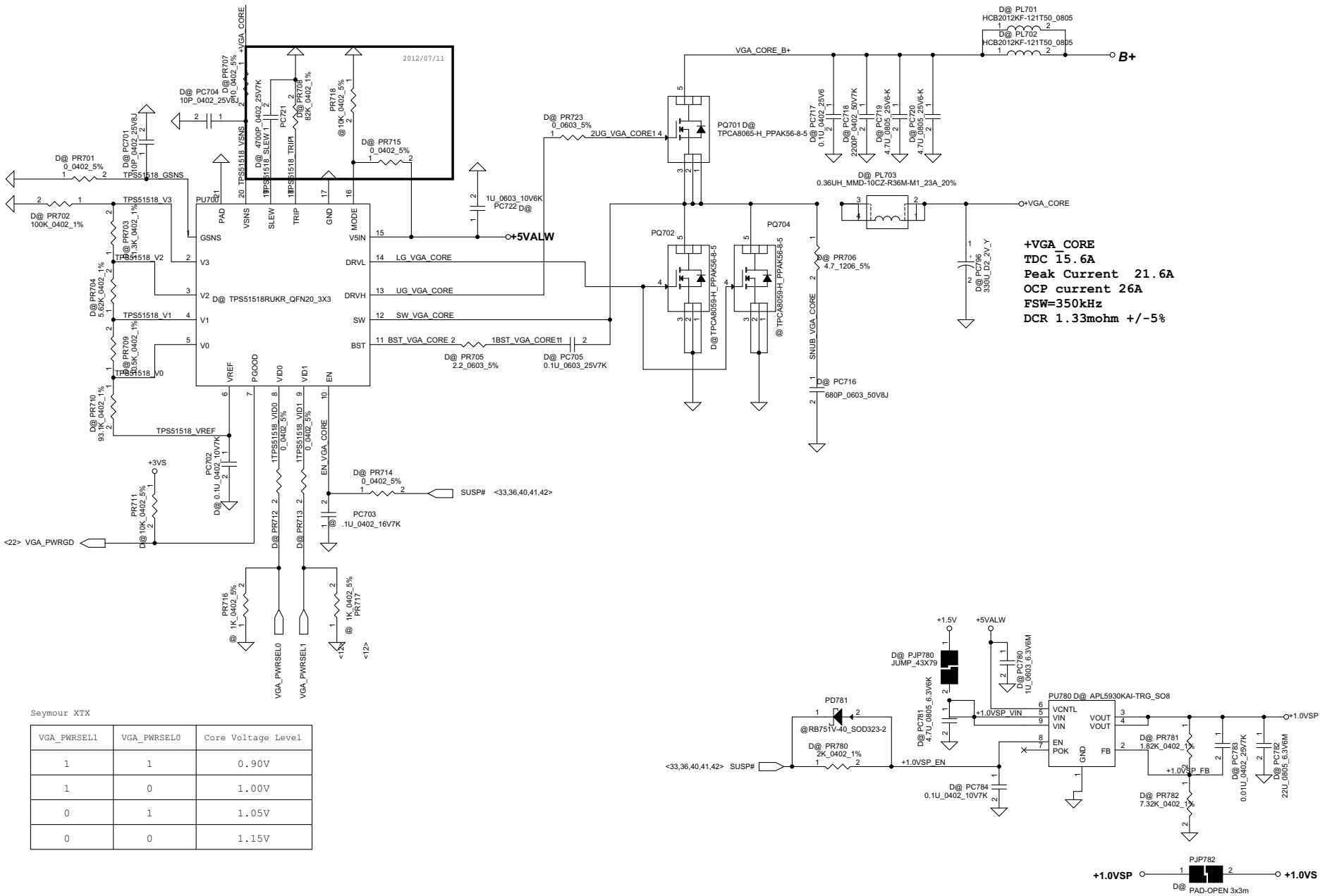
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Date:	Saturday, September 07, 2013	Sheet	41	of	47



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Size	Document Number	LA-8712P	Rev	B	
Date:	Saturday, September 07, 2013	Sheet	42	of	47



Seymour XTx

VGA_PWRSEL1	VGA_PWRSEL0	Core Voltage Level
1	1	0.90V
1	0	1.00V
0	1	1.05V
0	0	1.15V

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				4019K4	
Date:				Saturday, September 07, 2013	Sheet 45 of 47