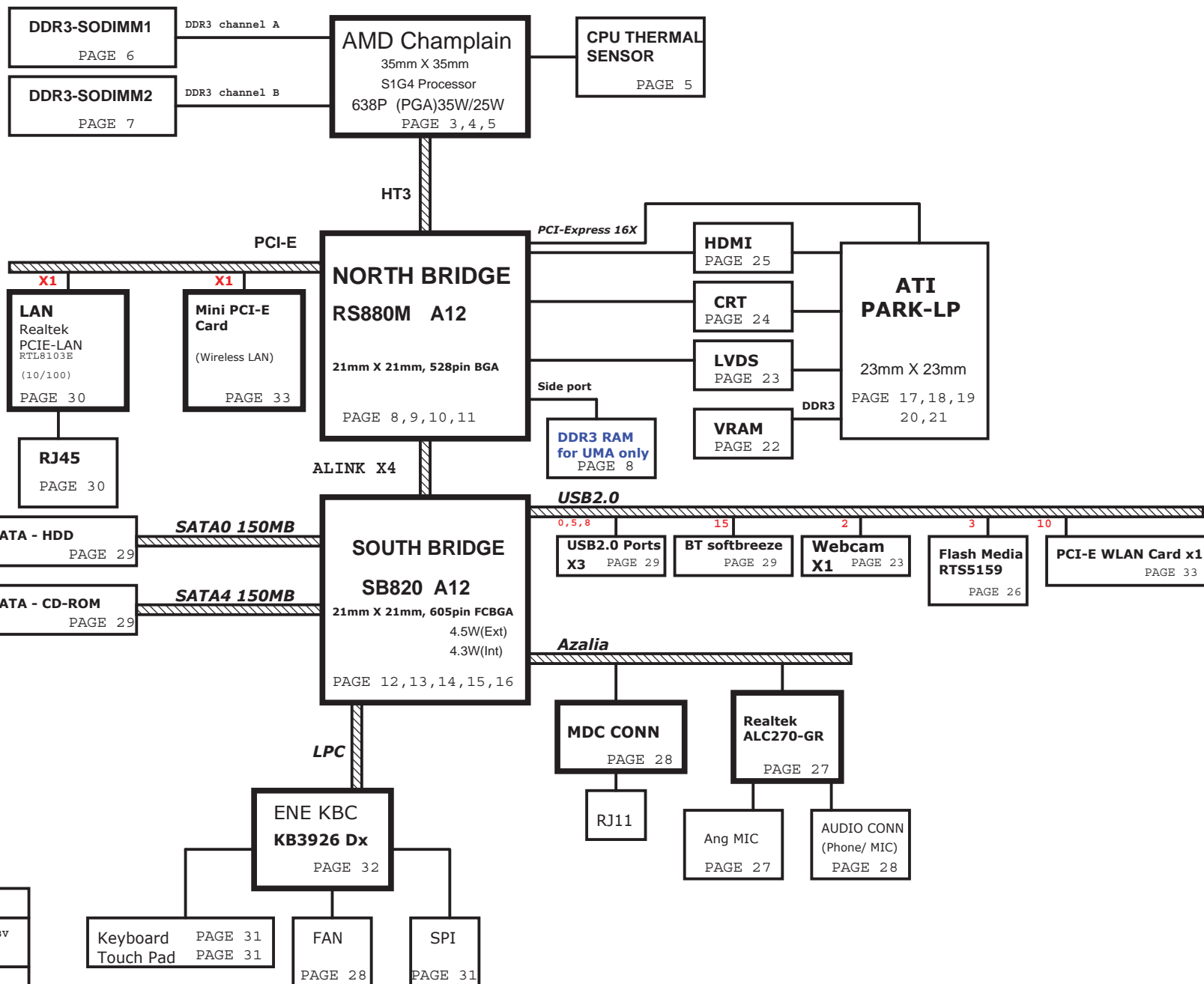


AX2/7 SYSTEM DIAGRAM



01




- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V~1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

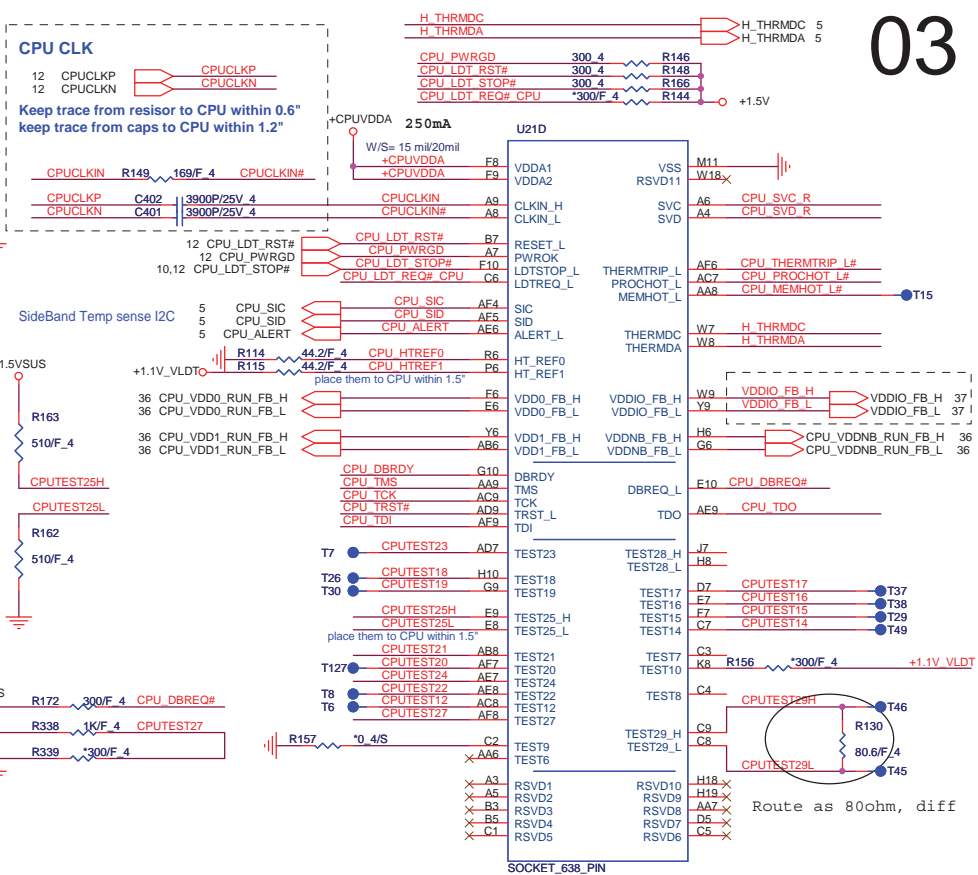
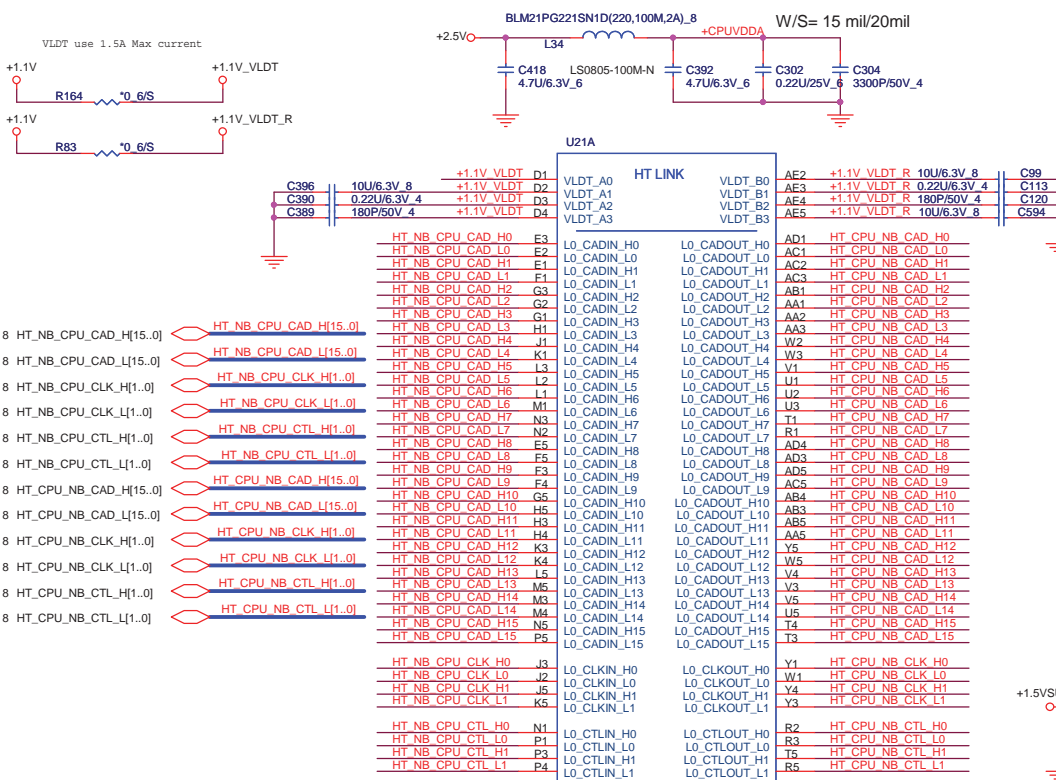
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

PROJECT : AX2/7
Quanta Computer Inc.

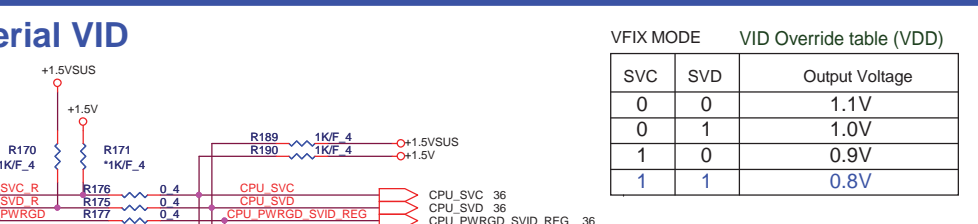
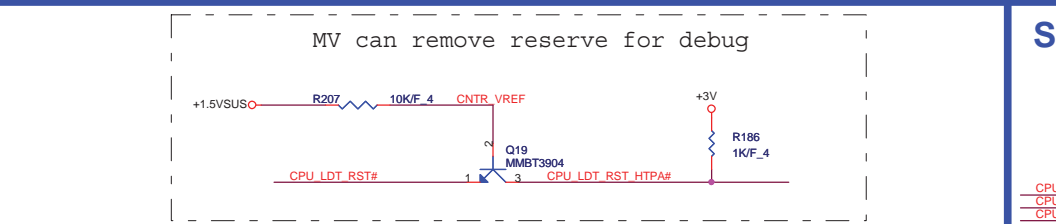
Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Thursday, December 24, 2009 Sheet 1 of 42		

PV,delete all external clock GEN reserve material

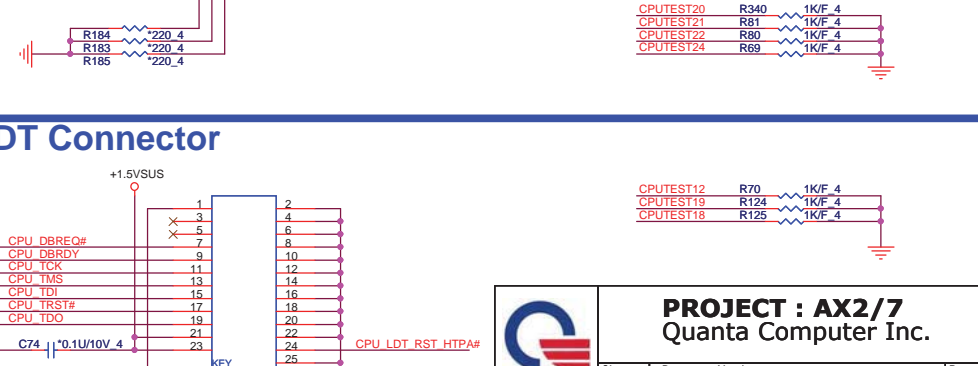
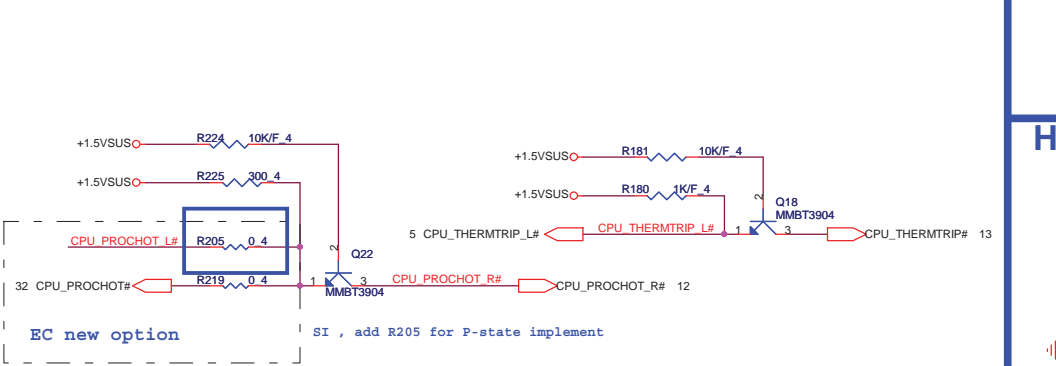
 NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc.	
	Size Custom	Document Number Clock Generator
Date: Wednesday, December 23, 2009 Sheet 2 of 42		Rev 1A



FOX PZ63826-284R-41F
 DG0*8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
 MLX 47296-4131
 DG0*8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
 TYC 4-1903401-2
 DG0*8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

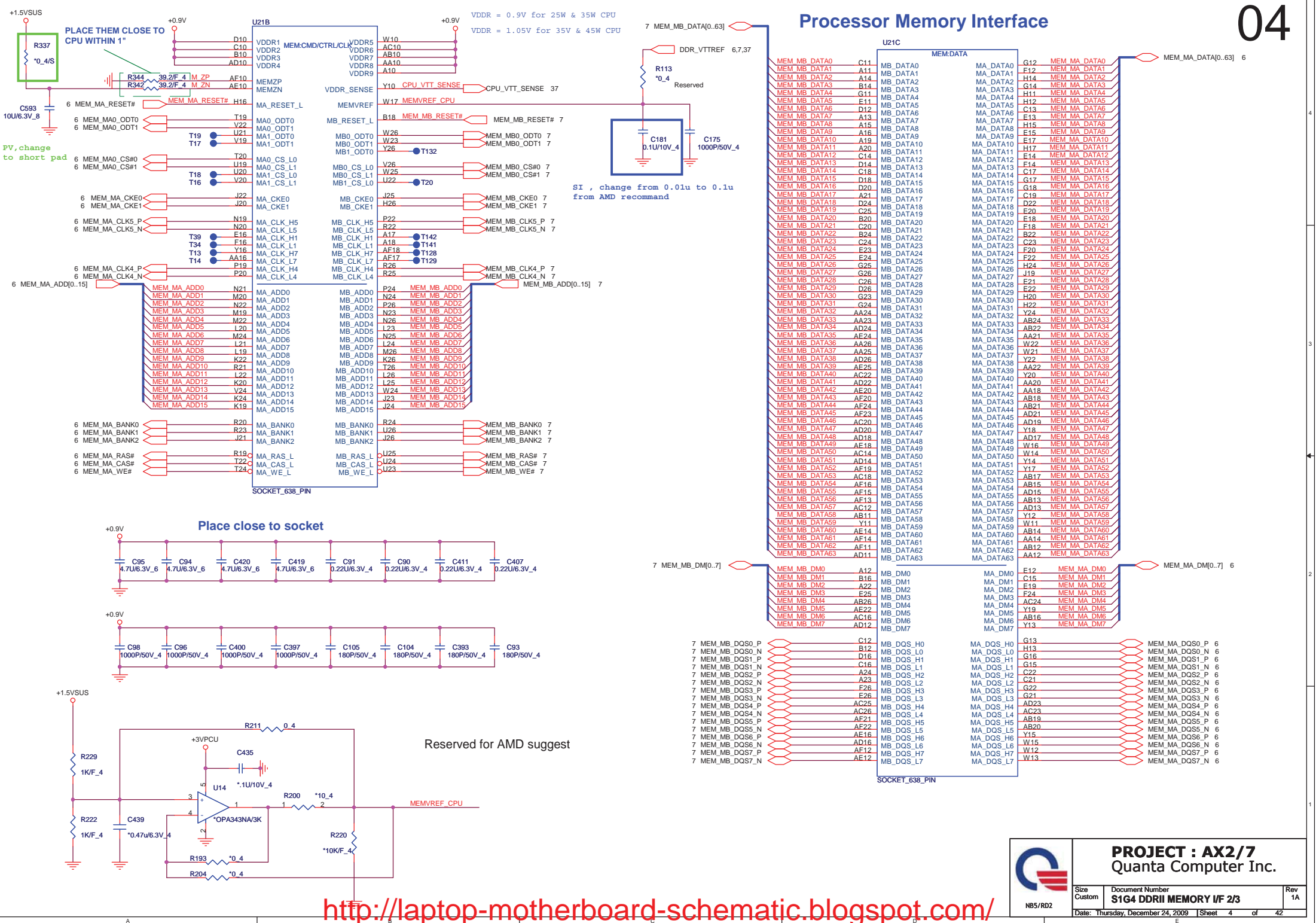


SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



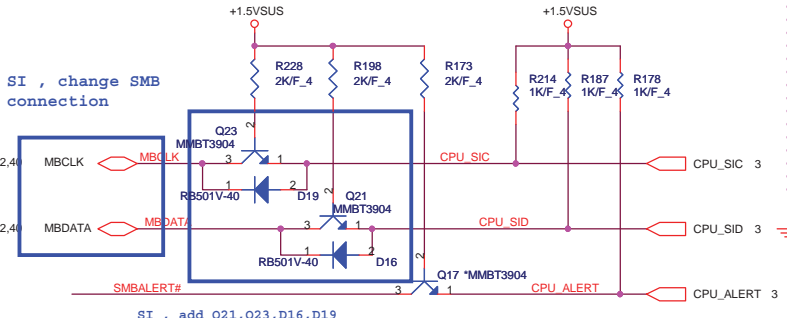
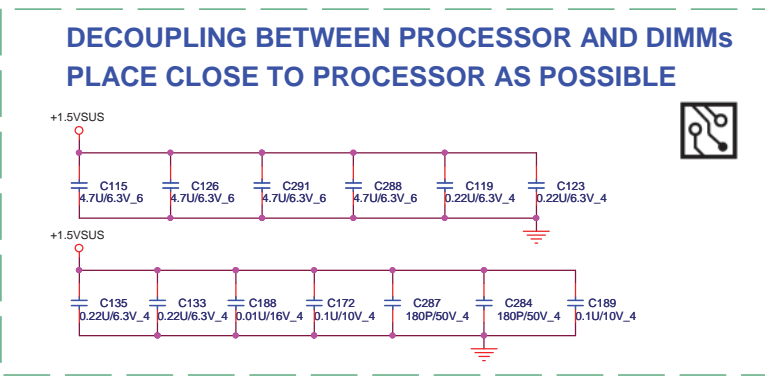
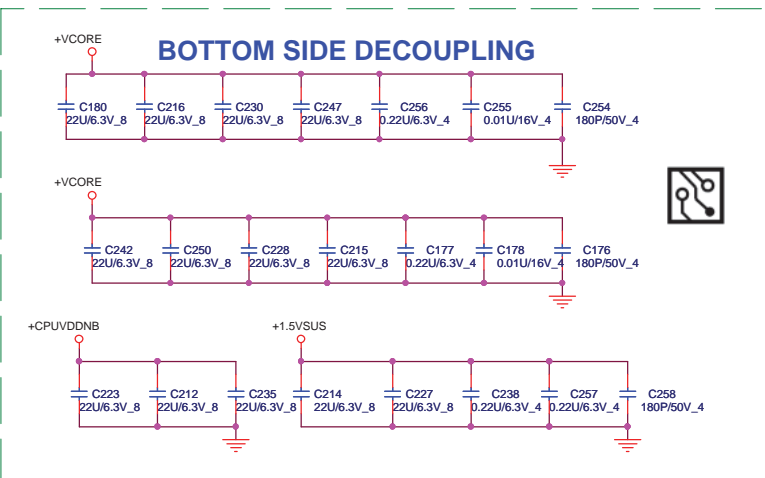
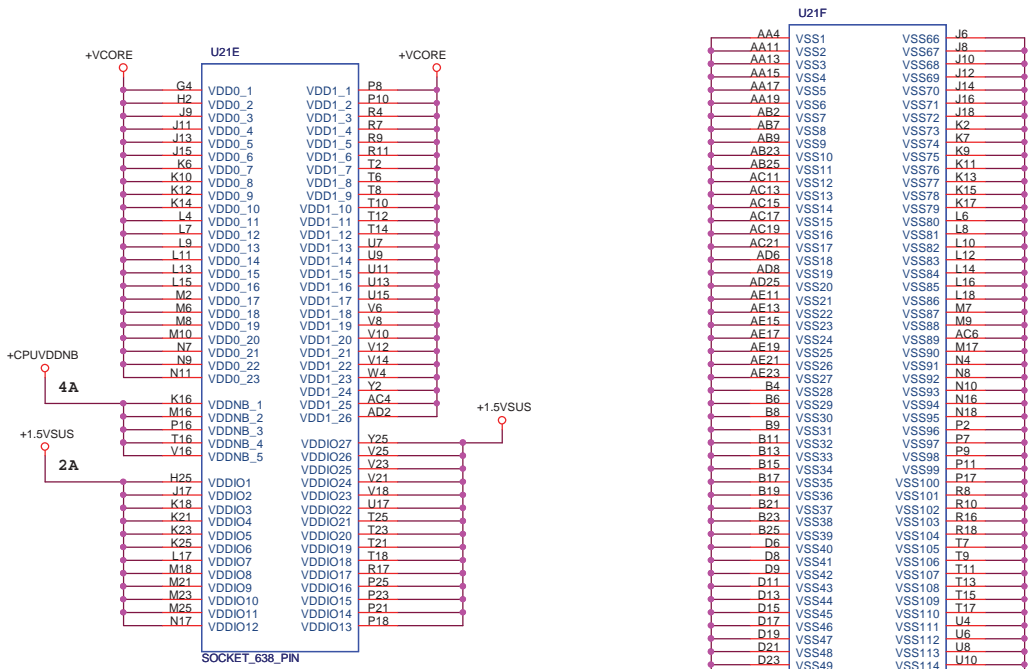
PROJECT : AX2/7
 Quanta Computer Inc.

Size Custom Document Number S1G4 HT,CTL I/F 1/3 Rev 1A
 Date: Thursday, December 24, 2009 Sheet 3 of 42

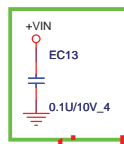
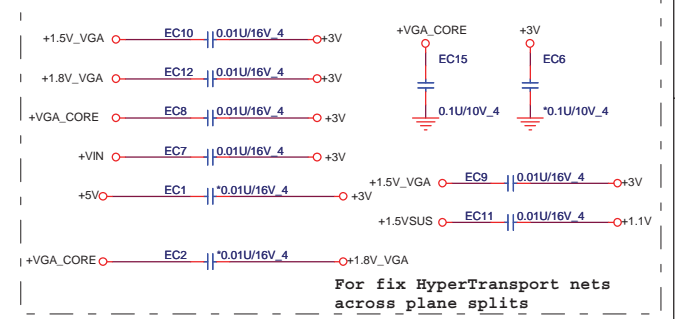
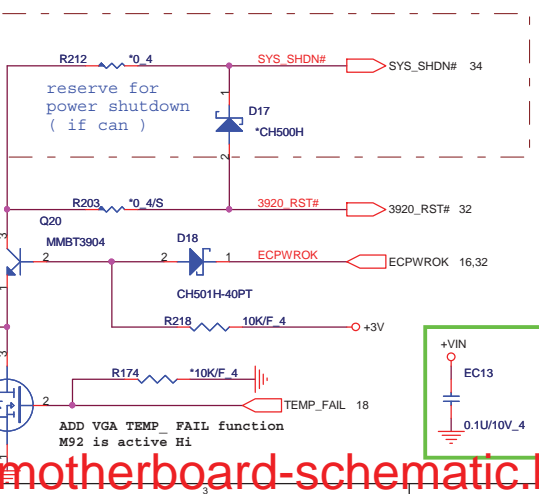
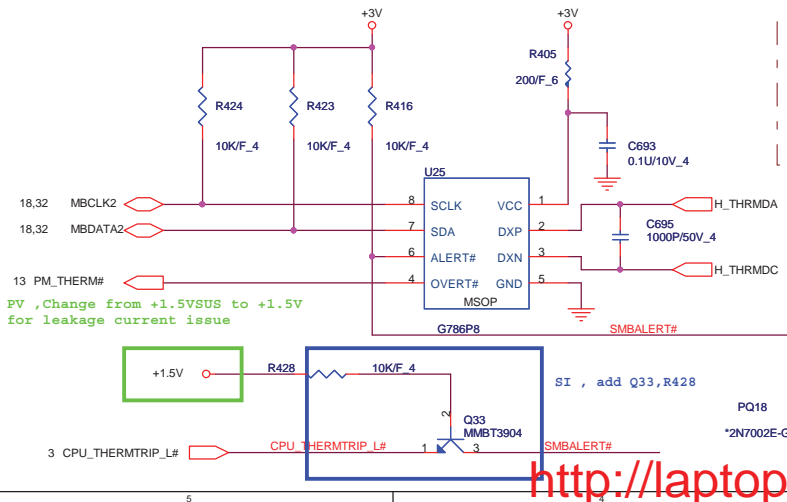


PROJECT : AX2/7
Quanta Computer Inc.

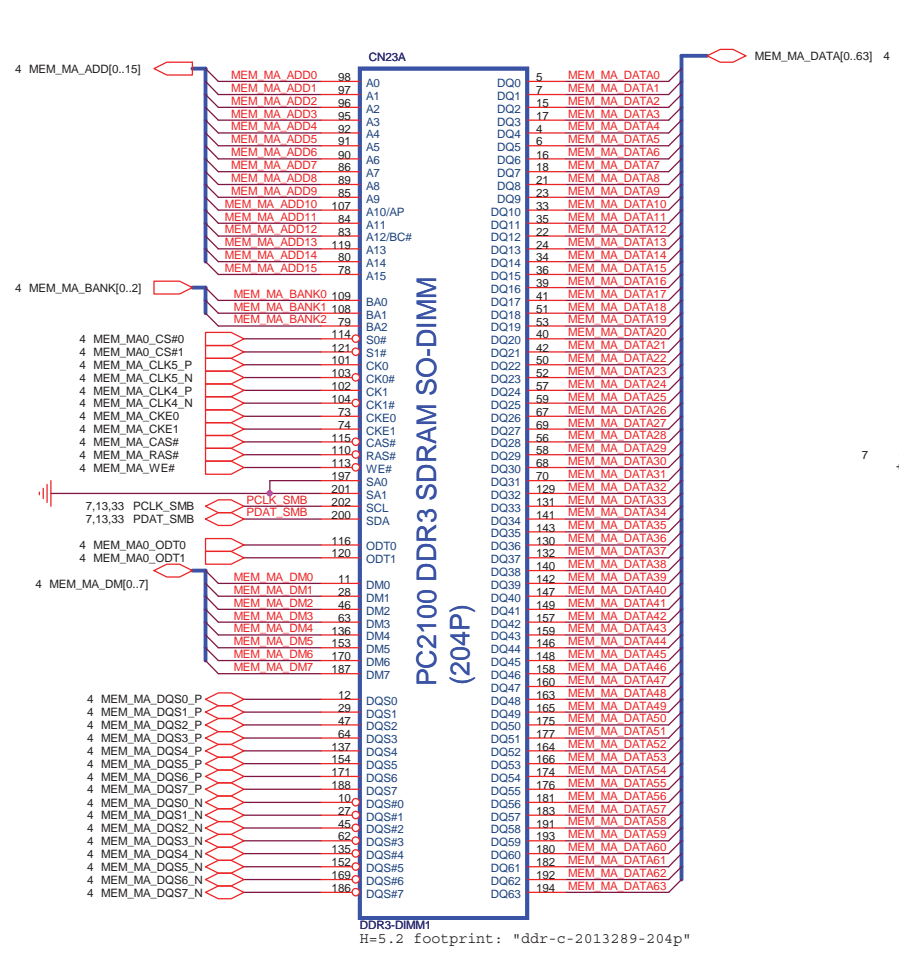
Size: Custom | Document Number: S1G4 DDRII MEMORY I/F 2/3 | Rev: 1A
 Date: Thursday, December 24, 2009 | Sheet: 4 of 42



PROCESSOR POWER AND GROUND



PROJECT : AX2/7
Quanta Computer Inc.

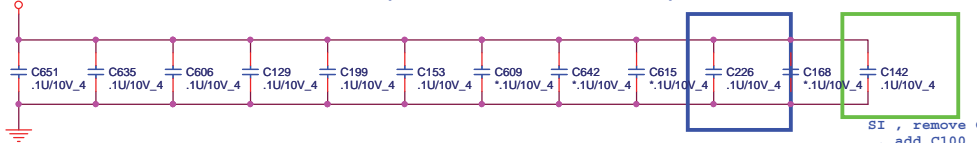


PC2100 DDR3 SDRAM SO-DIMM (204P)

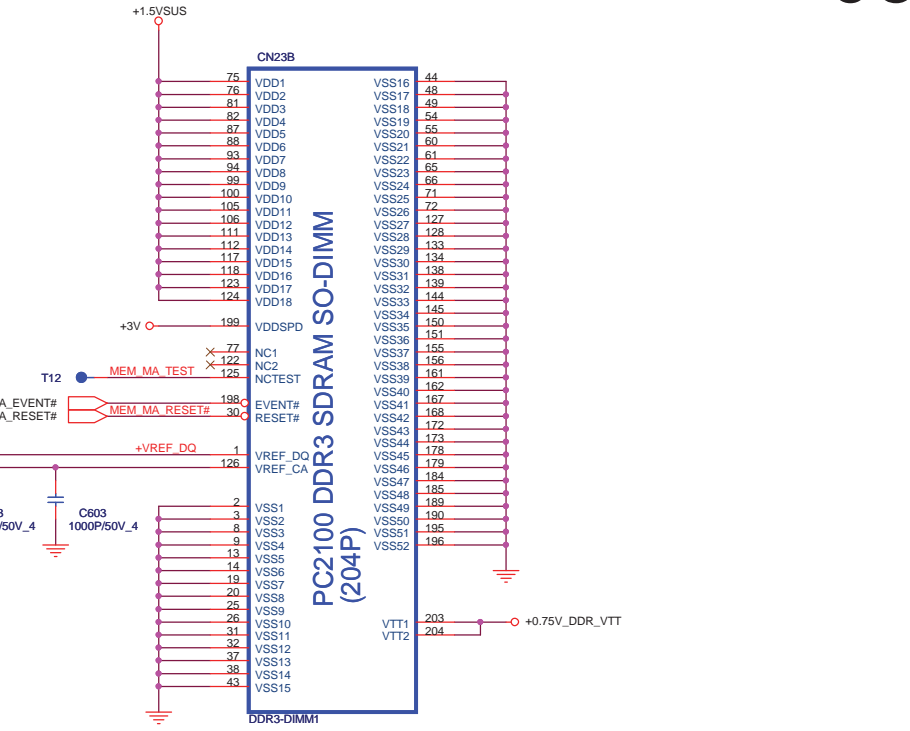
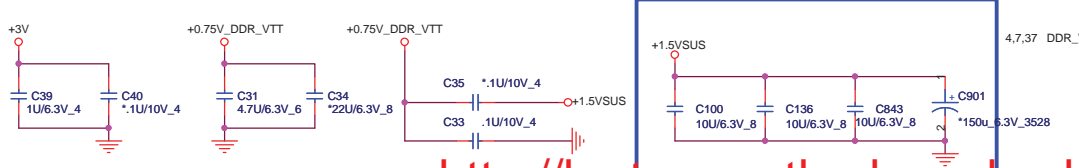
DDR3-DIMM1
H=5.2 footprint: "ddr-c-2013289-204p"

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

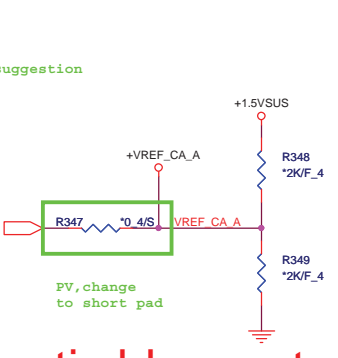
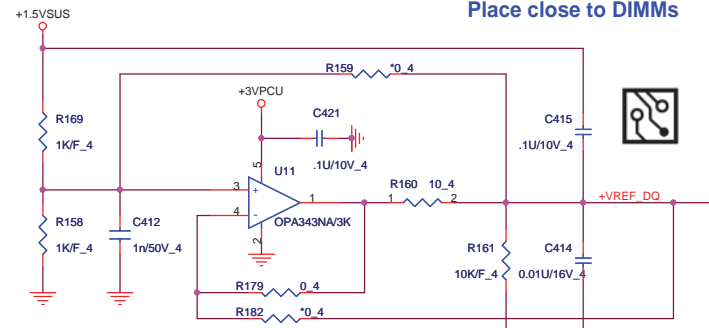
DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN) SI , add C226 from EMI suggest



DE-COUPLING FOR DIMM1

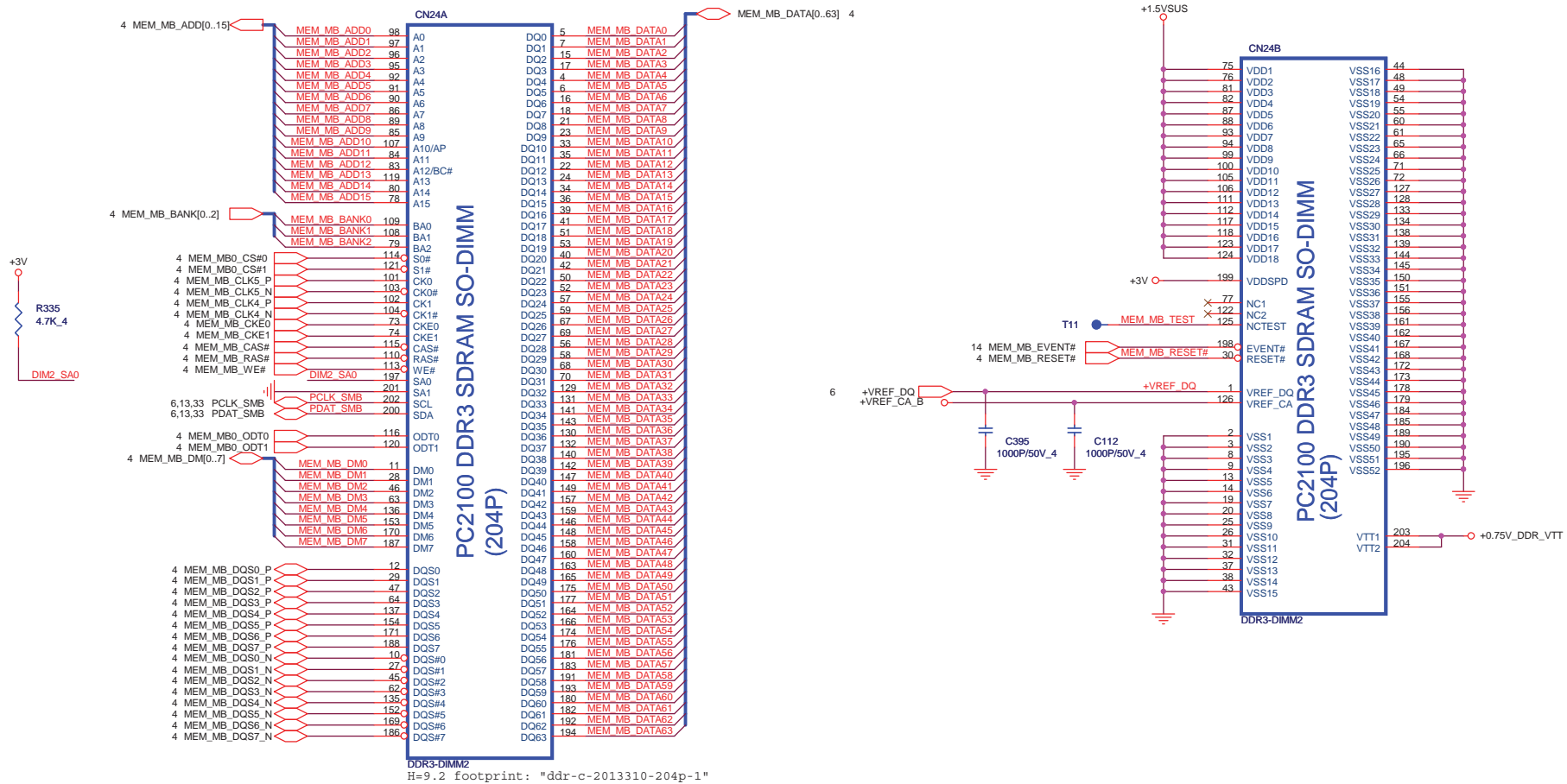


Place close to DIMMs



PROJECT : AX2/7
Quanta Computer Inc.

Size Custom Document Number **DDR3 SODIMMS: A/B CHANNEL** Rev 1A
NB5/RD2 Date: Thursday, December 24, 2009 1 Sheet 6 of 42

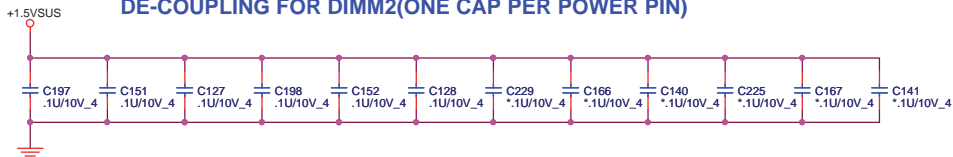


SO-DIMM BYPASS PLACEMENT :

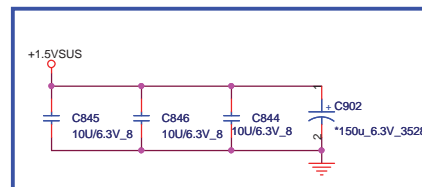
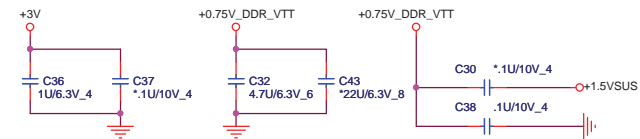
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

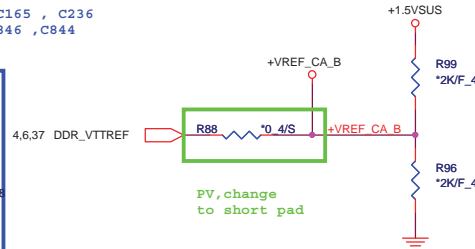
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)



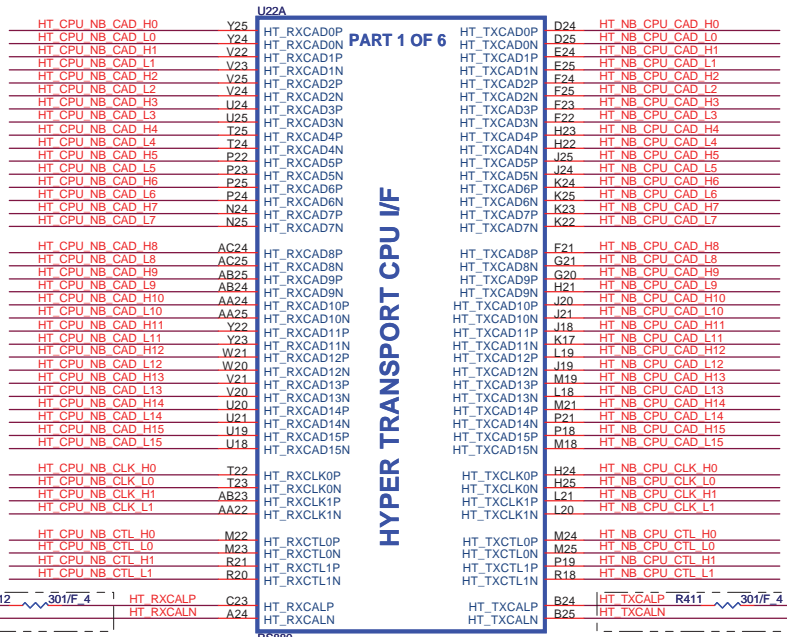
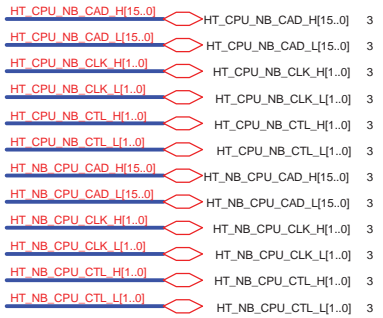
DE-COUPLING FOR DIMM2



SI , remove C165 , C236
add C845 , C846 , C844
Reserve C902



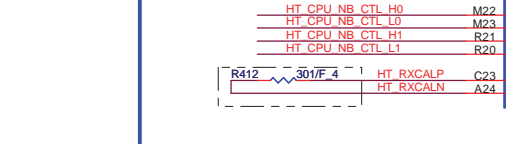
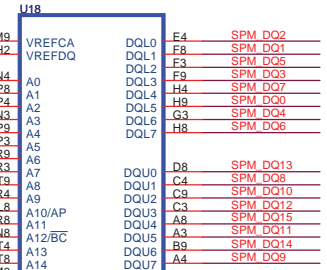
	PROJECT : AX2/7	
	Quanta Computer Inc.	
	Size Custom NBS/RD2	Document Number DDR3 SODIMMS TERMINATIONS
Date: Thursday, December 24, 2009 Sheet 7 of 42		



PART 1 OF 6

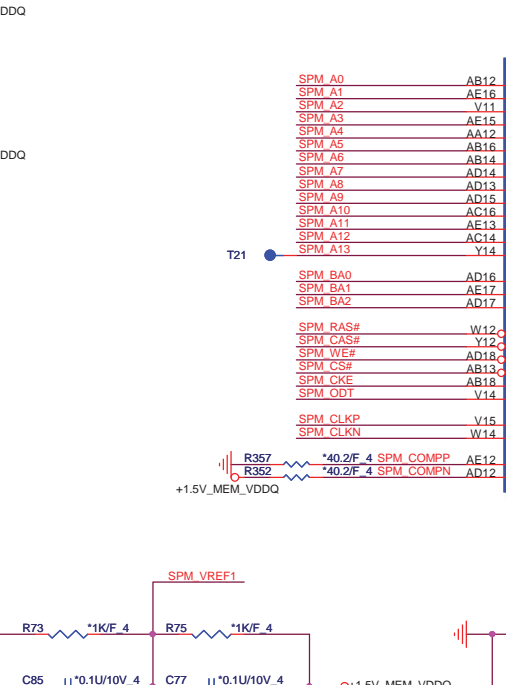
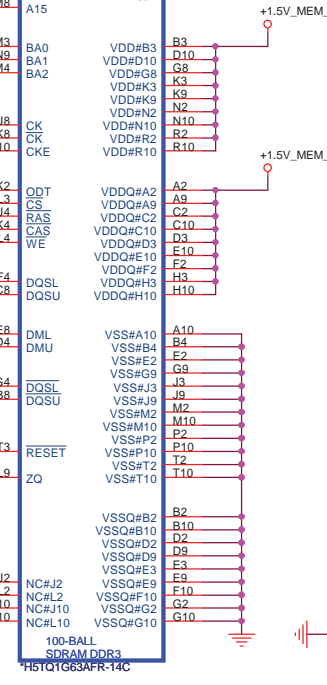
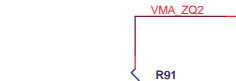
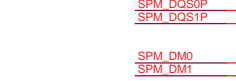
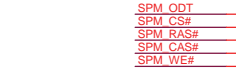
HYPER TRANSPORT CPU I/F

signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		



This block is for UMA only , DIS can remove all component

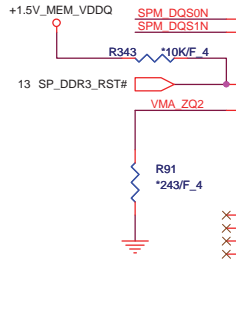
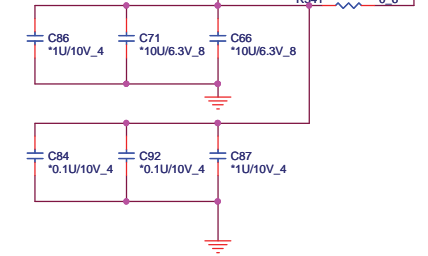
SI, exchange net name



PAR 4 OF 6

SBD_MEM/DVO_I/F

40mils width or more



PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number RS880-HT LINK I/F 1/5	Rev 1A
Date: Thursday, December 24, 2009	Sheet 8	of 42

GFX_RX can remove at next stage for MUXLESS

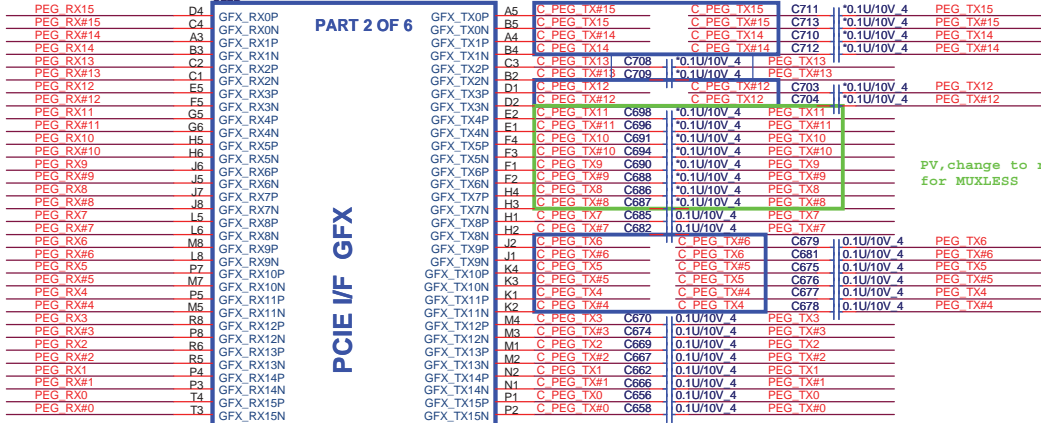
SI , for routing smooth
GFX_TX 0/1/3/9/10/11

UMA can remove all GFX_TX CAP

SI remove C711,C713,C710,
C712,C708,C709,C703,C704
for MUXLESS

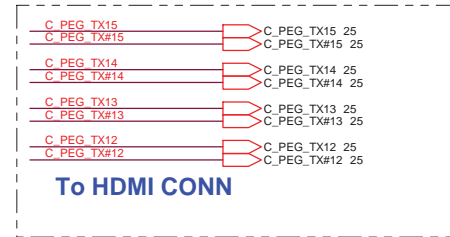
PART 2 OF 6

PCI-E I/F GFX



FV,change to reserve for MUXLESS

Close to North Bridge



To HDMI CONN



RS880

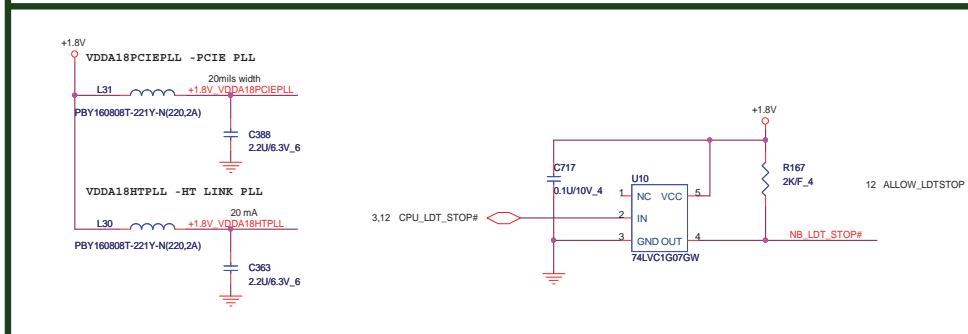
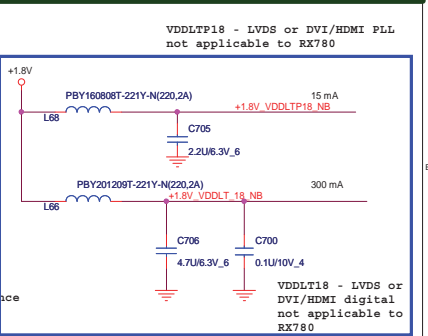
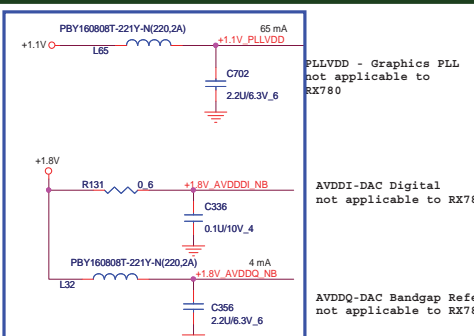
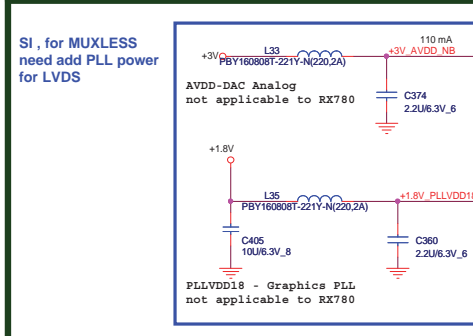
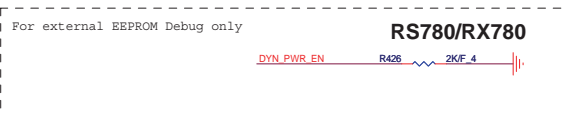
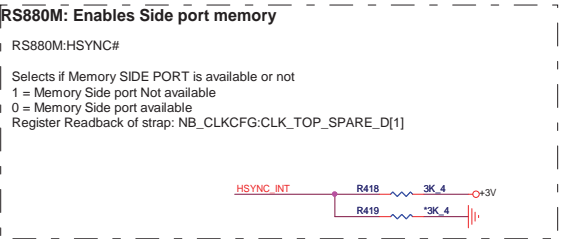
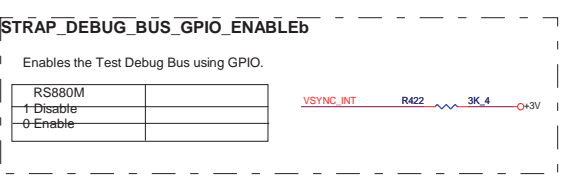
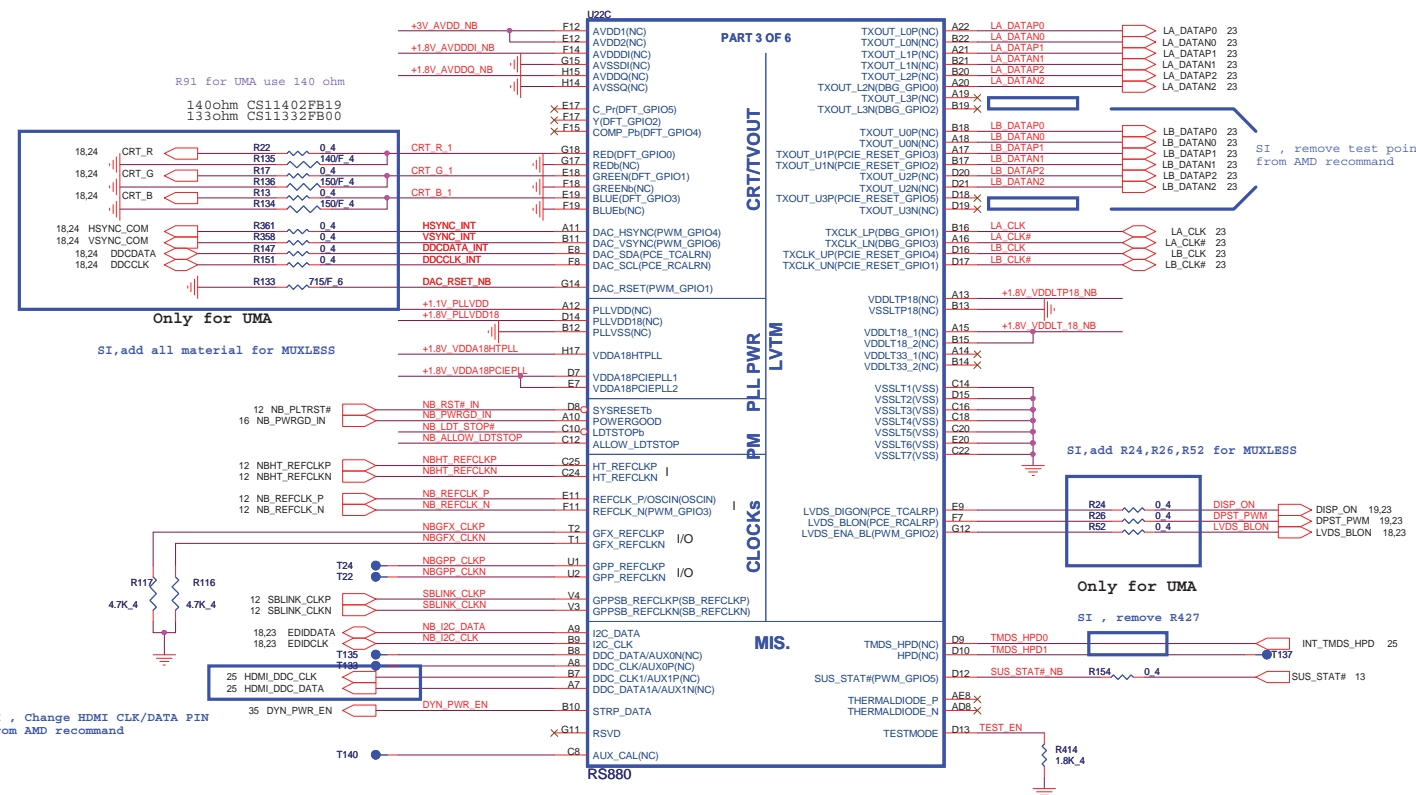
RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

PROJECT : AX2/7
Quanta Computer Inc.

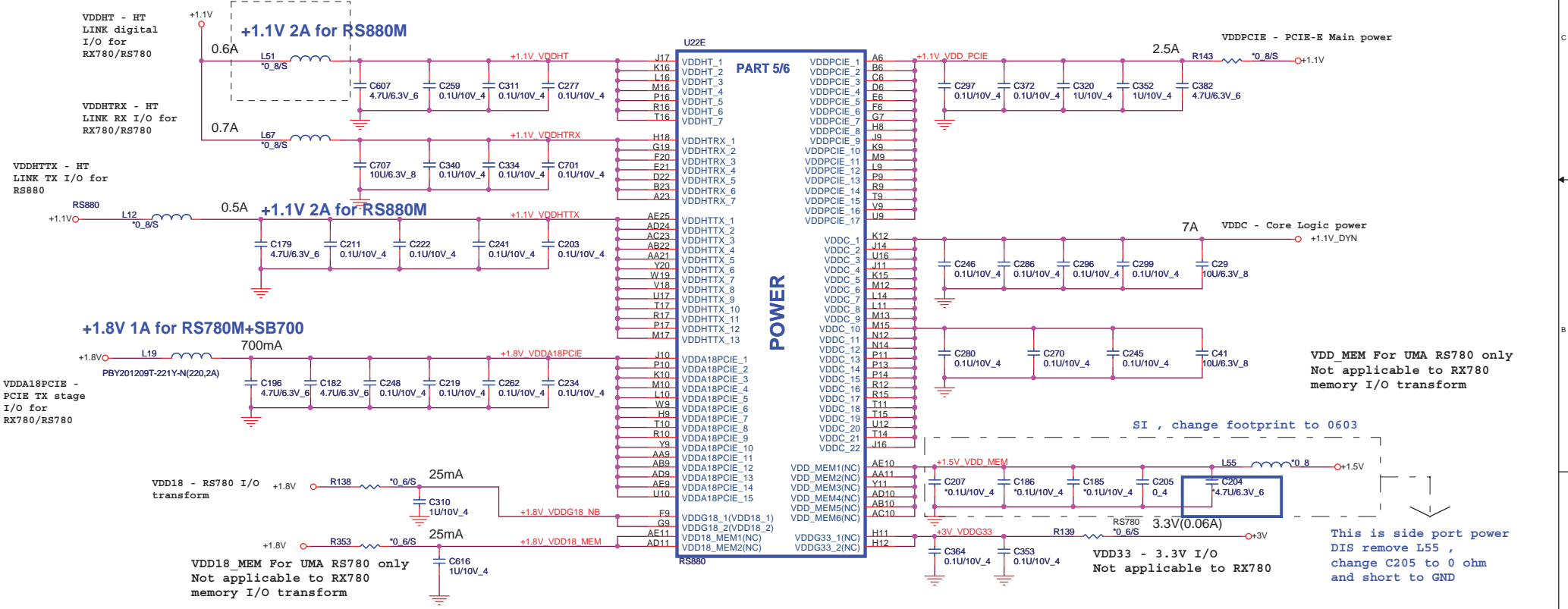
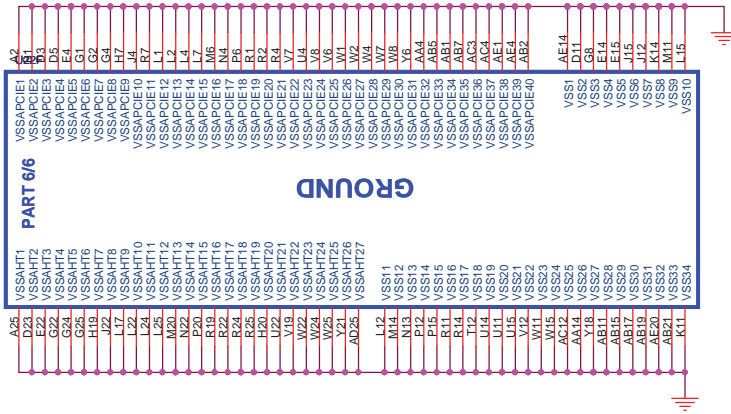
Size Custom
Document Number **RS880-PCIE I/F 2/5**
Date: Thursday, December 24, 2009 | Sheet 9 of 42

Rev 1A



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLTP18	+1.8V
IOPLLVD18	+1.8V	VDDLTP18	+1.8V
		VDDLTP18	NC



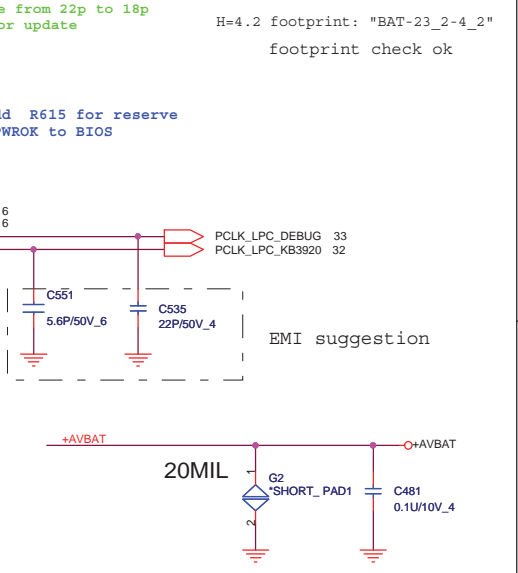
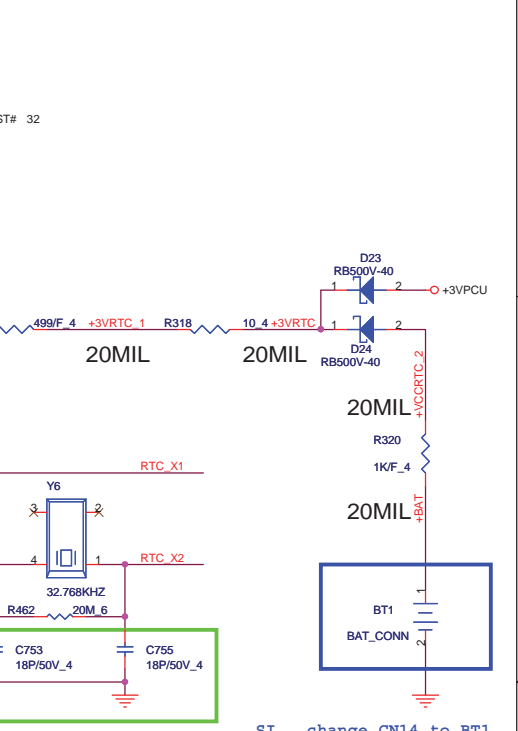
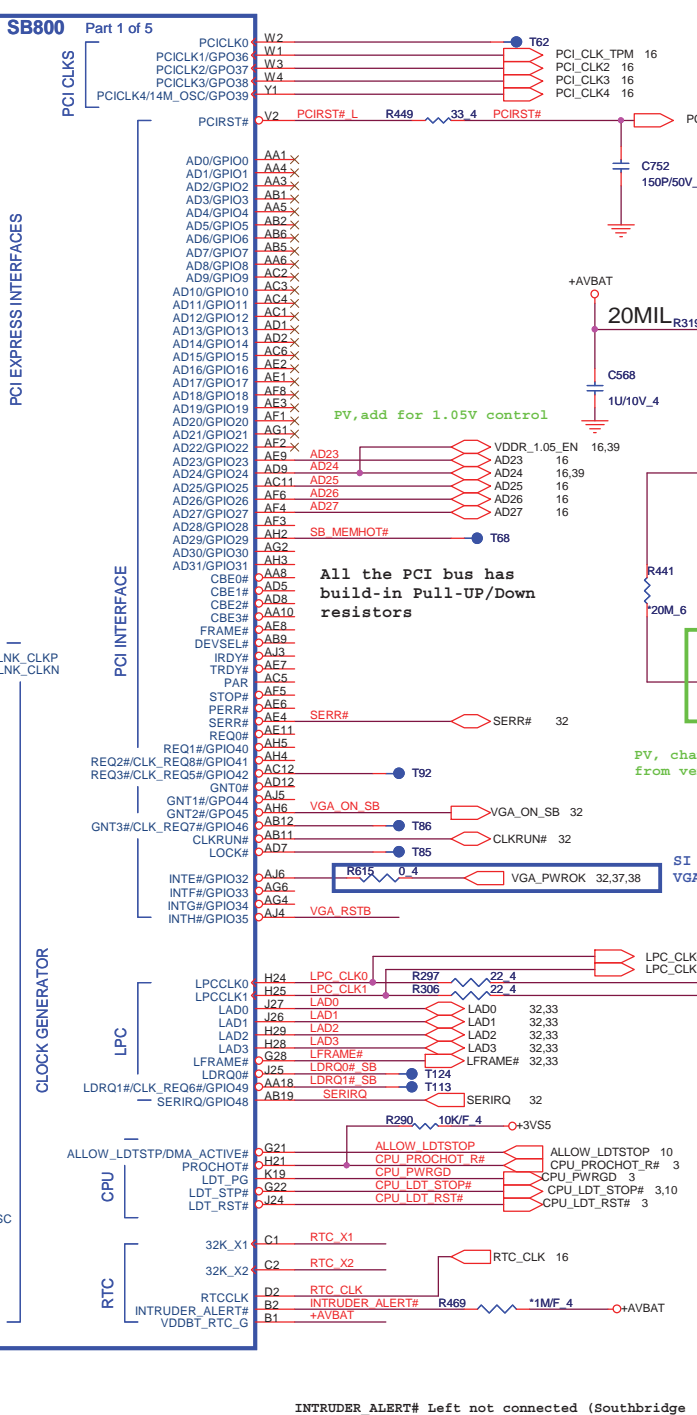
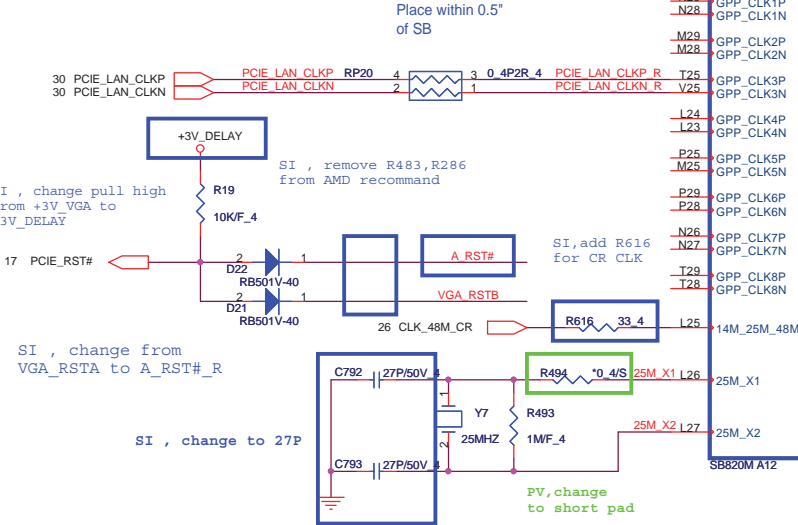
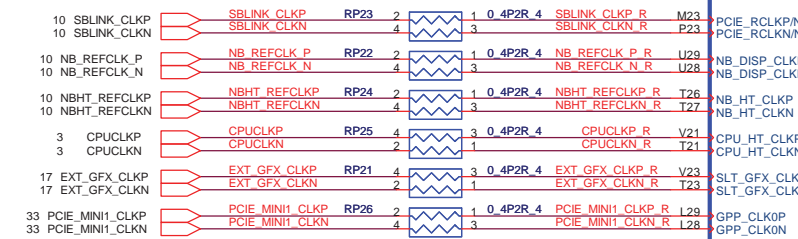
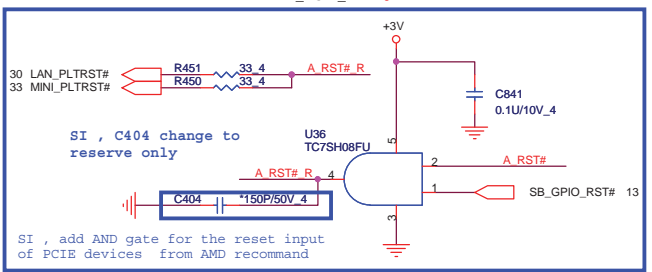
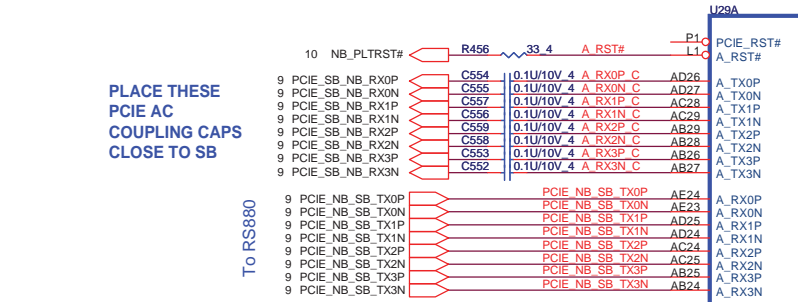
VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

This is side port power
DIS remove L55,
change C205 to 0 ohm
and short to GND



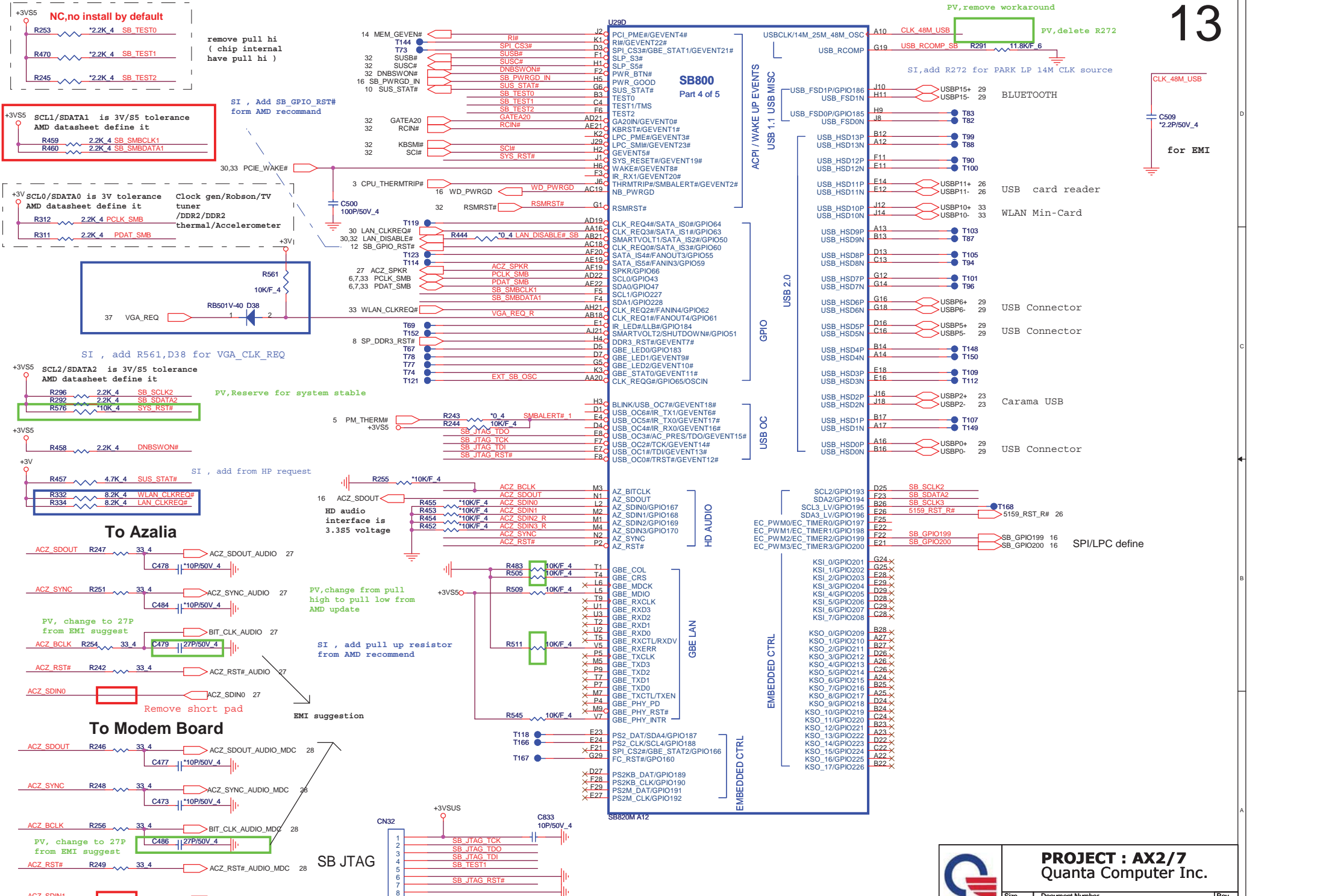
PROJECT : AX2/7
Quanta Computer Inc.

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB



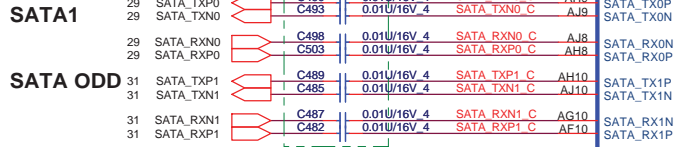
PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number SB820-PCIE/PCU/CPU/LPC 1/4	Rev 1A
Date: Thursday, December 24, 2009		Sheet 12 of 42



SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB820



IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SI define side port ID

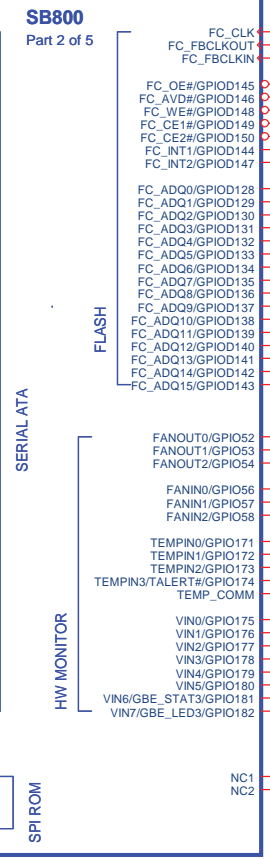
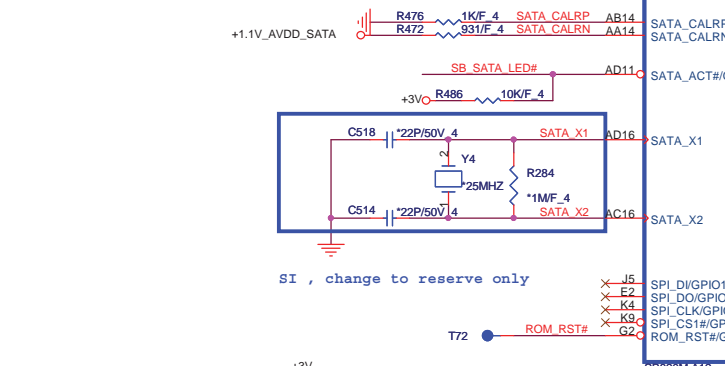
SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

PLACE SATA CAL RES VERY CLOSE TO BALL OF SB820

NOTE:
 R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

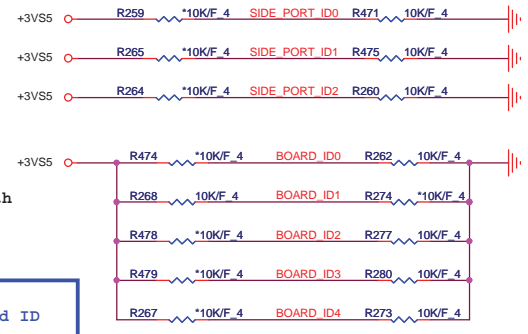


SI, remove test point from AMD recommend

PV, change to short pad

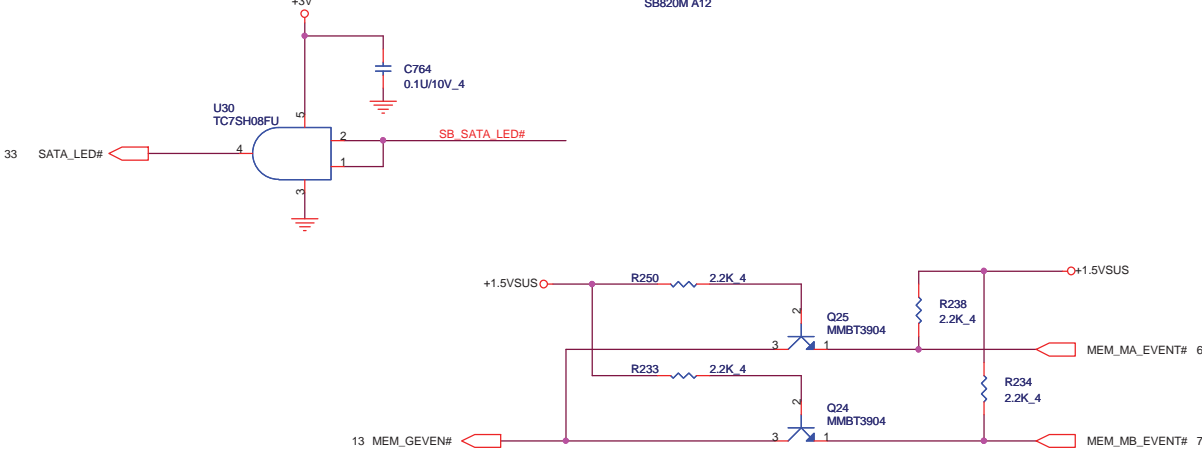
For blue tooth & wireless merge card

SI define board ID



ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	AX2 UMA DF
0	0	0	0	1	AX7 UMA DF
0	0	0	1	0	AX2 PARK DF
0	0	0	1	1	AX7 PARK DF
0	0	1	0	0	AX2 UMA FF
0	0	1	0	1	AX7 UMA FF
0	0	1	1	0	AX2 PARK FF
0	0	1	1	1	AX7 PARK FF
0	1	0	1	0	AX2 M93 DF
0	1	0	1	1	AX7 M93 DF
0	1	1	1	0	AX2 M93 FF
0	1	1	1	1	AX7 M93 FF

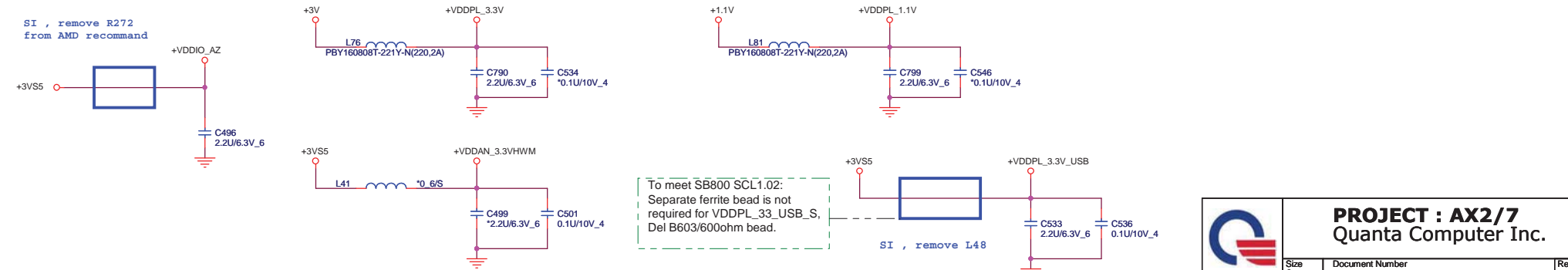
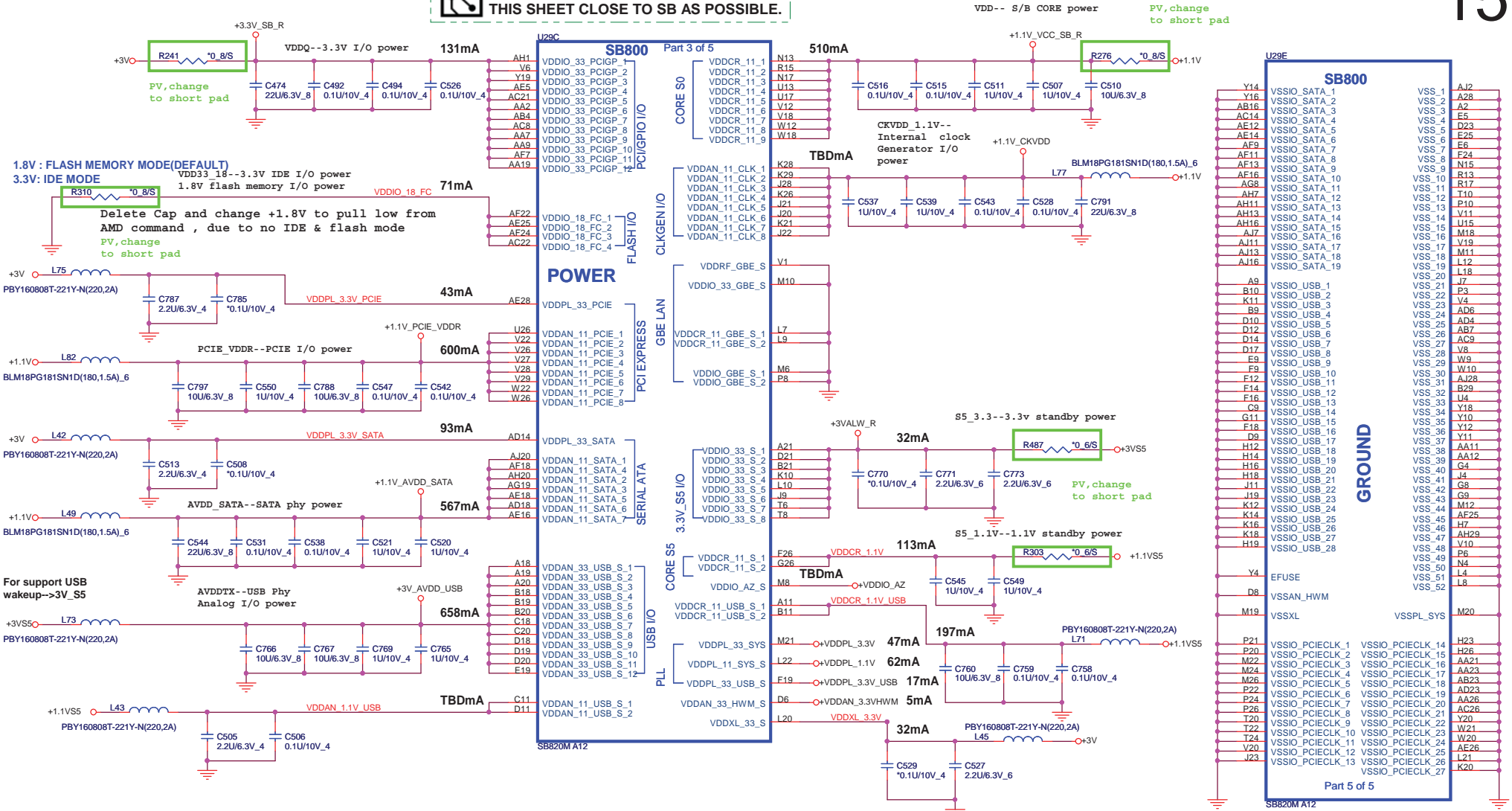
PV define for M93



PROJECT : AX2/7
 Quanta Computer Inc.

Size Custom Document Number SB820-ACPI/GPIO/USB 2/4 Rev 1A
 Date: Thursday, December 24, 2009 Sheet 14 of 42

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



PROJECT : AX2/7
 Quanta Computer Inc.

Date: Tuesday, December 22, 2009 | Sheet 15 of 42

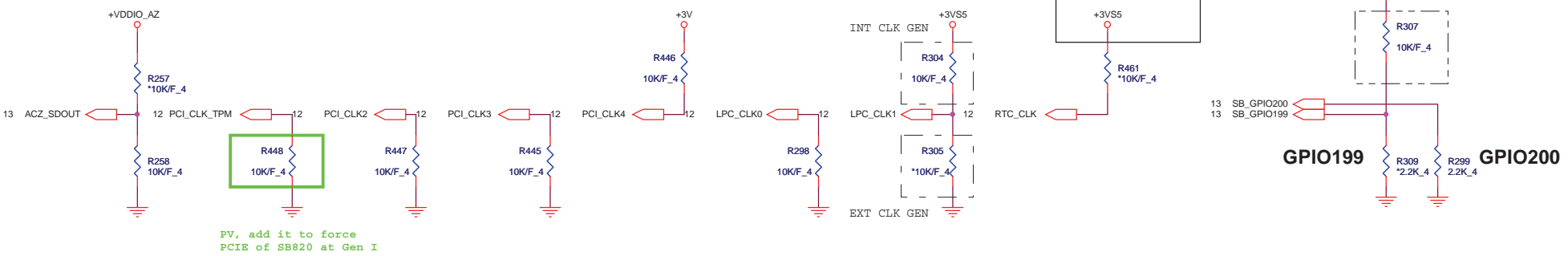
Rev 1A

Document Number: SB820-PWR/DECOUPLING 4/4

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull Hi 10K , confirm AMD ward this pull Hi not need

REQUIRED STRAPS



PV, add it to force PCIE of SB820 at Gen I

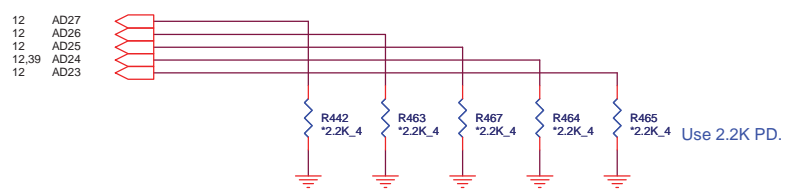
It must ready before RSMRST#

REQUIRED STRAPS

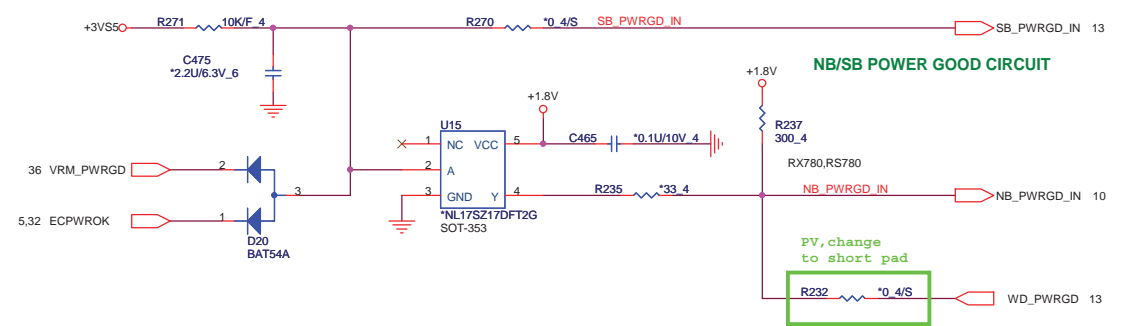
	AZ_SDOOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



NB_PWRGD_IN: RS780/RX780 = 1.8V; RS740 = 3.3V Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

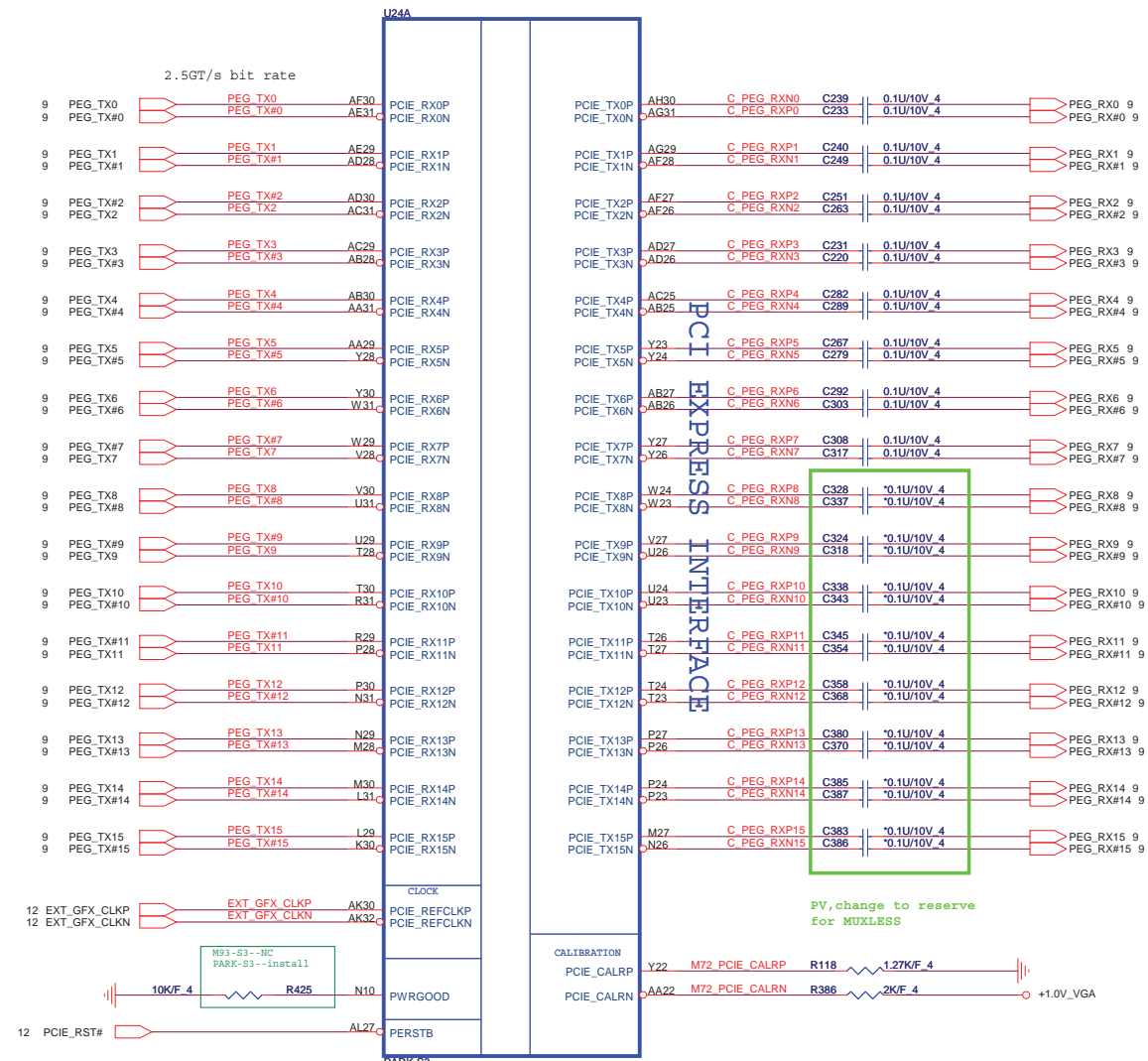


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

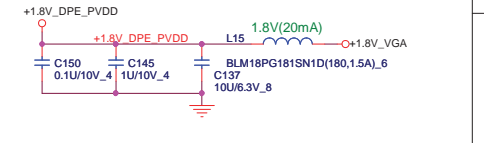
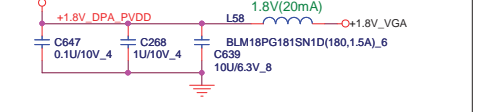
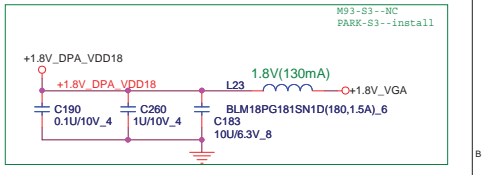
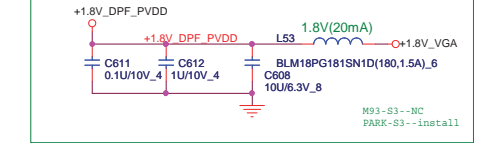
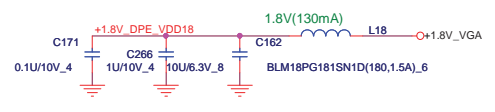
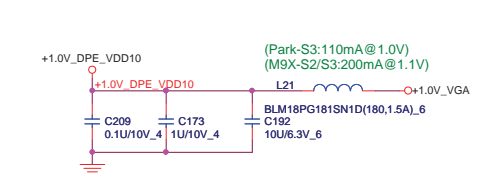
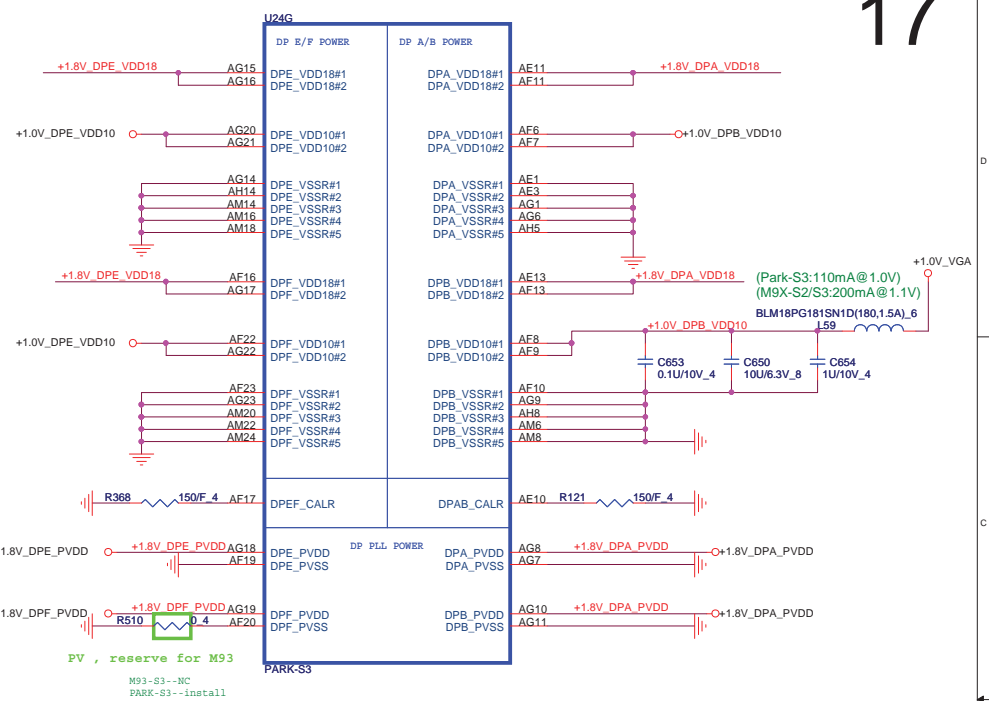
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : AX2/7
Quanta Computer Inc.

Size: Custom | Document Number: SB820-STRAPS | Rev: 1A
Date: Thursday, December 24, 2009 | Sheet: 16 of 42



100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

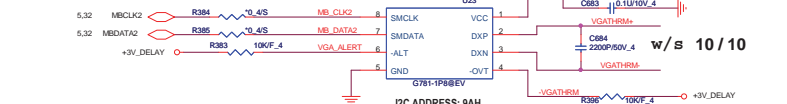
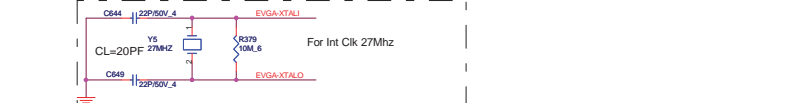
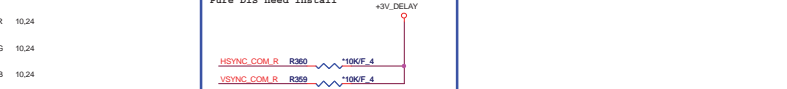
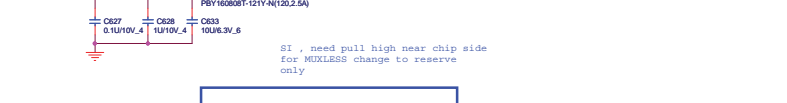
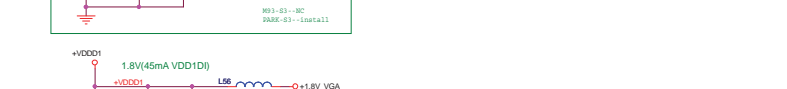
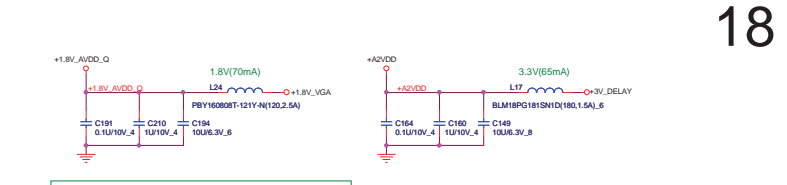
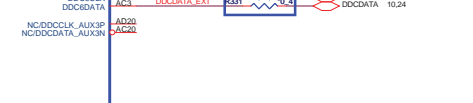
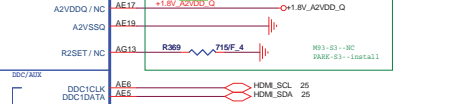
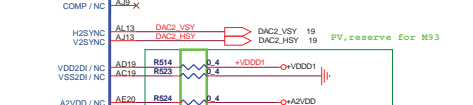
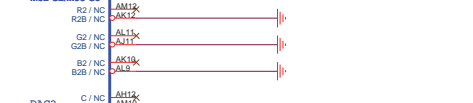
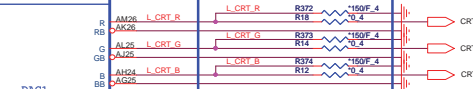
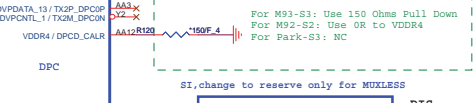
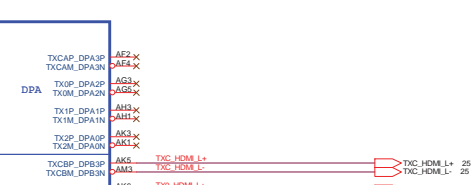
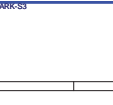
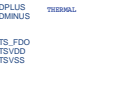
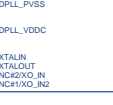
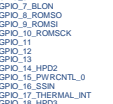
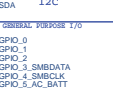
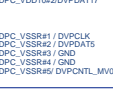
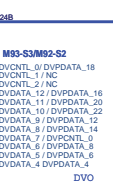
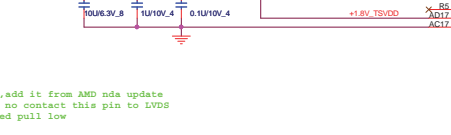
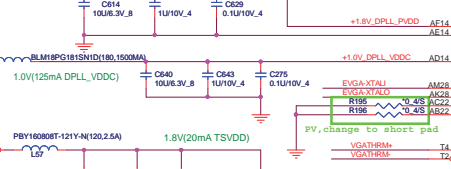
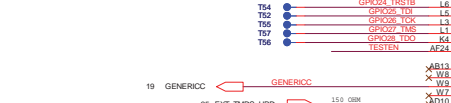
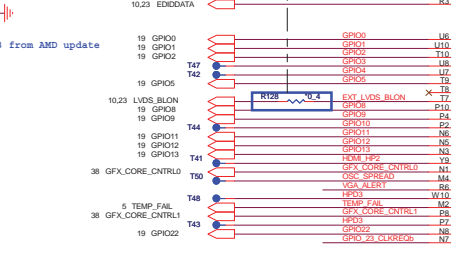
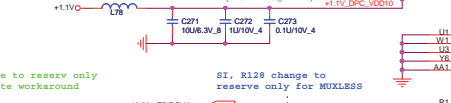
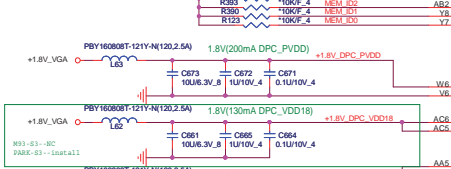
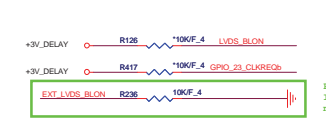
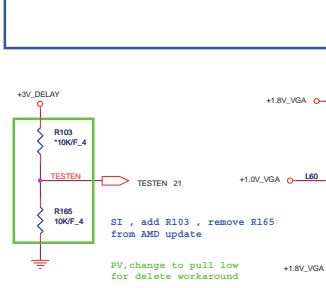
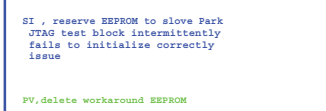
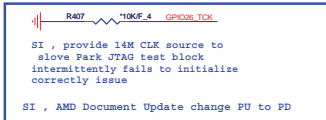
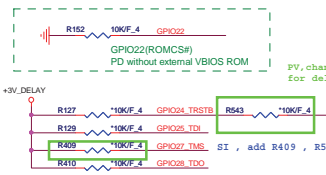


PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
NBS/RD2	PARK_PCIE Interface	
Date: Thursday, December 24, 2009	Sheet 17	of 42

MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung	E die	K4WIG1646E-NC12
0001	Bynix	Orion	HF70JG538F-12C
0010	Reserved		Reserved
0011	Reserved		Reserved
0100	Reserved		Reserved
0101	Reserved		Reserved
0110	Reserved		Reserved
0111	Reserved		Reserved
1000	Reserved		Reserved
1001	Reserved		Reserved
1010	Reserved		Reserved
1011	Reserved		Reserved
1100	Reserved		Reserved
1101	Reserved		Reserved
1110	Reserved		Reserved
1111	Reserved		Reserved

	PWRCTRL1	PWRCTRL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V



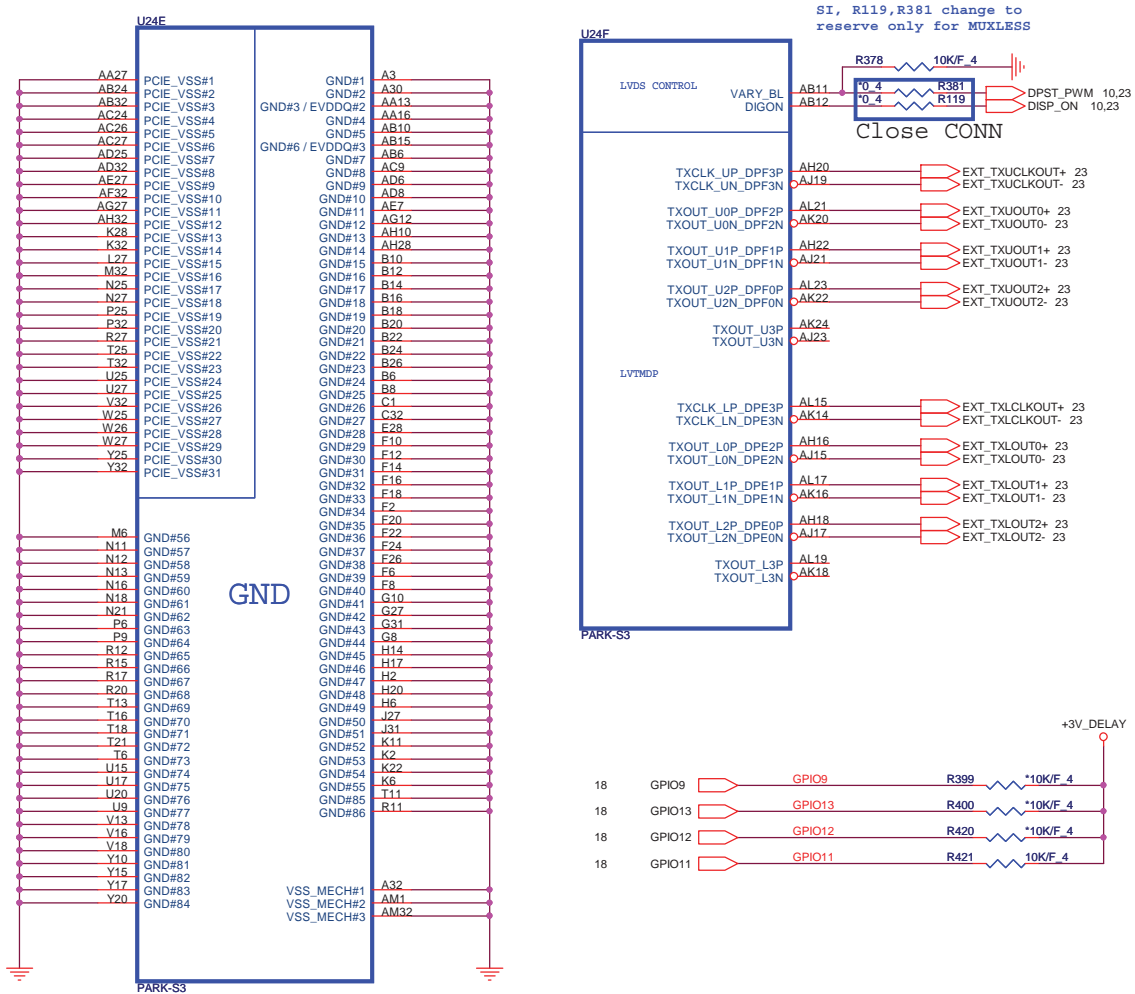
PROJECT : AX2/7
Quanta Computer Inc.

Rev 1A

Doc Number: PARK_Main

Date: Thursday, December 24, 2009

Sheet 18 of 22



CONFIGURATION STRAPS

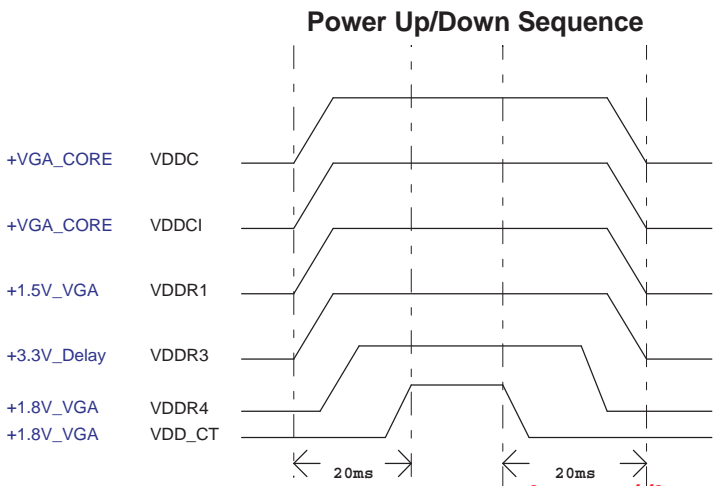
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

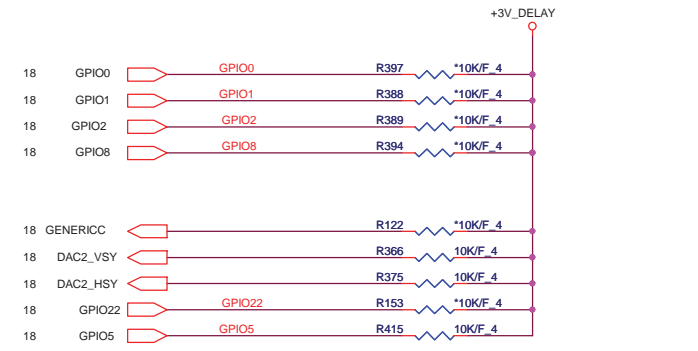
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		



Memory Aperture size

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

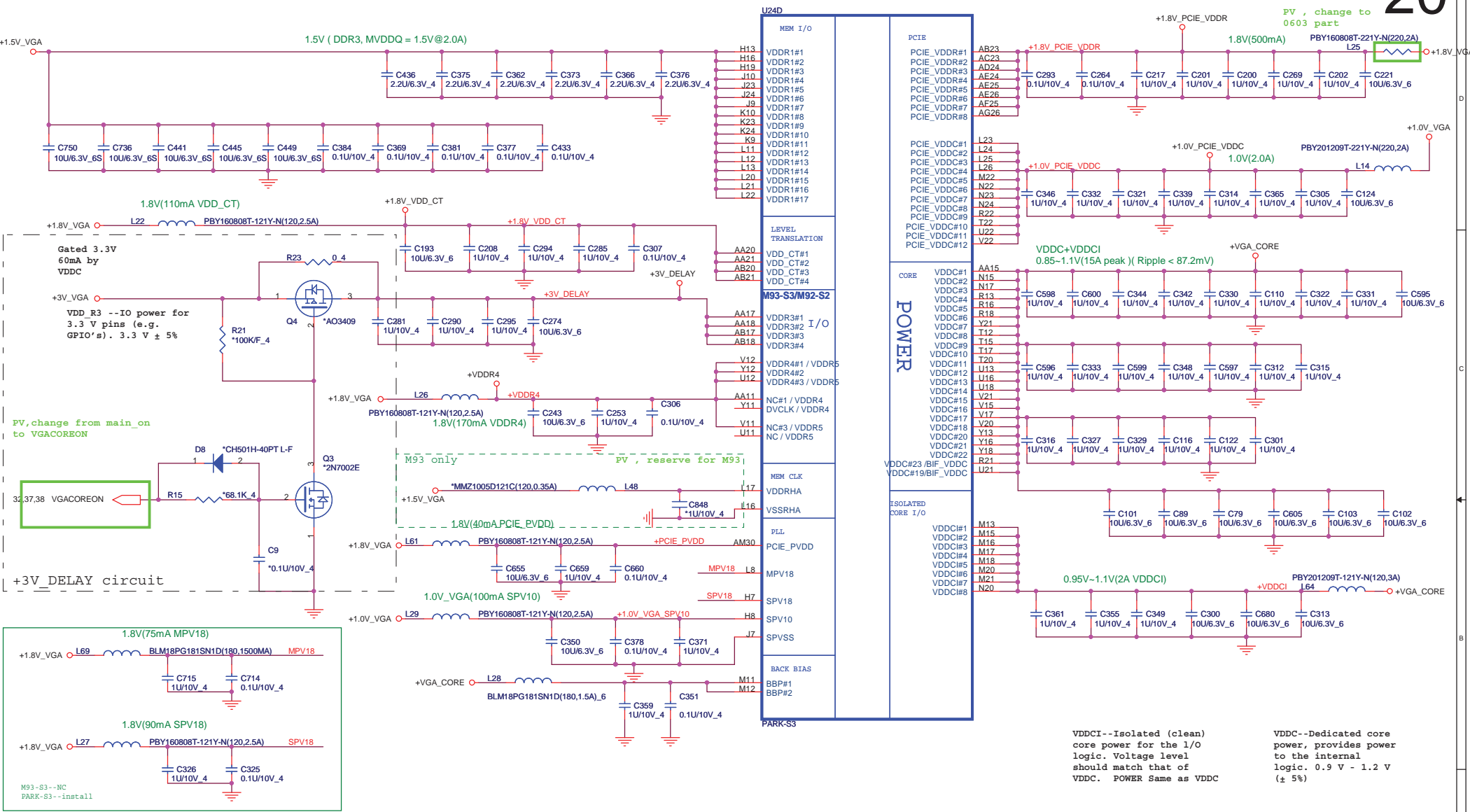


It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

PROJECT : AX2/7
Quanta Computer Inc.

Size Custom | Document Number **PARK_GND / LVDS/ Straps** | Rev 1A

Date: Thursday, December 24, 2009 | Sheet 19 of 42



VDDR1_1 & VDDR2_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

M93-S3--NC
 PARK-S3--Install

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

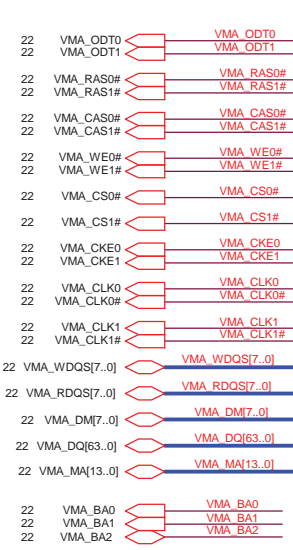
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (\pm 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%



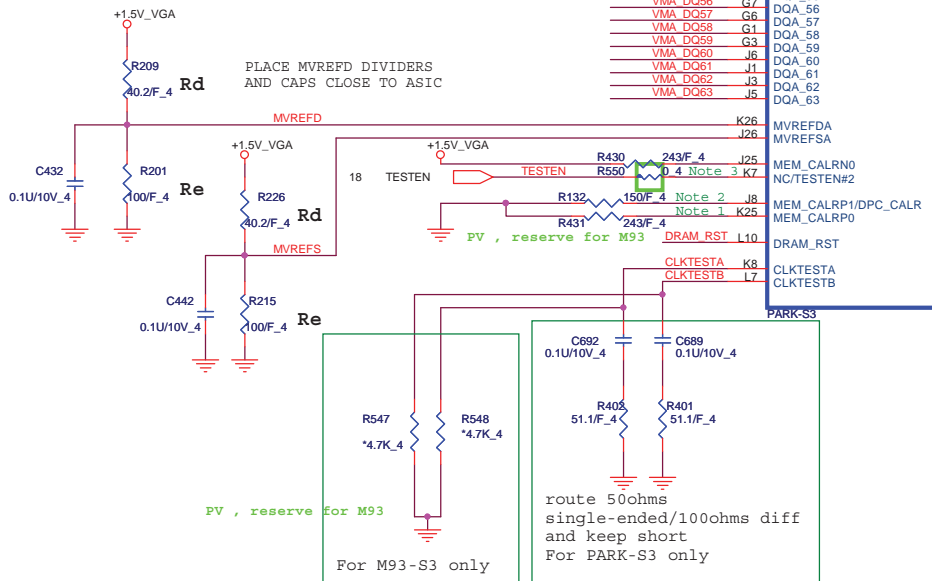
PROJECT : AX2/7
 Quanta Computer Inc.

Size Custom	Document Number PARK Power_and_NC	Rev 1A
Date: Thursday, December 24, 2009		Sheet 20 of 42

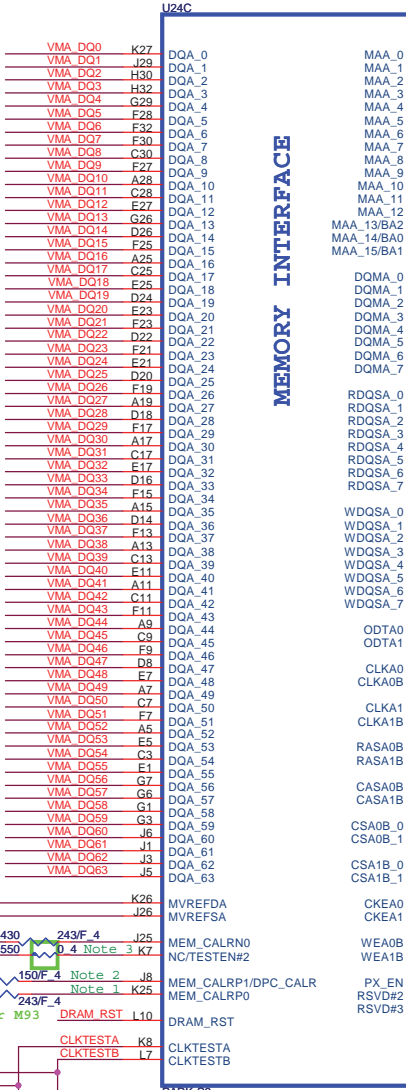


support 1gbt
VRAM (64M X 16)

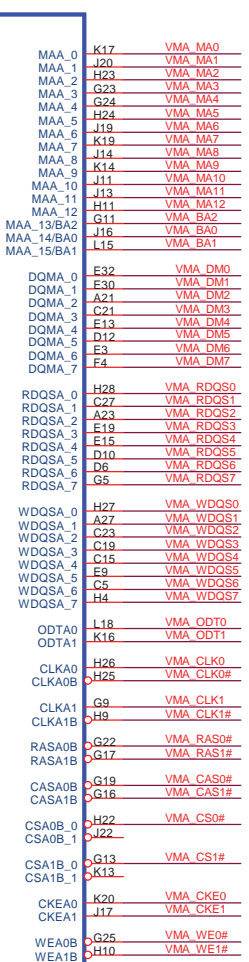
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



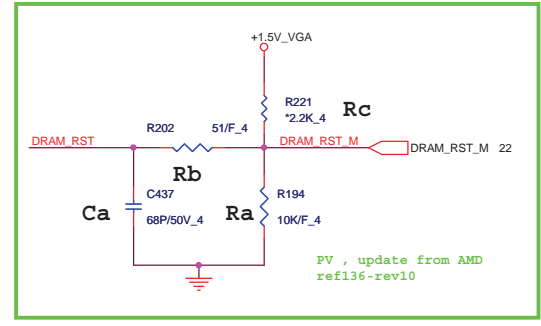
Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
 Note 2 :For M9X-S2/S3, J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
 For Park-S3, J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
 Note 3 :For M9X-92/93, K7 Pin (NC MEM_CALRP1) is Not connected.
 For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24



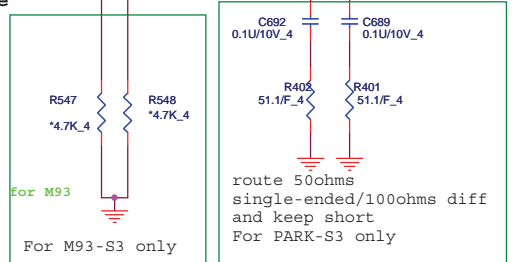
MEMORY INTERFACE



Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF



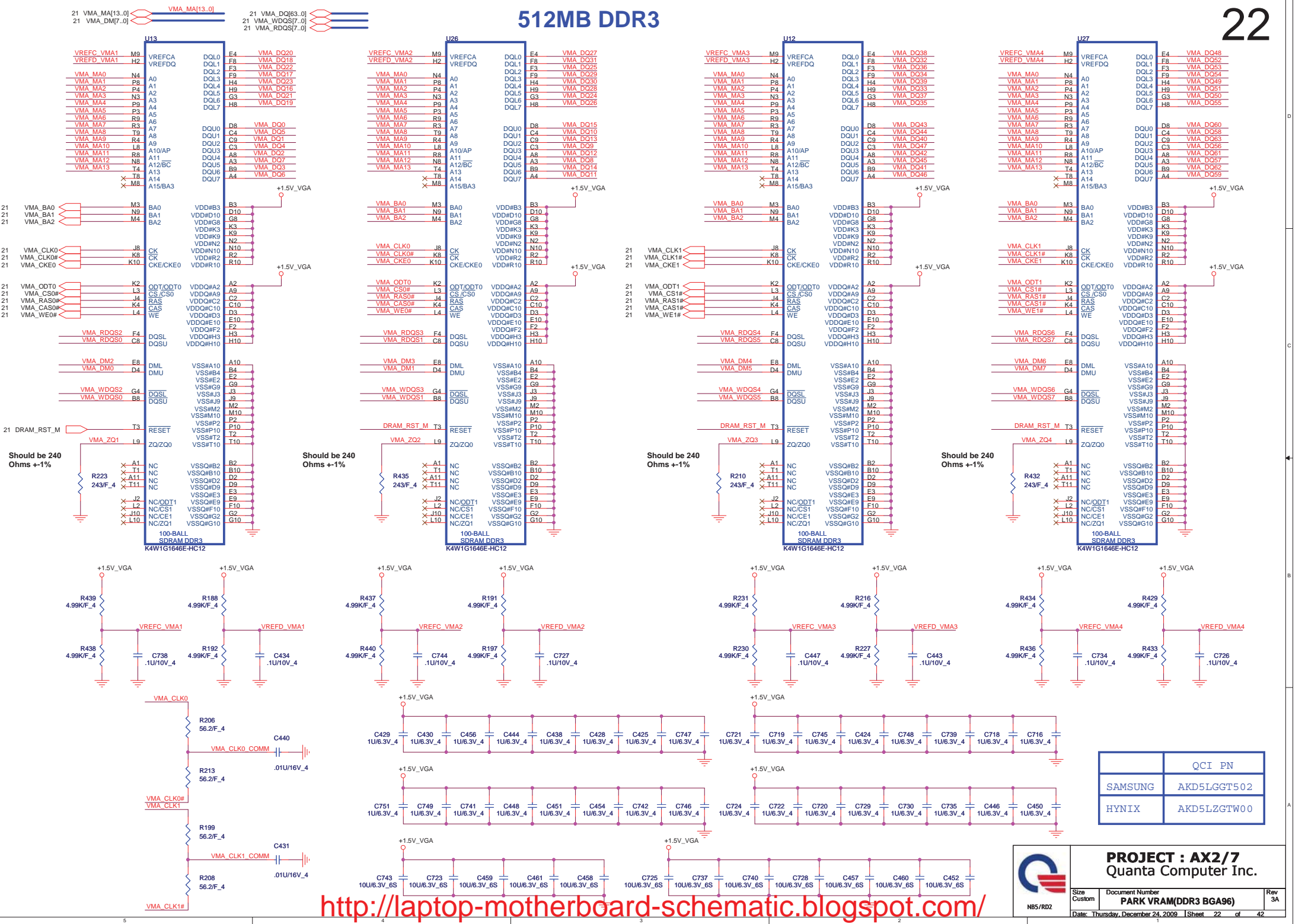
For PARK-S3 only
 For M9X-S2/S3 with DDR3: this pin is not in use.



PROJECT : AX2/7
 Quanta Computer Inc.

Size Custom	Document Number PARK/MEM_Interface	Rev 1A
Date: Thursday, December 24, 2009 Sheet 21 of 42		

512MB DDR3



	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

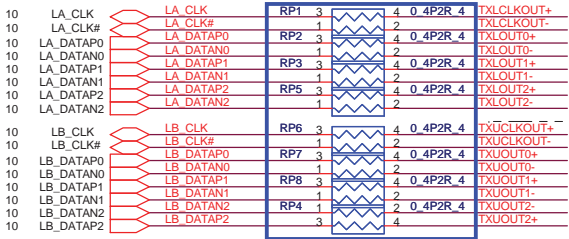
PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
	PARK VRAM(DDR3 BGA96)	
Date: Thursday, December 24, 2009	Sheet 22	of 42

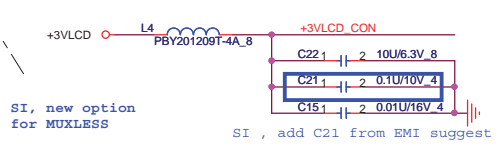
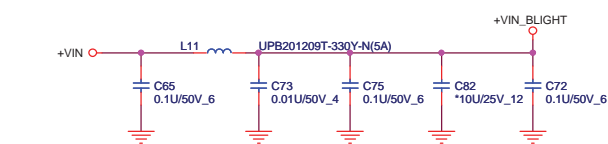
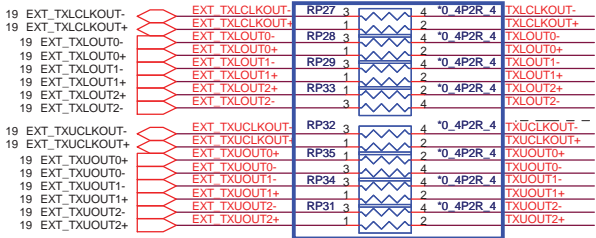
NBS/RDZ

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

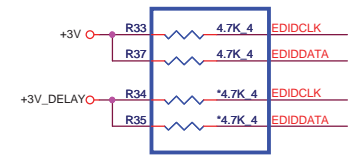


OPTION SIGNAL FROM PARK to LVDS for discrete

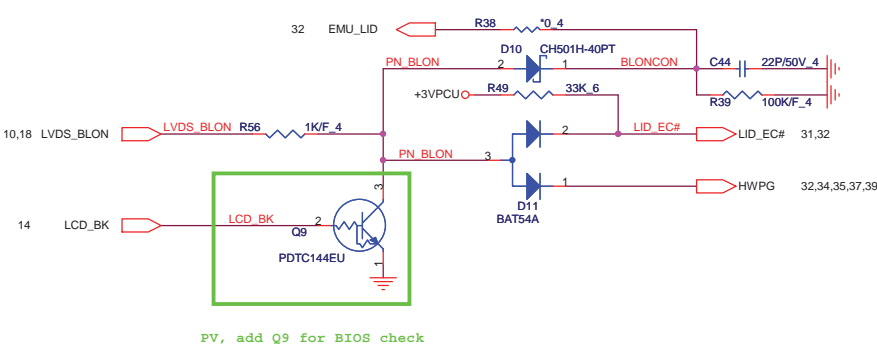
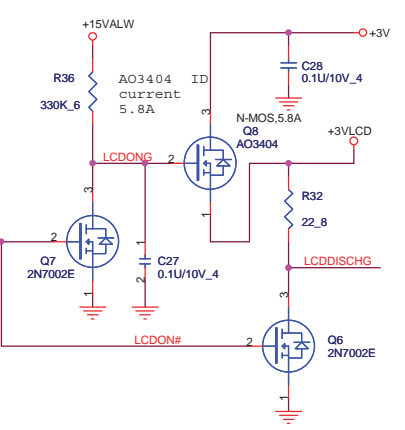


SI, new option for MUXLESS

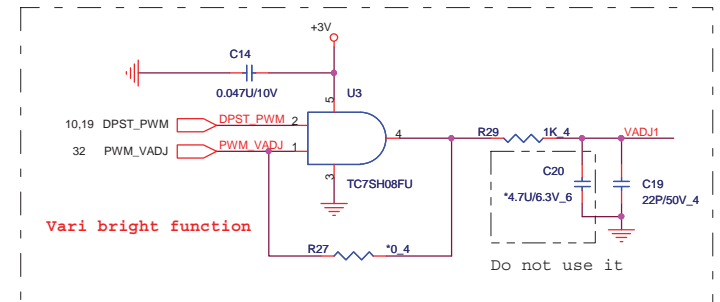
SI, add C21 from EMI suggest



SI, R34,R35 change to reserve only and add R33,R37 for MUXLESS

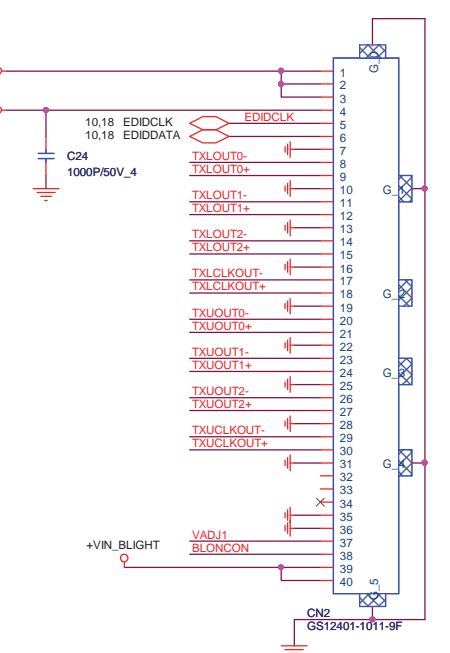


PV, add Q9 for BIOS check

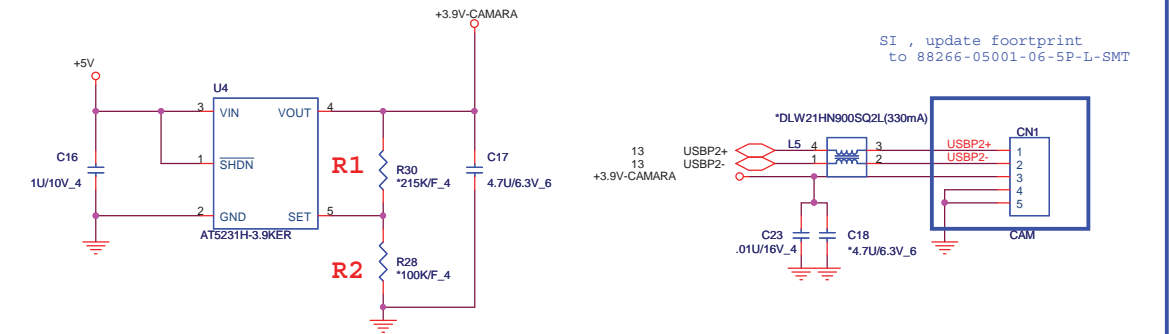


Vari bright function

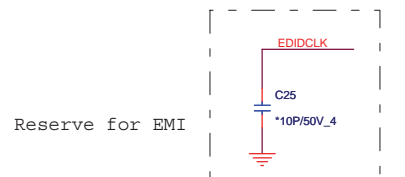
Do not use it



CAMERA



SI, update footprint to 88266-05001-06-5P-L-SMT



Reserve for EMI

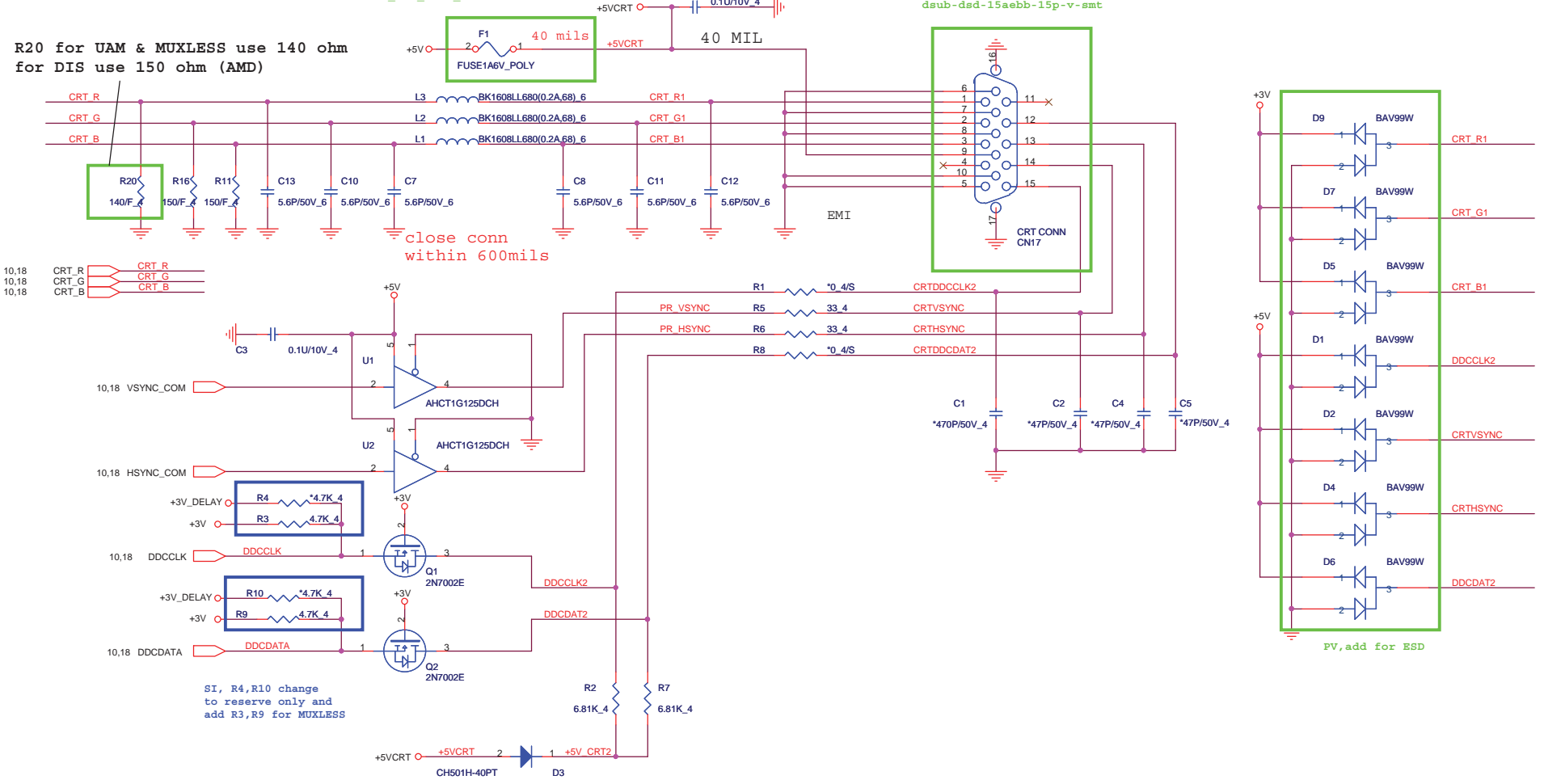
<p>PROJECT : AX2/7 Quanta Computer Inc.</p>		
Size Custom	Document Number LCD CONN	Rev 1A
Date: Thursday, December 24, 2009	Sheet 23 of 42	

CRT PORT

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)

PV , change footprint to F3_2X1_65-2_8

PV , change footprint to dsub-dsd-15aebb-15p-v-smt



- 10,18 CRT_R CRT R
- 10,18 CRT_G CRT G
- 10,18 CRT_B CRT B

SI, R4,R10 change to reserve only and add R3,R9 for MUXLESS

close conn within 600mils

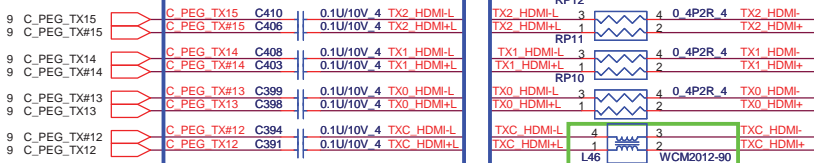
PV,add for BSD

	PROJECT : AX2/7 Quanta Computer Inc.	
	Size Custom	Document Number CRT
Date: Thursday, December 24, 2009		Rev 1A
Sheet 24 of 42		

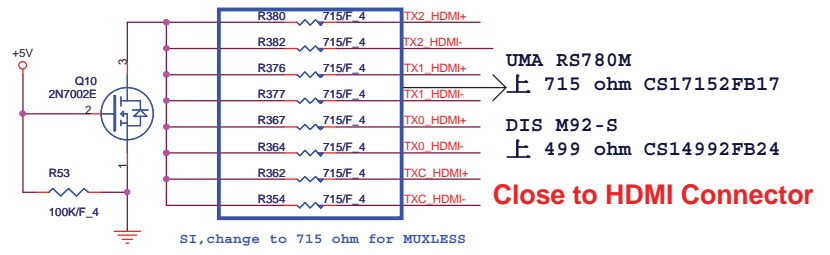
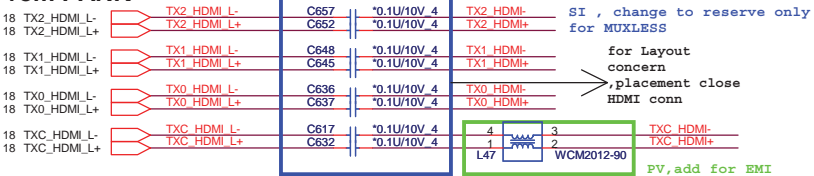
UMA/DISCRETE select for HDMI

From RS880M

SI, all add for MUXLESS

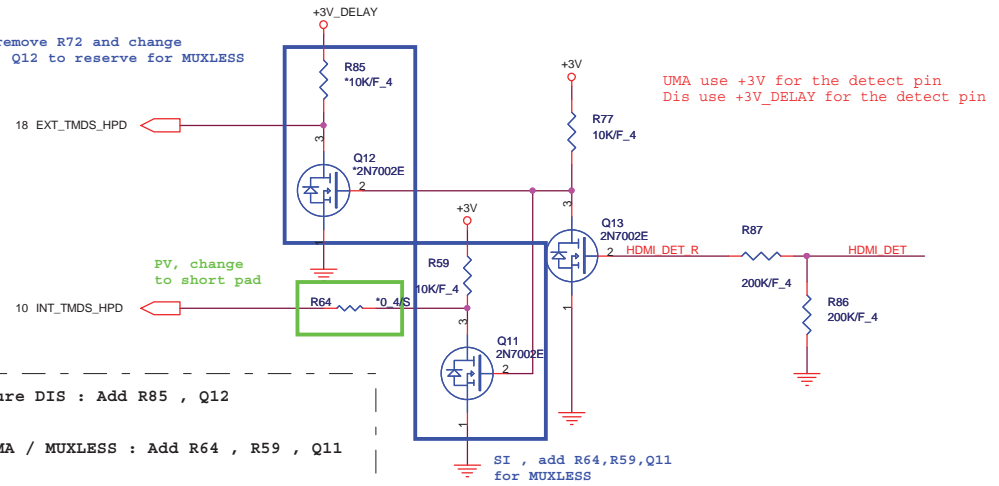


From PARK



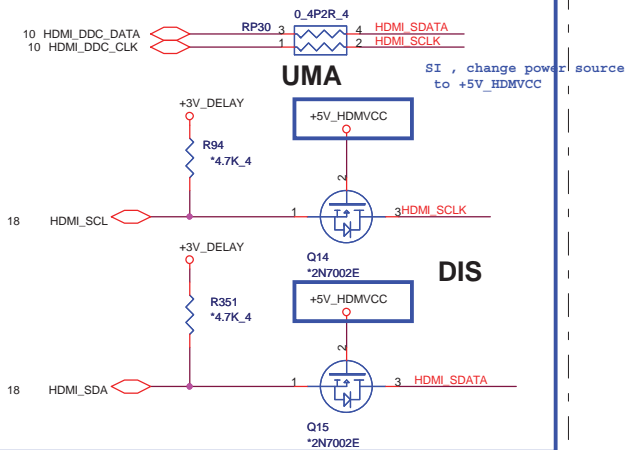
HDMI HPD SENSE

SI, remove R72 and change R85, Q12 to reserve for MUXLESS



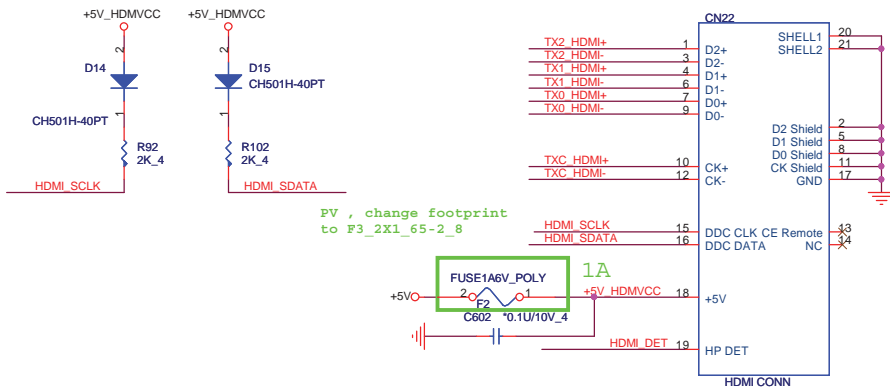
UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector



SI, remove R93, R350. Add RP30 R94, R351, Q14, Q15 change to reserve only for MUXLESS

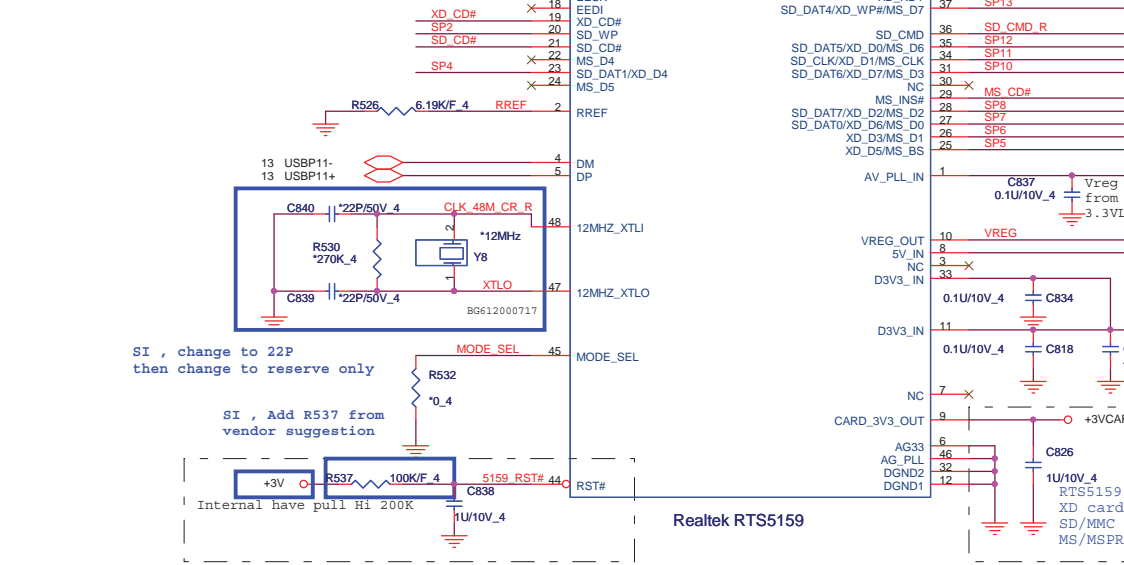
HDMI PORT



PROJECT : AX2/7
Quanta Computer Inc.

Size Custom	Document Number HDMI	Rev 1A
Date: Thursday, December 24, 2009	Sheet 25	of 42

PIN 13	CLK source	Remark
Floating	12M Hz	Xtal
Pull high	48M Hz	Input to RTS5159 pin48

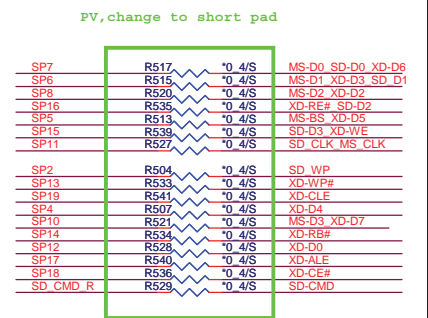


SI , change CLK source from SB internal CLK GEN

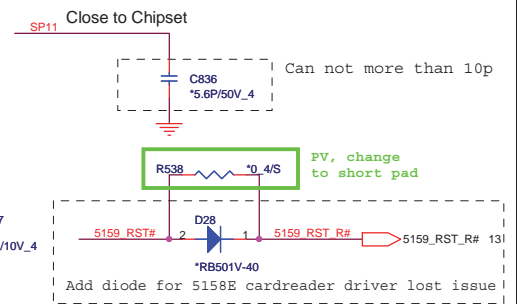
Note:

SD/MMC	MS	XD
SP1		XD_CD#
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	XD_D4
SP5	MS_BS	XD_D5
SP6	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9	MS_INS#	
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD_D0
SP13	SD_DAT4	XD_WP#
SP14		XD_R/#
SP15	SD_DAT3	XD_WE#
SP16	SD_DAT2	XD_RE#
SP17		XD_ALE
SP18		XD_CE#
SP19		XD_CLE

AL005158B10 -->RTS5158E
AL005159B00 -->RTS5159GR



PV, change to short pad

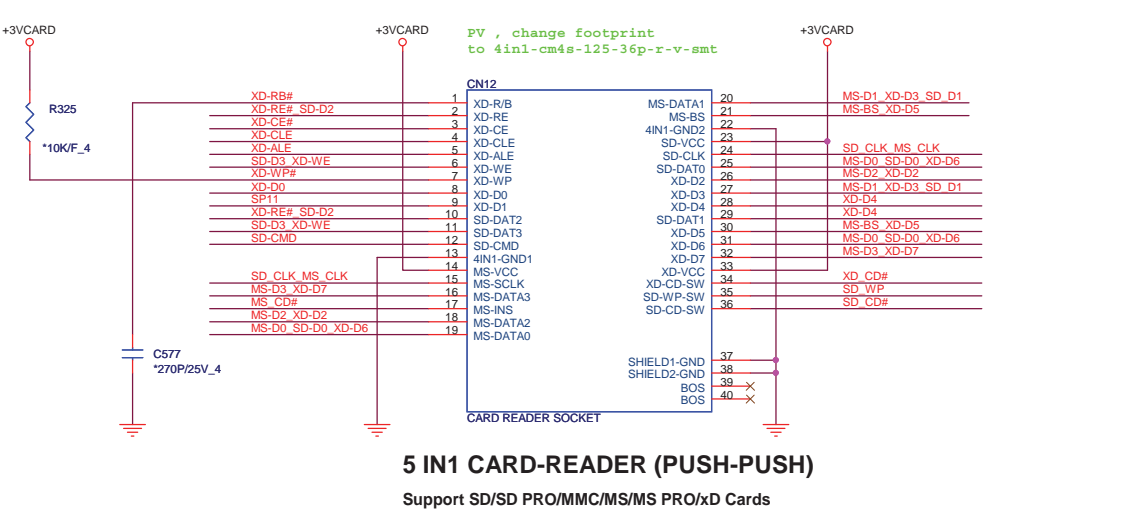


Close to Chipset

Can not more than 10p

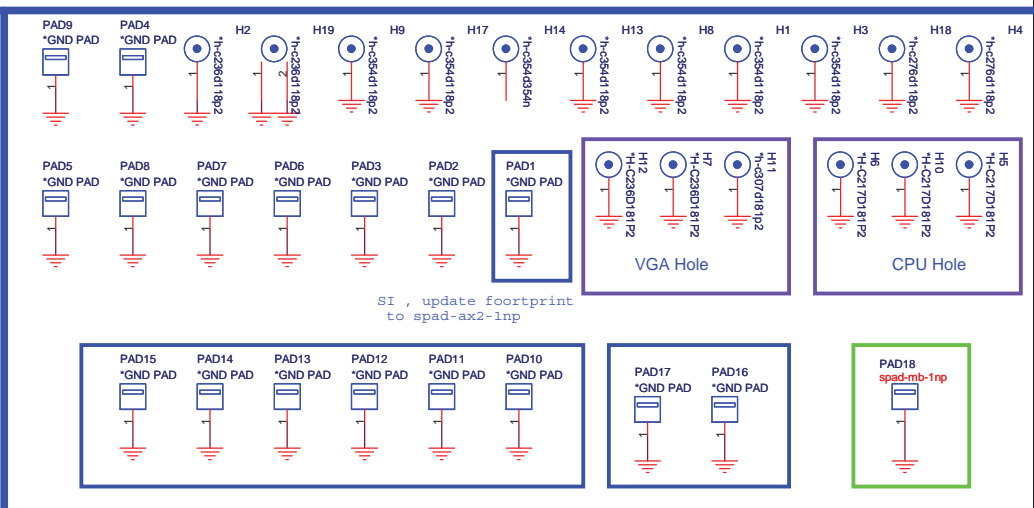
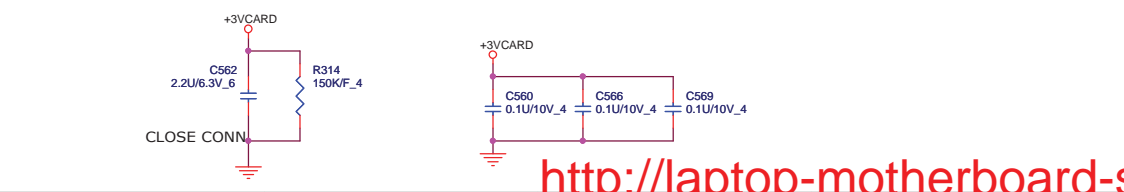
PV, change to short pad

Add diode for 5158E cardreader driver lost issue



5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/XD Cards



SI, add CPU & VGA hold pad from EMI request

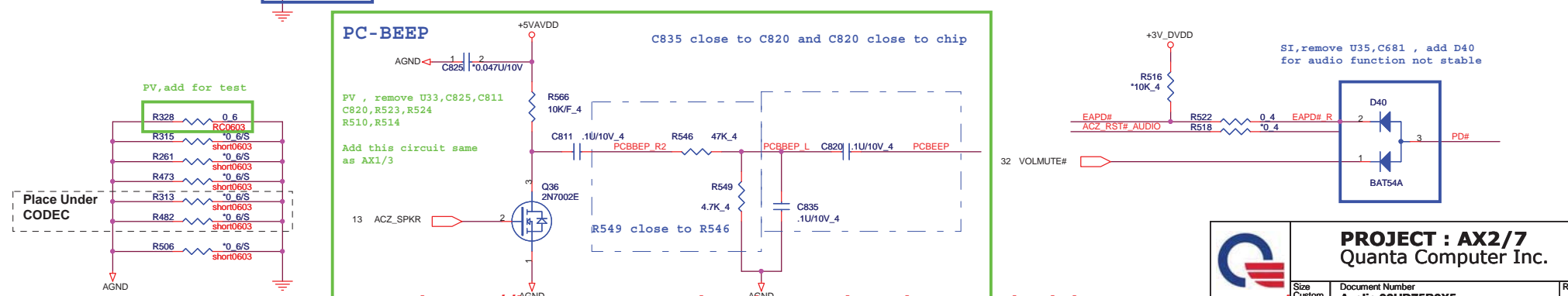
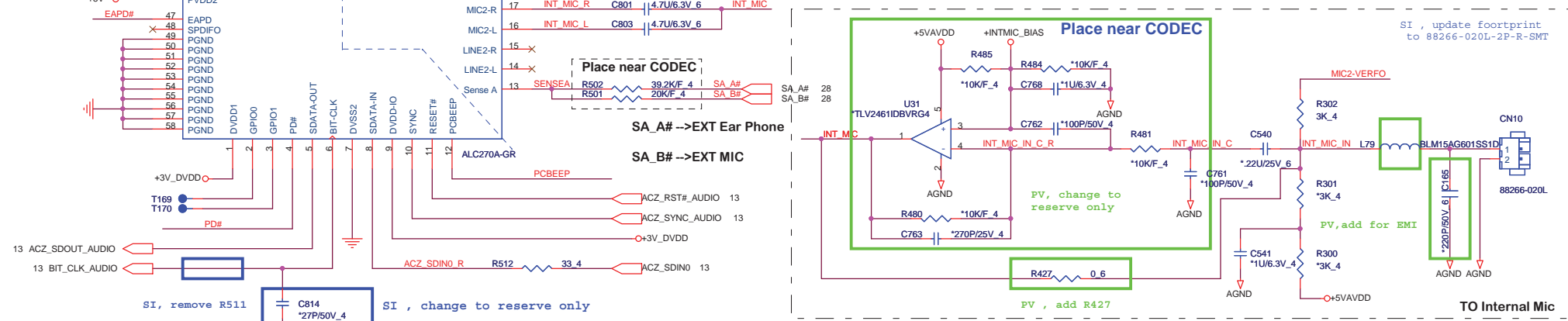
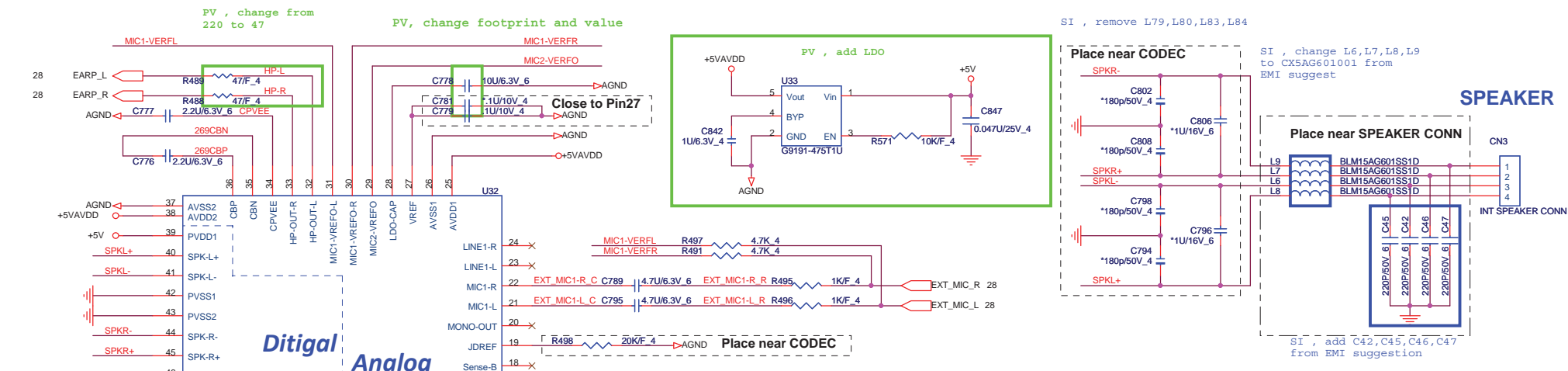
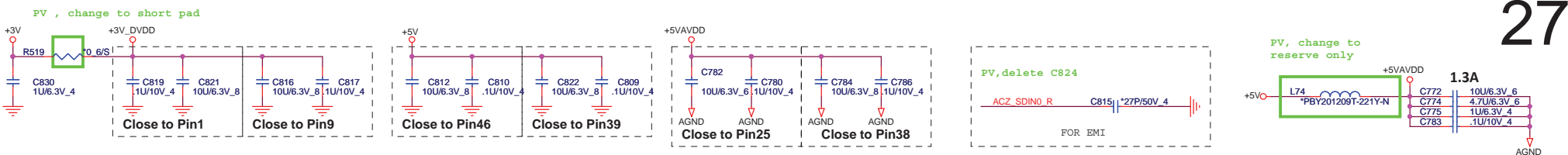
SI, add for ESD testing

PV, add new pad for new outline

PROJECT : AX2/7
Quanta Computer Inc.

Size Custom Document Number **RTS5159 & CR SOCKET & HOLE** Rev 1A

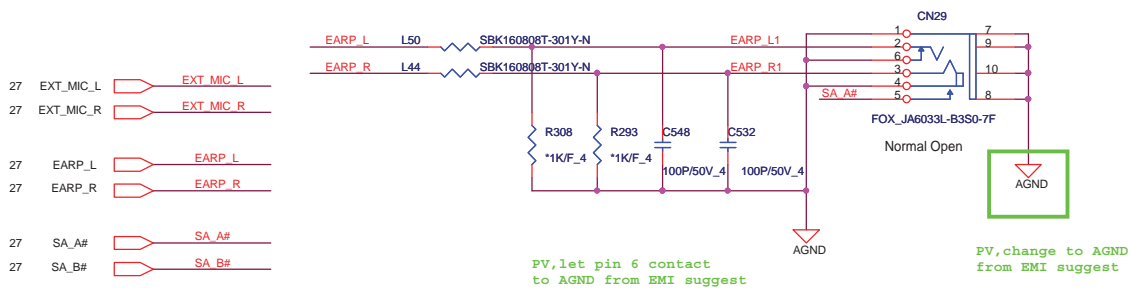
NB5/RD2 Date: Thursday, December 24, 2009 Sheet 26 of 42



PROJECT : AX2/7
 Quanta Computer Inc.

Size Custom	Document Number Azalia 92HD75B2X5	Rev 1A
Date: Thursday, December 24, 2009		Sheet 27 of 42

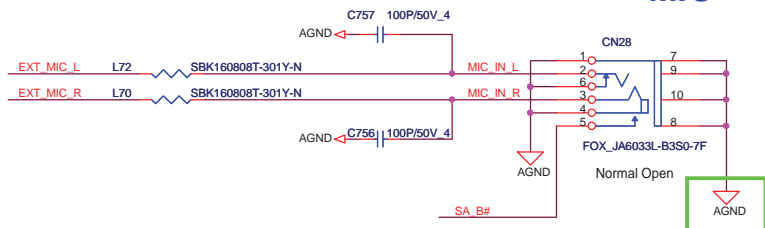
Line out



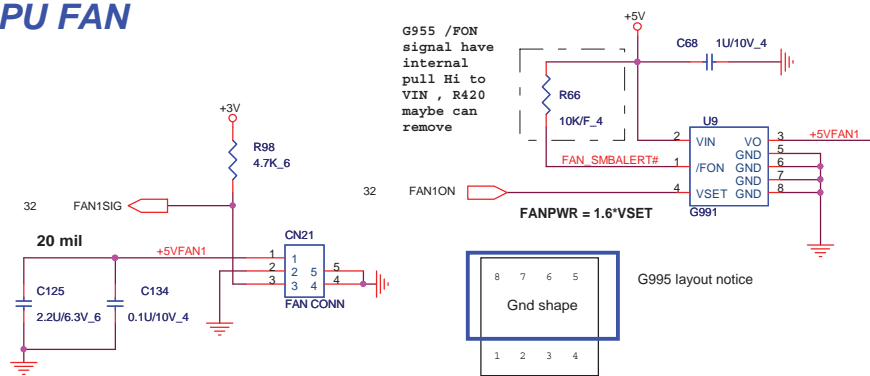
SA_A# -->EXT Ear Phone

SA_B# -->EXT MIC

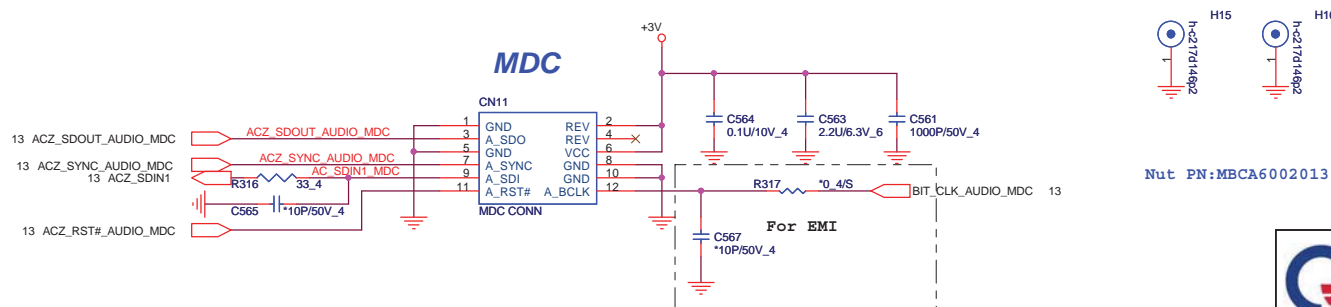
MIC



CPU FAN

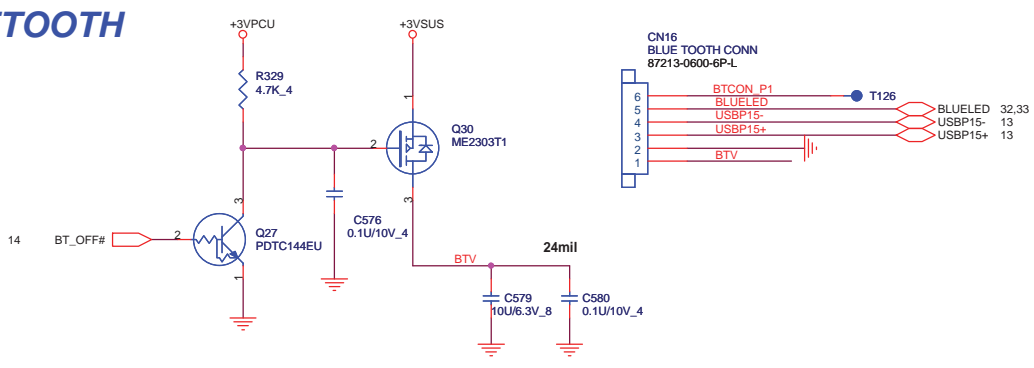


Modem CONN

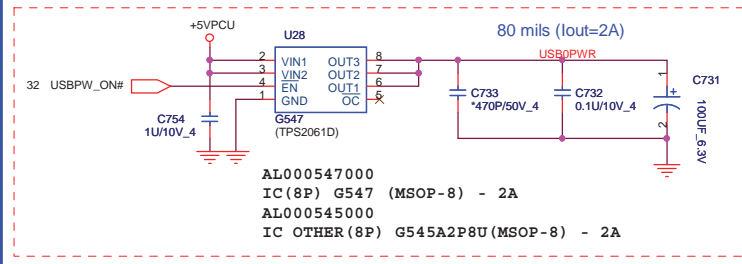


PROJECT : AX2/7 Quanta Computer Inc.		
Size Custom	Document Number AMP_TPA6017/MDC1.5/CPU FAN	Rev 1A
Date: Thursday, December 24, 2009		Sheet 28 of 42

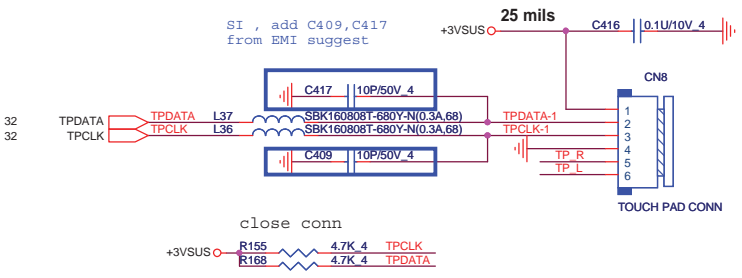
BLUETOOTH



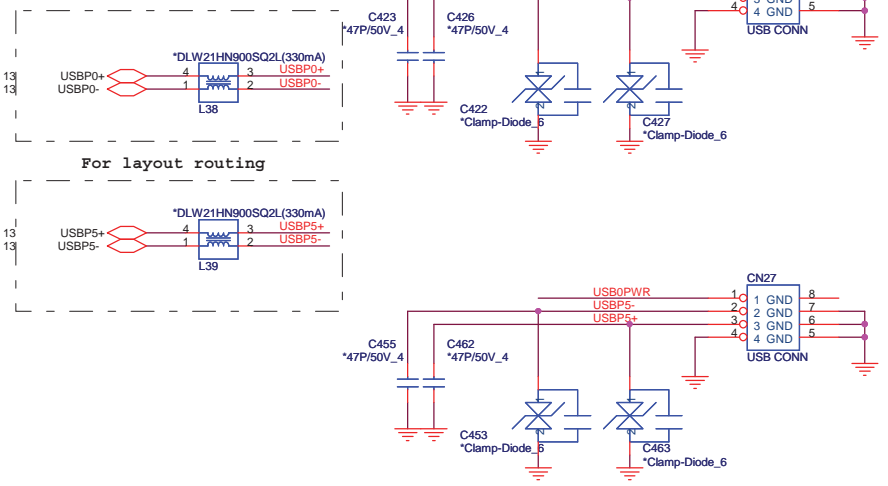
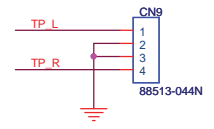
LEFT SIDE USBX2



TOUCH PAD CONN

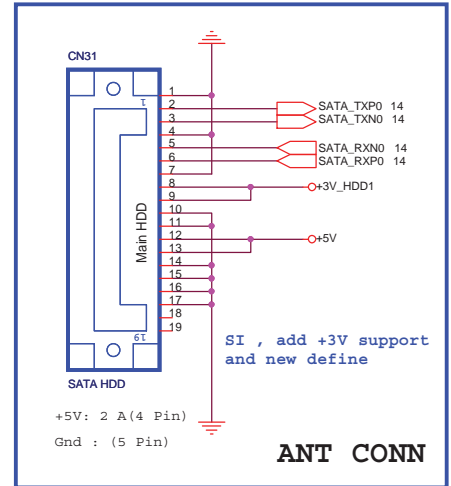
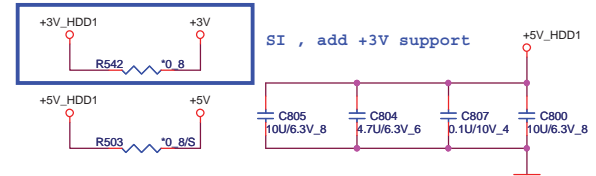


To TOUCH PAD SW board

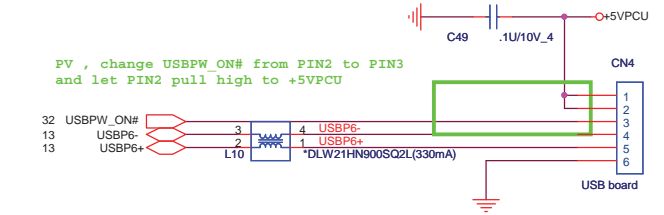


SATA HDD CONNECTOR

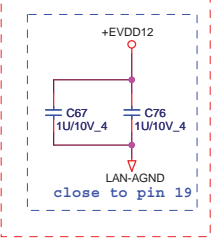
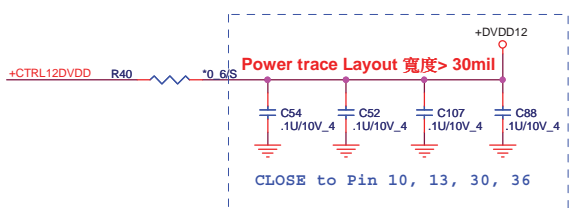
SI , update P/N : DFHS13FS019
 SI , delete CN30 change to ANT CONN



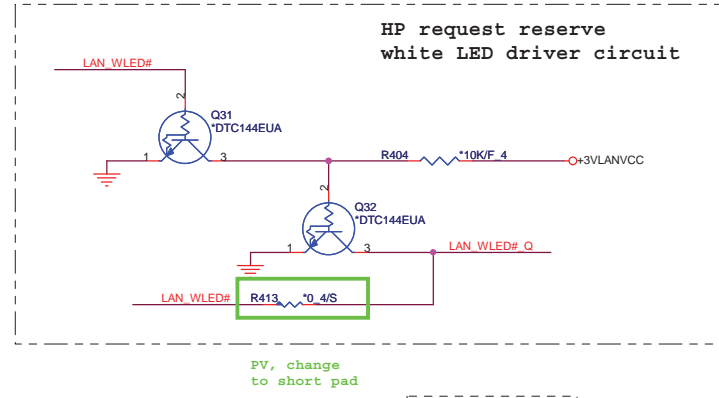
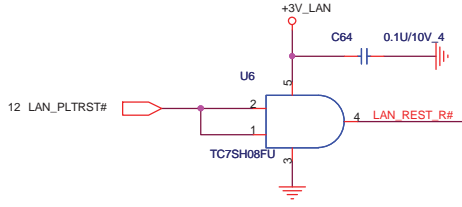
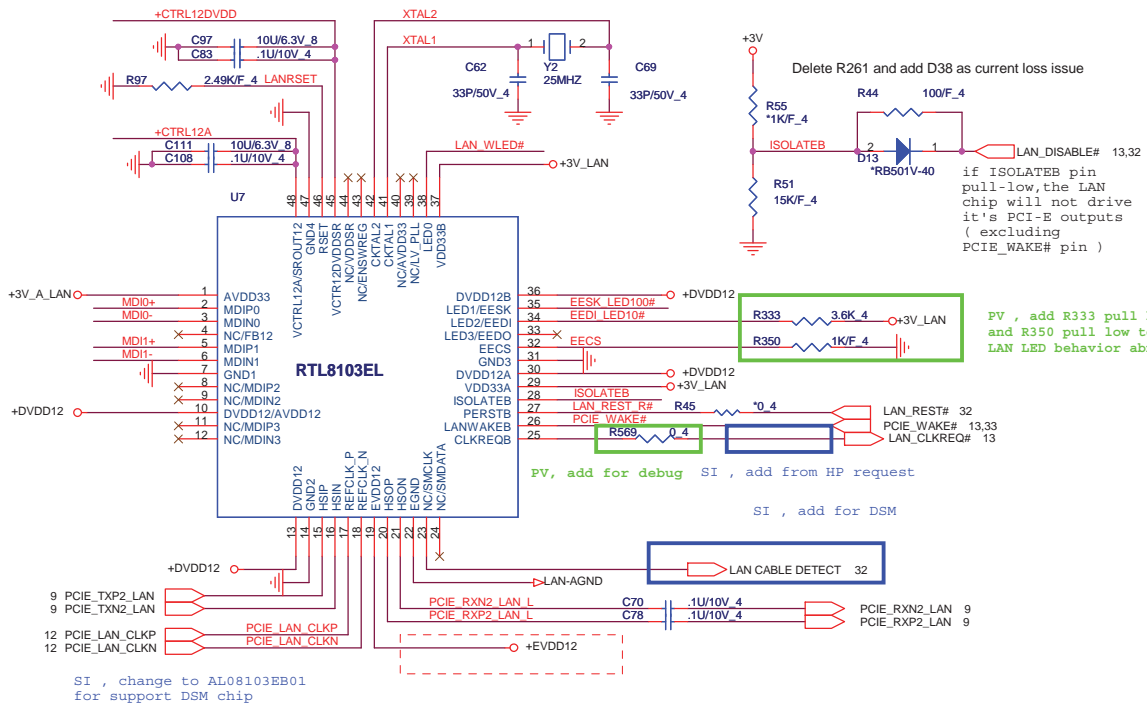
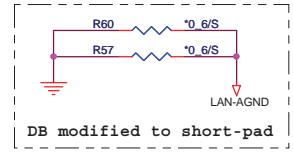
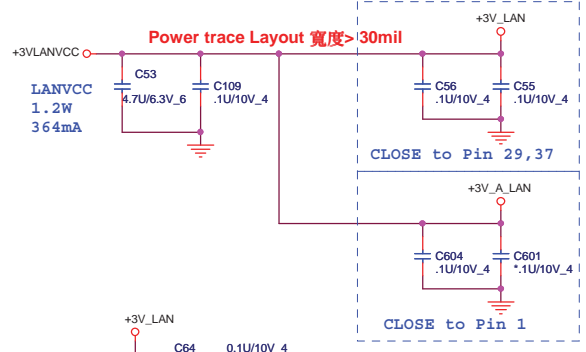
Right SIDE USBX1



PROJECT : AX2/7 Quanta Computer Inc.		
Size Custom	Document Number BT/USBX3/TP/HDD	Rev 1A
Date: Thursday, December 24, 2009 Sheet 29 of 42		

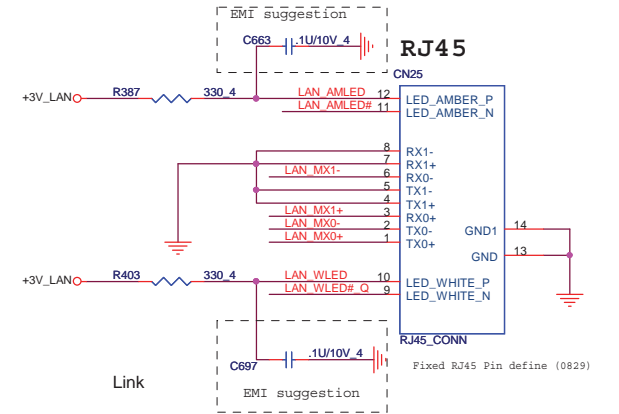
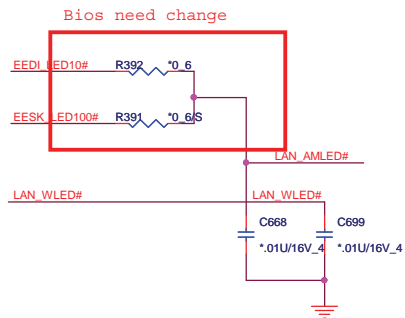
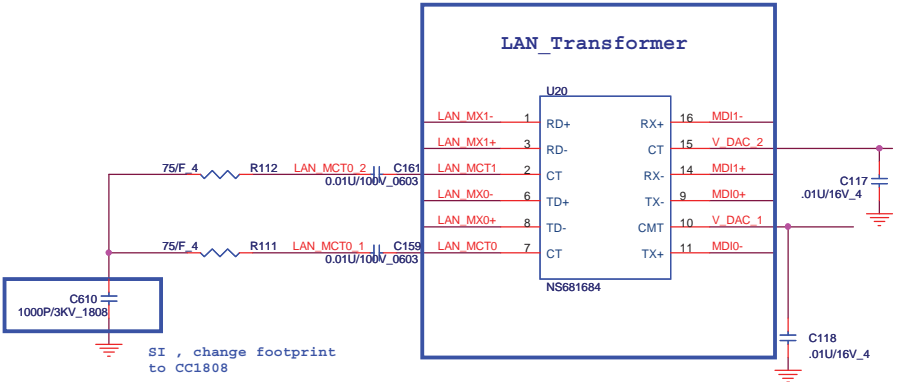


SI , remove EEPROM U5, C48, R42, R50



SI , rotate 180 degree for EMI suggestion

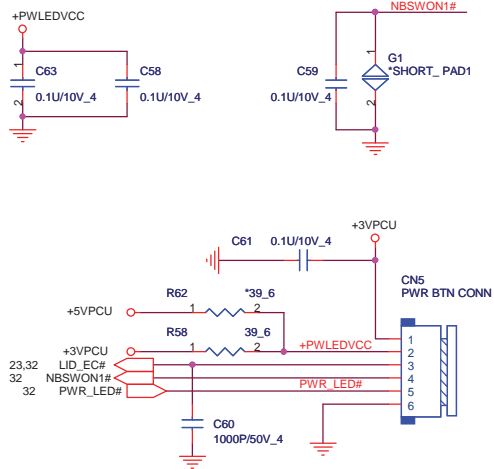
Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0 Tx Rs 00 01 10 11
LED1	O	56	35	LED1 LNK100 LNK LNK LNK LNK100
LED2	O	55	34	LED2 LNK10 FULL Rs LNK10
LED3	O	54	33	LED3 NA NA NA NA



PROJECT : AX2/7
 Quanta Computer Inc.

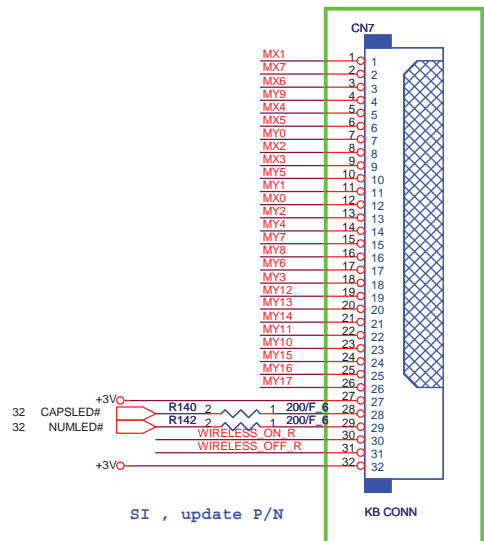
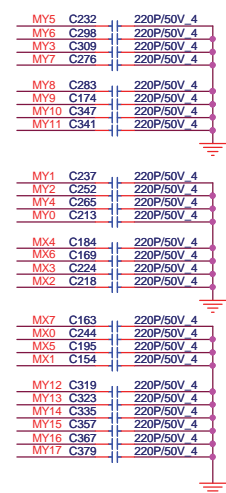
Size Custom	Document Number RTL8102EL/RJ45	Rev 1A
Date: Thursday, December 24, 2009	Sheet 30	of 42

POWER BUTTON CONNECTOR

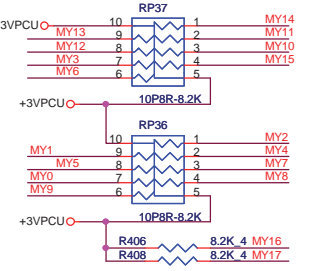


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

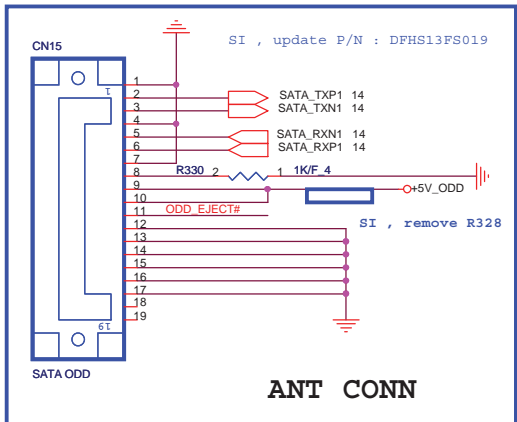
KEYBOARD CONN



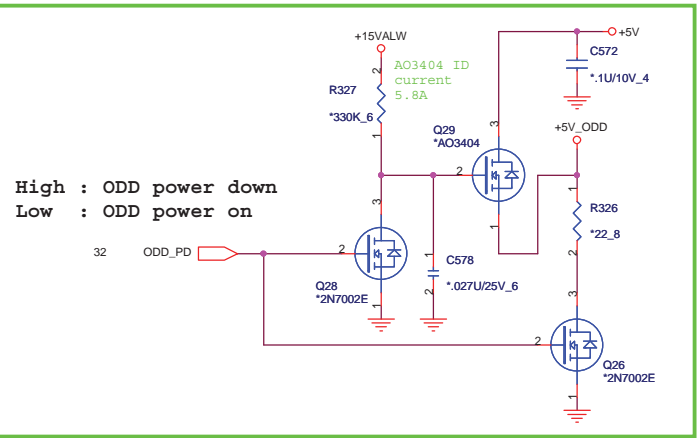
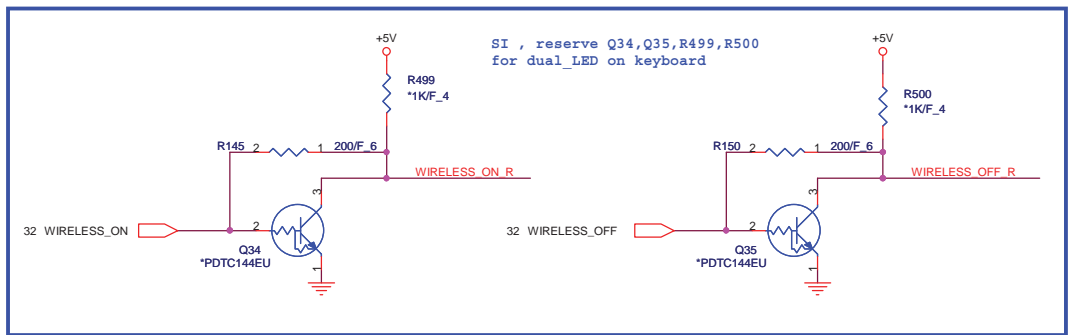
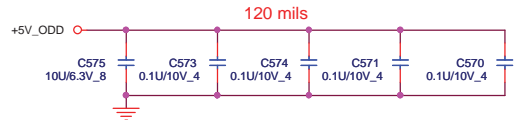
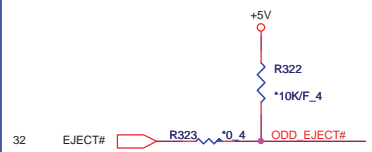
KEYBOARD PULL-UP



SATA CD-ROM



SI, delete CN13 change to ANT CONN

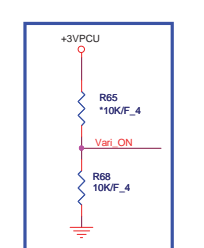
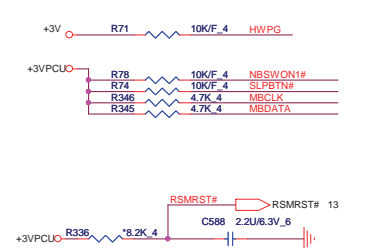
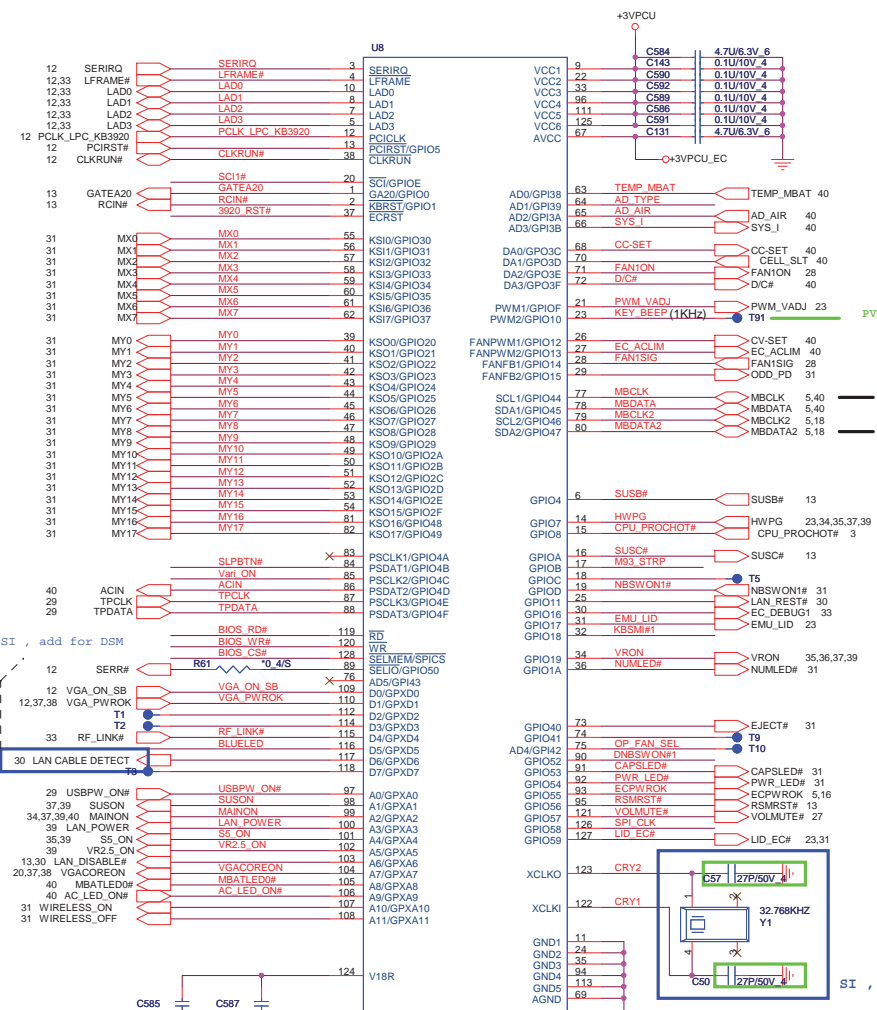


High : ODD power down
Low : ODD power on

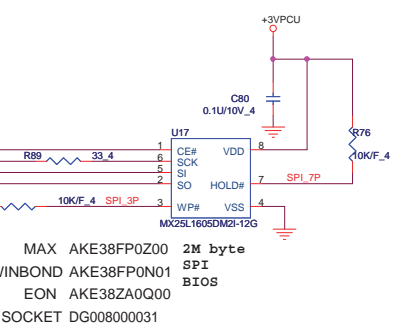
PV, change to reserve only

PROJECT : AX2/7
Quanta Computer Inc.

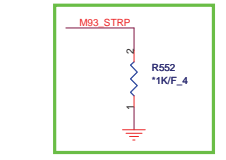
Size Custom	Document Number KEYBOARD/SW_BOARD/ODD	Rev 1A
Date: Thursday, December 24, 2009		Sheet 31 of 42



SI , enable Vari-bright need pull low



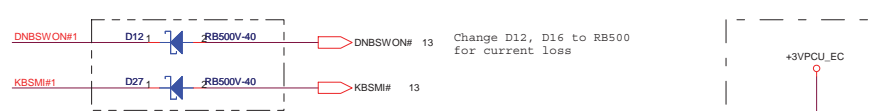
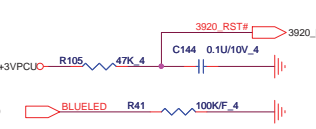
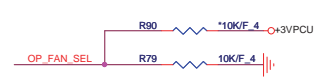
MAX AKE38FP0Z00 2M byte SPI BIOS
 WINBOND AKE38FP0N01 EON AKE38ZA0Q00 SOCKET DG08000031



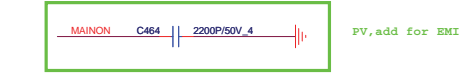
PV.reserve for identify M93-LP VGA chip

Project Model	GPIO42
AX 14 "	High
AX 15.6 "	Low
AX 17.3 "	Middle (1.5V)

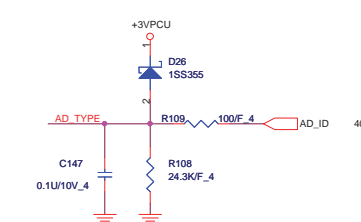
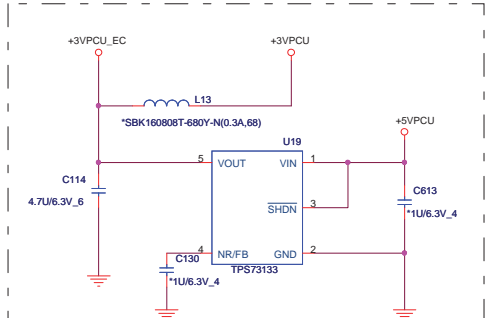
GPIO42 control fan table



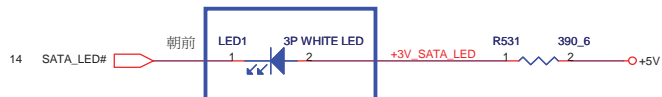
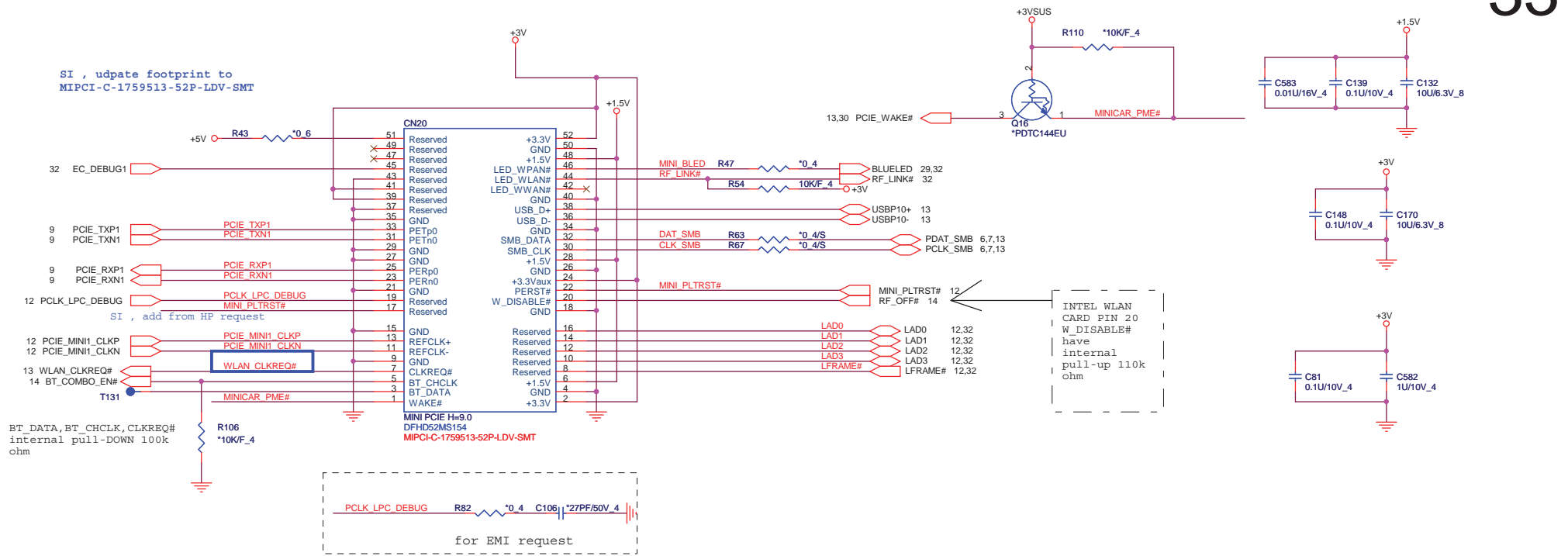
Change D12, D16 to RB500 for current loss



PV,add for EMI



Mini PCI-E Card 1 WLAN

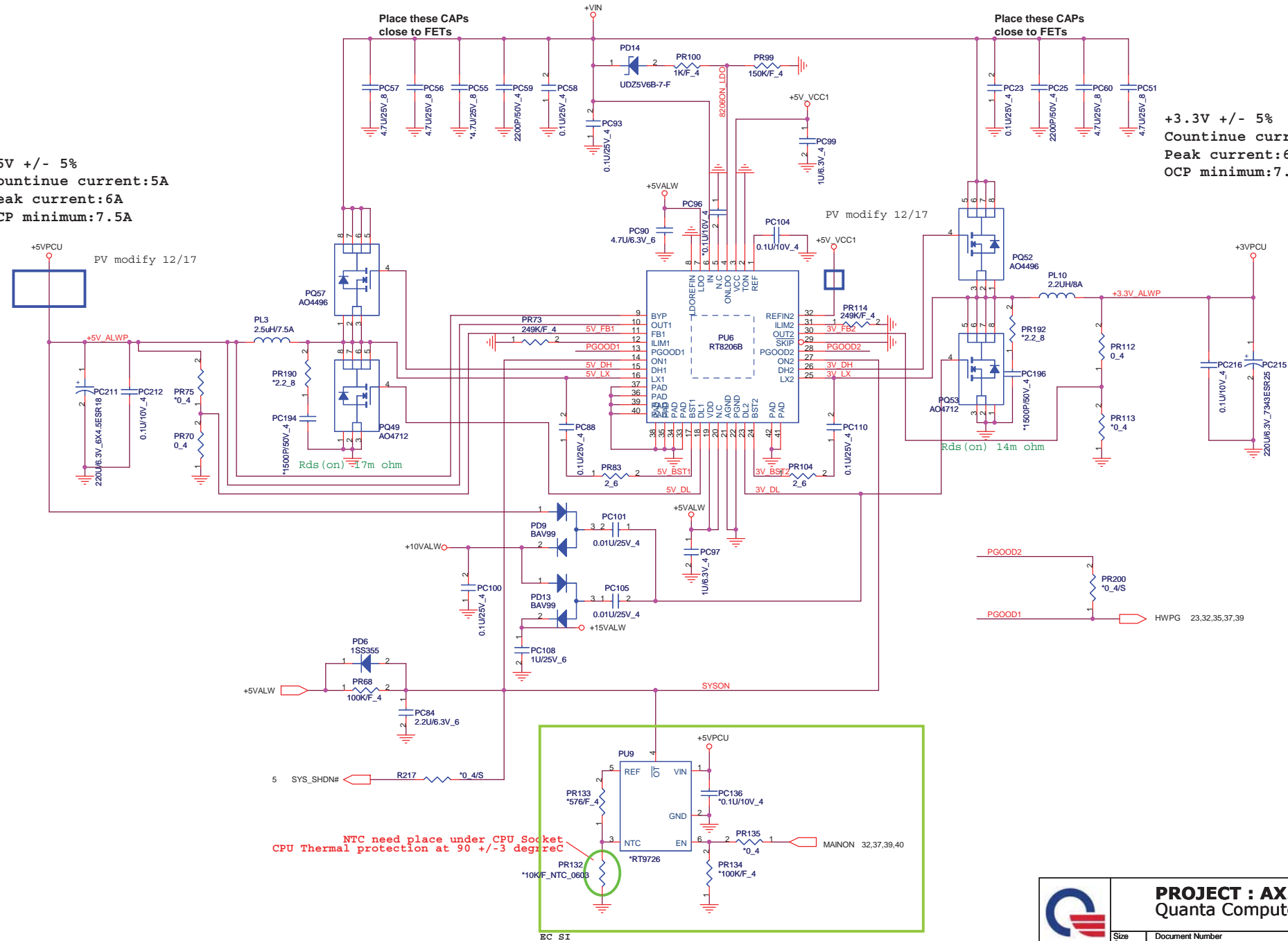


SI, change footprint to led1-s110kgct-3p-nb5

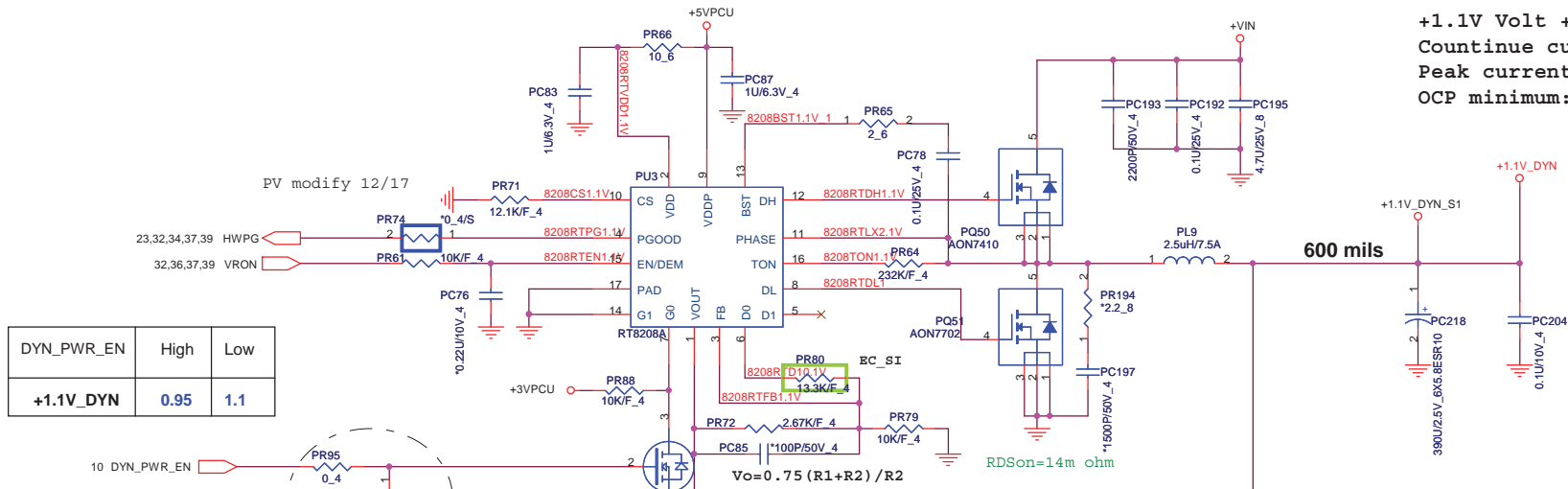
PROJECT : AX2/7 Quanta Computer Inc.		
Size Custom	Document Number Mini CARD/LED	Rev 1A
Date: Thursday, December 24, 2009 Sheet 33 of 42		

+5V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum:7.5A

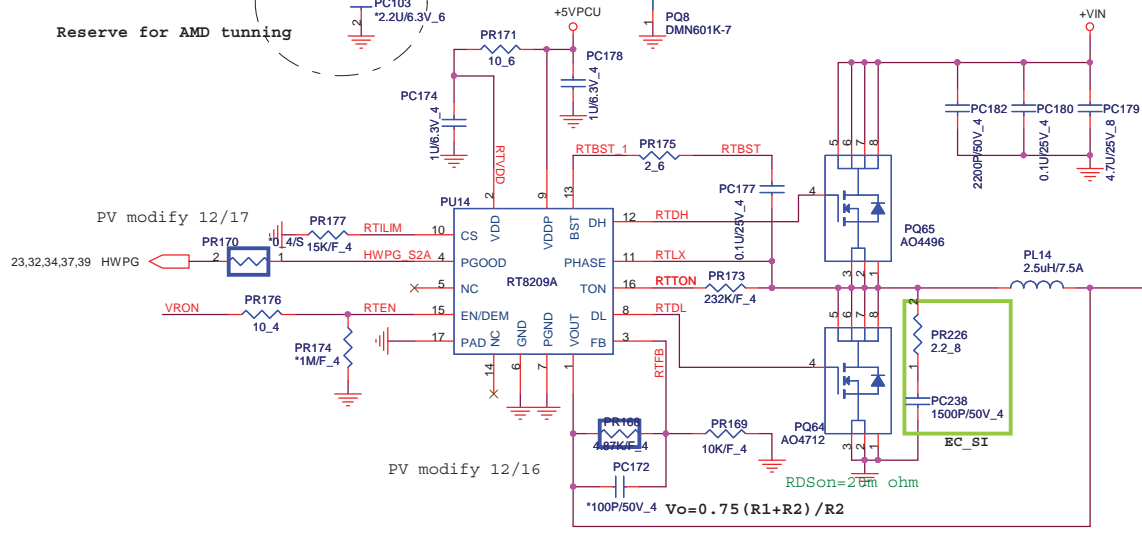
+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum:7.5A



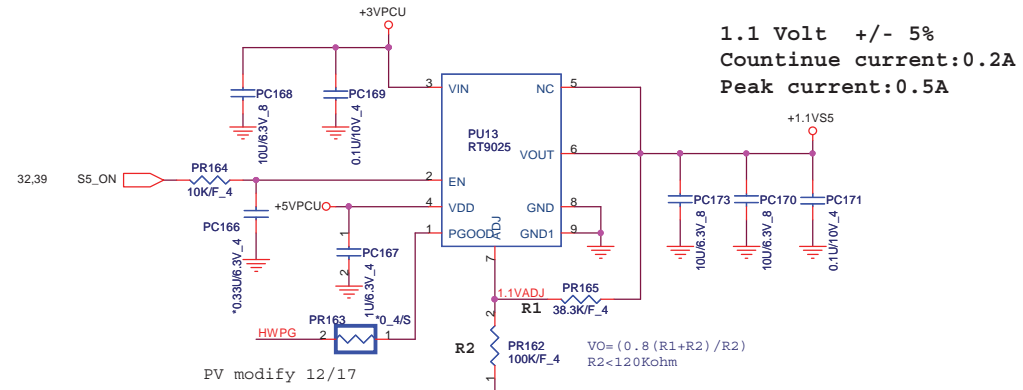
	PROJECT : AX2/7 Quanta Computer Inc.	
	Size Custom Document Number +5V/+3V (RT8206B) Date: Thursday, December 24, 2009 Sheet 34 of 42	Rev 1A



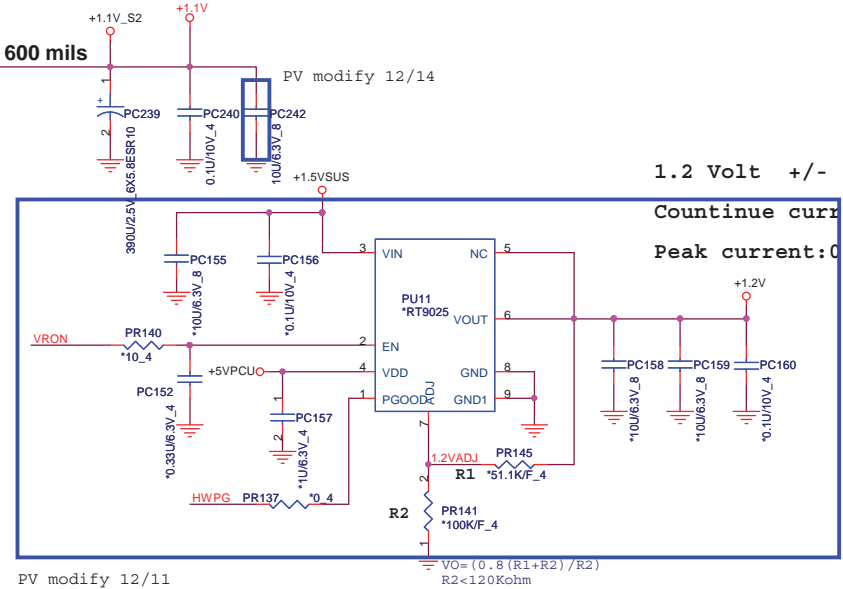
+1.1V Volt +/- 5%
 Countinue current:5A
 Peak current: 7A
 OCP minimum: 9A




+1.1V Volt +/- 5%
 Countinue current:5A
 Peak current: 7A
 OCP minimum: 9A



1.1 Volt +/- 5%
 Countinue current:0.2A
 Peak current:0.5A



1.2 Volt +/- 5%
 Countinue current:0.3A
 Peak current:0.5A



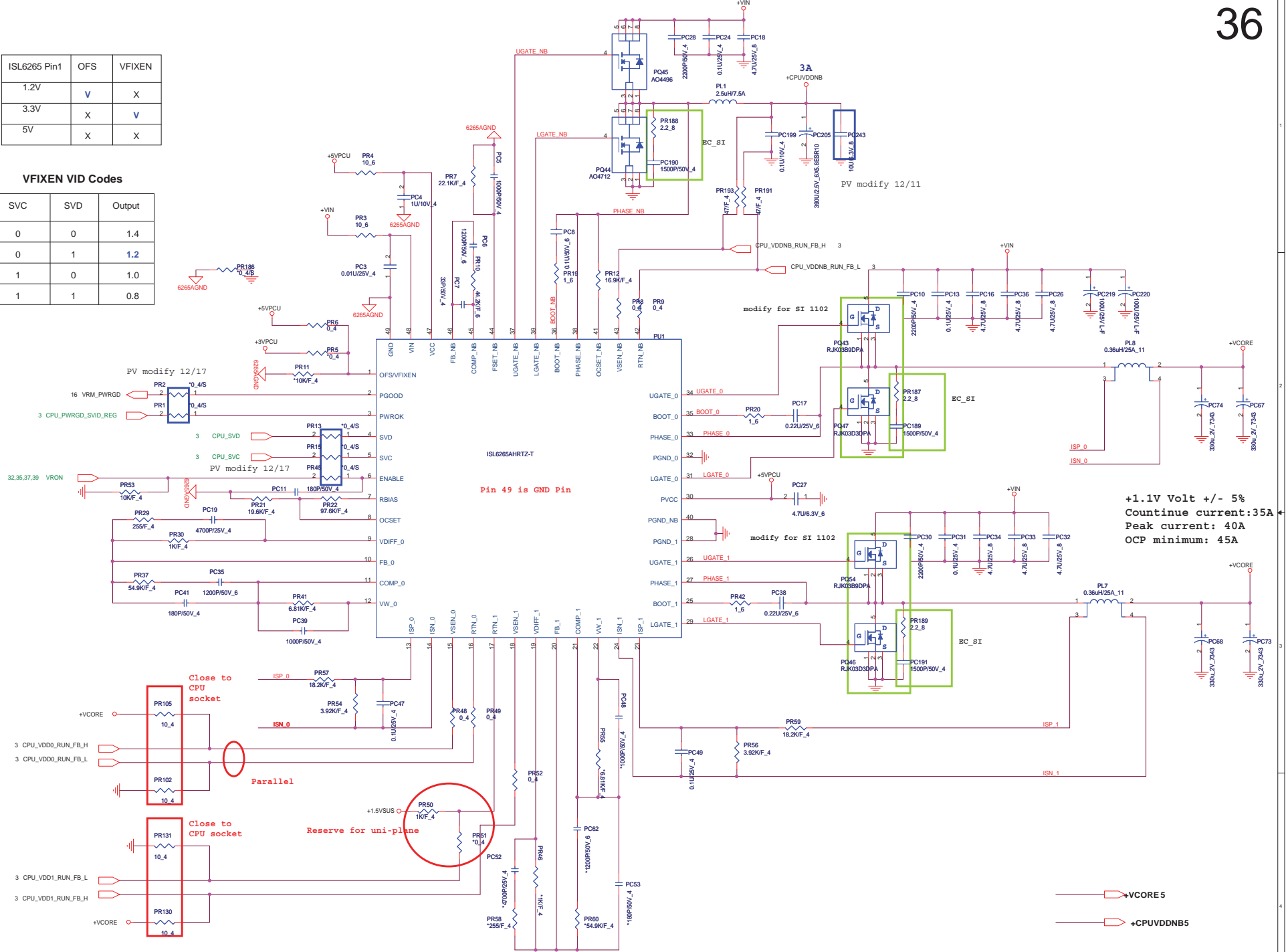
PROJECT : AX2/7
 Quanta Computer Inc.

Size Custom	Document Number VGA Core/4.8VGFHX/1.0VGFHX	Rev 1A
Date: Thursday, December 24, 2009 Sheet 35 of 42		

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

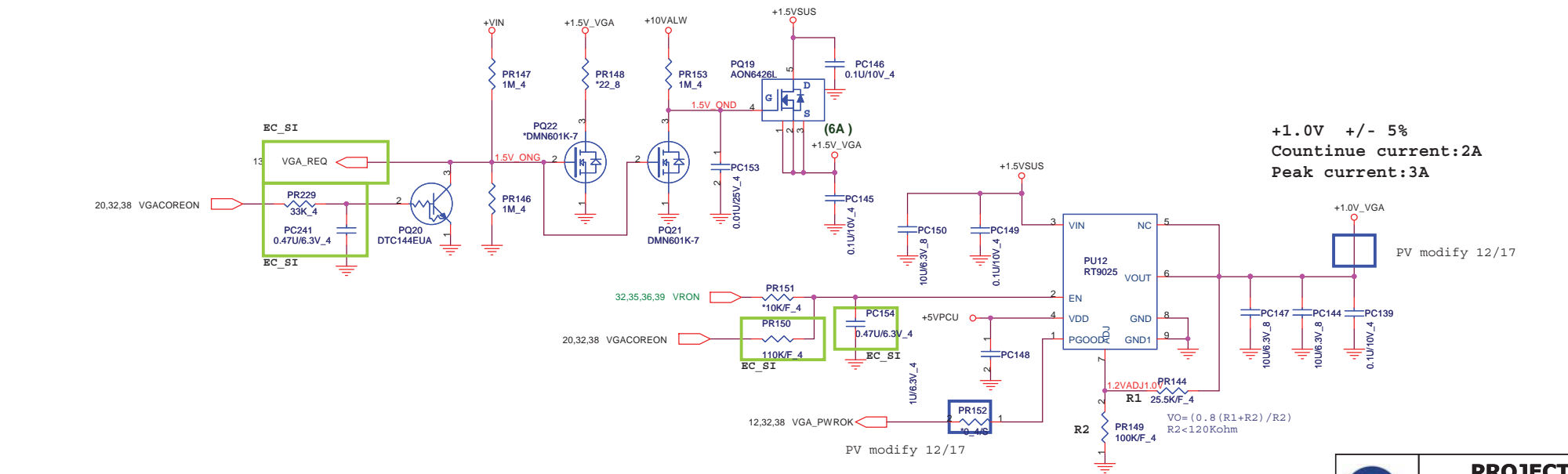
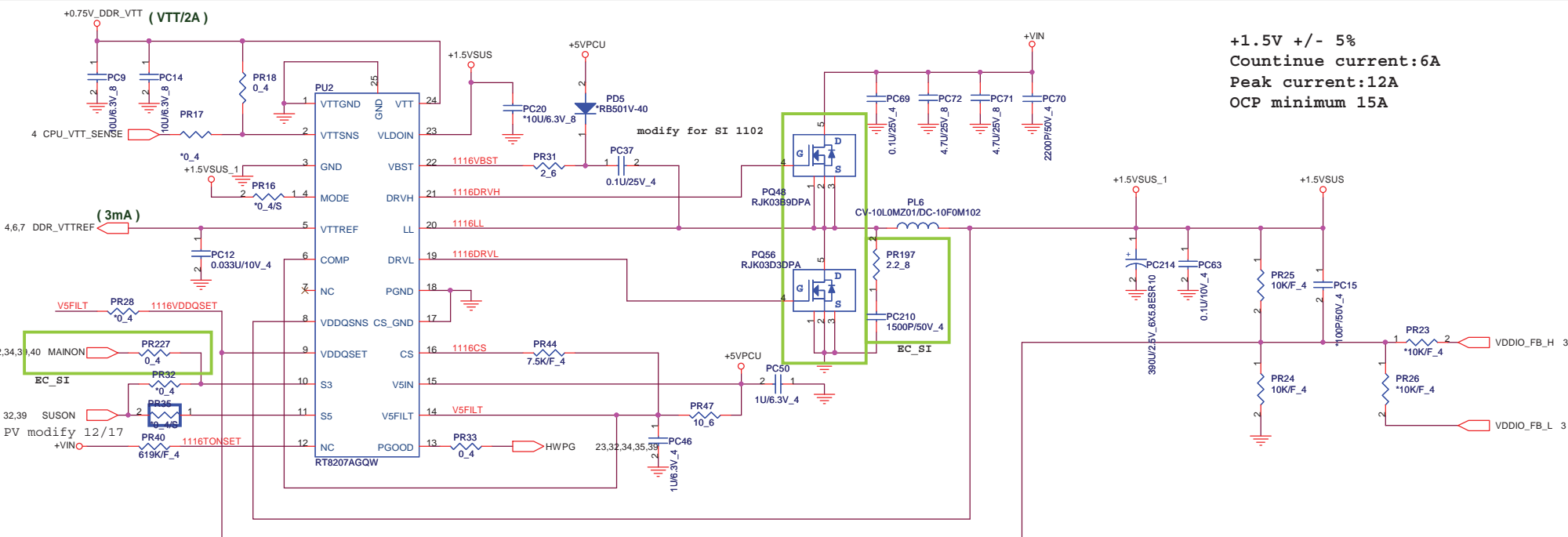
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8




+1.1V Volt +/- 5%
 Continue current: 35A
 Peak current: 40A
 OCP minimum: 45A

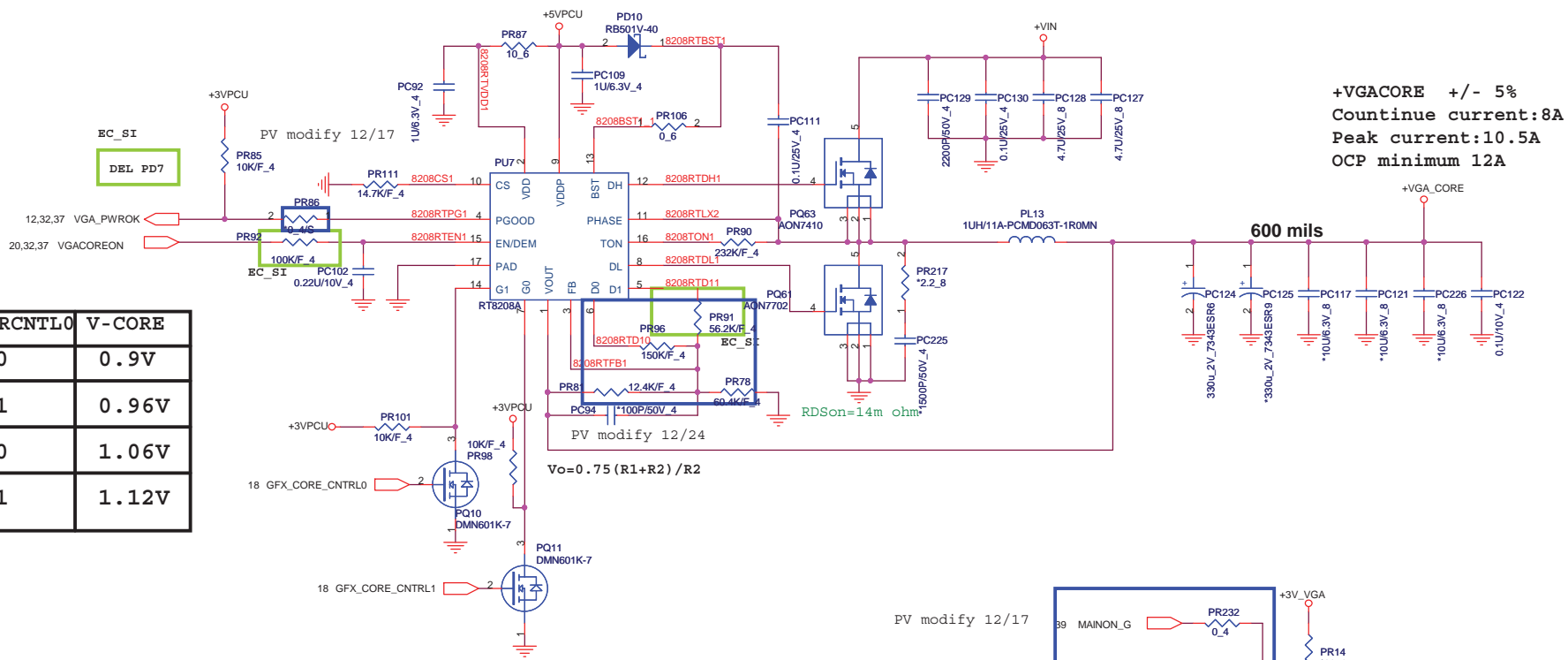
+VCORE5
 +CPUVDDNB5

	PROJECT : AX2/7 Quanta Computer Inc.	
	Size C Document Number CPU_CORE(ISL6265)	Rev 1A
Date: Thursday, December 24, 2009		Sheet 36 of 42

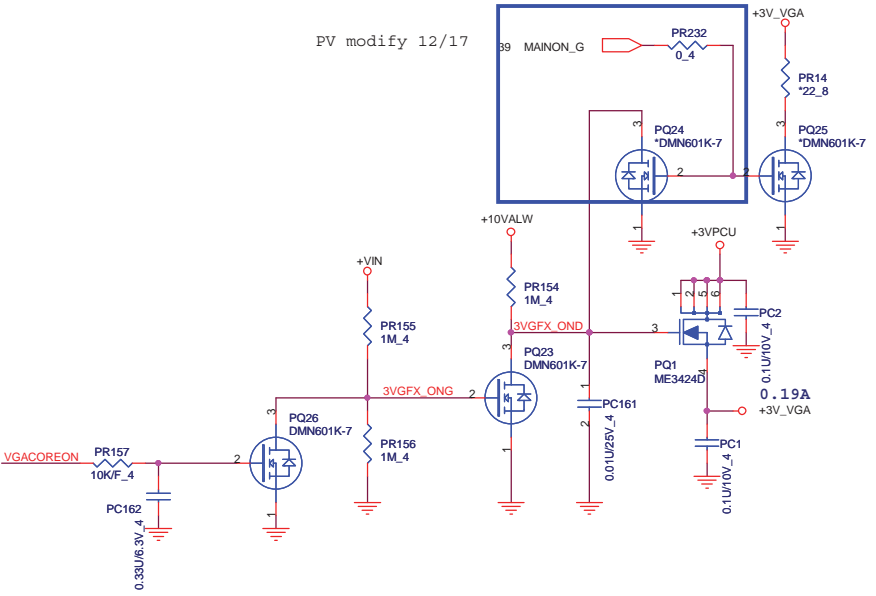
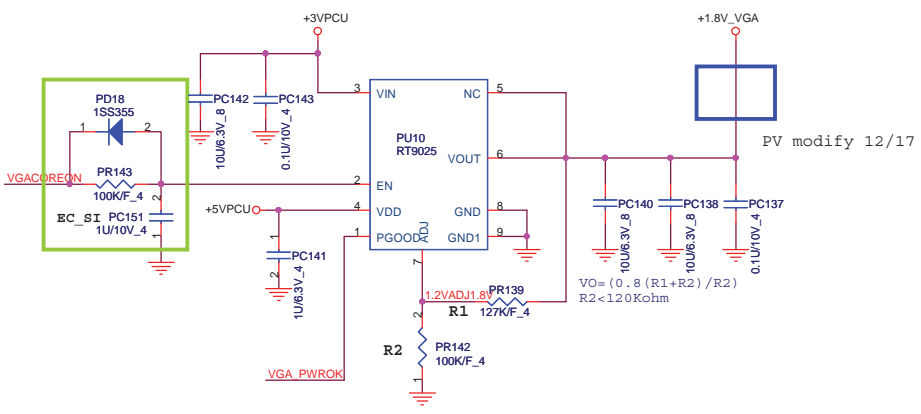


 NB5/RD2	PROJECT : AX2/7 Quanta Computer Inc. SANTOS INTEL	
	Size Document Number DDR3 (RT8207)	Date: Thursday, December 24, 2009 Sheet 37 of 42

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.96V
H	1	0	1.06V
TBD	1	1	1.12V



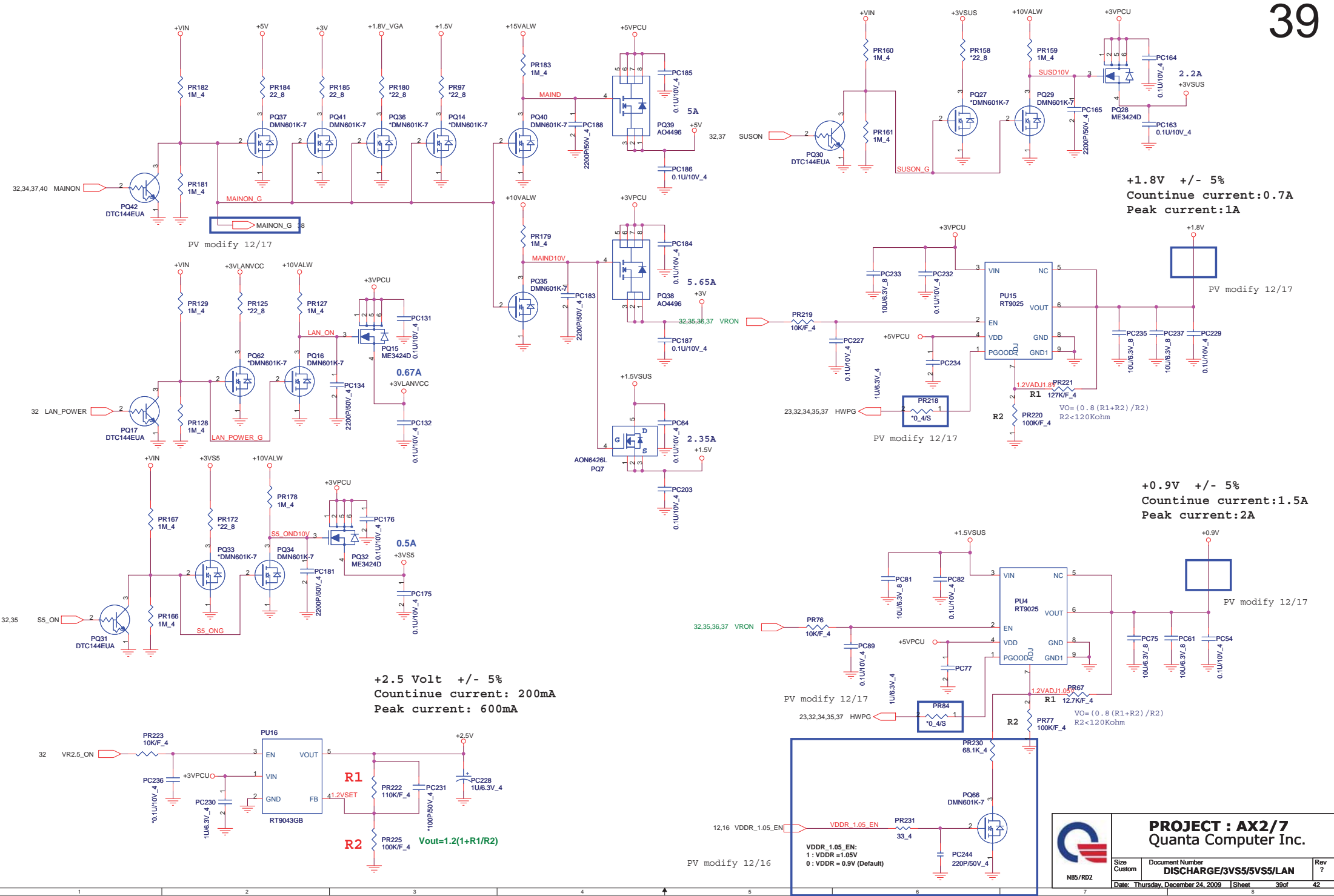
+1.8V +/- 5%
Continue current: 1.2A
Peak current: 3A



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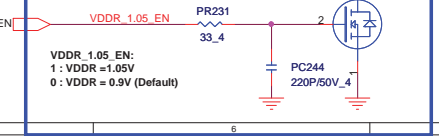
Date: Thursday, December 24, 2009 | Sheet 38 of 42



+1.8V +/- 5%
 Countinue current:0.7A
 Peak current:1A

+2.5 Volt +/- 5%
 Countinue current: 200mA
 Peak current: 600mA

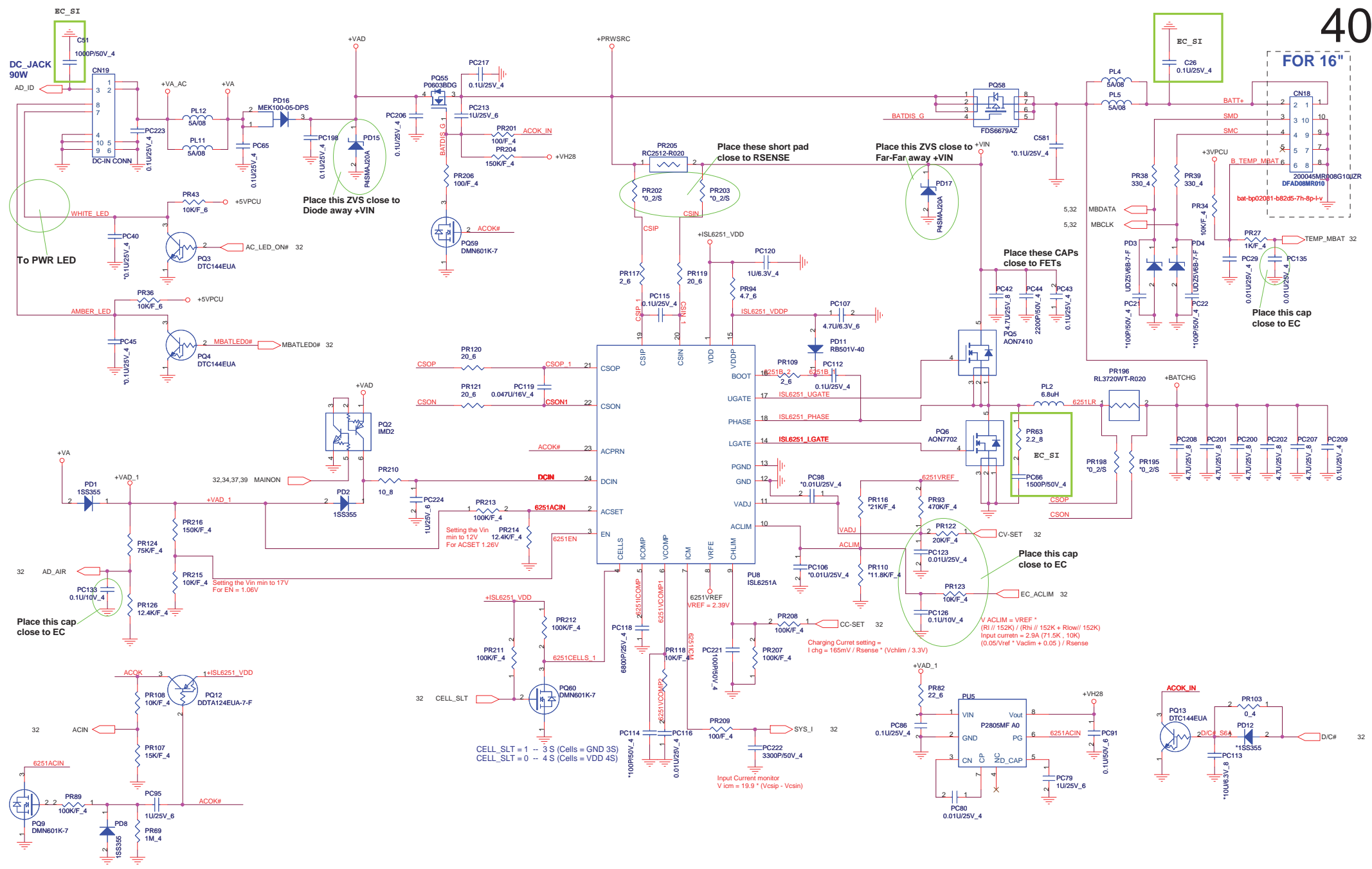
+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A



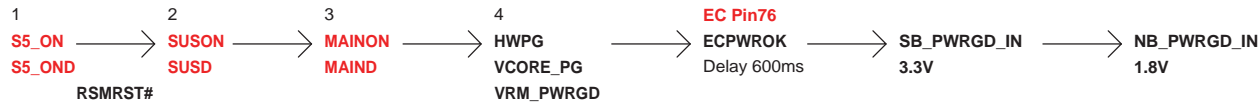
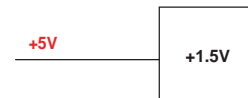
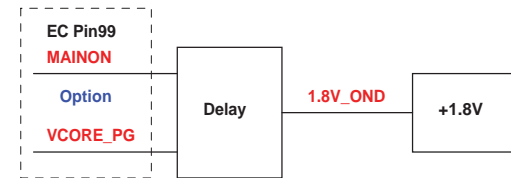
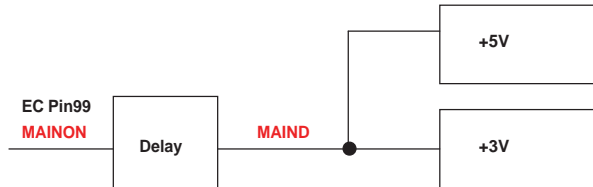
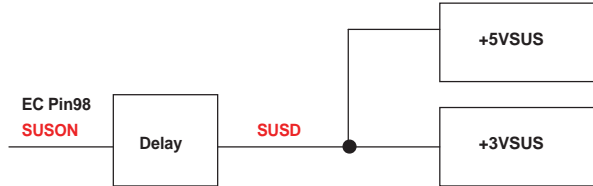
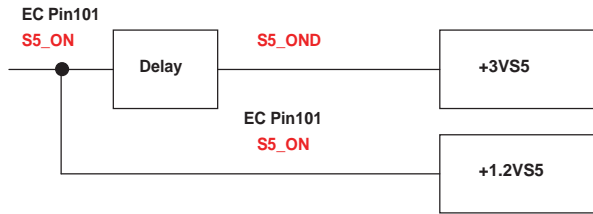
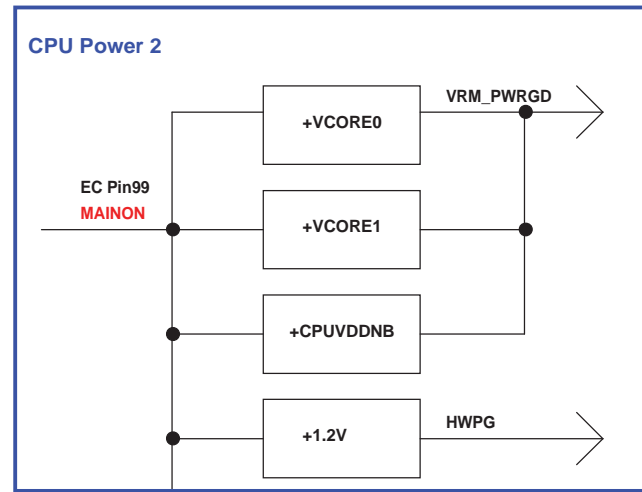
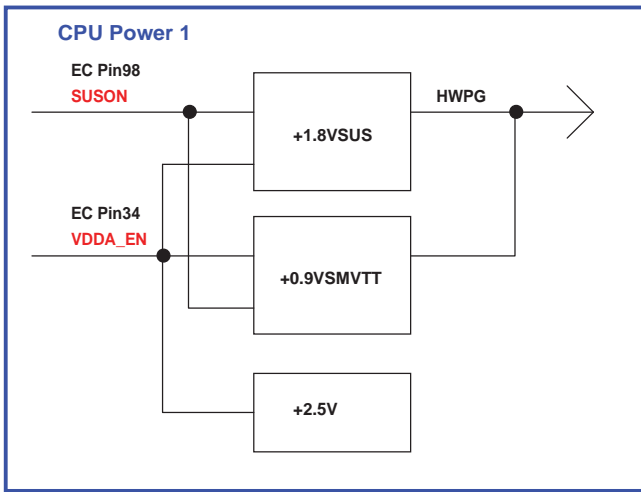
PROJECT : AX2/7
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Size Custom	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev ?
Date: Thursday, December 24, 2009		Sheet 39 of 42

FOR 16"



	PROJECT : AX2/7		
	Quanta Computer Inc.		
	Size Custom	Document Number CHARGER (ISL6251)	Rev 1A
Date: Thursday, December 24, 2009			Sheet 40 of 42



Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT



PROJECT : AX2/7
Quanta Computer Inc.

Size	Document Number	Rev 1A
Date: Wednesday, December 23, 2009 Sheet 42 of 42		