ALW POWER ASSERT

Insert AC adapter only, then without press power button

PS_ID

PS_ID is to confirm that insertion of AC adapter 65W or 90W

PWR_SRC

+RTCSRC is generated by PWR_SRC through D40

+RTCSRC

Power Plan:
0. RTC power plane.
1. Always power plane.
2. SUS power plane.
3. RUN power plane.

ACPI Power State:
1. S0: System Full On, All power planes are ON.
2. S3: Suspend to RAM, RUN power off.
3. S4: Suspend to Disk, RTC and Always power ON.(AC)
4. S5: Soft Off, power state like S4.

U9 Pin 1

+RTCSRC will be input of **MAXIM 1615**, then +RTC_PWR is the output of MAXIM 1615

Pin 3

+RTC_PWR

With either **LIVE_ON_BATT** or **ACAV_IN** existed, +RTC_PWR can convert to +5VALW through Q61

+5VALW

If no ALW power, what should we do?
A: Check all ACAV_IN relate circuit.

Pin 1 U13

+RTCSRC will be input of **MAXIM 1615**, then +3.3VRTC is the output of MAXIM 1615

Pin 3

+3.3VRTC

With either **LIVE_ON_BATT** or **ACAV_IN** existed, +3.3VRTC can convert to +3VALW through Q62

+3VALW

X7 XTAL 32.768K will oscillate after +3.3VRTC comes up high & U37.2 should driven high after +3VALW comes up.

32 K Hz

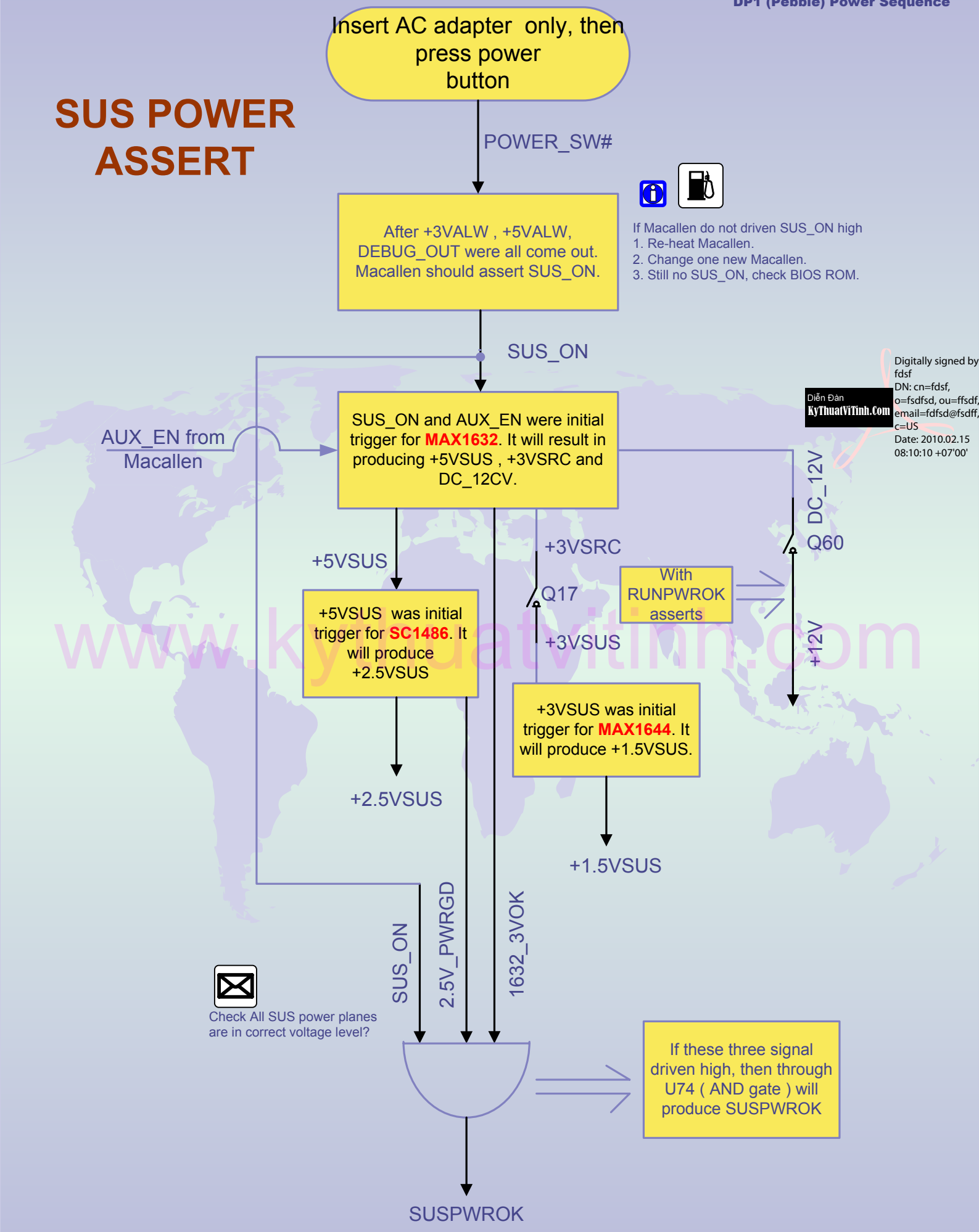
Macallen

Go!

If Macallen is working. CN8 pin2 will have 1,2,3,4 pulse when AC adapter attached(**DEBUG_OUT**)

Q: If no debug out pulse?
1. Macallen.
2. BIOS ROM.

SUS POWER ASSERT



RUN POWER ASSERT

If SUSPWROK is OK, it will drive to ICH4

SUSPWROK

When initialized ICH4, drives SLP_S3# which causes Macallen to drive RUN_ON.

RUN_ON

After approximate 10ms soft start delay, RUN power switches are turned on and connecting RUN planes with SUS planes

SUS POWER PLANES → **RUN POWER PLANES**

+5VSUS

+3VSUS

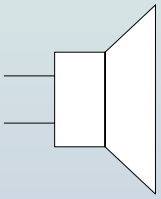
+5VSUS was initial trigger for **TPS793475**.It will produce +5VA

+3VSUS was initial trigger for **MAX1792**.It will produce +1.8VRUN

+5VA

+1.8VRUN

4.75V for audio circuit.



Make sure all RUN power planes are in correct voltage level.

+5VSUS

Q55

+5VRUN

Delay 10ms

+3VSRC

Q18

+3VRUN

+1.5VSUS

Q69

+1.5VRUN

+5VRUN

+5VRUN was initial trigger for **SC1486**.It will produce +1.25VRUN

+1.25VRUN

1.25V_PWRGD

If these three signal assert, then through U20 (AND gate) will produce RUNPWROK

RUNPWROK

DP1 (Pebble) Power Sequence

10ms after +5VRUN power plane comes up

RUNPWROK

RUNPWROK was initial trigger for **MAX1715**. It will produce +1.2VRUN and VCC_IO

RUNPWROK was initial trigger for **SC1476**. It will produce VCC_CORE

+1.2VRUN

VCC_IO

VCC_CORE

If no Vcore:
1. Check high/low side MOSFET.
2. Check U67 SC1476

When **Macallen** is ready to release the Banias, it will drive RESET_OUT#

RESET_OUT#

After +1.2VRUN and VCC_IO came out. **MAX1715** will produce 1715PWROK

After VCC_CORE came out. **SC1476** will produce VCORE_PWRGD

1715PWROK

VCORE_PWRGD

10ms after VCC_CORE and VCC_IO are within regulation. VCORE_PWRGD is driven to ICH4 (VGATE)

VCORE_PWRGD_D

VGATE

ICH4

Delay 10ms

If CPU power is OK and CPURST# de-assertion.
1. CPU: re-heat, change one new.
2. Change BIOS ROM.

CK408_IMVP_PWRGD
(TO CLOCK GEN)

All clocks

DELAY_IMVP_PWRGD

DELAY_IMVP_PWRGD is driven to ICH4 as PWROK allowing release of the Banias from INIT and deassertion of PCIRST#

Next step should check:
1. PCIRST#
2. CPURST#
3. GTL_ADS#