PCB STACK UP

6L DIS

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

R03/V03 UMA BLOCK DIAGRAM

DDRIII-SODIMM1 A 00 PAGE 16 — DDRIII 1333 MT/s
DDRIII-SODIMM2 A 01 PAGE 17 — DDRIII 1333 MT/s

CPU
Sandy Bridge 45W
PGA 989
PAGE 4~8

FDI LINK 2.5GT /s
DMI LINK 2.5GT /s

Mobile Intel Series 6 Chipset
PCH
HM67
Couger Point
BGA 989
25 mm X 25 mm
PAGE 9~15

iGFX Interfaces

INT HDMI → HDMI Switch PAGE 19 → HDMI CONN PAGE 19

INT Dual CHANNEL LVDS → LCD CONN 1600 x 900 (HD) PAGE 18

Re-Driver SN75LVCP412RTJR PAGE 20 — E-SATA PAGE 20 — SATA4 300MB /S
SATA -HDD PAGE 21 — SATA0 300MB /S
ODD PAGE 21 — SATA1 300MB /S
3-axis Fall Sensor PAGE 21 — SMBUS

USB2.0
- ESATA+USB2.0 PAGE 20 — USB[0]
- Camera PAGE 18 — USB[11]
- Card Reader RTS5128-GR PAGE 22 — USB[8]
- FP PAGE 28 — USB[10]
- Touch Screen PAGE 27 — USB[12]
- Express Card R5538D001 PAGE 02 — USB[8]

- CRT Board PAGE 03 — IO Board
- WLAN PAGE 05 — USB[4] — PCIE[1]
- WiMAX PAGE 04 — USB[5] — PCIE[2]
- USB3.0 Controller PAGE 06 — PCIE[3]
- BlueTooth PAGE 05 — USB[6]
- USB3.0 Ports x2 PAGE 07
- LAN Realtek RTL8111E-VB-GR PAGE 09 — PCIE[5] — 25MHz
- RJ45 PAGE 10
- USB Port x1 PAGE 08 — USB[2]

EXP Board
LED Board
PB Board
TP Board
HotKey Board

32.768KHz
KBC ITE 8518 PAGE 23 — LPC
- Keyboard Conn. PAGE 28
- Touch Pad PAGE 28
- LED PAGE 29
- PWM FAN &Thermal PAGE 31
- SPI ROM 512kB PAGE 27

SPI → SPI ROM 4MB PAGE 27

25MHz
32.768KHz

IHDA → Audio Codec ALC 269Q-VB6-GR PAGE 25
- Subwoofer MAX9759ETE PAGE 26
- Speaker PAGE 25
- Jack X2 PAGE 25
- Digital-MIC PAGE 25

- Charger PAGE 35
- 3/5V PAGE 36
- 1.5V_SUS/0.75V_DDR PAGE 37
- Batt/DC-IN PAGE 34
- 1.05V_PCH PAGE 38
- VCCSA PAGE 39
- CPU_CORE PAGE 40
- 1.8V_RUN PAGE 38

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

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power / State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+VCHGR +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+5V_SUS +3.3V_SUS +1.5V_SUS +1.5V_CPU +DDR_VTTREF +3.3V_LAN (for R03)	+VCC_CORE +1.05V_PCH +5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +VCCSA +0.75V_DDR_VTT +LCDVCC +VCC_GFX_CORE	
S0	ON	ON	ON	ON	ON	
S1						
S3	ON	ON	ON	ON	OFF	
S4/S5 AC	ON	ON				
S4/S5 DC Only	ON		ON	OFF	OFF	
AC/DC No Exist	ON	OFF	OFF	OFF	OFF	

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	Power Rails	2A

Date: Wednesday, October 27, 2010 Sheet 2 of 42

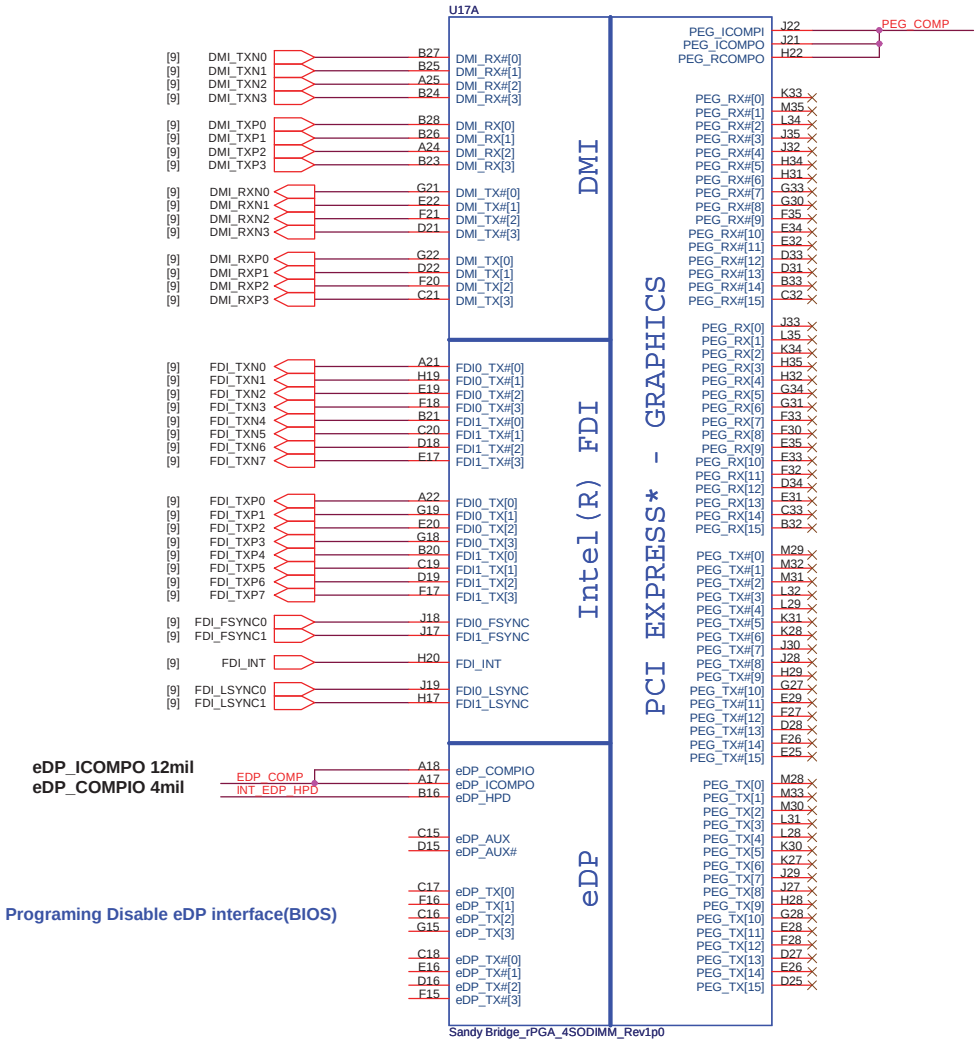
Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	BLANK	2A

Date: Wednesday, October 06, 2010 Sheet 3 of 42

Sandy Bridge Processor (DMI,PEG,FDI)

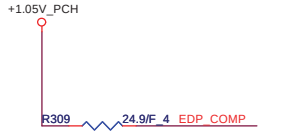


PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

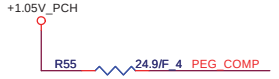
eDP_ICOMPO 12mil
eDP_COMPIO 4mil

Programing Disable eDP interface(BIOS)

DP & PEG Compensation



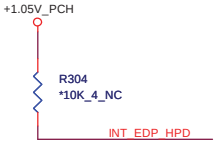
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 1/5	2A
Date: Friday, January 07, 2011	Sheet 4 of 42	

Sandy Bridge Processor (CLK,MISC,JTAG)

follow SS8: SNB_IVB# N.A at SNB EDS #27637 0.7v1

U17B

MISC
PROC_SELECT# C26 — TP43
SKTOCC# AN34 — [23] H_CPUDET#

THERMAL
CATERR# AL33 — TP34 — TP_CATERR#
PECI AN33 — [23] PECI_EC — R445 43/J_4 — H_PECI_R
PROCHOT# AL32 — [23,35,40] H_PROCHOT# — R181 56/J_4 — H_PROCHOT#_R
THERMTRIP# AN32 — [14] PM_THRMTRIP#

PWR MANAGEMENT
PM_SYNC AM34 — [9] H_PM_SYNC
UNCOREPWRGOOD AP33 — [14] H_PWRGOOD — R189 10K/J_4
SM_DRAMPWROK V8 — SM_DRAMPWROK
RESET# AR33 — CPU_PLTRST#_R — R193 *43/J_4_NC — CPU_PLTRST# — R192 *75/J_4_NC — +1.05V_PCH

CLOCKS
BCLK A28 — CLK_CPU_BCLKP [13]
BCLK# A27 — CLK_CPU_BCLKN [13]
DPLL_REF_CLK A16 — CLK_DP_P_R — R310 1K_4 — R305 *0_4_NC — CLK_DP_P [13]
DPLL_REF_CLK# A15 — CLK_DP_N_R — R306 *0_4_NC — R311 1K_4 — CLK_DP_N [13] — +1.05V_PCH

DDR3 MISC
SM_DRAMRST# R8 — CPU_DRAMRST#
SM_RCOMP[0] AK1 — SM_RCOMP_0 — R153 140/F_4
SM_RCOMP[1] A5 — SM_RCOMP_1 — R312 25.5/F_4
SM_RCOMP[2] A4 — SM_RCOMP_2 — R313 200/F_4

JTAG & BPM
PRDY# AP29
PREQ# AP27
TCK AR26 — XDP_TCLK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST# — R447 51/J_4
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBRST# — R443 1K_4 — +3.3V_RUN
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32

+1.05V_PCH
XDP_TMS R452 51/J_4
XDP_TDI R450 51/J_4
XDP_TDO R201 51/J_4
XDP_TCLK R202 51/J_4

Sandy Bridge_rPGA_4SODIMM_Rev1p0

Over 130 degree C will drive low

Schematic C/L_v1.0, P56 (PU,PD 1k/J) (Intel and PD3)
Reserve (Intel confirm now)

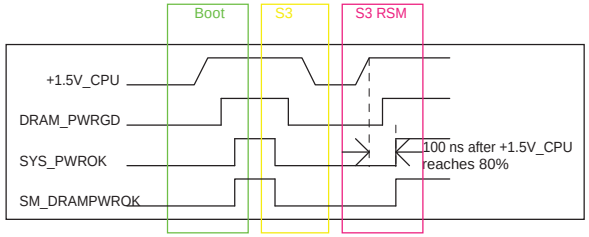
SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

When MP, JTAG PU/PD resistor can be removed?
Need to confirm with Intel

IN	OUT
L	L
H	High-Z

+3.3V_SUS
U8 *74LVC1G07GW_NC
C333 *0.1U/10V/X7R_4_NC
[12,23,24] PLTRST#
CPU_PLTRST#
R556 1.5K 1%
R557 750 1%
CPU_PLTRST#_R voltage level Ckt.



Change OD part same with PDC

Copy from PDC

R8239, R8241 change to 5%

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

+3.3V_SUS
R183 200_4
C301 0.1U/10V/X7R_4
U6 74AHC1G09GW
[9] PM_DRAM_PWRGD
[9] SYS_PWROK
+1.5V_CPU
R170 200/F_4
SM_DRAMPWROK_R
R176 130/F_4 SM_DRAMPWROK
R184 *39_NC
Q14 *2N7002K_NC
PS_S3CNTRL [7,16]

Follow #DG1.0 436735 P105
DDR Power Gating Topology

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration

+1.5V_SUS
R72 1K/F_4
R54 *0_4_NC
R63 1K/F_4
Q5 BSS138-7-F
[16,17] DDR3_DRAMRST#
DDR3_DRAMRST#_R
CPU_DRAMRST#
[13] DDR_HVREF_RST_PCH
C86 0.047U/10V_4
R56 4.99K/F_4

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 2/5	2A

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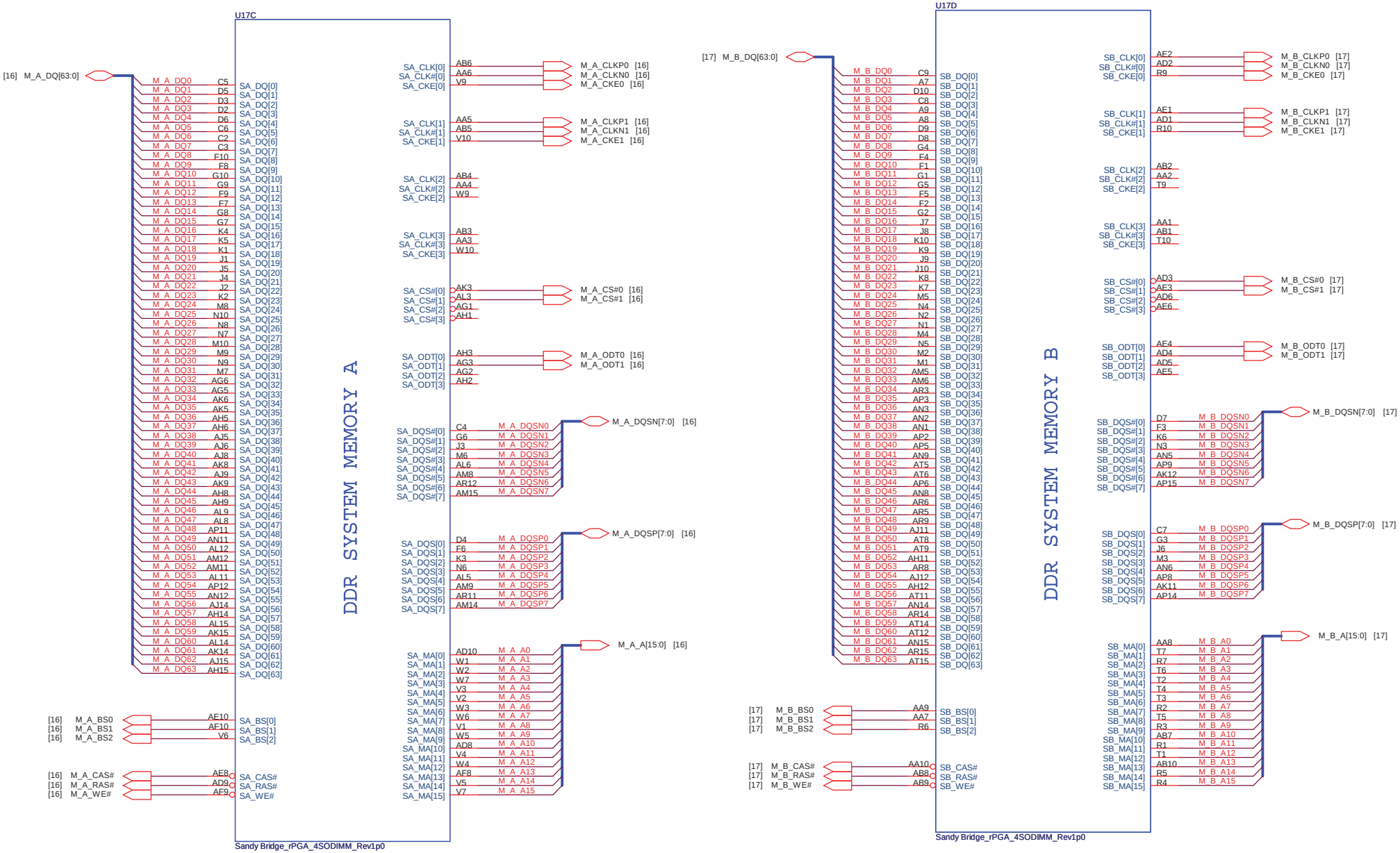
Sandy Bridge Processor (DDR3)



Quanta Computer Inc.			
PROJECT : R03/V03			
Size	Document Number: Sandy Bridge 3/5		Rev 2A
Date: Friday, January 07, 2011	Sheet 6 of 42		

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:95A
470uF/4mohm x 4
22uF x 16
10uF x 10

CPU VTT
SNB 45W:8.5A
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

S3 Power reduce

Take care Q3509 Vgs(MAX)=2.5

Change R8281,R8285, R8704,R8329 to +/-5%
54.9 ohm has no 5%

Layout note: need routing together and ALERT need between CLK and DATA

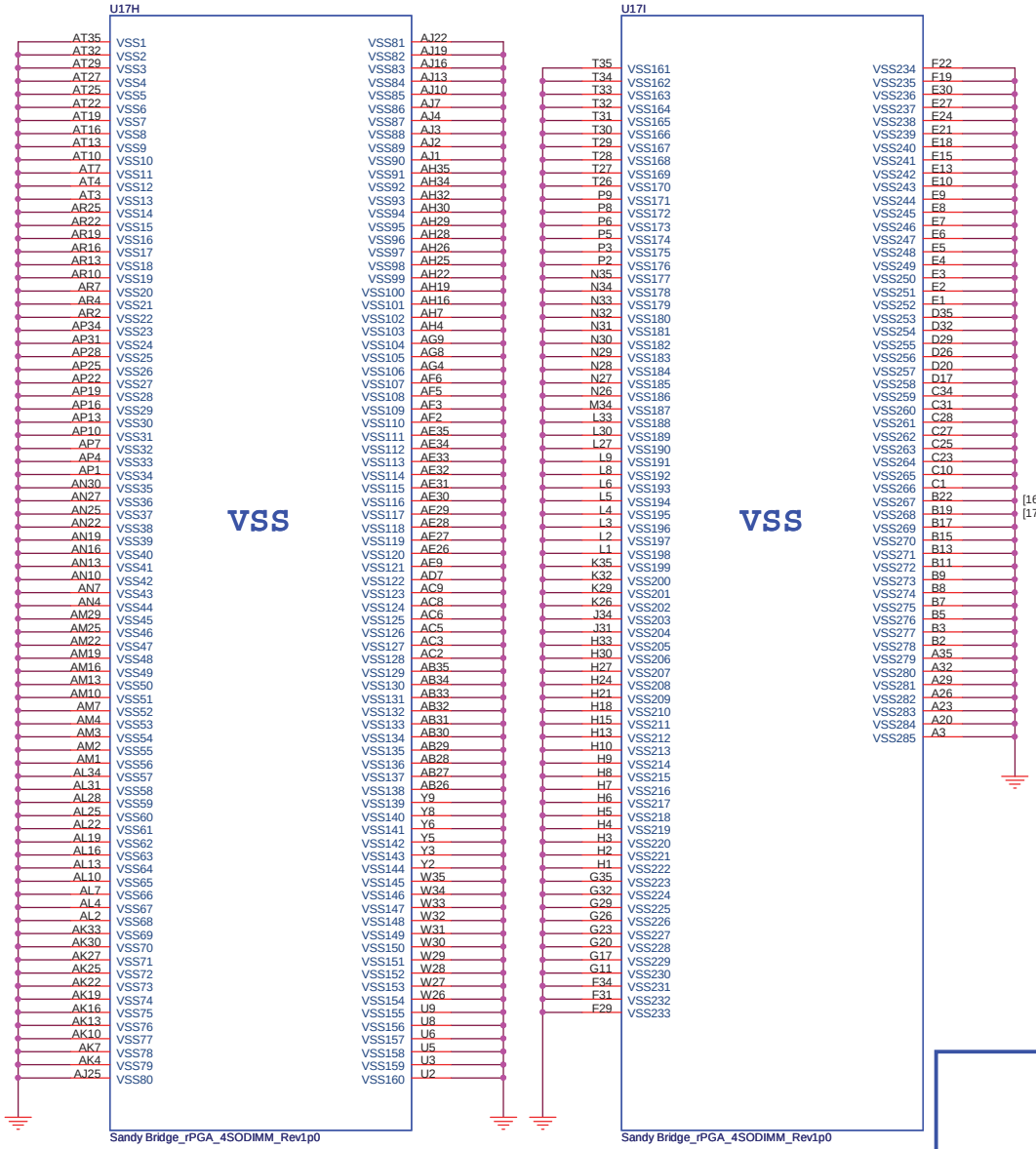
SVID CLK — PU Close to VR — Place PU resistor close to CPU

SVID DATA — PU Close to VR — Place PU resistor close to CPU

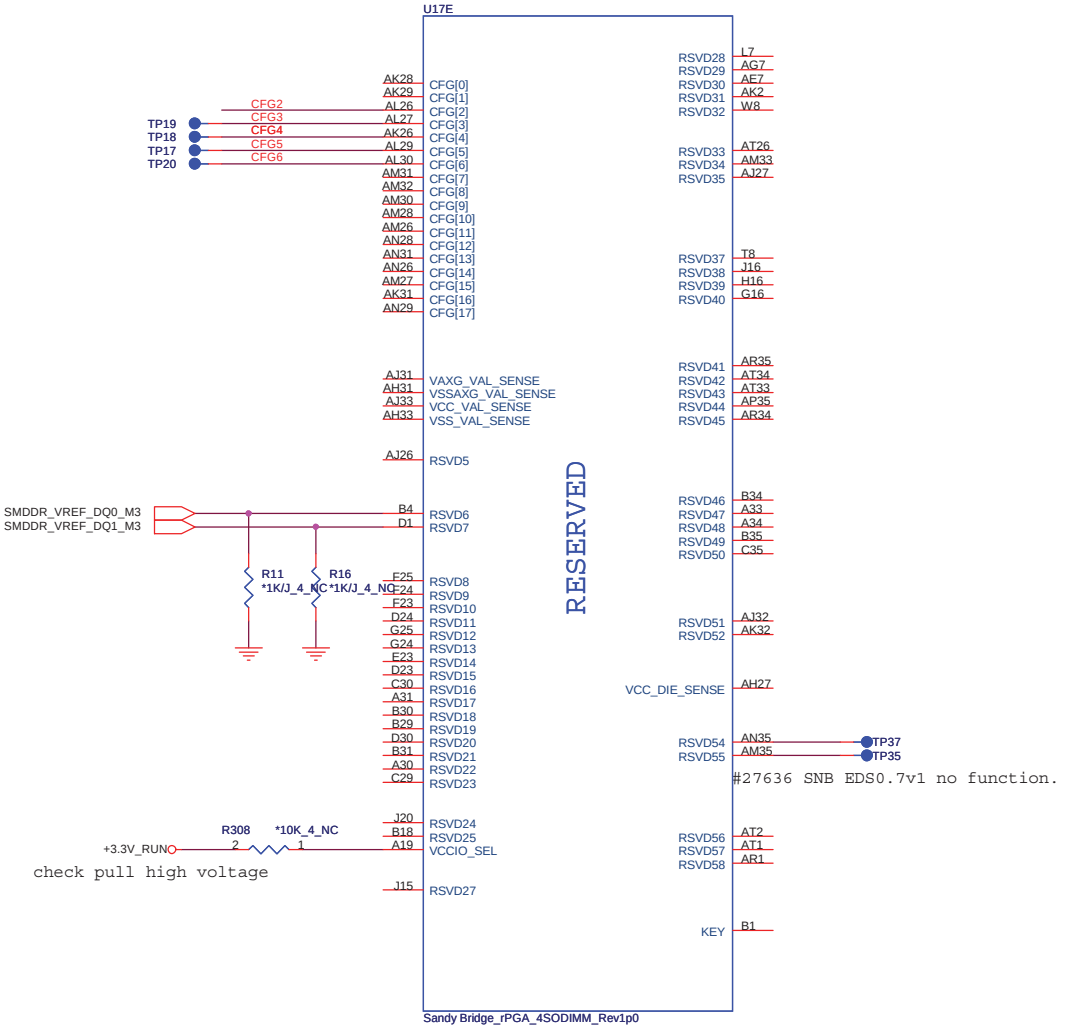
SVID ALERT

Quanta Computer Inc.
PROJECT : R03/V03
Sandy Bridge 4/5
Date: Monday, January 24, 2011 Sheet 7 of 42

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R199 1K/F_4

Quanta Computer Inc.
PROJECT : R03/V03

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	Sandy Bridge 5/5	2A
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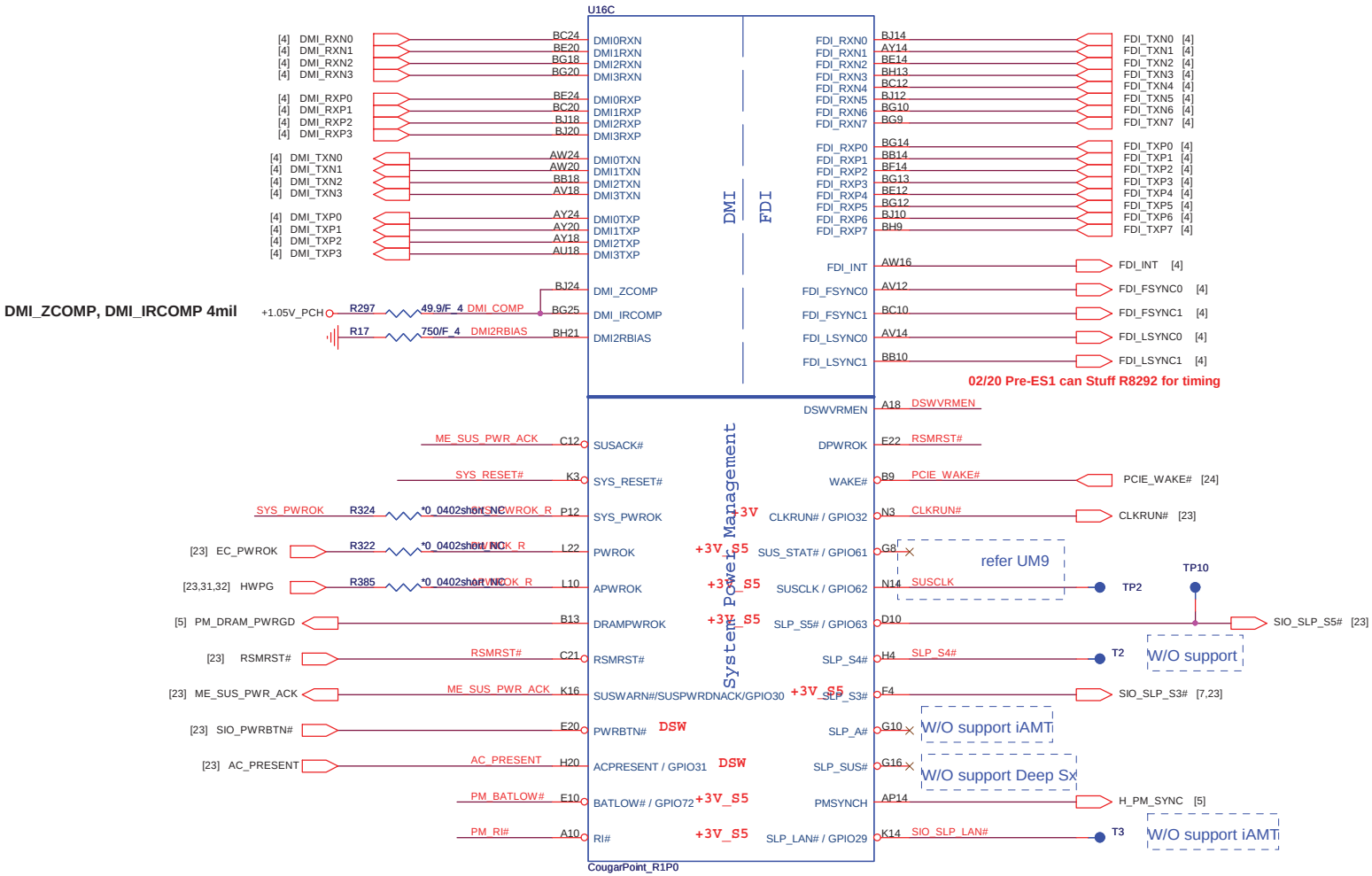
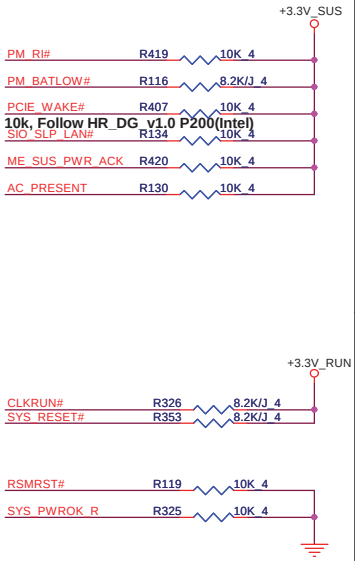
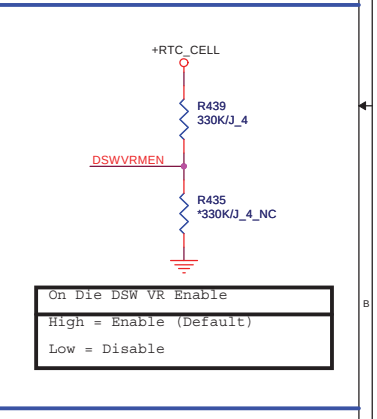
Cougar Point (DMI,FDI,PM)

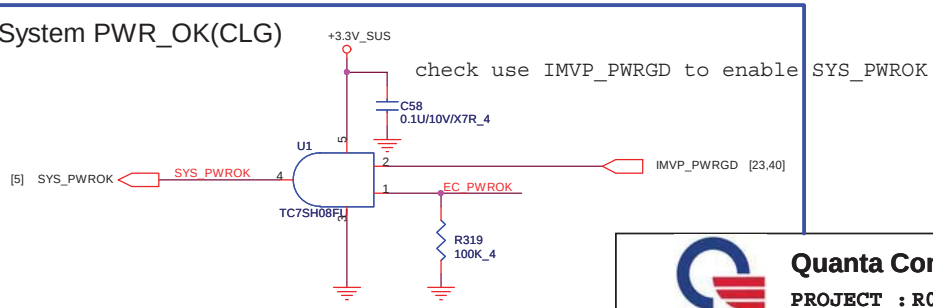


PCH Pull-high/low(CLG)





System PWR_OK(CLG)



Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Cougar Point 1/7	2A

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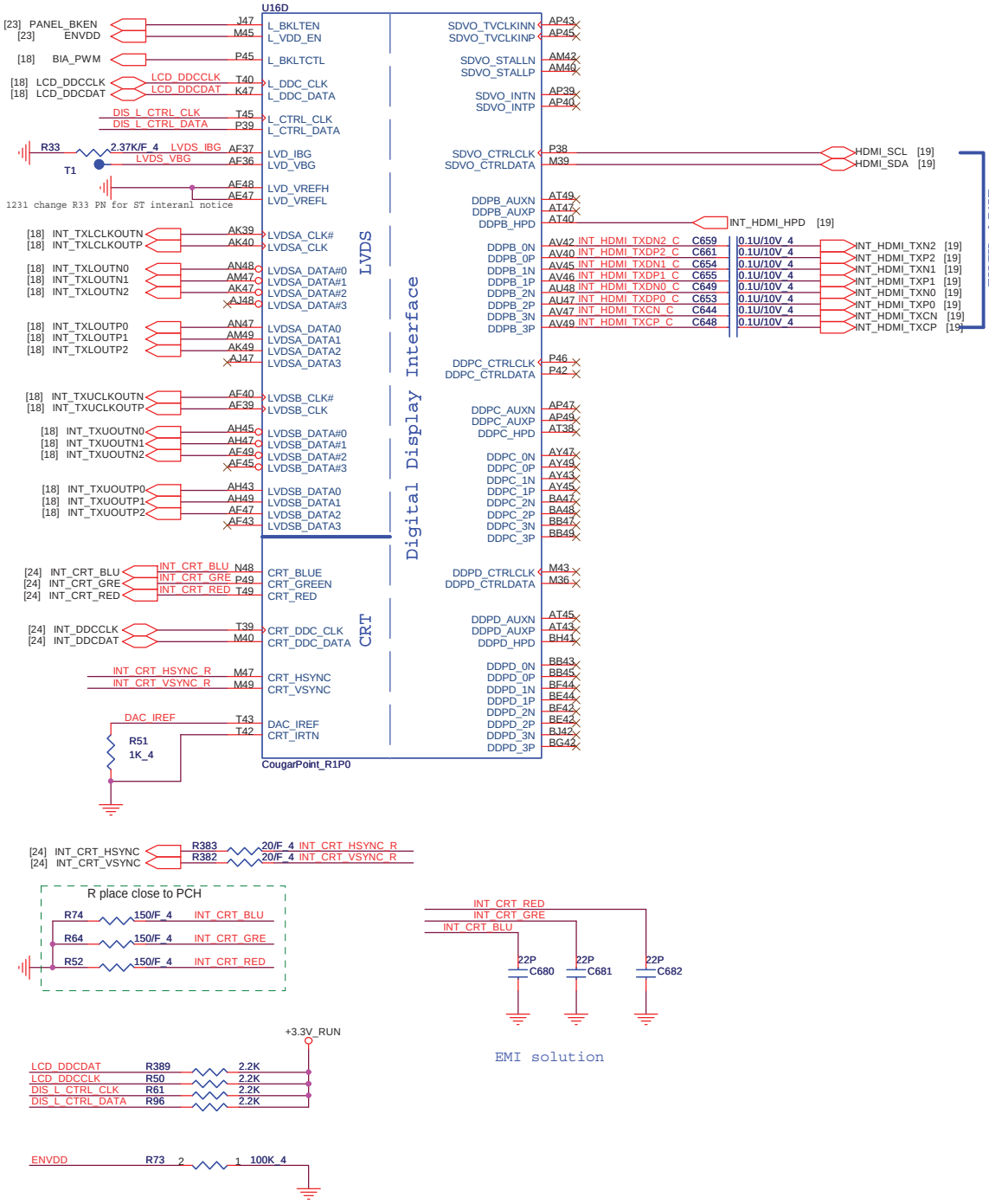
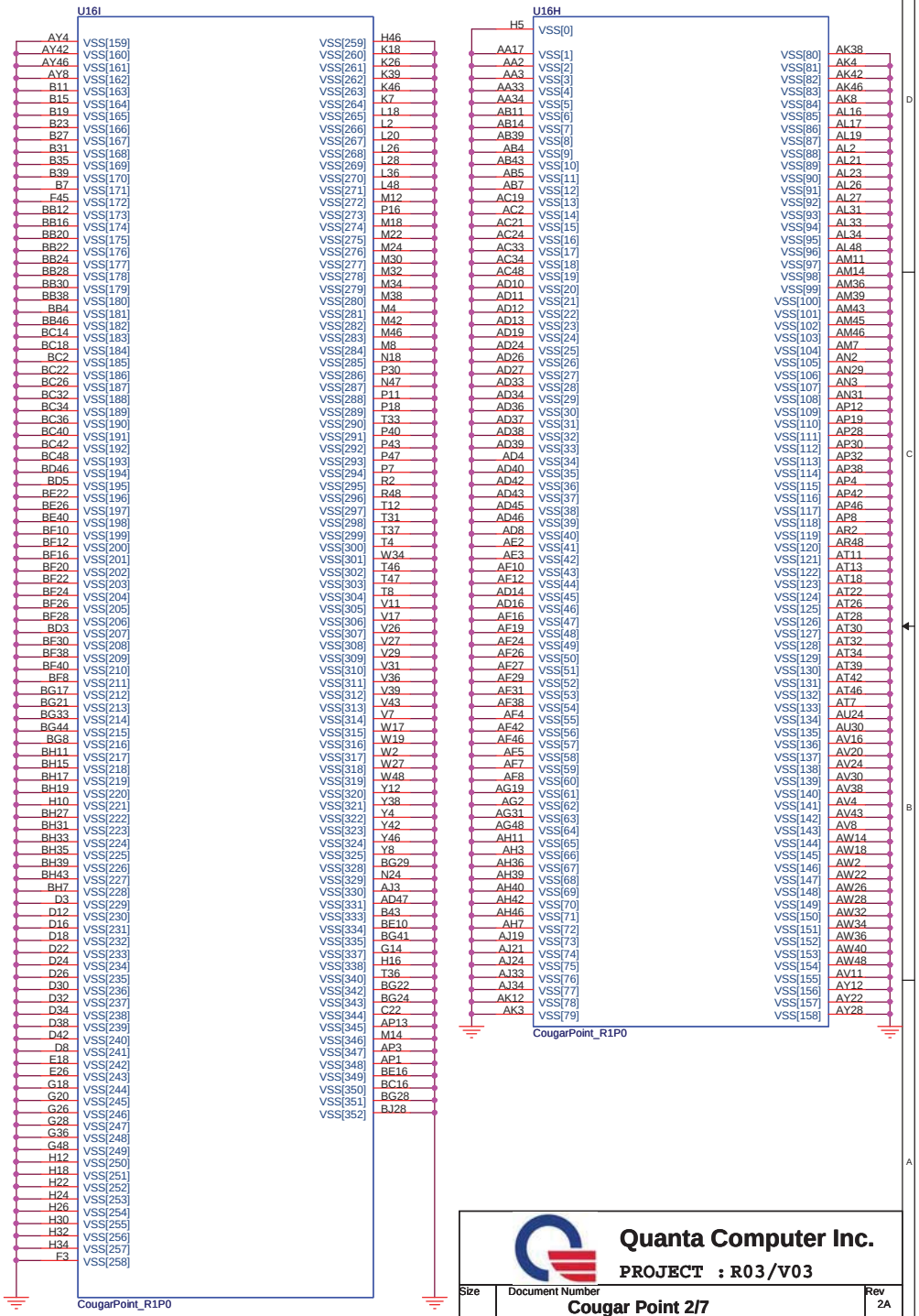
Cougar Point (LVDS,DDI)



Cougar Point (GND)



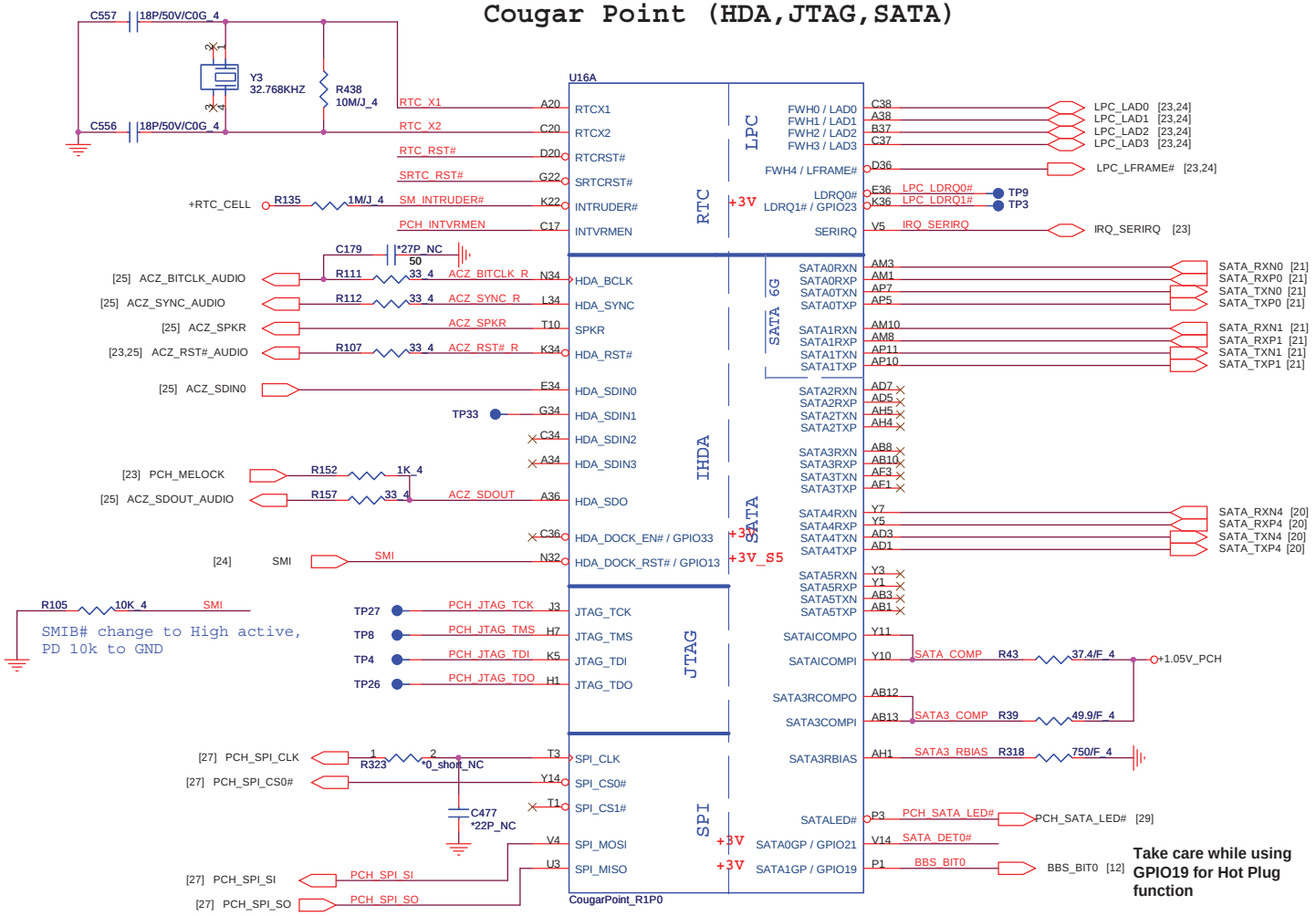
Quanta Computer Inc.

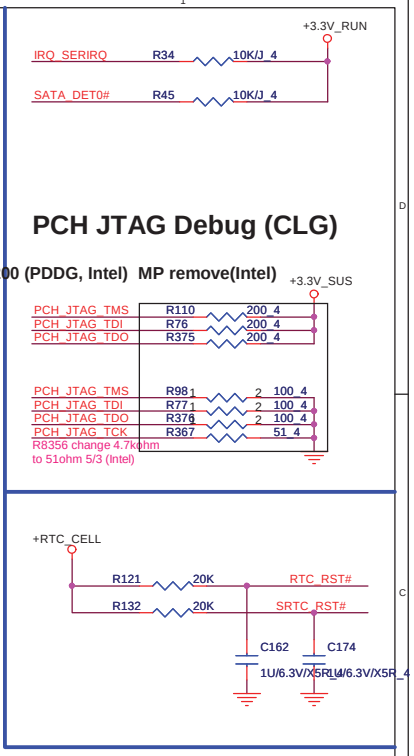
PROJECT : R03/V03

Size	Document Number	Rev
	Cougar Point 2/7	2A

Date: Monday, January 24, 2011 Sheet 10 of 42

Cougar Point (HDA,JTAG,SATA)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R41 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R146 *1K_4_NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R434 330K/J_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R118 1K_4 ACZ_SYNC_R

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Cougar Point 3/7	2A

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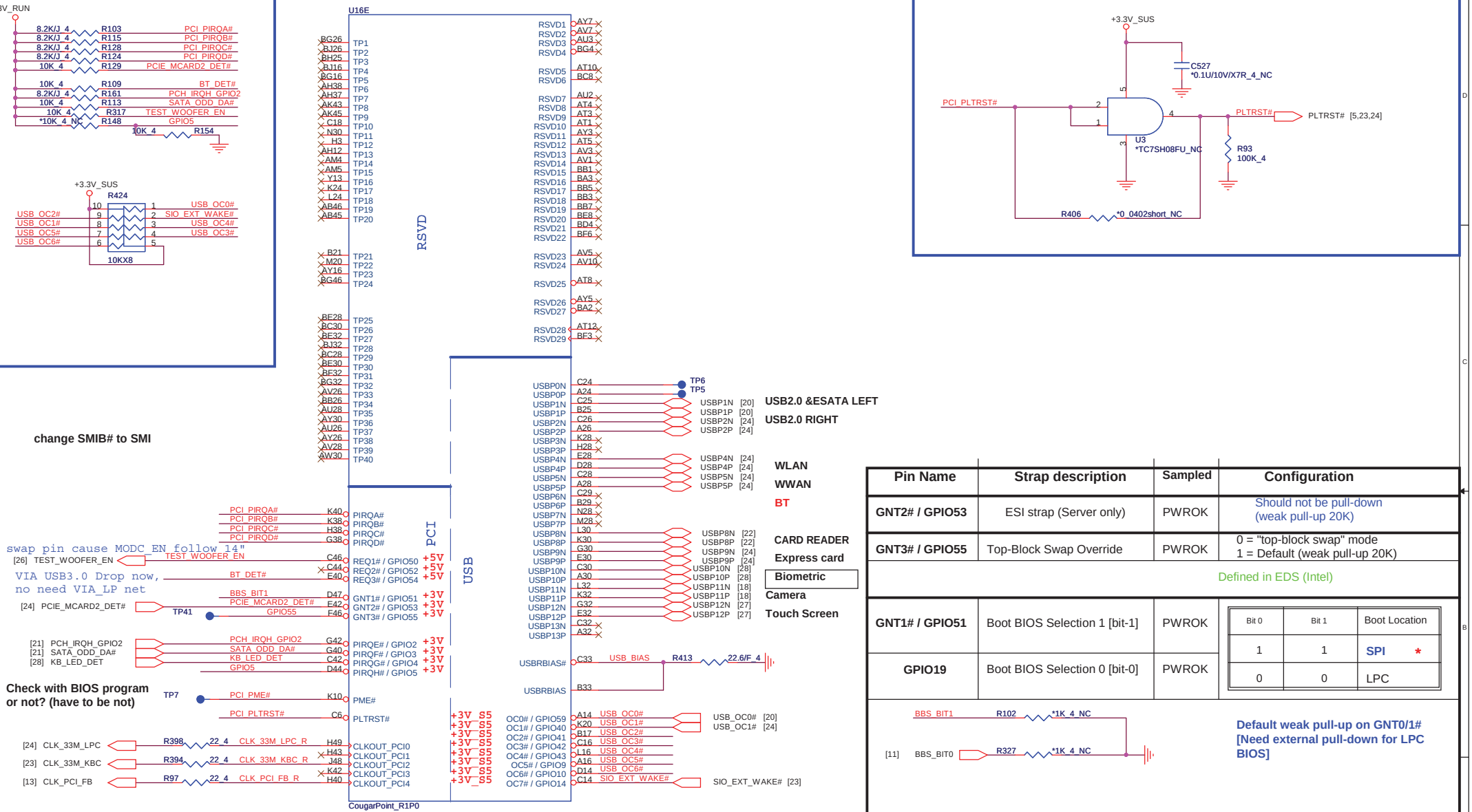
Cougar Point-M (PCI,USB,NVRAM)

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

change SMIB# to SMI



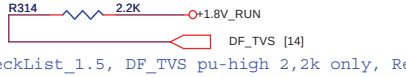
Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
			Defined in EDS (Intel)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	

Bit 0	Bit 1	Boot Location
1	1	SPI *
0	0	LPC

Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]

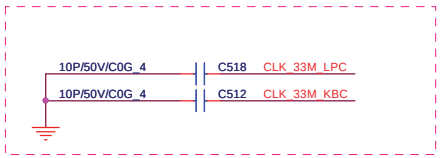
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm

CheckList_1.0 p58; HR_v1.0 p450



follow CheckList_1.5, DF_TVS pu-high 2,2k only, Remove R315

SV_SET_UP
High = Strong (Default)



EMI solution pop C518, C512

Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	Cougar Point 4/7	2A

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Cougar Point-M (PCI-E,SMBUS,CLK)

U16B

WLAN
[24] PCIE_RXN1 BG34
[24] PCIE_RXP1 BJ34
[24] PCIE_TXN1 C31 0.1U/10V/X7R_4 PCIE_TXN1_C AV32
[24] PCIE_TXP1 C30 0.1U/10V/X7R_4 PCIE_TXP1_C AU32

WWAN
[24] PCIE_RXN2 BE34
[24] PCIE_RXP2 BF34
[24] PCIE_TXN2 C11 0.1U/10V/X7R_4 PCIE_TXN2_C BB32
[24] PCIE_TXP2 C12 0.1U/10V/X7R_4 PCIE_TXP2_C AY32

USB 3.0
[24] PCIE_RXN3 BG36
[24] PCIE_RXP3 BJ36
[24] PCIE_TXN3 C16 0.1U/10V/X7R_4 PCIE_TXN3_C AV34
[24] PCIE_TXP3 C14 0.1U/10V/X7R_4 PCIE_TXP3_C AU34

BF36 BE36 AY34 BB34

LAN
[24] PCIE_RXN5 BG37
[24] PCIE_RXP5 BH37
[24] PCIE_TXN5 C24 0.1U/10V/X7R_4 PCIE_TXN5_C AY36
[24] PCIE_TXP5 C21 0.1U/10V/X7R_4 PCIE_TXP5_C BB36

Express card
[24] PCIE_RXN6 BJ38
[24] PCIE_RXP6 BG38
[24] PCIE_TXN6 C52 0.1U/10V/X7R_4 PCIE_TXN6_LAN_C AU36
[24] PCIE_TXP6 C46 0.1U/10V/X7R_4 PCIE_TXP6_LAN_C AV36

BG40 BJ40 AY40 BB40

BE38 BC38 AW38 AY38

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

PCI-E*

SMBUS

+3V_S5 SMBALERT# / GPIO11 E12 PCH_SMB_ALERT#
SMBCLK H14 SMBCLK → SMBCLK [24]
SMBDATA C9 SMBDATA → SMBDATA [24]
+3V_S5 SML0ALERT# / GPIO60 A12 1K_4 R421 +3.3V_SUS; A12 → DDR_HVREF_RST_PCH [5]
SML0CLK C8 SML0CLK
SML0DATA G12 SML0DATA
+3V_S5 SML1ALERT# / PCHHOT# / GPIO74 C13 PCH_GPIO74
+3V_S5 SML1CLK / GPIO58 E14 SMB_CLK_ME1
+3V_S5 SML1DATA / GPIO75 M16 SMB_DATA_ME1

Controller Link

CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

CLOCKS

+3V_S5 PEG_A_CLKRQ# / GPIO47 M10 PEG_A_CLKRQ#

WLAN
[24] CLK_PCIE_WLANN Y40 CLKOUT_PCIE0N
[24] CLK_PCIE_WLANP Y39 CLKOUT_PCIE0P
[24] PCIE_CLK_REQ0# PCIE_CLK_REQ0# J2 PCIECLKRQ0# / GPIO73 +3V_S5

WWAN
[24] CLK_PCIE_WMAXN AB49 CLKOUT_PCIE1N
[24] CLK_PCIE_WMAXP AB47 CLKOUT_PCIE1P
[24] PCIE_CLK_REQ1# PCIE_CLK_REQ1# M1 PCIECLKRQ1# / GPIO18 +3V

USB3.0
[24] CLK_PCIE_USB30N AA48 CLKOUT_PCIE2N
[24] CLK_PCIE_USB30P AA47 CLKOUT_PCIE2P
[24] PCIE_CLK_REQ2# PCIE_CLK_REQ2# V10 PCIECLKRQ2# / GPIO20 +3V

Y37 CLKOUT_PCIE3N
Y36 CLKOUT_PCIE3P
PCIE_CLK_REQ3# A8 PCIECLKRQ3# / GPIO25 +3V_S5

LAN
[24] CLK_PCIE_LANN Y43 CLKOUT_PCIE4N
[24] CLK_PCIE_LANP Y45 CLKOUT_PCIE4P
[24] PCIE_CLK_REQ4# PCIE_CLK_REQ4# L12 PCIECLKRQ4# / GPIO26 +3V_S5

Express card
[24] CLK_PCIE_EXPN V45 CLKOUT_PCIE5N
[24] CLK_PCIE_EXPP V46 CLKOUT_PCIE5P
[24] PCIE_CLK_REQ5# PCIE_CLK_REQ5# L14 PCIECLKRQ5# / GPIO44 +3V_S5

AB42 CLKOUT_PEG_B_N
AB40 CLKOUT_PEG_B_P
PEG_B_CLKRQ# E6 PEG_B_CLKRQ# / GPIO56 +3V_S5

V40 CLKOUT_PCIE6N
V42 CLKOUT_PCIE6P
PCIE_CLK_REQ6# T13 PCIECLKRQ6# / GPIO45 +3V_S5

V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
add test point for XDP
PCIE_CLK_REQ7# K12 PCIECLKRQ7# / GPIO46 +3V_S5

XDP
CLK_PCIE_XDPN T5 AK14 CLKOUT_ITPXDP_N
CLK_PCIE_XDPP T4 AK13 CLKOUT_ITPXDP_P

CLKIN_DMI_N BF18 CLK_DMIN
CLKIN_DMI_P BE18 CLK_DMIP
CLKIN_GND1_N BJ30 CLK_GND1_N
CLKIN_GND1_P BG30 CLK_GND1_P
CLKIN_DOT_96N G24 CLK_BUF_DREFCLKN
CLKIN_DOT_96P E24 CLK_BUF_DREFCLKP
CLKIN_SATA_N AK7 CLK_BUF_DREFSSCLKN
CLKIN_SATA_P AK5 CLK_BUF_DREFSSCLKP
REFCLK14IN K45 CLK_PCH_14M
CLKIN_PCILOOPBACK H45 CLK_PCI_FB → CLK_PCI_FB [12]
XTAL25_IN V47 XTAL25_IN
XTAL25_OUT V49 XTAL25_OUT
XCLK_RCOMP Y47 XCLK_RCOMP R329 90.9/F_4 +1.05V_PCH

CLKOUT_PEG_A_N AB37
CLKOUT_PEG_A_P AB38
CLKOUT_DMI_N AV22 → CLK_CPU_BCLKN [5]
CLKOUT_DMI_P AU22 → CLK_CPU_BCLKP [5]
CLKOUT_DP_N AM12 → CLK_DP_N [5]
CLKOUT_DP_P AM13 → CLK_DP_P [5]

FLEX CLOCKS

+3V CLKOUTFLEX0 / GPIO64 K43 CLK_48M_CARD_R R91 22_4 → CLK_48M_CARD [22]
+3V CLKOUTFLEX1 / GPIO65 F47 CLK_VGA_27M_R → T7
+3V CLKOUTFLEX2 / GPIO66 H47 CLK_FLEX2 → T6
+3V CLKOUTFLEX3 / GPIO67 K49 CLK_VGA_27M_SS_R → T8

C480 27P 50
R368 1M/J_4
Y2 25MHz
C493 27P 50
C131 *22P_NC

CougarPoint_R1P0

	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

+3.3V_RUN
Q3 2N7002W-7-F
R330 2.2K
R425 2.2K
SMBCLK → WLAN_SCLK [16,17,24]
Q33 2N7002W-7-F
SMBDATA → WLAN_SDATA [16,17,24]
Q4 2N7002W-7-F
SMB_CLK_ME1 → SMBCLK1 [23]
+3.3V_SUS
Q6 2N7002W-7-F
SMB_DATA_ME1 → SMBDAT1 [23]
change direction

CLK_REQ/Strap Pin(CLG)

+3.3V_SUS
PCIE_CLK_REQ0# 10K_4 R89
PCIE_CLK_REQ3# 10K_4 R399
PCIE_CLK_REQ4# 10K_4 R100
PCIE_CLK_REQ5# 10K_4 R123
PCIE_CLK_REQ6# 10K_4 R117
PCIE_CLK_REQ7# 10K_4 R101
PCIE_CLK_REQ2# 10K_4 R42
PEG_B_CLKRQ# 10K_4 R99

+3.3V_RUN
PCIE_CLK_REQ1# 10K_4 R349

+3.3V_SUS
PEG_A_CLKRQ# 10K_4 R94
*10K_4_NC R95

+3.3V_SUS
PCH_GPIO74 10K_4 R422
PCH_SMB_ALERT# 10K_4 R122

SMBCLK R334 2.2K
SMBDATA R411 2.2K
SMLOCLK R396 2.2K
SMLODATA R127 2.2K
SMB_CLK_ME1 R351 2.2K
SMB_DATA_ME1 R374 2.2K

Stuff for Integrated CLK Gen Mode

CLK_DMIN R25 10K_4
CLK_DMIP R29 10K_4
CLK_GND1_N
CLK_GND1_P R302 1 2 10K_4
CLK_BUF_DREFCLKN R126 10K_4
CLK_BUF_DREFCLKP R125 10K_4
CLK_BUF_DREFSSCLKN R31 10K_4
CLK_BUF_DREFSSCLKP R30 10K_4
CLK_PCH_14M R78 10K_4

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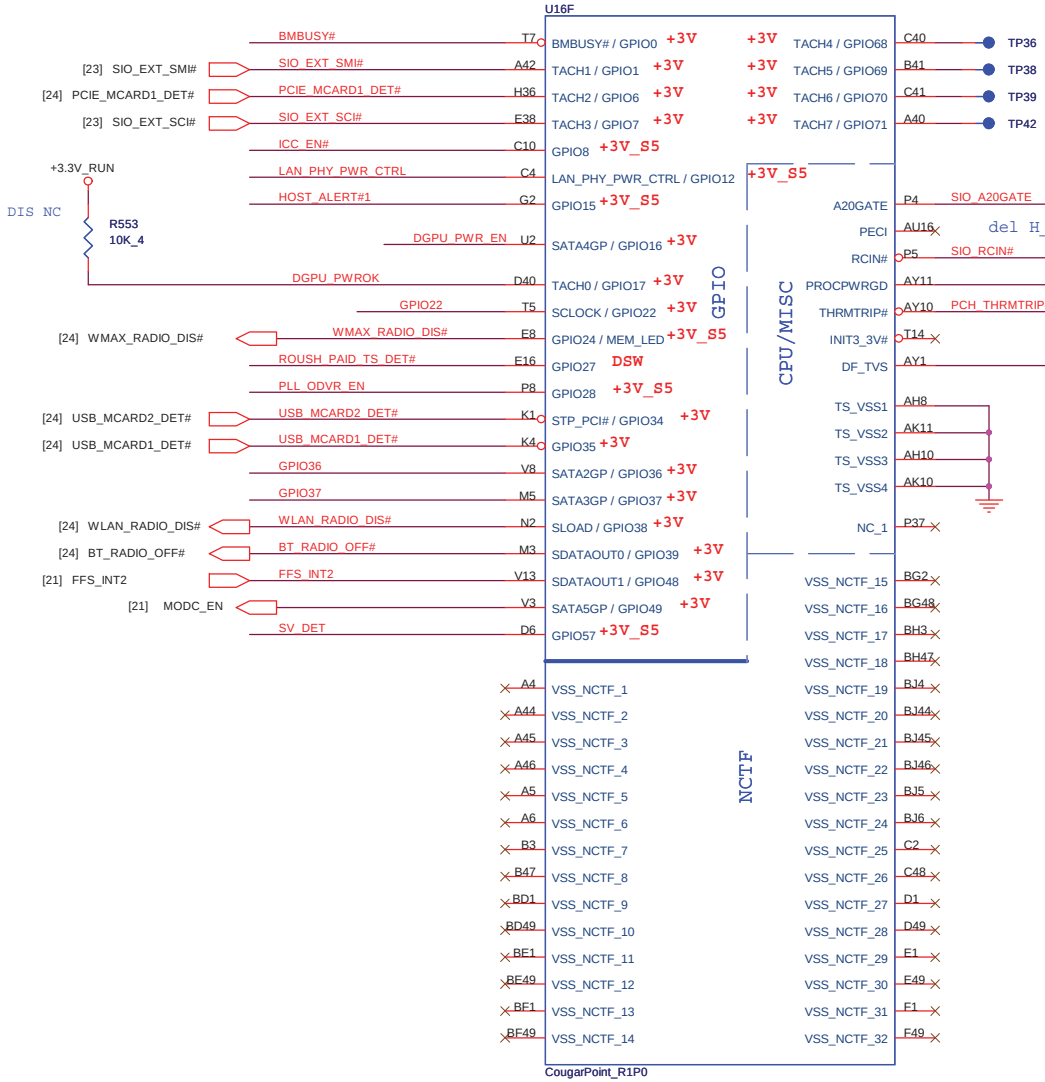
Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

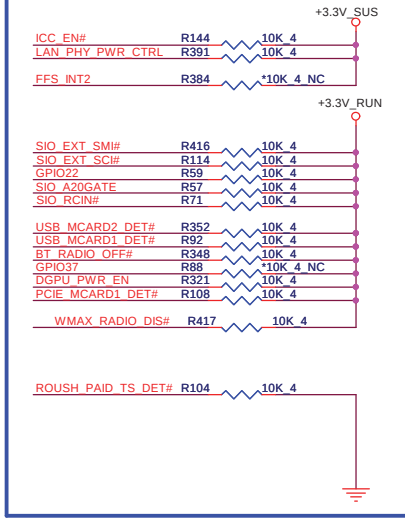
R70 *1K_4_NC PLL_ODVR_EN



Ask Intel, what's the function?

Add Description in EC GPIO table (keyboard controller reset)

GPIO Pull-up/Pull-down(CLG)



Can be del

+3.3V_SUS R377 *10K_4_NC SV_DET R380 100K_4

Have to Reserve

+3.3V_SUS HOST_ALERT#1 R381 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

GPIO36 R49 200K +3.3V_RUN

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

+3.3V_RUN BMBUSY# R58 10K_4

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

MFG-TEST Can be del

+3.3V_RUN WLAN_RADIO_DIS# R331 10K_4 R332 *0_4_NC

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COUGAR POINT (POWER)

Cougar Point (POWER)

Tie to 3.3V_SUS, when don't support Deep SX CP_v1.0 p88

VccCORE =1.14A(50mils)

VccADAC =1mA(8mils)

VccIO =2.925 A(120mils)

VccVRM(1.5V) =0.16 A(10mils)

VccDMI =0.042 A(10mils)

VccDSW3_3= 3mA(8mil)

VccASW =1.01A (50mils)

need 1206?

VccALVDS=1mA (8mils)

VccTX_LVDS=60mA (10mils)

Vcc3_3 = 0.266A (15mils)

VccDMI = 80mA (20mils)

VccCLKDMI = 20mA (8mils)

VCCPNAND = 190 mA(15mils)

VCCSPI = 20mA(8mils)

VCCVRM: 1.8V (Destop) 0.7/20 del for Pre-ES1
1.5V (Mobile)

the trace needs to be at least 20 mils width with full VSS/VCC reference plane.

Intel

Ask PD3 or Intel, why need 1ohm change to +/-5%

VCCSUS3_3 = 119mA (15mils)

VCC5REFSUS=1mA(8mil)

V5REF= 1mA(8mil)

VCCSUS3_3 = 119mA (15mils)

VCCPCORE = 28mA(10mils)

VCCVRM= 114mA(15mils)

VCCSUSHDA= 10mA(8mils)

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H=8.0mm,RVS

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

[6] M_A_A[15:0]

M_A_A0 98
M_A_A1 97
M_A_A2 96
M_A_A3 95
M_A_A4 92
M_A_A5 91
M_A_A6 90
M_A_A7 86
M_A_A8 89
M_A_A9 85
M_A_A10 107
M_A_A11 84
M_A_A12 83
M_A_A13 119
M_A_A14 80
M_A_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

[6] M_A_BS0 109
[6] M_A_BS1 108
[6] M_A_BS2 79
[6] M_A_CS#0 114
[6] M_A_CS#1 121
[6] M_A_CLKP0 101
[6] M_A_CLKN0 103
[6] M_A_CLKP1 102
[6] M_A_CLKN1 104
[6] M_A_CKE0 73
[6] M_A_CKE1 74
[6] M_A_CAS# 115
[6] M_A_RAS# 110
[6] M_A_WE# 113

BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

DIMM0_SA0 197
DIMM0_SA1 201

SA0 SA1

[13,17,21,24] WLAN_SCLK 202
[13,17,21,24] WLAN_SDATA 200

SCL SDA

[6] M_A_ODT0 116
[6] M_A_ODT1 120

ODT0 ODT1

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187

[6] M_A_DQSP[7:0]

M_A_DQSP0 12
M_A_DQSP1 29
M_A_DQSP2 47
M_A_DQSP3 64
M_A_DQSP4 137
M_A_DQSP5 154
M_A_DQSP6 171
M_A_DQSP7 188

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

[6] M_A_DQSN[7:0]

M_A_DQSN0 10
M_A_DQSN1 27
M_A_DQSN2 45
M_A_DQSN3 62
M_A_DQSN4 135
M_A_DQSN5 152
M_A_DQSN6 169
M_A_DQSN7 186

DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

M_A_DQ[63:0] [6]

DQ0 5 M_A_DQ5
DQ1 7 M_A_DQ4
DQ2 15 M_A_DQ3
DQ3 17 M_A_DQ2
DQ4 4 M_A_DQ1
DQ5 6 M_A_DQ0
DQ6 16 M_A_DQ6
DQ7 18 M_A_DQ7
DQ8 21 M_A_DQ8
DQ9 23 M_A_DQ9
DQ10 33 M_A_DQ15
DQ11 35 M_A_DQ10
DQ12 22 M_A_DQ12
DQ13 24 M_A_DQ13
DQ14 34 M_A_DQ14
DQ15 36 M_A_DQ11
DQ16 39 M_A_DQ17
DQ17 41 M_A_DQ16
DQ18 51 M_A_DQ18
DQ19 53 M_A_DQ19
DQ20 40 M_A_DQ21
DQ21 42 M_A_DQ20
DQ22 50 M_A_DQ22
DQ23 52 M_A_DQ23
DQ24 57 M_A_DQ25
DQ25 59 M_A_DQ28
DQ26 67 M_A_DQ30
DQ27 69 M_A_DQ31
DQ28 56 M_A_DQ24
DQ29 58 M_A_DQ29
DQ30 68 M_A_DQ26
DQ31 70 M_A_DQ27
DQ32 129 M_A_DQ33
DQ33 131 M_A_DQ32
DQ34 141 M_A_DQ35
DQ35 143 M_A_DQ34
DQ36 130 M_A_DQ36
DQ37 132 M_A_DQ37
DQ38 140 M_A_DQ39
DQ39 142 M_A_DQ38
DQ40 147 M_A_DQ40
DQ41 149 M_A_DQ41
DQ42 157 M_A_DQ43
DQ43 159 M_A_DQ47
DQ44 146 M_A_DQ44
DQ45 148 M_A_DQ45
DQ46 158 M_A_DQ42
DQ47 160 M_A_DQ46
DQ48 163 M_A_DQ48
DQ49 165 M_A_DQ49
DQ50 175 M_A_DQ54
DQ51 177 M_A_DQ55
DQ52 164 M_A_DQ52
DQ53 166 M_A_DQ53
DQ54 174 M_A_DQ51
DQ55 176 M_A_DQ50
DQ56 181 M_A_DQ56
DQ57 183 M_A_DQ60
DQ58 191 M_A_DQ58
DQ59 193 M_A_DQ59
DQ60 180 M_A_DQ57
DQ61 182 M_A_DQ61
DQ62 192 M_A_DQ63
DQ63 194 M_A_DQ62

JDIM1B

DDR3-DIMM0

+1.5V_SUS

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3.3V_RUN

VDDSPD 199

NC1 77
NC2 122
NCTEST 125

+3.3V_RUN R463 10K/F_4
[5,17] DDR3_DRAMRST# EVENT# 198 RESET# 30

M3 reserve

+SMDDR_VREF_DQ0 +SMDDR_VREF_DQ0 R14 *0_0603short_NC +SMDDR_VREF_DQ0_R
[8] SMDDR_VREF_DQ0_M3 R15 *0/J_6_NC +SMDDR_VREF_DIMM0 +SMDDR_VREF_DIMM0 1

VREF_DQ 126
VREF_CA

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +0.75V_DDR_VTT
VTT2 204

GND 207 GND 208 GND 205 GND 206

+3.3V_RUN

R210 *10K_4_NC DIMM0_SA0 R209 10K_4
R212 *10K_4_NC DIMM0_SA1 R211 10K_4

	DIMM0_SA0	DIMM0_SA1
DOMM0	0	0
DOMM1	0	1

S3 Power reduce

+0.75V_DDR_VTT

R164 22_4

Q9 BSS138-7-F

PS_S3CNTRL [5,7]

Place these Caps near So-Dimm0.

+1.5V_SUS

C137 *10U/6.3V/X5R_8_NC
C180 *10U/6.3V/X5R_8_NC
C539 *10U/6.3V/X5R_8_NC
C166 *10U/6.3V/X5R_8_NC
C490 10U/6.3V/X5R_8
C530 *10U/6.3V/X5R_8_NC
C103 0.1U/10V/X7R_4
C182 0.1U/10V/X7R_4
C202 0.1U/10V/X7R_4
C153 0.1U/10V/X7R_4
C160 0.1U/10V/X7R_4

+0.75V_DDR_VTT

C368 *1U/6.3V/X5R_4_NC
C350 *1U/6.3V/X5R_4_NC
C374 1U/6.3V/X5R_4
C353 1U/6.3V/X5R_4
C377 *10U/6.3V/X5R_8_NC
C378 *10U/6.3V/X5R_8_NC
C381 10U/6.3V/X5R_8

+3.3V_RUN

C342 2.2U/6.3V_6
C339 *0.1U/10V/X7R_4_NC

+SMDDR_VREF_DQ0_R

C18 0.1U/10V/X7R_4
C19 2.2U/6.3V_6

+SMDDR_VREF_DIMM0

C553 0.1U/10V/X7R_4
C550 2.2U/6.3V_6

For RF noise

+0.75V_DDR_VTT

C359 *47P/50V_4_NC
C360 *47P/50V_4_NC

+1.5V_SUS

C105 *47P/50V_4_NC
C104 *47P/50V_4_NC
C136 *47P/50V_4_NC
C96 *47P/50V_4_NC
C168 *47P/50V_4_NC

M1 VREF

+1.5V_SUS +DDR_VTTREF

R20 1K/F
R23 *0_4_NC
+SMDDR_VREF_DQ0
R18 1K/F
C25 0.1U

+1.5V_SUS +DDR_VTTREF

R426 1K/F
R441 *0_4_NC
+SMDDR_VREF_DIMM0
R436 1K/F
C552 0.1U

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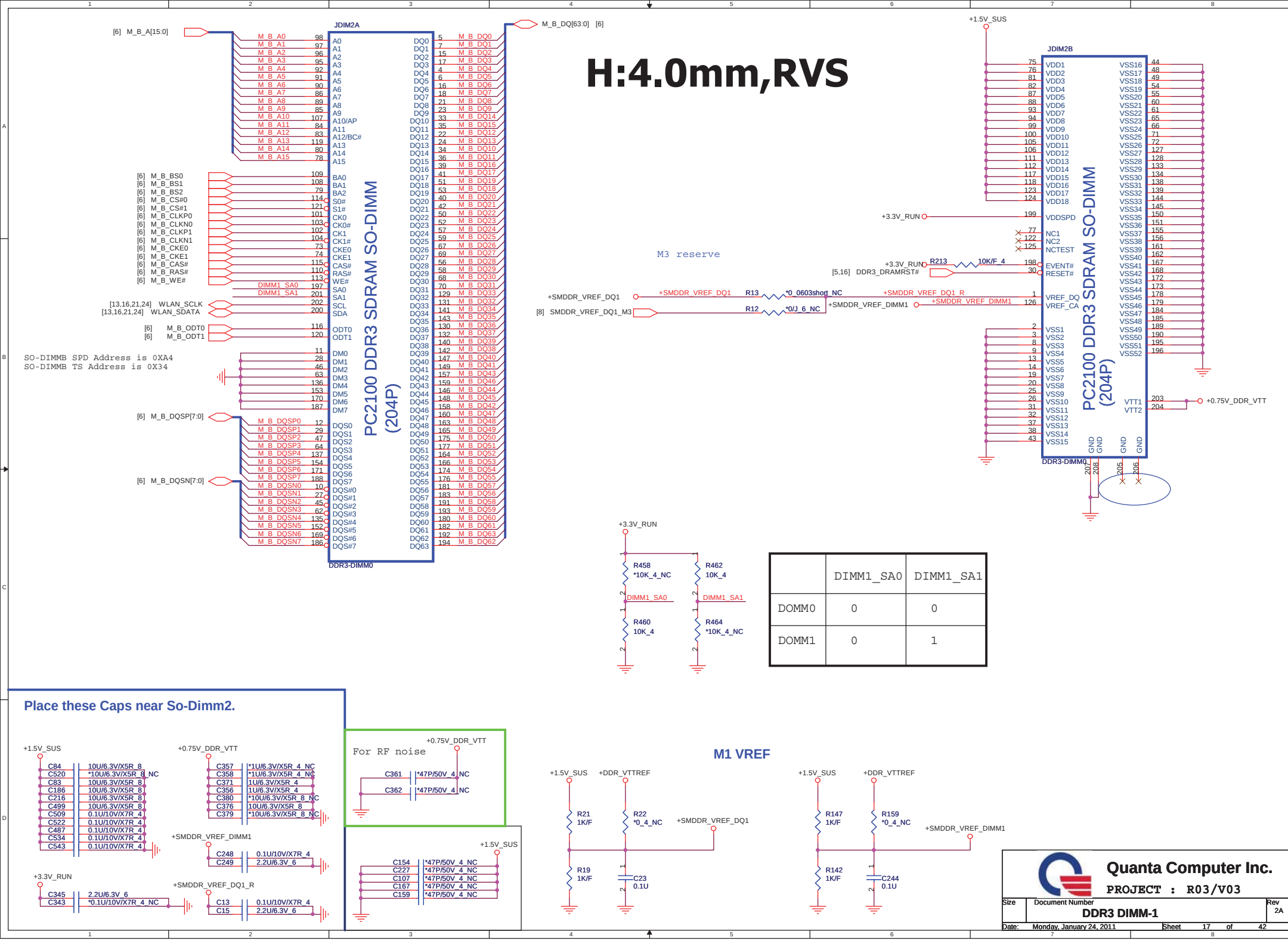
H:4.0mm,RVS



	DIMM1_SA0	DIMM1_SA1
DOMM0	0	0
DOMM1	0	1

Place these Caps near So-Dimm2.

M1 VREF

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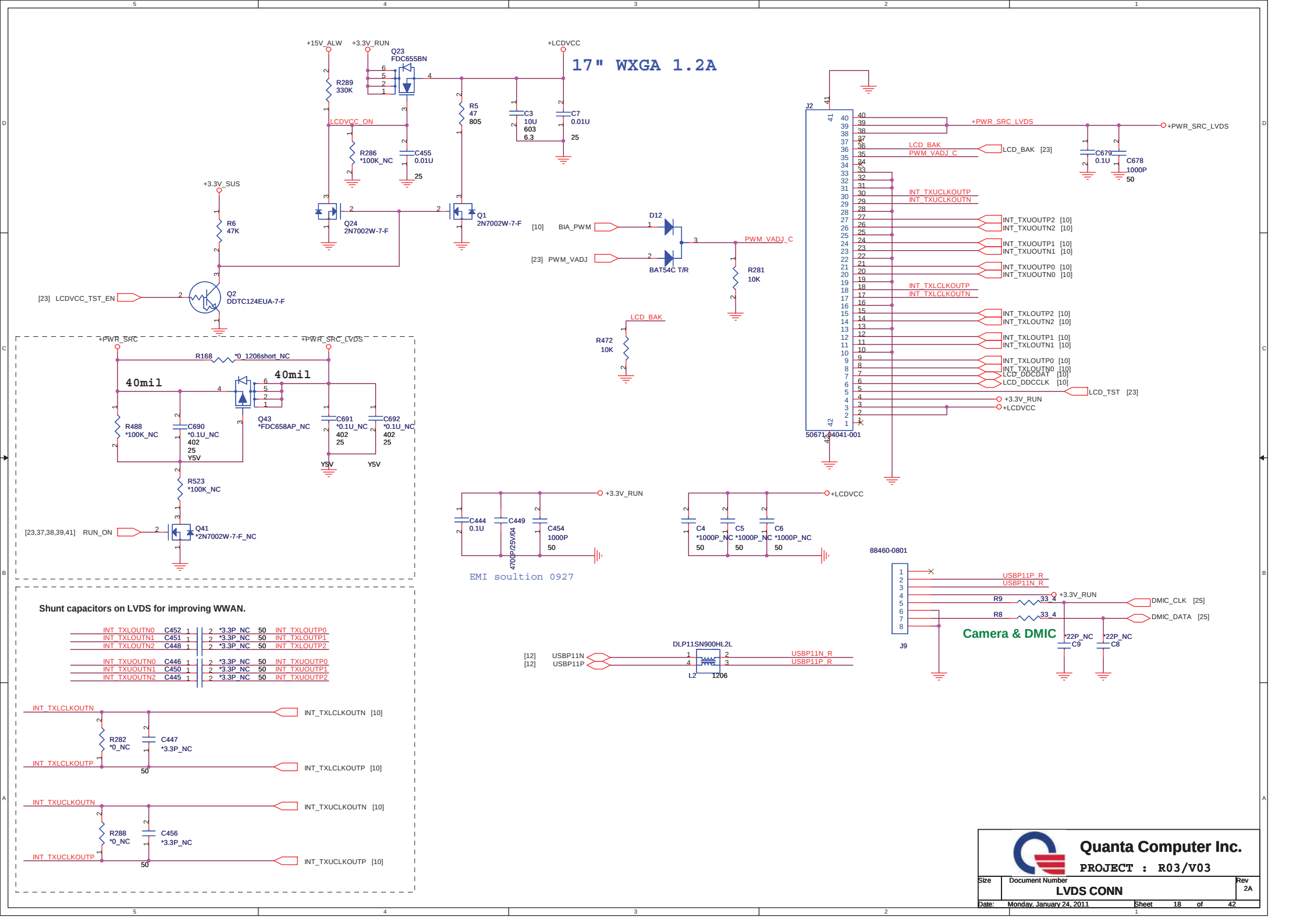
17" WXGA 1.2A
+15V_ALW
+3.3V_RUN
+LCDVCC
Q23
FDC655BN
R289
330K
LCDVCC_ON
R286
*100K_NC
C455
0.01U
25
R5
47
805
C3
10U
603
6.3
C7
0.01U
25
+3.3V_SUS
R6
47K
Q24
2N7002W-7-F
Q1
2N7002W-7-F
[23] LCDVCC_TST_EN
Q2
DDTC124EUA-7-F
[10] BIA_PWM
[23] PWM_VADJ
D12
BAT54C T/R
PWM_VADJ_C
R281
10K
R472
10K
LCD_BAK
J2
50671-04041-001
+PWR_SRC_LVDS
LCD_BAK [23]
C679
0.1U
C678
1000P
50
INT_TXUCLKOUTP
INT_TXUCLKOUTN
INT_TXUOUTP2 [10]
INT_TXUOUTN2 [10]
INT_TXUOUTP1 [10]
INT_TXUOUTN1 [10]
INT_TXUOUTP0 [10]
INT_TXUOUTN0 [10]
INT_TXLCLKOUTP
INT_TXLCLKOUTN
INT_TXLOUTP2 [10]
INT_TXLOUTN2 [10]
INT_TXLOUTP1 [10]
INT_TXLOUTN1 [10]
INT_TXLOUTP0 [10]
INT_TXLOUTN0 [10]
LCD_DDCDAT [10]
LCD_DDCCLK [10]
LCD_TST [23]
+3.3V_RUN
+LCDVCC
+PWR_SRC
+PWR_SRC_LVDS
R168
*0_1206short_NC
40mil
40mil
R488
*100K_NC
C690
*0.1U_NC
402
25
Y5V
Q43
*FDC658AP_NC
C691
*0.1U_NC
402
25
C692
*0.1U_NC
402
25
R523
*100K_NC
[23,37,38,39,41] RUN_ON
Q41
*2N7002W-7-F_NC
C444
0.1U
C449
470P/25V/04
C454
1000P
50
EMI soultion 0927
C4
*1000P_NC
50
C5
*1000P_NC
50
C6
*1000P_NC
50
88460-0801
J9
USBP11P_R
USBP11N_R
R9
33_4
R8
33_4
DMIC_CLK [25]
DMIC_DATA [25]
Camera & DMIC
*22P_NC
C9
*22P_NC
C8
DLP11SN900HL2L
L2
1206
[12] USBP11N
[12] USBP11P
Shunt capacitors on LVDS for improving WWAN.
INT_TXLOUTN0 C452 *3.3P_NC 50 INT_TXLOUTP0
INT_TXLOUTN1 C451 *3.3P_NC 50 INT_TXLOUTP1
INT_TXLOUTN2 C448 *3.3P_NC 50 INT_TXLOUTP2
INT_TXUOUTN0 C446 *3.3P_NC 50 INT_TXUOUTP0
INT_TXUOUTN1 C450 *3.3P_NC 50 INT_TXUOUTP1
INT_TXUOUTN2 C445 *3.3P_NC 50 INT_TXUOUTP2
INT_TXLCLKOUTN
R282
*0_NC
C447
*3.3P_NC
INT_TXLCLKOUTP
50
INT_TXLCLKOUTN [10]
INT_TXLCLKOUTP [10]
INT_TXUCLKOUTN
R288
*0_NC
C456
*3.3P_NC
INT_TXUCLKOUTP
50
INT_TXUCLKOUTN [10]
INT_TXUCLKOUTP [10]
Quanta Computer Inc.
PROJECT : R03/V03
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LVDS CONN
Rev
2A
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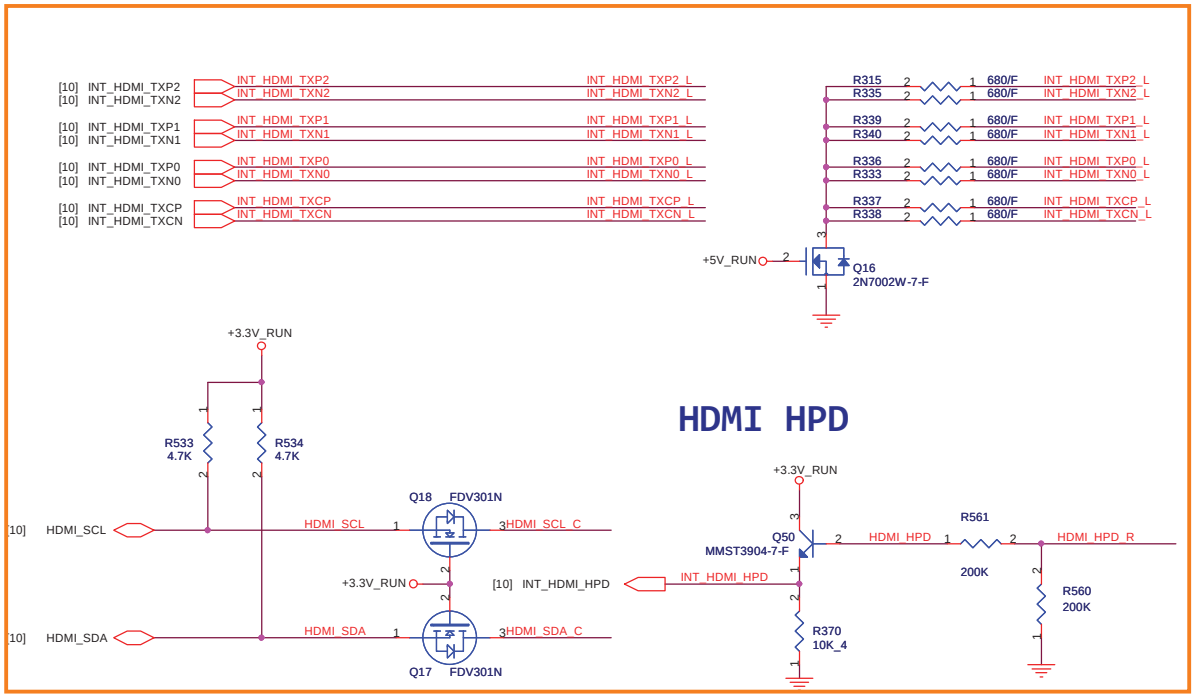

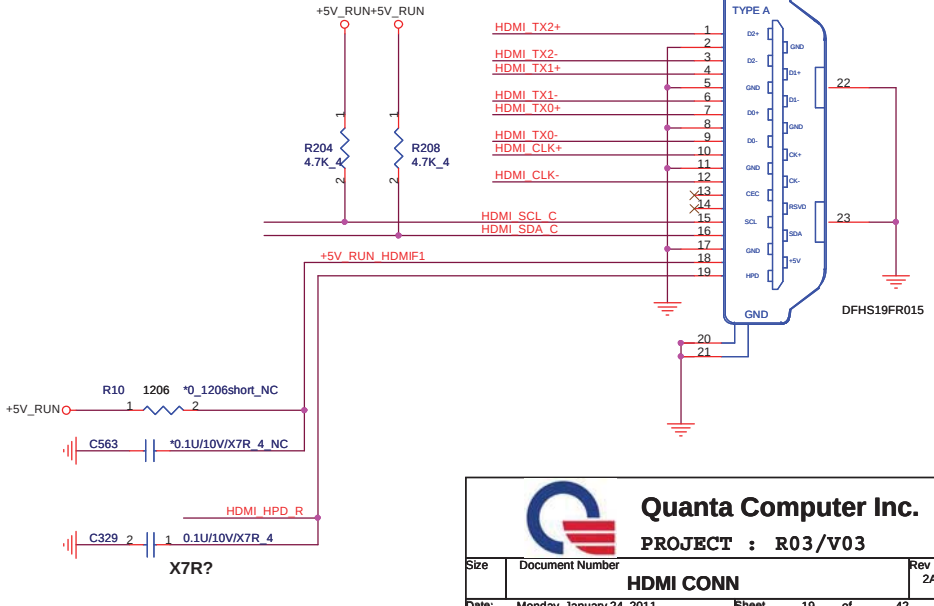

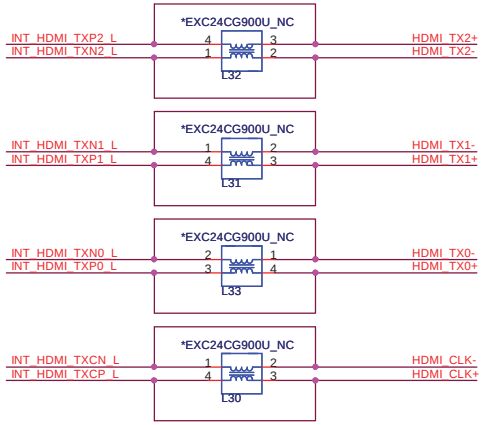

Quanta Computer Inc.

PROJECT : R03/V03

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	HDMI CONN	2A

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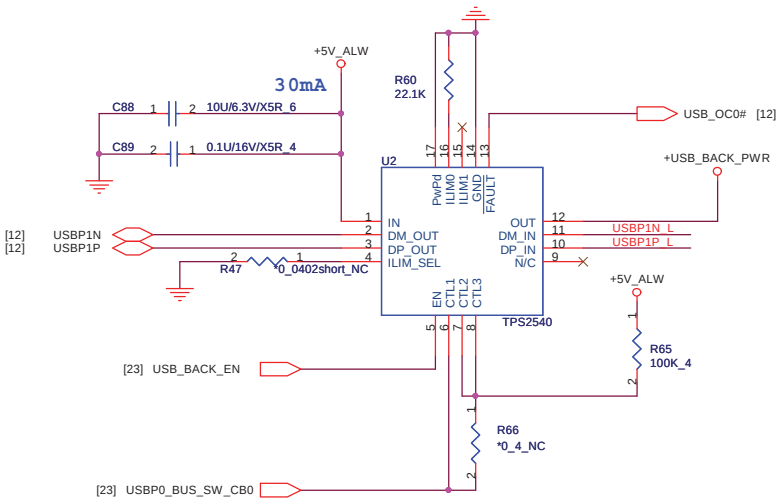
ESATA + USB Conn + Power share

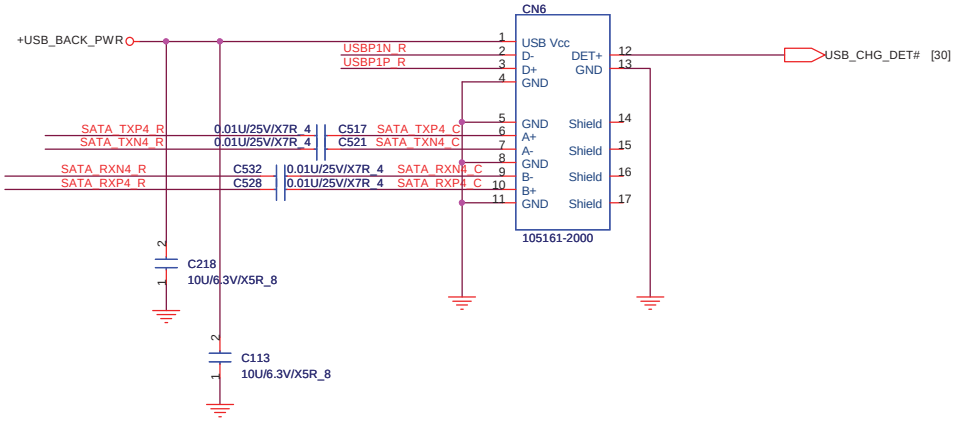
S3/S5 USB charging circuit

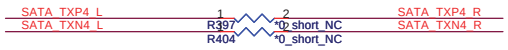


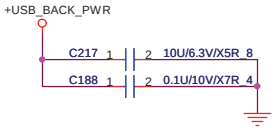
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

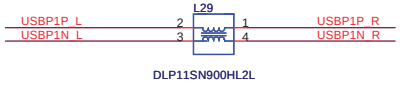
ES(PG1.0): Stuff R66, Remove R65
MP(PG1.1): Remove R66, Stuff R65

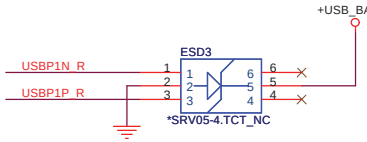
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now





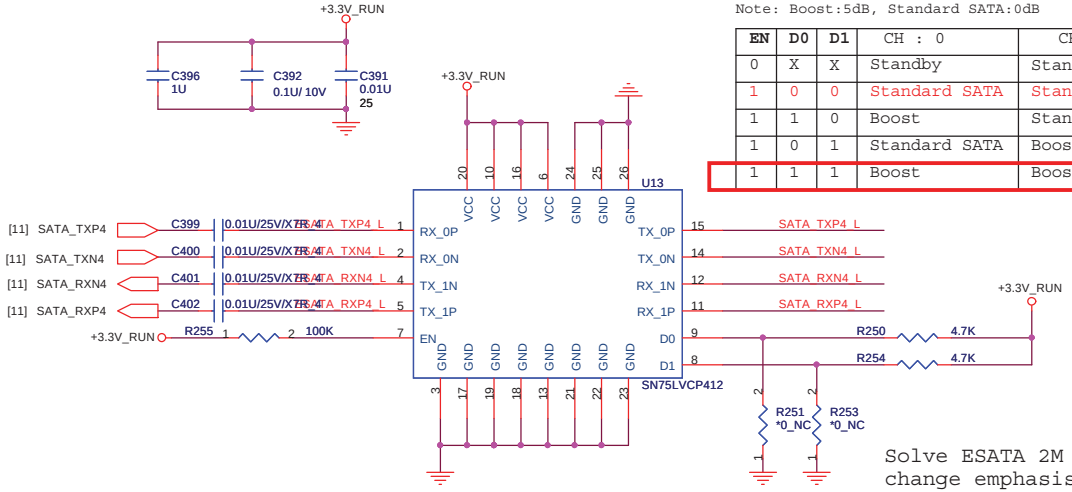






E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Solve ESATA 2M test fail issue, change emphasis setting

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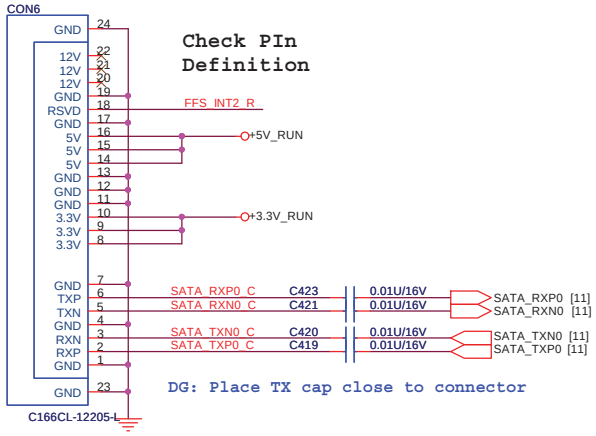
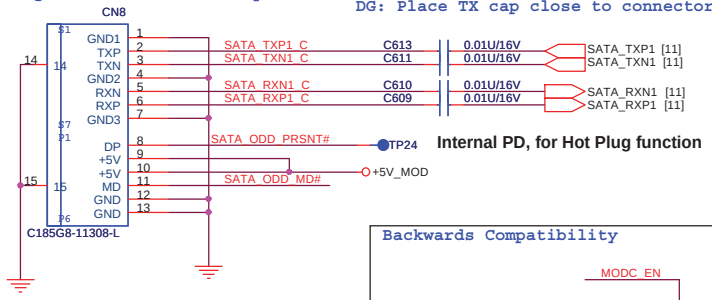
SATA Connector UM8

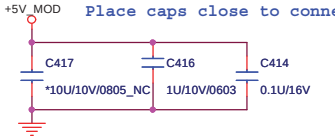


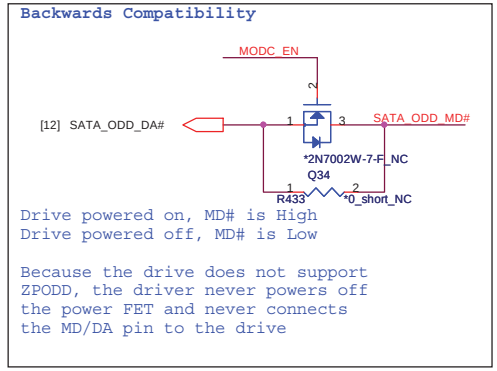
ODD Connector

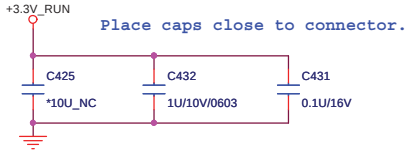
Change connector as ME request

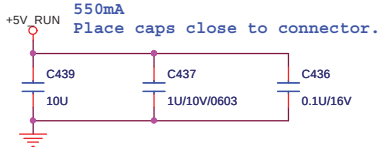
DG: Place TX cap close to connector



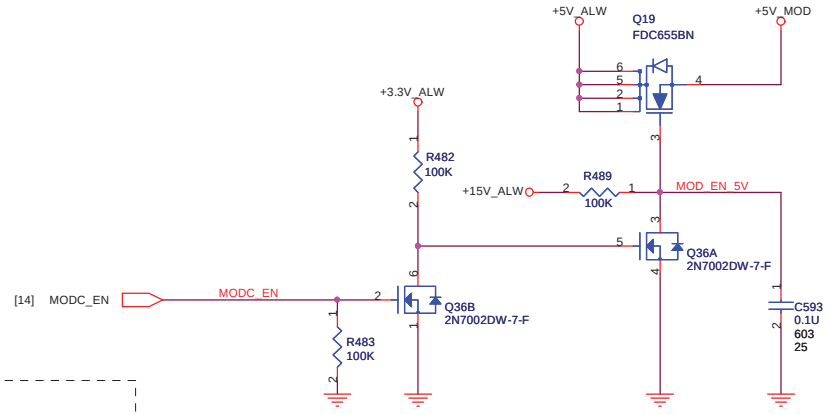


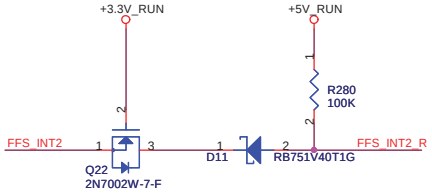


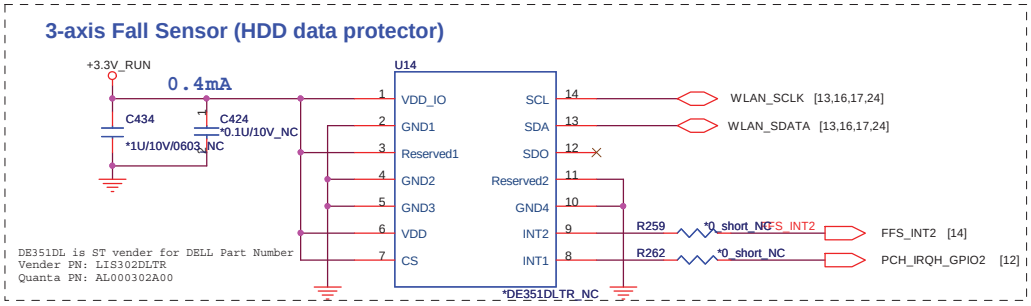




change RUN to ALW, change TRANS MOS for cost down







From FM9

Quanta Computer Inc.

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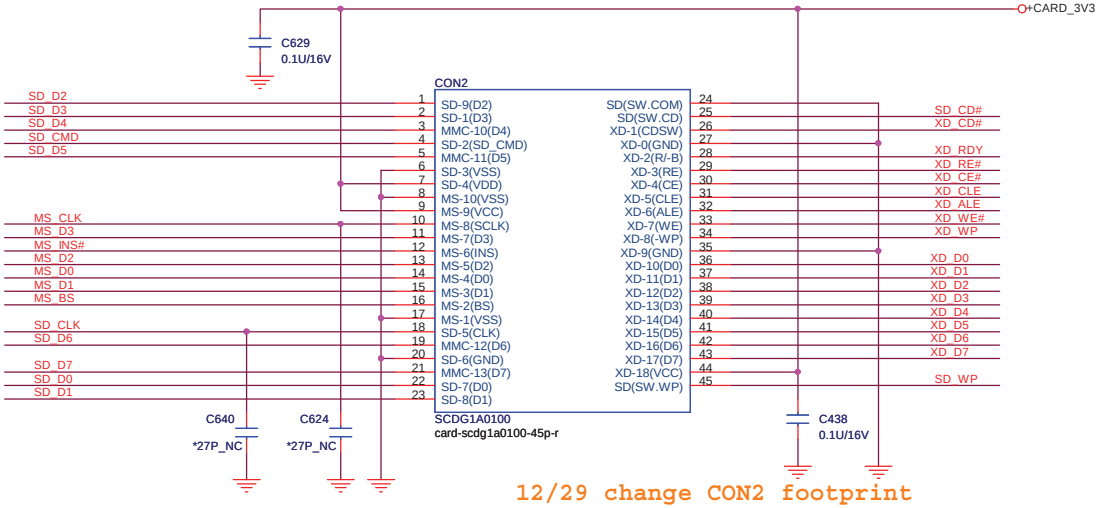
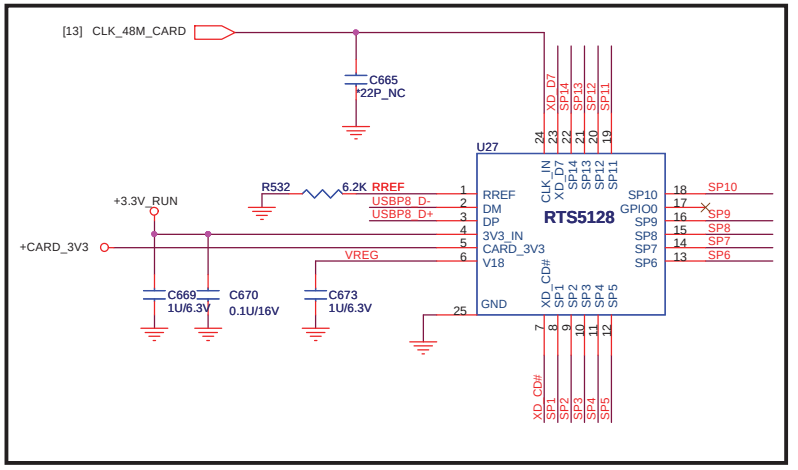
RTS5128-QFN24

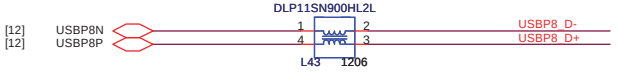


12/29 change CON2 footprint



SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



Quanta Computer Inc.

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	Cardreader (RTS5128)	2A

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CLK_33M_KBC
R207 10
C346 2.2P

+RTC_CELL
*0_0402short_NC R219
C355 0.1U/10V/X7R_4
+3.3V_ALW_AVCC
+RTC_VBAT1
+3.3V_ALW
+3.3V_RUN

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

U9

BAT1_LED [29]
ALW_ON [30,36]
EC_PWROK [9]
CAP_LED# [29]
ACZ_RST#_AUDIO [11,25]
IGFX_PWRGD [40]
BID0
*0_0402short_NC R455
USB_BACK_EN [20]
ADAPT_TRIP_SET [35]
CLKRUN# [9]

H_PROCHOT# Q R177 *0_0402short_NC H_PROCHOT# [5,35,40]
H_PROCHOT# EC
Q15 2N7002W-7-F
R197 100K/J_4

+3.3V_ALW
SMBDAT0 R239 2.2K_4
SMBCLK0 R238 2.2K_4
SMBDAT1 R241 10K/F_4
SMBCLK1 R240 10K/F_4
PCIE_EC_WAKE# R457 10K/F_4
USB_LEFT_EN# R237 10K/F_4

[11,24] LPC_LAD0
[11,24] LPC_LAD1
[11,24] LPC_LAD2
[11,24] LPC_LAD3
[5,12,24] PLTRST#
[12] CLK_33M_KBC
[11,24] LPC_LFRAME#
LPC
[18] LCD_TST
[14] SIO_A20GATE
[11] IRQ_SERIRQ
[14] SIO_EXT_SMI#
[14] SIO_EXT_SCI#
WRST#
[14] SIO_RCIN#
[30] USB_CHG_DET#_R
D6 RB751V40T1G
D20 RB751V40T1G
D1 RB751V40T1G
D5 RB751V40T1G

SM BUS
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
PECI/SMCLK2/WUI22/GPF6
SMDAT2/WUI23/GPF7
PS/2
PS2CLK0/TMB0/GPF0
PS2DAT0/TMB1/GPF1
PS2CLK2/WUI20/GPF4
PS2DAT2/WUI21/GPF5
GPIO
SMCLK0 [34,35]
SMDAT0 [34,35]
SMCLK1 [13]
SMDAT1 [13]
PECI_EC [5]
ENVDD [10]
PCH_MELOCK [11]
CLK_TP_SIO [28]
DAT_TP_SIO [28]
Charge ,BAT PCH

SUS_ON R233 100K_4
IMVP_VR_ON R178 *100K_4_NC
PANEL_BKEN R459 100K_4
KB_BACKLITE_EN R179 10K/F_4
HOT_KEY_LED1 R451 10K_4
HOT_KEY_LED2 R446 10K_4
HOT_KEY_LED3 R449 10K_4

[9,40] IMVP_PWRGD
[18,37,38,39,41] RUN_ON
CIR
CRX0/GPC0
CTX0/TMA0/GPB2

IT8518

PWM
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
BREATH_LED [29,30]
HOT_KEY_LED1 [24]
PWM_VADJ [18]
HOT_KEY_LED2 [24]
KB_BACKLITE_EN [28]

+3.3V_RUN
SMBDAT3 R221 2.2K_4
SMBCLK3 R217 2.2K_4
HOT_KEY1# R200 2.2K_4
Inspiron & Vostro R453
HOT_KEY3# R453 2.2K_4
LAN_PCIE_PWR_CTRL# R554 2.2K_4

[9] RSMRST#
[25,26] NB_MUTE#
[18] LCDVCC_TST_EN
[24,30] HOT_KEY3#
[9] SIO_PWRBTN#
[34] PS_ID
[24] USB_LEFT_EN#
[28] TP_LED2
R454 0_0402 INSTANT_ON
D3 RB751V40T1G
TACH0A/GPD6
TACH1A/TMA1/GPD7
LAN_PCIE_PWR_CTRL#
1.5V_SUS_PWRGD [37]
TMRI0/WUI2/GPC4
TMRI1/WUI3/GPC6
LID_SW# [28]
SIO_SLP_S3# [7,9]

UART port
[34] PBAT_PRES#
[35] IINP
[9] SIO_SLP_S5#
[29] BAT2_LED
[25] BEEP
MODEL_ID
[31] SMBDAT3
[31] SMBCLK3
ADC5/DCD1#/WUI29/GPI5
ADC6/DSR1#/WUI30/GPI6
ADC7/CTS1#/WUI31/GPI7
RTS1#/WUI5/GPE5
PWM7/RIG1#/GPA7
DTR1#/SBUSY/GPG1/ID7
CTX1/WUI18/SOUT1/GPH2/SMDAT3/ID2
CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1

WAKE UP
PWRSW/GPE4
RI1#/WUI0/GPD0
RI2#/WUI1/GPD1
R203 *100K_4_NC +3.3V_ALW
RB751V40T1G D2
SYS_PWR_SW# [30]
LCD_BAK [18]
ACAV_IN [30,35]
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
AC_PRESENT [9]

change BAT1_LED to BAT2_LED
Thermal

EXTERNAL SERIAL FLASH
EC_FLASH_SPI_CLK_R
[27] EC_FLASH_SPI_CS#
[27] EC_FLASH_SPI_DIN
[27] EC_FLASH_SPI_DO
FSCK
FSCE#
FMOSI
FMISO

change BID2 to ENVDD as BIOS's request
change USB_BACK_EN change to BID0

add instant function
KSO16
[40] IMVP_VR_ON
[24] HOT_KEY_LED3
KSO16/SMOSI/GPC3
KSO17/SMISO/GPC5
PWM6/SSCK/GPA6

A/D D/A
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/WUI28/GPI4
HWPG [9,31,32]
H_CPUDET# [5]
ME_SUS_PWR_ACK [9]
HOT_KEY1# [24]
PANEL_BKEN [10]

[37,41] SUS_ON
[28] KB_DET#
SPI ENABLE
SSCE0#/GPG2
SSCE1#/GPG0

GPJ0
GPJ1
DAC2/TACH0B/GPJ2
DAC3/TACH1B/GPJ3
USBP0_BUS_SW_CB0 [20]
SIO_EXT_WAKE# [12]
PCIE_EC_WAKE# [24]
HOT_KEY2_EC# [30]

Board ID Straps
DIS
Vostro
UMA
Inspiron
R242 *10K_4_NC
R235 *10K_4_NC
R231 10K_4
R227 10K_4
R243 10K_4
R236 10K_4
R232 *10K_4_NC
R224 *10K_4_NC

USB_BACK_EN	ADAPT_TRIP_SET	V03
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)

R454 (Vostro support Instant ON function)	
Vostro	De-POP
Inspiron	POP

+3.3V_ALW
R470 100K_4
WRST#
C574 1U/10V/X5R_6

KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KBMX
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSO0/STB#
KSO1/AFD#
KSO2/INIT#
KSO3/SLIN#
KSO4
KSO5
KSO6
KSO7

CLOCK
CK32KE
CK32K
For Crystal-Free

[28] KSO[0..16]
[28] KSI[0..7]
[30] INSTANT_ON
INSTANT_ON

VSS
VCORE
AVSS
ITE8502IX_JX
C348 0.1U/10V/X7R_4

[27] EC_FLASH_SPI_CLK
R234 *0_short_NC
EC_FLASH_SPI_CLK_R
C382 *22P_NC

+3.3V_ALW
L12 BLM11A05S 603
+3.3V_ALW_AVCC
C328 0.1U/10V/X7R_4
L13 BLM11A05S 603

C286 10U/6.3V/X5R_8
C567 10U/6.3V/X5R_8
C383 0.1U/16V_4
C566 0.1U/16V_4
C351 0.1U/16V_4
Place these caps close to ITE8518.

Quanta Computer Inc.
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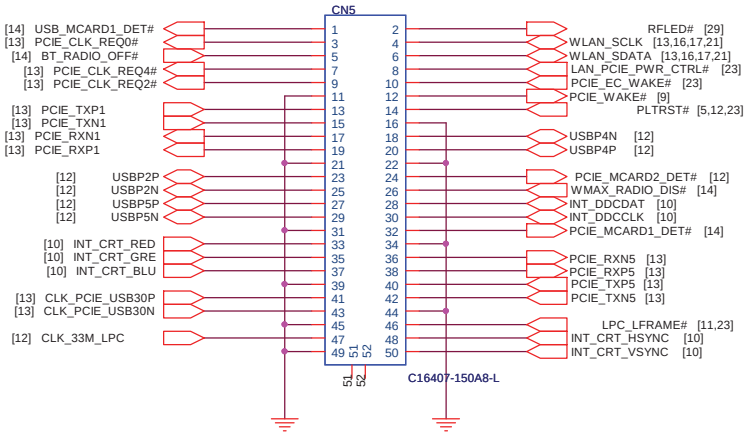
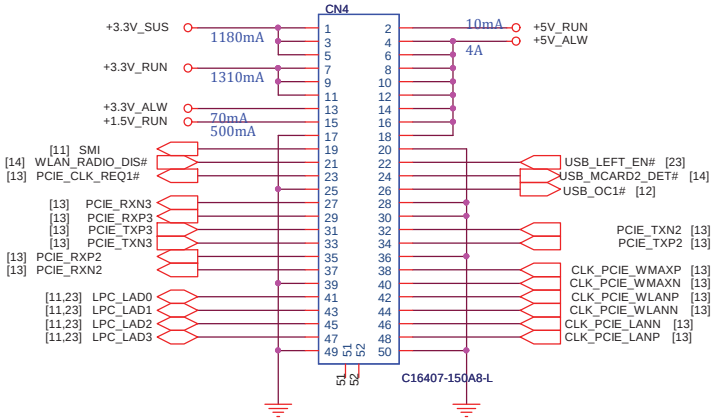
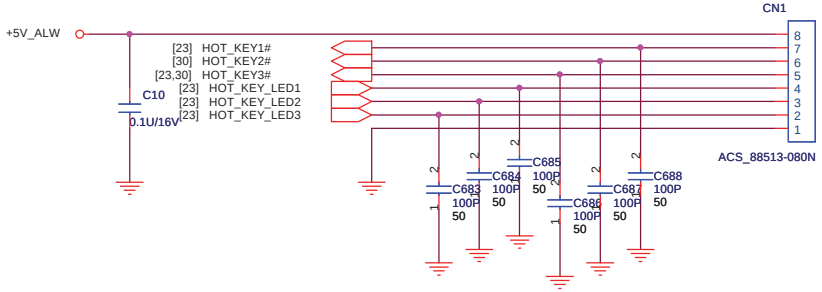


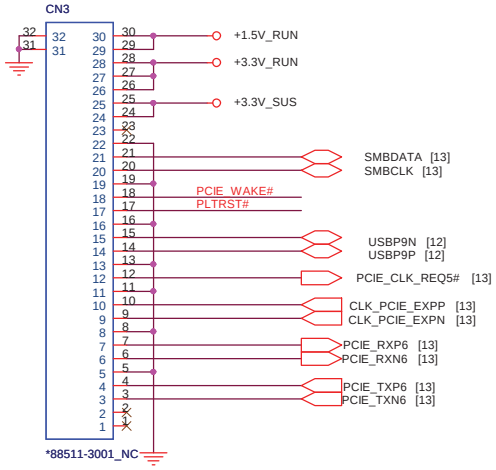


HOTKEY CON



EMI solution

MB to Express Card Board



Quanta Computer Inc.

PROJECT : R03/V03

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*NOTE: ALC269_VB type add the LDO circuit in IC
VA type: PIN28 作爲MIC之偏壓
PIN31接A-GND

VB type: PIN31 作爲MIC之偏壓
PIN28接CAP作爲內部LDO
output 輸出濾波用

AVDD1, AVDD2 TYP=48mA

AVDD1, AVDD2 TYP=48mA

ALC269Q VB6

ALC269Q-VB6-GR

Analog Plane

Digital Plane

reserve EMI solution

DVDD & DVDD-IO TYP=50mA

del 0ohm NC 0928

please close to ALC269 Pin 28

must close to ALC269 Pin12

modify single net GND SIGNAL

Trace width >= 40mil, Trace length < 20cm

Int. Stereo Speakers

5V / 4 Ohm / 2W

L34.L35,L36,L37,
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC

AUDIOJACK-SIT_NORMALOPEN_2
Normal Open
HP JACKN

POP noise VB6 fixed,
keep NC first

AUDIOJACK-SIT_NORMALOPEN_2
Normal Open
MIC JACK

PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.

Reserve RC for EMI

Digital GND Analog GND

Quanta Computer Inc.
PROJECT : R03/V03

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	Azelia CODEC	2A
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INTERNAL SUBWOOFER AMP Only for 17''

SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

3W

3W 4ohm device(subwoofer)

MAX9759 TQFN 16PIN

MAX9759ETE+

Change to X7R

GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB

MAX4492AUD need to change part?

reserve EMI solution

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Layout Note: Place close to pin 8.

place close to connector side

Quanta Computer Inc.			
PROJECT : R03/V03			
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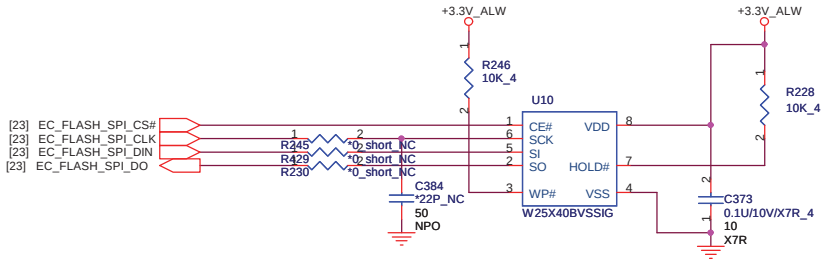
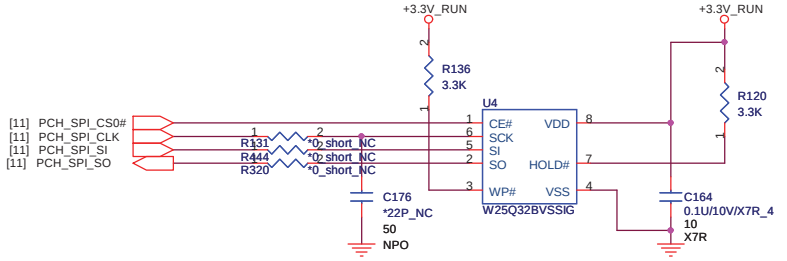
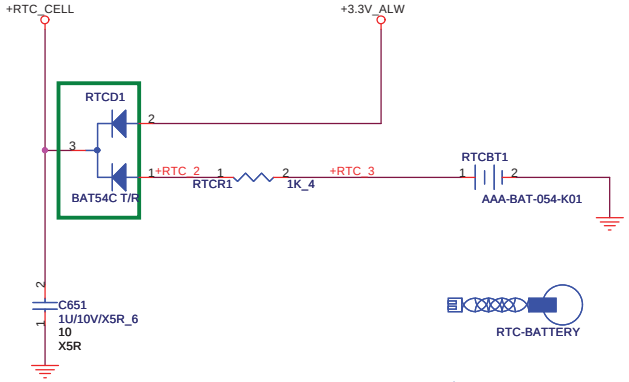
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC

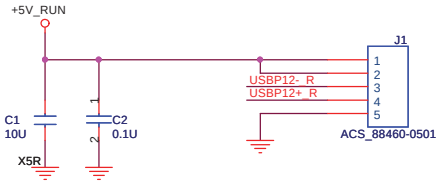


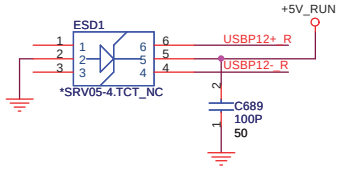
james command change part number

Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

Touch Screen Module

Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.





Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: FLASH / RTC	Rev: 2A
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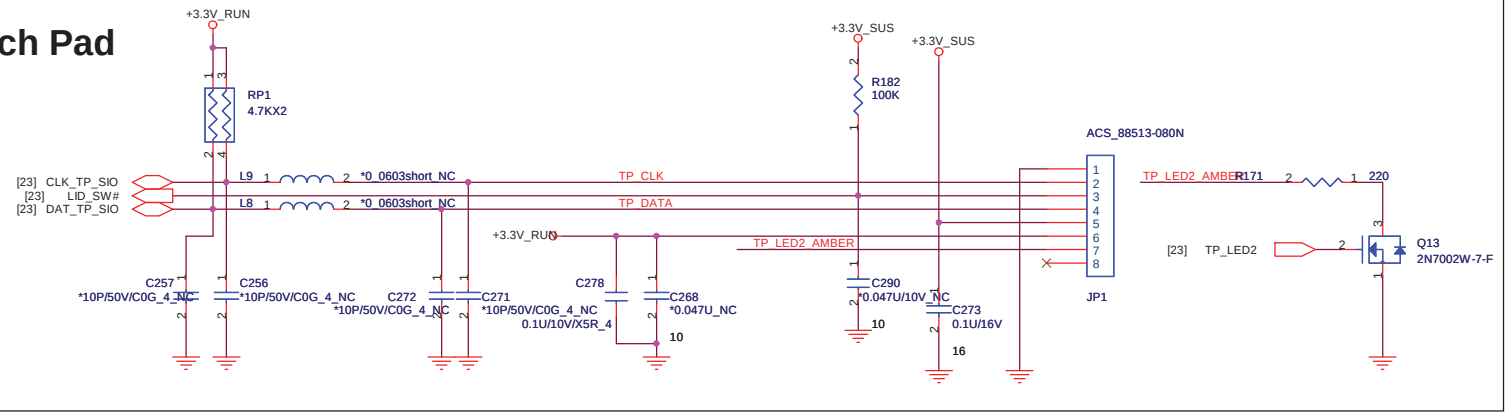
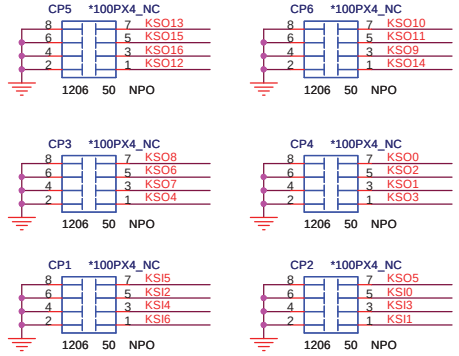
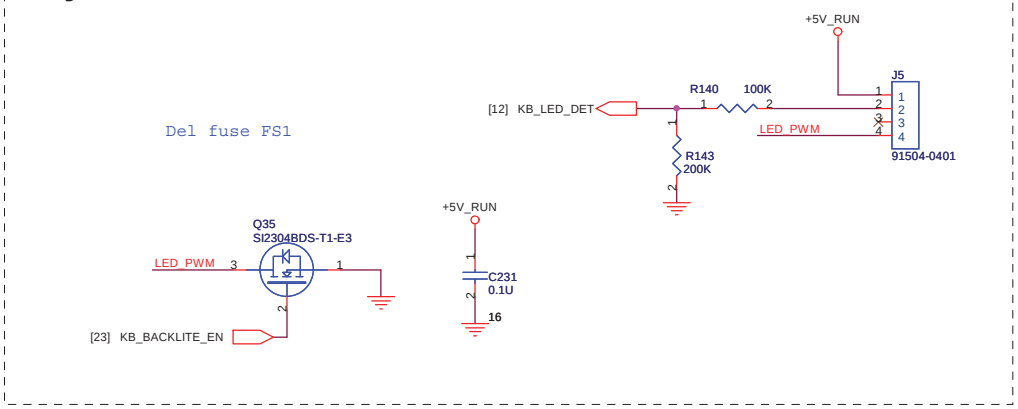
Touch Pad

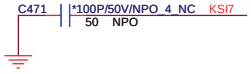




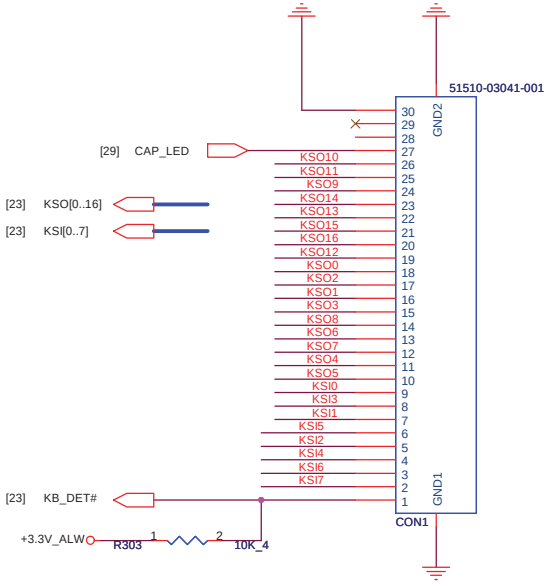
Key board illumination

+KB_LED power trace width >10 mil

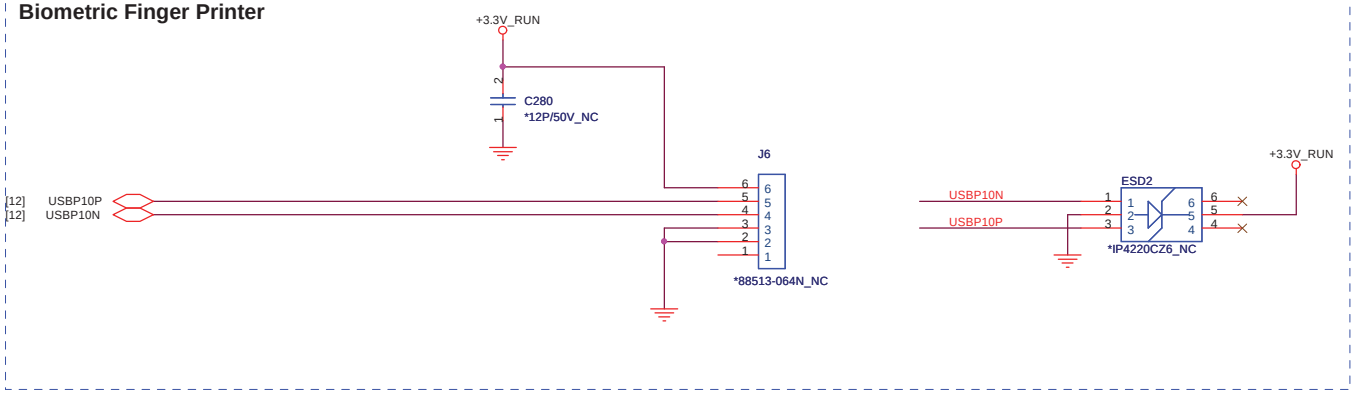




KEYBOARD CONNECTOR



Biometric Finger Printer



Quanta Computer Inc.			
PROJECT : R03/V03			
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	TP / KB		2A
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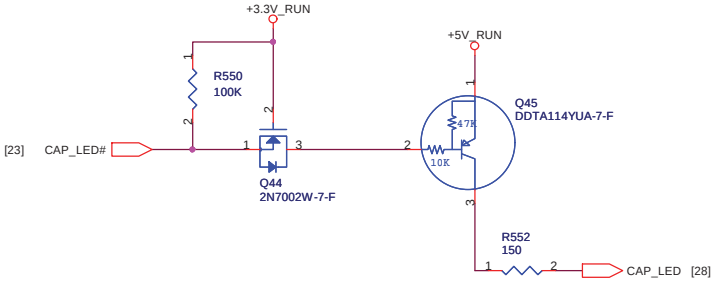
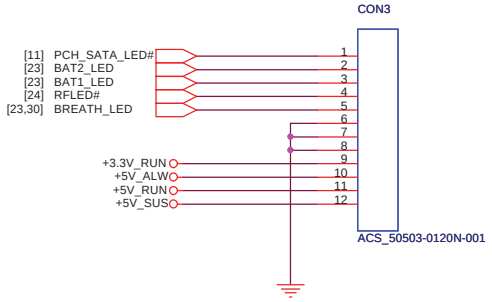
CAP lock LED



MB to LED Board conn



Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: LED	Rev 2A
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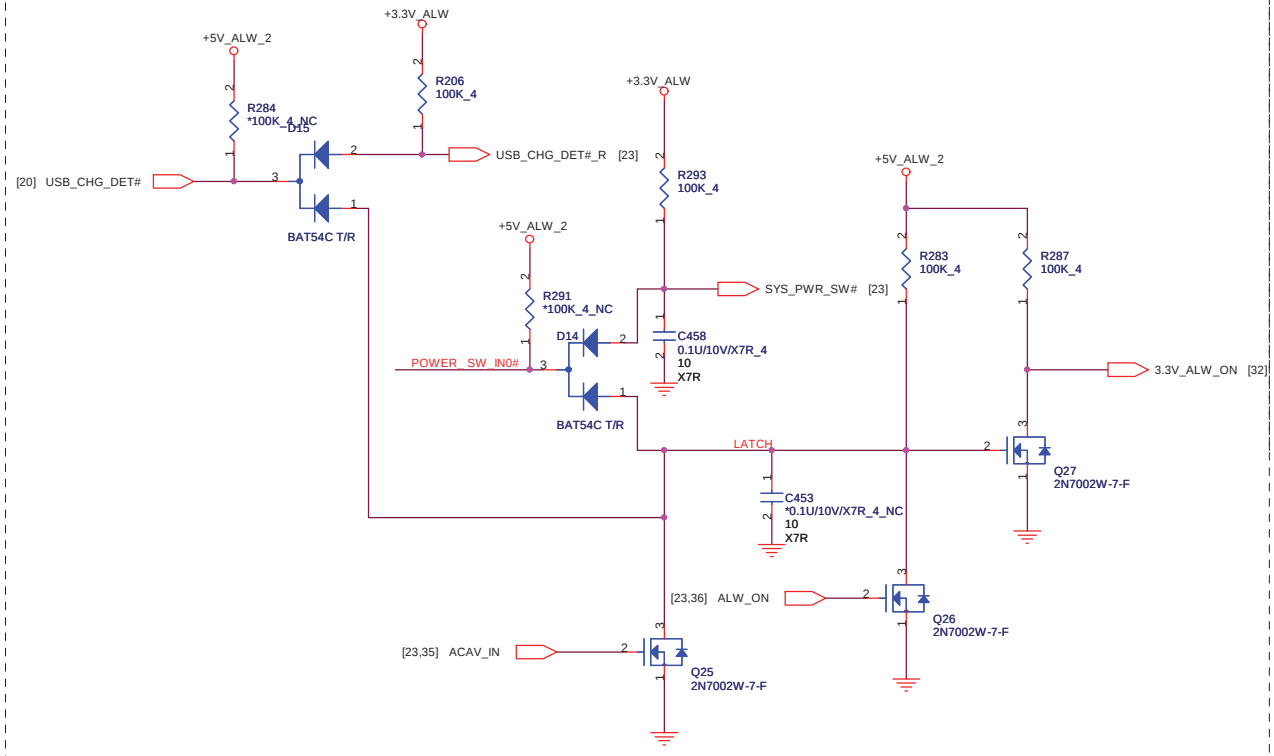
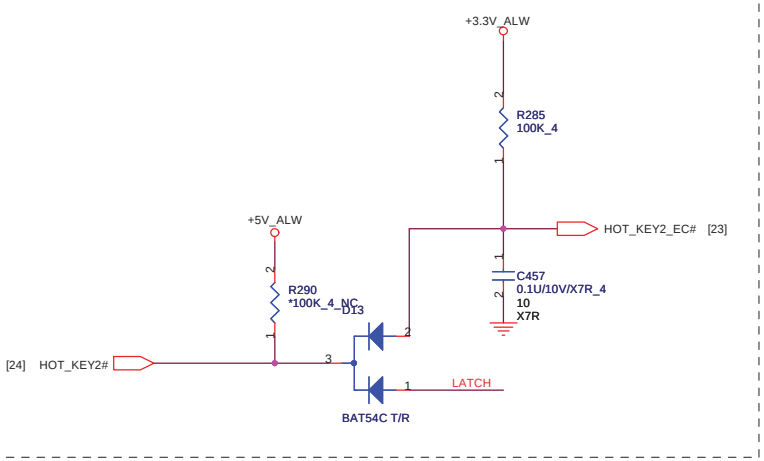
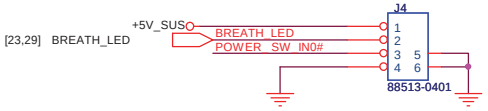
3VALW ON POWER LOGIC

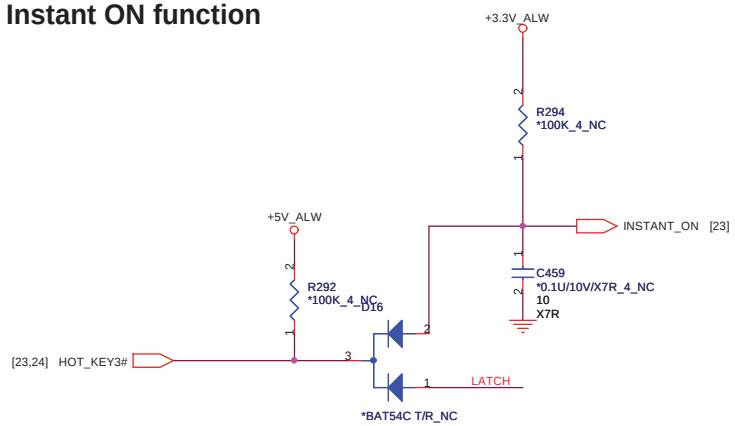




PWR button board form UM7



Instant ON function



Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	PWR SW/LED	2A

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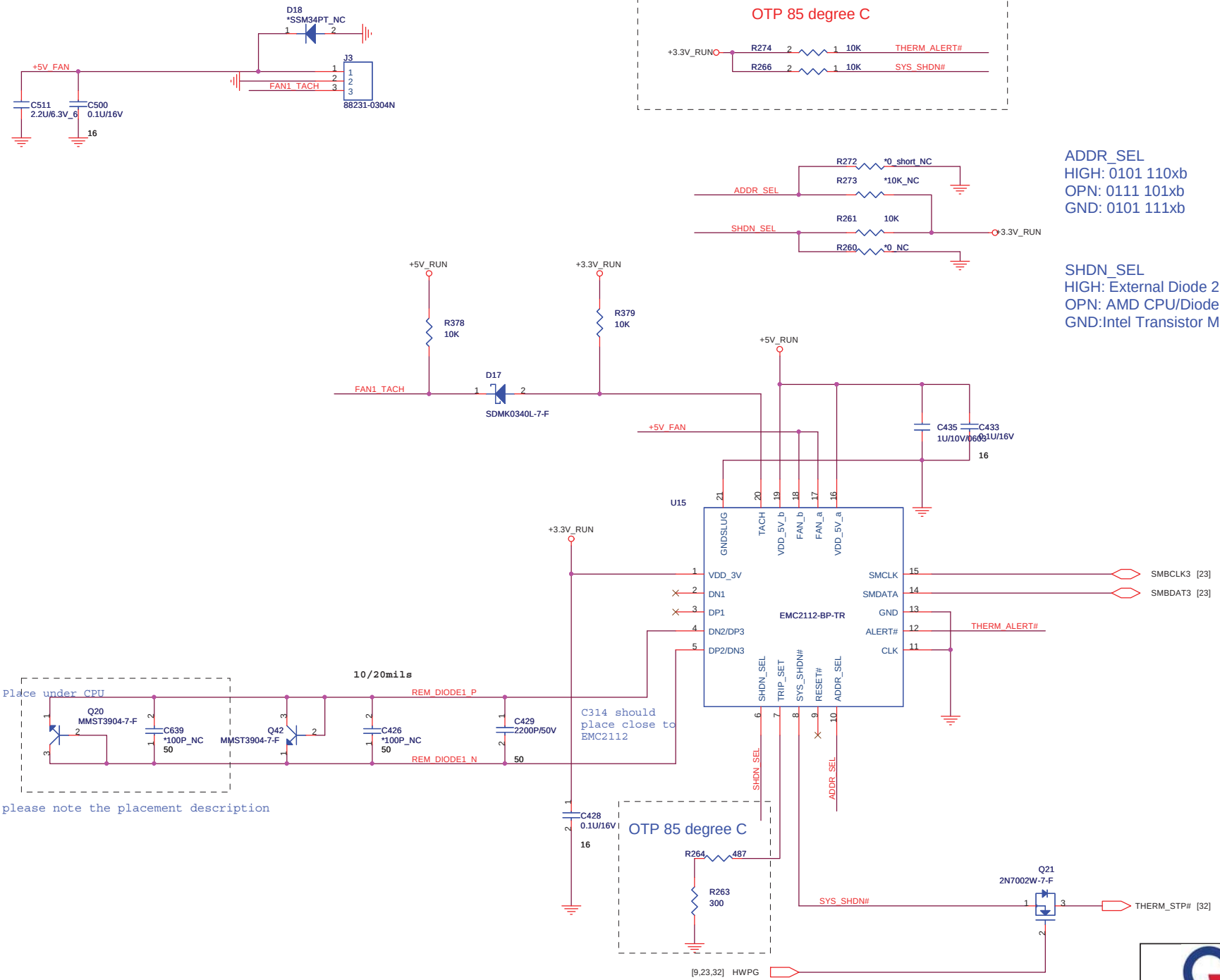
FAN CONTROL



Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: FAN & THERMAL	Rev 2A
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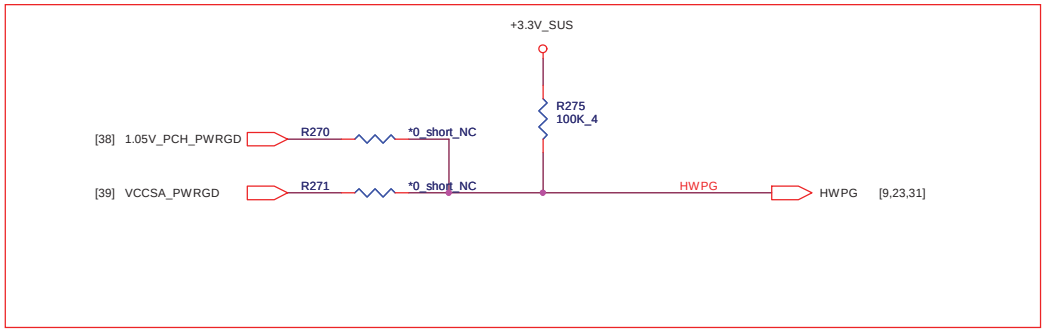

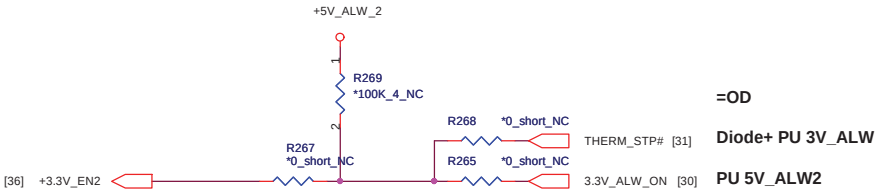

=OD

Diode+ PU 3V_ALW

PU 5V_ALW2

Quanta Computer Inc.

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Size	Document Number	Rev
	System Reset Circuit	2A
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H2
H-TC236BC197D110P2
H-TC236BC197D110P2

H7
H-TC236BC197D110P2
H-TC236BC197D110P2

H14
h-tc335bc276d126p2
h-tc335bc276d126p2

H5
h-tc335bc276d126p2
h-tc335bc276d126p2

H8
h-c276d177p2
h-c276d177p2

H12
h-c276d126p2
h-c276d126p2

H19
H-C276IN130D110P2
H-C276IN130D110P2

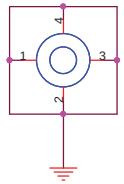
H17
H-C276IN130D110P2
H-C276IN130D110P2

H16
h-c354d126p2
h-c354d126p2

H15
h-t354i130b296d110p2
H-T354I130B296D110P2

CPU bracket

H10 Intel-cpu-bkt2
Intel-cpu-bkt2



H18
H-C142D142N
H-C142D142N

H6, H11 on the button side

H20
h-c295d126p2
h-c295d126p2

H6
h-tc197bc236d102p2
h-tc236bc197d102p2

H11
h-tc197bc236d102p2
h-tc236bc197d102p2

H4
H-T236I130B276D110P2
H-T236I130B276D110P2

H24
H-TC276BC236D110P2
H-TC276BC236D110P2

H1
h-c142d142n
h-c142d142n

H3
H-T315I130B276D110P2
H-TC335BC276D126P2

H22
h-c205d91pt
H-C276D110PT

Quanta Computer Inc.

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Size	Document Number	Rev
	SCREW PAD	2A
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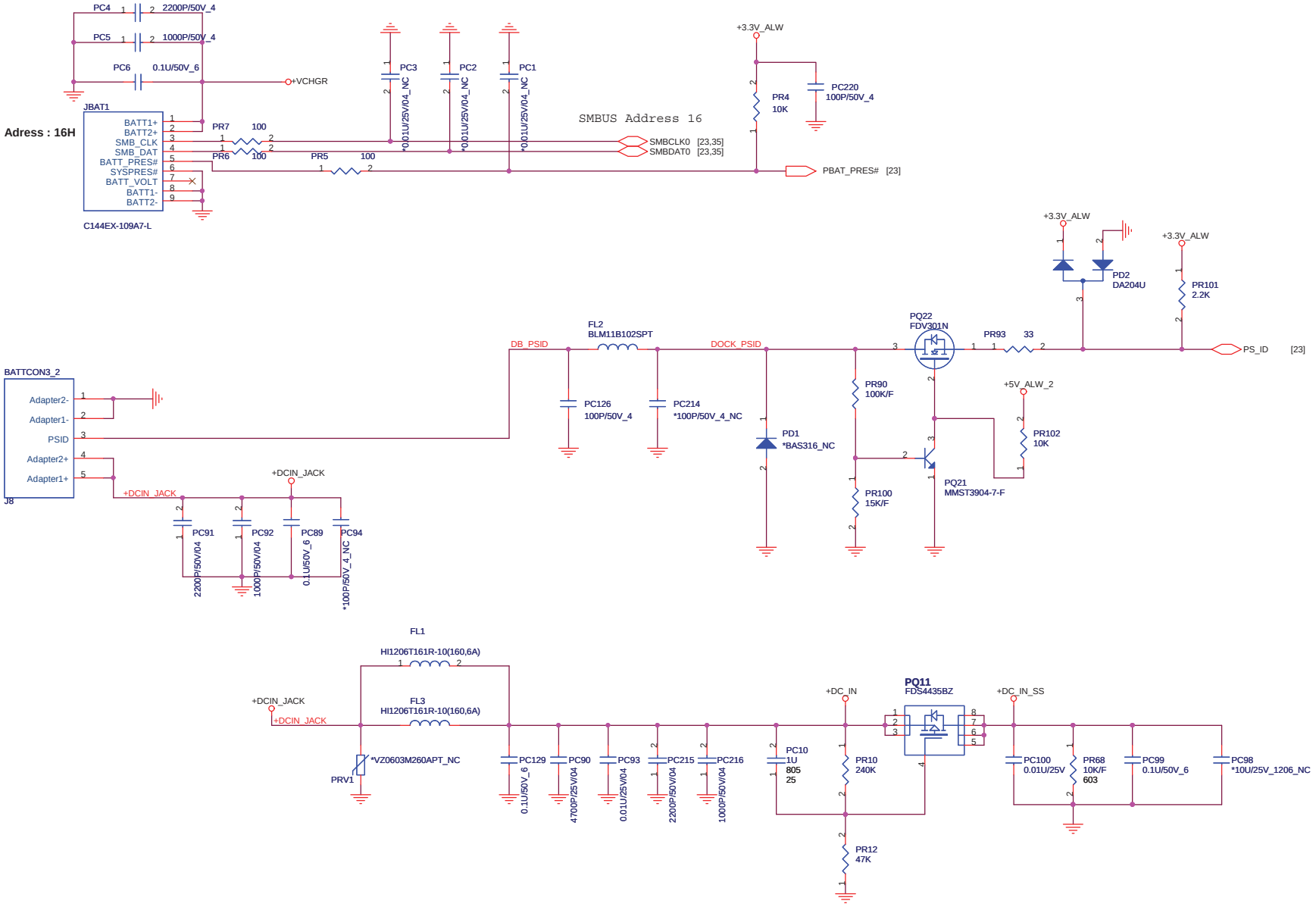
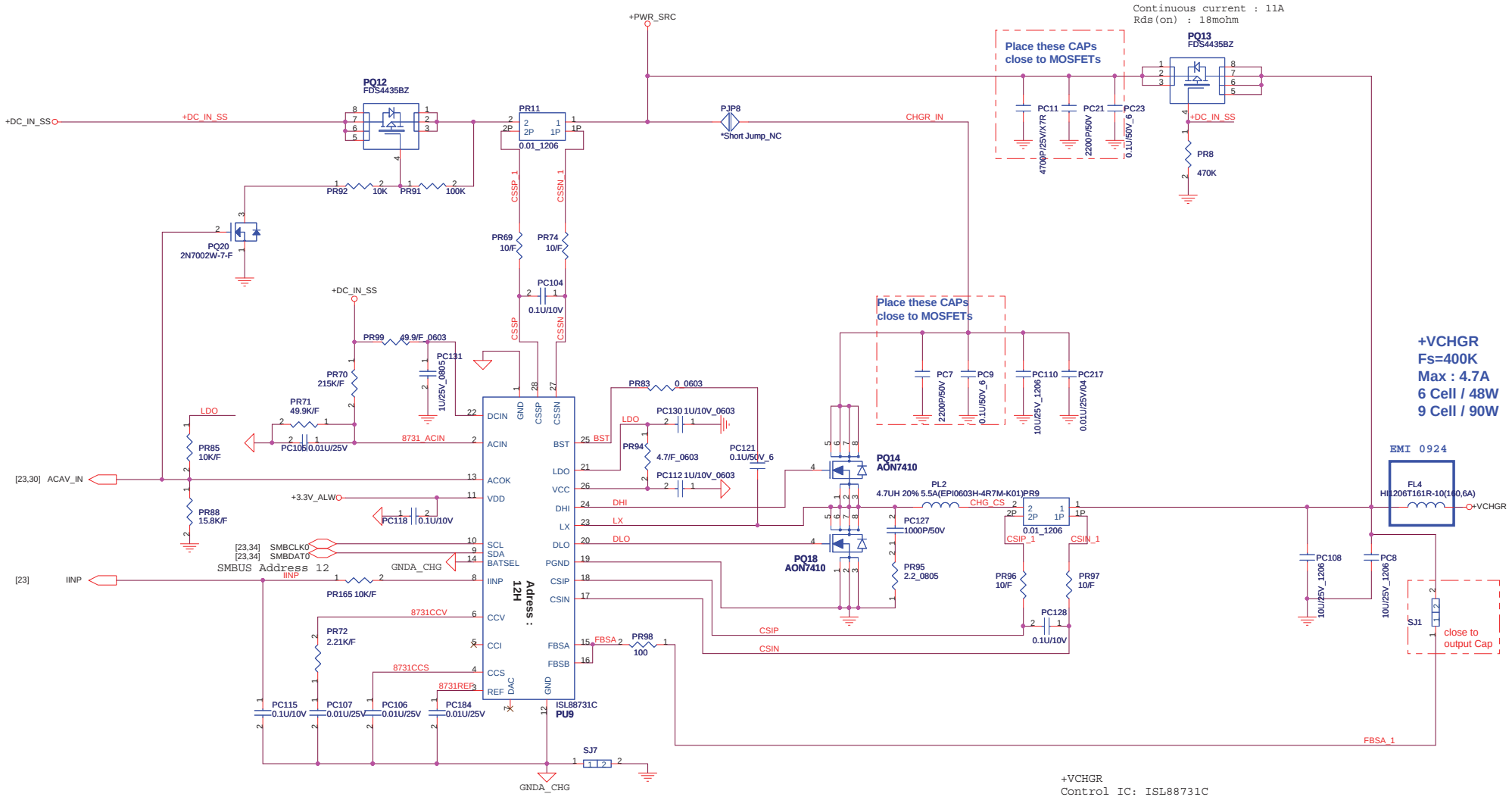


Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: DCIN,BATT CONNECTOR	Rev: 2A
Date: Monday, January 24, 2011	Sheet 34 of 42	



+VCHGR
Control IC: ISL88731C
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 5.8UH +-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=22mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number	Rev
	Charger (ISL88731C)	2A
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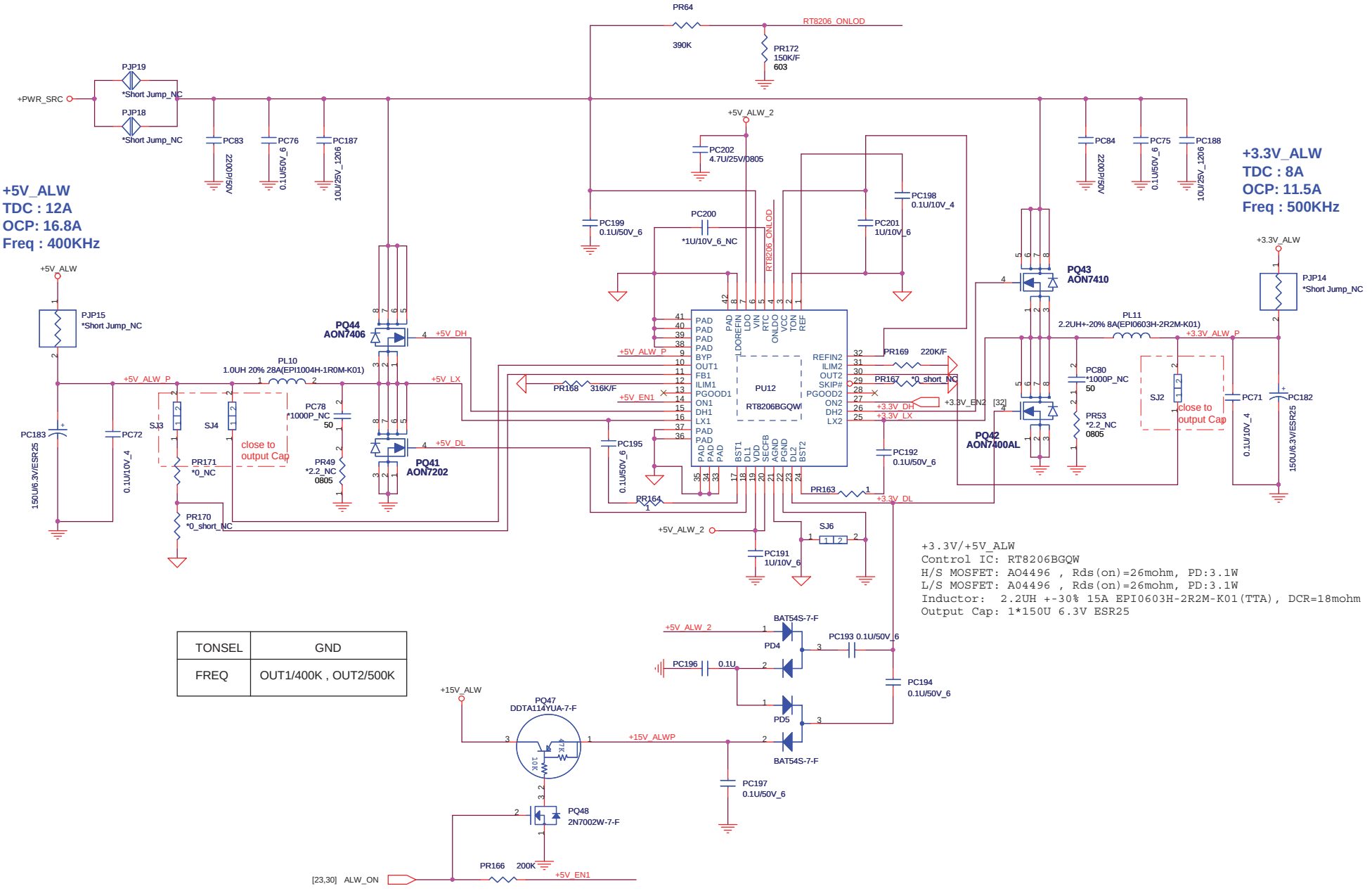
DC/DC +3V_ALW/+5V_ALW /+15V_ALW



TONSEL	GND
FREQ	OUT1/400K , OUT2/500K

Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206BGQW)	2A
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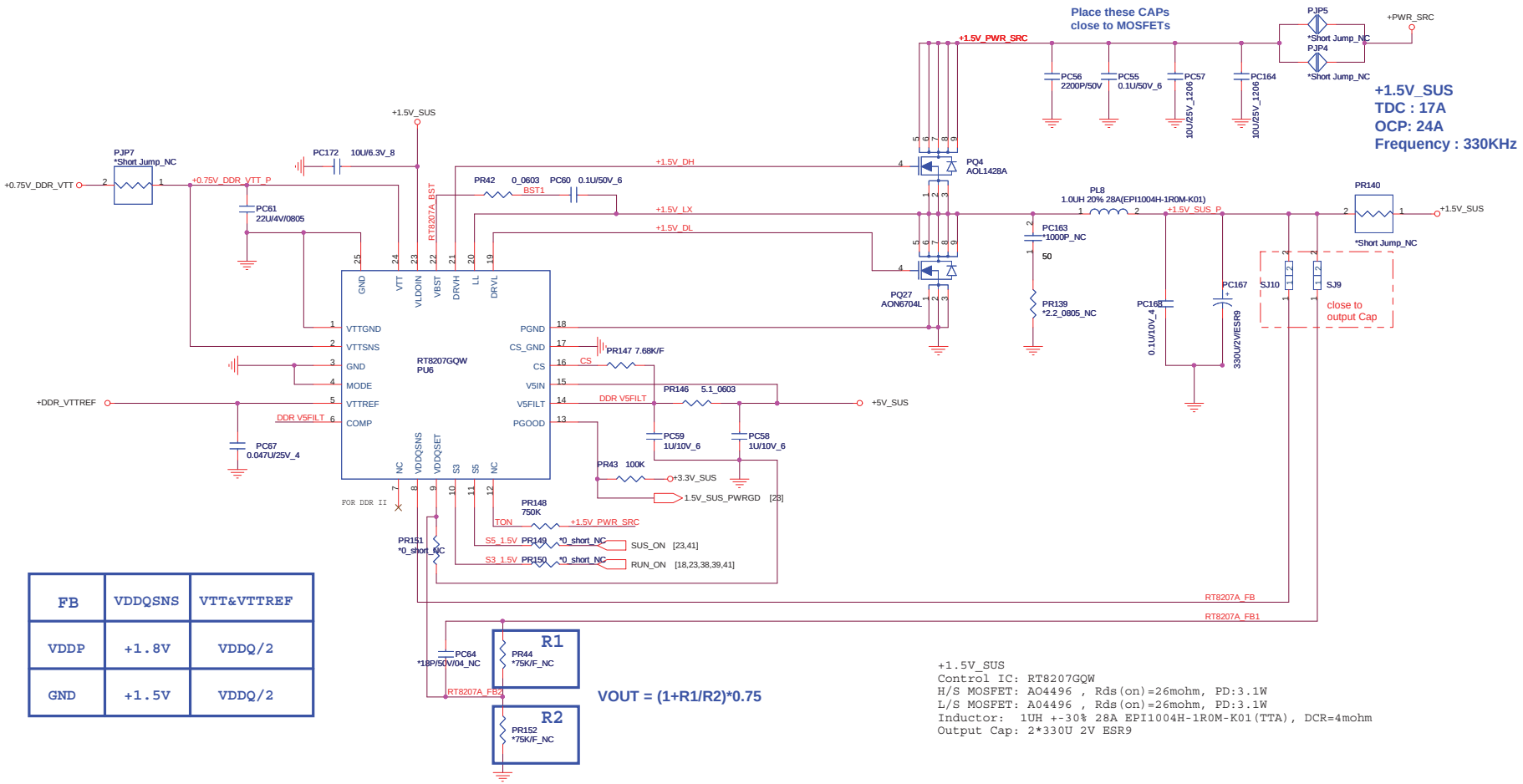

FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

+1.5V_SUS
Control IC: RT8207GQW
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 1UH +-30% 28A EPI1004H-1R0M-K01(TTA), DCR=4mohm
Output Cap: 2*330U 2V ESR9

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : R03/V03
Size | Document Number: DDR3 +1.5V_SUS(RT8207AGQW) | Rev 2A
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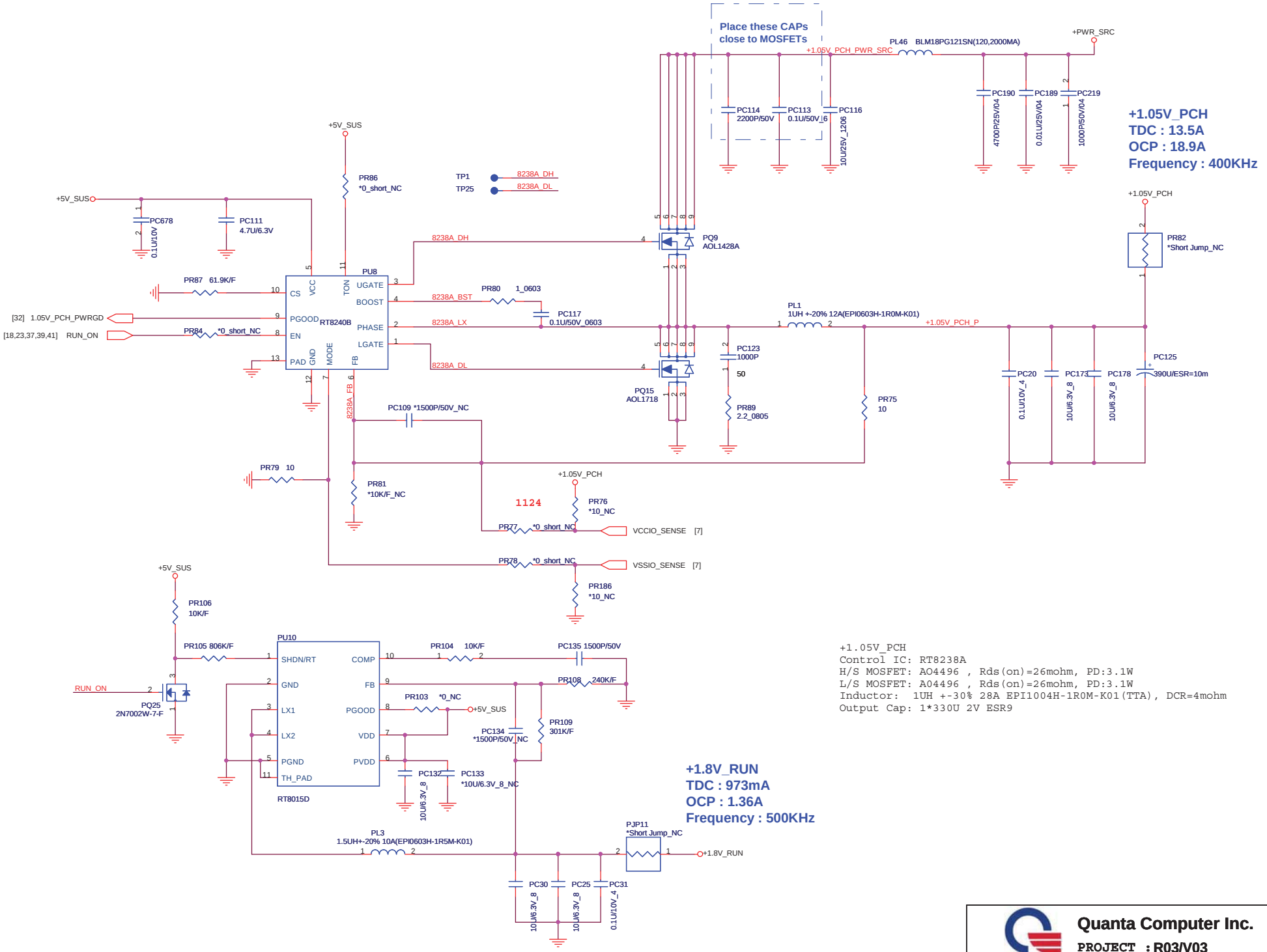
Place these CAPs close to MOSFETs
+1.05V_PCH
TDC : 13.5A
OCP : 18.9A
Frequency : 400KHz
+1.8V_RUN
TDC : 973mA
OCP : 1.36A
Frequency : 500KHz
+1.05V_PCH
Control IC: RT8238A
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 1UH +-30% 28A EPI1004H-1R0M-K01(TTA), DCR=4mohm
Output Cap: 1*330U 2V ESR9
Quanta Computer Inc.
PROJECT : R03/V03
Size
Document Number
+1.05V_PCH(RT8209A)
Rev 2A
Date: Monday, January 24, 2011
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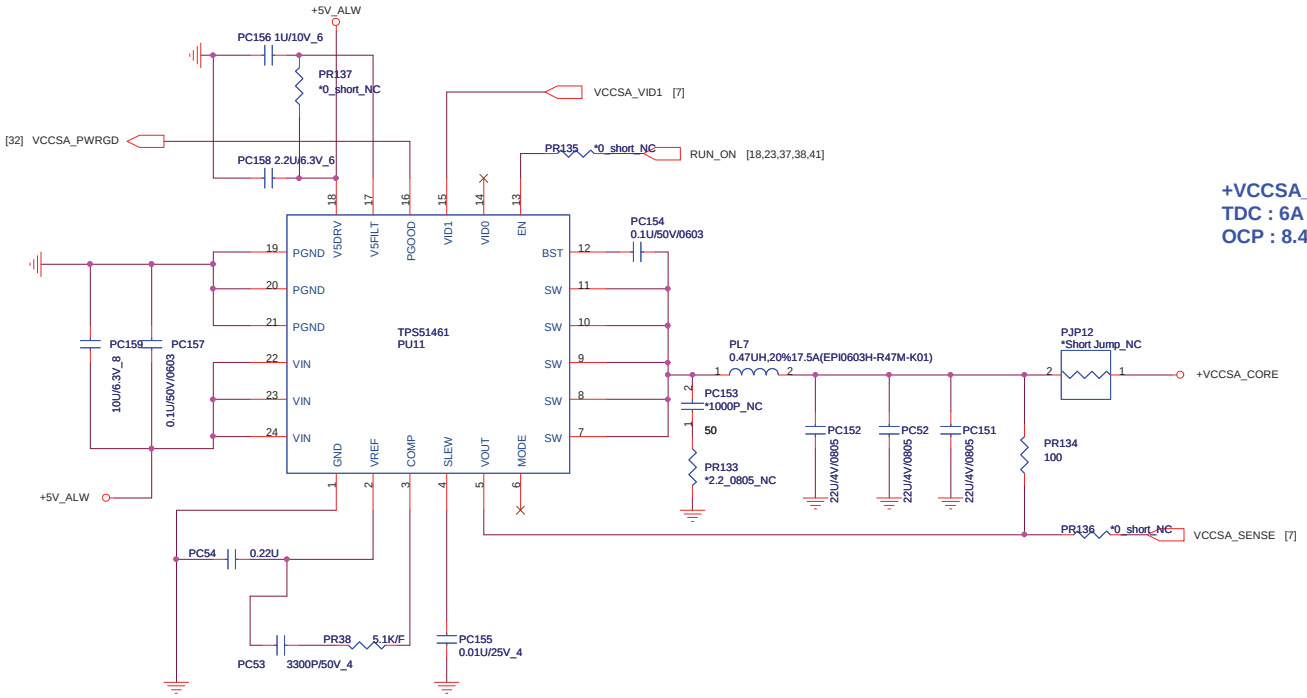

+VCCSA_CORE
TDC : 6A
OCP : 8.4A

+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	VCCSA (TPS51461)	2A
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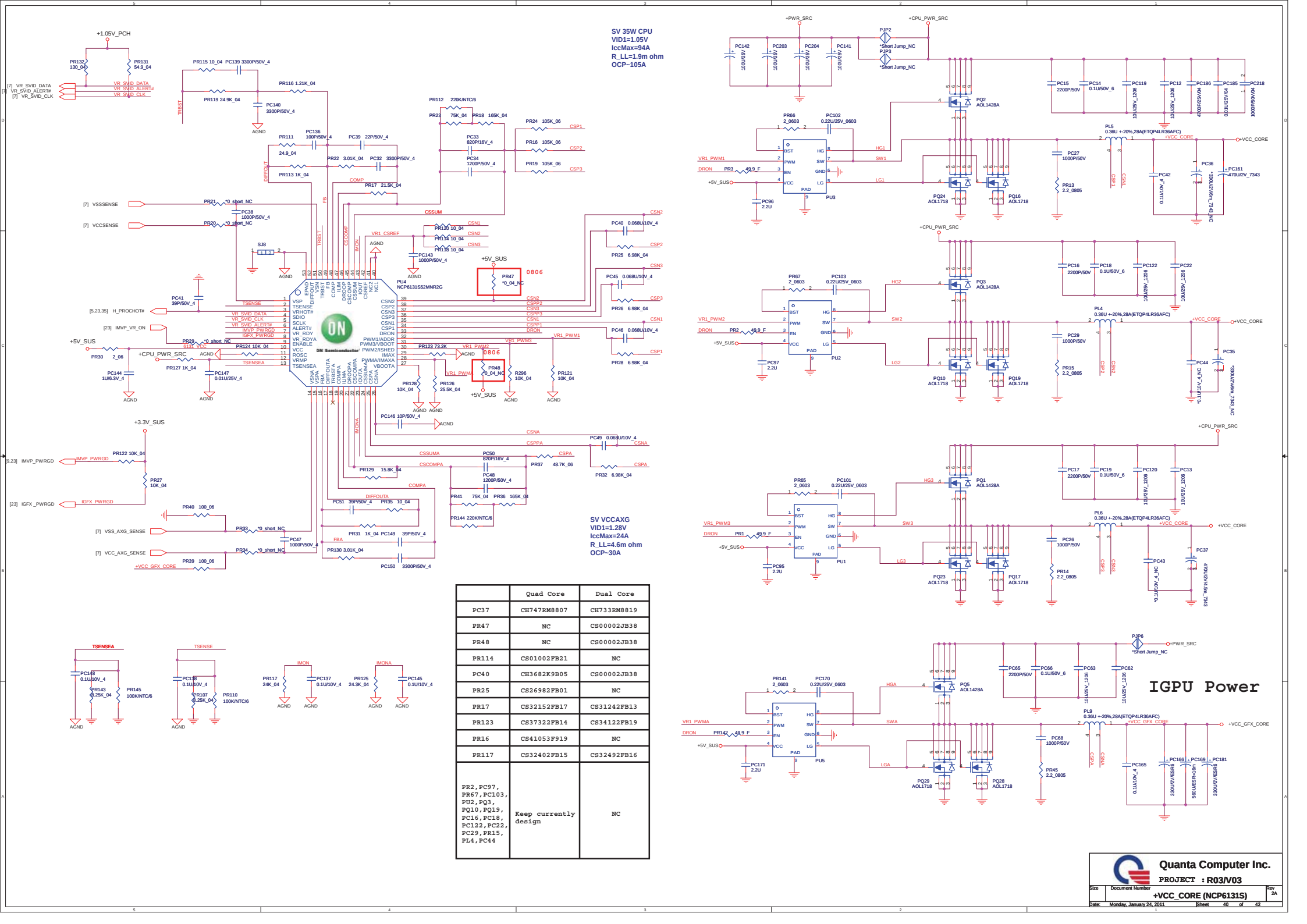

	Quad Core	Dual Core
PC37	CH747RM8807	CH733RM8819
PR47	NC	CS00002JB38
PR48	NC	CS00002JB38
PR114	CS01002FB21	NC
PC40	CH3682K9B05	CS00002JB38
PR25	CS26982FB01	NC
PR17	CS32152FB17	CS31242FB13
PR123	CS37322FB14	CS34122FB19
PR16	CS41053F919	NC
PR117	CS32402FB15	CS32492FB16
PR2,PC97, PR67,PC103, PU2,PQ3, PQ10,PQ19, PC16,PC18, PC122,PC22, PC29,PR15, PL4,PC44	Keep currently design	NC

Quanta Computer Inc.
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+VCC_CORE (NCP6131S)
Size: Document Number: Rev: 2A
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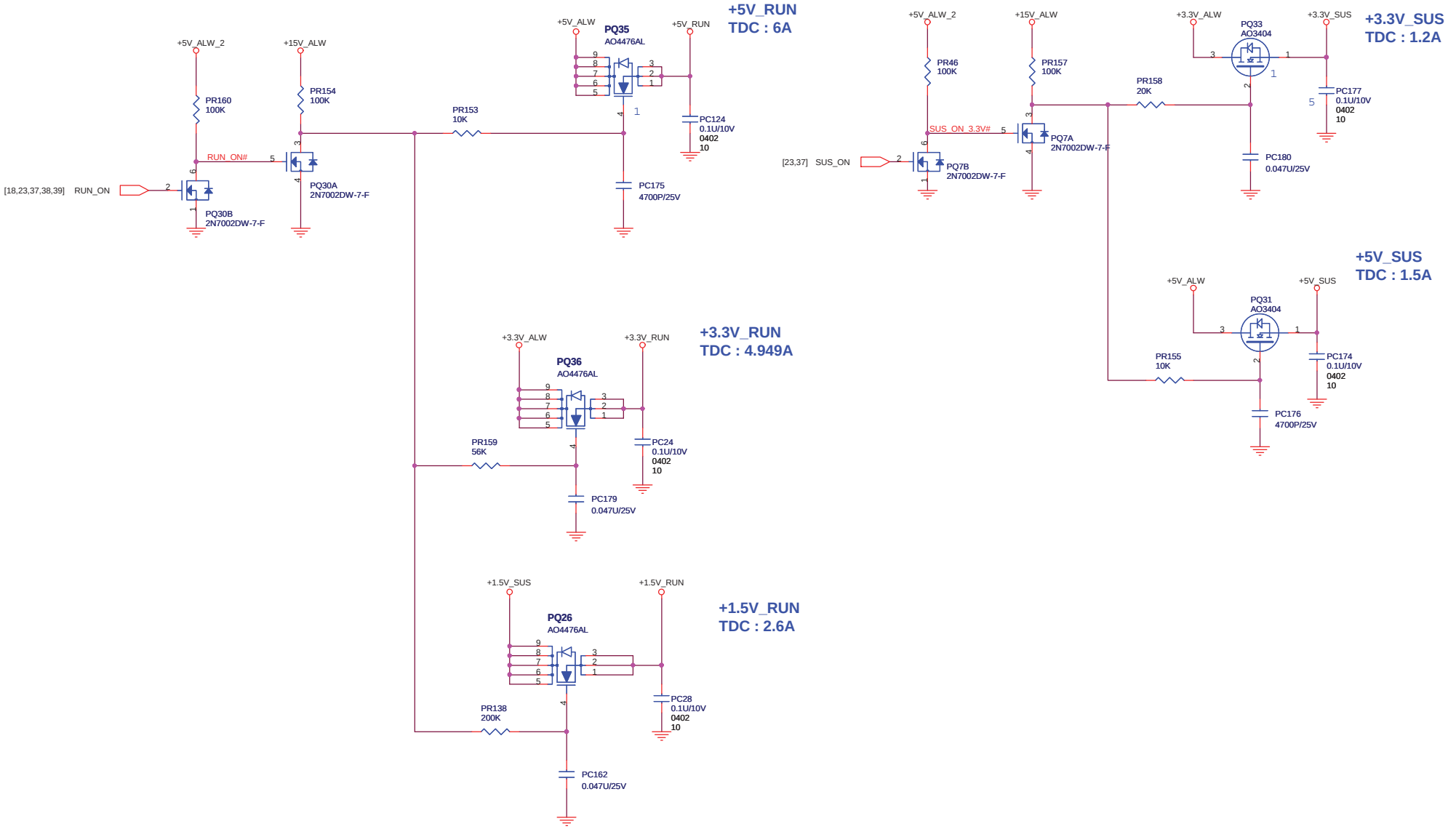

Quanta Computer Inc.

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Size	Document Number	Rev
	RUN / SUS POWER SW	2A

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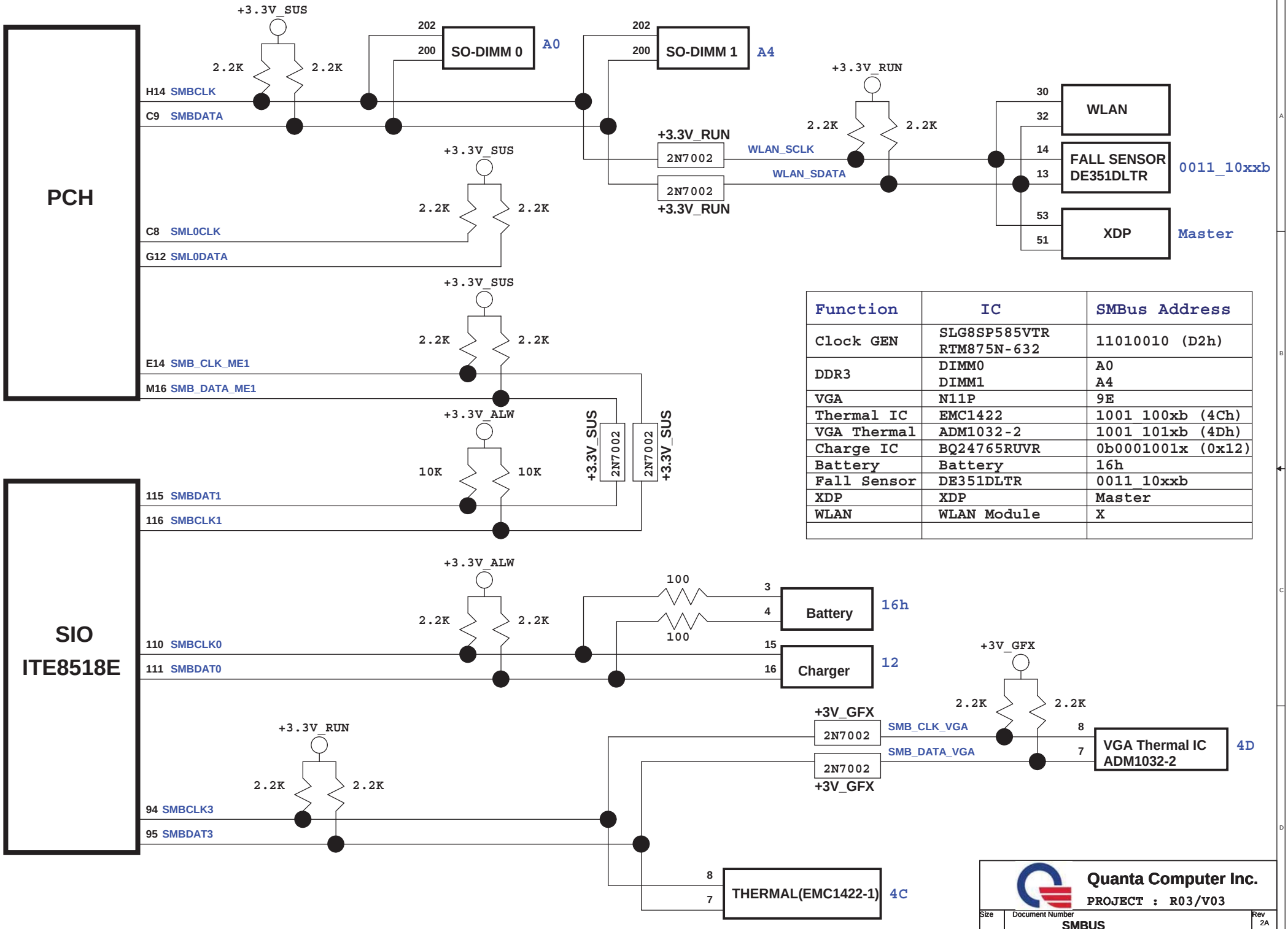

Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001 100xb (4Ch)
VGA Thermal	ADM1032-2	1001 101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011_10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

Quanta Computer Inc.
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Size	Document Number	Rev
	SMBUS	2A

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