


Quanta Project Name: XM1

Dell Project Name: Nike

2008-03-18

REV : A1A

X01 Stage

		Quanta Computer Inc.	
		Project Name: Nike	
Title: Cover Page			
Size: Custom	Document Number: ?	Rev: 1A	
Date: Wednesday, March 19, 2008		Sheet 1 of 55	



XM1 M/B PCB

PWA XXX, PWB XXX,
SCHEM XXX.
VER : XX Date: 071010

System Block Diagram of Nike

POWER

CHARGER	PG 46
LDO	PG 47
0.75V_DDR_VTT, 1.8V_RUN	
DC/DC	PG 49
+3.3V_ALW/+5V_ALW/+15V_ALW	
DC/DC	PG 48
1.1V_VCCP and 1.5V_MEM	
VCORE	PG 51
VCC_VCORE	
Power Good	PG 45,52
Misc. Power	PG 45,52

DDR3-SODIMM_A1

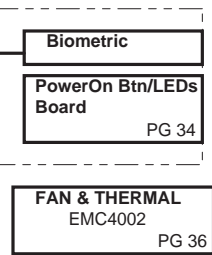
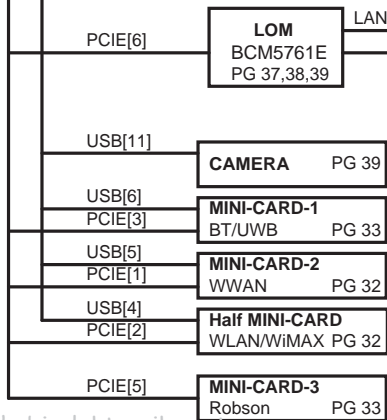
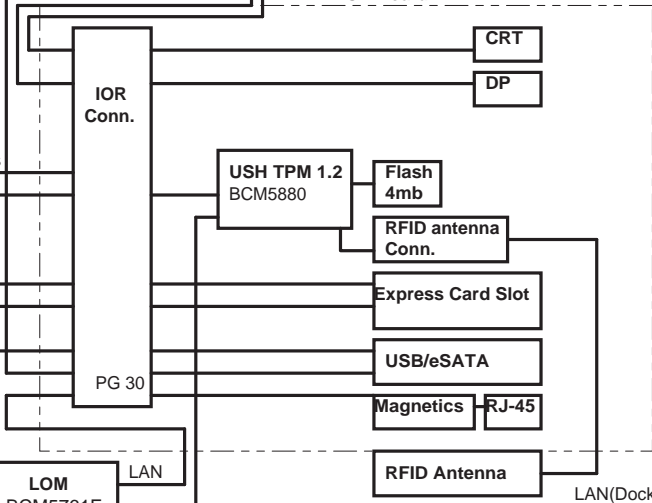
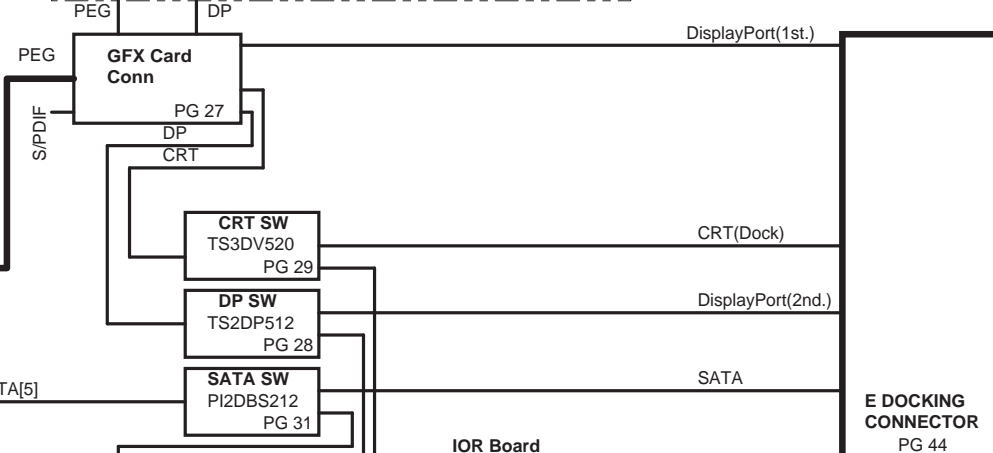
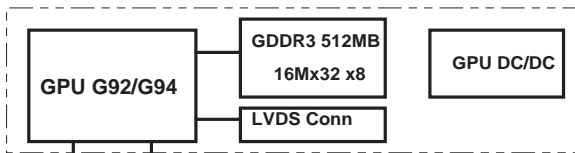
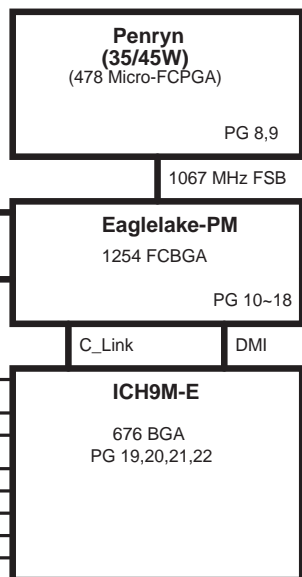
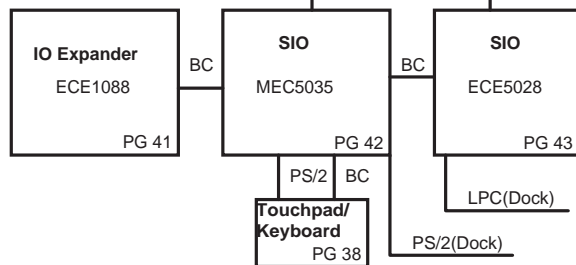
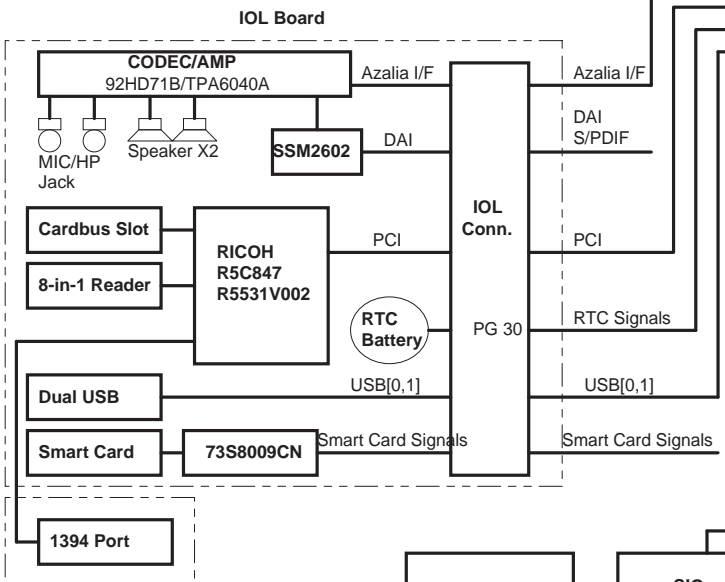
DDR3-SODIMM_A0	PG 22,23
800/1067 MHz DDR III	
DDR3-SODIMM_B0	PG 25,26
800/1067 MHz DDR III	
DDR3-SODIMM_B1	PG 25,26
800/1067 MHz DDR III	

E-Module Bay ODD PG 31

SATA - HDD0 PG 31

SATA - HDD1 PG 31

SPI FLASH 32mb PG18



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Project Name: Nike

Title: Block Diagram

Size: Custom


Document Number: ?

Date: Wednesday, March 19, 2008

Sheet: 2 of 55

Rev: 1A

INDEX	
Pg#	Description
01	CoverPage
02	MB Block Diagram
03	Index
04	Config.
05	SMBus Topology
06	Power Sequence Diagram
07	Clock Generator
08-09	Penryn
10-18	Eaglelake
19-22	ICH9M
23-26	DDR3
27	GFX CARD CONN.
28	DisplayPort SWITCH
29	CRT SWITCH
30	IOR and IOL connector.
31	SATA(HDD_ODD) eSATA SWITCH
32	MINI Card
33	MINI Card
34	TP PWR BUTTON
35	CCD SNIFFER LED.
36	THERMAL EMC4002
37-39	BCM5761E_LOM
40	SSX35BCB (TPM for China)
41	IO EXPAND_ECE1088
42	SIO_MEC5035
43	SIO-ECE5028
44	E-DOCKING CONNECTOR.
45	System Power Good.
46	Battery Charger.
47	0.75V_DDR_VTT, 1.8V_RUN
48	1.1V_VCCP and 1.5V_MEM
49	5V_ALW, 3V_ALW
50	DCIN, Battery Connector
51	CPU_VCORE (ADP3207A)
52	Power Misc
53	Screw hole

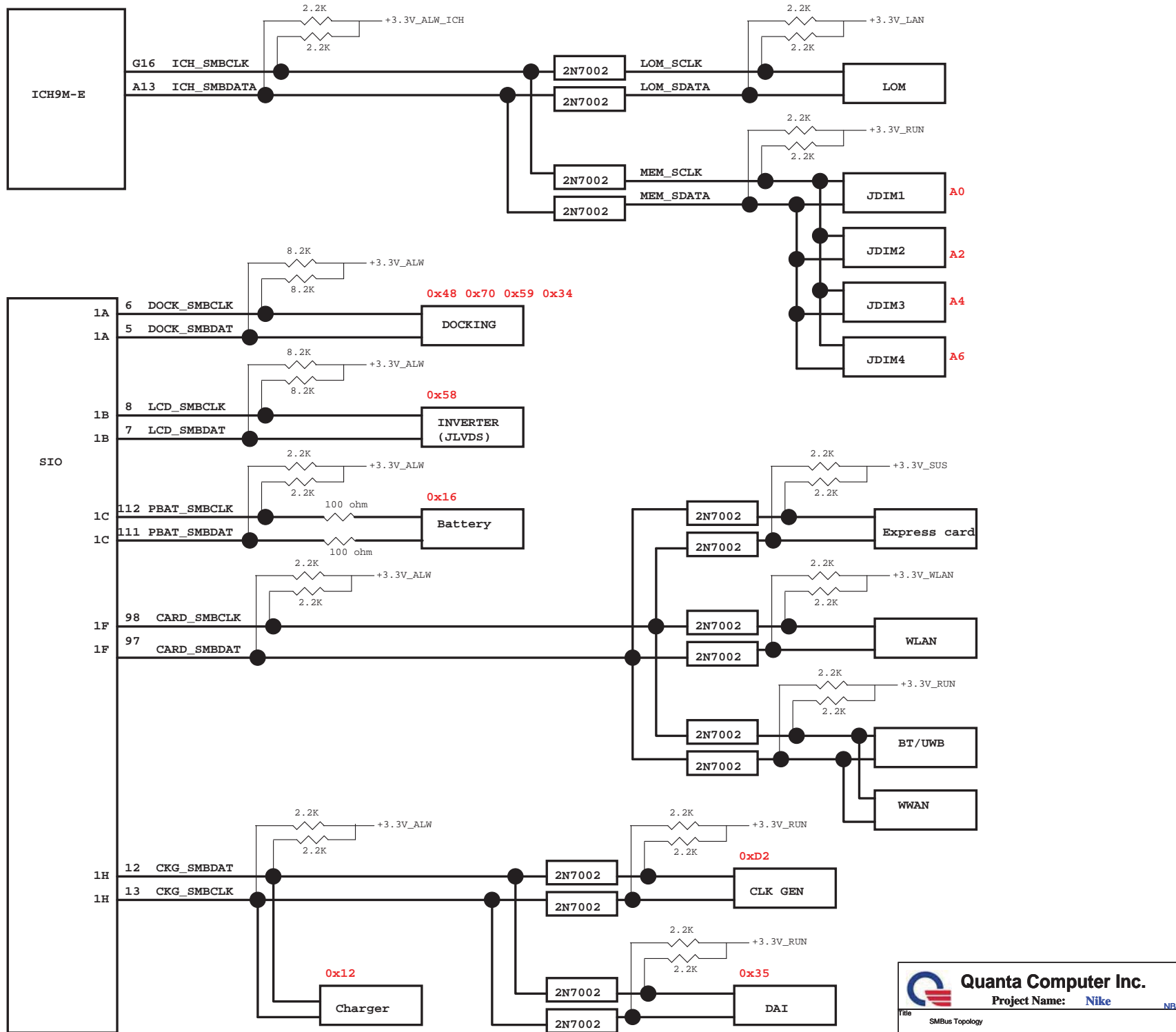
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		Project Name: Nike	
Title		Front Page	
Size	Document Number	Rev	
Custom	?	1A	
Date: Wednesday, March 19, 2008		Sheet	3 of 55

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

Power Plane State	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +1.1V_VCCP +VCC_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

ICH9M-E	USB PORT#	DESTINATION
	0	Left Top
	1	Left Bot
	2	Right Top
	3	Right Bot
	4	WLAN
	5	WWAN
	6	WPAN
	7	Express card
	8	DOCKING
	9	DOCKING
	10	USH
11	Camera	

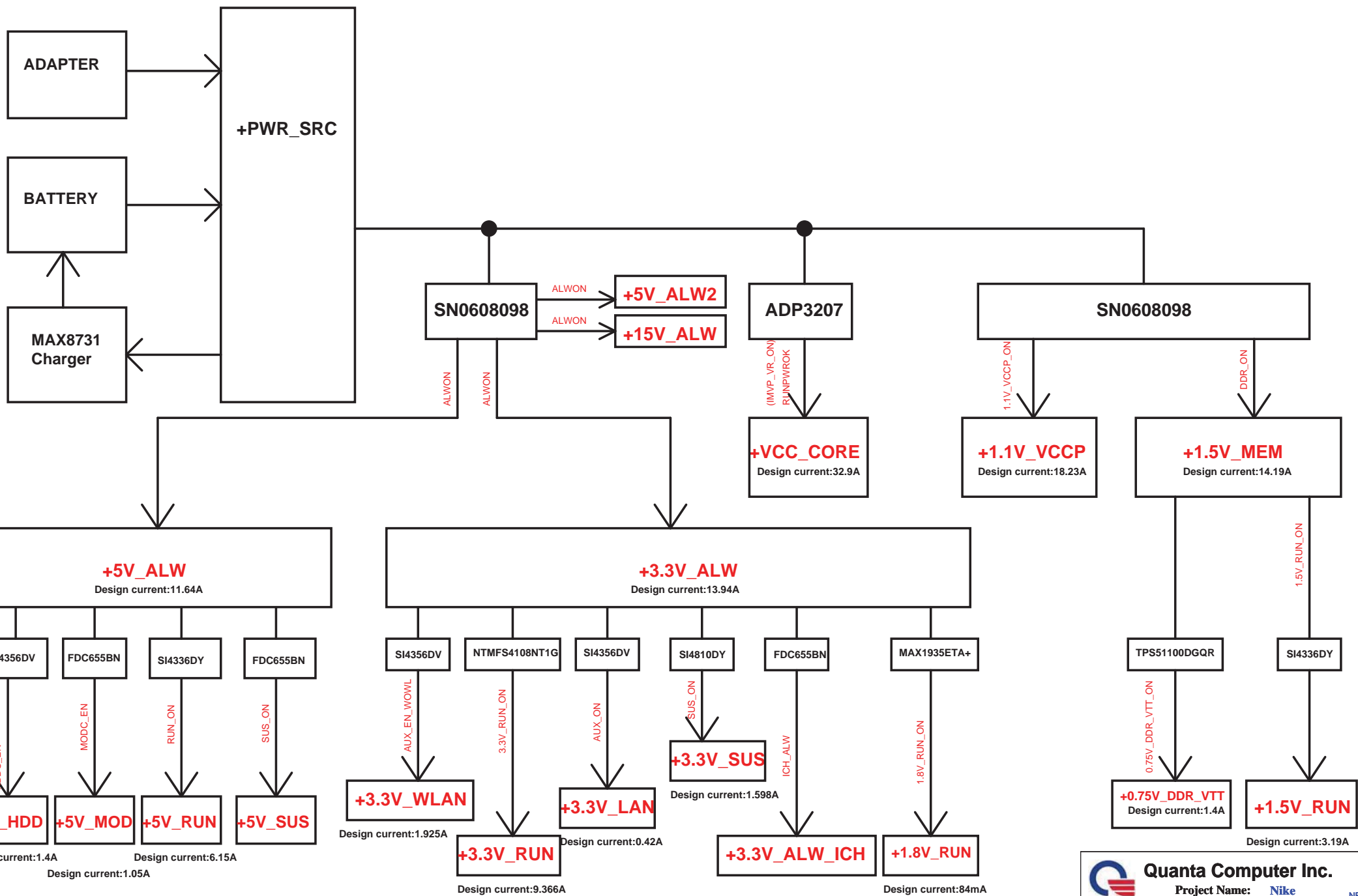
ICH9M-E	PCI EXPRESS	DESTINATION
	Lane 1	WWAN
	Lane 2	WLAN
	Lane 3	BT/UWB
	Lane 4	Express Card
	Lane 5	Robson
Lane 6	Giga Bit LOM	

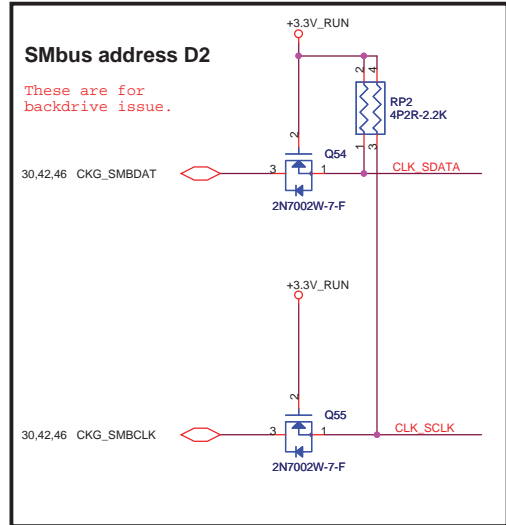
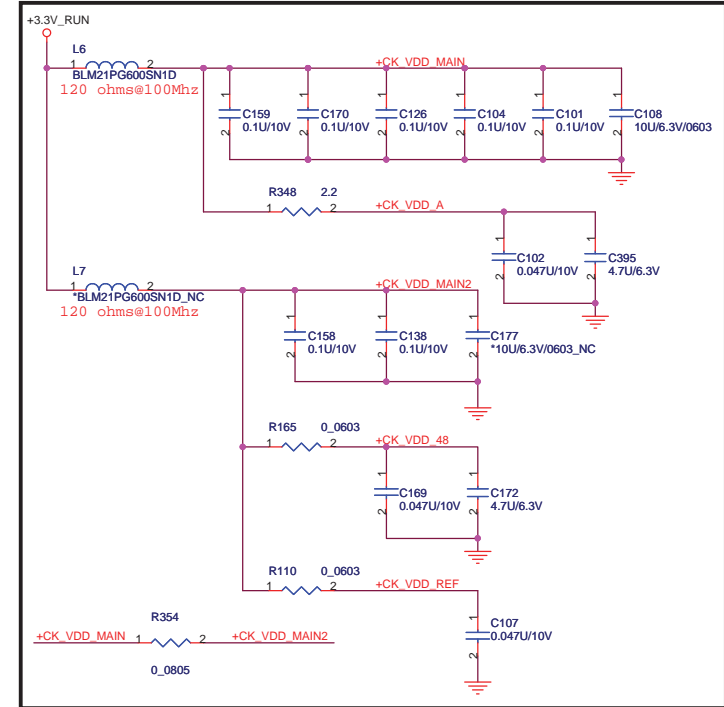
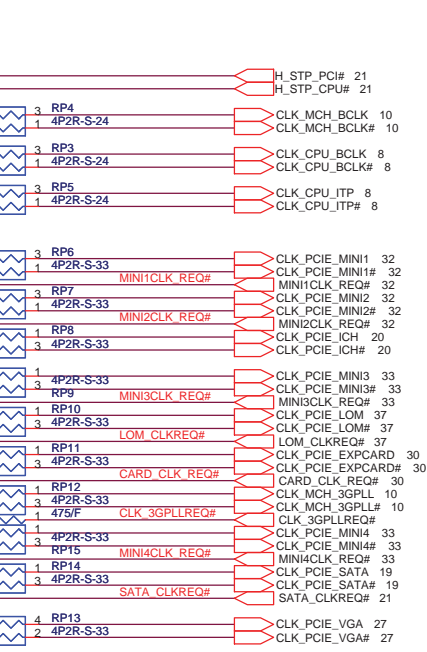
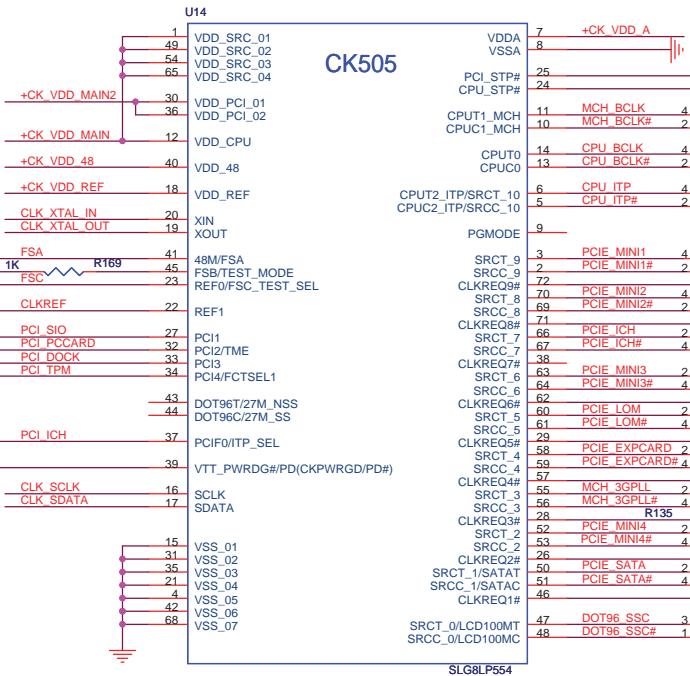
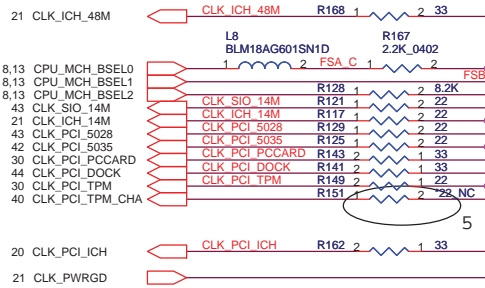
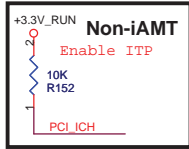
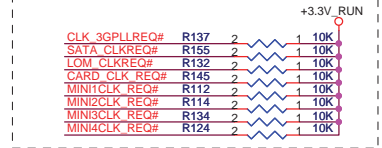
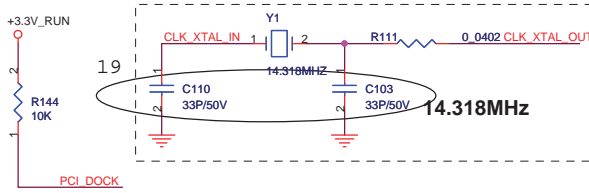
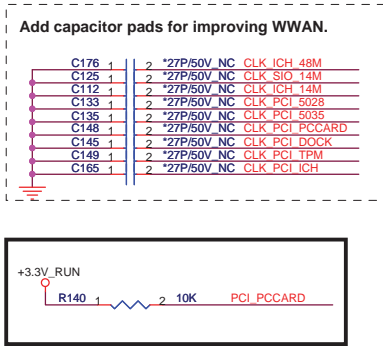
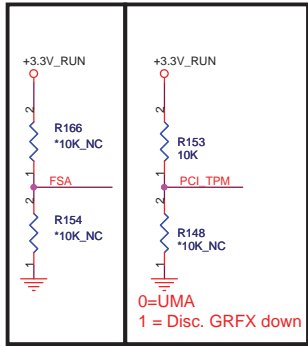


<http://hobi-elektronika.net>

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File	SMBus Topology	
Size	Document Number	Rev
Custom	?	1A
Date:	Wednesday, March 18, 2009	Sheet 5 of 55





FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	RSVD	RSVD

PCI_LOM = FCTSEL1

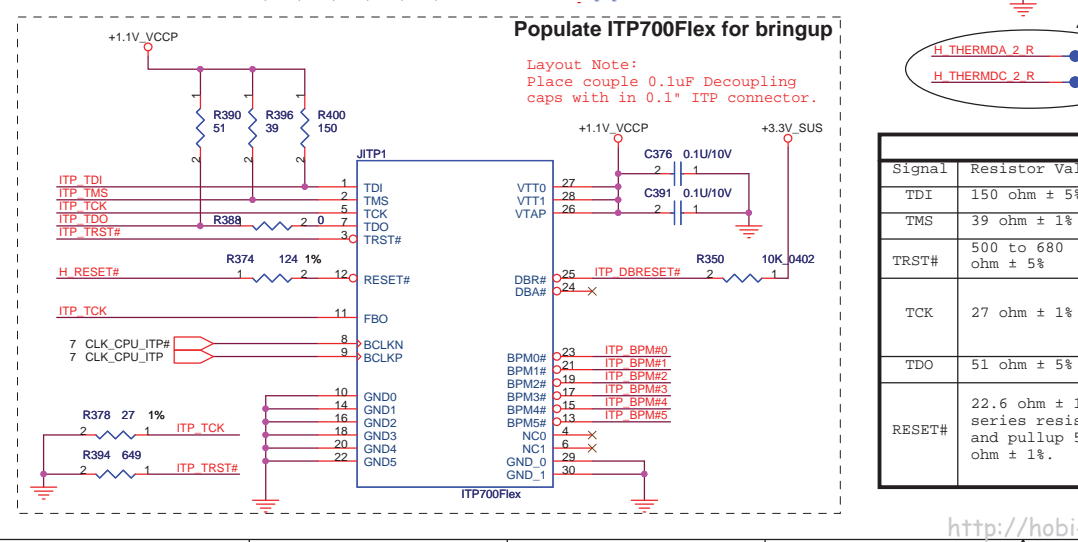
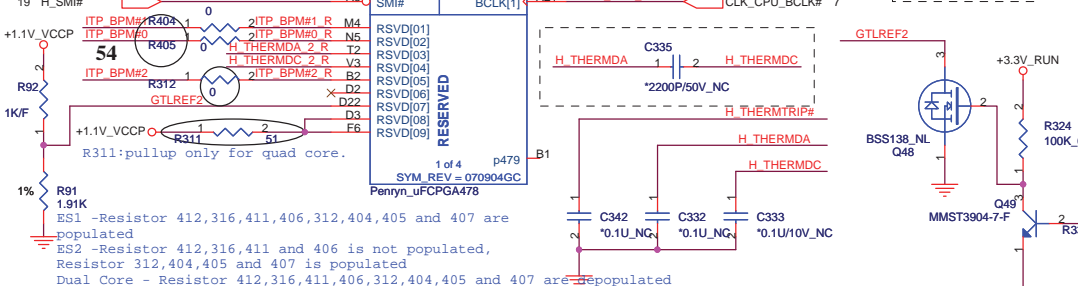
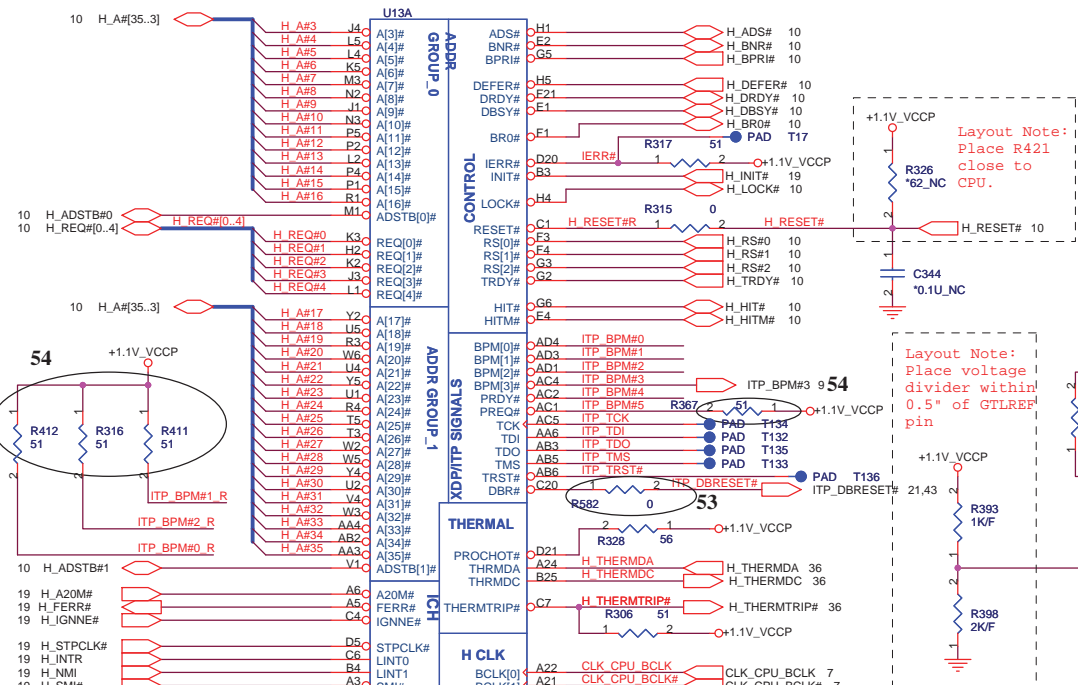
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

Quanta Computer Inc.
Project Name: Nike

Title: Clock Generator

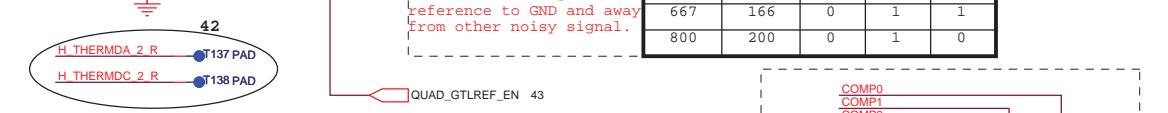
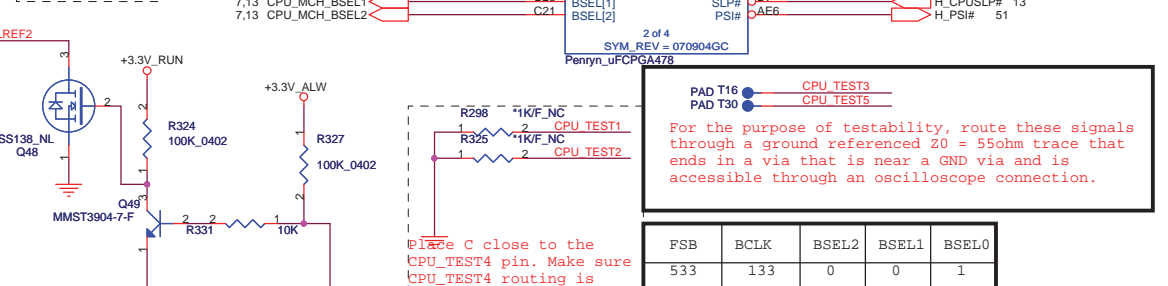
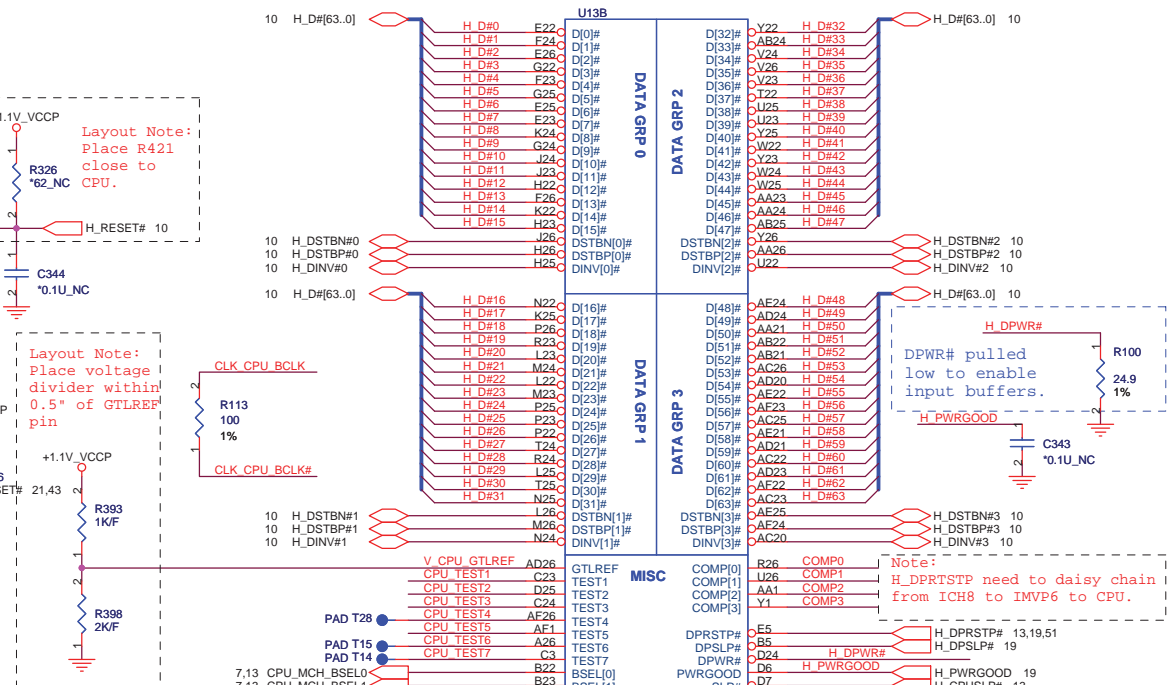
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Date: Wednesday, March 19, 2008 Sheet 7 of 55



Populate ITP700Flex for bringup

Layout Note:
Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.



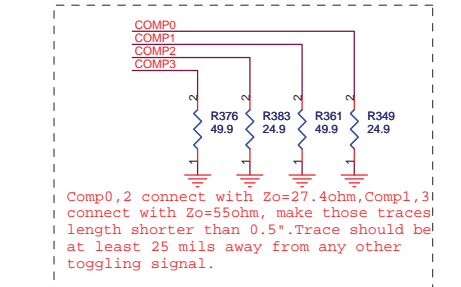
ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

Note:
H_DPRTSTP need to daisy chain from ICH8 to IMPV6 to CPU.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



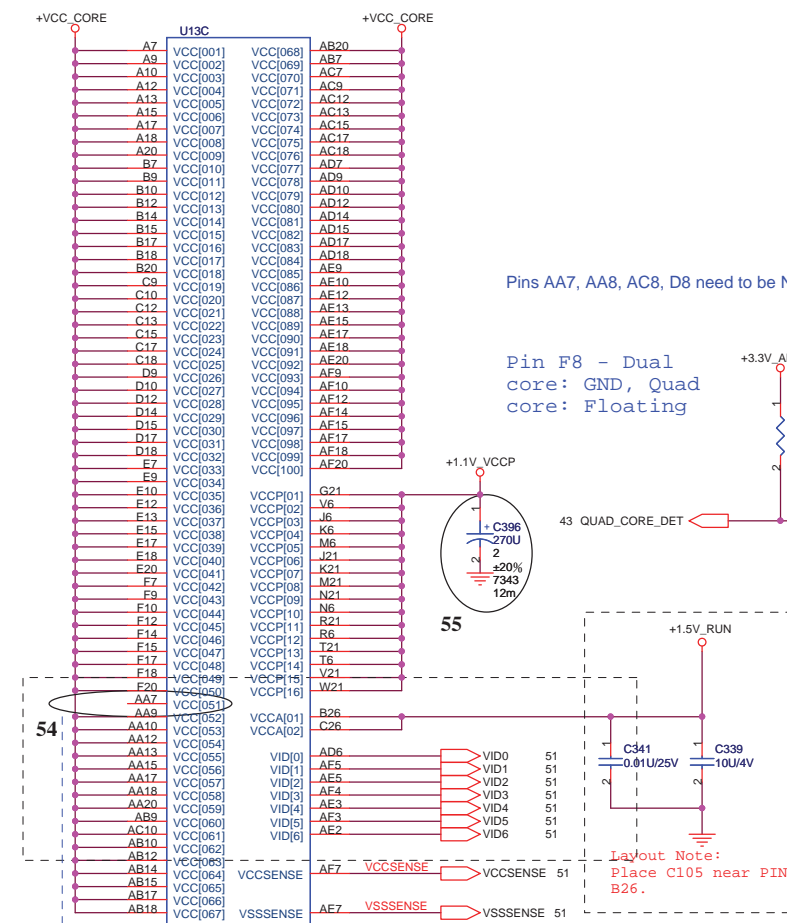
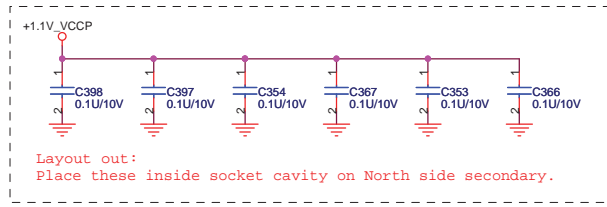
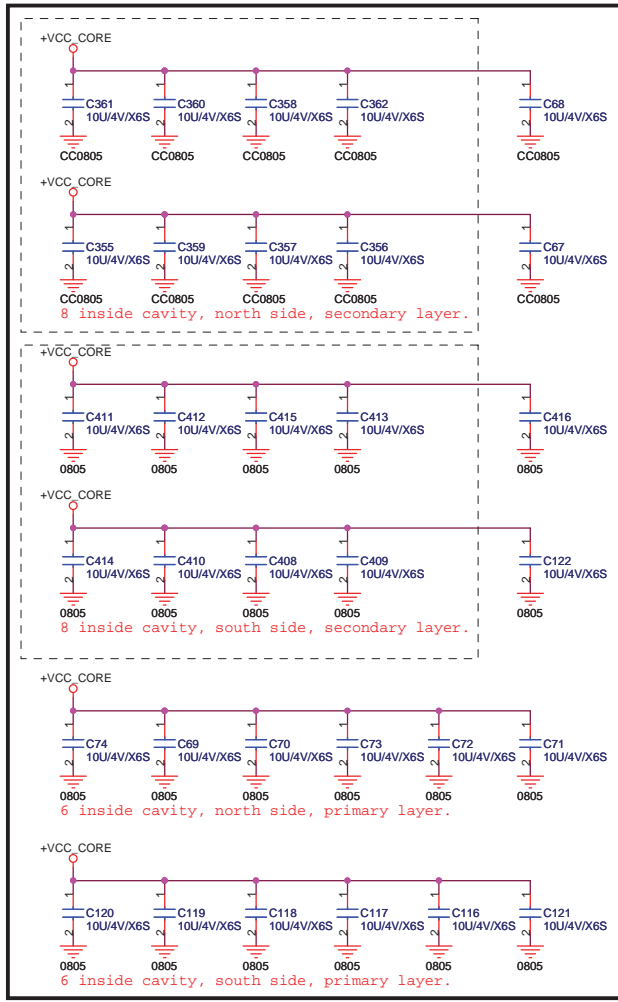
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Project Name: **Nike**

Title: Penryn (1 of 2)

Size: Custom Document Number: ?

Date: Wednesday, March 19, 2008 Sheet 8 of 55

All use 22U 10V(+/-20%,X5R,1210)Pb-Free.



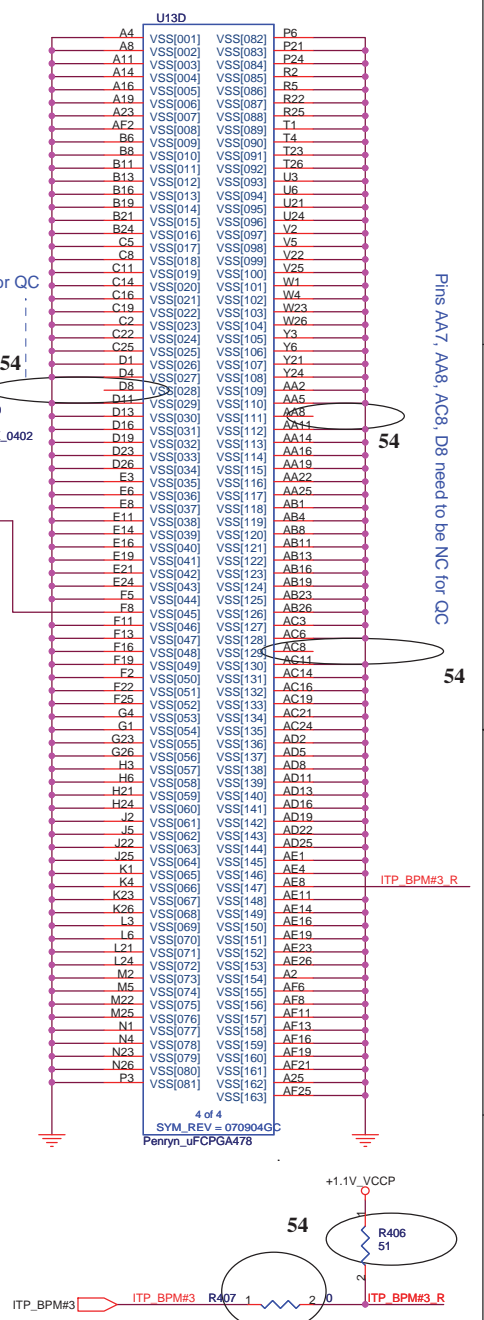
Pins AA7, AA8, AC8, D8 need to be NC for QC

Pin F8 - Dual core: GND, Quad core: Floating

Pins AA7, AA8, AC8, D8 need to be NC for QC

Pins AA7, AA8, AC8, D8 need to be NC for QC

Route VCCsense and VSSsense traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.



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Project Name: Nike

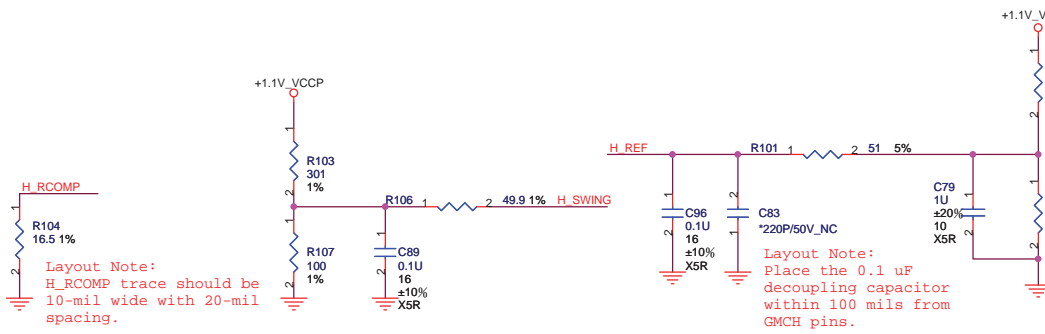
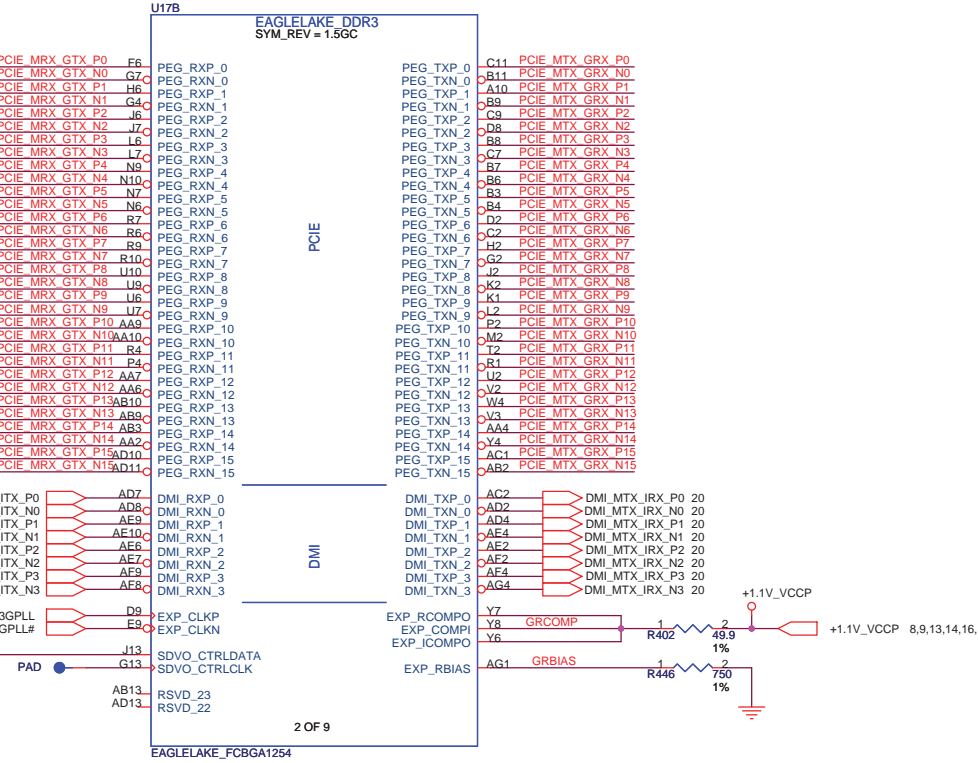
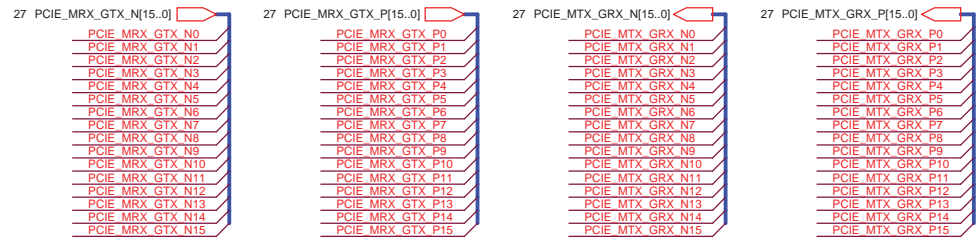
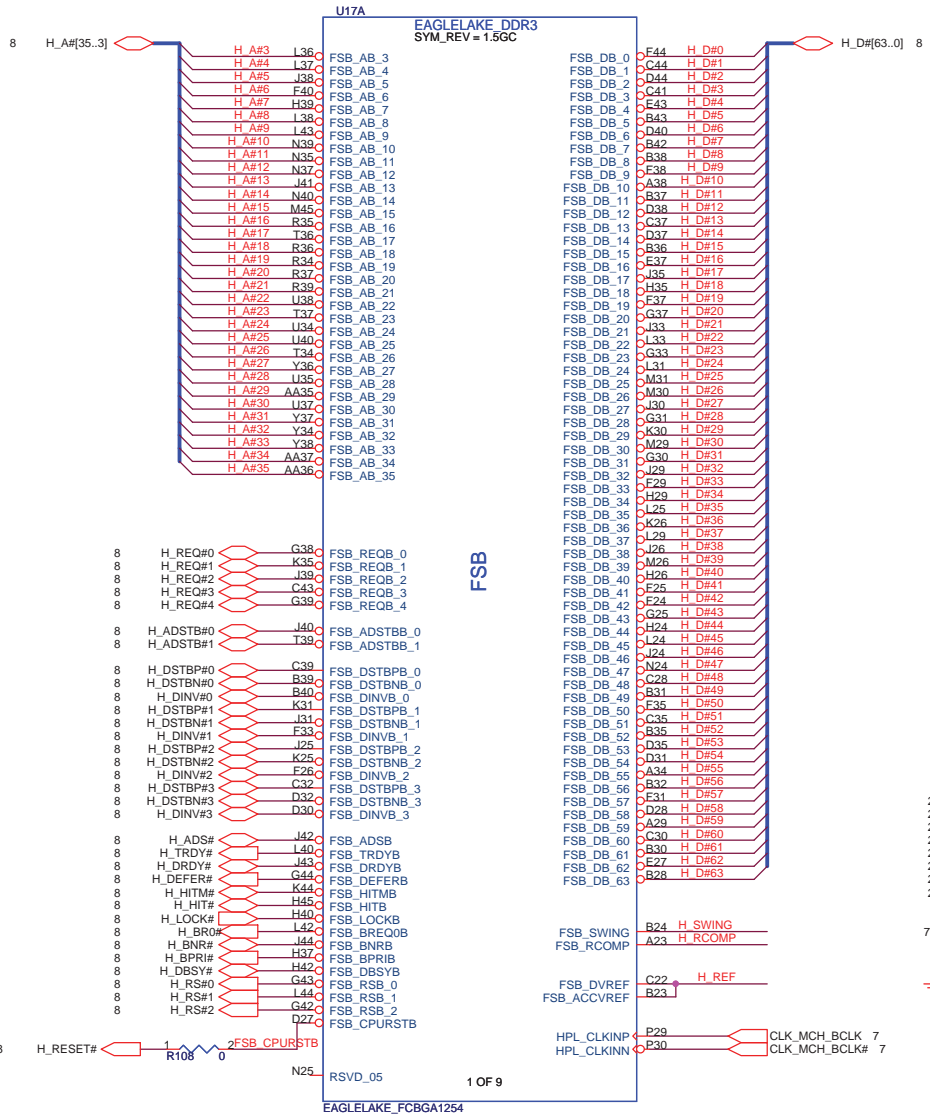
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Size: Custom Document Number: ?

Date: Wednesday, March 19, 2008

Sheet: 9 of 55

Rev: 1A

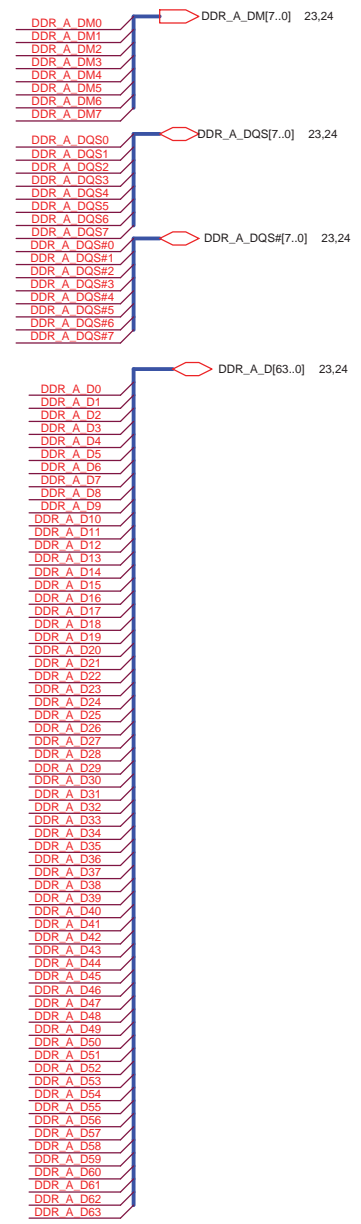
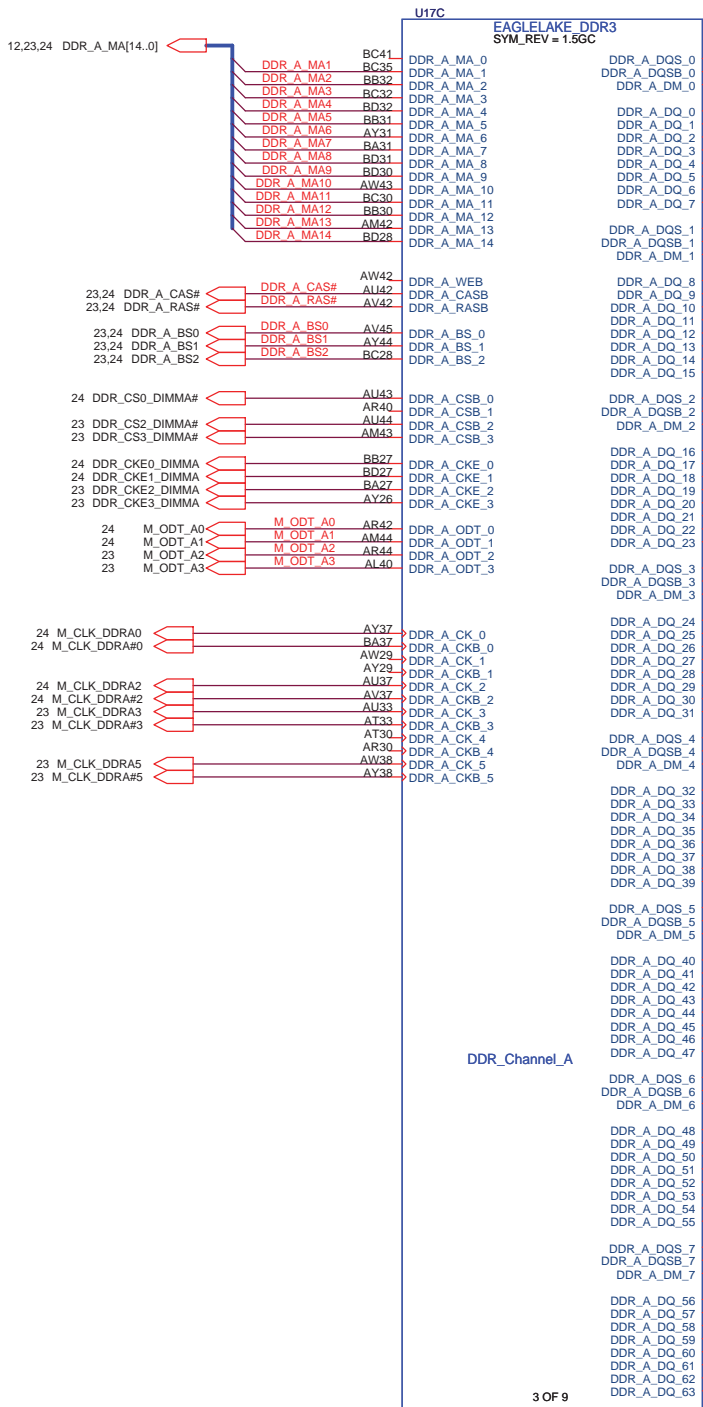


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 Project Name: **Nike**

Title: Eaglelake(1 of 10)

Size	Document Number	Rev
Custom	?	1A

Date: Wednesday, March 19, 2008 Sheet 10 of 55



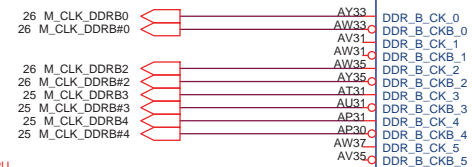
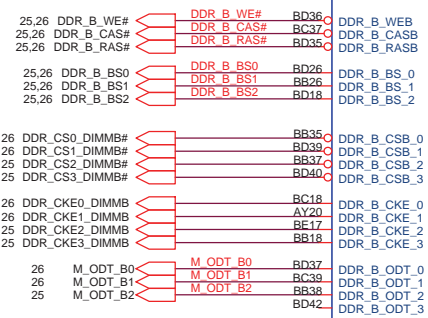
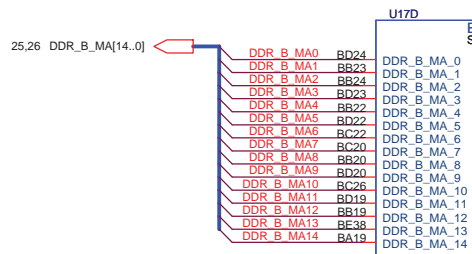
EAGLELAKE_FCBGA1254

Quanta Computer Inc.
Project Name: **Nike**

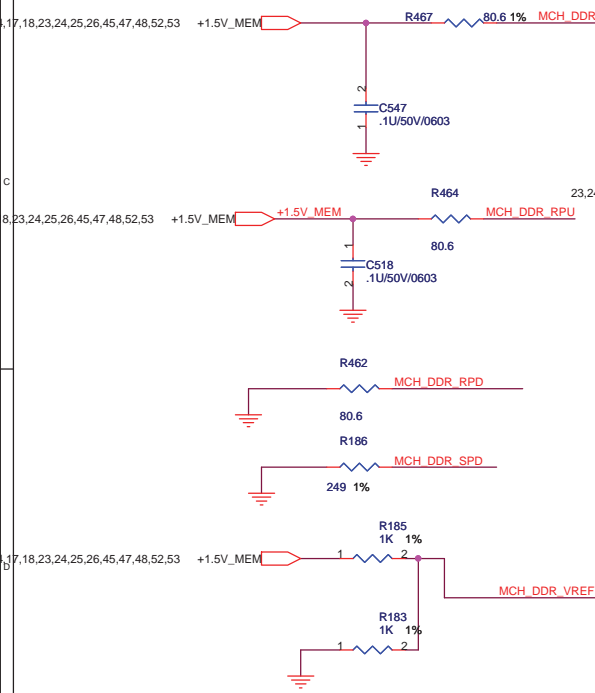
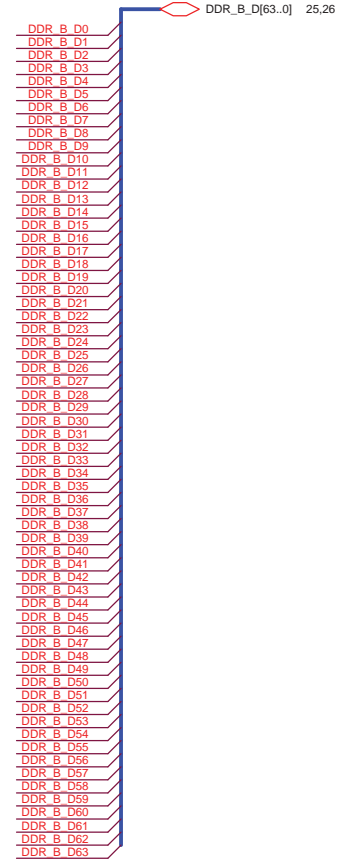
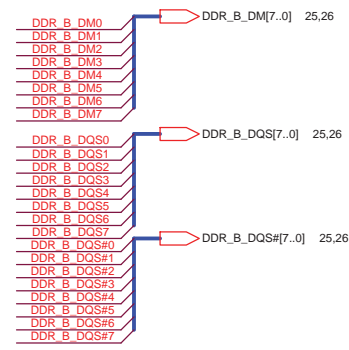
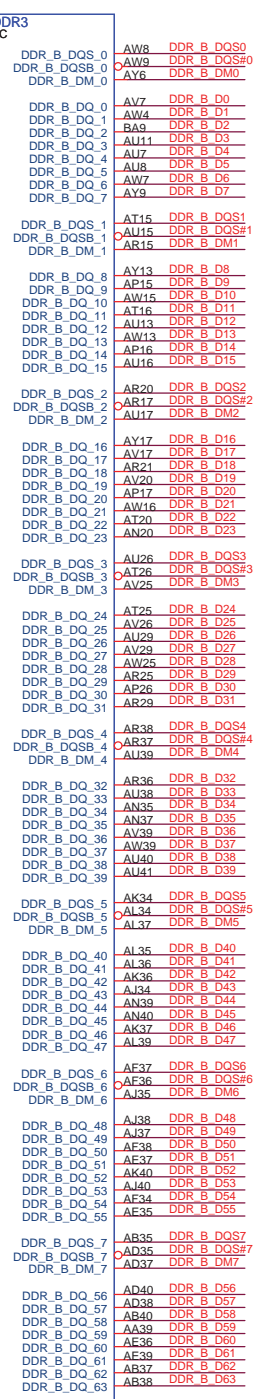
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Size: Custom	Document Number: ?	Rev: 1A
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Date: Wednesday, March 19, 2008 Sheet 11 of 55



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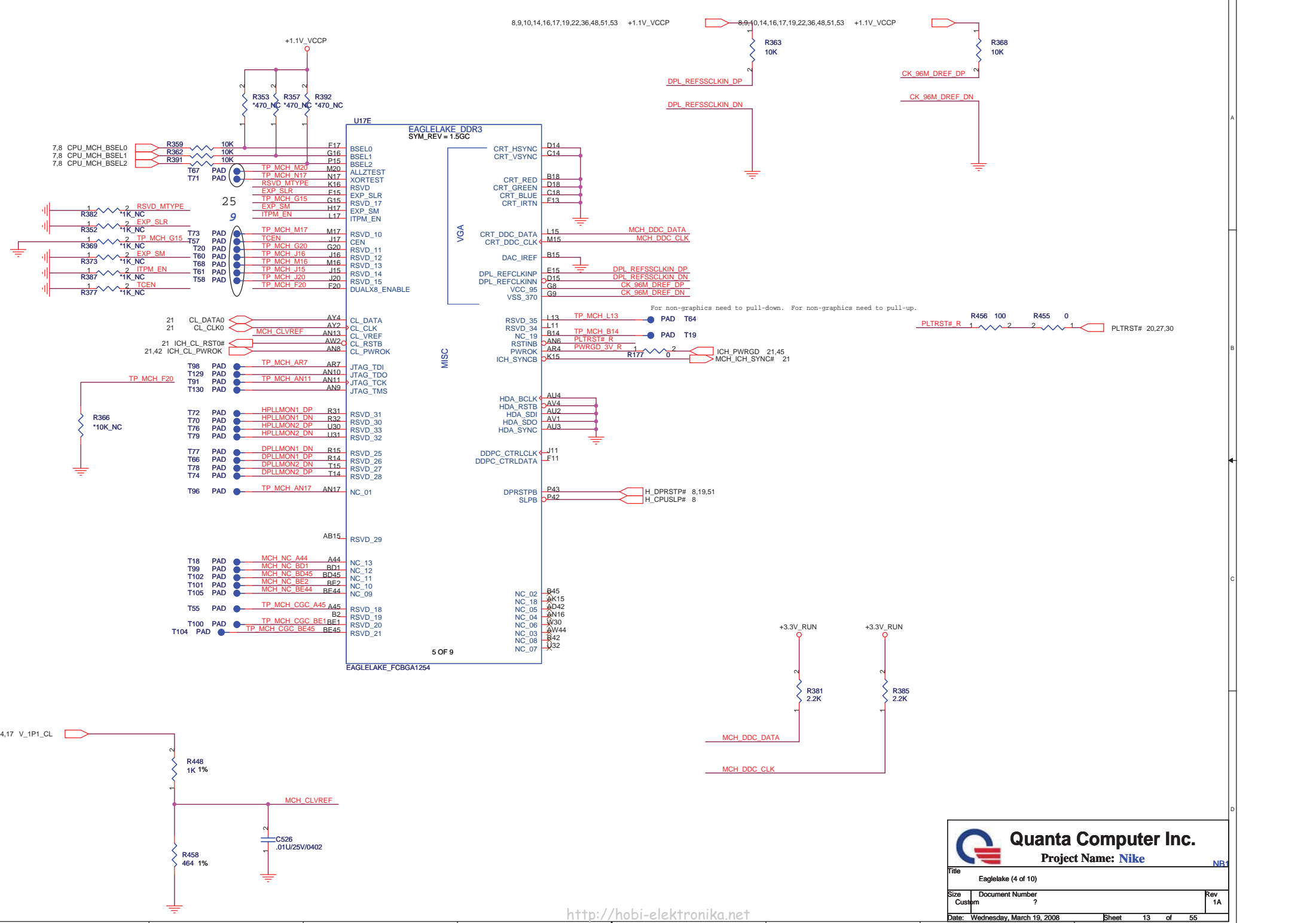


Quanta Computer Inc.
Project Name: Nike

Title: Eaglelake (3 of 10)

Size	Document Number	Rev
Custom	?	1A

Date: Wednesday, March 19, 2008 Sheet 12 of 55



8,9,10,14,16,17,19,22,36,48,51,53 +1.1V_VCCP

8,9,10,14,16,17,19,22,36,48,51,53 +1.1V_VCCP

U17E
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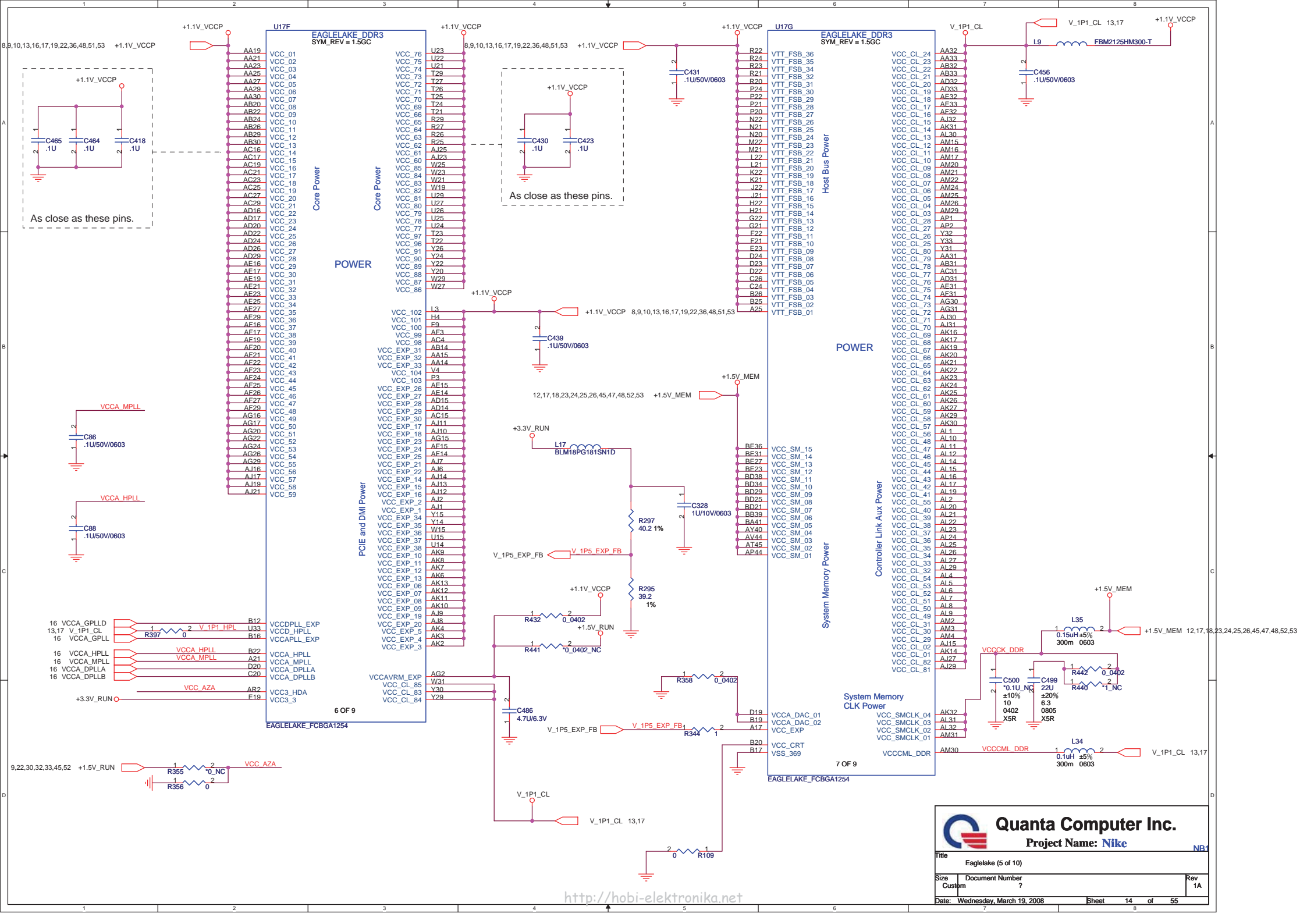
VGA

MISC

5 OF 9

EAGLELAKE_FCBGA1254

		Quanta Computer Inc. Project Name: Nike	
		Title: Eaglelake (4 of 10)	
Size: Custom	Document Number: ?	Rev: 1A	
Date: Wednesday, March 19, 2008		Sheet: 13	of 55

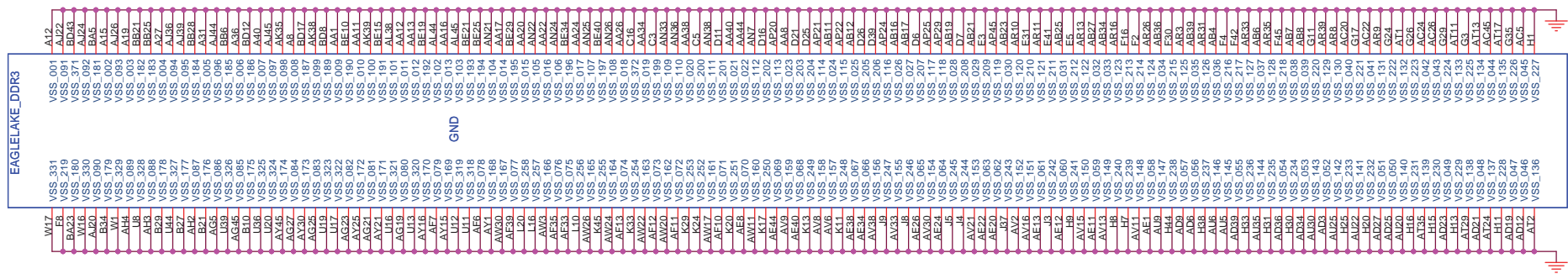


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 Project Name: Nike

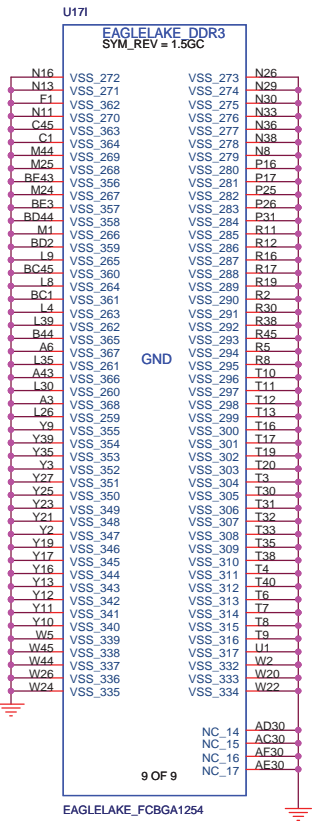
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Size: Custom	Document Number: ?	Rev: 1A
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Date: Wednesday, March 19, 2008 Sheet: 14 of 55



U17H
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8 OF 9



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Project Name: Nike

Title: Eaglelake (6 of 10)

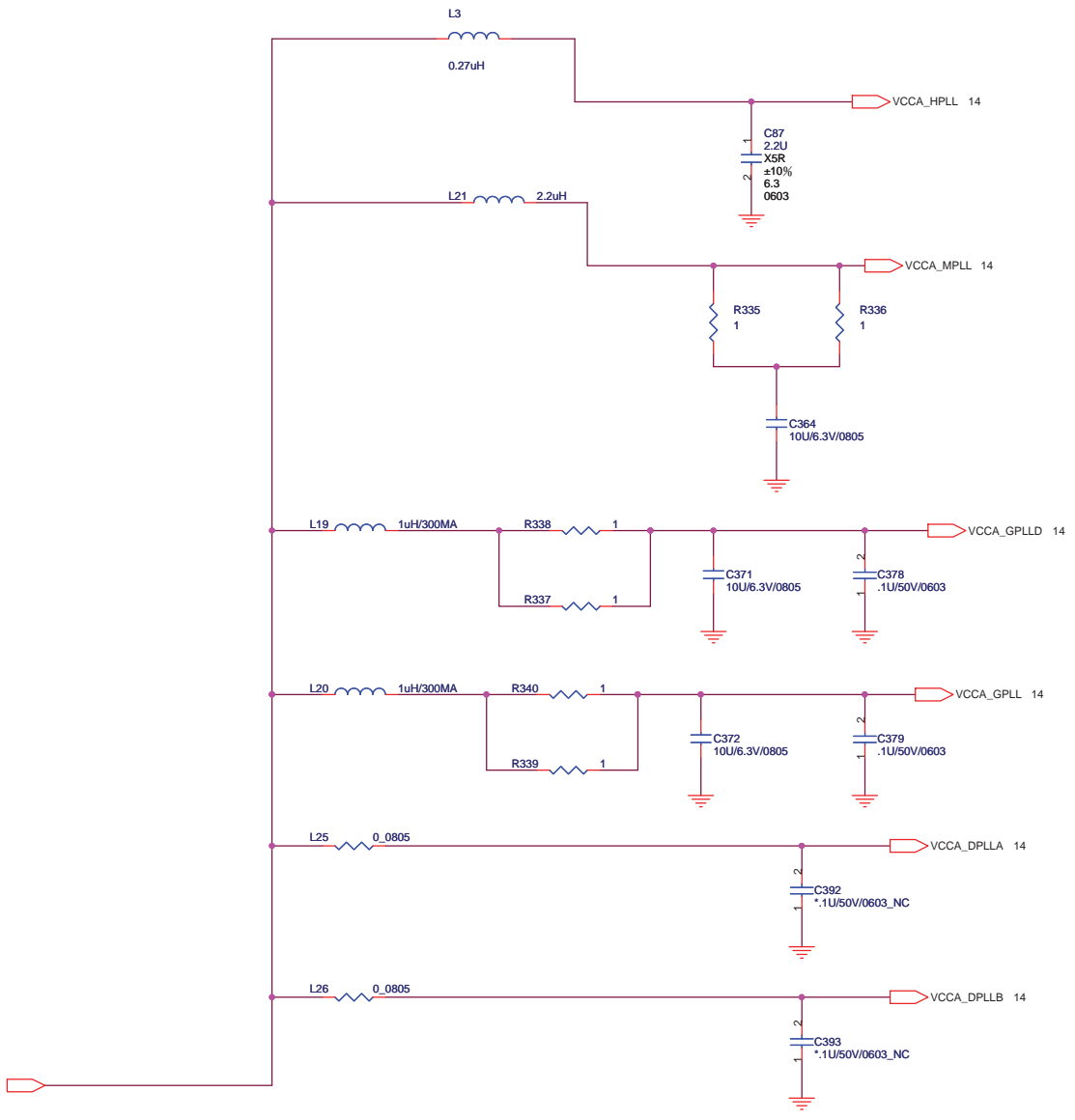
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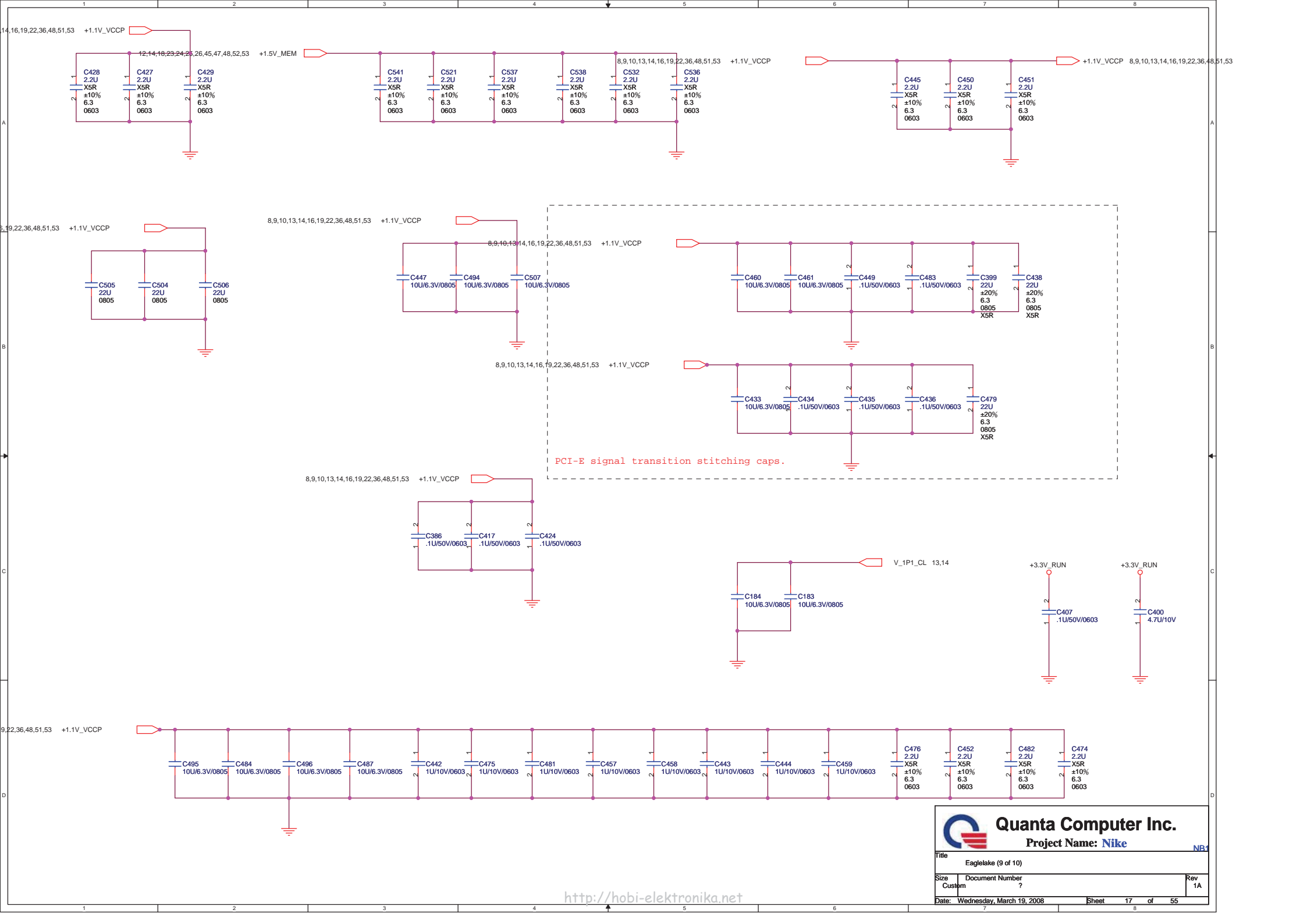
Sheet: 15 of 55

Rev: 1A

8,9,10,13,14,17,19,22,36,48,51,53 +1.1V_VCCP



 Quanta Computer Inc.	
Project Name: Nike	
Title: Eaglelake (7 of 10)	
Size: Custom	Document Number: ?
Date: Wednesday, March 19, 2008	Sheet: 16 of 55
	Rev: 1A

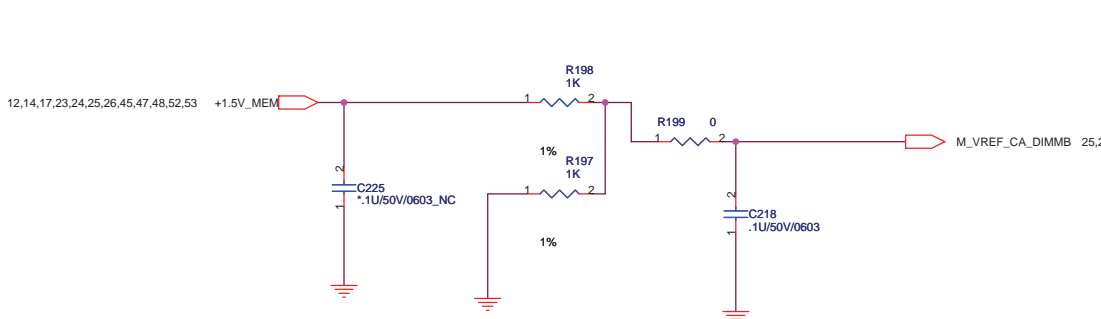
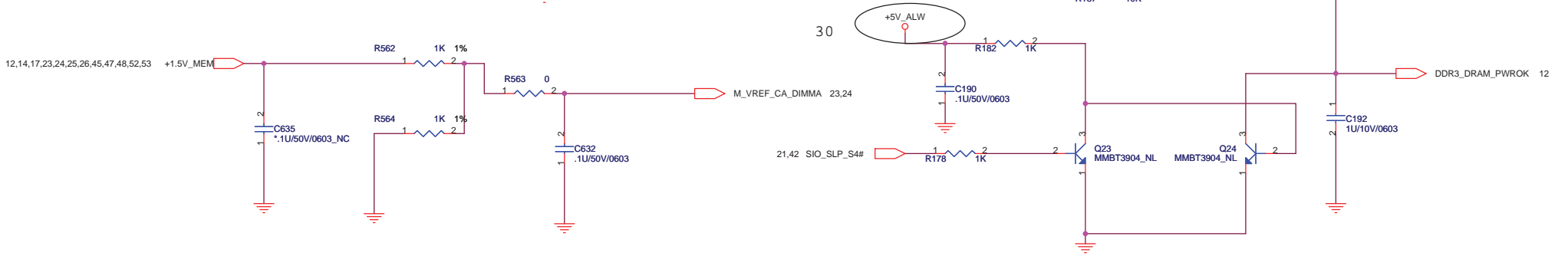
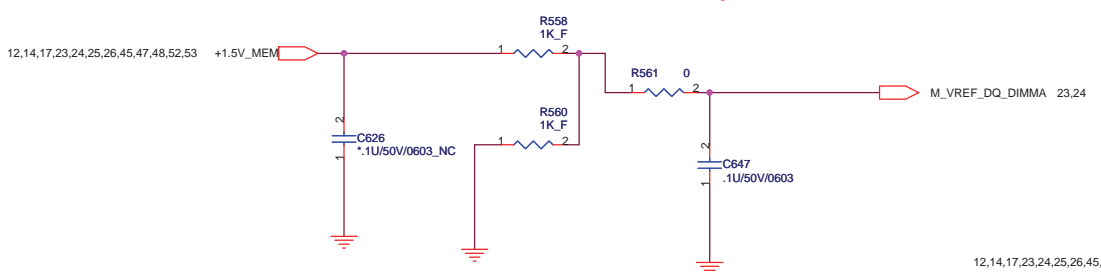
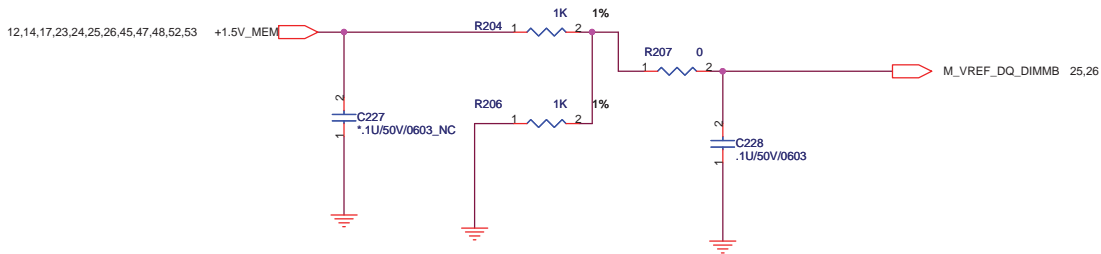


Quanta Computer Inc.
Project Name: Nike

Title: Eaglelake (9 of 10)

Size: Custom	Document Number: ?	Rev: 1A
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Date: Wednesday, March 19, 2008 Sheet 17 of 55

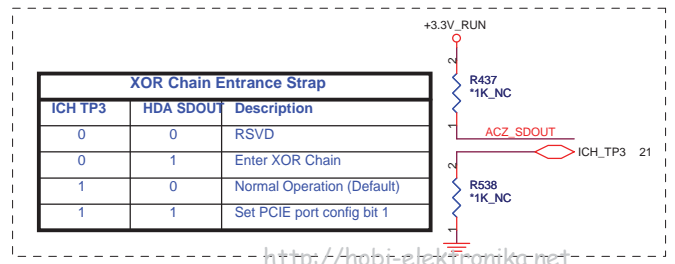
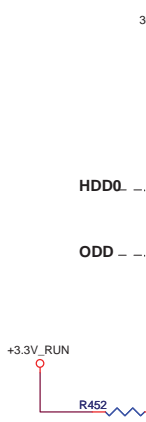
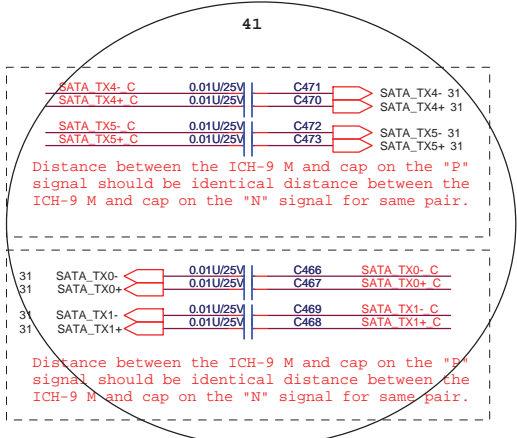
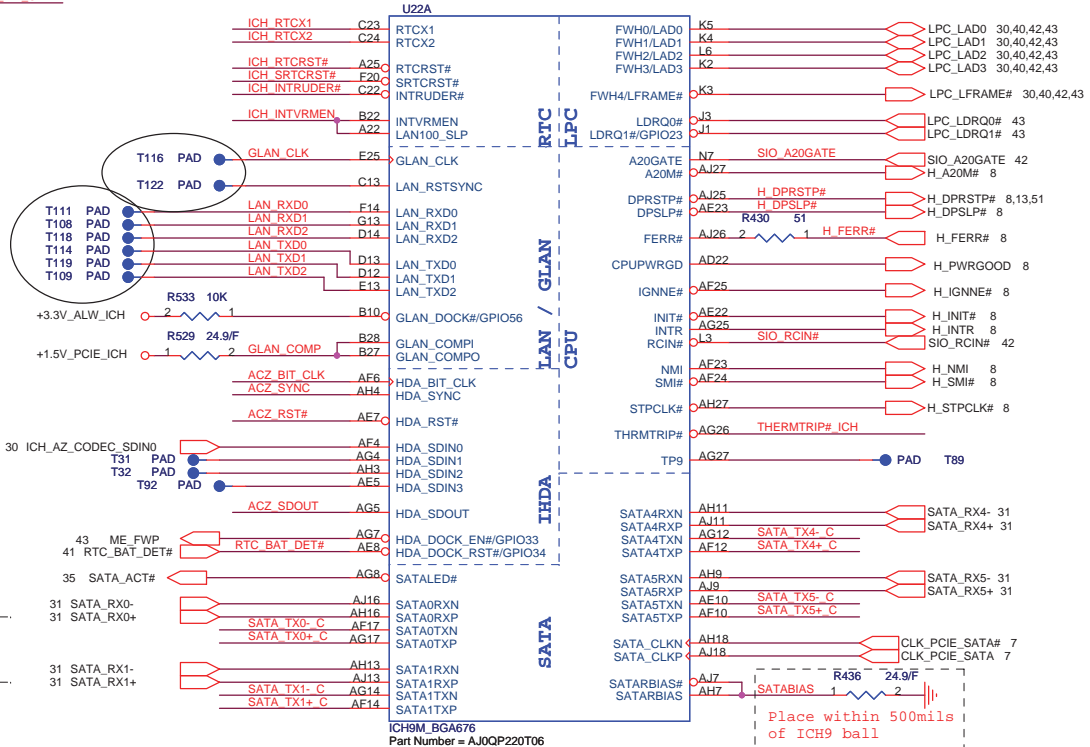
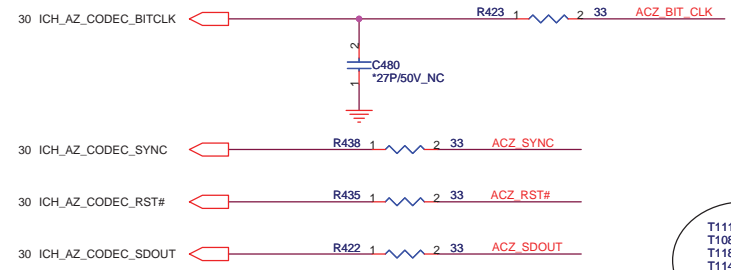
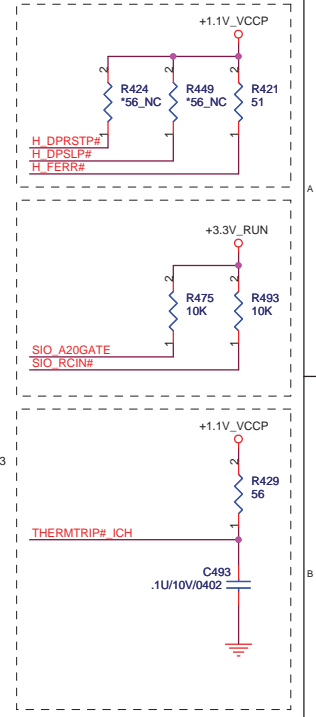
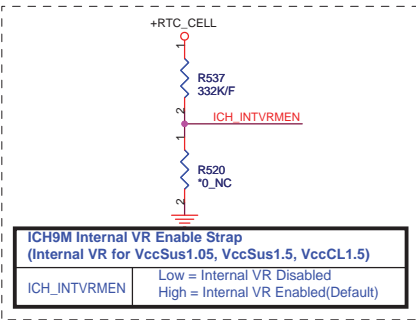
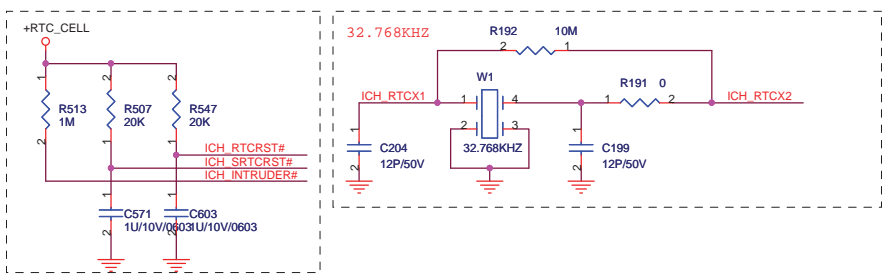


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Project Name: Nike

Title: Eaglelake (10 of 10)

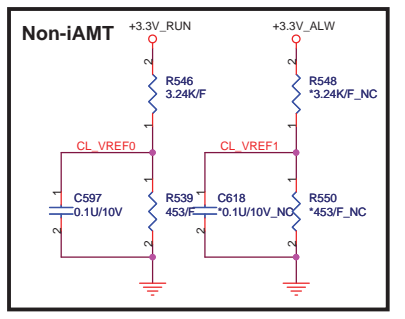
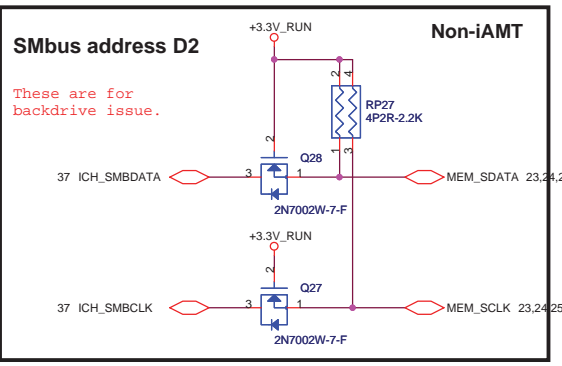
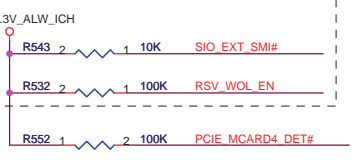
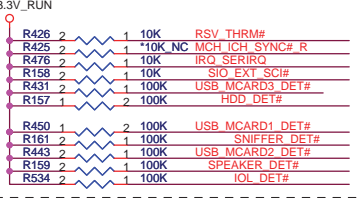
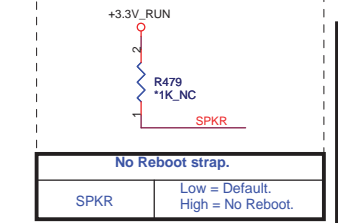
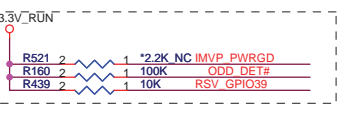
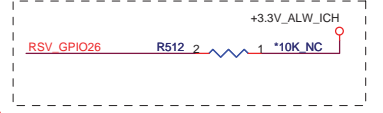
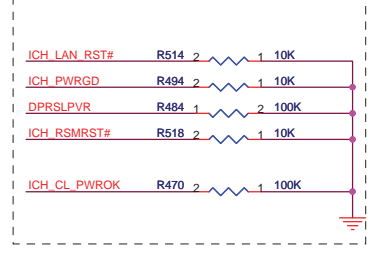
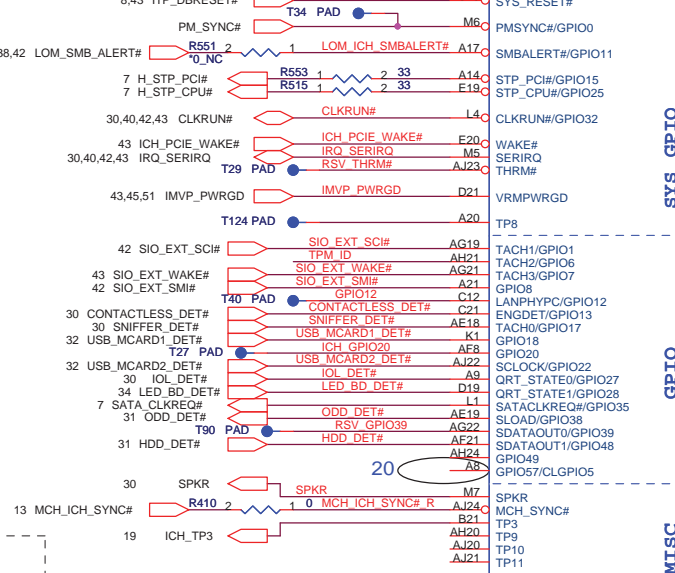
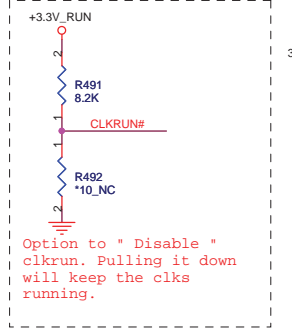
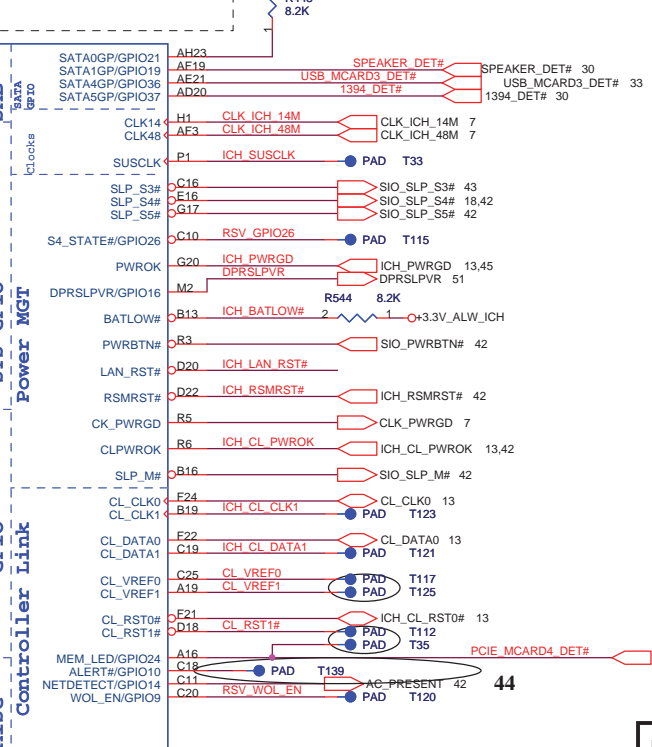
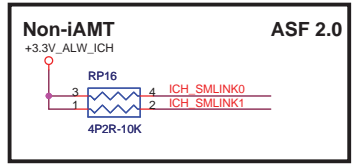
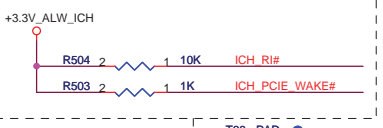
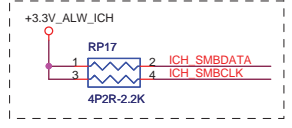
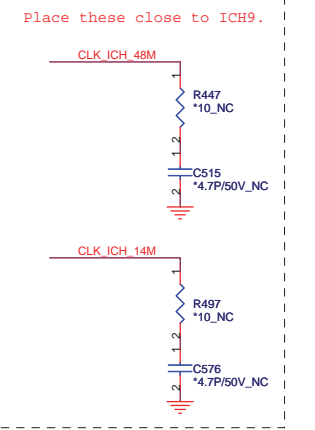
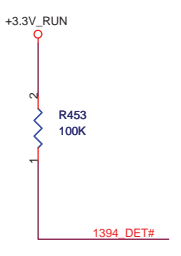
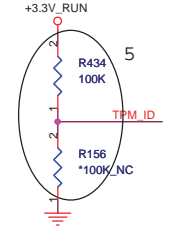
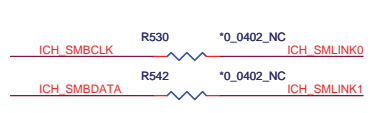
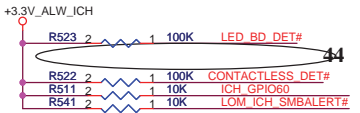
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Date: Wednesday, March 19, 2008 Sheet 18 of 55



Quanta Computer Inc.
Project Name: Nike

Title: ICH9M (1 of 4)
Size: Custom Document Number ?
Date: Wednesday, March 19, 2008 Sheet 19 of 55



Quanta Computer Inc.
Project Name: Nike

Title: ICH9M (3 of 4)

Size: Custom

Document Number: ?

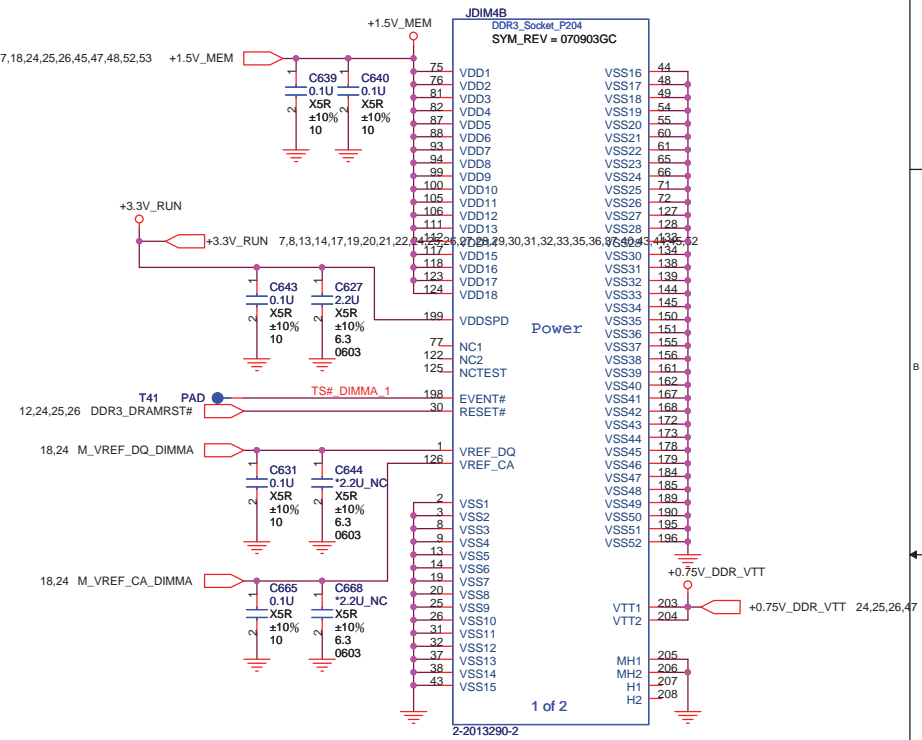
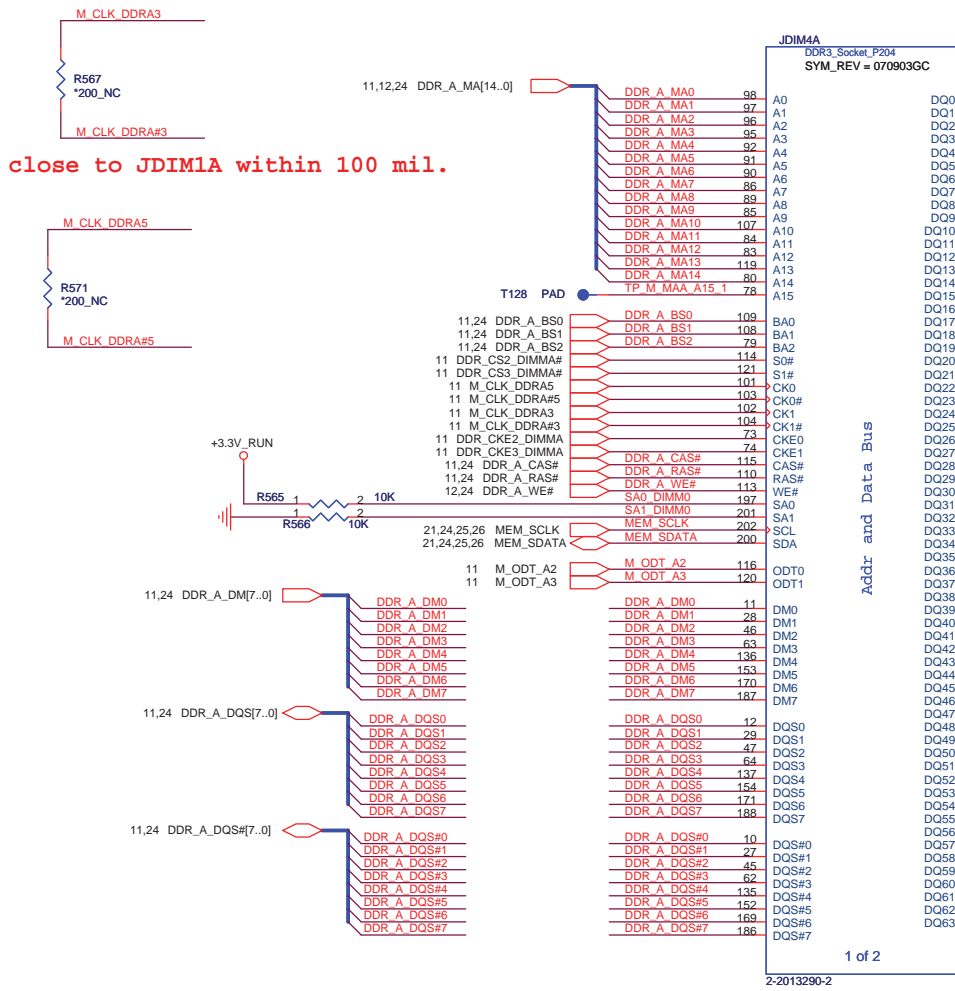
Date: Wednesday, March 19, 2008

Sheet: 21 of 55

Rev: 1A

close to JDIM1A within 100 mil.

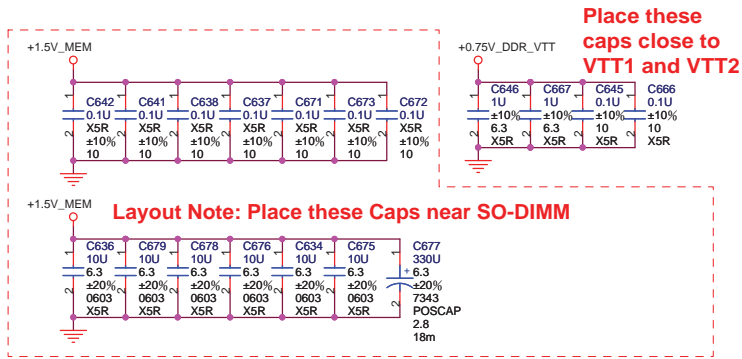
CHA_DIMM1_Bottom Layer



close to JDIM1A within 100 mil.

Select the Serial Presence Detect and Temp sensor base address.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	



Quanta Computer Inc.
Project Name: Nike

Title: DDR3 Channel A0 (1 of 5)

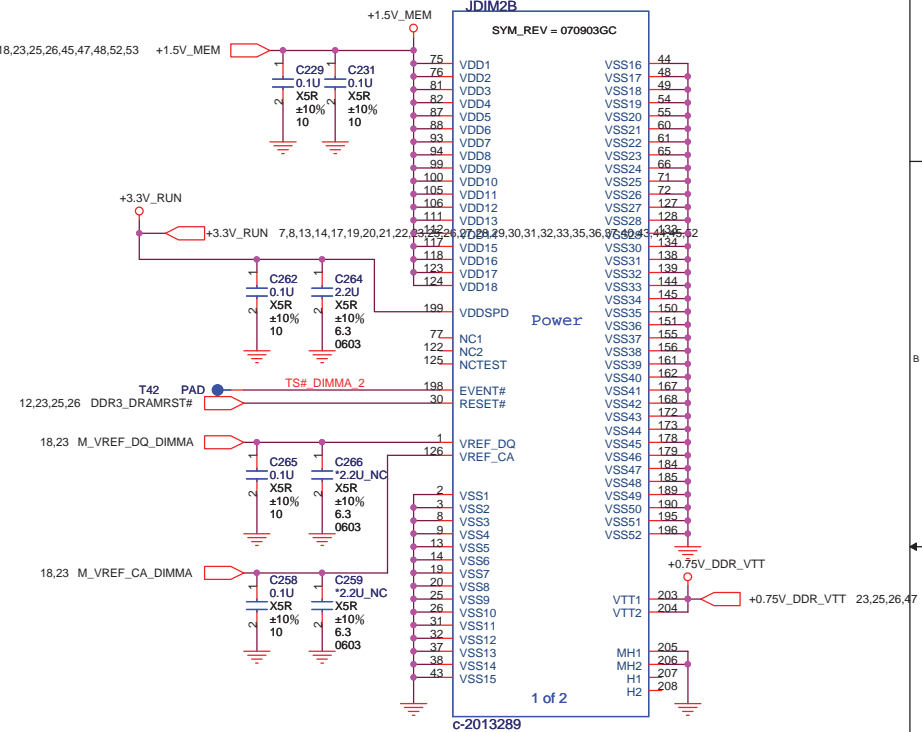
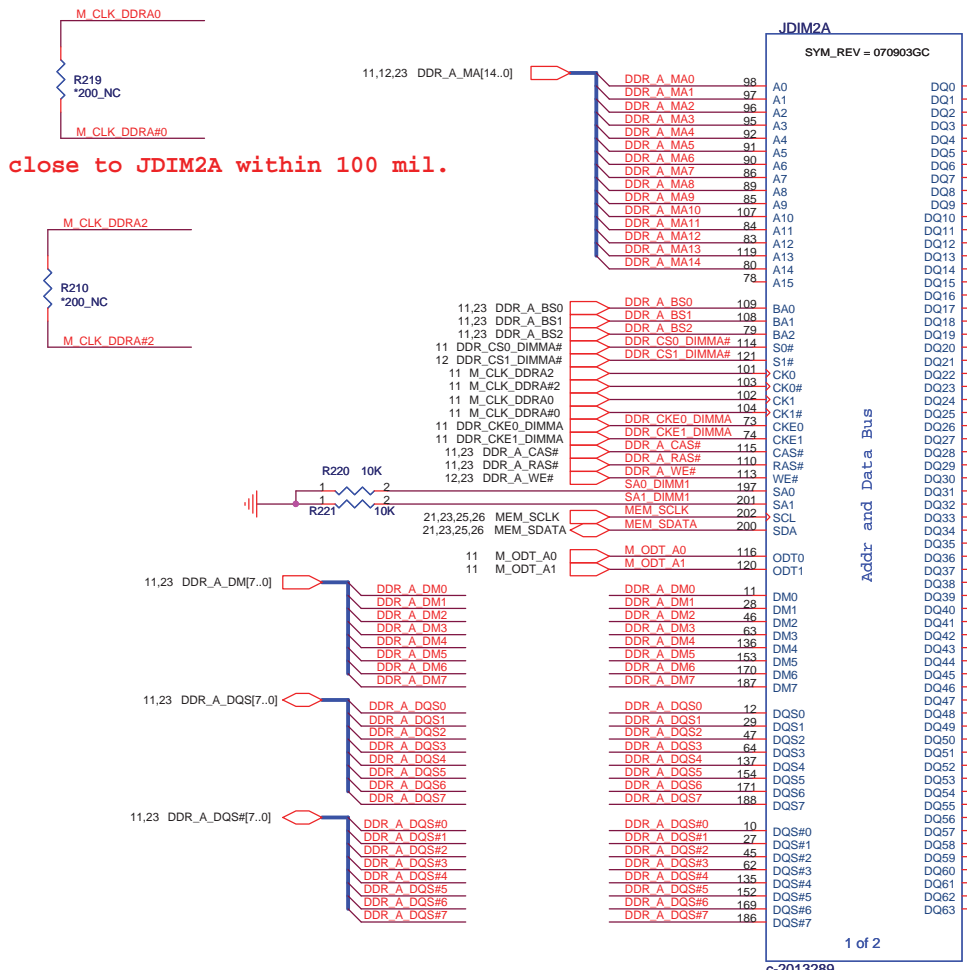
Size: Custom Document Number: ? Rev: 1A

Date: Wednesday, March 19, 2008 Sheet: 23 of 55

close to JDIM2A within 100 mil.

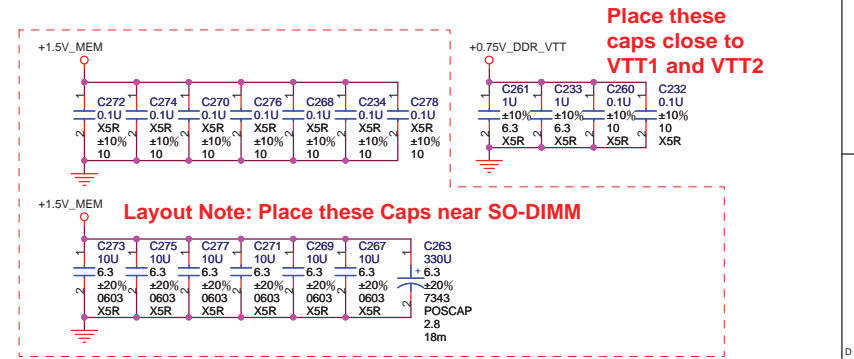
CHA_DIMM0_TOP Layer

close to JDIM2A within 100 mil.



Select the Serial Presence Detect and Temp sensor base address.

	SA1	SA0	Note
CHA0	0	0	
CHA1	0	1	Pull-High to +3.3V_RUN
CHB0	1	0	
CHB1	1	1	



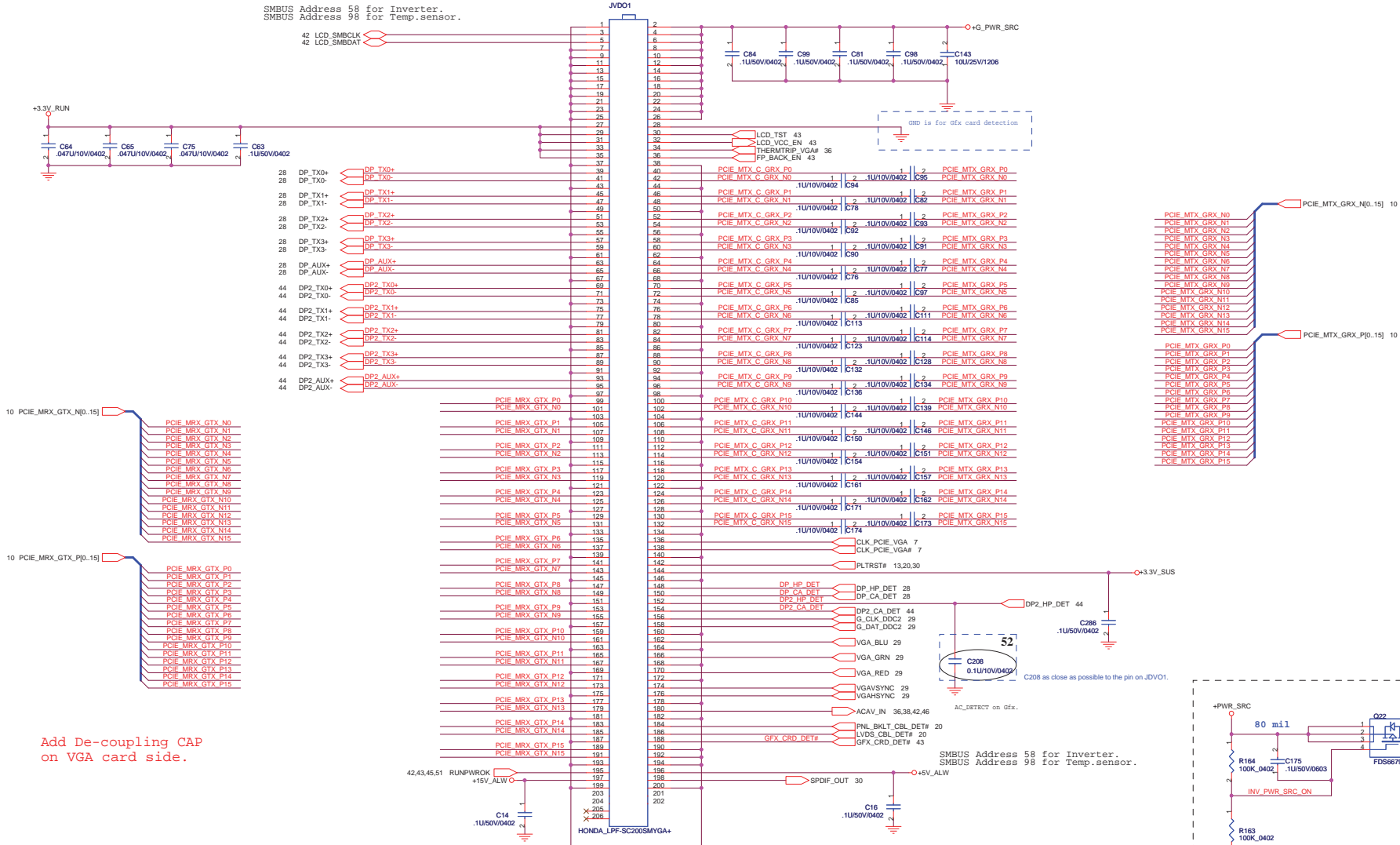
Quanta Computer Inc.
Project Name: Nike

Title: DDR3 Channel A1 (2 of 5)

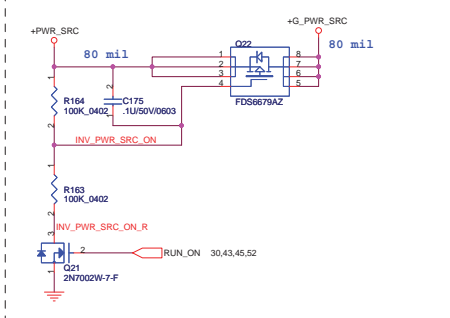
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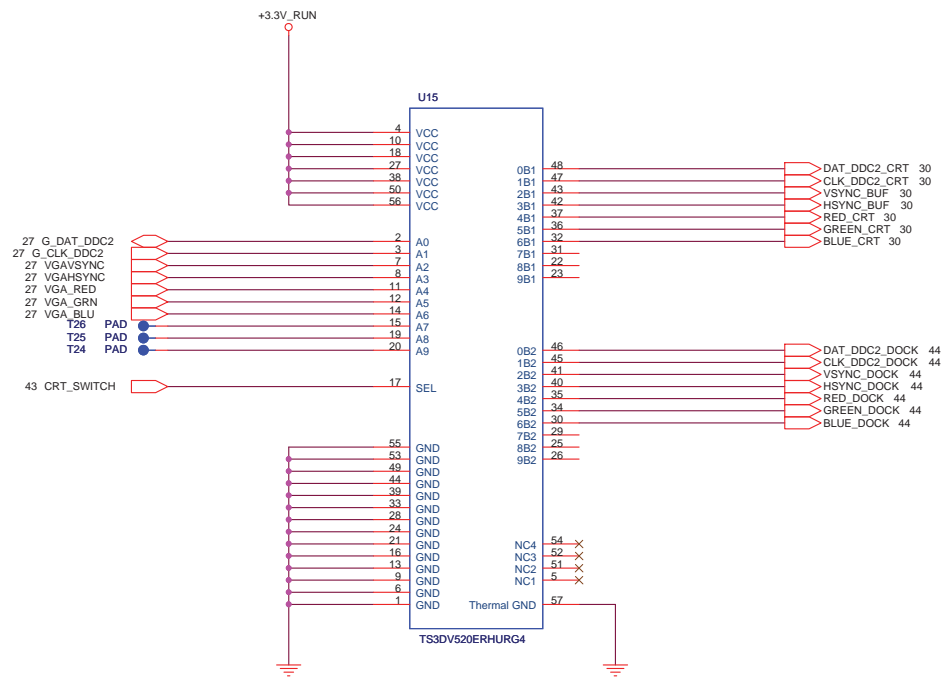
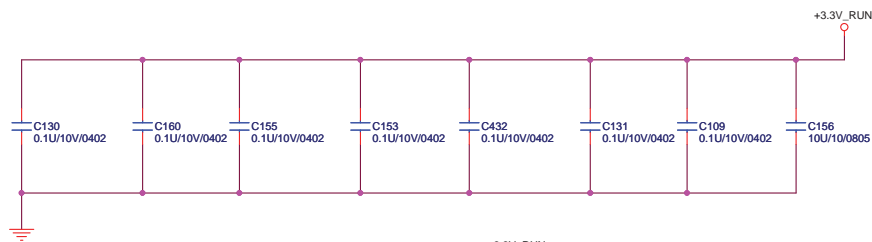
Date: Wednesday, March 19, 2008 Sheet: 24 of 55

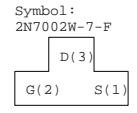
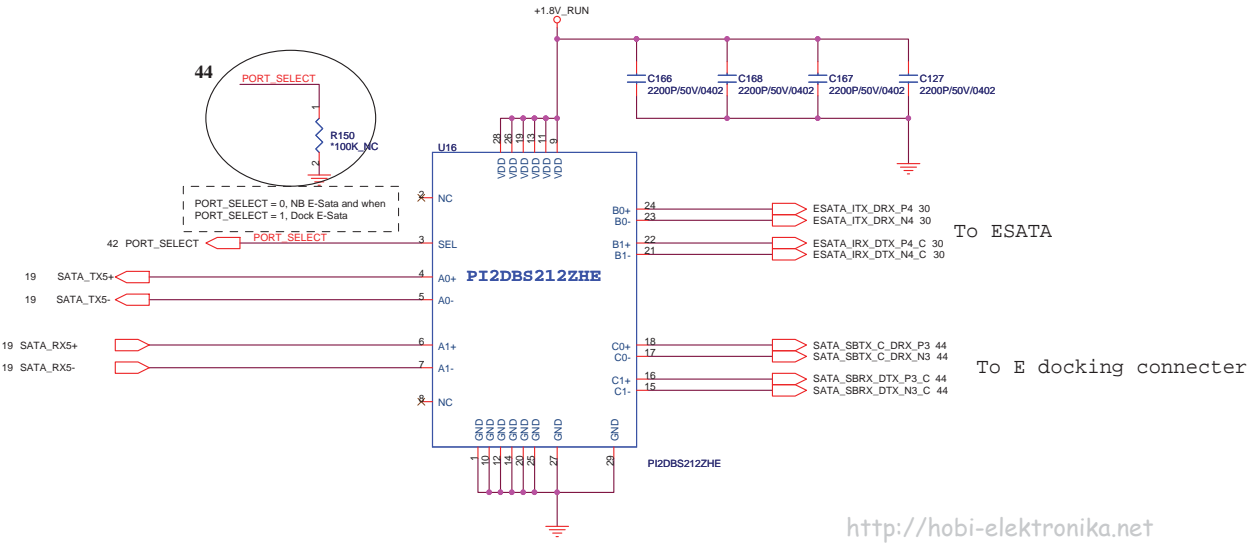
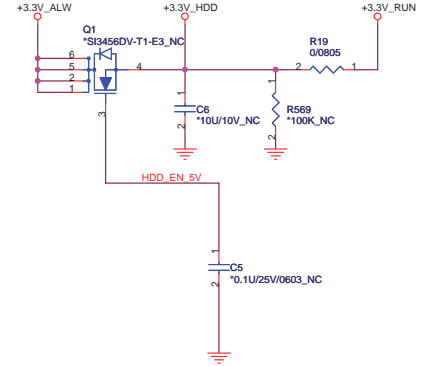
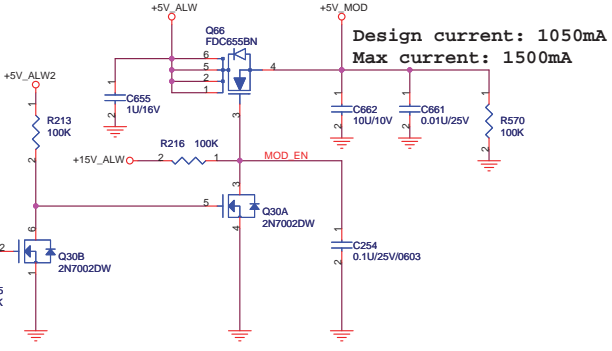
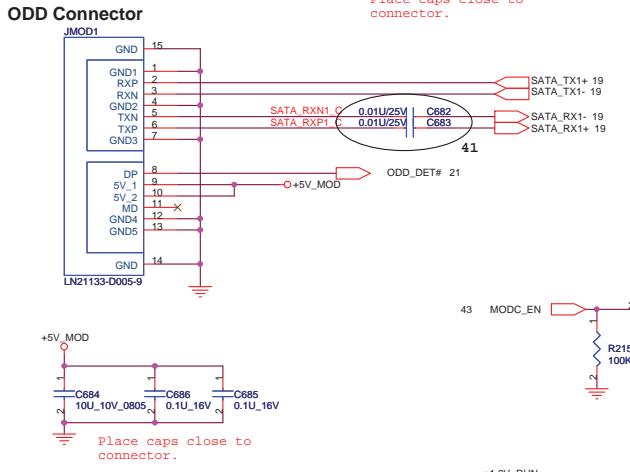
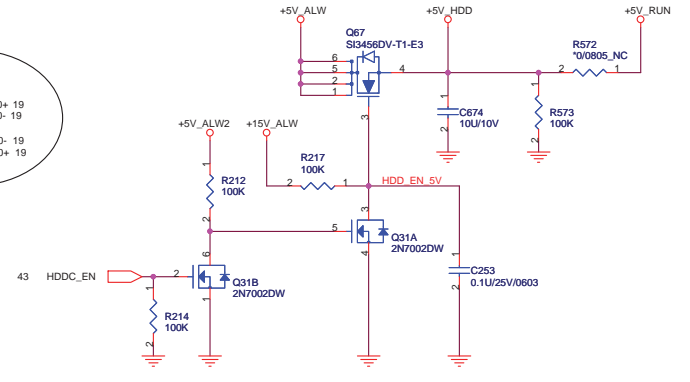
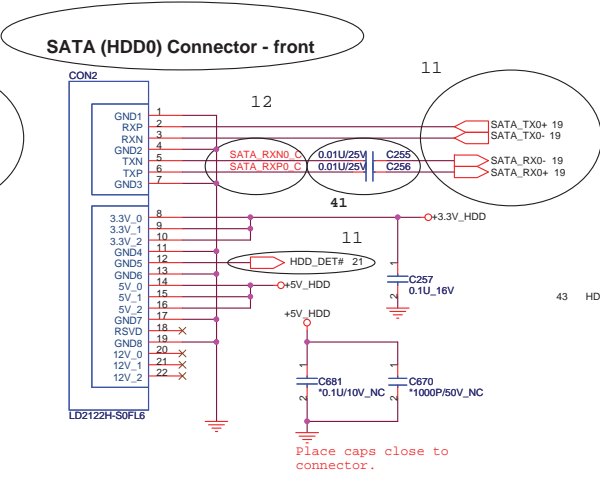
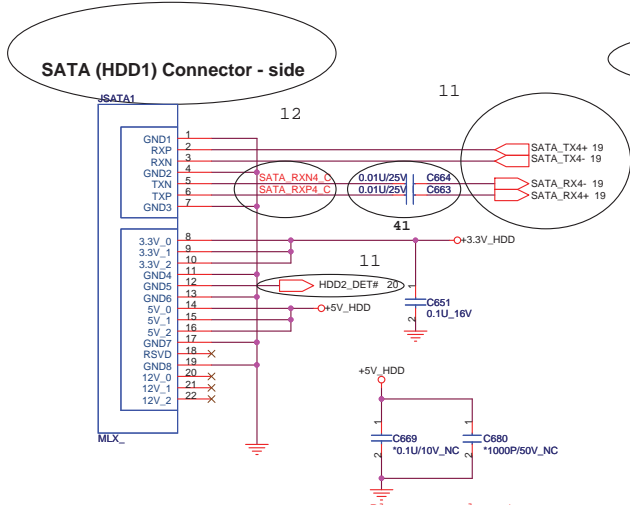
SMBUS Address 58 for Inverter.
SMBUS Address 98 for Temp.sensor.



Add De-coupling CAP on VGA card side.





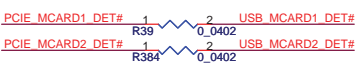
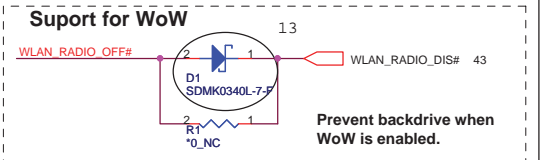
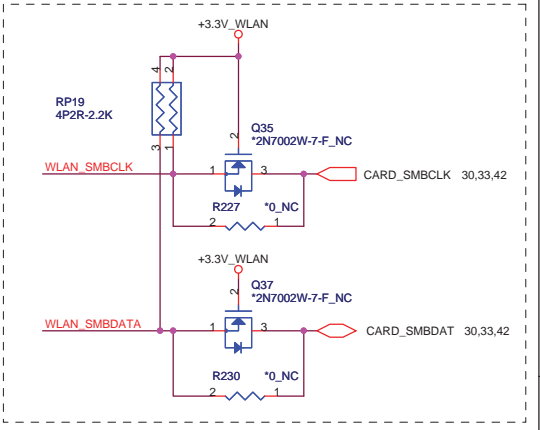
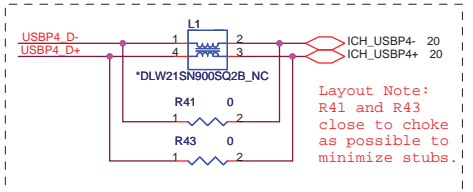
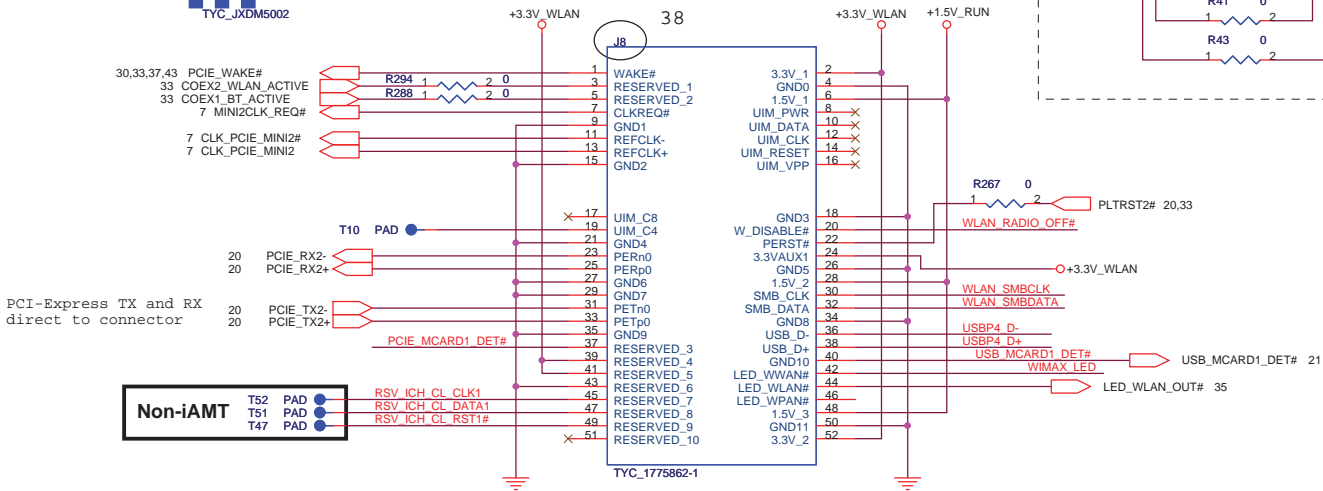


Quanta Computer Inc.
Project Name: Nike

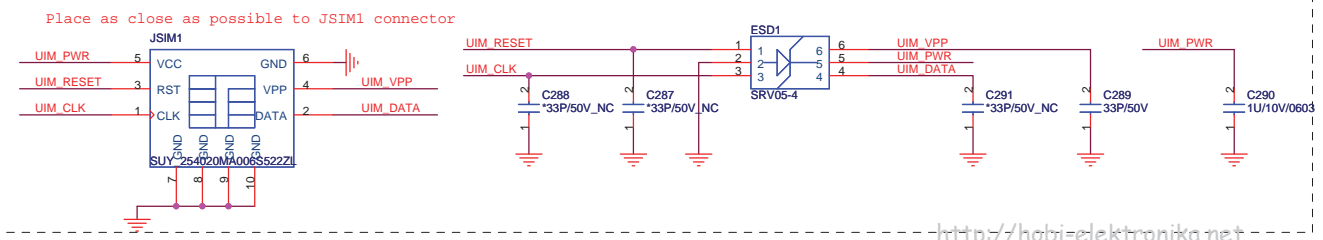
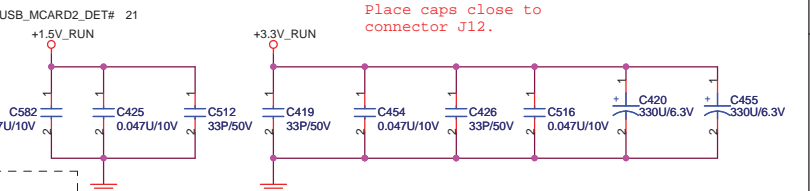
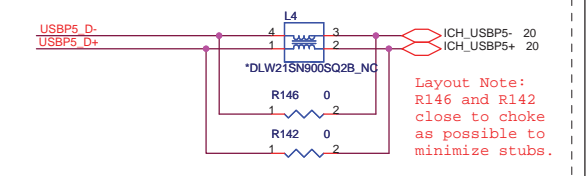
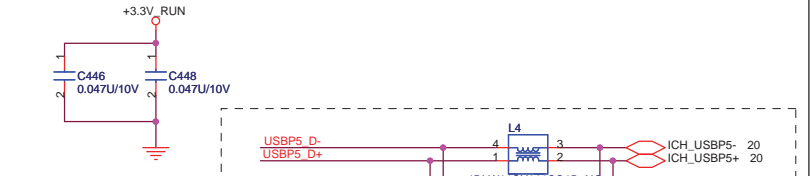
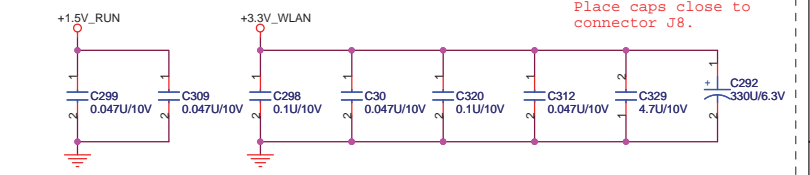
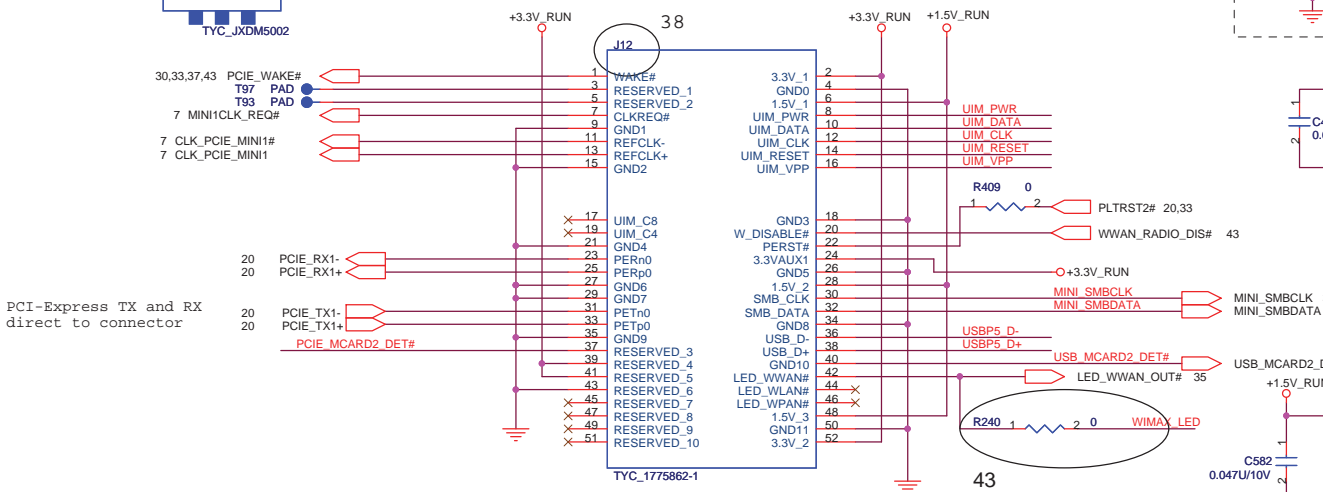
Title: SATA (HDD_ODD) eSATA SWITCH		Rev: 1A
Size: Custom	Document Number: SATA (HDD&ODD)	Sheet: 31 of 55
Date: Wednesday, March 19 2008		



MiniCard WLAN connector



MiniCard WWAN connector

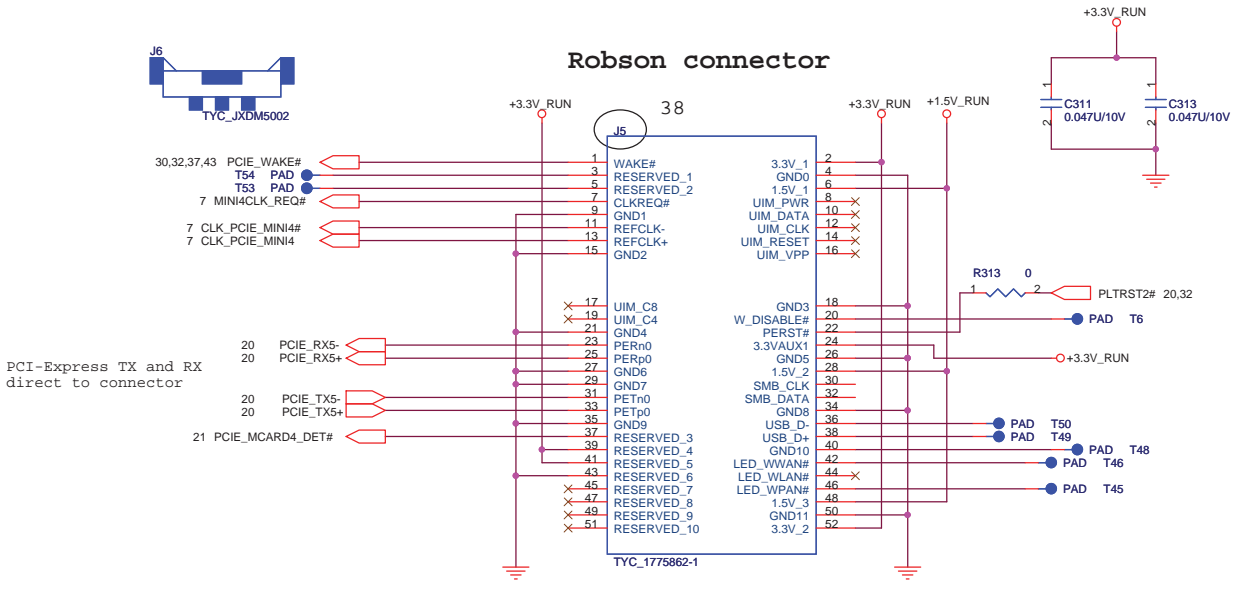


Quanta Computer Inc.
 Project Name: Nike

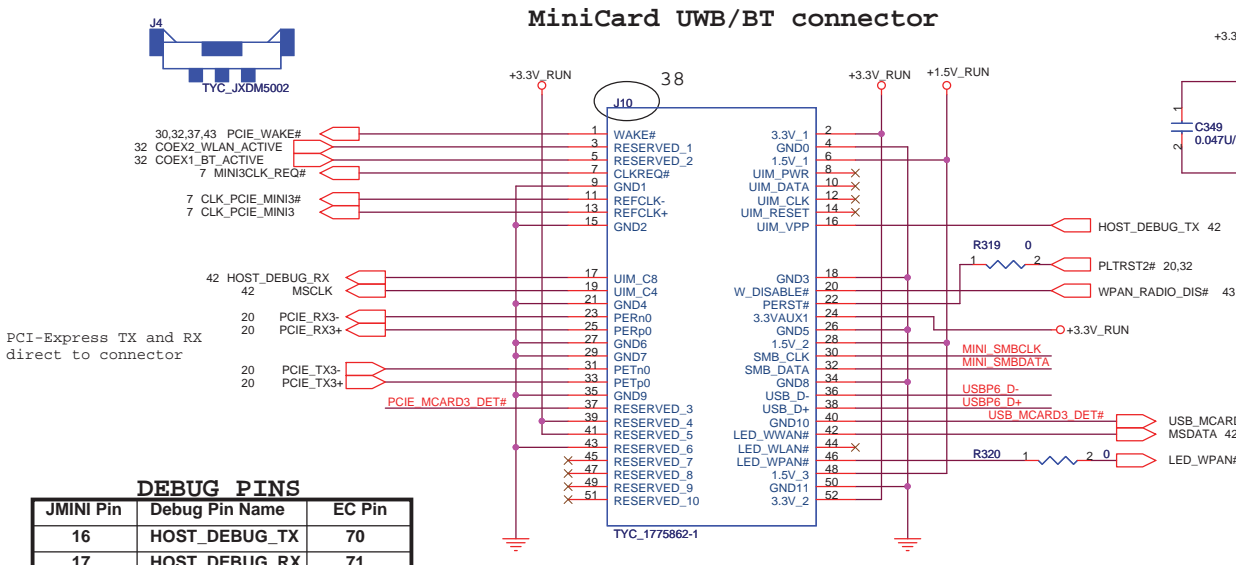
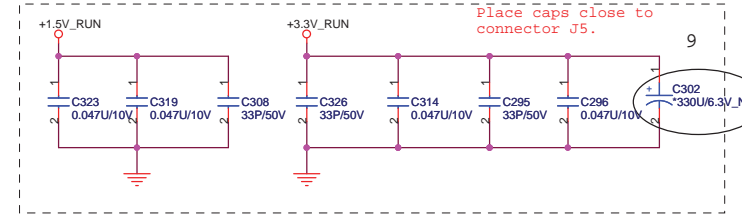
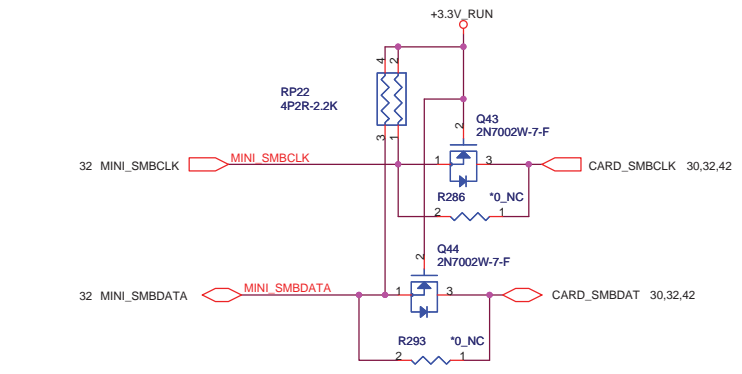
Title: MINI CARD

Size: Custom	Document Number: ?	Rev: 1A
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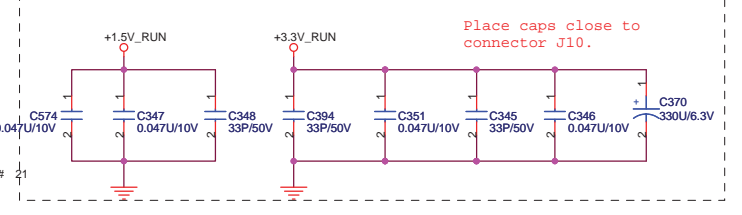
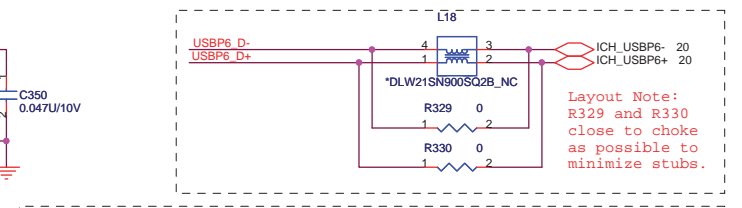
Date: Wednesday, March 19, 2008 Sheet 32 of 55



PCI-Express TX and RX direct to connector



PCI-Express TX and RX direct to connector



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

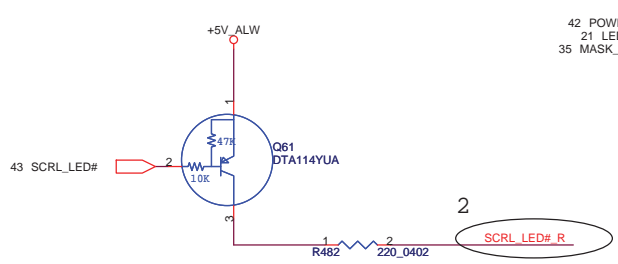
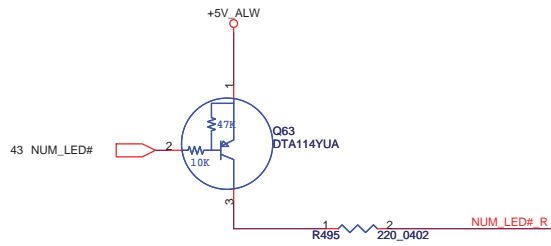
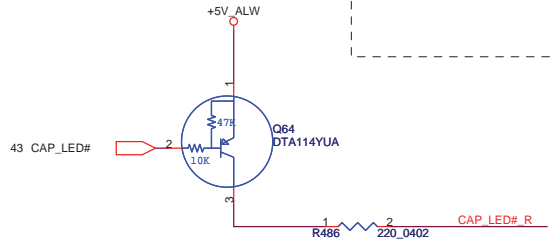
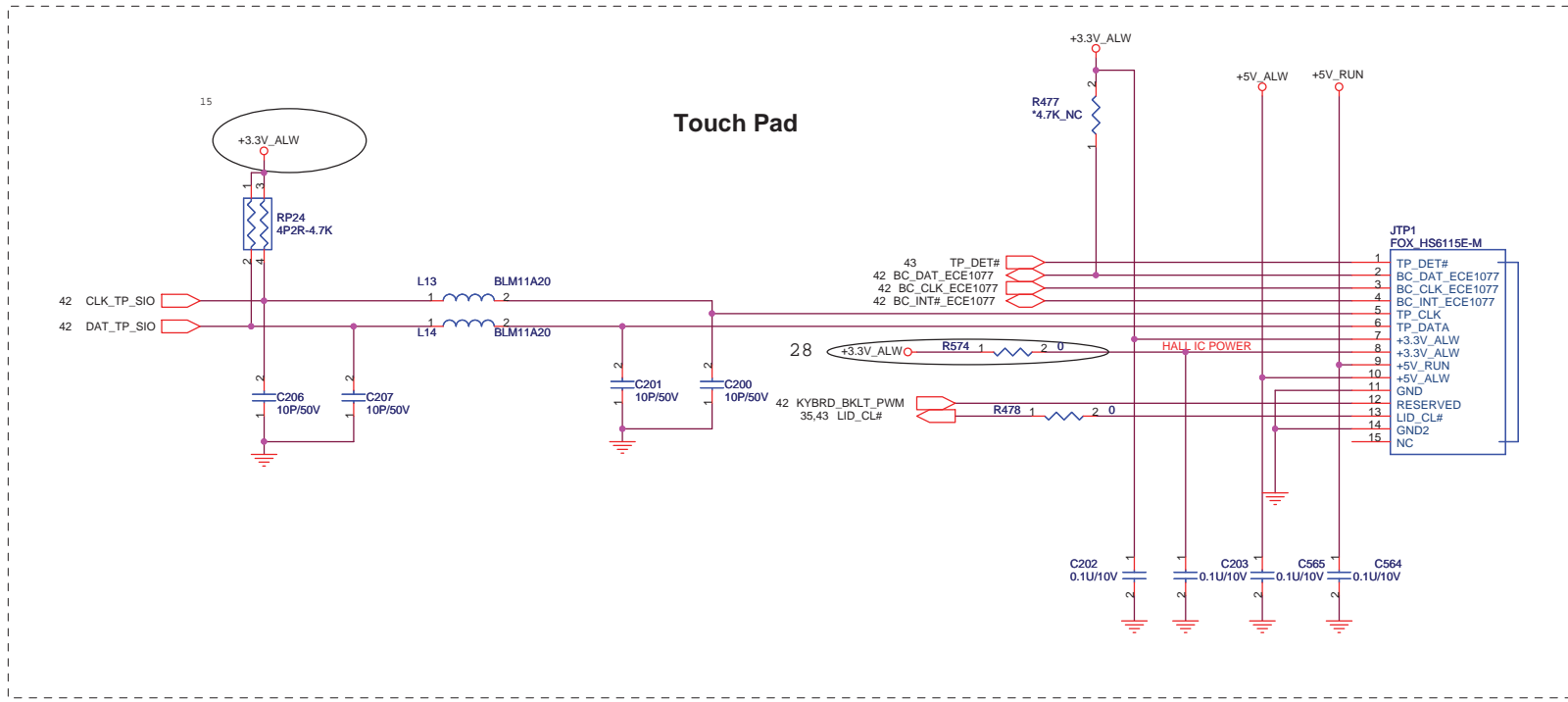


Quanta Computer Inc.
Project Name: Nike

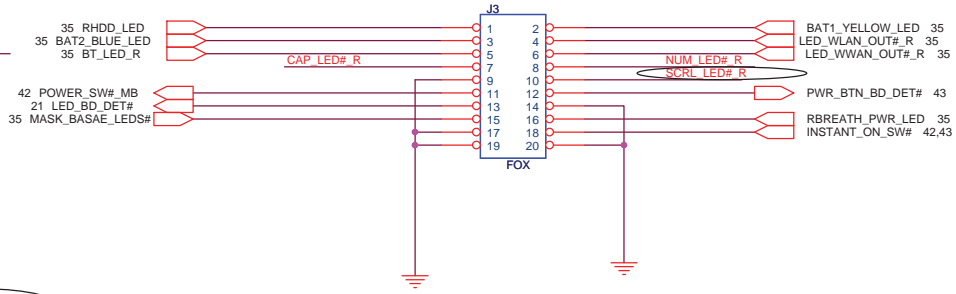
Title: MINI CARD

Size: Custom Document Number: ? Rev: 1A

Date: Wednesday, March 19, 2008 Sheet: 33 of 55

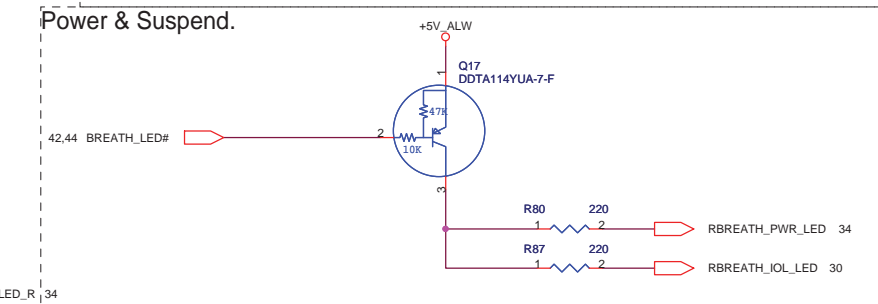
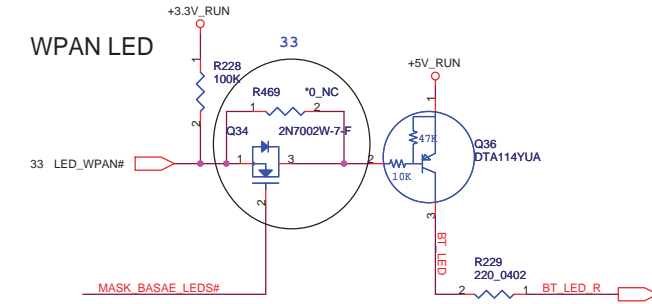
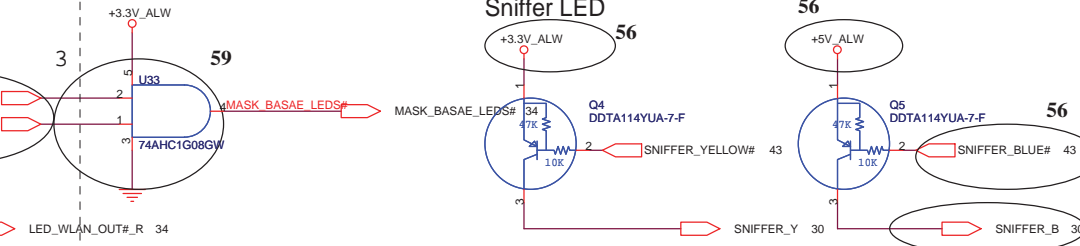
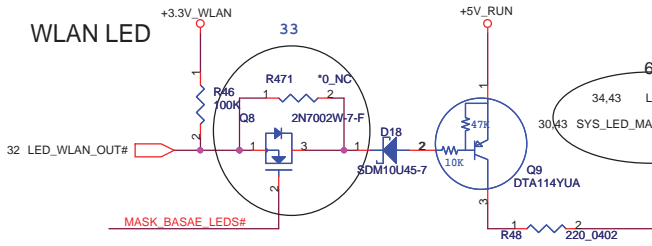
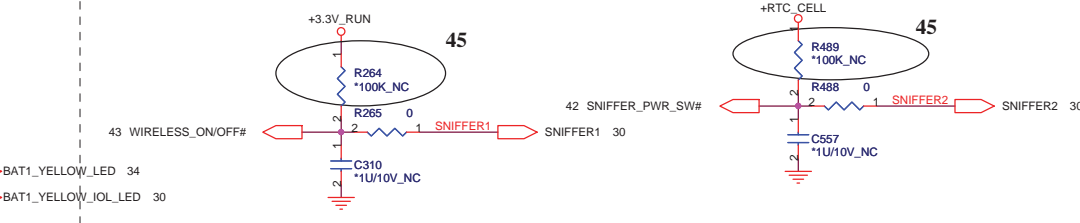
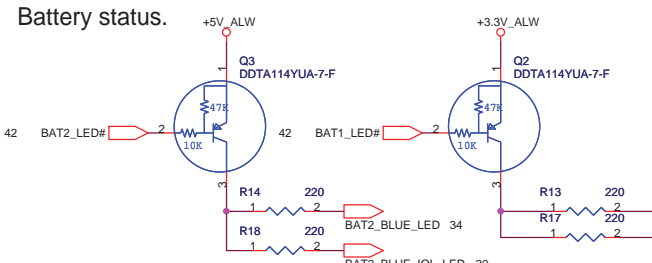
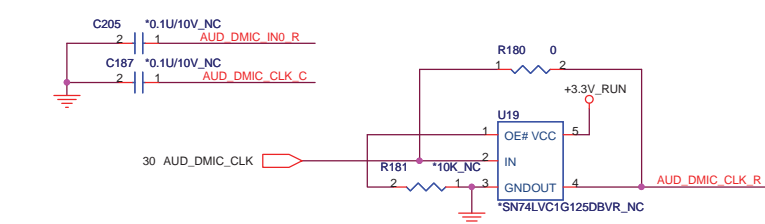
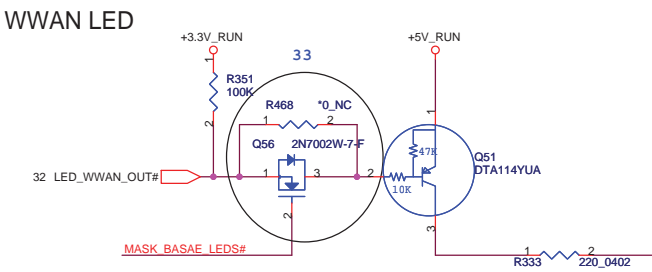
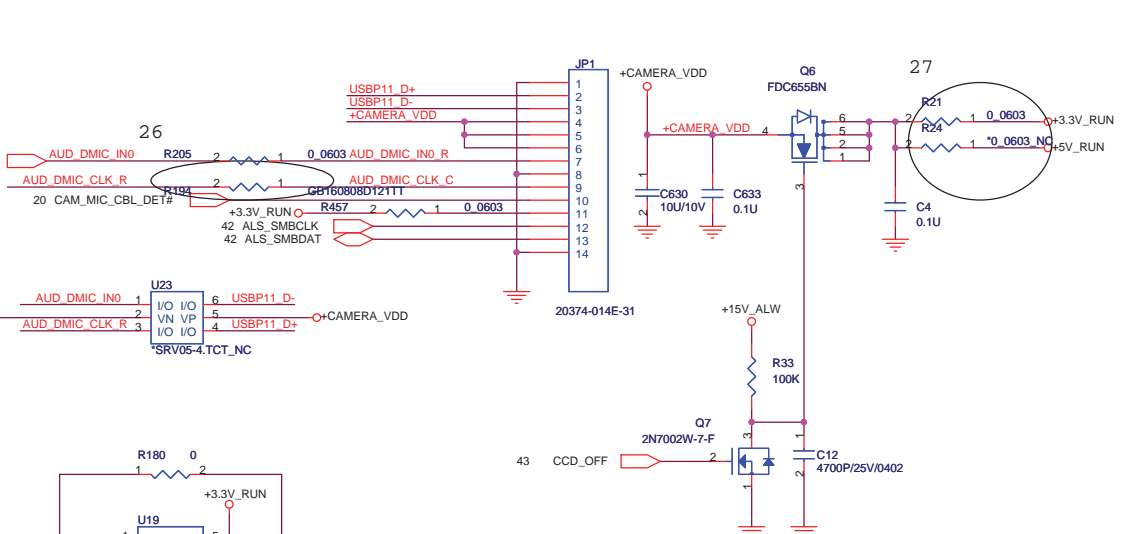
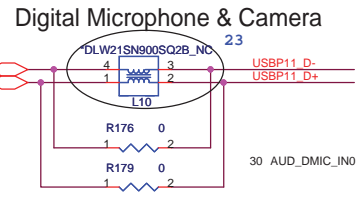
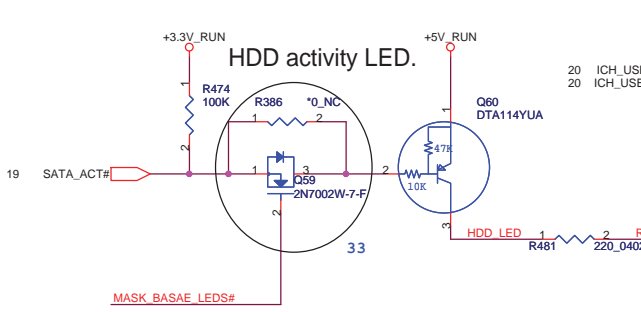


PWR_BTN board connector



Quanta Computer Inc.
Project Name: **Nike**

Title TP_PWR_BUTTON	
Size Custom	Document Number ?
Date: Wednesday, March 19, 2008	Rev 1A
Sheet	34 of 55



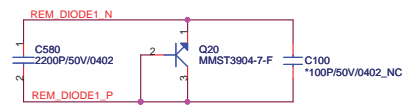
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base LEDs (Lid Closed)	1	0
Do Not Mask LEDs (Lid Open)	1	1

Quanta Computer Inc.
Project Name: **Nike**

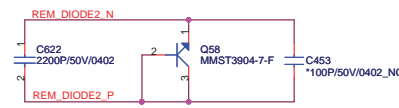
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Size: Custom Document Number: ?

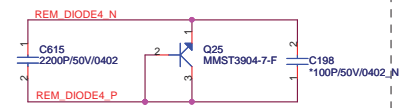
Date: Wednesday, March 19, 2008 Sheet 35 of 55



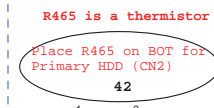
Put C580 close to Guardian.
Put C100 close to Diode
Place under CPU



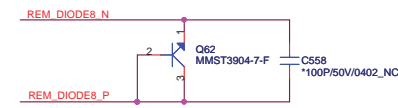
Put C622 close to Guardian.
Put C453 close to Diode
Skin Temperature



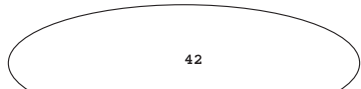
Put C615 close to Guardian.
Put C198 close to Diode
Place under DIMM Channel 1(TOP)



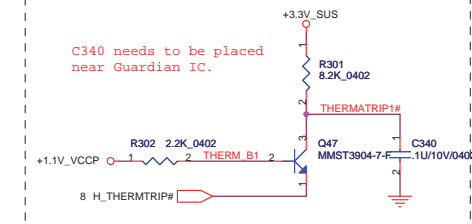
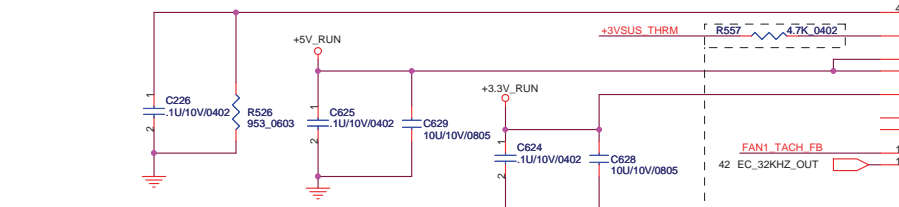
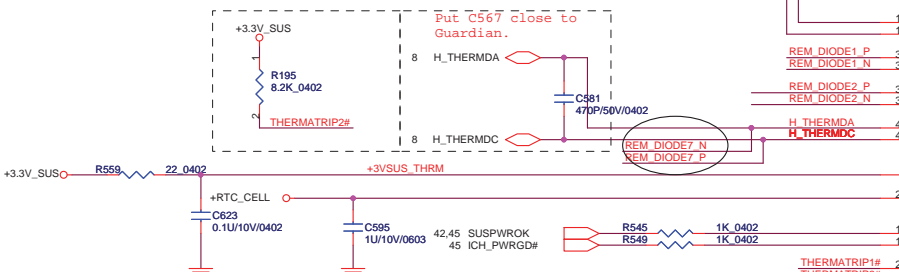
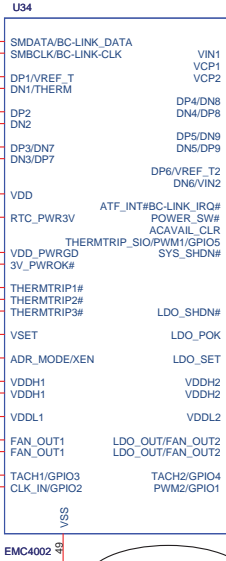
R465 is a thermistor
Place R465 on BOT for Primary HDD (CN2)
Put R463 and C589 close to Guardian.



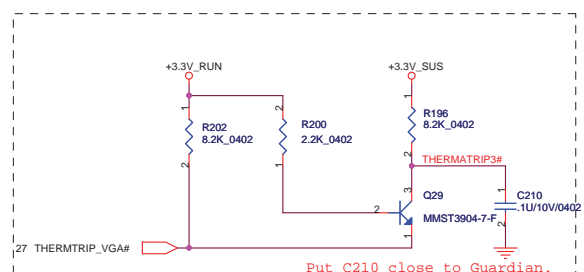
Put C558 close to Diode
Place under DIMM Channel 2(TOP)



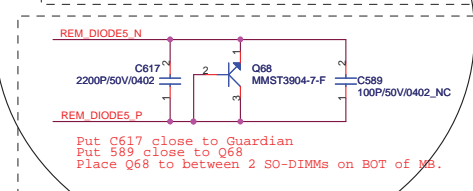
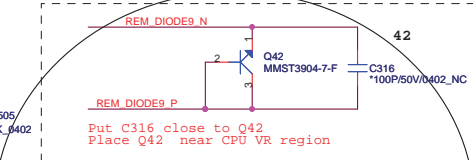
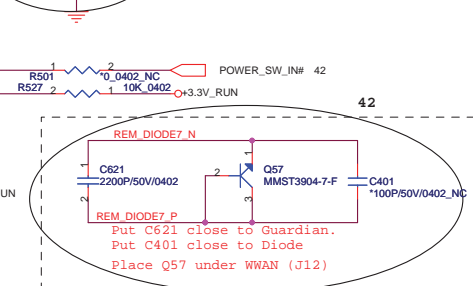
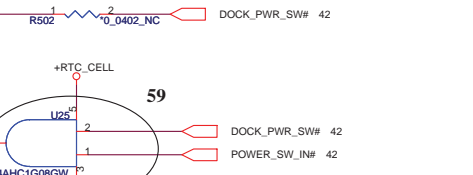
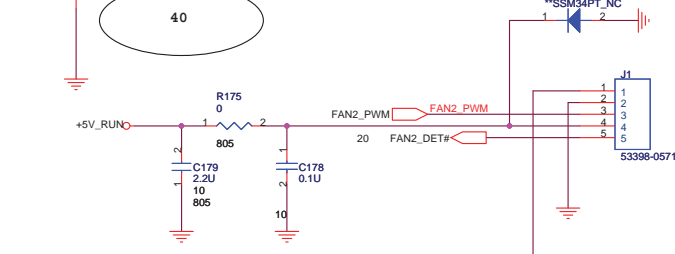
OTP temperature 88C



Pull-up Resistor on ADDR_MODE/XEN	For Remotel mode	SMBUS Address
<=4.7K	2N3904	2F(x/w)
10K	2N3904	2E(x/w)
18K	Thermistor	2F(x/w)
>=33K	Thermistor	2E(x/w)



Put C210 close to Guardian.



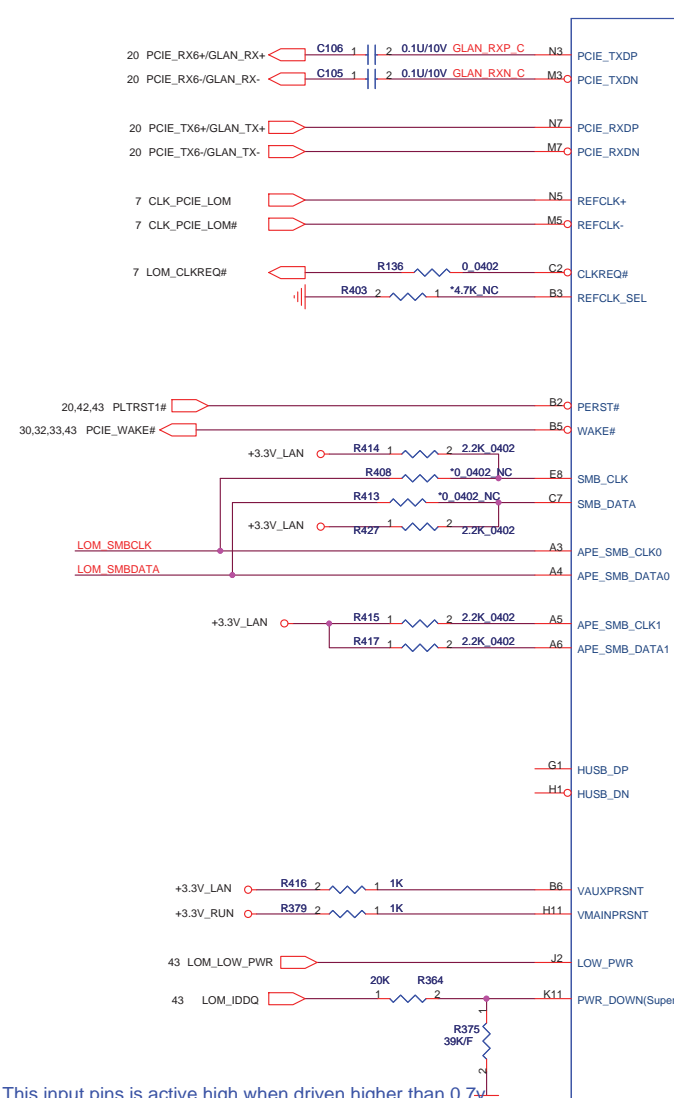
Quanta Computer Inc.
Project Name: Nike

Title: THERMAL_EMC4002

Date: Wednesday, March 19, 2008

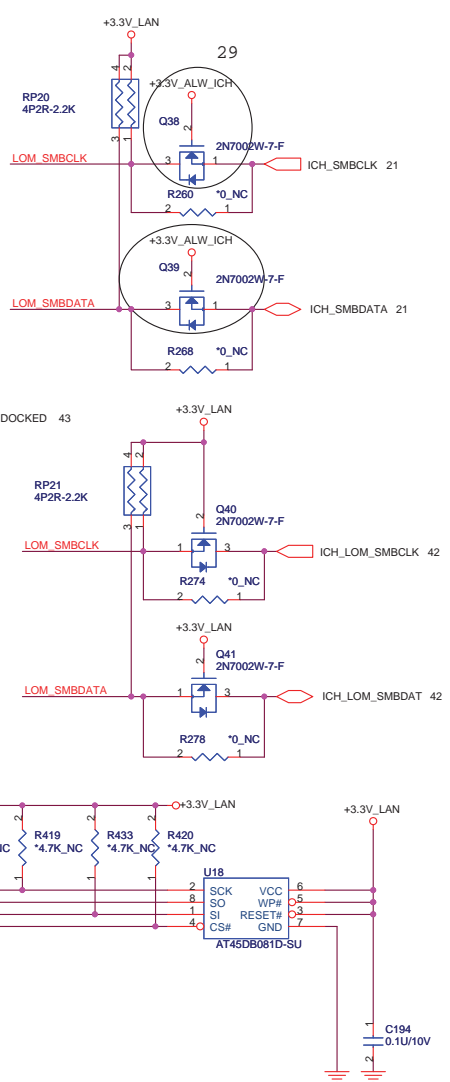
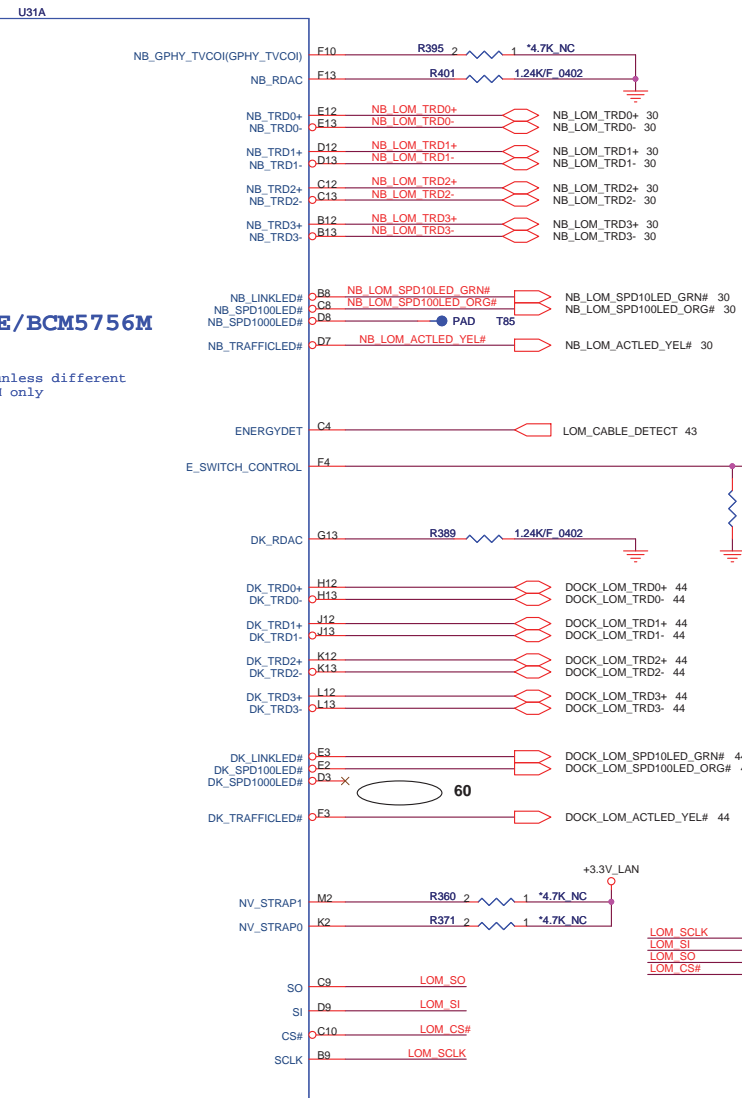
Sheet 36 of 55

Rev 1A

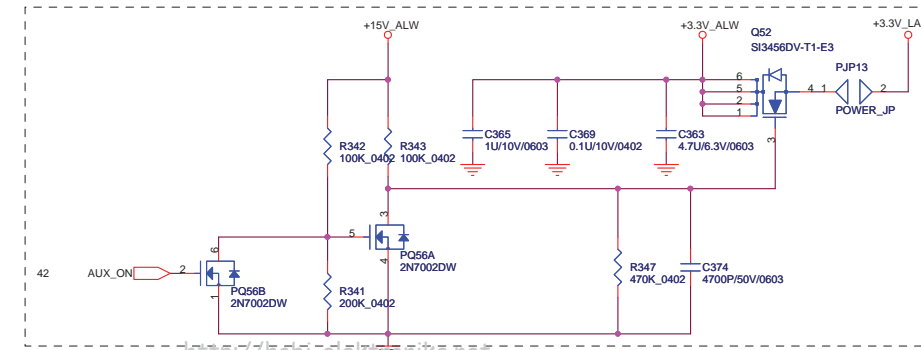


BCM5761E/BCM5756M

Name - 5761E
 Name - 5756M unless different
 (Name) - 5756M only

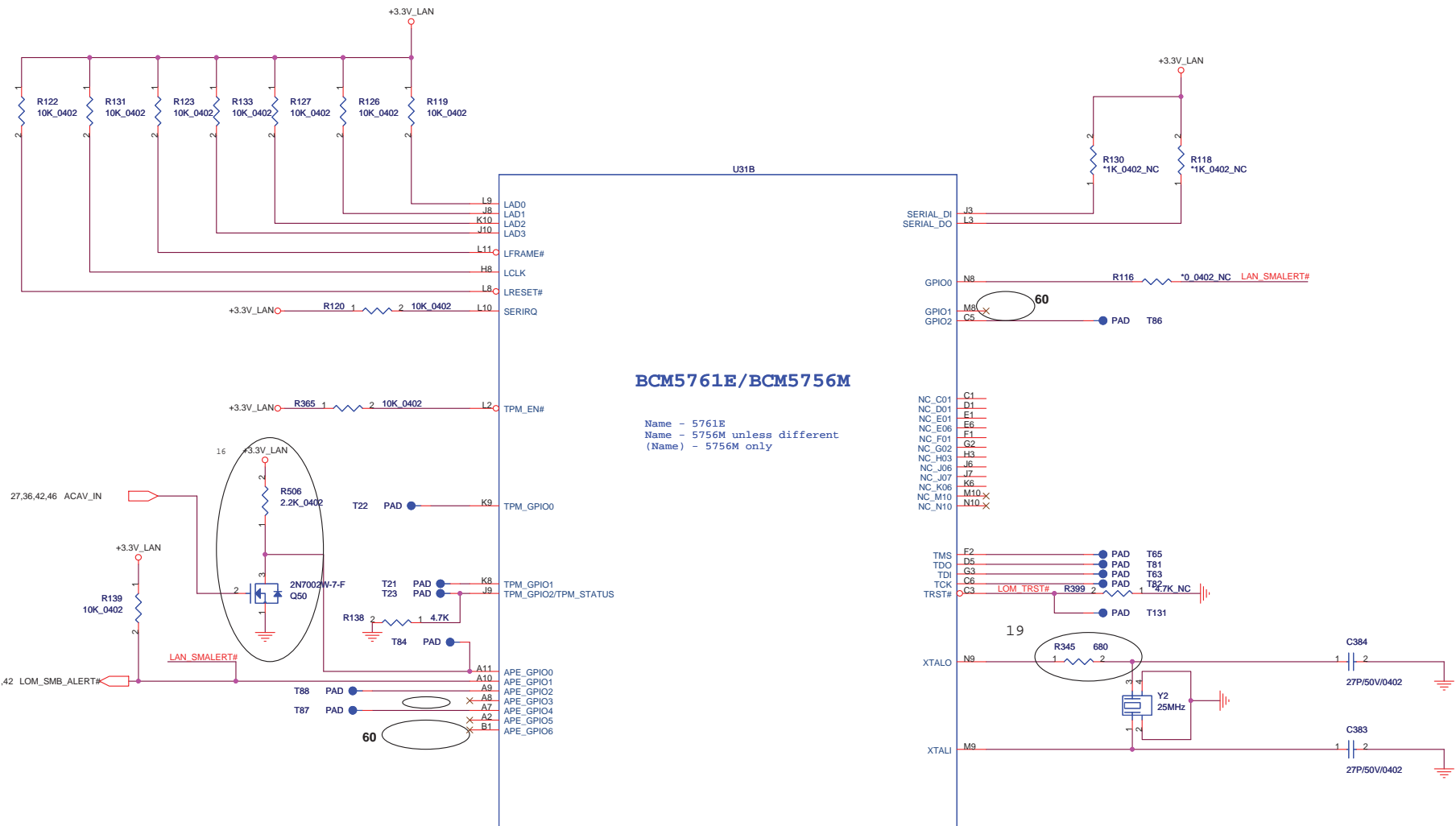


This input pins is active high when driven higher than 0.7V and its max voltage high is 2.75v. It's inactive when driven lower than 0.3v.



Quanta Computer Inc.
 Project Name: Nike NB1

Title	LOM (1 of 3)	
Size	Document Number	Rev
Custom	?	1A
Date: Wednesday, March 19, 2008	Sheet 37 of 55	

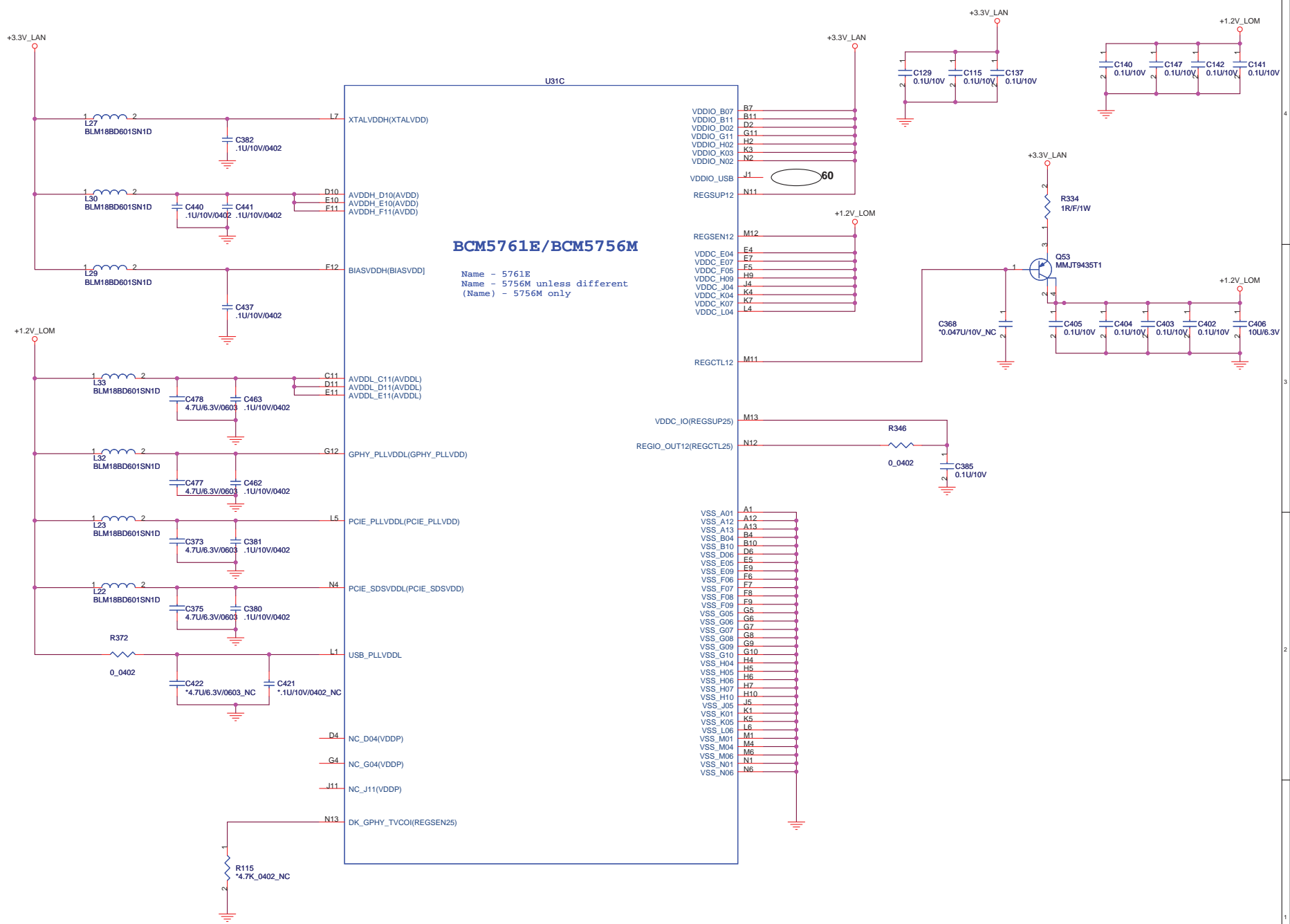


BCM5761E/BCM5756M

Name - 5761E
 Name - 5756M unless different
 (Name) - 5756M only

Quanta Computer Inc.
 Project Name: **Nike** NB1

Title		LOM (2 of 3)	
Size	Document Number	Rev	
Custom	?	1A	
Date:	Wednesday, March 19, 2008	Sheet	38 of 55

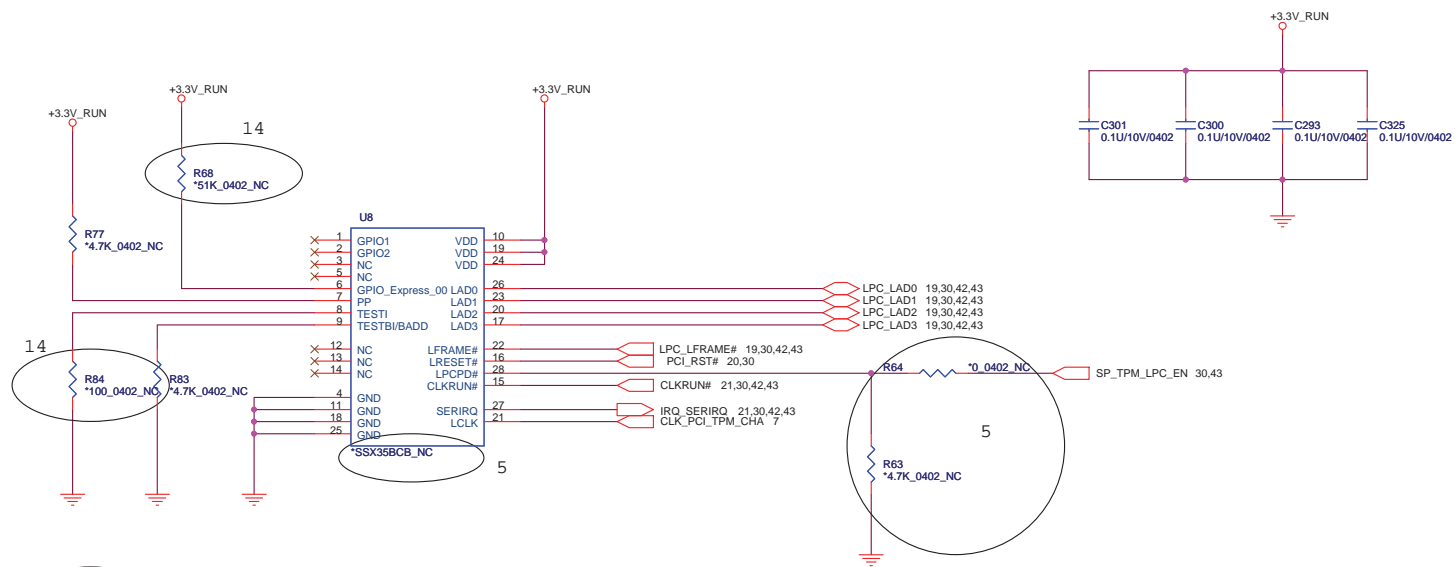


BCM5761E/BCM5756M

Name - 5761E
 Name - 5756M unless different
 (Name) - 5756M only

Quanta Computer Inc.
 Project Name: **Nike** NB1

Title			LOM (3 of 3)		
Size	Document Number	Rev			
Custom	?	1A			
Date: Wednesday, March 19, 2008		Sheet	39	of	55



14 Table1

BOM option scheme for USH TPM vs China TPM

		B0 USH	No TPM
MB	MB, U8	NC	NC
	MB, R27	NC	NC
	MB, R63	NC	NC
	MB, R64	NC	NC
	R77, R68, R84, R83	NC	NC
	MB, R149	POP	POP
	MB, R151	NC	NC
	MB, R156	NC	NC
MB, R434	POP	POP	

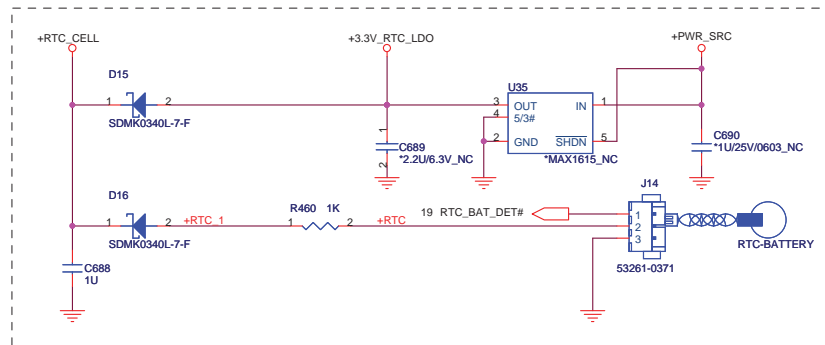
Quanta Computer Inc.
Project Name: **Nike**

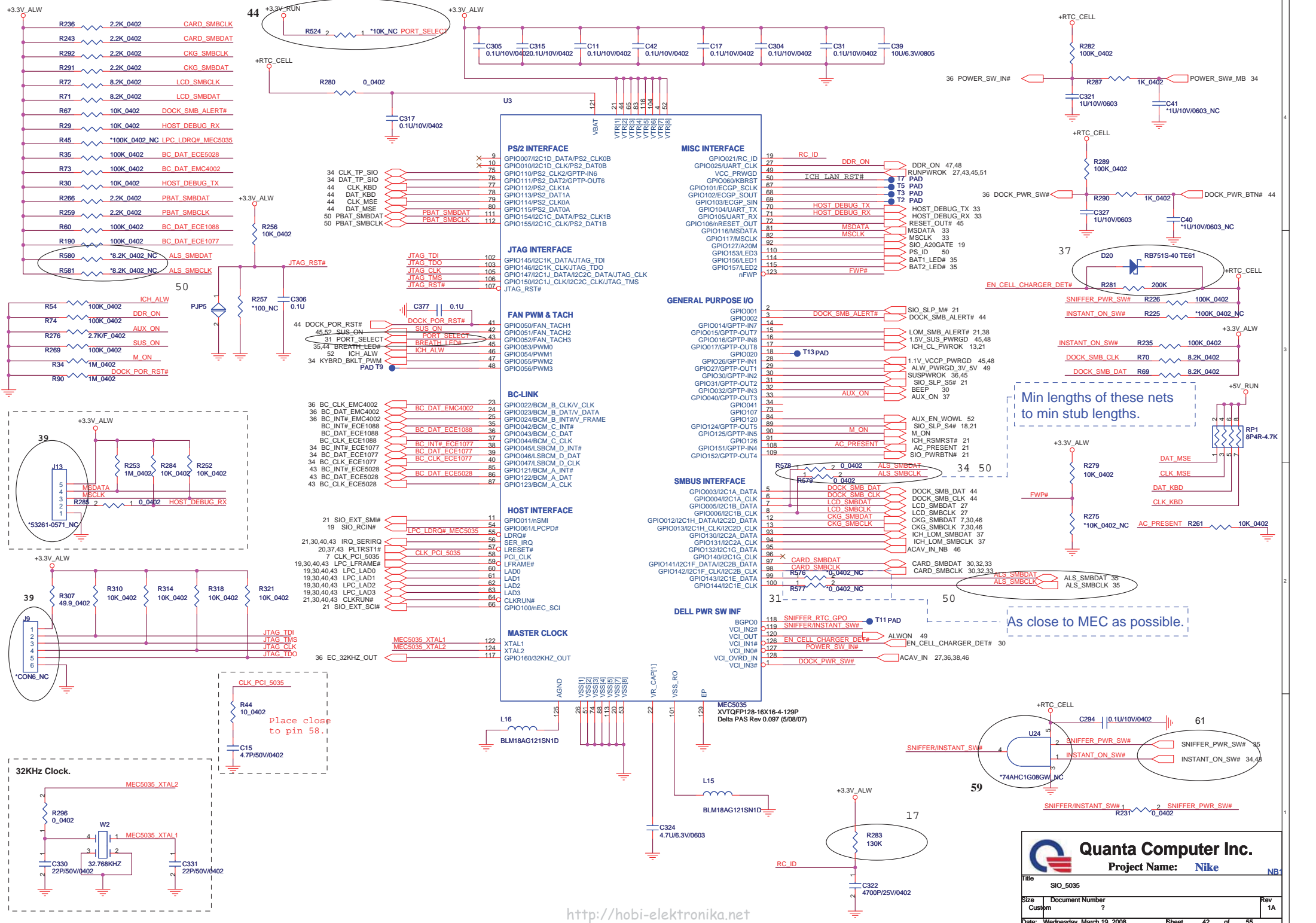
Title: TPM for CHINA

Size	Document Number	Rev
Custom	?	1A

Date: Wednesday, March 19, 2008 Sheet 40 of 55

RTC BATTERY



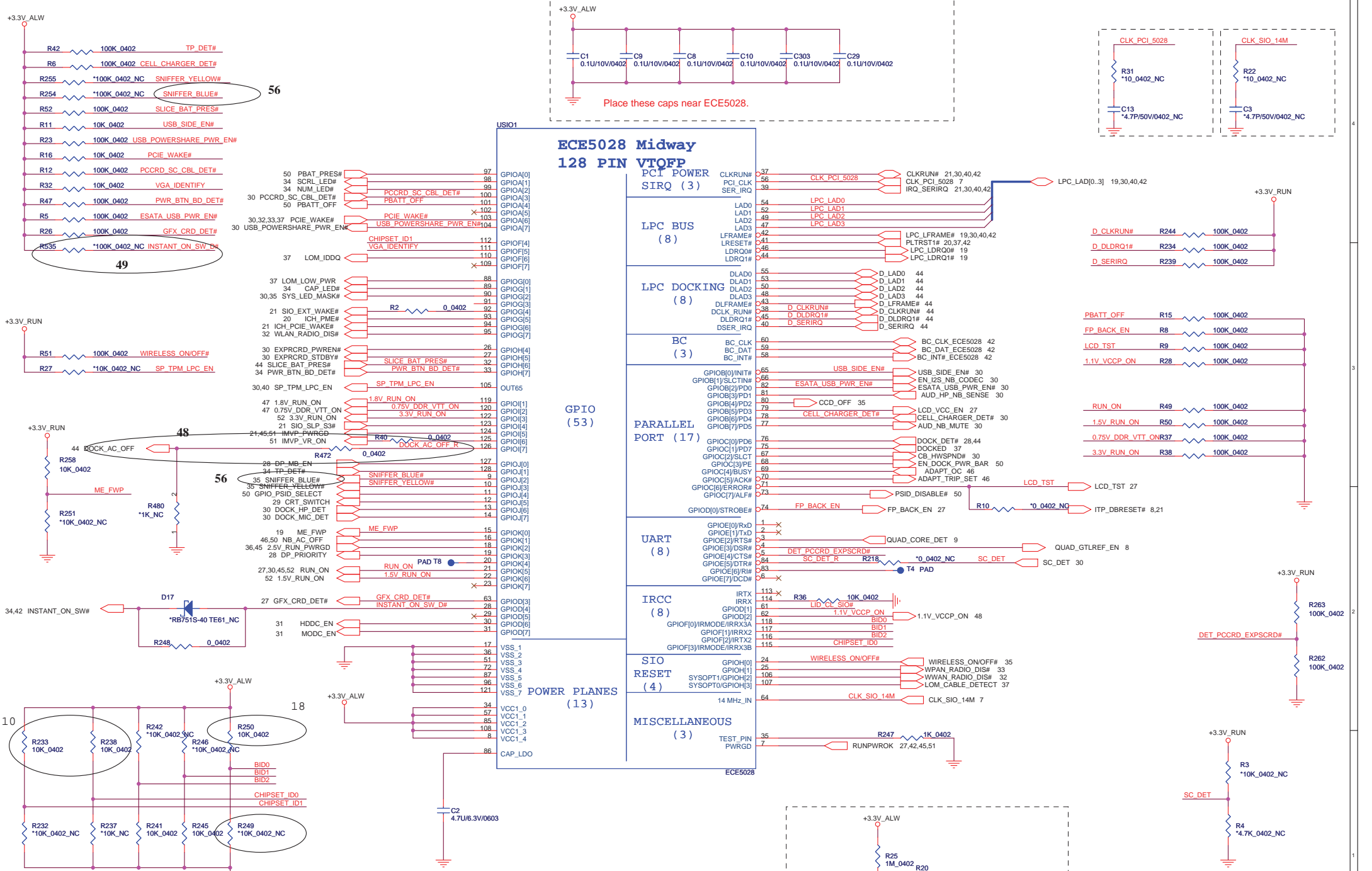


Min lengths of these nets to min stub lengths.

As close to MEC as possible.


Quanta Computer Inc.
 Project Name: **Nike** NB1

Title	SIO_5035	Rev	1A
Size	Document Number	?	
Custom			
Date:	Wednesday, March 19, 2008	Sheet	42 of 55



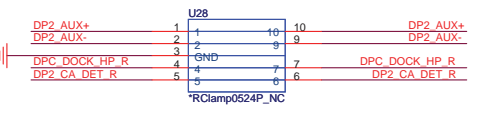
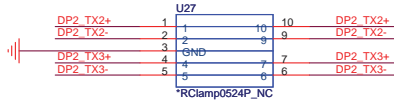
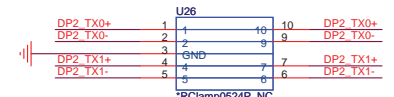
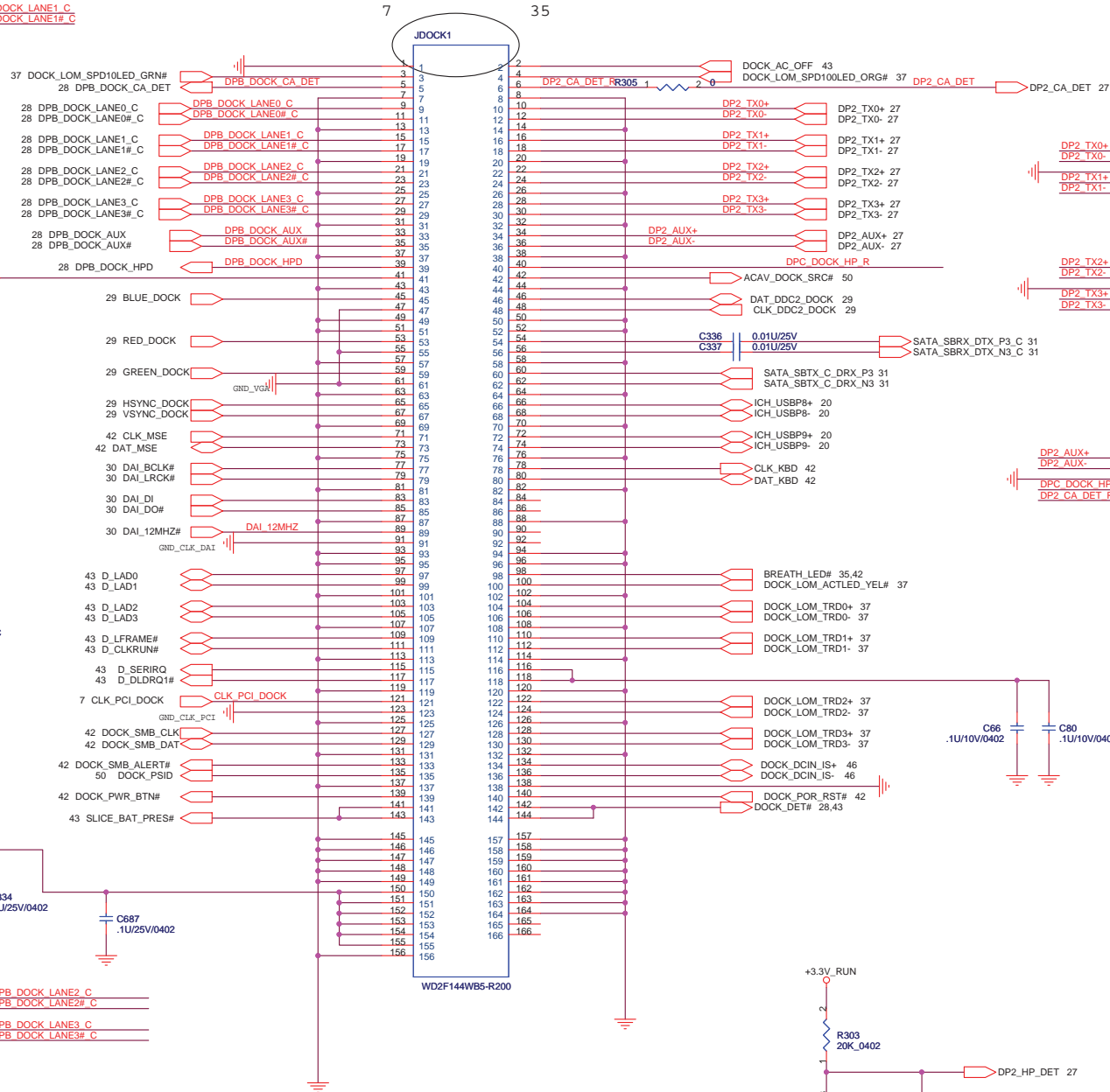
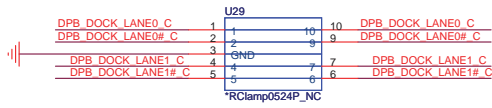
BID2	BID1	BID0	Board Revision
0	0	0	SST (X00)
0	0	1	PT (X01)
0	1	0	ST (X02)
0	0	0	QT (A00)
0	0	1	RAMP(A01)

CHIPSET ID0	CHIPSET ID1	Note
0	0	
1	1	Nike



Quanta Computer Inc.
Project Name: **Nike**

File: SIO_5028		NB1
Size: Custom	Document Number: ?	Rev: 1A
Date: Wednesday, March 19, 2008	Sheet: 43 of 55	

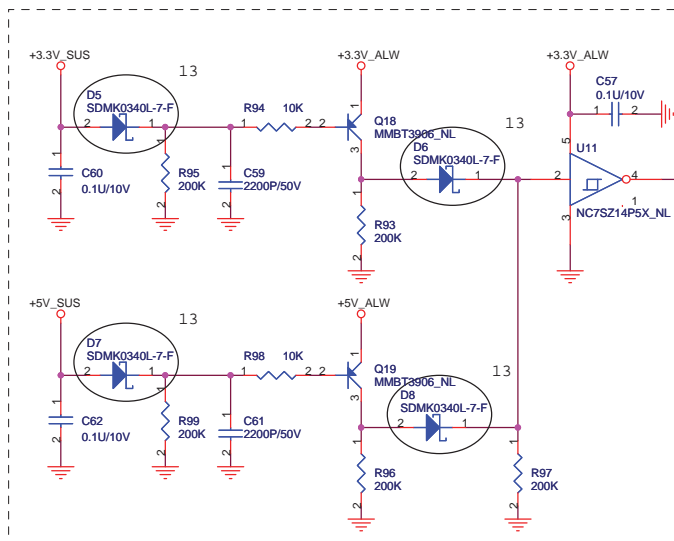
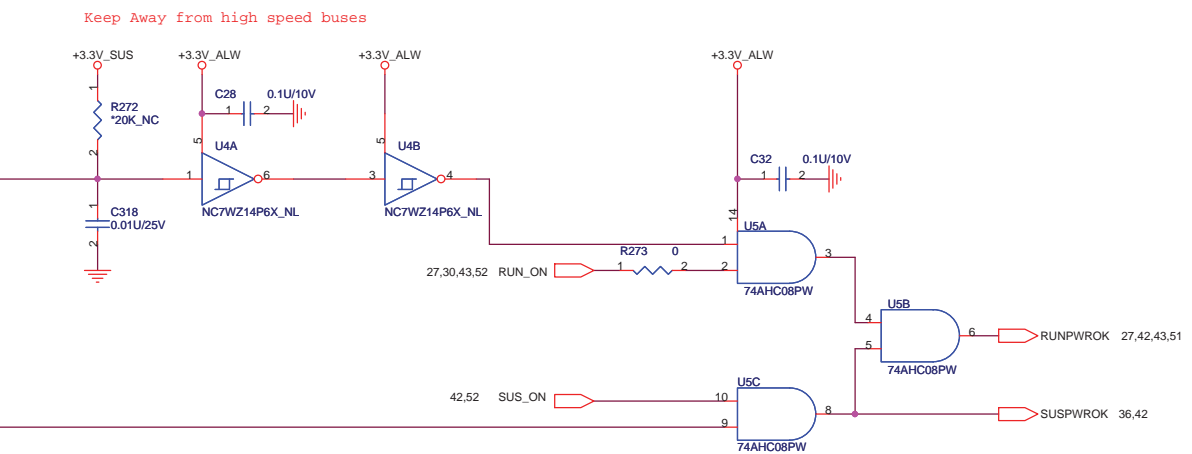
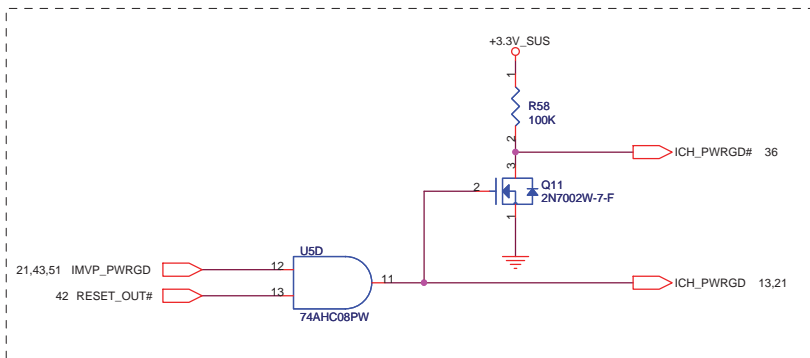
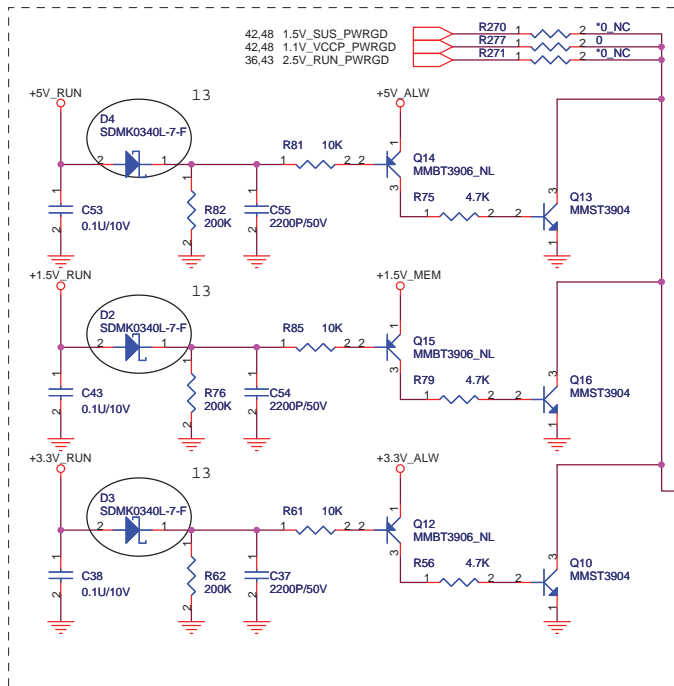


Quanta Computer Inc.
Project Name: Nike

File: E_DOCKING CONN

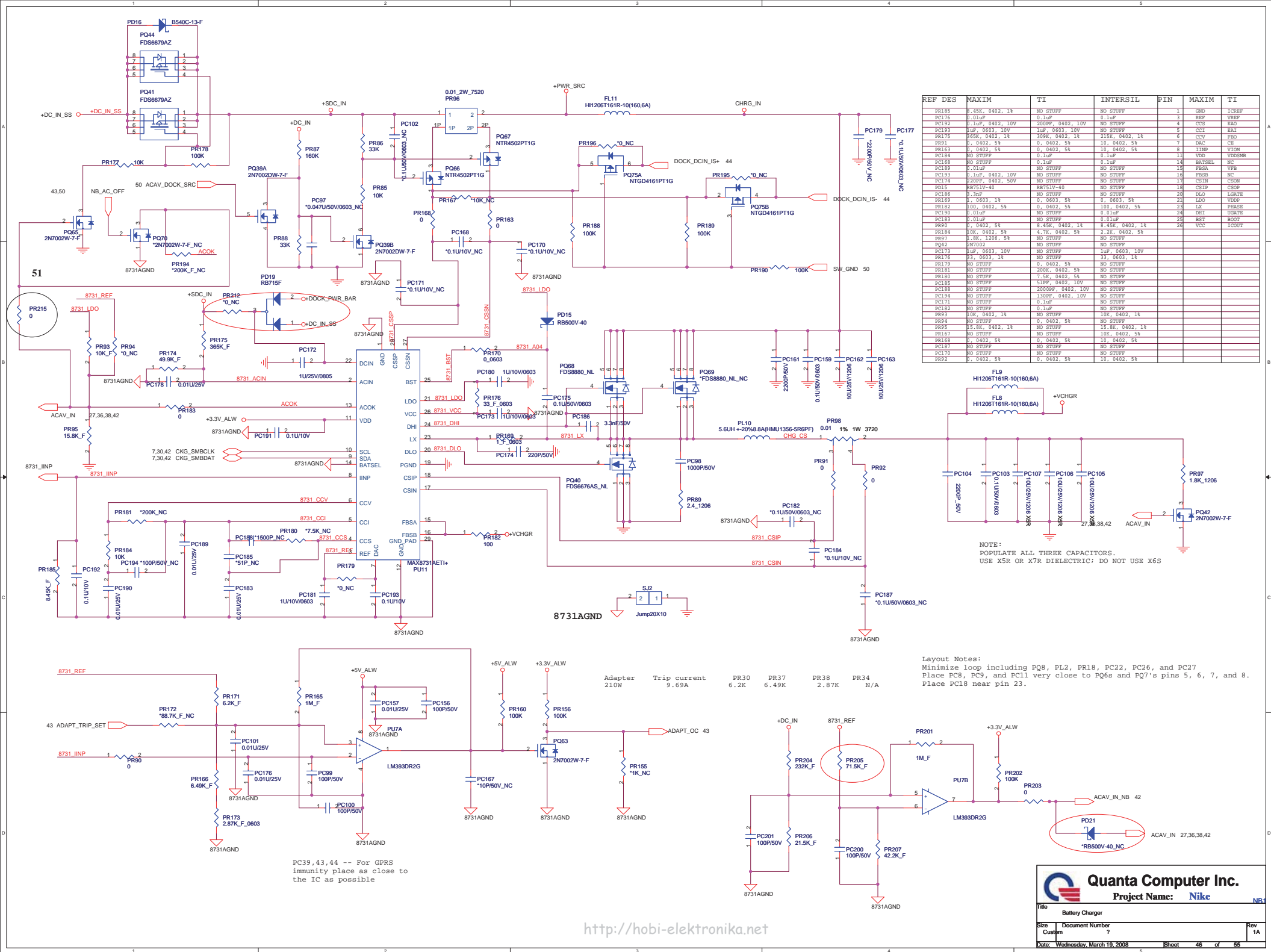
Size	Document Number	Rev
Custom	?	1A

Date: Wednesday, March 19, 2008 Sheet 44 of 55



Quanta Computer Inc.
 Project Name: **Nike**

Title		System Power Good
Size	Document Number	?
Custom		Rev 1A
Date: Wednesday, March 19, 2008	Sheet	45 of 55



REF	DES	MAXIM	TI	INTERSIL	PIN	MAXIM	TI
PR185	B	4.45K, 0402, 1%	NO STUFF		1	GND	ICREF
PC176	D	0.1uF	0.1uF		3	REF	VRFP
PC192	D	1uF, 0402, 10V	2000PF, 0402, 10V		4	CSS	BAQ
PC193	D	1uF, 0603, 10V	NO STUFF		5	CCI	BAI
PR175	B	85K, 0402, 1%	309K, 0402, 1%	215K, 0402, 1%	6	CCV	FBO
PR93	D	0.402, 5%	0.402, 5%	10.0402, 5%	7	DMC	CE
PR163	D	0.402, 5%	0.402, 5%	10.0402, 5%	8	IIND	VIOM
PC184	NO STUFF		0.1uF		11	VDD	VRSM8
PR95	B	0.402, 5%	NO STUFF		12	LDO	BATSEL
PC189	D	0.1uF	NO STUFF		13	FBSA	VFB
PC193	D	0.1uF, 0402, 10V	NO STUFF		16	FBSB	NC
PC174	D	220PF, 0402, 50V	NO STUFF		19	CSIN	CSIN
PR15	B	8B75V-40	NO STUFF		18	CSIP	CSOP
PC186	D	3.3nF	NO STUFF		20	DLO	LGAT8
PC183	D	0.0603, 1%	0.0603, 5%	0.0603, 5%	21	LDO	VDDP
PR182	D	100, 0402, 5%	0.402, 5%	100.0402, 5%	23	LX	PHASE
PC190	D	0.01uF	NO STUFF		24	DRI	DGATE
PR189	B	0.402, 5%	8.45K, 0402, 1%	8.45K, 0402, 1%	25	BOOT	BOOT
PR80	D	0.402, 5%	8.45K, 0402, 1%	8.45K, 0402, 1%	26	VCC	ICOUT
PR184	D	10K, 0402, 5%	4.7K, 0402, 5%	2.2K, 0402, 5%			
PR97	B	8K, 1206, 5%	NO STUFF				
PC42	B	2N7002	NO STUFF				
PC173	D	1uF, 0603, 10V	NO STUFF				
PR176	B	33, 0603, 1%	NO STUFF				
PR179	NO STUFF		0.402, 5%				
PR181	NO STUFF		200K, 0402, 5%				
PR180	NO STUFF		7.5K, 0402, 5%				
PC185	NO STUFF		51PF, 0402, 10V				
PC188	NO STUFF		2000PF, 0402, 10V				
PC194	NO STUFF		130PF, 0402, 10V				
PC171	NO STUFF		0.1uF				
PC182	NO STUFF		0.1uF				
PR93	B	0.402, 1%	NO STUFF				
PR94	NO STUFF		0.402, 5%				
PR95	B	15.8K, 0402, 1%	NO STUFF				
PR167	D	0.402, 5%	10.0402, 5%				
PR168	D	0.402, 5%	0.402, 5%				
PC187	NO STUFF		NO STUFF				
PC170	NO STUFF		NO STUFF				
PR92	D	0.402, 5%	0.402, 5%				

NOTE:
POPULATE ALL THREE CAPACITORS.
USE X5R OR X7R DIELECTRIC; DO NOT USE X6S

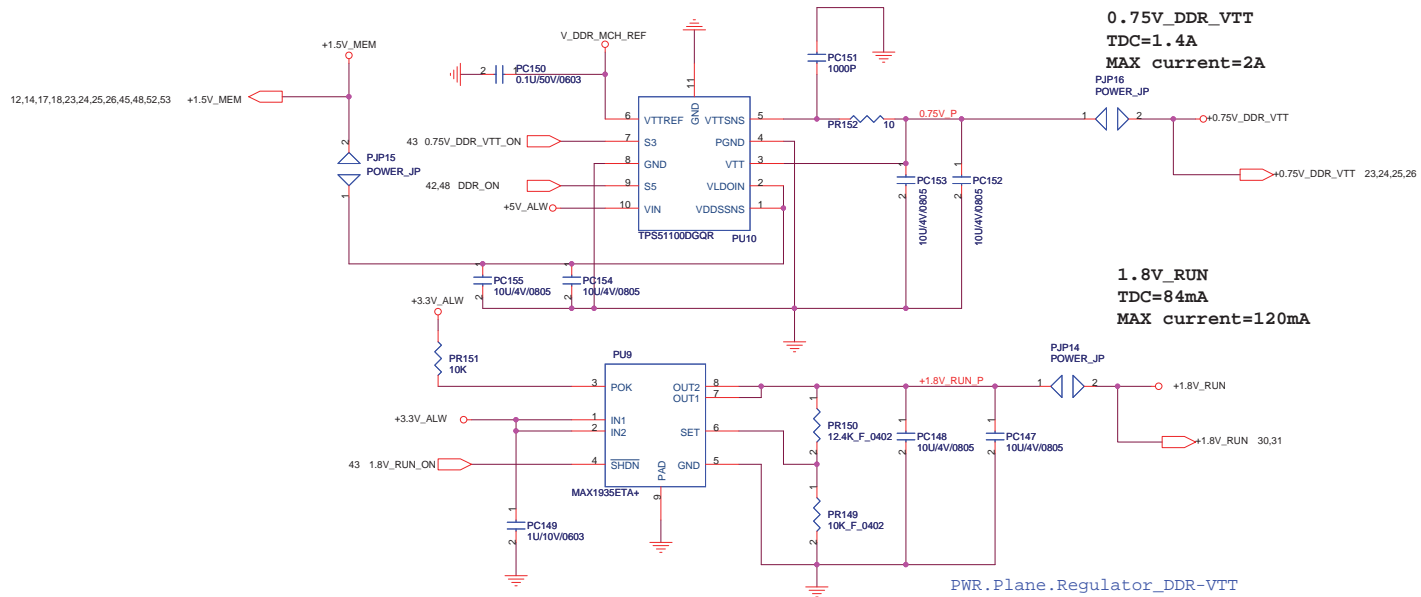
Layout Notes:
Minimize loop including PQ8, PL2, PR18, PC22, PC26, and PC27
Place PC8, PC9, and PC11 very close to PQ6 and PQ7's pins 5, 6, 7, and 8.
Place PC18 near pin 23.

Adapter	Trip current	PR30	PR37	PR38	PR34
210W	9.69A	6.2K	6.49K	2.87K	N/A

PC39,43,44 -- For GPRS
immunity place as close to
the IC as possible

Quanta Computer Inc.
Project Name: Nike

Title: Battery Charger
Size: Custom
Document Number: ?
Date: Wednesday, March 19, 2008
Sheet: 46 of 55
Rev: 1A

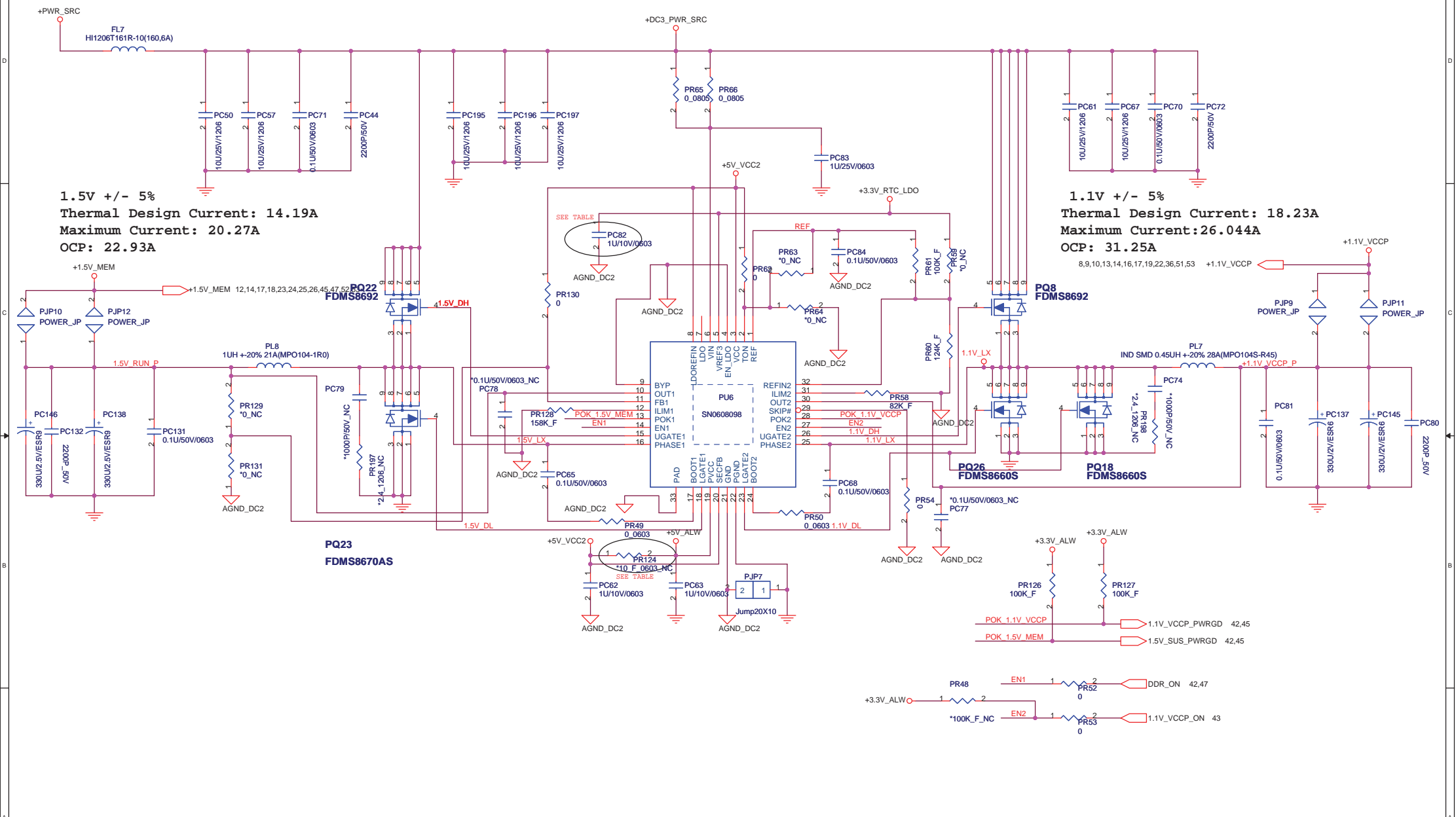


Quanta Computer Inc.
 Project Name: Nike

Title	<Title>	Rev	1A
Size	Document Number	?	
Date:	Wednesday, March 19, 2008	Sheet	47 of 55

M'09

+1.5V_MEM / +1.1V_VCCP / +3.3_RTC_LDO



1.5V +/- 5%
Thermal Design Current: 14.19A
Maximum Current: 20.27A
OCP: 22.93A

1.1V +/- 5%
Thermal Design Current: 18.23A
Maximum Current: 26.044A
OCP: 31.25A

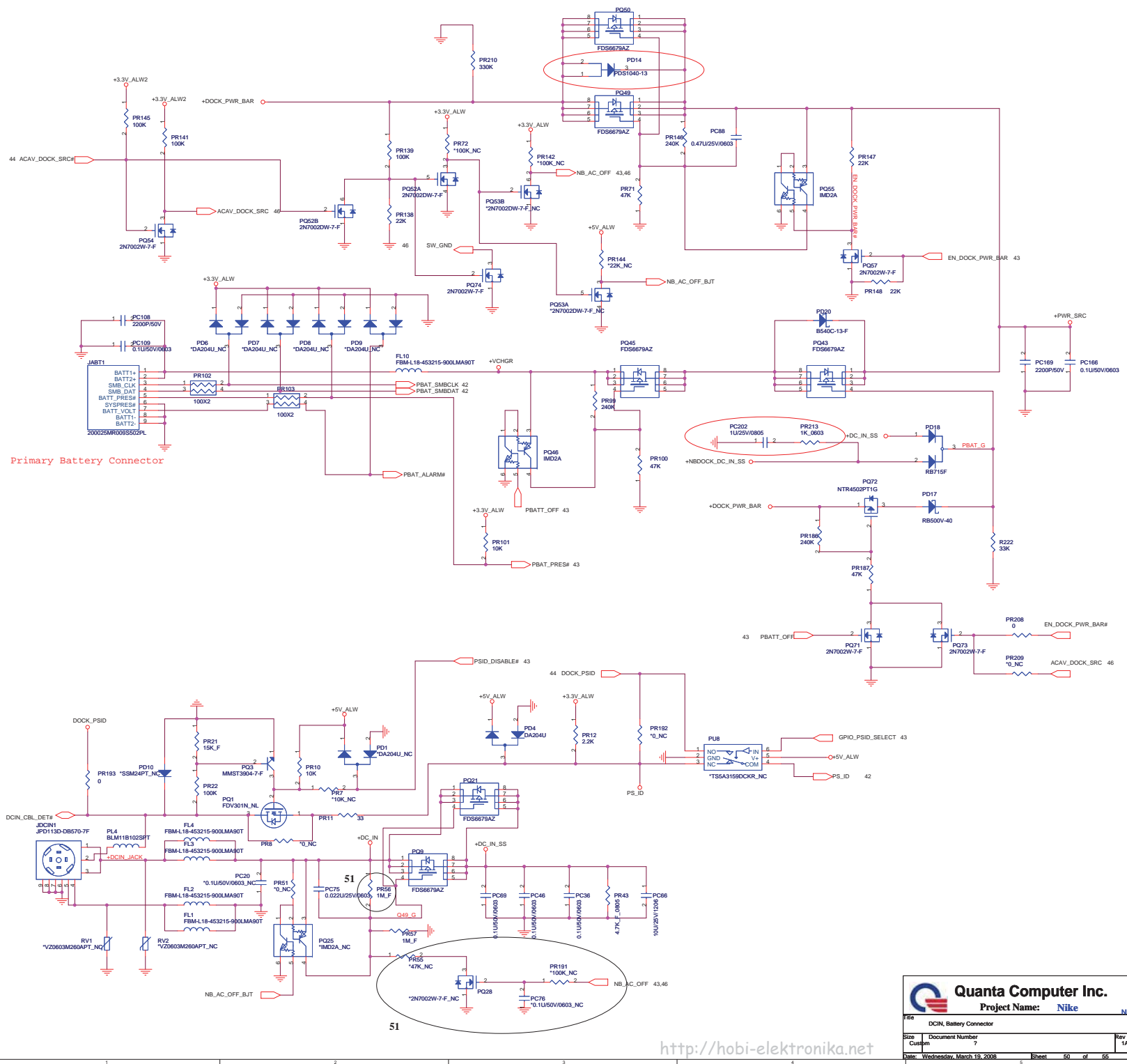
REF DESIGNATOR	MAXIM	INTERSIL	TI
PR56	10, 0603	NO STUFF	NO STUFF
PC61	1uF	0.1uF	1uF

Quanta Computer Inc.
Project Name: Nike

Title: 1.1V_VCCP and 1.5V_MEM

Size: Custom Document Number: ?

Date: Wednesday, March 19, 2008 Sheet 48 of 55

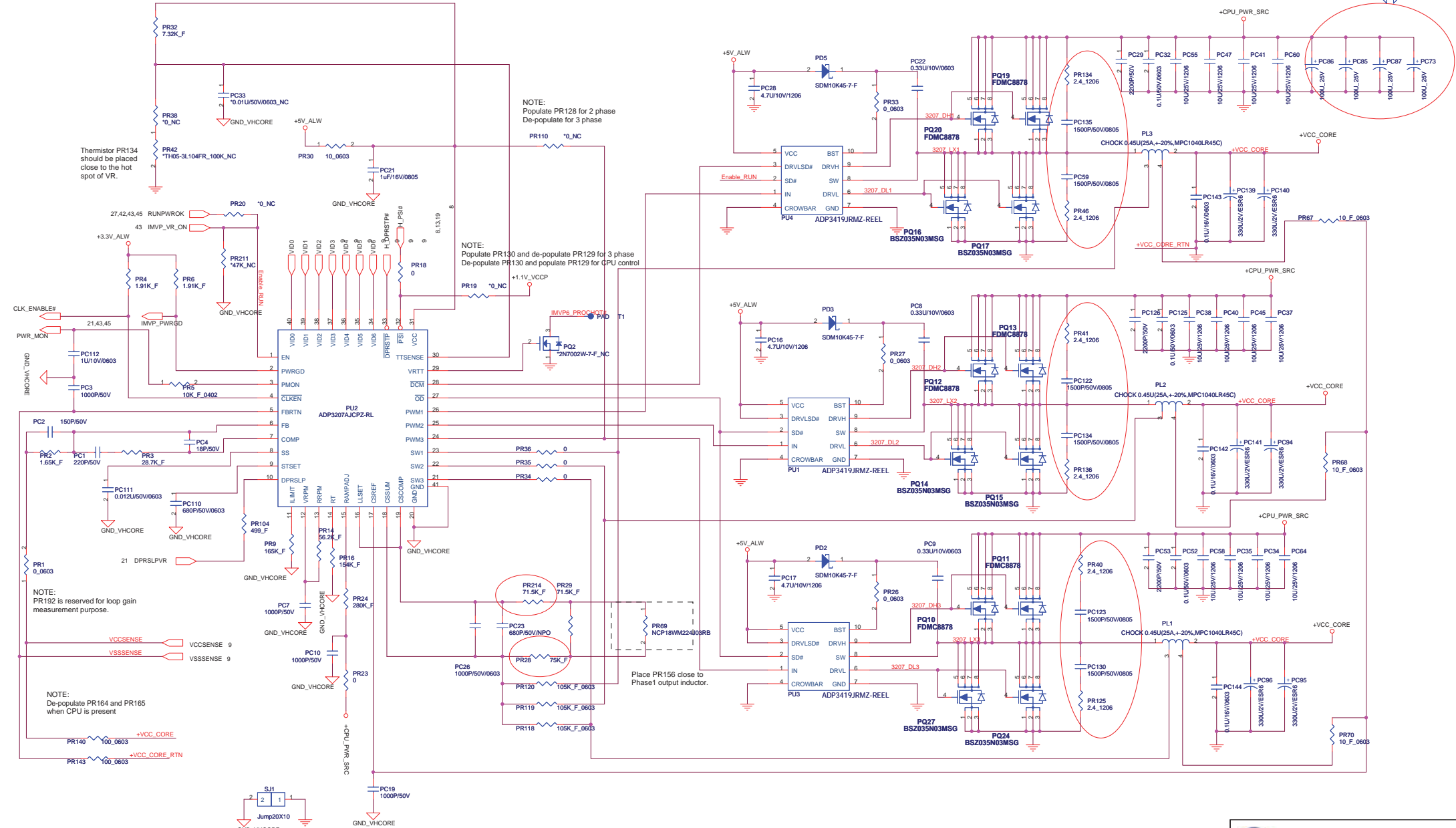
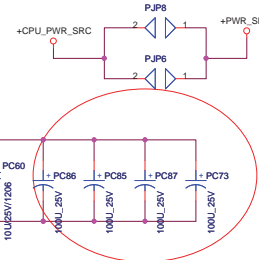


Primary Battery Connector

Quanta Computer Inc.
 Project Name: **Nike**

File	DCIN_Battery_Connector	Rev	7/A
Size	Document Number	Sheet	50 of 55
Date	Wednesday, March 18, 2008		

IMVP-6 solution for
 Penryn:
 Iccmax: 47A
 OCP: 56A, Intel spec: 50A



NOTE:
 Populate PR128 for 2 phase
 De-populate for 3 phase

NOTE:
 Populate PR130 and de-populate PR129 for 3 phase
 De-populate PR130 and populate PR129 for CPU control

NOTE:
 PR192 is reserved for loop gain
 measurement purpose.

NOTE:
 De-populate PR164 and PR165
 when CPU is present

Place PR156 close to
 Phase1 output inductor.

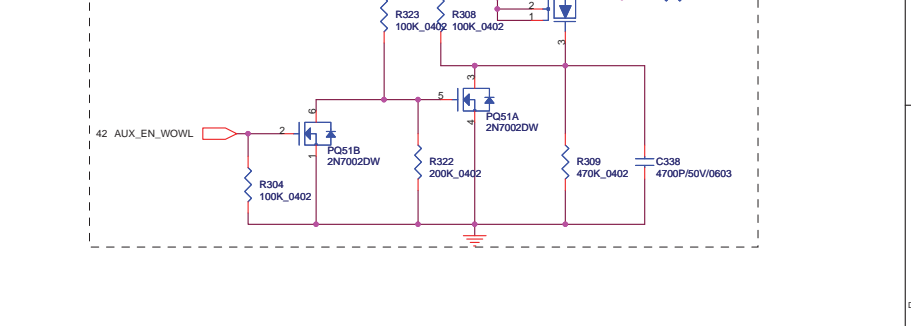
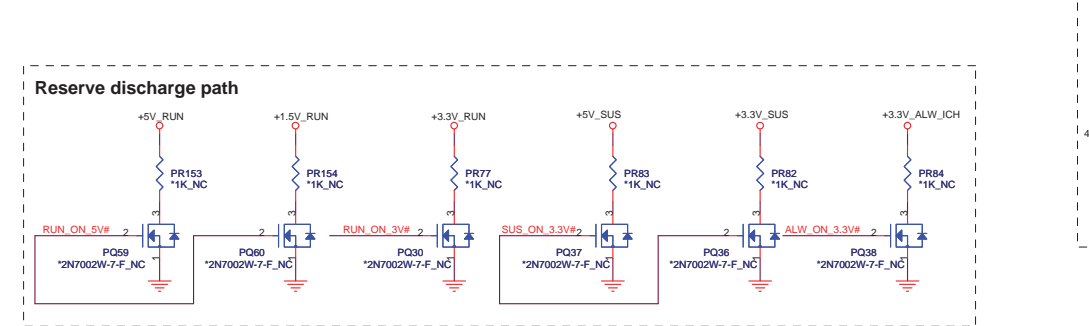
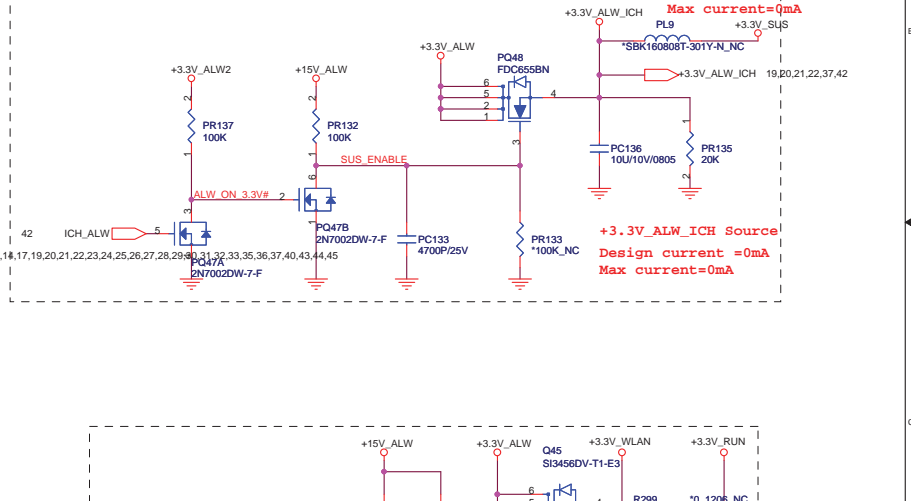
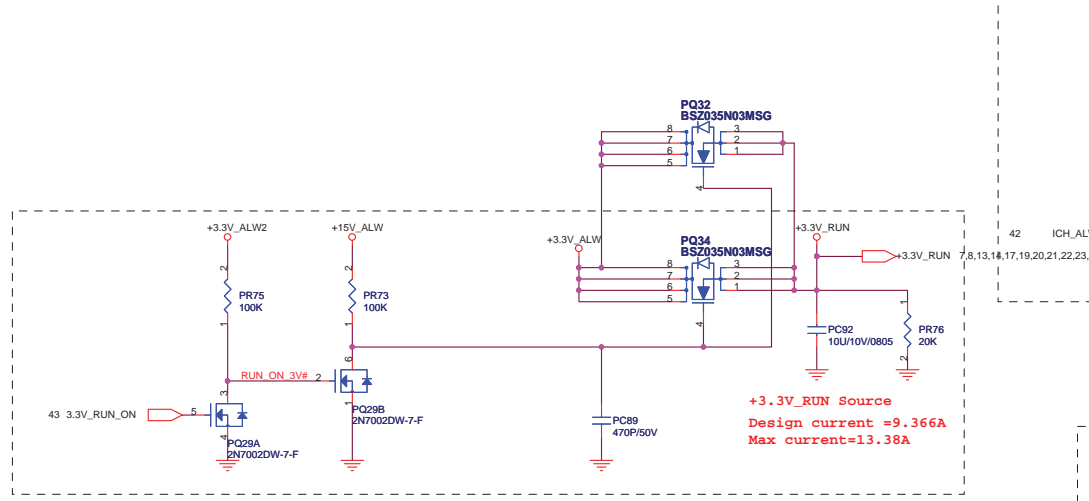
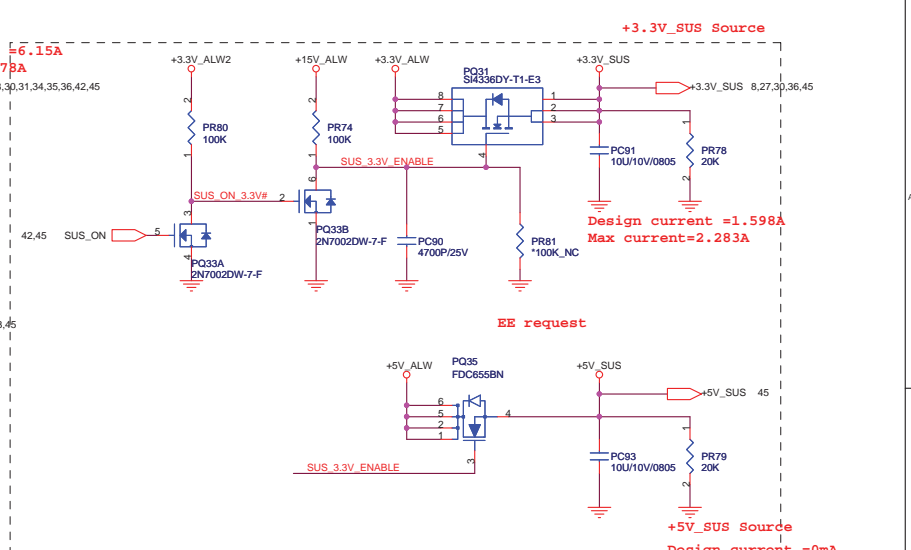
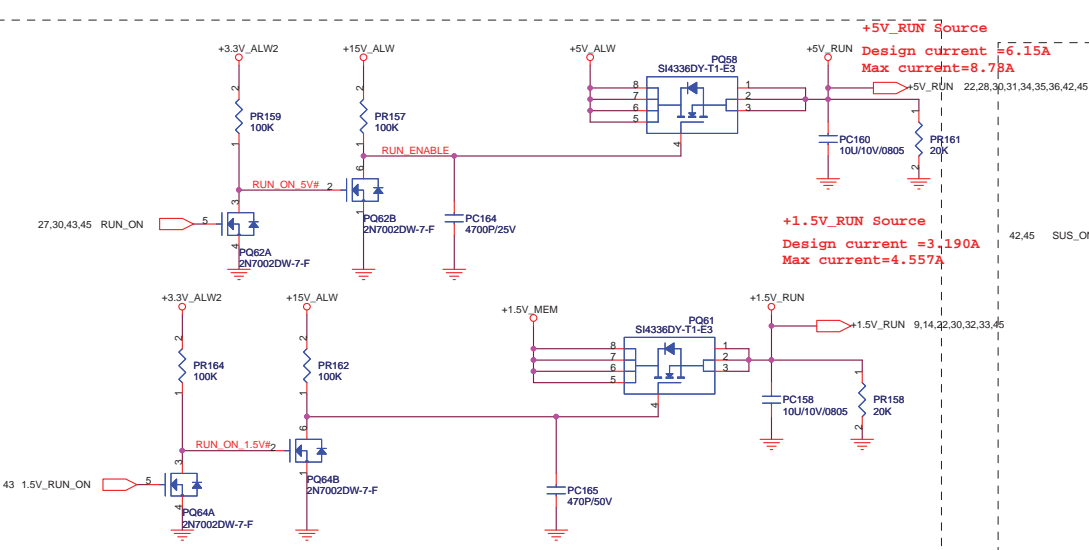
NOTE:
 ADP3207A: PR141=10K, PC1=1uF (Pin 3 output Power Signal)
 ADP3207: PR141=0, PC1=4.7nF (Pin 3 programs PWRGD Delay)

Quanta Computer Inc.
 Project Name: Nike

File: CPU_VCORE (ADP3207A)

Size: Custom Document Number: 7 Rev: 1A

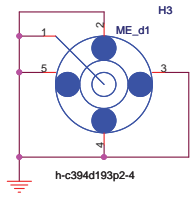
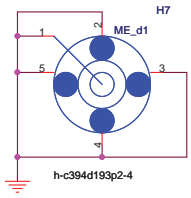
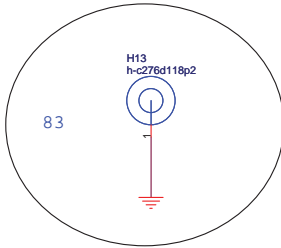
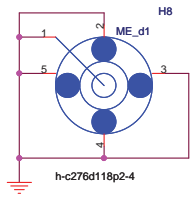
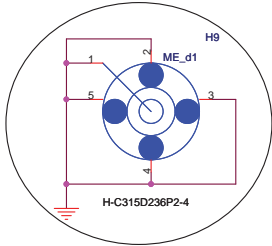
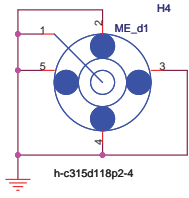
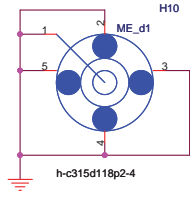
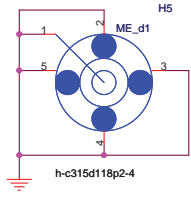
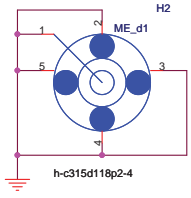
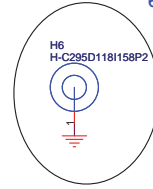
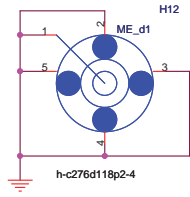
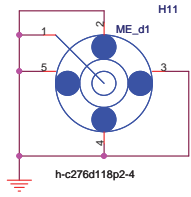
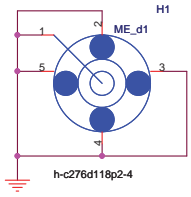
Date: Wednesday, March 16, 2008 Sheet: 51 of 55



Quanta Computer Inc. Project Name: Nike		Title Power Misc
Date: Wednesday, March 19, 2008		Document Number ?
Sheet 52 of 55		Rev 1A

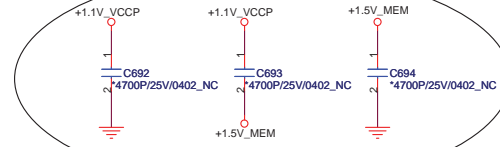
15

66



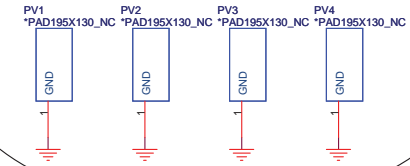
Stitching caps

54



EMI Clips


54



Quanta Computer Inc.
 Project Name: **Nike** NB1

Title	Screw hole		
Size	Custom	Document Number	?
Date	Wednesday, March 19, 2008	Sheet	53 of 55
Rev	1A		

Model	Item	Page	Date	Rev.	Description
XM1 MB	1	37~39	0124	X01	LOM need to use A2 version, update U31 QCI PN from AJ057610T00 to AJ057610T01
	2	34	0128	X01	Change the net name of SCRL from SCRL_LED# to SCRL_LED#_R.
	3	35	0128	X01	For X00 issue pop U33.
	4				Blank.
	5	40	0131	X01	Per p40 table 1: using USH B0 as default.
	6	38	0131	X01	Verify A2 version, adding a 0 ohm (nonpop) resistor between ACAV_IN and pin A11.
	7	44	0131	X01	Per Keivn's mail, change QCI PN from DFHSE4FS000 to DFHSE4FS001.
	8	35	0201	X01	Per WI 167200: Update the last row of the LED Mask Table on pg 35, It should be "Do Not Mask LEDs (Lid Open)" instead of "Mask Base LEDs (Lid Open)
	9	33	0201	X01	Per WI 167193: We should not require C302 (330uF) for Robson.
	10	43	0204	X01	Adding QCI PN at R233 and R238.
	11	31	0213	X01	Switching SATA channels for primary and secondary HDD
	12	31	0218	X01	CON2 comment should be "SATA (HDD0) Connector - front" JSATA1 comment should be "SATA (HDD1) Connector - side" Please fix nets after DC blocking caps to match channel For instance, Change SATA_RXN0_C to ATA_RXN4_C, etc.
	13	22,32,41,45	0213	X01	BC000751Z05 is not a PSL part. change to BC000340033.(Location: D1,D2,D3,D4,D5,D6,D7,D8,D9,D12).
	14	40	0304	X01	Per WI SCH168652. Update the tables on MB pg 40.
	15	34	0304	X01	Because TP pullup is ALW plane. change power plane from 5v_run to 3.3v_alw.
	16	38	0304	X01	For solving Broadcom issue.
	17	42	0304	X01	Change RC_ID pull-up (R283) to 130K for X01 Gerber
	18	43	0304	X01	Update board ID for PT build.
	19	07	0304	X01	Per crystal test report, C103; C110 27pF ---> 33pF. R345 from 200 to 680.
	20	46	0304	X01	PR205 change from 47K_F to 71.5K_F Add PD19 and PR212 to reduce charger leadage current in S5 on batt. Add PD21 connect to ACAV_IN net
	21	50	0304	X01	Add PC202 (1U_0805) and PR213 (1K_0603) PD14 change from B540C-13-F to PDS1040-13
	22	51	0304	X01	PR134, PC135, PC59, PR46, PR41, PC122, PC134, PR136, PR40, PC123, PC130, PR125 are stuff to slove EMI.
	23	35	0306	X01	Swap L10 pin 2,3 and pin 1,4 for trace routing smoothly.
	24	36	0306	X01	Change U34 footprint from "qfn48-7x7-5-57p-emc4002 to QFN48-7X7-5-49P-EMC4002 for trace rotuing."
	25	19	0306	X01	Change Test Pad footprint from TP3075 to TP3050 to improve test pad coverage rate
	26	35	0306	X01	Per WI:EMI_Change R194 value from 0 ohm resistor to 120 ohm bead
	27	35	0307	X01	CCD module power rail is supported by 3.3V.
	28	34	0307	X01	For solving lid sw can't wake up issue. change JTP1 pin 8 from 3.3v_RUN to 3.3V_ALW.
	29	37	0307	X01	Per WI 168833, DF201715, for backdrive issue, wake on LAN S4,S5.
	30	18	0307	X01	Per SCH168949, DDR3_DRAM_PWROK Glitch issue.
	31	42	0307	X01	For ALS issue, pull high resistors on ALS_SMBDAT and ALS_SMBCLK.
	32	42	0310	X01	Per WI, R500 need to depop.
	33	35	0310	X01	Per WI SCH168289, WLAN,WWAN,WPAN and HDD circuit need to modify
	34	42	0311	X01	Change ALS_SMBDAT/CLK to connect LCD_SMBDAT/CLK
	35	44	0311	X01	Per Keivn's mail, change QCI PN from DFHSE4FS001 to DFHSE4FS004.
	36	51	0313	X01	PR28 change from 147K to 75K and add PR214(71.5K) to slove thermal compensation.
	37	51	0313	X01	MB and IOR: Define a pin to carry +3.3V_ALW2 to the IOR MB: R281 = 200K MB: Add an RB751S40 Schottky Diode to clamp the voltage spike to +RTC_CELL +RTC_CELL




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Project Name: ?

Title: ?

Size: Custom Document Number: ? Rev: ?

Date: Wednesday, March 19, 2008 Sheet: 54 of 55

Model	Item	Page	Date	Rev.	Description
XM1 MB	38	32,33	0313	X01	MPCI socket needs to change source priority from Molex to Tyco. Molex has quality issue of solder tails coplanarity and that will impact to SMT performance.
	39	42	0314	X01	Depop J9 and J13 debug connectors from M/B.
	40	36	0314	X01	Remove U34 pin 50~57 for layout symbol change.
	41	19,31	0314	X01	Change C470~C473, C466~C469, C663~C664, C682,C683,C255 and C256 from 3900pf to 0.01uf per Intel schematics.
	42	36, 8	0314	X01	Del C617, R472, R480. Add Q68, C695 for New thermal sensor locations from thermal team.
	43	32	0315	X01	Populate R240 on WIMAX_LED signal for WiMAX LED support & test.
	44	21,42	0315	X01	Work Item SCH169422: X01: MB : Change PORT_SELECT to MEC GPIO per BIOS request
	45	35	0315	X01	Work Item SCH169263: X01: MB: No-pop duplicate pull-up on Sniffer_Pwr_Sw# and Wireless_On/Off#
	47	36	0315	X01	Work Item SCH169379: X01: MB : Add a 10K pull-down option on LDO_SHDN# (EMC4002)
	48	43	0315	X01	SCH169440: X01: MB : Add pull-down option on DOCK_AC_OFF
	49	43	0315	X01	SCH169374: X01: MB : Instant_On_Sw# has duplicate pull-up's to +3.3V_ALW
	50	43	0315	X01	SCH169439: X01 : MB : Change ALS SMBus circuit
	51	46	0315	X01	X01: MB : Power circuit changes
	52	28,44	0315	X01	SCH169313: EMI - Aligning w/Roush for DP Enhanced ESD Issue
	53	8	0315	X01	SCH169312: Aligning w/Roush on Enhanced ESD Issues w/E-Dock
	54	9	0315	X01	SCH169254: Changes for QC CPU support
	55	9	0315	X01	EEFCX0D271R (CH727RM8810) to replace EEFUE0D271R (CH7270LM885 => EOL)
	56	35,43	0315	X01	SCH169326: X01: MB, IOR: Change to the Sniffer LED net name & power rails.
	57	8,9	0318	X01	Update CPU socket PN from DGG^9000001 to DGG^9000002.
	58	51	0318	X01	PC85~PC87, PC73 change to stuff.
	59		0318	X01	U9,U25,U33,U24 need change to AL1G0008039
60	37~39	0319	X01	Del test pad T56, T62, T69, T75, T80, T83 per DFx request for LOM chip.	
61	35,42	0319	X01	Swap pin 1& pin 2 net for AND gate logic change to "H" type (Not HC)	



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Title: <Title>

Size: Custom Document Number: ? Rev: ?

Date: Wednesday, March 19, 2008 Sheet: 55 of 55