

IM3 (Jolie) Discrete 256M & UMA Block Diagram

VER : 3A

POWER

AC/BATT CONNECTOR PG 55

BATT CHARGER PG 48

HybridSLI POWER

VGA Core
+1.1V_GFX PG 53

REGULATOR For GDDR3
+1.8V_RUN PG 50

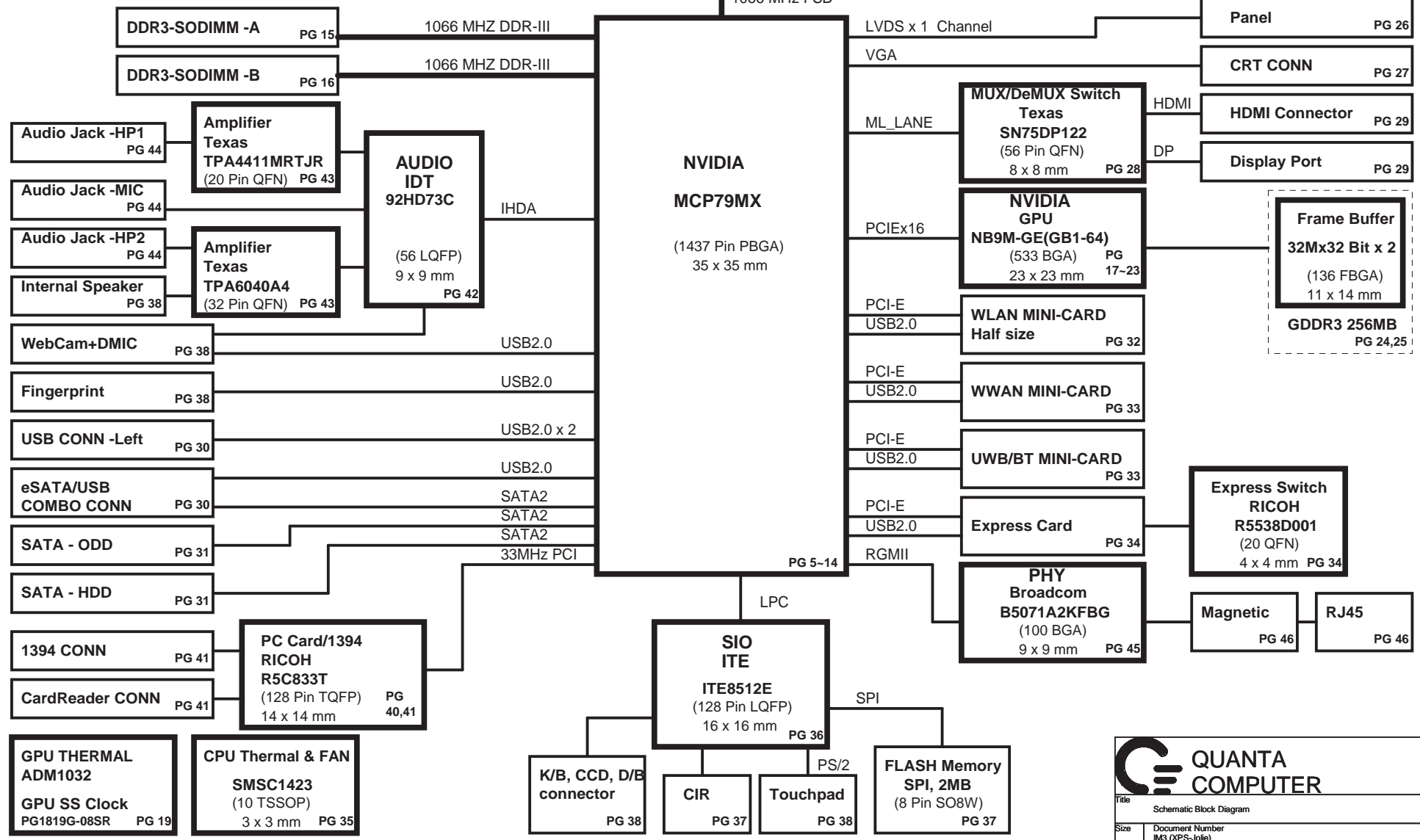
HybridSLI SW
+3.3V_NB9X/+1.8V_FBVDDQ/
+1.1V_GFX_PCIE PG 23

Dual Core CPU Intel Penryn (25W)

(478 Micro-FCPGA)
35 x 35 mm PG 3,4

SYSTEM POWER

MCP VR +MCP_CORE PG 50	CPU VR +VCC_CORE/ +1.05V_VCCP PG 49,54
REGULATOR For DDR3 +1.5V_DDR/ +0.75V_DDR_VTT PG 51	REGULATOR +3.3V_ALW/+5V_SRC/ +15V_ALW PG 52
RUN/SUS POWER SW +5V/+3.3V/+1.5V_RUN +3.3V_SUS PG 56	LDO +1.1V_SUS PG 53
	LDO +1.1V_RUN PG 51



QUANTA COMPUTER

Title: Schematic Block Diagram

Size: Document Number IM3 (XPS-Jolie) Rev 2A


Date: Thursday, October 23, 2008 Sheet 1 of 59

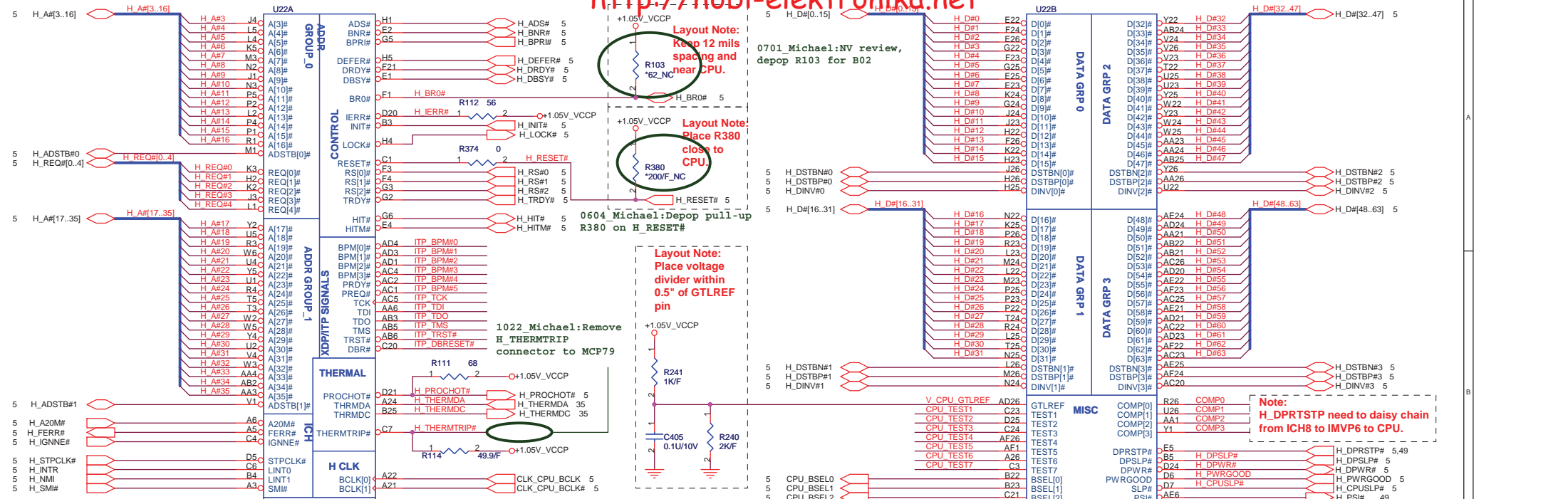
INDEX

Page#	Description
1	Block Diagram
2	Front Page
3-4	Penryn (CPU)
5-14	MCP79 (NB+SB+CKG)
15-16	DDRIII SO-DIMM(204P)
17-25	VGA (NB9M)
26	LCD CONN
27	CRT CONN
28	DeMux SW (SN75DP122)
29	HDMI & DP CONN
30	USB & eSATA & TV
31	HDD & ODD (SATA)
32	MINI-CARD (WLAN)
33	MINI-CARD (WPAN,WWAN)
34	Express Card
35	FAN & Thermal
36	SIO (ITE8512)
37	Flash ROM/ RTC/ CIR
38	KB/ CCD/ User Interface
39	LED
40-41	Card Reader & 1394
42-43	Audio CODEC(92HD73C)/ AMP/ Jack/ Subwoofer
45-46	LAN PHY (B5071)/ RJ45/ Transformer
47	System Reset Circuit
48	CHARGER (MAX8731)
49	CPU Core (ISL6266)
50	MCP79 CORE/ 1.05V (MAX17007)
51	DDR 1.5V/ 1.1V (TPS51116)
52	SYS 5V/ 3V(MAX17020)
53	NB9 Core (MAX8632)
54	GRAM_1.8V (TPS51117)
55	DCIN,Batt
56	RUN POWER SW
57	Debug Port (Mini PCI)
58	PAD & SCREW

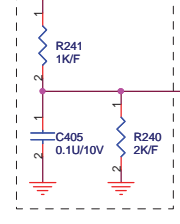
Power States

Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDDC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			

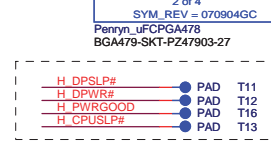
 QUANTA COMPUTER		
Title Index & Power Status		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 2 of 59



Layout Note: Place voltage divider within 0.5" of GTLREF pin



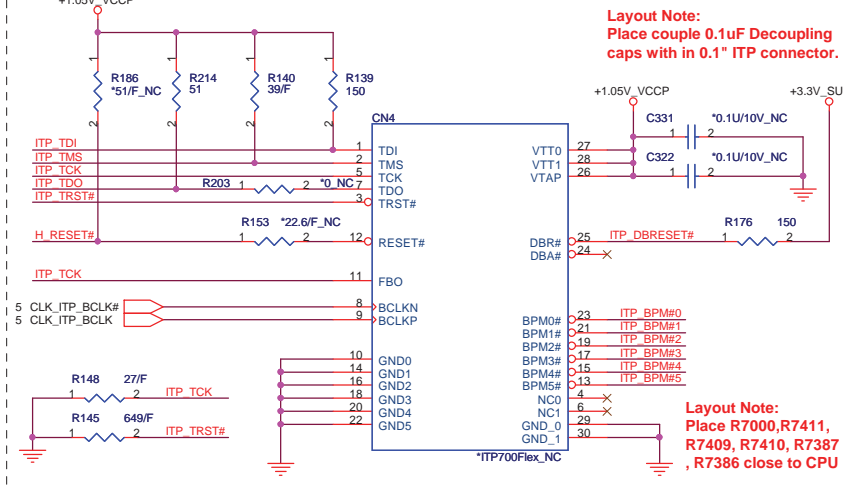
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0



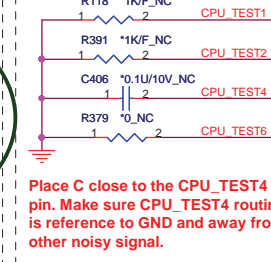
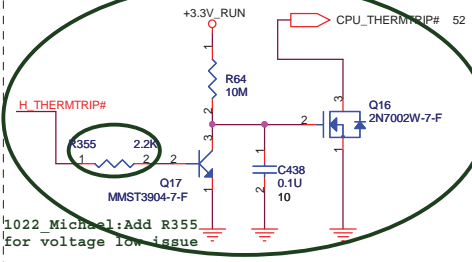
Note: H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Populate ITP700Flex for bringup



CPU THERMTRIP Circuit

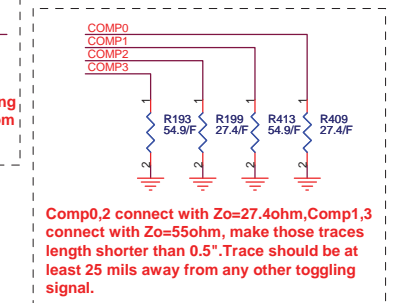


Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

0823_Michael: Follow RM2 to change CPU THERMTRIP circuit

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8



Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

QUANTA COMPUTER

Penryn Processor (HOST BUS)

Penryn uFCPGA478 BGA479-SKT-PZ47903-27

SYM_REV = 070904GC

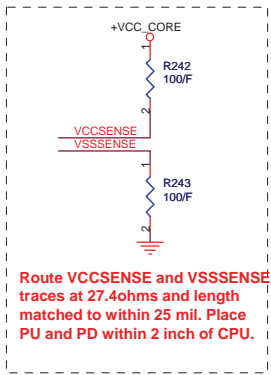
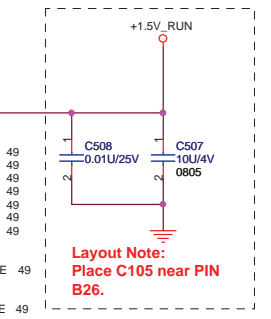
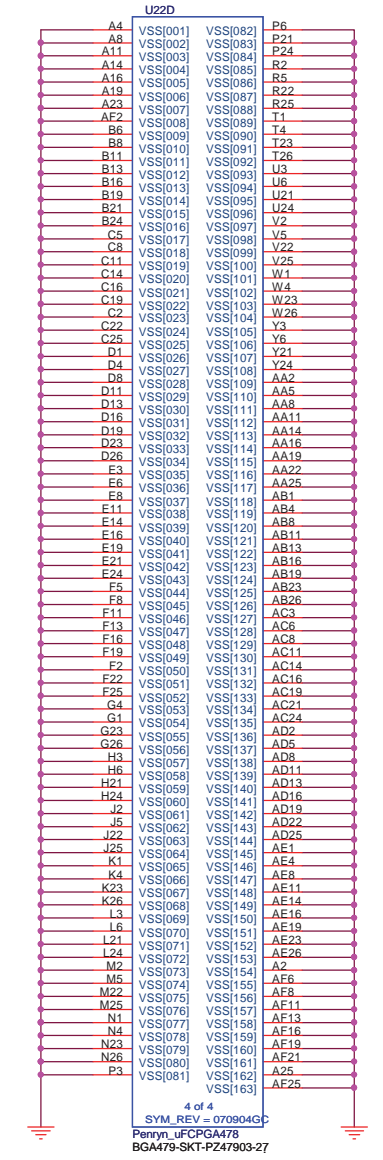
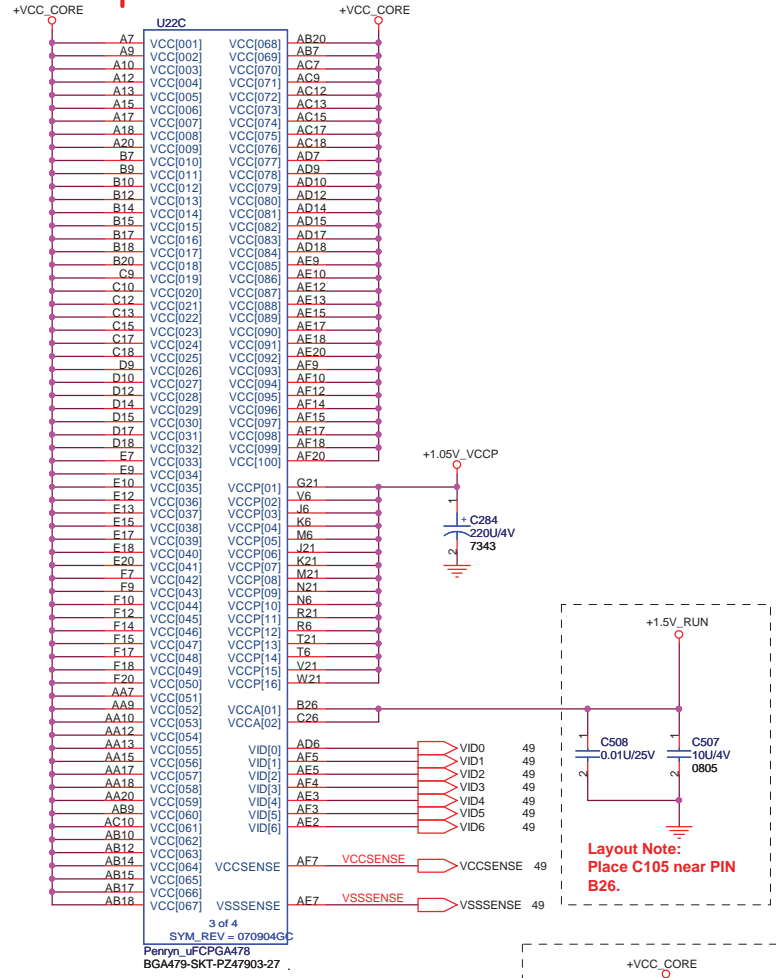
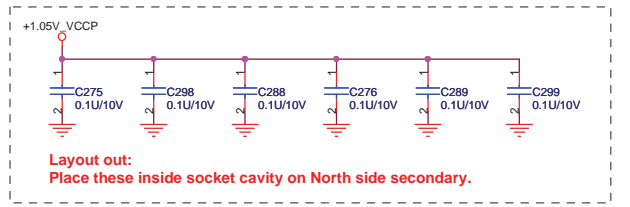
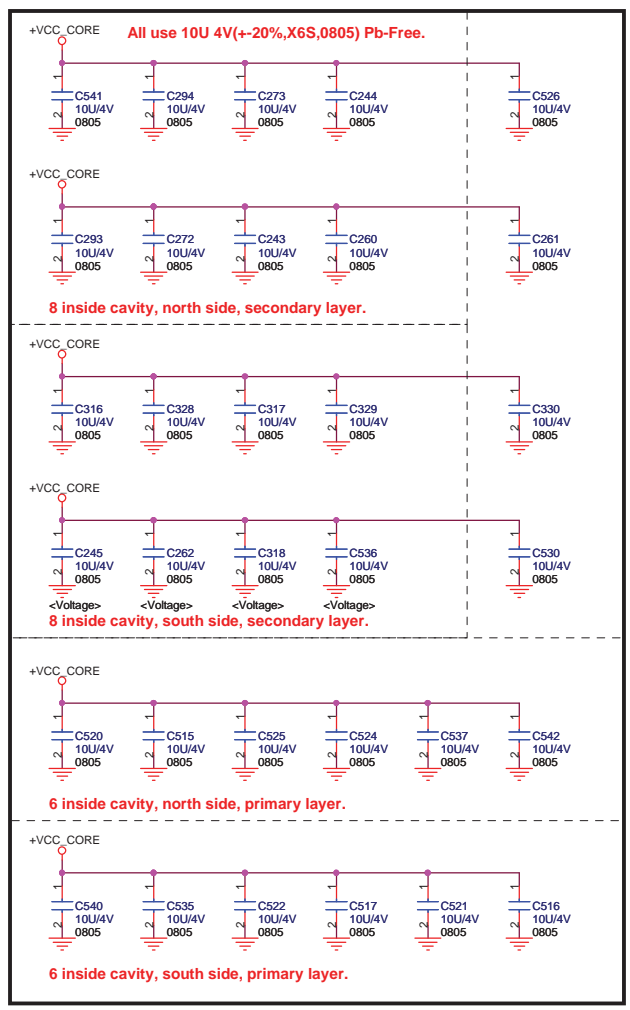
1 of 4 p479

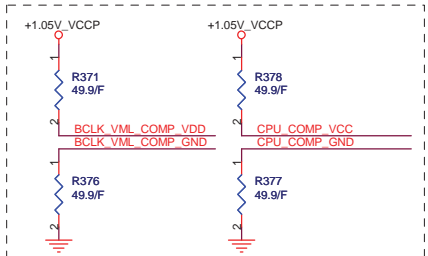
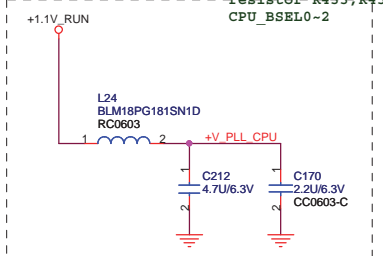
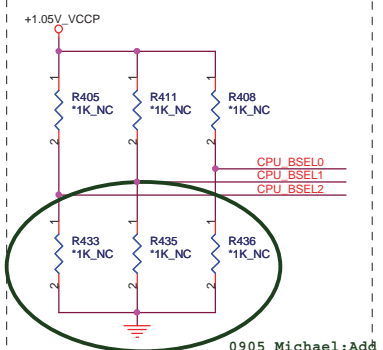
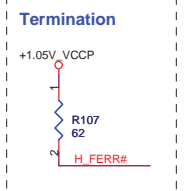
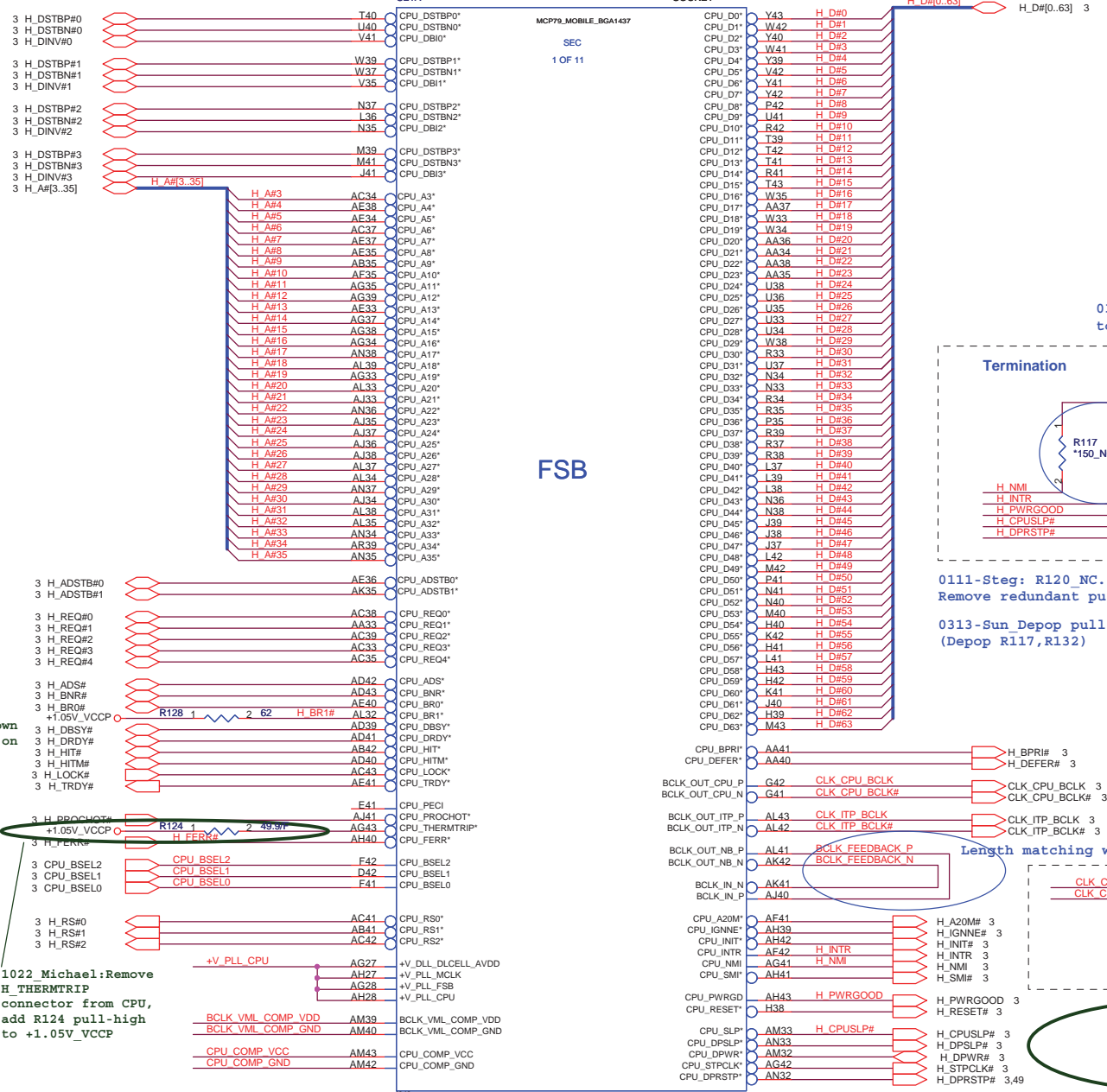
SYM_REV = 070904GC

Penryn uFCPGA478 BGA479-SKT-PZ47903-27

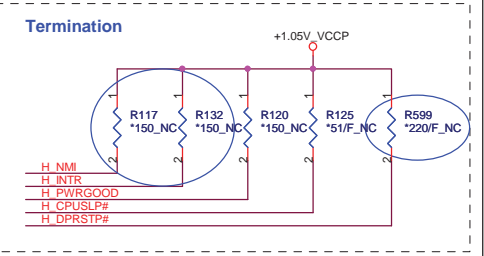
Size	Document Number	Rev
	IM3 (XPS-Jolie)	2A

Date: Thursday, October 23, 2008 Sheet 3 of 59



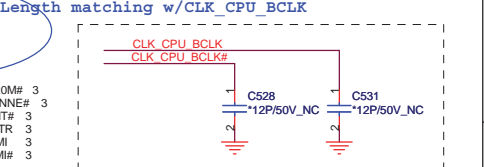


+V_DLL_DLCELL_AVDD 150mA with RUN rail	+V_PLL_MCLK 20mA with RUN rail	+V_PLL_FSB 29mA with RUN rail	+V_PLL_CPU 15mA with RUN rail
1 x ferrite bead	1 x ferrite bead	1 x ferrite bead	1 x ferrite bead
1 x 4.7uF X5R ceramic	1 x 1uF X5R ceramic	1 x 4.7uF X5R ceramic	1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic



0111-Steg: R120_NC. Remove redundant pull-up R120 on H_PWRGOOD

0313-Sun Depop pull-up on H_NMI & H_INTR. (Depop R117, R132)



0605 Michael: NV review, remove pull-down C509 on CLK_ITP_BCLK & C510 on CLK_ITP_BCLK#

QUANTA COMPUTER

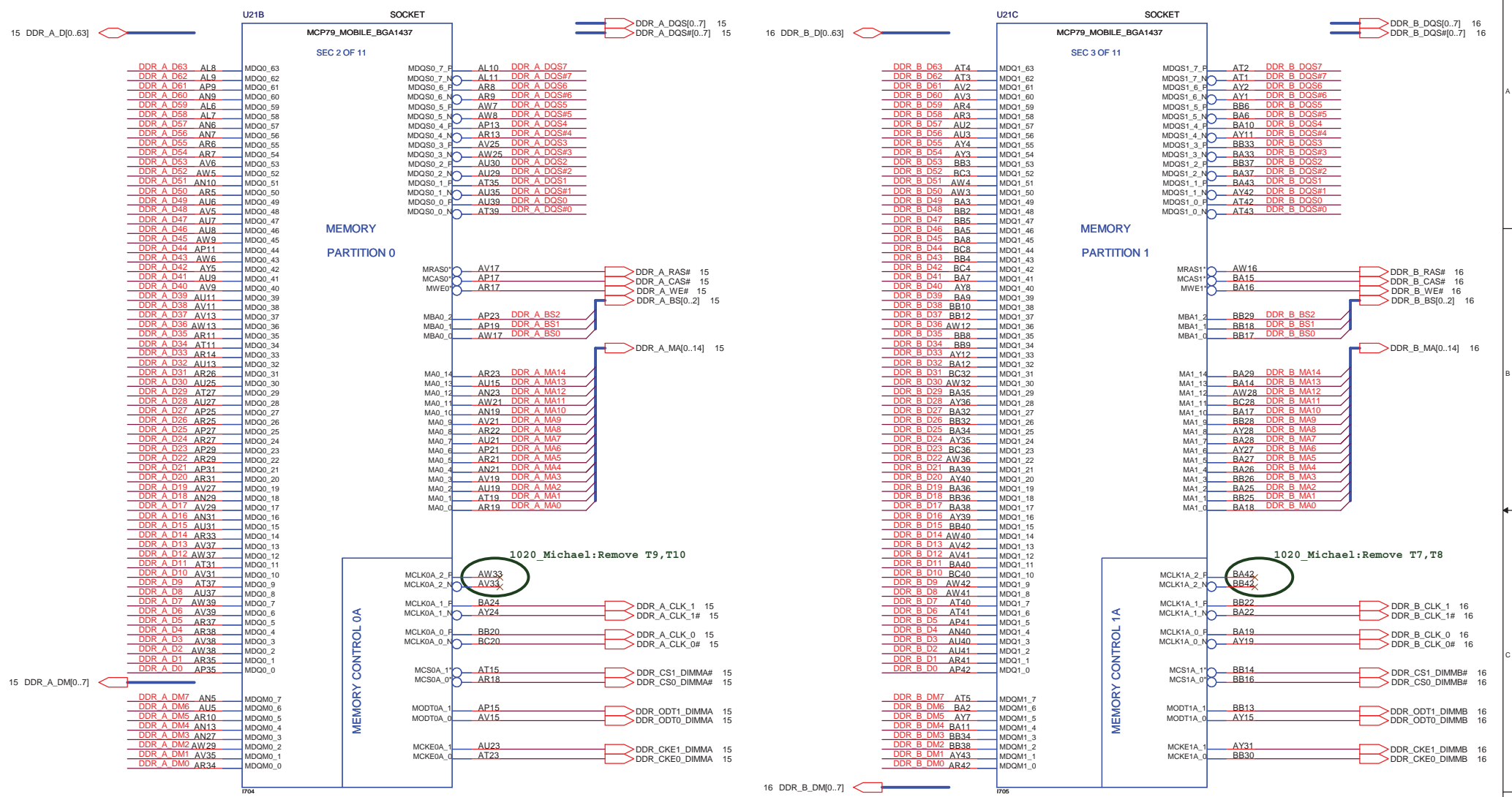
Title: MCP79 (HOST)

Size: Document Number IM3 (XPS-Jolie)

Date: Thursday, October 23, 2008

Sheet: 5 of 59

Rev: 2A



Layout Notice:
Memory Data Signal Group
MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

Memory Data Strobes
Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

Memory Clock Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.
After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

Memory Address/Command/Control Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

QUANTA COMPUTER

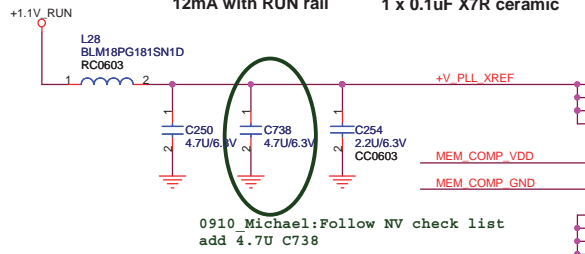
Title: MCP79 (DDR3)

Size	Document Number IM3 (XPS-Joie)	Rev 2A
------	-----------------------------------	-----------

Date: Wednesday, October 29, 2008 Sheet 6 of 59

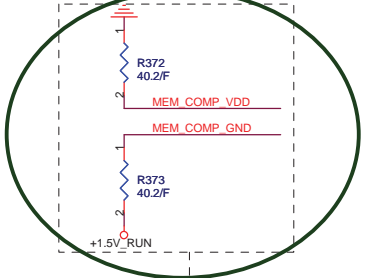
- +V_VPLL**
39mA with RUN rail
- +V_PLL_XREF_XS**
17mA with RUN rail
- +V_PLL_CORE**
19mA with RUN rail
- +V_PLL_DP**
12mA with RUN rail

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic



0910 Michael: Follow NV check list
add 4.7U C738

0102-Sun_Change MEM_COMP_VDD & MEM_COMP_GND setting
MEM_COMP_VDD from +1.5V_RUN to GND &
MEM_COMP_GND from GND to +1.5V_RUN



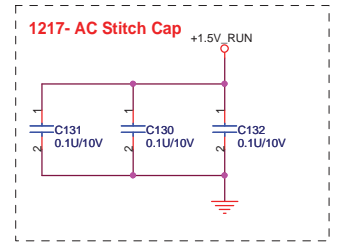
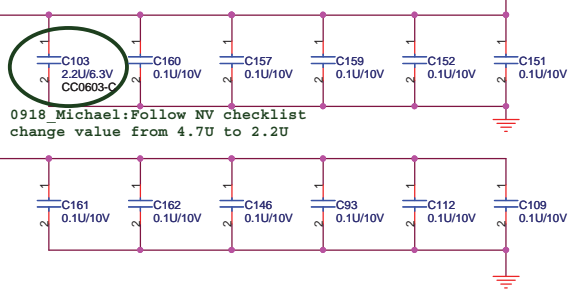
Layout Notice:
1. 40.2 +/-1% ohm to +1.5V_SUS less than 1 inch from MCP79 for DDR3.
2. Route with 7 mils trace width and 8 mils spacing to termination resistor.

U21D SOCKET		MCP79_MOBILE_BGA1437	
SEC 4 OF 11			
U33	MCLK0B_2_P	MCLK1B_2_F	BA41
U34	MCLK0B_2_N	MCLK1B_2_N	BB41
BB24	MCLK0B_1_P	MCLK1B_1_F	AY23
CC24	MCLK0B_1_N	MCLK1B_1_N	BA23
BA21	MCLK0B_0_P	MCLK1B_0_F	BA20
BB21	MCLK0B_0_N	MCLK1B_0_N	AY20
AL17	MCS0B_0*	MCS1B_0*	BC16
AR15	MCS0B_1*	MCS1B_1*	BA13
AN17	MODT0B_0	MODT1B_0	AY16
AN15	MODT0B_1	MODT1B_1	BC13
AV23	MCKE0B_0	MCKE1B_0	BA30
AN25	MCKE0B_1	MCKE1B_1	BA31
MEMORY CONTROL 0B		MEMORY CONTROL 1B	
AA22	GND	AM17	+VDD_MEM
AP12	GND	AM19	+VDD_MEM
G30	GND	AM21	+VDD_MEM
P10	GND	AM23	+VDD_MEM
T10	GND	AM25	+VDD_MEM
T16	GND	AM27	+VDD_MEM
V10	GND	AM29	+VDD_MEM
V34	GND	AM20	+VDD_MEM
V5	GND	AN24	+VDD_MEM
AA39	GND	AT17	+VDD_MEM
AG24	GND	AP16	+VDD_MEM
AH35	GND	AR20	+VDD_MEM
AK7	GND	AR24	+VDD_MEM
AM28	GND	AW15	+VDD_MEM
AT25	GND	AP22	+VDD_MEM
AP30	GND	AP18	+VDD_MEM
AR36	GND	AU16	+VDD_MEM
AL10	GND	AN18	+VDD_MEM
F28	GND	AU24	+VDD_MEM
BC21	GND	AT21	+VDD_MEM
AY9	GND	AY29	+VDD_MEM
BC9	GND	AV24	+VDD_MEM
D34	GND	AU20	+VDD_MEM
F24	GND	AU22	+VDD_MEM
G32	GND	AW27	+VDD_MEM
H31	GND	BC17	+VDD_MEM
K7	GND	AV20	+VDD_MEM
M38	GND	AU17	+VDD_MEM
M5	GND	AY18	+VDD_MEM
M6	GND	AM15	+VDD_MEM
M7	GND	AU18	+VDD_MEM
M9	GND	AY25	+VDD_MEM
N38	GND	AY26	+VDD_MEM
N8	GND	AW19	+VDD_MEM
P33	GND	AW24	+VDD_MEM
P34	GND	BC25	+VDD_MEM
P37	GND	AL30	+VDD_MEM
P4	GND	AM31	+VDD_MEM
P40	GND		
E7	GND	T33	GND
R36	GND	T34	GND
R40	GND	T35	GND
R43	GND	T37	GND
R5	GND	T38	GND
T18	GND	T7	GND
T20	GND	T9	GND
AK11	GND	U18	GND
T24	GND	U20	GND
T26	GND	U22	GND

4.3A with ALW rail for S0
318mA for S0 Idle
1 x 2.2uF ceramic
12 x 0.1uF X7R ceramic

0605_Michael: Remove 0ohm R93

0918 Michael: Follow NV checklist
change value from 4.7U to 2.2U



17 PCIE_MRX_GTX_P[0..15]
17 PCIE_MRX_GTX_N[0..15]

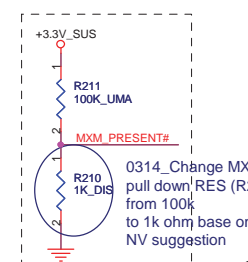
PCIE_MTX_GRX_P[0..15] 17
PCIE_MTX_GRX_N[0..15] 17

PCIE Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

0605 Michael:Remove 0ohm
R185 on MXM_ON#
R433,R435,168 pull-down to GND
R177 on PE_RESET# MXM#
R458 on PCIE_WAKE#

PCIE MRX GTX	Pin	PCIE MTX GRX C	Pin
PCIE MRX GTX P0	E7	PCIE MTX GRX C P0	C347
PCIE MRX GTX N0	E7	PCIE MTX GRX C N0	C340
PCIE MRX GTX P1	D7	PCIE MTX GRX C P1	C373
PCIE MRX GTX N1	C7	PCIE MTX GRX C N1	C384
PCIE MRX GTX P2	E6	PCIE MTX GRX C P2	C556
PCIE MRX GTX N2	E6	PCIE MTX GRX C N2	C565
PCIE MRX GTX P3	F6	PCIE MTX GRX C P3	C552
PCIE MRX GTX N3	F5	PCIE MTX GRX C N3	C548
PCIE MRX GTX P4	E4	PCIE MTX GRX C P4	C358
PCIE MRX GTX N4	E3	PCIE MTX GRX C N4	C367
PCIE MRX GTX P5	D3	PCIE MTX GRX C P5	C333
PCIE MRX GTX N5	C3	PCIE MTX GRX C N5	C323
PCIE MRX GTX P6	G5	PCIE MTX GRX C P6	C547
PCIE MRX GTX N6	H5	PCIE MTX GRX C N6	C544
PCIE MRX GTX P7	J7	PCIE MTX GRX C P7	C543
PCIE MRX GTX N7	J6	PCIE MTX GRX C N7	C539
PCIE MRX GTX P8	J5	PCIE MTX GRX C P8	C311
PCIE MRX GTX N8	J4	PCIE MTX GRX C N8	C319
PCIE MRX GTX P9	L11	PCIE MTX GRX C P9	C534
PCIE MRX GTX N9	L10	PCIE MTX GRX C N9	C538
PCIE MRX GTX P10	L9	PCIE MTX GRX C P10	C297
PCIE MRX GTX N10	L8	PCIE MTX GRX C N10	C307
PCIE MRX GTX P11	L7	PCIE MTX GRX C P11	C291
PCIE MRX GTX N11	L6	PCIE MTX GRX C N11	C280
PCIE MRX GTX P12	N11	PCIE MTX GRX C P12	C532
PCIE MRX GTX N12	N10	PCIE MTX GRX C N12	C529
PCIE MRX GTX P13	N9	PCIE MTX GRX C P13	C523
PCIE MRX GTX N13	N7	PCIE MTX GRX C N13	C527
PCIE MRX GTX P14	N7	PCIE MTX GRX C P14	C263
PCIE MRX GTX N14	N6	PCIE MTX GRX C N14	C267
PCIE MRX GTX P15	N5	PCIE MTX GRX C P15	C519
PCIE MRX GTX N15	N4	PCIE MTX GRX C N15	C518

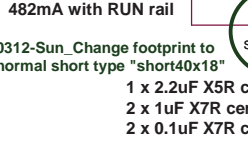
PCIE



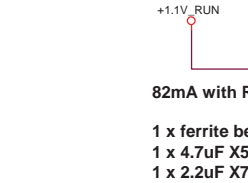
0314_Change MXM_PRESENT# pull down! RES (R210) from 100k to 1k ohm base on NV suggestion

0825_Michael:Add KB detect function
0918_Michael:Remove KB detect function
0920_Michael:Add KB detect function

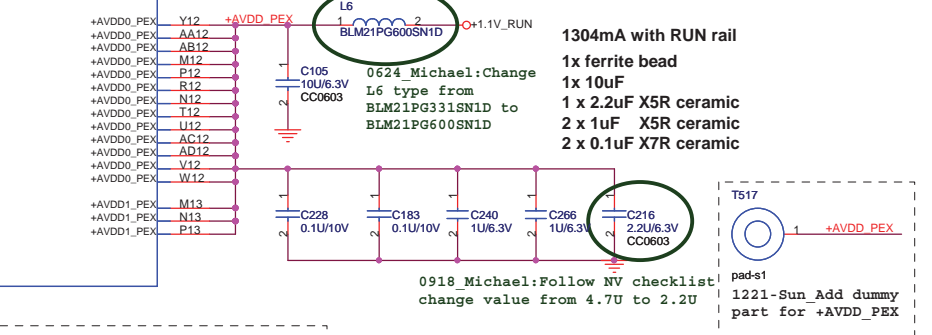
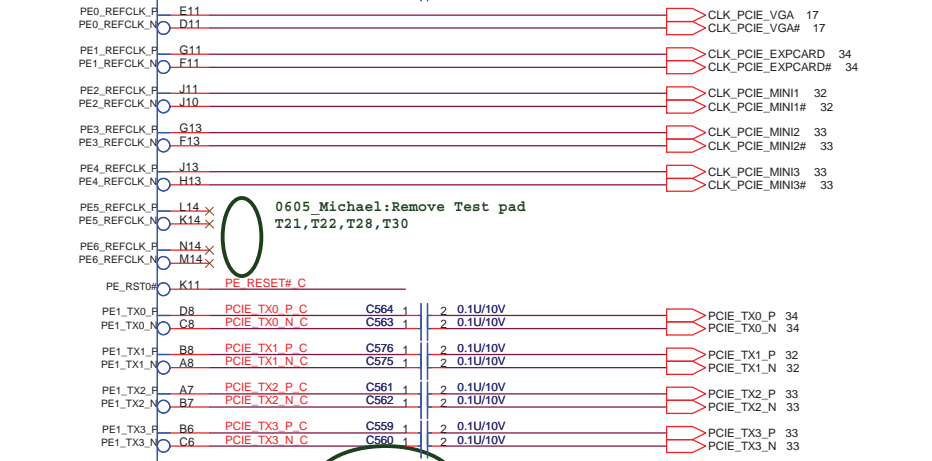
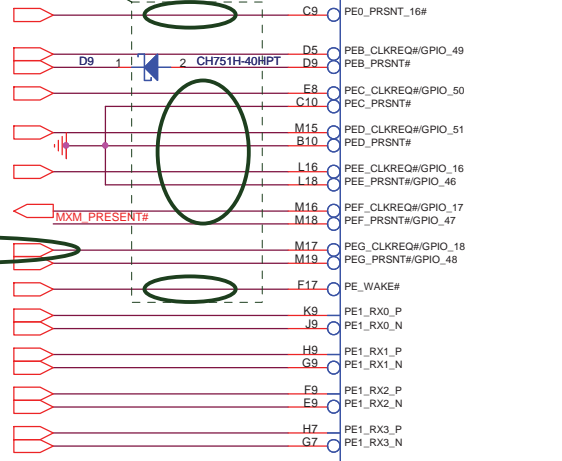
Express Card
34 CARD_CLK_REQ#
34,36 EXPRCD_PWREN#
WLAN
32 MINI1CLK_REQ#
UWB/BT
33 MINI2CLK_REQ#
WWAN
33 MINI3CLK_REQ#
17 PE_RESET_MXM#



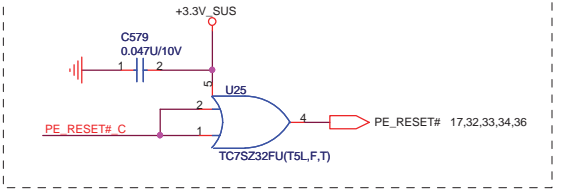
0918_Michael:Follow NV checklist change value from 4.7U to 2.2U and add 1U



82mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic



0918_Michael:Follow NV checklist change value from 4.7U to 2.2U

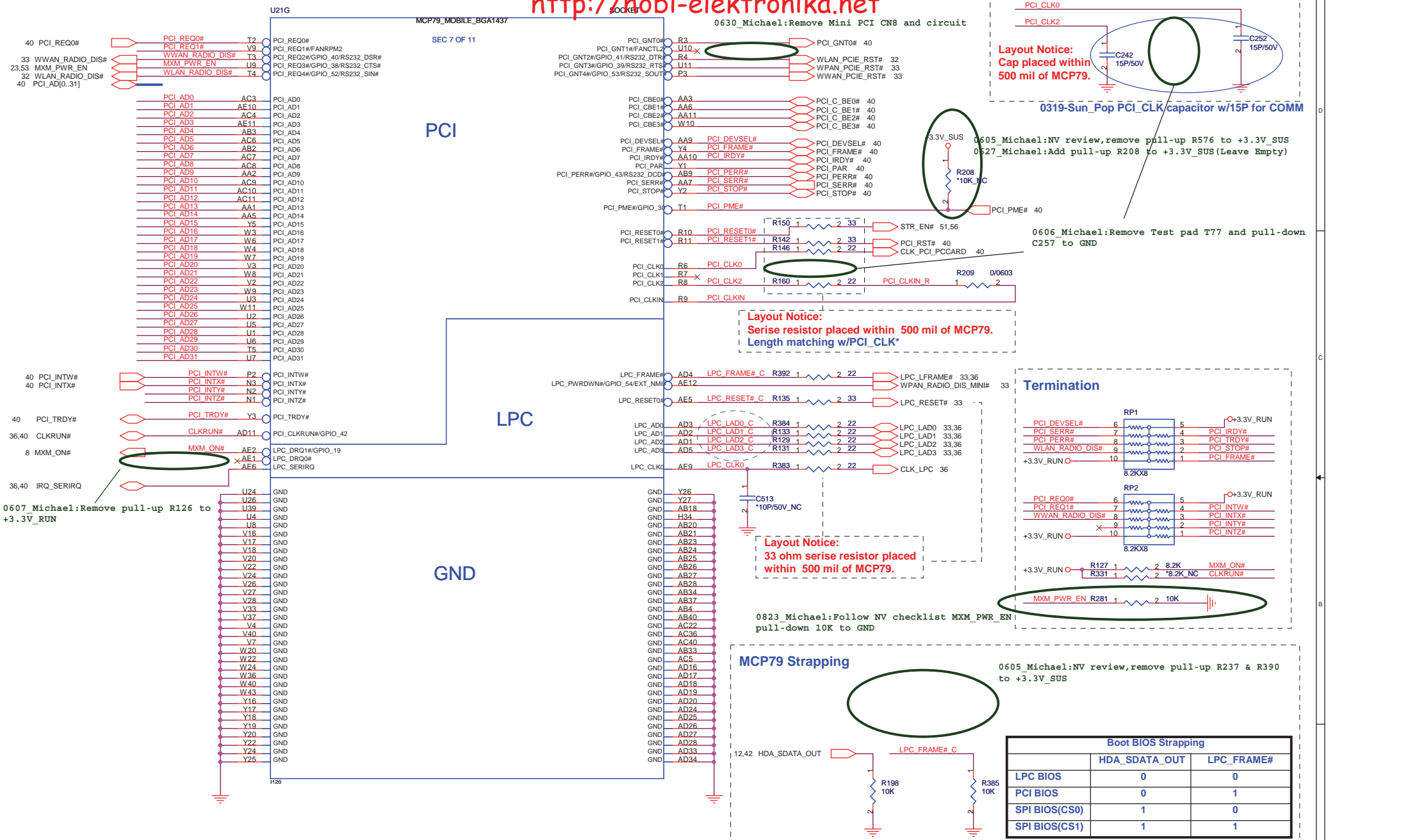


QUANTA COMPUTER

Title: MCP79 (PCIE)

Size	Document Number	Rev
	IM3 (XPS-Joie)	2A

Date: Saturday, September 20, 2008 Sheet 8 of 59



Layout Notice:
Cap placed within 500 mil of MCP79.

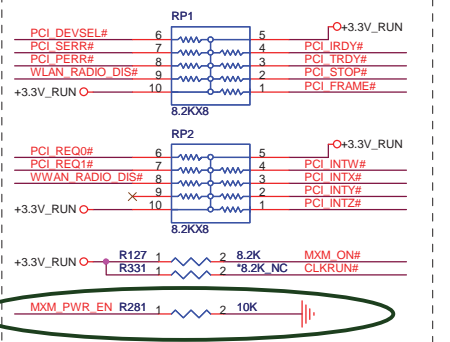
0319-Sun_Pop PCI_CLK/capacitor w/15P for COMM

0605 Michael:NV review,remove pull-up R576 to +3.3V_SUS
0627 Michael:Add pull-up R208 to +3.3V_SUS (Leave Empty)

0606 Michael:Remove Test pad T77 and pull-down C257 to GND

Layout Notice:
Serise resistor placed within 500 mil of MCP79.
Length matching w/PCI_CLK*

Termination



Layout Notice:
33 ohm serise resistor placed within 500 mil of MCP79.

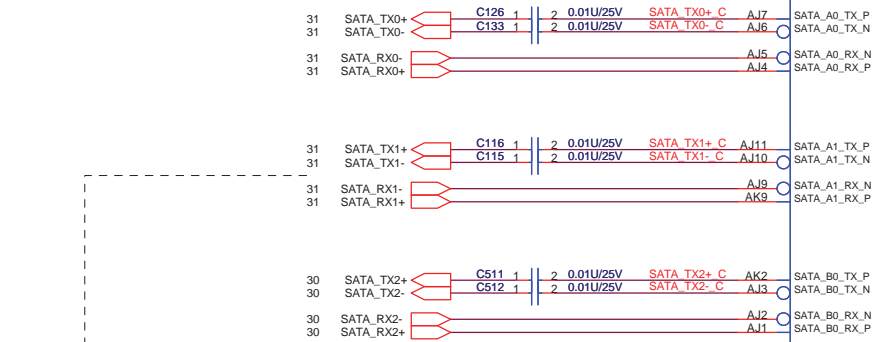
0823 Michael:Follow NV checklist MXM_PWR_EN pull-down 10K to GND

MCP79 Strapping

0605 Michael:NV review,remove pull-up R237 & R390 to +3.3V_SUS

Boot BIOS Strapping

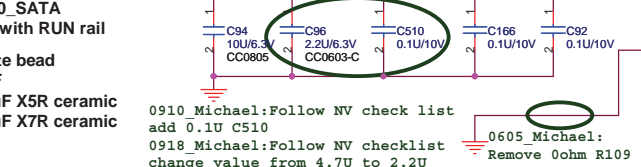
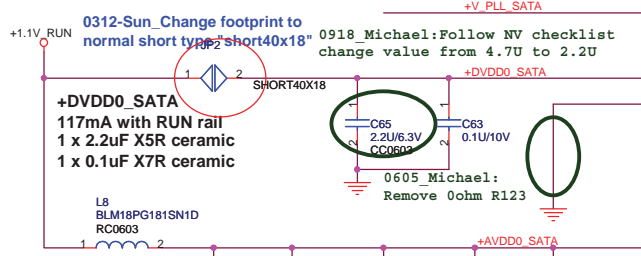
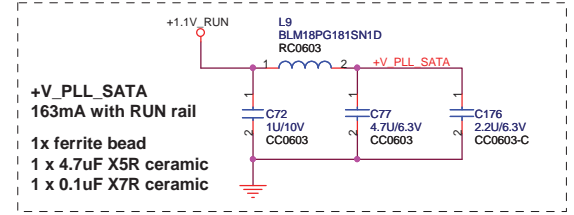
	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS(CS0)	1	0
SPI BIOS(CS1)	1	1



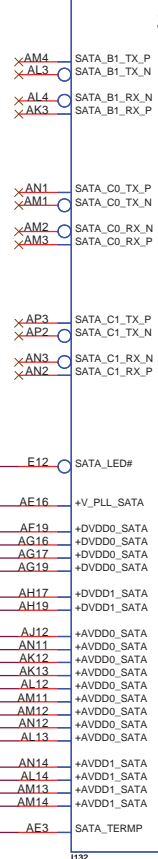
SATA Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 400 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 500 mils.
After Brackout:
 Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
TX and RX intra-pair skew for a differential pair is 5 mils.

SATA

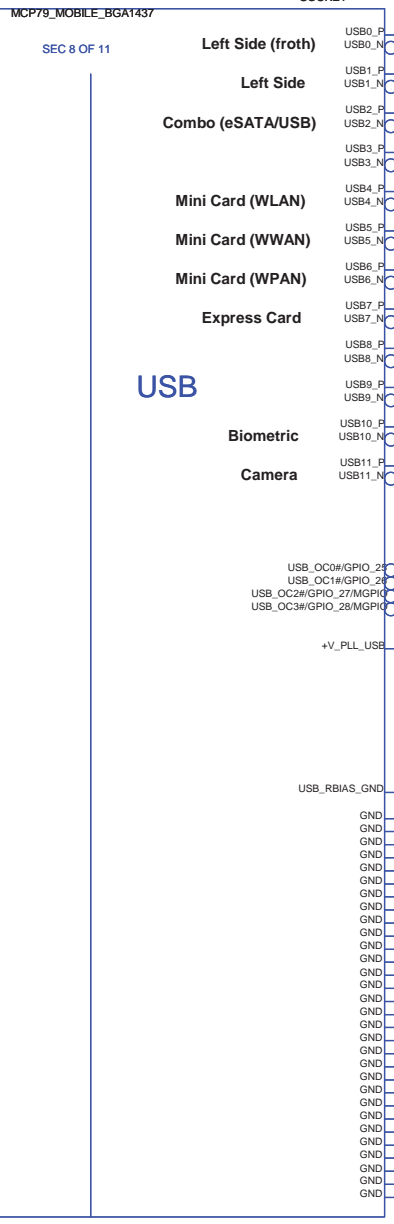
USB



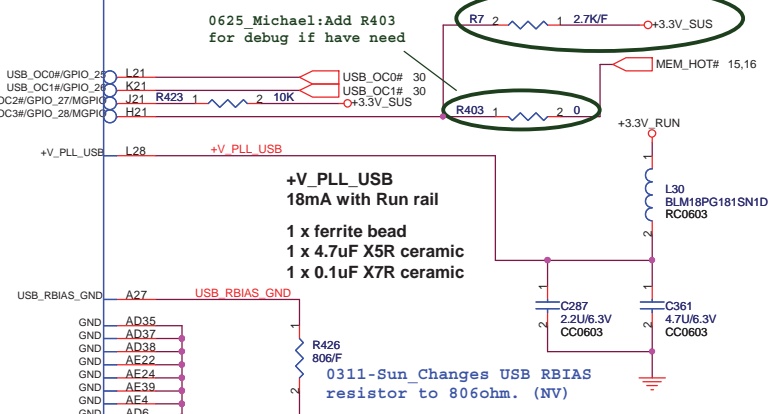
Layout Notice:
 2.49K ohm to GND within 500 mils of MCP79.
 Routing 8 mils spacing to resistor.



USB Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 300 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 400 mils.
After Brackout:
 Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals.
 Each USB pair must be length matched to within 50 mil.



- Left Side (froth)
- Left Side
- Combo (eSATA/USB)
- Mini Card (WLAN)
- Mini Card (WWAN)
- Mini Card (WPAN)
- Express Card
- Biometric
- Camera

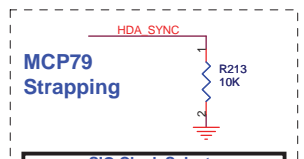
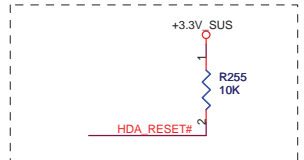
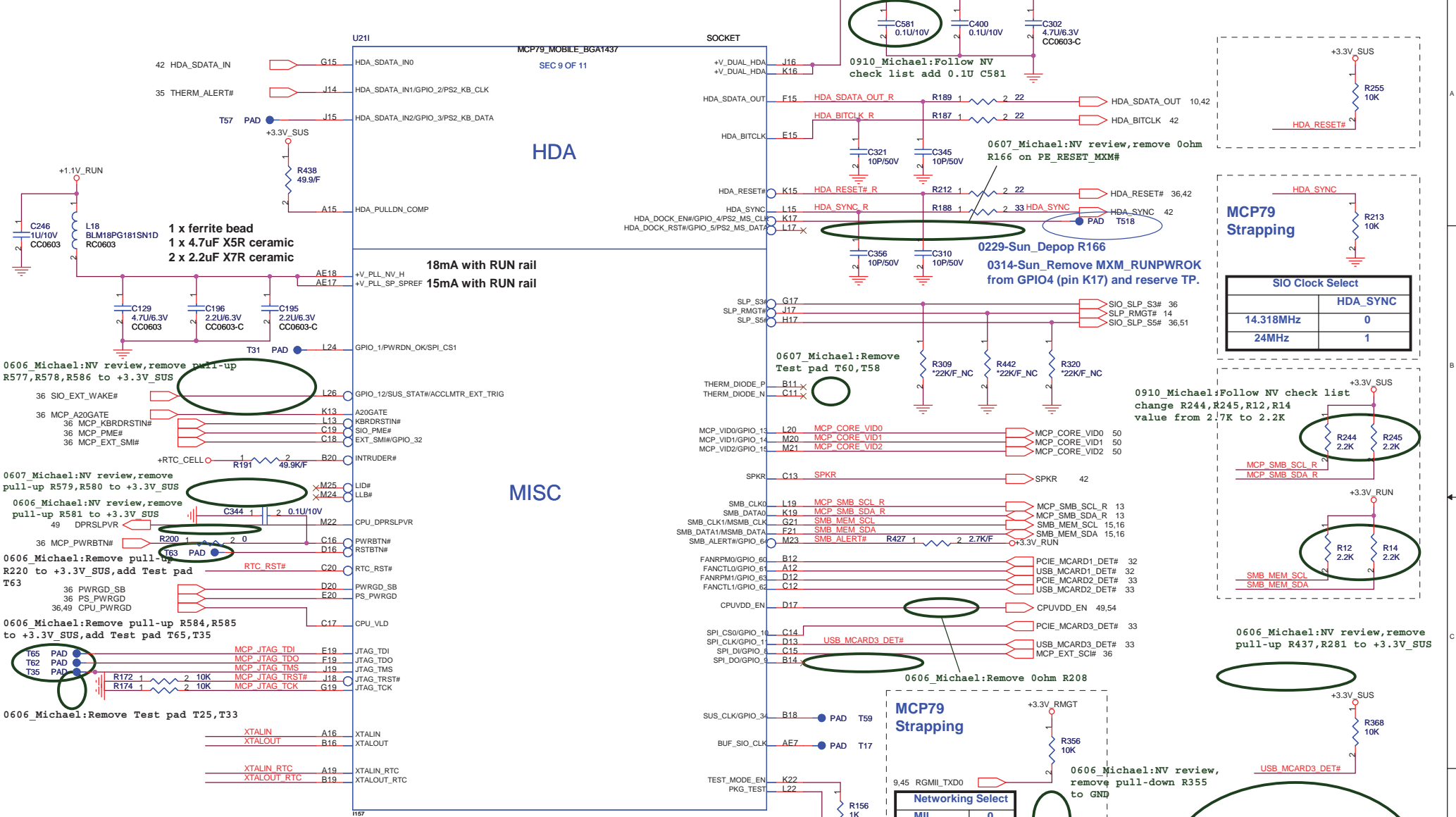


Layout Notice:
 909 ohm +-1% to GND within 1000 mil of MCP79.
 Routing trace at least 8 mil wide to resistor.

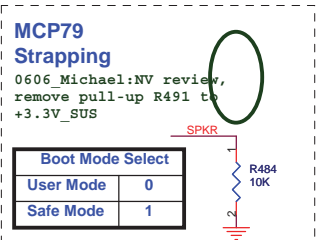
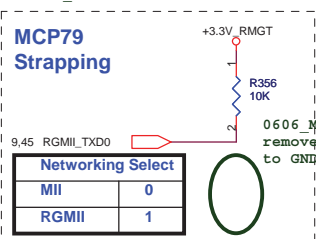
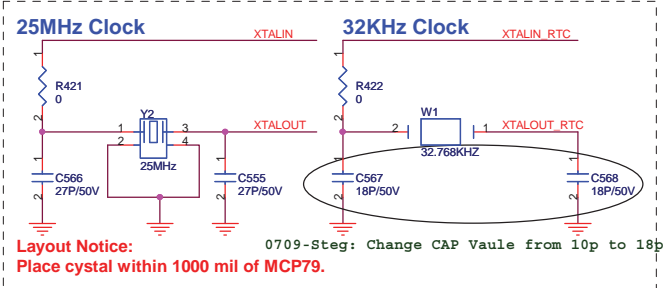
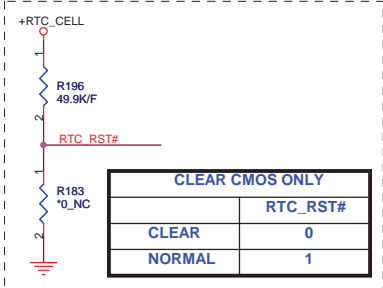
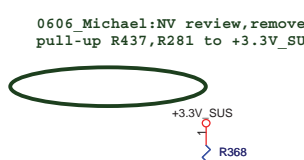
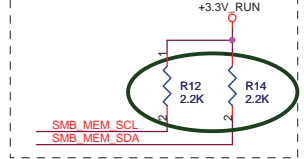
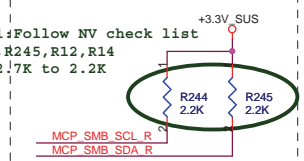


Title MCP79 (SATA,USB)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Monday, October 20, 2008	Sheet 11 of 59

1 x 0.1uF X7R ceramic



SIO Clock Select	
	HDA_SYNC
14.318MHz	0
24MHz	1



QUANTA COMPUTER

Title: MCP79 (HDA,MISC)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Thursday, September 18, 2008 Sheet 12 of 59

1 x 10uF ceramic
 2 x 2.2uF X5R ceramic
 3 x 1uF X5R ceramic
 3 x 0.22uF X5R ceramic
 12 x 0.1uF X7R ceramic

17.756A with RUN rail for S0
 2850mA for S0 Idle

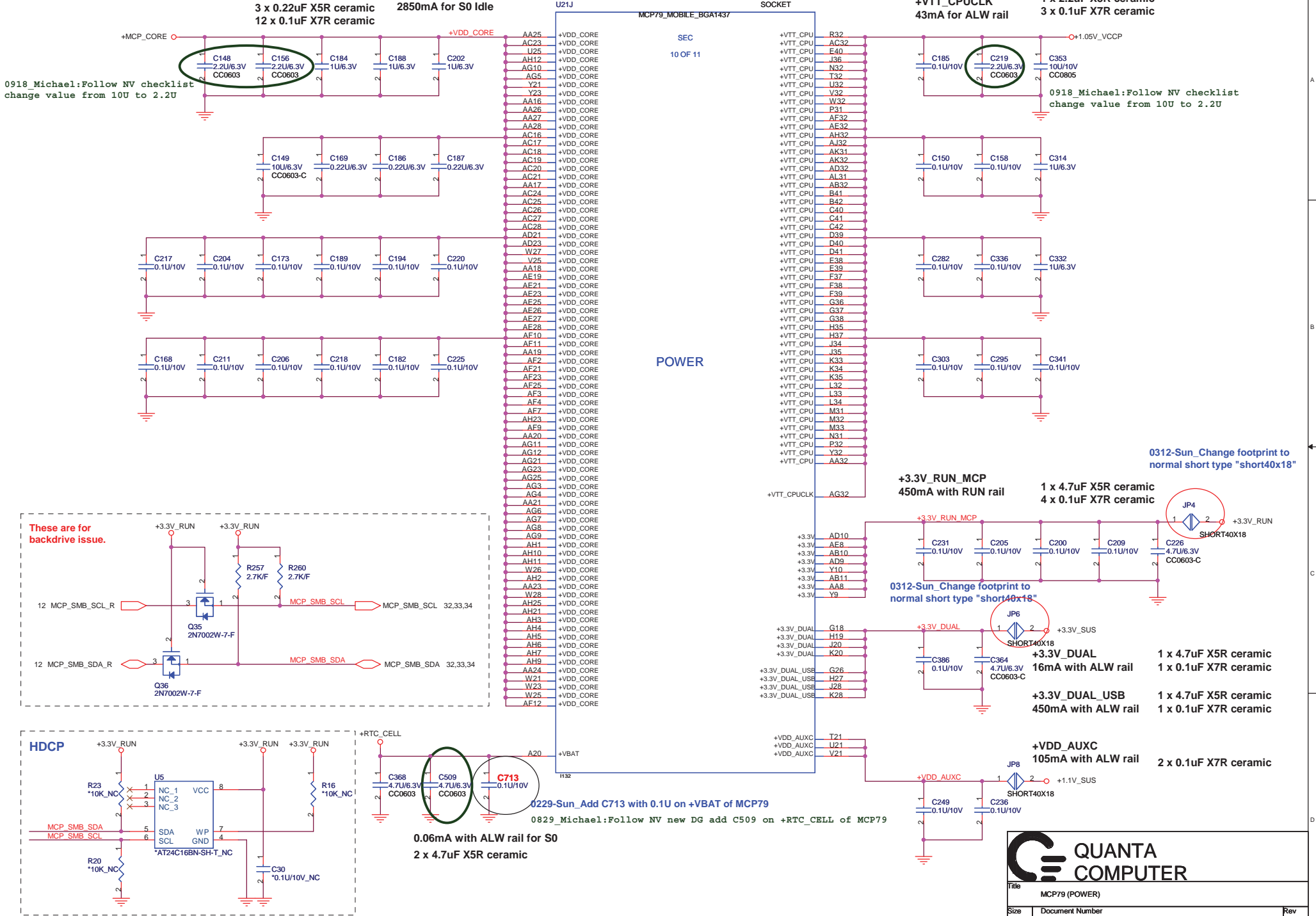
+VTT_CPU
 1139mA for ALW rail

+VTT_CPUCLK
 43mA for ALW rail

1 x 10uF ceramic
 1 x 2.2uF X5R ceramic
 3 x 0.1uF X7R ceramic

0918 Michael: Follow NV checklist
 change value from 10U to 2.2U

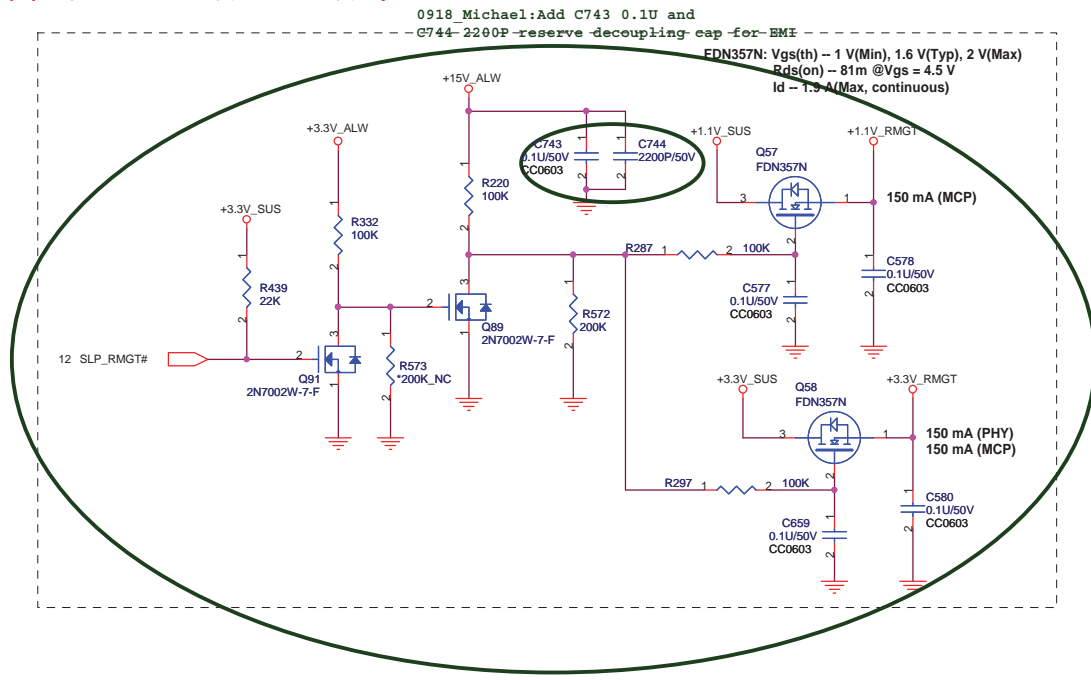
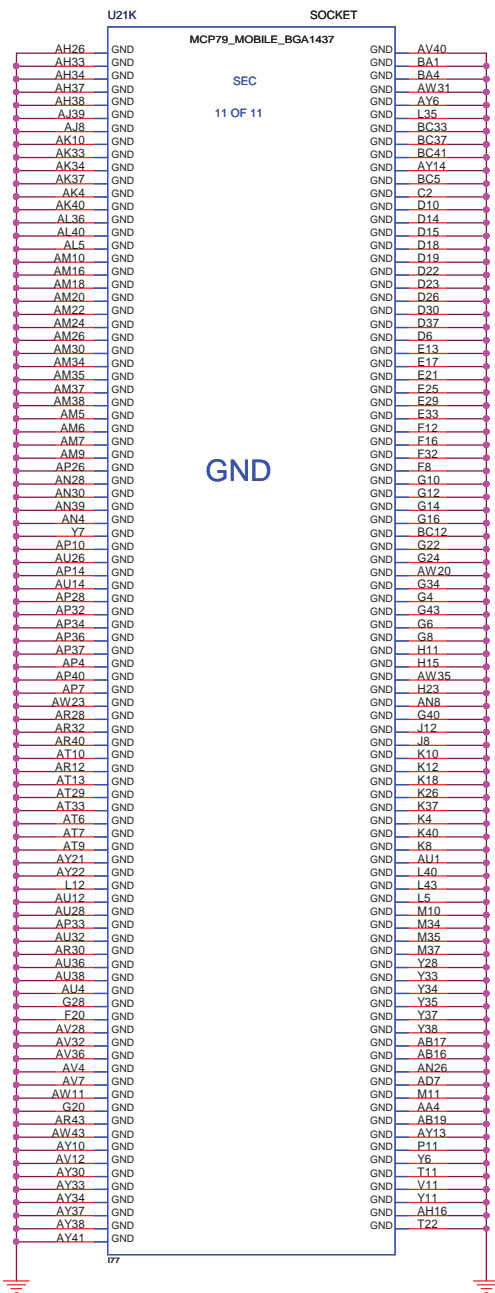
0918 Michael: Follow NV checklist
 change value from 10U to 2.2U



QUANTA COMPUTER

Title: MCP79 (POWER)

Size:	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date:	Friday, September 19, 2008	Sheet: 13 of 59

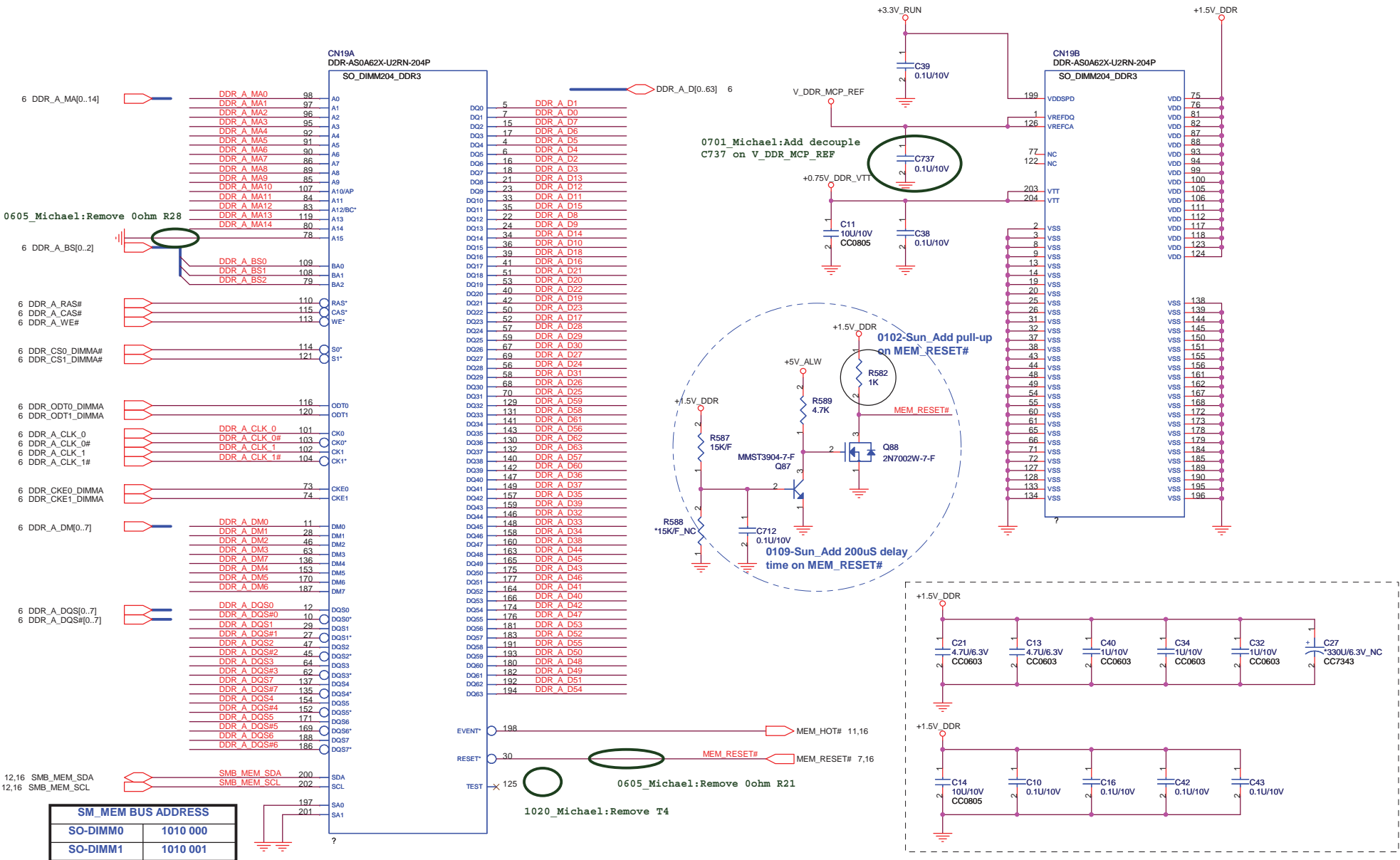


0229-Sun 1.1V_RMGT & +3.3V_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB (Del JP11, JP12)
 Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3
 Add Q89 with 2N7002, R591 with 10K)

0825 Michael: Change Q58 type from SI2301BDS to FDN357N and add MOS 2N7002W-7-F, R&C for +1.1V_RMGT and +3.3V_RMGT power low issue

QUANTA COMPUTER

Title		MCP79 (GND)
Size	Document Number	Rev
	IM3 (XPS-Jolie)	2A
Date:	Tuesday, October 26, 2006	Sheet 14 of 59

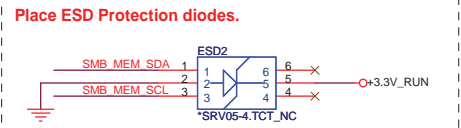


12,16 SMB_MEM_SDA
12,16 SMB_MEM_SCL

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

For EMI Reserved

DDR_A_CLK_1 R19 1 *200/F_NC DDR_A_CLK_1#
DDR_A_CLK_0 R30 1 *200/F_NC DDR_A_CLK_0#

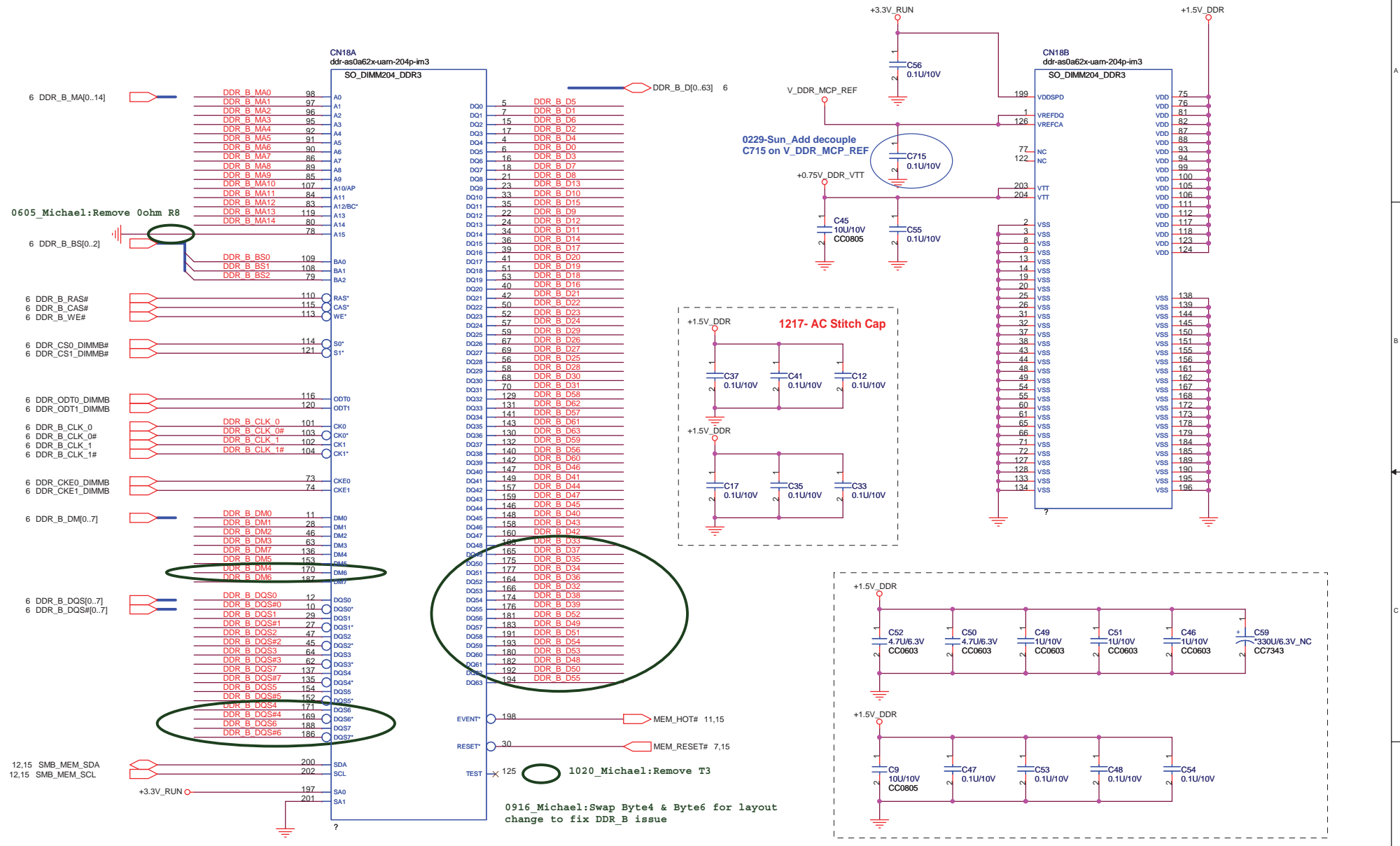


**QUANTA
COMPUTER**

Title: DDR3 SO-DIMM (204P)

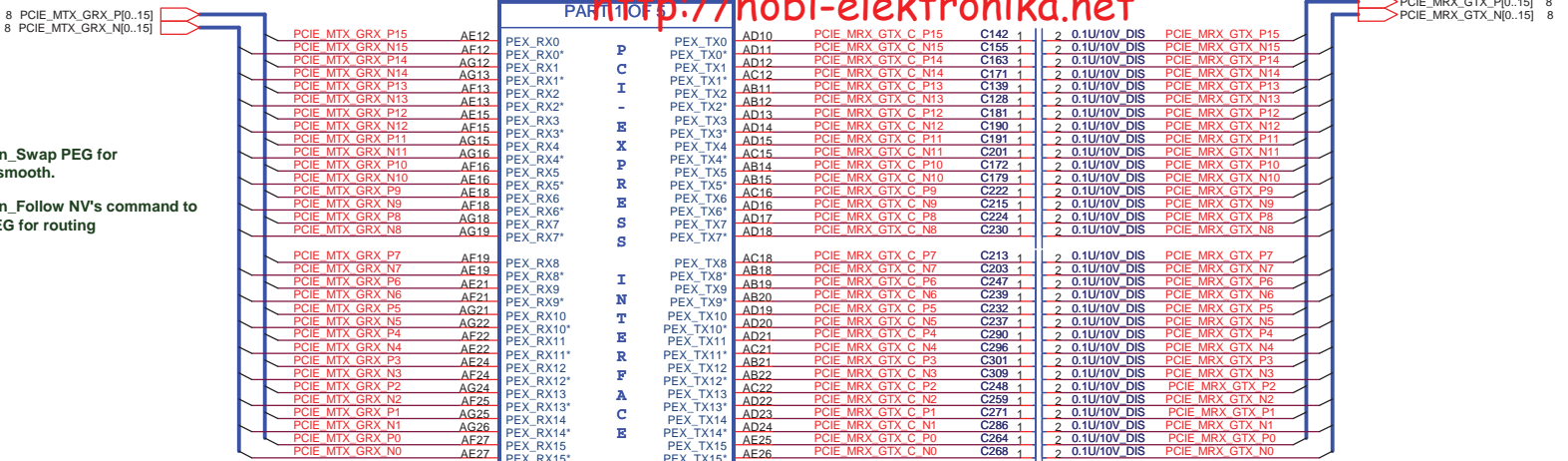
Size: Document Number IM3 (XPS-Joie) Rev 2A

Date: Monday, October 20, 2008 Sheet 15 of 59

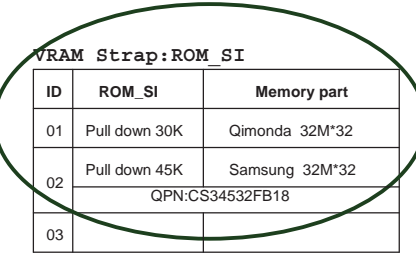


1113-Sun_Swap PEG for routing smooth.
1115-Sun_Follow NV's command to swap PEG for routing

IM3 dedicated.



1115-Sun_Follow NV's command to swap PEG for routing smooth

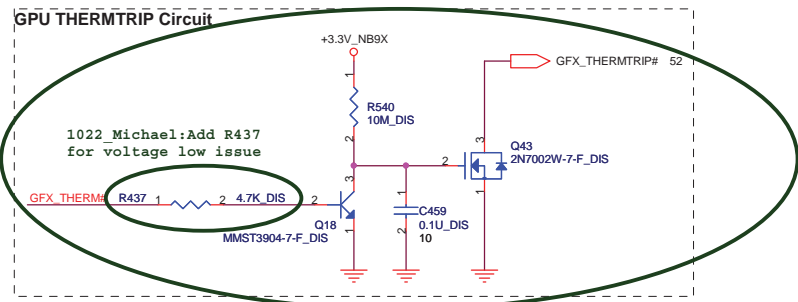
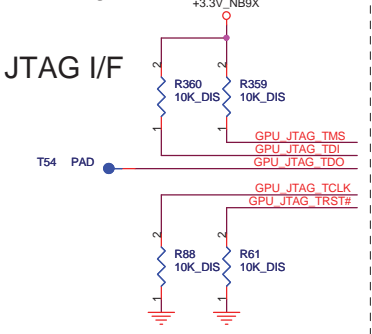


0604_Michael: Follow NV command to modify VRAM Strap resistor vaule

GPIO USAGE

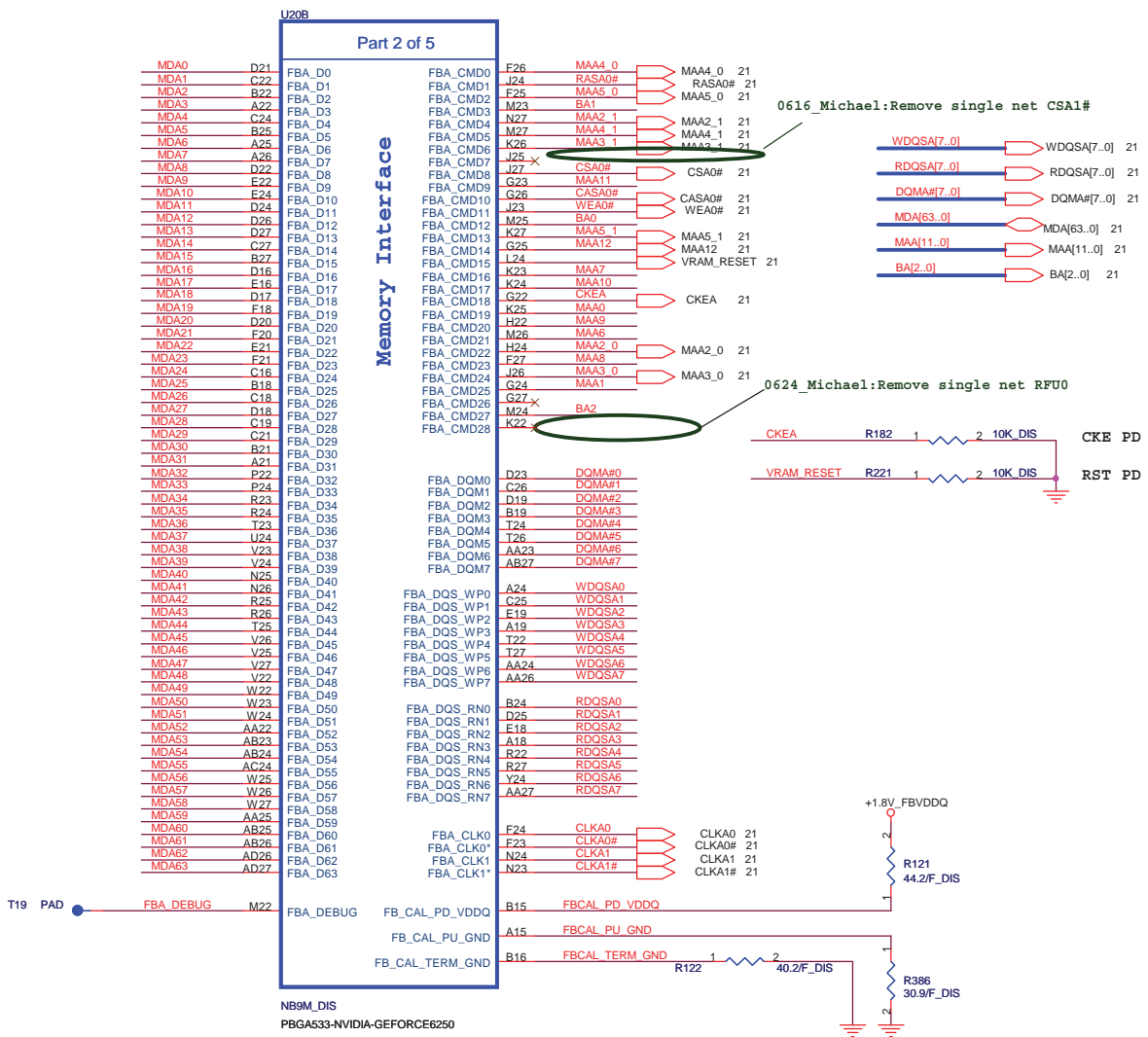
GPIO	I/O	ACTIVE	USAGE	Used
0	IN	N/A	NVGEM HOTPLUG DETECT	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT	
2	OUT	HIGH	PANEL BACKLIGHT PWM	
3	OUT	HIGH	PANEL POWER ENABLE	
4	OUT	HIGH	PANEL BACKLIGHT ENABLE	
5	OUT	HIGH	NVVDD ALTV0	
6	OUT	HIGH	NVVDD ALTV1	
7	OUT	HIGH	FBVDD VIDO	
8	IN	LOW	OVERTEMP ALERT	
9	OUT	LOW	THERMAL ALERT	
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)	
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)	
12	IN	N/A	AC DETECT	
13	OUT	LOW	POWER SUPPLY CONTROL0	
14	OUT	HIGH	POWER SUPPLY CONTROL1	
15	IN	N/A	HPD_E	
16	IN	N/A	DVI_E	No
17	IN	N/A	HDMI_E	No
18	IN	N/A	DVI_F (not used)	No
19	IN	N/A	HDMI_F (not used)	No

Place together.



0825 Michael: Modify THERMTRIP circuit, add MOS and CAP





NB9M_DIS
PBG533-NVIDIA-GEFORCE6250

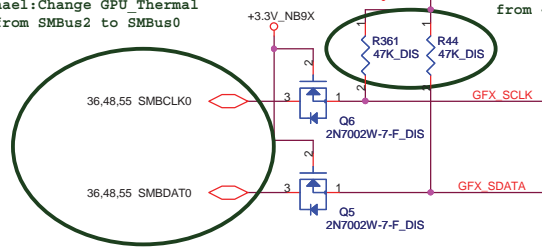
Update as "PUN-03303-001_V01".

GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

Note: Use only 1% resistors for driver calibration

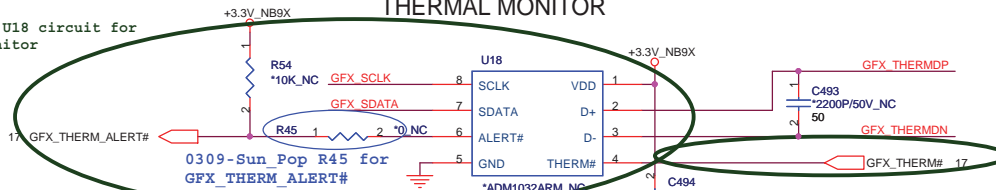


0627 Michael: Change GPU_Thermal control from SMBus2 to SMBus0



0807 Change R361, R44 from 4.7k to 47k for battery issue

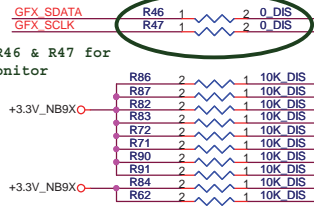
0708 Michael: Depop U18 circuit for internal thermal monitor



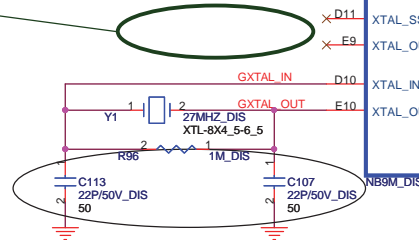
0309-Sun Pop R45 for GFX_THERM_ALERT#

0605 Michael: Add R56 connect to GFX_THERM#
0904 Michael: Remove R56 and change port type from output to input

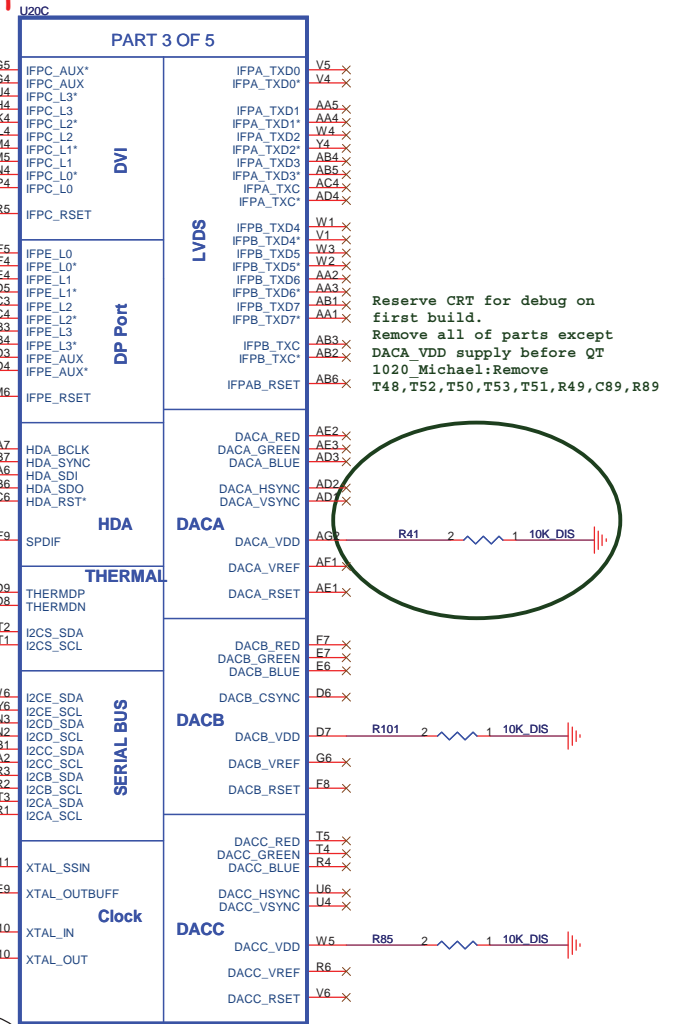
0708 Michael: Pop R46 & R47 for internal thermal monitor



0701 Michael: Remove SPREAD SPECTRUM circuit

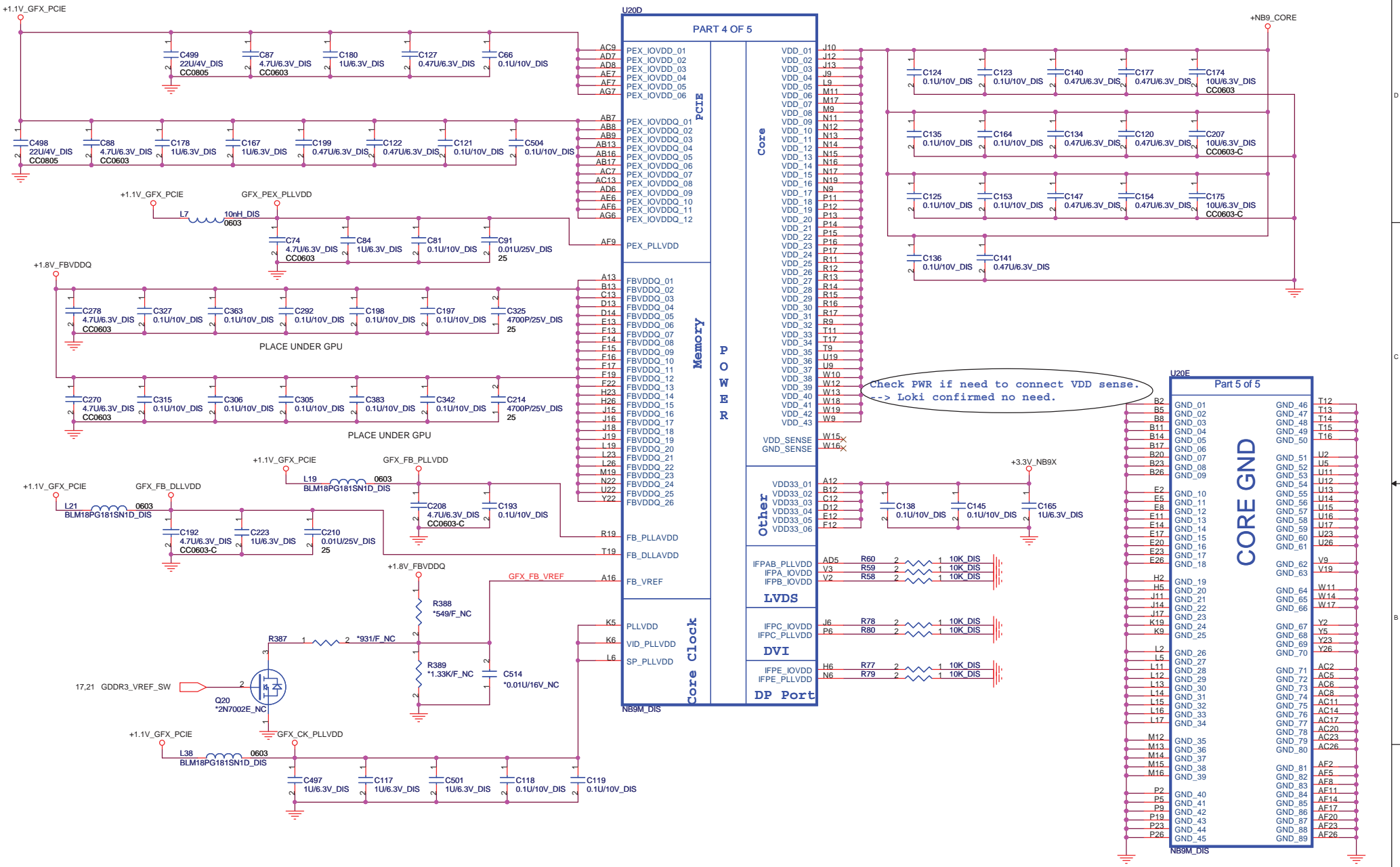


0709-Steg: Change CAP Value from 18p to 22p



Reserve CRT for debug on first build.
Remove all of parts except DACA_VDD supply before QT
1020 Michael: Remove T48, T52, T50, T53, T51, R49, C89, R89





QUANTA COMPUTER

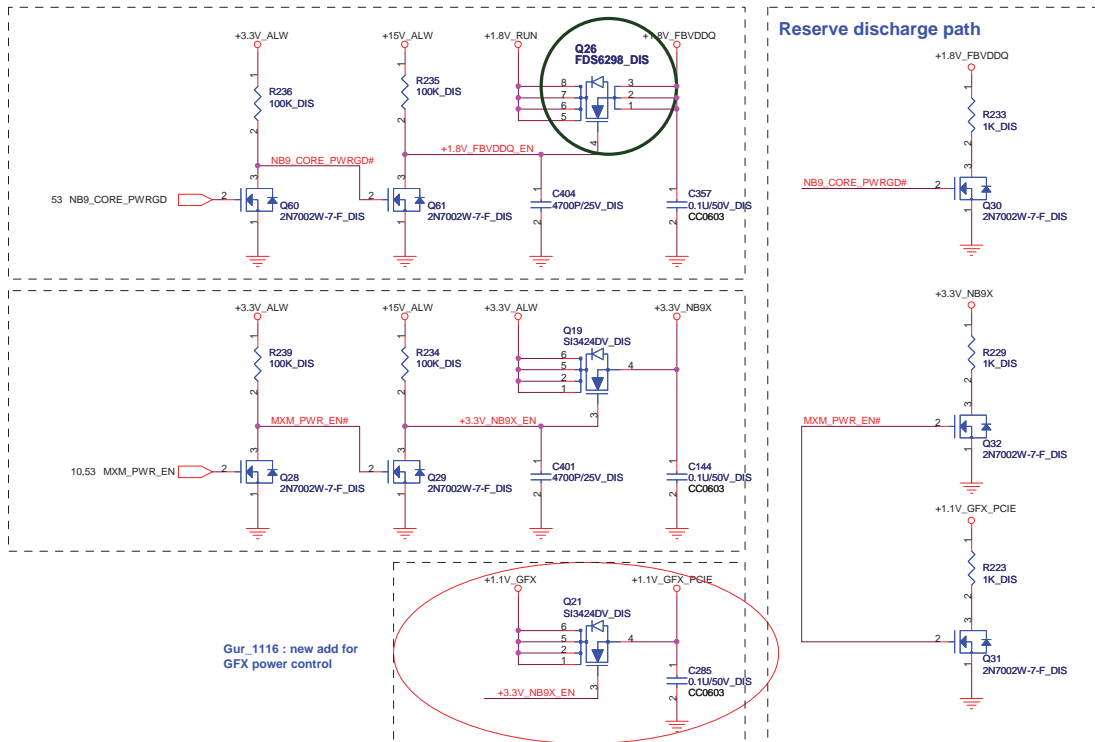
Title: VGA-NB9X GB1-64 (POWER,GND)

Size: Document Number IM3 (XPS-Joie) Rev 2A

Date: Friday, September 05, 2008 Sheet 20 of 59

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

1225-Sun_Chenge Q26 from SI4812BDY to SI4800BDY-T1-E3
 1022_Michael:Change Q26 from SI4800BDY-T1-E3 to BAM62980005

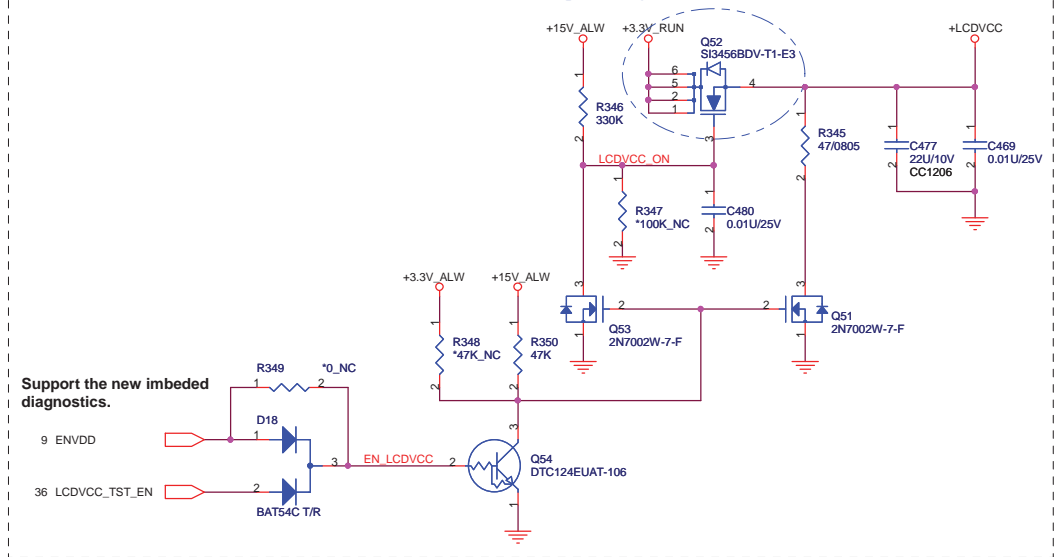


**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

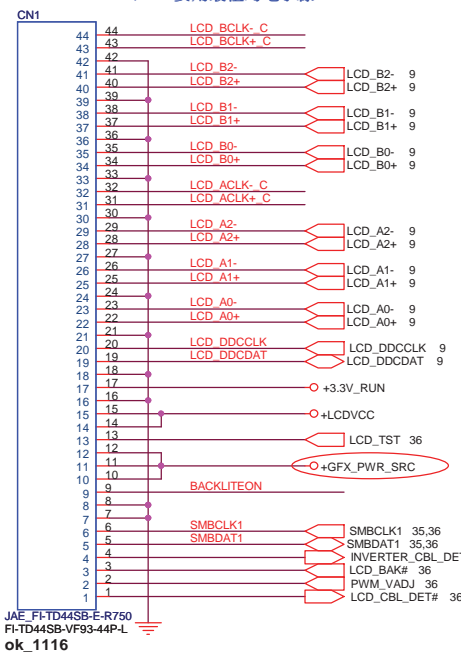
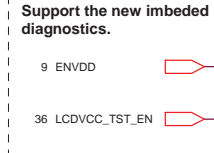
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

0112-Stanley: Change BOM for EOL issue (SI3456BDV).

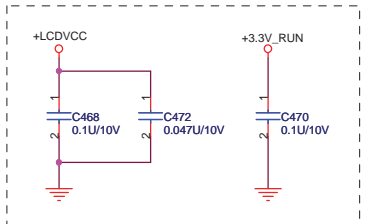
GND,VCC要用最粗的電子線



Support the new imbedded diagnostics.



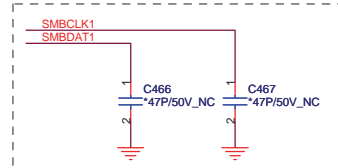
JAE FI-TD44SB-E-R750
FI-TD44SB-VF93-44P-L
ok_1116



WXGA 1280*800=>70 MHz
WXGA+ 1440*900=>108 MHz
WSXGA+ 1680*1050=>120MHz
WUXGA 1920*1200=>166 MHz

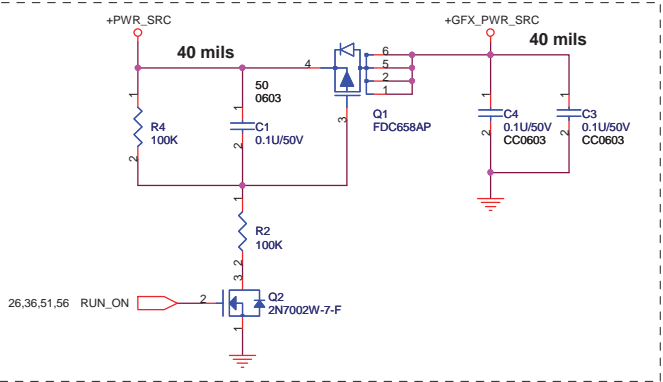
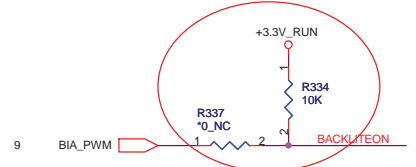
Address : A9H --Contrast
AAH --Backlight

MBRAI specification of antenna gain is
10dBi@474MHz, -7dBi@698MHz,
-5dBi@858MHz.



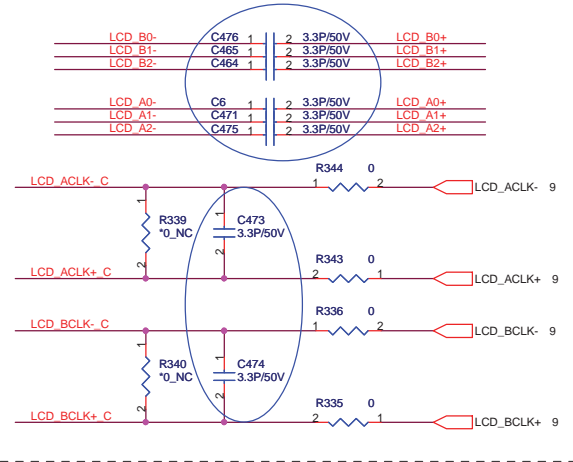
Populate R65 for DPST implementation only.

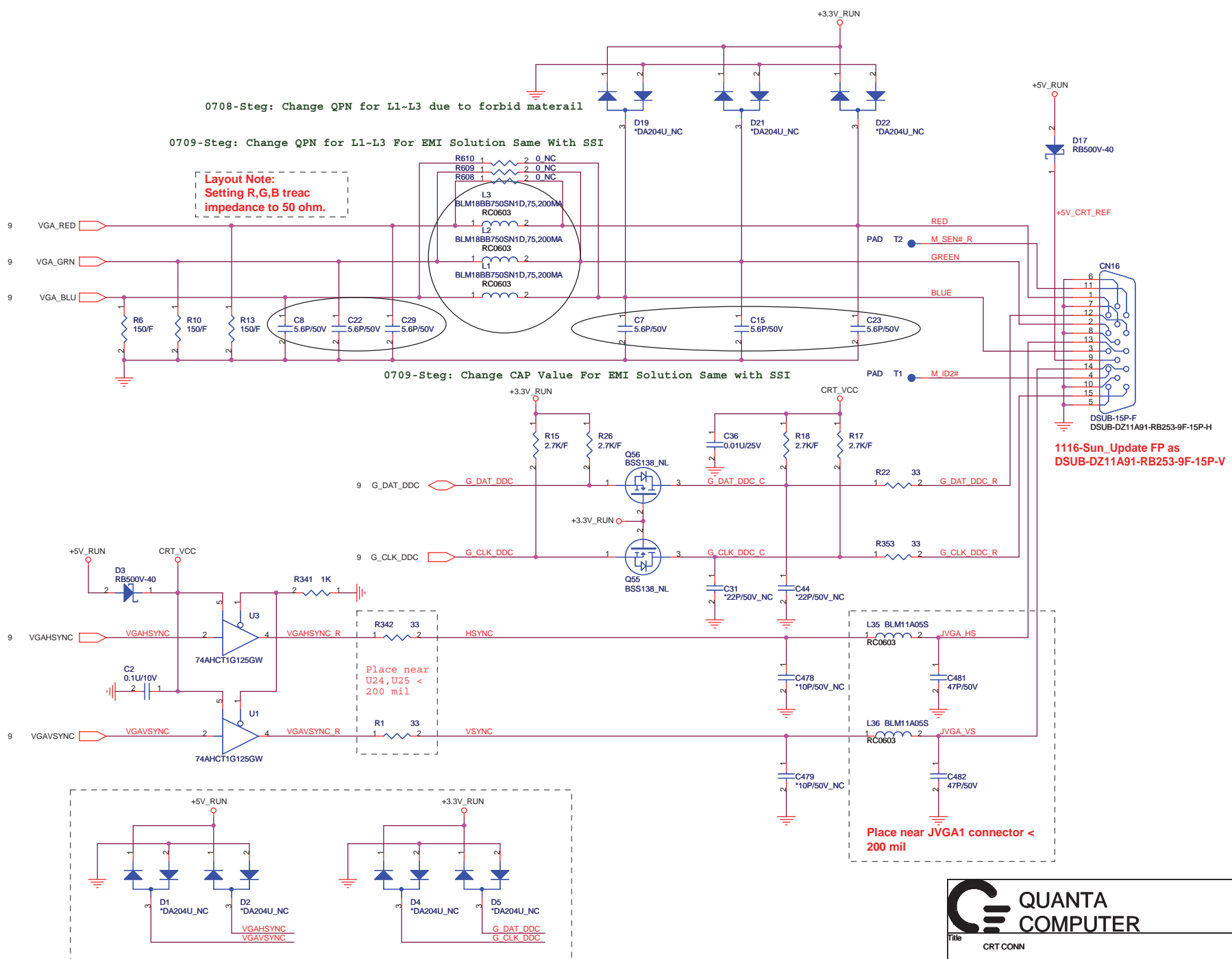
Populate R341 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.



0319-Sun_Pop 3.3P on LVDS bus for COMM team demand

Shunt capacitors on LVDS for improving WWAN.

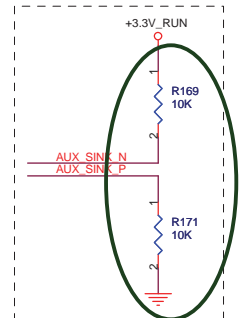
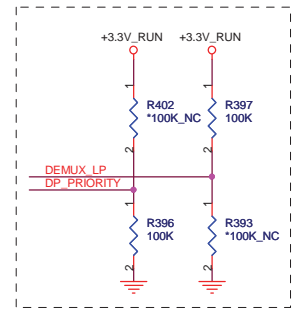
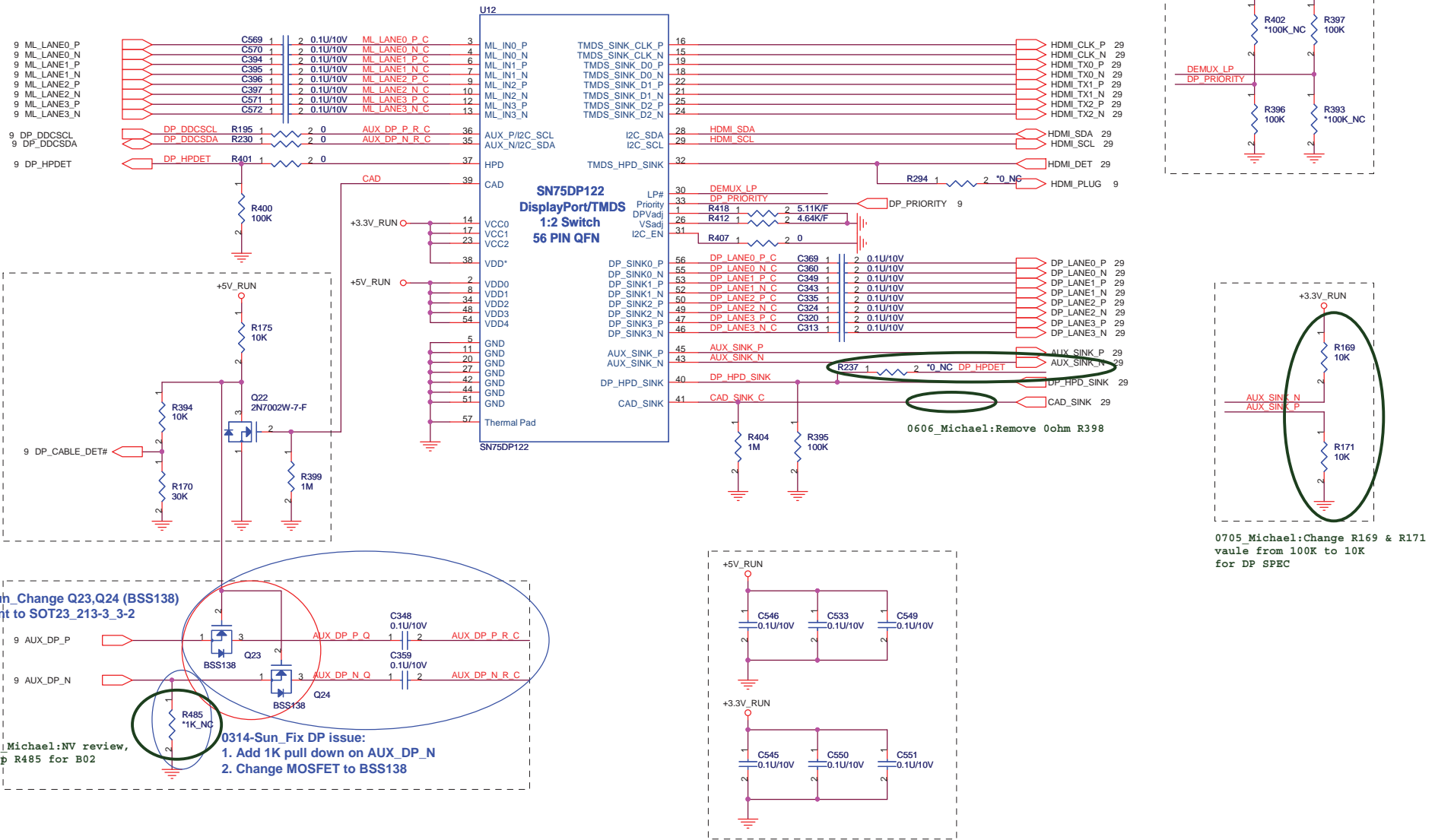




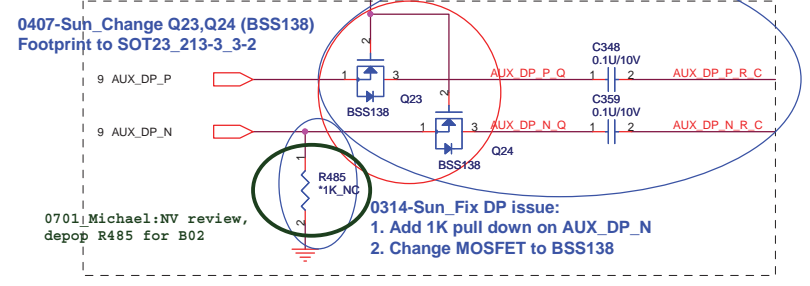
1116-Sun_Update FP as DSUB-DZ11A91-RB253-9F-15P-H



Title CRT CONN		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 27 of 59

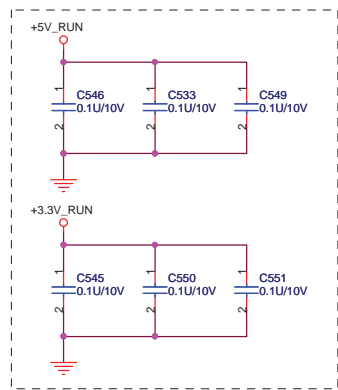


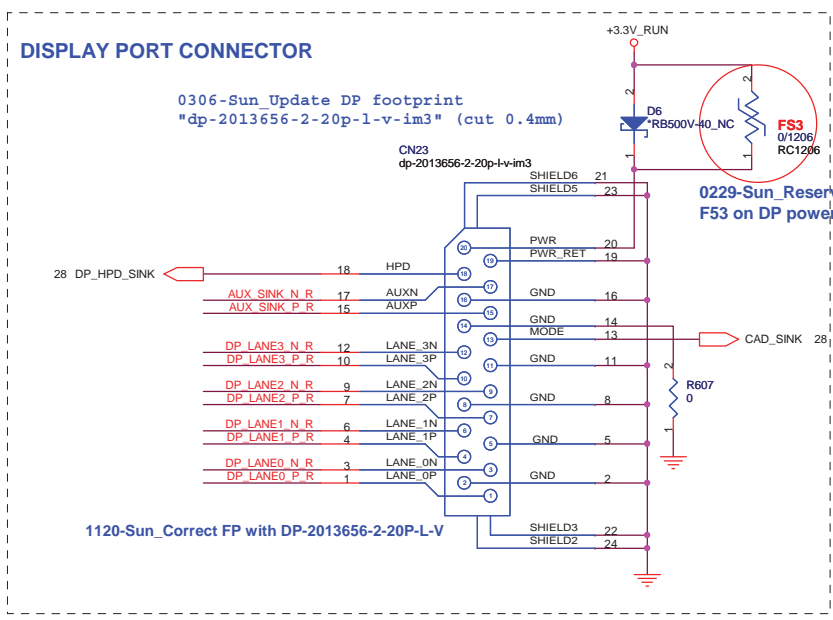
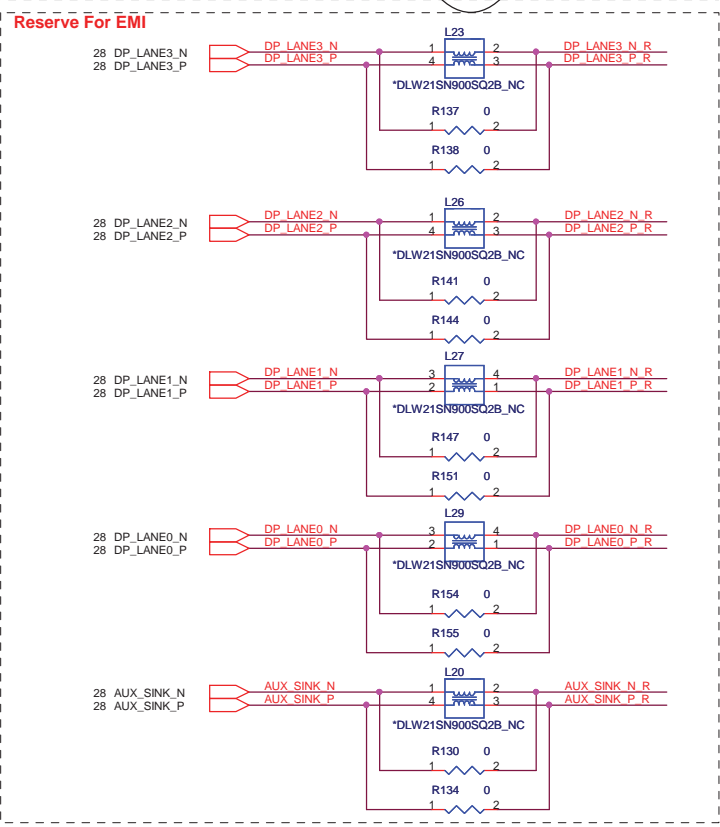
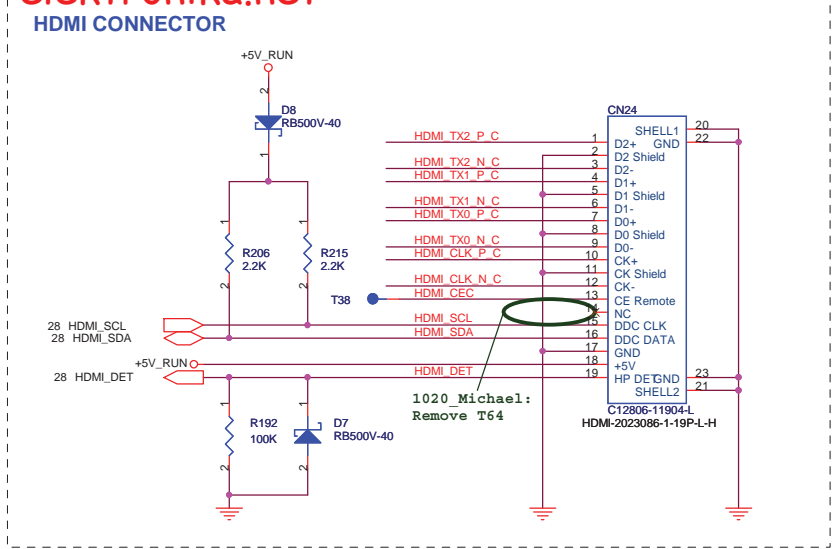
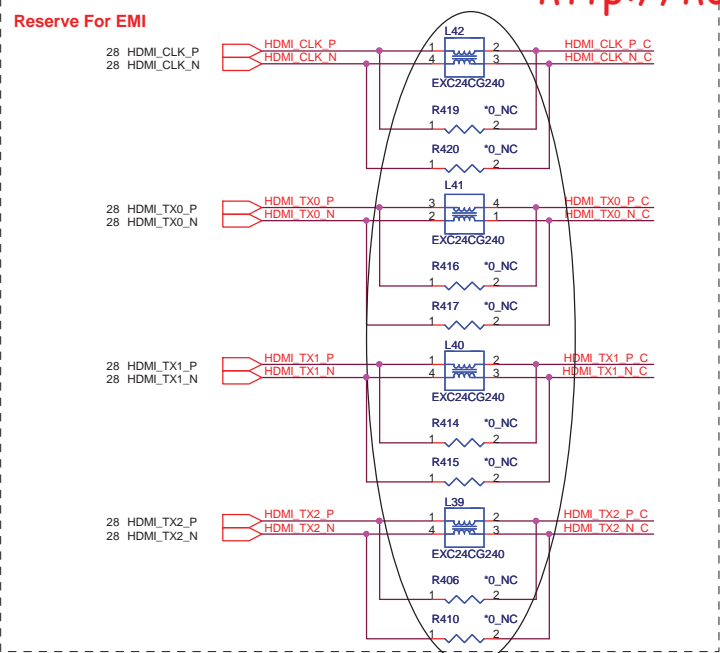
0705 Michael: Change R169 & R171 value from 100K to 10K for DP SPEC

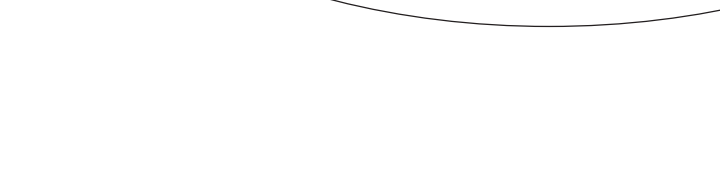
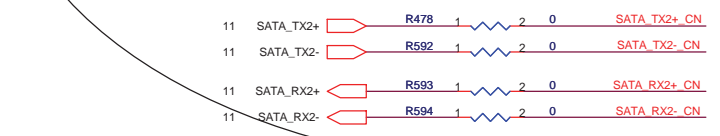
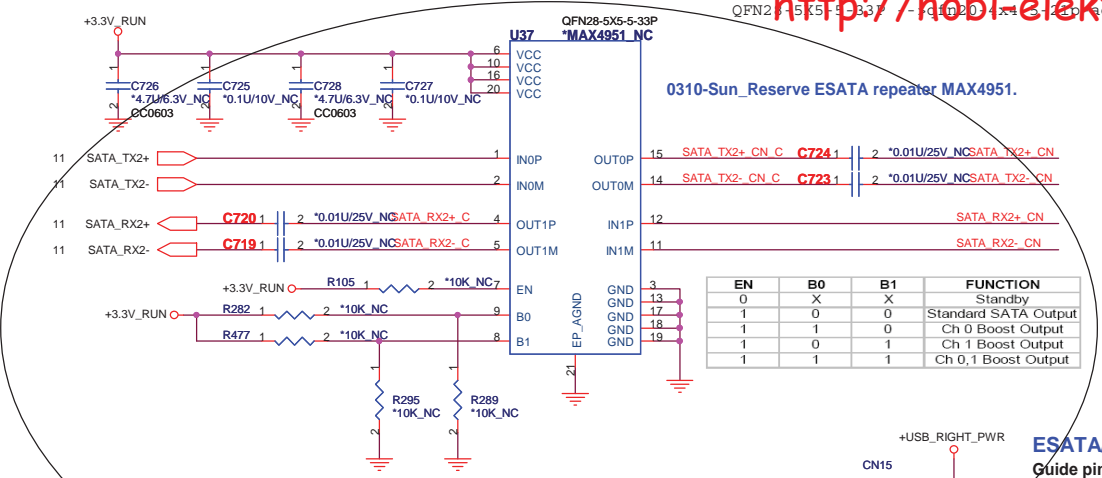


0701 Michael: NV review, depop R485 for B02

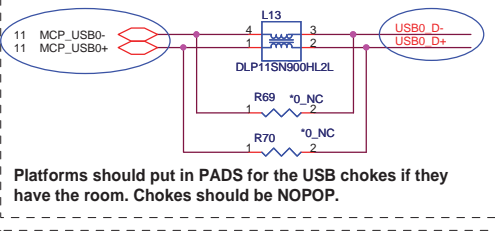
0314-Sun Fix DP issue:
 1. Add 1K pull down on AUX_DP_N
 2. Change MOSFET to BSS138



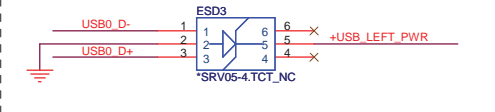




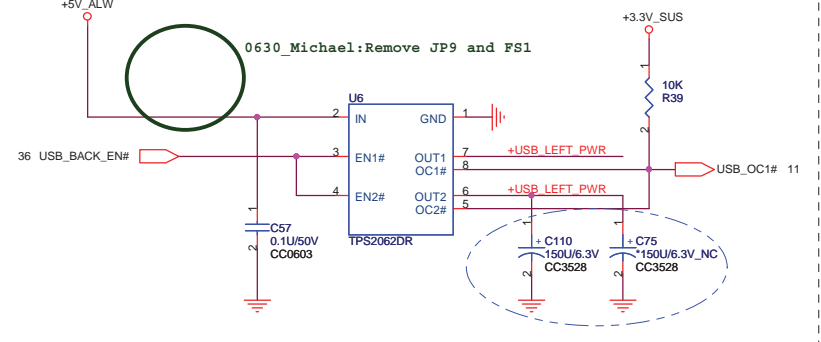
0318-Sun_change left USB port from port1 to port0



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

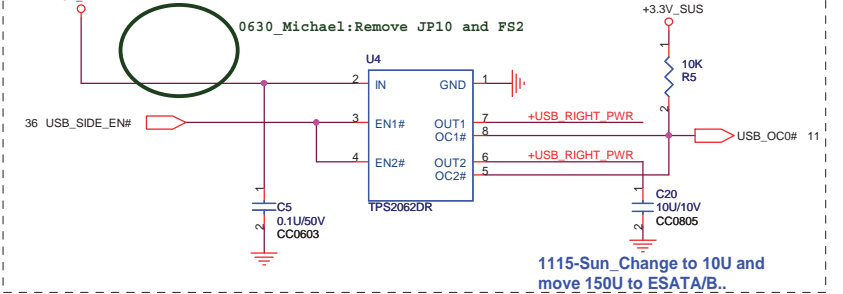


USB POWER SW Place one 150uF cap by each USB connector. Each channel is 1A



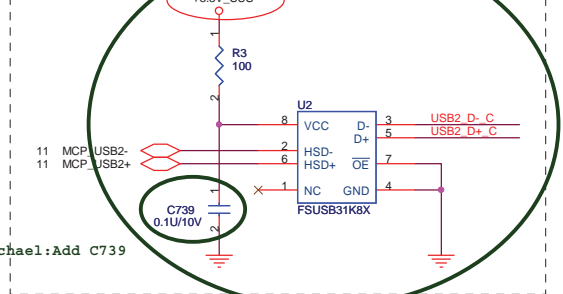
0111-Stanley: Change BOM from to 6.3V_3528.

USB POWER SW Place one 150uF cap by each USB connector. Each channel is 1A IM3 dedicated.



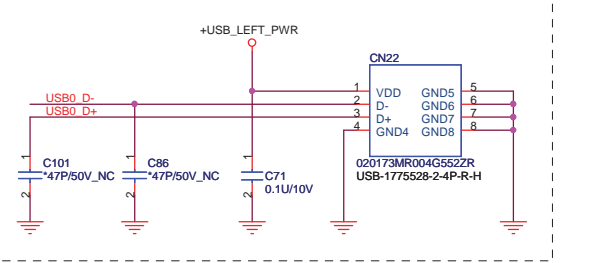
1115-Sun_Change to 10U and move 150U to ESATA/B..

USB BUS SW



0630 Michael: Modify Connect pin define
pin1=NC
pin2=HSD-
pin3=D-
pin5=D+
pin6=HSD+
pin7=OE

USB CONN



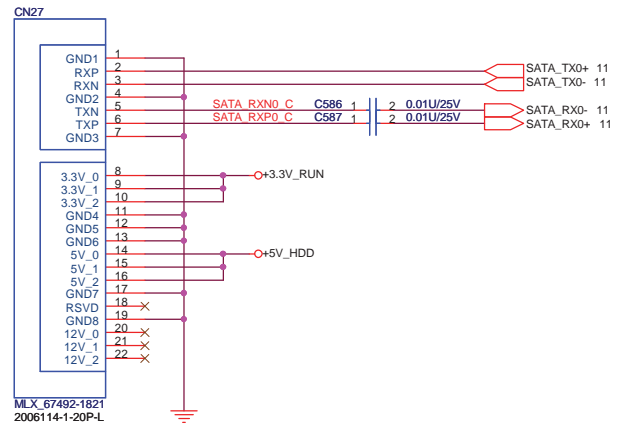
QUANTA COMPUTER

Title: USB, eSATA

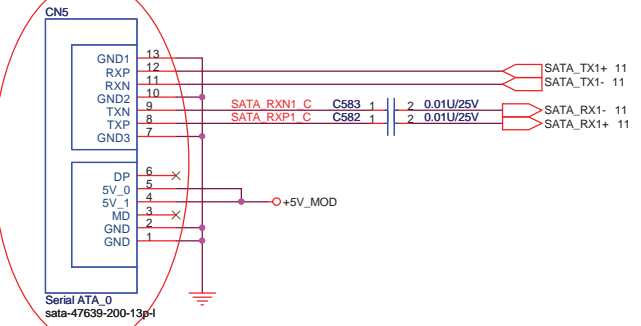
Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Thursday, September 11, 2008 Sheet 30 of 59

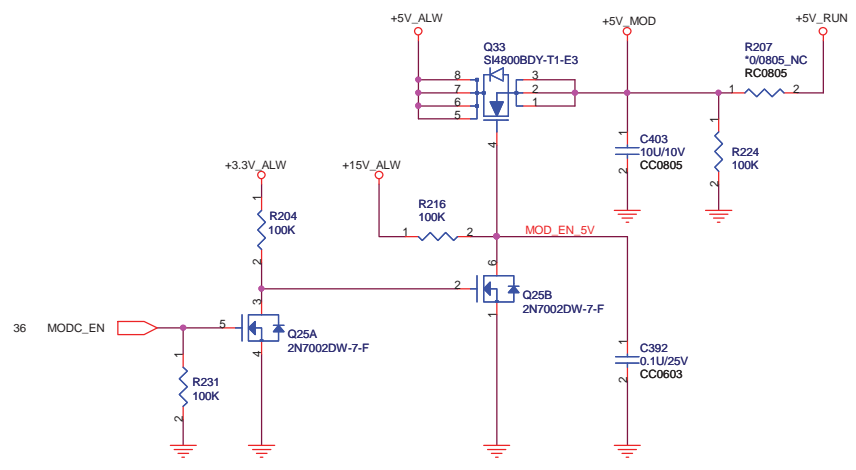
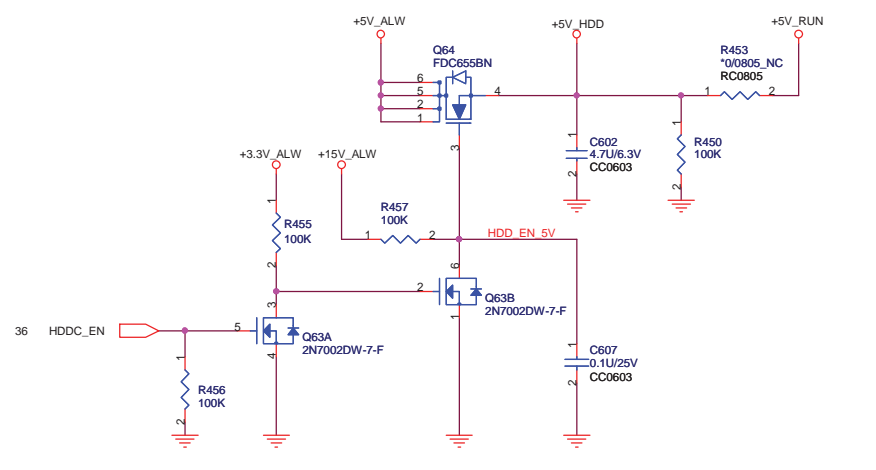
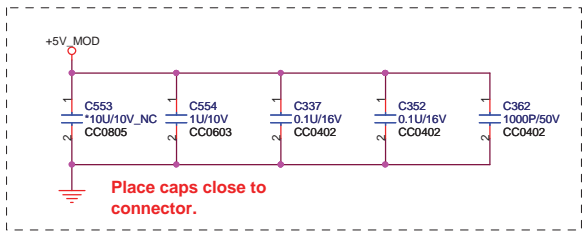
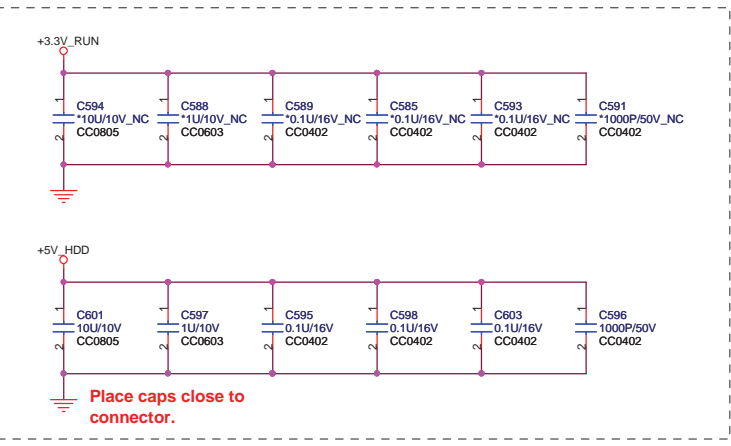
SATA HDD Connector



SATA ODD Connector

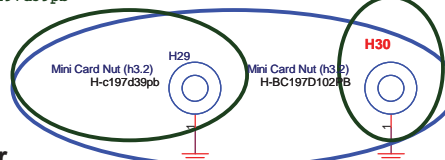


0306-Sun_Change to new footprint_sata-47639-200-13p-I
0407-Sun_Swap pin assignment due to pin direction is reversed



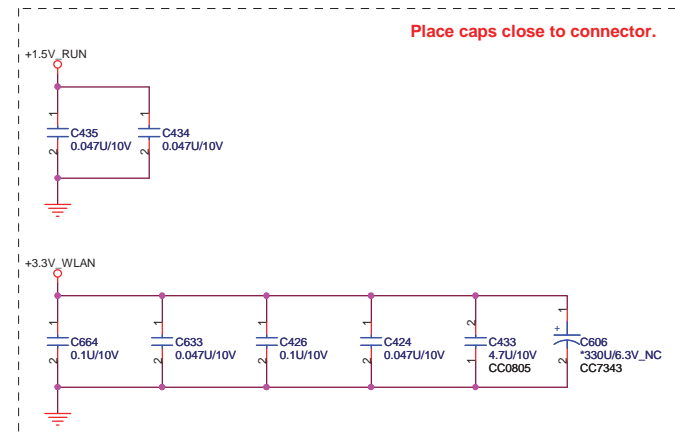
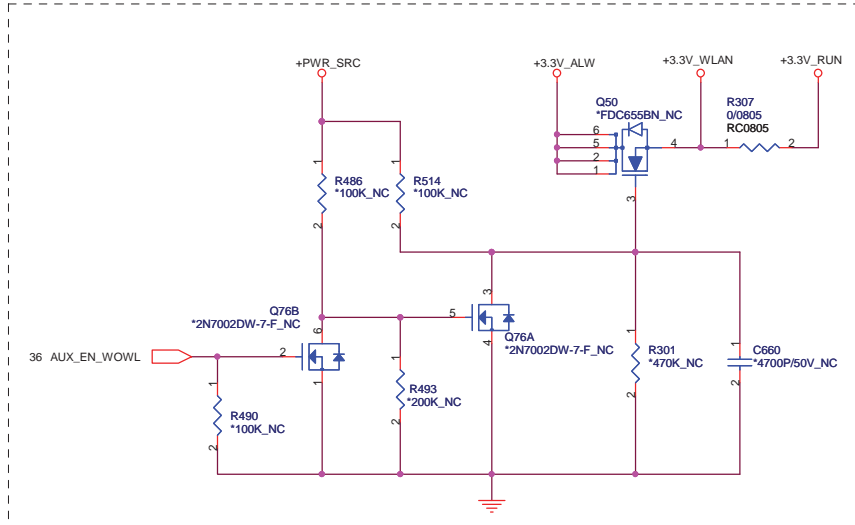
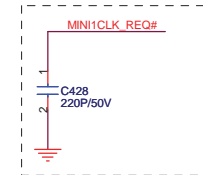
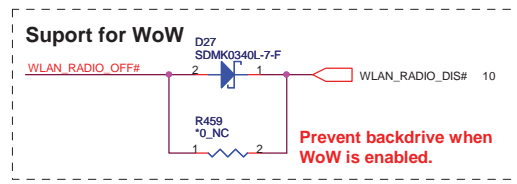
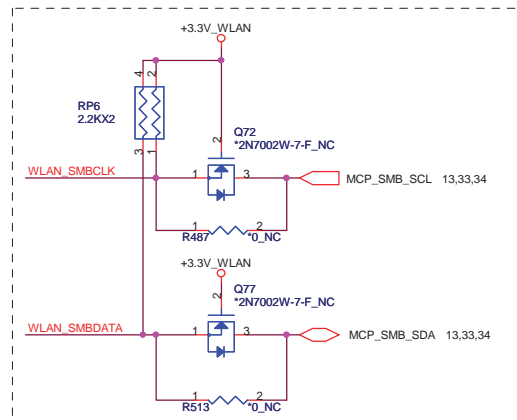
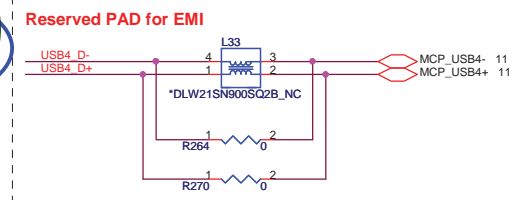
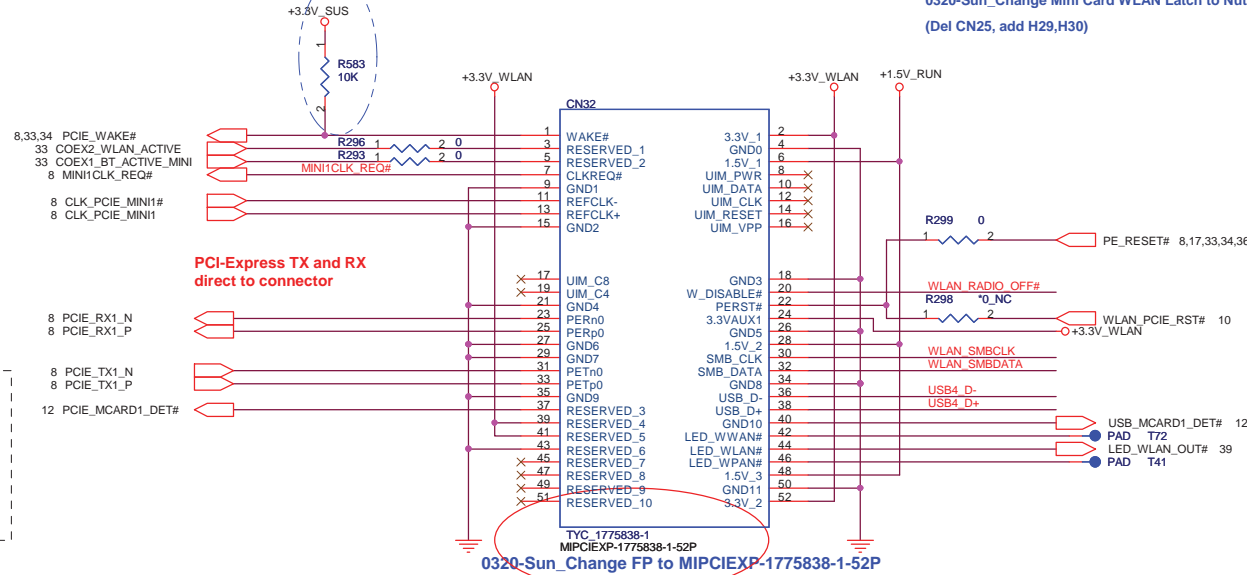
0829_Michael:Change Footprint from H-C197PB to H-c197d39pb

0616_Michael:Change footprint



MiniCard WLAN Connector

0320-Sun_Change Mini Card WLAN Latch to Nut
(Del CN25, add H29,H30)



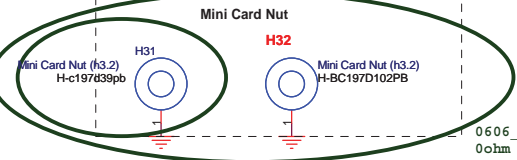
QUANTA COMPUTER

Title: MINI-CARD (WLAN)

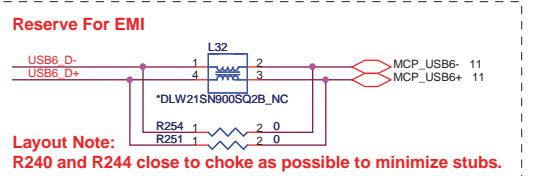
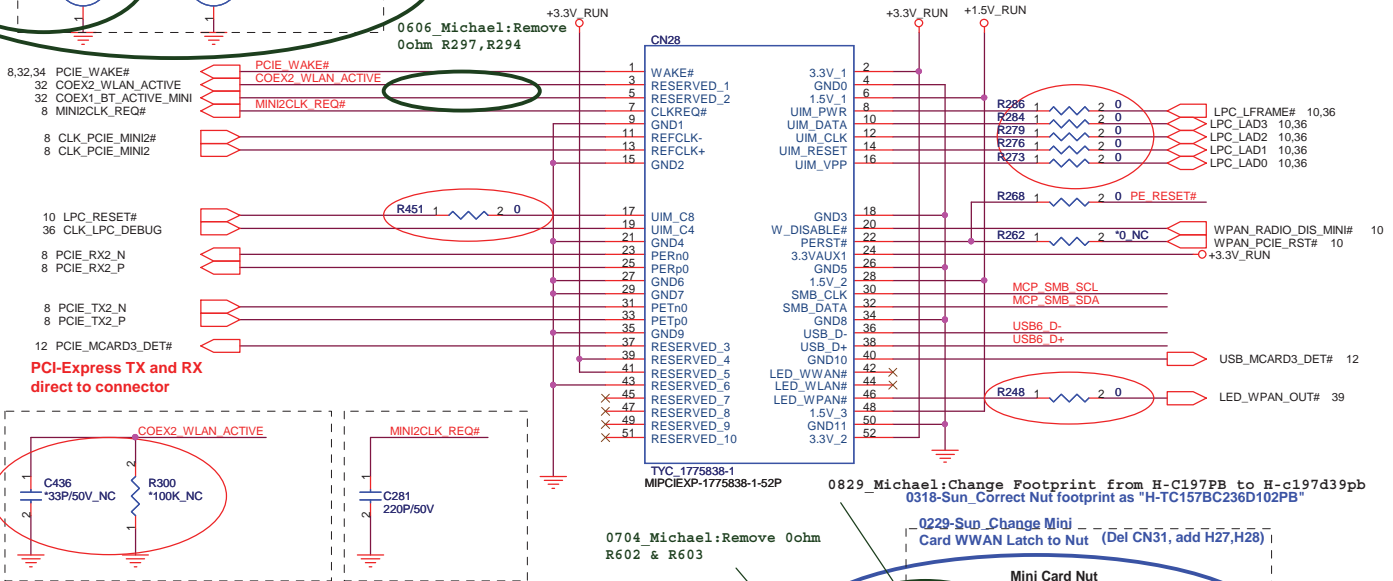
Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Thursday, October 23, 2008 Sheet 32 of 59

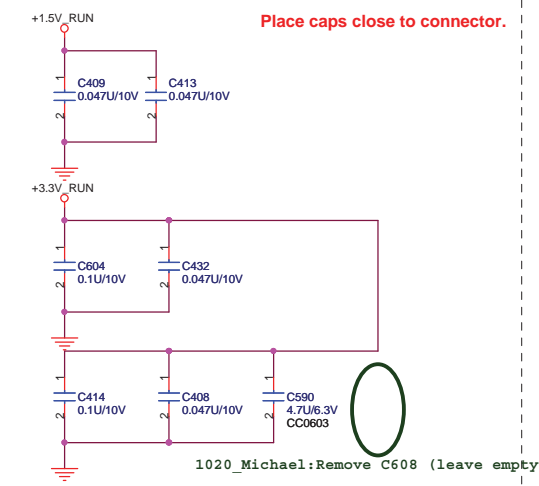
0829_Michael:Change Footprint from H-C197PB to H-c197d39pb
0605_Michael: Del MiniCard WPAN latch add Nut H31,H32



MiniCard Robson, BT. UWB Connector



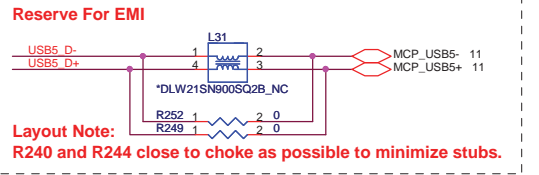
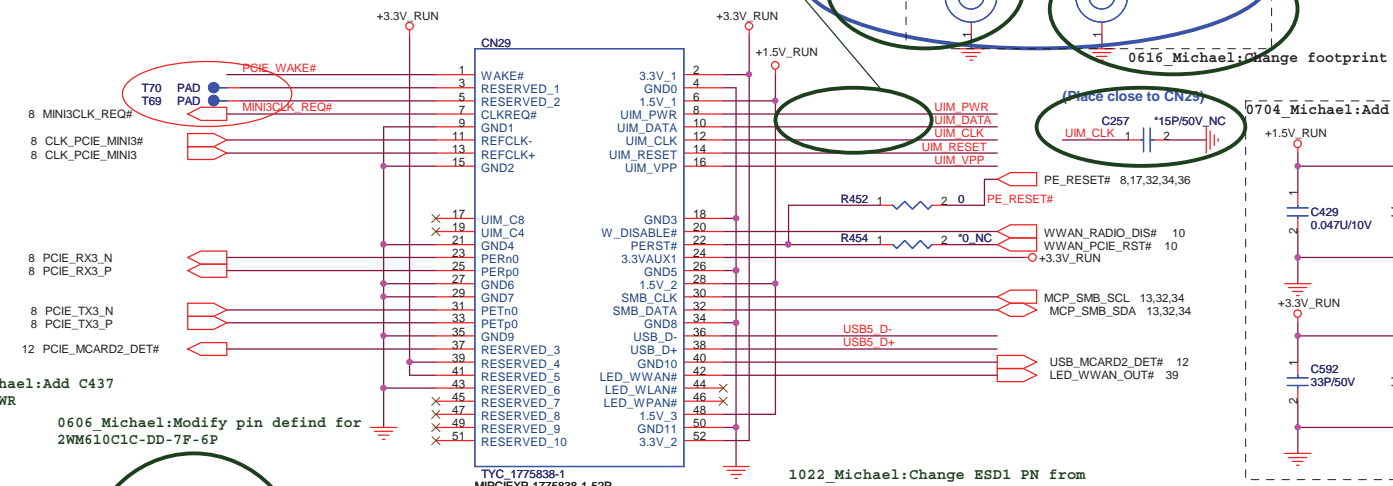
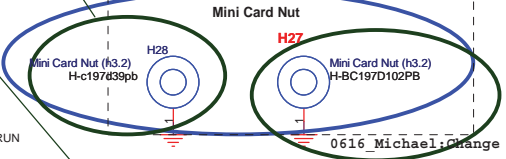
Layout Note: R240 and R244 close to choke as possible to minimize stubs.



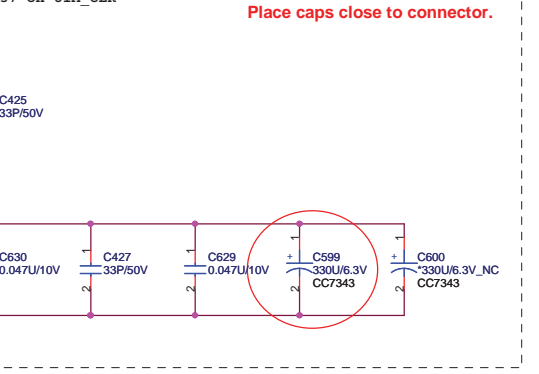
Place caps close to connector.

1020_Michael:Remove C608 (leave empty)

MiniCard WWAN Connector



Layout Note: R240 and R244 close to choke as possible to minimize stubs.

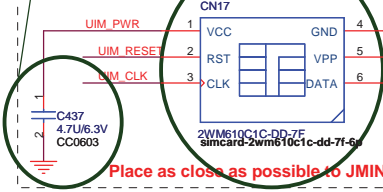


Place caps close to connector.

0704_Michael:Add C437 on UIM_PWR

0606_Michael:Modify pin defind for 2WM610C1C-DD-7F-6P

1022_Michael:Change ESD1 PN from ALSRV054011-to-ALB04220007-for EOL

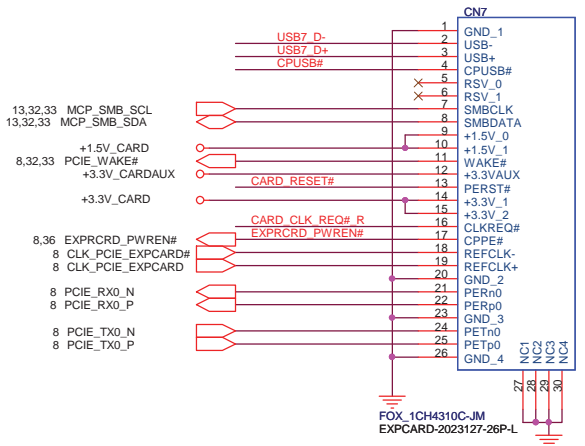


Place as close as possible to JMINI connector

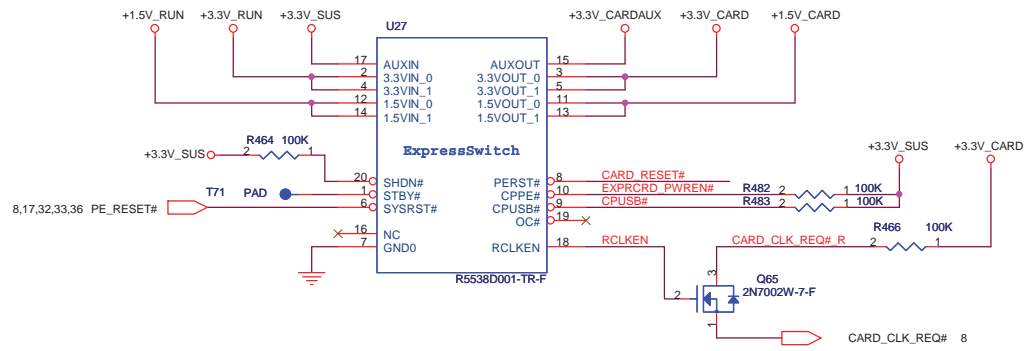


Title MINI-CARD (WWAN,WPAN)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Thursday, October 23, 2008	Sheet 33 of 59

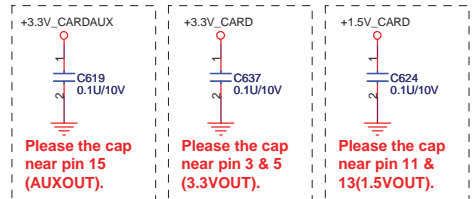
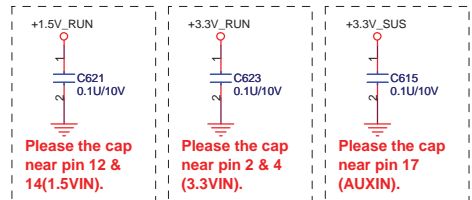
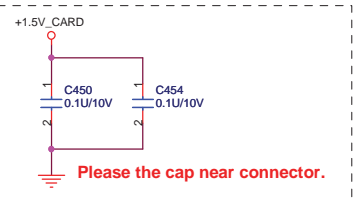
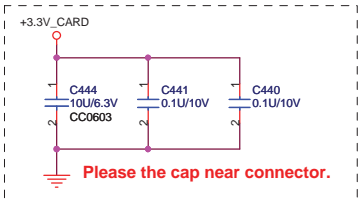
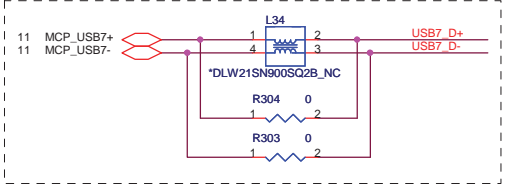
Express Card

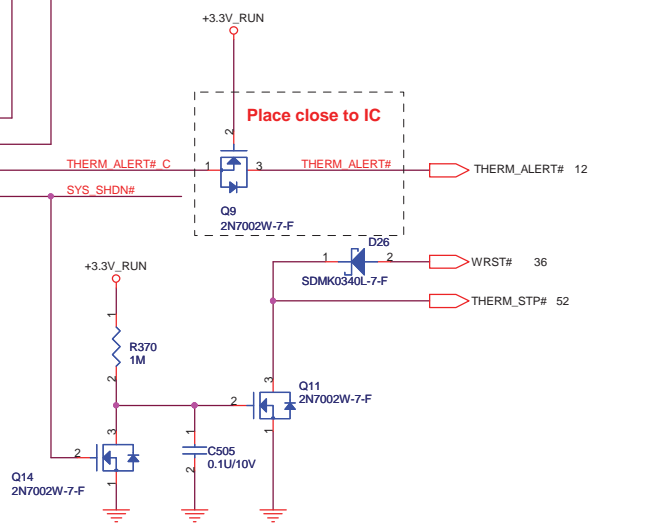
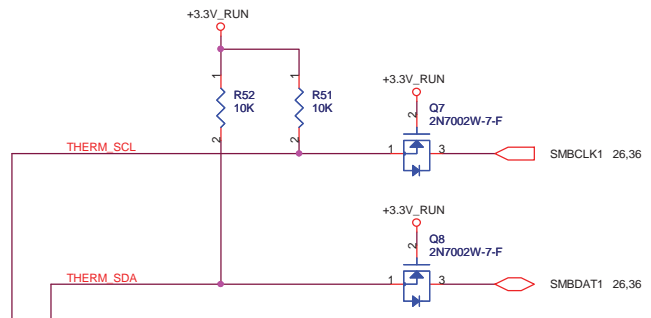
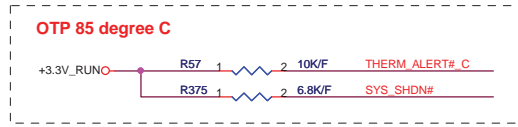
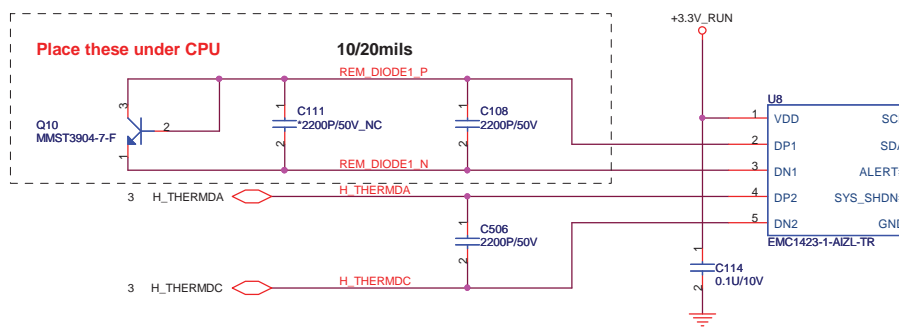
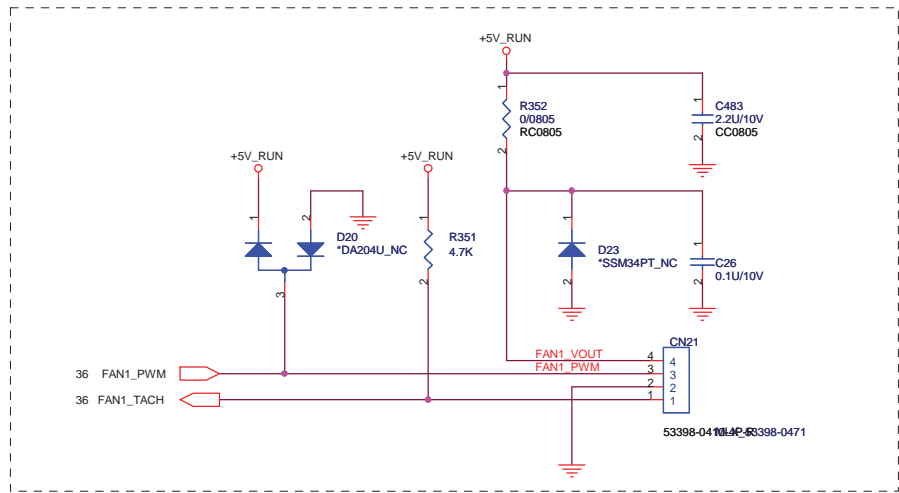


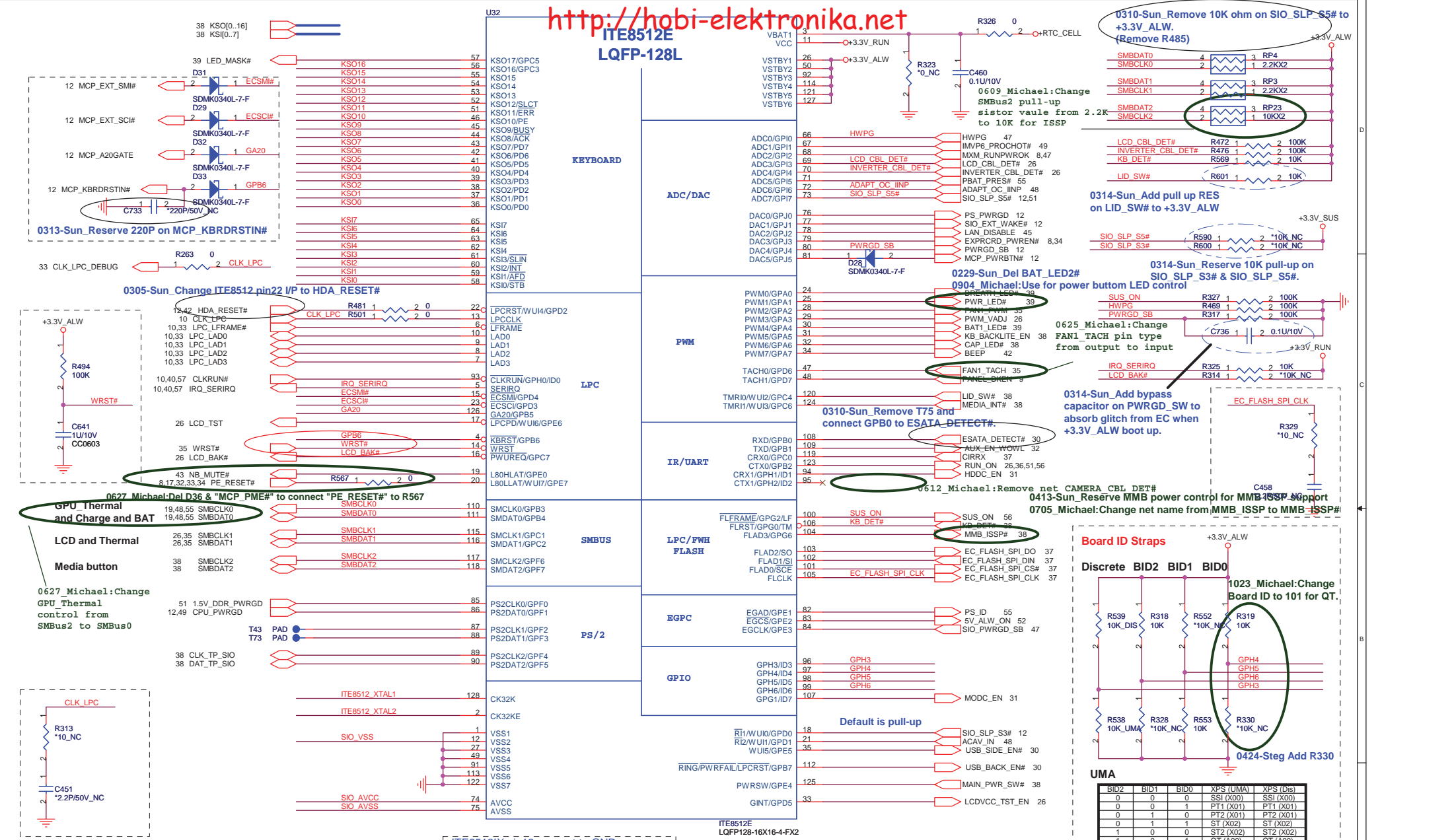
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.







BID2	BID1	BID0	XPS (UMA)	XPS (DS)
0	0	0	SSI (X0)	SSI (X0)
0	0	1	PT1 (X0)	PT1 (X0)
0	1	0	PT2 (X0)	PT2 (X0)
0	1	1	ST (X0)	ST (X0)
1	0	0	ST2 (X0)	ST2 (X0)
1	0	1	QT (A0)	QT (A0)

VGA_IDENTIFY : USB_SIDE_EN#
1 = Discrete Gfx / 0 = UMA

QUANTA COMPUTER

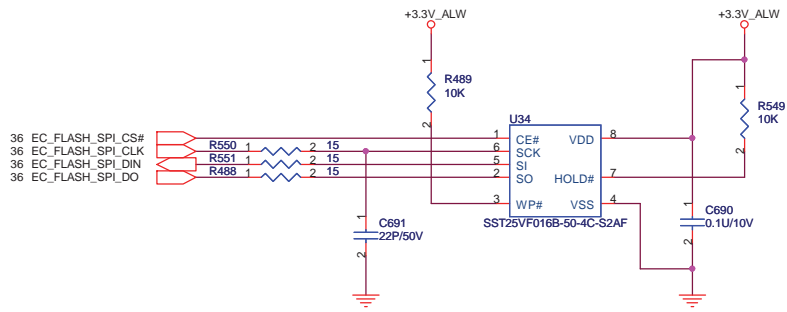
Title: SIO(ITE8512)

Size: Document Number IM3 (XPS-Joie) Rev 2A

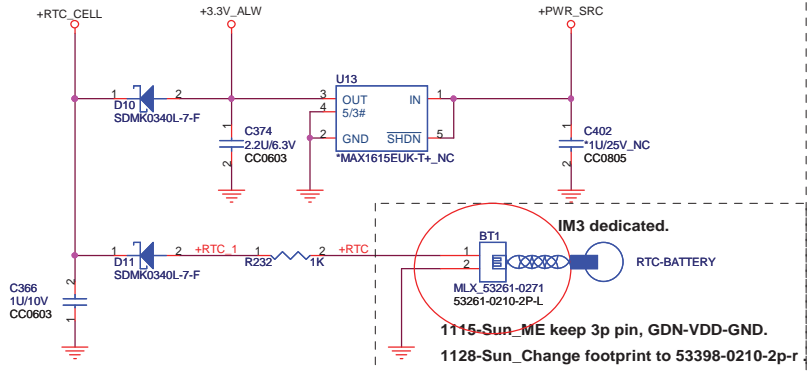
Date: Thursday, October 23, 2008 Sheet 36 of 59

Place these caps close to ITE8512.

16Mbit (2M Byte), SPI

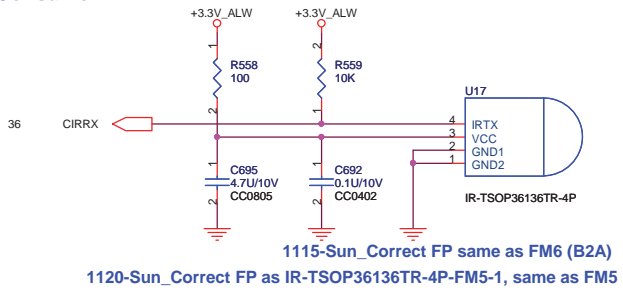


RTC BATTERY



BT1 IM3 dedicated.
MLX_53261-0271
53261-0210-2P-L
1115-Sun_ME keep 3p pin, GDN-VDD-GND.
1128-Sun_Change footprint to 53398-0210-2p-r

Consumer IR

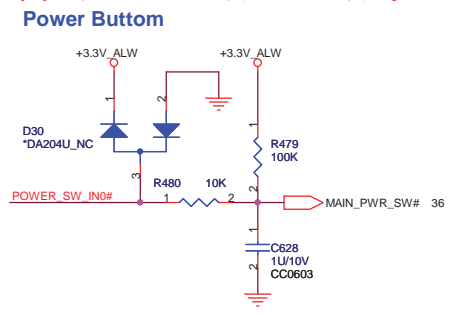


1115-Sun_Correct FP same as FM6 (B2A)
1120-Sun_Correct FP as IR-TSOP36136TR-4P-FM5-1, same as FM5

0605_Michael: Change CN6 from 32pin to 28pin but need to check footprint and PN

BREATH_PWRLED_BOT:
 Solid = System On, Normal Activity, "Breathing" = System in Standby; Off = System Off (or in Hibernation)

0420 Michael: Add KB detect function
 1023 Michael: Disable KB LED function
 depop R722 and change R723 from 200K to 0 ohm



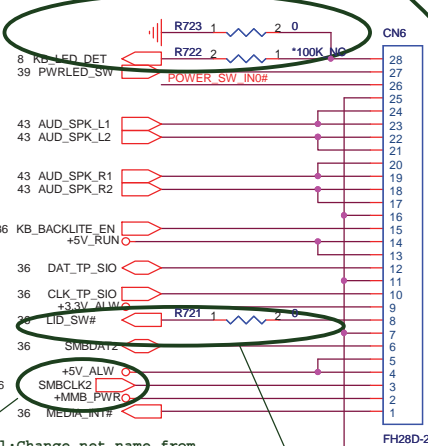
Power Button

Speaker

KB LED

Touch Pad

Media Button

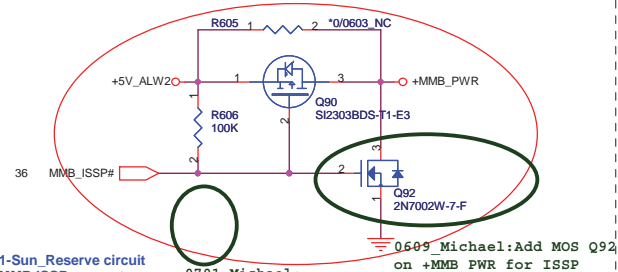


0909 Michael: Remove LID_SW# and connector to GND

0624 Michael: Change net name from +5V_ALW2 to +MMB_PWR
 0704 Michael: Swap SMBCLK2 and +MMB_PWR for Ass'y issue

0825 Michael: Add KB detect function
 0911 Michael: Change pin from 16 to 8
 0918 Michael: Return to LID_SW#

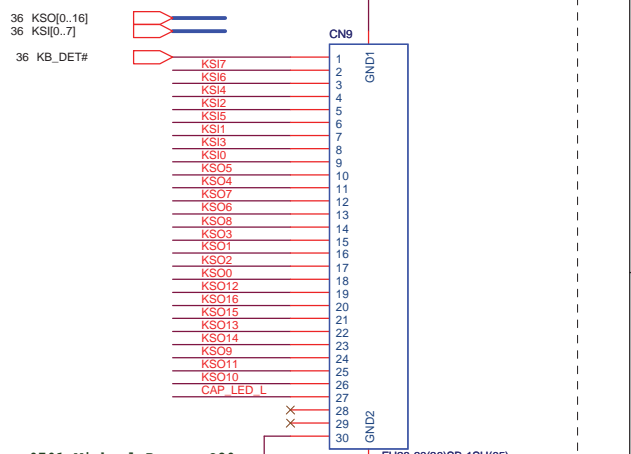
0411-Sun_Reserve circuit for MMB ISSP support
 0414-Sun_Change MOSFET control voltage level



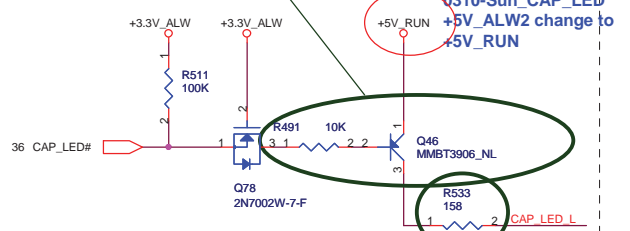
0609 Michael: Add MOS Q92 on +MMB_PWR for ISSP

0701 Michael: Remove Q91 for ISSP

KEYBOARD CONNECTOR



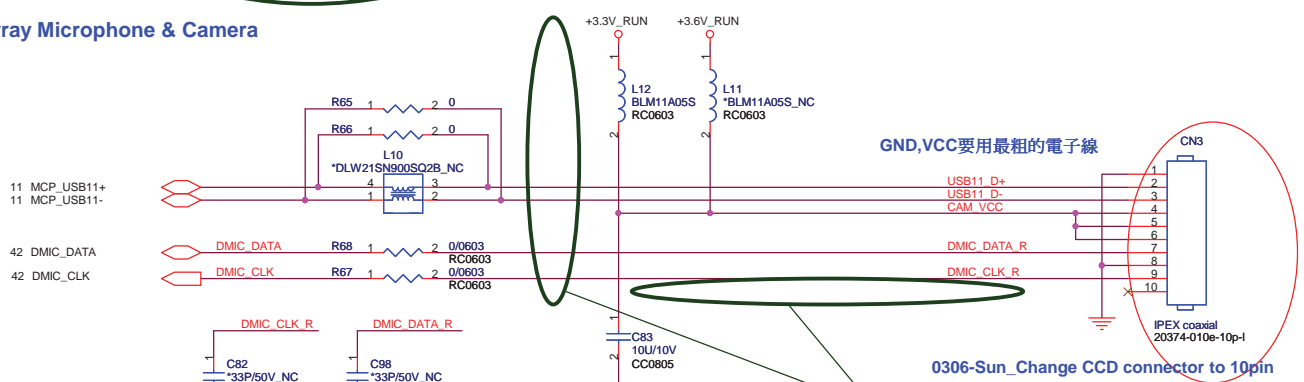
0701 Michael: Remove Q80 and add Q46 & R491 for leakage issue on S3



0310-Sun_CAP_LED +5V_ALW2 change to +5V_RUN

1022 Michael: Change R533 from 2.49K to 158ohm for LED brightness

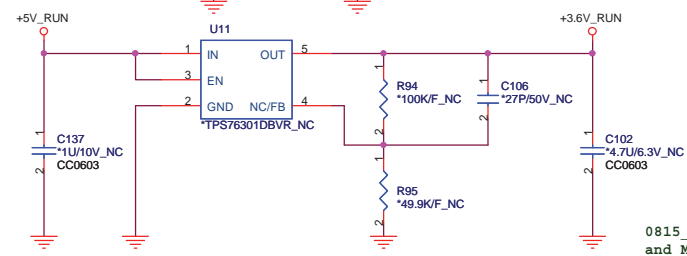
Array Microphone & Camera



GND,VCC要用最粗的电子线

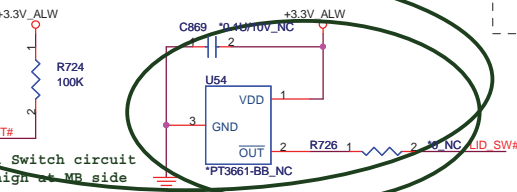
0306-Sun_Change CCD connector to 10pin

0612 Michael: Remove CAMERA DET circuit, R64 pull-up to +3.3V_RUN and connector to U32 pin95

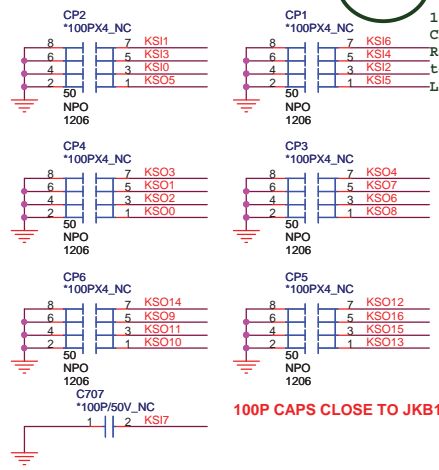


0815 Michael: Add Hall Switch circuit and MEDIA_INT# pull-high at MB side

Hall Switch



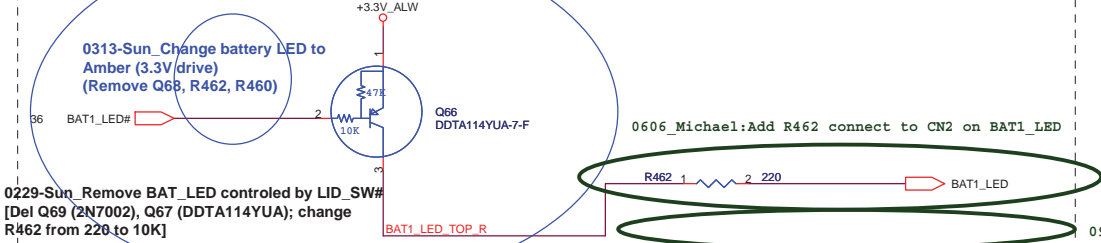
1023_Michael: Depop LID_Switch function on MB side



100P CAPS CLOSE TO JKB1

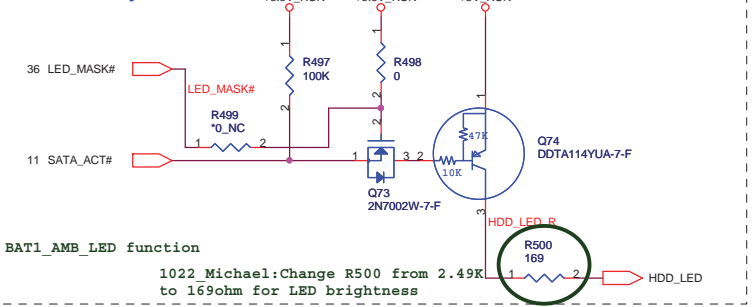


Battery status

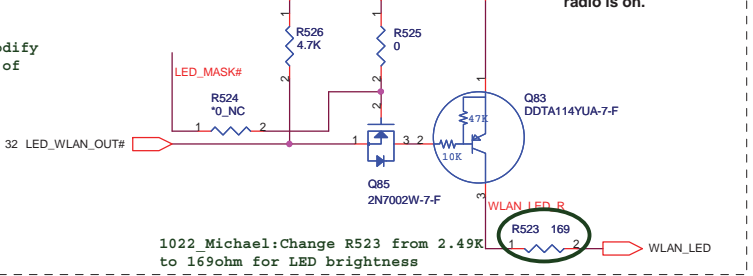


0229-Sun_Del BAT_LED2 [Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

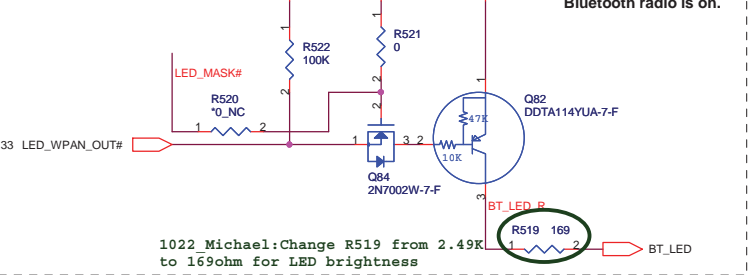
HDD Activity LED



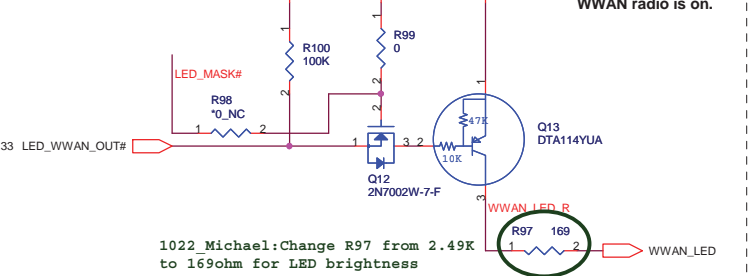
WLAN



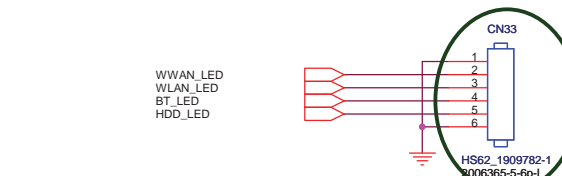
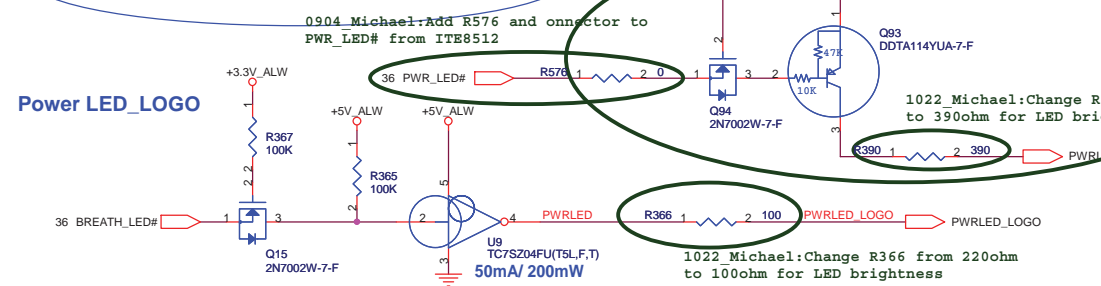
BT / UWB LED



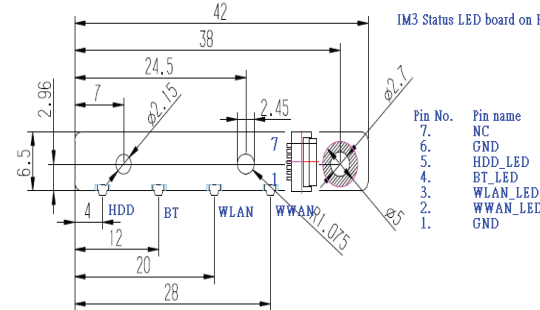
WWAN



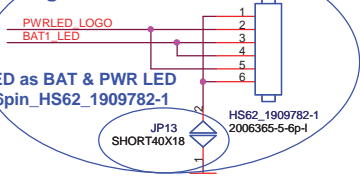
0229-Sun_Change PWRLED_SW control same as PWRLED_LOGO [Del U10 (TC7S204F), Q16 (2N7002)]



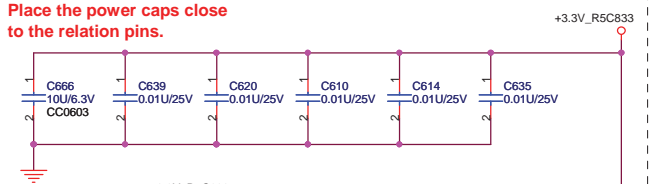
0229-Sun_Remove LED control by LID_SW# (Del R478,R477,Q75)



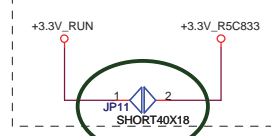
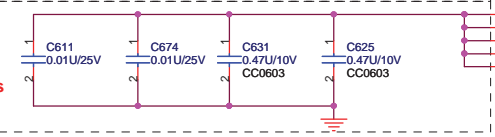
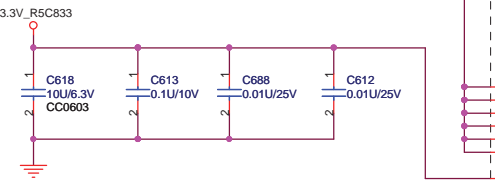
Logo LED/B connector



Place the power caps close to the relation pins.

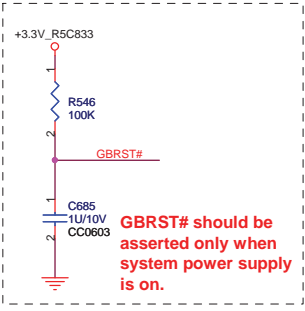
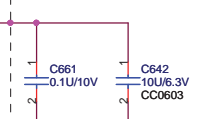


Please place capacitors for VCC_ROUTx as close to R5C833 as possible.

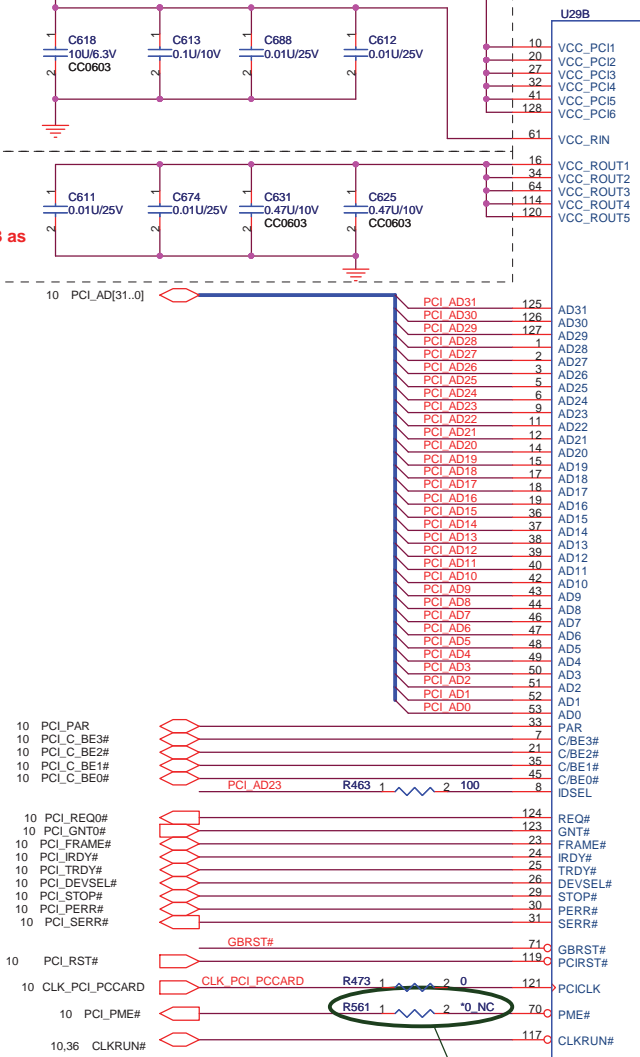
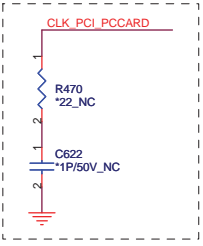


0606_Michael:Change footprint from 0ohm R468 to normal short type JP11 (short40x18)

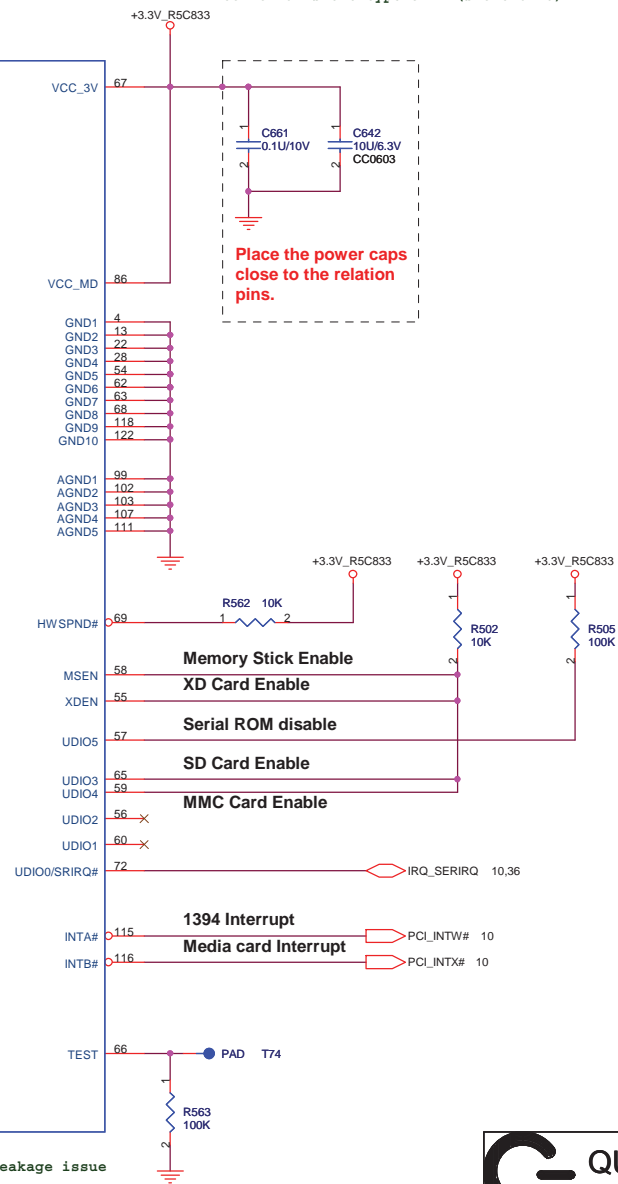
Place the power caps close to the relation pins.



GBRST# should be asserted only when system power supply is on.



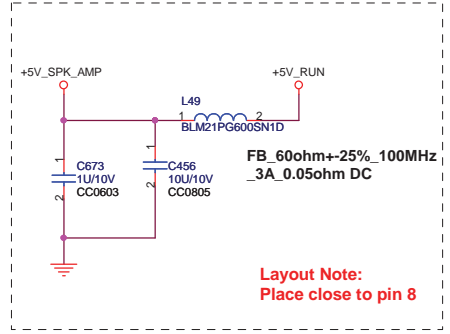
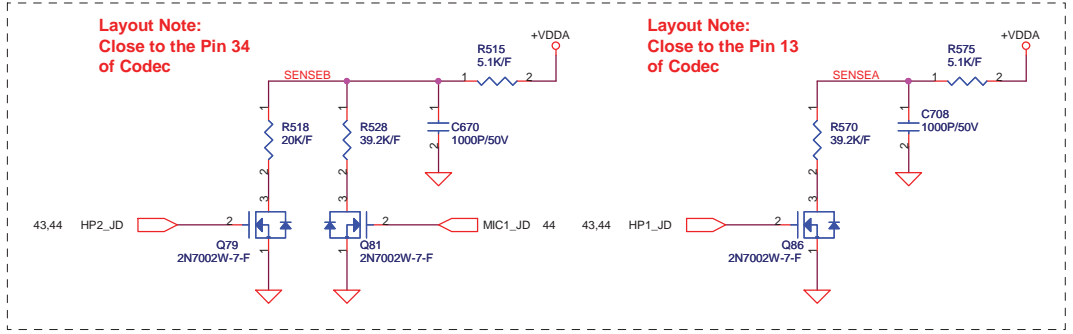
PCI / OTHER



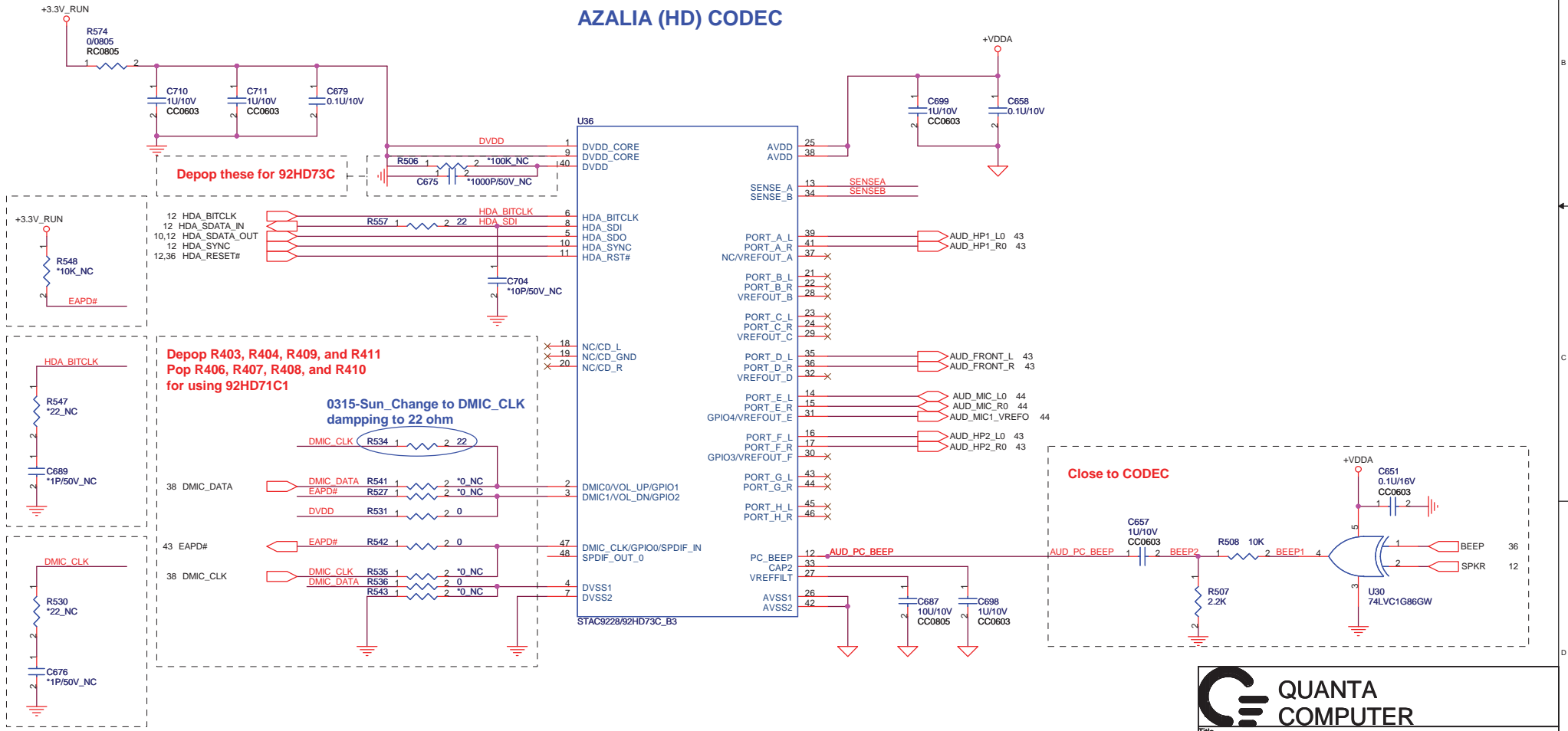
0630_Michael:Remove Mini PCI CN8 and circuit

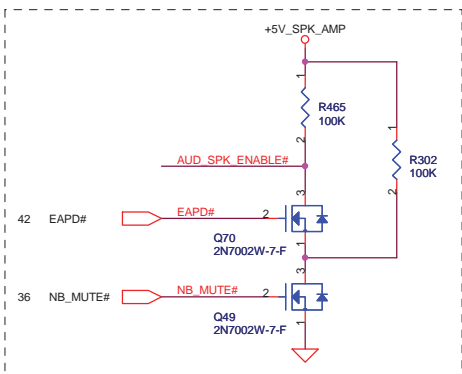
0707_Michael:Depop R561 for leakage issue



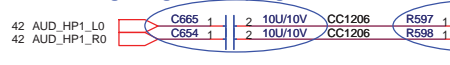


AZALIA (HD) CODEC





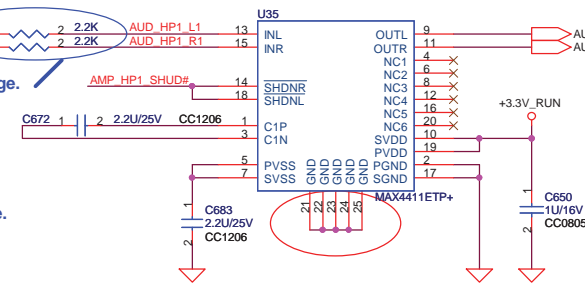
0315-Sun_Improve Dynamic Range.
0320-StegeChange AC coupling to 10U/10V



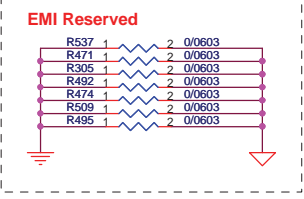
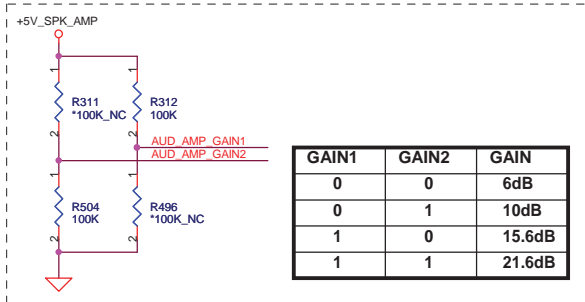
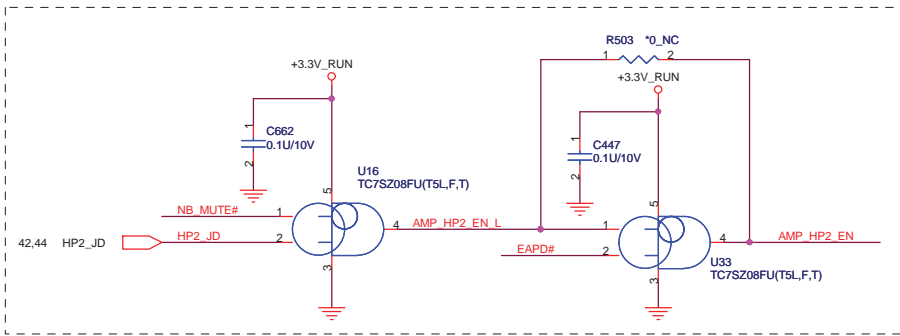
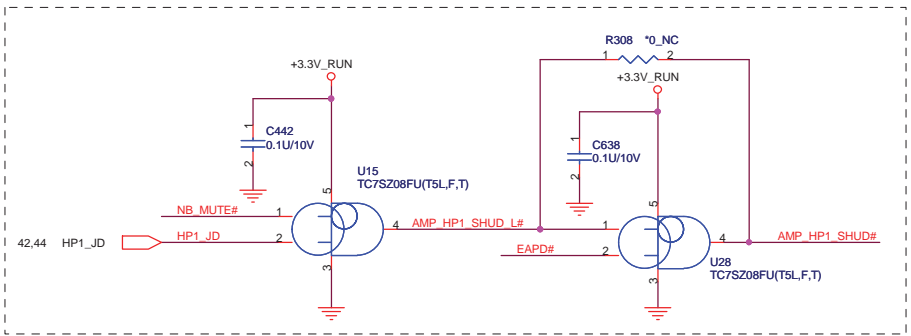
0310-Sun_Improve Dynamic Range.
Add R597,R598 w/2.2K



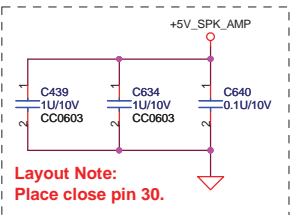
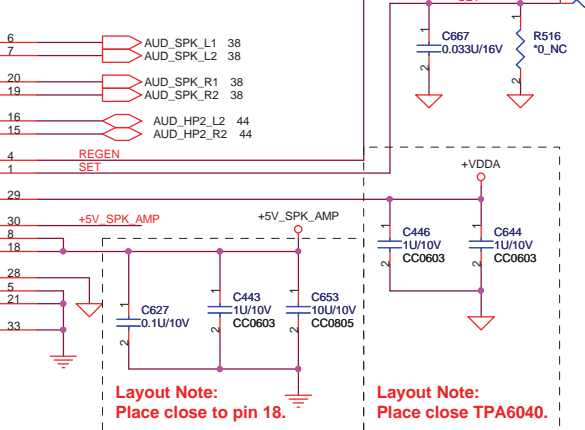
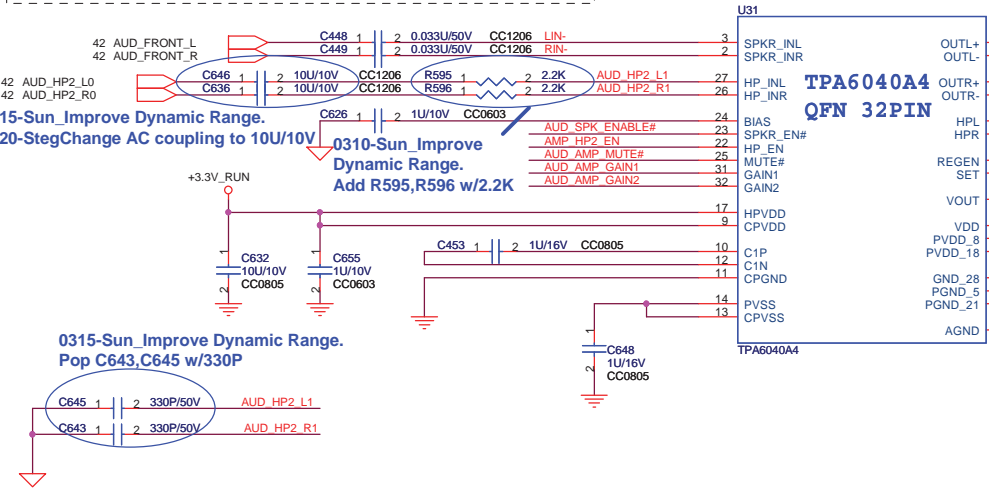
0315-Sun_Improve Dynamic Range.
Pop C452,C455 to 330P



Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



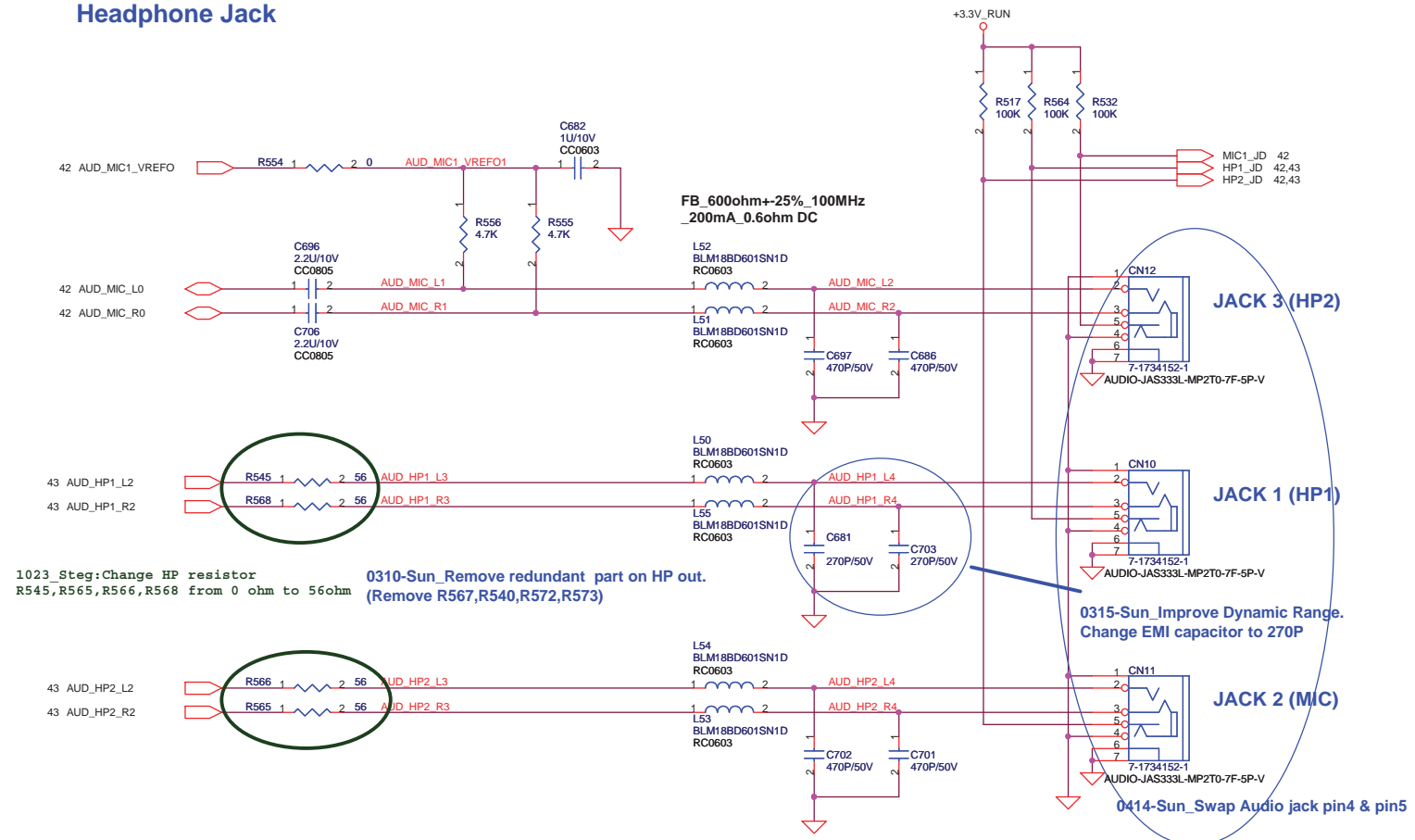
Layout Note:
Place close pin 30.

Layout Note:
Place close to pin 18.

Layout Note:
Place close TPA6040.



Headphone Jack




1023_Step: Change HP resistor
R545, R565, R566, R568 from 0 ohm to 56ohm

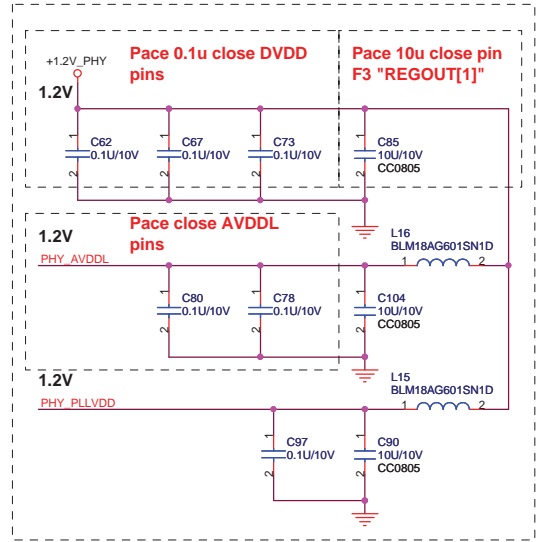
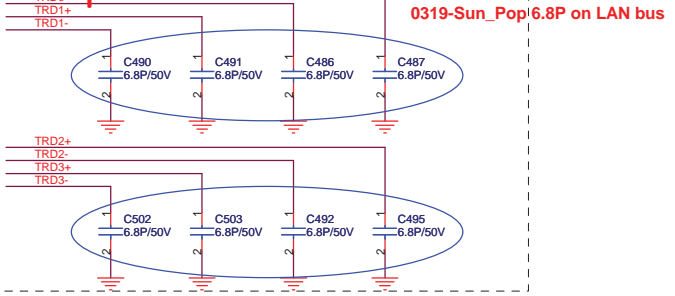
0310-Sun_Remove redundant part on HP out.
(Remove R567, R540, R572, R573)

0315-Sun_Improve Dynamic Range.
Change EMI capacitor to 270P

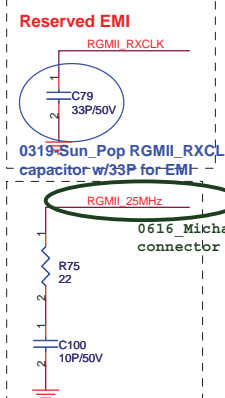
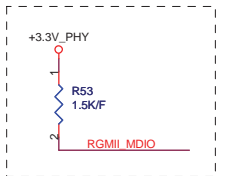
0414-Sun_Swap Audio jack pin4 & pin5

 QUANTA COMPUTER		
Title: AUDIO CONN		
Size:	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date:	Thursday, October 30, 2008	Sheet: 44 of 59

Layout Note:
 1. Use 50 ohm impedance for all trace.
 2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
 3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.

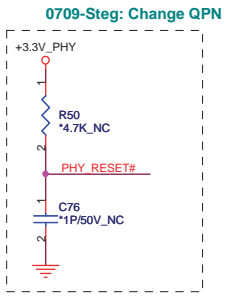


Layout Note:
 Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.

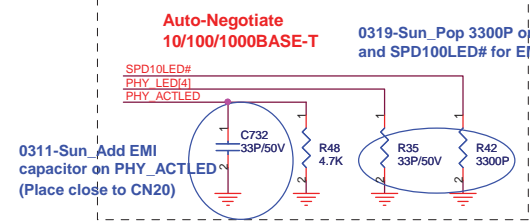
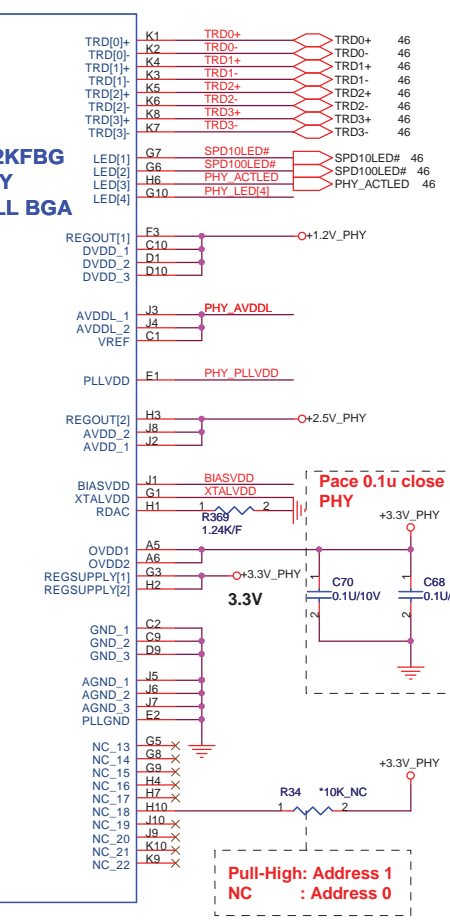
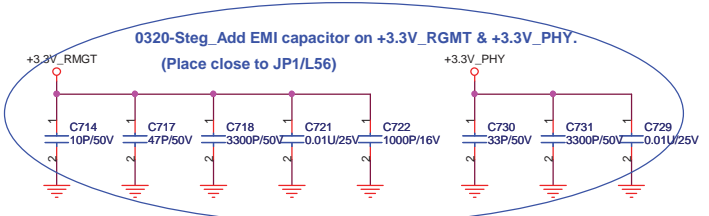
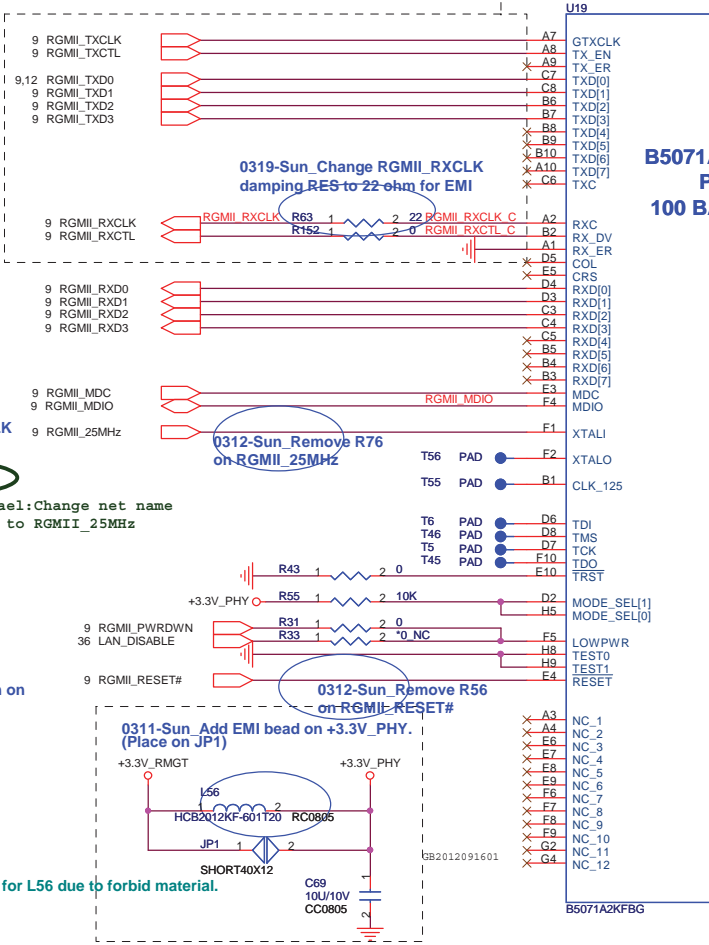


0319-Sun_Pop RGMII_RXCLK capacitor w/33P for EMI

0312-Sun_Remove R74 on PHY_XTALI.



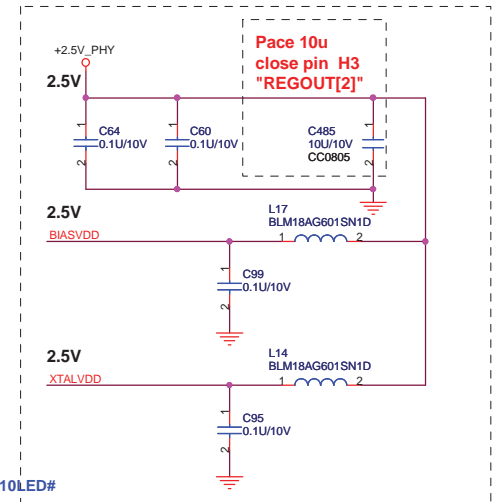
0709-Step: Change QPN for L56 due to forbid material.



0311-Sun_Add EMI capacitor on PHY_ACTLED (Place close to CN20)

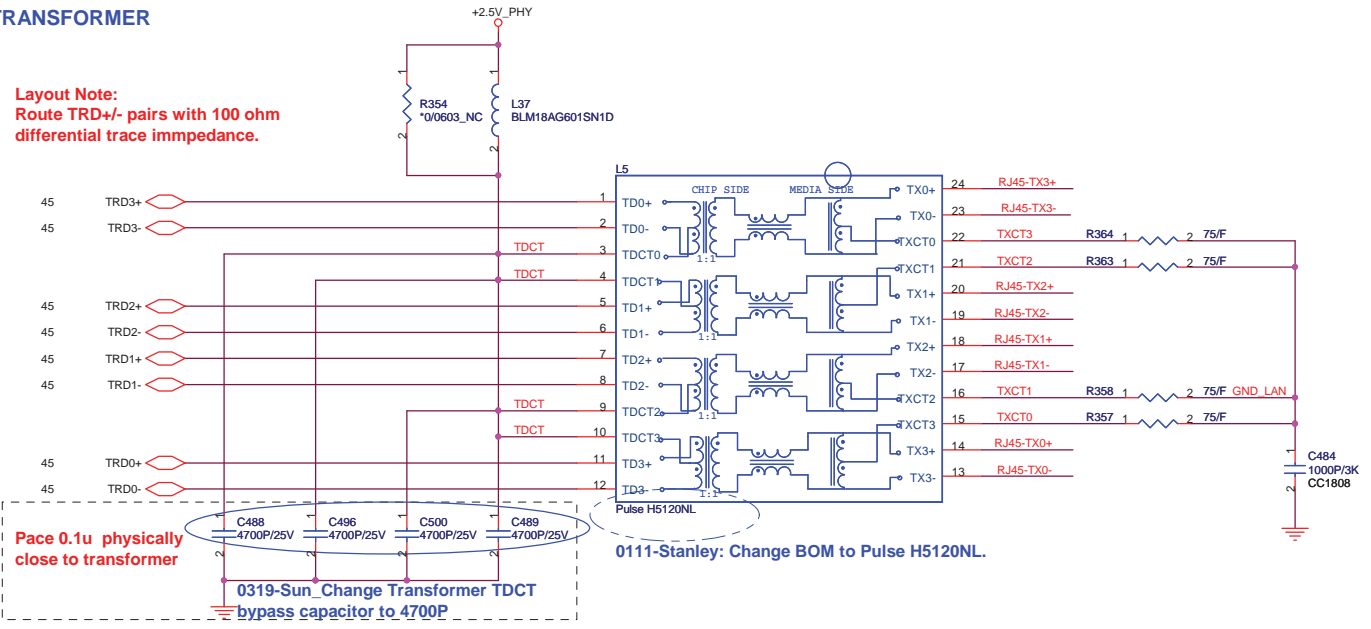
Auto-Negotiate 10/100/1000BASE-T

0319-Sun_Pop 3300P on SPD10LED# and SPD100LED# for EMI



TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



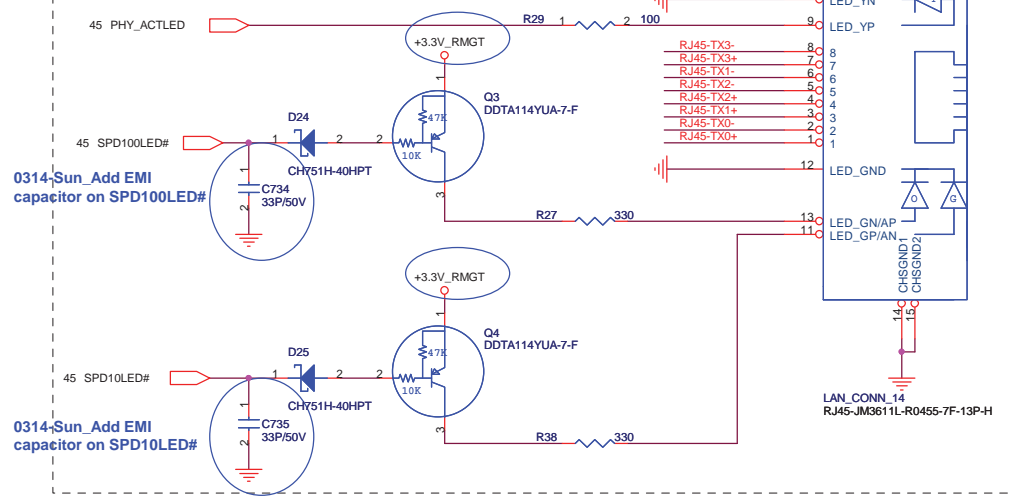
Place 0.1u physically close to transformer

0319-Sun_Change Transformer TDCT bypass capacitor to 4700P

0111-Stanley: Change BOM to Pulse H5120NL.

RJ-45 Connector

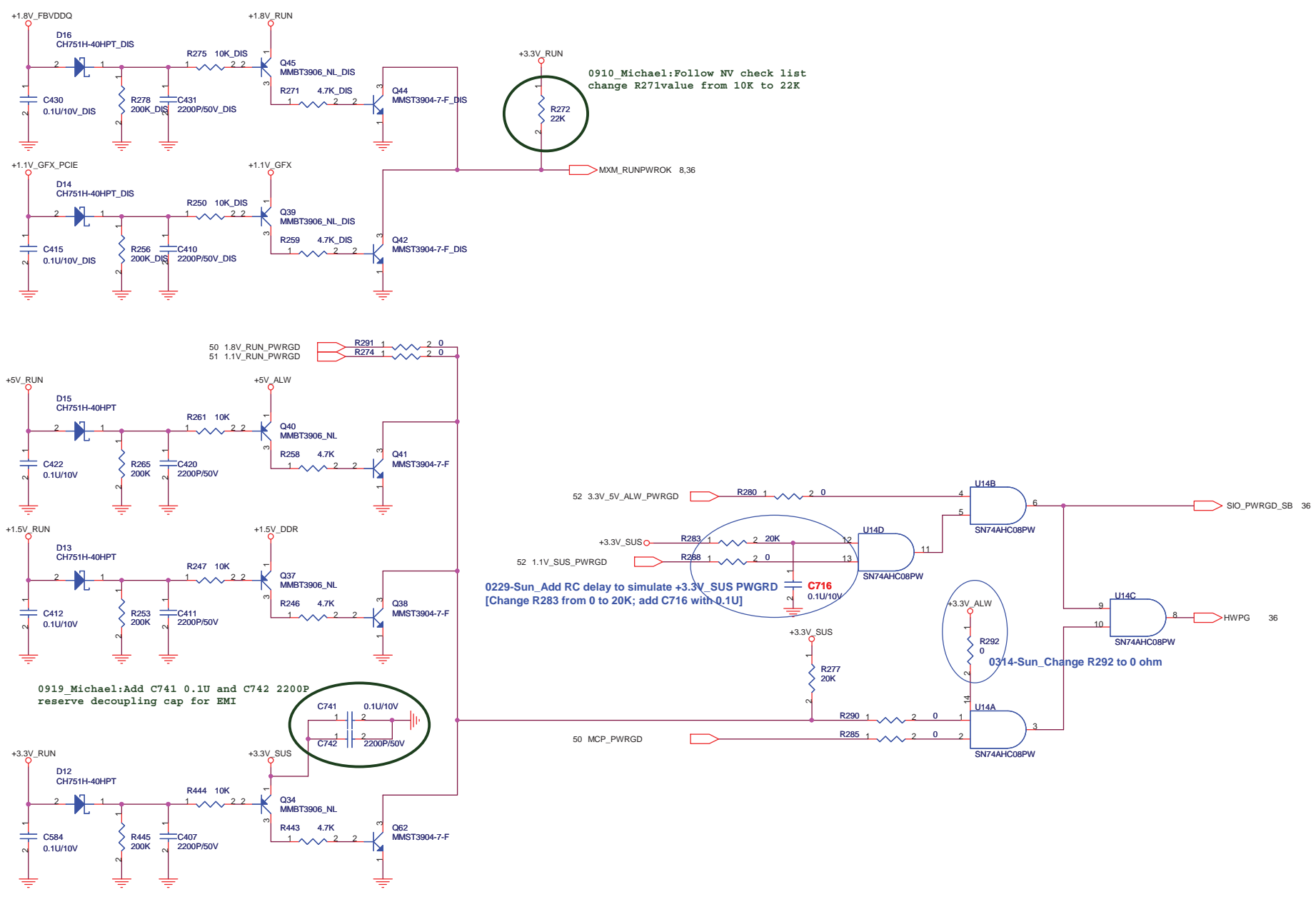
0314-Sun_Change RJ45 LED power to +3.3V_RMGT for EMI request



0314-Sun_Add EMI capacitor on SPD100LED#

0314-Sun_Add EMI capacitor on SPD10LED#





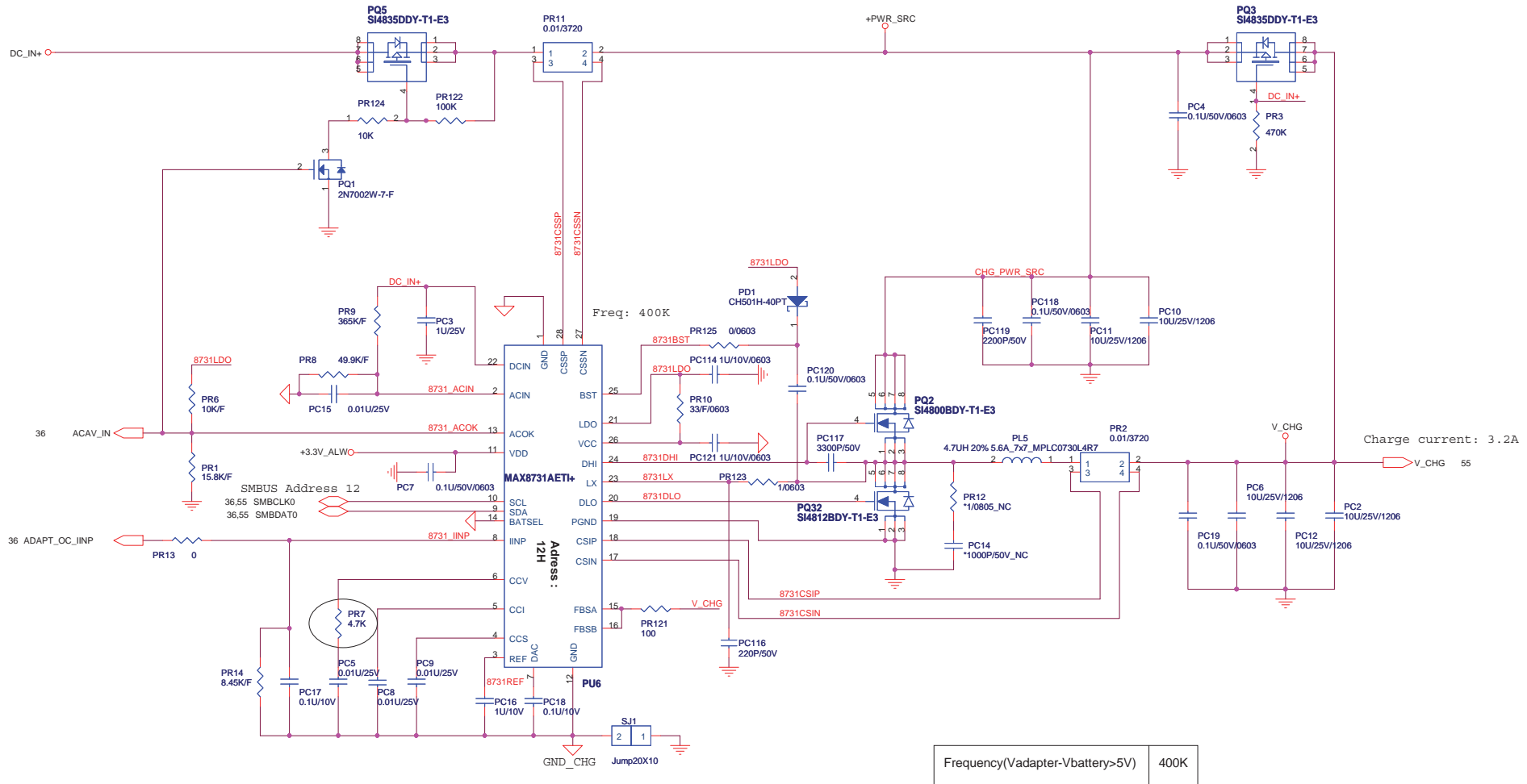
0919_Michael: Add C741 0.1U and C742 2200P reserve decoupling cap for EMI

0229-Sun_Add RC delay to simulate +3.3V_SUS PWGRD [Change R283 from 0 to 20K; add C716 with 0.1U]

0314-Sun_Change R292 to 0 ohm

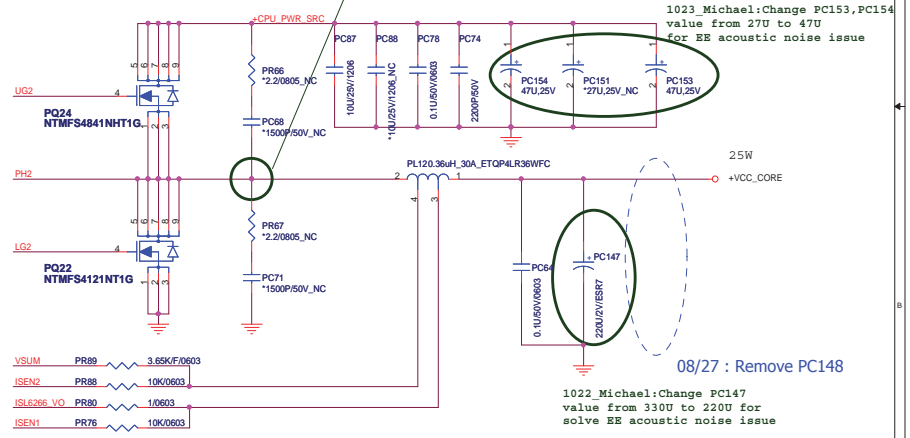
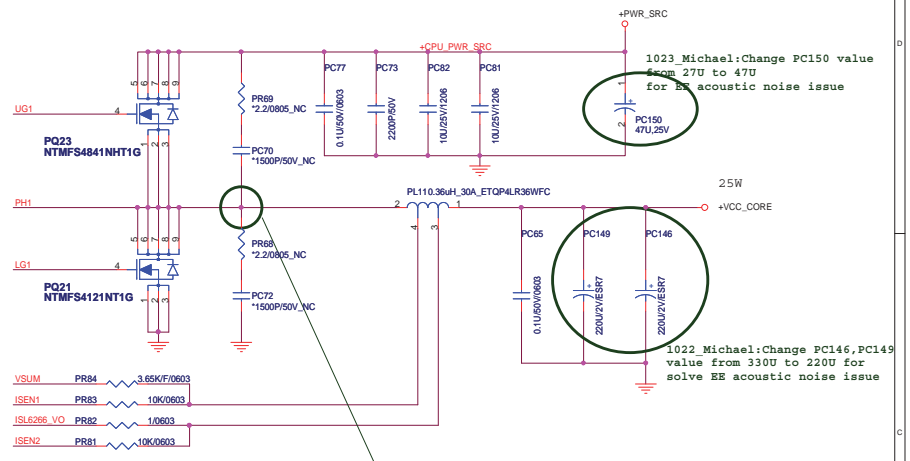
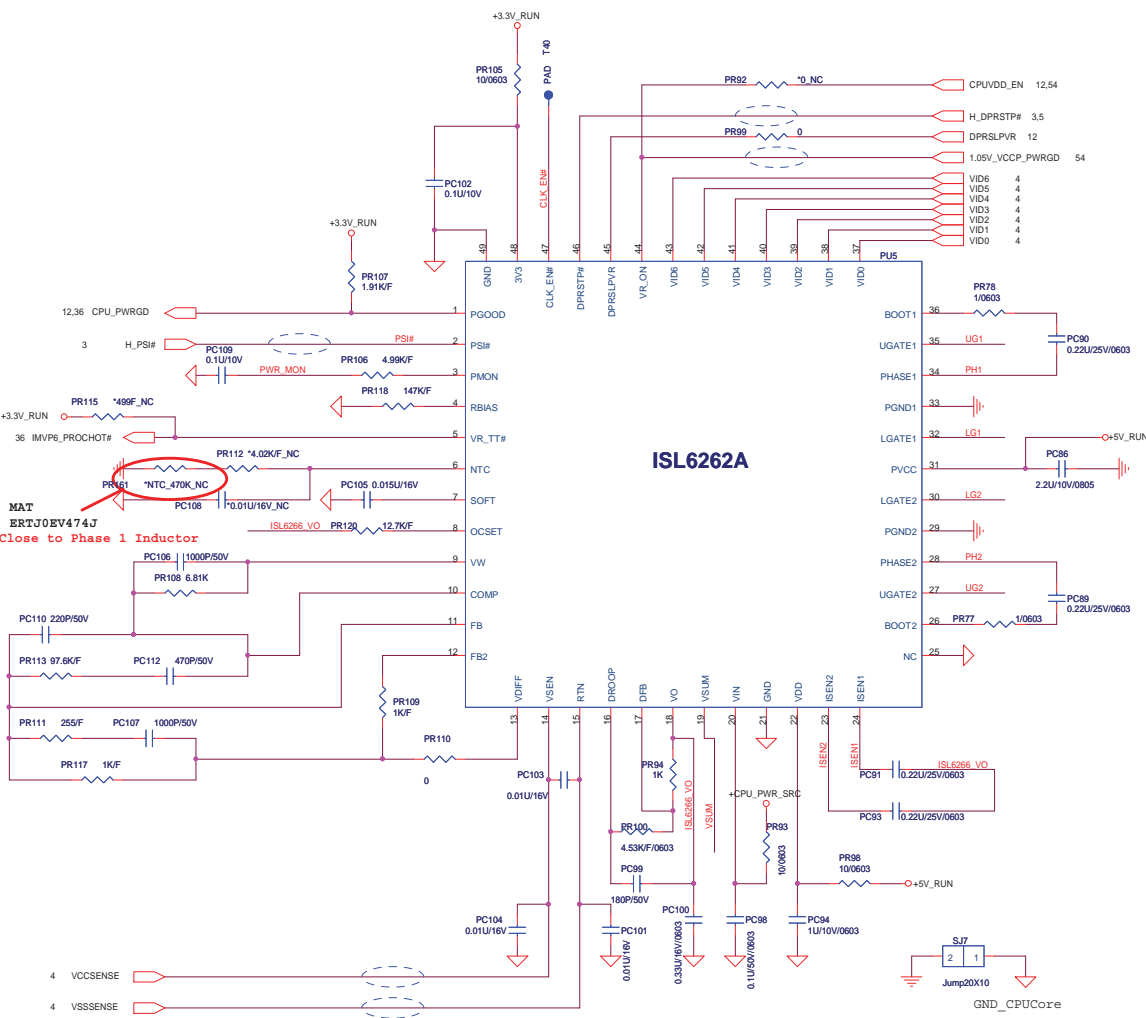


Title		
System Reset Circuit		
Size	Document Number	Rev
	IM3 (XPS-Jolie)	2A
Date:	Thursday, October 23, 2008	Sheet 47 of 59

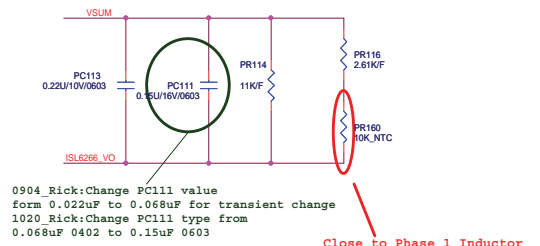


Frequency(Vadapter-Vbattery>5V) 400K

08/27 : Remove 0 ohm (PR102, PR97, PR119, PR104, PR103)



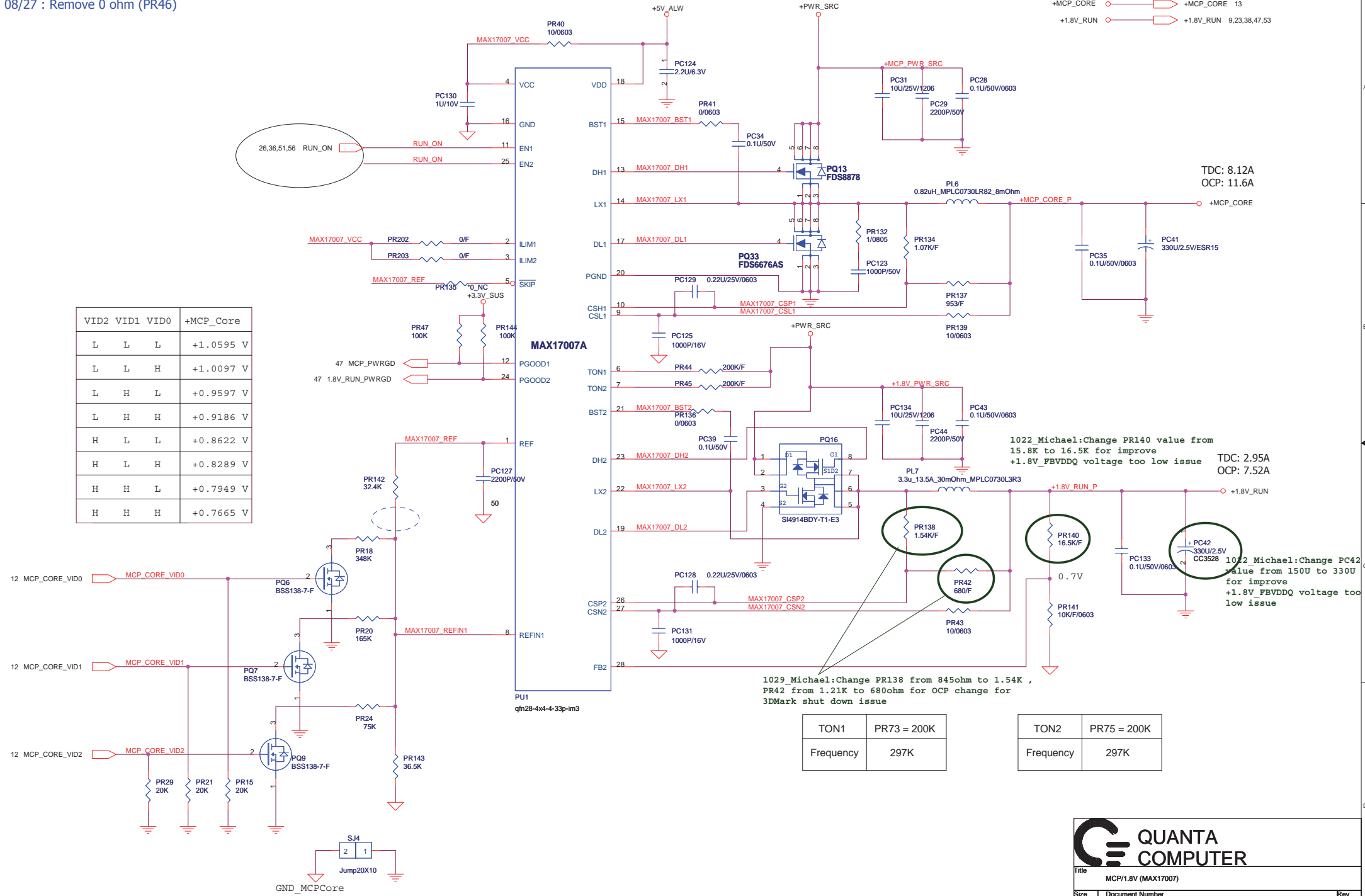
VW	PR37
Frequency	270KHZ@0A / 310KHZ@44A



0904 Rick: Change PC111 value form 0.022uF to 0.068uF for transient change
 1020 Rick: Change PC111 type from 0.068uF 0402 to 0.15uF 0603
 Close to Phase 1 Inductor

08/27 : Remove 0 ohm (PR46)

+MCP_CORE ○ → +MCP_CORE 13
 +1.8V_RUN ○ → +1.8V_RUN 9,23,38,47,53



VID2	VID1	VID0	+MCP_Core
L	L	L	+1.0595 V
L	L	H	+1.0097 V
L	H	L	+0.9597 V
L	H	H	+0.9186 V
H	L	L	+0.8622 V
H	L	H	+0.8289 V
H	H	L	+0.7949 V
H	H	H	+0.7665 V

TON1	PR73 = 200K
Frequency	297K

TON2	PR75 = 200K
Frequency	297K

QUANTA COMPUTER

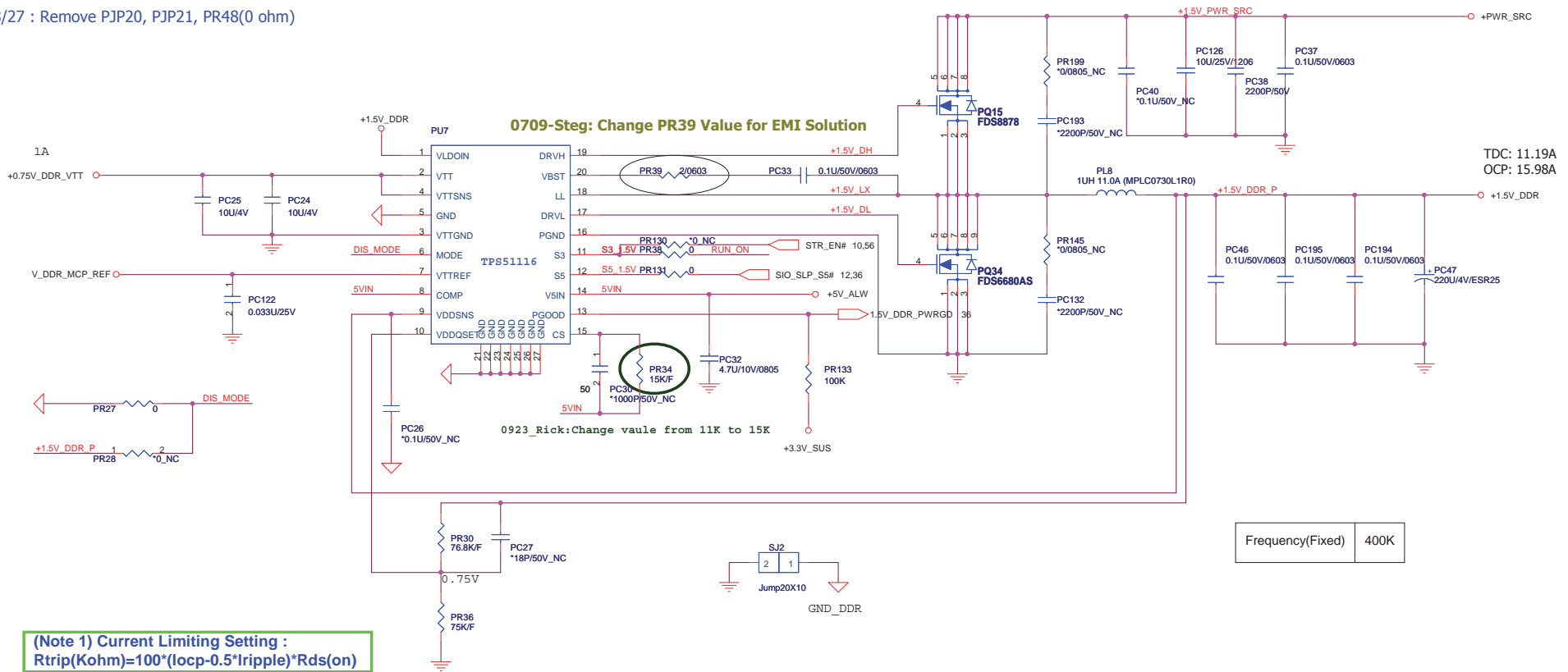
Title: MCP/1.8V (MAX17007)

Size: Document Number IM3 (XPS-Jolie) Rev 1B

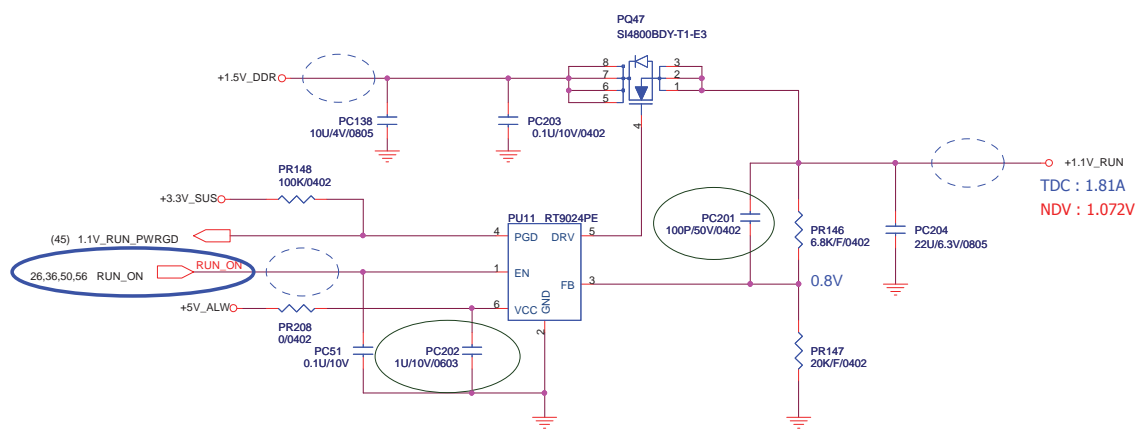
Date: Thursday, October 30, 2008 Sheet 50 of 59

- +1.5V_DDR ○ → +1.5V_DDR 15,16,47,56
- +0.75V_DDR_VTT ○ → +0.75V_DDR_VTT 15,16,56
- +1.1V_RUN ○ → +1.1V_RUN 5,7,8,9,11,12
- V_DDR_MCP_REF ○ → V_DDR_MCP_REF 15,16

08/27 : Remove PJP20, PJP21, PR48(0 ohm)



(Note 1) Current Limiting Setting :
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$



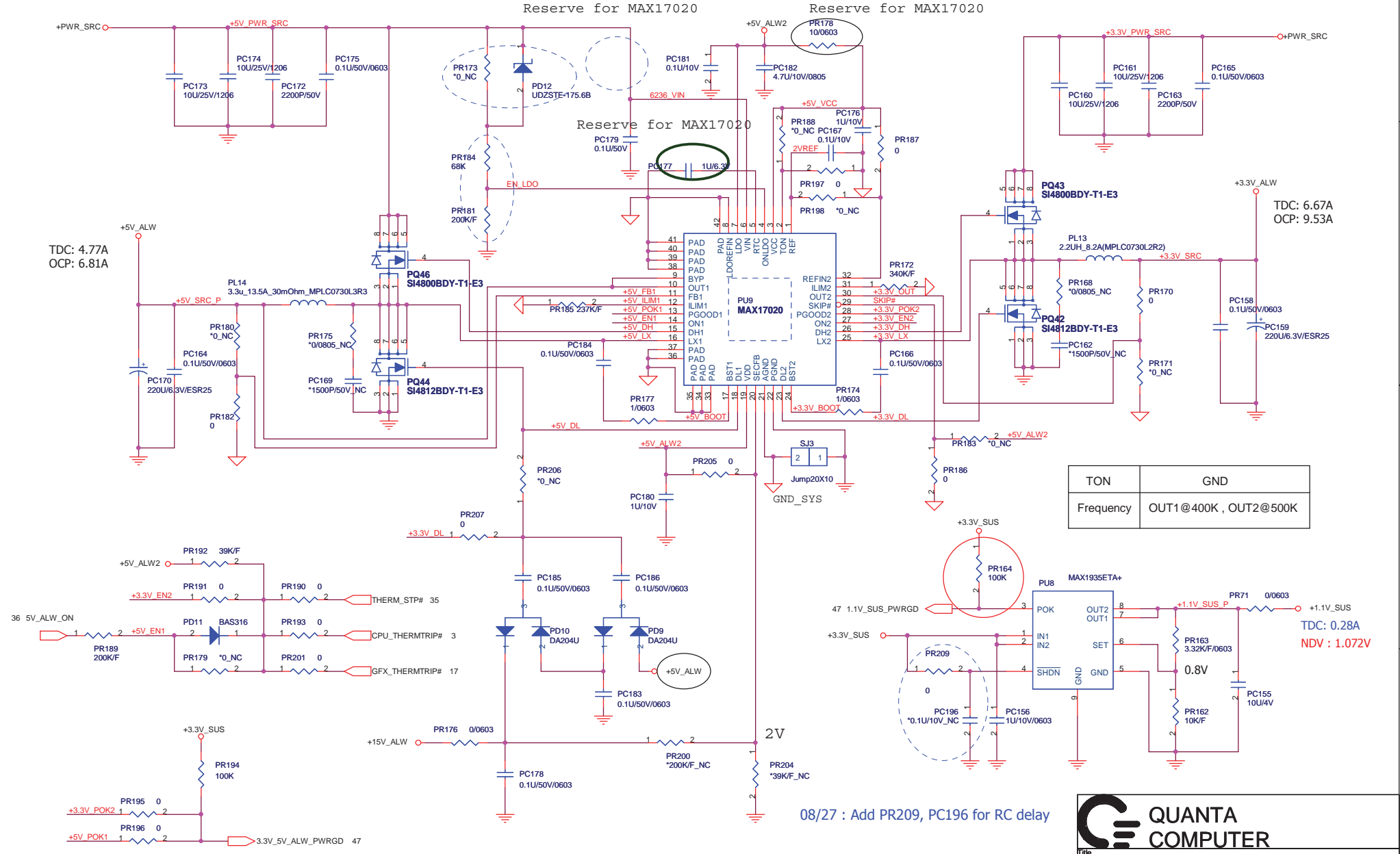
QUANTA COMPUTER

Title		1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	1A	
Date:	Tuesday, October 28, 2008	Sheet	51 of 59

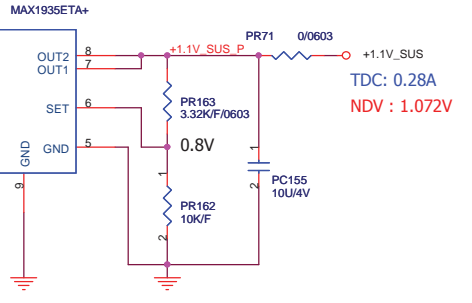
- +1.1V_SUS +1.1V_SUS 13,14
- +5V_ALW +5V_ALW 15,30,31,38,39,47,50,51,53,54,56
- +3.3V_ALW +3.3V_ALW 23,26,31,32,36,37,38,39,47,48,55,56

08/27 : Remove PR169, PR173 (0 ohm)
 08/27 : Add Zener Diode (PD12), PR173 and change PR184=68K, PR181=200K to fix +3.3V_ALW glitch issue when adapter unplug

0916_Rick:Change PC177 value from 0.1u to 1u



TON	GND
Frequency	OUT1@400K , OUT2@500K



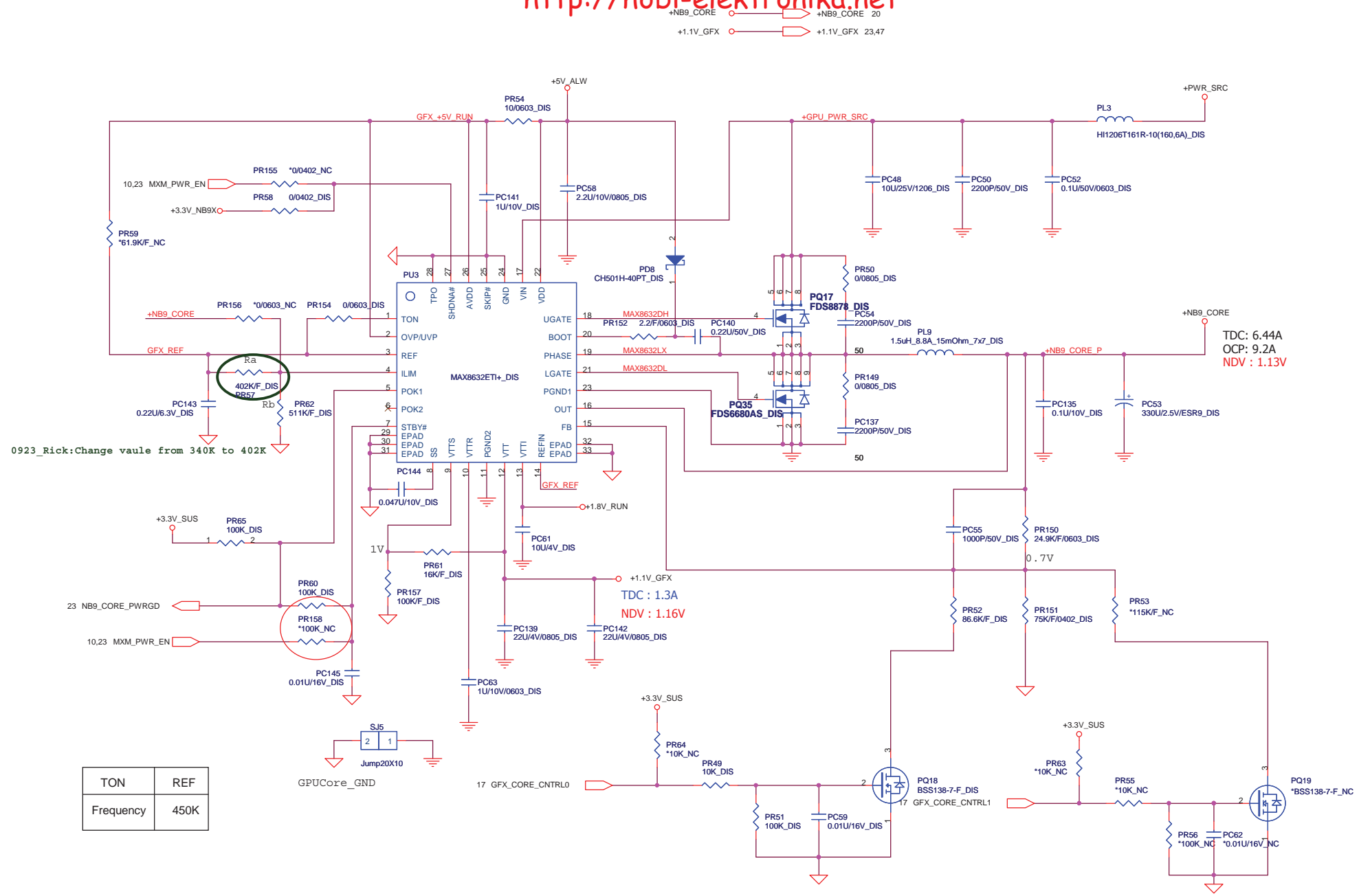
08/27 : Add PR209, PC196 for RC delay

QUANTA COMPUTER

Title: SYS 5V/3V(MAX17020)

Size: Document Number IM3 (XPS-JoSe) Rev 1A

Date: Thursday, October 30, 2008 Sheet 52 of 59



0923_Rick:Change vaule from 340K to 402K

TDC: 6.44A
 OCP: 9.2A
 NDV: 1.13V

TDC: 1.3A
 NDV: 1.16V

TON	REF
Frequency	450K

ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / RDSON) + (I_{DELTA} / 2))$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVF	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+NB9_CORE
LOW	LOW	0.9
HIGH	LOW	0.9
HIGH	HIGH	1.1V

QUANTA COMPUTER

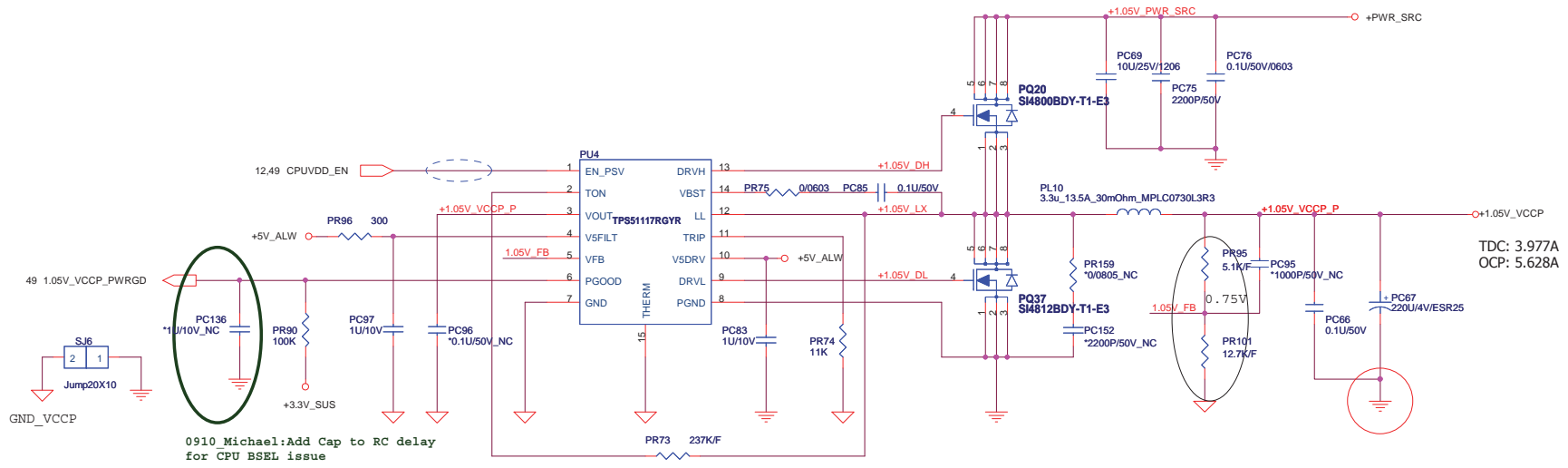
Title: VGA DC/DC

Size: Document Number IM3 (XPS-Jolie) Rev 1A

Date: Tuesday, October 26, 2008 Sheet 53 of 59

+1.05V_VCCP

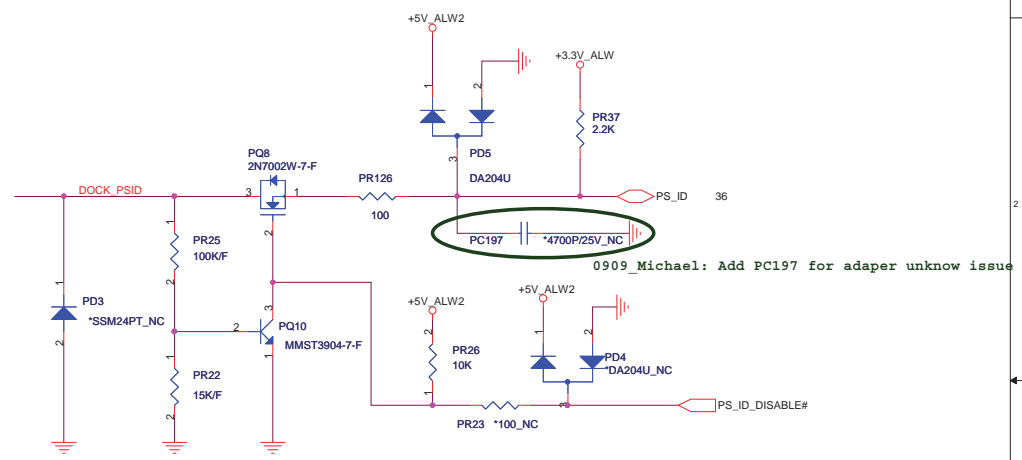
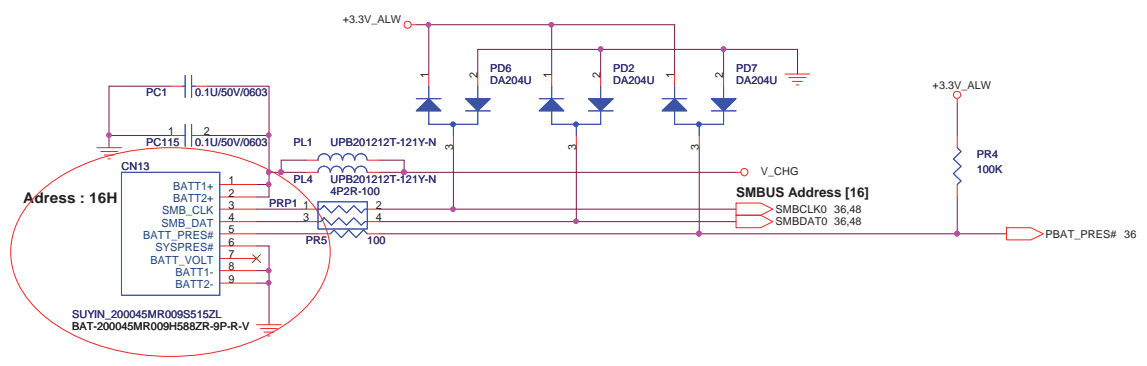
08/27 : Remove 0 ohm (PR79)



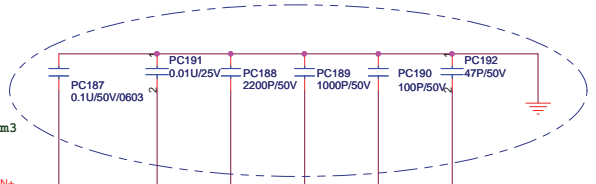
0910 Michael: Add Cap to RC delay for CPU BSEL issue

TDC: 3.977A
OCP: 5.628A

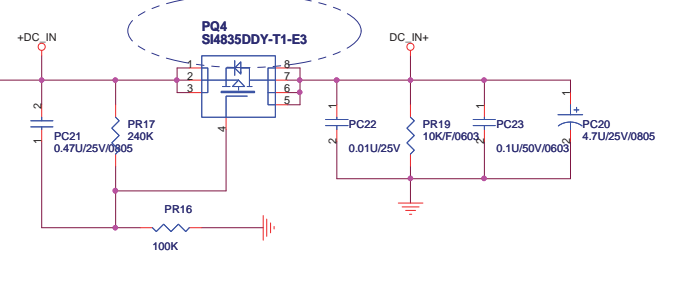
TON	PR185=237K
Frequency	300K



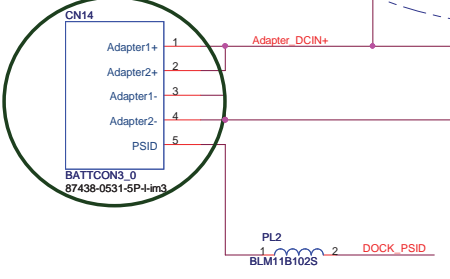
0311-Rick: Add PC187~PC192 for EMC

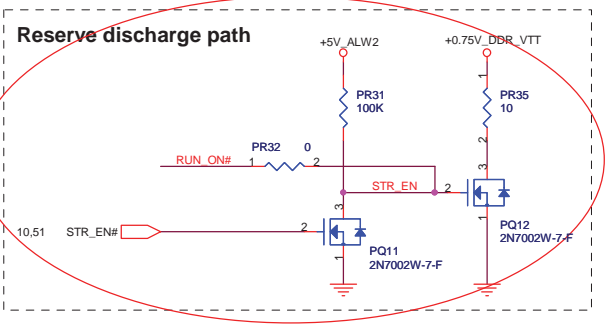
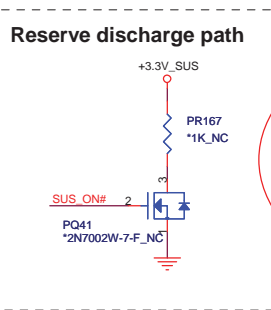
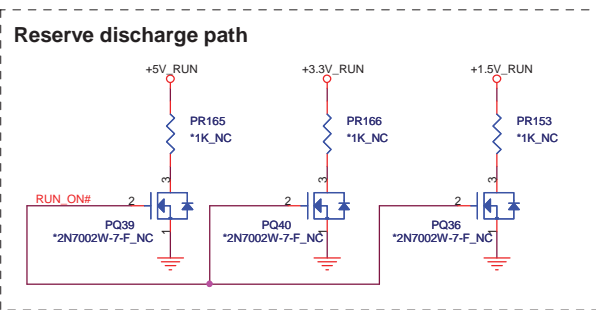
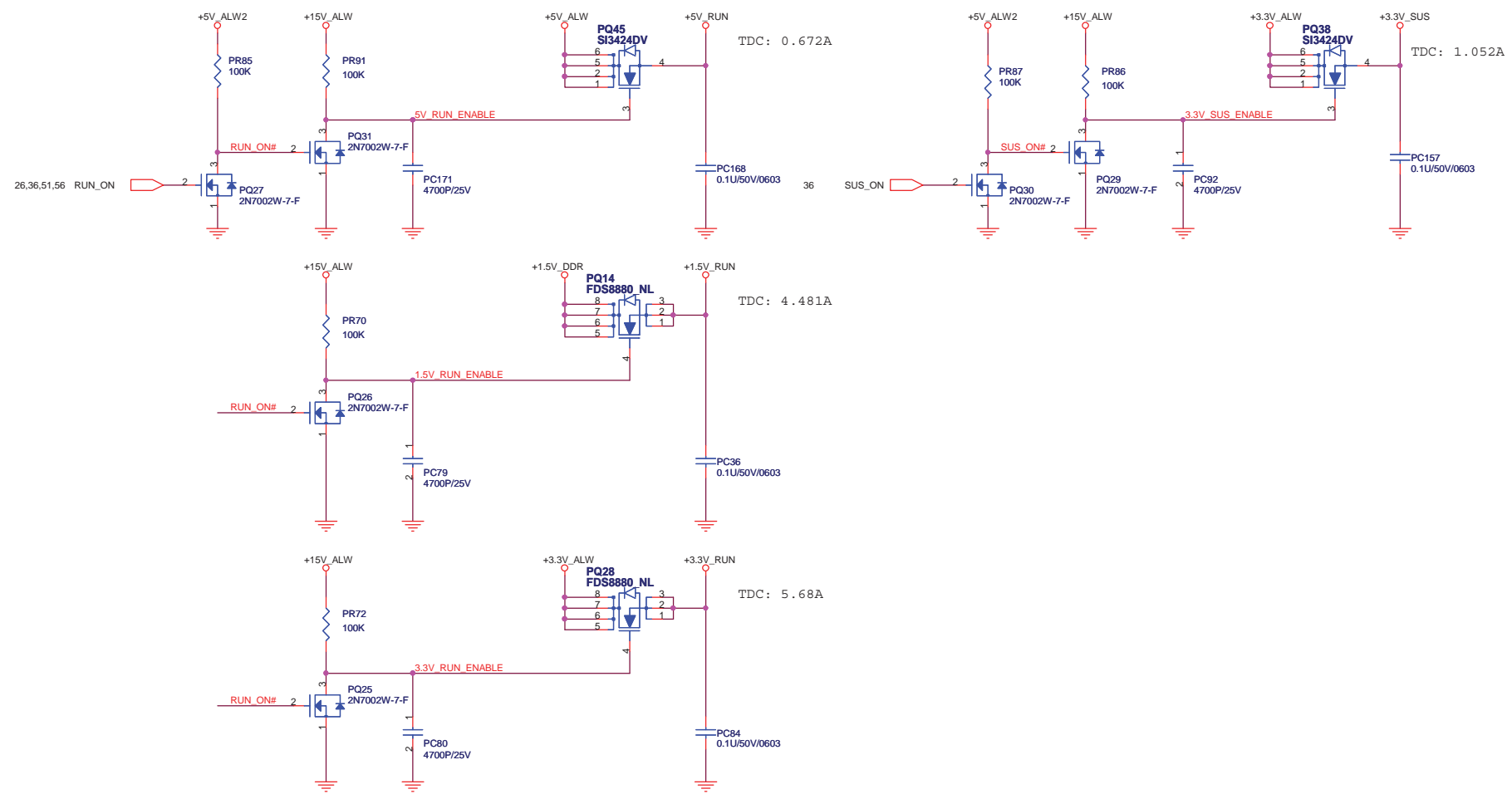


0709-Rick: Change PQ4 Value



0823 Michael: Change Footprint from 87438-0531-5p-L to 87438-0531-5p-1-im3



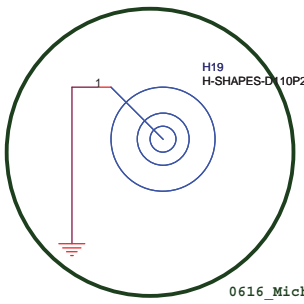


QUANTA COMPUTER

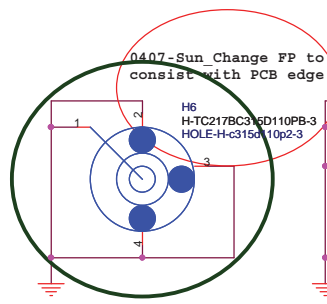
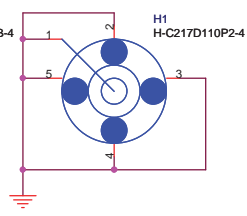
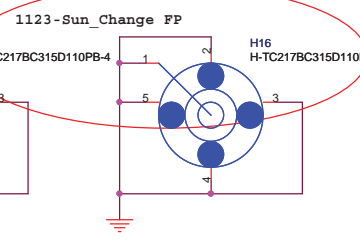
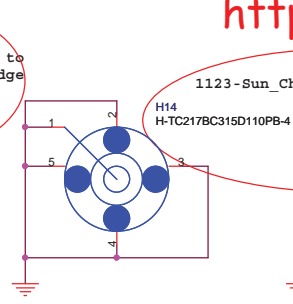
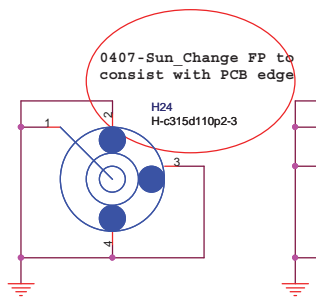
Title: RUN POWER SW

Size: Document Number IM3 (XPS-Jolie) Rev 1A

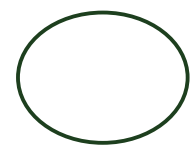
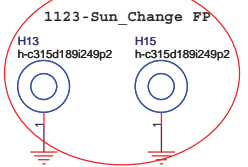
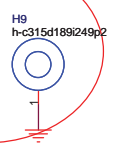
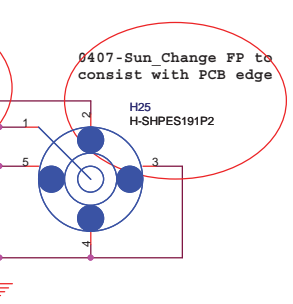
Date: Tuesday, September 09, 2008 Sheet 56 of 59



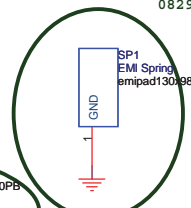
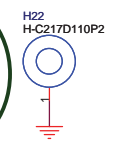
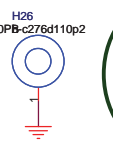
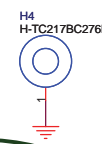
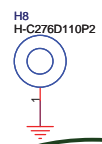
0616_Michael:Change footprint



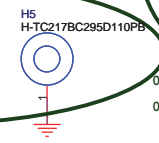
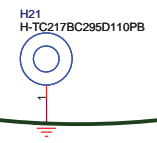
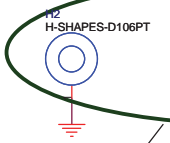
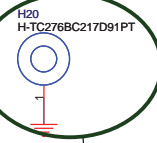
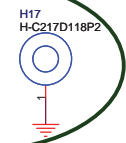
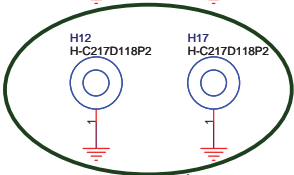
0616_Michael:Change footprint



0829_Michael:Remove H3



0605_Michael: Add connect to GND



0616_Michael:Change footprint

