1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

EVT -- 05/19/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
17		440406	ENGINEERING RELEASED	05/19/06	06/22/04

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9	9	CPU DECAPS & VID<>	M51_HENRY	05/19/2006
10	10	ASIC TEMP SENSORS	M51_DAVE	(MASTER)
11	11	CPU ITP700FLEX DEBUG	M50_HENRY	05/19/2006
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14	14	NB Misc Interfaces	M50_HENRY	05/19/2006
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19	19	NB (GM) Decoupling	M51_DAVE	(MASTER)
20	20	NB Config Straps	M50_HENRY	05/19/2006
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27	27	M51 SMBus Connections	M51_DAVE	(MASTER)
28	28	DDR2 SO-DIMM Connector A	M50_HENRY	05/19/2006
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31	31	Memory Vtt Supply	M50_HENRY	05/19/2006
32	33	CLOCKS	M50_HENRY	05/19/2006
33	34	CLOCKS: TERMINATIONS	M51_HENRY	05/19/2006
34	38	Disk Connectors	M51_DOUG	05/19/2006
35	41	ETHERNET CONTROLLER	M50_DOUG	05/19/2006
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PDF	CSA	CONTENTS	MASTER	DATE
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39	45	FW: 1394B MISC	M51_DOUG	05/19/2006
40	46	FIREWIRE CONNECTORS	M51_DOUG	05/19/2006
41	47	USB Device Interfaces	M51_DOUG	05/19/2006
42	53	AIRPORT CONN	M51_DOUG	05/19/2006
43	54	PCI-E CONNECTIONS	M51_DOUG	05/19/2006
44	58	SMC	M50_HENRY	05/19/2006
45	59	SMC & TPM SUPPORT	M51_HENRY	05/19/2006
46	60	LPC+ CONN	M51_HENRY	05/19/2006
47	63	SPI BOOTROM	M50_DOUG	05/19/2006
48	65	HD AND OD FAN	M51_HENRY	05/19/2006
49	66	CPU FAN, HD & OD TEMP	M51_HENRY	05/19/2006
50	67	TPM	M50_HENRY	05/19/2006
51	68	AUDIO: CODEC	AUDIO	05/19/2006
52	69	AUDIO: LINE INPUT AMP	AUDIO	05/19/2006
53	70	AUDIO: COMBO OUT AMP	AUDIO	05/19/2006
54	71	AUDIO: SPEAKER AMP_1	AUDIO	05/19/2006
55	72	AUDIO: SPEAKER AMP	AUDIO	05/19/2006
56	73	AUDIO: CONNECTORS	AUDIO	05/19/2006
57	74	AUDIO: POWER SUPPLIES	AUDIO	05/19/2006
58	75	IMVP6 CPU VCore Regulator	M50_PAUL	05/19/2006
59	76	CPU & SYSTEM SENSE	M51_DAVE	(MASTER)
60	77	PWR GOOD	M51_PAUL	05/19/2006
61	78	3V DC/DC 2.5V	M51_PAUL	05/19/2006
62	79	1.8V & 1.2V VREG	M51_PAUL	05/19/2006
63	80	1.5V_S0 & 1.05V_S0 VREG	M51_PAUL	05/19/2006
64	82	5V DC/DC	M50_PAUL	05/19/2006
65	83	S0 AND S3 FETS	M51_PAUL	05/19/2006
66	84	MXM PCI-E & PWR	M51_DAVE	(MASTER)
67	85	MXM I/O	M51_DAVE	(MASTER)
68	94	Internal Display Conns	M51_DAVE	(MASTER)
69	97	External Display Conns	M51_DAVE	(MASTER)

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB,SCHEM,MLB,M51	SCH1		
820-1984	1	PCB,FAB,MLB,M51	MLB1		

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM SANTANA

DRAWING NUMBER 051-7039 REV. 17

SHT 1 OF 97

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CPU
(1.83/2.17GHZ)
CORE (~1.2V)
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ITP CONN
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64-BIT
FSB
667MHZ

J9700
MINI-DVI
(TMDS - VGA)
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LVDS
(INTERNAL)
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6DUAL CHANNEL LVDS - 6BIT

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SEE POWER BLOCK DIAGRAM
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U6700
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J6000
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CAMERA

JE351
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IR

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SATA2
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U2100
SB
CORE (1.05V)

JC901
UATA CONNECTOR
OPTICAL
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3.3V/133MHZ

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1
3,7
5
6
J5300 (AIRPORT CONN)

USB
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PCI-E
PAGE 22
PORT 1
PORT 2
PORT 3
PORT 4

X1 - 1.5GHZ
X1 - 1.5GHZ

CORE
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GPIOS
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AZALIA
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SMB
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J2900
DIMM'S
U3301
CK410M
J5300
AIRPORT

33MHZ
32-BIT

TSB82AA2
FIREWIRE B
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J5300
MINI-PCIE
AIRPORT
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U4101
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4 Diff pairs

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100MHZ
8-BIT

TSB81BA3
FIREWIRE B
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0 1 2

2 Diff pairs

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STA9221
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PORT C
PORT F
PORT B

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LINE OUT

SPEAKER AMP
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R/L SPEAKER CONNECTORS
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OPTICAL IN
J7303
COMBO IN CONNECTOR
PAGE 73
LINE IN

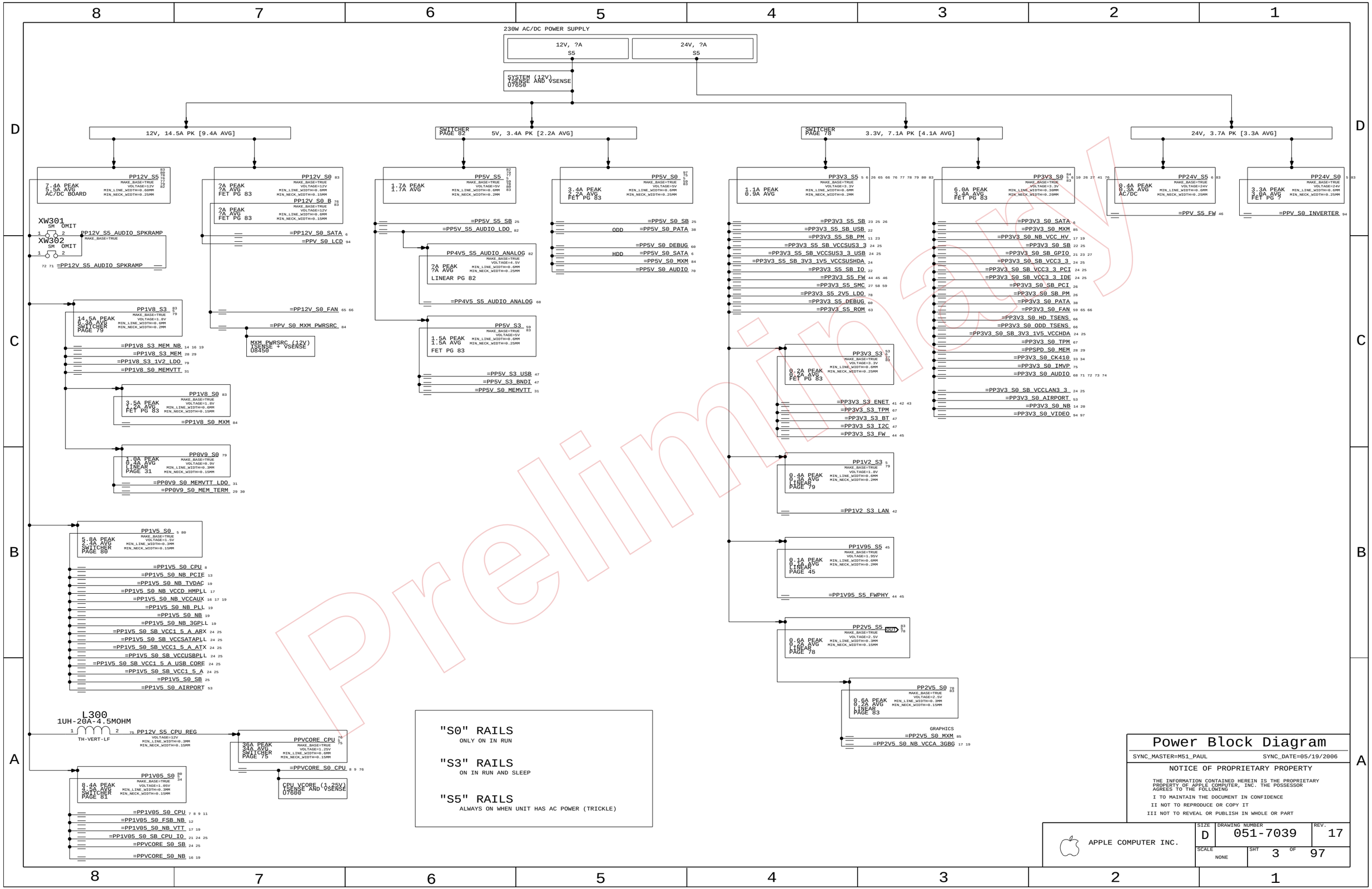
JE350
MIC IN
BNDI
INTERFACE

System Block Diagram

SYNC_MASTER=M51_PAUL
SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 2 OF 97	


230W AC/DC POWER SUPPLY
12V, ?A
S5
24V, ?A
S5
SYSTEM (12V)
ISENSE AND VSENSE
U7650
12V, 14.5A PK [9.4A AVG]
SWITCHER
PAGE 82
5V, 3.4A PK [2.2A AVG]
SWITCHER
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3.3V, 7.1A PK [4.1A AVG]
24V, 3.7A PK [3.3A AVG]
PP12V_S5
7.4A PEAK
5.5A AVG
AC/DC BOARD
PP12V_S0
2A PEAK
2A AVG
FET PG 83
PP12V_S0_B
2A PEAK
2A AVG
FET PG 83
PP5V_S5
1.7A PEAK
1.7A AVG
PP5V_S0
3.4A PEAK
2.2A AVG
FET PG 83
PP3V3_S5
1.1A PEAK
0.9A AVG
PP3V3_S0
6.0A PEAK
3.4A AVG
FET PG 83
PP24V_S5
0.4A PEAK
0.3A AVG
AC/DC
PP24V_S0
3.3A PEAK
3.0A AVG
FET PG 7
XW301
SM OMIT
XW302
SM OMIT
PP12V_S5_AUDIO_SPKRAMP
=PP12V_S5_AUDIO_SPKRAMP
=PP12V_S0_SATA
=PPV_S0_LCD
=PP12V_S0_FAN
=PPV_S0_MXM_PWRSRC
MXM PWRSRC (12V)
ISENSE + VSENSE
U8450
=PPV_S5_FW
=PPV_S0_INVERTER
=PP5V_S5_SB
=PP5V_S5_AUDIO_LDO
PP4V5_S5_AUDIO_ANALOG
2A PEAK
2A AVG
LINEAR PG 82
=PP4V5_S5_AUDIO_ANALOG
=PP5V_S0_SB
ODD =PP5V_S0_PATA
=PP5V_S0_DEBUG
HDD =PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_AUDIO
=PP3V3_S5_SB
=PP3V3_S5_SB_USB
=PP3V3_S5_SB_PM
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
=PP3V3_S5_SB_IO
=PP3V3_S5_FW
=PP3V3_S5_SMC
=PP3V3_S5_2V5_LDO
=PP3V3_S5_DEBUG
=PP3V3_S5_ROM
=PP3V3_S0_SATA
=PP3V3_S0_MXM
=PP3V3_S0_NB_VCC_HV
=PP3V3_S0_SB
=PP3V3_S0_SB_GPIO
=PP3V3_S0_SB_VCC3_3
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_PCI
=PP3V3_S0_SB_PM
=PP3V3_S0_PATA
=PP3V3_S0_FAN
=PP3V3_S0_HD_TSENS
=PP3V3_S0_ODD_TSENS
=PP3V3_S0_SB_3V3_1V5_VCCHDA
=PP3V3_S0_TPM
=PPSPD_S0_MEM
=PP3V3_S0_CK410
=PP3V3_S0_IMVP
=PP3V3_S0_AUDIO
=PP3V3_S0_SB_VCCLAN3_3
=PP3V3_S0_AIRPORT
=PP3V3_S0_NB
=PP3V3_S0_VIDEO
PP3V3_S3
0.2A PEAK
0.2A AVG
FET PG 83
=PP3V3_S3_ENET
=PP3V3_S3_TPM
=PP3V3_S3_BT
=PP3V3_S3_I2C
=PP3V3_S3_FW
PP1V2_S3
0.4A PEAK
0.3A AVG
LINEAR
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=PP1V2_S3_LAN
PP1V95_S5
0.1A PEAK
0.1A AVG
LINEAR
PAGE 45
=PP1V95_S5_FWPHY
PP2V5_S5
OUT
0.6A PEAK
0.2A AVG
LINEAR
PAGE 78
PP2V5_S0
0.6A PEAK
0.2A AVG
LINEAR
PAGE 83
GRAPHICS
=PP2V5_S0_MXM
=PP2V5_S0_NB_VCCA_3GBG
PP1V8_S3
14.5A PEAK
8.3A AVG
SWITCHER
PAGE 79
=PP1V8_S3_MEM_NB
=PP1V8_S3_MEM
=PP1V8_S3_1V2_LDO
=PP1V8_S0_MEMVTT
PP1V8_S0
3.5A PEAK
1.2A AVG
FET PG 83
=PP1V8_S0_MXM
PP0V9_S0
1.0A PEAK
0.4A AVG
LINEAR
PAGE 31
=PP0V9_S0_MEMVTT_LDO
=PP0V9_S0_MEM_TERM
PP1V5_S0
5.8A PEAK
2.4A AVG
SWITCHER
PAGE 80
=PP1V5_S0_CPU
=PP1V5_S0_NB_PCIE
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_NB_VCCD_HMPLL
=PP1V5_S0_NB_VCCAUX
=PP1V5_S0_NB_PLL
=PP1V5_S0_NB
=PP1V5_S0_NB_3GPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCCSATAPLL
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCCUSBPLL
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB
=PP1V5_S0_AIRPORT
L300
1UH-20A-4.5MOHM
TH-VERT-LF
PP12V_S5_CPU_REG
PPVCORE_CPU
38A PEAK
34A AVG
SWITCHER
PAGE 75
=PPVCORE_S0_CPU
CPU VCORE (1.25V)
ISENSE AND VSENSE
U7600
PP1V05_S0
8.4A PEAK
4.5A AVG
SWITCHER
PAGE 81
=PP1V05_S0_CPU
=PP1V05_S0_FSB_NB
=PP1V05_S0_NB_VTT
=PP1V05_S0_SB_CPU_IO
=PPVCORE_S0_SB
=PPVCORE_S0_NB
"S0" RAILS
ONLY ON IN RUN
"S3" RAILS
ON IN RUN AND SLEEP
"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)
Power Block Diagram
SYNC_MASTER=M51_PAUL
SYNC_DATE=05/19/2006
NOTICE OF PROPRIETARY PROPERTY
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. 17
SCALE NONE
SHT 3 OF 97

Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7512	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_V4K
630-7595	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_VMD

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	NB_TSENS_EXT,CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_PWR_SENSE,CPU_TSENS_INT,MXM_PWR_SENSE,SYS_PWR_SENSE,AMB_TSENS

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

BarCode Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:VMD]	CRITICAL	EEE_VMD
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:V4K]	CRITICAL	EEE_V4K

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
(335S0384) 341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	
(338S0274) 341T0020	1	IC,SMC,M51	U5800	CRITICAL	
337S3292	1	MEROM 2.3GHZ, M51	CPU	CRITICAL	M51_BEST
337S3293	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF	BATTERY IS INSTALLED AT FATP
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL		
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL		

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
359S0117	359S0101		U3301	SILEGO CK410 CLOCK
353S1461	353S1465		U7500	CPU VREG NEW REV

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7039 | REV. 17

SCALE NONE | SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 PP OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 PP OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 PP OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 PP OMIT P4MM

34 22 PCI_CLK_SB PP6D0 PP OMIT P4MM
44 34 PCI_CLK_FW PP626 PP OMIT P4MM
58 34 PCI_CLK_SMC PP627 PP OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 PP OMIT P4MM
38 21 IDE_PDIORDY PP6C7 PP OMIT P4MM
38 21 IDE_PDD<9> PP6C8 PP OMIT P4MM

54 22 PCIE_B_D2R_P PP600 PP OMIT P4MM
54 22 PCIE_B_D2R_N PP601 PP OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 PP OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 PP OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 PP OMIT P4MM

63 58 22 SPI_SO PP612 PP OMIT P4MM
63 58 22 SPI_SI PP613 PP OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 PP OMIT P4MM
27 SMBUS_SB_SDA PP605 PP OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 PP OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 PP OMIT P4MM

FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 PP OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 PP OMIT P4MM
14 NB_RST_IN_L_R PP666 PP OMIT P4MM

22 14 DMI_S2N_N<0> PP673 PP OMIT P4MM
22 14 DMI_S2N_P<0> PP674 PP OMIT P4MM

19 14 MEM_VREF_NB_0 PP6E1 PP OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 PP OMIT P4MM

I473
14 NB_CFG<17> — NC_NB_CFG<17> MAKE_BASE=TRUE
I474
14 NB_CFG<15> — NC_NB_CFG<15> MAKE_BASE=TRUE
I475
14 NB_CFG<14> — NC_NB_CFG<14> MAKE_BASE=TRUE
I476
14 NB_CFG<13> — NC_NB_CFG<13> MAKE_BASE=TRUE
I477
14 NB_CFG<12> — NC_NB_CFG<12> MAKE_BASE=TRUE
I478
14 NB_CFG<11> — NC_NB_CFG<11> MAKE_BASE=TRUE
I479
14 NB_CFG<10> — NC_NB_CFG<10> MAKE_BASE=TRUE
I481
14 NB_CFG<8> — NC_NB_CFG<8> MAKE_BASE=TRUE
I480
14 NB_CFG<6> — NC_NB_CFG<6> MAKE_BASE=TRUE
I482
14 NB_CFG<4> — NC_NB_CFG<4> MAKE_BASE=TRUE
I483
14 NB_CFG<3> — NC_NB_CFG<3> MAKE_BASE=TRUE

I513
22 PCI_GNT3_L — TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT
22 USB_F_N — TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P — TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
19 13 LVDS_BKLTEN — TP_LVDS_BKLTEN MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN PEG_R2D_C_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<15> NO_TEST=TRUE

84 13 IN PEG_R2D_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_P<15> NO_TEST=TRUE

84 13 IN PEG_D2R_N<0> NO_TEST=TRUE
84 13 IN PEG_D2R_P<0> NO_TEST=TRUE
84 13 IN PEG_D2R_N<1> NO_TEST=TRUE
84 13 IN PEG_D2R_P<1> NO_TEST=TRUE
84 13 IN PEG_D2R_N<2> NO_TEST=TRUE
84 13 IN PEG_D2R_P<2> NO_TEST=TRUE
84 13 IN PEG_D2R_N<3> NO_TEST=TRUE
84 13 IN PEG_D2R_P<3> NO_TEST=TRUE
84 13 IN PEG_D2R_N<4> NO_TEST=TRUE
84 13 IN PEG_D2R_P<4> NO_TEST=TRUE
84 13 IN PEG_D2R_N<5> NO_TEST=TRUE
84 13 IN PEG_D2R_P<5> NO_TEST=TRUE
84 13 IN PEG_D2R_N<6> NO_TEST=TRUE
84 13 IN PEG_D2R_P<6> NO_TEST=TRUE
84 13 IN PEG_D2R_N<7> NO_TEST=TRUE
84 13 IN PEG_D2R_P<7> NO_TEST=TRUE
84 13 IN PEG_D2R_N<8> NO_TEST=TRUE
84 13 IN PEG_D2R_P<8> NO_TEST=TRUE
84 13 IN PEG_D2R_N<9> NO_TEST=TRUE
84 13 IN PEG_D2R_P<9> NO_TEST=TRUE
84 13 IN PEG_D2R_N<10> NO_TEST=TRUE
84 13 IN PEG_D2R_P<10> NO_TEST=TRUE
84 13 IN PEG_D2R_N<11> NO_TEST=TRUE
84 13 IN PEG_D2R_P<11> NO_TEST=TRUE
84 13 IN PEG_D2R_N<12> NO_TEST=TRUE
84 13 IN PEG_D2R_P<12> NO_TEST=TRUE
84 13 IN PEG_D2R_N<13> NO_TEST=TRUE
84 13 IN PEG_D2R_P<13> NO_TEST=TRUE
84 13 IN PEG_D2R_N<14> NO_TEST=TRUE
84 13 IN PEG_D2R_P<14> NO_TEST=TRUE
84 13 IN PEG_D2R_N<15> NO_TEST=TRUE
84 13 IN PEG_D2R_P<15> NO_TEST=TRUE

76 75 3 IN PPVCORE_CPU FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 IN PP3V3_S5 FUNC_TEST=TRUE
83 IN PP2V5_S5 FUNC_TEST=TRUE
83 78 3 IN PP1V8_S3 FUNC_TEST=TRUE
83 79 3 IN PP1V2_S3 FUNC_TEST=TRUE
79 3 IN PP1V5_S0 FUNC_TEST=TRUE
80 3 IN PP1V05_S0 FUNC_TEST=TRUE
80 34 3 IN PP5V_S5 FUNC_TEST=TRUE
83 82 80 79 78 77 59 5 3 IN PP5V_S0 FUNC_TEST=TRUE
97 83 75 59 3 IN PP5V_S5 FUNC_TEST=TRUE
83 82 80 79 78 77 59 5 3 IN PP3V3_S5 FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 IN PP3V3_S0 FUNC_TEST=TRUE
63 IN PP24V_S0 FUNC_TEST=TRUE
84 83 76 41 27 26 10 6 3 IN
83 3 IN

11 7 IN XDP_BPM_L<3> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<2> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<1> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<0> FUNC_TEST=TRUE
26 11 7 IN XDP_DBRESET_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<0> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<1> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<2> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<3> FUNC_TEST=TRUE
67 60 58 21 5 IN LPC_FRAME_L FUNC_TEST=TRUE
67 60 58 23 IN PM_CLKRUN_L FUNC_TEST=TRUE
60 58 22 IN BOOT_LPC_SPI_L FUNC_TEST=TRUE
60 6 IN DEBUG_RST_L FUNC_TEST=TRUE
60 59 21 IN FWH_INIT_L FUNC_TEST=TRUE
60 34 IN PCI_CLK_PORT80 FUNC_TEST=TRUE
67 60 58 23 IN INT_SERIRQ FUNC_TEST=TRUE
67 60 58 23 IN PM_SUS_STAT_L FUNC_TEST=TRUE
60 58 IN SMC_MD1 FUNC_TEST=TRUE
60 59 58 IN SMC_RST_L FUNC_TEST=TRUE
60 58 IN SMC_NMI FUNC_TEST=TRUE
60 23 IN SV_SET_UP FUNC_TEST=TRUE
76 58 IN ISENSE_CAL_EN FUNC_TEST=TRUE
94 85 IN INV_ENABLE_BL FUNC_TEST=TRUE
94 IN LCD_PWM FUNC_TEST=TRUE
75 8 IN CPU_VID<0> FUNC_TEST=TRUE
75 8 IN CPU_VID<1> FUNC_TEST=TRUE
75 8 IN CPU_VID<2> FUNC_TEST=TRUE
75 8 IN CPU_VID<3> FUNC_TEST=TRUE
75 8 IN CPU_VID<4> FUNC_TEST=TRUE
75 8 IN CPU_VID<5> FUNC_TEST=TRUE
75 8 IN CPU_VID<6> FUNC_TEST=TRUE
75 23 14 IN PM_DPRSLPVR FUNC_TEST=TRUE
75 21 7 IN CPU_DPRSTP_L FUNC_TEST=TRUE
75 26 14 5 IN VR_PWRGOOD_DELAY FUNC_TEST=TRUE
26 23 IN VR_PWRGD_CK410 FUNC_TEST=TRUE
84 77 58 26 IN ALL_SYS_PWRGD FUNC_TEST=TRUE
77 58 23 IN PM_SLP_S4_L FUNC_TEST=TRUE
80 79 77 58 23 IN PM_SLP_S3_L FUNC_TEST=TRUE

60 59 58 IN SMC_TCK FUNC_TEST=TRUE
60 59 58 IN SMC_TDI FUNC_TEST=TRUE
60 59 58 IN SMC_TDO FUNC_TEST=TRUE
60 59 58 IN SMC_TMS FUNC_TEST=TRUE
60 58 IN SMC_TRST_L FUNC_TEST=TRUE
60 59 58 IN SMC_TX_L FUNC_TEST=TRUE
60 59 58 IN SMC_RX_L FUNC_TEST=TRUE
59 IN SMC_MANUAL_RST_L FUNC_TEST=TRUE
11 7 IN XDP_TCK FUNC_TEST=TRUE
11 7 IN XDP_TDI FUNC_TEST=TRUE
11 7 IN XDP_TDO FUNC_TEST=TRUE
11 7 IN XDP_TMS FUNC_TEST=TRUE
11 7 IN XDP_TRST_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXP FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXN FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_N FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_P FUNC_TEST=TRUE
11 IN ITPRESET_L FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<5> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<4> FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA 1 | ZH510 HOLE-VIA 1 | ZH520 HOLE-VIA 1
ZH501 HOLE-VIA 1 | ZH511 HOLE-VIA 1 | ZH521 HOLE-VIA 1
ZH502 HOLE-VIA 1 | ZH512 HOLE-VIA 1 | ZH522 HOLE-VIA 1
ZH503 HOLE-VIA 1 | ZH513 HOLE-VIA 1 | ZH523 HOLE-VIA 1
ZH504 HOLE-VIA 1 | ZH514 HOLE-VIA 1 | ZH524 HOLE-VIA 1
ZH505 HOLE-VIA 1 | ZH515 HOLE-VIA 1 | ZH525 HOLE-VIA 1
ZH506 HOLE-VIA 1 | ZH516 HOLE-VIA 1 | ZH526 HOLE-VIA 1
ZH507 HOLE-VIA 1 | ZH517 HOLE-VIA 1 | ZH527 HOLE-VIA 1
ZH508 HOLE-VIA 1 | ZH518 HOLE-VIA 1 | ZH528 HOLE-VIA 1
ZH509 HOLE-VIA 1 | ZH519 HOLE-VIA 1 | ZH529 HOLE-VIA 1

FUNC TEST 1 OF 2

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 5 OF 97	

SYSTEM STATUS

PP3V3_S5 → R602 1K 5% 1/16W MF-LF 402 → ITS_PLUGGED_IN → LED601 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:1

PP3V3_S3 → R600 1K 5% 1/16W MF-LF 402 → ITS_ALIVE → LED602 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:2

PP12V_LCD_CONN → R601 3.3K 5% 1/16W MF-LF 402 → LCD_SHOULD_ON → LED603 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:3

PP3V3_S0 → DEVELOPMENT R605 1K 5% 1/16W MF-LF 402 → ITS_RUNNING → DEVELOPMENT LED600 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:RUN

GPU_PRESENT_R → DEVELOPMENT R604 1K 5% 1/16W MF-LF 402 → GPU_PRESENT → DEVELOPMENT LED604 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:EFI OK

AC/DC CONN

PP3V3_S0 → R606 1.5K 1% 1/16W MF-LF 402 (CRITICAL)

pp3v3_s5 → R607 10K 5% 1/16W MF-LF 402

J601 HM9606E-M2 M-RT-TH

SYS_POWERFAIL_L

ACDC_TEMP

FROM AC/DC TO HDD

=PP12V_S0_SATA → NOSTUFF C624 100UF 20% 16V ELEC 6.3X5.5-SM

PP12V_S5_AC_DC TO SYS ISENSE

PP24V_S5

=PP5V_S0_SATA → NOSTUFF C625 100UF 20% 16V ELEC SM1-LF; NOSTUFF C623 150UF 20% 16V ELEC SM

NOSTUFF C622 100PF 5% 50V CERM 402; NOSTUFF C620 100PF 5% 50V CERM 402; NOSTUFF C621 100PF 5% 50V CERM 402

GND_CHASSIS_POWER_ZH611 OMIT ZH611 4P25R3P5

=PP3V3_S0_SATA OUT

NOT SENDING 3.3V TO THE DRIVE BECAUSE IT IS NOT NEEDED AND THERE IS NO FREE PIN ON THE CONNECTOR

GND RAILS

GND_AUDIO → XW601 SM OMIT

GND_AUDIO_SPKRAMP → XW602 SM OMIT; XW603 SM OMIT

CHASSIS GND

GND_CHASSIS_IO_LEFT MAKE_BASE=TRUE VOLTAGE=0 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM → GND_CHASSIS_AUDIO_EXTERNAL

TO NONPLATED HOLE TO LEFT OF EXTERNAL AUDIO CONNECTORS

GND_CHASSIS_USB, GND_CHASSIS_FIREWIRE, GND_CHASSIS_DVI, GND_CHASSIS_RJ45 → GND_CHASSIS_IO_RIGHT MAKE_BASE=TRUE VOLTAGE=0 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

TO NONPLATED SLOT TO RIGHT OF EXTERNAL IO

GND_CHASSIS_AUDIO_INTERNAL → OMIT ZH632 4P25R3P5

GND_CHASSIS_BNDI MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM VOLTAGE=0 MAKE_BASE=TRUE

CHASSIS NEXT TO AUDIO CONNECTORS

PP3V3_S5 → C600 0.1UF 20% 10V CERM 402

CRITICAL U600 74LC125 125 TSSOP

PLT_RST_L → U600_3 → R618 68 5% 1/16W 402 MF-LF → FW_RST_L

R619 68 5% 1/16W 402 MF-LF → SMC_LRESET_L

U600_6 → R611 68 5% 1/16W 402 MF-LF → NB_RST_IN_L

R612 68 5% 1/16W 402 MF-LF → PEG_RESET_L

U600_8 → R614 68 5% 1/16W 402 MF-LF → ENET_RST_L

R615 68 5% 1/16W 402 MF-LF → TPM_LRESET_L

U600_11 → R616 68 5% 1/16W 402 MF-LF → AIRPORT_RST_L

R617 68 5% 1/16W 402 MF-LF → DEBUG_RST_L

GND_CHASSIS_NEAR_MXM VOLTAGE=0 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE → GND_CHASSIS_ODD_TEMP, GND_CHASSIS_GPU_TEMP

OMIT ZH630 4P25R3P5 — CHASSIS HOLE NEAR MXM

OMIT ZH631 4P25R3P5 — CHASSIS HOLE UPPER RIGHT CORNER OF BOARD

GND_CHASSIS_TOP_RIGHT MAKE_BASE=TRUE VOLTAGE=0 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM → GND_CHASSIS_HDD_TEMP, GND_CHASSIS_CPU_TEMP

NOSTUFF C630 0.01UF 20% 16V CERM 402

NOSTUFF C631 0.01UF 20% 16V CERM 402

CHASSIS HOLE NEAR ODD CONNECTOR (TOP MID)

GND_CHASSIS_NEAR_ODD_CON MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0 → OMIT ZH633 4P25R3P5

NOSTUFF C633 0.01UF 20% 16V CERM 402

CHASSIS HOLE NEAR POWER SWITCH CONNECTOR (BOT RIGHT)

GND_CHASSIS_NEAR_PWR_SW MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0 → OMIT ZH634 4P25R3P5

NOSTUFF C634 0.01UF 20% 16V CERM 402

HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU

SDF600 HSK-NUT-6.5MM TH

SDF601 HSK-NUT-6.5MM TH

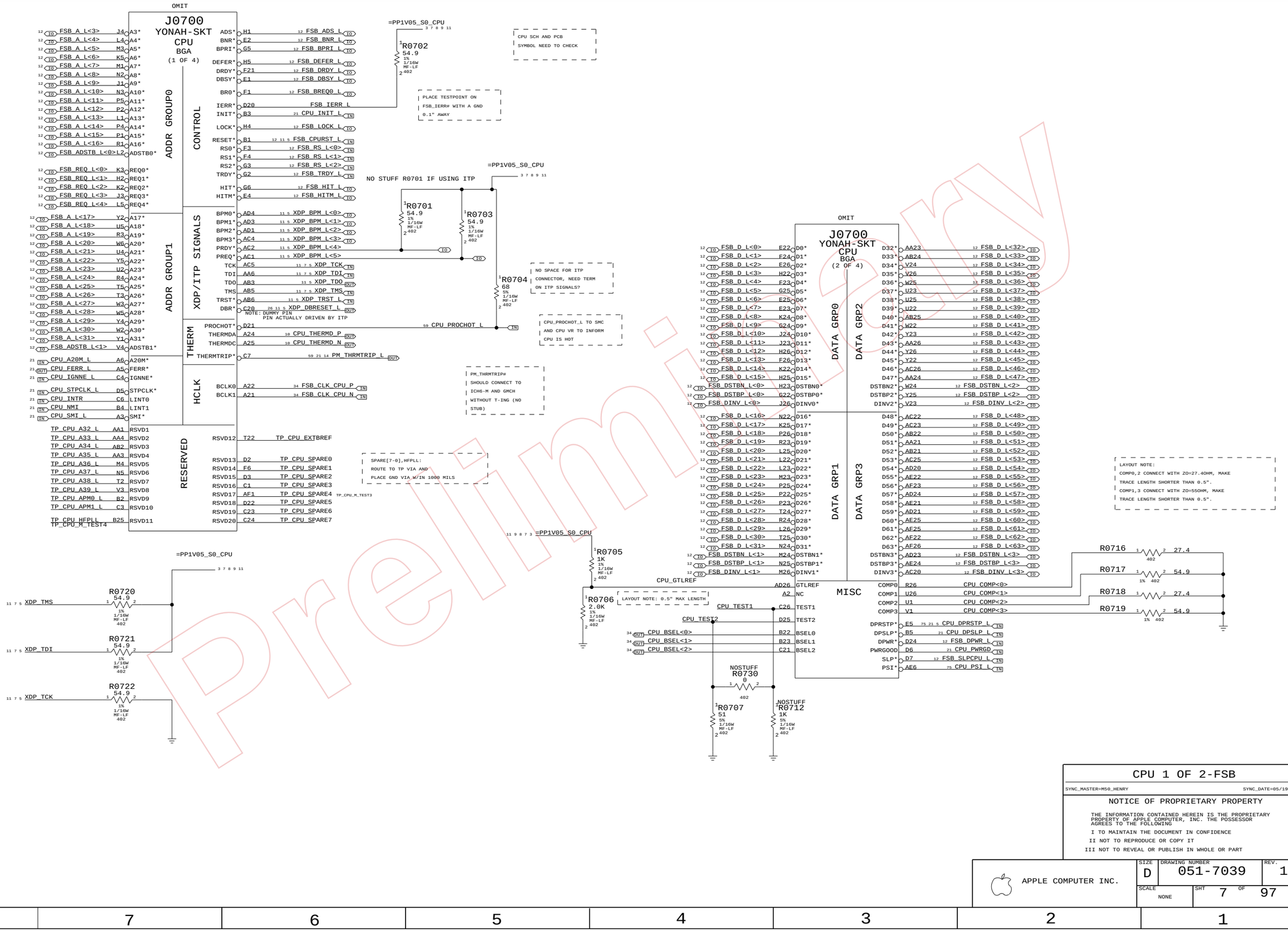
POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE: NONE SHT 6 OF 97



CPU 1 OF 2-FSB

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 7 OF 97	

=PPVCORE_S0_CPU 3 8 9 76

OMIT

J0700
YONAH-SKT
CPU
BGA
(3 OF 4)

A7	VCC_1	VCC_68	AB20
A9	VCC_2	VCC_69	AB7
A10	VCC_3	VCC_70	AC7
A12	VCC_4	VCC_71	AC9
A13	VCC_5	VCC_72	AC12
A15	VCC_6	VCC_73	AC13
A17	VCC_7	VCC_74	AC15
A18	VCC_8	VCC_75	AC17
A20	VCC_9	VCC_76	AC18
B7	VCC_10	VCC_77	AD7
B9	VCC_11	VCC_78	AD9
B10	VCC_12	VCC_79	AD10
B12	VCC_13	VCC_80	AD12
B14	VCC_14	VCC_81	AD14
B15	VCC_15	VCC_82	AD15
B17	VCC_16	VCC_83	AD17
B18	VCC_17	VCC_84	AD18
B20	VCC_18	VCC_85	AE9
C9	VCC_19	VCC_86	AE10
C10	VCC_20	VCC_87	AE12
C12	VCC_21	VCC_88	AE13
C13	VCC_22	VCC_89	AE15
C15	VCC_23	VCC_90	AE17
C17	VCC_24	VCC_91	AE18
C18	VCC_25	VCC_92	AE20
D9	VCC_26	VCC_93	AF9
D10	VCC_27	VCC_94	AF10
D12	VCC_28	VCC_95	AF12
D14	VCC_29	VCC_96	AF14
D15	VCC_30	VCC_97	AF15
D17	VCC_31	VCC_98	AF17
D18	VCC_32	VCC_99	AF18
E7	VCC_33	VCC_100	AF20
E9	VCC_34		
E10	VCC_35	VCCP_1	V6
E12	VCC_36	VCCP_2	G21
E13	VCC_37	VCCP_3	J6
E15	VCC_38	VCCP_4	K6
E17	VCC_39	VCCP_5	M6
E18	VCC_40	VCCP_6	J21
E20	VCC_41	VCCP_7	K21
F7	VCC_42	VCCP_8	M21
F9	VCC_43	VCCP_9	N21
F10	VCC_44	VCCP_10	N6
F12	VCC_45	VCCP_11	R21
F14	VCC_46	VCCP_12	R6
F15	VCC_47	VCCP_13	T21
F17	VCC_48	VCCP_14	T6
F18	VCC_49	VCCP_15	V21
F20	VCC_50	VCCP_16	W21
AA7	VCC_51		
AA9	VCC_52	VCCA	B26
AA10	VCC_53		
AA12	VCC_54		
AA13	VCC_55	VID0	AD6
AA15	VCC_56	VID1	AF5
AA17	VCC_57	VID2	AE5
AA18	VCC_58	VID3	AF4
AA20	VCC_59	VID4	AE3
AB9	VCC_60	VID5	AF2
AC10	VCC_61	VID6	AE2
AB10	VCC_62		
AB12	VCC_63		
AB14	VCC_64		
AB15	VCC_65	VCCSENSE	AF7
AB17	VCC_66		
AB18	VCC_67	VSSSENSE	AE7

=PPVCORE_S0_CPU 3 8 9 76

=PP1V05_S0_CPU 3 7 9 11

=PP1V5_S0_CPU 3 8

VCCA=1.5 ONLY

VID0 75 5 CPU_VID<0> OUT
VID1 75 5 CPU_VID<1> OUT
VID2 75 5 CPU_VID<2> OUT
VID3 75 5 CPU_VID<3> OUT
VID4 75 5 CPU_VID<4> OUT
VID5 75 5 CPU_VID<5> OUT
VID6 75 5 CPU_VID<6> OUT

=PPVCORE_S0_CPU 3 8 9 76

R0802
100
1%
1/16W
MF-LF
402

VCCSENSE 75 CPU_VCCSENSE_P OUT

VSSSENSE 75 CPU_VCCSENSE_N OUT

R0803
100
1%
1/16W
MF-LF
402

LAYOUT NOTE: CONNECT R0802-03
TO VCCSENSE_P/N WITH NO STUB

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENCTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE AT THE
LOCATION WHERE THE TWO 54.9 OHM
RESISTORS TERMINATE THE 55 OHM
TRANSMISSION LINE

=PP1V5_S0_CPU 3 8

C0800
0.01UF
20%
16V
CERM
402

C0801
10UF
20%
6.3V
CERM
805-1

OMIT

J0700
YONAH-SKT
CPU
BGA
(4 OF 4)

A4	VSS_1	VSS_82	P6
A8	VSS_2	VSS_83	P21
A11	VSS_3	VSS_84	P24
A14	VSS_4	VSS_85	R2
A16	VSS_5	VSS_86	R5
A19	VSS_6	VSS_87	R22
A23	VSS_7	VSS_88	R25
A26	VSS_8	VSS_89	T1
B6	VSS_9	VSS_90	T4
B8	VSS_10	VSS_91	T23
B11	VSS_11	VSS_92	T26
B13	VSS_12	VSS_93	U3
B16	VSS_13	VSS_94	U6
B19	VSS_14	VSS_95	U21
B21	VSS_15	VSS_96	U24
B24	VSS_16	VSS_97	V2
C5	VSS_17	VSS_98	V5
C8	VSS_18	VSS_99	V22
C11	VSS_19	VSS_100	V25
C14	VSS_20	VSS_101	W1
C16	VSS_21	VSS_102	W4
C19	VSS_22	VSS_103	W23
C2	VSS_23	VSS_104	W26
C22	VSS_24	VSS_105	Y3
C25	VSS_25	VSS_106	Y6
D1	VSS_26	VSS_107	Y21
D4	VSS_27	VSS_108	Y24
D8	VSS_28	VSS_109	AA2
D11	VSS_29	VSS_110	AA5
D13	VSS_30	VSS_111	AA8
D16	VSS_31	VSS_112	AA11
D19	VSS_32	VSS_113	AA14
D23	VSS_33	VSS_114	AA16
D26	VSS_34	VSS_115	AA19
E3	VSS_35	VSS_116	AA22
E6	VSS_36	VSS_117	AA25
E8	VSS_37	VSS_118	AB1
E11	VSS_38	VSS_119	AB4
E14	VSS_39	VSS_120	AB8
E16	VSS_40	VSS_121	AB11
E19	VSS_41	VSS_122	AB13
E21	VSS_42	VSS_123	AB16
E24	VSS_43	VSS_124	AB19
E5	VSS_44	VSS_125	AB23
F8	VSS_45	VSS_126	AB26
F11	VSS_46	VSS_127	AC3
F13	VSS_47	VSS_128	AC6
F16	VSS_48	VSS_129	AC8
F19	VSS_49	VSS_130	AC11
F2	VSS_50	VSS_131	AC14
F22	VSS_51	VSS_132	AC16
F25	VSS_52	VSS_133	AC19
G4	VSS_53	VSS_134	AC21
G1	VSS_54	VSS_135	AC24
G23	VSS_55	VSS_136	AD2
G26	VSS_56	VSS_137	AD5
H3	VSS_57	VSS_138	AD8
H6	VSS_58	VSS_139	AD11
H21	VSS_59	VSS_140	AD13
H24	VSS_60	VSS_141	AD16
J2	VSS_61	VSS_142	AD19
J5	VSS_62	VSS_143	AD22
J22	VSS_63	VSS_144	AD25
J25	VSS_64	VSS_145	AE1
K1	VSS_65	VSS_146	AE4
K4	VSS_66	VSS_147	AE8
K23	VSS_67	VSS_148	AE11
K26	VSS_68	VSS_149	AE14
L3	VSS_69	VSS_150	AE16
L6	VSS_70	VSS_151	AE19
L21	VSS_71	VSS_152	AE23
L24	VSS_72	VSS_153	AE26
M2	VSS_73	VSS_154	AF3
M5	VSS_74	VSS_155	AF6
M22	VSS_75	VSS_156	AF8
M25	VSS_76	VSS_157	AF11
N1	VSS_77	VSS_158	AF13
N4	VSS_78	VSS_159	AF16
N23	VSS_79	VSS_160	AF19
N26	VSS_80	VSS_161	AF21
P3	VSS_81	VSS_162	AF24

CPU 2 OF 2-PWR/GND

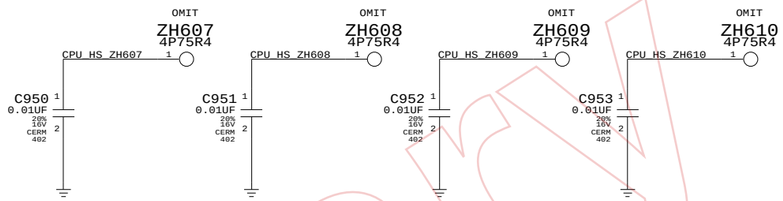
SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

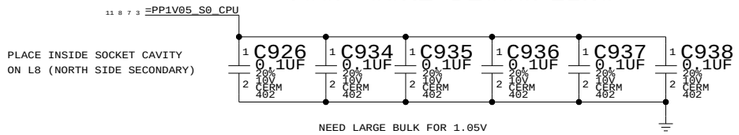
SCALE NONE SHT 8 OF 97

CPU HEATSINK MOUNTING HOLES

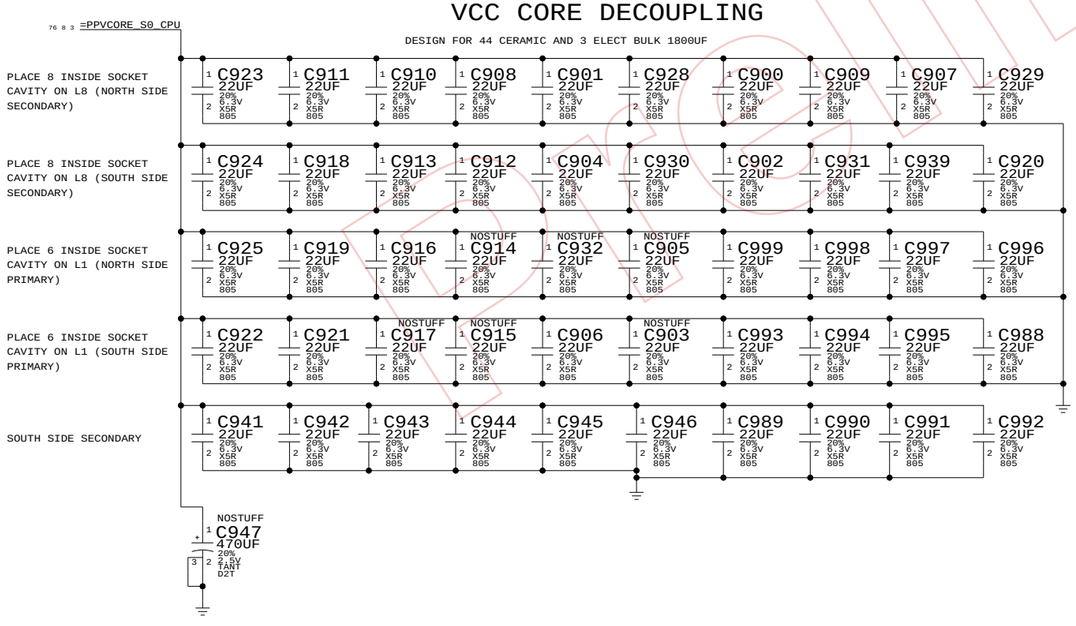


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

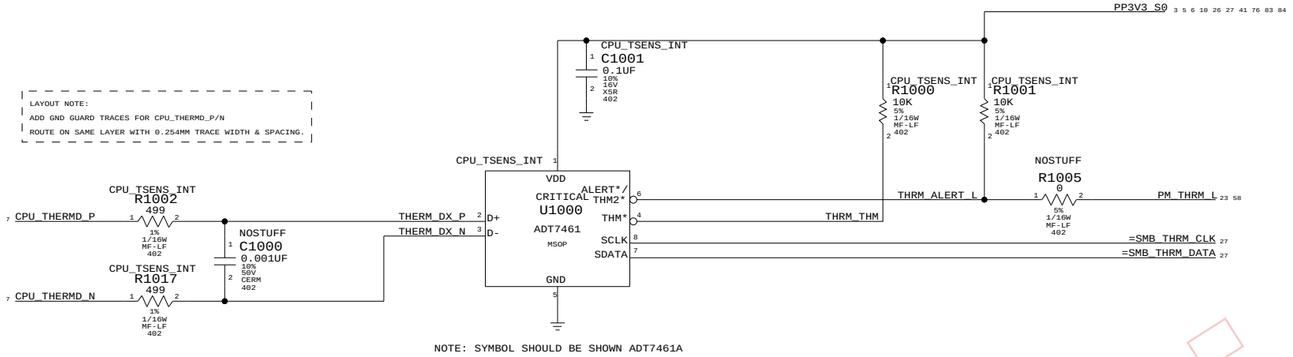
SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE	SHT	OF
NONE	9	97

CPU INTERNAL DIODE THERMAL SENSOR

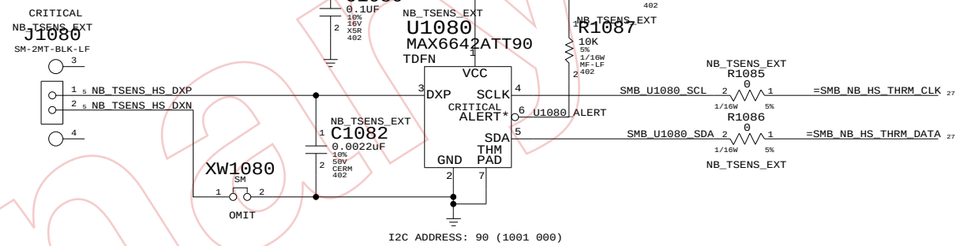
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



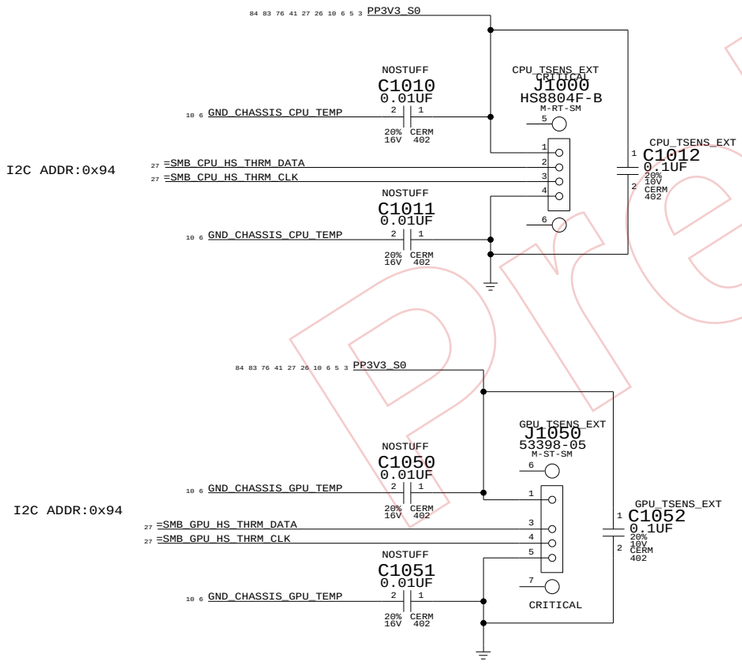
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

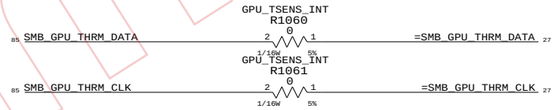


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

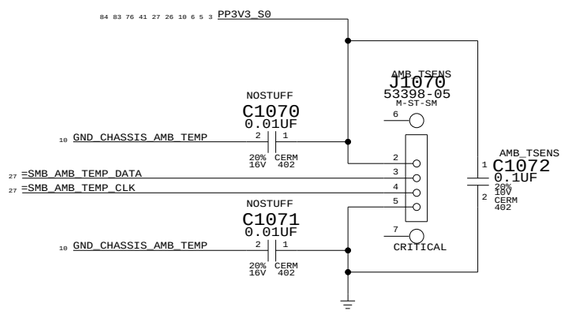


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



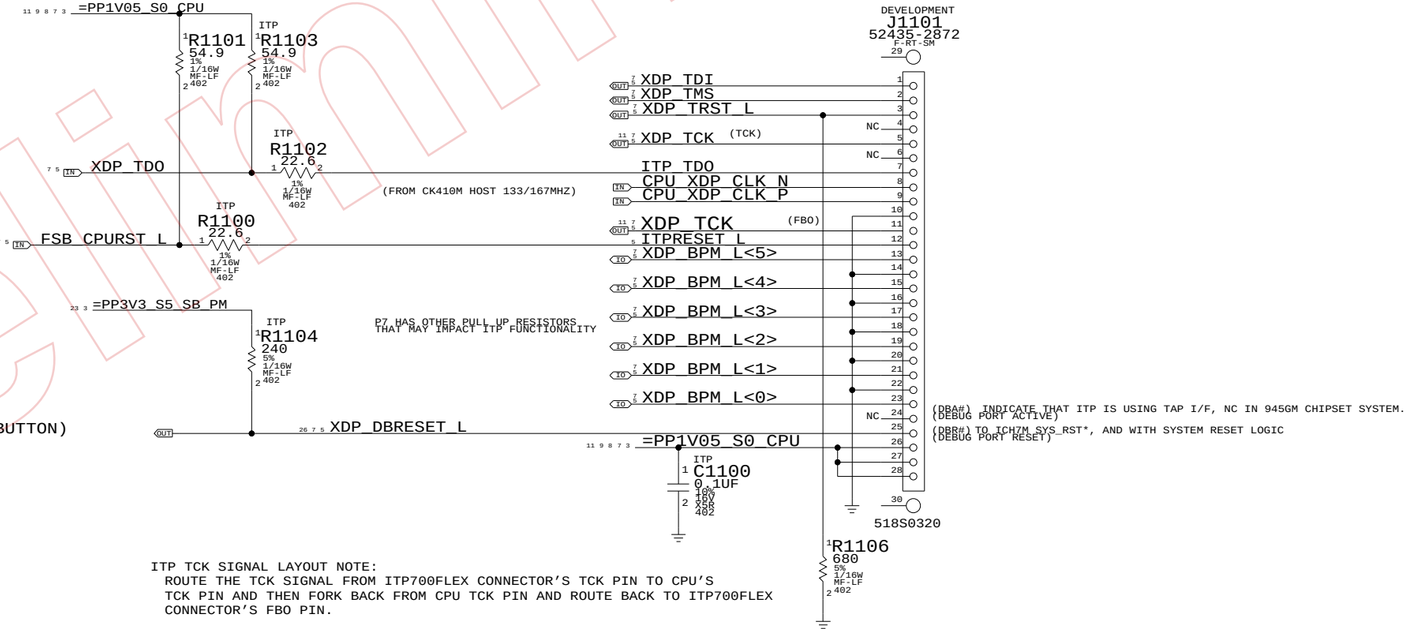
ASIC TEMP SENSORS

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 10 OF 97	

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
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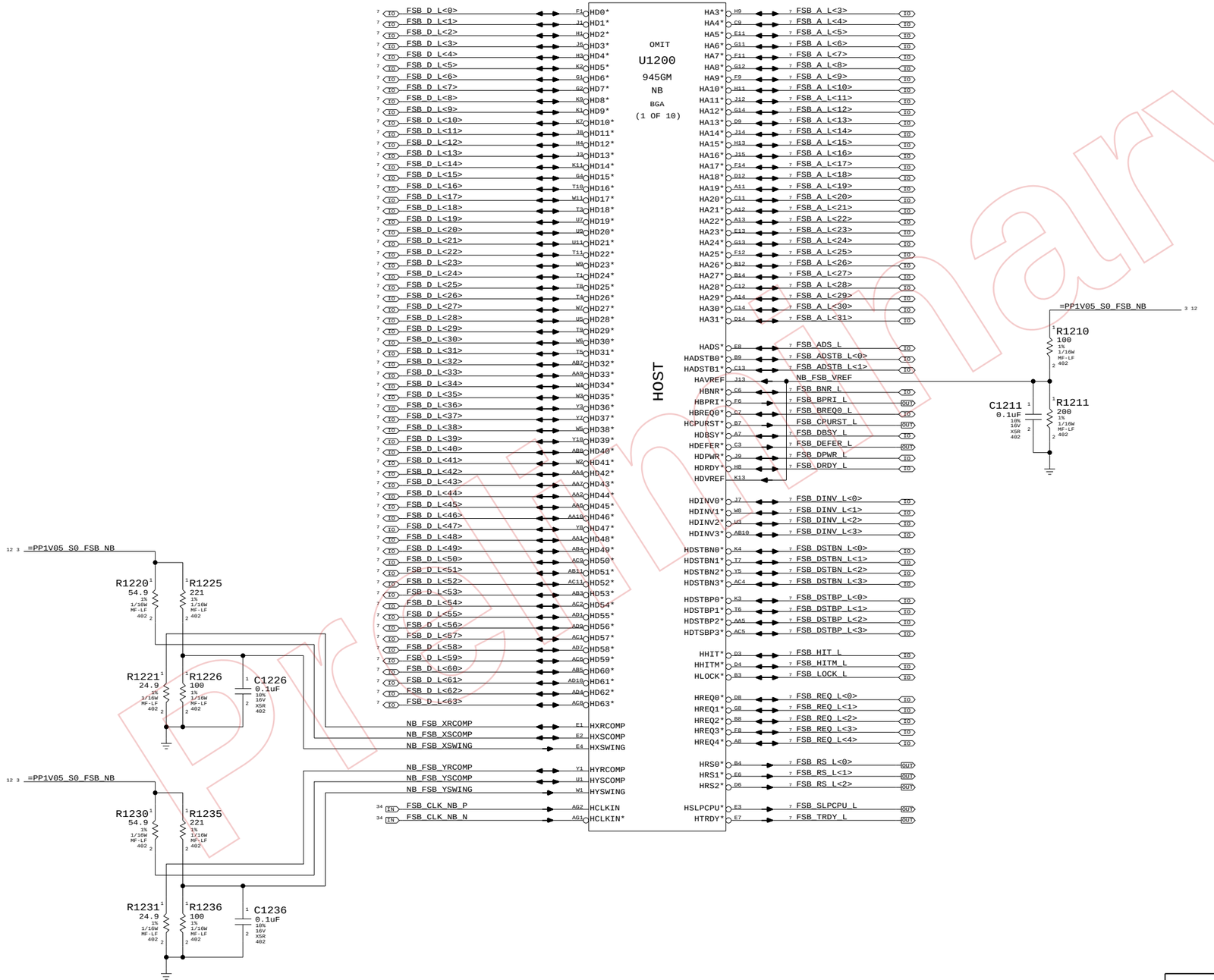


NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 12 OF 97	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

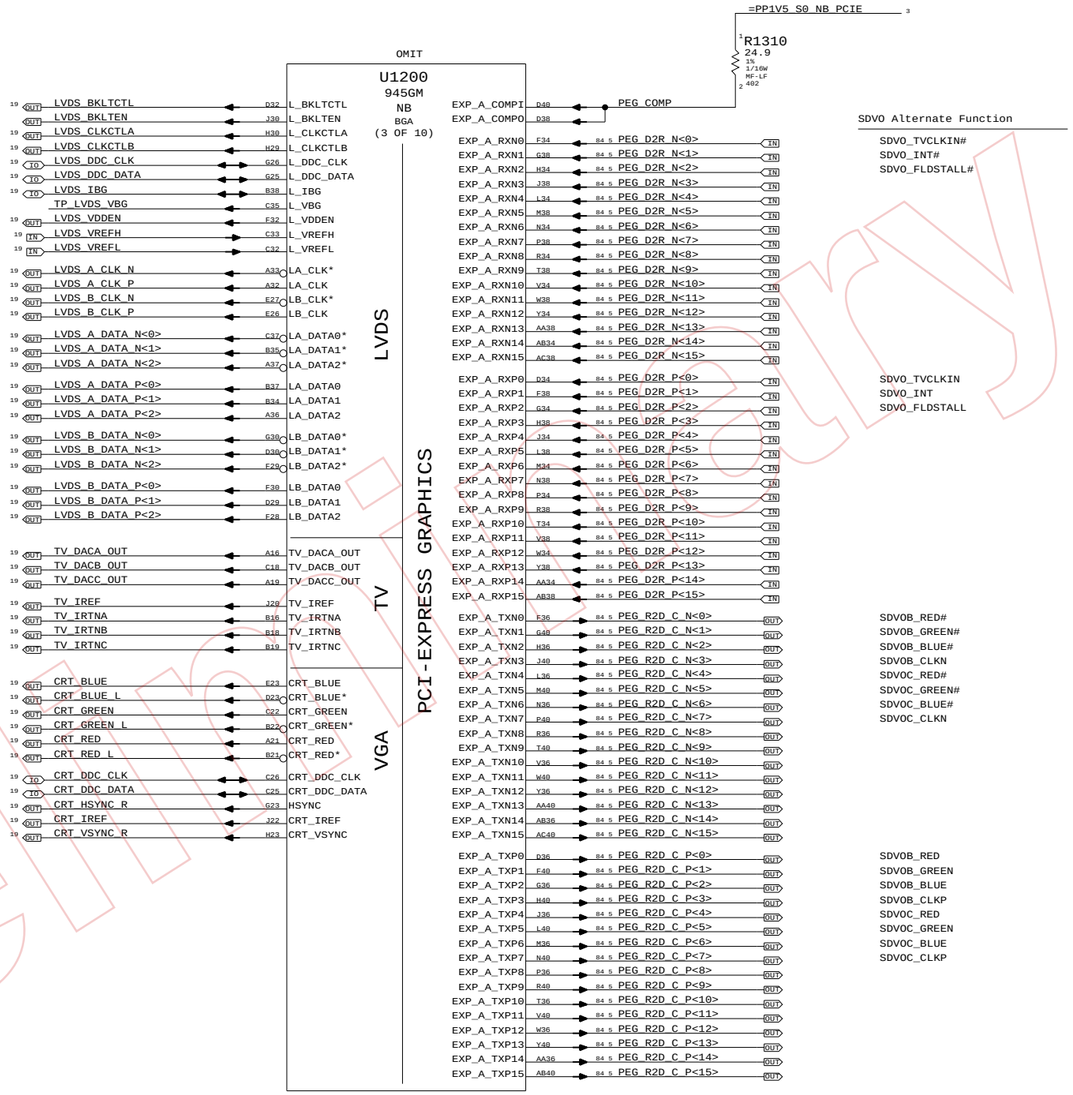
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

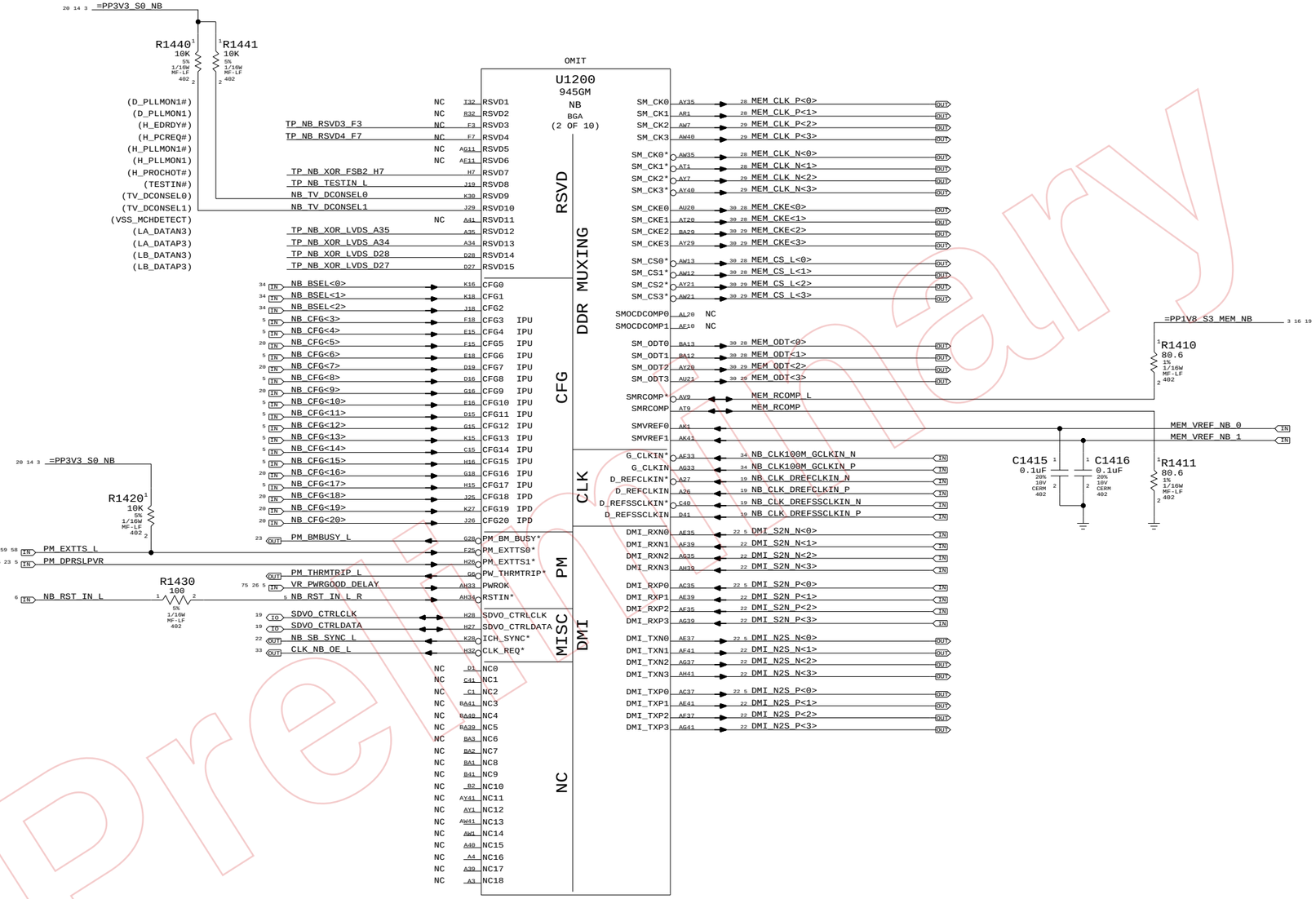


NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 13 OF 97	



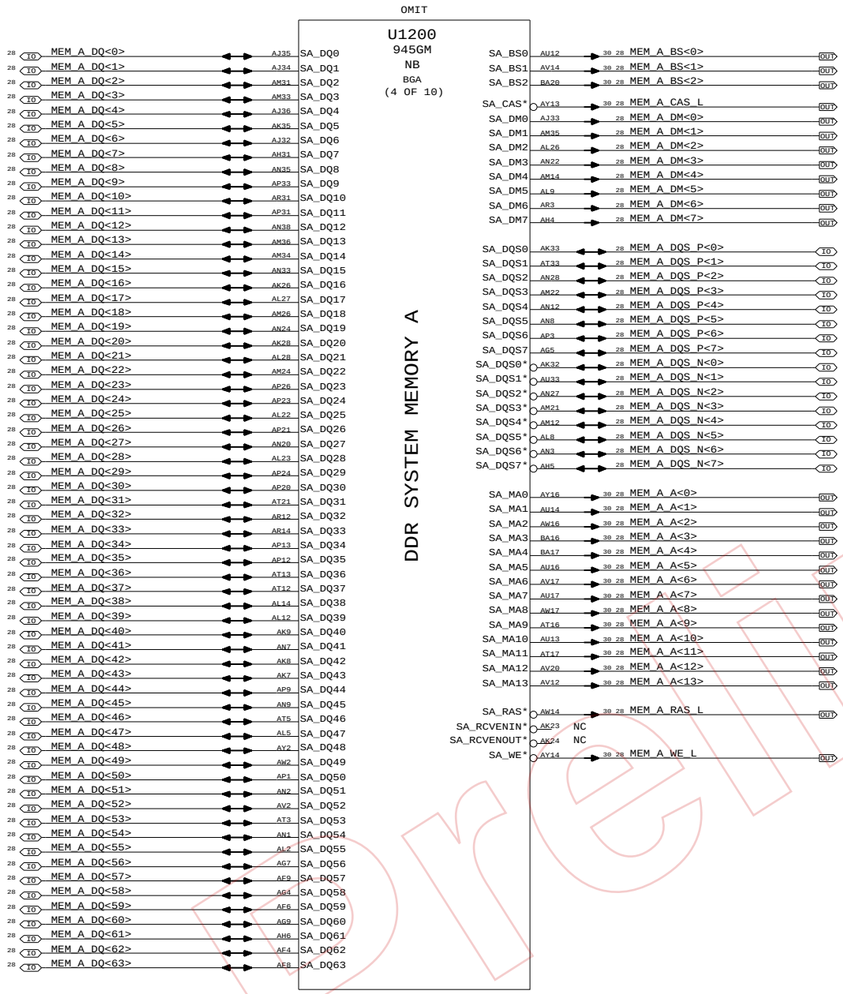
NB Misc Interfaces

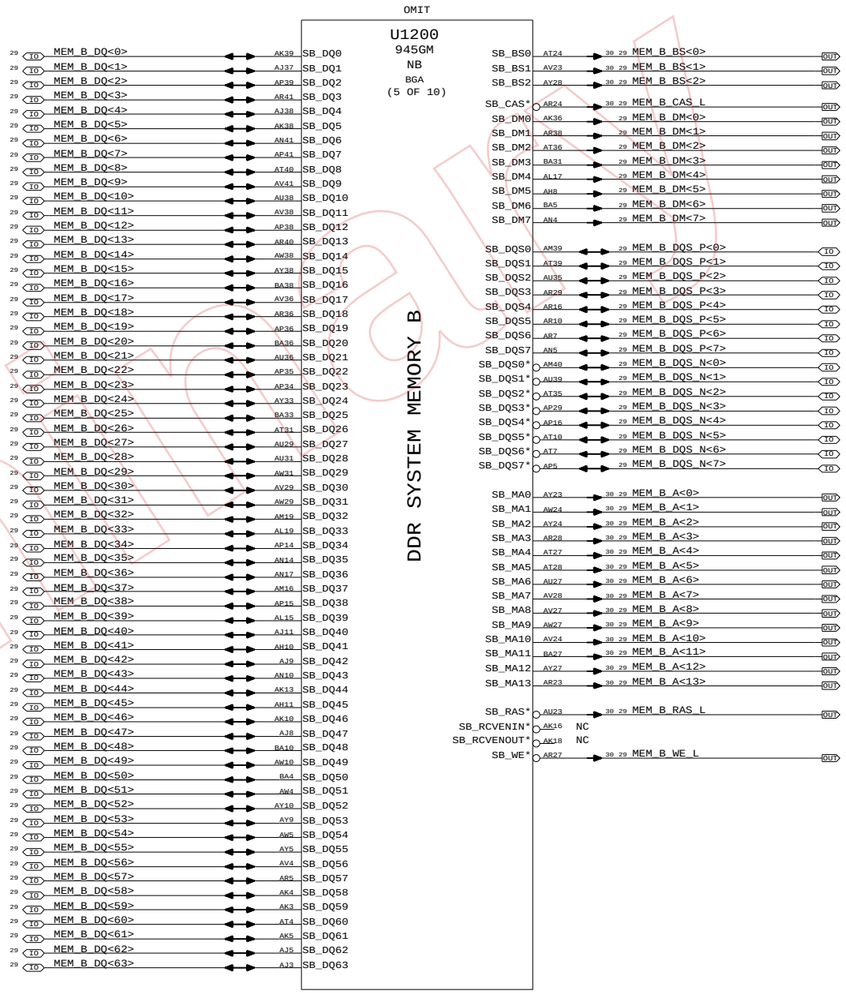
SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE: NONE SHT 14 OF 97





NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 15 OF 97	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 3 16 19

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) OMIT VCC

VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402

C1613 0.47uF 20% 6.3V CERM-X5R 402

C1615 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA23

19 14 3 =PP1V8_S3_MEM_NB

C1620 10UF 20% 6.3V CERM 805-1

C1621 10UF 20% 6.3V CERM 805-1

Layout Note: Place in cavity (Need to better define cavity)

C1610 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA15

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 0.47uF 20% 6.3V CERM-X5R 402

C1611 0.47uF 20% 6.3V CERM-X5R 402

19 16 3 =PPVCORE_S0_NB

OMIT

U1200 945GM NB BGA (7 OF 10) NCTF

VCC_NCTF0 VCC_NCTF1 VCC_NCTF2 VCC_NCTF3 VCC_NCTF4 VCC_NCTF5 VCC_NCTF6 VCC_NCTF7 VCC_NCTF8 VCC_NCTF9 VCC_NCTF10 VCC_NCTF11 VCC_NCTF12 VCC_NCTF13 VCC_NCTF14 VCC_NCTF15 VCC_NCTF16 VCC_NCTF17 VCC_NCTF18 VCC_NCTF19 VCC_NCTF20 VCC_NCTF21 VCC_NCTF22 VCC_NCTF23 VCC_NCTF24 VCC_NCTF25 VCC_NCTF26 VCC_NCTF27 VCC_NCTF28 VCC_NCTF29 VCC_NCTF30 VCC_NCTF31 VCC_NCTF32 VCC_NCTF33 VCC_NCTF34 VCC_NCTF35 VCC_NCTF36 VCC_NCTF37 VCC_NCTF38 VCC_NCTF39 VCC_NCTF40 VCC_NCTF41 VCC_NCTF42 VCC_NCTF43 VCC_NCTF44 VCC_NCTF45 VCC_NCTF46 VCC_NCTF47 VCC_NCTF48 VCC_NCTF49 VCC_NCTF50 VCC_NCTF51 VCC_NCTF52 VCC_NCTF53 VCC_NCTF54 VCC_NCTF55 VCC_NCTF56 VCC_NCTF57 VCC_NCTF58 VCC_NCTF59 VCC_NCTF60 VCC_NCTF61 VCC_NCTF62 VCC_NCTF63 VCC_NCTF64 VCC_NCTF65 VCC_NCTF66 VCC_NCTF67 VCC_NCTF68 VCC_NCTF69 VCC_NCTF70 VCC_NCTF71 VCC_NCTF72

VSS_NCTF0 VSS_NCTF1 VSS_NCTF2 VSS_NCTF3 VSS_NCTF4 VSS_NCTF5 VSS_NCTF6 VSS_NCTF7 VSS_NCTF8 VSS_NCTF9 VSS_NCTF10 VSS_NCTF11 VSS_NCTF12

=PP1V5_S0_NB_VCCAUX 3 17 19

VCCAUX_NCTF0 VCCAUX_NCTF1 VCCAUX_NCTF2 VCCAUX_NCTF3 VCCAUX_NCTF4 VCCAUX_NCTF5 VCCAUX_NCTF6 VCCAUX_NCTF7 VCCAUX_NCTF8 VCCAUX_NCTF9 VCCAUX_NCTF10 VCCAUX_NCTF11 VCCAUX_NCTF12 VCCAUX_NCTF13 VCCAUX_NCTF14 VCCAUX_NCTF15 VCCAUX_NCTF16 VCCAUX_NCTF17 VCCAUX_NCTF18 VCCAUX_NCTF19 VCCAUX_NCTF20 VCCAUX_NCTF21 VCCAUX_NCTF22 VCCAUX_NCTF23 VCCAUX_NCTF24 VCCAUX_NCTF25 VCCAUX_NCTF26 VCCAUX_NCTF27 VCCAUX_NCTF28 VCCAUX_NCTF29 VCCAUX_NCTF30 VCCAUX_NCTF31 VCCAUX_NCTF32 VCCAUX_NCTF33 VCCAUX_NCTF34 VCCAUX_NCTF35 VCCAUX_NCTF36 VCCAUX_NCTF37 VCCAUX_NCTF38 VCCAUX_NCTF39 VCCAUX_NCTF40 VCCAUX_NCTF41 VCCAUX_NCTF42 VCCAUX_NCTF43 VCCAUX_NCTF44 VCCAUX_NCTF45 VCCAUX_NCTF46 VCCAUX_NCTF47 VCCAUX_NCTF48 VCCAUX_NCTF49 VCCAUX_NCTF50 VCCAUX_NCTF51 VCCAUX_NCTF52 VCCAUX_NCTF53 VCCAUX_NCTF54 VCCAUX_NCTF55 VCCAUX_NCTF56 VCCAUX_NCTF57

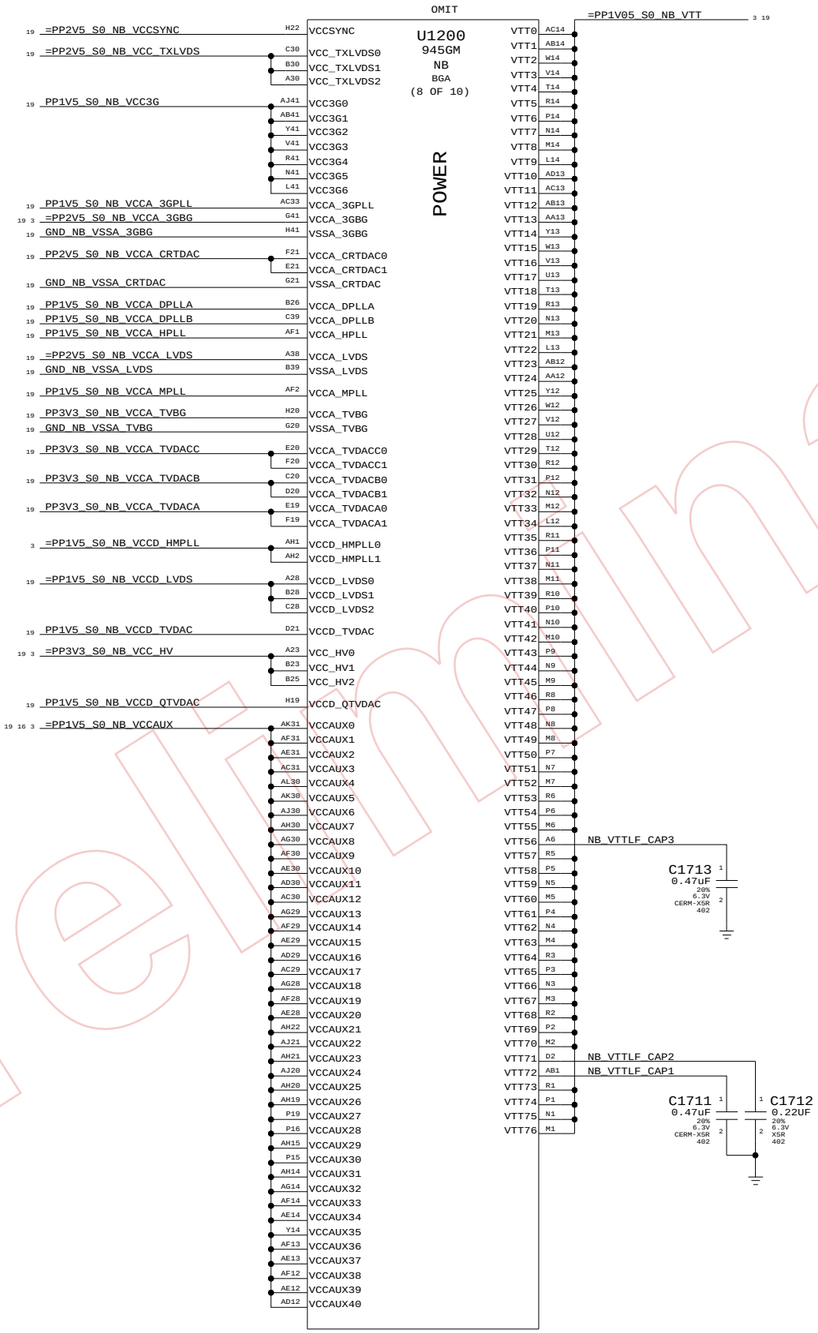
NB Power 1

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE	SHT
NONE	16 OF 97

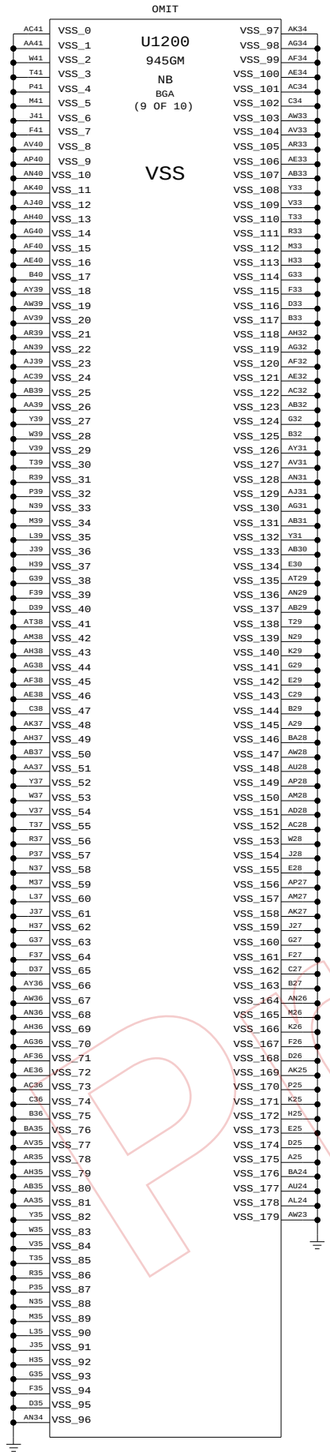


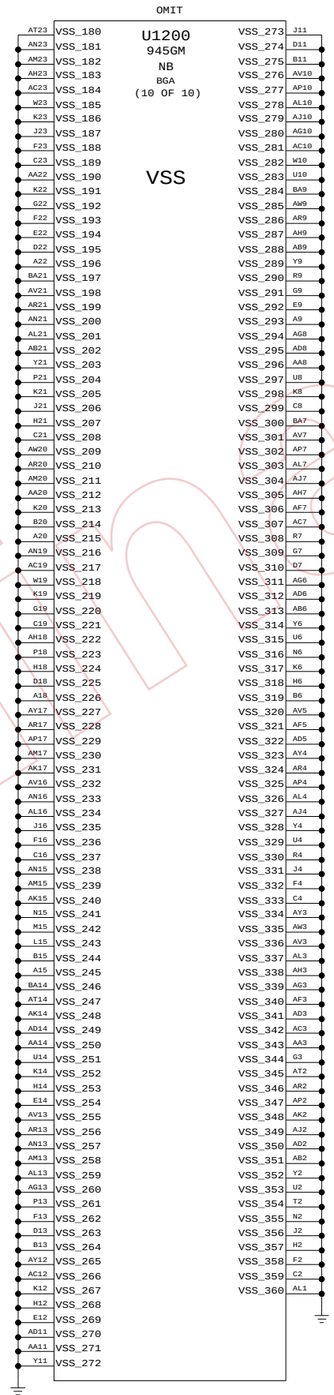
NB Power 2

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 17 OF 97	



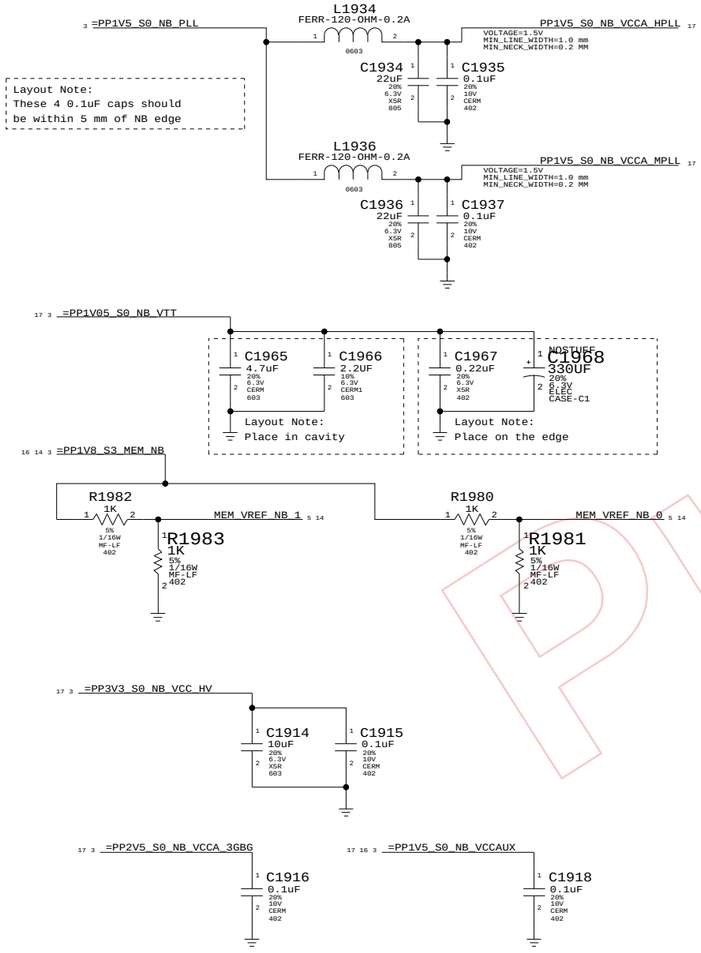


NB Grounds

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 18 OF 97	



TVOUT DISABLE

16 3 19 =PPVCORE_S0_NB
PP2V5_S0_NB_VCCA_CRTDAC 17
CRT_RED 13
CRT_RED_L 13
CRT_GREEN 13
CRT_GREEN_L 13
CRT_BLUE 13
CRT_BLUE_L 13
CRT_IREF 13
CRT_VSYNC_R 13
CRT_HSYNC_R 13
=PP2V5_S0_NB_VCCSYNC 17
GND_NB_VSSA_CRTDAC 17
TP_CRT_DDC_CLK TRUE CRT_DDC_CLK 13
TP_CRT_DDC_DATA TRUE CRT_DDC_DATA 13

DISPLAY DISABLE

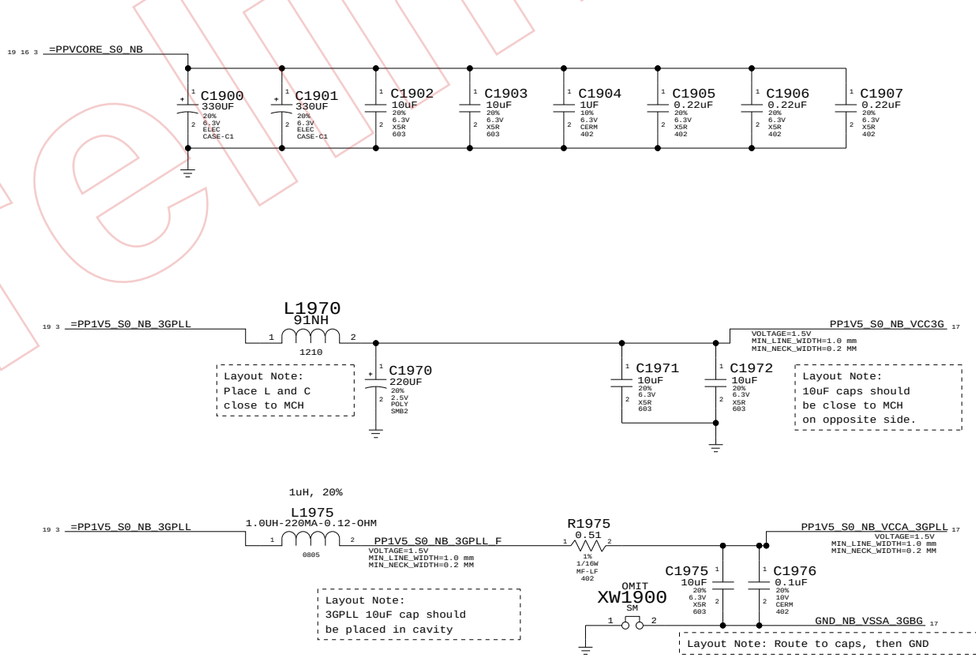
TP_NB_VCCA_DPLLA TRUE PP1V5_S0_NB_VCCA_DPLLA 17
TP_NB_VCCA_DPLLB TRUE PP1V5_S0_NB_VCCA_DPLLB 17
NB_CLK_DREFCLKIN_N 14
NB_CLK_DREFCLKIN_P 14
NB_CLK_DREFSSCLKIN_P 14
NB_CLK_DREFSSCLKIN_N 14

LVDS DISABLE

13 LVDS_A_CLK_N TRUE TP_LVDS_A_CLK_N
13 LVDS_A_CLK_P TRUE TP_LVDS_A_CLK_P
13 LVDS_B_CLK_N TRUE TP_LVDS_B_CLK_N
13 LVDS_B_CLK_P TRUE TP_LVDS_B_CLK_P
13 LVDS_A_DATA_N<0> TRUE TP_LVDS_A_DATA_N<0>
13 LVDS_A_DATA_N<1> TRUE TP_LVDS_A_DATA_N<1>
13 LVDS_A_DATA_N<2> TRUE TP_LVDS_A_DATA_N<2>
13 LVDS_A_DATA_P<0> TRUE TP_LVDS_A_DATA_P<0>
13 LVDS_A_DATA_P<1> TRUE TP_LVDS_A_DATA_P<1>
13 LVDS_A_DATA_P<2> TRUE TP_LVDS_A_DATA_P<2>
13 LVDS_B_DATA_N<0> TRUE TP_LVDS_B_DATA_N<0>
13 LVDS_B_DATA_N<1> TRUE TP_LVDS_B_DATA_N<1>
13 LVDS_B_DATA_N<2> TRUE TP_LVDS_B_DATA_N<2>
13 LVDS_B_DATA_P<0> TRUE TP_LVDS_B_DATA_P<0>
13 LVDS_B_DATA_P<1> TRUE TP_LVDS_B_DATA_P<1>
13 LVDS_B_DATA_P<2> TRUE TP_LVDS_B_DATA_P<2>
13 5 LVDS_BKLTEN TRUE TP_LVDS_BKLTEN 5
13 LVDS_VDDEN TRUE TP_LVDS_VDDEN
13 LVDS_IBG TRUE TP_LVDS_IBG
17 GND_NB_VSSA_LVDS TRUE TP_GND_NB_VSSA_LVDS
13 LVDS_VREFH TRUE TP_LVDS_VREFH
13 LVDS_VREFL TRUE TP_LVDS_VREFL
17 =PP2V5_S0_NB_VCCA_LVDS
17 =PP1V5_S0_NB_VCCD_LVDS
17 =PP2V5_S0_NB_VCC_TXLVDS
13 LVDS_BKLTCTL TRUE TP_LVDS_BKLTCTL
13 LVDS_CLKCTLA TRUE TP_LVDS_CLKCTLA
13 LVDS_CLKCTLB TRUE TP_LVDS_CLKCTLB
13 LVDS_DDC_CLK TRUE TP_LVDS_DDC_CLK
13 LVDS_DDC_DATA TRUE TP_LVDS_DDC_DATA

TVOUT DISABLE

3 =PP1V5_S0_NB
PP3V3_S0_NB_VCCA_TVDACA 17
PP3V3_S0_NB_VCCA_TVDACB 17
PP3V3_S0_NB_VCCA_TVDACC 17
PP3V3_S0_NB_VCCA_TVBG 17
TV_DACA_OUT 13
TV_DACB_OUT 13
TV_DACC_OUT 13
TV_IREF 13
TV_IRTNA 13
TV_IRTNB 13
TV_IRTNC 13
GND_NB_VSSA_TVBG 17
3 =PP1V5_S0_NB_TVDAC
PP1V5_S0_NB_VCCD_TVDAC 17
PP1V5_S0_NB_VCCD_QTVDAC 17
14 SDVO_CTRLCLK TRUE TP_SDVO_CTRLCLK
14 SDVO_CTRLDATA TRUE TP_SDVO_CTRLDATA



NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075 2.2K 5% 1/16W MF-LF 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077 2.2K 5% 1/16W MF-LF 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079 2.2K 5% 1/16W MF-LF 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085 2.2K 5% 1/16W MF-LF 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058 2.2K 5% 1/16W MF-LF 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059 2.2K 5% 1/16W MF-LF 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060 2.2K 5% 1/16W MF-LF 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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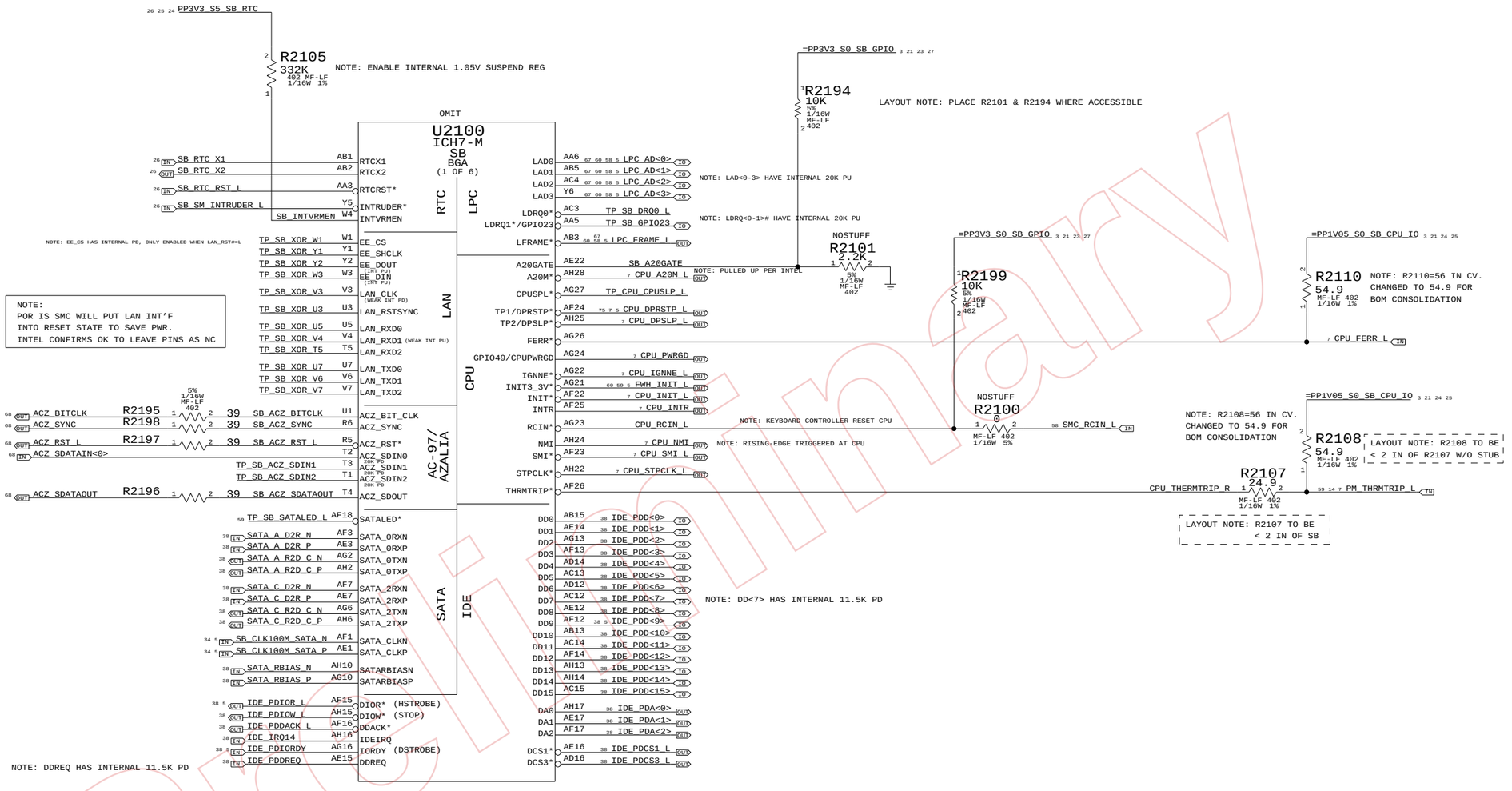
SCALE NONE SHT 20 OF 97



NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
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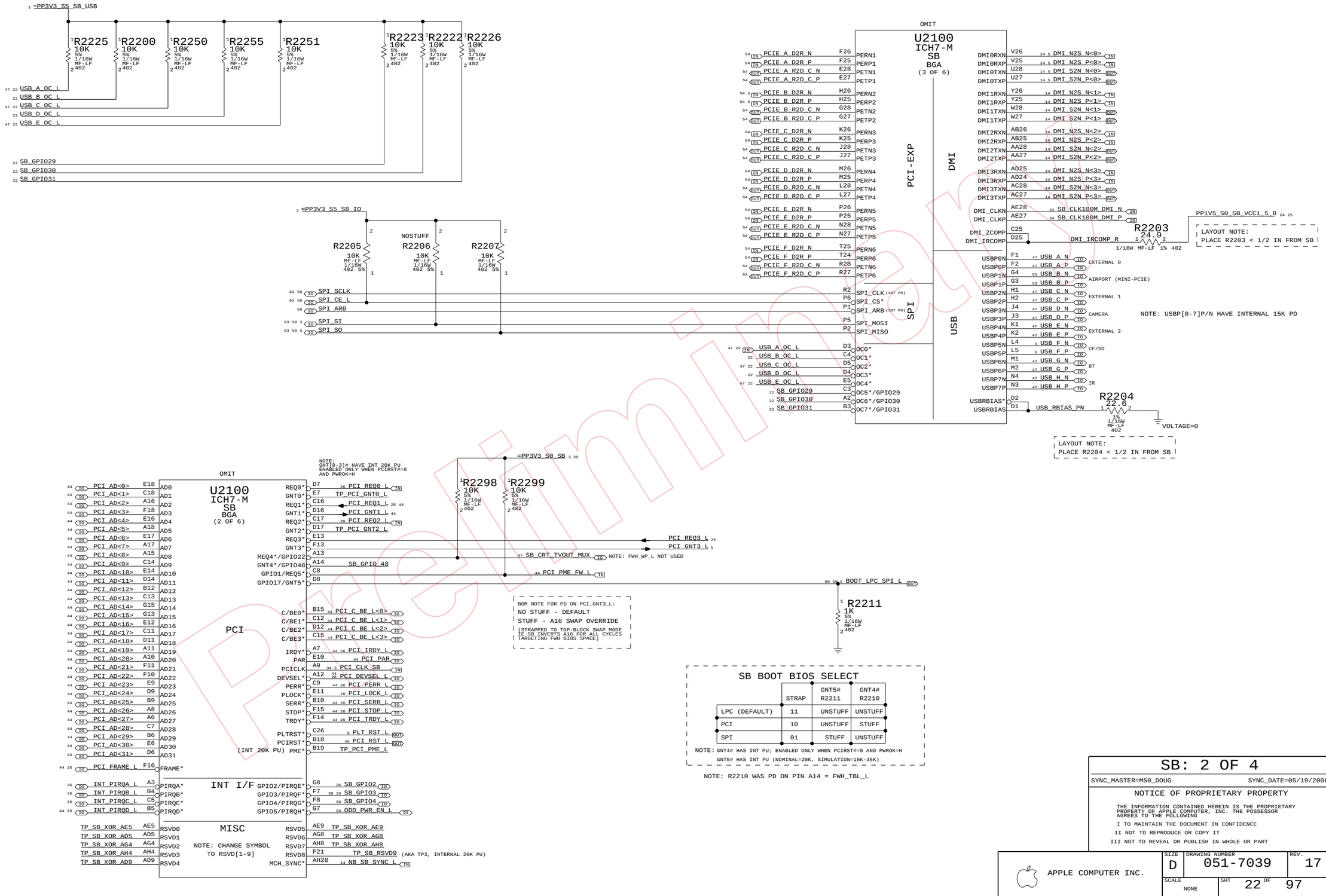
=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2222 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCI-EXP
DMI
SPI
USB
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
SPI_CLK
SPI_CS*
SPI_ARB
SPI_MOSI
SPI_MISO
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2203 24.9 1% 1/16W MF-LF 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
R2204 22.6 1% 1/16W MF-LF 402
USB_RBIAS_PN
VOLTAGE=0
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
PCI
INT I/F
MISC
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
TP_SB_XOR_AE5
TP_SB_XOR_AD5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AD9
NOTE: CHANGE SYMBOL TO RSVD[1-9]
REQ0*
GNT0*
REQ1*
GNT1*
REQ2*
GNT2*
REQ3*
GNT3*
REQ4*/GPIO22
GNT4*/GPIO48
GPIO1/REQ5*
GPIO17/GNT5*
PCI_REQ0_L
TP_PCI_GNT0_L
PCI_REQ1_L
PCI_GNT1_L
PCI_REQ2_L
TP_PCI_GNT2_L
PCI_REQ3_L
PCI_GNT3_L
SB_CRT_TVOUT_MUX
SB_GPIO_48
PCI_PME_FW_L
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IE SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
C/BE0*
C/BE1*
C/BE2*
C/BE3*
IRDY*
PAR
PCICLK
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
PLTRST*
PCIRST*
(INT 20K PU) PME*
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
GPIO2/PIRQE*
GPIO3/PIRQF*
GPIO4/PIRQG*
GPIO5/PIRQH*
SB_GPIO2
SB_GPIO3
SB_GPIO4
ODD_PWR_EN_L
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
NB_SB_SYNC_L
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
SYNC_MASTER=M50_DOUG
SYNC_DATE=05/19/2006
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SIZE D
DRAWING NUMBER 051-7039
REV. 17
SCALE NONE
SHT 22 OF 97

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 3 21 23 27

=PP3V3_S5_SB 3 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

26 25 23 3 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 TO SMB_CLK	C22	SMBCLK
27 TO SMB_DATA	B22	SMBDATA
SMB_LINK_ALERT_L	A26	LINKALERT*
SMLINK<0>	B25	SMLINK0
SMLINK<1>	A25	SMLINK1
NOT USED		
PM_RI_L	A28	RI*
SB_SPKR	A19	SPKR (INT WEAK PD)
67 60 58 5 OUT PM_SUS_STAT_L	A27	SUS_STAT*
58 26 IN PM_SYSRST_L	A22	SYS_RST*
14 IN PM_BMBUSY_L	AB18	GPIO0/BM_BUSY*
SMB_ALERT_L NOTE: RESERVED FOR FUTURE	B23	GPIO11/SMBALERT*
33 OUT PM_STPPCI_L	AC20	GPIO18/STPPCI*
33 OUT PM_STPCPU_L	AF21	GPIO20/STPCPU*
SB_GPIO26	A21	GPIO26
23 BIOS_REC	B21	GPIO27
23 FWH_MFG_MODE	E23	GPIO28
67 60 58 5 TO PM_CLKRUN_L	AG18	GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F TP_AZ_DOCK_EN_L	AC19	GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L	U2	GPIO34/AZ_DOCK_RST*
53 41 IN PCIE_WAKE_L	F20	WAKE*
67 60 58 5 TO INT_SERIRQ	AH21	SERIRQ
58 10 IN PM_THRM_L	AF20	THRM*
26 5 IN VR_PWRGD_CK410	AD22	VRMPWRGD
6 GPU_PRESENT_R	AC21	GPIO6
58 IN SMC_RUNTIME_SCI_L	AC18	GPIO7
58 IN SMC_EXTSMI_L	E21	GPIO8

SATA GPIO

GPIO21/SATA0GP	AF19	SB_GPIO21 100 R2302
GPIO19/SATA1GP	AH18	SB_GPIO19 100 R2303
GPIO36/SATA2GP	AH19	
GPIO37/SATA3GP	AE19	SB_GPIO37 100 R2305

38 SATA_C_DET_L IN

CLKS

CLK14	AC1	34 5 SB_CLK14P3M_TIMER IN
CLK48	B2	34 5 SB_CLK48M_USBCTLR IN
SUSCLK	C20	59 SUS_CLK_SB OUT

SYS GPIO
PWR MNGT

SLP_S3*	B24	79 77 58 5 PM_SLP_S3_L OUT
SLP_S4*	D23	77 58 5 PM_SLP_S4_L OUT
SLP_S5*	F22	58 PM_SLP_S5_L OUT
PWROK	AA4	26 PM_SB_PWROK IN
GPIO16/DPRSLPVR	AC22	75 14 5 PM_DPRSLPVR OUT
TP0/BATLOW*	C21	NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN*	C23	58 PM_PWRBTN_L IN
LAN_RST*	C19	58 PM_LAN_ENABLE IN
RSMRST*	Y4	

NOTE:
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F
IN RESET STATE TO SAVE PWR

58 PM_BATLOW_L IN

58 PM_RSMRST_L IN

R2399 100K 5% 1/16W 402 MF-LF

GPIO

GPIO9	E20	58 26 SMS_INT_L IN
GPIO10	A20	58 SMC_SB_NMI IN
DEF=GPI GPIO12	F19	23 PATA_PWR_EN_L OUT
GPIO13	E19	
DEF=GPI GPIO14	R4	38 IDE_RESET_L OUT
GPIO15	E22	SV_SET_UP 5 23 60
GPIO24	R3	TP_SB_GPIO24
GPIO25	D20	TP_SB_GPIO25_DO_NOT_USE
OD GPIO35	AD21	33 SB_CLK100M_SATA_OE_L OUT
GPIO38	AD20	TP_SB_GPIO38 TO
DEF=GPI GPIO39	AE20	23 SATA_C_PWR_EN_L OUT

58 SMC_WAKE_SCI_L IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 3 11

R2387 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

26 25 23 3 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 10K 1/16W 402 MF-LF 5%

SV_SET_UP 5 23 60
EFI_OK_R

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 3 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 3 23 25 26

R2390 10K 5% 1/16W MF-LF 402

23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 3 21 23 27

R2388 10K 5% 1/16W MF-LF 402

23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

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SIZE	DRAWING NUMBER	REV.
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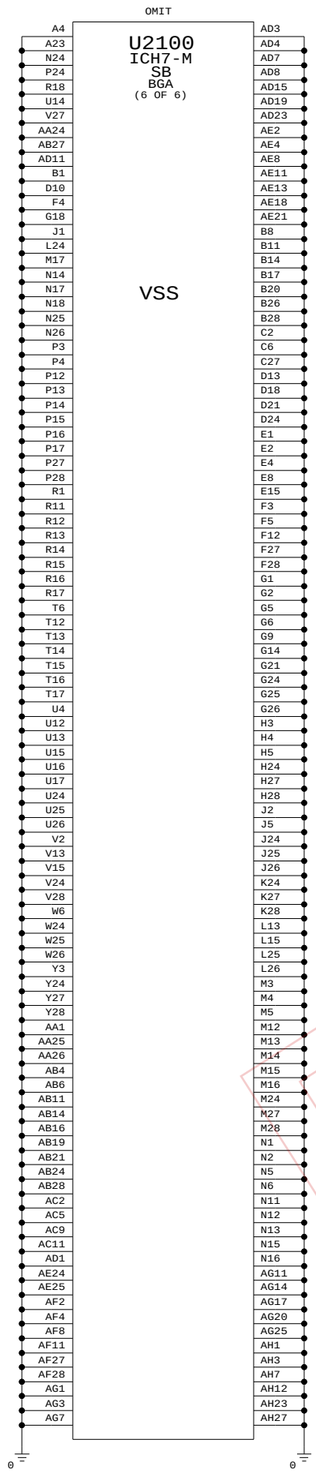
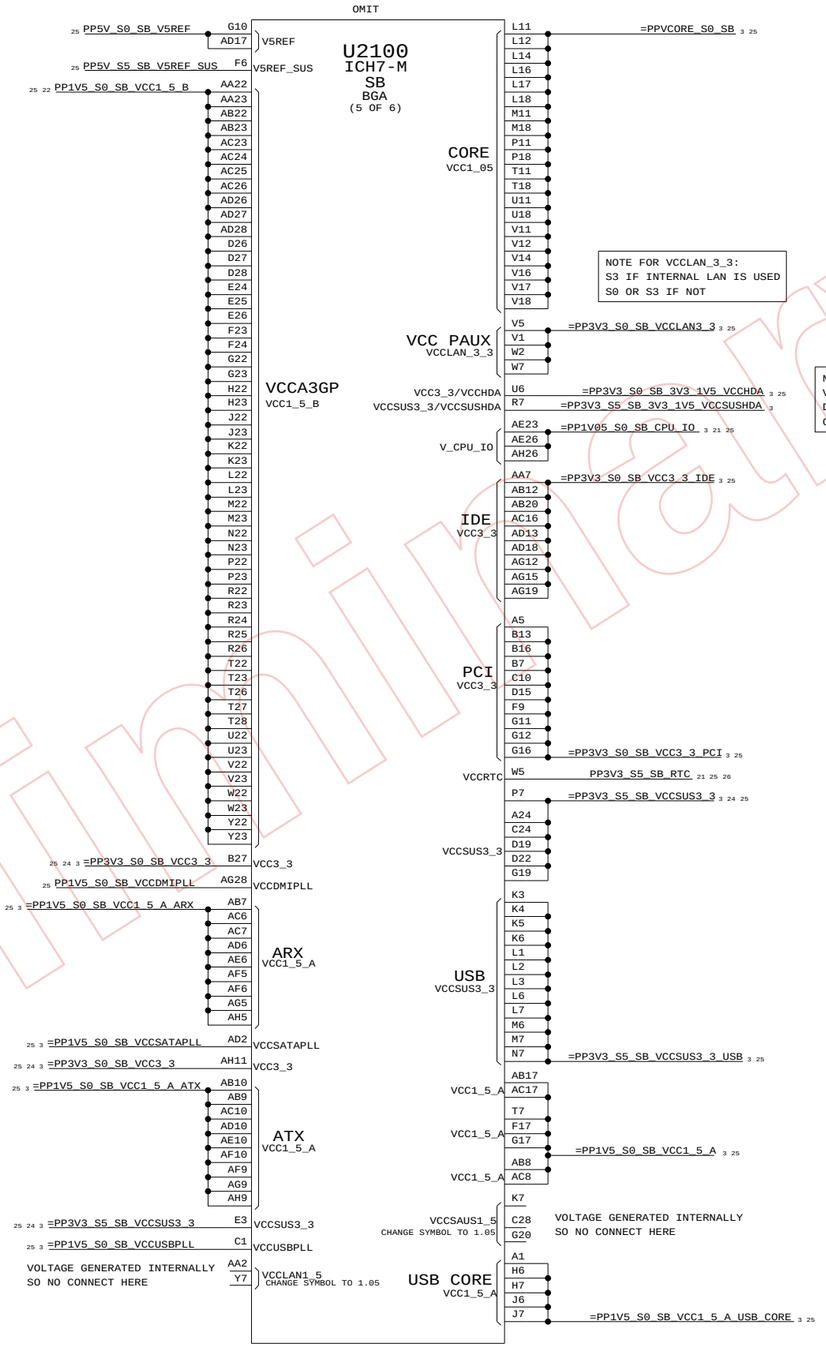
SCALE: NONE	SHT 23 OF 97	



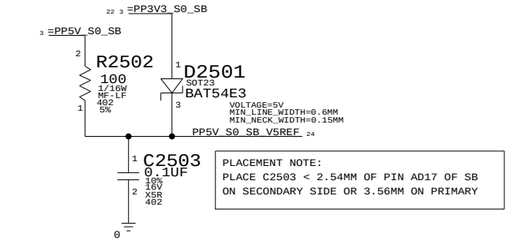


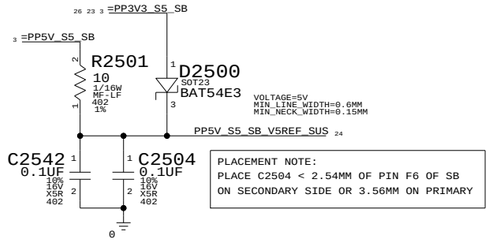
SB: 4 OF 4

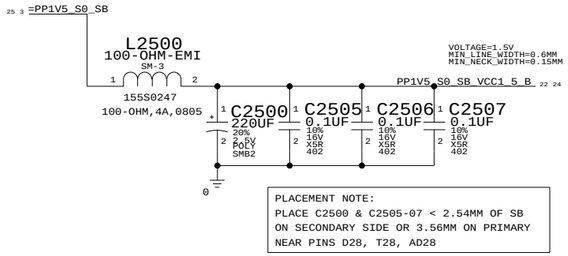
SYNC_MASTER=M50_DOUG SYNC_DATE=05/19/2006

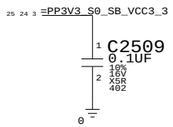
APPLE COMPUTER INC.

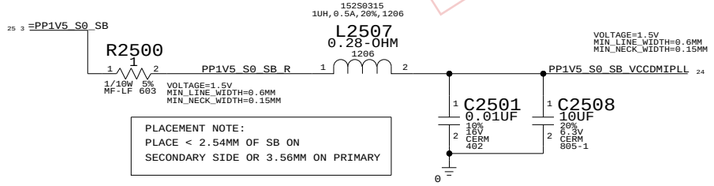
SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 24 OF 97	

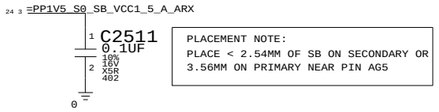


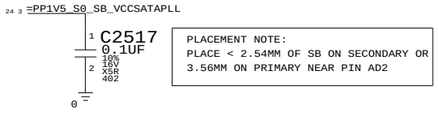


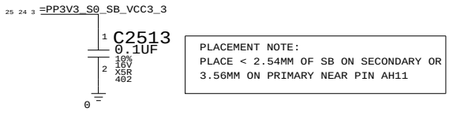


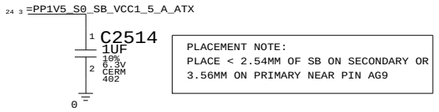


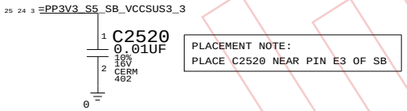


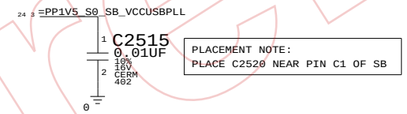


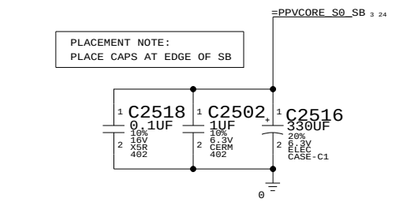


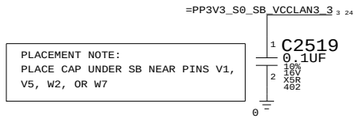


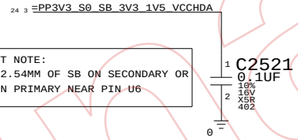


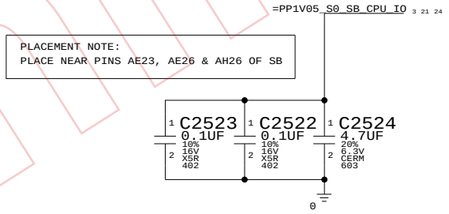


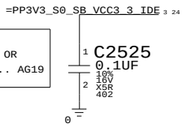


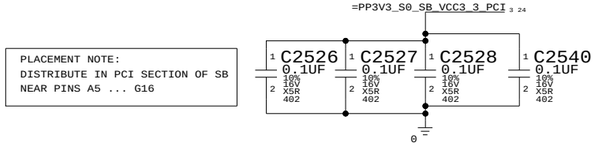


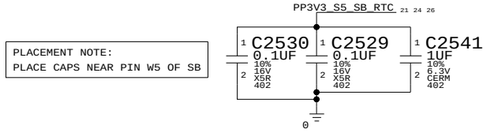


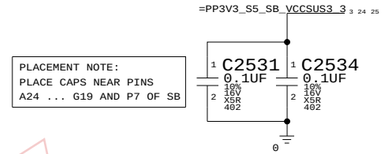


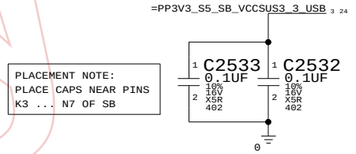


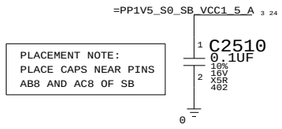


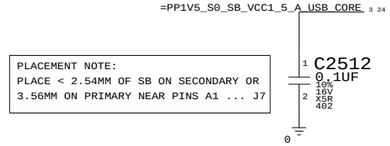












SB:DECOUPLING

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

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APPLE COMPUTER INC.

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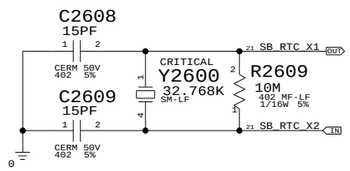
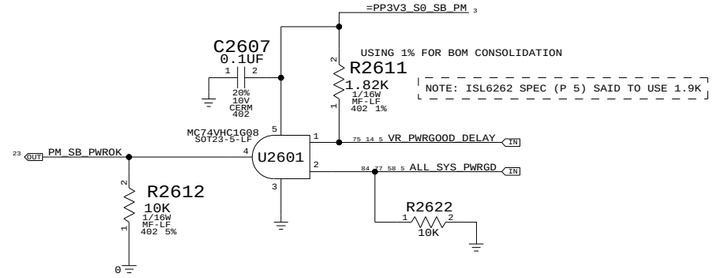
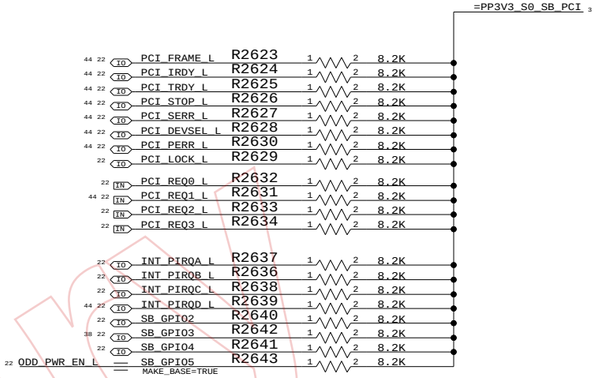
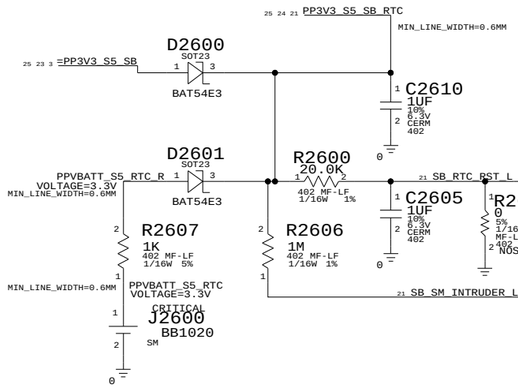
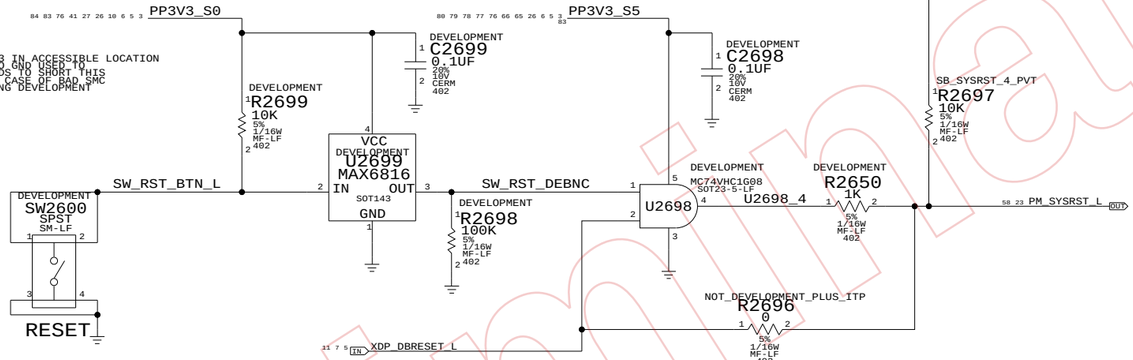
D	051-7039	17
SCALE: NONE	SHT 25 OF 97	

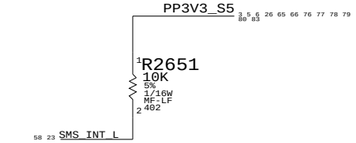


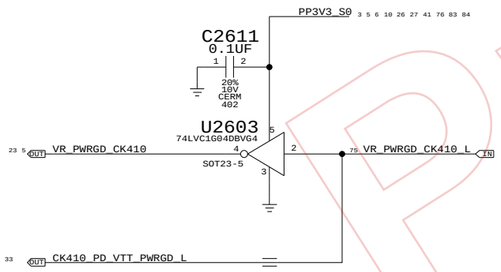












SB: MISC

SYNC_MASTER=M50_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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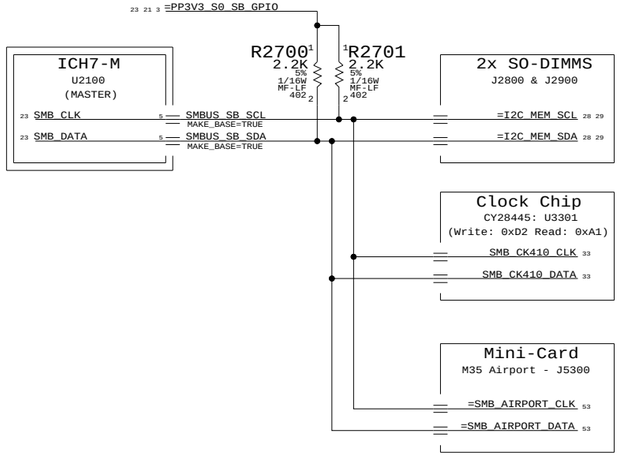
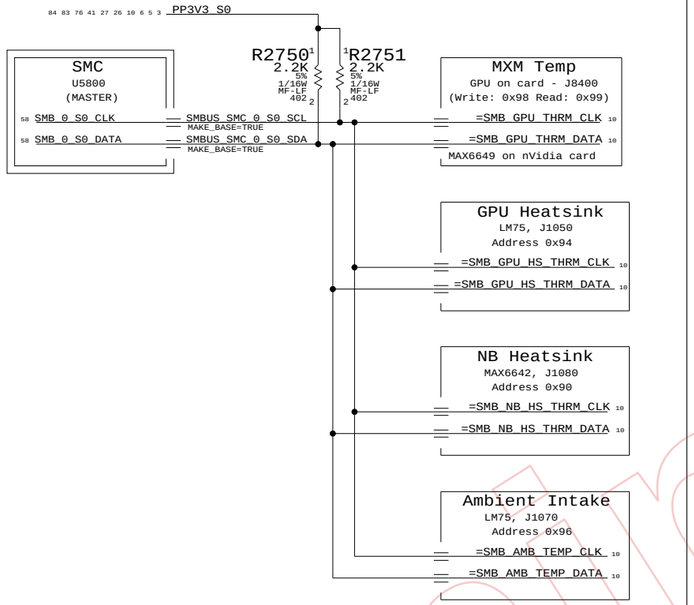
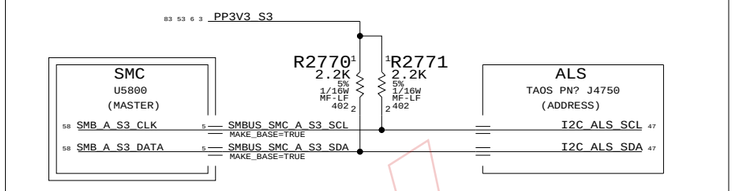
ICH7-M SMBus Connections



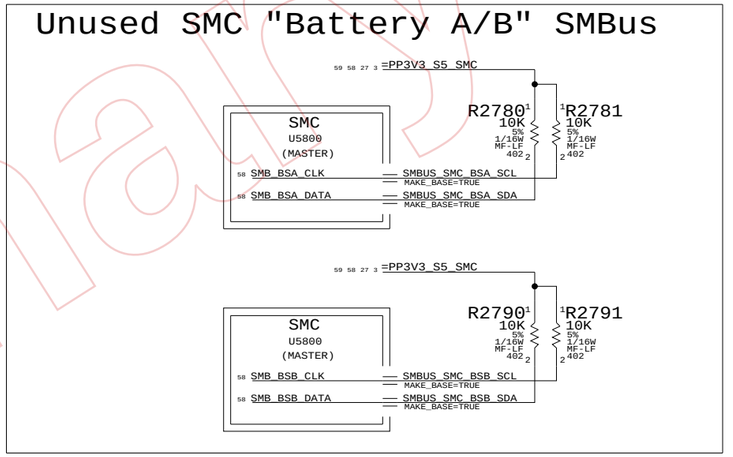
SMC "0" SMBus Connections



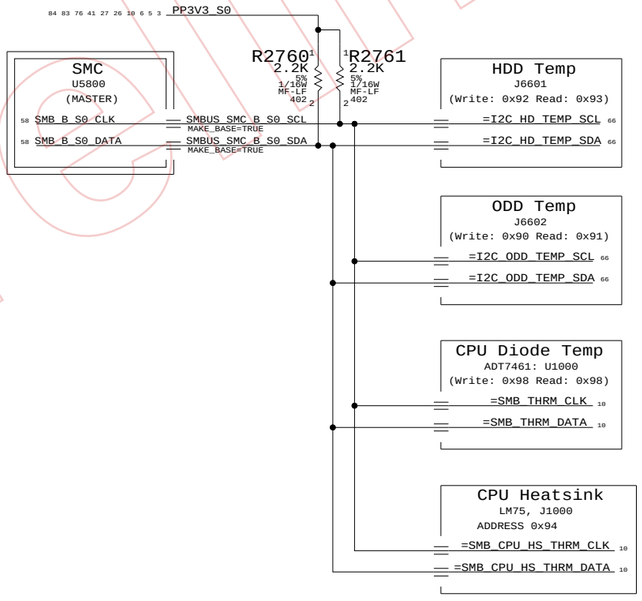
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 27 OF 97	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

=PP1V8_S3_MEM (29 28 3)

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF (28 29)
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

MEM_VREF (29 28)

C2850 2.2UF 10% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM (29 28 3)

J2800

CRITICAL
F-RT-SM1
DDR2-SODIMM-STD

	VREF	1	2	VSS0			
	VSS1	3	4	DQ4	MEM_A_DQ<4>	15	
MEM_A_DQ<0>	DQ0	5	6	DQ5	MEM_A_DQ<5>	15	
MEM_A_DQ<1>	DQ1	7	8	VSS2			
	VSS4	9	10	DM0	MEM_A_DM<0>	15	
MEM_A_DQS_N<0>	DQS0*	11	12	VSS5			
MEM_A_DQS_P<0>	DQS0	13	14	DQ6	MEM_A_DQ<6>	15	
	VSS6	15	16	DQ7	MEM_A_DQ<7>	15	
MEM_A_DQ<2>	DQ2	17	18	VSS7			
MEM_A_DQ<3>	DQ3	19	20	DQ12	MEM_A_DQ<12>	15	
	VSS8	21	22	DQ13	MEM_A_DQ<13>	15	
MEM_A_DQ<8>	DQ8	23	24	VSS9			
MEM_A_DQ<9>	DQ9	25	26	DM1	MEM_A_DM<1>	15	
	VSS10	27	28	VSS11			
MEM_A_DQS_N<1>	DQS1*	29	30	CK0	MEM_CLK_P<0>	14	
MEM_A_DQS_P<1>	DQS1	31	32	CK0*	MEM_CLK_N<0>	14	
	VSS12	33	34	VSS13			
MEM_A_DQ<10>	DQ10	35	36	DQ14	MEM_A_DQ<14>	15	
MEM_A_DQ<11>	DQ11	37	38	DQ15	MEM_A_DQ<15>	15	
	VSS14	39	40	VSS15			
			KEY				
	VSS16	41	42	VSS17			
MEM_A_DQ<16>	DQ16	43	44	DQ20	MEM_A_DQ<20>	15	
MEM_A_DQ<17>	DQ17	45	46	DQ21	MEM_A_DQ<21>	15	
	VSS18	47	48	VSS19			
MEM_A_DQS_N<2>	DQS2*	49	50	NC0	DIMM_OVERTEMP_L	29 59	
MEM_A_DQS_P<2>	DQS2	51	52	DM2	MEM_A_DM<2>	15	
	VSS21	53	54	VSS22			
MEM_A_DQ<18>	DQ18	55	56	DQ22	MEM_A_DQ<22>	15	
MEM_A_DQ<19>	DQ19	57	58	DQ23	MEM_A_DQ<23>	15	
	VSS23	59	60	VSS24			
MEM_A_DQ<24>	DQ24	61	62	DQ28	MEM_A_DQ<28>	15	
MEM_A_DQ<25>	DQ25	63	64	DQ29	MEM_A_DQ<29>	15	
	VSS25	65	66	VSS26			
MEM_A_DM<3>	DM3	67	68	DQS3*	MEM_A_DQS_N<3>	15	
NC	NC1	69	70	DQS3	MEM_A_DQS_P<3>	15	
	VSS27	71	72	VSS28			
MEM_A_DQ<26>	DQ26	73	74	DQ30	MEM_A_DQ<30>	15	
MEM_A_DQ<27>	DQ27	75	76	DQ31	MEM_A_DQ<31>	15	
	VSS29	77	78	VSS30			
MEM_CKE<0>	CKE0	79	80	NC/CKE1	MEM_CKE<1>	14 30	
	VDD0	81	82	VDD1			
NC	NC2	83	84	NC/A15	TP_MEM_A_A<15>		
MEM_A_BS<2>	BA2	85	86	NC/A14	TP_MEM_A_A<14>		
	VDD2	87	88	VDD3			
MEM_A_A<12>	A12	89	90	A11	MEM_A_A<11>	15 30	
MEM_A_A<9>	A9	91	92	A7	MEM_A_A<7>	15 30	
MEM_A_A<8>	A8	93	94	A6	MEM_A_A<6>	15 30	
	VDD4	95	96	VDD5			
MEM_A_A<5>	A5	97	98	A4	MEM_A_A<4>	15 30	
MEM_A_A<3>	A3	99	100	A2	MEM_A_A<2>	15 30	
MEM_A_A<1>	A1	101	102	A0	MEM_A_A<0>	15 30	
	VDD6	103	104	VDD7			
MEM_A_A<10>	A10/AP	105	106	BA1	MEM_A_BS<1>	15 30	
MEM_A_BS<0>	BA0	107	108	RAS*	MEM_A_RAS_L	15 30	
MEM_A_WE_L	WE*	109	110	S0*	MEM_CS_L<0>	14 30	
	VDD8	111	112	VDD9			
MEM_A_CAS_L	CAS*	113	114	ODT0	MEM_ODT<0>	14 30	
MEM_CS_L<1>	NC/S1*	115	116	NC/A13	MEM_A_A<13>	15 30	
	VDD10	117	118	VDD11			
MEM_ODT<1>	NC/ODT1	119	120	NC3	NC		
	VSS31	121	122	VSS32			
MEM_A_DQ<32>	DQ32	123	124	DQ36	MEM_A_DQ<36>	15	
MEM_A_DQ<33>	DQ33	125	126	DQ37	MEM_A_DQ<37>	15	
	VSS33	127	128	VSS34			
MEM_A_DQS_N<4>	DQS4*	129	130	DM4	MEM_A_DM<4>	15	
MEM_A_DQS_P<4>	DQS4	131	132	VSS35			
	VSS36	133	134	DQ38	MEM_A_DQ<38>	15	
MEM_A_DQ<34>	DQ34	135	136	DQ39	MEM_A_DQ<39>	15	
MEM_A_DQ<35>	DQ35	137	138	VSS37			
	VSS38	139	140	DQ44	MEM_A_DQ<44>	15	
MEM_A_DQ<40>	DQ40	141	142	DQ45	MEM_A_DQ<45>	15	
MEM_A_DQ<41>	DQ41	143	144	VSS39			
	VSS40	145	146	DQS5*	MEM_A_DQS_N<5>	15	
MEM_A_DM<5>	DM5	147	148	DQS5	MEM_A_DQS_P<5>	15	
	VSS41	149	150	VSS42			
MEM_A_DQ<42>	DQ42	151	152	DQ46	MEM_A_DQ<46>	15	
MEM_A_DQ<43>	DQ43	153	154	DQ47	MEM_A_DQ<47>	15	
	VSS43	155	156	VSS44			
MEM_A_DQ<48>	DQ48	157	158	DQ52	MEM_A_DQ<52>	15	
MEM_A_DQ<49>	DQ49	159	160	DQ53	MEM_A_DQ<53>	15	
	VSS45	161	162	VSS46			
NC	NC_TEST	163	164	CK1	MEM_CLK_P<1>	14	
	VSS47	165	166	CK1*	MEM_CLK_N<1>	14	
MEM_A_DQS_N<6>	DQS6*	167	168	VSS48			
MEM_A_DQS_P<6>	DQS6	169	170	DM6	MEM_A_DM<6>	15	
	VSS49	171	172	VSS50			
MEM_A_DQ<50>	DQ50	173	174	DQ54	MEM_A_DQ<54>	15	
MEM_A_DQ<51>	DQ51	175	176	DQ55	MEM_A_DQ<55>	15	
	VSS51	177	178	VSS52			
MEM_A_DQ<56>	DQ56	179	180	DQ60	MEM_A_DQ<60>	15	
MEM_A_DQ<57>	DQ57	181	182	DQ61	MEM_A_DQ<61>	15	
	VSS53	183	184	VSS54			
MEM_A_DM<7>	DM7	185	186	DQS7*	MEM_A_DQS_N<7>	15	
	VSS55	187	188	DQS7	MEM_A_DQS_P<7>	15	
MEM_A_DQ<58>	DQ58	189	190	VSS56			
MEM_A_DQ<59>	DQ59	191	192	DQ62	MEM_A_DQ<62>	15	
	VSS57	193	194	DQ63	MEM_A_DQ<63>	15	
=I2C_MEM_SDA	SDA	195	196	VSS58			
=I2C_MEM_SCL	SCL	197	198	SA0			
	VDDSPD	199	200	SA1	ADDR=0xA0(WR)/0xA1(RD)		

=PP1V8_S3_MEM (3 28 29)

GND (201 202 203 204 205)

=PP1V8_S3_MEM (3 28 29)

SOME ANCHOR PINS CONNECTED TO NETS TO IMPROVE PLANE POUR

516S0403

=PPSPD_S0_MEM (29 3)

C2851 2.2UF 10% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM (29 28 3)

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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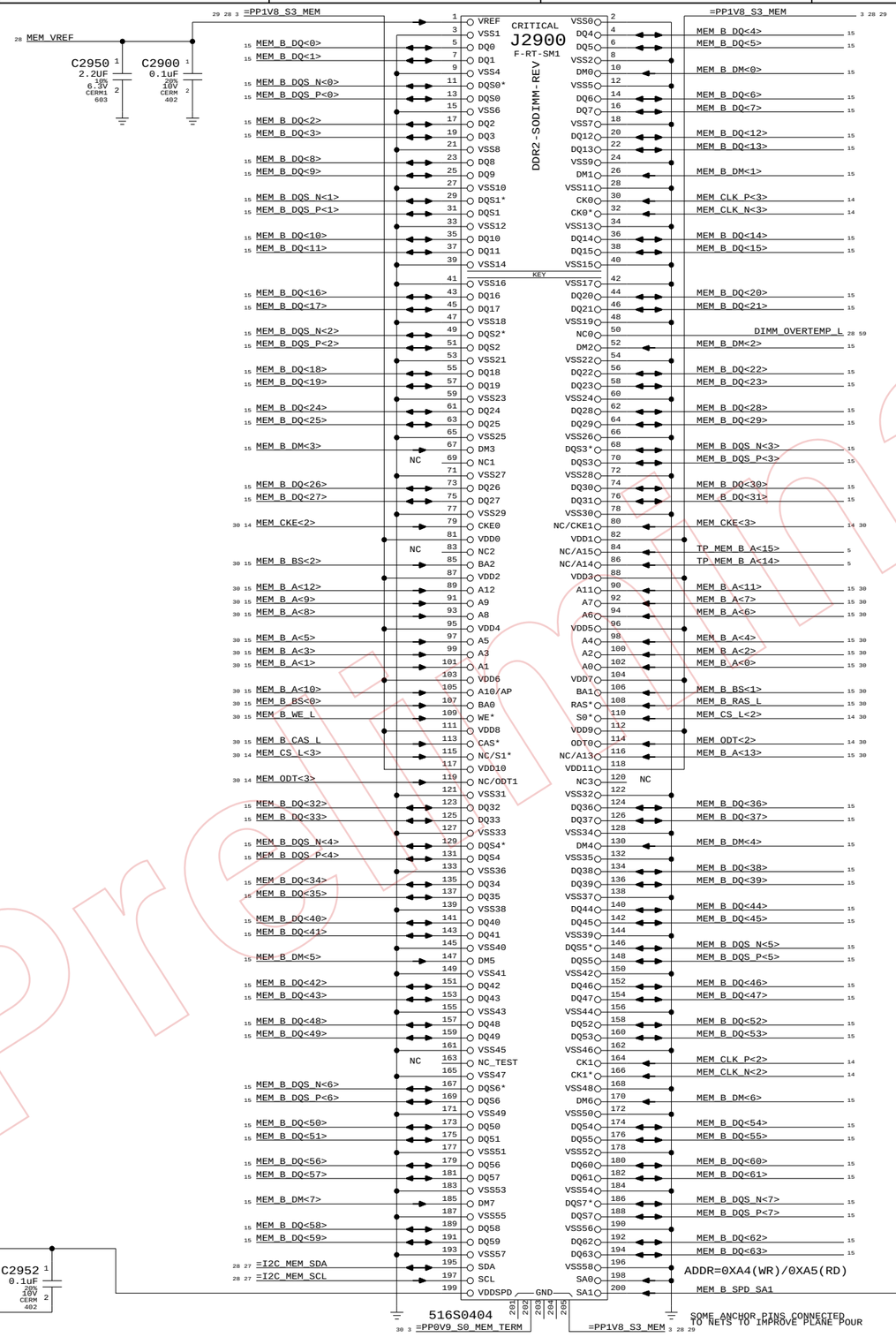
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

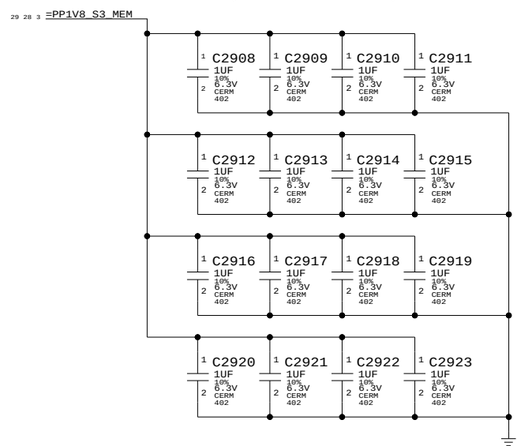
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



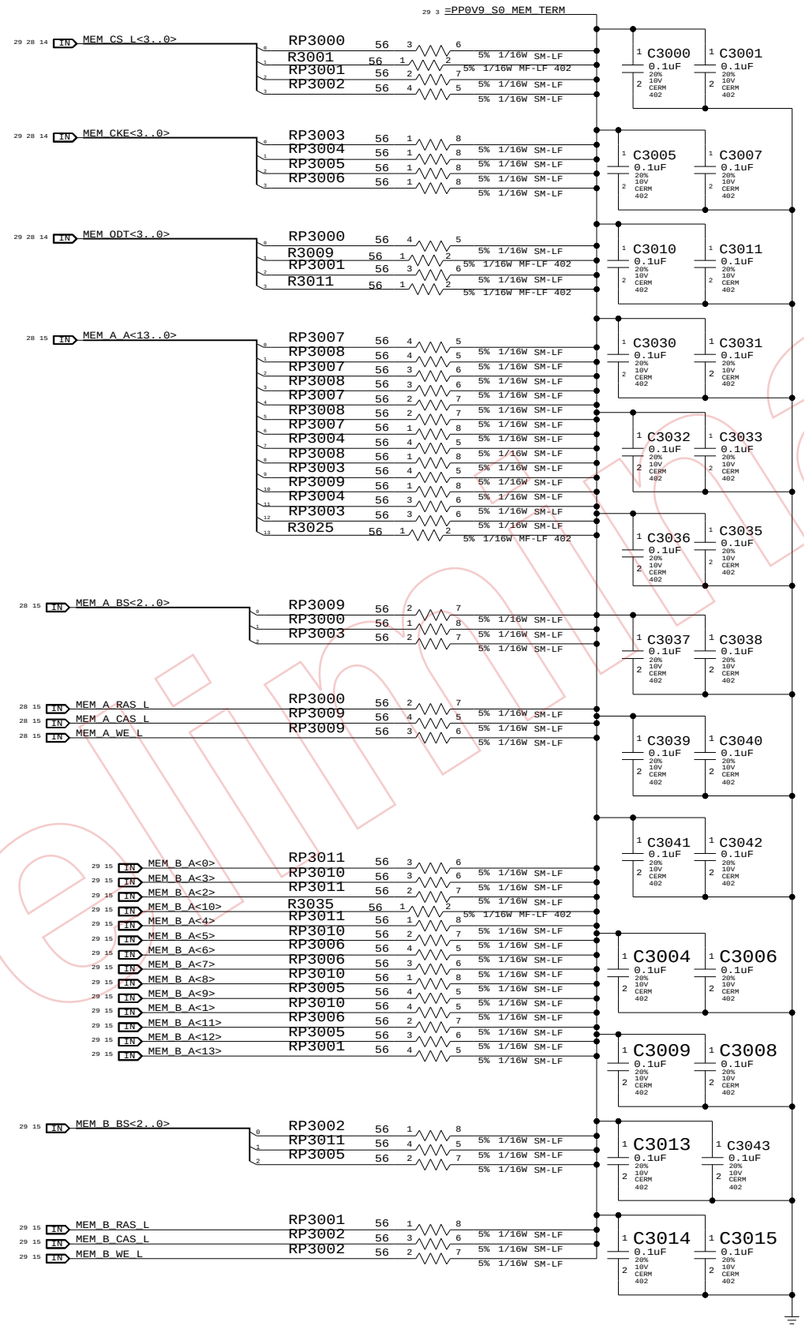
DDR2 SO-DIMM Connector B

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 29 OF 97	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 30 OF 97	

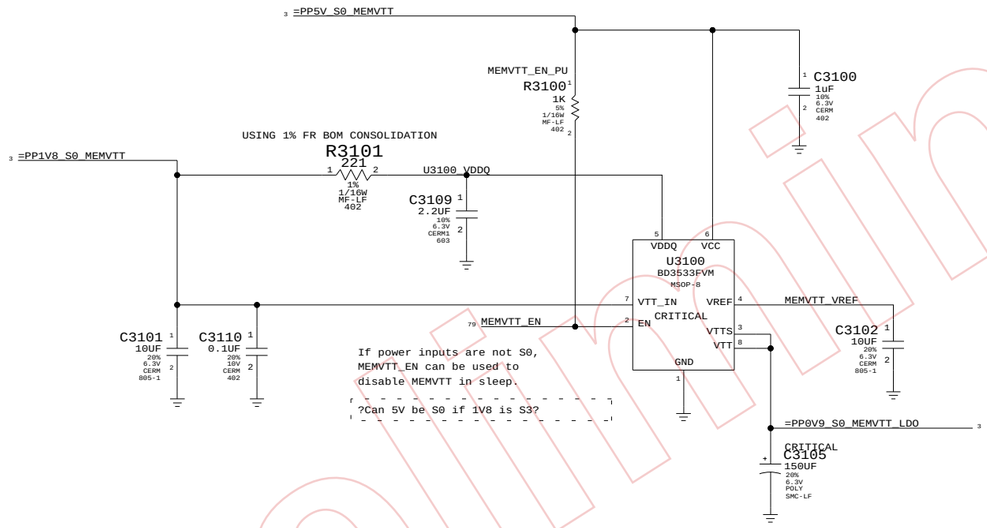
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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SCALE: NONE

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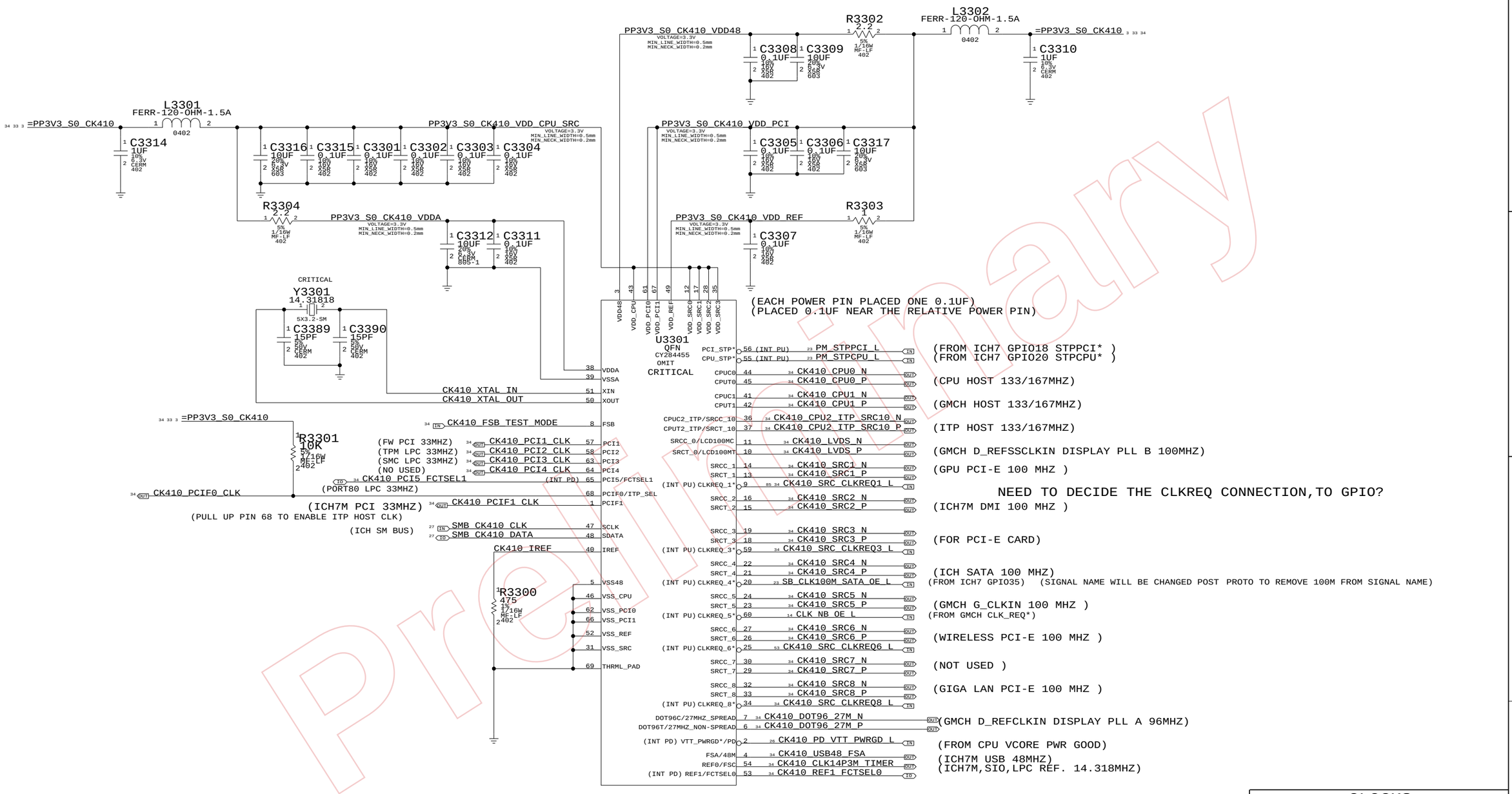

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

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FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

80 34 5 3 PP1V05_S0

14 NB_BSEL<0> — R3453 1K 1/16W 5% MF-LF 402 — 34 CK410_FSA

R3455 1K 1/16W 5% MF-LF 402

NOSTUFF R3452 56 5% 1/16W MF-LF 402

R3454 0 5% 1/16W MF-LF 402

7 CPU_BSEL<0>

80 34 5 3 PP1V05_S0

14 NB_BSEL<1> — R3458 1K 1/16W 5% MF-LF 402 — 33 CK410_FSB_TEST_MODE

R3456 1K 5% 1/16W MF-LF 402

NOSTUFF R3457 0 5% 1/16W MF-LF 402

R3459 0 5% 1/16W MF-LF 402

7 CPU_BSEL<1>

80 34 5 3 PP1V05_S0

14 NB_BSEL<2> — R3462 1K 1/16W 5% MF-LF 402 — 34 CK410_FSC

R3460 1K 5% 1/16W MF-LF 402

NOSTUFF R3461 0 5% 1/16W MF-LF 402

R3463 0 5% 1/16W MF-LF 402

7 CPU_BSEL<2>

33 CK410_PCI5_FCTSEL1 — R3499 1K 1/16W 5% MF-LF 402 — =PP3V3_S0_CK410 3 33

R3497 2.2K 5% 1/16W MF-LF 402 — CK410_FSC 34

33 CK410_CLK14P3M_TIMER — R3498 33 1/16W 5% MF-LF 402 — SB_CLK14P3M_TIMER 5 23

33 CK410_REF1_FCTSEL0 — R3496 33 — TP_CLK14P3M_SPARE

R3451 2.2K 5% 1/16W MF-LF 402 — CK410_FSA 34

33 CK410_USB48_FSA — R3400 33 1/16W 5% MF-LF 402 — SB_CLK48M_USBCTLR 5 23

33 CK410_PCI4_CLK — R3406 33 — TP_PCI_CLK_SPARE

32 CK410_PCI3_CLK — R3405 33 — PCI_CLK_SMC 5 58

32 CK410_PCI2_CLK — R3404 33 — PCI_CLK_TPM 67

33 CK410_PCI1_CLK — R3403 33 — PCI_CLK_FW 5 44

32 CK410_PCIF1_CLK — R3401 33 — PCI_CLK_SB 5 22

32 CK410_PCIF0_CLK — R3402 33 — PCI_CLK_PORT80 5 60

33 CK410_SRC3_P — 33 R3492 — SPARE_SRC3_P — R3488 49.9

33 CK410_SRC3_N — 33 R3491 — SPARE_SRC3_N — R3487 49.9

33 CK410_SRC7_P — 33 R3490 — SPARE_SRC7_P — R3486 49.9

33 CK410_SRC7_N — 33 R3489 — SPARE_SRC7_N — R3485 49.9

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

85 33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) — R3495 NOSTUFF 1K

33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) — R3494 1K

33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) — R3493 1K

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

33 CK410_CPU1_P — 33 R3407 — 12 FSB_CLK_NB_P — R3429 1% 402 1/16W MF-LF 49.9

33 CK410_CPU1_N — 33 R3408 — 12 FSB_CLK_NB_N — R3430 49.9

33 CK410_CPU0_P — 33 R3409 — 7 FSB_CLK_CPU_P — R3431 49.9

33 CK410_CPU0_N — 33 R3410 — 7 FSB_CLK_CPU_N — R3432 49.9

33 CK410_CPU2_ITP_SRC10_P — 33 R3411 — 11 5 CPU_XDP_CLK_P (MAKE_BASE=TRUE) FSB_CLK_XDP_P — R3433 49.9

33 CK410_CPU2_ITP_SRC10_N — 33 R3412 — 11 5 CPU_XDP_CLK_N (MAKE_BASE=TRUE) FSB_CLK_XDP_N — R3434 49.9

33 CK410_SRC6_P — 33 R3413 — 53 AIRPORT_CLK100M_PCIE_P — R3435 49.9

33 CK410_SRC6_N — 33 R3414 — 53 AIRPORT_CLK100M_PCIE_N — R3436 49.9

33 CK410_SRC5_P — 33 R3415 — 14 NB_CLK100M_GCLKIN_P — R3438 49.9

33 CK410_SRC5_N — 33 R3416 — 14 NB_CLK100M_GCLKIN_N — R3437 49.9

33 CK410_SRC4_P — 33 R3417 — 21 5 SB_CLK100M_SATA_P — R3439 49.9

33 CK410_SRC4_N — 33 R3418 — 21 5 SB_CLK100M_SATA_N — R3440 49.9

33 CK410_SRC2_P — 33 R3419 — 22 SB_CLK100M_DMI_P — R3442 49.9

33 CK410_SRC2_N — 33 R3420 — 22 SB_CLK100M_DMI_N — R3441 49.9

33 CK410_SRC8_P — 33 R3421 — 41 ENET_CLK100M_PCIE_P — R3443 49.9

33 CK410_SRC8_N — 33 R3422 — 41 ENET_CLK100M_PCIE_N — R3444 49.9

33 CK410_SRC1_P — 33 R3423 — 85 GPU_CLK100M_PCIE_P — R3446 49.9

33 CK410_SRC1_N — 33 R3424 — 85 GPU_CLK100M_PCIE_N — R3445 49.9

33 CK410_LVDS_P — MAKE_BASE=TRUE — TP_CK410_LVDS_P

33 CK410_LVDS_N — MAKE_BASE=TRUE — TP_CK410_LVDS_N

33 CK410_DOT96_27M_N — MAKE_BASE=TRUE — TP_CK410_27M_SPREAD

33 CK410_DOT96_27M_P — MAKE_BASE=TRUE — TP_CK410_27M_NONSPREAD

CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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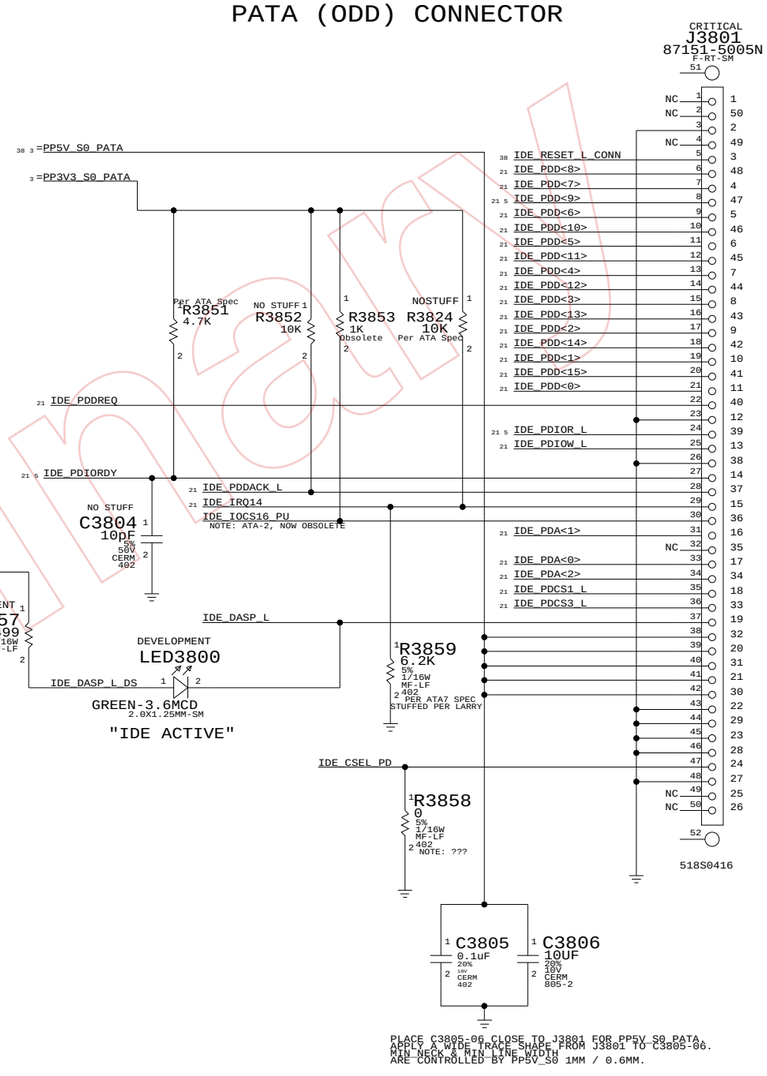
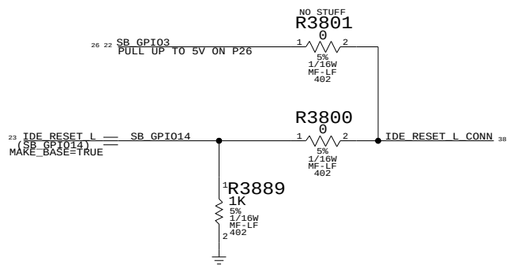
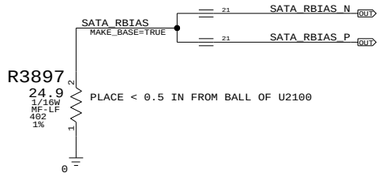
SCALE NONE SHT 34 OF 97

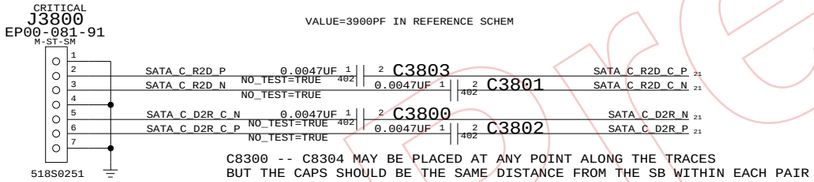
PATA (ODD) CONNECTOR

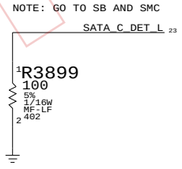


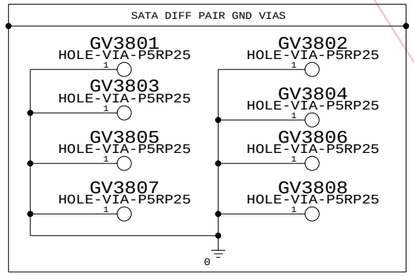


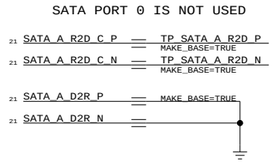


SATA CONNECTOR







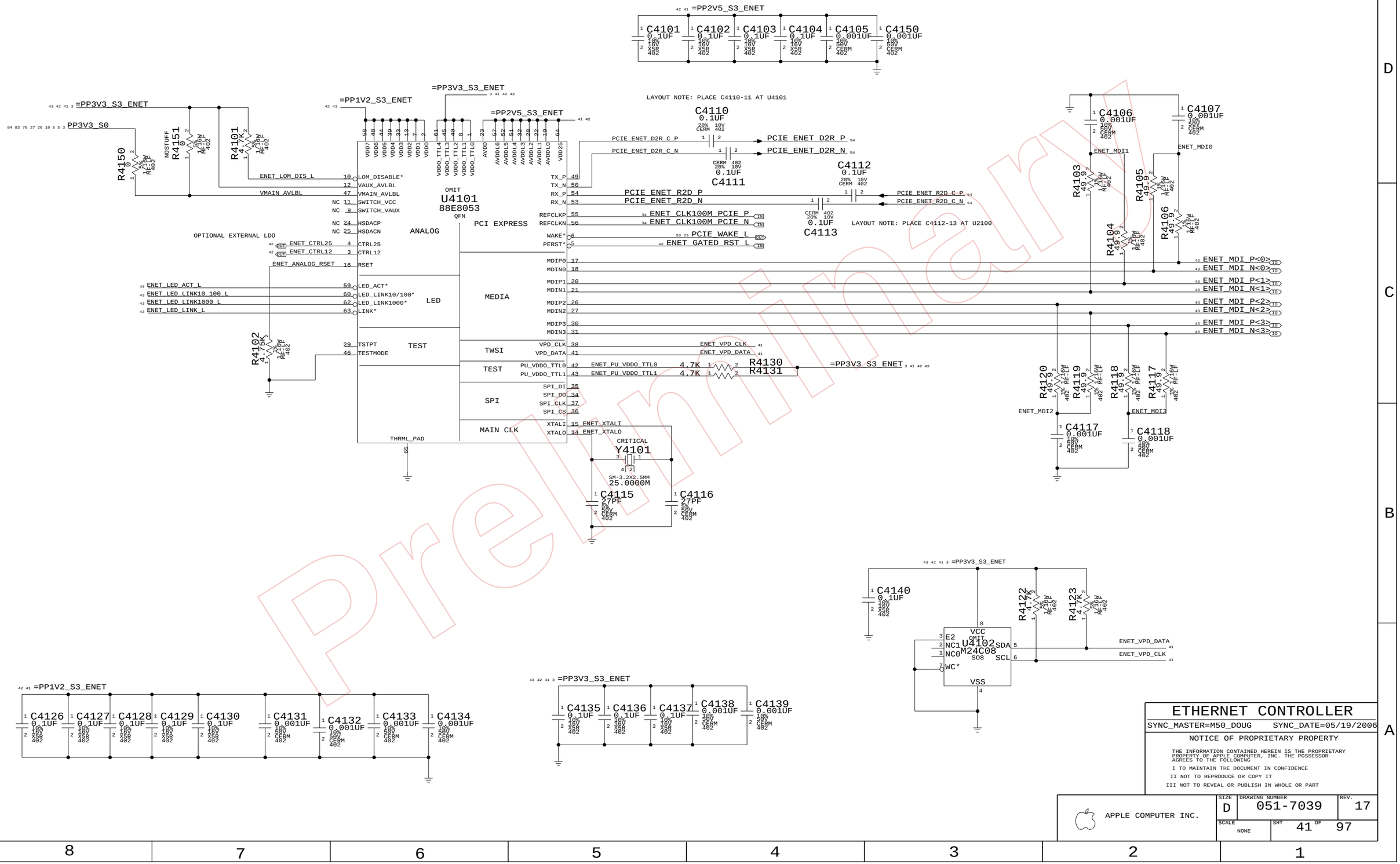


Disk Connectors

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 38 OF 97	



ETHERNET CONTROLLER

SYNC_MASTER=M50_DOUG SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
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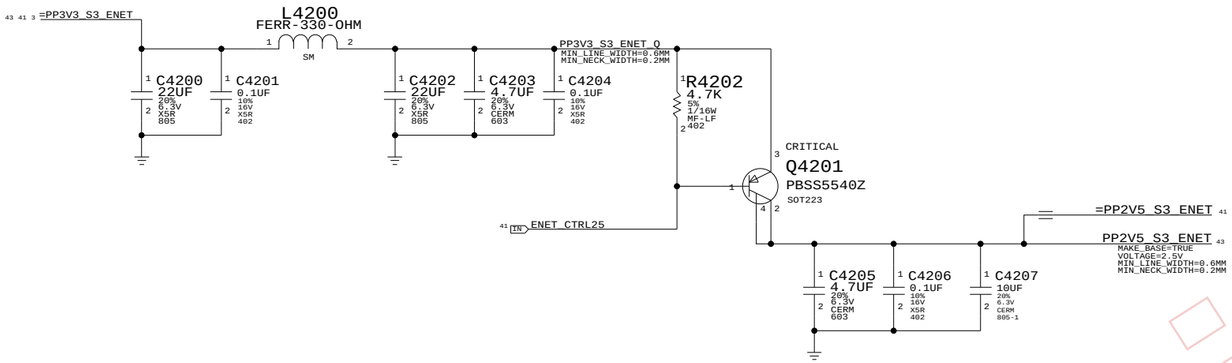
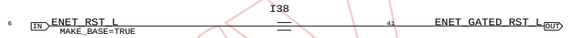
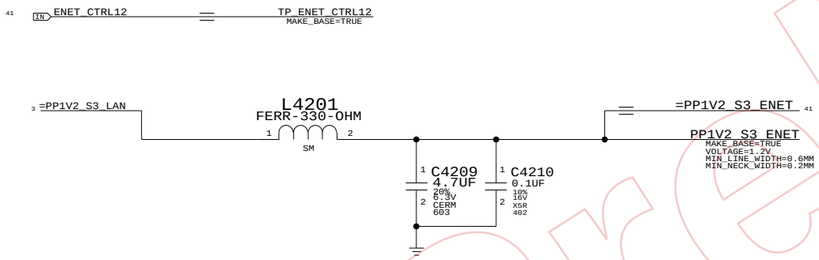




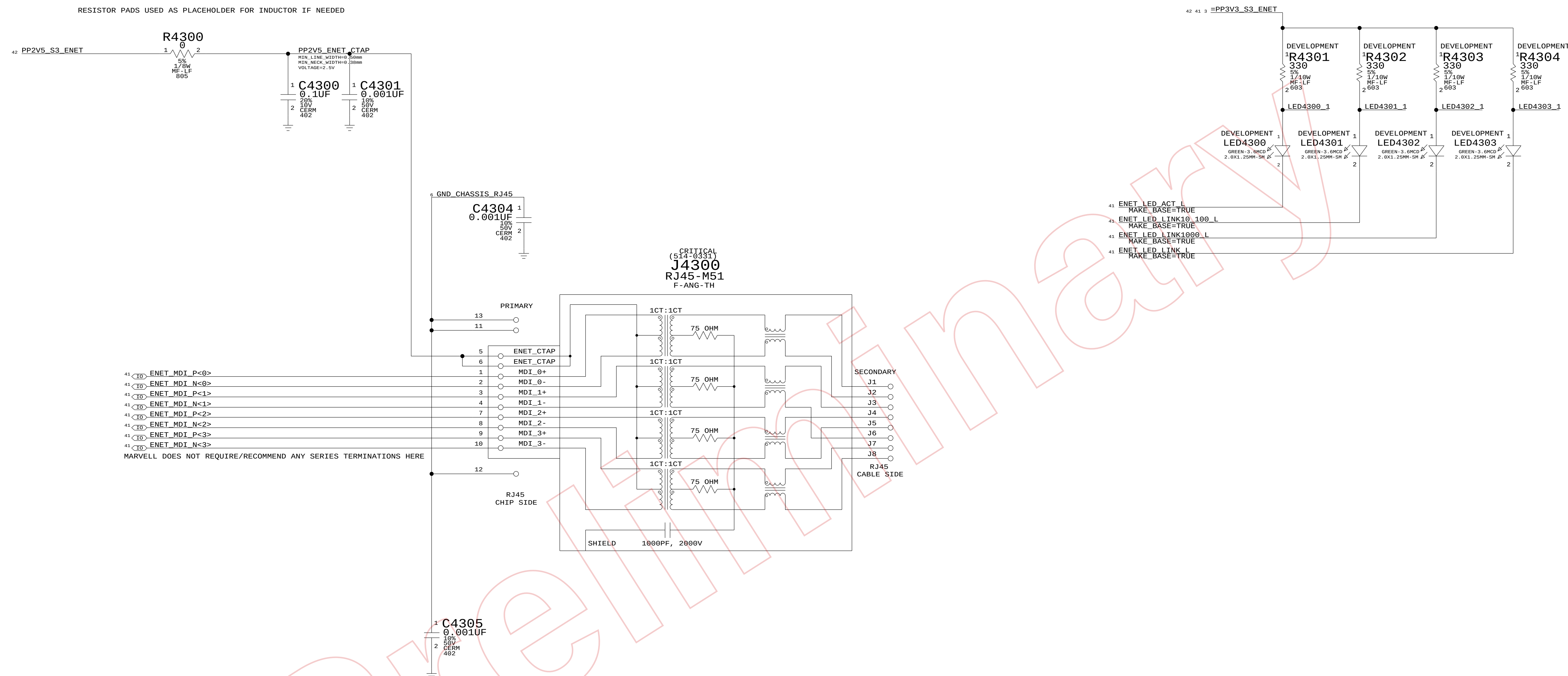


ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 42 OF 97	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED
42 PP2V5_S3_ENET
R4300 0 5% 1/8W MF-LF 805
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm
VOLTAGE=2.5V
C4300 0.1UF 20% 10V CERM 402
C4301 0.001UF 10% 50V CERM 402
6 GND_CHASSIS_RJ45
C4304 0.001UF 10% 50V CERM 402
CRITICAL
(514-0331)
J4300
RJ45-M51
F-ANG-TH
PRIMARY
SECONDARY
1CT:1CT
75 OHM
ENET_CTAP
MDI_0+
MDI_0-
MDI_1+
MDI_1-
MDI_2+
MDI_2-
MDI_3+
MDI_3-
J1 J2 J3 J4 J5 J6 J7 J8
RJ45 CABLE SIDE
RJ45 CHIP SIDE
SHIELD
1000PF, 2000V
41 ENET_MDI_P<0>
41 ENET_MDI_N<0>
41 ENET_MDI_P<1>
41 ENET_MDI_N<1>
41 ENET_MDI_P<2>
41 ENET_MDI_N<2>
41 ENET_MDI_P<3>
41 ENET_MDI_N<3>
MARVELL DOES NOT REQUIRE/RECOMMEND ANY SERIES TERMINATIONS HERE
C4305 0.001UF 10% 50V CERM 402
42 41 3 =PP3V3_S3_ENET
DEVELOPMENT R4301 330 5% 1/10W MF-LF 603
DEVELOPMENT R4302 330 5% 1/10W MF-LF 603
DEVELOPMENT R4303 330 5% 1/10W MF-LF 603
DEVELOPMENT R4304 330 5% 1/10W MF-LF 603
LED4300_1
LED4301_1
LED4302_1
LED4303_1
DEVELOPMENT LED4300 GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT LED4301 GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT LED4302 GREEN-3.6MCD 2.0X1.25MM-SM
DEVELOPMENT LED4303 GREEN-3.6MCD 2.0X1.25MM-SM
41 ENET_LED_ACT_L MAKE_BASE=TRUE
41 ENET_LED_LINK10_100_L MAKE_BASE=TRUE
41 ENET_LED_LINK1000_L MAKE_BASE=TRUE
41 ENET_LED_LINK_L MAKE_BASE=TRUE

ETHERNET CONNECTOR

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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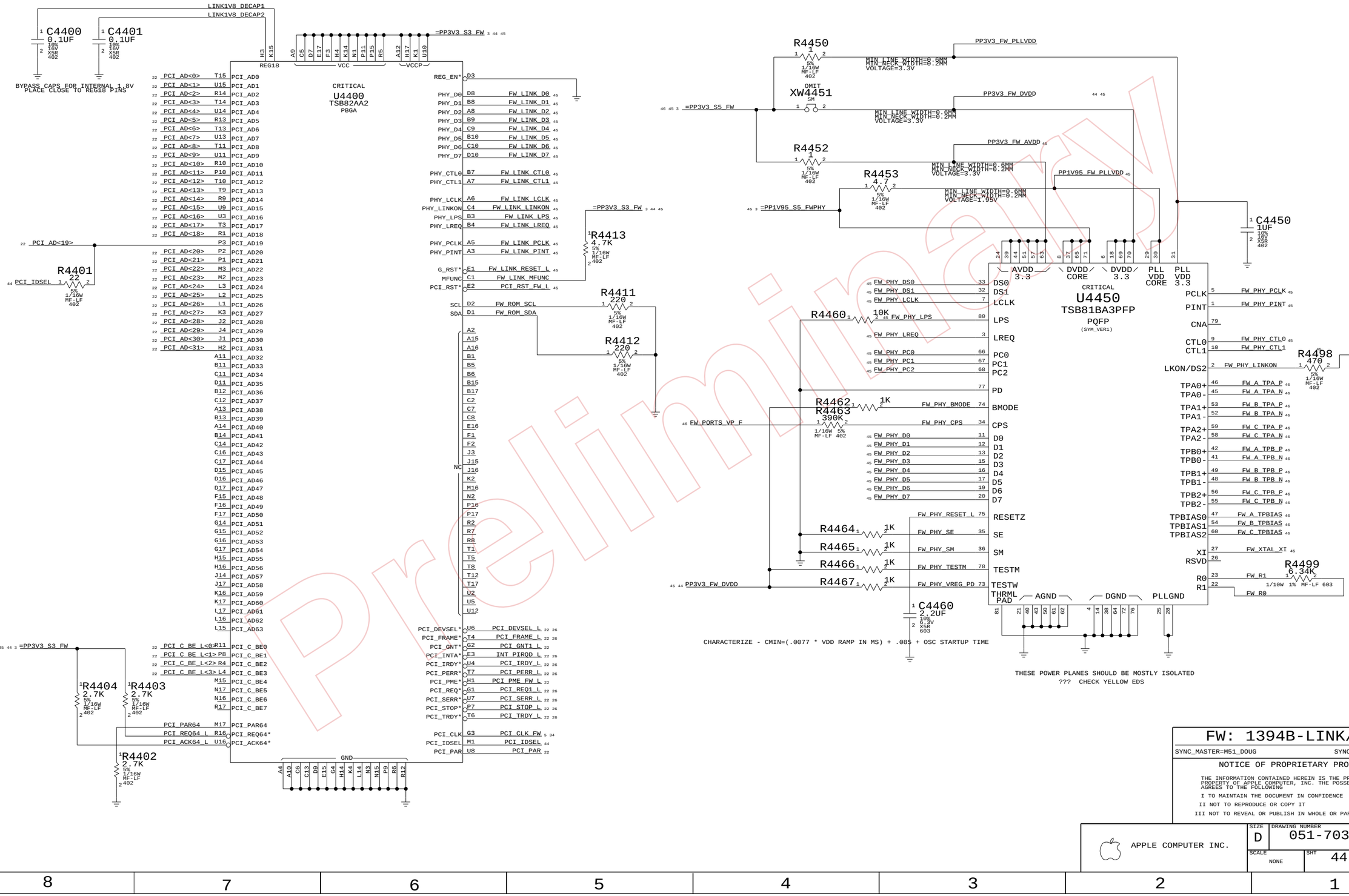
D	051-7039	17
SCALE NONE	SHT 43 OF 97	


LINK1V8_DECAP1
LINK1V8_DECAP2
C4400 0.1UF 10% 10V X5R 402
C4401 0.1UF 10% 10V X5R 402
BYPASS CAPS FOR INTERNAL 1.8V
PLACE CLOSE TO REG18 PINS
REG18
VCC
VCCP
=PP3V3_S3_FW
CRITICAL
U4400
TSB82AA2
PBGA
REG_EN*
PHY_D0 PHY_D1 PHY_D2 PHY_D3 PHY_D4 PHY_D5 PHY_D6 PHY_D7
PHY_CTL0 PHY_CTL1
PHY_LCLK PHY_LINKON PHY_LPS PHY_LREQ
PHY_PCLK PHY_PINT
G_RST* MFUNC PCI_RST*
SCL SDA
NC
PCI_DEVSEL* PCI_FRAME* PCI_GNT* PCI_INTA* PCI_IRDY* PCI_PERR* PCI_PME* PCI_REQ* PCI_SERR* PCI_STOP* PCI_TRDY*
PCI_CLK PCI_IDSEL PCI_PAR
PCI_AD<0> ... PCI_AD<31>
PCI_AD0 ... PCI_AD63
PCI_C_BE0 PCI_C_BE1 PCI_C_BE2 PCI_C_BE3 PCI_C_BE4 PCI_C_BE5 PCI_C_BE6 PCI_C_BE7
PCI_PAR64 PCI_REQ64* PCI_ACK64*
R4401 22
R4402 2.7K
R4403 2.7K
R4404 2.7K
R4411 220
R4412 220
R4413 4.7K
GND
R4450 1
R4451 SM
R4452 1
R4453 4.7
PP3V3_FW_PLLVDD
PP3V3_FW_DVDD
PP3V3_FW_AVDD
PP1V95_FW_PLLVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
VOLTAGE=1.95V
=PP3V3_S5_FW
=PP1V95_S5_FWPHY
C4450 1UF 10% 10V X5R 402
AVDD 3.3
DVDD CORE
DVDD 3.3
PLL VDD CORE 3.3
PLL VDD 3.3
CRITICAL
U4450
TSB81BA3PFP
PQFP
(SYM_VER1)
DS0 DS1 LCLK LPS LREQ PC0 PC1 PC2 PD BMODE CPS D0 D1 D2 D3 D4 D5 D6 D7 RESETZ SE SM TESTM TESTW THRML PAD
PCLK PINT CNA CTL0 CTL1 LKON/DS2 TPA0+ TPA0- TPA1+ TPA1- TPA2+ TPA2- TPB0+ TPB0- TPB1+ TPB1- TPB2+ TPB2- TPBIAS0 TPBIAS1 TPBIAS2 XI RSVD R0 R1
R4460 10K
R4462 1K
R4463 390K
R4464 1K
R4465 1K
R4466 1K
R4467 1K
R4498 470
R4499 6.34K
1/10W 1% MF-LF 603
C4460 2.2UF 10% 6.3V X5R 603
AGND DGND PLLGND
CHARACTERIZE - CMIN=(.0077 * VDD RAMP IN MS) + .085 + OSC STARTUP TIME
THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
??? CHECK YELLOW EDS
FW: 1394B-LINK/PHY
SYNC_MASTER=M51_DOUG
SYNC_DATE=05/19/2006
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
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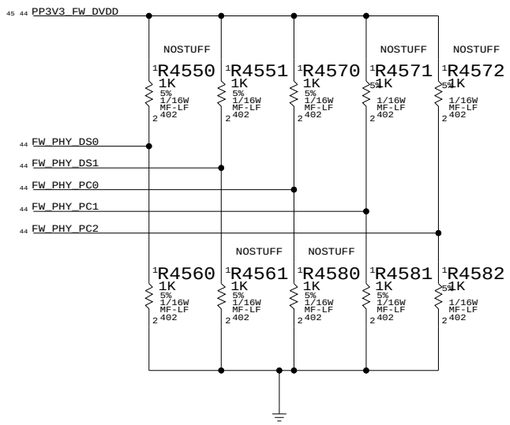
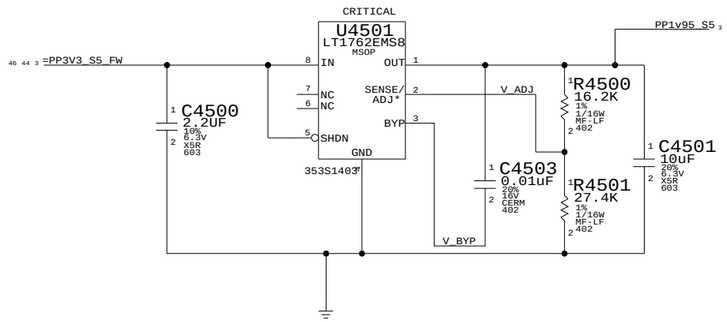
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. 17
SCALE NONE
SHT 44 OF 97

1394 PHY DATA/STROBE AND POWER CLASS OPTIONS



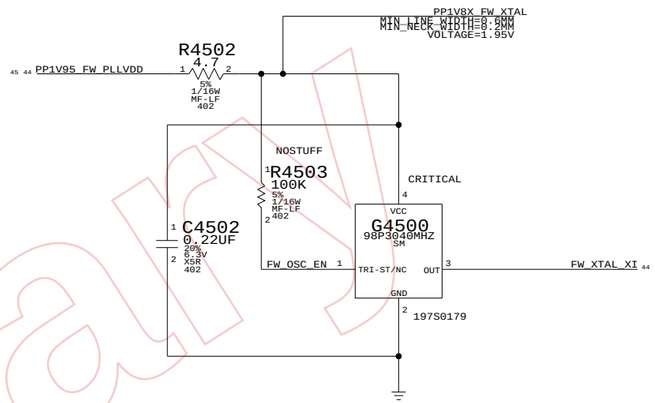
1394 PHY 1.95V REGULATOR



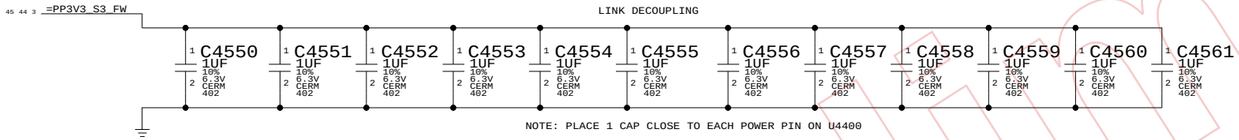
VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V

1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION

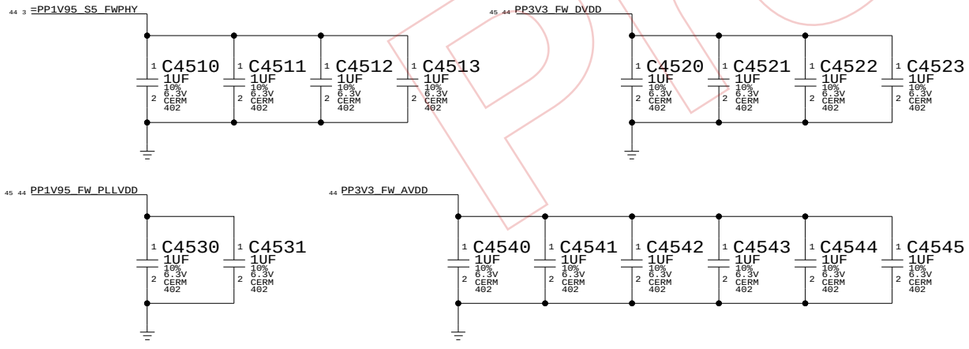


LINK DECOUPLING



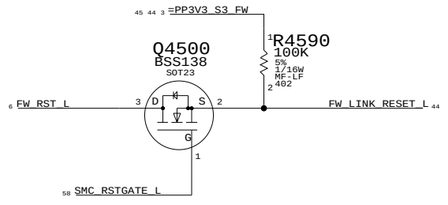
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

PHY DECOUPLING



NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

1394 LINK POWER ON RESET AND PCI RESET



NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT

44 FW_LINK_D0 MAKE_BASE=TRUE	FW_PHY_D0	44 FW_LINK_LINKON	FW_PHY_LINKON 44
44 FW_LINK_D1 MAKE_BASE=TRUE	FW_PHY_D1	44 FW_LINK_PINT MAKE_BASE=TRUE	FW_PHY_PINT 44
44 FW_LINK_D2 MAKE_BASE=TRUE	FW_PHY_D2		
44 FW_LINK_D3 MAKE_BASE=TRUE	FW_PHY_D3		
44 FW_LINK_D4 MAKE_BASE=TRUE	FW_PHY_D4		
44 FW_LINK_D5 MAKE_BASE=TRUE	FW_PHY_D5		
44 FW_LINK_D6 MAKE_BASE=TRUE	FW_PHY_D6		
44 FW_LINK_D7 MAKE_BASE=TRUE	FW_PHY_D7		
44 FW_LINK_CTL0 MAKE_BASE=TRUE	FW_PHY_CTL0		
44 FW_LINK_CTL1 MAKE_BASE=TRUE	FW_PHY_CTL1		
44 FW_LINK_LCLK MAKE_BASE=TRUE	FW_PHY_LCLK		
44 FW_LINK_LPS MAKE_BASE=TRUE	FW_PHY_LPS		
44 FW_LINK_LREQ MAKE_BASE=TRUE	FW_PHY_LREQ		
44 FW_LINK_PCLK MAKE_BASE=TRUE	FW_PHY_PCLK		

R4520 1K

NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2

NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

FW: 1394B MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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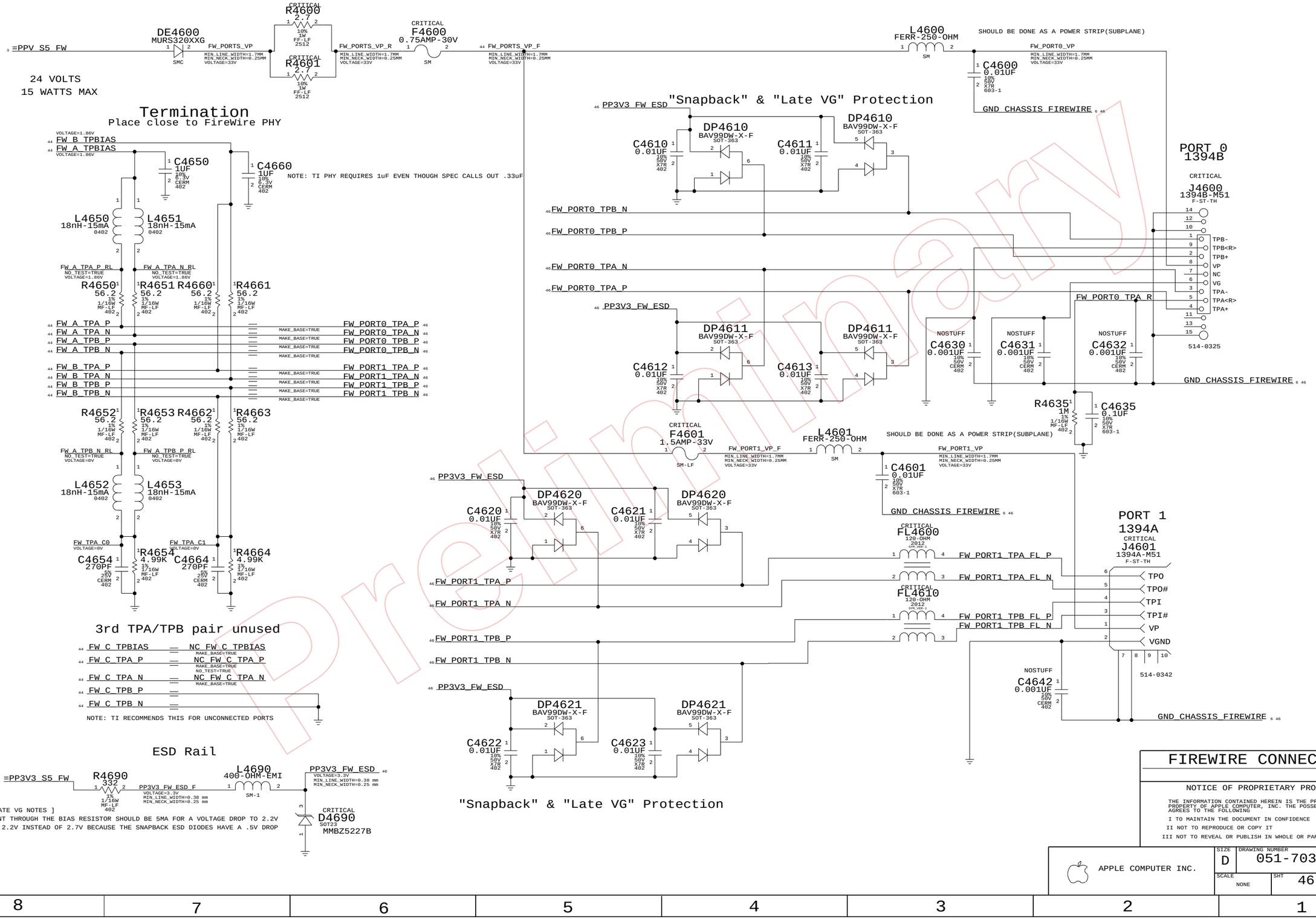
=PPV_S5_FW
DE4600
MURS320XXG
SMC
FW_PORTS_VP
MIN_LINE_WIDTH=1.7MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V
CRITICAL
R4600
2.7
10%
1W
FF-LF
2512
CRITICAL
R4601
2.7
10%
1W
FF-LF
2512
FW_PORTS_VP_R
CRITICAL
F4600
0.75AMP-30V
SM
FW_PORTS_VP_F
24 VOLTS
15 WATTS MAX
L4600
FERR-250-OHM
SM
SHOULD BE DONE AS A POWER STRIP(SUBPLANE)
FW_PORT0_VP
C4600
0.01UF
10%
50V
X7R
603-1
GND_CHASSIS_FIREWIRE
Termination
Place close to FireWire PHY
FW_B_TPBIAS
FW_A_TPBIAS
VOLTAGE=1.86V
C4650
1UF
10%
6.3V
CERM
402
C4660
1UF
10%
6.3V
CERM
402
NOTE: TI PHY REQUIRES 1uF EVEN THOUGH SPEC CALLS OUT .33uF
L4650
18nH-15mA
0402
L4651
18nH-15mA
0402
FW_A_TPA_P_RL
FW_A_TPA_N_RL
NO_TEST=TRUE
VOLTAGE=1.86V
R4650
56.2
R4651
56.2
R4660
56.2
R4661
56.2
1%
1/16W
MF-LF
402
FW_A_TPA_P
FW_A_TPA_N
FW_A_TPB_P
FW_A_TPB_N
FW_B_TPA_P
FW_B_TPA_N
FW_B_TPB_P
FW_B_TPB_N
MAKE_BASE=TRUE
FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N
FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N
R4652
56.2
R4653
56.2
R4662
56.2
R4663
56.2
FW_A_TPB_N_RL
FW_A_TPB_P_RL
VOLTAGE=0V
L4652
18nH-15mA
0402
L4653
18nH-15mA
0402
FW_TPA_C0
FW_TPA_C1
C4654
270PF
50V
25V
CERM
402
C4664
270PF
R4654
4.99K
R4664
4.99K
3rd TPA/TPB pair unused
FW_C_TPBIAS
FW_C_TPA_P
FW_C_TPA_N
FW_C_TPB_P
FW_C_TPB_N
NC_FW_C_TPBIAS
NC_FW_C_TPA_P
NC_FW_C_TPA_N
NOTE: TI RECOMMENDS THIS FOR UNCONNECTED PORTS
ESD Rail
=PP3V3_S5_FW
R4690
332
PP3V3_FW_ESD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
L4690
400-OHM-EMI
SM-1
PP3V3_FW_ESD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
CRITICAL
D4690
SOT23
MMBZ5227B
[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP
"Snapback" & "Late VG" Protection
PP3V3_FW_ESD
DP4610
BAV99DW-X-F
SOT-363
C4610
0.01UF
C4611
0.01UF
DP4611
C4612
0.01UF
C4613
0.01UF
DP4620
C4620
0.01UF
C4621
0.01UF
DP4621
C4622
0.01UF
C4623
0.01UF
10%
50V
X7R
402
FW_PORT0_TPB_N
FW_PORT0_TPB_P
FW_PORT0_TPA_N
FW_PORT0_TPA_P
FW_PORT0_TPA_R
PORT 0
1394B
CRITICAL
J4600
1394B-M51
F-ST-TH
TPB-
TPB<R>
TPB+
VP
NC
VG
TPA-
TPA<R>
TPA+
514-0325
NOSTUFF
C4630
0.001UF
C4631
0.001UF
C4632
0.001UF
R4635
1M
C4635
0.1UF
CRITICAL
F4601
1.5AMP-33V
SM-LF
FW_PORT1_VP_F
L4601
FERR-250-OHM
SM
FW_PORT1_VP
C4601
0.01UF
FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N
CRITICAL
FL4600
120-OHM
2012
FW_PORT1_TPA_FL_P
FW_PORT1_TPA_FL_N
CRITICAL
FL4610
120-OHM
2012
FW_PORT1_TPB_FL_P
FW_PORT1_TPB_FL_N
PORT 1
1394A
CRITICAL
J4601
1394A-M51
F-ST-TH
TPO
TPO#
TPI
TPI#
VP
VGND
514-0342
C4642
0.001UF
"Snapback" & "Late VG" Protection
FIREWIRE CONNECTORS
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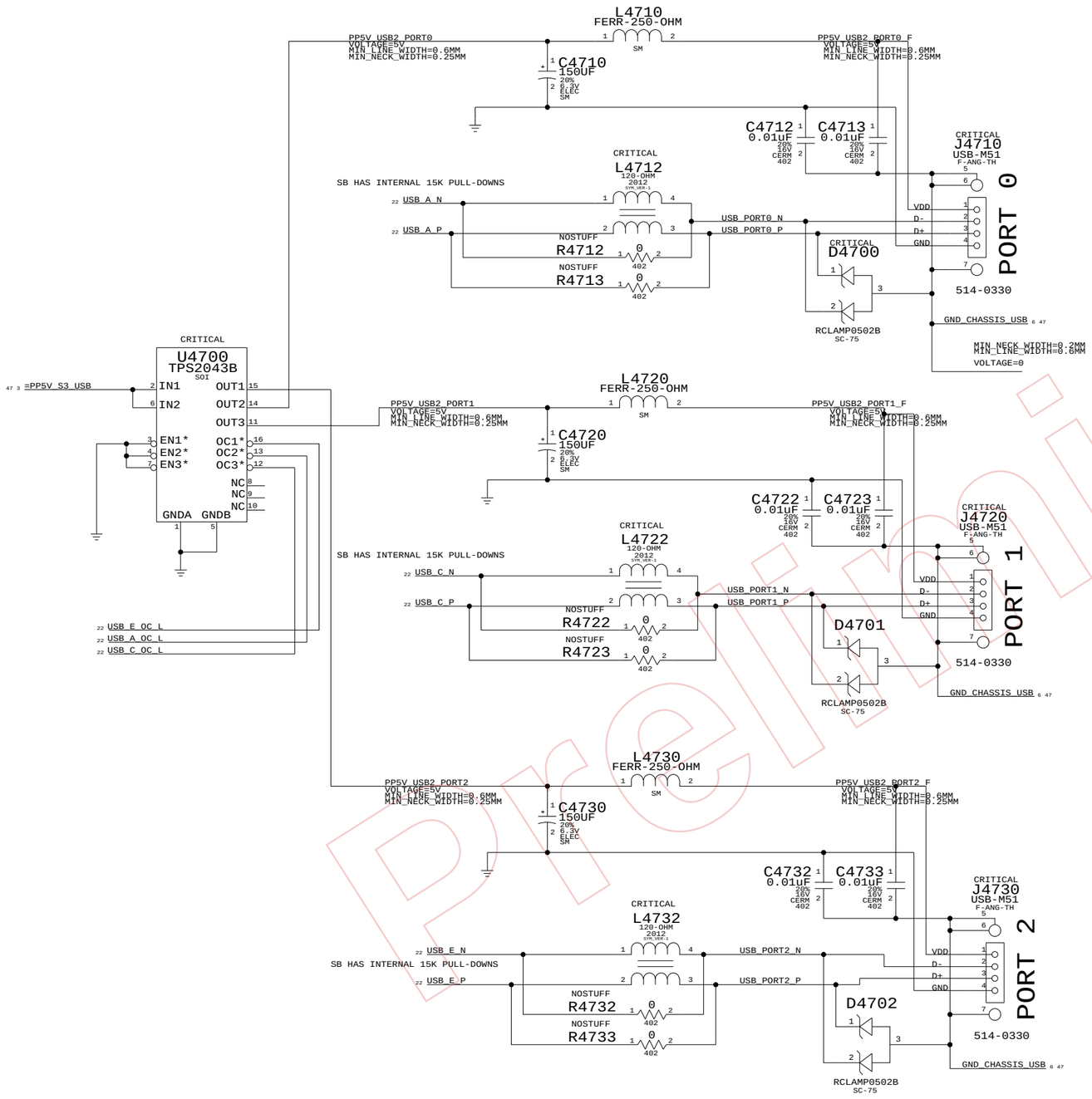
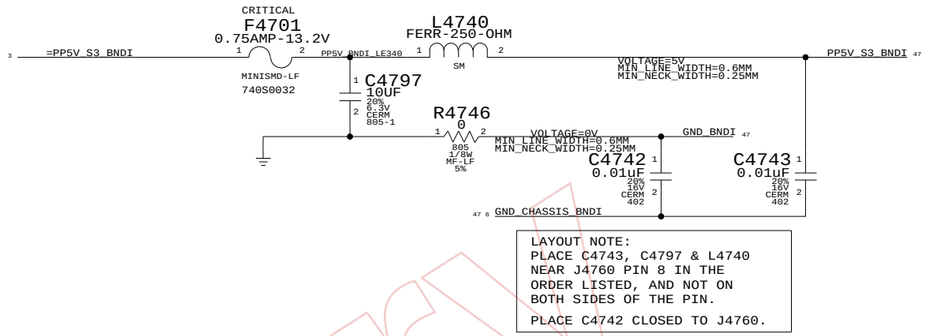
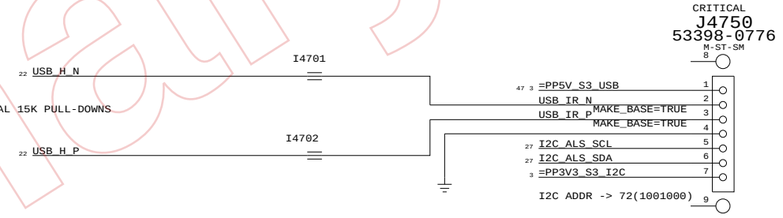
D
DRAWING NUMBER
051-7039
REV.
17
SCALE
NONE
SHT
46
OF
97

External USB Ports

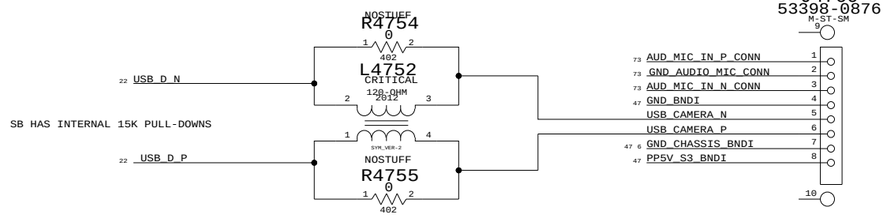




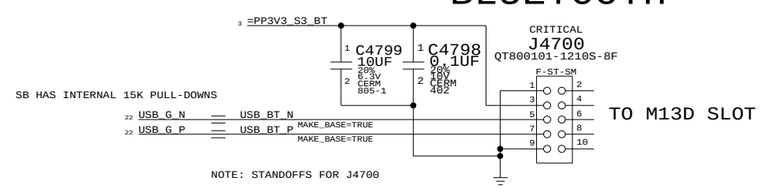
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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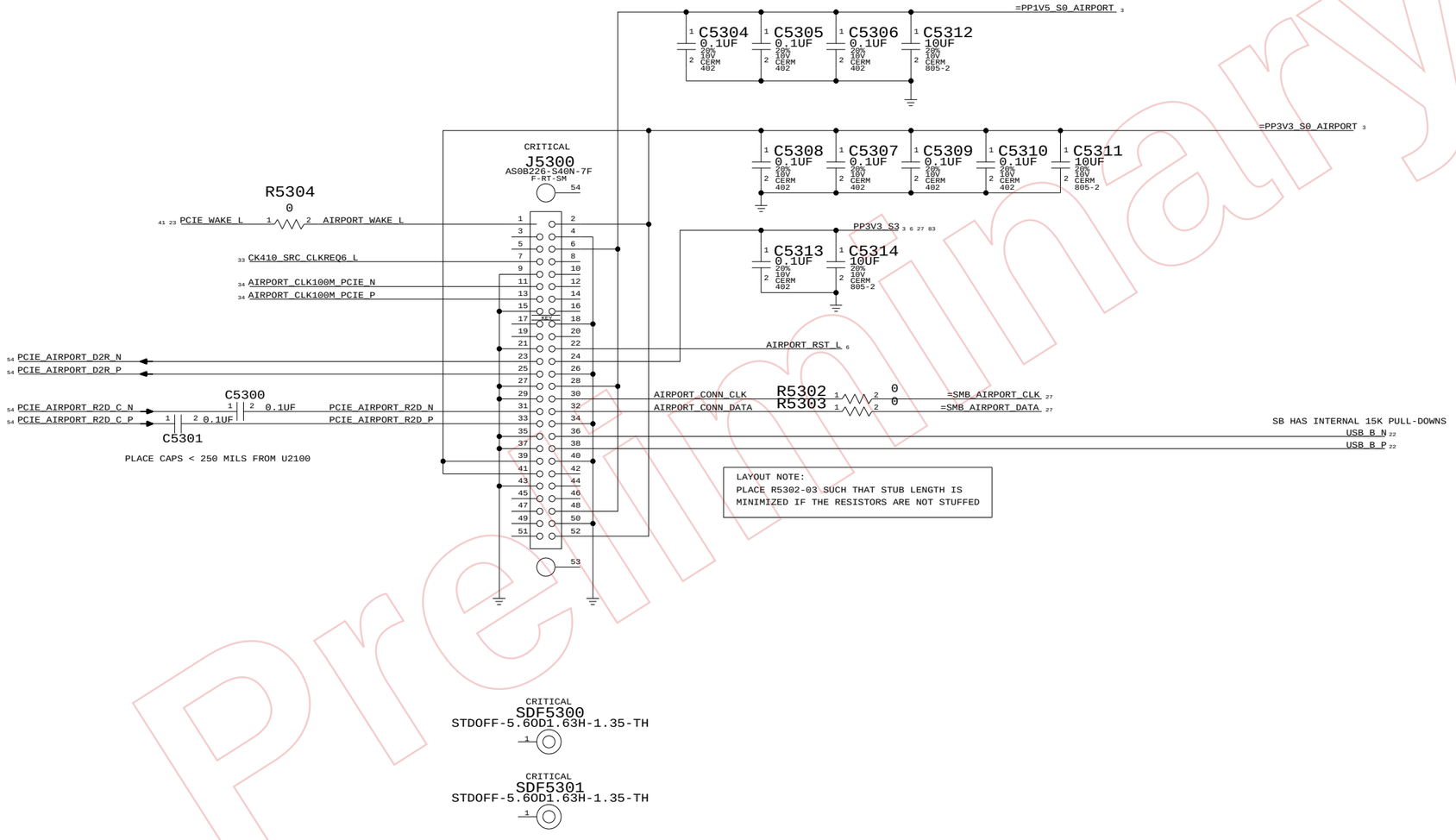

AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

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PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=05/19/2006

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SIZE	DRAWING NUMBER	REV.
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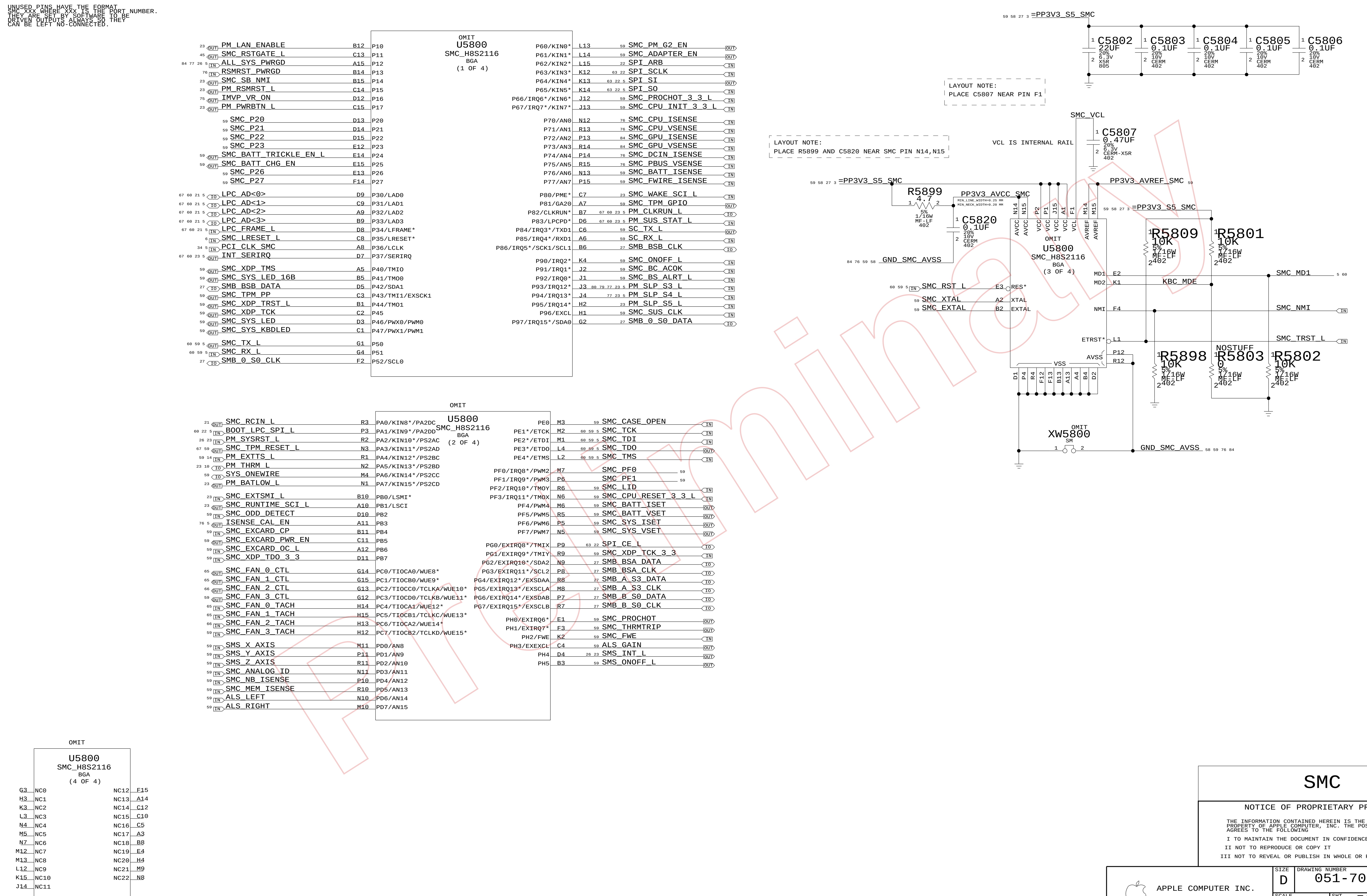
SCALE: NONE	SHT 54 OF 97	



SMC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE NONE — SHT 58 OF 97

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
378S0193	1	LED,WHITE,740MCD,LF,3X2MM	LED5950	CRITICAL	

WHITE SYSLED

SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS ACROSS LARGE VOLUME MANUFACTURING

SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

PP5V_S3

PLACE C5951 NEXT TO Q5952

CURRENT SET TO DRIVE LED AT 20MA NOMINAL

C5951 1UF 10% 6.3V CERM 402

R5952 43 5% 1/16W MF-LF 402

R5951 2.2K 5% 1/10W MF-LF 402

R5955 4.7K 5% 1/10W MF-LF 402

SYS_LED_BRT_D

SYS_LED_CTL_B

SYS_LED_CTL_C

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q5952 2N3906 SOT23-LF

Q5951 2N7002 SOT23-LF

SMC_SYS_LED

R5957 4.7K 5% 1/10W MF-LF 402

SYS_LED_CTL_D

SYS_LED_C

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q5950 2N7002 SOT23-LF

SMC_SYS_LED_16B

NOSTUFF R5950 4.7K 5% 1/16W MF-LF 402

OMIT LED5950 WHITE-740MCD 3X2MM-SM

378S0193

* BRIGHTER FOR LARGER IMACS

SMC 3.3V -> CPU 1.05V SHIFTER

CPU_PROCHOT_L

Q5901 2N7002DW-X-F SOT-363

SMC_PROCHOT

PM_THRMTRIP_L

Q5901 2N7002DW-X-F SOT-363

SMC_THRMTRIP

CPU 1.05V -> SMC 3.3V SHIFTER

GENERATE 0.48V MID-VREF

=PP3V3_S0_FAN

R5930 6.2K 5% 1/16W MF-LF 402

C5903 0.1UF 20% 16V CERM 402

=PP3V3_S5_SMC

R5932 1K 5% 1/16W MF-LF 402

P0V48_SMC_LSREF

C5930 100PF 5% 50V CERM 402

R5931 1K 5% 1/16W MF-LF 402

U5999 LM393A SOI-1-LF GND

CPU_PROCHOT_L

SMC_PROCHOT_3_3_L

PCB: ENSURE FSB_CPURST_L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

U5999 LM393A SOI-1-LF GND

SPARE COMPARATOR

POWER BUTTON HEADER

CRITICAL J5903 53398-0276 M-ST-SM

518S0327

POWER_BUTTON_L

SYS POWER BUTTON

DEVELOPMENT SW5901 SPST SM-LF

R5907 1K 5% 1/16W MF-LF 402

SMC_ONOFF_L

NOSTUFF C5904 0.01UF 20% 50V CERM 603

C5902 0.1UF 20% 10V CERM 402

LAYOUT: PLACE C5904 ON OPPOSITE LAYER OF SW5901 C5904 FOR TWEEZERS TO TURN ON SYSTEM

* NEVER STUFF C5904

PRECISION 3.3V AVREF FOR SMC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	INTERSIL ISL60002-33

=PP3V3_S5_SMC

PP5V_S5

R5942 10K 5% 1/16W MF-LF 402

Q5910 NTR4101P SOT-23

SMC_REF_GATE1

SMC_REF_GATE2

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM

Q5911 2N7002 SOT23-LF

R5941 10K 5% 1/16W MF-LF 402

C5943 1UF 10% 6.3V CERM 402

TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

NOSTUFF R5940 0 5% 1/16W MF-LF 402

CRITICAL U5940 REF3133 SOT23-3 353S1278 GND IN OUT

SMC_REF_IN

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM

PP3V3_AVREF_SMC

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

C5940 0.47UF 20% 6.3V CERM-X5R 402

C5942 10UF 20% 6.3V CERM 805-1

C5941 0.01UF 20% 16V CERM 402

GND_SMC_AVSS

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V

SMC RESET BUTTON

=PP3V3_S5_SMC

C5901 0.1UF 20% 10V CERM 402

CRITICAL U5900 RN5VD30A-F SOT23-5 VDD CD NC OUT GND

R5900 1K 5% 1/16W MF-LF 402

SMC_MANUAL_RST_L

DEVELOPMENT SW5900 SPST SM-LF

C5900 0.01UF 10% 16V CERM 402

SMC_RST_L

SMC CRYSTAL

C5980 22PF 5% 50V CERM 402

SMC_XTAL

CRITICAL Y5980 20.000M 8X4.5-SM

C5981 22PF 5% 50V CERM 402

SMC_EXTAL

TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

C5982 15PF 5% 50V CERM 402

TPM_XTALI

CRITICAL Y5981 32.768K 4.1X1.5X.9-SM

C5983 15PF 5% 50V CERM 402

TPM_XTALO

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20	MAKE_BASE=TRUE
SMC_P21	NC_SMC_P21	MAKE_BASE=TRUE
SMC_P22	NC_SMC_P22	MAKE_BASE=TRUE
SMC_P23	NC_SMC_P23	MAKE_BASE=TRUE
SMC_P26	NC_SMC_P26	MAKE_BASE=TRUE
SMC_P27	NC_SMC_P27	MAKE_BASE=TRUE
SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE, FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE
SMC_XDP_TCK	TP_SMC_XDP_TCK	MAKE_BASE=TRUE
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L	MAKE_BASE=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE, FUNC_TEST=TRUE

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE
SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE
SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE
SMC_NB_ISENSE	NC_SMC_NB_ISENSE	MAKE_BASE=TRUE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE

UNUSED_SMC_SENSE — 10K — R5924 5% 1/16W MF-LF

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS & PULL-DOWNS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K
SMC_LID	R5916	10K
SMC_EXCARD_OC_L	R5831	10K
SMC_XDP_TCK_3_3	R5934	1K
SMC_CPU_RESET_3_3_L	R5933	1K
SMC_EXCARD_CP	R5830	10K
SMC_CASE_OPEN	R5917	10K

TPM RESET PULLUP

PP3V3_TPM_3VSB — R5827 10K — SMC_TPM_RESET_L

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE

SC_RX_L — 0 — R5922 — SMC_RX_L

SC_TX_L — 0 — R5923 — SMC_TX_L

SELECT TPM GPIO

SMC_TPM_GPIO — 0 — R5920 — SMC_TPM_GPIO1 — TPM_GPIO1

SMC_TPM_GPIO — 0 — R5921 — SMC_TPM_GPIO2 — TPM_GPIO2

SMC_TPM_PP

SMC_TPM_PP — 0 R5995 — TPM_PP

POWER SUPPLY TEMP SENSE

SMC_ANALOG_ID — ACDC_TEMP

HDD ACTIVITY MONITOR

PP5V_S0

M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING

TP_SB_SATALED_L — PU_HDD_ACTIVITY_LED — R5960 10K

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS END TRACE AND TIE TRACE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM — GND_NEXT_TO_SMC — OMIT

M51 SPECIFIC: GPU MONITORING SIGNALS

I327	SMC_XDP_TMS	MXM_AC_BATT_L	MAKE_BASE=TRUE
I328	SMC_XDP_TDO_3_3	GPU_OVERTEMP_L	MAKE_BASE=TRUE

SMC & TPM SUPPORT

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

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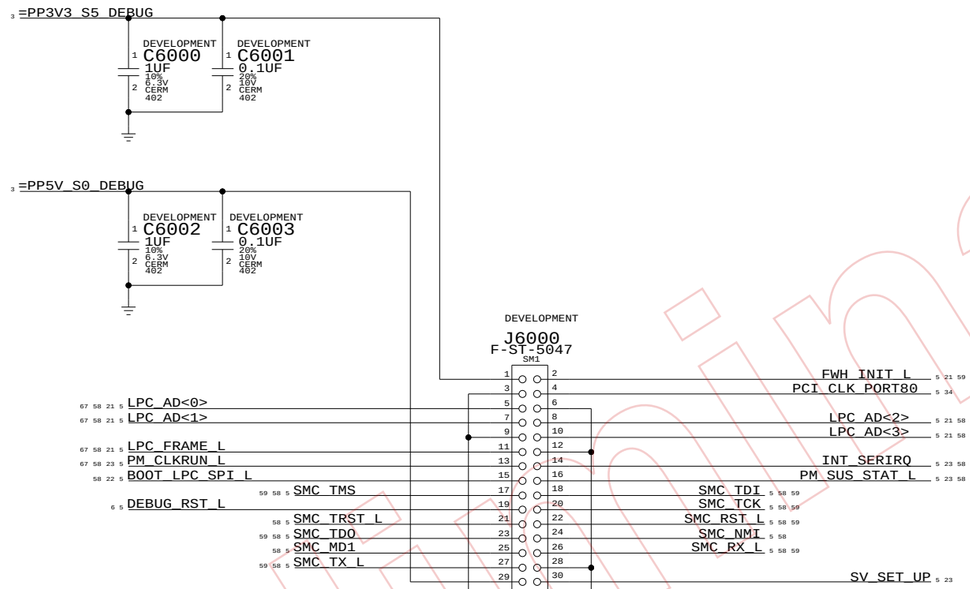
D	051-7039	17
SCALE: NONE	SHT 59 OF 97	



LPC+ CONN

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

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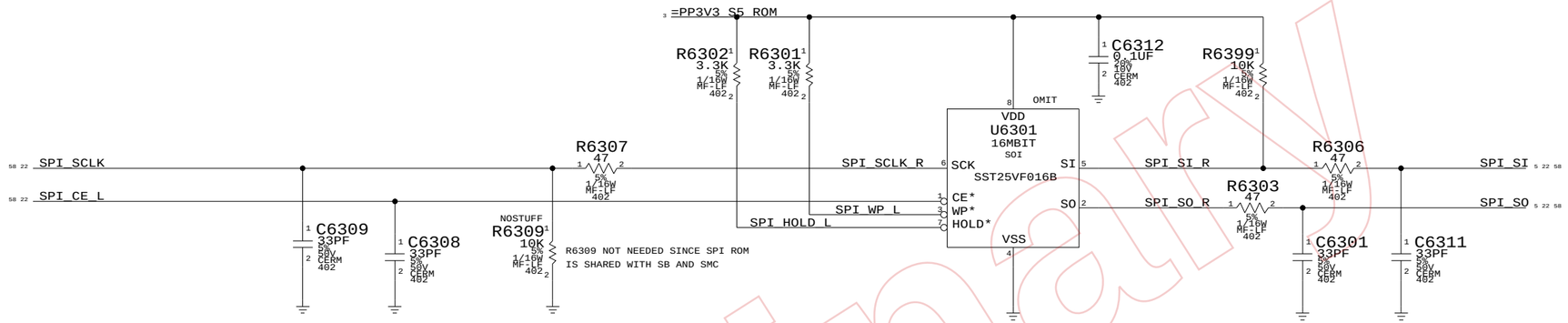
SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE: NONE

SHT 60 OF 97



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

SYNC_MASTER=M50_DOUG SYNC_DATE=05/19/2006

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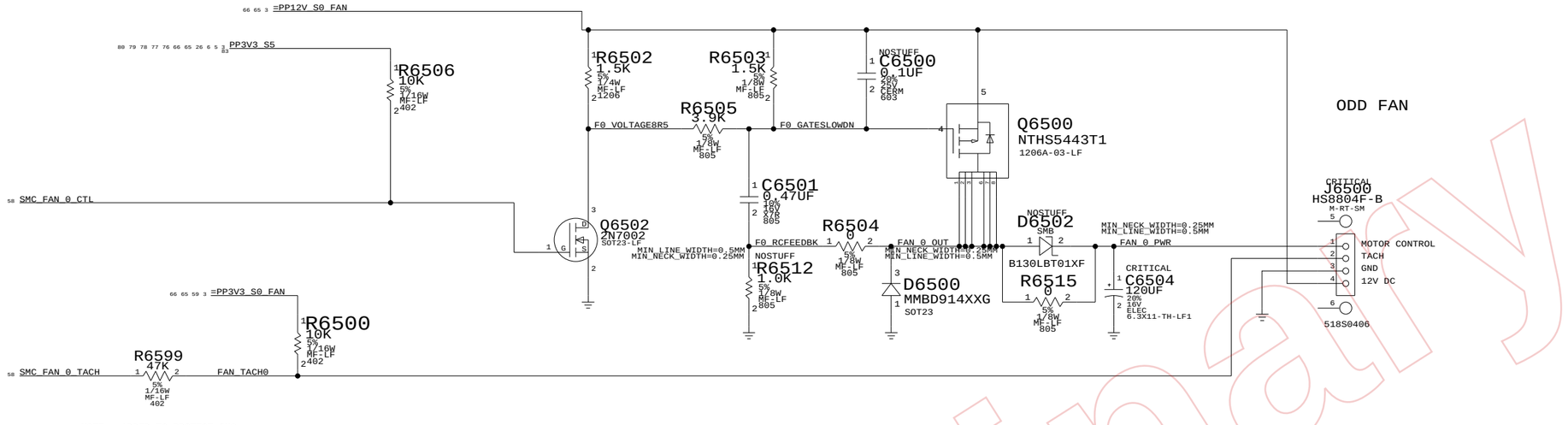
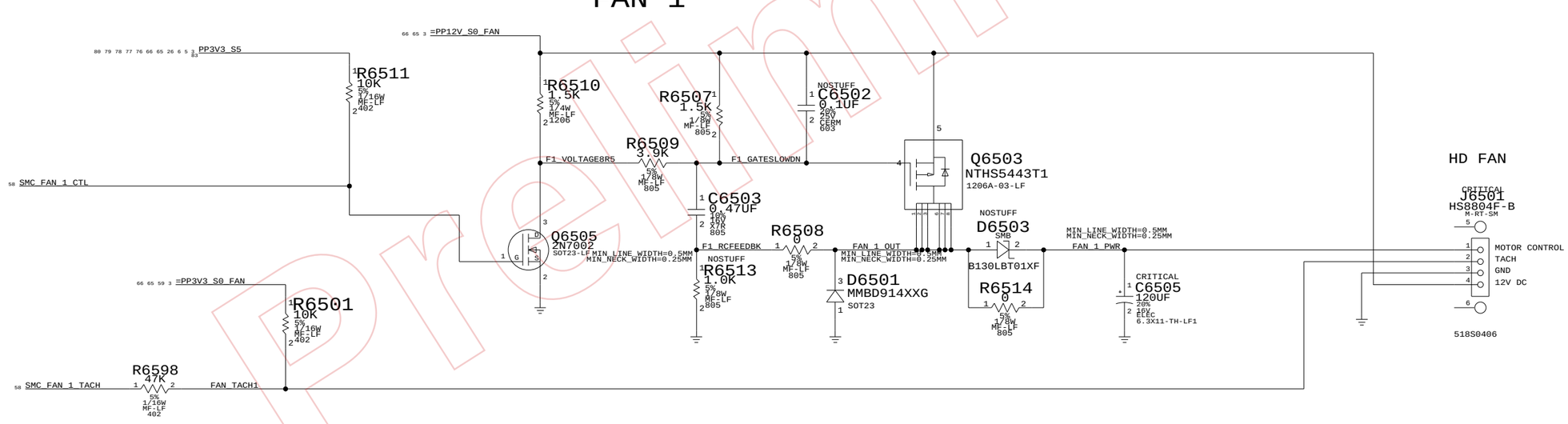
SCALE: NONE	SHT 63 OF 97	

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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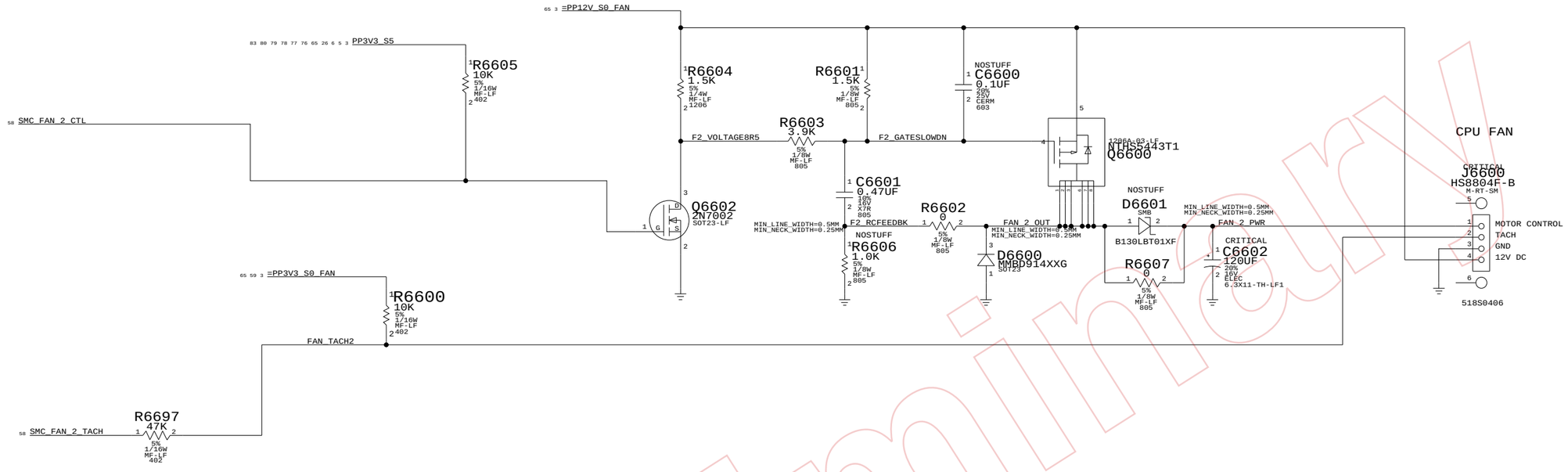
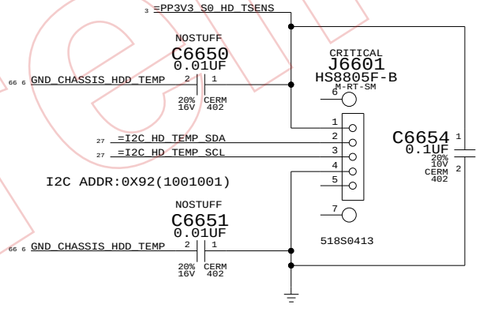
D	051-7039	17
SCALE: NONE	SHT 65 OF 97	

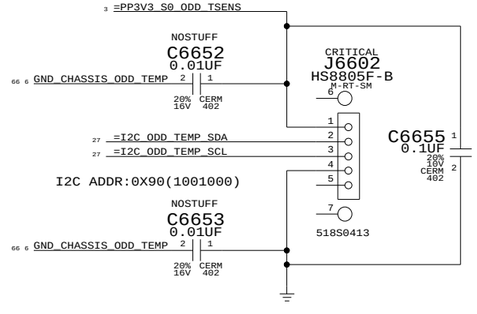
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR

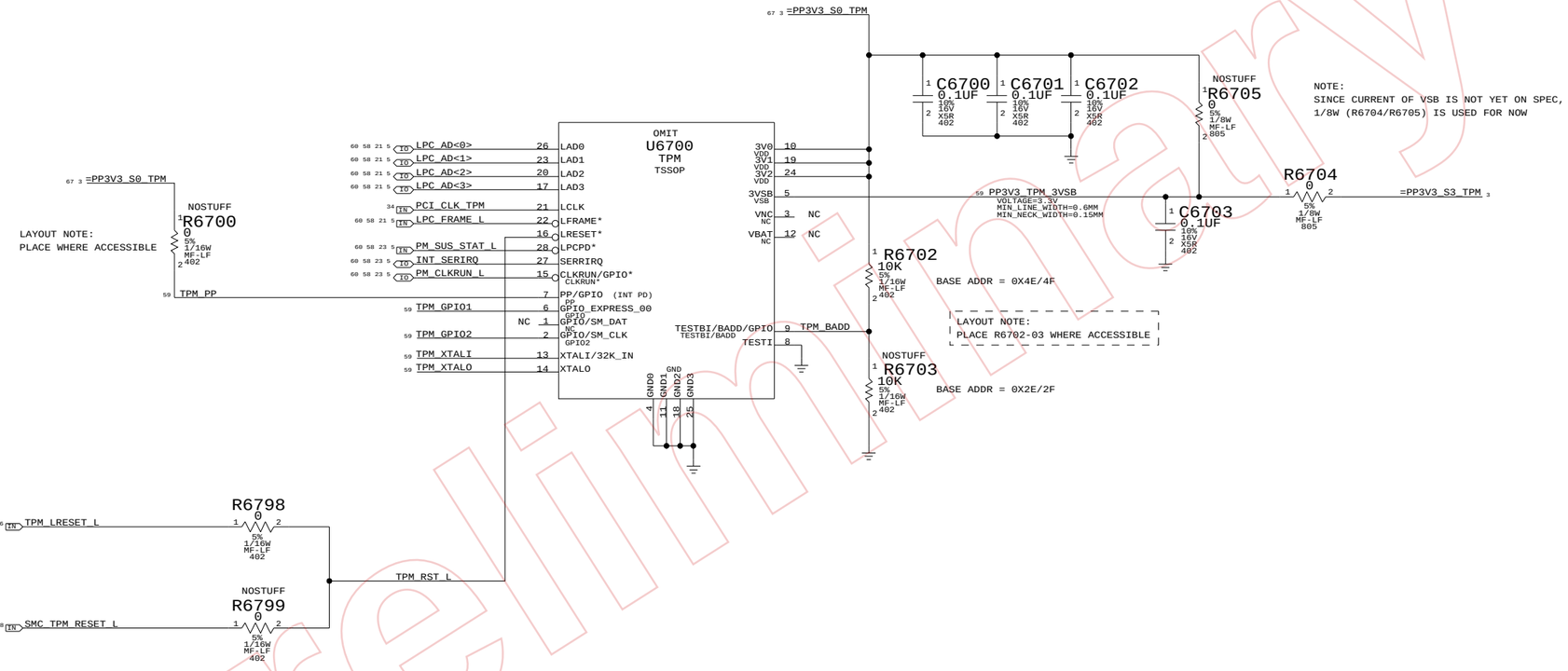


CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 66 OF 97	



TPM

SYNC_MASTER=M50_HENRY SYNC_DATE=05/19/2006

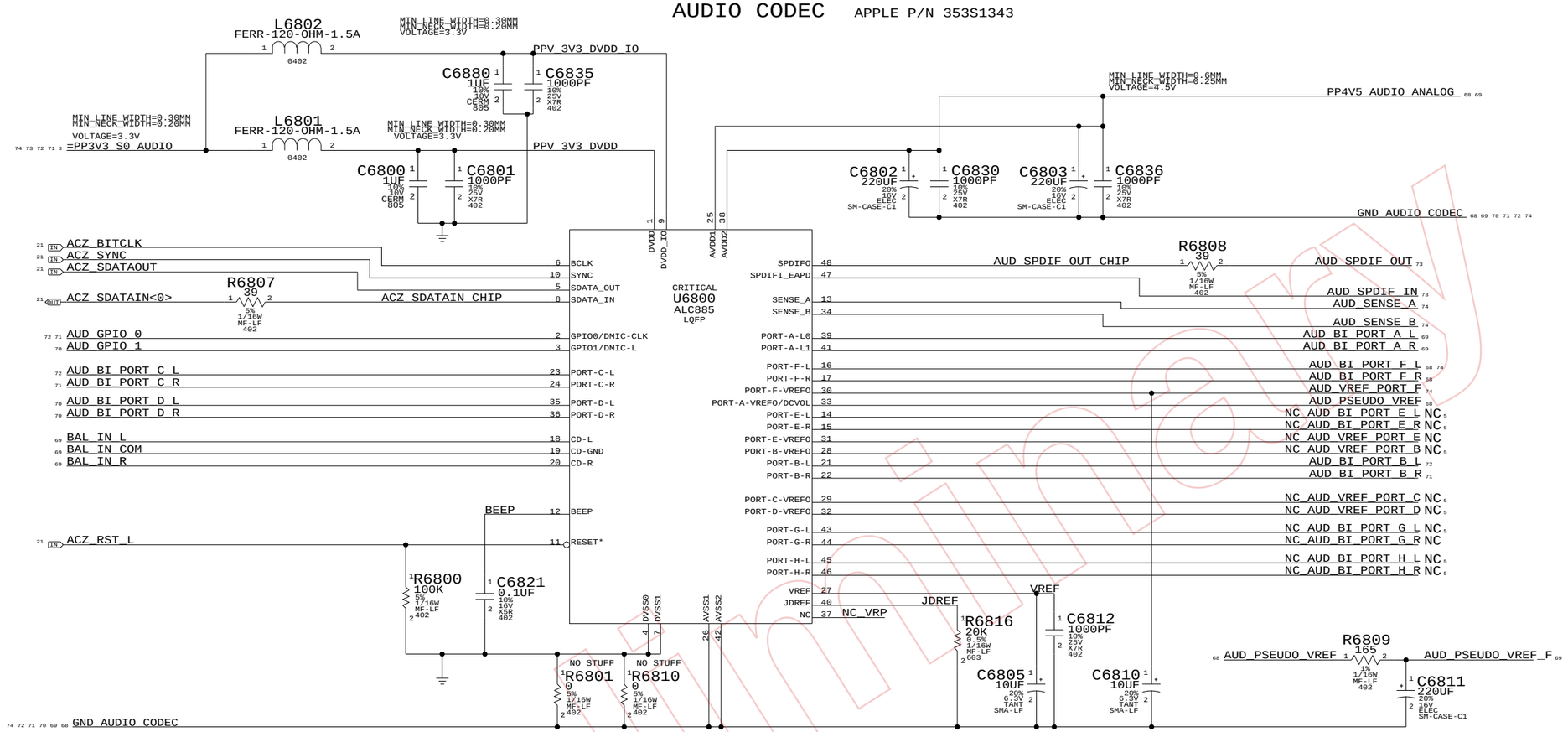
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

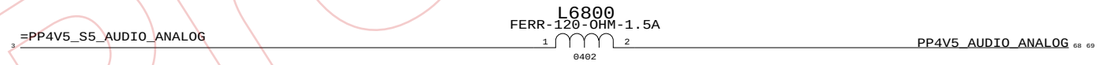
SCALE	SHT
NONE	67 OF 97

AUDIO CODEC

APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



MIC INPUT TO BOTH L&R

AUD_BI_PORT_F_L — AUD_BI_PORT_F_R

SYNC_MASTER=AUDIO	SYNC_DATE=05/19/2006

NOTICE OF PROPRIETARY PROPERTY

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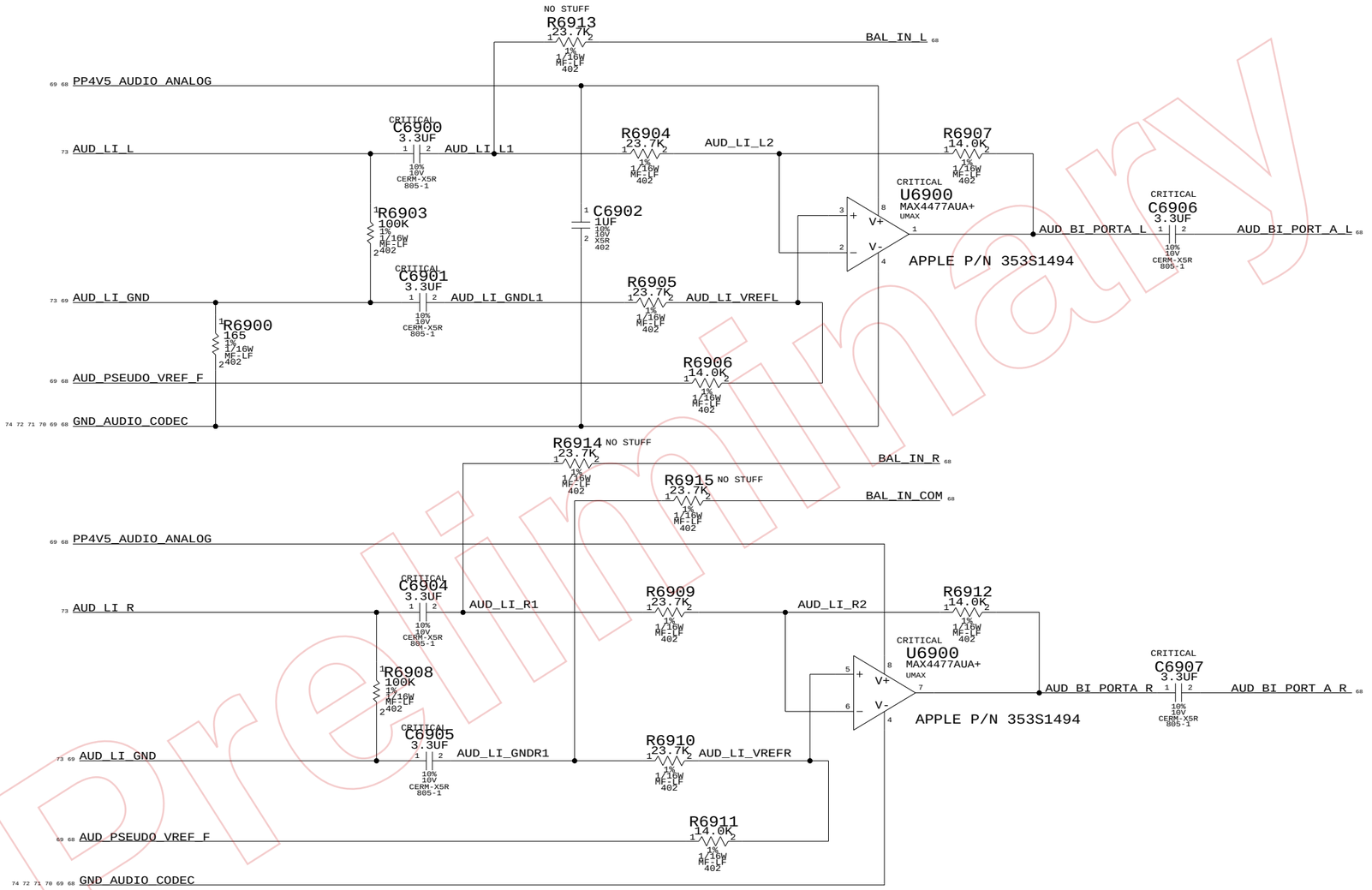
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17

SCALE	SHT
NONE	68 OF 97

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59



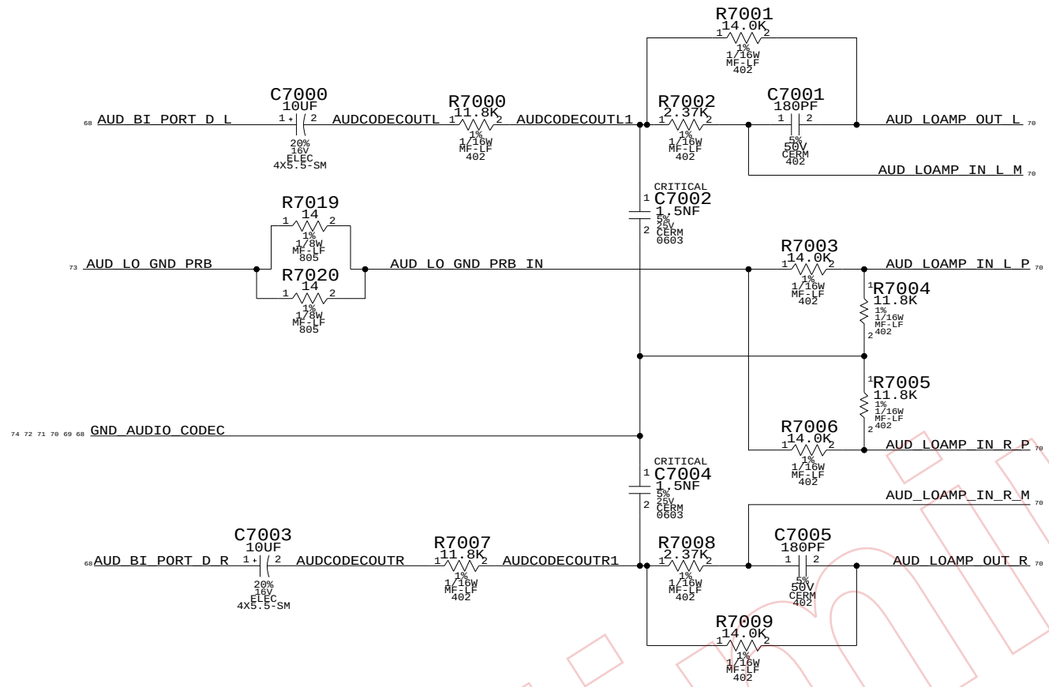
AUDIO: LINE INPUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 69 OF 97	

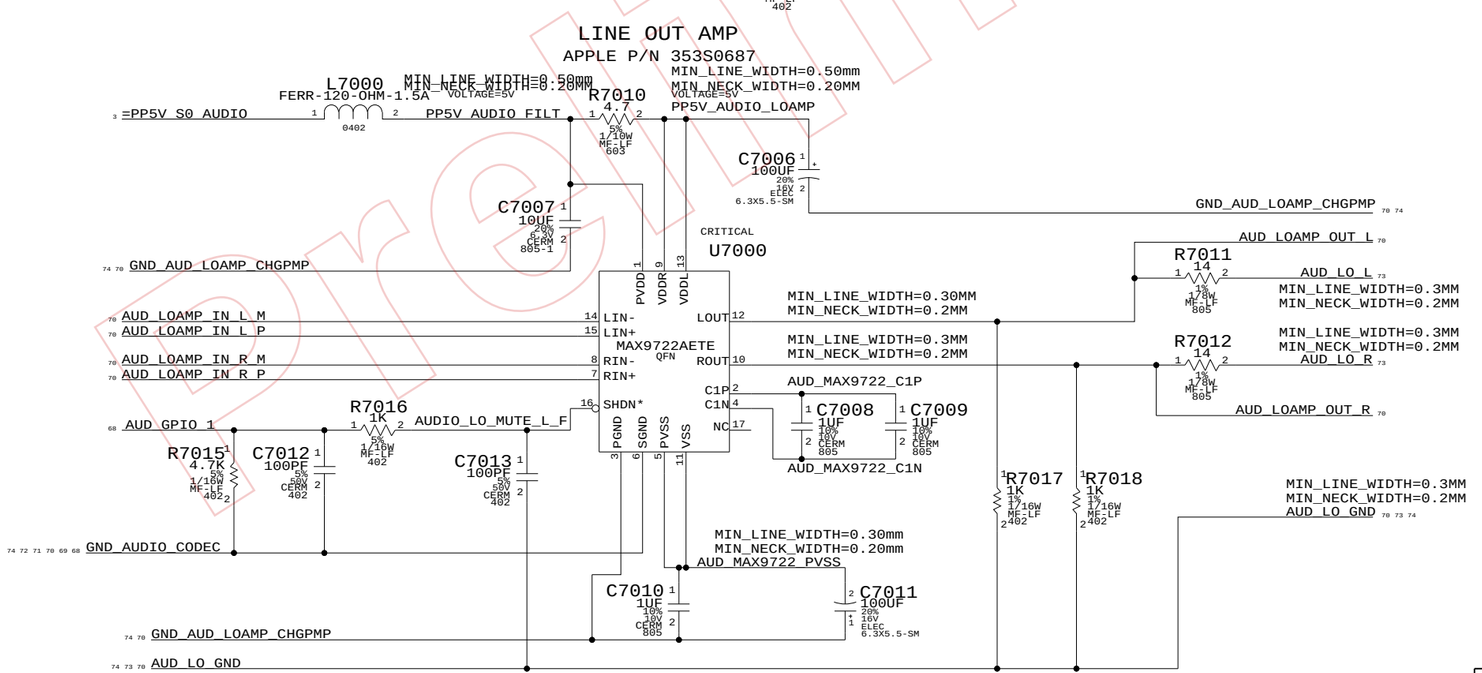
LINE OUT LOW-PASS FILTER

Fc = 37 KHZ, Av = -1.18



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: COMBO OUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 70 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

=PP12V_S5_AUDIO_SPKRAMP
R7170 0.005 1% 1/4W MF-LF 1206
L7122 FERR-250-OHM SM-1
L7100 FERR-250-OHM SM-1
12V_S5_SPKRAMP
PP12V_AUD_SPKRAMP_PLANE
C7117 470UF 20% 25V ELEC 10X10-SM
C7100 470UF 20% 25V ELEC 10X10-SM
C7101 10UF 10% 16V CERM 1210
C7118 0.1UF 20% 16V CERM 603
C7102 1UF 10% 16V X7R 805
C7119 0.1UF 20% 16V CERM 603
C7103 10UF 10% 16V CERM 1210
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC
AUD_BI_PORT_C_R
AUD_BI_PORT_B_R
L7105 1000-OHM-200MA 0603
L7106 1000-OHM-200MA 0603
L7107 1000-OHM-200MA 0603
L7108 1000-OHM-200MA 0603
C7104 0.47UF 10% 16V X7R 805
C7105 0.47UF 10% 16V X7R 805
C7106 0.47UF 10% 16V X7R 805
C7107 0.47UF 10% 16V X7R 805
C7115 100PF 5% 50V CERM 402
C7116 100PF 5% 50V CERM 402
AUDSAMPINLN
AUDSAMPINLP
AUDSAMPINRP
AUDSAMPINRN
AUD_SAMP_INL_N
AUD_SAMP_INL_P
AUD_SAMP_INR_P
AUD_SAMP_INR_N
AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2
AUD_SAMP_SHDN_L
AUD_MAX9714_VREG
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
CRITICAL
U7100
MAX9714
QFN-LF
VDD
CHOLD
INL-
INL+
INR+
INR-
G1
G2
FS1
FS2
SHDN*
NC
REG
THM
AGND PAD
PGND
SS
OUTL+
OUTL-
C1+
C1-
OUTR+
OUTR-
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD
AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPCPP
AUDSAMPCPN
C7108 0.1UF 10% 50V X7R 603-1
AUDSAMPOURTP
AUDSAMPOUTRN
SPKRAMP_SS
C7109 0.47UF 10% 16V X7R 805
L7101 180-OHM-1.5A 0603-LF
L7102 180-OHM-1.5A 0603-LF
L7103 180-OHM-1.5A 0603-LF
L7104 180-OHM-1.5A 0603-LF
AUD_SPKR_OUTCR_P
AUD_SPKR_OUTCR_N
AUD_SPKR_OUTBR_P
AUD_SPKR_OUTBR_N
C7110 1000PF 10% 25V X7R 402
C7111 1000PF 10% 25V X7R 402
C7112 1000PF 10% 25V X7R 402
C7113 1000PF 10% 25V X7R 402
XW7102 SM OMIT
XW7101 SM OMIT
GND_AUDIO_SPKRAMP
R7113 47K 5% 1/16W MF-LF 402
R7112 4.7K 5% 1/16W MF-LF 402
C7120 100PF 5% 50V CERM 402
C7121 100PF 5% 50V CERM 402
C7114 1UF 10% 25V X5R 603
R7119 NOSTUFF 0 5% 1/16W MF-LF 402

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO
RP7100 47K 5% 1/16W SM-LF
AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1
R7118 NOSTUFF 0 5% 1/16W MF-LF 402
R7108 NOSTUFF 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP_1
SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006

APPLE COMPUTER INC.
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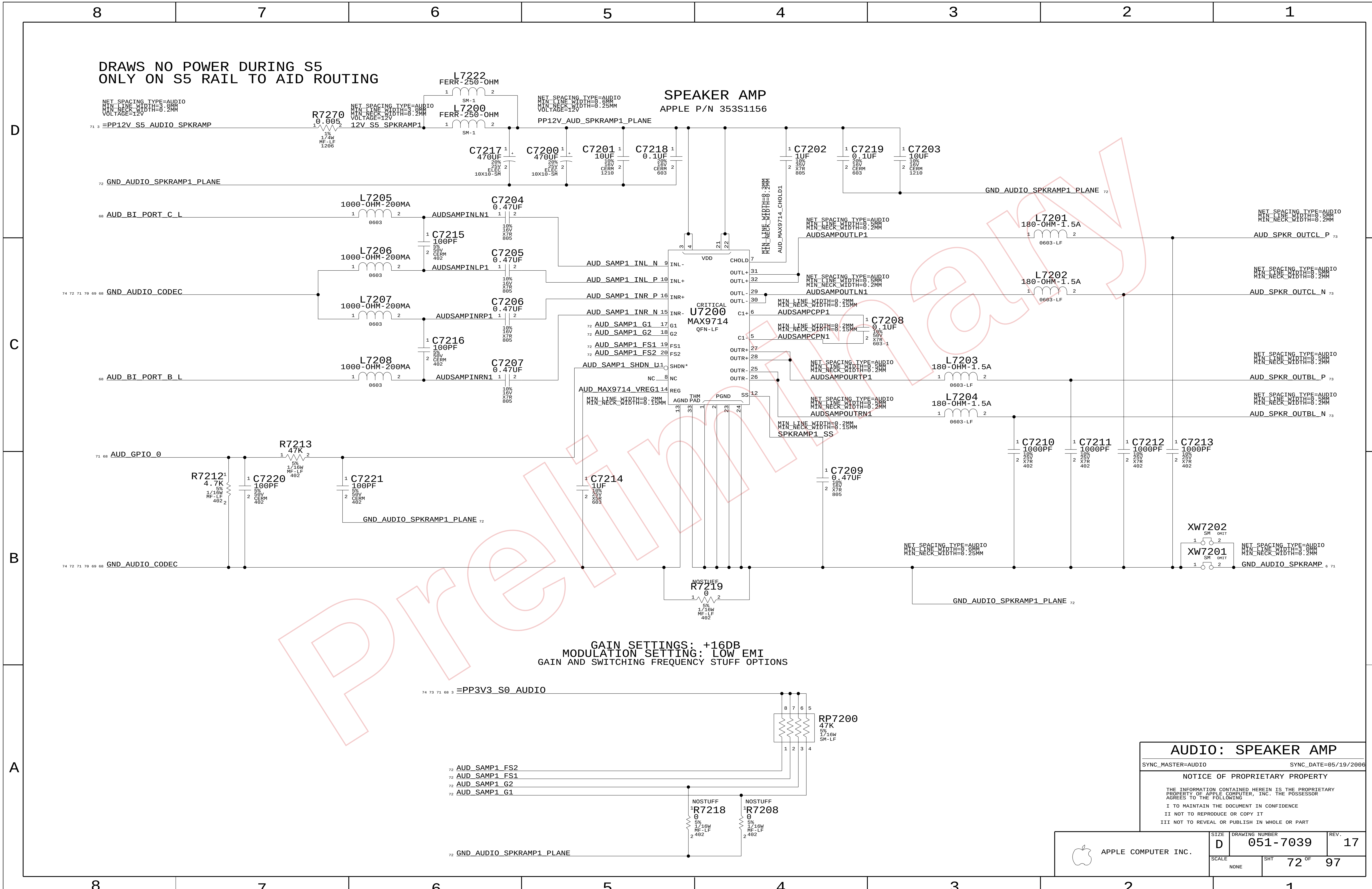
DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING
SPEAKER AMP
APPLE P/N 353S1156
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
=PP12V_S5_AUDIO_SPKRAMP
R7270
0.005
1%
1/4W
MF-LF
1206
12V_S5_SPKRAMP1
L7222
FERR-250-OHM
SM-1
L7200
FERR-250-OHM
SM-1
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V
PP12V_AUD_SPKRAMP1_PLANE
C7217
470UF
20%
25V
ELEC
10X10-SM
C7200
470UF
20%
25V
ELEC
10X10-SM
C7201
10UF
10%
16V
CERM
1210
C7218
0.1UF
20%
16V
CERM
603
C7202
1UF
10%
35V
X7R
805
C7219
0.1UF
20%
16V
CERM
603
C7203
10UF
10%
16V
CERM
1210
GND_AUDIO_SPKRAMP1_PLANE
L7205
1000-OHM-200MA
0603
AUD_BI_PORT_C_L
AUDSAMPINLN1
C7204
0.47UF
10%
16V
X7R
805
C7215
100PF
5%
50V
CERM
402
L7206
1000-OHM-200MA
0603
AUDSAMPINLP1
C7205
0.47UF
GND_AUDIO_CODEC
L7207
1000-OHM-200MA
0603
AUDSAMPINRP1
C7206
0.47UF
C7216
100PF
L7208
1000-OHM-200MA
0603
AUD_BI_PORT_B_L
AUDSAMPINRN1
C7207
0.47UF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD1
AUD_SAMP1_INL_N
AUD_SAMP1_INL_P
AUD_SAMP1_INR_P
AUD_SAMP1_INR_N
AUD_SAMP1_G1
AUD_SAMP1_G2
AUD_SAMP1_FS1
AUD_SAMP1_FS2
AUD_SAMP1_SHDN_L
AUD_MAX9714_VREG1
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
VDD
INL-
INL+
INR+
INR-
G1
G2
FS1
FS2
SHDN*
NC
REG
AGND
THM PAD
PGND
SS
CHOLD
OUTL+
OUTL-
C1+
C1-
OUTR+
OUTR-
CRITICAL
U7200
MAX9714
QFN-LF
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP1
AUDSAMPOUTLN1
AUDSAMPCPP1
AUDSAMPCPN1
C7208
0.1UF
10%
50V
X7R
603-1
AUDSAMPOUTRP1
AUDSAMPOUTRN1
SPKRAMP1_SS
L7201
180-OHM-1.5A
0603-LF
L7202
180-OHM-1.5A
0603-LF
L7203
180-OHM-1.5A
0603-LF
L7204
180-OHM-1.5A
0603-LF
AUD_SPKR_OUTCL_P
AUD_SPKR_OUTCL_N
AUD_SPKR_OUTBL_P
AUD_SPKR_OUTBL_N
C7210
1000PF
10%
25V
X7R
402
C7211
1000PF
C7212
1000PF
C7213
1000PF
AUD_GPIO_0
R7213
47K
5%
1/16W
MF-LF
402
R7212
4.7K
C7220
100PF
C7221
100PF
C7214
1UF
10%
25V
X5R
603
C7209
0.47UF
10%
16V
X7R
805
XW7202
SM
OMIT
XW7201
SM
OMIT
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP
NOSTUFF
R7219
0
5%
1/16W
MF-LF
402
GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS
=PP3V3_S0_AUDIO
RP7200
47K
5%
1/16W
SM-LF
AUD_SAMP1_FS2
AUD_SAMP1_FS1
AUD_SAMP1_G2
AUD_SAMP1_G1
NOSTUFF
R7218
0
NOSTUFF
R7208
0
GND_AUDIO_SPKRAMP1_PLANE
Preliminary

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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COMBO IN JACK
APPLE P/N 514-0328

CRITICAL
J7300
OPTI-AUD-IN-JCK-M51
F-ANG-TH

NC_AUD_LI_TYPE_JACK NC
AUD_LI_L_JACK
AUD_LI_DET_JACK
AUD_LI_R_JACK
AUD_LI_GND_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_SPDIFIN_JACK
AUD_SPDIF_GND
NC
GND_CHASSIS_AUDIO_EXTERNAL

OPTICAL RECEIVER

C7326 0.1UF 20% 10V CERM 402
R7305 0 5% 1/10W MF-LF 402
DZ7300 14V-15A 0405
DZ7303 14V-15A 0405

L7300 180-OHM-1.5A 0603-LF — AUD_LI_L_EMI
L7301 180-OHM-1.5A 0603-LF — AUD_LI_DET_EMI
L7302 180-OHM-1.5A 0603-LF — AUD_LI_R_EMI
L7303 180-OHM-1.5A 0603-LF — AUD_LI_GND_EMI
L7304 180-OHM-1.5A 0603-LF — AUD_LI_L
L7305 180-OHM-1.5A 0603-LF — AUD_LI_DET_H
L7306 180-OHM-1.5A 0603-LF — AUD_LI_R
L7307 180-OHM-1.5A 0603-LF — AUD_LI_GND

R7306 39 5% 1/16W MF-LF 402 — AUD_SPDIF_IN

C7300 100PF 5% 50V CERM 402
C7301 100PF 5% 50V CERM 402
C7302 100PF 5% 50V CERM 402
C7303 100PF 5% 50V CERM 402

XW7300 SM

L7309 180-OHM-1.5A 0603-LF — AUD_MIC_IN_P
L7310 180-OHM-1.5A 0603-LF — AUD_MIC_IN_N
L7312 180-OHM-1.5A 0603-LF — GND_AUDIO_MIC_CONN, AUD_MIC_IN_P_CONN
L7313 180-OHM-1.5A 0603-LF — AUD_MIC_IN_N_CONN

C7321 100PF 5% 50V CERM 402
C7322 100PF 5% 50V CERM 402
DZ7304 NOSTUFF 14V-15A 0405

TO FHB CONNECTOR PAGE 47
TO POWER SUPPLY PAGE 6

SPEAKER CABLE CONNECTORS
APPLE P/N 518-0193
APPLE P/N 518-0255

PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO

CRITICAL
J7301
87833-0431
M-RT-TH

AUD_SPKR_OUTBL_P — AUD_SPKR_OUTBL_N
AUD_SPKR_OUTCL_N — AUD_SPKR_OUTCL_P

PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO

CRITICAL
J7302
87833-0631
M-RT-TH

AUD_SPKR_OUTBR_P — AUD_SPKR_OUTBR_N
NC_J7302_3 — NC_J7302_6
AUD_SPKR_OUTCR_N — AUD_SPKR_OUTCR_P

LINE OUT JACK
APPLE P/N 514-0329

L7314 180-OHM-1.5A 0603-LF — AUD_SPDIF_OUT, AUD_SPDIF_OUT_JACK
L7315 180-OHM-1.5A 0603-LF — =PP3V3_S0_AUDIO, PP3V3_AUDIO_SPDIF_EMI
L7316 180-OHM-1.5A 0603 — AUD_LO_DET1, AUD_LO_DET1_EMI
L7318 180-OHM-1.5A 0603-LF — AUD_LO_L, AUD_LO_L_EMI
L7319 180-OHM-1.5A 0603-LF — AUD_LO_DET2, AUD_LO_DET2_EMI
L7317 180-OHM-1.5A 0603-LF — AUD_LO_R, AUD_LO_R_EMI
L7320 180-OHM-1.5A 0603-LF — AUD_LO_GND_PRB, AUD_LO_GND_EMI
L7380 180-OHM-1.5A 0603-LF — AUD_LO_GND, GND_AUDIO_CODEC_EMI1

L7323 180-OHM-1.5A 0603-LF — PP3V3_AUDIO_SPDIF_JACK
L7324 180-OHM-1.5A 0603-LF
L7326 180-OHM-1.5A 0603-LF — AUD_LO_DET1_JACK, AUD_LO_L_JACK
L7327 180-OHM-1.5A 0603-LF — AUD_LO_DET2_JACK, AUD_LO_R_JACK
L7325 180-OHM-1.5A 0603-LF
L7328 180-OHM-1.5A 0603-LF — AUD_LO_GND_JACK
L7381 180-OHM-1.5A 0603-LF

C7317 0.1UF 20% 10V CERM 402
C7318 1UF 10% 10V CERM 805

CRITICAL
J7303
OPTI-AUD-OUT-JCK-M51
F-ANG-TH

TYPE_DET, TIP, TIP_DET, RING, GND_1, GND_2
VIN, VCC, GND (LED)

R7302 0 5% 1/10W MF-LF 402
AUD_SPDIF_GND — NC

C7311 100PF 5% 50V CERM 402
C7312 100PF 5% 50V CERM 402
C7314 100PF 5% 50V CERM 402
C7313 100PF 5% 50V CERM 402
C7315 100PF 5% 50V CERM 402
C7323 100PF 5% 50V CERM 402
C7380 100PF 5% 50V CERM 402

DZ7301 14V-15A 0405
DZ7302 14V-15A 0405

GND_CHASSIS_AUDIO_EXTERNAL

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 73 OF 97	

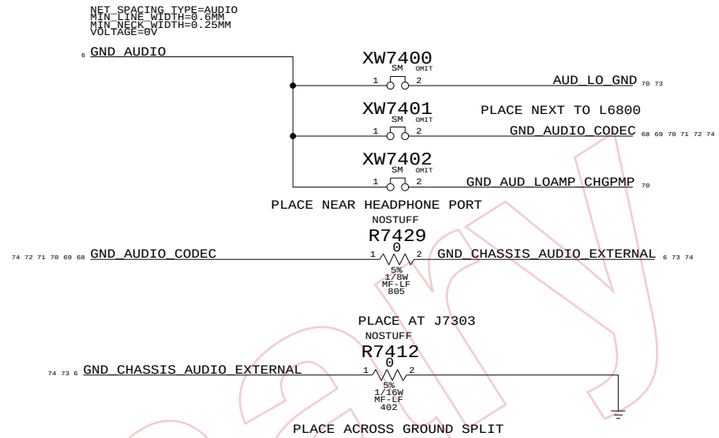
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14(D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18(B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A(C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN 0X16H		

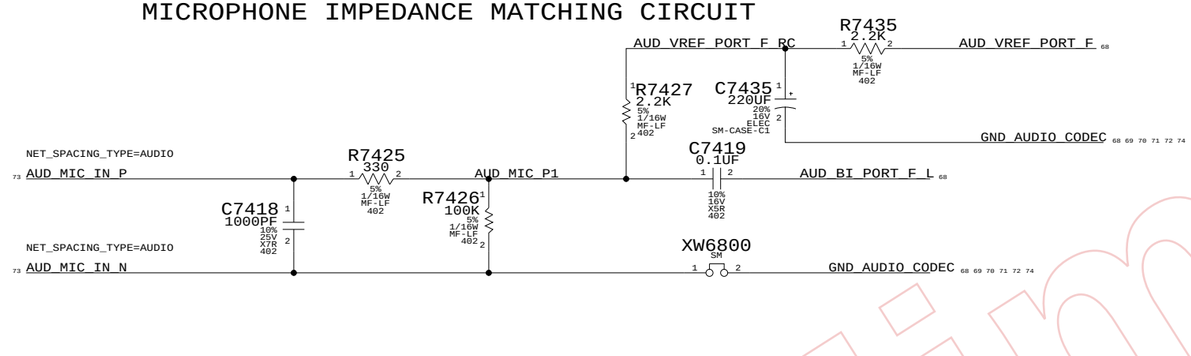
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19(F)	80%
LINE INPUT	0X08	0X23	0X15(A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

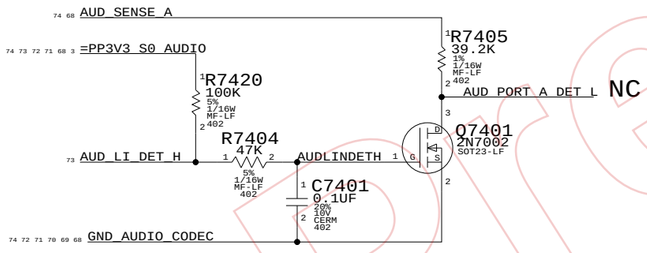
AUDIO GROUND RETURNS



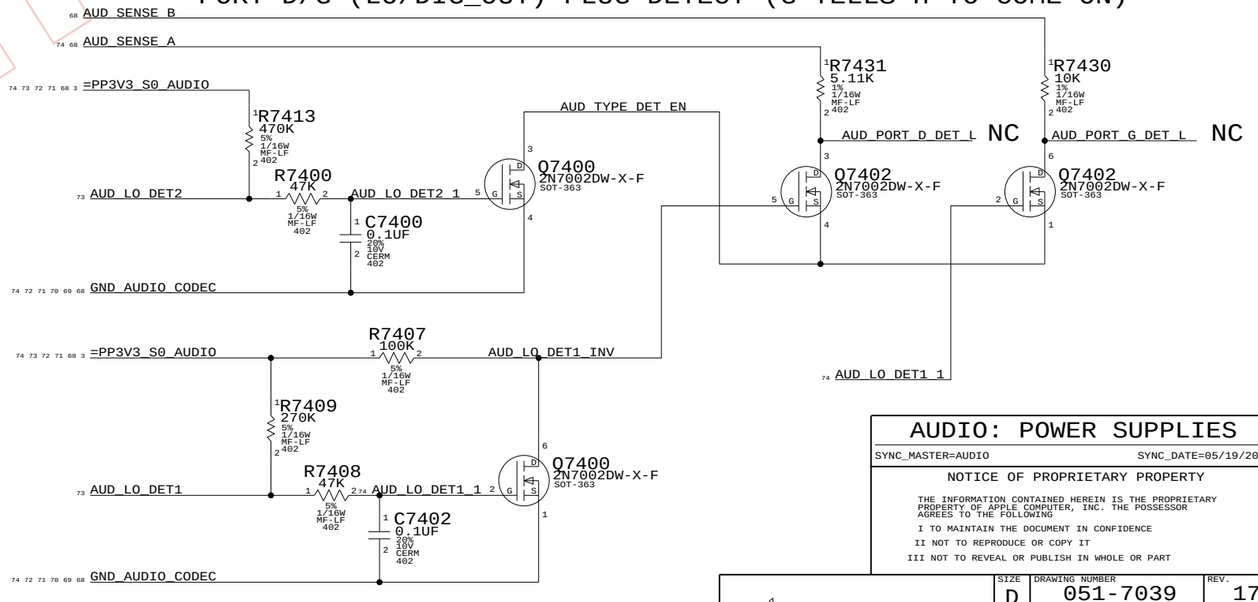
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 74 OF 97	

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCORE REGULATOR

CPU_VCCSENSE_P & N ARE DIFF PAIRS
ROUTE AS 18MIL WIDE, 7MIL SPACE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator	
SYNC_MASTER=M50_PAUL	SYNC_DATE=05/19/2006

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 17
	SCALE NONE	SHT 75 OF 97	

PROCESSOR VCORE SENSE

PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)

75 5 3 PPVCORE_CPU — R7612 4.53K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — SMC_CPU_VSENSE 58

C7612 0.22UF 20% 6.3V X5R 402 (CPU_PWR_SENSE)

GND_SMC_AVSS 58 59 76 84

PROCESSOR VCORE CURRENT SENSE

(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

C7600 470PF 10% 50V CERM 402 (CPU_PWR_SENSE) — CPU_ISENSE_OUT_R

R7609 1M 1% 1/16W MF-LF 402 (CPU_PWR_SENSE)

C7601 0.1UF CERM 20% 402 10V CRITICAL (CPU_PWR_SENSE)

84 83 76 41 27 26 10 6 5 3 PP3V3_S0

75 IMVP6_VO — R7659 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — IMVP6_VO_R_OA

R7605 40.2K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — CPU_ISENSE_R_POS

U7600 LMV2011MF SOT23-5 (CRITICAL, CPU_PWR_SENSE) — GND_CPU_ISENSE_OPAMP

75 IMVP6_DROOP — R7669 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — IMVP6_DROOP_R

R7606 40.2K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — CPU_ISENSE_R_NEG

MIN_LINE_WIDTH=0.20 MM

C7603 470PF 10% 50V CERM 402 (CPU_PWR_SENSE)

R7603 1M 1% 1/16W MF-LF 402 (CPU_PWR_SENSE)

NOSTUFF R7604 0 5% 1/16W MF-LF 402

R7607 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — GND_NEXT_TO_SMC 59

PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)

R7602 4.53K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — SMC_CPU_ISENSE 58

C7602 0.22UF 20% 6.3V X5R 402 (CPU_PWR_SENSE)

GND_SMC_AVSS 58 59 76 84

CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

83 3 PP12V_S0_B

R7639 10K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

Q7640 NTR4101P SOT-23 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L — MIN_LINE_WIDTH=0.20 MM, MIN_NECK_WIDTH=0.20 MM

R7641 10K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L_R

Q7639 2N7002 SOT23-LF (CPU_PWR_SENSE)

58 5 ISENSE_CAL_EN

R7640 100K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

ISENSE_CAL_EN_LS12V

R7642 470K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

9 8 3 =PPVCORE_S0_CPU

R7643 1.00 1% 1/4W MF-LF 1206 (CPU_PWR_SENSE)

CPUVCORE_ISENSE_CAL — MIN_LINE_WIDTH=0.50 mm, MIN_NECK_WIDTH=0.20 mm

Q7641 FDC796N SUPERSOT-6 CRITICAL (CPU_PWR_SENSE)

SMC PWRGD PULLUP

83 80 79 78 77 66 65 26 6 5 3 PP3V3_S5

R7623 10K 1% 1/16W MF-LF 402

NOSTUFF R7620 0 5% 1/16W MF-LF 402

82 78 6 SYS_POWERFAIL_L — RSMRST_PWRGD 58

SYSTEM CURRENT SENSE

PP12V_S5_AC_DC — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

R7650 0.005 1% 1W MF 2010 CRITICAL (SYS_PWR_SENSE)

PP12V_S5 3 76 77 78 79 80 82 83

PCB:KEEP SHORTS NEXT TO U7602

PCB:PLACE D7650,R7652,C7650 BY SMC

U7602 ZXCT1010 SOT23-5 CRITICAL (SYS_PWR_SENSE) — VIN, IOUT, NC, LOAD, GND

OMIT XW7650 SM — SYSTEM_DCIN_SENSE — SYSTEM_SENSE_I_R

R7651 5.90K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

R7652 4.53K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SMC_DCIN_ISENSE 58

PP3V3_S0 3 5 6 10 26 27 41 76 83 84

D7650 BAS16-75V-0.25A SOT23-LF NOSTUFF → TO SMC

C7650 0.22UF 20% 6.3V X5R 402 (SYS_PWR_SENSE) — 1 MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.

GND_SMC_AVSS 58 59 76 84

R7656 100 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SYSTEM_SENSE_SET

SCALE	COUNT
3.33333 A/V	.010753 A/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION

SYSTEM VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)

83 82 80 79 78 77 76 3 PP12V_S5

R7653 6.04K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

R7654 2.0K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

SMC_SYSTEM_VSENSE_R

R7655 4.53K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SMC_PBUS_VSENSE 58

C7651 0.22UF 20% 6.3V X5R 402 (SYS_PWR_SENSE)

GND_SMC_AVSS 58 59 76 84

PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)

SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	0 TO 3.3V

CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE — SYNC_DATE=(MASTER)

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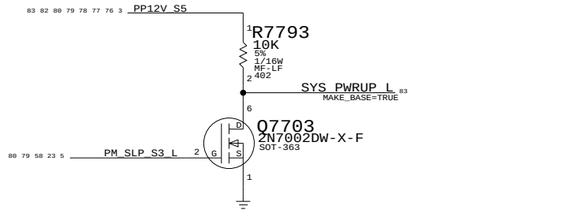
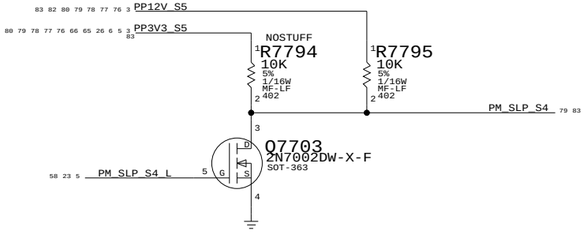
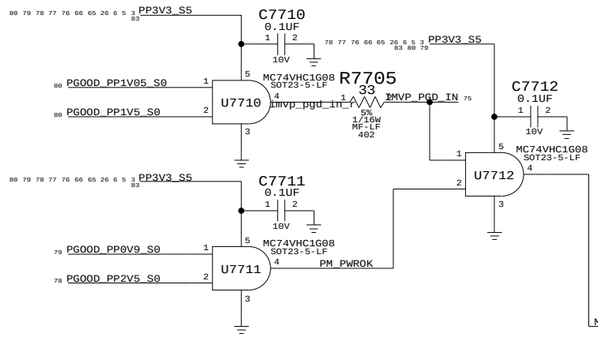
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 76 OF 97	

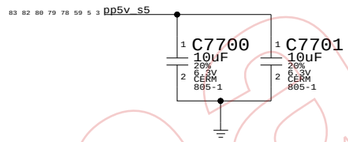


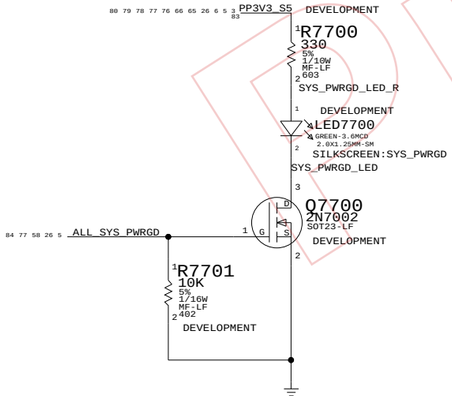




ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 on page 82





PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 77 OF 97	

3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

3.3V S5
POWER BUDGET
MISC=1.500A
SB=0.500A
AIRPORT=1.000A
PANEL=1.000A
TOTAL=4.000A

C7892 1UF 10% 25V XSR 603

PP12V_S5

=PP3V3_S5_2V5_LDO

C7820 22UF 20% 6.3V X5R 805

CRITICAL Q7803 IRF1902PBF SO-8

3V3REG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7805 10 1% 1/16W MF-LF 402

C7800 1UF 10% 6.3V CERM 402

3V3REG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

3V3REG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7823 1000PF 10% 25V X7R 402

2V5_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7821 2.7K 5% 1/10W MF-LF 402

C7824 1000PF 10% 25V X7R 402

3V3REG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

U7800 ISL6549 QFN

VCC12 VCC5 PVCC5 LDO_DR LDO_FB FS_DIS THRML_PAD DGND AGND PGND BOOT PHASE UGATE LGATE FB COMP

3V3REG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7840 2.2 5% 1/10W MF-LF 402

3V3REG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

3V3REG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7801 0.1UF 20% 25V CERM 603

3V3REG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

CRITICAL Q7800 IRLR7807Z TO-252AA

CRITICAL Q7801 IRLR7807Z TO-252AA

3V3REG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

3V3REG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

3V3REG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7804 8.06K 1% 1/16W MF-LF 402

C7808 0.047UF 10% 16V CERM 402

3V3REG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7806 560PF 10% 50V CERM 402

C7802 1000PF 10% 25V X7R 402

D7800 CTLSH3-30M833 TLM833

nostuff

CRITICAL C7853 1000UF 20% 16V ELEC TH-KZJ-LF

C7811 10UF 10% 16V CERM 1210

L7803 3.0UH TH1 CRITICAL

PP3V3_S5 3.35V NOMINAL

R7802 5.11 1% 1/4W MF-LF 1206

3V3REG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7809 1000PF 5% 50V CERM 1206

CRITICAL C7815 1800UF 20% 6.3V ELEC TH-KZJ-LF

C7814 10UF 20% 6.3V CERM 805-1

C7813 10UF 20% 6.3V CERM 805-1

PP2V5_S5 2.50V NOMINAL

C7825 10UF 20% 6.3V CERM 805-1

C7822 10UF 20% 6.3V CERM 805-1

C7821 10UF 20% 6.3V CERM 805-1

C7826 10UF 20% 6.3V CERM 805-1

R7820 1K 1% 1/16W MF-LF 402

R7822 470 1% 1/16W MF-LF 402

XW7800 SM

R7899 22 5% 1/16W MF-LF 402

3V3REG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7807 0.01UF 10% 16V CERM 402

R7803 1.24K 1% 1/16W MF-LF 402 (R2)

R7801 392 1% 1/16W MF-LF 402 (R1)

5% OK ON R7801?

VOUT=VREF*(1+R2/R1)

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

3V3REG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7892 100K 5% 1/16W MF-LF 402

NOSTUFF Q7802 2N7002 SOT23-LF

SYS_POWERFAIL_L

C7803 4.7UF 20% 6.3V CERM 603

3V3REG_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PP5V_S5

PP3V3_S5

C7880 0.1UF 20% 10V CERM 402

R7811 2.49K 1% 1/16W MF-LF 402

R7810 10K 1% 1/16W MF-LF 402

2V2_REF 2.219V

U7810 LM339A SOI-LF

PP2V5_S0

PGOOD_PP2V5_S0

R7812 5.11K 1% 1/16W MF-LF 402

SPARE COMPARATOR

3V DC/DC 2.5V

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7039 | REV. 17

SCALE NONE | SHT 78 OF 97

TRUE

1.8V AND 1.2V S3 REGULATOR

1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A

C7992 1UF 10% 25V X5R 603

=PP1V8_S3_1V2_LDO

C7920 22UF 20% 6.3V X5R 805

CRITICAL Q7903 IRF1902PBF SO-8

PP12V_S5

1V8REG_DDR_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7905 10 1% 1/16W MF-LF 402

C7900 1UF 10% 6.3V CERM 402

1V8REG_DDR_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

1V8REG_DDR_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7923 1000PF 10% 16V X7R 402

VCC12
CRITICAL U7900 ISL6549 QFN
VCC5 PVCC5 LDO_DR LDO_FB FS_DIS THRML_PAD DGND AGND PGND
UGATE BOOT PHASE LGATE FB COMP

1V8REG_DDR_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7940 2.2 5% 1/16W MF-LF 402

1V8REG_DDR_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

1V8REG_DDR_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7901 0.1UF 20% 25V CERM 603

1V8REG_DDR_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q7900 IRLR7807Z TO-252AA

CRITICAL C7953 1000UF 20% 16V ELEC TH-KZJ-LF

CRITICAL C7954 1000UF 20% 16V ELEC TH-KZJ-LF

C7911 10UF 10% 16V CERM 1210

C7912 10UF 10% 16V CERM 1210

1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A

L7903 1.53UH TH-LF CRITICAL

PP1V8_S3 1.81V NOMINAL

CRITICAL C7956 1500UF 20% 6.3V ELEC TH-MCZ

CRITICAL C7957 1500UF 20% 6.3V ELEC TH-MCZ

C7913 10UF 20% 6.3V CERM 805-1

C7958 1UF 10% 6.3V CERM 402

C7959 1UF 10% 6.3V CERM 402

C7960 1UF 10% 6.3V CERM 402

PP1V2_S3 1.21V NOMINAL

C7925 10UF 20% 6.3V CERM 805-1

C7922 10UF 20% 6.3V CERM 805-1

C7921 10UF 20% 6.3V CERM 805-1

C7926 10UF 20% 6.3V CERM 805-1

R7920 1K 1% 1/16W MF-LF 402

1V2_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7921 2.7K 5% 1/16W MF-LF 402

C7924 1000PF 10% 25V X7R 402

1V8REG_DDR_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7922 1.96K 1% 1/16W MF-LF 402

1V8REG_DDR_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

1V8REG_DDR_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

1V8REG_DDR_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7904 8.06K 1% 1/16W MF-LF 402

C7908 0.047UF 10% 16V CERM 402

1V8REG_DDR_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7906 560PF 10% 50V CERM 402

XW7900 SM

D7900 CTLSH3-30M833 TLM833

Q7901 IRLR7807Z TO-252AA

C7902 1000PF 10% 25V X7R 402

nostuff

R7902 5.11 1% 1/4W MF-LF 1206

1V8REG_DDR_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7909 1000PF 5% 50V CERM 1206

R7999 22 5% 1/10W MF-LF 402

R7903 1.24K 1% 1/16W MF-LF 402 (R2)

1V8REG_DDR_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7907 0.01UF 10% 16V CERM 402

R7901 953 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1V8REG_DDR_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7992 100K 5% 1/16W MF-LF 402

PM_SLP_S4

Q7902 2N7002 SOT23-LF

C7903 4.7UF 20% 6.3V CERM 603

1V8REG_DDR_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

PM_SLP_S3_L — MEMVTT_EN

PP5V_S5
PP3V3_S5

R7911 5.49K 1% 1/16W MF-LF 402

R7910 10K 1% 1/16W MF-LF 402

1V2_REF 1.21V

U7810 LM339A SOI-LF GND V+

PP1V8_S3

PGOOD_PP1V8_S3

R7912 2.7K 5% 1/16W MF-LF 402

PP5V_S5
PP3V3_S5

R7914 8.45K 1% 1/16W MF-LF 402

R7913 10K 1% 1/16W MF-LF 402

0V7_REF 0.723V

U7810 LM339A SOI-LF GND V+

PP0V9_S0

PGOOD_PP0V9_S0

R7915 2.37K 1% 1/16W MF-LF 402

PP3V3_S5

DEVELOPMENT R7906 330 5% 1/16W MF-LF 402

LED_PP1V8_S3_P

DEVELOPMENT LED7900 GREEN-3.6MCD 2.0X1.25MM-SM

PLACE_LED NEAR VREG

PP1V8_S3

DEVELOPMENT U7901 LM339A SOI-LF GND V+

1V0_REF

LED_PP1V8_S3_N

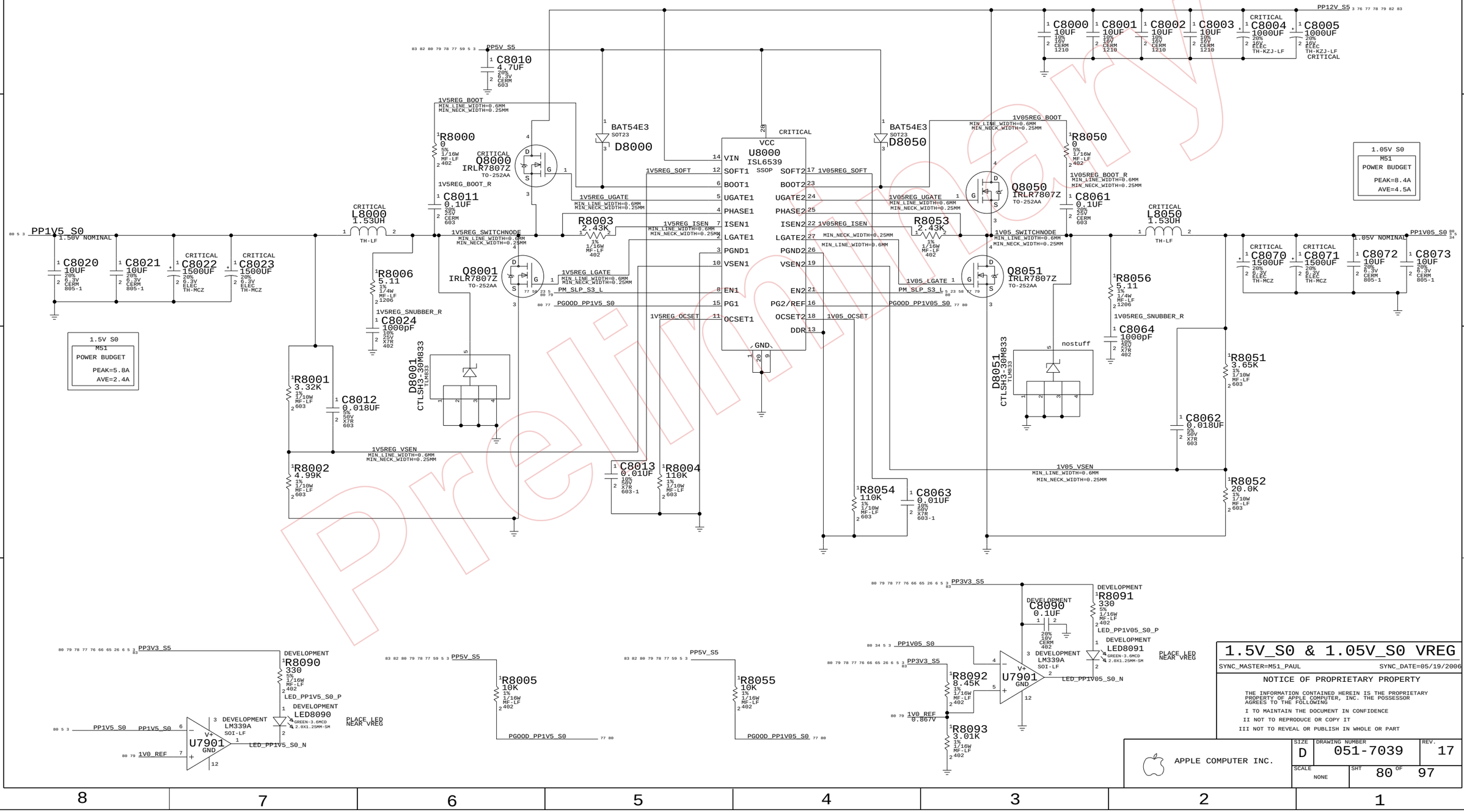
1.8V & 1.2V VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	17
SCALE: NONE	SHT 79 OF 97	

1.5V S0 AND 1.05V S0 RAILS



5V S5 AND 5V AUDIO S5 REGULATOR

=PP5V_S5_AUDIO_LDO
C8220 22UF 20% 6.3V X5R 805
CRITICAL Q8203 IRF1902PBF SO-8
5V AUDIO S5 — M50 POWER BUDGET — AUDIO=?A TOTAL=?A
PP4V5_S5_AUDIO_ANALOG 4.50V NOMINAL
C8225 10UF 20% 6.3V CERM 805-1
C8222 10UF 20% 6.3V CERM 805-1
C8221 10UF 20% 6.3V CERM 805-1
C8226 10UF 20% 6.3V CERM 805-1
R8220 1K 1% 1/16W MF-LF 402
R8222 221 1% 1/16W MF-LF 402
C8223 1000PF 10% 25V X7R 402
R8221 2.7K 5% 1/16W MF-LF 402
NOSTUFF C8224 1000PF 10% 25V X7R 402
5V_AUDIO_LDODR_C MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

83 80 79 78 77 76 3 PP12V_S5
C8292 1UF 10% 25V X5R 603
5VREG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8205 10 1% 1/10W MF-LF 402
5VREG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8200 1UF 10% 6.3V CERM 402

U8200 ISL6549 QFN
VCC12
VCC5
PVCC5 CRITICAL
LDO_DR
LDO_FB
FS_DIS
DGND AGND PGND THRML_PAD
UGATE BOOT PHASE LGATE FB COMP

5VREG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8240 2.2 5% 1/16W MF-LF 402
5VREG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8201 0.1UF 20% 25V CERM 603
5VREG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8204 8.06K 1% 1/16W MF-LF 402
5VREG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8206 470PF 10% 50V CERM 402
C8208 0.047UF 10% 16V CERM 402
XW8200 SM

CRITICAL Q8200 IRLR7807Z TO-252AA
CRITICAL Q8201 IRLR7807Z TO-252AA
C8202 1000PF 10% 25V X7R 402
NOSTUFF D8200 CTLSH3-30M833 TLM833
CRITICAL C8253 1000UF 20% 16V ELEC TH-KZJ-LF
C8211 10UF 20% 16V CERM 1210
L8203 3.0UH TH1 CRITICAL
R8202 5.11 1% 1/4W MF-LF 1206
5VREG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8209 1000PF 5% 50V CERM 1206
5V S5 — M50 POWER BUDGET — MISC=1.500A USB=1.500A AUDIO=1.000A ODD=1.000A TOTAL=5.000A
PP5V_S5 5.10V NOMINAL 3 5 59 77 78 79 80 83
CRITICAL C8215 1800UF 20% 6.3V ELEC TH-KZJ-LF
C8214 10UF 20% 6.3V CERM 805-1
C8213 10UF 20% 6.3V CERM 805-1
R8299 22 5% 1/16W MF-LF 402
R8203 1.24K 1% 1/16W MF-LF 402 (R2)
5VREG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8207 0.01UF 10% 16V CERM 402
R8201 232 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN, 0.800V TYP, 0.816V MAX

5VREG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8292 100K 5% 1/10W MF-LF 402
NOSTUFF Q8202 2N7002 SOT23-LF
78 76 6 SYS_POWERFAIL_L
C8203 4.7UF 20% 6.3V CERM 603
5VREG_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

SYNC_MASTER=M50_PAUL SYNC_DATE=05/19/2006

APPLE COMPUTER INC.

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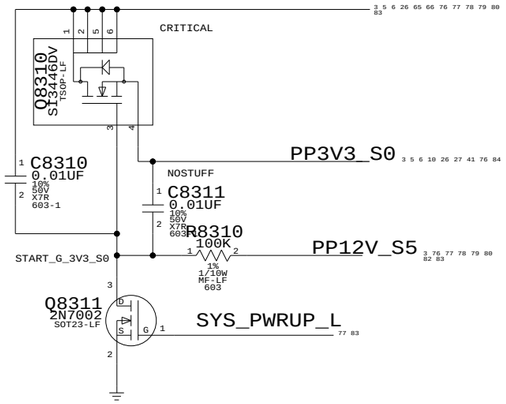
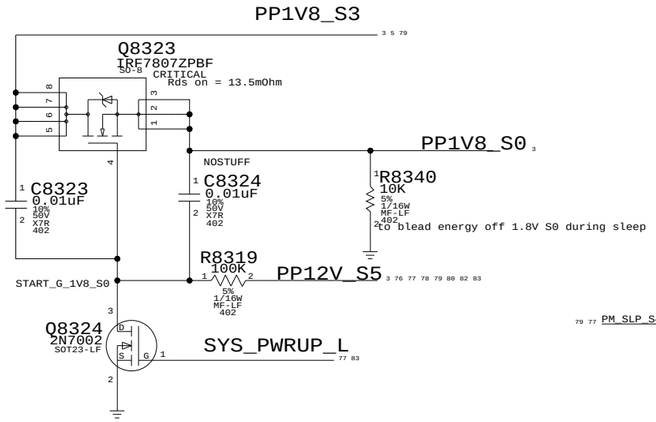
D	051-7039	17

SCALE: NONE — SHT 82 OF 97

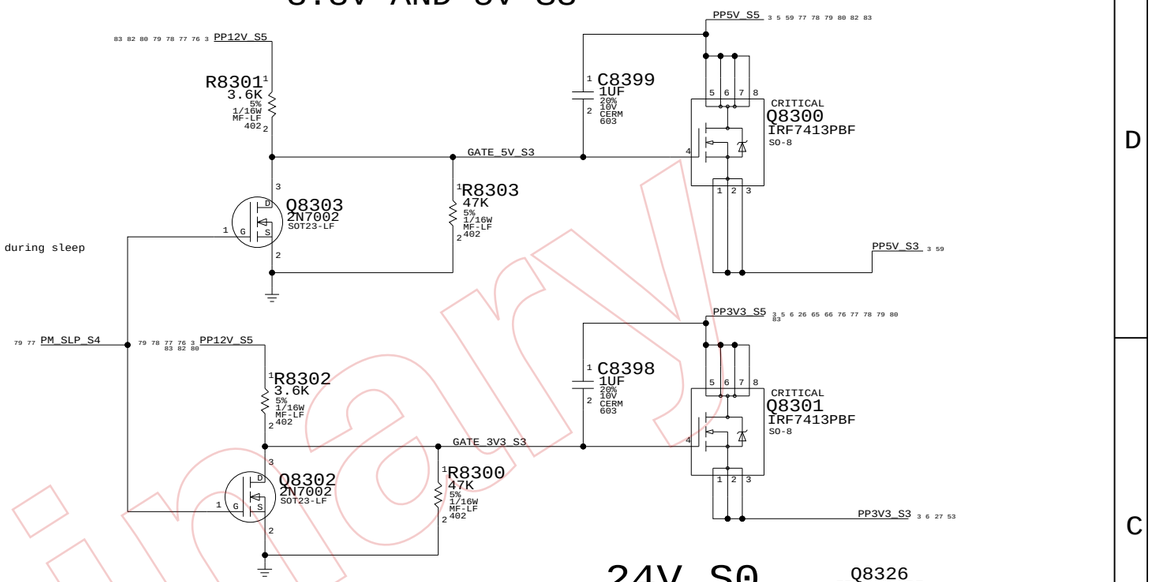
3.3V S0



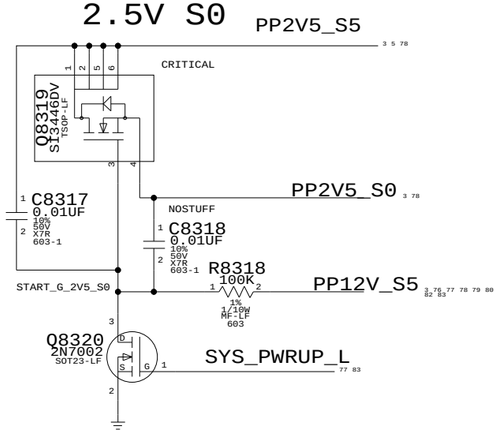
1.8V S0



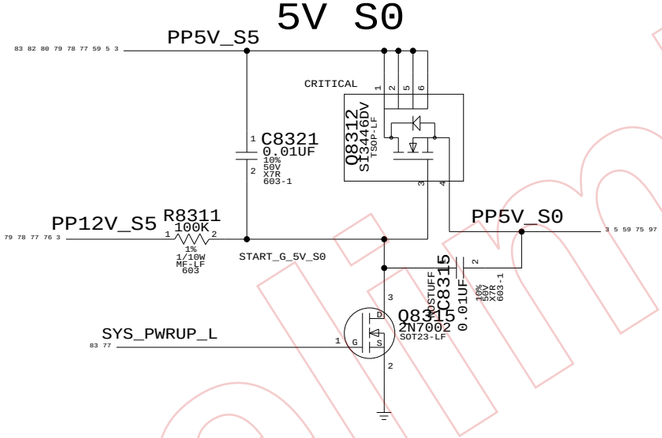
3.3V AND 5V S3



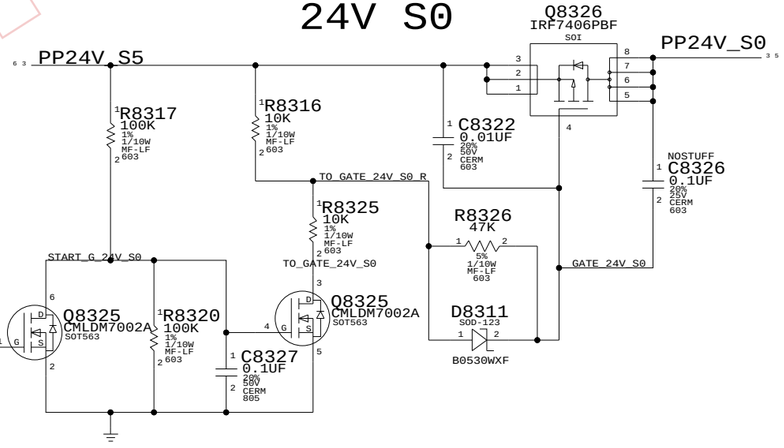
2.5V S0



5V S0

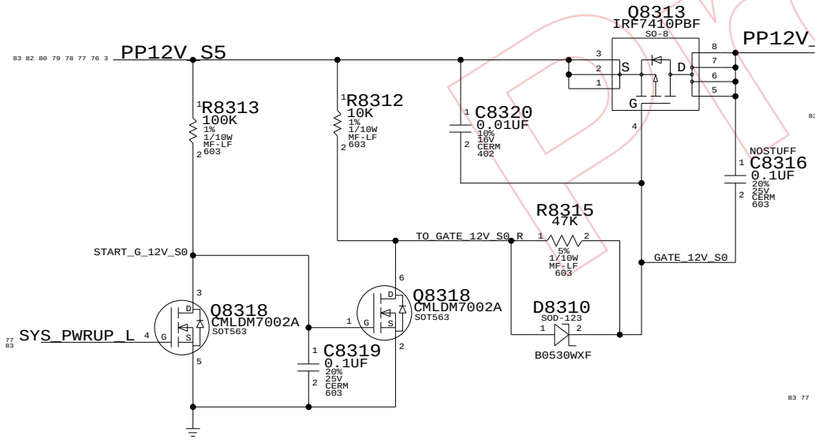


24V S0

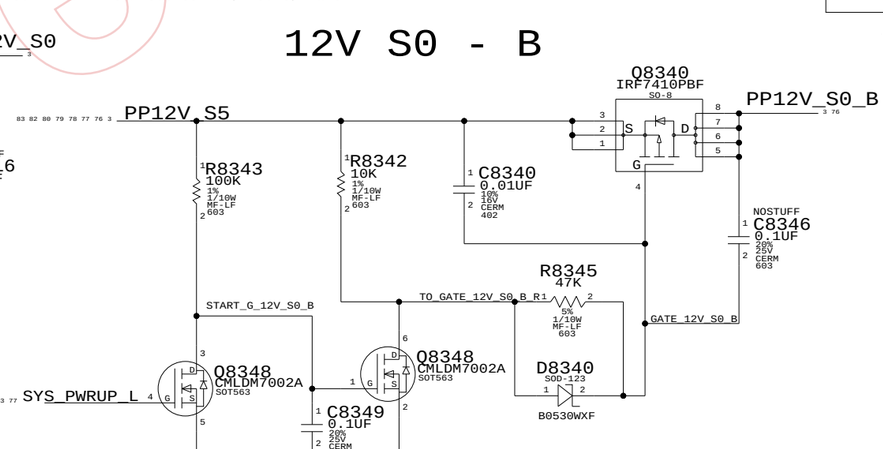


12V S0

Split 12V S0 is for better power plane structure
12VS0 - B will connect to MXM, Audio, Fans



12V S0 - B



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=05/19/2006

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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

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D	051-7039	17
SCALE: NONE	SHT 83 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

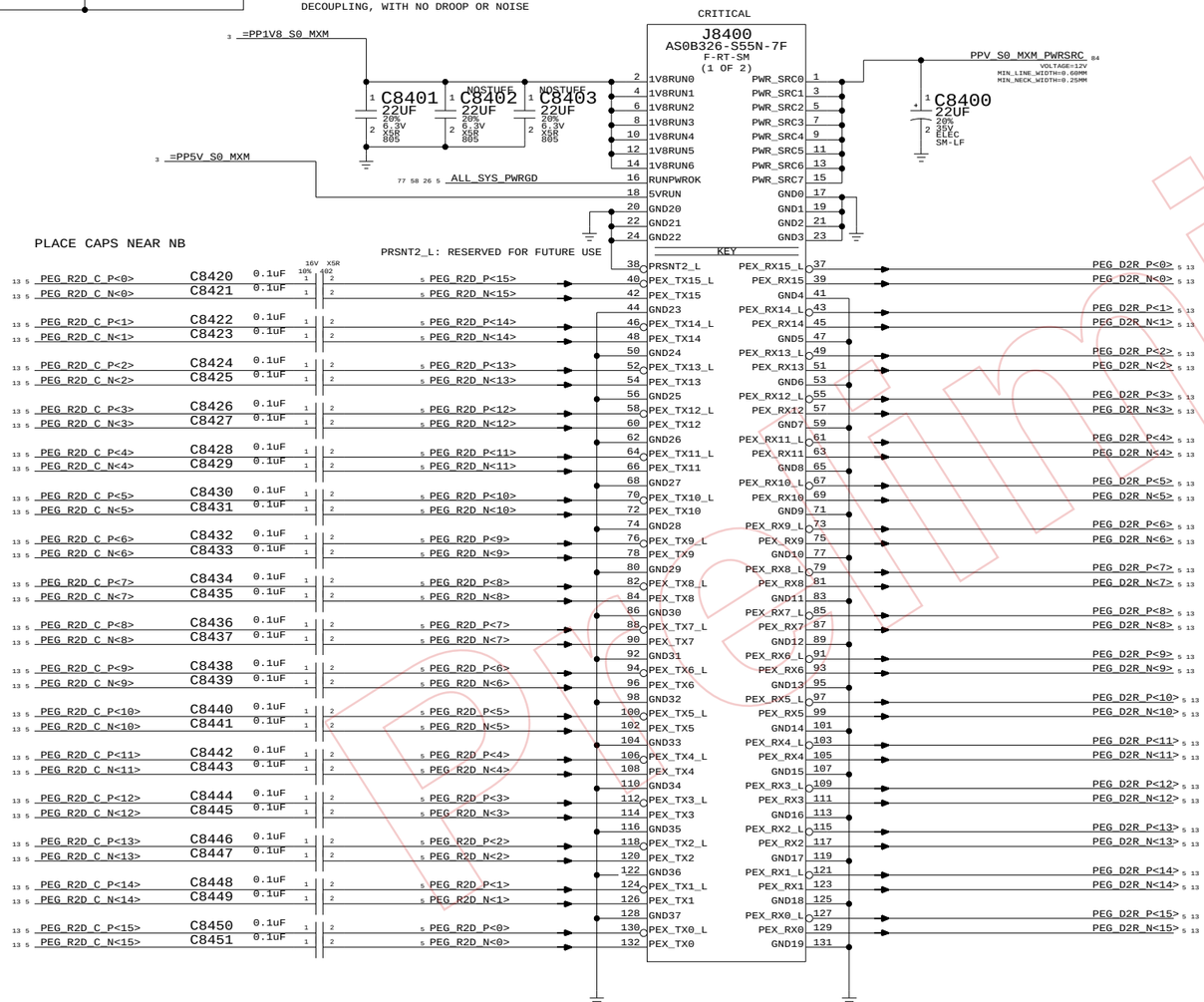
Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS

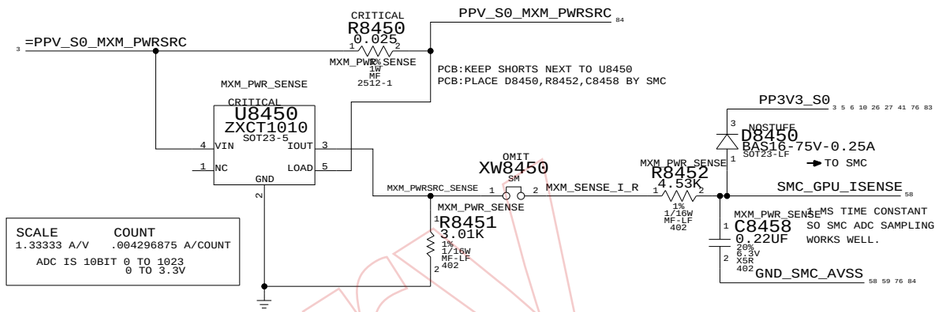
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

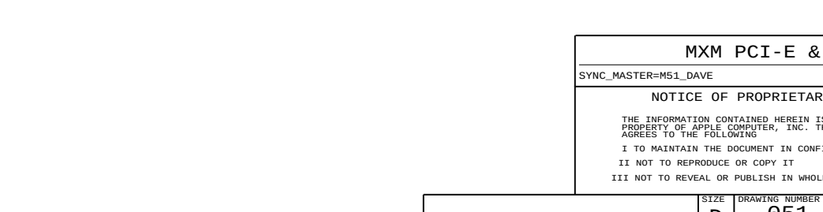


MXM PWRSRC (GPU CORE) CURRENT SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	PRODUCTION

MXM PWRSRC VOLTAGE SENSE (SCALING 12V INPUT VOLTAGE TO SMC)



MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7039	17

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)

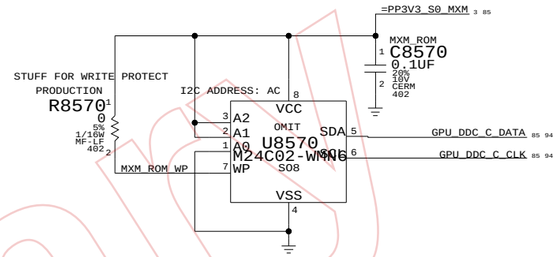
MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

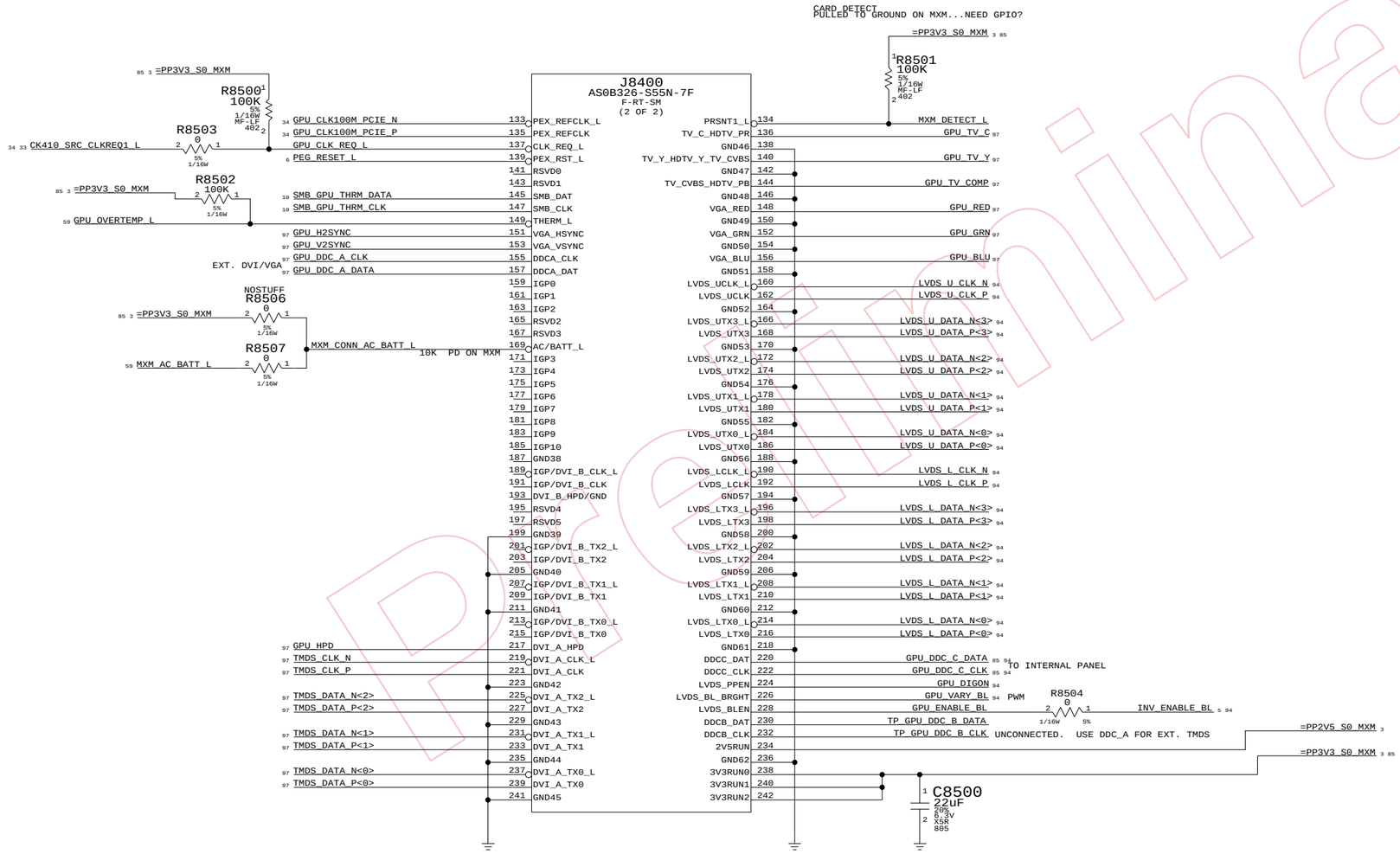
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



CARD DETECT
PULLED TO GROUND ON MXM...NEED GPIO?



MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

3 =PPV_S0_LCD

NOSTUFF R9490 0 5% 1/8W MF-LF 805

C9400 0.1UF 10% 50V X7R 603-1

PLACE NEAR J9402

R9400[1] 100K 5% 1/16W MF-LF 402

R9401 29.4K 1% 1/16W MF-LF 402

LCD_PWREN_DIV

LCD_PWREN_L_RC

TSOP-LF SI3443DV Q9400

PP12V_LCD_SW

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

L9400 FERR-250-OHM SM

VOLTAGE=12V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

PP12V_LCD_CONN 6 94

C9420 10UF 10% 16V CERM 1210

C9401 0.001uF 20% 50V CERM 402

R9499[1] 100K 5% 1/16W MF-LF 402

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

85 GPU_DIGON

R9470[1] 100K 5% 1/16W MF-LF 402

CRITICAL SDF9400 STDOFF-3MMOD4.6MMH-1.35-TH

CRITICAL J9402 53307-3072 F-ST-SM

85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0> 85
85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1> 85
85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2> 85
	7	8	LVDS_U_CLK_N 85
85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3> 85
85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0> 85
85 LVDS_L_DATA_P<0>	13	14	
85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1> 85
	17	18	LVDS_L_DATA_N<2> 85
85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N 85
85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3> 85
85 LVDS_L_DATA_P<3>	23	24	
85 GPU_DDC_C_CLK	25	26	GPU_DDC_C_DATA 85
	27	28	
	29	30	

94 =PP3V3_DDC_LCD

94 6 PP12V_LCD_CONN

PP12V_LCD_CONN 6 94

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9410 0.001uF 20% 50V CERM 402

CRITICAL SDF9401 STDOFF-3MMOD4.6MMH-1.35-TH

INVERTER INTERFACE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS

CRITICAL J9400 88290-14XG M-ST-SM

3 =PPV_S0_INVERTER

C9440 2.2UF 10% 50V X7R 1206

97 94 3 =PP3V3_S0_VIDEO

NOSTUFF R9440[1] 10K 5% 1/16W MF-LF 402

85 5 INV_ENABLE_BL

94 5 LCD_PWM

85 GPU_VARY_BL

NOSTUFF R9474[1] 10K 5% 1/16W MF-LF 402

R9475 47 5% 1/16W MF-LF 402

LCD_PWM 5 94

Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

TMDS_DATA_N<0> — R9700 0 (NOSTUFF) — L9700 90-OHM CRITICAL — TMDS_CONN_DN<0>
TMDS_DATA_P<0> — R9702 0 (NOSTUFF) — TMDS_CONN_DP<0>
TMDS_DATA_N<1> — R9703 0 (NOSTUFF) — L9701 90-OHM CRITICAL — TMDS_CONN_DN<1>
TMDS_DATA_P<1> — R9705 0 (NOSTUFF) — TMDS_CONN_DP<1>
TMDS_DATA_N<2> — R9704 0 (NOSTUFF) — L9702 90-OHM CRITICAL — TMDS_CONN_DN<2>
TMDS_DATA_P<2> — R9709 0 (NOSTUFF) — TMDS_CONN_DP<2>
TMDS_CLK_N — R9708 0 (NOSTUFF) — L9703 90-OHM CRITICAL — TMDS_CONN_CLKN
TMDS_CLK_P — R9715 0 (NOSTUFF) — TMDS_CONN_CLKP

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

PP5V_S0 — D9710 SOD-123 B0530WXF — PP5V_S0_DDC_DIODE — F9710 0.5AMP-13.2V CRITICAL SM-LF — PP5V_S0_DDC_FUSE — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC

J9710 MINI-DVI-M51 F-ST-SM CRITICAL

DVI_HPD_UF	25	1	TMDS_CONN_DP<2>
	17	9	
DVI_DDC_CLK_UF	26	2	TMDS_CONN_DN<2>
DVI_DDC_DATA_UF	18	10	
	27	3	TMDS_CONN_DP<1>
	19	11	
	28	4	TMDS_CONN_DN<1>
VGA_BLU	20	12	
VGA_HSYNC	29	5	TMDS_CONN_DP<0>
		13	
	30	6	TMDS_CONN_DN<0>
VGA_GRN	22	14	
VGA_VSYNC	31	7	TMDS_CONN_CLKP
		15	
	32	8	TMDS_CONN_CLKN
VGA_RED	24	16	

DVI_CHASSIS 33 — C9720 0.1UF 10% 16V X5R 402 — C9721 0.1UF 10% 16V X5R 402 — GND_CHASSIS_DVI

PLACE CLOSE TO MINI-DVI CONNECTOR
3V LEVEL SHIFTERS

=PP3V3_S0_VIDEO

DVI_DDC_CLK_UF — R9710 4.7K — R9712 4.7K — Q9711 2N7002DW-X-F SOT-363 — R9711 100 — DVI_DDC_CLK — C9711 100pF — GPU_DDC_A_CLK
DVI_DDC_DATA_UF — Q9711 2N7002DW-X-F SOT-363 — R9713 100 — DVI_DDC_DATA — C9713 100pF — GPU_DDC_A_DATA
DVI_HPD_UF — R9714 0 — GPU_HPD

R9720 10K, R9721 10K

C9710 0.01uF 20% 50V CERM 603
C9714 100pF 5% 50V CERM 402

NOSTUFF R9722 100K — NOSTUFF D9700 CASE425 MMSZ4681XXG

Note: this clamp is supposed to be on the MXM card

=PP3V3_S0_VIDEO

C9730 0.1UF 20% 10V CERM 402 — C9731 10uF 20% 6.3V CERM 805-1

U9730 SOP TS3V330 CRITICAL

VIDEO_MUX_RED	DA	S1A	GPU_TV_C
VIDEO_MUX_GRN	DB	S2A	GPU_RED
		S1B	GPU_TV_Y
		S2B	GPU_GRN
VIDEO_MUX_BLU	DC	S1C	GPU_TV_COMP
		S2C	GPU_BLU
NC	DD	S1D	NC
SB_CRT_TVOUT_MUX	IN	S2D	NC
	EN_L		
	VCC		
	GND		

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR

GPU_V2SYNC — U9760 74LC125 TSSOP — R9760 33 — GPU_VSYNC_BUF — VGA_VSYNC
GPU_H2SYNC — U9760 74LC125 TSSOP — R9761 33 — GPU_HSYNC_BUF — VGA_HSYNC

C9760 0.1UF 20% 10V CERM 402
C9762 22PF 5% 50V CERM 402 — C9763 22PF 5% 50V CERM 402

DISABLE UNUSED BUFFERS

U9760 74LC125 TSSOP (pins 9/8/10) — U9760 74LC125 TSSOP (pins 12/11/13)

=PP3V3_S0_VIDEO

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

	R	FL	C
VIDEO_MUX_BLU	R9740 150 1% 1/16W MF-LF 402	FL9740 LCFILTER CRITICAL SM-220MHZ-LF	C9740 3.3pF 0.25% 50V CERM 402
VIDEO_MUX_GRN	R9741 150 1% 1/16W MF-LF 402	FL9741 LCFILTER CRITICAL SM-220MHZ-LF	C9741 3.3pF 0.25% 50V CERM 402
VIDEO_MUX_RED	R9742 150 1% 1/16W MF-LF 402	FL9742 LCFILTER CRITICAL SM-220MHZ-LF	C9742 3.3pF 0.25% 50V CERM 402

CHECK MXM VENDOR RECOMMENDATIONS FOR FILTER

External Display Conns

SYNC_MASTER=M51_DAVE — SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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