1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SANTANA - M51 MLB

DVT -- 06/29/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
21		446951	ENGINEERING RELEASED	06/29/06	06/22/04

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7039	1	PCB,SCHEM,MLB,M51	SCH1		
820-1984	1	PCB,FAB,MLB,M51	MLB1		

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM SANTANA

DRAWING NUMBER 051-7039 REV. 21

SHT 1 OF 97

J0700
CPU
(1.83/2.17GHZ)
CORE (~1.2V)
PAGE 8
PAGE 7

J1101
ITP
CONN
PAGE 11

J9700
MINI-DVI
(TMDS - VGA)
PAGE 97

J9402
LVDS
(INTERNAL)
PAGE 94

64-BIT
FSB
667MHZ

PAGE 12

U1200
PCI-E
PAGE 13
NB- GM
CORE (1.05V)
PAGE 16-17
MAIN MEMORY
PAGE 15

DDR2 - DUAL CHAN
1.8V/667MHZ
64-BIT

J2800
J2900
DIMM
PAGE 28-29

PARALLEL
TERM
PAGES 30

6DUAL CHANNEL LVDS - 6BIT

J8400
MXM CONNECTOR
PAGES 84-85

MISC
PAGE 14
DMI
PAGE 14

4-BIT
DMI
1.2V/800MHZ
CONTROL = 2.5V

U3301
CK410
CLOCKS
PAGE 33
TERMS
PAGE 34

J2901 ALS+AMBIENT TSENS P. 59
TEMP SENSE
SEE I2C PG 27

POWER SENSE
SEE POWER BLOCK DIAGRAM
PG 3

J6500,J6501,J6600 FAN CONNS

U6300/01
SPI
BOOTROM
PAGE 63

SMB
GPIO ADC FAN
SMC
U5800
PAGE 58

U6700
TPM
PAGE 67

J6000
LPC+ CONN
PAGE 60

JC900
SATA
CONNECTOR
HARD DRIVE
PAGE 38

1.2V/1.5GHZ

SATA
PAGE 21
SATA2
SATA0

DMI
PAGE 22
SPI
PAGE 22
LPC
PAGE 21

4-BIT (3.3V/33MHZ)

JE310/JE320/JE330
USB
CONNECTORS
0 2 4
PAGE 47

JE350
CAMERA
PAGE 47
3
CAMERA

JE351
IR RCV
PAGE 47
7
IR

J4700
BT
CONN
PAGE 48

JC901
UATA
CONNECTOR
OPTICAL
PAGE 38

UATA/133
3.3V/133MHZ

U2100
SB
CORE (1.05V)

UATA
PAGE 21

0,2,4
1
3,7
5
6

J5300 (AIRPORT CONN)

USB
PAGE 22

PCI-E
PAGE 22
PORT 1
PORT 2
PORT 3
PORT 4

CORE
PAGE 24
GPIOS
PAGE 23
AZALIA
PCI
PAGE 22
PAGE 21

SMB
PAGE 27

J2800
J2900
DIMM'S

U3301
CK410M

J5300
AIRPORT

X1 - 1.5GHZ
X1 - 1.5GHZ

33MHZ
32-BIT

TSB82AA2
FIREWIRE B
PAGE 44

J5300
MINI-PCIE
AIRPORT
PAGE 53

U4101
YUKON
GIG ETHERNET
PAGE 41

4 Diff pairs

JD600
ETHERNET
CONNECTOR
PAGE 43

100MHZ
8-BIT

TSB81BA3
FIREWIRE B
PAGE 45
0 1 2

2 Diff pairs

JE600, JE601
FIREWIRE B
CONNECTORS
PAGE 46

U6800
AUDIO CODEC
STA9221
PAGE 68
PORT A
PORT C
PORT F
PORT B

S/PDIF

OPTICAL OUT
J7303
COMBO OUT
CONNECTOR
PAGE 73
LINE OUT

SPEAKER
AMP
PAGE 72

J7301,J7302
R/L
SPEAKER
CONNECTORS
PAGE 73

OPTICAL IN
J7303
COMBO IN
CONNECTOR
PAGE 73
LINE IN

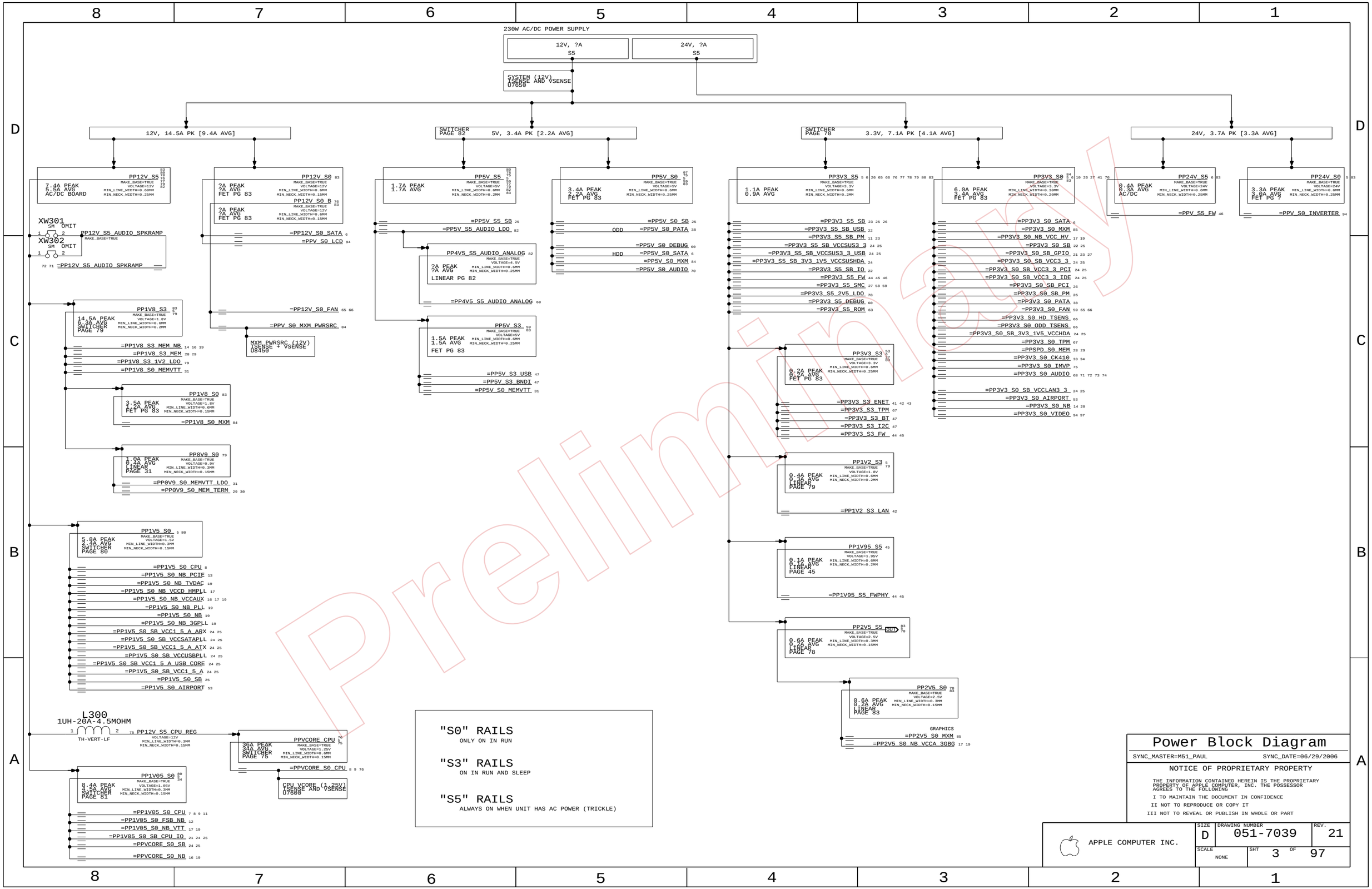
JE350
MIC IN
BNDI
INTERFACE

System Block Diagram

SYNC_MASTER=M51_PAUL
SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 2 OF 97	


230W AC/DC POWER SUPPLY
12V, ?A
S5
24V, ?A
S5
SYSTEM (12V)
ISENSE AND VSENSE
U7650
12V, 14.5A PK [9.4A AVG]
SWITCHER
PAGE 82
5V, 3.4A PK [2.2A AVG]
SWITCHER
PAGE 78
3.3V, 7.1A PK [4.1A AVG]
24V, 3.7A PK [3.3A AVG]
PP12V_S5
7.4A PEAK
5.5A AVG
AC/DC BOARD
PP12V_S0
2A PEAK
2A AVG
FET PG 83
PP12V_S0_B
2A PEAK
2A AVG
FET PG 83
PP5V_S5
1.7A PEAK
1.7A AVG
PP5V_S0
3.4A PEAK
2.2A AVG
FET PG 83
PP3V3_S5
1.1A PEAK
0.9A AVG
PP3V3_S0
6.0A PEAK
3.4A AVG
FET PG 83
PP24V_S5
0.4A PEAK
0.3A AVG
AC/DC
PP24V_S0
3.3A PEAK
3.0A AVG
FET PG ?
XW301
SM OMIT
XW302
SM OMIT
PP12V_S5_AUDIO_SPKRAMP
=PP12V_S5_AUDIO_SPKRAMP
=PP12V_S0_SATA
=PPV_S0_LCD
=PP12V_S0_FAN
=PPV_S0_MXM_PWRSRC
MXM PWRSRC (12V)
ISENSE + VSENSE
U8450
=PP5V_S5_SB
=PP5V_S5_AUDIO_LDO
PP4V5_S5_AUDIO_ANALOG
2A PEAK
2A AVG
LINEAR PG 82
=PP4V5_S5_AUDIO_ANALOG
PP5V_S3
1.5A PEAK
1.5A AVG
FET PG 83
=PP5V_S5_USB
=PP5V_S3_BNDI
=PP5V_S0_MEMVTT
=PP5V_S0_SB
=PP5V_S0_PATA
=PP5V_S0_DEBUG
=PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_AUDIO
=PP3V3_S5_SB
=PP3V3_S5_SB_USB
=PP3V3_S5_SB_PM
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
=PP3V3_S5_SB_IO
=PP3V3_S5_FW
=PP3V3_S5_SMC
=PP3V3_S5_2V5_LDO
=PP3V3_S5_DEBUG
=PP3V3_S5_ROM
=PP3V3_S0_SATA
=PP3V3_S0_MXM
=PP3V3_S0_NB_VCC_HV
=PP3V3_S0_SB
=PP3V3_S0_SB_GPIO
=PP3V3_S0_SB_VCC3_3
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_PCI
=PP3V3_S0_SB_PM
=PP3V3_S0_PATA
=PP3V3_S0_FAN
=PP3V3_S0_HD_TSENS
=PP3V3_S0_ODD_TSENS
=PP3V3_S0_SB_3V3_1V5_VCCHDA
=PP3V3_S0_TPM
=PPSPD_S0_MEM
=PP3V3_S0_CK410
=PP3V3_S0_IMVP
=PP3V3_S0_AUDIO
=PP3V3_S0_SB_VCCLAN3_3
=PP3V3_S0_AIRPORT
=PP3V3_S0_NB
=PP3V3_S0_VIDEO
=PPV_S5_FW
=PPV_S0_INVERTER
PP3V3_S3
0.2A PEAK
0.2A AVG
FET PG 83
=PP3V3_S3_ENET
=PP3V3_S3_TPM
=PP3V3_S3_BT
=PP3V3_S3_I2C
=PP3V3_S3_FW
PP1V2_S3
0.4A PEAK
0.3A AVG
LINEAR
PAGE 79
=PP1V2_S3_LAN
PP1V95_S5
0.1A PEAK
0.1A AVG
LINEAR
PAGE 45
=PP1V95_S5_FWPHY
PP2V5_S5
0.6A PEAK
0.2A AVG
LINEAR
PAGE 78
PP2V5_S0
0.6A PEAK
0.2A AVG
LINEAR
PAGE 83
=PP2V5_S0_NB_VCCA_3GBG
GRAPHICS
=PP2V5_S0_MXM
PP1V8_S3
14.5A PEAK
8.3A AVG
SWITCHER
PAGE 79
=PP1V8_S3_MEM_NB
=PP1V8_S3_MEM
=PP1V8_S3_1V2_LDO
=PP1V8_S0_MEMVTT
PP1V8_S0
3.5A PEAK
1.2A AVG
FET PG 83
=PP1V8_S0_MXM
PP0V9_S0
1.0A PEAK
0.4A AVG
LINEAR
PAGE 31
=PP0V9_S0_MEMVTT_LDO
=PP0V9_S0_MEM_TERM
PP1V5_S0
5.8A PEAK
2.4A AVG
SWITCHER
PAGE 80
=PP1V5_S0_CPU
=PP1V5_S0_NB_PCIE
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_NB_VCCD_HMPLL
=PP1V5_S0_NB_VCCAUX
=PP1V5_S0_NB_PLL
=PP1V5_S0_NB
=PP1V5_S0_NB_3GPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCCSATAPLL
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCCUSBPLL
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB
=PP1V5_S0_AIRPORT
L300
1UH-20A-4.5MOHM
TH-VERT-LF
PP12V_S5_CPU_REG
PPVCORE_CPU
38A PEAK
34A AVG
SWITCHER
PAGE 75
=PPVCORE_S0_CPU
CPU VCORE (1.25V)
ISENSE AND VSENSE
U7600
PP1V05_S0
8.4A PEAK
4.5A AVG
SWITCHER
PAGE 81
=PP1V05_S0_CPU
=PP1V05_S0_FSB_NB
=PP1V05_S0_NB_VTT
=PP1V05_S0_SB_CPU_IO
=PPVCORE_S0_SB
=PPVCORE_S0_NB
"S0" RAILS
ONLY ON IN RUN
"S3" RAILS
ON IN RUN AND SLEEP
"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)
Power Block Diagram
SYNC_MASTER=M51_PAUL
SYNC_DATE=06/29/2006
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-7039
REV.
21
SCALE
NONE
SHT
3
OF
97

Production BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7512	PCBA,MLB,2.33GHz,M51	M51_COMMON,M51_BEST,EEE_V4K
630-7595	PCBA,MLB,2.16GHz,M51	M51_COMMON,M51_BETTER,EEE_VMD,PRODUCTION

Development BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
603-8960	PCBA,DEVBOM,M51	M51_DEVELOPMENT

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M51_COMMON	COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE
M51_COMMON1	CPU_TSENS_EXT,GPU_TSENS_INT,GPU_TSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE
M51_COMMON2	SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSENS,CPU_PWR_SENSE,MXM_PWR_SENSE
M51_DEVELOPMENT	DEVELOPMENT,M51_DEV1
M51_DEV1	CPU_TSENS_INT,SYS_PWR_SENSE

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

BarCode Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:VMD]	CRITICAL	EEE_VMD
825-6447	1	BAR CODE LABLE, MLB, M51	[EEE:V4K]	CRITICAL	EEE_V4K

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE,SCREENED	U7500	CRITICAL	
341S1892	1	IC,2K I2C EEPROM,MXM,M51	U8570	CRITICAL	MXM_ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
(335S0384) 341T0019	1	IC,EFI BOOT ROM,M51	U6301	CRITICAL	
(338S0274) 341T0020	1	IC,SMC,M51	U5800	CRITICAL	
337S3292	1	MEROM 2.3GHZ, M51	CPU	CRITICAL	M51_BEST
337S3293	1	MEROM 2.16GHZ, M51	CPU	CRITICAL	M51_BETTER

Misc. Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	NOSTUFF
820-2038	1	IO ALIGNMENT BOARD, M51	PCB2	CRITICAL	
946-0743	1	IO ALIGNMENT BOARD ADHESIVE	ADH1	CRITICAL	

BATTERY IS INSTALLED AT FATP

FOR DVT, TRYING AN EVEN BRIGHTER LED ON 2.16GHZ CONFIG

378S0199	1	LED,WHITE,DUAL,2500MCD,SMD	LED5950	CRITICAL	M51_BETTER
378S0193	1	LED,WHITE,740MCD,LF,3X2MM	LED5950	CRITICAL	M51_BEST

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		ALL	Sanyo alt for Nich.
126S0099	126S0073		ALL	Sanyo alt for Nich.
126S0068	126S0088		ALL	Sanyo alt for Nich.
124-0361	124-0339		ALL	SANYO ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0141	378S0140		ALL	GREEN LED ALT.
359S0117	359S0101		U3301	SILEGO CK410 CLOCK
353S1461	353S1465		U7500	CPU VREG NEW REV
740S0044	740S0028		F9710	DVI DDC (LITTLEFUSE)
516S0511	516S0460		J8400	MXM CONN SPEEDTECH

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS_PWR_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
102S0699	1	RES,0-OHM,2010	R7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION
116S0090	1	RES,10K-OHM,5%,0402	C7650	PRODUCTION

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
107S0070	1	RES,0-OHM,2512	R8450	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C8458	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C8459	NOSTUFF

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU_PWR_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K-OHM,5%,0402	C7602	NOSTUFF
116S0090	1	RES,10K-OHM,5%,0402	C7612	NOSTUFF

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

BOM Config

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7039 | REV. 21

SCALE NONE | SHT 4 OF 97

LAYOUT: PLACE CLOSE TO DESTINATION
* OPPOSITE END FROM CLOCK BUFFER

34 21 SB_CLK100M_SATA_P PP6C4 PP OMIT P4MM
34 21 SB_CLK100M_SATA_N PP6C5 PP OMIT P4MM

34 23 SB_CLK14P3M_TIMER PP6D9 PP OMIT P4MM
34 23 SB_CLK48M_USBCTLR PP6E0 PP OMIT P4MM

34 22 PCI_CLK_SB PP6D0 PP OMIT P4MM
44 34 PCI_CLK_FW PP626 PP OMIT P4MM
58 34 PCI_CLK_SMC PP627 PP OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE_PDIOR_L PP6C6 PP OMIT P4MM
38 21 IDE_PDIORDY PP6C7 PP OMIT P4MM
38 21 IDE_PDD<9> PP6C8 PP OMIT P4MM

54 22 PCIE_B_D2R_P PP600 PP OMIT P4MM
54 22 PCIE_B_D2R_N PP601 PP OMIT P4MM
22 14 DMI_N2S_P<0> PP6D3 PP OMIT P4MM
22 14 DMI_N2S_N<0> PP6D4 PP OMIT P4MM

67 60 58 21 5 LPC_FRAME_L PP6D8 PP OMIT P4MM

63 58 22 SPI_SO PP612 PP OMIT P4MM
63 58 22 SPI_SI PP613 PP OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS_SB_SCL PP604 PP OMIT P4MM
27 SMBUS_SB_SDA PP605 PP OMIT P4MM

27 SMBUS_SMC_A_S3_SCL PP610 PP OMIT P4MM
27 SMBUS_SMC_A_S3_SDA PP611 PP OMIT P4MM

FSB SIGNALS

12 11 7 FSB_CPURST_L PP621 PP OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR_PWRGOOD_DELAY PP665 PP OMIT P4MM
14 NB_RST_IN_L_R PP666 PP OMIT P4MM

22 14 DMI_S2N_N<0> PP673 PP OMIT P4MM
22 14 DMI_S2N_P<0> PP674 PP OMIT P4MM

19 14 MEM_VREF_NB_0 PP6E1 PP OMIT P4MM
19 14 MEM_VREF_NB_1 PP675 PP OMIT P4MM

I473
14 NB_CFG<17> — NC_NB_CFG<17> MAKE_BASE=TRUE
I474
14 NB_CFG<15> — NC_NB_CFG<15> MAKE_BASE=TRUE
I475
14 NB_CFG<14> — NC_NB_CFG<14> MAKE_BASE=TRUE
I476
14 NB_CFG<13> — NC_NB_CFG<13> MAKE_BASE=TRUE
I477
14 NB_CFG<12> — NC_NB_CFG<12> MAKE_BASE=TRUE
I478
14 NB_CFG<11> — NC_NB_CFG<11> MAKE_BASE=TRUE
I479
14 NB_CFG<10> — NC_NB_CFG<10> MAKE_BASE=TRUE
I481
14 NB_CFG<8> — NC_NB_CFG<8> MAKE_BASE=TRUE
I480
14 NB_CFG<6> — NC_NB_CFG<6> MAKE_BASE=TRUE
I482
14 NB_CFG<4> — NC_NB_CFG<4> MAKE_BASE=TRUE
I483
14 NB_CFG<3> — NC_NB_CFG<3> MAKE_BASE=TRUE

I513
22 PCI_GNT3_L — TP_PCI_GNT3_L MAKE_BASE=TRUE

SPARE USB PORT
22 USB_F_N — TP_USB_F_N MAKE_BASE=TRUE
22 USB_F_P — TP_USB_F_P MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL
19 13 LVDS_BKLTEN — TP_LVDS_BKLTEN MAKE_BASE=TRUE

68 IN NC_AUD_BI_PORT_G_L NO_TEST=TRUE
59 IN NC_ALS_GAIN NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_C NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_D NO_TEST=TRUE
59 IN NC_SMC_BATT_CHG_EN NO_TEST=TRUE
59 IN NC_SMC_BATT_ISET NO_TEST=TRUE
59 IN NC_SMC_BATT_TRICKLE_EN_L NO_TEST=TRUE
59 IN NC_SMC_BATT_VSET NO_TEST=TRUE
59 IN NC_SMC_P20 NO_TEST=TRUE
59 IN NC_SMC_P21 NO_TEST=TRUE
59 IN NC_SMC_P22 NO_TEST=TRUE
59 IN NC_SMC_P23 NO_TEST=TRUE
59 IN NC_SMC_P26 NO_TEST=TRUE
59 IN NC_SMC_P27 NO_TEST=TRUE
59 IN NC_SMC_SYS_ISET NO_TEST=TRUE
59 IN NC_SMC_SYS_VSET NO_TEST=TRUE
59 IN NC_SMS_X_AXIS NO_TEST=TRUE
59 IN NC_SMS_Y_AXIS NO_TEST=TRUE
59 IN NC_SMS_Z_AXIS NO_TEST=TRUE

73 IN NC_J7302_3 NO_TEST=TRUE
73 IN NC_J7302_6 NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_E_R NO_TEST=TRUE
59 IN NC_SMC_MEM_ISENSE NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_L NO_TEST=TRUE
68 IN NC_AUD_BI_PORT_H_R NO_TEST=TRUE
68 IN NC_AUD_VREF_PORT_B NO_TEST=TRUE

29 IN TP_MEM_B_A<15> NO_TEST=TRUE
29 IN TP_MEM_B_A<14> NO_TEST=TRUE

84 13 IN PEG_R2D_C_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_C_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_C_P<15> NO_TEST=TRUE

84 13 IN PEG_R2D_N<0> NO_TEST=TRUE
84 13 IN PEG_R2D_P<0> NO_TEST=TRUE
84 13 IN PEG_R2D_N<1> NO_TEST=TRUE
84 13 IN PEG_R2D_P<1> NO_TEST=TRUE
84 13 IN PEG_R2D_N<2> NO_TEST=TRUE
84 13 IN PEG_R2D_P<2> NO_TEST=TRUE
84 13 IN PEG_R2D_N<3> NO_TEST=TRUE
84 13 IN PEG_R2D_P<3> NO_TEST=TRUE
84 13 IN PEG_R2D_N<4> NO_TEST=TRUE
84 13 IN PEG_R2D_P<4> NO_TEST=TRUE
84 13 IN PEG_R2D_N<5> NO_TEST=TRUE
84 13 IN PEG_R2D_P<5> NO_TEST=TRUE
84 13 IN PEG_R2D_N<6> NO_TEST=TRUE
84 13 IN PEG_R2D_P<6> NO_TEST=TRUE
84 13 IN PEG_R2D_N<7> NO_TEST=TRUE
84 13 IN PEG_R2D_P<7> NO_TEST=TRUE
84 13 IN PEG_R2D_N<8> NO_TEST=TRUE
84 13 IN PEG_R2D_P<8> NO_TEST=TRUE
84 13 IN PEG_R2D_N<9> NO_TEST=TRUE
84 13 IN PEG_R2D_P<9> NO_TEST=TRUE
84 13 IN PEG_R2D_N<10> NO_TEST=TRUE
84 13 IN PEG_R2D_P<10> NO_TEST=TRUE
84 13 IN PEG_R2D_N<11> NO_TEST=TRUE
84 13 IN PEG_R2D_P<11> NO_TEST=TRUE
84 13 IN PEG_R2D_N<12> NO_TEST=TRUE
84 13 IN PEG_R2D_P<12> NO_TEST=TRUE
84 13 IN PEG_R2D_N<13> NO_TEST=TRUE
84 13 IN PEG_R2D_P<13> NO_TEST=TRUE
84 13 IN PEG_R2D_N<14> NO_TEST=TRUE
84 13 IN PEG_R2D_P<14> NO_TEST=TRUE
84 13 IN PEG_R2D_N<15> NO_TEST=TRUE
84 13 IN PEG_R2D_P<15> NO_TEST=TRUE

84 13 IN PEG_D2R_N<0> NO_TEST=TRUE
84 13 IN PEG_D2R_P<0> NO_TEST=TRUE
84 13 IN PEG_D2R_N<1> NO_TEST=TRUE
84 13 IN PEG_D2R_P<1> NO_TEST=TRUE
84 13 IN PEG_D2R_N<2> NO_TEST=TRUE
84 13 IN PEG_D2R_P<2> NO_TEST=TRUE
84 13 IN PEG_D2R_N<3> NO_TEST=TRUE
84 13 IN PEG_D2R_P<3> NO_TEST=TRUE
84 13 IN PEG_D2R_N<4> NO_TEST=TRUE
84 13 IN PEG_D2R_P<4> NO_TEST=TRUE
84 13 IN PEG_D2R_N<5> NO_TEST=TRUE
84 13 IN PEG_D2R_P<5> NO_TEST=TRUE
84 13 IN PEG_D2R_N<6> NO_TEST=TRUE
84 13 IN PEG_D2R_P<6> NO_TEST=TRUE
84 13 IN PEG_D2R_N<7> NO_TEST=TRUE
84 13 IN PEG_D2R_P<7> NO_TEST=TRUE
84 13 IN PEG_D2R_N<8> NO_TEST=TRUE
84 13 IN PEG_D2R_P<8> NO_TEST=TRUE
84 13 IN PEG_D2R_N<9> NO_TEST=TRUE
84 13 IN PEG_D2R_P<9> NO_TEST=TRUE
84 13 IN PEG_D2R_N<10> NO_TEST=TRUE
84 13 IN PEG_D2R_P<10> NO_TEST=TRUE
84 13 IN PEG_D2R_N<11> NO_TEST=TRUE
84 13 IN PEG_D2R_P<11> NO_TEST=TRUE
84 13 IN PEG_D2R_N<12> NO_TEST=TRUE
84 13 IN PEG_D2R_P<12> NO_TEST=TRUE
84 13 IN PEG_D2R_N<13> NO_TEST=TRUE
84 13 IN PEG_D2R_P<13> NO_TEST=TRUE
84 13 IN PEG_D2R_N<14> NO_TEST=TRUE
84 13 IN PEG_D2R_P<14> NO_TEST=TRUE
84 13 IN PEG_D2R_N<15> NO_TEST=TRUE
84 13 IN PEG_D2R_P<15> NO_TEST=TRUE

76 75 3 IN PPVCORE_CPU FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 IN PP3V3_S5 FUNC_TEST=TRUE
83 IN PP2V5_S5 FUNC_TEST=TRUE
83 78 3 IN PP1V8_S3 FUNC_TEST=TRUE
83 79 3 IN PP1V2_S3 FUNC_TEST=TRUE
79 3 IN PP1V5_S0 FUNC_TEST=TRUE
80 3 IN PP1V05_S0 FUNC_TEST=TRUE
80 34 3 IN PP5V_S5 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP5V_S0 FUNC_TEST=TRUE
97 83 75 59 3 IN PP5V_S5 FUNC_TEST=TRUE
83 82 80 79 78 77 75 59 5 3 IN PP3V3_S5 FUNC_TEST=TRUE
80 79 78 77 76 66 65 26 6 5 3 IN PP3V3_S0 FUNC_TEST=TRUE
63 IN PP24V_S0 FUNC_TEST=TRUE
84 83 76 41 27 26 10 6 3 IN
83 3 IN

11 7 IN XDP_BPM_L<3> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<2> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<1> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<0> FUNC_TEST=TRUE
26 11 7 IN XDP_DBRESET_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<0> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<1> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<2> FUNC_TEST=TRUE
67 60 58 21 IN LPC_AD<3> FUNC_TEST=TRUE
67 60 58 21 5 IN LPC_FRAME_L FUNC_TEST=TRUE
67 60 58 23 IN PM_CLKRUN_L FUNC_TEST=TRUE
60 58 22 IN BOOT_LPC_SPI_L FUNC_TEST=TRUE
60 6 IN DEBUG_RST_L FUNC_TEST=TRUE
60 59 21 IN FWH_INIT_L FUNC_TEST=TRUE
60 34 IN PCI_CLK_PORT80 FUNC_TEST=TRUE
67 60 58 23 IN INT_SERIRQ FUNC_TEST=TRUE
67 60 58 23 IN PM_SUS_STAT_L FUNC_TEST=TRUE
60 58 IN SMC_MD1 FUNC_TEST=TRUE
60 59 58 IN SMC_RST_L FUNC_TEST=TRUE
60 58 IN SMC_NMI FUNC_TEST=TRUE
60 23 IN SV_SET_UP FUNC_TEST=TRUE
76 58 IN ISENSE_CAL_EN FUNC_TEST=TRUE
94 85 IN INV_ENABLE_BL FUNC_TEST=TRUE
94 IN LCD_PWM FUNC_TEST=TRUE
75 8 IN CPU_VID<0> FUNC_TEST=TRUE
75 8 IN CPU_VID<1> FUNC_TEST=TRUE
75 8 IN CPU_VID<2> FUNC_TEST=TRUE
75 8 IN CPU_VID<3> FUNC_TEST=TRUE
75 8 IN CPU_VID<4> FUNC_TEST=TRUE
75 8 IN CPU_VID<5> FUNC_TEST=TRUE
75 8 IN CPU_VID<6> FUNC_TEST=TRUE
75 23 14 IN PM_DPRSLPVR FUNC_TEST=TRUE
75 21 7 IN CPU_DPRSTP_L FUNC_TEST=TRUE
75 26 14 5 IN VR_PWRGOOD_DELAY FUNC_TEST=TRUE
26 23 IN VR_PWRGD_CK410 FUNC_TEST=TRUE
84 77 58 26 IN ALL_SYS_PWRGD FUNC_TEST=TRUE
77 58 23 IN PM_SLP_S4_L FUNC_TEST=TRUE
80 79 77 58 23 IN PM_SLP_S3_L FUNC_TEST=TRUE

60 59 58 IN SMC_TCK FUNC_TEST=TRUE
60 59 58 IN SMC_TDI FUNC_TEST=TRUE
60 59 58 IN SMC_TDO FUNC_TEST=TRUE
60 59 58 IN SMC_TMS FUNC_TEST=TRUE
60 58 IN SMC_TRST_L FUNC_TEST=TRUE
60 59 58 IN SMC_TX_L FUNC_TEST=TRUE
60 59 58 IN SMC_RX_L FUNC_TEST=TRUE
59 IN SMC_MANUAL_RST_L FUNC_TEST=TRUE
11 7 IN XDP_TCK FUNC_TEST=TRUE
11 7 IN XDP_TDI FUNC_TEST=TRUE
11 7 IN XDP_TDO FUNC_TEST=TRUE
11 7 IN XDP_TMS FUNC_TEST=TRUE
11 7 IN XDP_TRST_L FUNC_TEST=TRUE
59 5 IN POWER_BUTTON_L FUNC_TEST=TRUE
26 5 IN SW_RST_BTN_L FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXP FUNC_TEST=TRUE
10 IN NB_TSENS_HS_DXN FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_N FUNC_TEST=TRUE
34 11 IN CPU_XDP_CLK_P FUNC_TEST=TRUE
11 IN ITPRESET_L FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<5> FUNC_TEST=TRUE
11 7 IN XDP_BPM_L<4> FUNC_TEST=TRUE

MISC GROUND VIAS

ZH500 HOLE-VIA 1 1
ZH510 HOLE-VIA 1 1
ZH520 HOLE-VIA 1 1
ZH501 HOLE-VIA 1 1
ZH511 HOLE-VIA 1 1
ZH521 HOLE-VIA 1 1
ZH502 HOLE-VIA 1 1
ZH512 HOLE-VIA 1 1
ZH522 HOLE-VIA 1 1
ZH503 HOLE-VIA 1 1
ZH513 HOLE-VIA 1 1
ZH523 HOLE-VIA 1 1
ZH504 HOLE-VIA 1 1
ZH514 HOLE-VIA 1 1
ZH524 HOLE-VIA 1 1
ZH505 HOLE-VIA 1 1
ZH515 HOLE-VIA 1 1
ZH525 HOLE-VIA 1 1
ZH506 HOLE-VIA 1 1
ZH516 HOLE-VIA 1 1
ZH526 HOLE-VIA 1 1
ZH507 HOLE-VIA 1 1
ZH517 HOLE-VIA 1 1
ZH527 HOLE-VIA 1 1
ZH508 HOLE-VIA 1 1
ZH518 HOLE-VIA 1 1
ZH528 HOLE-VIA 1 1
ZH509 HOLE-VIA 1 1
ZH519 HOLE-VIA 1 1
ZH529 HOLE-VIA 1 1

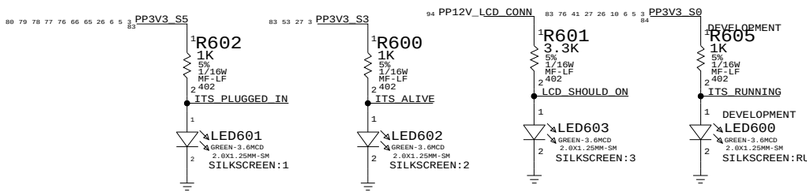
FUNC TEST 1 OF 2

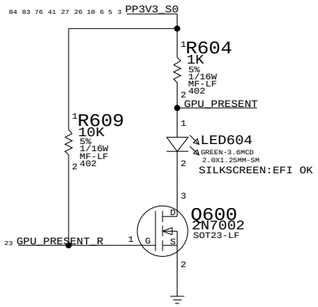
SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

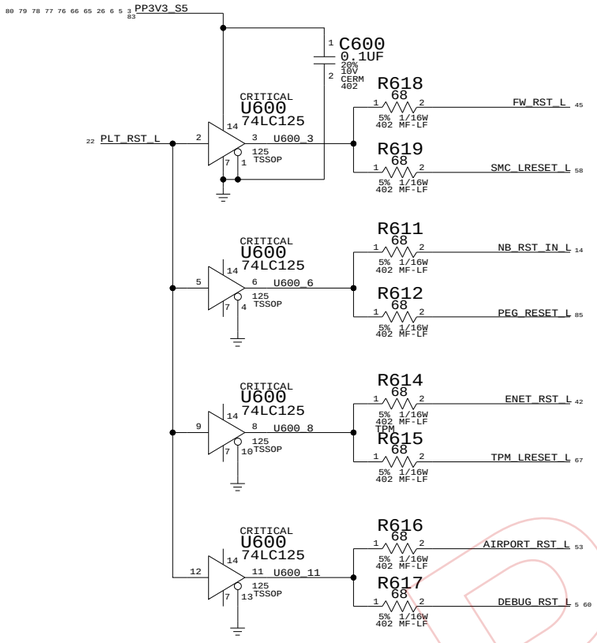
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 5 OF 97	

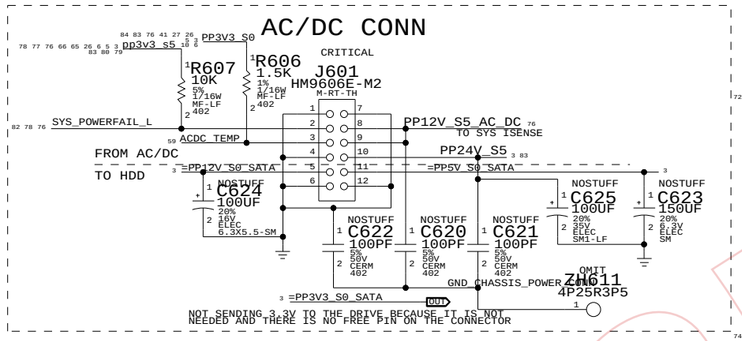
SYSTEM STATUS



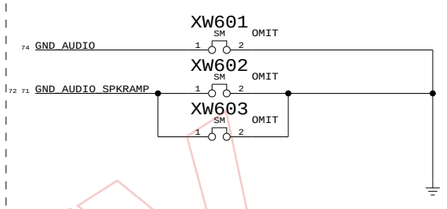




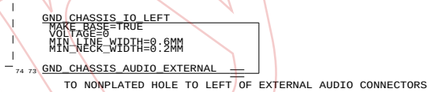
AC/DC CONN

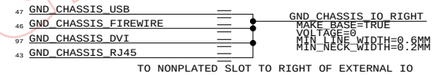


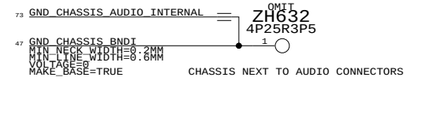
GND RAILS

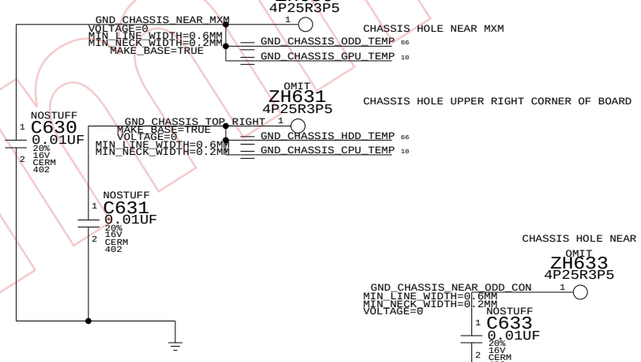


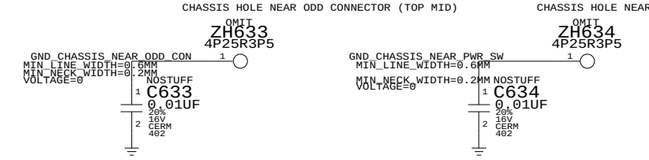
CHASSIS GND





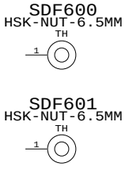






HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU

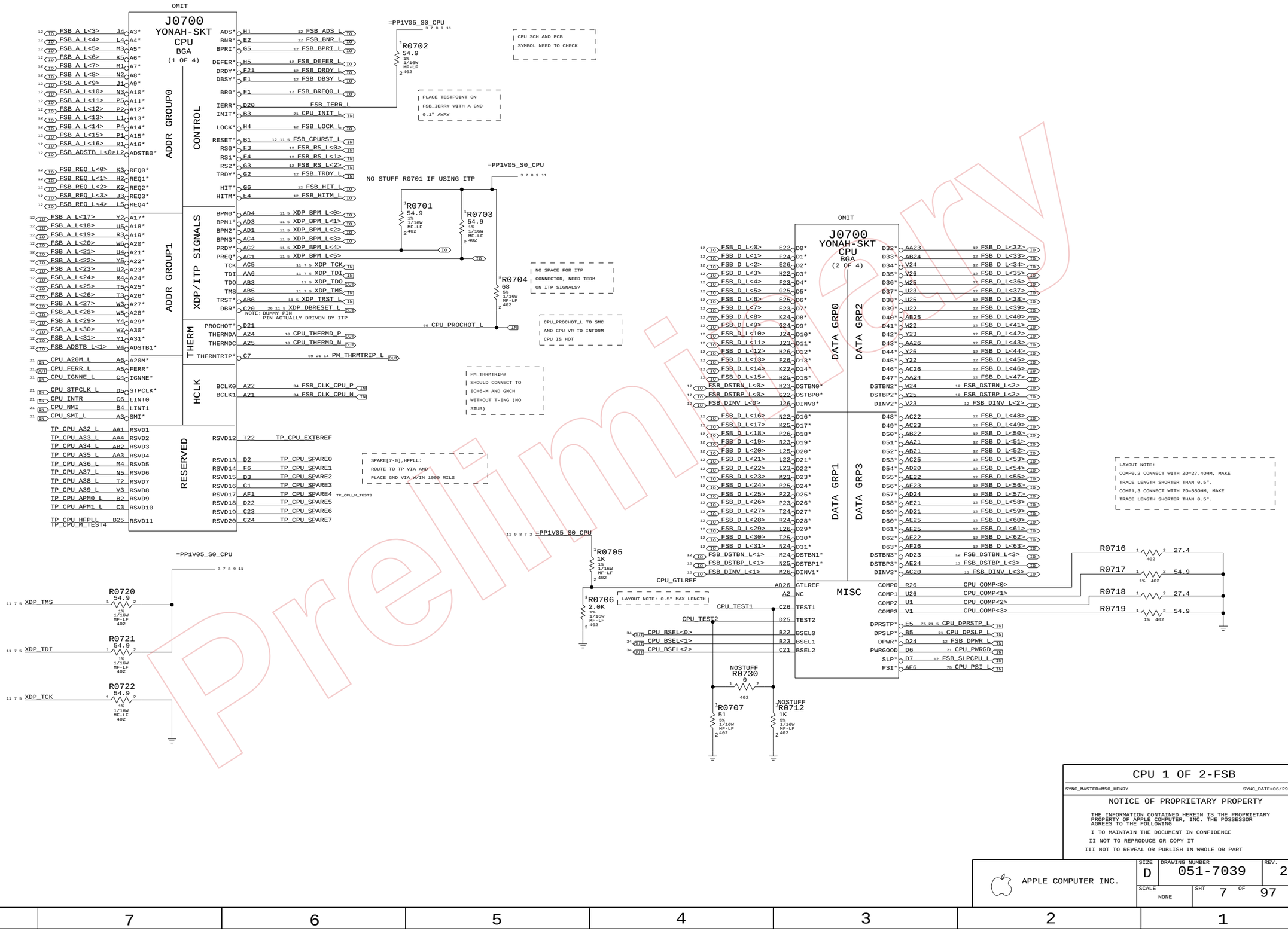


POWER CONN / MISC

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 6 OF 97	



CPU 1 OF 2-FSB

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

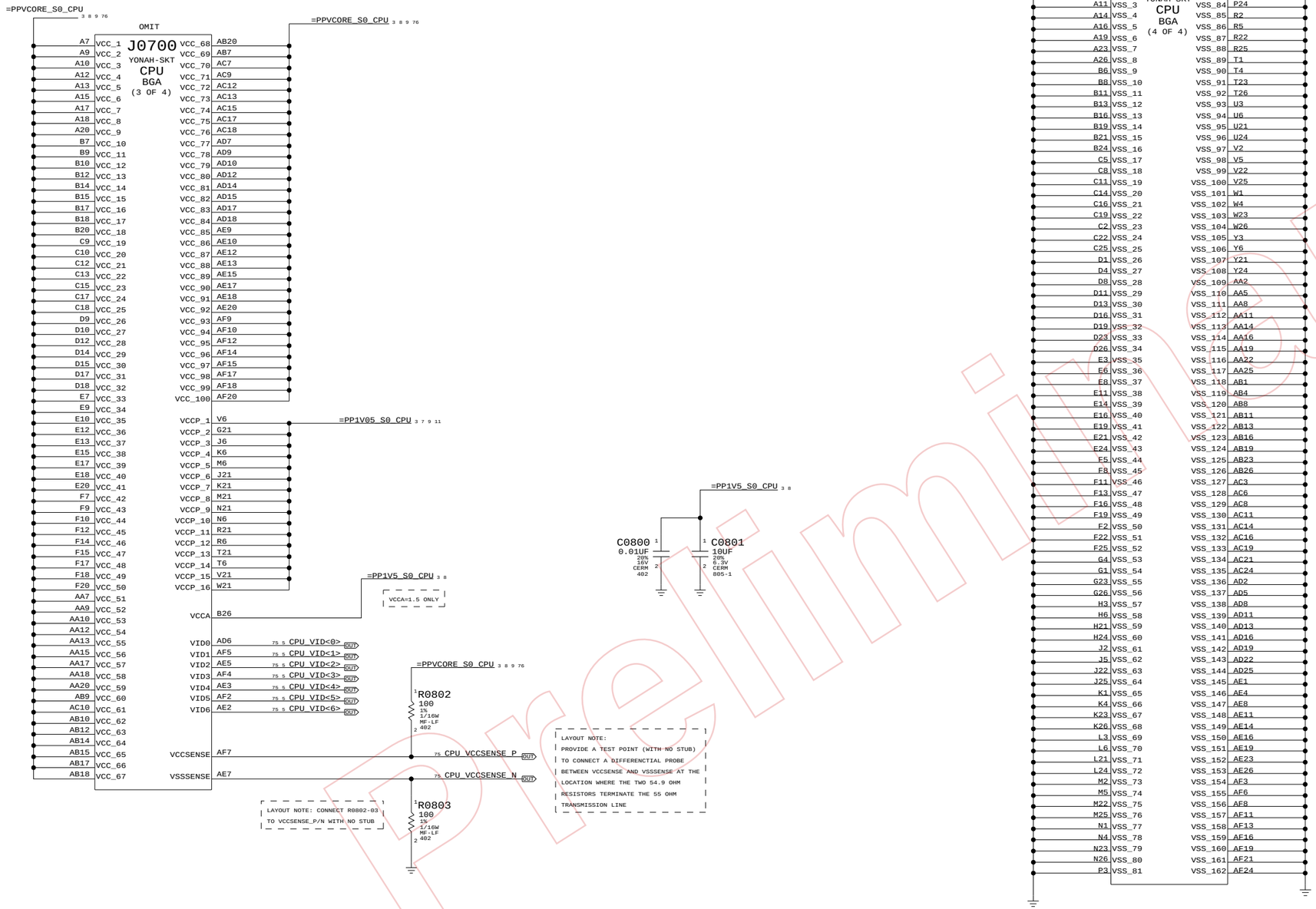
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 7 OF 97	



CPU 2 OF 2-PWR/GND

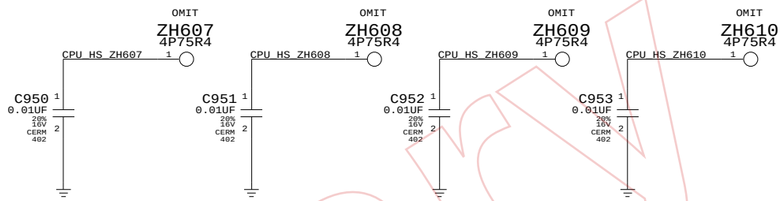
SYNC_MASTER=M59_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

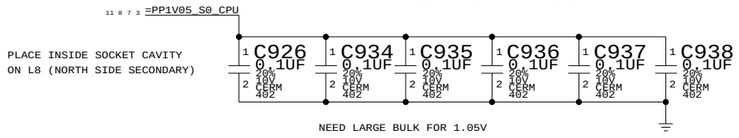
SCALE	SHT	OF
NONE	8	97

CPU HEATSINK MOUNTING HOLES

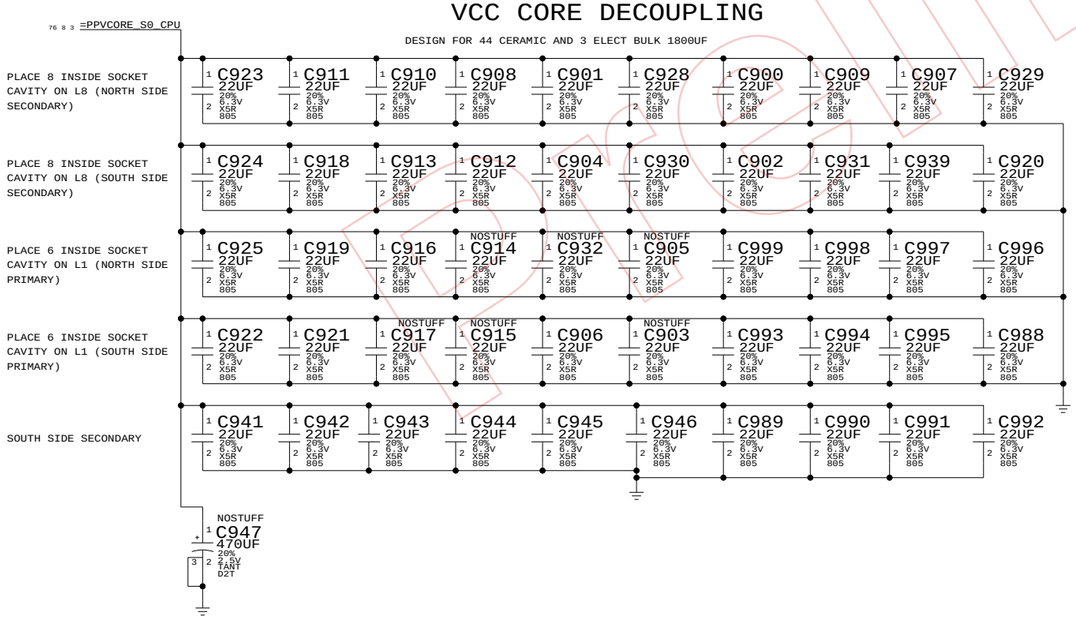


WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

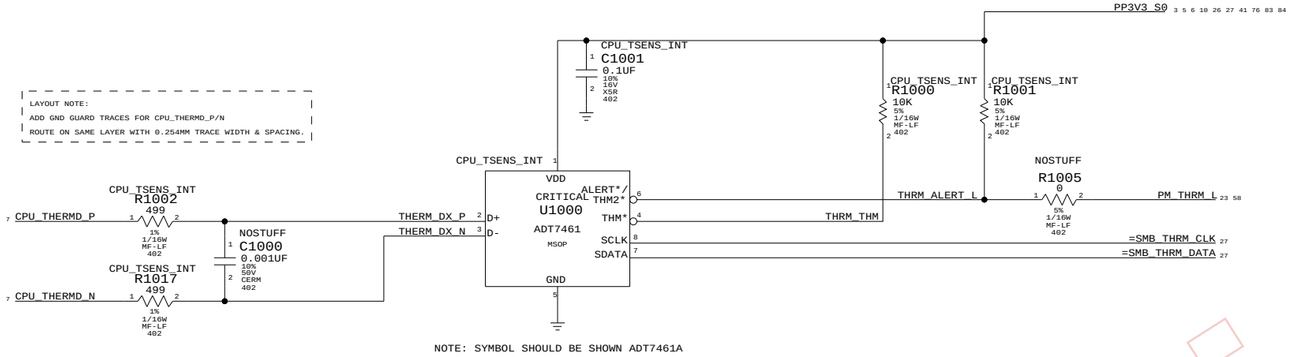
SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE	SHT	OF
NONE	9	97

CPU INTERNAL DIODE THERMAL SENSOR

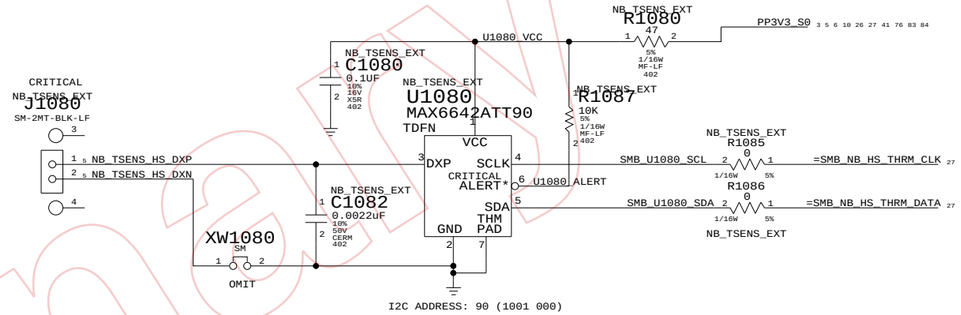
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



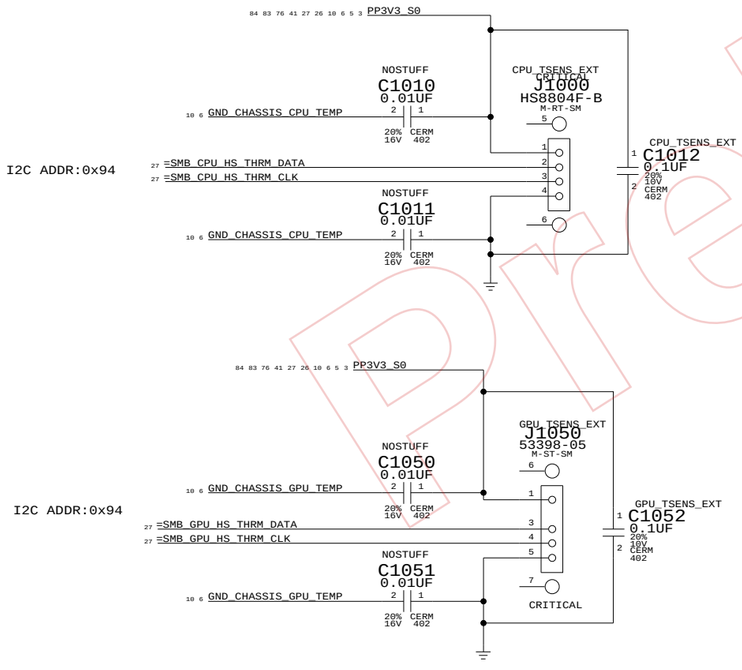
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

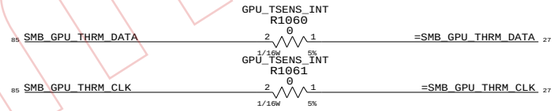


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

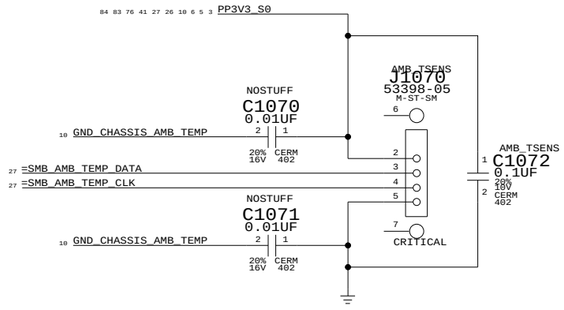


MXM CARD TEMPERATURE SENSOR (GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD
MAY NOT BE CONSISTENT WITH OTHER CARDS

AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



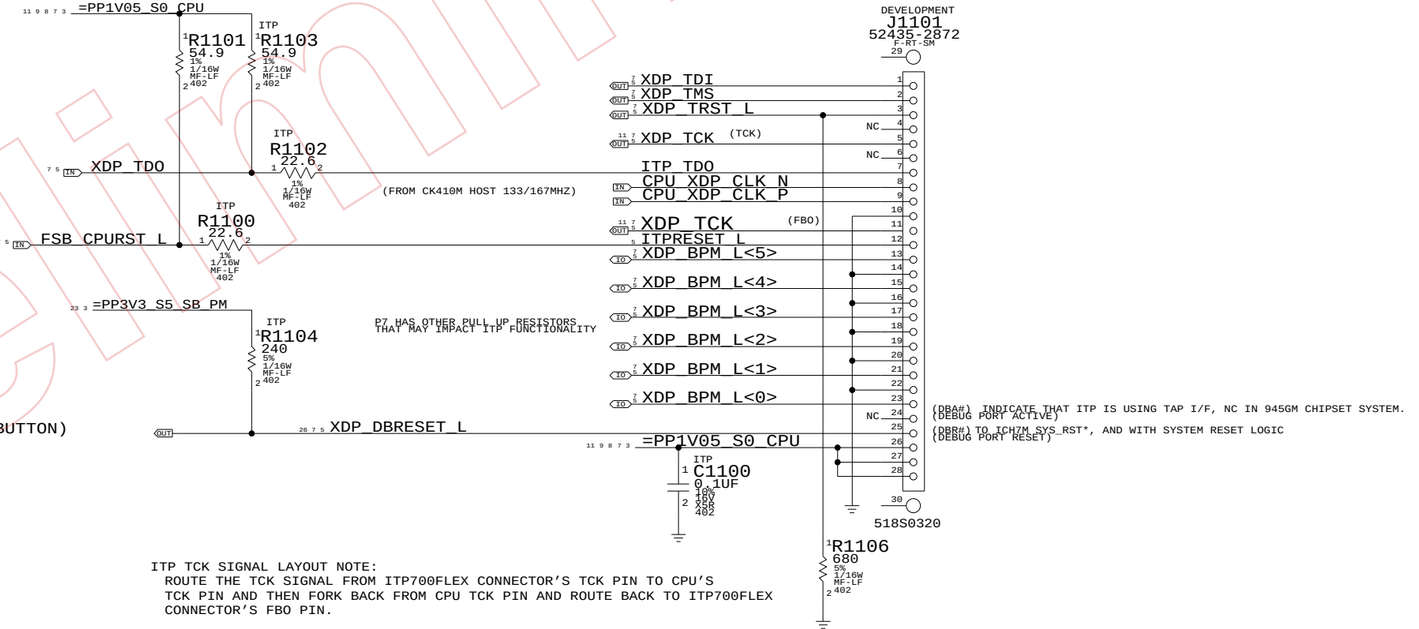
ASIC TEMP SENSORS

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 10 OF 97	

CPU ITP700FLEX DEBUG SUPPORT



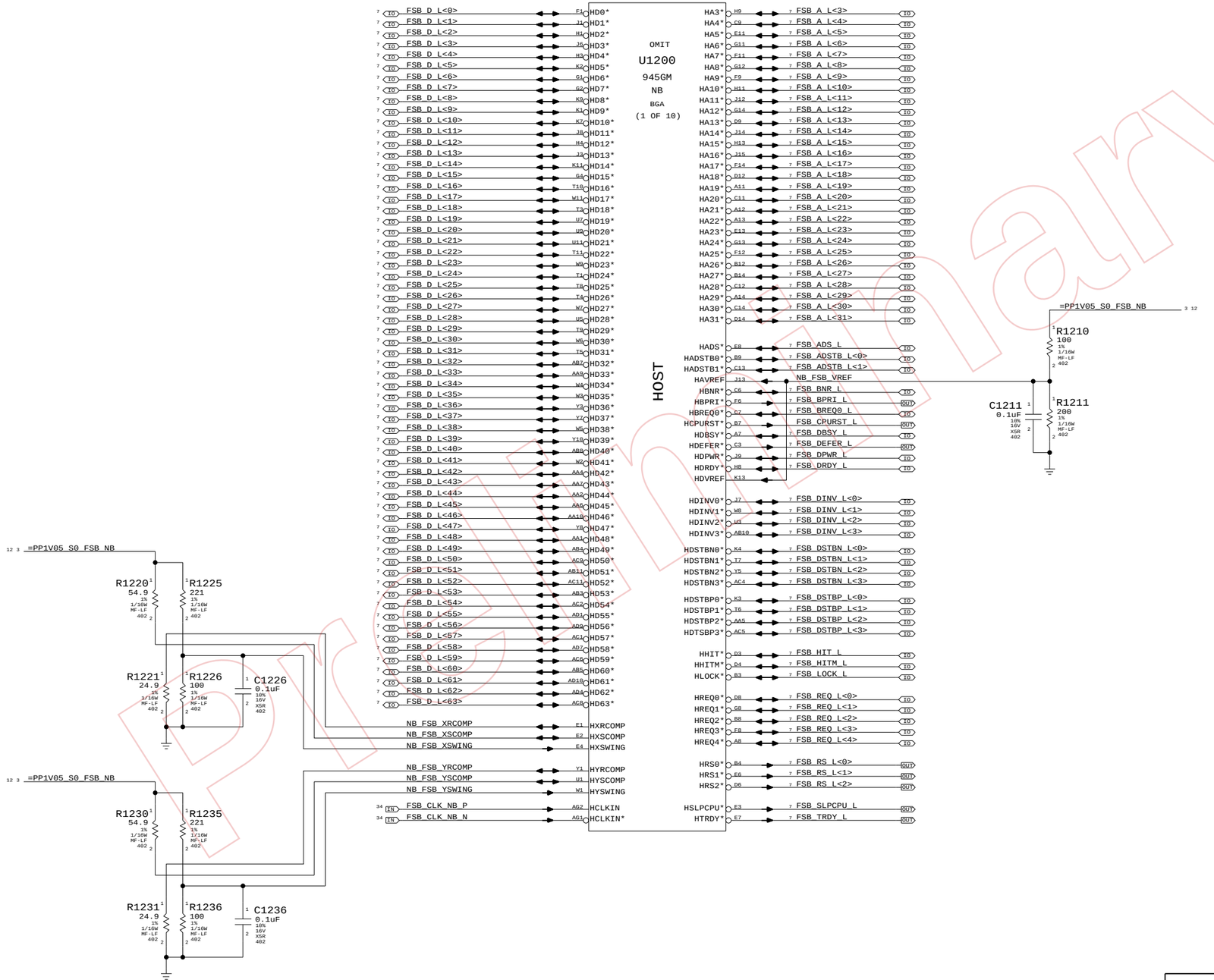
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 11 OF 97	



NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 12 OF 97	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

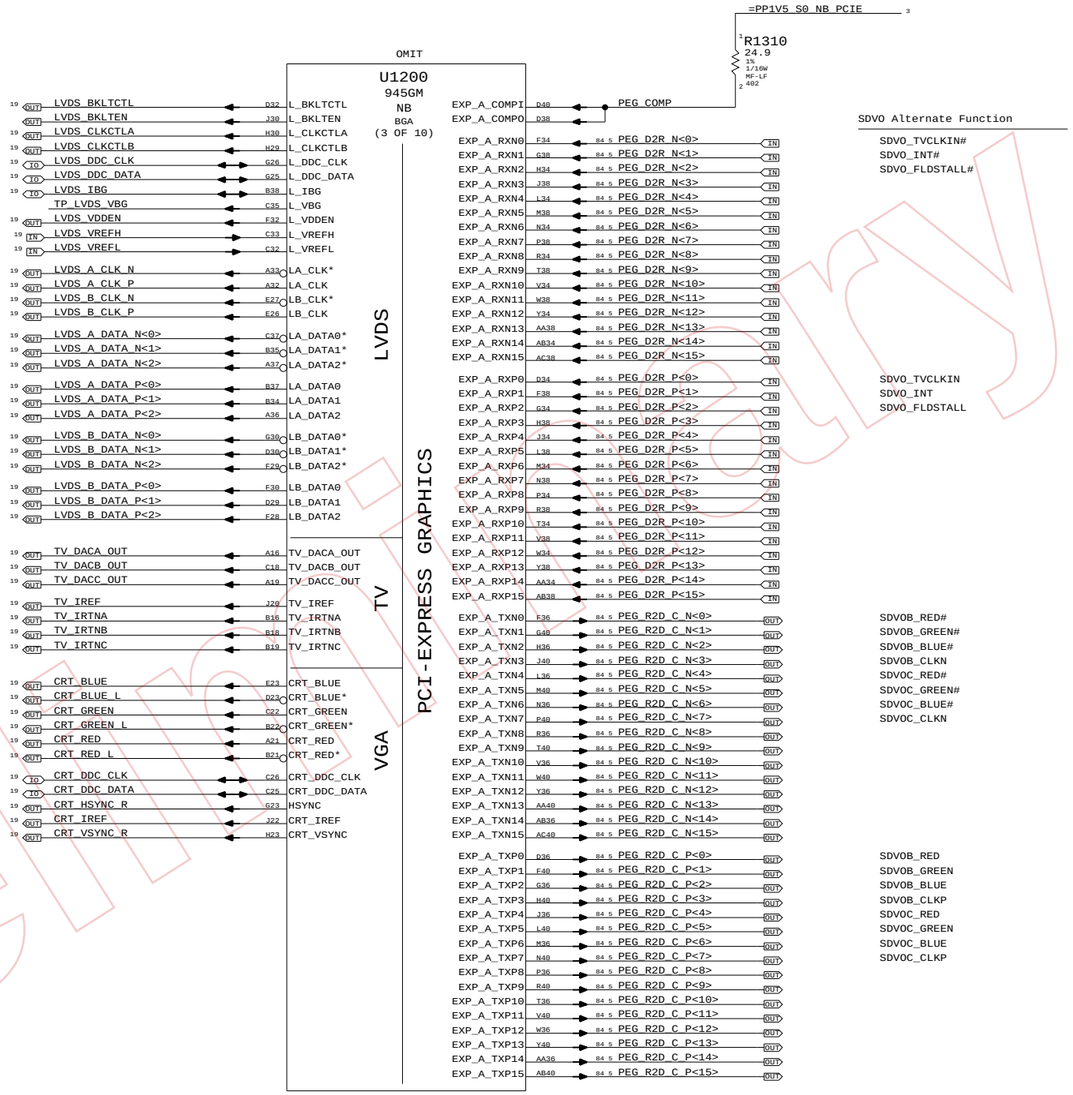
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

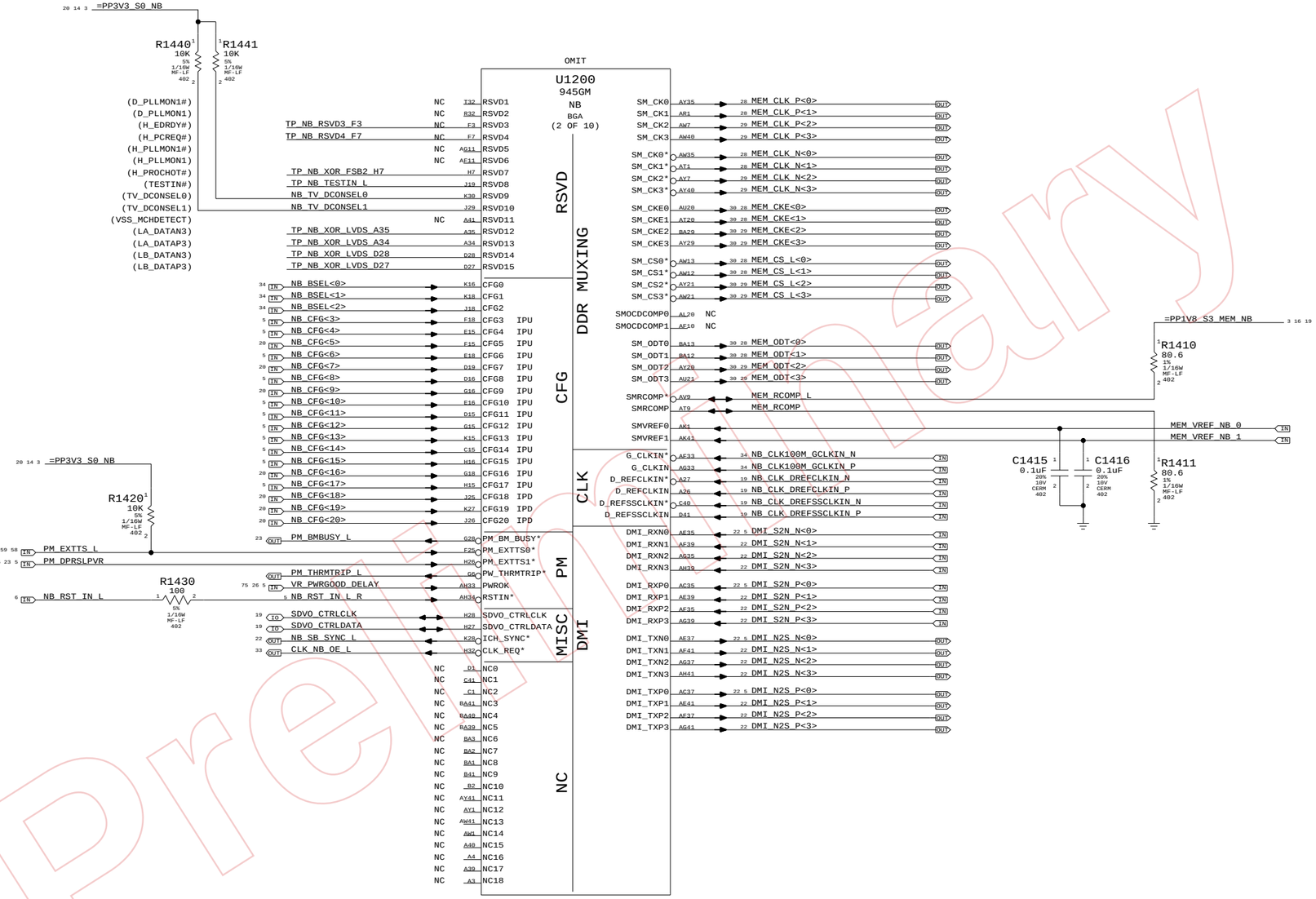


NB PEG / Video Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 13 OF 97	



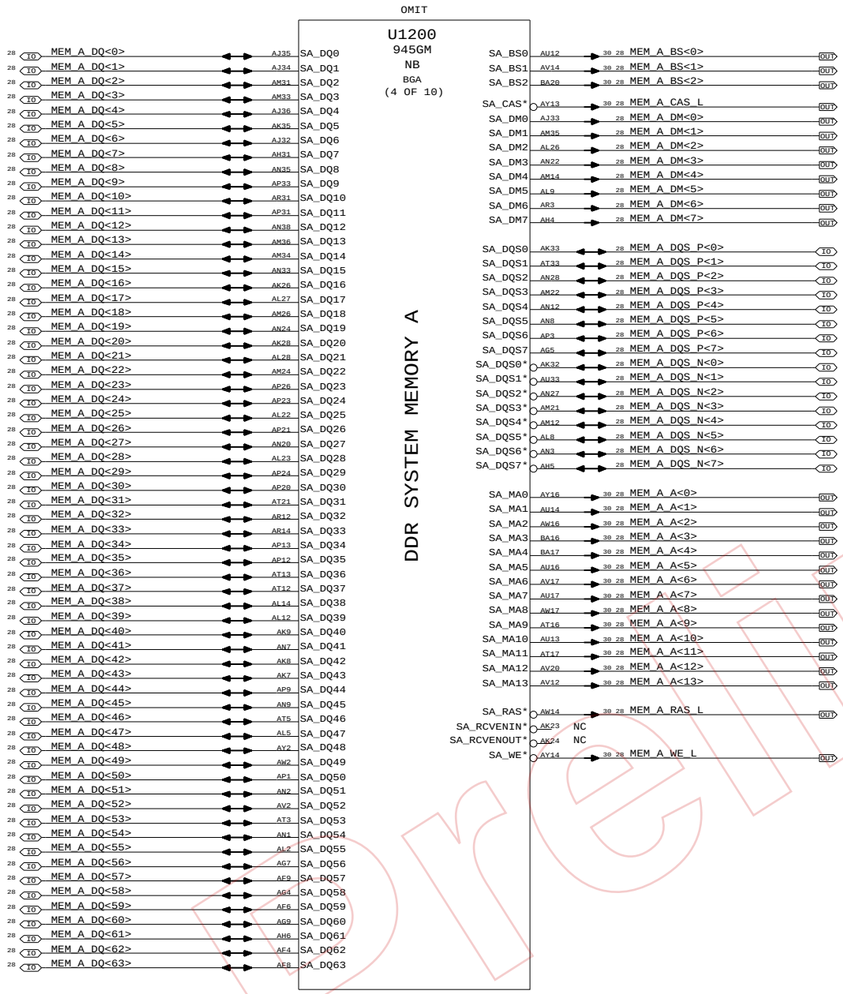
NB Misc Interfaces

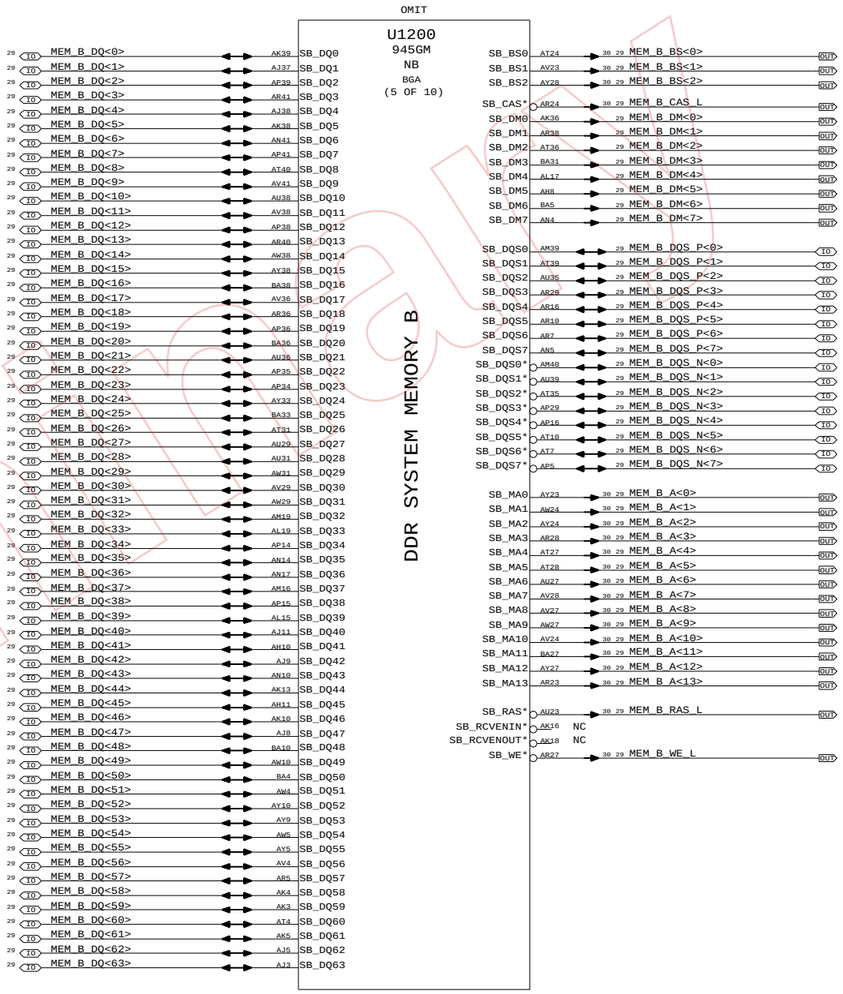
SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE SHT 14 OF 97



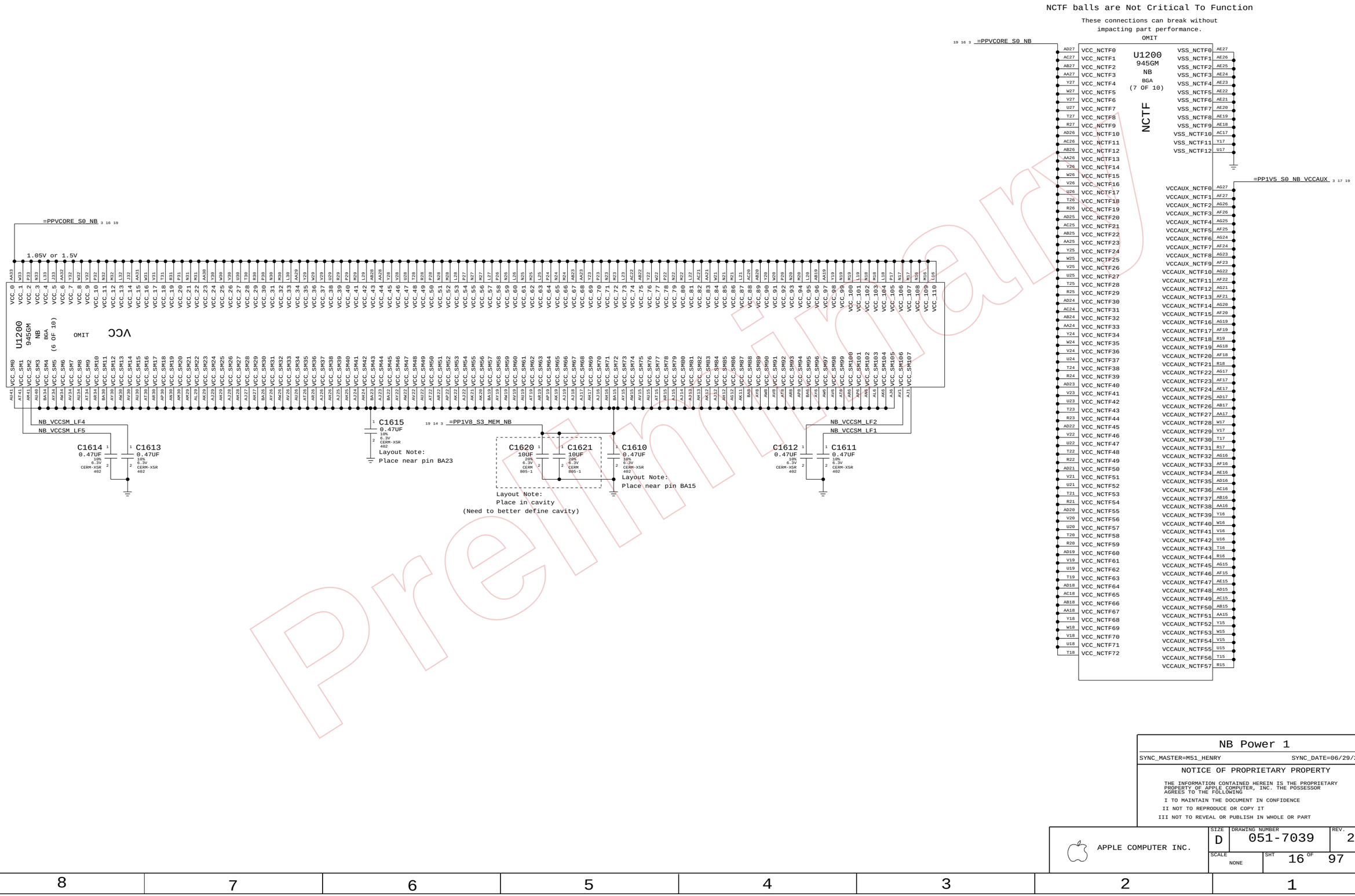


NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 15 OF 97	



NB Power 1

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

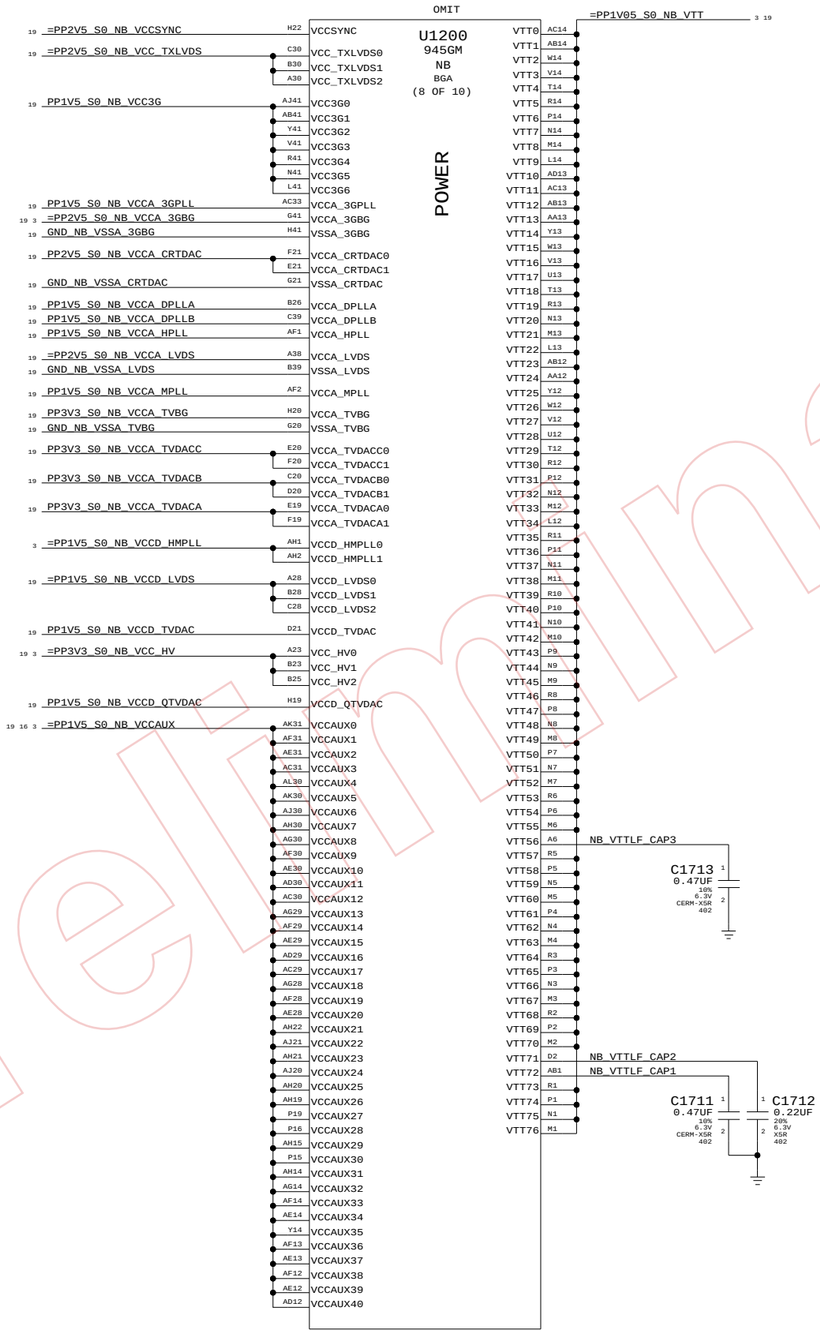
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE SHT 16 OF 97



NB Power 2

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 17 OF 97	

OMIT

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0		VSS_97	AK34	
AA41	VSS_1		VSS_98	AG34	
W41	VSS_2		VSS_99	AF34	
T41	VSS_3		VSS_100	AE34	
P41	VSS_4		VSS_101	AC34	
M41	VSS_5		VSS_102	C34	
J41	VSS_6		VSS_103	AW33	
F41	VSS_7		VSS_104	AV33	
AV40	VSS_8		VSS_105	AR33	
AP40	VSS_9		VSS_106	AE33	
AN40	VSS_10		VSS_107	AB33	
AK40	VSS_11		VSS_108	Y33	
AJ40	VSS_12		VSS_109	V33	
AH40	VSS_13		VSS_110	T33	
AG40	VSS_14		VSS_111	R33	
AF40	VSS_15		VSS_112	M33	
AE40	VSS_16		VSS_113	H33	
B40	VSS_17		VSS_114	G33	
AY39	VSS_18		VSS_115	F33	
AW39	VSS_19		VSS_116	D33	
AV39	VSS_20		VSS_117	B33	
AR39	VSS_21		VSS_118	AH32	
AN39	VSS_22		VSS_119	AG32	
AJ39	VSS_23		VSS_120	AF32	
AC39	VSS_24		VSS_121	AE32	
AB39	VSS_25		VSS_122	AC32	
AA39	VSS_26		VSS_123	AB32	
Y39	VSS_27		VSS_124	G32	
W39	VSS_28		VSS_125	B32	
V39	VSS_29		VSS_126	AY31	
T39	VSS_30		VSS_127	AV31	
R39	VSS_31		VSS_128	AN31	
P39	VSS_32		VSS_129	AJ31	
N39	VSS_33		VSS_130	AG31	
M39	VSS_34		VSS_131	AB31	
L39	VSS_35		VSS_132	Y31	
J39	VSS_36		VSS_133	AB30	
H39	VSS_37		VSS_134	E30	
G39	VSS_38		VSS_135	AT29	
F39	VSS_39		VSS_136	AN29	
D39	VSS_40		VSS_137	AB29	
AT38	VSS_41		VSS_138	T29	
AM38	VSS_42		VSS_139	N29	
AH38	VSS_43		VSS_140	K29	
AG38	VSS_44		VSS_141	G29	
AF38	VSS_45		VSS_142	E29	
AE38	VSS_46		VSS_143	C29	
C38	VSS_47		VSS_144	B29	
AK37	VSS_48		VSS_145	A29	
AH37	VSS_49		VSS_146	BA28	
AB37	VSS_50		VSS_147	AW28	
AA37	VSS_51		VSS_148	AU28	
Y37	VSS_52		VSS_149	AP28	
W37	VSS_53		VSS_150	AM28	
V37	VSS_54		VSS_151	AD28	
T37	VSS_55		VSS_152	AC28	
R37	VSS_56		VSS_153	W28	
P37	VSS_57		VSS_154	J28	
N37	VSS_58		VSS_155	E28	
M37	VSS_59		VSS_156	AP27	
L37	VSS_60		VSS_157	AM27	
J37	VSS_61		VSS_158	AK27	
H37	VSS_62		VSS_159	J27	
G37	VSS_63		VSS_160	G27	
F37	VSS_64		VSS_161	F27	
D37	VSS_65		VSS_162	C27	
AY36	VSS_66		VSS_163	B27	
AW36	VSS_67		VSS_164	AN26	
AN36	VSS_68		VSS_165	M26	
AH36	VSS_69		VSS_166	K26	
AG36	VSS_70		VSS_167	F26	
AF36	VSS_71		VSS_168	D26	
AE36	VSS_72		VSS_169	AK25	
AC36	VSS_73		VSS_170	P25	
C36	VSS_74		VSS_171	K25	
B36	VSS_75		VSS_172	H25	
BA35	VSS_76		VSS_173	E25	
AV35	VSS_77		VSS_174	D25	
AR35	VSS_78		VSS_175	A25	
AH35	VSS_79		VSS_176	BA24	
AB35	VSS_80		VSS_177	AU24	
AA35	VSS_81		VSS_178	AL24	
Y35	VSS_82		VSS_179	AW23	
W35	VSS_83				
V35	VSS_84				
T35	VSS_85				
R35	VSS_86				
P35	VSS_87				
N35	VSS_88				
M35	VSS_89				
L35	VSS_90				
J35	VSS_91				
H35	VSS_92				
G35	VSS_93				
F35	VSS_94				
D35	VSS_95				
AN34	VSS_96				

OMIT

U1200
945GM
NB
BGA
(10 OF 10)

VSS

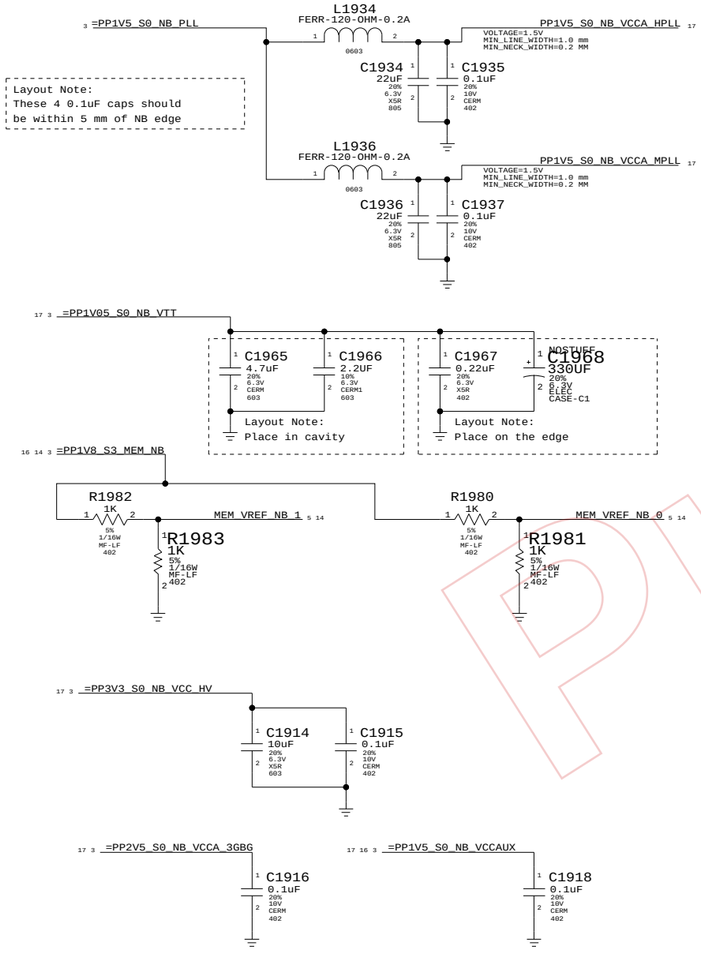
AT23	VSS_180		VSS_273	J11	
AN23	VSS_181		VSS_274	D11	
AM23	VSS_182		VSS_275	B11	
AH23	VSS_183		VSS_276	AV10	
AC23	VSS_184		VSS_277	AP10	
W23	VSS_185		VSS_278	AL10	
K23	VSS_186		VSS_279	AJ10	
J23	VSS_187		VSS_280	AG10	
F23	VSS_188		VSS_281	AC10	
C23	VSS_189		VSS_282	W10	
AA22	VSS_190		VSS_283	U10	
K22	VSS_191		VSS_284	BA9	
G22	VSS_192		VSS_285	AW9	
F22	VSS_193		VSS_286	AR9	
E22	VSS_194		VSS_287	AH9	
D22	VSS_195		VSS_288	AB9	
A22	VSS_196		VSS_289	Y9	
BA21	VSS_197		VSS_290	R9	
AV21	VSS_198		VSS_291	G9	
AR21	VSS_199		VSS_292	E9	
AN21	VSS_200		VSS_293	A9	
AL21	VSS_201		VSS_294	AG8	
AB21	VSS_202		VSS_295	AD8	
Y21	VSS_203		VSS_296	AA8	
P21	VSS_204		VSS_297	U8	
K21	VSS_205		VSS_298	K8	
J21	VSS_206		VSS_299	C8	
H21	VSS_207		VSS_300	BA7	
C21	VSS_208		VSS_301	AV7	
AW20	VSS_209		VSS_302	AP7	
AR20	VSS_210		VSS_303	AL7	
AM20	VSS_211		VSS_304	AJ7	
AA20	VSS_212		VSS_305	AH7	
K20	VSS_213		VSS_306	AF7	
B20	VSS_214		VSS_307	AC7	
A20	VSS_215		VSS_308	R7	
AN19	VSS_216		VSS_309	G7	
AC19	VSS_217		VSS_310	D7	
W19	VSS_218		VSS_311	AG6	
K19	VSS_219		VSS_312	AD6	
G19	VSS_220		VSS_313	AB6	
C19	VSS_221		VSS_314	Y6	
AH18	VSS_222		VSS_315	U6	
P18	VSS_223		VSS_316	N6	
H18	VSS_224		VSS_317	K6	
D18	VSS_225		VSS_318	H6	
A18	VSS_226		VSS_319	B6	
AY17	VSS_227		VSS_320	AV5	
AR17	VSS_228		VSS_321	AF5	
AP17	VSS_229		VSS_322	AD5	
AM17	VSS_230		VSS_323	AY4	
AK17	VSS_231		VSS_324	AR4	
AV16	VSS_232		VSS_325	AP4	
AN16	VSS_233		VSS_326	AL4	
AL16	VSS_234		VSS_327	AJ4	
J16	VSS_235		VSS_328	Y4	
F16	VSS_236		VSS_329	U4	
C16	VSS_237		VSS_330	R4	
AN15	VSS_238		VSS_331	J4	
AM15	VSS_239		VSS_332	F4	
AK15	VSS_240		VSS_333	C4	
N15	VSS_241		VSS_334	AY3	
M15	VSS_242		VSS_335	AW3	
L15	VSS_243		VSS_336	AV3	
B15	VSS_244		VSS_337	AL3	
A15	VSS_245		VSS_338	AH3	
BA14	VSS_246		VSS_339	AG3	
AT14	VSS_247		VSS_340	AF3	
AK14	VSS_248		VSS_341	AD3	
AD14	VSS_249		VSS_342	AC3	
AA14	VSS_250		VSS_343	AA3	
U14	VSS_251		VSS_344	G3	
K14	VSS_252		VSS_345	AT2	
H14	VSS_253		VSS_346	AR2	
E14	VSS_254		VSS_347	AP2	
AV13	VSS_255		VSS_348	AK2	
AR13	VSS_256		VSS_349	AJ2	
AN13	VSS_257		VSS_350	AD2	
AM13	VSS_258		VSS_351	AB2	
AL13	VSS_259		VSS_352	Y2	
AG13	VSS_260		VSS_353	U2	
P13	VSS_261		VSS_354	T2	
F13	VSS_262		VSS_355	N2	
D13	VSS_263		VSS_356	J2	
B13	VSS_264		VSS_357	H2	
AY12	VSS_265		VSS_358	F2	
AC12	VSS_266		VSS_359	C2	
K12	VSS_267		VSS_360	AL1	
H12	VSS_268				
E12	VSS_269				
AD11	VSS_270				
AA11	VSS_271				
Y11	VSS_272				

NB Grounds

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 18 OF 97	



TVOUT DISABLE

16 3 19 =PPVCORE_S0_NB

PP2V5_S0_NB_VCCA_CRTDAC 17

CRT_RED 13
CRT_RED_L 13
CRT_GREEN 13
CRT_GREEN_L 13
CRT_BLUE 13
CRT_BLUE_L 13
CRT_IREF 13

CRT_VSYNC_R 13
CRT_HSYNC_R 13
=PP2V5_S0_NB_VCCSYNC 17
GND_NB_VSSA_CRTDAC 17

TP_CRT_DDC_CLK TRUE CRT_DDC_CLK 13
TP_CRT_DDC_DATA TRUE CRT_DDC_DATA 13

DISPLAY DISABLE

TP_NB_VCCA_DPLLA TRUE PP1V5_S0_NB_VCCA_DPLLA 17
TP_NB_VCCA_DPLLB TRUE PP1V5_S0_NB_VCCA_DPLLB 17

NB_CLK_DREFCLKIN_N 14
NB_CLK_DREFCLKIN_P 14
NB_CLK_DREFSSCLKIN_P 14
NB_CLK_DREFSSCLKIN_N 14

LVDS DISABLE

13 LVDS_A_CLK_N TRUE TP_LVDS_A_CLK_N
13 LVDS_A_CLK_P TRUE TP_LVDS_A_CLK_P
13 LVDS_B_CLK_N TRUE TP_LVDS_B_CLK_N
13 LVDS_B_CLK_P TRUE TP_LVDS_B_CLK_P

13 LVDS_A_DATA_N<0> TRUE TP_LVDS_A_DATA_N<0>
13 LVDS_A_DATA_N<1> TRUE TP_LVDS_A_DATA_N<1>
13 LVDS_A_DATA_N<2> TRUE TP_LVDS_A_DATA_N<2>

13 LVDS_A_DATA_P<0> TRUE TP_LVDS_A_DATA_P<0>
13 LVDS_A_DATA_P<1> TRUE TP_LVDS_A_DATA_P<1>
13 LVDS_A_DATA_P<2> TRUE TP_LVDS_A_DATA_P<2>

13 LVDS_B_DATA_N<0> TRUE TP_LVDS_B_DATA_N<0>
13 LVDS_B_DATA_N<1> TRUE TP_LVDS_B_DATA_N<1>
13 LVDS_B_DATA_N<2> TRUE TP_LVDS_B_DATA_N<2>

13 LVDS_B_DATA_P<0> TRUE TP_LVDS_B_DATA_P<0>
13 LVDS_B_DATA_P<1> TRUE TP_LVDS_B_DATA_P<1>
13 LVDS_B_DATA_P<2> TRUE TP_LVDS_B_DATA_P<2>

13 5 LVDS_BKLTEN TRUE TP_LVDS_BKLTEN 5
13 LVDS_VDDEN TRUE TP_LVDS_VDDEN
13 LVDS_IBG TRUE TP_LVDS_IBG
17 GND_NB_VSSA_LVDS TRUE TP_GND_NB_VSSA_LVDS

13 LVDS_VREFH TRUE TP_LVDS_VREFH
13 LVDS_VREFL TRUE TP_LVDS_VREFL

17 =PP2V5_S0_NB_VCCA_LVDS
17 =PP1V5_S0_NB_VCCD_LVDS
17 =PP2V5_S0_NB_VCC_TXLVDS

13 LVDS_BKLTCTL TRUE TP_LVDS_BKLTCTL
13 LVDS_CLKCTLA TRUE TP_LVDS_CLKCTLA
13 LVDS_CLKCTLB TRUE TP_LVDS_CLKCTLB
13 LVDS_DDC_CLK TRUE TP_LVDS_DDC_CLK
13 LVDS_DDC_DATA TRUE TP_LVDS_DDC_DATA

TVOUT DISABLE

3 =PP1V5_S0_NB

PP3V3_S0_NB_VCCA_TVDACA 17
PP3V3_S0_NB_VCCA_TVDACB 17
PP3V3_S0_NB_VCCA_TVDACC 17
PP3V3_S0_NB_VCCA_TVBG 17

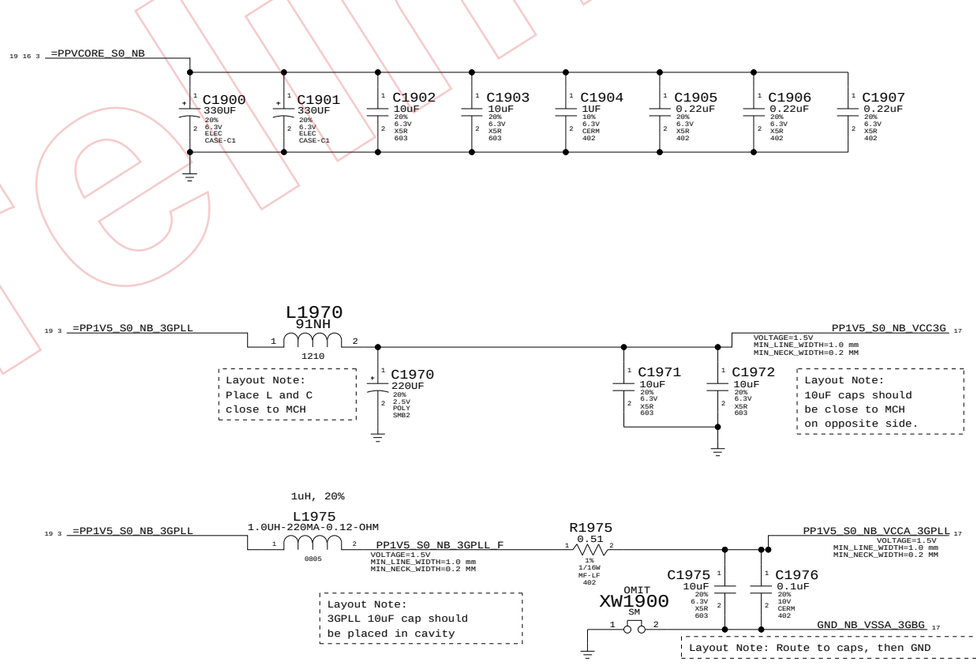
TV_DACA_OUT 13
TV_DACB_OUT 13
TV_DACC_OUT 13
TV_IREF 13
TV_IRTNA 13
TV_IRTNB 13
TV_IRTNC 13

GND_NB_VSSA_TVBG 17

3 =PP1V5_S0_NB_TVDAC

PP1V5_S0_NB_VCCD_TVDAC 17
PP1V5_S0_NB_VCCD_QTVDAC 17

14 SDVO_CTRLCLK TRUE TP_SDVO_CTRLCLK
14 SDVO_CTRLDATA TRUE TP_SDVO_CTRLDATA



NB (GM) Decoupling

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 19 OF 97	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075 2.2K 5% 1/16W MF-LF 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077 2.2K 5% 1/16W MF-LF 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079 2.2K 5% 1/16W MF-LF 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085 2.2K 5% 1/16W MF-LF 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 3 14 20
NBCFG_VCC_1V5
R2058 2.2K 5% 1/16W MF-LF 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 3 14 20
NBCFG_DMI_REVERSE
R2059 2.2K 5% 1/16W MF-LF 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 3 14 20
NBCFG_SDVO_AND_PCIE
R2060 2.2K 5% 1/16W MF-LF 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

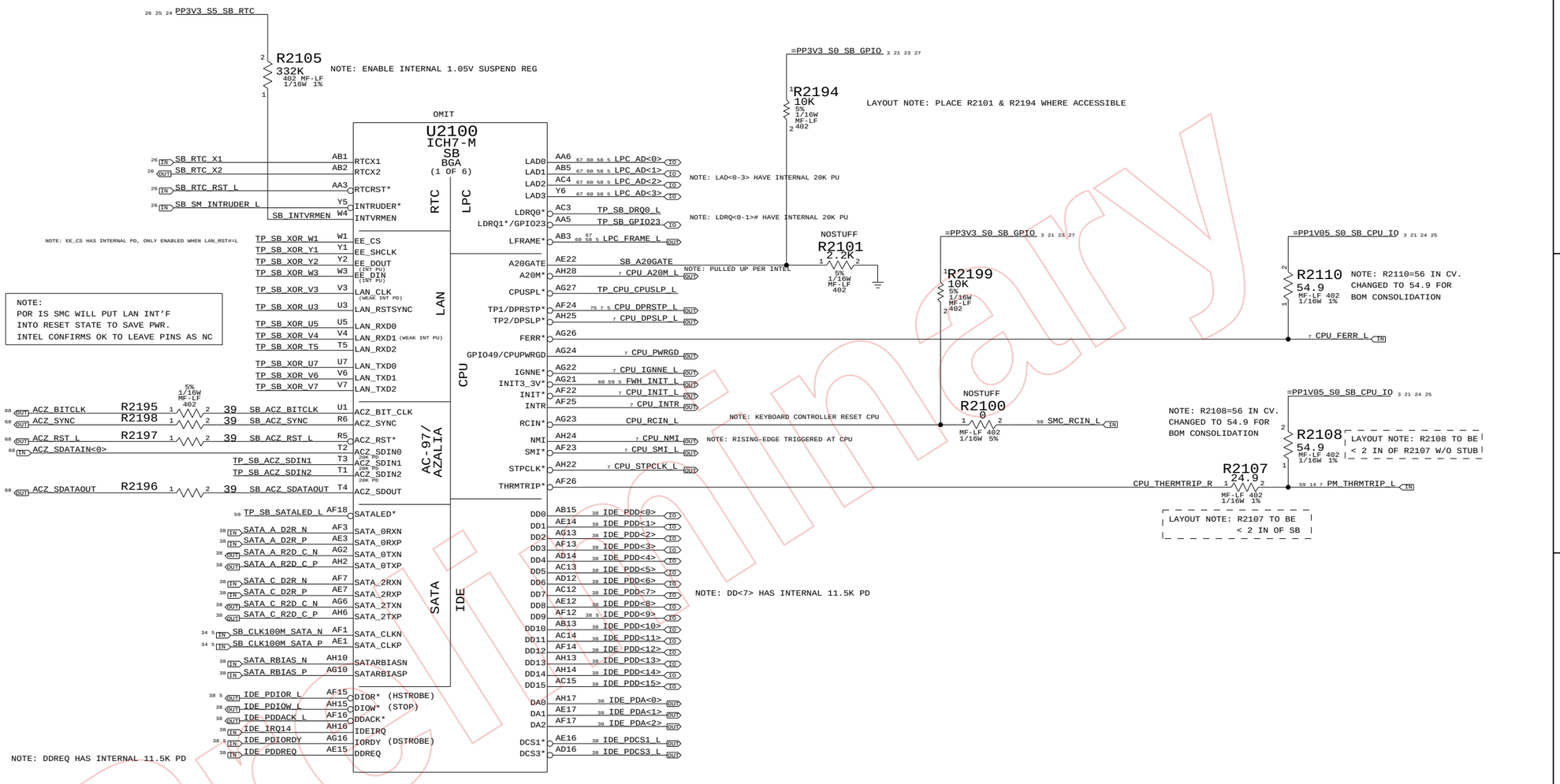
NB Config Straps

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE NONE SHT 20 OF 97



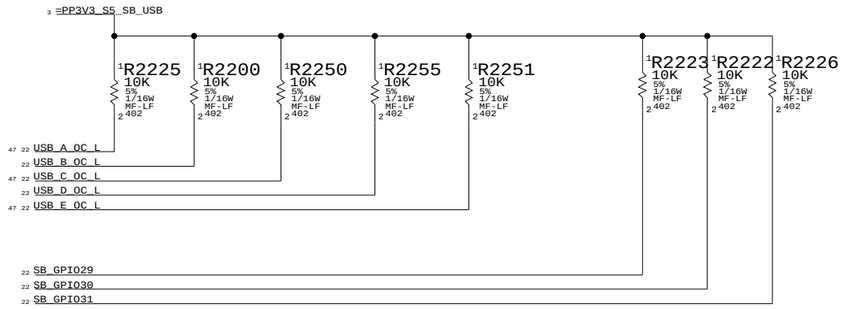
	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

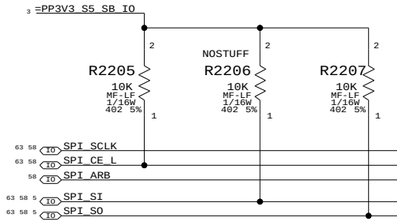
SB: 1 OF 4

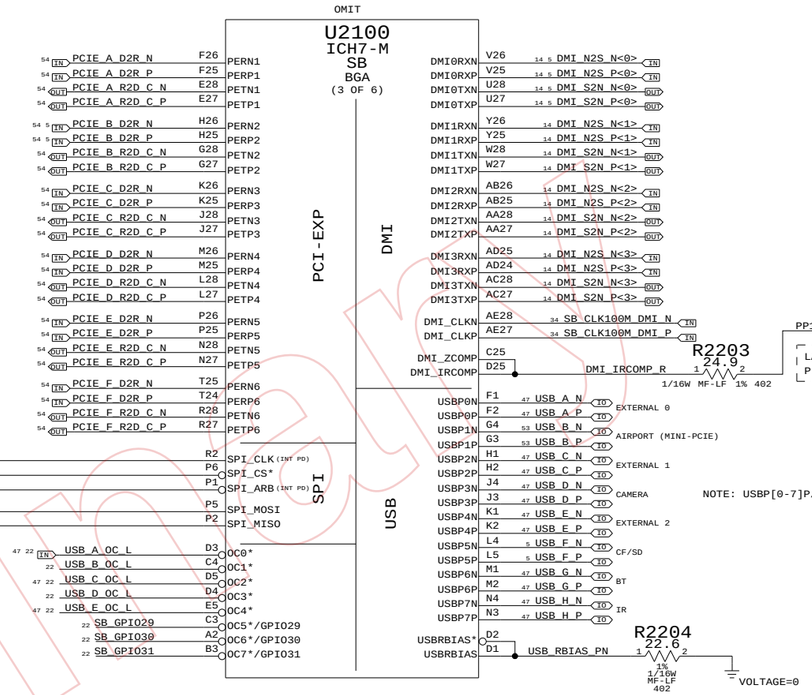
SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

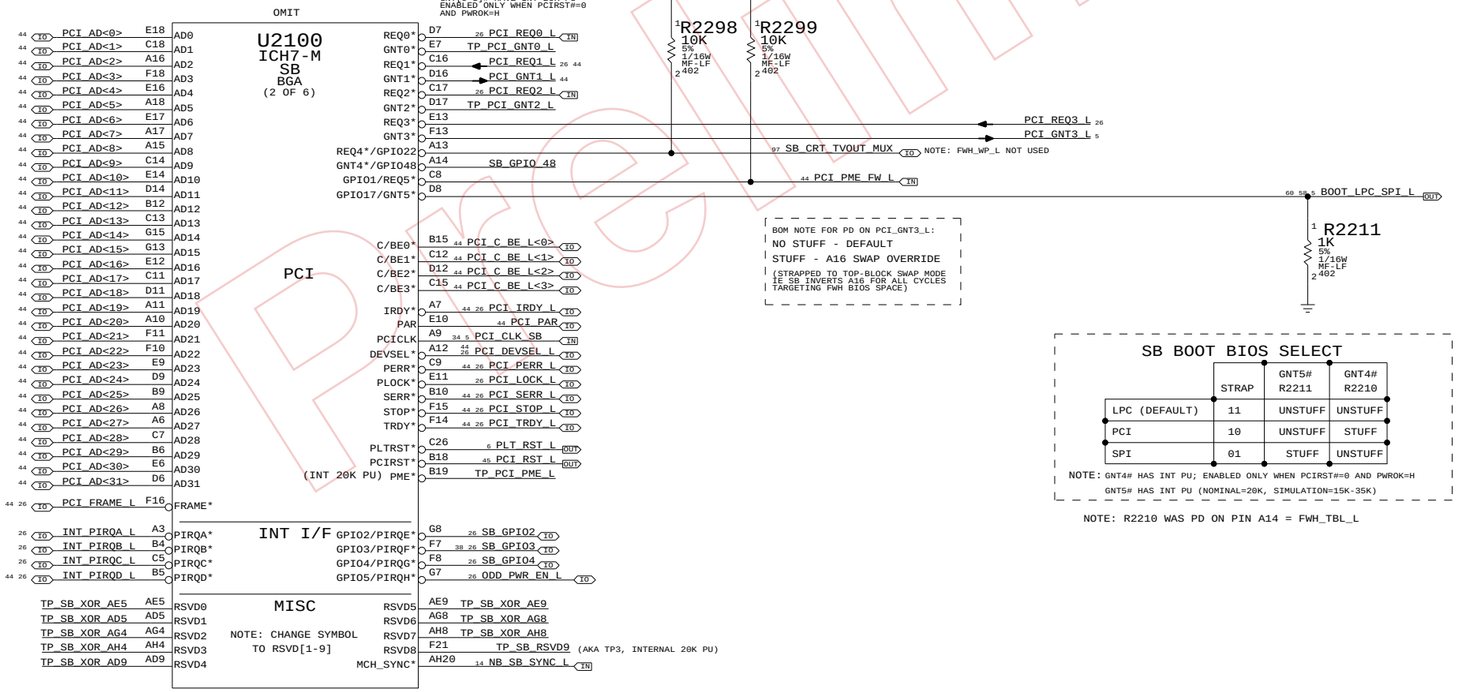
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 21 OF 97	









SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE SHT 22 OF 97

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 3 21 23 27

=PP3V3_S5_SB 3 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

26 25 23 3 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 TO SMB_CLK — C22 SMBCLK
27 TO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
67 60 58 5 OUT PM_SUS_STAT_L — A27 SUS_STAT*
58 26 IN PM_SYSRST_L — A22 SYS_RST*
14 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

SYS GPIO / PWR MNGT

33 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
34 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23 BIOS_REC — B21 GPIO27
23 FWH_MFG_MODE — E23 GPIO28
67 60 58 5 TO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*
53 41 IN PCIE_WAKE_L — F20 WAKE*
67 60 58 5 TO INT_SERIRQ — AH21 SERIRQ
58 10 IN PM_THRM_L — AF20 THRM*
26 5 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
6 GPU_PRESENT_R — AC21 GPIO6
58 IN SMC_RUNTIME_SCI_L — AC18 GPIO7
58 IN SMC_EXTSMI_L — E21 GPIO8

GPIO

SATA GPIO

GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
38 SATA_C_DET_L IN

CLKS

CLK14 — AC1 — 34 5 SB_CLK14P3M_TIMER IN
CLK48 — B2 — 34 5 SB_CLK48M_USBCTLR IN
SUSCLK — C20 — 59 SUS_CLK_SB OUT

SLP_S3* — B24 — 79 77 58 5 PM_SLP_S3_L OUT
SLP_S4* — D23 — 77 58 5 PM_SLP_S4_L OUT
SLP_S5* — F22 — 58 PM_SLP_S5_L OUT
PWROK — AA4 — 26 PM_SB_PWROK IN
AC22 — 75 14 5 PM_DPRSLPVR OUT
GPIO16/DPRSLPVR
TP0/BATLOW* — C21 — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 — 58 PM_PWRBTN_L IN
LAN_RST* — C19 — 58 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO9 — E20 — 58 26 SMS_INT_L IN
GPIO10 — A20 — 58 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 38 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 5 23 60
GPIO24 — R3 — TP_SB_GPIO24
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 33 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 TO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 3 11

NOSTUFF R2387 10K 1/16W 402 MF-LF 5%
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L IN
58 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
58 SMC_WAKE_SCI_L IN

26 25 23 3 =PP3V3_S5_SB

NOSTUFF R2306 10K 1/16W 402 MF-LF 5%
NOSTUFF R2308 10K 1/16W 402 MF-LF 5%

SV_SET_UP 5 23 60
EFI_OK_R

R2307 10K 1/16W 402 MF-LF 5%
R2309 10K 1/16W 402 MF-LF 5%

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 3 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

NOSTUFF R2314 0 1/16W 402 MF-LF 5%
NOSTUFF R2311 10K 1/16W 402 MF-LF 5%

=PP3V3_S5_SB 3 23 25 26

R2390 10K 5% 1/16W MF-LF 402
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 3 21 23 27

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L

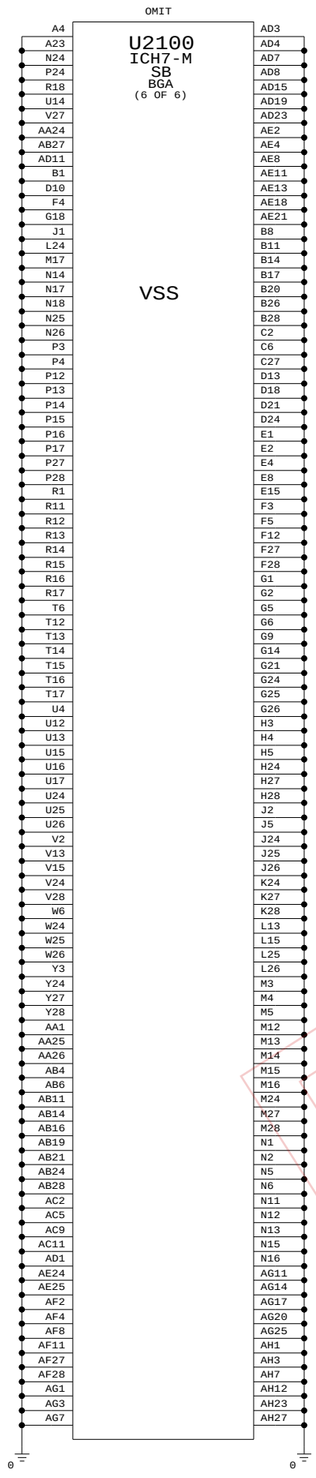
SB: 3 OF 4

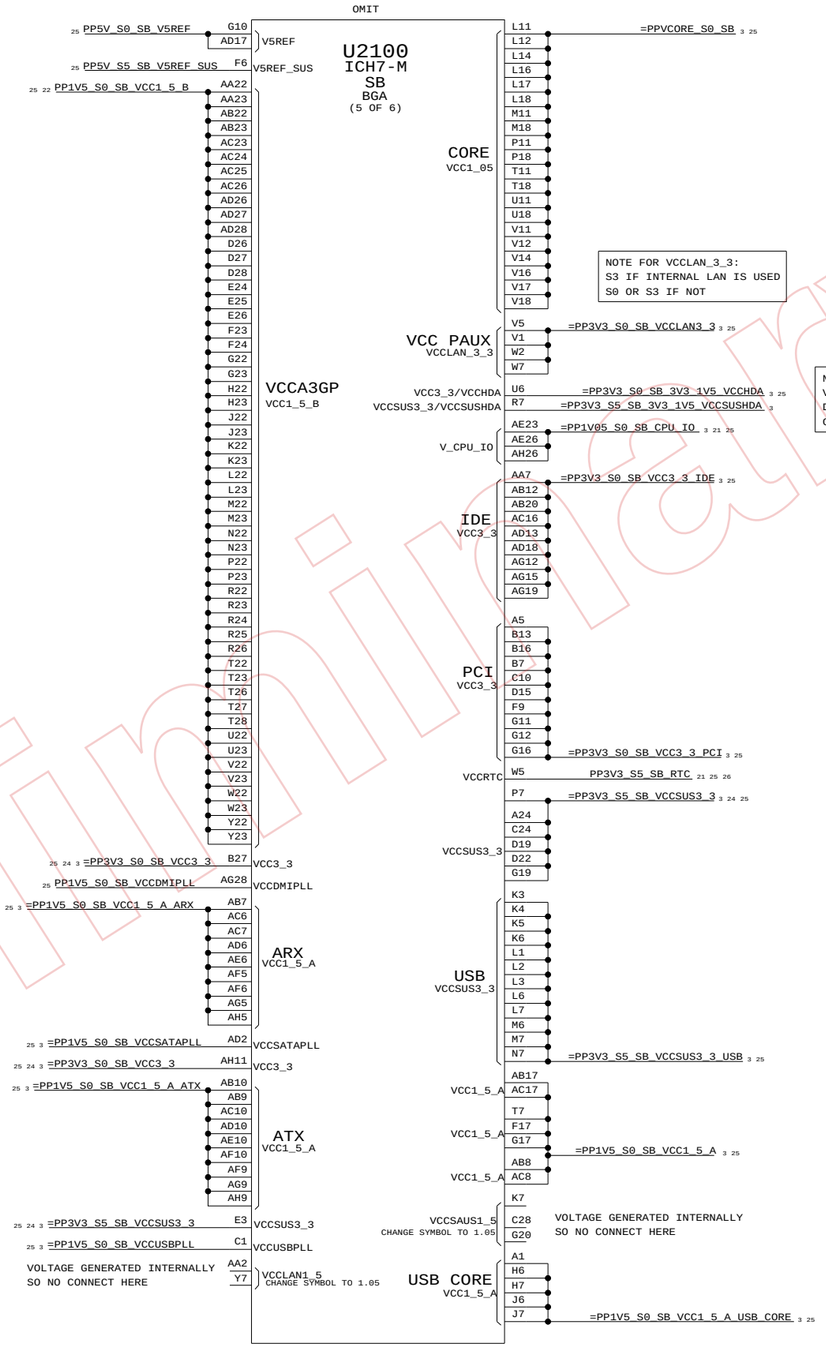
SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE	SHT
NONE	23 OF 97



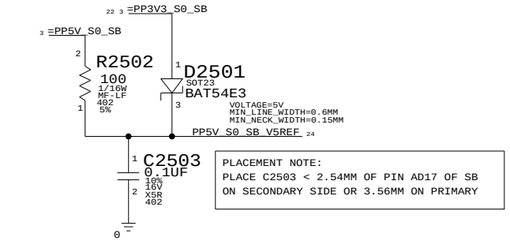


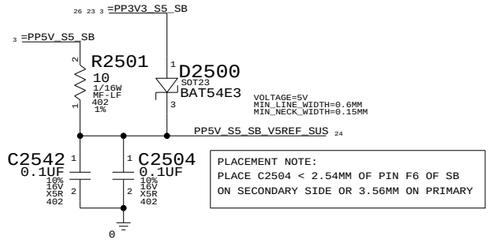
SB: 4 OF 4

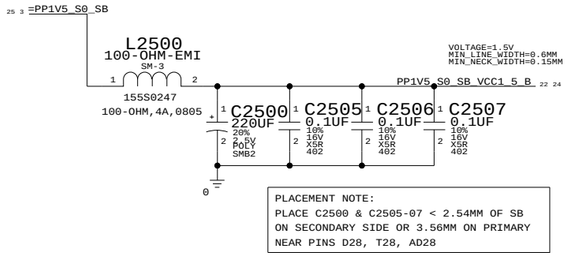
SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

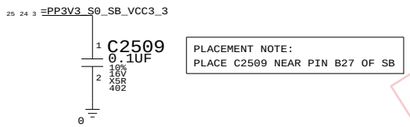
APPLE COMPUTER INC.

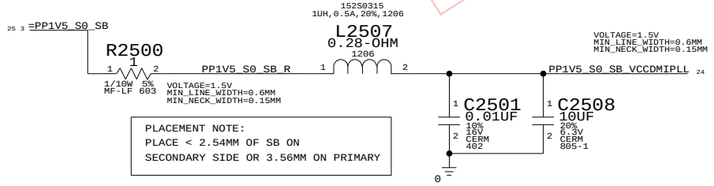
SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 24 OF 97	

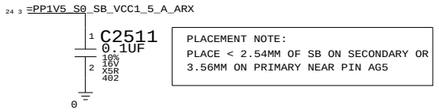


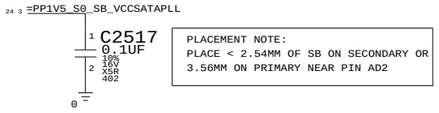


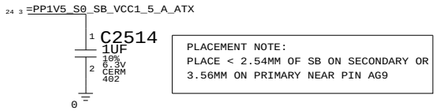


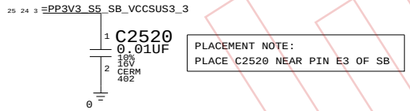


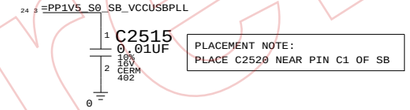


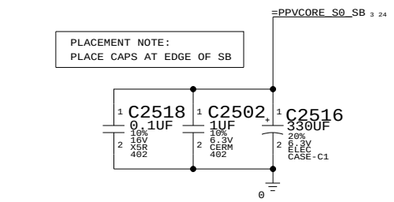


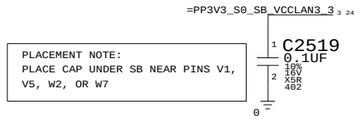


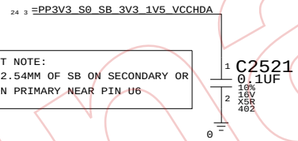


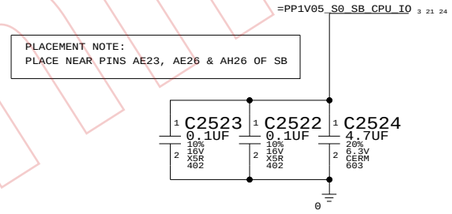


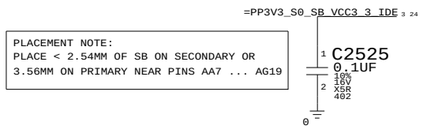


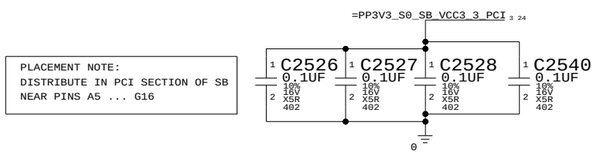


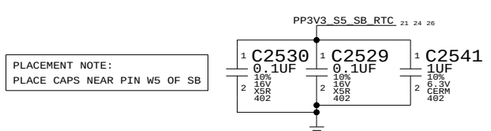


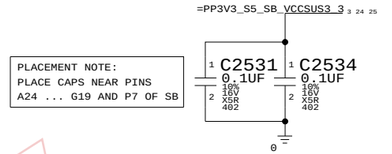


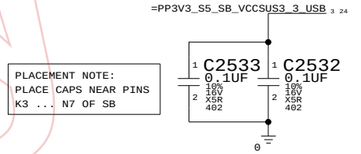


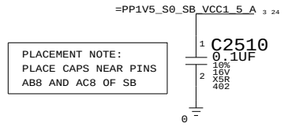


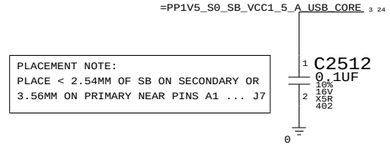












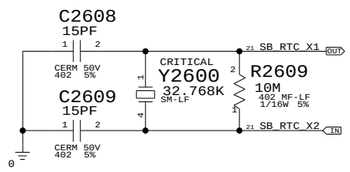
SB:DECOUPLING

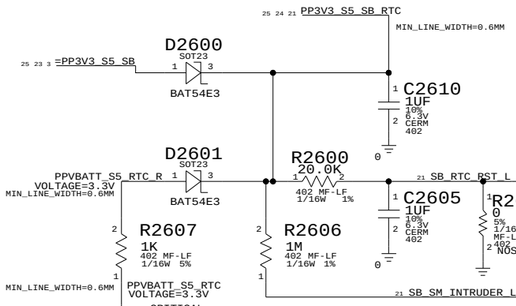
SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

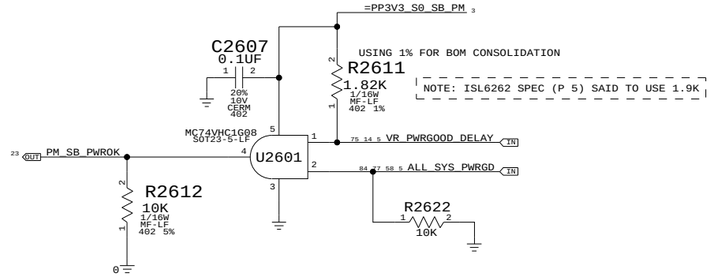
APPLE COMPUTER INC.

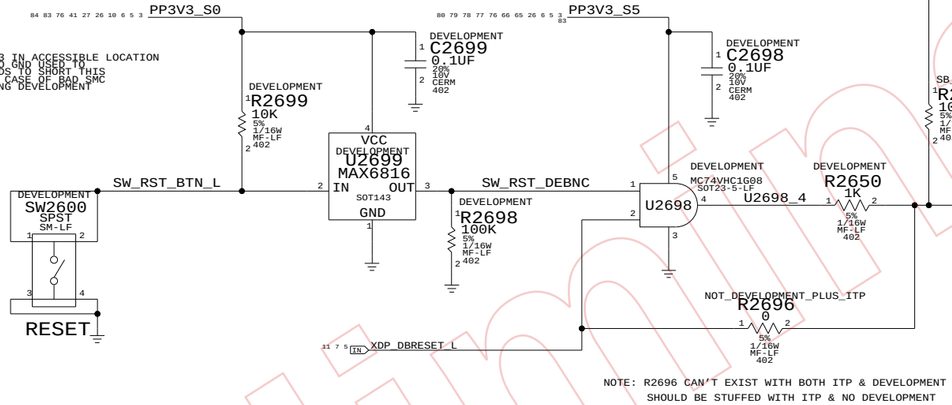
SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE SHT 25 OF 97

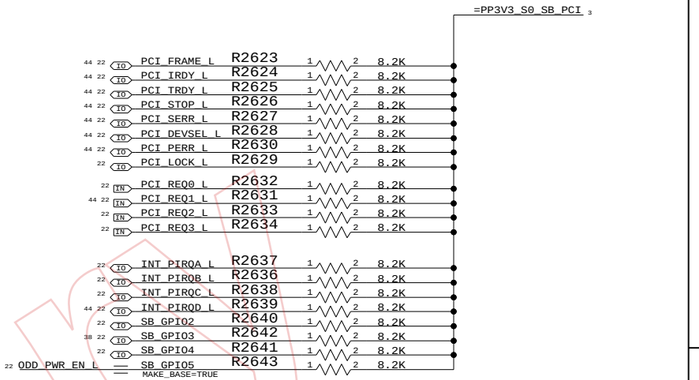


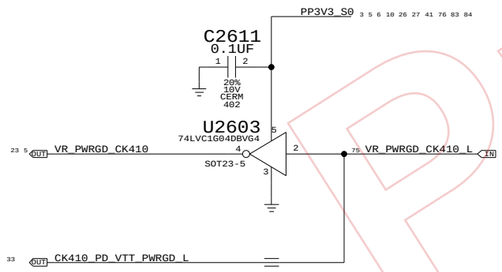






NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT





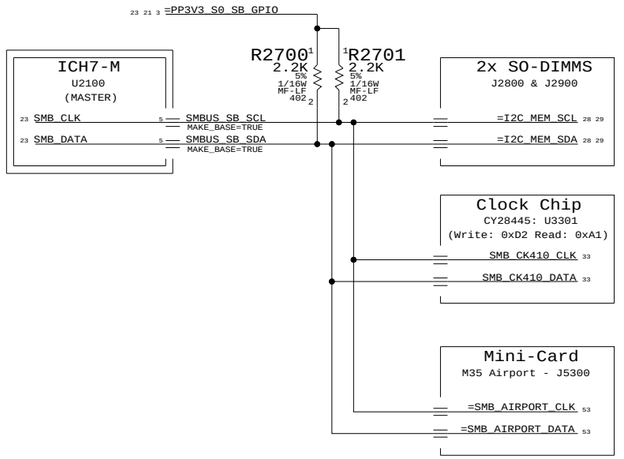
SB: MISC

SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

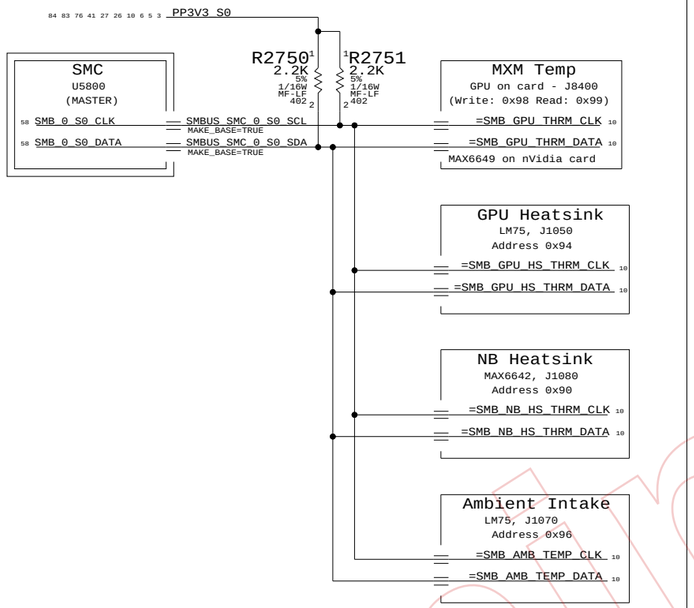
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 26 OF 97	

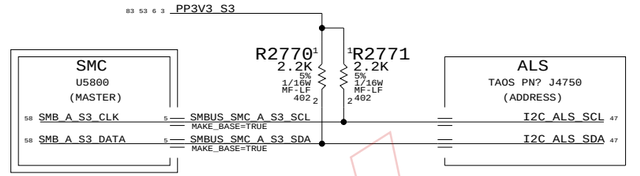
ICH7-M SMBus Connections



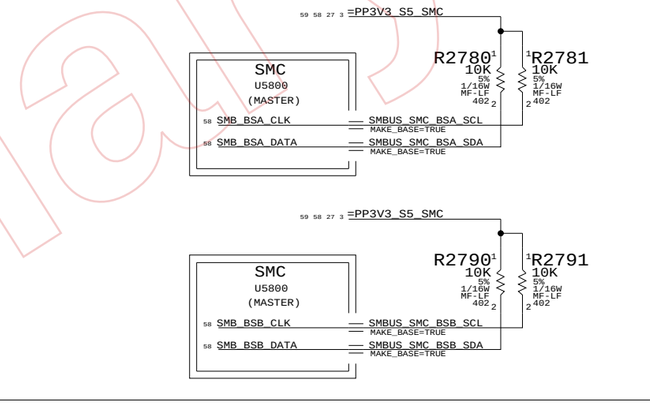
SMC "0" SMBus Connections



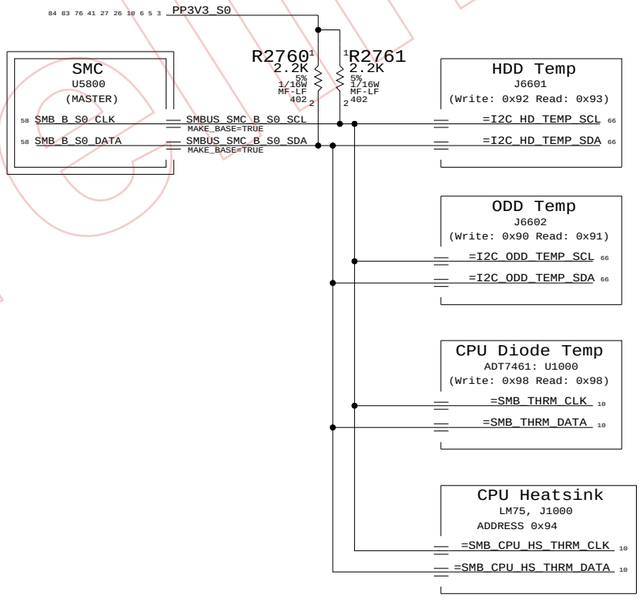
SMC "A" SMBus Connections



Unused SMC "Battery A/B" SMBus



SMC "B" SMBus Connections



M51 SMBus Connections

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 27 OF 97	

Page Notes

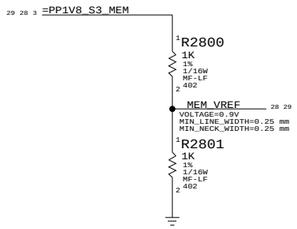
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

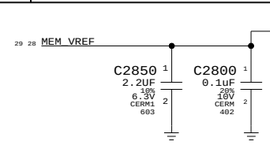
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

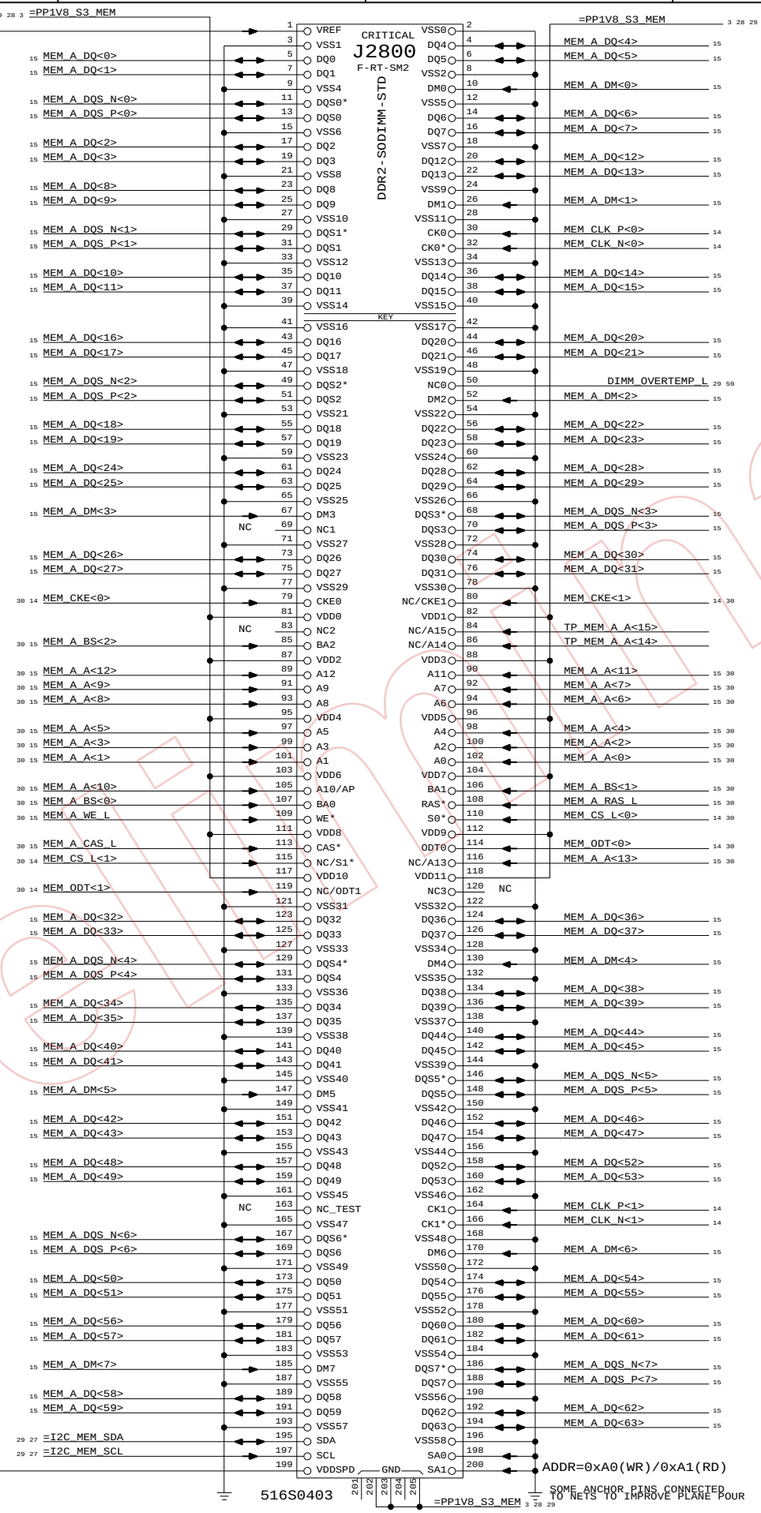
BOM options provided by this page:
(NONE)

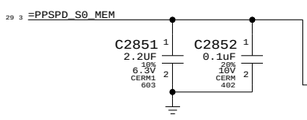
DDR2 VRef

One 0.1uF per connector



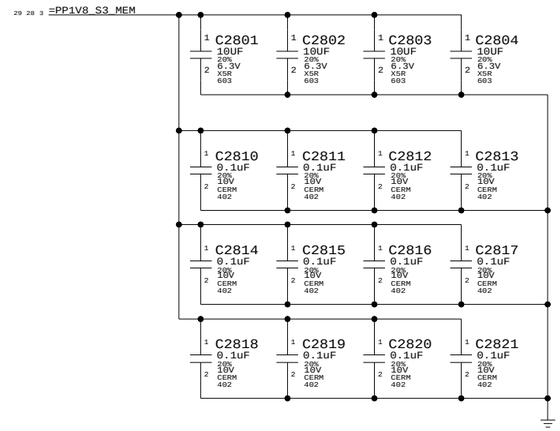






DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE SHT 28 OF 97

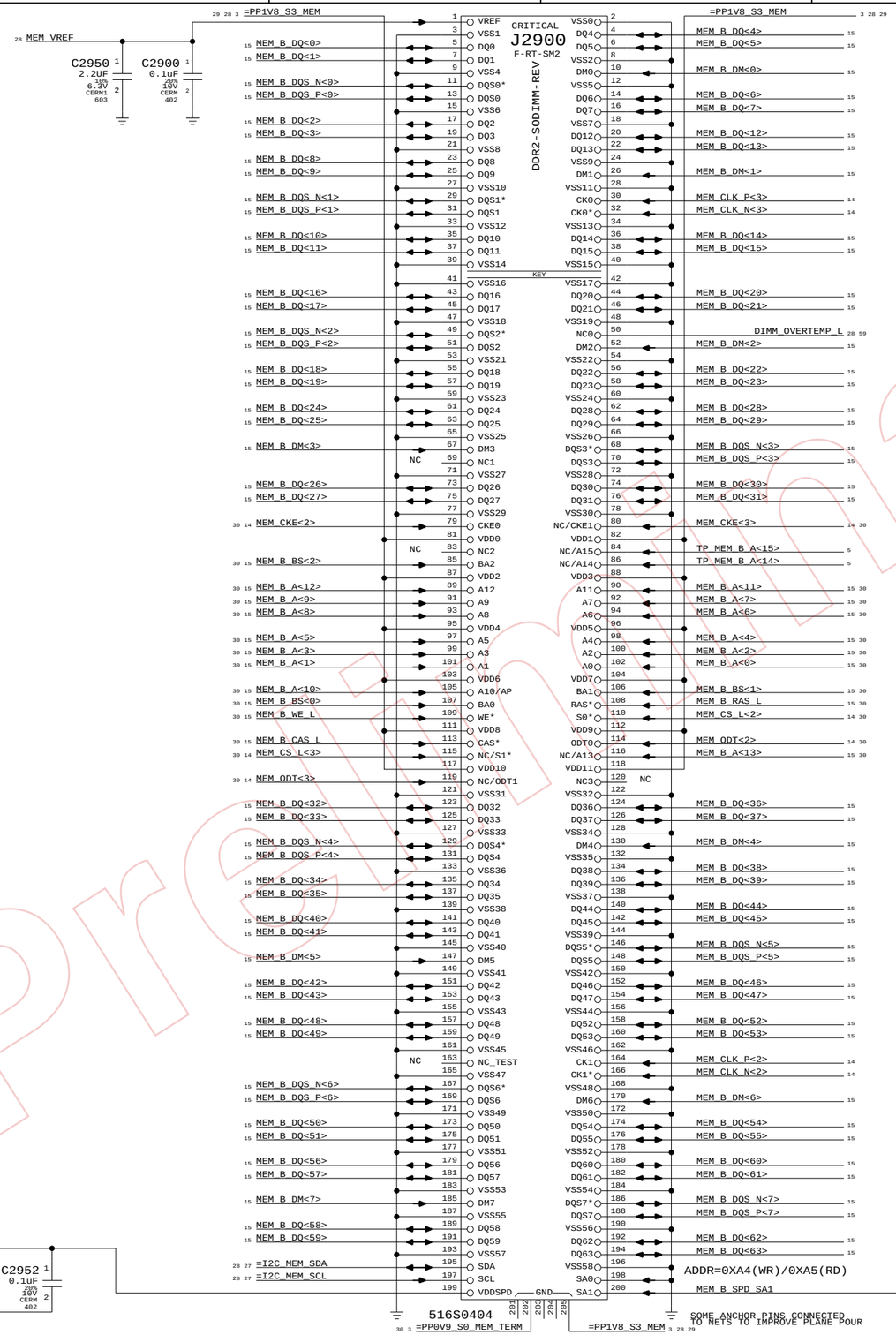
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

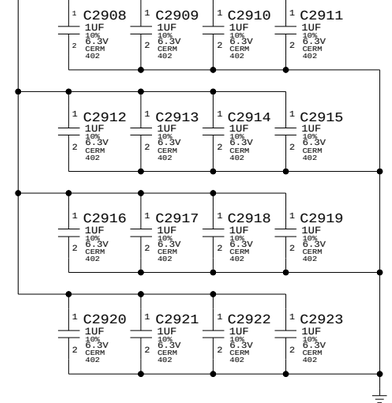
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

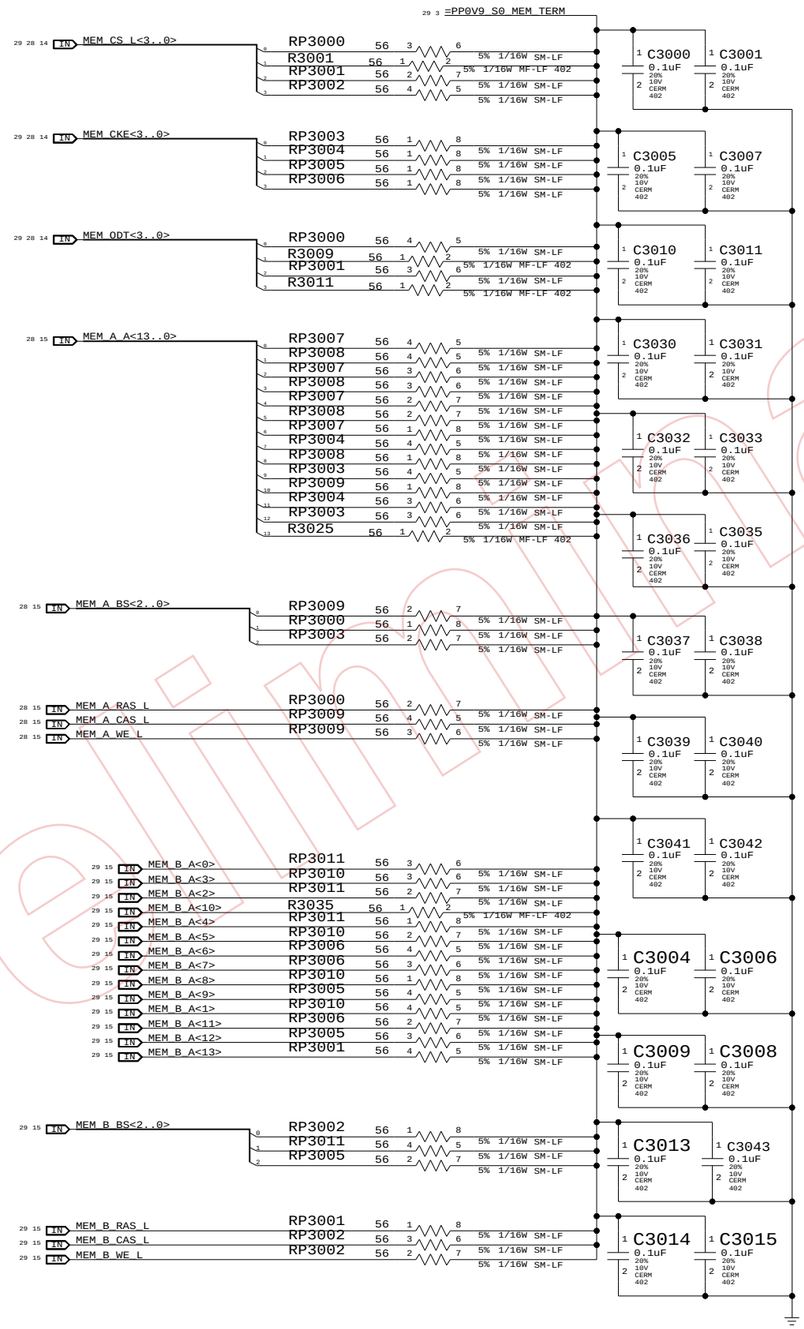
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 29 OF 97	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 30 OF 97	

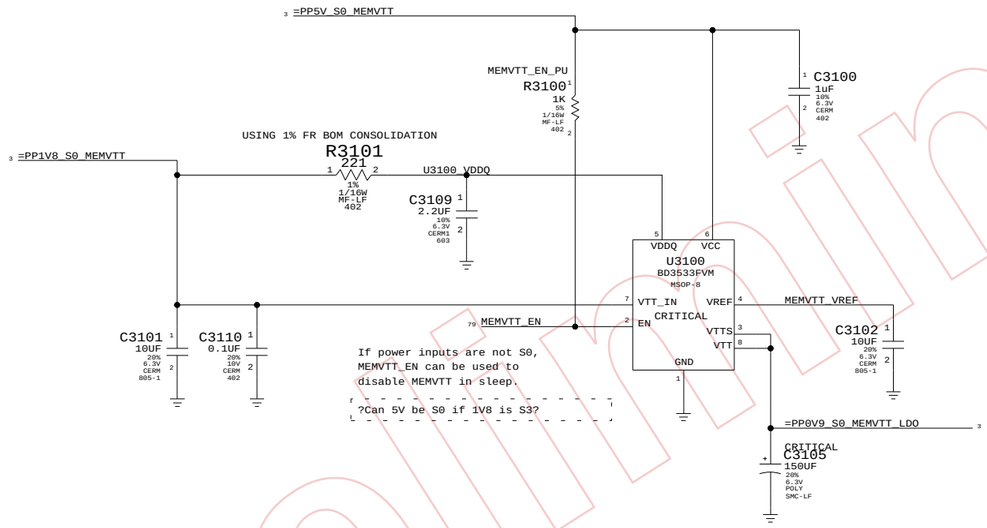
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

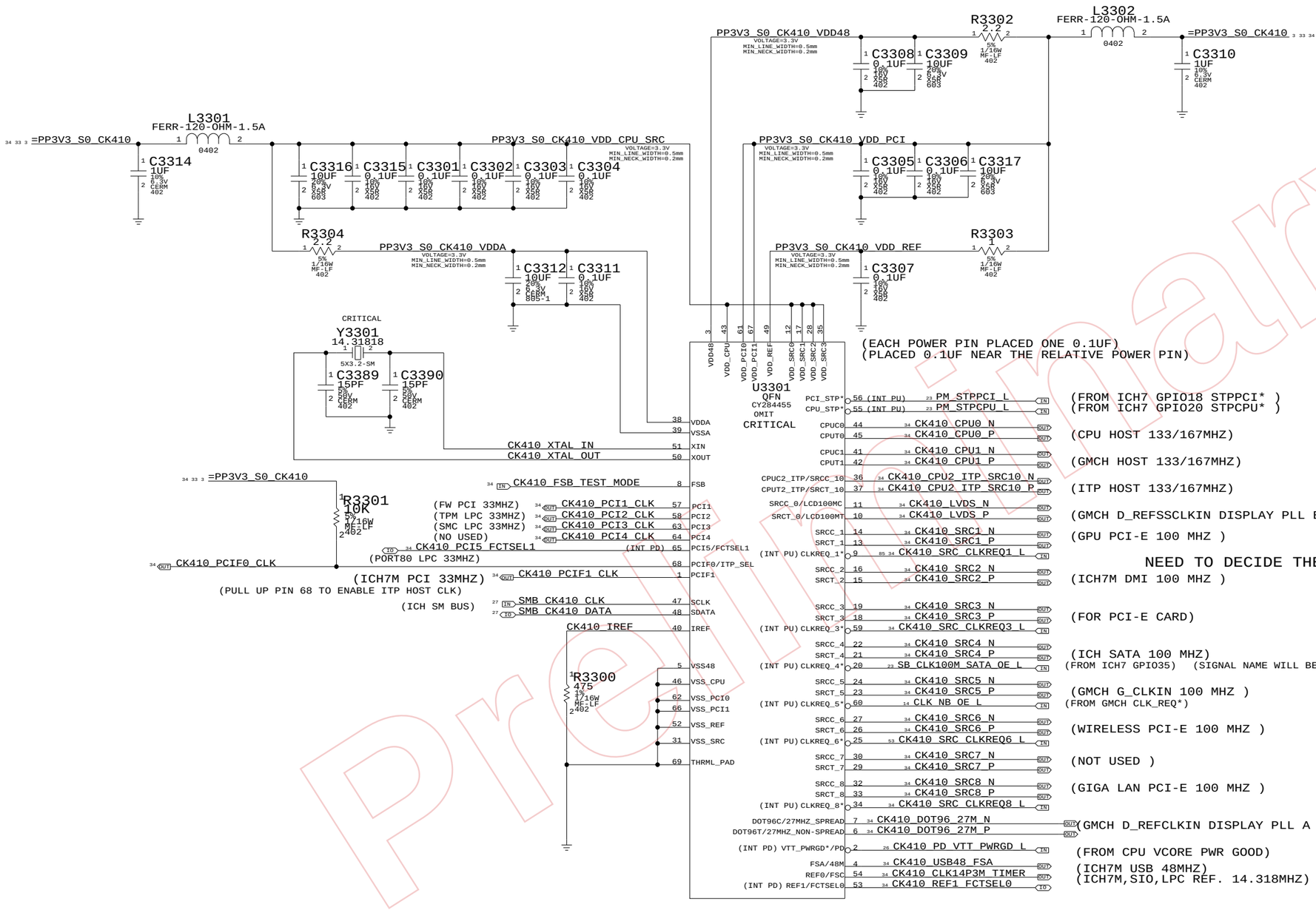
SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE

SHT 31 OF 97



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE NONE SHT 33 OF 97

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

80 34 5 3 PP1V05_S0

14 NB_BSEL<0> — R3453 1K 1/16W 5% MF-LF 402 — 34 CK410_FSA

R3455 1K 1/16W 5% MF-LF 402

NOSTUFF R3452 56 5% 1/16W MF-LF 402

R3454 0 5% 1/16W MF-LF 402

7 CPU_BSEL<0>

80 34 5 3 PP1V05_S0

14 NB_BSEL<1> — R3458 1K 1/16W 5% MF-LF 402 — 33 CK410_FSB_TEST_MODE

R3456 1K 5% 1/16W MF-LF 402

NOSTUFF R3457 0 5% 1/16W MF-LF 402

R3459 0 5% 1/16W MF-LF 402

7 CPU_BSEL<1>

80 34 5 3 PP1V05_S0

14 NB_BSEL<2> — R3462 1K 1/16W 5% MF-LF 402 — 34 CK410_FSC

R3460 1K 5% 1/16W MF-LF 402

NOSTUFF R3461 0 5% 1/16W MF-LF 402

R3463 0 5% 1/16W MF-LF 402

7 CPU_BSEL<2>

33 CK410_PCI5_FCTSEL1 — R3499 1K 1/16W 5% MF-LF 402 — =PP3V3_S0_CK410 3 33

R3497 2.2K 5% 1/16W MF-LF 402 — CK410_FSC 34

33 CK410_CLK14P3M_TIMER — R3498 33 1/16W 5% MF-LF 402 — SB_CLK14P3M_TIMER 5 23

33 CK410_REF1_FCTSEL0 — R3496 33 — TP_CLK14P3M_SPARE

R3451 2.2K 5% 1/16W MF-LF 402 — CK410_FSA 34

33 CK410_USB48_FSA — R3400 33 1/16W 5% MF-LF 402 — SB_CLK48M_USBCTLR 5 23

33 CK410_PCI4_CLK — R3406 33 — TP_PCI_CLK_SPARE

32 CK410_PCI3_CLK — R3405 33 — PCI_CLK_SMC 8 58

32 CK410_PCI2_CLK — R3404 33 NOSTUFF — PCI_CLK_TPM 67

33 CK410_PCI1_CLK — R3403 33 — PCI_CLK_FW 5 44

TPM CLOCK IS TURNED OFF IN SW AND RESISTOR NOSTUFF

32 CK410_PCIF1_CLK — R3401 33 — PCI_CLK_SB 5 22

32 CK410_PCIF0_CLK — R3402 33 — PCI_CLK_PORT80 5 60

33 CK410_CPU1_P — R3407 33 — 12 FSB_CLK_NB_P — R3429 1% 402 1/16W MF-LF 49.9

33 CK410_CPU1_N — R3408 33 — 12 FSB_CLK_NB_N — R3430 1% 402 1/16W MF-LF 49.9

33 CK410_CPU0_P — R3409 33 — 7 FSB_CLK_CPU_P — R3431 1% 402 1/16W MF-LF 49.9

33 CK410_CPU0_N — R3410 33 — 7 FSB_CLK_CPU_N — R3432 1% 402 1/16W MF-LF 49.9

33 CK410_CPU2_ITP_SRC10_P — R3411 33 — 11 5 CPU_XDP_CLK_P — MAKE_BASE=TRUE FSB_CLK_XDP_P — R3433 1% 402 1/16W MF-LF 49.9

33 CK410_CPU2_ITP_SRC10_N — R3412 33 — 11 5 CPU_XDP_CLK_N — FSB_CLK_XDP_N MAKE_BASE=TRUE — R3434 1% 402 1/16W MF-LF 49.9

33 CK410_SRC6_P — R3413 33 — 53 AIRPORT_CLK100M_PCIE_P — R3435 1% 402 1/16W MF-LF 49.9

33 CK410_SRC6_N — R3414 33 — 53 AIRPORT_CLK100M_PCIE_N — R3436 1% 402 1/16W MF-LF 49.9

33 CK410_SRC5_P — R3415 33 — 14 NB_CLK100M_GCLKIN_P — R3438 1% 402 1/16W MF-LF 49.9

33 CK410_SRC5_N — R3416 33 — 14 NB_CLK100M_GCLKIN_N — R3437 1% 402 1/16W MF-LF 49.9

33 CK410_SRC4_P — R3417 33 — 21 5 SB_CLK100M_SATA_P — R3439 1% 402 1/16W MF-LF 49.9

33 CK410_SRC4_N — R3418 33 — 21 5 SB_CLK100M_SATA_N — R3440 1% 402 1/16W MF-LF 49.9

33 CK410_SRC2_P — R3419 33 — 22 SB_CLK100M_DMI_P — R3442 1% 402 1/16W MF-LF 49.9

33 CK410_SRC2_N — R3420 33 — 22 SB_CLK100M_DMI_N — R3441 1% 402 1/16W MF-LF 49.9

33 CK410_SRC8_P — R3421 33 — 41 ENET_CLK100M_PCIE_P — R3443 1% 402 1/16W MF-LF 49.9

33 CK410_SRC8_N — R3422 33 — 41 ENET_CLK100M_PCIE_N — R3444 1% 402 1/16W MF-LF 49.9

33 CK410_SRC1_P — R3423 33 — 85 GPU_CLK100M_PCIE_P — R3446 1% 402 1/16W MF-LF 49.9

33 CK410_SRC1_N — R3424 33 — 85 GPU_CLK100M_PCIE_N — R3445 1% 402 1/16W MF-LF 49.9

33 CK410_LVDS_P — MAKE_BASE=TRUE — TP_CK410_LVDS_P

33 CK410_LVDS_N — MAKE_BASE=TRUE — TP_CK410_LVDS_N

33 CK410_DOT96_27M_N — MAKE_BASE=TRUE — TP_CK410_27M_SPREAD

33 CK410_DOT96_27M_P — MAKE_BASE=TRUE — TP_CK410_27M_NONSPREAD

R3492 33 — CK410_SRC3_P — SPARE_SRC3_P — R3488 49.9

R3491 33 — CK410_SRC3_N — SPARE_SRC3_N — R3487 49.9

R3490 33 — CK410_SRC7_P — SPARE_SRC7_P — R3486 49.9

R3489 33 — CK410_SRC7_N — SPARE_SRC7_N — R3485 49.9

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

85 33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) — R3495 NOSTUFF 1K

33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) — R3494 1K

33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) — R3493 1K

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MXM GRAPHICS CARD.

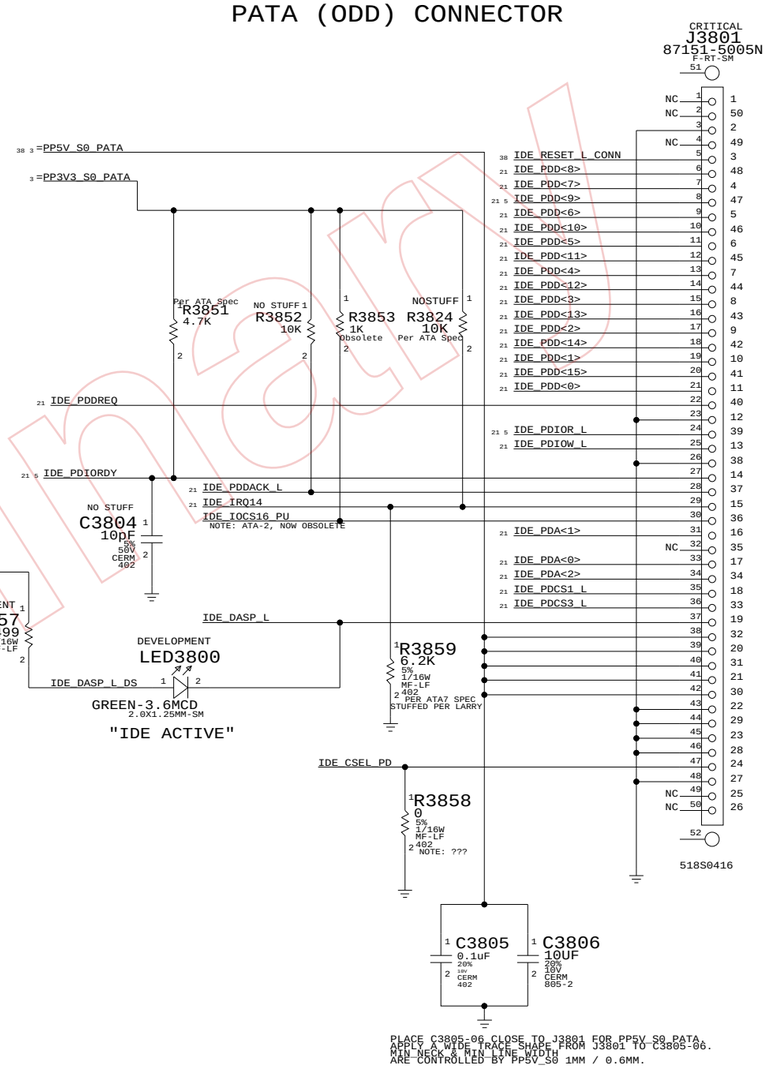
CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

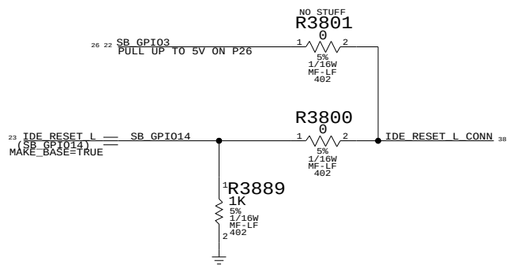
APPLE COMPUTER INC.

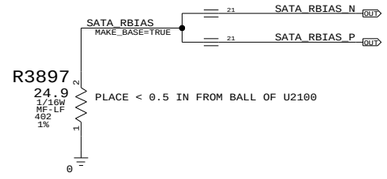
SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 34 OF 97	

PATA (ODD) CONNECTOR

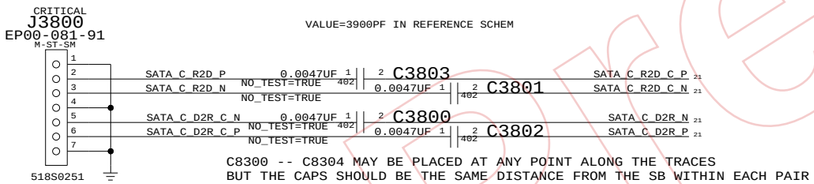


PLACE C3805-06 CLOSE TO J3801 FOR PP5V_S0_PATA.
APPLY A WIDE TRACE SHAPE FROM J3801 TO C3805-06.
MIN NECK & MIN LINE WIDTH
ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.

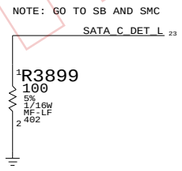


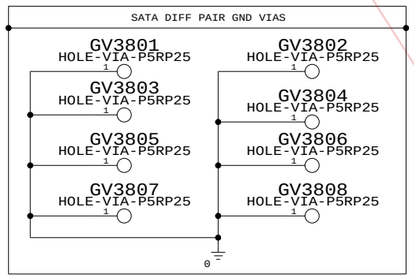


SATA CONNECTOR

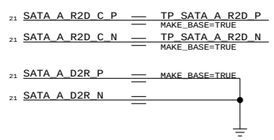


C8300 -- C8304 MAY BE PLACED AT ANY POINT ALONG THE TRACES
BUT THE CAPS SHOULD BE THE SAME DISTANCE FROM THE SB WITHIN EACH PAIR





SATA PORT 0 IS NOT USED

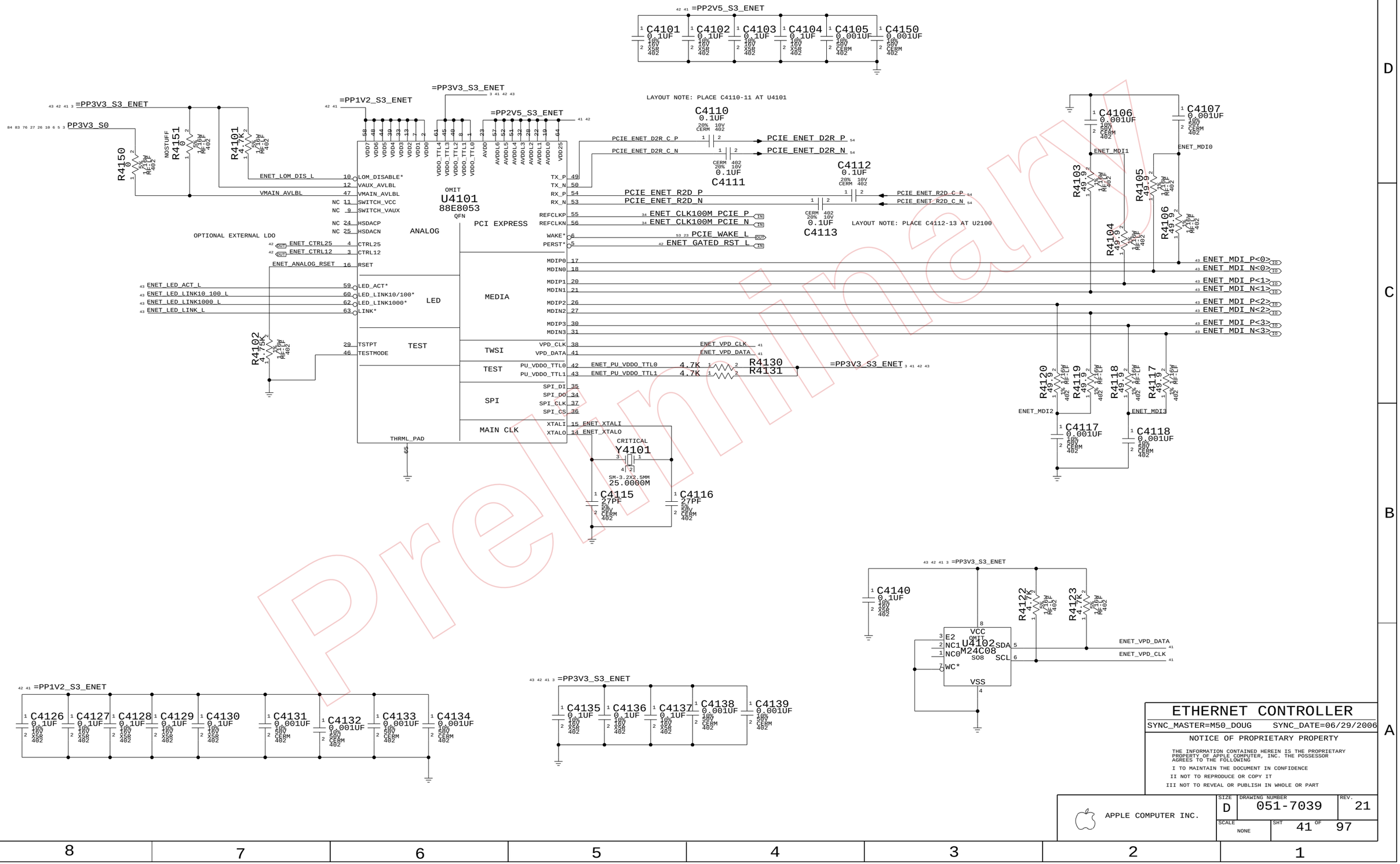


Disk Connectors

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 38 OF 97	

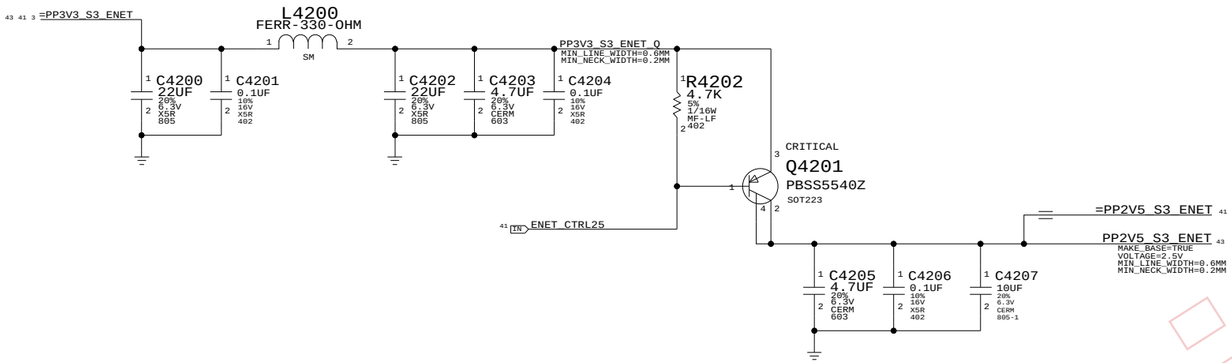


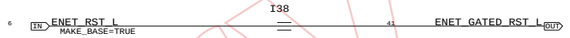
ETHERNET CONTROLLER

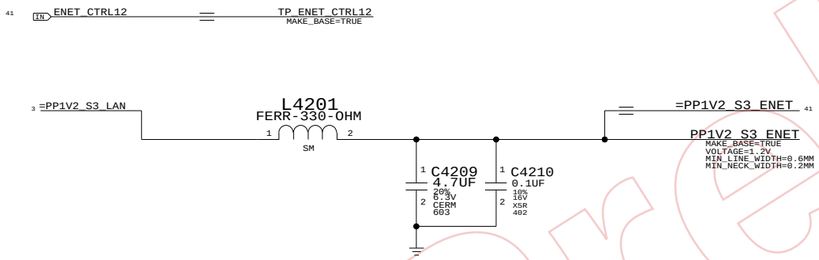
SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 41 OF 97	





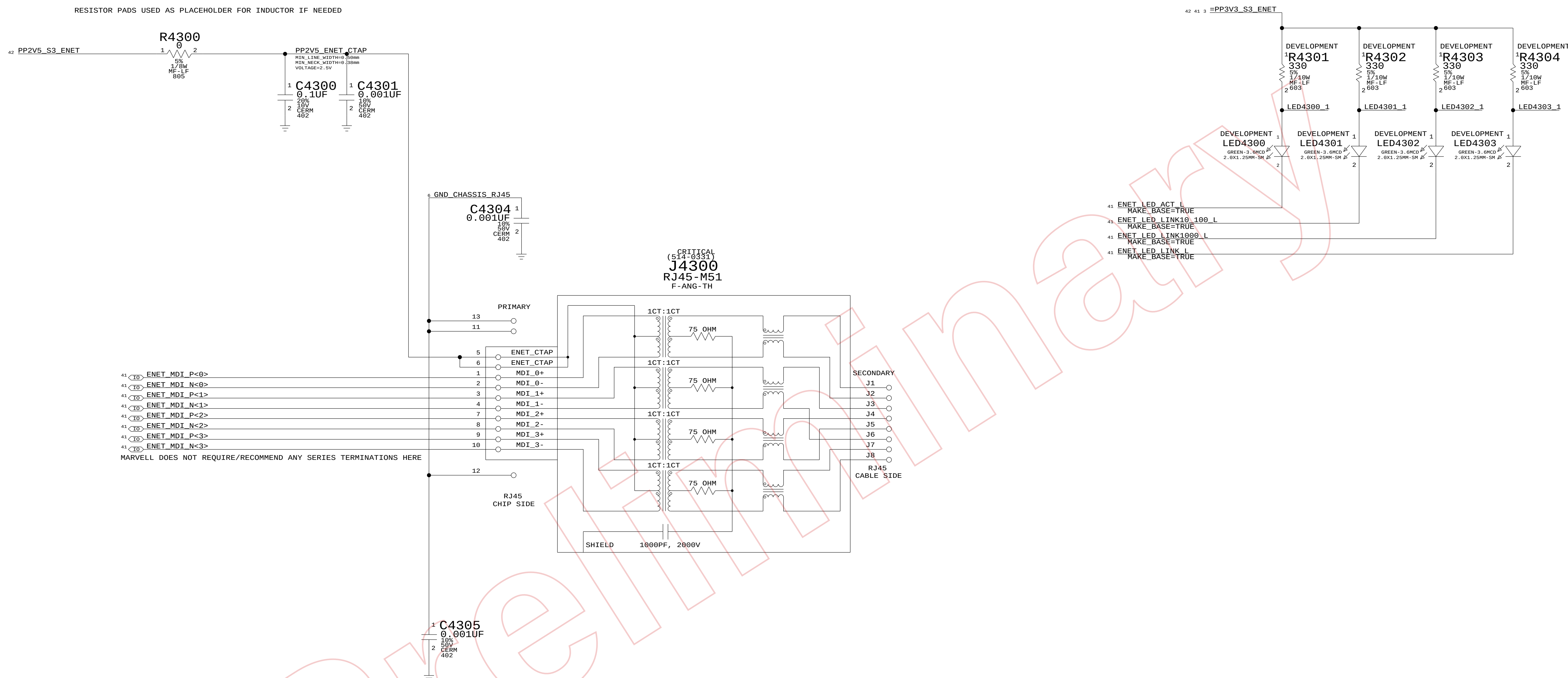


ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 42 OF 97	

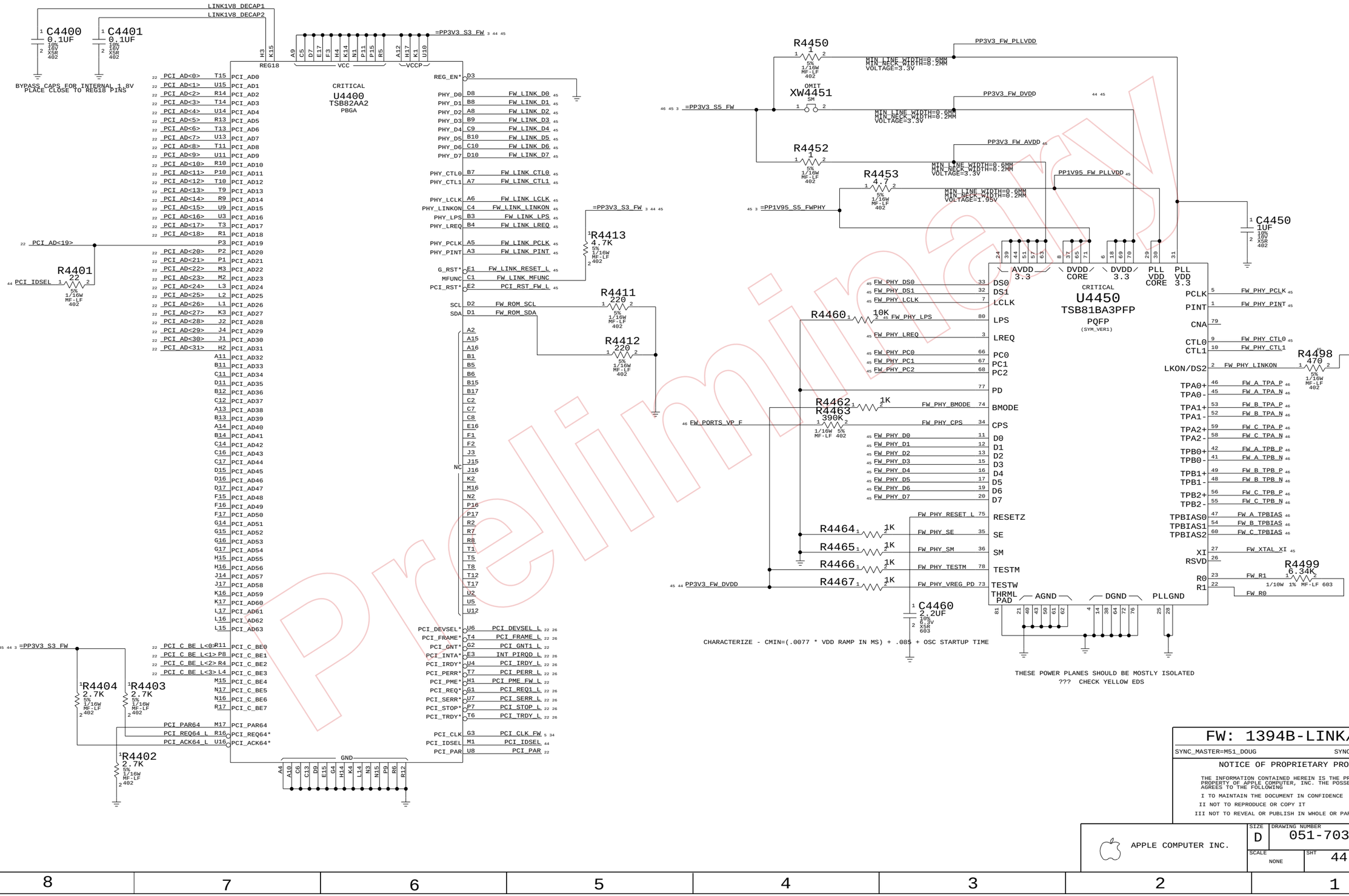

RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED
42 PP2V5_S3_ENET
R4300
0
5%
1/8W
MF-LF
805
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm
VOLTAGE=2.5V
C4300
0.1UF
20%
10V
CERM
402
C4301
0.001UF
10%
50V
CERM
402
6 GND_CHASSIS_RJ45
C4304
0.001UF
10%
50V
CERM
402
CRITICAL
(514-0331)
J4300
RJ45-M51
F-ANG-TH
PRIMARY
ENET_CTAP
ENET_CTAP
MDI_0+
MDI_0-
MDI_1+
MDI_1-
MDI_2+
MDI_2-
MDI_3+
MDI_3-
1CT:1CT
75 OHM
SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45
CABLE SIDE
RJ45
CHIP SIDE
SHIELD
1000PF, 2000V
41 ENET_MDI_P<0>
41 ENET_MDI_N<0>
41 ENET_MDI_P<1>
41 ENET_MDI_N<1>
41 ENET_MDI_P<2>
41 ENET_MDI_N<2>
41 ENET_MDI_P<3>
41 ENET_MDI_N<3>
MARVELL DOES NOT REQUIRE/RECOMMEND ANY SERIES TERMINATIONS HERE
C4305
0.001UF
10%
50V
CERM
402
42 41 3 =PP3V3_S3_ENET
DEVELOPMENT
R4301
330
DEVELOPMENT
R4302
330
DEVELOPMENT
R4303
330
DEVELOPMENT
R4304
330
5%
1/10W
MF-LF
603
LED4300_1
LED4301_1
LED4302_1
LED4303_1
DEVELOPMENT
LED4300
DEVELOPMENT
LED4301
DEVELOPMENT
LED4302
DEVELOPMENT
LED4303
GREEN-3.6MCD
2.0X1.25MM-SM
41 ENET_LED_ACT_L
MAKE_BASE=TRUE
41 ENET_LED_LINK10_100_L
MAKE_BASE=TRUE
41 ENET_LED_LINK1000_L
MAKE_BASE=TRUE
41 ENET_LED_LINK_L
MAKE_BASE=TRUE

ETHERNET CONNECTOR

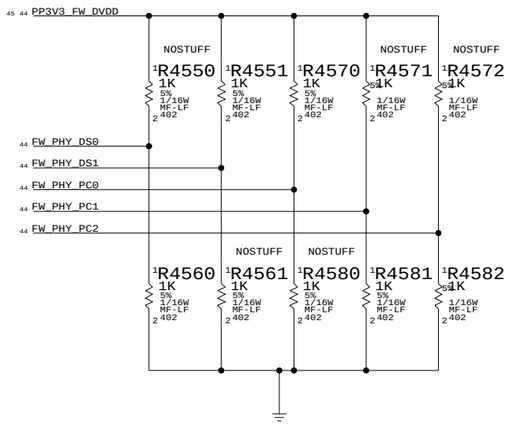
SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

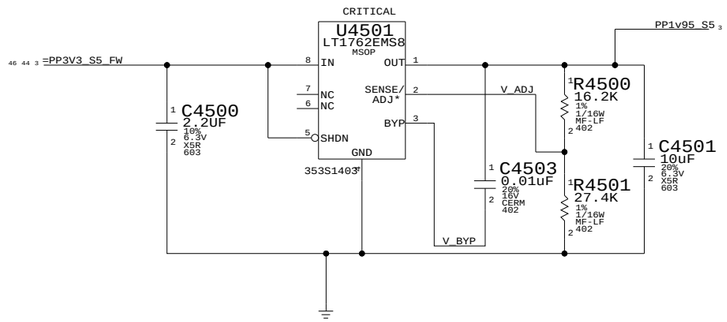
SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE NONE	SHT 43 OF 97	


LINK1V8_DECAP1
LINK1V8_DECAP2
C4400 0.1UF 10% 10V X5R 402
C4401 0.1UF 10% 10V X5R 402
BYPASS CAPS FOR INTERNAL 1.8V
PLACE CLOSE TO REG18 PINS
REG18
=PP3V3_S3_FW
VCC
VCCP
CRITICAL
U4400
TSB82AA2
PBGA
PCI_AD<0> T15 PCI_AD0
PCI_AD<1> U15 PCI_AD1
PCI_AD<2> R14 PCI_AD2
PCI_AD<3> T14 PCI_AD3
PCI_AD<4> U14 PCI_AD4
PCI_AD<5> R13 PCI_AD5
PCI_AD<6> T13 PCI_AD6
PCI_AD<7> U13 PCI_AD7
PCI_AD<8> T11 PCI_AD8
PCI_AD<9> U11 PCI_AD9
PCI_AD<10> R10 PCI_AD10
PCI_AD<11> P10 PCI_AD11
PCI_AD<12> T10 PCI_AD12
PCI_AD<13> T9 PCI_AD13
PCI_AD<14> R9 PCI_AD14
PCI_AD<15> U9 PCI_AD15
PCI_AD<16> U3 PCI_AD16
PCI_AD<17> T3 PCI_AD17
PCI_AD<18> R1 PCI_AD18
PCI_AD<19> P3 PCI_AD19
PCI_AD<20> P2 PCI_AD20
PCI_AD<21> P1 PCI_AD21
PCI_AD<22> M3 PCI_AD22
PCI_AD<23> M2 PCI_AD23
PCI_AD<24> L3 PCI_AD24
PCI_AD<25> L2 PCI_AD25
PCI_AD<26> L1 PCI_AD26
PCI_AD<27> K3 PCI_AD27
PCI_AD<28> J2 PCI_AD28
PCI_AD<29> J4 PCI_AD29
PCI_AD<30> J1 PCI_AD30
PCI_AD<31> H2 PCI_AD31
A11 PCI_AD32
B11 PCI_AD33
C11 PCI_AD34
D11 PCI_AD35
B12 PCI_AD36
C12 PCI_AD37
A13 PCI_AD38
B13 PCI_AD39
A14 PCI_AD40
B14 PCI_AD41
C14 PCI_AD42
C16 PCI_AD43
C17 PCI_AD44
D15 PCI_AD45
D16 PCI_AD46
D17 PCI_AD47
F15 PCI_AD48
F16 PCI_AD49
F17 PCI_AD50
G14 PCI_AD51
G15 PCI_AD52
G16 PCI_AD53
G17 PCI_AD54
H15 PCI_AD55
H16 PCI_AD56
J14 PCI_AD57
J17 PCI_AD58
K16 PCI_AD59
K17 PCI_AD60
L17 PCI_AD61
L16 PCI_AD62
L15 PCI_AD63
R4401 22 5% 1/16W MF-LF 402
PCI_IDSEL
REG_EN*
PHY_D0 FW_LINK_D0
PHY_D1 FW_LINK_D1
PHY_D2 FW_LINK_D2
PHY_D3 FW_LINK_D3
PHY_D4 FW_LINK_D4
PHY_D5 FW_LINK_D5
PHY_D6 FW_LINK_D6
PHY_D7 FW_LINK_D7
PHY_CTL0 FW_LINK_CTL0
PHY_CTL1 FW_LINK_CTL1
PHY_LCLK FW_LINK_LCLK
PHY_LINKON FW_LINK_LINKON
PHY_LPS FW_LINK_LPS
PHY_LREQ FW_LINK_LREQ
PHY_PCLK FW_LINK_PCLK
PHY_PINT FW_LINK_PINT
G_RST* FW_LINK_RESET_L
MFUNC FW_LINK_MFUNC
PCI_RST* PCI_RST_FW_L
R4413 4.7K 5% 1/16W MF-LF 402
R4411 220 5% 1/16W MF-LF 402
R4412 220 5% 1/16W MF-LF 402
SCL FW_ROM_SCL
SDA FW_ROM_SDA
NC
PCI_C_BE<0> R11 PCI_C_BE0
PCI_C_BE<1> P8 PCI_C_BE1
PCI_C_BE<2> R4 PCI_C_BE2
PCI_C_BE<3> L4 PCI_C_BE3
M15 PCI_C_BE4
N17 PCI_C_BE5
N16 PCI_C_BE6
R17 PCI_C_BE7
PCI_PAR64 M17 PCI_PAR64
PCI_REQ64_L R16 PCI_REQ64*
PCI_ACK64_L U16 PCI_ACK64*
R4404 2.7K 5% 1/16W MF-LF 402
R4403 2.7K 5% 1/16W MF-LF 402
R4402 2.7K 5% 1/16W MF-LF 402
GND
PCI_DEVSEL* U6 PCI_DEVSEL_L
PCI_FRAME* T4 PCI_FRAME_L
PCI_GNT* G2 PCI_GNT1_L
PCI_INTA* E3 INT_PIRQD_L
PCI_IRDY* U4 PCI_IRDY_L
PCI_PERR* T7 PCI_PERR_L
PCI_PME* H1 PCI_PME_FW_L
PCI_REQ* G1 PCI_REQ1_L
PCI_SERR* U7 PCI_SERR_L
PCI_STOP* P7 PCI_STOP_L
PCI_TRDY* T6 PCI_TRDY_L
PCI_CLK G3 PCI_CLK_FW
PCI_IDSEL M1 PCI_IDSEL
PCI_PAR U8 PCI_PAR
R4450 1 5% 1/10W MF-LF 402
PP3V3_FW_PLLVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
OMIT
XW4451
SM
=PP3V3_S5_FW
PP3V3_FW_DVDD
R4452 1 5% 1/10W MF-LF 402
PP3V3_FW_AVDD
R4453 4.7 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.95V
PP1V95_FW_PLLVDD
=PP1V95_S5_FWPHY
C4450 1UF 10% 10V X5R 402
AVDD 3.3
DVDD CORE
DVDD 3.3
PLL VDD CORE 3.3
PLL VDD 3.3
CRITICAL
U4450
TSB81BA3PFP
PQFP
(SYM_VER1)
R4460 10K
FW_PHY_DS0
FW_PHY_DS1
FW_PHY_LCLK
FW_PHY_LPS
FW_PHY_LREQ
FW_PHY_PC0
FW_PHY_PC1
FW_PHY_PC2
R4462 1K
R4463 390K 5% 1/16W MF-LF 402
FW_PHY_BMODE
FW_PHY_CPS
FW_PORTS_VP_F
FW_PHY_D0
FW_PHY_D1
FW_PHY_D2
FW_PHY_D3
FW_PHY_D4
FW_PHY_D5
FW_PHY_D6
FW_PHY_D7
FW_PHY_RESET_L
R4464 1K
R4465 1K
R4466 1K
R4467 1K
FW_PHY_SE
FW_PHY_SM
FW_PHY_TESTM
FW_PHY_VREG_PD
PP3V3_FW_DVDD
C4460 2.2UF 10% 6.3V X5R 603
CHARACTERIZE - CMIN=(.0077 * VDD RAMP IN MS) + .085 + OSC STARTUP TIME
DS0
DS1
LCLK
LPS
LREQ
PC0
PC1
PC2
PD
BMODE
CPS
D0
D1
D2
D3
D4
D5
D6
D7
RESETZ
SE
SM
TESTM
TESTW
THRML PAD
AGND
DGND
PLLGND
PCLK FW_PHY_PCLK
PINT FW_PHY_PINT
CNA
CTL0 FW_PHY_CTL0
CTL1 FW_PHY_CTL1
LKON/DS2 FW_PHY_LINKON
R4498 470 5% 1/10W MF-LF 402
TPA0+ FW_A_TPA_P
TPA0- FW_A_TPA_N
TPA1+ FW_B_TPA_P
TPA1- FW_B_TPA_N
TPA2+ FW_C_TPA_P
TPA2- FW_C_TPA_N
TPB0+ FW_A_TPB_P
TPB0- FW_A_TPB_N
TPB1+ FW_B_TPB_P
TPB1- FW_B_TPB_N
TPB2+ FW_C_TPB_P
TPB2- FW_C_TPB_N
TPBIAS0 FW_A_TPBIAS
TPBIAS1 FW_B_TPBIAS
TPBIAS2 FW_C_TPBIAS
XI FW_XTAL_XI
RSVD
R0 FW_R1
R1 FW_R0
R4499 6.34K 1/10W 1% MF-LF 603
THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
??? CHECK YELLOW EDS
FW: 1394B-LINK/PHY
SYNC_MASTER=M51_DOUG
SYNC_DATE=06/29/2006
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7039
REV. 21
SCALE NONE
SHT 44 OF 97

1394 PHY DATA/STROBE AND POWER CLASS OPTIONS



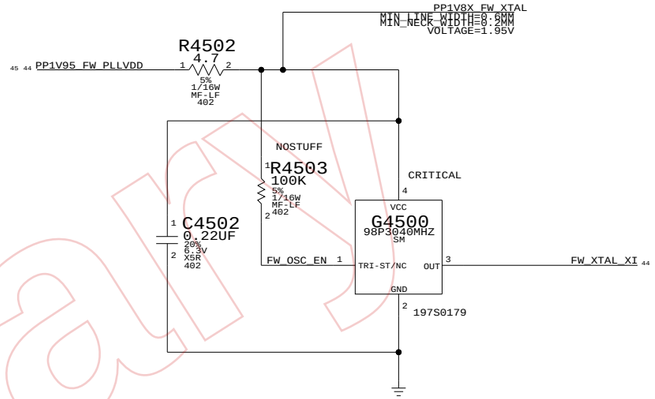
1394 PHY 1.95V REGULATOR



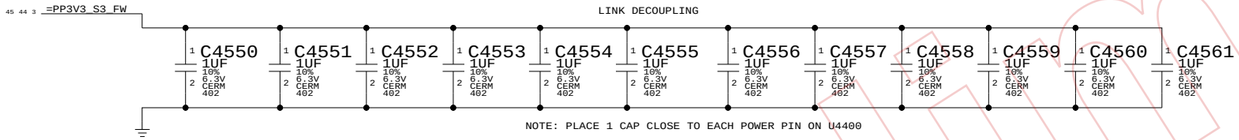
VOUT = 1.22V * (1 + R4500 / R4501) + (Iadj * R4500)
Iadj = 30nA @ 25 deg C
VOUT = 1.946V

1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION

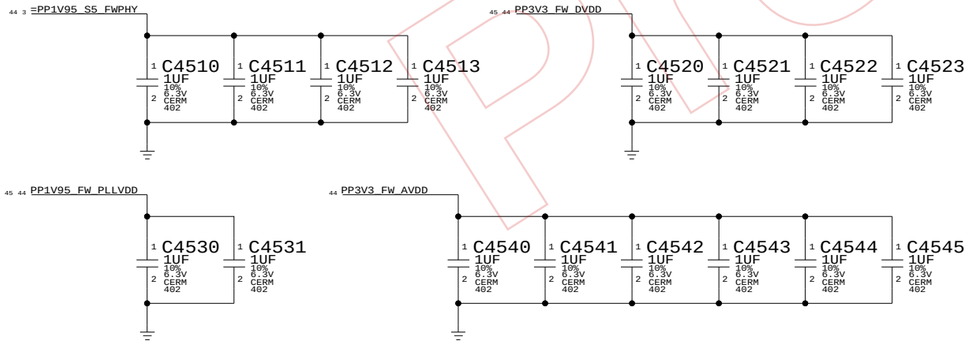


LINK DECOUPLING



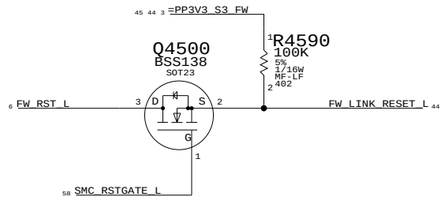
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

PHY DECOUPLING



NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

1394 LINK POWER ON RESET AND PCI RESET



NOTE: 1% FOR BOM CONSOLIDATION(APPLIED TO M50)
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT

44 FW_LINK_D0 MAKE_BASE=TRUE	=	FW_PHY_D0 44
44 FW_LINK_D1 MAKE_BASE=TRUE	=	FW_PHY_D1 44
44 FW_LINK_D2 MAKE_BASE=TRUE	=	FW_PHY_D2 44
44 FW_LINK_D3 MAKE_BASE=TRUE	=	FW_PHY_D3 44
44 FW_LINK_D4 MAKE_BASE=TRUE	=	FW_PHY_D4 44
44 FW_LINK_D5 MAKE_BASE=TRUE	=	FW_PHY_D5 44
44 FW_LINK_D6 MAKE_BASE=TRUE	=	FW_PHY_D6 44
44 FW_LINK_D7 MAKE_BASE=TRUE	=	FW_PHY_D7 44
44 FW_LINK_CTL0 MAKE_BASE=TRUE	=	FW_PHY_CTL0 44
44 FW_LINK_CTL1 MAKE_BASE=TRUE	=	FW_PHY_CTL1 44
44 FW_LINK_LCLK MAKE_BASE=TRUE	=	FW_PHY_LCLK 44
44 FW_LINK_LPS MAKE_BASE=TRUE	=	FW_PHY_LPS 44
44 FW_LINK_LREQ MAKE_BASE=TRUE	=	FW_PHY_LREQ 44
44 FW_LINK_PCLK MAKE_BASE=TRUE	=	FW_PHY_PCLK 44
44 FW_LINK_LINKON	R4520 1K	FW_PHY_LINKON 44
44 FW_LINK_PINT MAKE_BASE=TRUE	=	FW_PHY_PINT 44

NOTE: 1K IS PER TI SPEC TO BALANCE OUT THE 470 PULLUP ON DS2

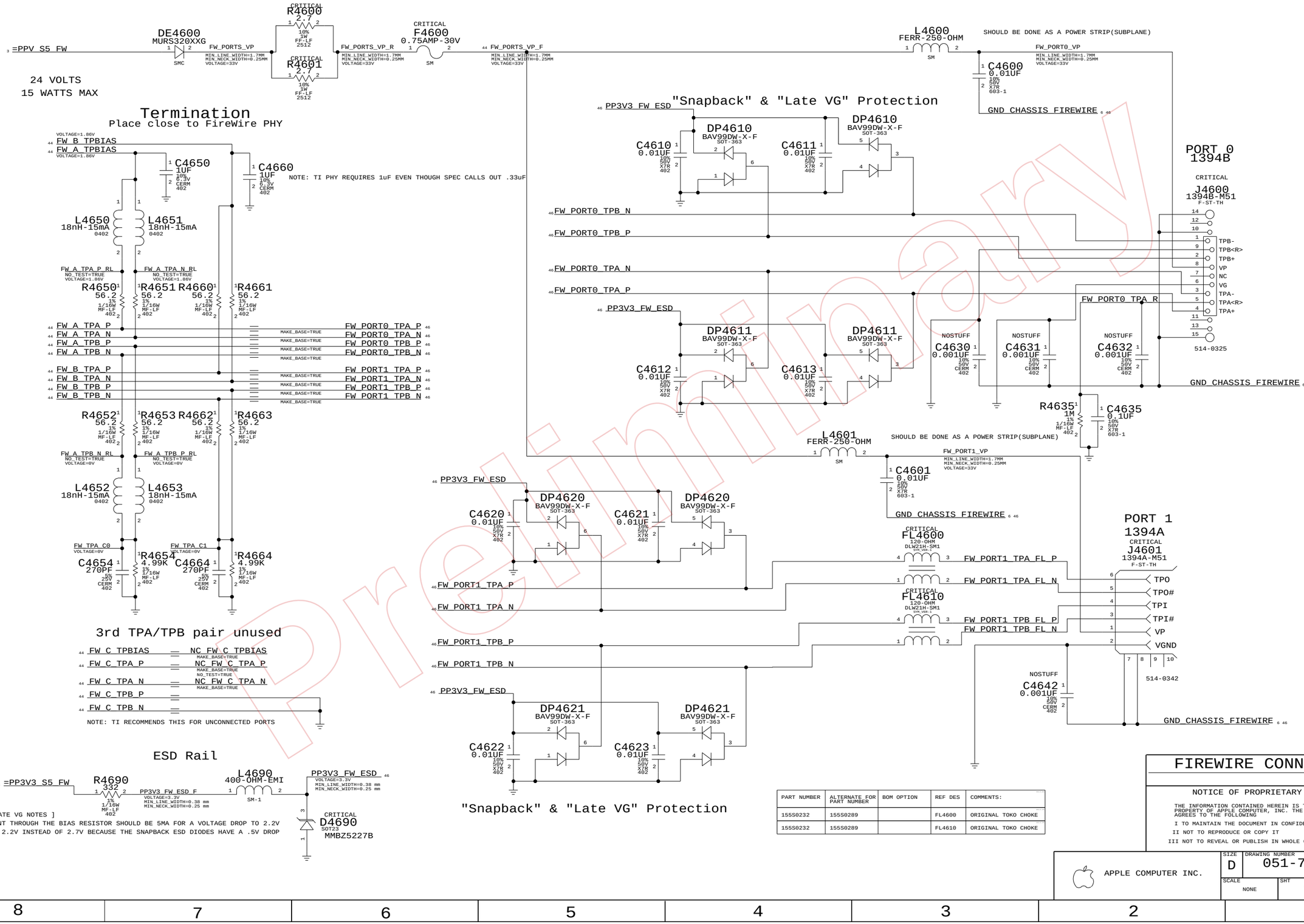
NORMALLY TERMINATIONS WOULD GO HERE...
SIMULATIONS SHOW THAT THERMINATIONS WERE NOT NEEDED FOR M51
CONSTRAIN NETS TO 200-250PS IF NO TERM-Rs...

FW: 1394B MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 45 OF 97	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

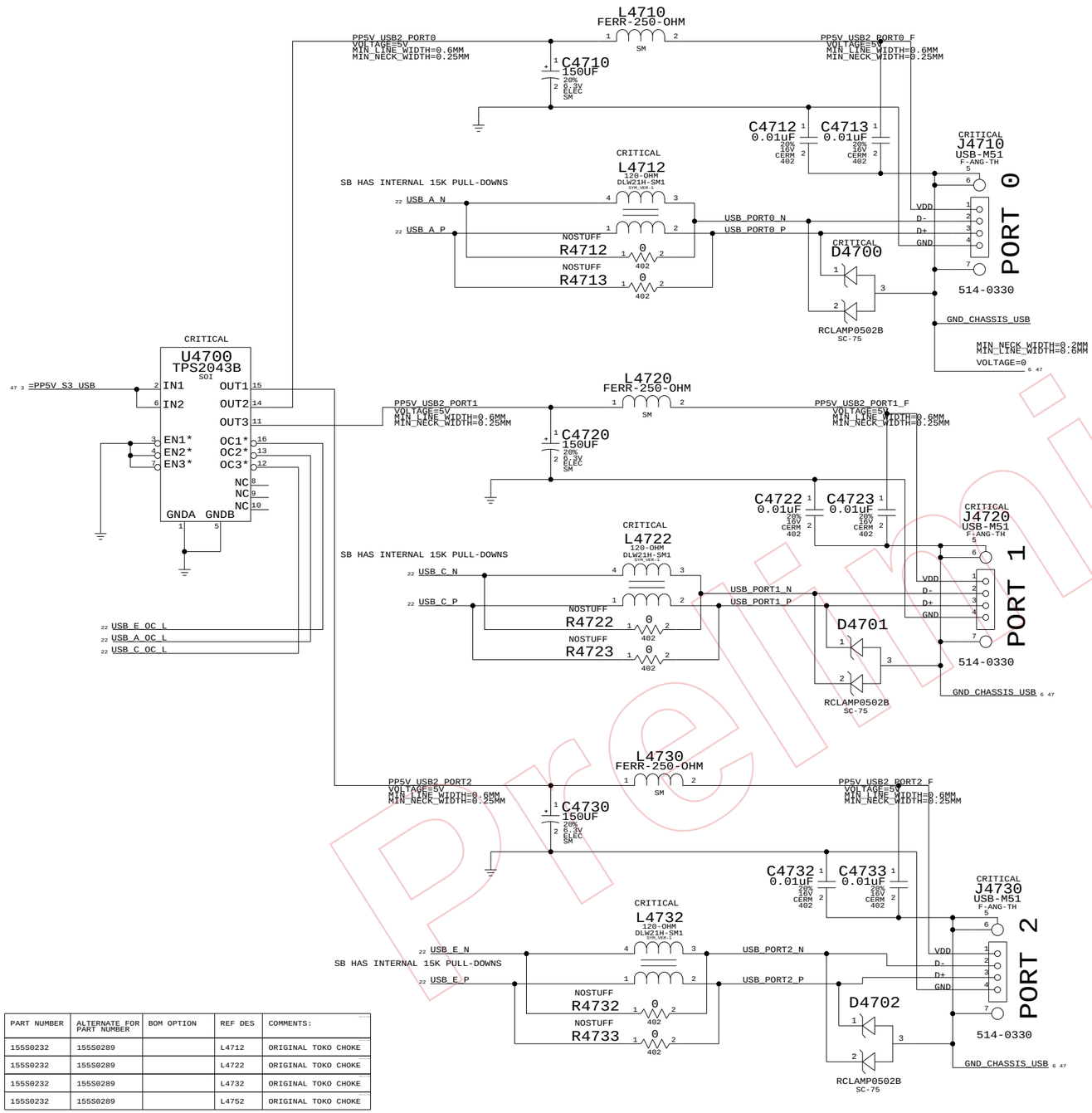
FIREWIRE CONNECTORS

APPLE COMPUTER INC.

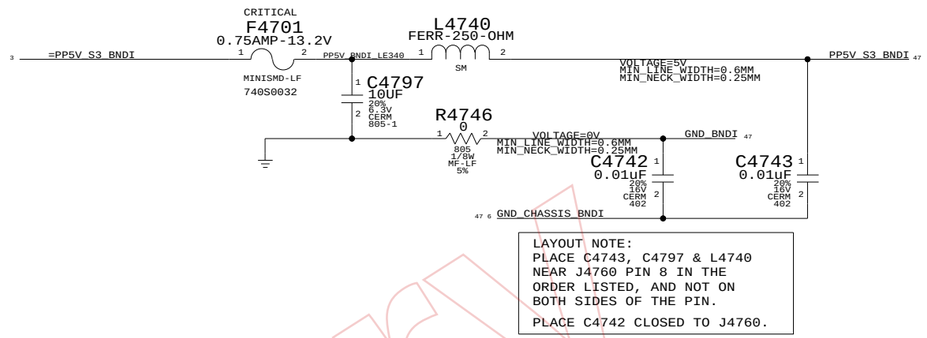
SIZE D | DRAWING NUMBER 051-7039 | REV. 21

SCALE NONE | SHT 46 OF 97

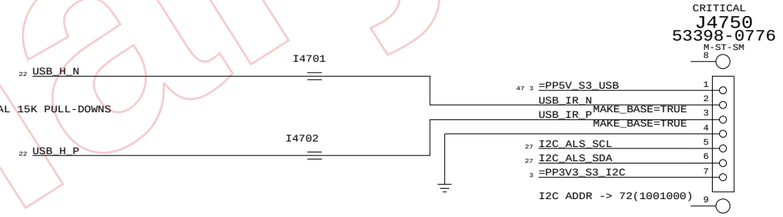
External USB Ports



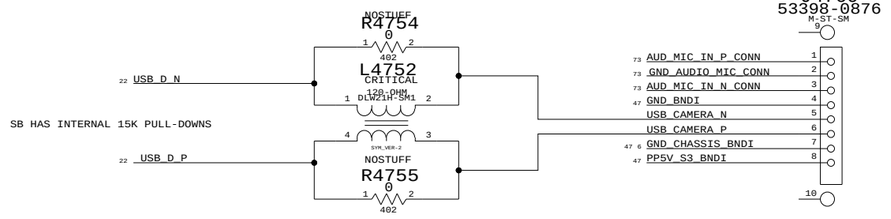
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE



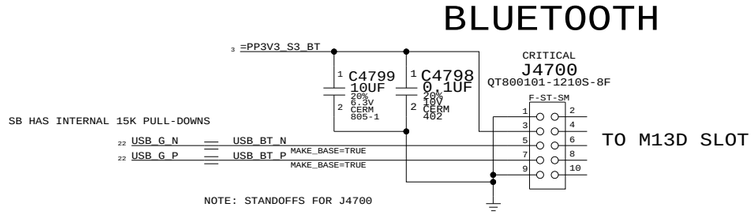
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



CRITICAL
SDF4700
STDOFF-40D4.5H-1.35-TH

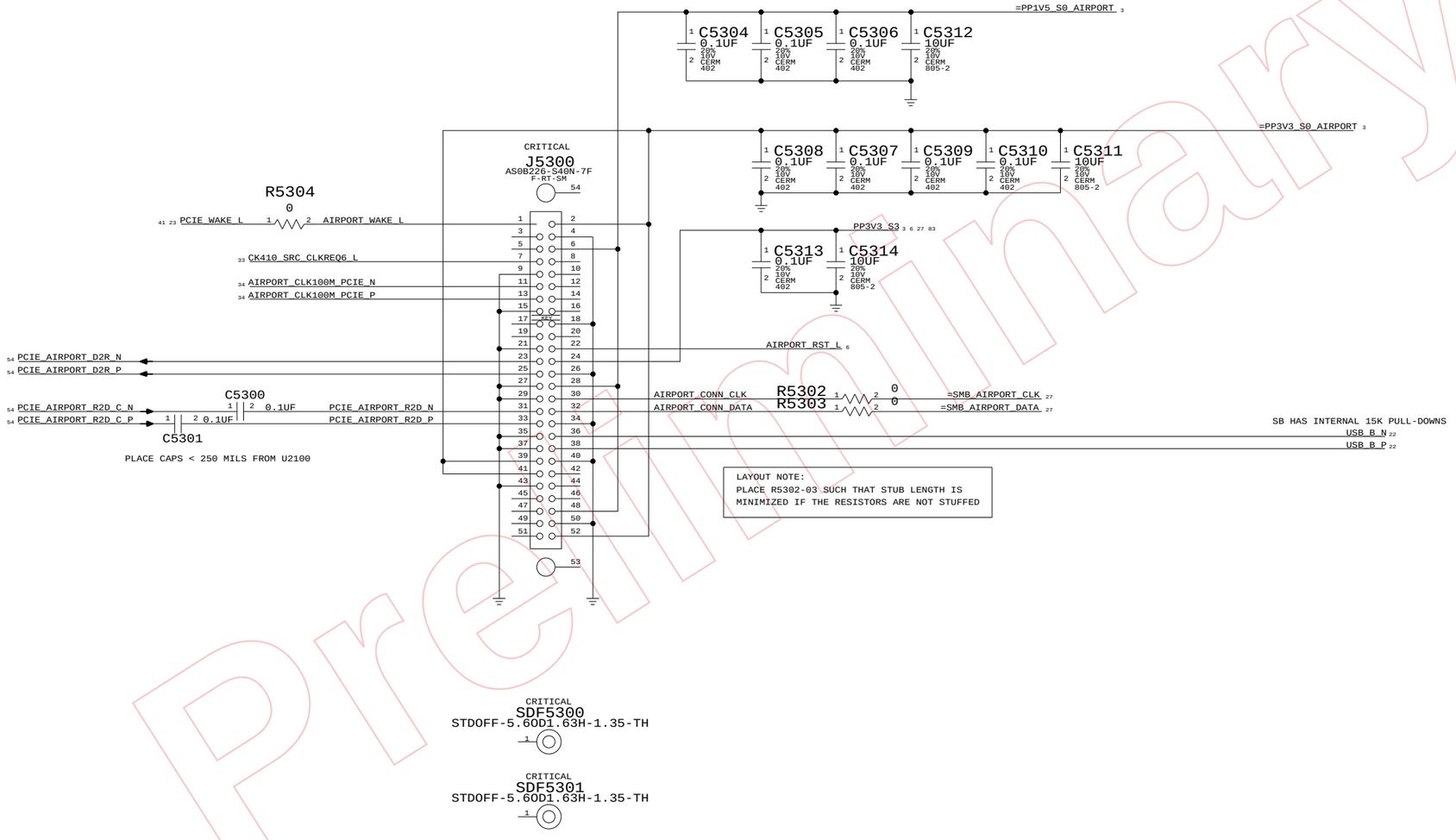
CRITICAL
SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 47 OF 97	



AIRPORT CONN

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 53 OF 97	

PCI-E X1 PORT "A" = ETHERNET (YUKON)

22 PCIE_A_R2D_C_N — PCIE_ENET_R2D_C_N 41
MAKE_BASE=TRUE
22 PCIE_A_R2D_C_P — PCIE_ENET_R2D_C_P 41
MAKE_BASE=TRUE

22 PCIE_A_D2R_N — PCIE_ENET_D2R_N 41
MAKE_BASE=TRUE
22 PCIE_A_D2R_P — PCIE_ENET_D2R_P 41
MAKE_BASE=TRUE

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)

22 PCIE_B_R2D_C_N — PCIE_AIRPORT_R2D_C_N 53
MAKE_BASE=TRUE
22 PCIE_B_R2D_C_P — PCIE_AIRPORT_R2D_C_P 53
MAKE_BASE=TRUE

22 5 PCIE_B_D2R_N — PCIE_AIRPORT_D2R_N 53
MAKE_BASE=TRUE
22 5 PCIE_B_D2R_P — PCIE_AIRPORT_D2R_P 53
MAKE_BASE=TRUE

PCI-E X1 PORTS C, D, E, F = UNUSED

22 PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_C_D2R_N — TP_PCIE_C_D2R_N
MAKE_BASE=TRUE
22 PCIE_C_D2R_P — TP_PCIE_C_D2R_P
MAKE_BASE=TRUE

22 PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_D_D2R_N — TP_PCIE_D_D2R_N
MAKE_BASE=TRUE
22 PCIE_D_D2R_P — TP_PCIE_D_D2R_P
MAKE_BASE=TRUE

22 PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P
MAKE_BASE=TRUE

22 PCIE_E_D2R_N — TP_PCIE_E_D2R_N
MAKE_BASE=TRUE
22 PCIE_E_D2R_P — TP_PCIE_E_D2R_P
MAKE_BASE=TRUE

22 PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N
MAKE_BASE=TRUE
22 PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P
MAKE_BASE=TRUE

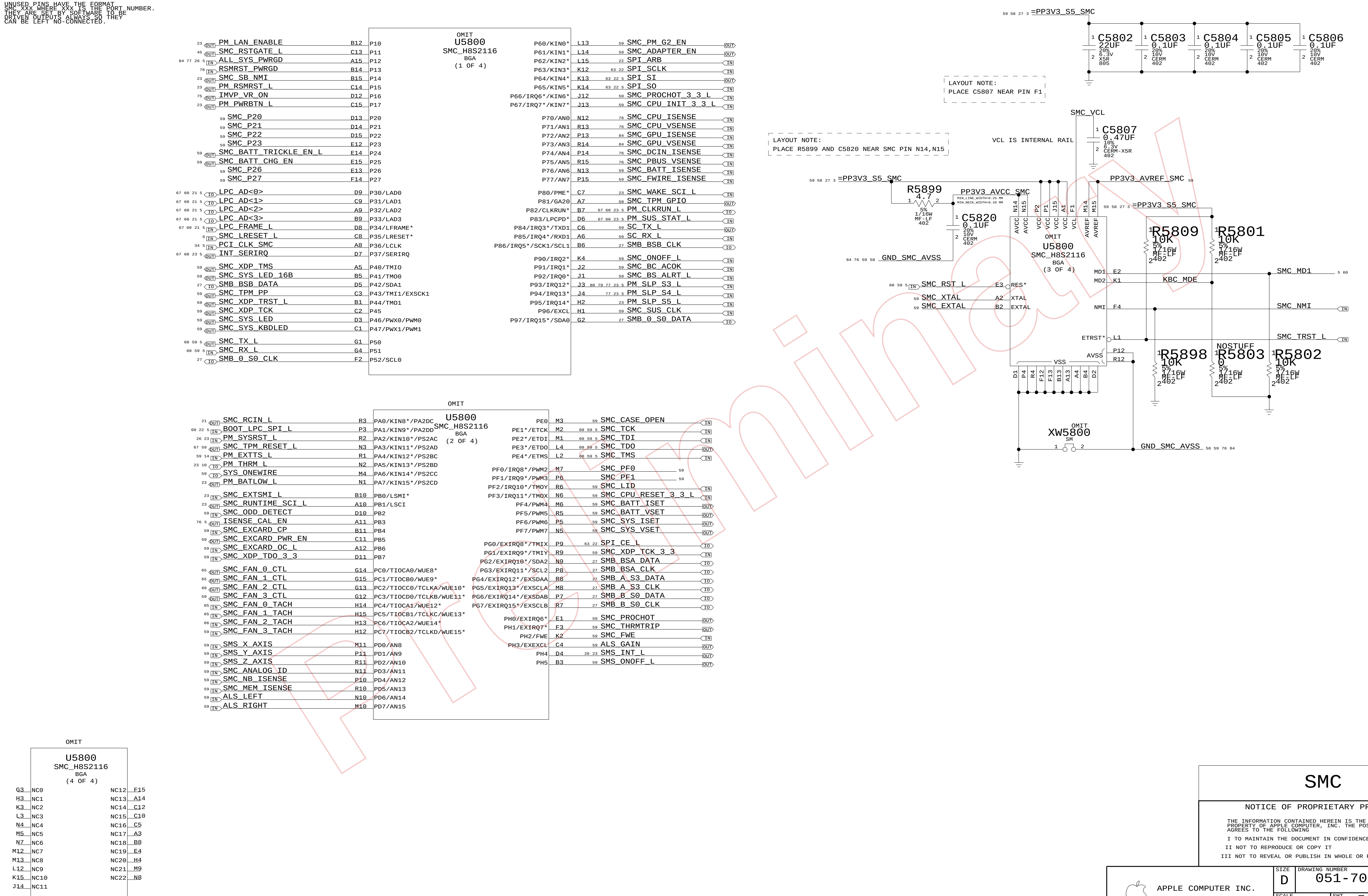
22 PCIE_F_D2R_N — TP_PCIE_F_D2R_N
MAKE_BASE=TRUE
22 PCIE_F_D2R_P — TP_PCIE_F_D2R_P
MAKE_BASE=TRUE

PCI-E CONNECTIONS

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 54 OF 97	



SMC

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

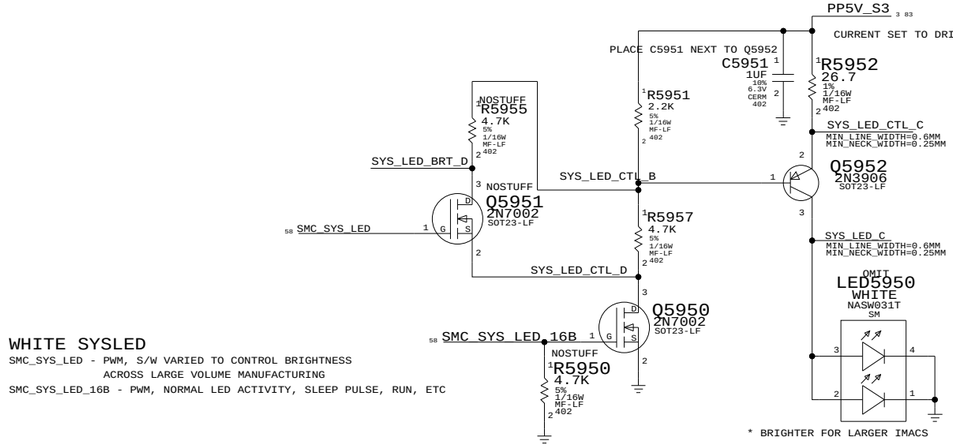
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

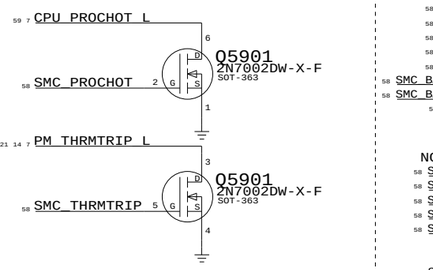
SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE NONE	SHT 58 OF 97	



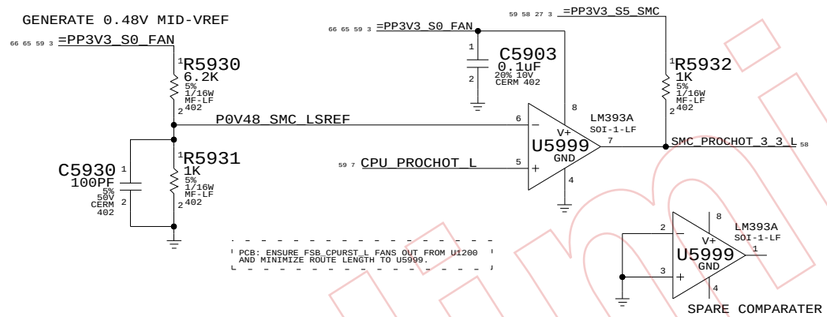
WHITE SYSLED

SMC_SYS_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS
ACROSS LARGE VOLUME MANUFACTURING
SMC_SYS_LED_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC

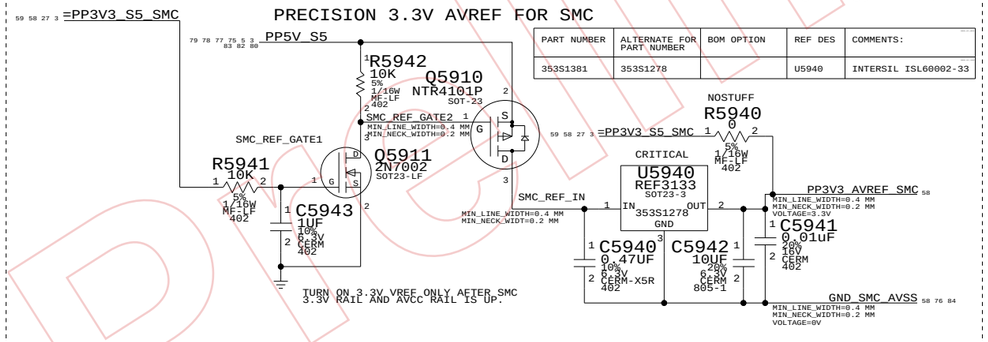
SMC 3.3V -> CPU 1.05V SHIFTER



CPU 1.05V -> SMC 3.3V SHIFTER

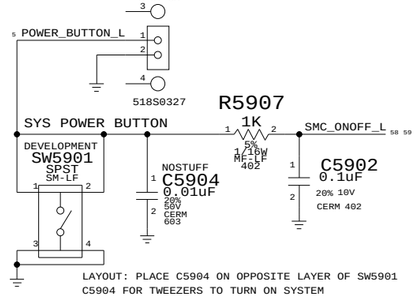


PRECISION 3.3V AVREF FOR SMC



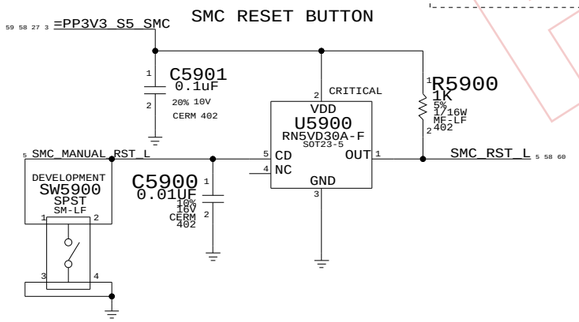
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	INTERSIL ISL60002-33

POWER BUTTON HEADER

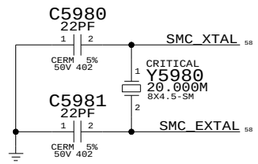


LAYOUT: PLACE C5904 ON OPPOSITE LAYER OF SW5901
C5904 FOR TWEEZERS TO TURN ON SYSTEM
* NEVER STUFF C5904

SMC RESET BUTTON

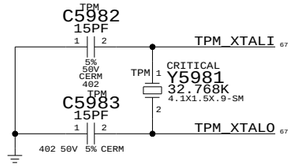


SMC CRYSTAL



TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20	MAKE_BASE=TRUE
SMC_P21	NC_SMC_P21	MAKE_BASE=TRUE
SMC_P22	NC_SMC_P22	MAKE_BASE=TRUE
SMC_P23	NC_SMC_P23	MAKE_BASE=TRUE
SMC_P26	NC_SMC_P26	MAKE_BASE=TRUE
SMC_P27	NC_SMC_P27	MAKE_BASE=TRUE
SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE
SMC_PM_G2_EN	TP_PM_G2_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE, FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE
SMC_XDP_TCK	TP_SMC_XDP_TCK	MAKE_BASE=TRUE
SMC_XDP_TRST_L	TP_SMC_XDP_TRST_L	MAKE_BASE=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE, FUNC_TEST=TRUE

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_NB_ISENSE	NC_SMC_NB_ISENSE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE

SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE, FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE, FUNC_TEST=TRUE

SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE

UNUSED_SMC_SENSE — 10K — R5924 5% 1/16W MF-LF

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS & PULL-DOWNS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K
SMC_LID	R5916	10K
SMC_EXCARD_OC_L	R5831	10K
SMC_XDP_TCK_3_3	R5934	1K
SMC_CPU_RESET_3_3_L	R5933	1K
SMC_EXCARD_CP	R5830	10K
SMC_CASE_OPEN	R5917	10K

TPM RESET PULLUP

SMC_TPM_RESET_L — R5827 10K — PP3V3_TPM_3VSB

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE

SC_RX_L — 0 R5922 — SMC_RX_L

SC_TX_L — 0 R5923 — SMC_TX_L

POWER SUPPLY TEMP SENSE

SMC_ANALOG_ID — ACDC_TEMP (MAKE_BASE=TRUE)

SELECT TPM GPIO

SMC_TPM_GPIO — 0 R5920 SMC_TPM_GPIO1 — TPM_GPIO1; 0 R5921 SMC_TPM_GPIO2 — TPM_GPIO2

5% 1/16W MF-LF 402

HDD ACTIVITY MONITOR

PP5V_S0

M51: FOLLOWED M50, NOT CONNECTING TO SMC, AND TERMINATING

SMC_TPM_PP — 0 R5995 — TPM_PP

TP_SB_SATALED_L — PU_HDD_ACTIVITY_LED — R5960 10K (MAKE_BASE=TRUE)

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO_DIFFERENTIALLY NEXT TO THIS END TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM — GND_NEXT_TO_SMC — OMIT

M51 SPECIFIC: GPU MONITORING SIGNALS

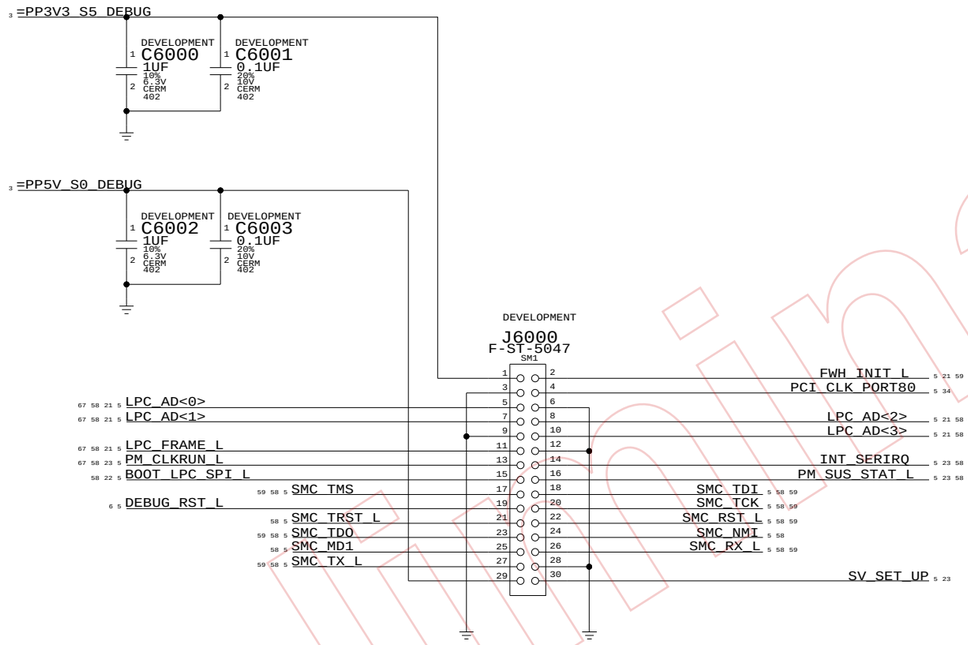
I327 SMC_XDP_TMS	MXM_AC_BATT_L	MAKE_BASE=TRUE
I328 SMC_XDP_TDO_3_3	GPU_OVERTEMP_L	MAKE_BASE=TRUE

SMC & TPM SUPPORT

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 59 OF 97	



LPC+ CONN

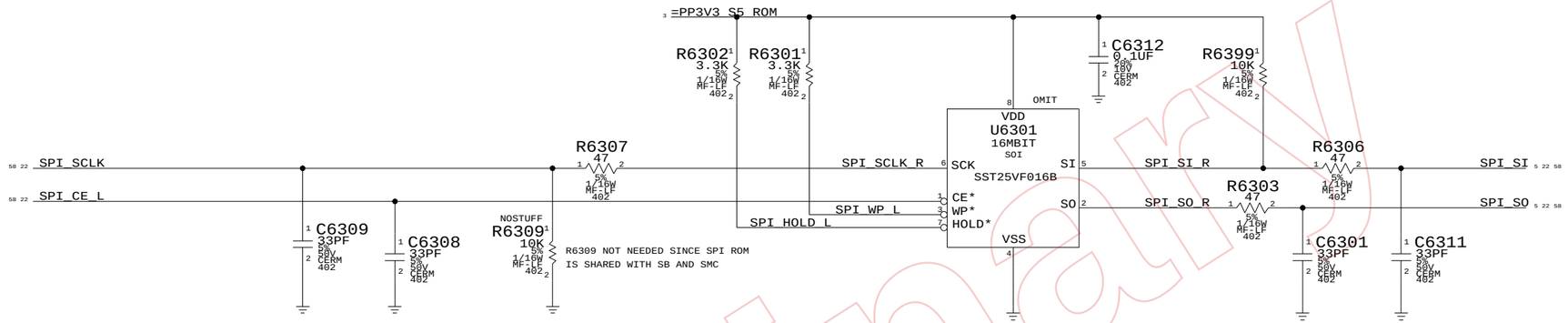
SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE

SHT 60 OF 97



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

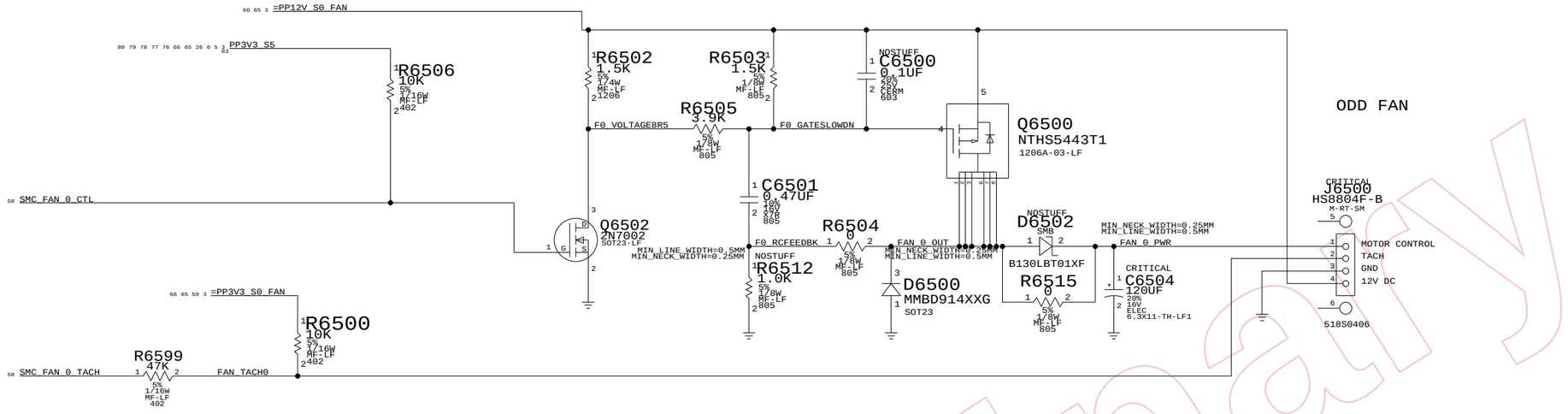
SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

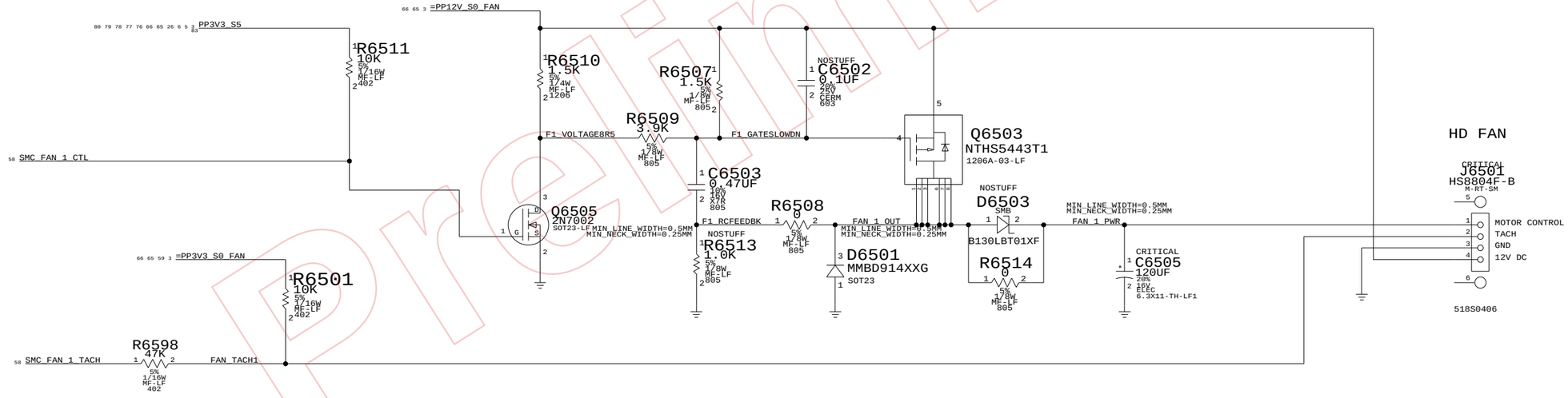
SCALE	SHT
NONE	63 OF 97

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



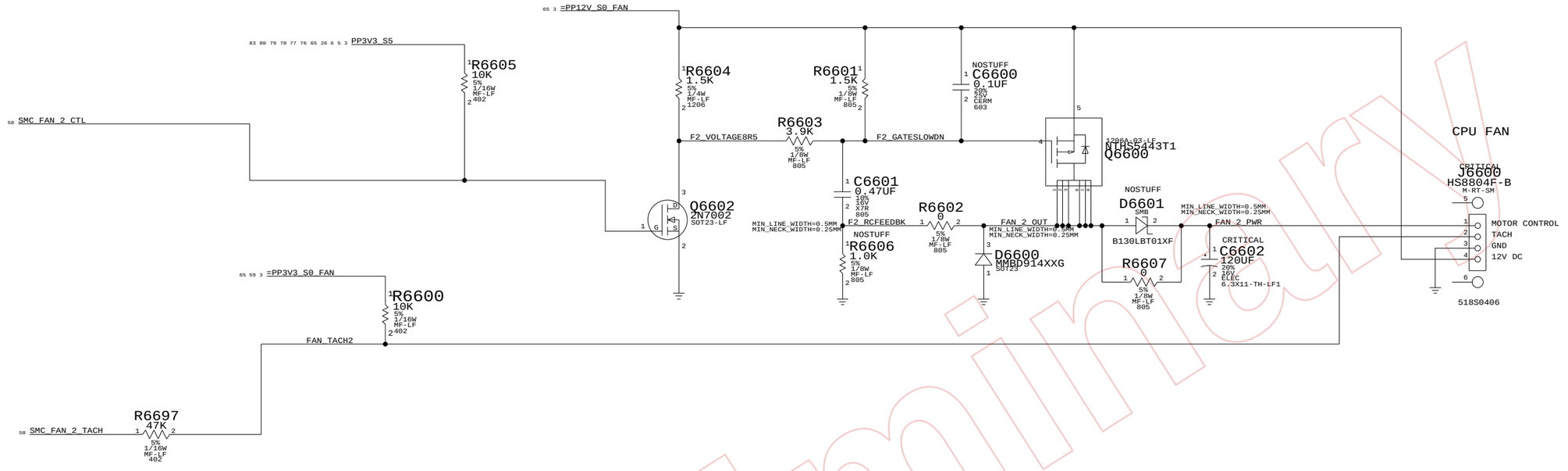
HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

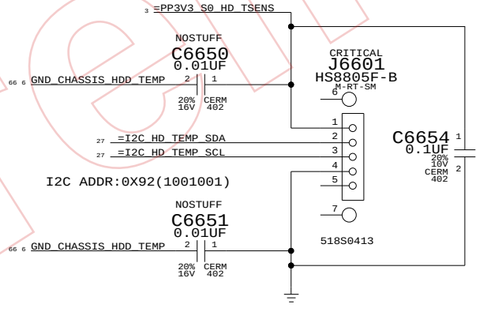
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 65 OF 97	

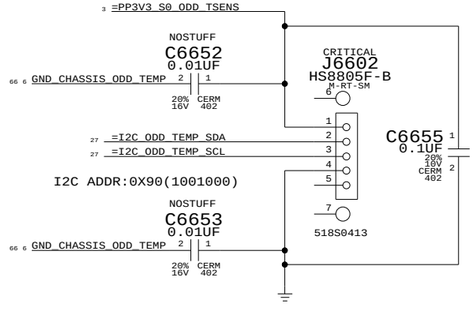
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR

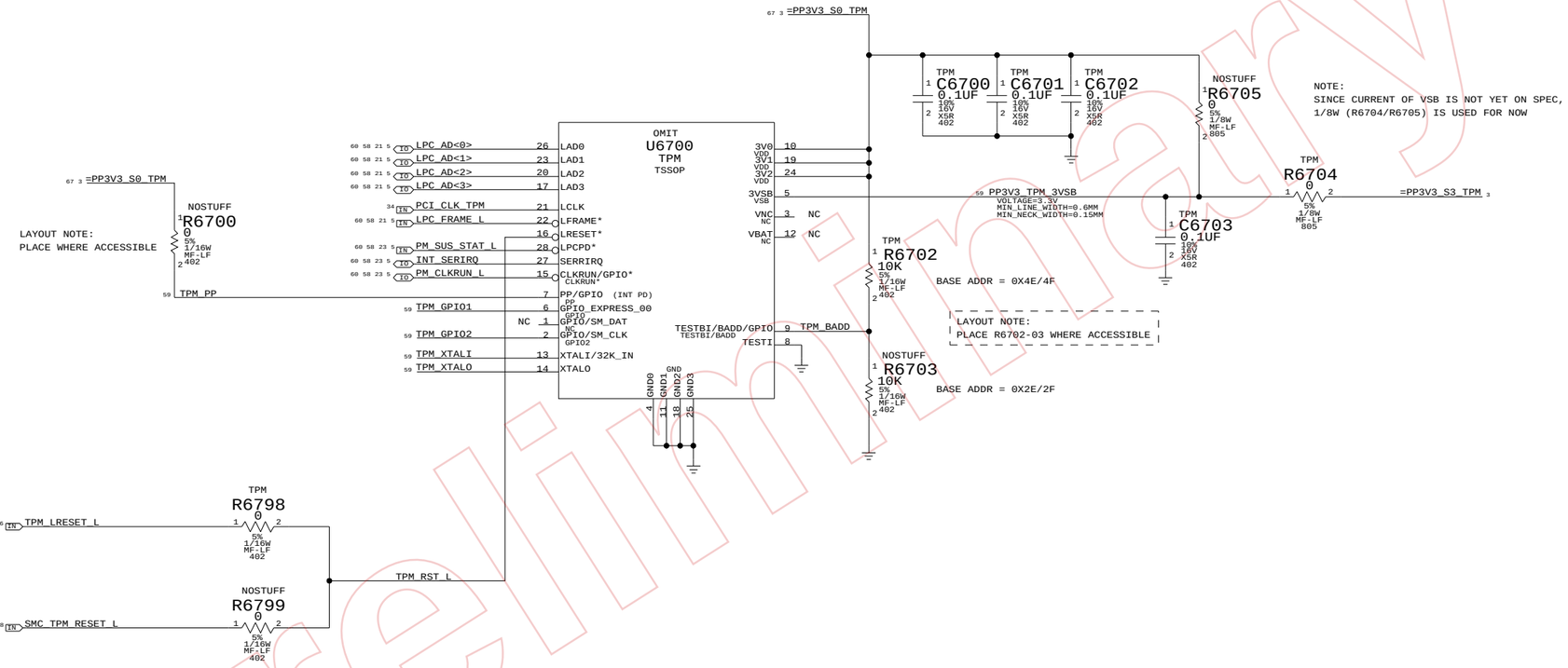


CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 66 OF 97	



TPM

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

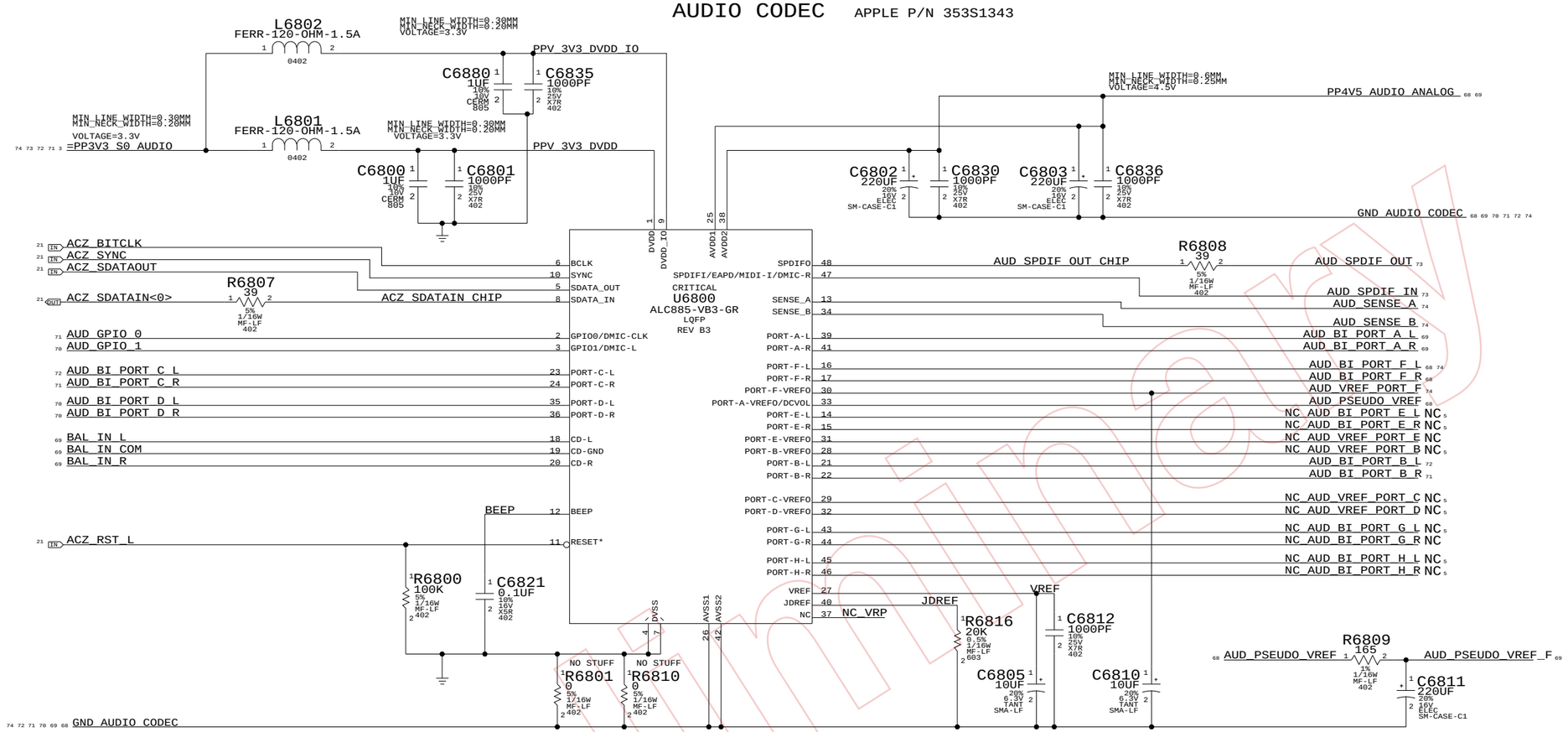
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

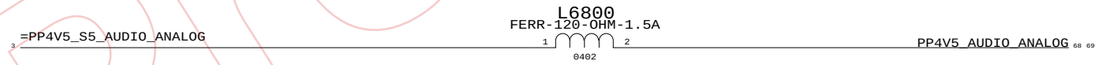
SCALE	SHT
NONE	67 OF 97

AUDIO CODEC

APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



MIC INPUT TO BOTH L&R

AUD_BI_PORT_F_L — AUD_BI_PORT_F_R

AUDIO: CODEC

SYNC_MASTER=AUDIO

SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

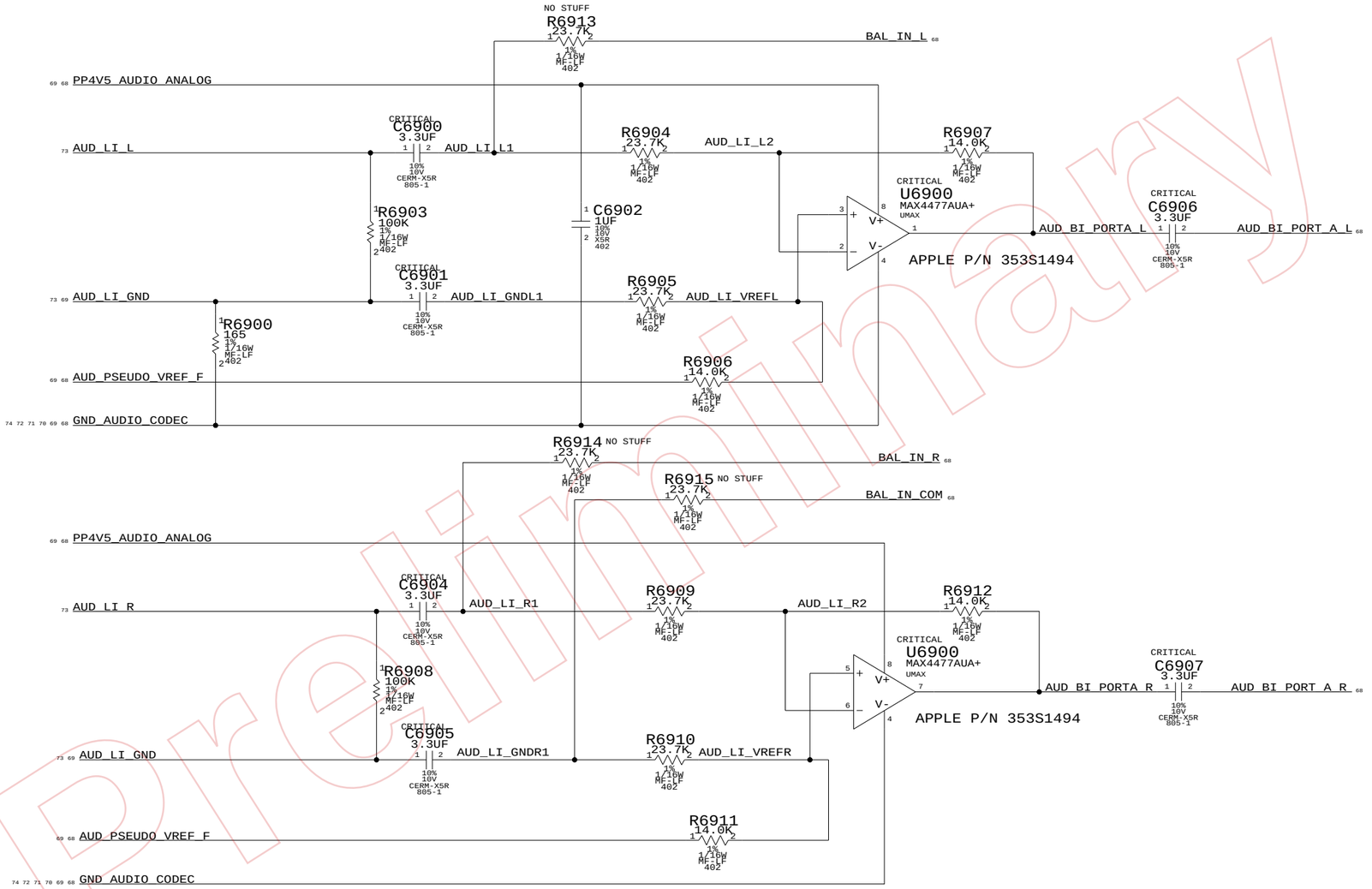
SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE: NONE

SHT 68 OF 97

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.59



AUDIO: LINE INPUT AMP

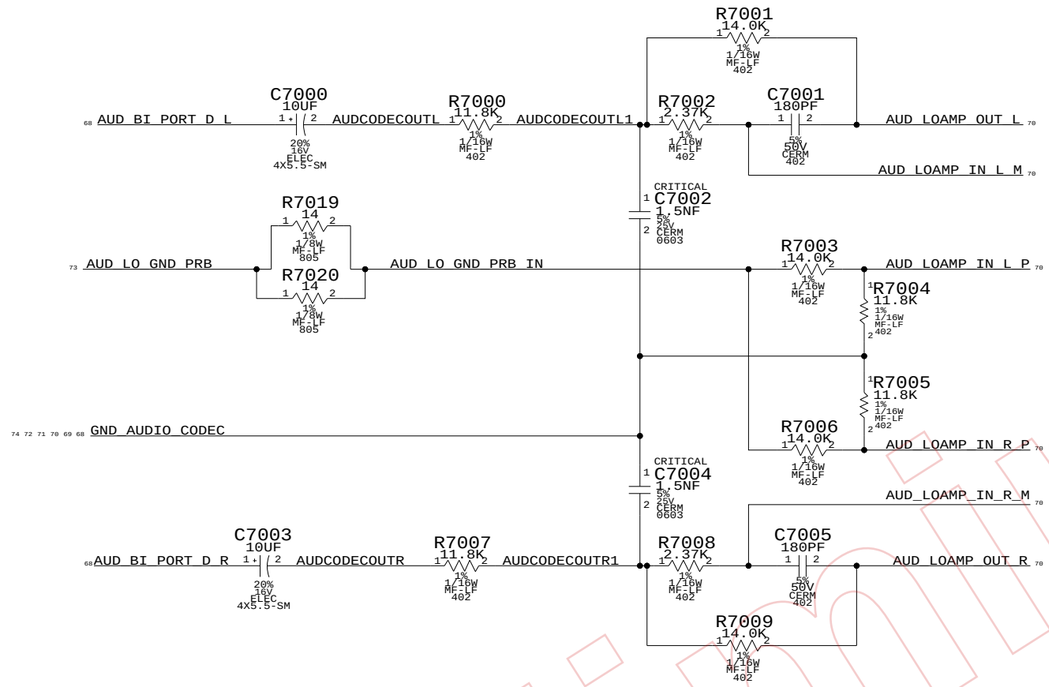
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE	SHT
NONE	69 OF 97

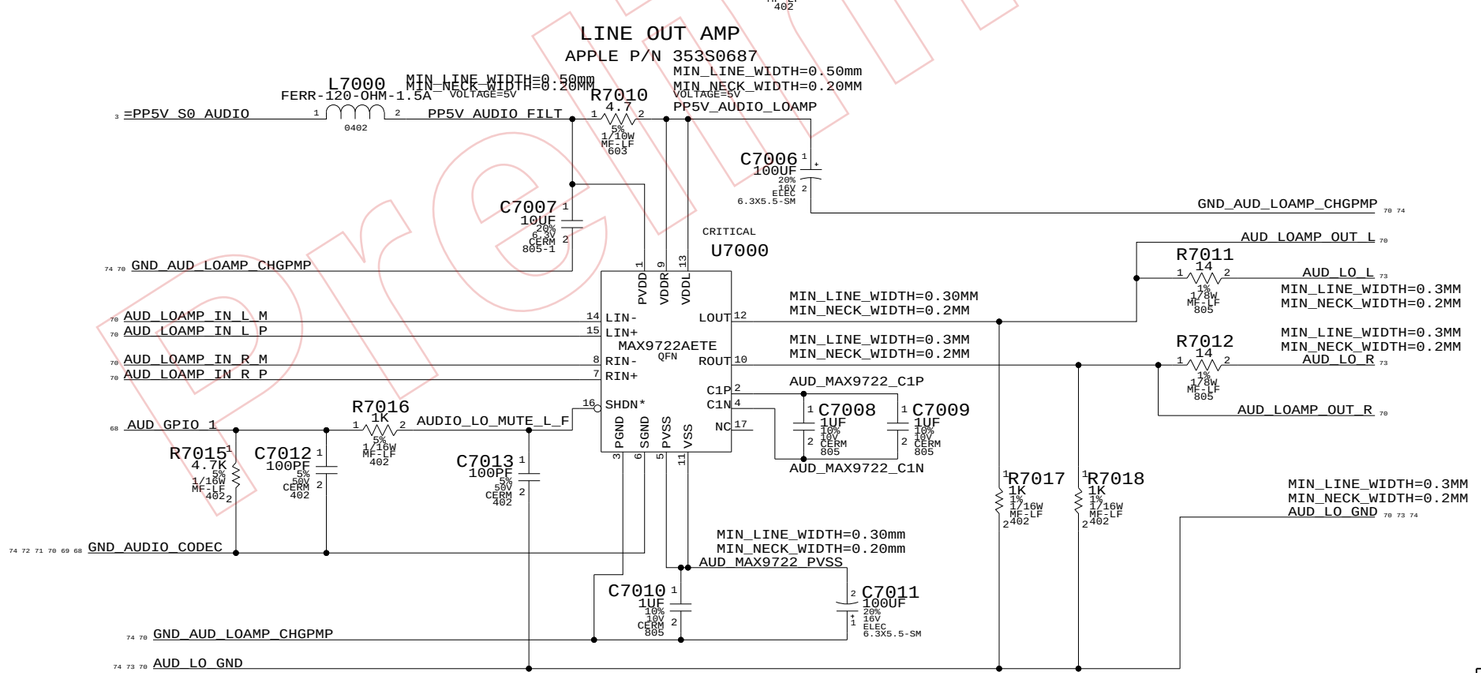
LINE OUT LOW-PASS FILTER

Fc = 37 KHZ, Av = -1.18



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: COMBO OUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 70 OF 97	

DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING

SPEAKER AMP
APPLE P/N 353S1156

=PP12V_S5_AUDIO_SPKRAMP
R7170 0.005 1% 1/4W MF-LF 1206
L7122 FERR-250-OHM SM-1
L7100 FERR-250-OHM SM-1
12V_S5_SPKRAMP
PP12V_AUD_SPKRAMP_PLANE
C7117 470UF 20% 25V ELEC 10X10-SM
C7100 470UF 20% 25V ELEC 10X10-SM
C7101 10UF 10% 16V CERM 1210
C7118 0.1UF 10% 16V CERM 603
C7102 1UF 10% 35V X7R 805
C7119 0.1UF 20% 16V CERM 603
C7103 10UF 10% 16V CERM 1210
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC
AUD_BI_PORT_C_R
L7105 1000-OHM-200MA 0603
C7104 0.47UF 10% 16V X7R 805
AUDSAMPINLN
C7115 100PF 5% 50V CERM 402
L7106 1000-OHM-200MA 0603
C7105 0.47UF 10% 16V X7R 805
AUDSAMPINLP
L7107 1000-OHM-200MA 0603
C7106 0.47UF 10% 16V X7R 805
AUDSAMPINRP
C7116 100PF 5% 50V CERM 402
AUD_BI_PORT_B_R
L7108 1000-OHM-200MA 0603
C7107 0.47UF 10% 16V X7R 805
AUDSAMPINRN
=PP3V3_S0_AUDIO
R7114 47K 5% 1/10W MF-LF 402
AUD_SAMP_SHDN_L
AUD_SPKRAMP_MUTE
R7115 47K 5% 1/10W MF-LF 402
=PP3V3_S0_AUDIO
R7113 47K 5% 1/16W MF-LF 402
AUD_GPIO_0
AUD_SPKRAMP_MUTE_L
Q7100 2N7002DW-X-F SOT-363
R7112 4.7K 5% 1/16W MF-LF 402
C7120 100PF 5% 50V CERM 402
C7121 100PF 5% 50V CERM 402
GND_AUDIO_CODEC
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
SPKRAMP_SS
Q7100 2N7002DW-X-F SOT-363
C7114 1UF 10% 25V X5R 603
C7190 100PF 5% 50V CERM 402
C7109 0.47UF 10% 16V X7R 805
NOSTUFF
R7119 0 5% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_MAX9714_CHOLD

CRITICAL
U7100 MAX9714 QFN-LF

AUD_SAMP_INL_N
AUD_SAMP_INL_P
AUD_SAMP_INR_P
AUD_SAMP_INR_N
AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2
AUD_SAMP_SHDN_L
AUD_MAX9714_VREG
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
VDD CHOLD OUTL+ OUTL+ OUTL- OUTL- C1+ C1- OUTR+ OUTR+ OUTR- OUTR- INL- INL+ INR+ INR- G1 G2 FS1 FS2 SHDN* NC REG THM AGND PAD PGND SS

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPOUTRP
AUDSAMPOUTRN
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUDSAMPCPP
AUDSAMPCPN
C7108 0.1UF 10% 50V X7R 603-1

L7101 180-OHM-1.5A 0603-LF
L7102 180-OHM-1.5A 0603-LF
L7103 180-OHM-1.5A 0603-LF
L7104 180-OHM-1.5A 0603-LF
AUD_SPKR_OUTCR_P
AUD_SPKR_OUTCR_N
AUD_SPKR_OUTBR_P
AUD_SPKR_OUTBR_N

C7110 1000PF 10% 25V X7R 402
C7111 1000PF 10% 25V X7R 402
C7112 1000PF 10% 25V X7R 402
C7113 1000PF 10% 25V X7R 402

XW7102 SM OMIT
XW7101 SM OMIT
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_SPKRAMP_PLANE

GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

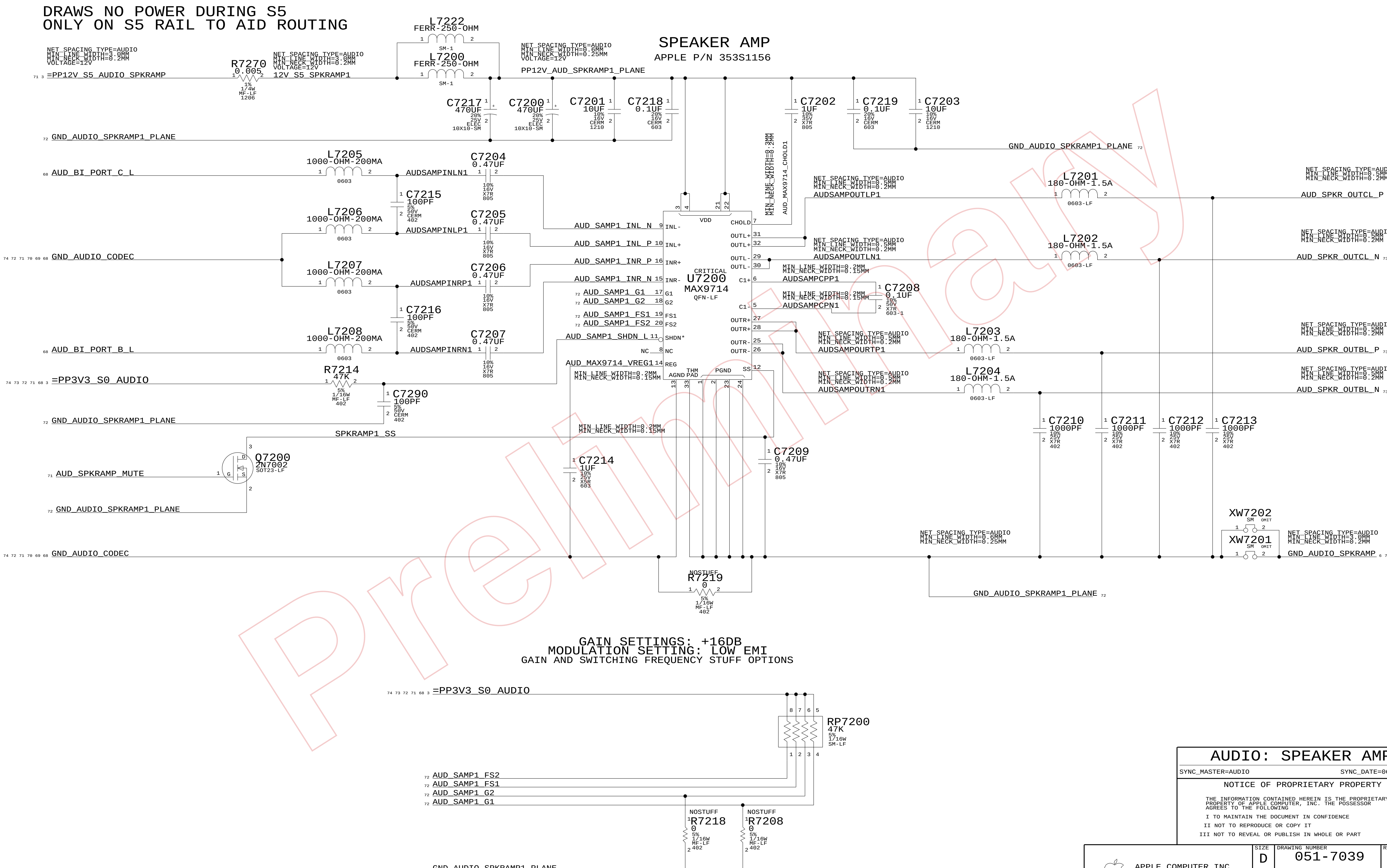
=PP3V3_S0_AUDIO
RP7100 47K 5% 1/16W SM-LF
AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1
NOSTUFF
R7118 0 5% 1/16W MF-LF 402
NOSTUFF
R7108 0 5% 1/16W MF-LF 402
GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 71 OF 97	



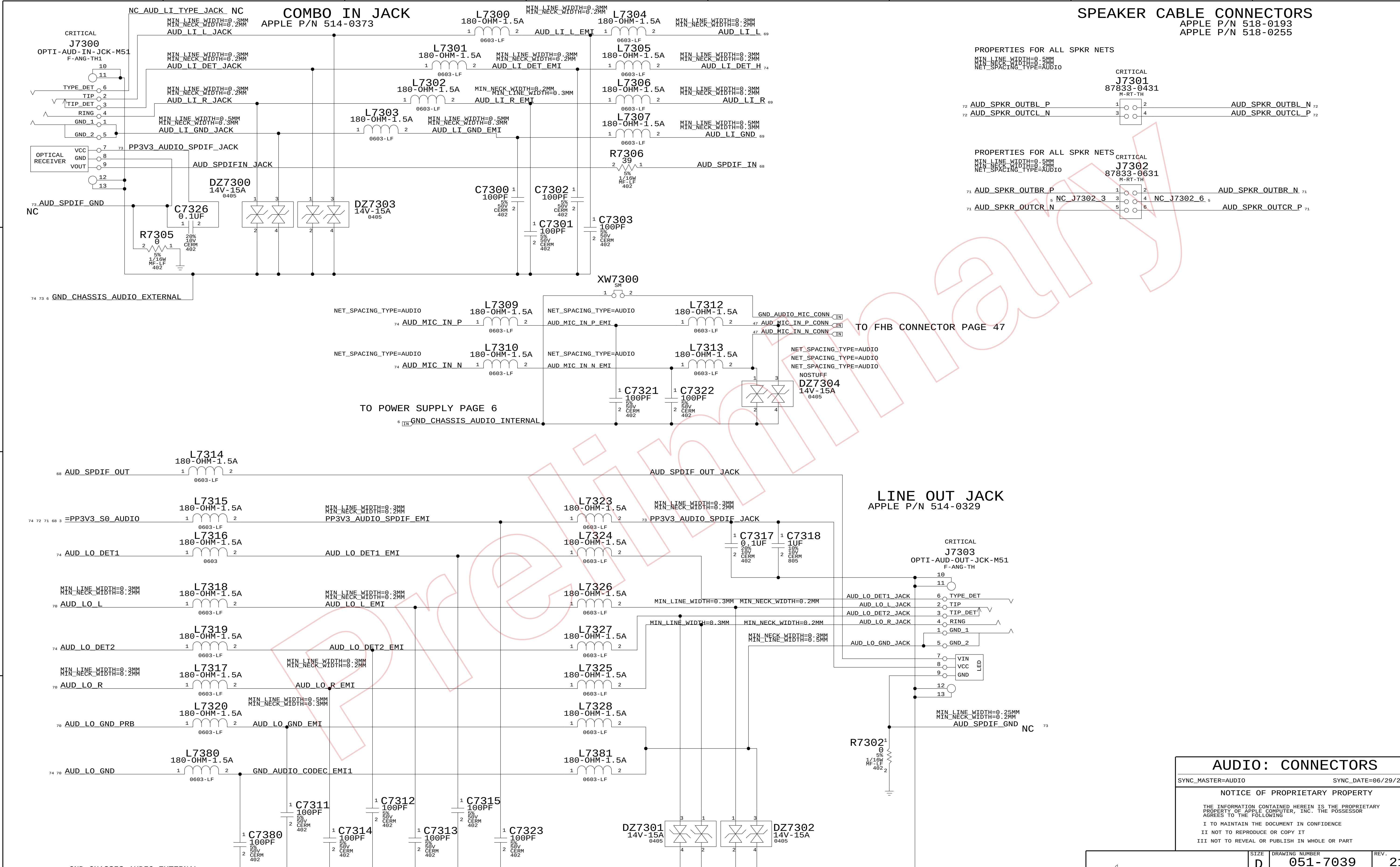
DRAWS NO POWER DURING S5
ONLY ON S5 RAIL TO AID ROUTING
SPEAKER AMP
APPLE P/N 353S1156
=PP12V_S5_AUDIO_SPKRAMP
R7270 0.005 1% 1/4W MF-LF 1206
12V_S5_SPKRAMP1
L7222 FERR-250-OHM SM-1
L7200 FERR-250-OHM SM-1
PP12V_AUD_SPKRAMP1_PLANE
NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=3.0MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=12V
C7217 470UF 20% 25V ELEC 10X10-SM
C7200 470UF 20% 25V ELEC 10X10-SM
C7201 10UF 10% 16V CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 35V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V CERM 1210
GND_AUDIO_SPKRAMP1_PLANE
AUD_BI_PORT_C_L
L7205 1000-OHM-200MA 0603
C7204 0.47UF 10% 16V X7R 805
AUDSAMPINLN1
C7215 100PF 5% 50V CERM 402
L7206 1000-OHM-200MA 0603
C7205 0.47UF 10% 16V X7R 805
AUDSAMPINLP1
GND_AUDIO_CODEC
L7207 1000-OHM-200MA 0603
C7206 0.47UF 10% 16V X7R 805
AUDSAMPINRP1
C7216 100PF 5% 50V CERM 402
L7208 1000-OHM-200MA 0603
C7207 0.47UF 10% 16V X7R 805
AUD_BI_PORT_B_L
AUDSAMPINRN1
=PP3V3_S0_AUDIO
R7214 47K 5% 1/16W MF-LF 402
C7290 100PF 5% 50V CERM 402
SPKRAMP1_SS
Q7200 2N7002 SOT23-LF
AUD_SPKRAMP_MUTE
AUD_SAMP1_INL_N
AUD_SAMP1_INL_P
AUD_SAMP1_INR_P
AUD_SAMP1_INR_N
AUD_SAMP1_G1
AUD_SAMP1_G2
AUD_SAMP1_FS1
AUD_SAMP1_FS2
AUD_SAMP1_SHDN_L
AUD_MAX9714_VREG1
CRITICAL
U7200
MAX9714
QFN-LF
VDD INL- INL+ INR+ INR- G1 G2 FS1 FS2 SHDN* NC REG AGND THM PAD PGND SS
CHOLD OUTL+ OUTL+ OUTL- OUTL- C1+ C1- OUTR+ OUTR+ OUTR- OUTR-
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD1
AUDSAMPOUTLP1
AUDSAMPOUTLN1
AUDSAMPCPP1
AUDSAMPCPN1
C7208 0.1UF 10% 50V X7R 603-1
AUDSAMPOUTRP1
AUDSAMPOUTRN1
L7201 180-OHM-1.5A 0603-LF
L7202 180-OHM-1.5A 0603-LF
L7203 180-OHM-1.5A 0603-LF
L7204 180-OHM-1.5A 0603-LF
AUD_SPKR_OUTCL_P
AUD_SPKR_OUTCL_N
AUD_SPKR_OUTBL_P
AUD_SPKR_OUTBL_N
C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402
C7214 1UF 10% 25V X5R 603
C7209 0.47UF 10% 16V X7R 805
NOSTUFF
R7219 0 5% 1/16W MF-LF 402
XW7202 SM OMIT
XW7201 SM OMIT
GND_AUDIO_SPKRAMP
GAIN SETTINGS: +16DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS
RP7200 47K 5% 1/16W SM-LF
R7218 0 5% 1/16W MF-LF 402
R7208 0 5% 1/16W MF-LF 402

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE NONE	SHT 72 OF 97	


COMBO IN JACK
APPLE P/N 514-0373
CRITICAL
J7300
OPTI-AUD-IN-JCK-M51
F-ANG-TH1
NC_AUD_LI_TYPE_JACK NC
TYPE_DET
TIP
TIP_DET
RING
GND_1
GND_2
OPTICAL RECEIVER
VCC
GND
VOUT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
AUD_LI_L_JACK
AUD_LI_DET_JACK
AUD_LI_R_JACK
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM
AUD_LI_GND_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_SPDIFIN_JACK
AUD_SPDIF_GND
NC
C7326
0.1UF
R7305
0
DZ7300
14V-15A
DZ7303
14V-15A
GND_CHASSIS_AUDIO_EXTERNAL
L7300
180-OHM-1.5A
L7301
180-OHM-1.5A
L7302
180-OHM-1.5A
L7303
180-OHM-1.5A
AUD_LI_L_EMI
AUD_LI_DET_EMI
AUD_LI_R_EMI
AUD_LI_GND_EMI
L7304
180-OHM-1.5A
L7305
180-OHM-1.5A
L7306
180-OHM-1.5A
L7307
180-OHM-1.5A
AUD_LI_L
AUD_LI_DET_H
AUD_LI_R
AUD_LI_GND
R7306
39
AUD_SPDIF_IN
C7300
100PF
C7301
100PF
C7302
100PF
C7303
100PF
XW7300
SM
NET_SPACING_TYPE=AUDIO
L7309
180-OHM-1.5A
AUD_MIC_IN_P
AUD_MIC_IN_P_EMI
L7310
180-OHM-1.5A
AUD_MIC_IN_N
AUD_MIC_IN_N_EMI
L7312
180-OHM-1.5A
L7313
180-OHM-1.5A
GND_AUDIO_MIC_CONN
AUD_MIC_IN_P_CONN
AUD_MIC_IN_N_CONN
TO FHB CONNECTOR PAGE 47
NOSTUFF
DZ7304
14V-15A
C7321
100PF
C7322
100PF
TO POWER SUPPLY PAGE 6
GND_CHASSIS_AUDIO_INTERNAL
SPEAKER CABLE CONNECTORS
APPLE P/N 518-0193
APPLE P/N 518-0255
PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO
CRITICAL
J7301
87833-0431
M-RT-TH
AUD_SPKR_OUTBL_P
AUD_SPKR_OUTCL_N
AUD_SPKR_OUTBL_N
AUD_SPKR_OUTCL_P
CRITICAL
J7302
87833-0631
M-RT-TH
AUD_SPKR_OUTBR_P
NC_J7302_3
AUD_SPKR_OUTCR_N
AUD_SPKR_OUTBR_N
NC_J7302_6
AUD_SPKR_OUTCR_P
L7314
180-OHM-1.5A
AUD_SPDIF_OUT
AUD_SPDIF_OUT_JACK
L7315
180-OHM-1.5A
=PP3V3_S0_AUDIO
PP3V3_AUDIO_SPDIF_EMI
L7316
180-OHM-1.5A
AUD_LO_DET1
AUD_LO_DET1_EMI
L7318
180-OHM-1.5A
AUD_LO_L
AUD_LO_L_EMI
L7319
180-OHM-1.5A
AUD_LO_DET2
AUD_LO_DET2_EMI
L7317
180-OHM-1.5A
AUD_LO_R
AUD_LO_R_EMI
L7320
180-OHM-1.5A
AUD_LO_GND_PRB
AUD_LO_GND_EMI
L7380
180-OHM-1.5A
AUD_LO_GND
GND_AUDIO_CODEC_EMI1
C7380
100PF
C7311
100PF
C7314
100PF
C7312
100PF
C7313
100PF
C7315
100PF
C7323
100PF
L7323
180-OHM-1.5A
L7324
180-OHM-1.5A
L7326
180-OHM-1.5A
L7327
180-OHM-1.5A
L7325
180-OHM-1.5A
L7328
180-OHM-1.5A
L7381
180-OHM-1.5A
PP3V3_AUDIO_SPDIF_JACK
C7317
0.1UF
C7318
1UF
LINE OUT JACK
APPLE P/N 514-0329
CRITICAL
J7303
OPTI-AUD-OUT-JCK-M51
F-ANG-TH
AUD_LO_DET1_JACK
AUD_LO_L_JACK
AUD_LO_DET2_JACK
AUD_LO_R_JACK
AUD_LO_GND_JACK
VIN
VCC
GND
LED
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM
AUD_SPDIF_GND
NC
R7302
0
DZ7301
14V-15A
DZ7302
14V-15A

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE NONE	SHT 73 OF 97	

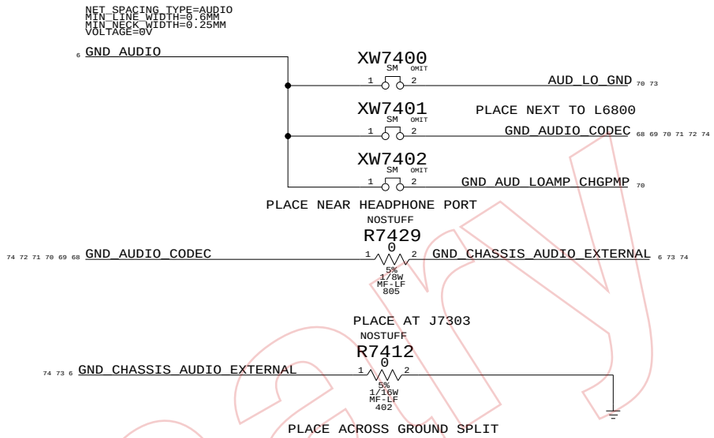
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	DAC	PIN COMPLEX	MUTE CONTROL
LINE OUT	0X0C	0X02	0X14(D)	GPIO 1
SPKR AMP	0X0D	0X03	0X18(B)	GPIO 0
SPKR AMP1	0X0F	0X05	0X1A(C)	GPIO 0
SPDIFOUT		CONVERTER=0X06	PIN=0X1E	
		DETECT DELEGATE PIN 0X16H		

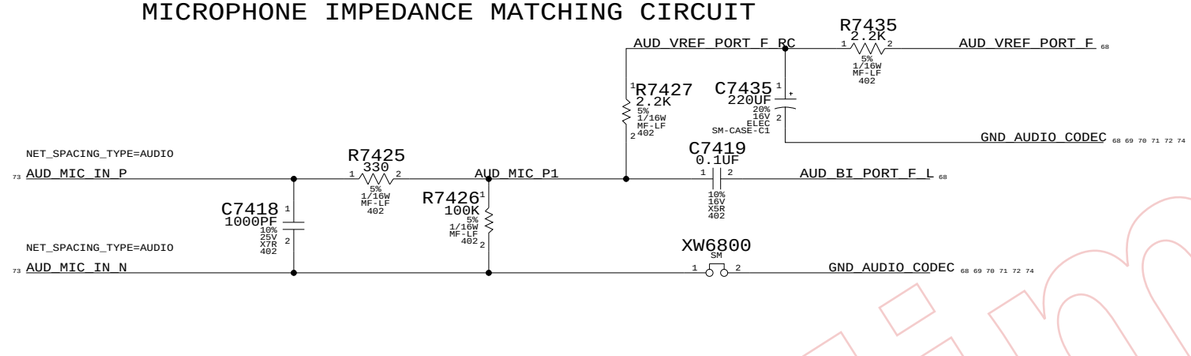
CODEC INPUT SIGNAL PATHS

FUNCTION	ADC	MIXER	PORT	VREF
MIC INPUT	0X07	0X24	0X19(F)	80%
LINE INPUT	0X08	0X23	0X15(A)	50%
SPDIFIN	CONVERTER=0X0A		PIN=0X1F	

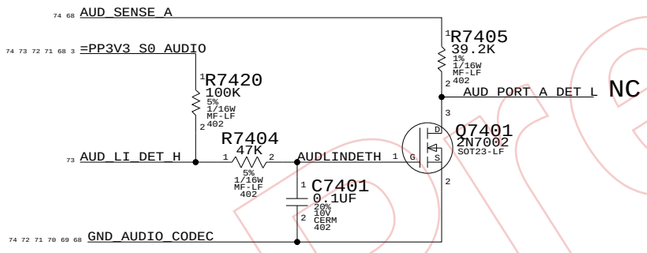
AUDIO GROUND RETURNS



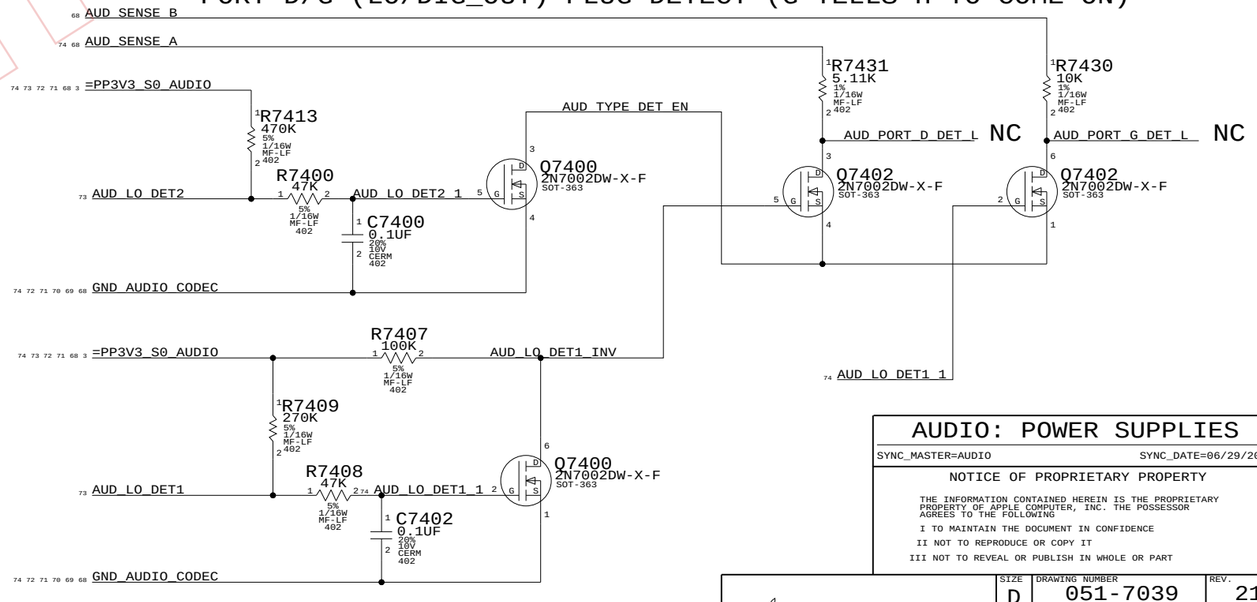
MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A (LI) PLUG DETECT



PORT D/G (LO/DIG_OUT) PLUG DETECT (G TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 74 OF 97	

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

CPU_VCCSENSE_P & N ARE DIFF PAIRS
ROUTE AS 18MIL WIDE, 7MIL SPACE

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator	
SYNC_MASTER=M51_PAUL	SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 75 OF 97	

PROCESSOR VCORE SENSE

PCB: PLACE R7612, C7612 WITHIN 1" OF SMC (U5800)

75 5 3 PPVCORE_CPU — R7612 4.53K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — SMC_CPU_VSENSE 58

C7612 0.22UF 20% 6.3V X5R 402 (CPU_PWR_SENSE)

GND_SMC_AVSS 58 59 76 84

PROCESSOR VCORE CURRENT SENSE

(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

C7600 470PF 10% 50V CERM 402 (CPU_PWR_SENSE) — CPU_ISENSE_OUT_R

R7609 1M 1% 1/16W MF-LF 402 (CPU_PWR_SENSE)

75 IMVP6_VO — R7659 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — IMVP6_VO_R_OA

84 83 76 41 27 26 10 6 5 3 PP3V3_S0 — C7601 0.1UF CERM 20% 10V CRITICAL (CPU_PWR_SENSE) — GND_CPU_ISENSE_OPAMP

R7605 40.2K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — CPU_ISENSE_R_POS

U7600 LMV2011MF SOT23-5

75 IMVP6_DROOP — R7669 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — IMVP6_DROOP_R

R7606 40.2K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — CPU_ISENSE_R_NEG

MIN_LINE_WIDTH=0.20 MM MIN_NECK_WIDTH=0.20 MM

PCB: PLACE R7602, C7602 WITHIN 1" OF SMC (U5800)

R7602 4.53K 1% 1/16W MF-LF 402 (CPU_PWR_SENSE) — SMC_CPU_ISENSE 58

C7602 0.22UF 20% 6.3V X5R 402 (CPU_PWR_SENSE)

GND_SMC_AVSS 58 59 76 84

NOSTUFF R7604 0 5% 1/16W MF-LF 402

C7603 470PF 10% 50V CERM 402 (CPU_PWR_SENSE) — R7603 1M 1% 1/16W MF-LF 402 (CPU_PWR_SENSE)

R7607 0 5% 1/16W MF-LF 402 (CPU_PWR_SENSE) — GND_NEXT_TO_SMC 59

CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

83 3 PP12V_S0_B

R7639 10K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

Q7640 NTR4101P SOT-23 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L — MIN_LINE_WIDTH=0.20 MM MIN_NECK_WIDTH=0.20 MM

R7641 10K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L_R

Q7639 2N7002 SOT23-LF (CPU_PWR_SENSE)

58 5 ISENSE_CAL_EN — R7640 100K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

ISENSE_CAL_EN_L12V — R7642 470K 5% 1/16W MF-LF 402 (CPU_PWR_SENSE)

9 8 3 =PPVCORE_S0_CPU — R7643 1.00 1% 1/4W MF-LF 1206 (CPU_PWR_SENSE)

CPUVCORE_ISENSE_CAL — MIN_LINE_WIDTH=0.50 MM MIN_NECK_WIDTH=0.20 MM

Q7641 FDC796N SUPERSOT-6 CRITICAL (CPU_PWR_SENSE)

SMC PWRGD PULLUP

83 80 79 78 77 66 65 26 6 5 3 PP3V3_S5 — R7623 10K 1% 1/16W MF-LF 402

NOSTUFF R7620 0 5% 1/16W MF-LF 402

82 78 6 SYS_POWERFAIL_L — RSMRST_PWRGD 58

SYSTEM CURRENT SENSE

PP12V_S5_AC_DC — MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM VOLTAGE=12V

R7650 0.005 1% 1W MF 2010 (SYS_PWR_SENSE) CRITICAL — PP12V_S5 3 76 77 78 79 80 82 83

PCB:KEEP SHORTS NEXT TO U7602

PCB:PLACE D7650,R7652,C7650 BY SMC

U7602 ZXCT1010 SOT23-5 (SYS_PWR_SENSE) CRITICAL

4 VIN — IOUT 3 — LOAD 5 — GND 2 — NC 1

OMIT XW7650 SM — SYSTEM_DCIN_SENSE — SYSTEM_SENSE_I_R

R7651 5.90K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

R7656 100 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SYSTEM_SENSE_SET

SCALE 3.33333 A/V — COUNT .010753 A/COUNT — ADC IS 10BIT 0 TO 3.3V

PP3V3_S0 3 5 6 10 26 27 41 76 83 84

D7650 BAS16-75V-0.25A SOT23-LF NOSTUFF → TO SMC

R7652 4.53K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SMC_DCIN_ISENSE 58

C7650 0.22UF 20% 6.3V X5R 402 (SYS_PWR_SENSE) — 1 MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.

GND_SMC_AVSS 58 59 76 84

PCB: PLACE D7599, C7599, R7597 WITHIN 1" OF SMC (U5800)

SYSTEM VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)

83 82 80 79 78 77 76 3 PP12V_S5

R7653 6.04K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

R7654 2.0K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE)

SMC_SYSTEM_VSENSE_R

R7655 4.53K 1% 1/16W MF-LF 402 (SYS_PWR_SENSE) — SMC_PBUS_VSENSE 58

C7651 0.22UF 20% 6.3V X5R 402 (SYS_PWR_SENSE)

GND_SMC_AVSS 58 59 76 84

SCALE 4 V/V — COUNT .0129 V/COUNT — ADC IS 10BIT 0 TO 3.3V

PCB: PLACE R7655, C7651 WITHIN 1" OF SMC (U5800)

CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE — SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

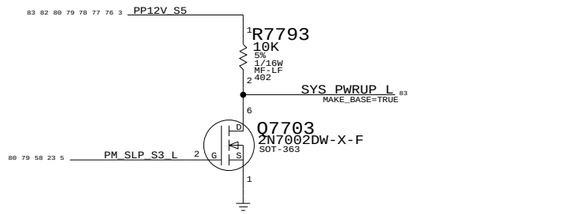
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

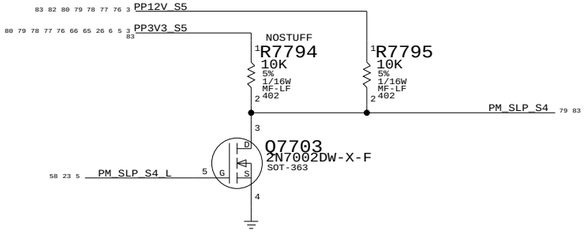
II NOT TO REPRODUCE OR COPY IT

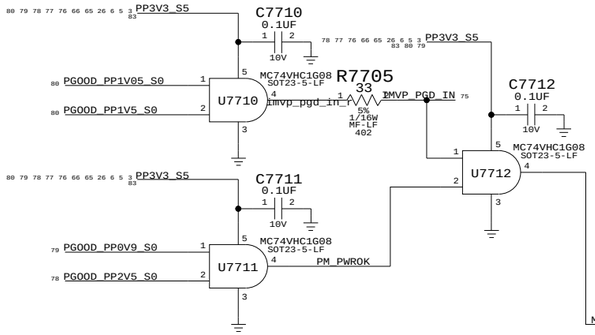
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

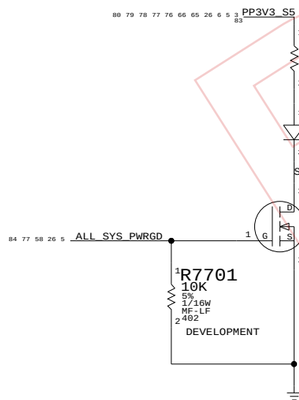
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 76 OF 97	



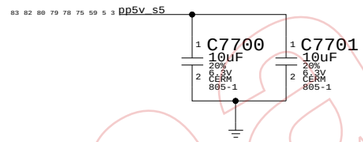






ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin
put here to stay in sync with M50 on page 82



PWR GOOD

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE	SHT
NONE	77 OF 97

3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

3.3V S5
POWER BUDGET
MISC=1.500A
SB=0.500A
AIRPORT=1.000A
PANEL=1.000A
TOTAL=4.000A

=PP3V3_S5_2V5_LDO
C7820 22UF 20% 6.3V X5R 805
CRITICAL Q7803 IRF1902PBF SO-8

PP12V_S5
C7892 1UF 10% 25V X5R 603

3V3REG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7805 10 1% 1/16W MF-LF 402
C7800 1UF 10% 6.3V CERM 402
3V3REG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7823 1000PF 10% 25V X7R 402

U7800 ISL6549 QFN
VCC12 CRITICAL
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
THRML_PAD DGND AGND PGND
UGATE BOOT PHASE LGATE FB COMP

3V3REG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7840 2.2 5% 1/16W MF-LF 402
3V3REG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7801 0.1UF 20% 25V CERM 603
3V3REG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
3V3REG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7804 8.06K 1% 1/16W MF-LF 402
C7808 0.047UF 10% 16V CERM 402
3V3REG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7806 560PF 10% 50V CERM 402

CRITICAL Q7800 IRLR7807Z TO-252AA
CRITICAL Q7801 IRLR7807Z TO-252AA
D7800 CTLSH3-30M833 TLM833
nostuff

CRITICAL C7853 680UF 20% 16V ELEC TH-MCZ
C7811 10UF 10% 16V CERM 1210
L7803 3.0UH TH1 CRITICAL
PP3V3_S5 3.35V NOMINAL
R7802 5.11 1% 1/4W MF-LF 1206
3V3REG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7809 1000PF 5% 50V CERM 1206
CRITICAL C7815 1800UF 20% 6.3V ELEC TH-KZJ-LF
C7814 10UF 20% 6.3V CERM 805-1
C7813 10UF 20% 6.3V CERM 805-1

PP2V5_S5
2.50V NOMINAL
C7825 10UF 20% 6.3V CERM 805-1
C7822 10UF 20% 6.3V CERM 805-1
C7821 10UF 20% 6.3V CERM 805-1
C7826 10UF 20% 6.3V CERM 805-1
R7820 1K 1% 1/16W MF-LF 402
R7821 2.7K 1% 1/16W MF-LF 402
2V5_LDODR_C nostuff MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7824 1000PF 10% 25V X7R 402
3V3REG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7822 470 1% 1/16W MF-LF 402

XW7800 SM

3V3REG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7892 100K 5% 1/16W MF-LF 402
NOSTUFF
Q7802 2N7002 SOT23-LF
SYS_POWERFAIL_L
C7803 4.7UF 20% 6.3V CERM 603
3V3REG_GND VOLTAGE=0 V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R7899 22 5% 1/16W MF-LF 402
3V3REG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C7807 0.01UF 10% 16V CERM 402
R7803 1.24K 1% 1/16W MF-LF 402 (R2)
R7801 392 1% 1/16W MF-LF 402 (R1)

5% OK ON R7801?
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

PP5V_S5
PP3V3_S5
C7880 0.1UF 20% 10V CERM 402
R7811 2.49K 1% 1/16W MF-LF 402
R7810 10K 1% 1/16W MF-LF 402
2V2_REF 2.219V
U7810 LM339A SOI-LF
PP2V5_S0
PGOOD_PP2V5_S0
R7812 5.11K 1% 1/16W MF-LF 402

PP2V5_S0
U7810 LM339A SOI-LF
SPARE COMPARATOR

3V DC/DC 2.5V

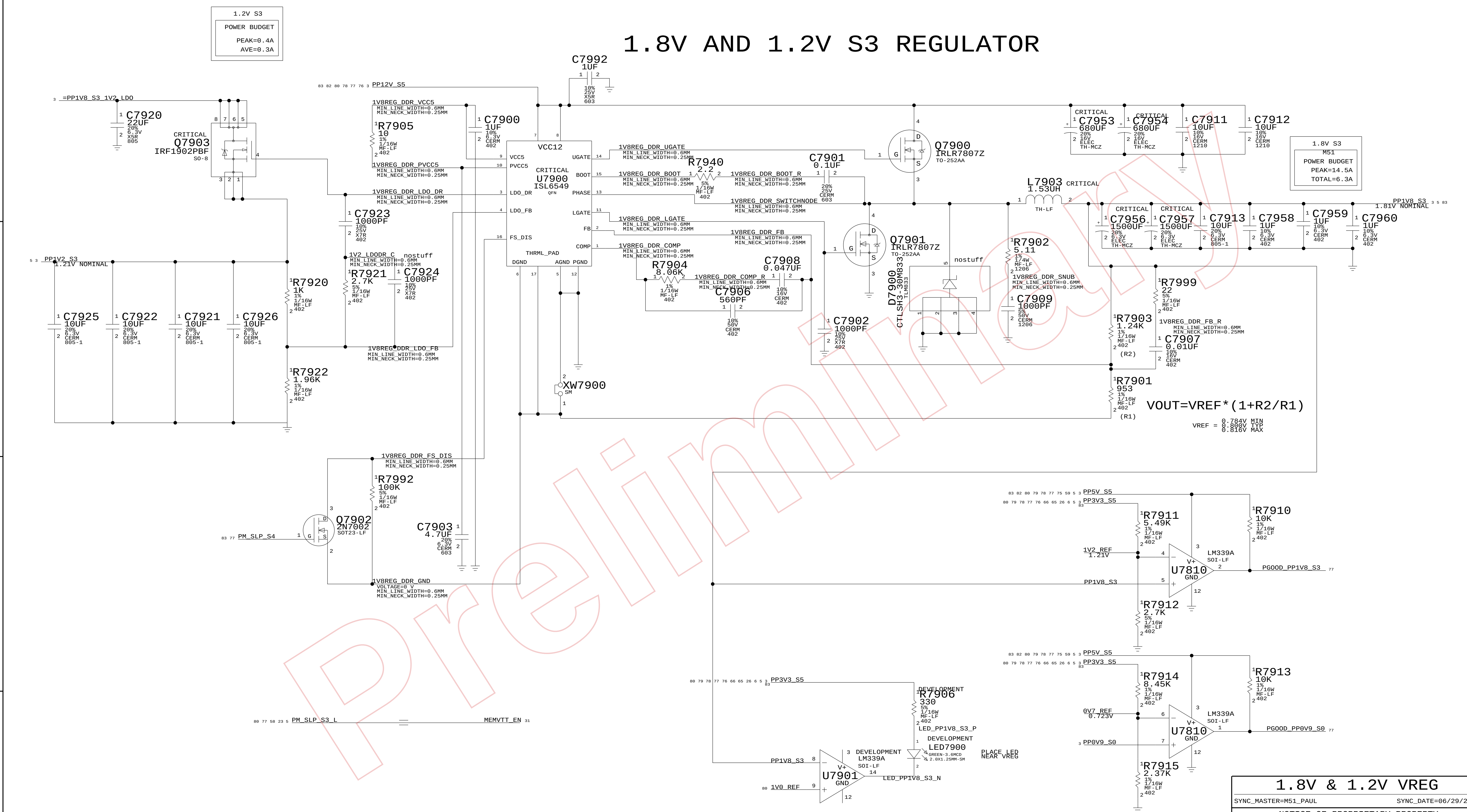
SYNC_MASTER=M51_PAUL
SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 78 OF 97	

TRUE

1.8V AND 1.2V S3 REGULATOR



1.2V S3
POWER BUDGET
PEAK=0.4A
AVE=0.3A
C7992
1UF
10% 25V X5R 603
83 82 80 78 77 76 3 PP12V_S5
3 =PP1V8_S3_1V2_LDO
C7920
22UF
20% 6.3V X5R 805
CRITICAL
Q7903
IRF1902PBF
SO-8
1V8REG_DDR_VCC5
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
R7905
10
1% 1/16W MF-LF 402
C7900
1UF
10% 6.3V CERM 402
1V8REG_DDR_PVCC5
1V8REG_DDR_LDO_DR
C7923
1000PF
10% 25V X7R 402
1V2_LDODR_C
nostuff
R7921
2.7K
5% 1/16W MF-LF 402
C7924
1000PF
10% 25V X7R 402
1V8REG_DDR_LDO_FB
5 3 PP1V2_S3
1.21V NOMINAL
C7925
10UF
20% 6.3V CERM 805-1
C7922
10UF
20% 6.3V CERM 805-1
C7921
10UF
20% 6.3V CERM 805-1
C7926
10UF
20% 6.3V CERM 805-1
R7920
1K
1% 1/16W MF-LF 402
R7922
1.96K
1% 1/16W MF-LF 402
VCC12
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
CRITICAL
U7900
ISL6549
QFN
UGATE
BOOT
PHASE
LGATE
FB
COMP
THRML_PAD
DGND
AGND
PGND
1V8REG_DDR_UGATE
1V8REG_DDR_BOOT
R7940
2.2
5% 1/16W MF-LF 402
1V8REG_DDR_BOOT_R
C7901
0.1UF
20% 25V CERM 603
1V8REG_DDR_SWITCHNODE
1V8REG_DDR_LGATE
1V8REG_DDR_FB
1V8REG_DDR_COMP
R7904
8.06K
1% 1/16W MF-LF 402
1V8REG_DDR_COMP_R
C7908
0.047UF
10% 16V CERM 402
C7906
560PF
10% 50V CERM 402
XW7900
SM
Q7900
IRLR7807Z
TO-252AA
Q7901
IRLR7807Z
TO-252AA
C7902
1000PF
10% 25V X7R 402
D7900
CTLSH3-30M833
TLM833
nostuff
L7903
1.53UH
CRITICAL
TH-LF
R7902
5.11
1% 1/4W MF-LF 1206
1V8REG_DDR_SNUB
C7909
1000PF
5% 50V CERM 1206
CRITICAL
C7953
680UF
20% 16V ELEC TH-MCZ
CRITICAL
C7954
680UF
20% 16V ELEC TH-MCZ
C7911
10UF
10% 16V CERM 1210
C7912
10UF
10% 16V CERM 1210
1.8V S3
M51
POWER BUDGET
PEAK=14.5A
TOTAL=6.3A
PP1V8_S3 3 5 83
1.81V NOMINAL
CRITICAL
C7956
1500UF
20% 6.3V ELEC TH-MCZ
CRITICAL
C7957
1500UF
20% 6.3V ELEC TH-MCZ
C7913
10UF
20% 6.3V CERM 805-1
C7958
1UF
10% 6.3V CERM 402
C7959
1UF
10% 6.3V CERM 402
C7960
1UF
10% 6.3V CERM 402
R7999
22
5% 1/16W MF-LF 402
1V8REG_DDR_FB_R
R7903
1.24K
1% 1/16W MF-LF 402
(R2)
C7907
0.01UF
10% 16V CERM 402
R7901
953
1% 1/16W MF-LF 402
(R1)
VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN 0.800V TYP 0.816V MAX
1V8REG_DDR_FS_DIS
R7992
100K
5% 1/16W MF-LF 402
83 77 PM_SLP_S4
Q7902
2N7002
SOT23-LF
C7903
4.7UF
20% 6.3V CERM 603
1V8REG_DDR_GND
VOLTAGE=0 V
80 77 58 23 5 PM_SLP_S3_L
MEMVTT_EN 31
83 82 80 79 78 77 75 59 5 3 PP5V_S5
80 79 78 77 76 66 65 26 6 5 3 PP3V3_S5 83
R7911
5.49K
1% 1/16W MF-LF 402
1V2_REF
1.21V
PP1V8_S3
LM339A
SOI-LF
U7810
V+
GND
R7910
10K
1% 1/16W MF-LF 402
PGOOD_PP1V8_S3 77
R7912
2.7K
5% 1/16W MF-LF 402
R7914
8.45K
1% 1/16W MF-LF 402
0V7_REF
0.723V
3 PP0V9_S0
R7913
10K
1% 1/16W MF-LF 402
PGOOD_PP0V9_S0 77
R7915
2.37K
1% 1/16W MF-LF 402
80 79 78 77 76 66 65 26 6 5 3 PP3V3_S5 83
DEVELOPMENT
R7906
330
5% 1/16W MF-LF 402
LED_PP1V8_S3_P
DEVELOPMENT
LED7900
GREEN-3.6MCD
2.0X1.25MM-SM
PLACE LED NEAR VREG
PP1V8_S3
80 1V0_REF
DEVELOPMENT
LM339A
SOI-LF
U7901
LED_PP1V8_S3_N

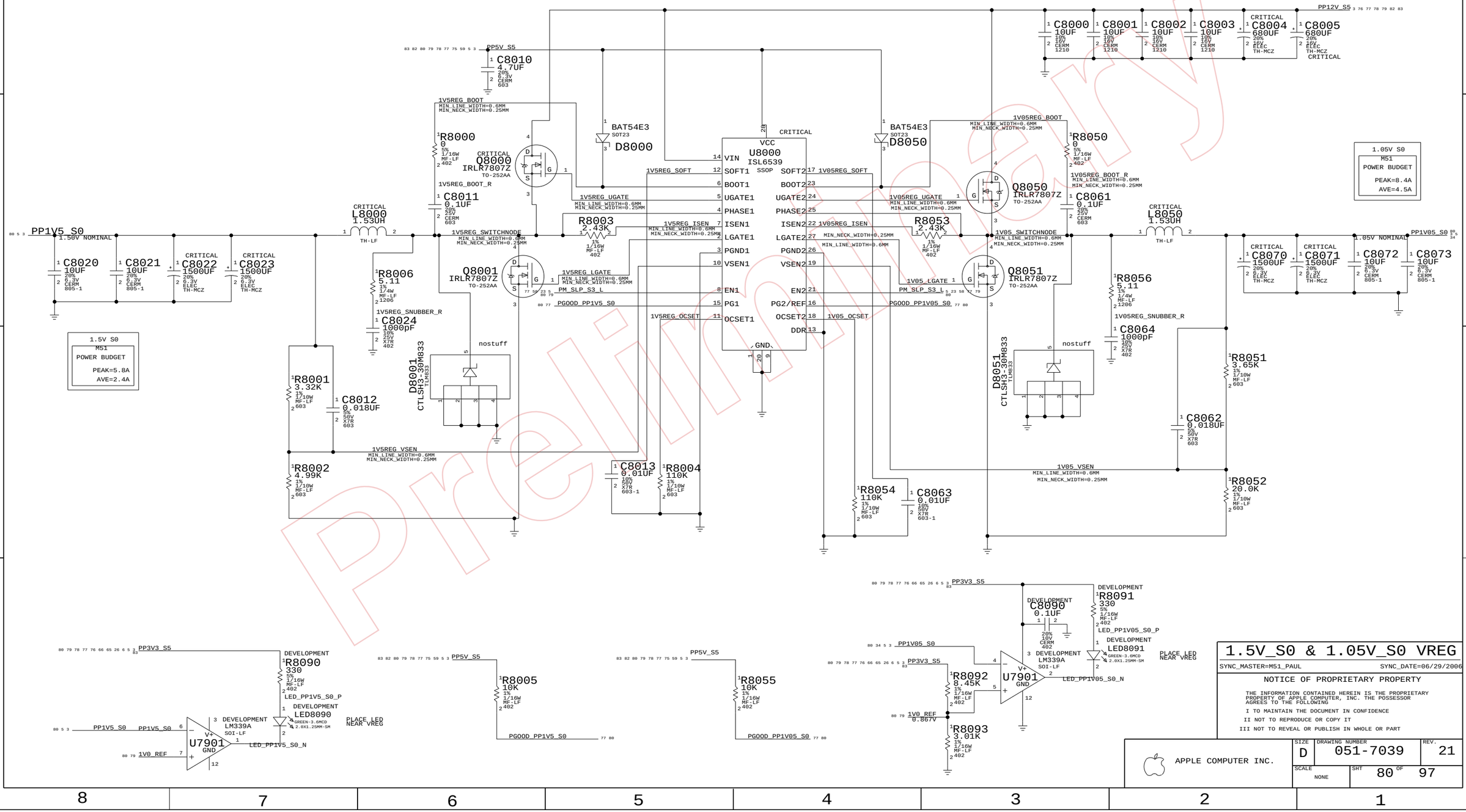
1.8V & 1.2V VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

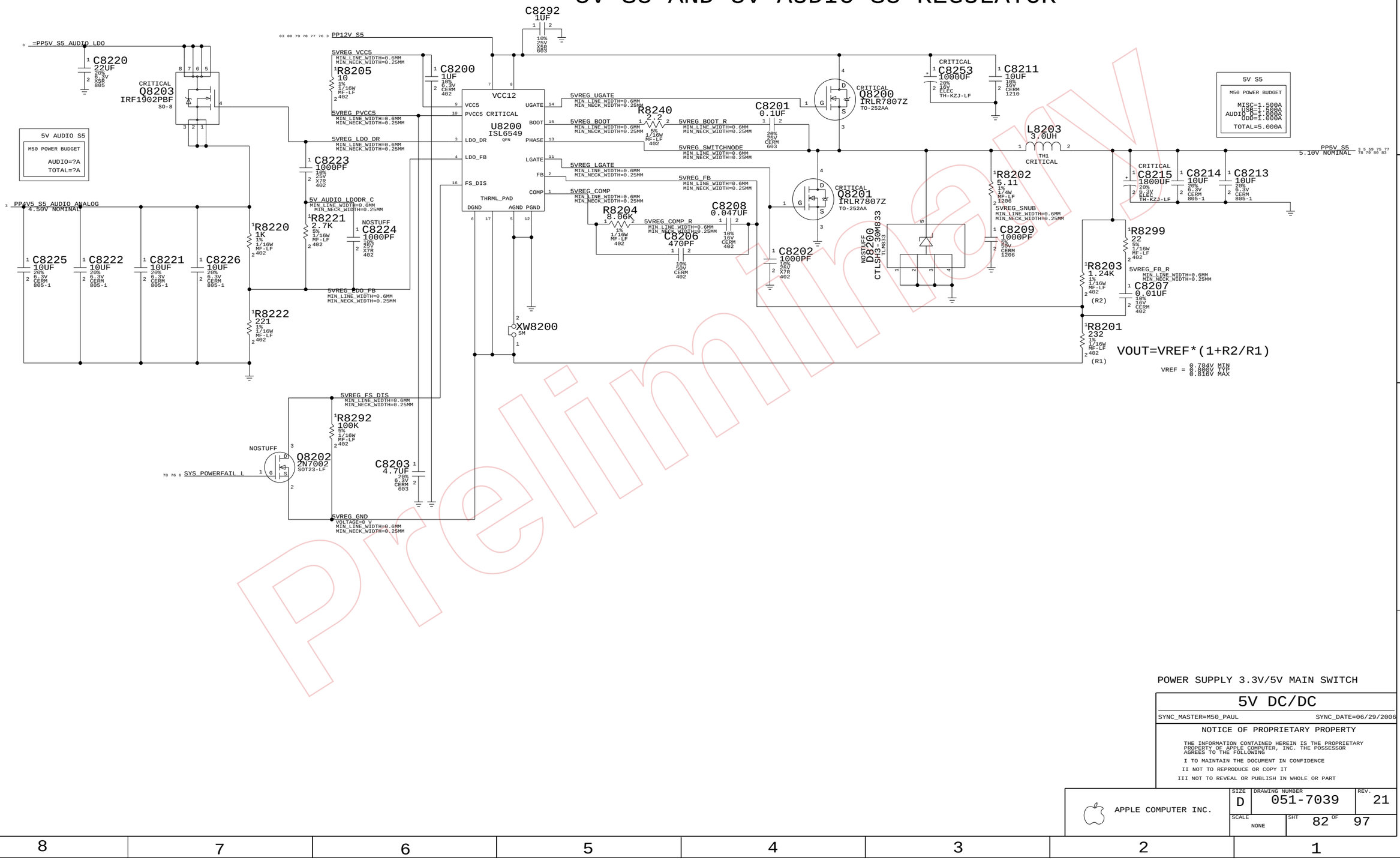
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE NONE	SHT 79 OF 97	

1.5V S0 AND 1.05V S0 RAILS



5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

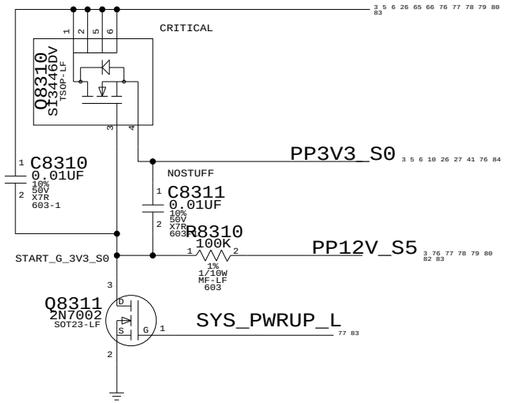
SYNC_MASTER=M50_PAUL SYNC_DATE=06/29/2006

APPLE COMPUTER INC.

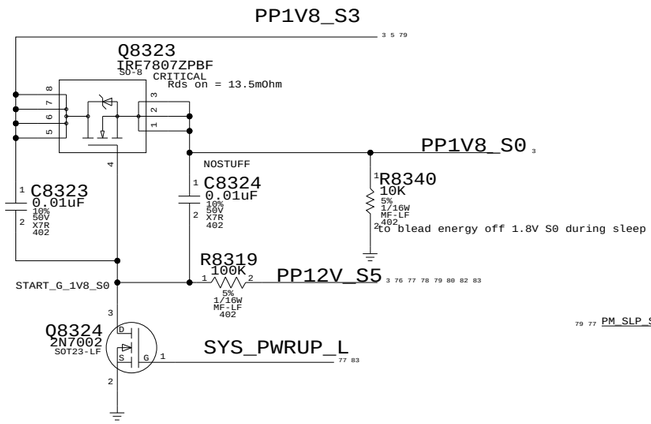
SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE NONE SHT 82 OF 97

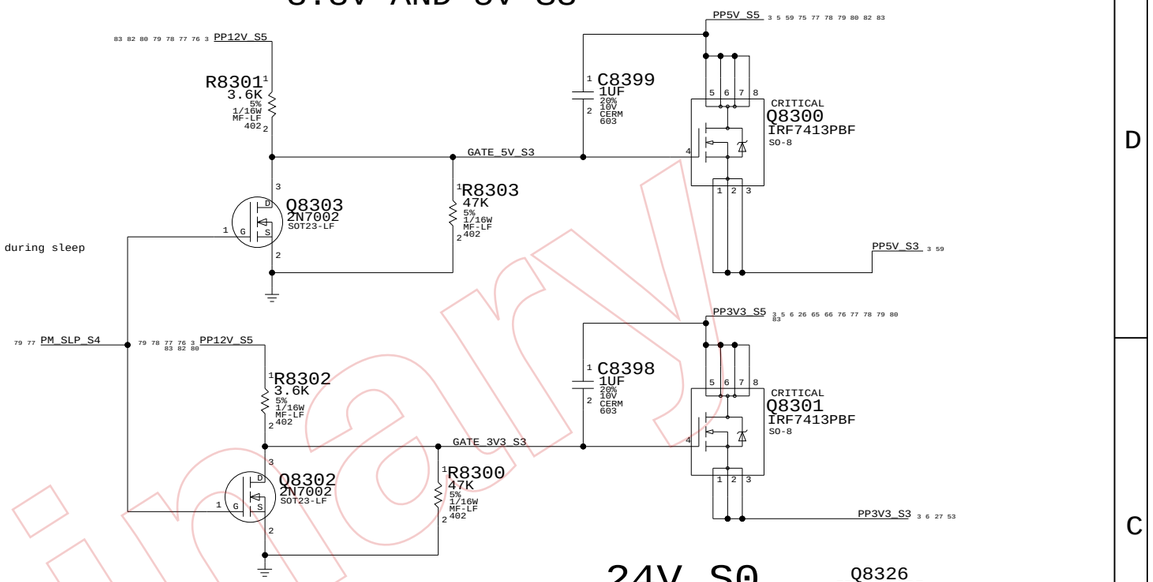
3.3V S0



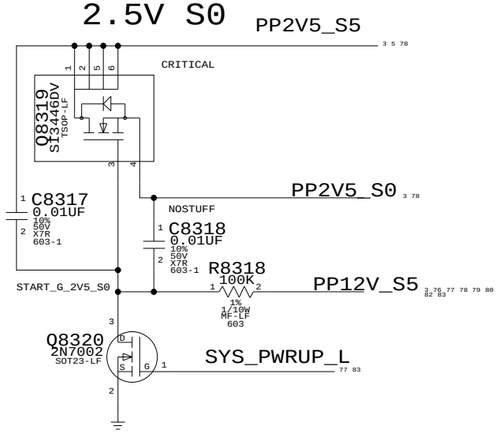
1.8V S0



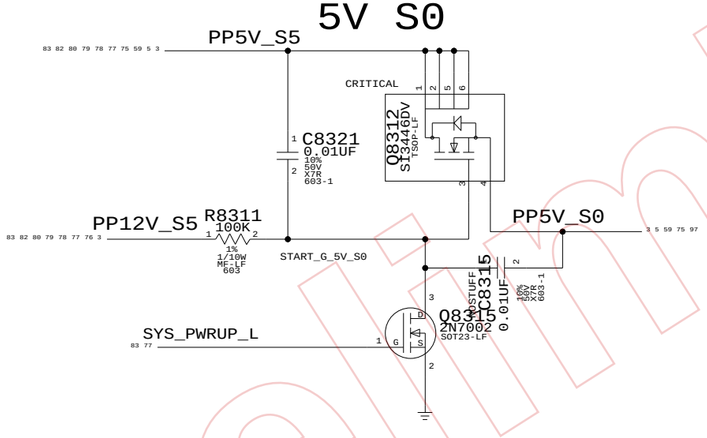
3.3V AND 5V S3



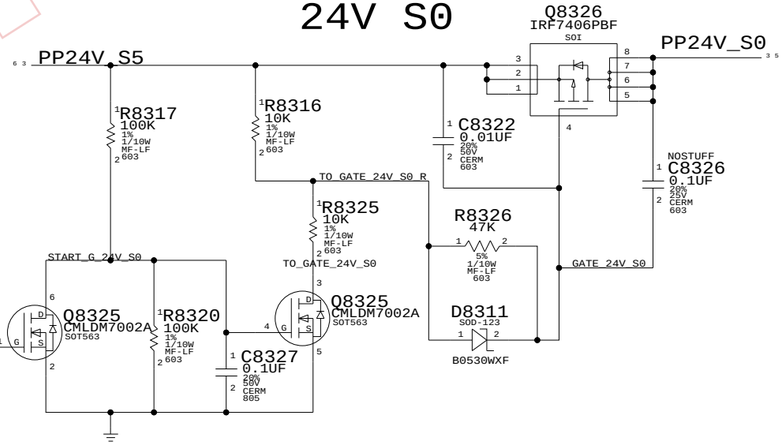
2.5V S0



5V S0

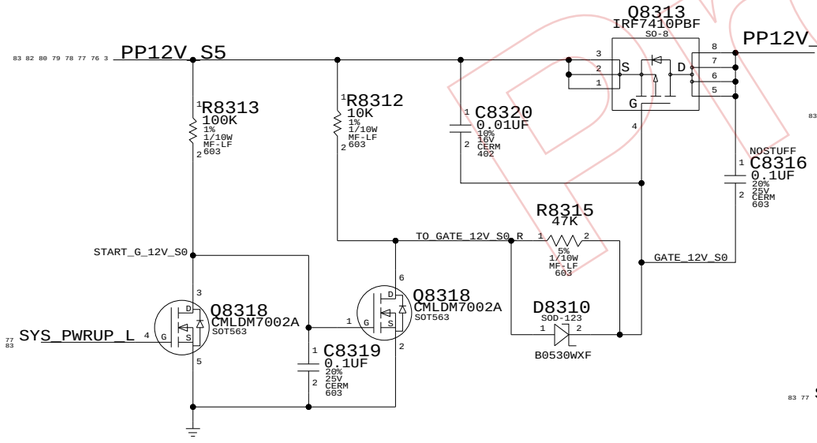


24V S0

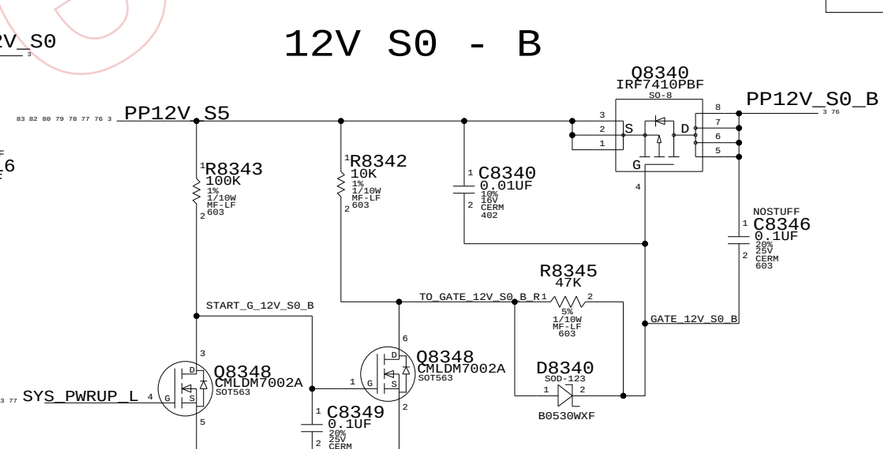


12V S0

Split 12V S0 is for better power plane structure
12VS0 - B will connect to MXM, Audio, Fans



12V S0 - B



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 83 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

MXM PWRSRC (GPU CORE) CURRENT SENSE

=PPV_S0_MXM_PWRSRC → CRITICAL R8450 0.025 1% 1W MF 2512-1 → PPV_S0_MXM_PWRSRC

PCB:KEEP SHORTS NEXT TO U8450
PCB:PLACE D8450,R8452,C8458 BY SMC

MXM_PWR_SENSE
CRITICAL U8450 ZXCT1010 SOT23-5
VIN, NC, GND, IOUT, LOAD

PP3V3_S0 → D8450 BAS16-75V-0.25A SOT23-LF (NOSTUFF) → TO SMC

OMIT XW8450 SM

MXM_PWR_SENSE R8452 4.53K 1% 1/16W MF-LF 402 → SMC_GPU_ISENSE

MXM_PWR_SENSE R8451 3.01K 1% 1/16W MF-LF 402

MXM_PWR_SENSE C8458 0.22UF 20% 6.3V X5R 402 — 1MS TIME CONSTANT SO SMC ADC SAMPLING WORKS WELL.

GND_SMC_AVSS

SCALE	COUNT
1.33333 A/V	.004296875 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

MXM PWRSRC VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

PPV_S0_MXM_PWRSRC

MXM_PWR_SENSE R8453 6.04K 1% 1/16W MF-LF 402

MXM_PWR_SENSE R8454 2.0K 1% 1/16W MF-LF 402

SMC_MXM_VSENSE_R

MXM_PWR_SENSE R8455 4.53K 1% 1/16W MF-LF 402 → SMC_GPU_VSENSE

PCB: PLACE R8455, C8459 WITHIN 1" OF SMC (U5800)

MXM_PWR_SENSE C8459 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

SCALE	COUNT
4 V/V	.0129 V/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

J8400 AS0B326-S55N-7F F-RT-SM (1 OF 2)

CRITICAL

=PP1V8_S0_MXM
C8401 22UF 20% 6.3V X5R 805
C8402 22UF 20% 6.3V X5R 805 NOSTUFF
C8403 22UF 20% 6.3V X5R 805 NOSTUFF
C8400 22UF 20% 35V ELEC SM-LF
PPV_S0_MXM_PWRSRC (VOLTAGE=12V, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.25MM)
=PP5V_S0_MXM
ALL_SYS_PWRGD

PLACE CAPS NEAR NB

PRSNT2_L: RESERVED FOR FUTURE USE

KEY

1V8RUN0	2	PWR_SRC0	1				
1V8RUN1	4	PWR_SRC1	3				
1V8RUN2	6	PWR_SRC2	5				
1V8RUN3	8	PWR_SRC3	7				
1V8RUN4	10	PWR_SRC4	9				
1V8RUN5	12	PWR_SRC5	11				
1V8RUN6	14	PWR_SRC6	13				
RUNPWROK	16	PWR_SRC7	15				
5VRUN	18	GND0	17				
GND20	20	GND1	19				
GND21	22	GND2	21				
GND22	24	GND3	23				
PRSNT2_L	38	PEX_RX15_L	37	PEG_R2D_C_P<1>	C8420 0.1uF	PEG_R2D_P<15>	PEG_D2R_P<0>
PEX_TX15_L	40	PEX_RX15	39	PEG_R2D_C_N<1>	C8421 0.1uF	PEG_R2D_N<15>	PEG_D2R_N<0>
PEX_TX15	42	GND4	41				
GND23	44	PEX_RX14_L	43	PEG_R2D_C_P<1>	C8422 0.1uF	PEG_R2D_P<14>	PEG_D2R_P<1>
PEX_TX14_L	46	PEX_RX14	45	PEG_R2D_C_N<1>	C8423 0.1uF	PEG_R2D_N<14>	PEG_D2R_N<1>
PEX_TX14	48	GND5	47				
GND24	50	PEX_RX13_L	49	PEG_R2D_C_P<2>	C8424 0.1uF	PEG_R2D_P<13>	PEG_D2R_P<2>
PEX_TX13_L	52	PEX_RX13	51	PEG_R2D_C_N<2>	C8425 0.1uF	PEG_R2D_N<13>	PEG_D2R_N<2>
PEX_TX13	54	GND6	53				
GND25	56	PEX_RX12_L	55	PEG_R2D_C_P<3>	C8426 0.1uF	PEG_R2D_P<12>	PEG_D2R_P<3>
PEX_TX12_L	58	PEX_RX12	57	PEG_R2D_C_N<3>	C8427 0.1uF	PEG_R2D_N<12>	PEG_D2R_N<3>
PEX_TX12	60	GND7	59				
GND26	62	PEX_RX11_L	61	PEG_R2D_C_P<4>	C8428 0.1uF	PEG_R2D_P<11>	PEG_D2R_P<4>
PEX_TX11_L	64	PEX_RX11	63	PEG_R2D_C_N<4>	C8429 0.1uF	PEG_R2D_N<11>	PEG_D2R_N<4>
PEX_TX11	66	GND8	65				
GND27	68	PEX_RX10_L	67	PEG_R2D_C_P<5>	C8430 0.1uF	PEG_R2D_P<10>	PEG_D2R_P<5>
PEX_TX10_L	70	PEX_RX10	69	PEG_R2D_C_N<5>	C8431 0.1uF	PEG_R2D_N<10>	PEG_D2R_N<5>
PEX_TX10	72	GND9	71				
GND28	74	PEX_RX9_L	73	PEG_R2D_C_P<6>	C8432 0.1uF	PEG_R2D_P<9>	PEG_D2R_P<6>
PEX_TX9_L	76	PEX_RX9	75	PEG_R2D_C_N<6>	C8433 0.1uF	PEG_R2D_N<9>	PEG_D2R_N<6>
PEX_TX9	78	GND10	77				
GND29	80	PEX_RX8_L	79	PEG_R2D_C_P<7>	C8434 0.1uF	PEG_R2D_P<8>	PEG_D2R_P<7>
PEX_TX8_L	82	PEX_RX8	81	PEG_R2D_C_N<7>	C8435 0.1uF	PEG_R2D_N<8>	PEG_D2R_N<7>
PEX_TX8	84	GND11	83				
GND30	86	PEX_RX7_L	85	PEG_R2D_C_P<8>	C8436 0.1uF	PEG_R2D_P<7>	PEG_D2R_P<8>
PEX_TX7_L	88	PEX_RX7	87	PEG_R2D_C_N<8>	C8437 0.1uF	PEG_R2D_N<7>	PEG_D2R_N<8>
PEX_TX7	90	GND12	89				
GND31	92	PEX_RX6_L	91	PEG_R2D_C_P<9>	C8438 0.1uF	PEG_R2D_P<6>	PEG_D2R_P<9>
PEX_TX6_L	94	PEX_RX6	93	PEG_R2D_C_N<9>	C8439 0.1uF	PEG_R2D_N<6>	PEG_D2R_N<9>
PEX_TX6	96	GND13	95				
GND32	98	PEX_RX5_L	97	PEG_R2D_C_P<10>	C8440 0.1uF	PEG_R2D_P<5>	PEG_D2R_P<10>
PEX_TX5_L	100	PEX_RX5	99	PEG_R2D_C_N<10>	C8441 0.1uF	PEG_R2D_N<5>	PEG_D2R_N<10>
PEX_TX5	102	GND14	101				
GND33	104	PEX_RX4_L	103	PEG_R2D_C_P<11>	C8442 0.1uF	PEG_R2D_P<4>	PEG_D2R_P<11>
PEX_TX4_L	106	PEX_RX4	105	PEG_R2D_C_N<11>	C8443 0.1uF	PEG_R2D_N<4>	PEG_D2R_N<11>
PEX_TX4	108	GND15	107				
GND34	110	PEX_RX3_L	109	PEG_R2D_C_P<12>	C8444 0.1uF	PEG_R2D_P<3>	PEG_D2R_P<12>
PEX_TX3_L	112	PEX_RX3	111	PEG_R2D_C_N<12>	C8445 0.1uF	PEG_R2D_N<3>	PEG_D2R_N<12>
PEX_TX3	114	GND16	113				
GND35	116	PEX_RX2_L	115	PEG_R2D_C_P<13>	C8446 0.1uF	PEG_R2D_P<2>	PEG_D2R_P<13>
PEX_TX2_L	118	PEX_RX2	117	PEG_R2D_C_N<13>	C8447 0.1uF	PEG_R2D_N<2>	PEG_D2R_N<13>
PEX_TX2	120	GND17	119				
GND36	122	PEX_RX1_L	121	PEG_R2D_C_P<14>	C8448 0.1uF	PEG_R2D_P<1>	PEG_D2R_P<14>
PEX_TX1_L	124	PEX_RX1	123	PEG_R2D_C_N<14>	C8449 0.1uF	PEG_R2D_N<1>	PEG_D2R_N<14>
PEX_TX1	126	GND18	125				
GND37	128	PEX_RX0_L	127	PEG_R2D_C_P<15>	C8450 0.1uF	PEG_R2D_P<0>	PEG_D2R_P<15>
PEX_TX0_L	130	PEX_RX0	129	PEG_R2D_C_N<15>	C8451 0.1uF	PEG_R2D_N<0>	PEG_D2R_N<15>
PEX_TX0	132	GND19	131				

MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 84 OF 97	

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
(NONE)

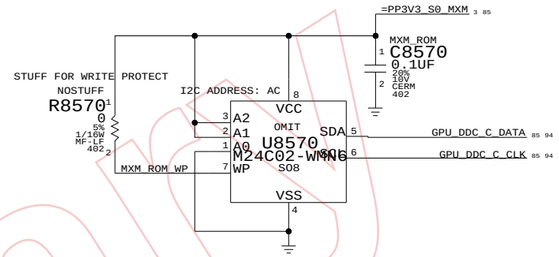
MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

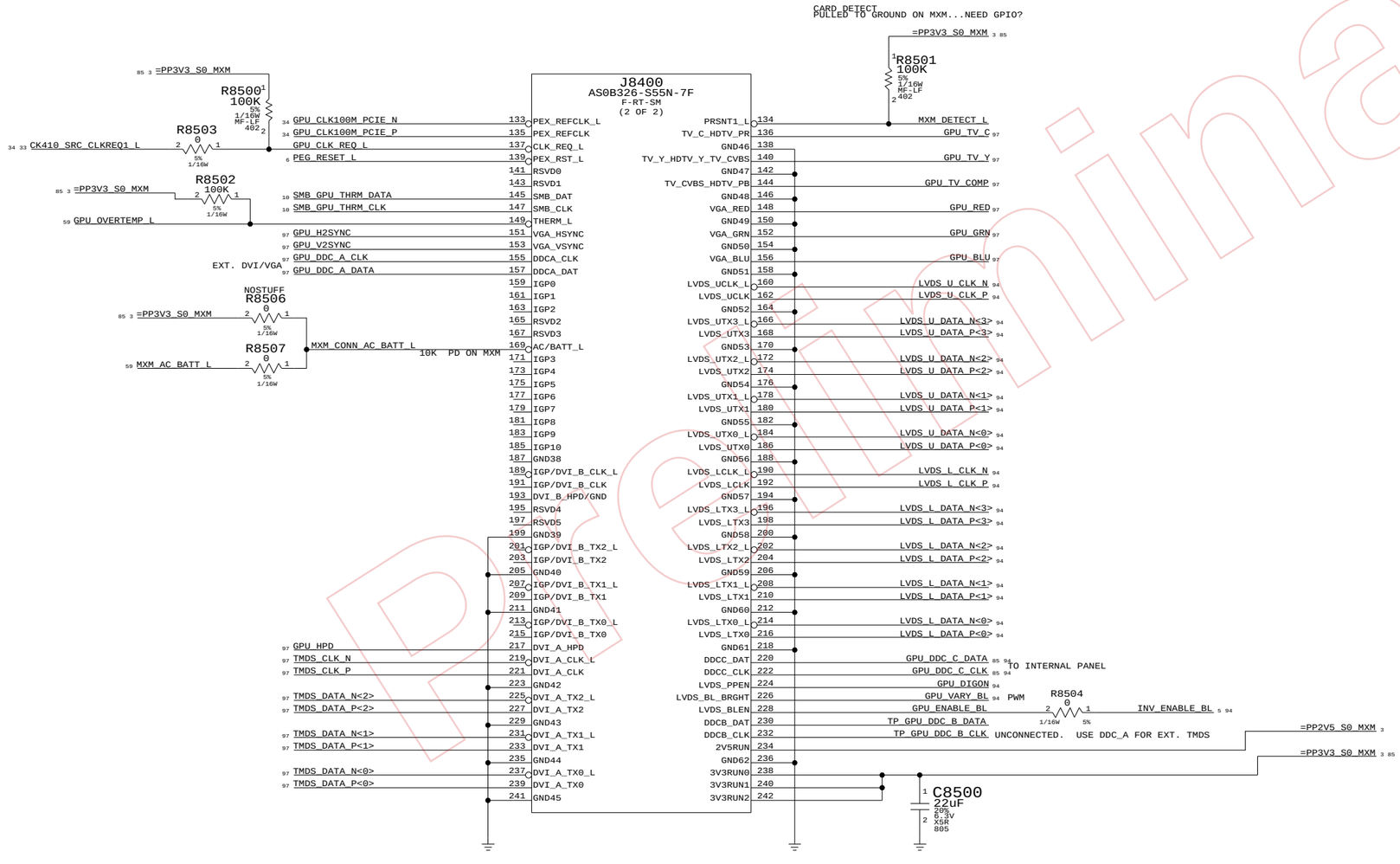
VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



CARD DETECT
PULLED TO GROUND ON MXM...NEED GPIO?



MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 85 OF 97	

Page Notes

Power aliases required by this page:
- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

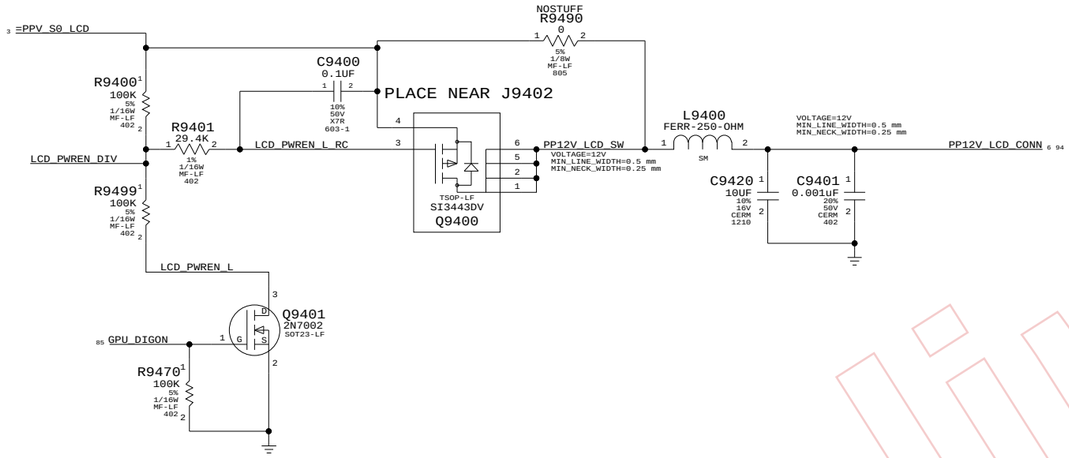
Signal aliases required by this page:
(NONE)

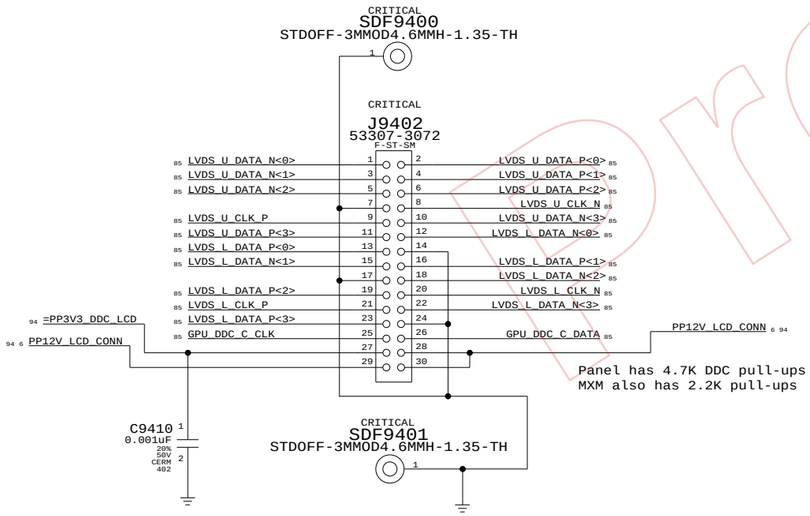
BOM options provided by this page:
(NONE)

97 94 3 =PP3V3_S0_VIDEO ═══ =PP3V3_DDC_LCD 94

LCD (LVDS) INTERFACE

PANEL POWER SEQUENCING

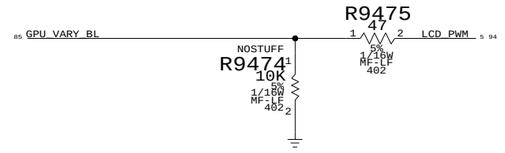




Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

INVERTER INTERFACE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS



Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 94 OF 97	

DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

TMDS_DATA_N<0> — R9700 0 (NOSTUFF) — L9700 90-OHM CRITICAL — TMDS_CONN_DN<0>
TMDS_DATA_P<0> — R9702 0 (NOSTUFF) — TMDS_CONN_DP<0>
TMDS_DATA_N<1> — R9703 0 (NOSTUFF) — L9701 90-OHM CRITICAL — TMDS_CONN_DN<1>
TMDS_DATA_P<1> — R9705 0 (NOSTUFF) — TMDS_CONN_DP<1>
TMDS_DATA_N<2> — R9704 0 (NOSTUFF) — L9702 90-OHM CRITICAL — TMDS_CONN_DN<2>
TMDS_DATA_P<2> — R9709 0 (NOSTUFF) — TMDS_CONN_DP<2>
TMDS_CLK_N — R9708 0 (NOSTUFF) — L9703 90-OHM CRITICAL — TMDS_CONN_CLKN
TMDS_CLK_P — R9715 0 (NOSTUFF) — TMDS_CONN_CLKP

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

PP5V_S0 — D9710 SOD-123 B0530WXF — PP5V_S0_DDC_DIODE — F9710 0.5AMP-13.2V SM-LF CRITICAL — PP5V_S0_DDC_FUSE — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC

VOLTAGE=5V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

J9710 MINI-DVI-M51 F-ST-SM CRITICAL

DVI_HPD_UF	25	1	TMDS_CONN_DP<2>
	17	9	
DVI_DDC_CLK_UF	26	2	TMDS_CONN_DN<2>
DVI_DDC_DATA_UF	18	10	
	27	3	TMDS_CONN_DP<1>
	19	11	
	28	4	TMDS_CONN_DN<1>
VGA_BLU	20	12	
VGA_HSYNC	29	5	TMDS_CONN_DP<0>
		13	
	30	6	TMDS_CONN_DN<0>
VGA_GRN	22	14	
VGA_VSYNC	31	7	TMDS_CONN_CLKP
		15	
	32	8	TMDS_CONN_CLKN
VGA_RED	24	16	

DVI_CHASSIS 33 — C9720 0.1UF 10% 16V X5R 402 — C9721 0.1UF 10% 16V X5R 402 — GND_CHASSIS_DVI 6

PLACE CLOSE TO MINI-DVI CONNECTOR 3V LEVEL SHIFTERS

PP5V_S0_DDC — R9710 4.7K 5% 1/16W MF-LF 402 — R9712 4.7K 5% 1/16W MF-LF 402

=PP3V3_S0_VIDEO — R9720 10K 5% 1/10W MF-LF 402 — R9721 10K 5% 1/10W MF-LF 402

DVI_DDC_CLK_UF — R9711 100 5% 1/16W MF-LF 402 — Q9711 2N7002DW-X-F SOT-363 — DVI_DDC_CLK — GPU_DDC_A_CLK
C9711 100pF 5% 50V CERM 402

DVI_DDC_DATA_UF — R9713 100 5% 1/16W MF-LF 402 — Q9711 2N7002DW-X-F SOT-363 — DVI_DDC_DATA — GPU_DDC_A_DATA
C9713 100pF 5% 50V CERM 402

DVI_HPD_UF — R9714 0 5% 1/16W MF-LF 402 — GPU_HPD

C9710 0.01uF 20% 50V CERM 603
C9714 100pF 5% 50V CERM 402

NOSTUFF R9722 100K 5% 1/16W MF-LF 402 — NOSTUFF D9700 CASE425 MMSZ4681XXG

Note: this clamp is supposed to be on the MXM card

=PP3V3_S0_VIDEO

C9730 0.1UF 20% 10V CERM 402 — C9731 10uF 20% 6.3V CERM 805-1

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR

U9730 TS3V330 SOP CRITICAL

VIDEO_MUX_RED	DA	S1A	GPU_TV_C
VIDEO_MUX_GRN	DB	S2A	GPU_RED
		S1B	GPU_TV_Y
VIDEO_MUX_BLU	DC	S2B	GPU_GRN
		S1C	GPU_TV_COMP
NC	DD	S2C	GPU_BLU
		S1D	NC
SB_CRT_TVOUT_MUX	IN	S2D	NC
	EN_L		
	GND		
	VCC		

GPU_V2SYNC — U9760 74LC125 TSSOP — R9760 33 5% 1/10W MF-LF 402 — GPU_VSYNC_BUF — VGA_VSYNC
C9760 0.1UF 20% 10V CERM 402

GPU_H2SYNC — U9760 74LC125 TSSOP — R9761 33 5% 1/16W MF-LF 402 — GPU_HSYNC_BUF — VGA_HSYNC
C9762 22PF 5% 50V CERM 402 — C9763 22PF 5% 50V CERM 402

DISABLE UNUSED BUFFERS

U9760 74LC125 TSSOP — U9760 74LC125 TSSOP

=PP3V3_S0_VIDEO

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

VIDEO_MUX_BLU — R9740 150 1% 1/16W MF-LF 402 — FL9740 LCFILTER CRITICAL SM-220MHZ-LF — VGA_BLU
C9740 3.3pF 0.25% 50V CERM 402

VIDEO_MUX_GRN — R9741 150 1% 1/16W MF-LF 402 — FL9741 LCFILTER CRITICAL SM-220MHZ-LF — VGA_GRN
C9741 3.3pF 0.25% 50V CERM 402

VIDEO_MUX_RED — R9742 150 1% 1/16W MF-LF 402 — FL9742 LCFILTER CRITICAL SM-220MHZ-LF — VGA_RED
C9742 3.3pF 0.25% 50V CERM 402

CHECK MXM VENDOR RECOMMENDATIONS FOR FILTER

External Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE: NONE	SHT 97 OF 97	