

M38A - PVT

09/27/06

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
D		464236	PRODUCTION RELEASED	09/27/06	06/22/04

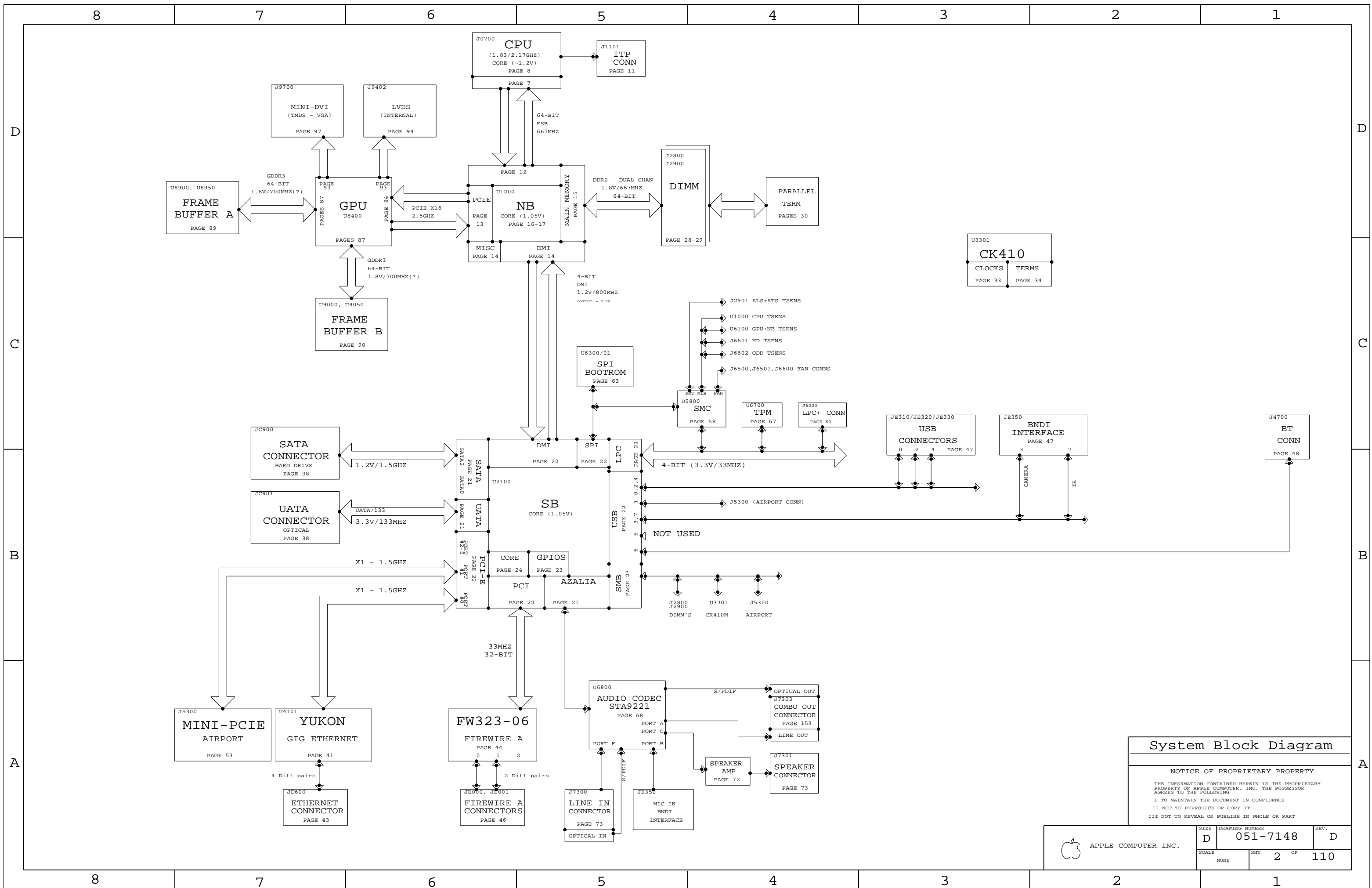
PAGE	DRI	PDF	CIRCUIT	
1	JD	JD	1	TABLE OF CONTENTS
2	JD	JD	2	SYSTEM BLOCK DIAGRAM
3	RT	RT	3	POWER BLOCK DIAGRAM
4	JD	JD	4	TABLE ITEMS & REVISION HISTORY
5	JD	JD	5	FUNC TEST
6	RT	RT	6	POWER CONNECTOR / POWER ALIAS
(M42) 7	MS	JD	7	CPU - BUS INTERFACE
(M42) 8	MS	JD	8	CPU - PWR & GND
9	MS	JD	9	CPU - DECAPS
(M42) 10	MS	JD	10	CPU - THERMAL SENSOR
M42 11	MS	JD	11	CPU - ITP CONN
M1 12	PS	JH	12	NB - CPU INTERFACE
M1 13	PS	JH	13	NB - VIDEO INTERFACE
14	PS	JH	14	NB - MISC INTERFACES
M1 15	PS	JH	15	NB - DDR2 INTERFACE
M1 16	PS	JH	16	NB - POWER 1
M1 17	PS	JH	17	NB - POWER 2
M1 18	PS	JH	18	NB - GROUNDS
19	PS	JH	19	NB - DECAPS
M1 20	PS	JH	20	NB - CONFIG STRAPS
21	JD	JD	21	SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	JD	22	SB - PCIE, SPI, USB, DMI, PCI
23	JD	JD	23	SB - SMB, GPIO, PM, CLKS
24	JD	JD	24	SB - POWERS AND GROUNDS
25	JD	JD	25	SB - DECAPS
26	JD	JD	26	SB - MISC
27	JD	JD	27	SB - SMB BUS CONNECTIONS
28	PS	JD	28	DDR2 - SO-DIMM CONN A
29	PS	JD	29	DDR2 - SO-DIMM CONN B (REVERSED)
30	PS	JD	30	DDR2 - TERMINATION
M1 31	RT	RT	31	DDR2 - VTT SUPPLY
M42 33	JD	JD	32	CLOCKS - GENERATOR
34	JD	JD	33	CLOCKS - TERMINATIONS
38	JD	JD	34	ATA (SATA AND IDE) CONN'S
(M42) 41	JD	JD	35	LAN - YUKON'S PCIE INTERFACE
42	JD	JD	36	LAN - YUKON'S PWR, MISC
43	JD	JD	37	LAN - CONN
44	JD	JD	38	FIREWIRE - FW323-06
45	JD	JD	39	FIREWIRE - DECAPS
46	JD	JD	40	FIREWIRE - CONN'S
47	JD	JD	41	USB - CONN'S

PAGE	DRI	PDF	CIRCUIT	
53	JD	JD	43	PCI-E - AIRPORT MINI-PCIE CONN
54	JD	JD	44	PCI-E - UNUSED PORTS
58	MS	MS	45	SMC - H8S2116
59	MS	MS	46	SMC - SMB BUSSES, MISC
60	MS	MS	47	SMC - LPC+ CONN
61	JH	JH	48	SMC - GPU/NB THERMAL SENSOR
RX 63	MS	JD	49	SMC - SPI BOOTROM
65	MS	MS	50	SMC - FANS
66	MS	MS	51	SMC - FANS
67	JD	JD	52	SMC - TPM
SO 68	PT	JD	53	AUDIO - CODEC, VREG, MIC BIAS
SO 72	PT	JD	54	AUDIO - INTERNAL SPEAKER AMP
SO 73	PT	JD	55	AUDIO - I/O CONN'S, EMC
SO 74	PT	JD	56	AUDIO - DETECT TRANSLATORS
RP 75	RT	RT	57	VR - CPU CORE
RP 76	RT	RT	58	VR - CPU I-V SENSE CKT
RP 77	RT	RT	59	VR - "S0" 1.2V & 2.5V (GRAFIX)
RP 78	RT	RT	60	VR - "S0" 1.8V
RP 79	RT	RT	61	VR - "S3" 1.8V
RP 80	RT	RT	62	VR - "S0" 1.5V
RP 81	RT	RT	63	VR - "S0" 1.05V
RP 83	RT	RT	64	VR - "S3" 3.3V AND 5V
JH 84	JH	JH	65	GPU - M56 PCI-E
M1 85	JH	JH	66	GPU - VCORE SUPPLY
M1 86	JH	JH	67	GPU - M56 CORE PWR
M1 87	JH	JH	68	GPU - M56 FRAME BUFFER
M1 88	JH	JH	69	GPU - MISC
M1 89	JH	JH	70	GPU - GDDR SDRAM A
M1 90	JH	JH	71	GPU - GDDR SDRAM B
M1 91	JH	JH	72	GPU - M56 GPIO, DVO, MISC
M1 92	JH	JH	73	GPU - M56 CLOCKS
M1 93	JH	JH	74	GPU - M56 VIDEO INTERFACES
JH 94	JH	JH	75	GPU - INTERNAL DISPLAY CONN'S
JH 95	JH	JH	76	GPU - TP'S
JH 96	JH	JH	77	GPU - TMDS, INVERTER, EXT VGA
JH 97	JH	JH	78	GPU - EXTERNAL DISPLAY CONN'S

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<div style="text-align: right;"> <p>Apple Computer Inc.</p> </div> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small; text-align: center;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small; text-align: center;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <div style="text-align: center;"> <p>TITLE</p> <p style="font-size: large;">SCH, MLB, M38A</p> </div> <div style="display: flex; justify-content: space-between;"> <div style="font-size: x-small;"> <p>DRAWING NUMBER</p> <p style="font-size: large;">051-7148</p> </div> <div style="font-size: x-small;"> <p>REV.</p> <p style="font-size: large;">D</p> </div> </div>
<p>RELEASE</p> <p>MATERIAL/FINISH NOTED AS APPLICABLE</p>	<p>SCALE</p> <p>NONE</p> <p>SIZE</p> <p>D</p>	<p>DRAPTER</p> <p>DESIGN CK</p> <p>ENG APPD</p> <p>MFG APPD</p> <p>QA APPD</p> <p>DESIGNER</p>
<p>SHT 1 OF 110</p>		

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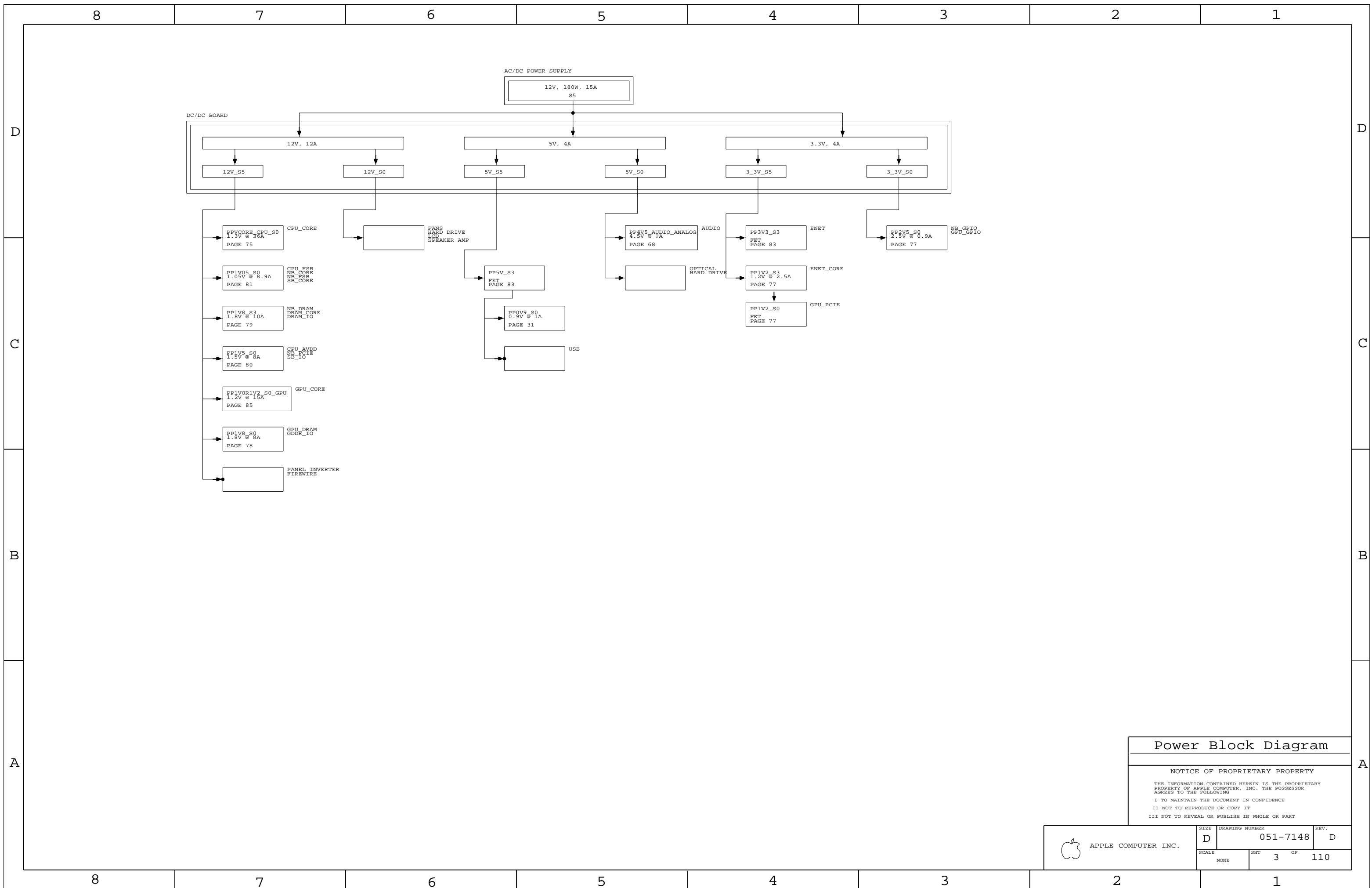


System Block Diagram

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	D	051-7148	D
SCALE	SHT	OF	REV.
NONE	2	110	



Power Block Diagram

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	3	110	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
338S0344	1	IC,ATI,M56P,GRAPHIC,880BGA,LF	U8400	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,SMD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	

341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1235 353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

128S0078	3	CAP,EL,AL,330UF,20V,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	
825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
155S0289	7	EMI CHOKE	FLR011,FLR021,FL4610,FL4620,L4712,L4722,L4732	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16C680EX 680UF 16V LP
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330F8 330UF 6.3V LP
128S0080	128S0078		C7517,C7518,C7910	SANYO 16SV330W 330UF 16V SMD LP
124-0338	124-0333		C7501,C8014	CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
353S1321	353S1105		U7910	LM339
378S0141	378S0140		LED01,LED602,LED603	SMD

353S1461	353S1465		U7500	CPU REGULATOR - ISL9504
138S0598	138S0512			SAMSUNG

155S0232	155S0289		FLR011,FLR021,FL4610,FL4620,L4712,L4722,L4732	EMI CHOKE
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7148	1	PCB,SCHM,MLB,M38A	SCH1		17_INCH_LCD
820-2052	1	PCB,FAB,MLB,M38A	MLB1		17_INCH_LCD
(341S1908 - DEVEL) (341S1909 - FINAL) (335S0384 - BLNK) 341T0040	1	EFI ROM,M38A	U6301	CRITICAL	17_INCH_LCD
114S0264	1	3.01K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P2V
(341S1907 - PROG) (338S0274 - BLNK) 341T0039	1	IC,SMC,M38A	U5800	CRITICAL	17_INCH_LCD
338S0315	1	IC,ATI,M56LP,GRAPHIC,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
114S0287	1	5.11K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_0P953V
114S0281	1	4.53K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P0V
337S3388	1	2.00GHZ MEROM	CPU	CRITICAL	2P00_CPU
337S3390	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

Table Items

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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7148 REV. D

SCALE NONE SH 4 OF 110

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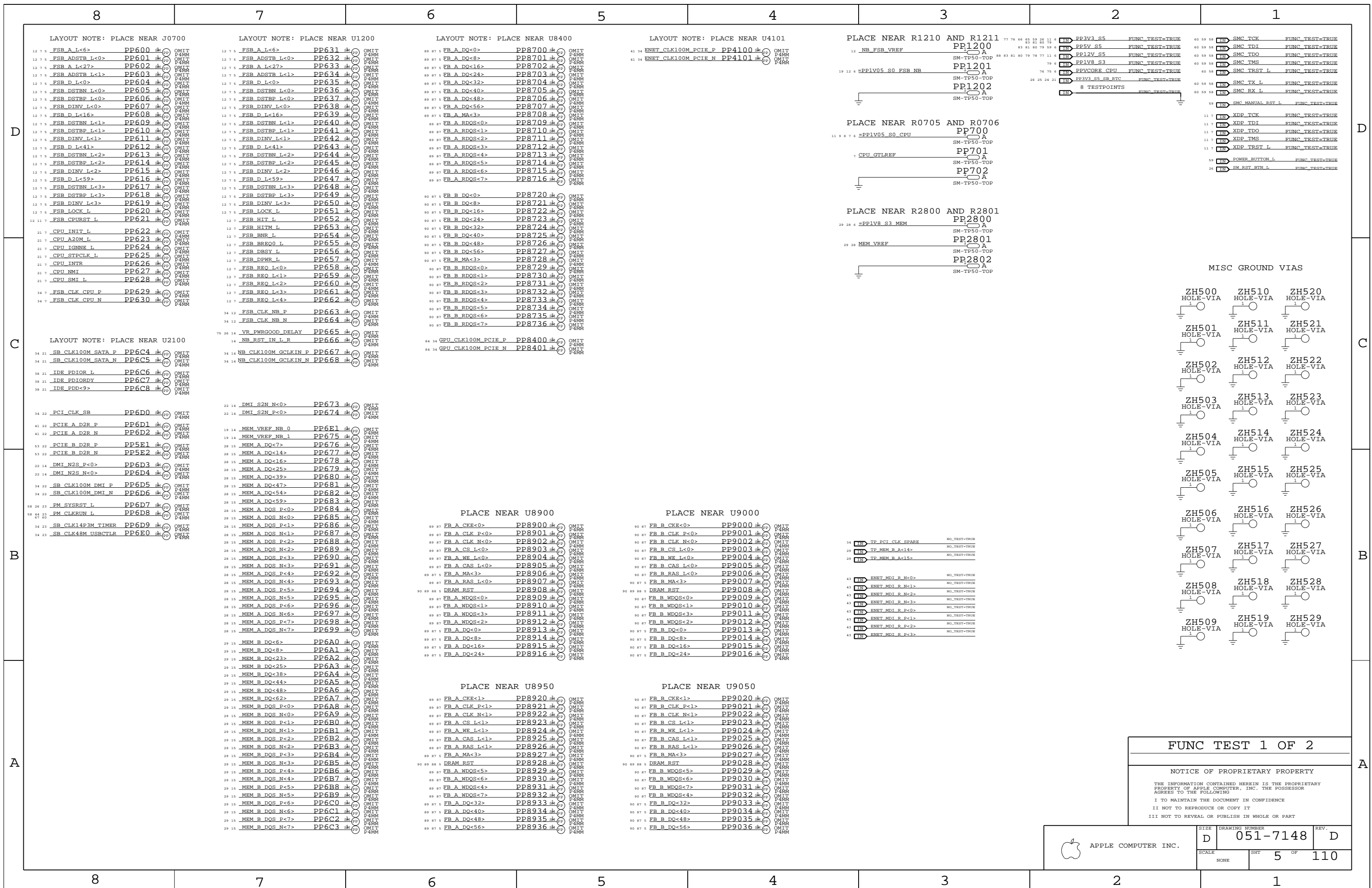
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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

LAYOUT NOTE: PLACE NEAR U2100

PLACE NEAR U8900

PLACE NEAR U9000

PLACE NEAR U8950

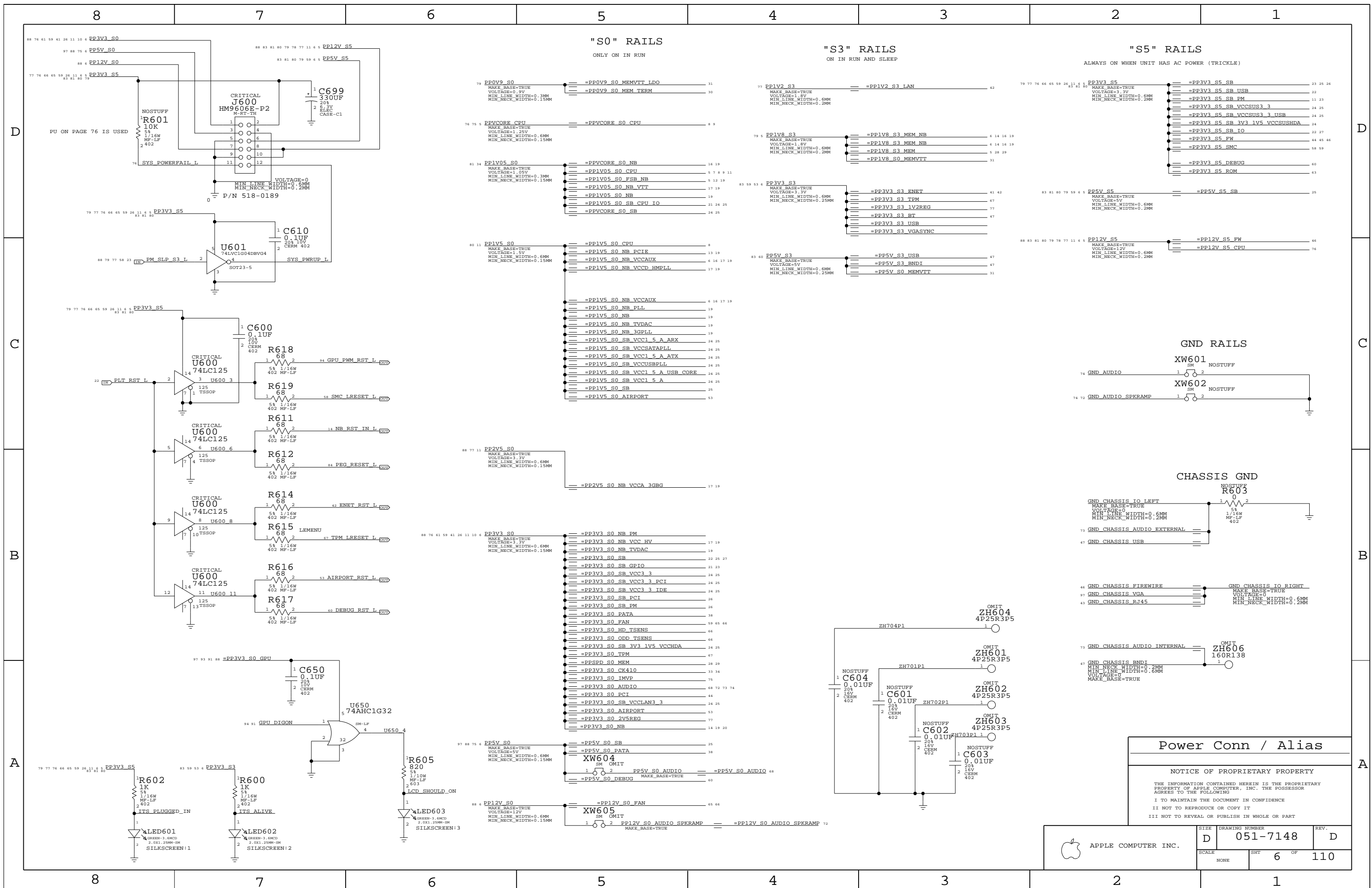
PLACE NEAR U9050

FUNC TEST 1 OF 2

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SCALE	SHEET	OF	TOTAL
NONE	5	110	

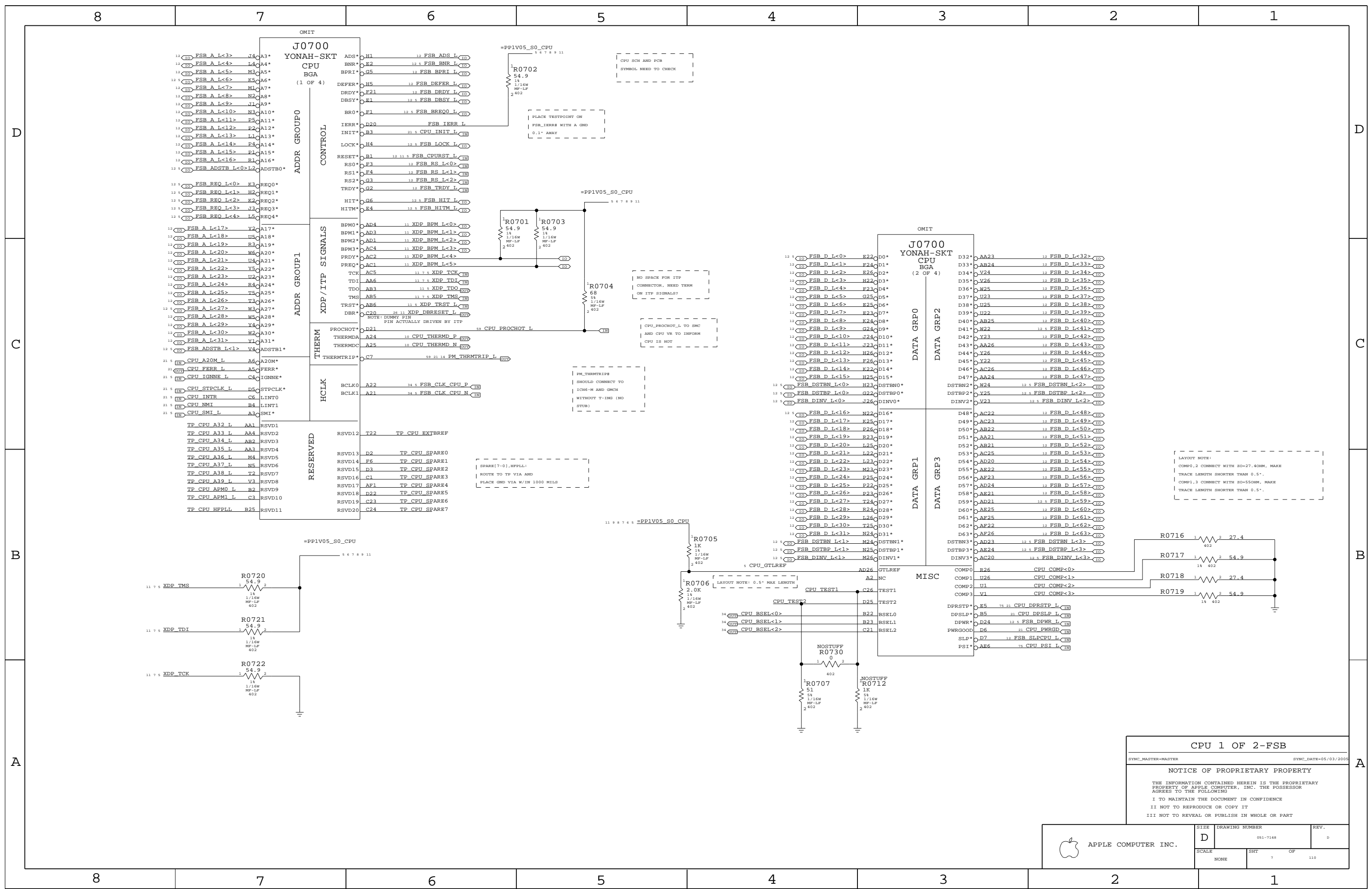


Power Conn / Alias

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	SCALE NONE	SHEET 6	OF 110



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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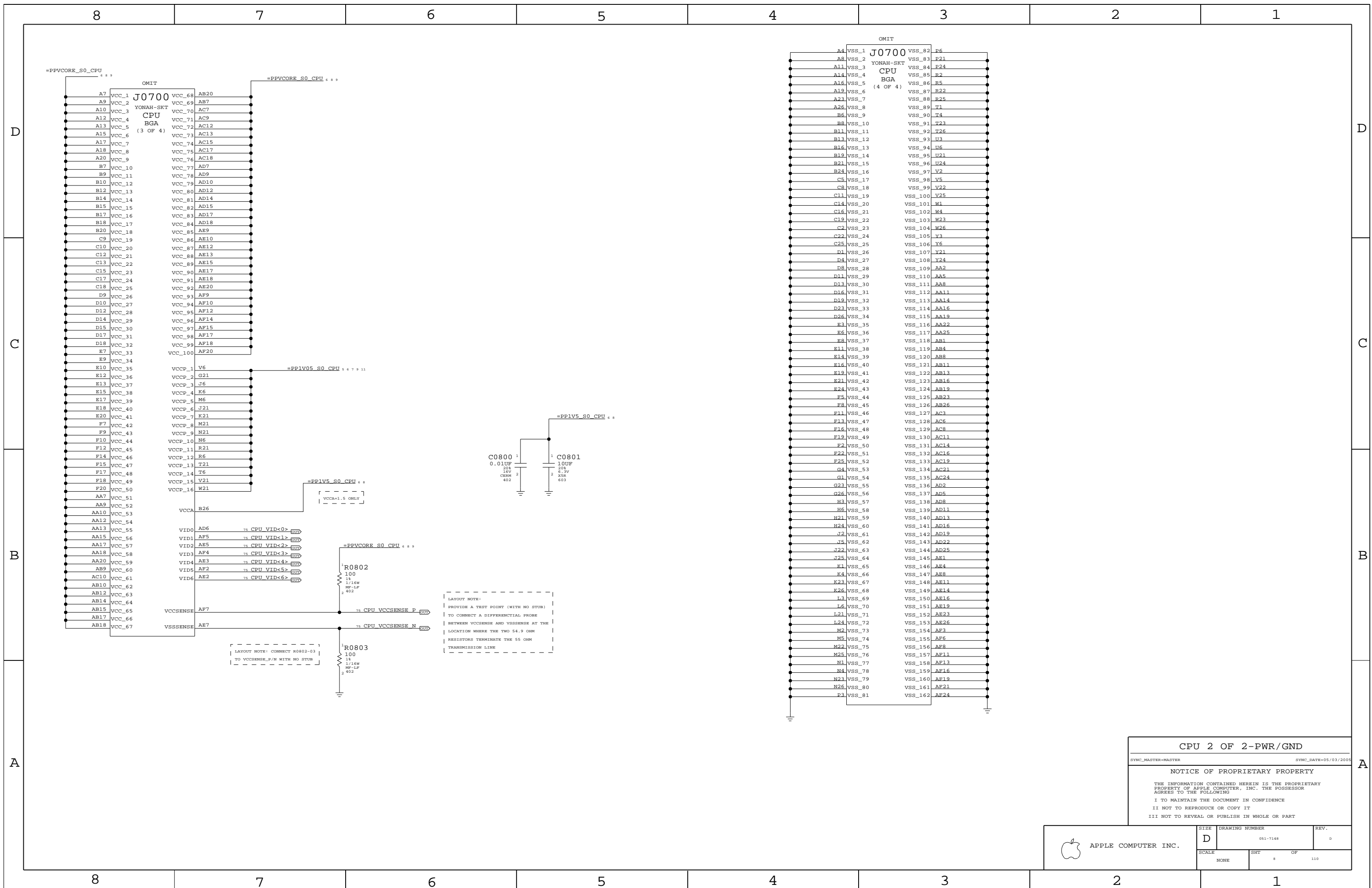
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	SCALE NONE	SHEET 7	OF 110



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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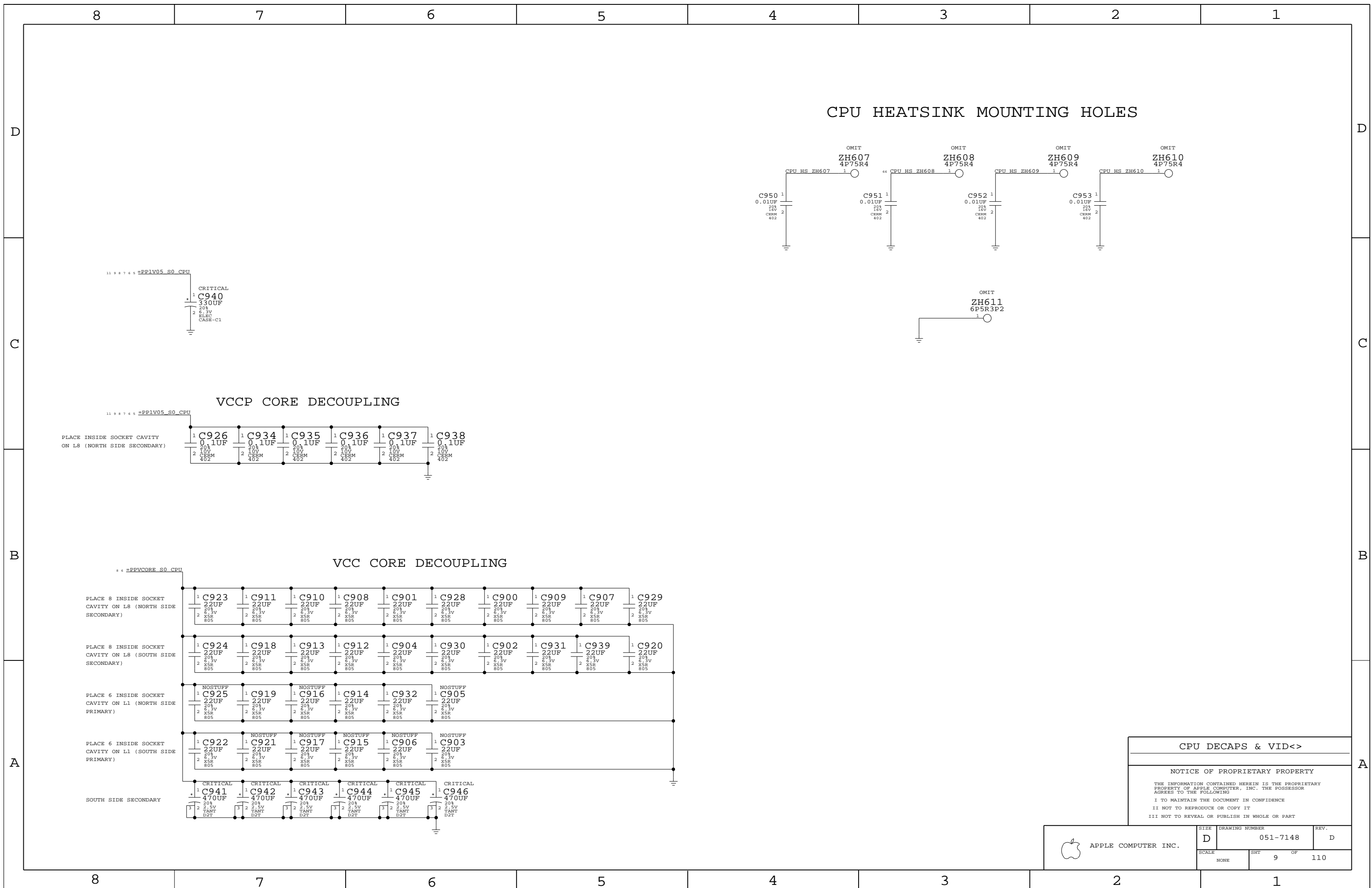
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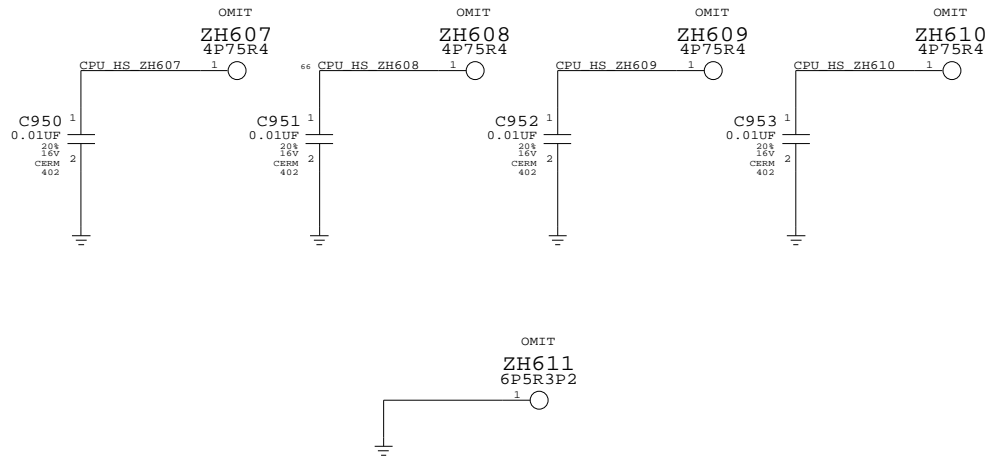
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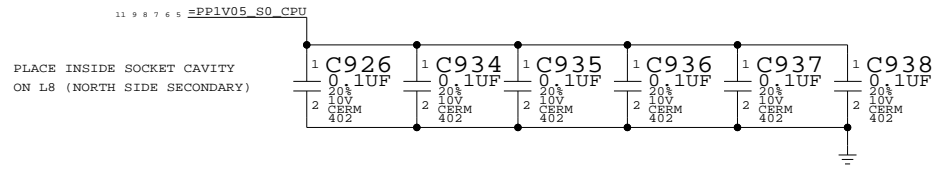
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SCALE	SHT		OF
NONE	8		110



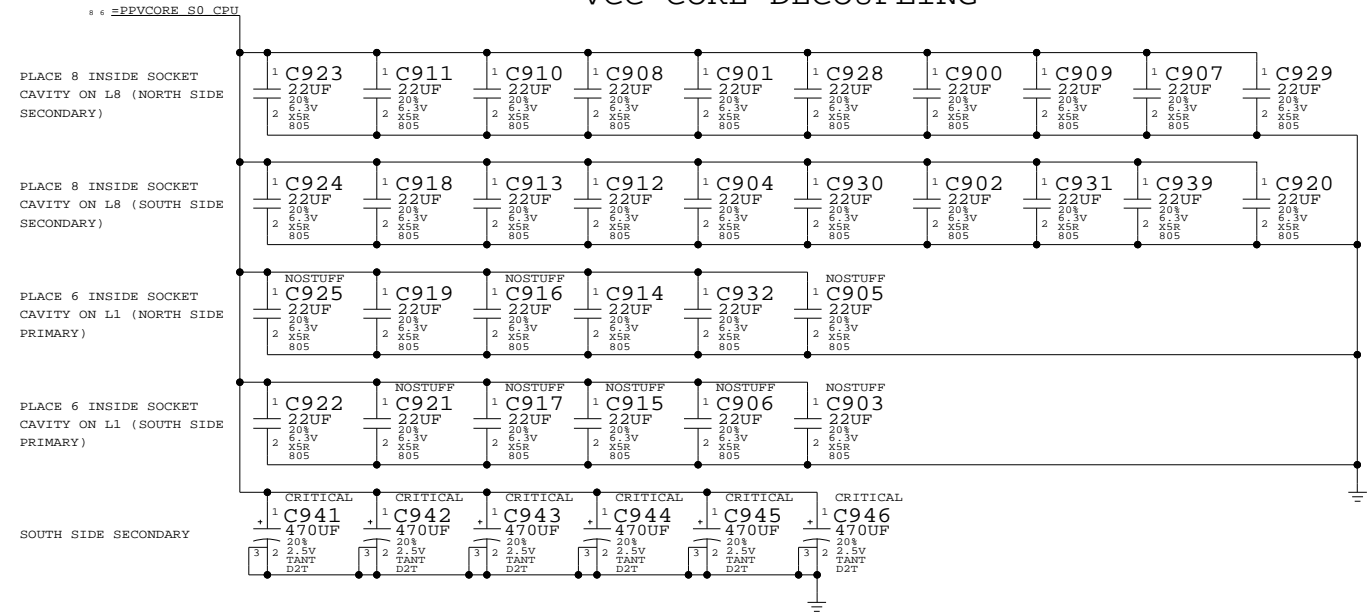
CPU HEATSINK MOUNTING HOLES



VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

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SCALE	SHT	OF	REV.
NONE	9	110	

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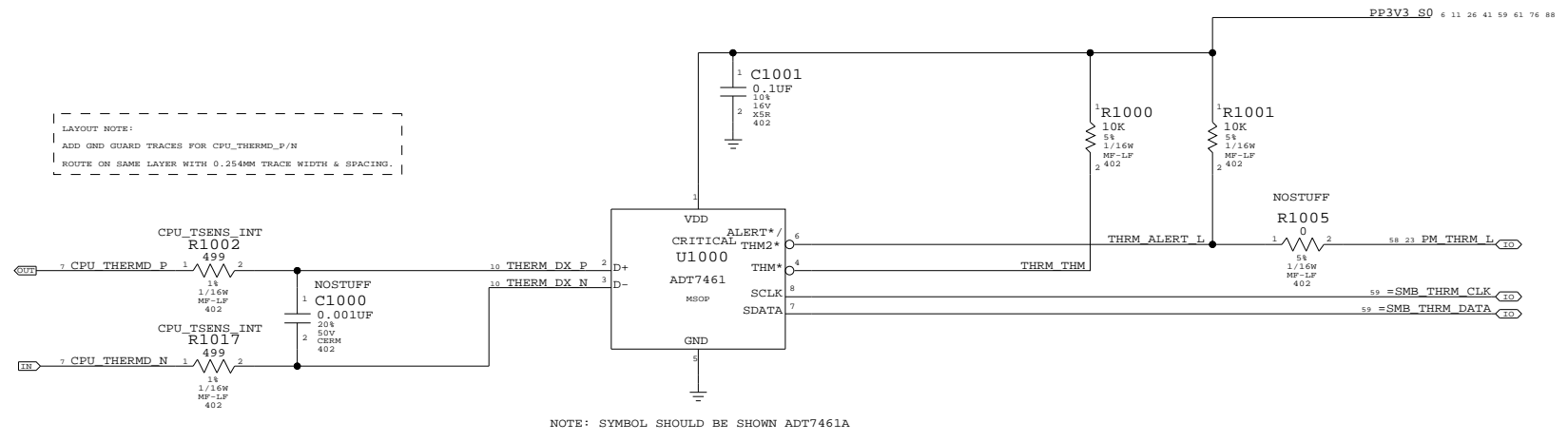
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CPU THERMAL SENSOR

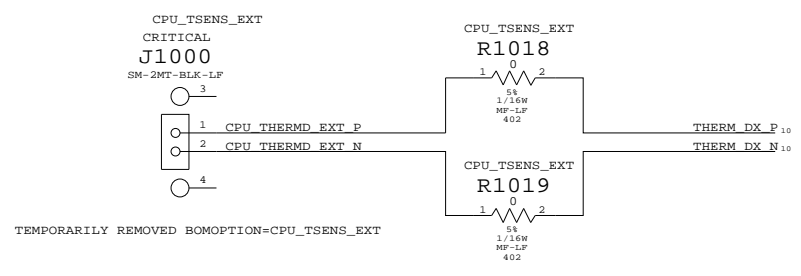
NOTE:
 IF CPU T DIODE TO BE READ IN OFF STATE,
 THEN THIS SHOULD BE S5

LAYOUT NOTE:
 ADD GND GUARD TRACES FOR CPU_THERMD_P/N
 ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
 PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
 PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

CPU TEMP SENSOR

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SCALE	SHT	OF	REV.
NONE	10	110	

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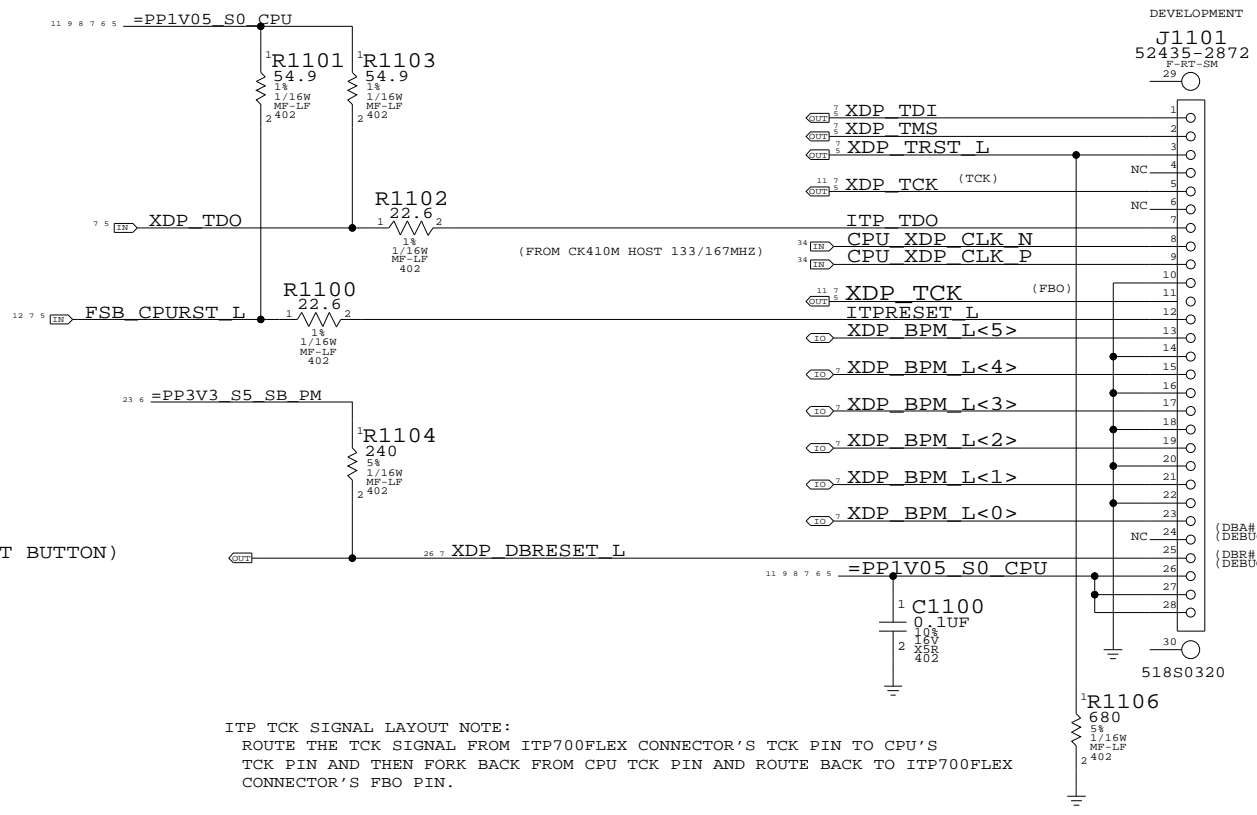
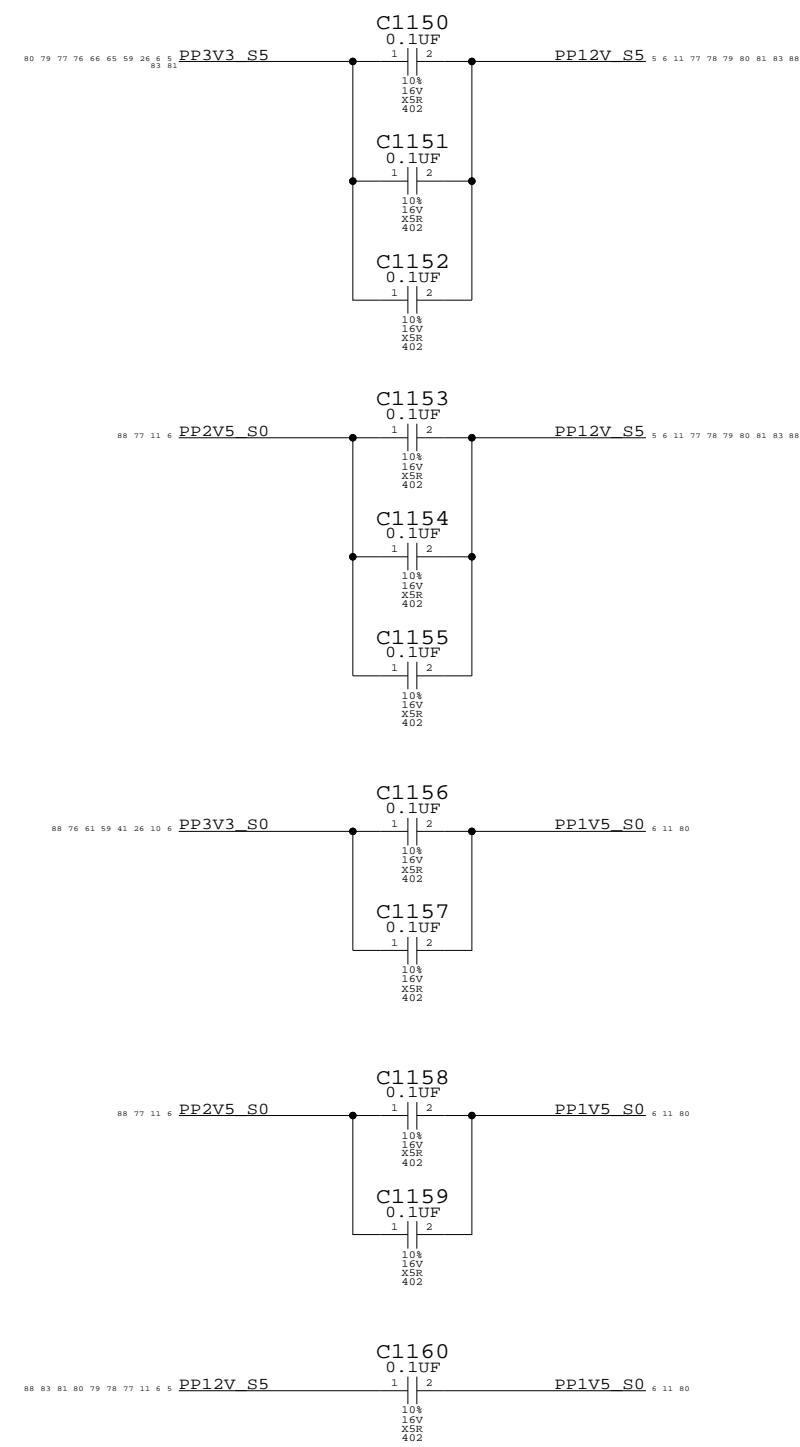
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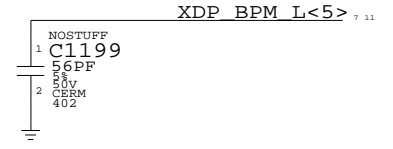
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CPU ITP700FLEX DEBUG SUPPORT



NOTE: PLACE C1199 AT J1101 PINS 13 AND 14



(AND WITH RESET BUTTON)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DBG#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC (DEBUG PORT RESET)

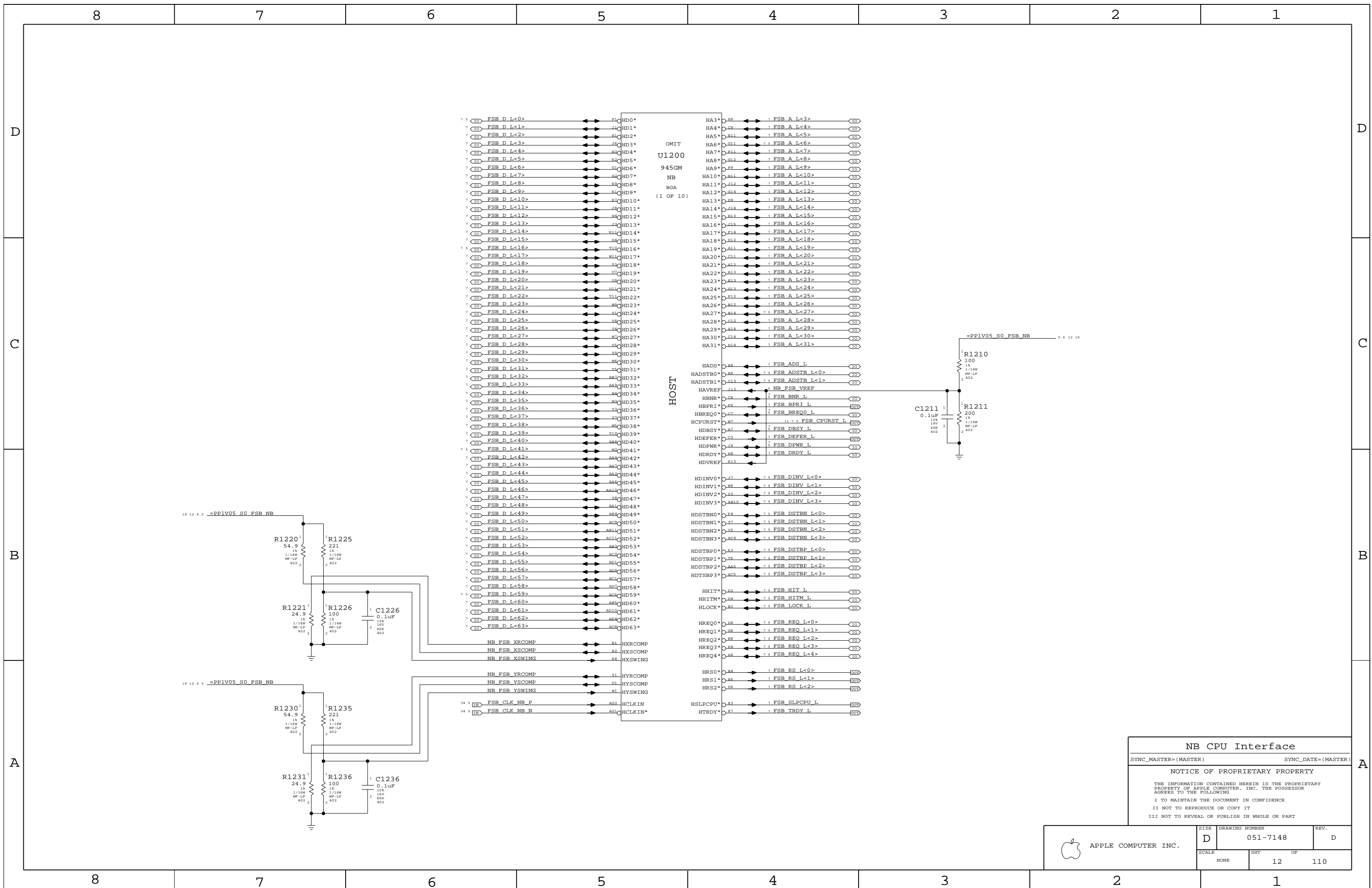
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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	D	051-7148	D
SCALE	SHT	OF	110
NONE	11		



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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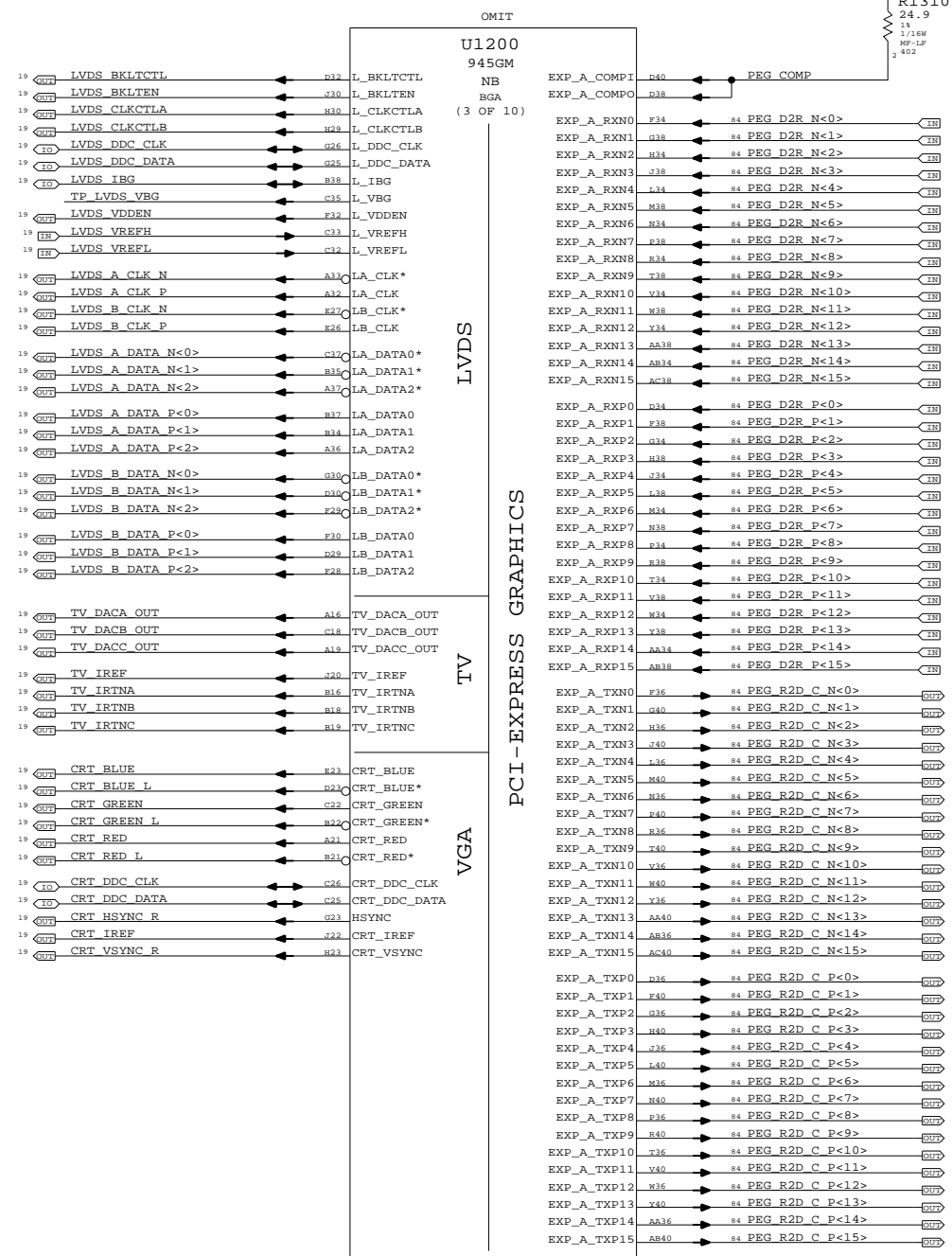
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. D
	SCALE NONE	SHEET 12	OF 110

LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC
 Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

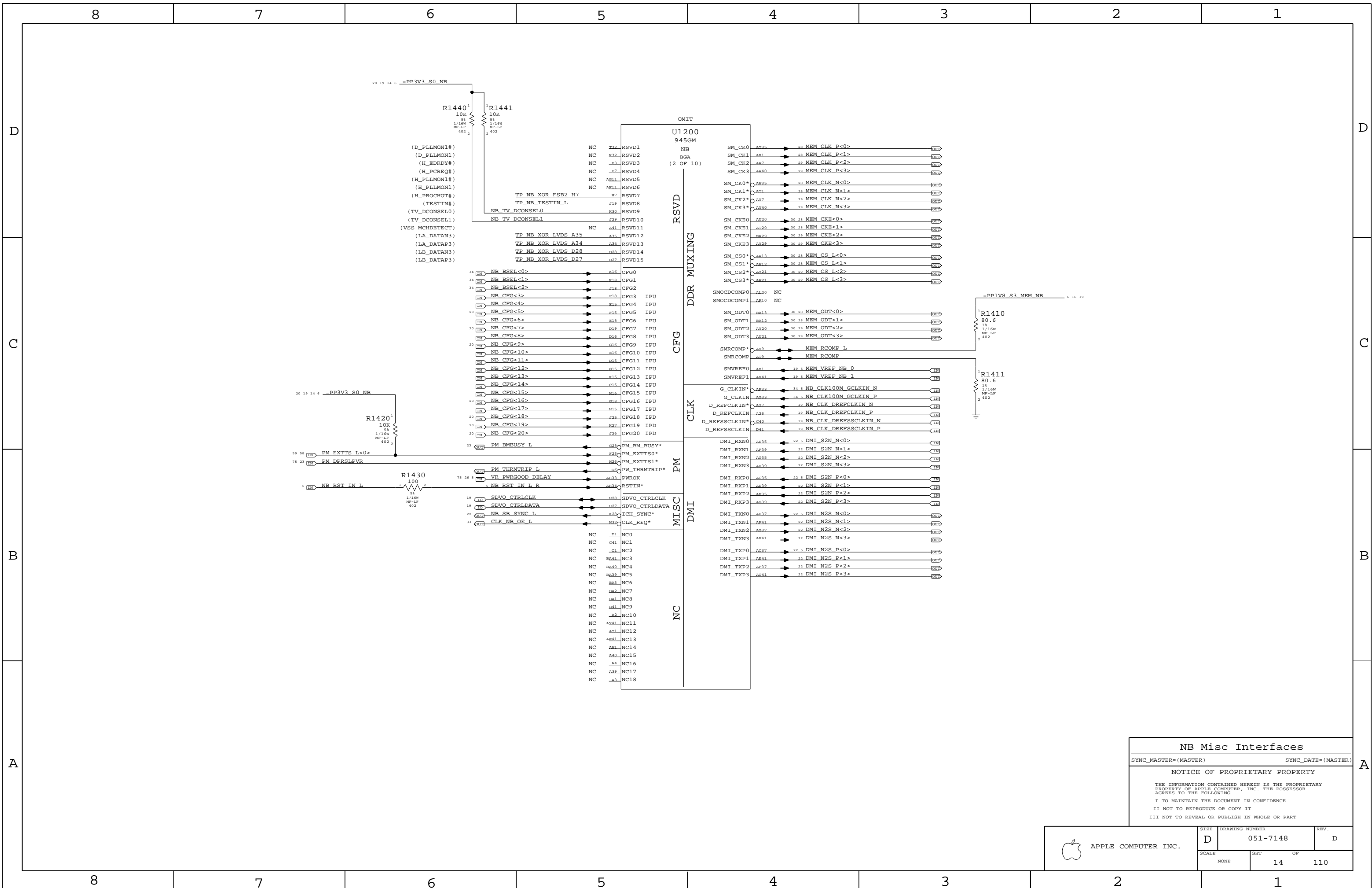
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7148	D
SCALE	SHT	OF	
NONE	13	110	



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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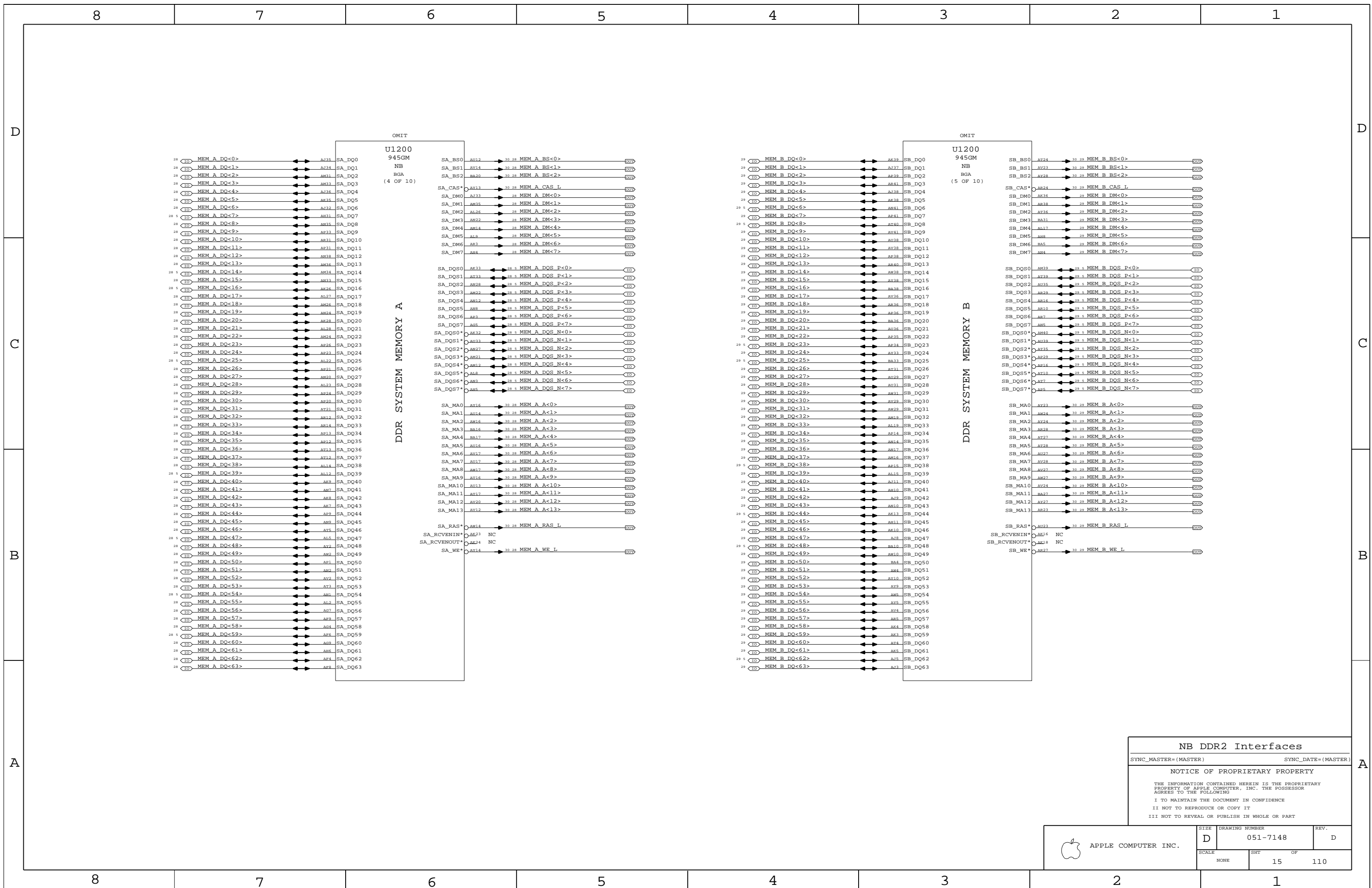
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SCALE	SHT	OF	
NONE	14		110



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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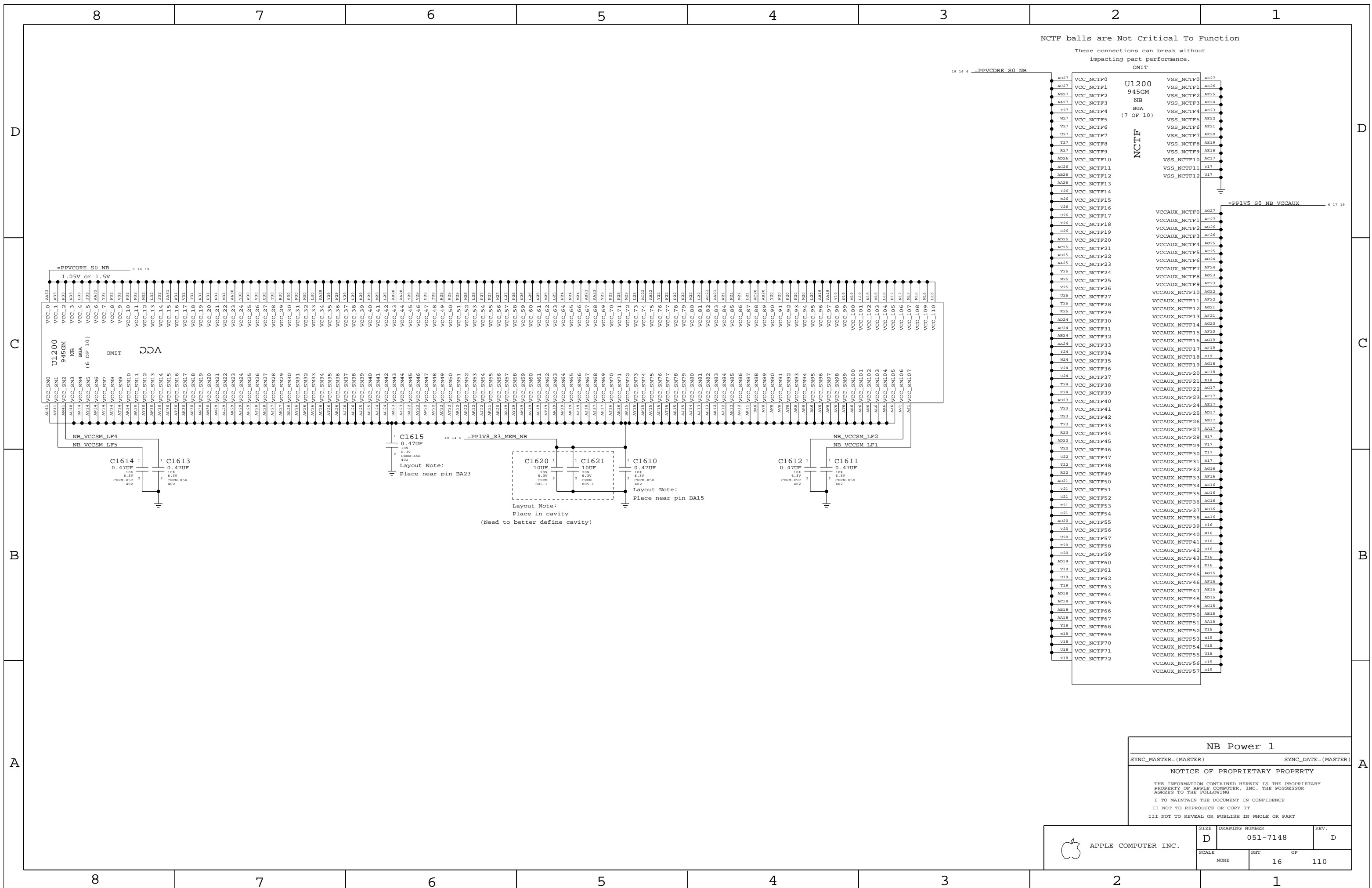
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	D	051-7148	D
SCALE	SHT	OF	
NONE	15	110	



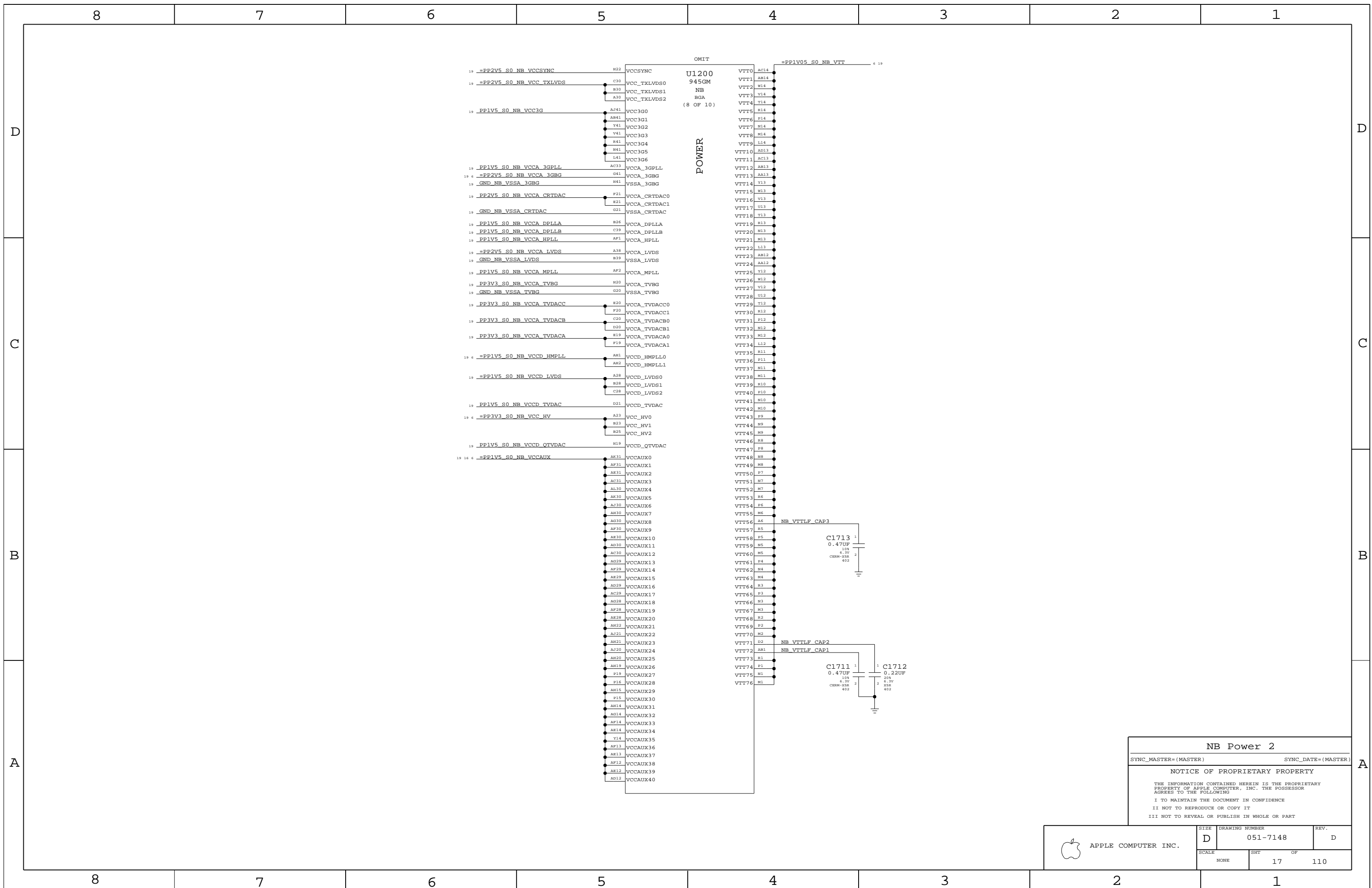
NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

VSS_NCTF0
 VSS_NCTF1
 VSS_NCTF2
 VSS_NCTF3
 VSS_NCTF4
 VSS_NCTF5
 VSS_NCTF6
 VSS_NCTF7
 VSS_NCTF8
 VSS_NCTF9
 VSS_NCTF10
 VSS_NCTF11
 VSS_NCTF12
 VCCAUX_NCTF0
 VCCAUX_NCTF1
 VCCAUX_NCTF2
 VCCAUX_NCTF3
 VCCAUX_NCTF4
 VCCAUX_NCTF5
 VCCAUX_NCTF6
 VCCAUX_NCTF7
 VCCAUX_NCTF8
 VCCAUX_NCTF9
 VCCAUX_NCTF10
 VCCAUX_NCTF11
 VCCAUX_NCTF12
 VCCAUX_NCTF13
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 VCCAUX_NCTF32
 VCCAUX_NCTF33
 VCCAUX_NCTF34
 VCCAUX_NCTF35
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 VCCAUX_NCTF37
 VCCAUX_NCTF38
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 VCCAUX_NCTF50
 VCCAUX_NCTF51
 VCCAUX_NCTF52
 VCCAUX_NCTF53
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 VCCAUX_NCTF55
 VCCAUX_NCTF56
 VCCAUX_NCTF57

NB Power 1
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	16	110	



NB Power 2

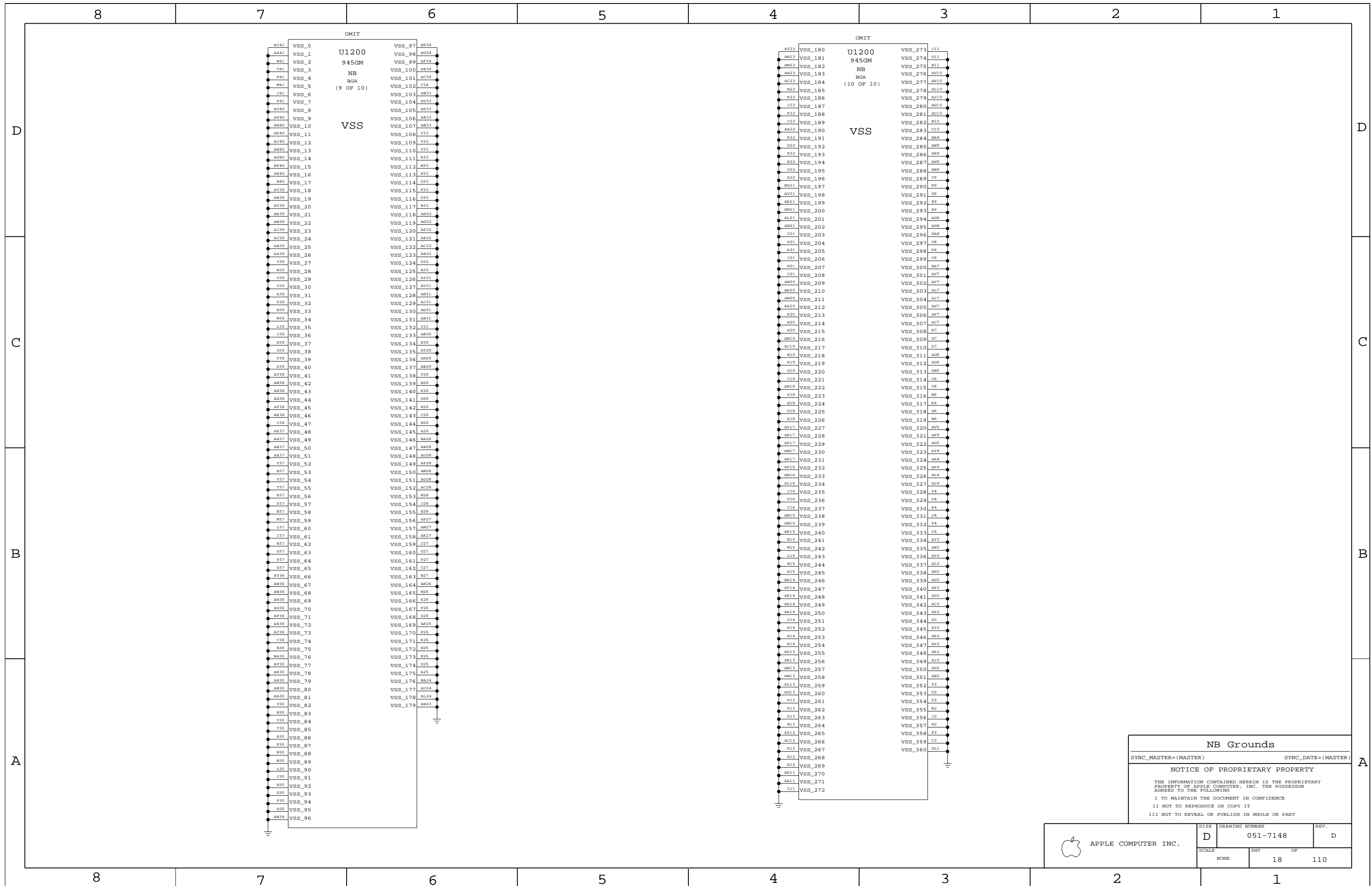
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	SCALE NONE	SHEET 17	OF 110



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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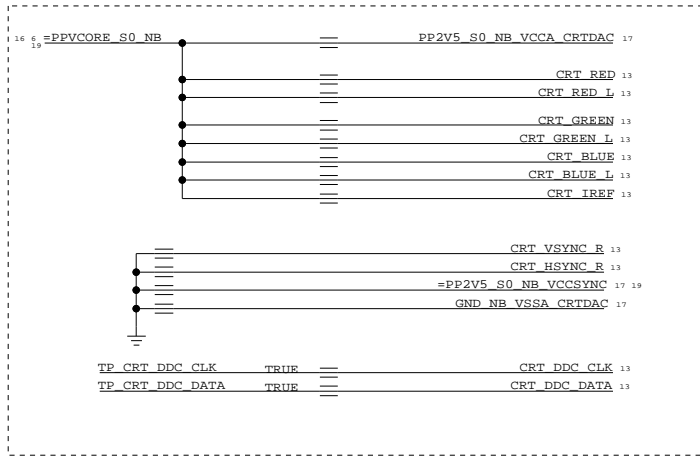
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. D
	SCALE NONE	SHEET 18	OF 110

Power Interface

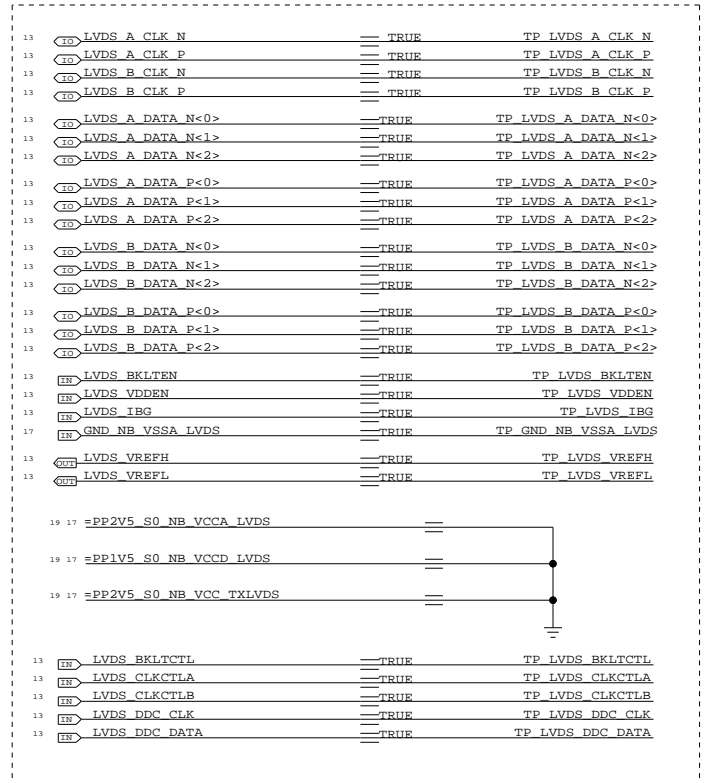
These are the power signals that leave the NB "block"

PP1V05_S0_FSB_NB	5 6 12
PPVCORE_S0_NB	6 16 19
PP1V05_S0_NB	6
PP1V05_S0_NB_VTT	6 17 19
PP1V5_S0_NB	6 19
PP1V5_S0_NB_PCIE	6 13
PP1V5_S0_NB_PLL	6 19
PP1V5_S0_NB_TVDAC	6 19
PP1V5_S0_NB_VCCD_HMPLL	6 19
PP1V5_S0_NB_VCCD_HMPLL	6 17
PP1V5_S0_NB_VCCD_LVDS	17 19
PP1V5_S0_NB_VCCAUX	6 16 17 19
PP1V8_S3_MEM_NB	6 14 16 19
PP2V5_S0_NB_VCCSYNCR	17 19
PP2V5_S0_NB_VCC_TXLVDS	17 19
PP2V5_S0_NB_VCCA_3GBG	6 17 19
PP2V5_S0_NB_VCCA_LVDS	17 19
PP3V3_S0_NB	6 14 20
PP3V3_S0_NB_TVDAC	6
PP3V3_S0_NB_VCC_HV	6 17 19

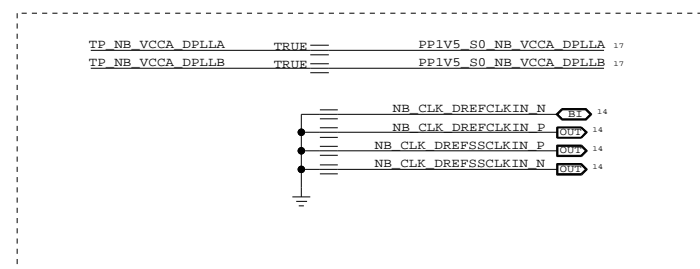
TVOUT DISABLE



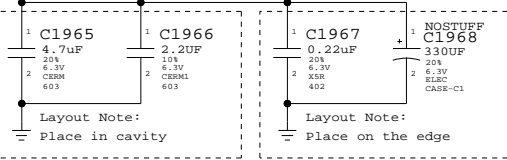
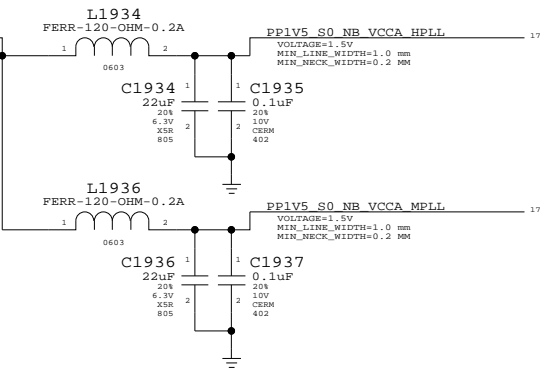
LVDS DISABLE



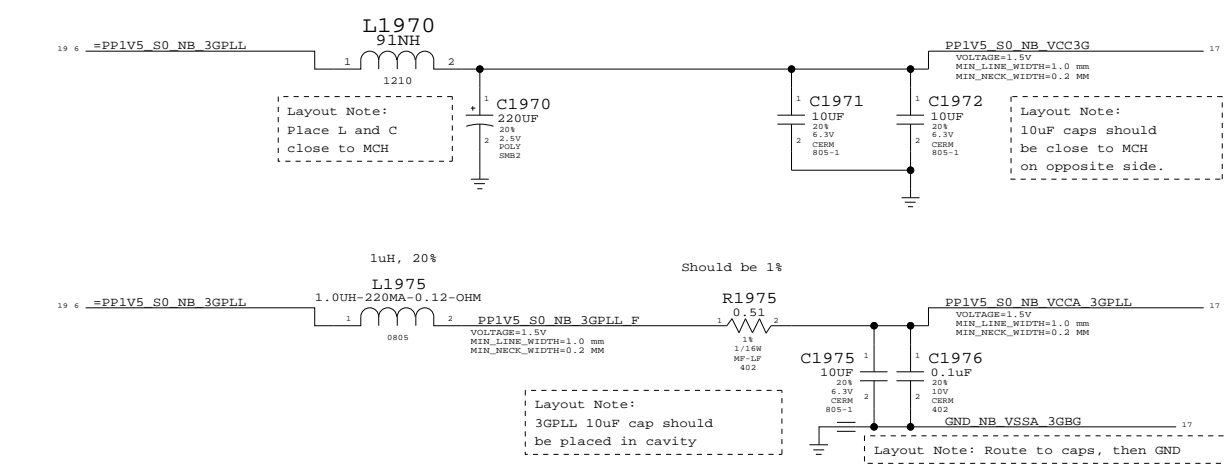
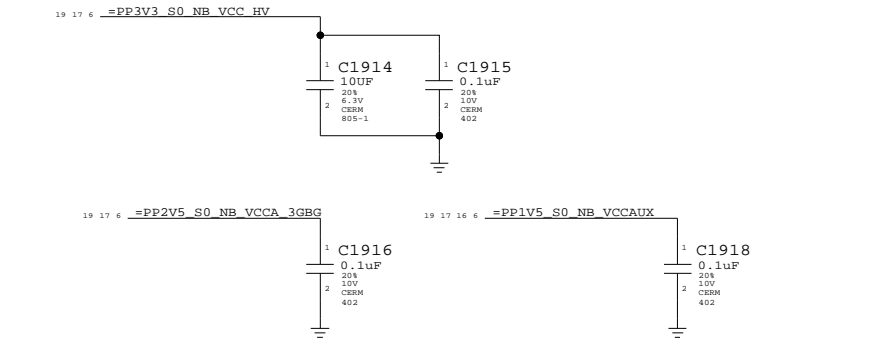
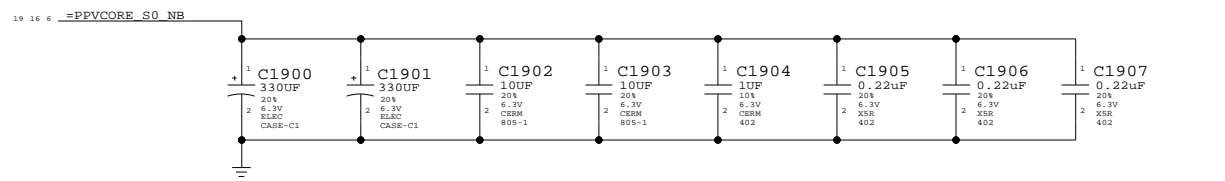
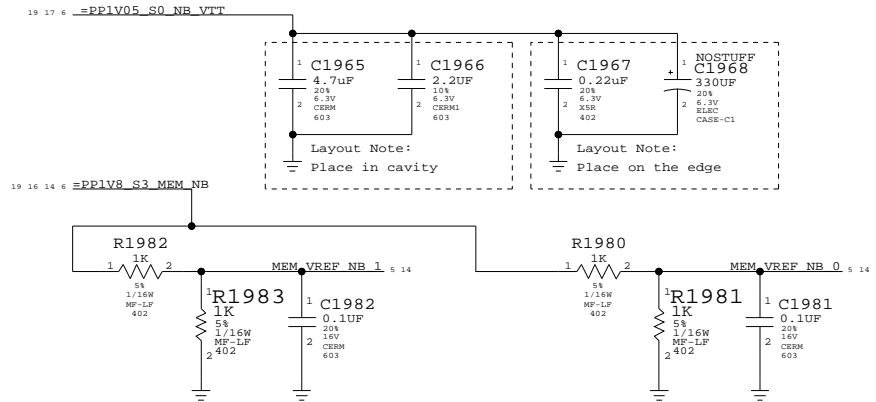
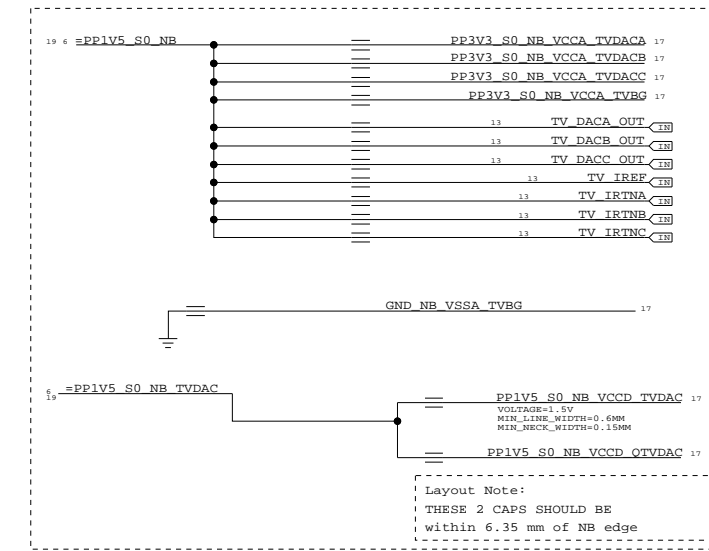
DISPLAY DISABLE



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge



TVOUT DISABLE

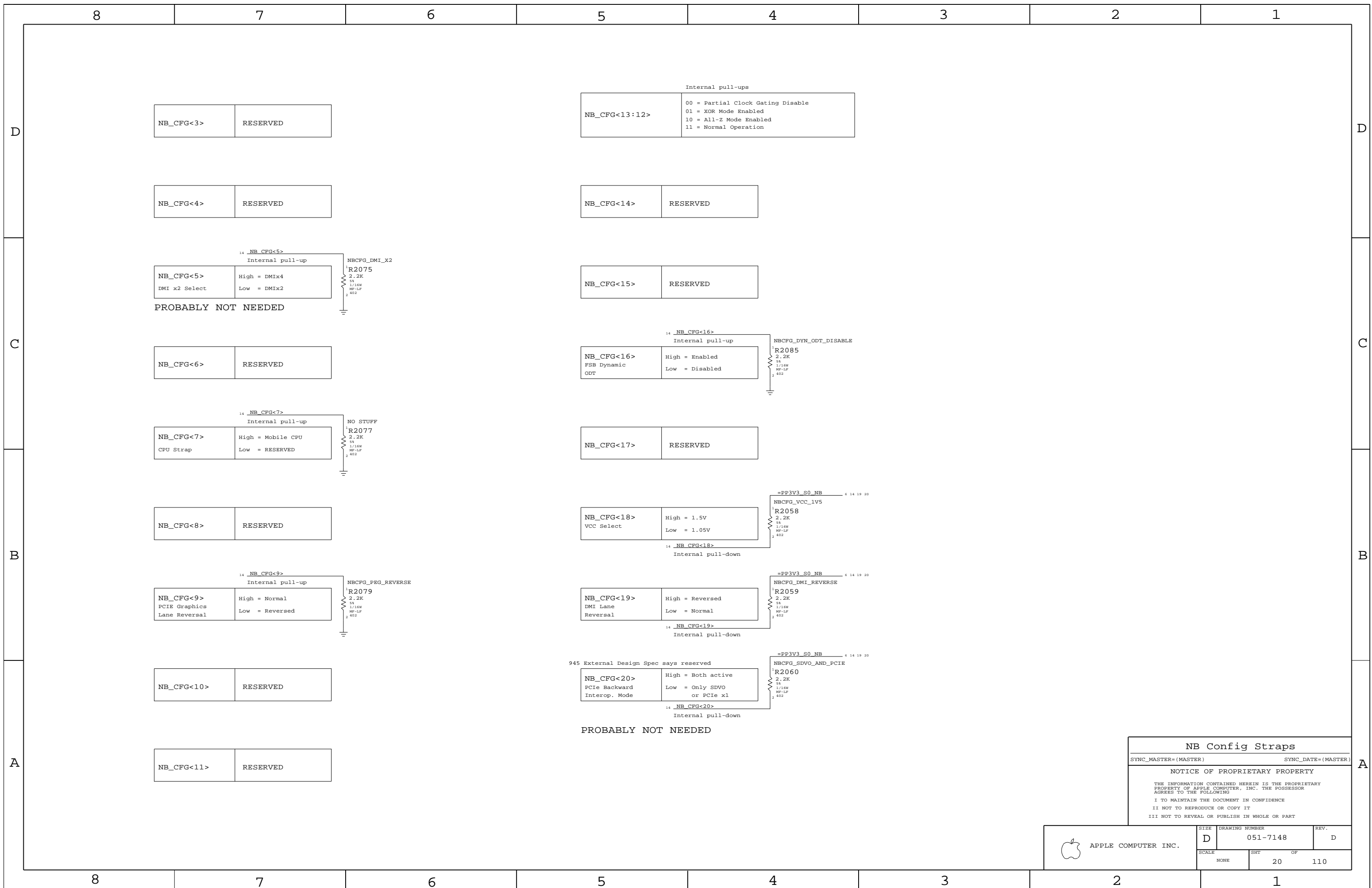


NB (GM) Decoupling
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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D	051-7148	D
SCALE	SHT	OF
NONE	19	110



APPLE COMPUTER INC.



NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<13:12>	Internal pull-ups 00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	---

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

14 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2

PROBABLY NOT NEEDED

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled

14 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V

14 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

14 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved	
14 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

NB Config Straps

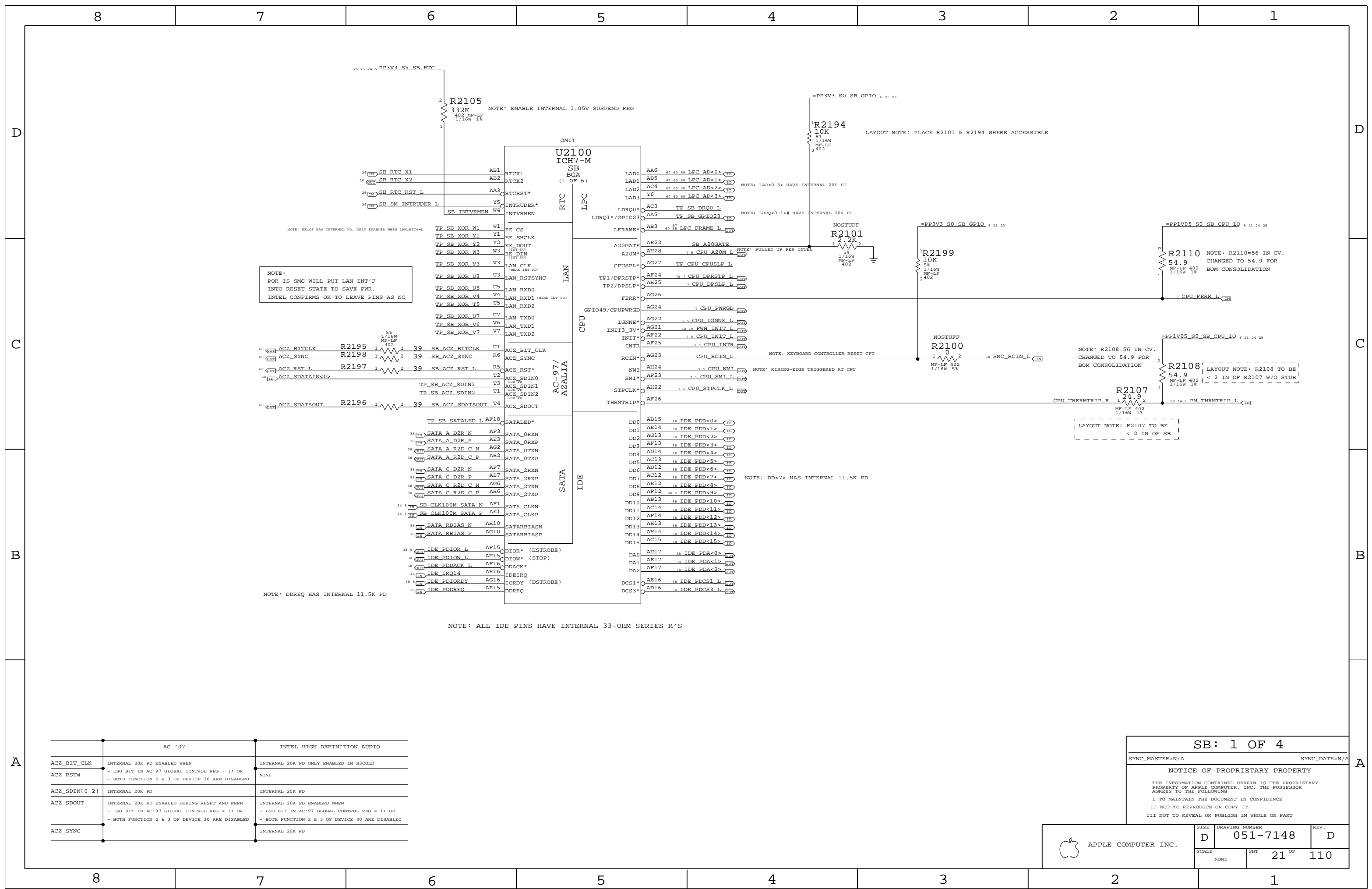
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	20	110	



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

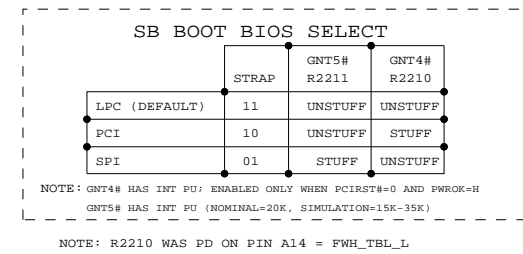
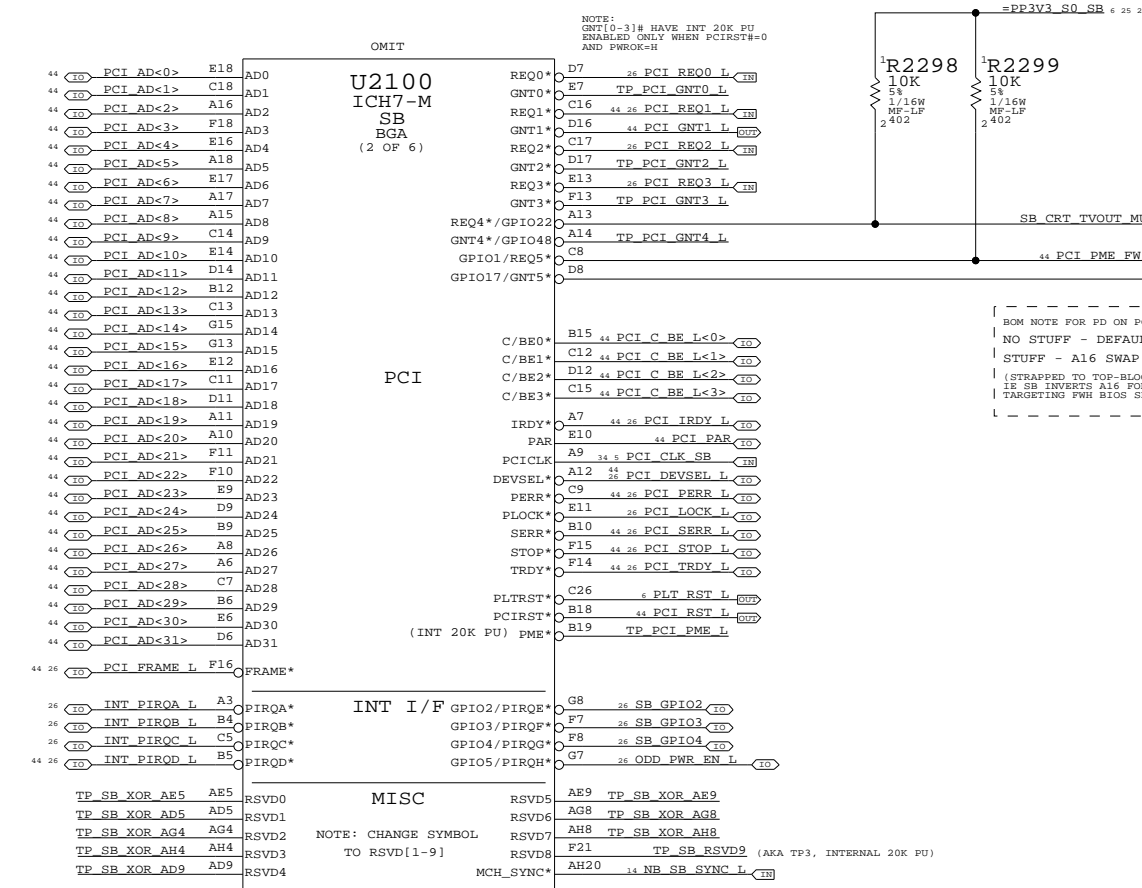
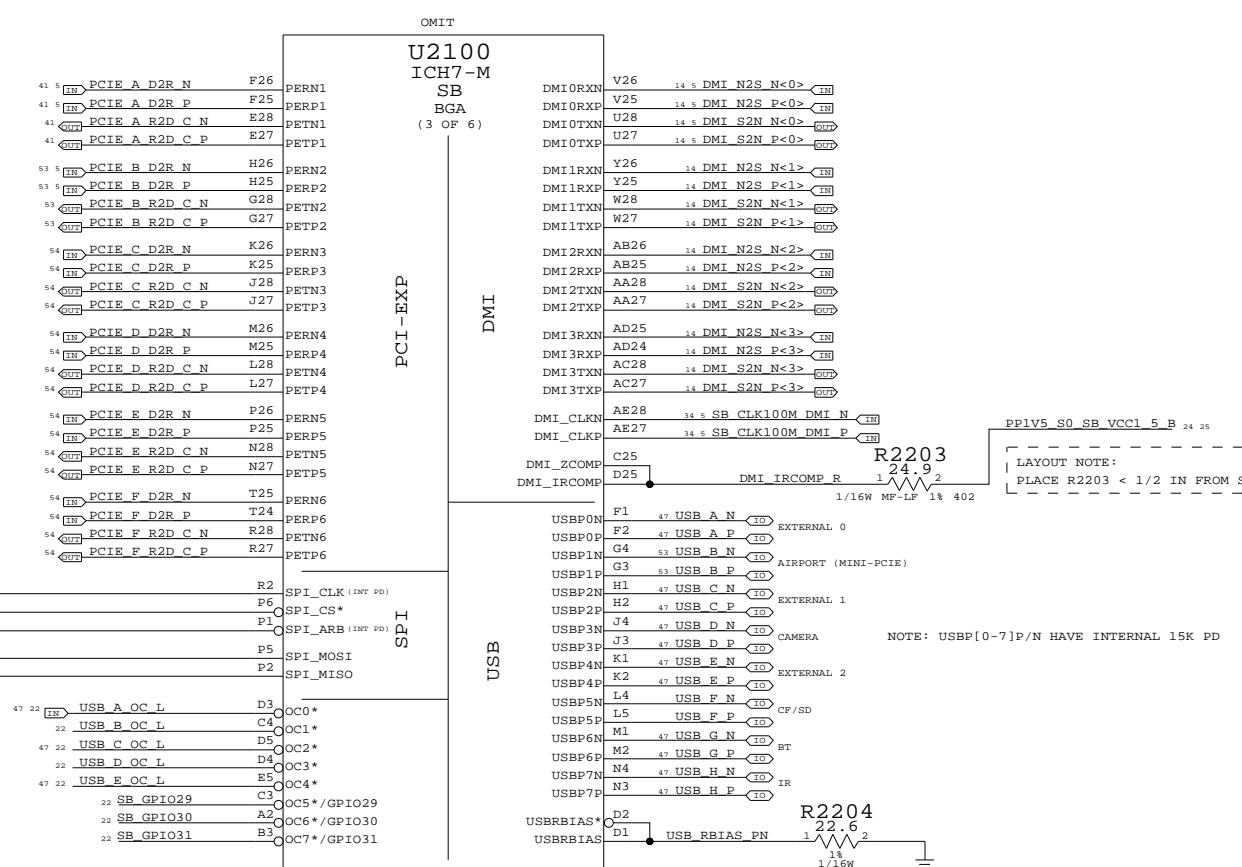
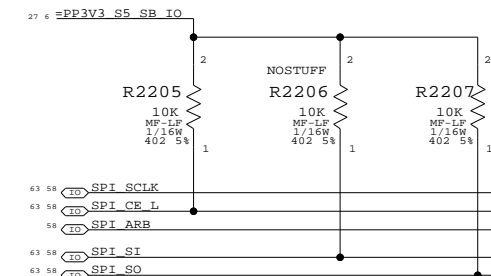
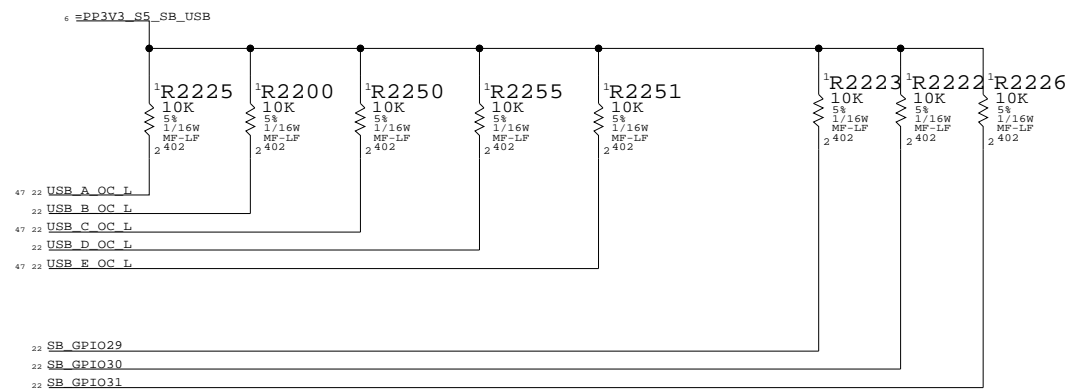
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SCALE	SHT	21 OF	110
NONE			



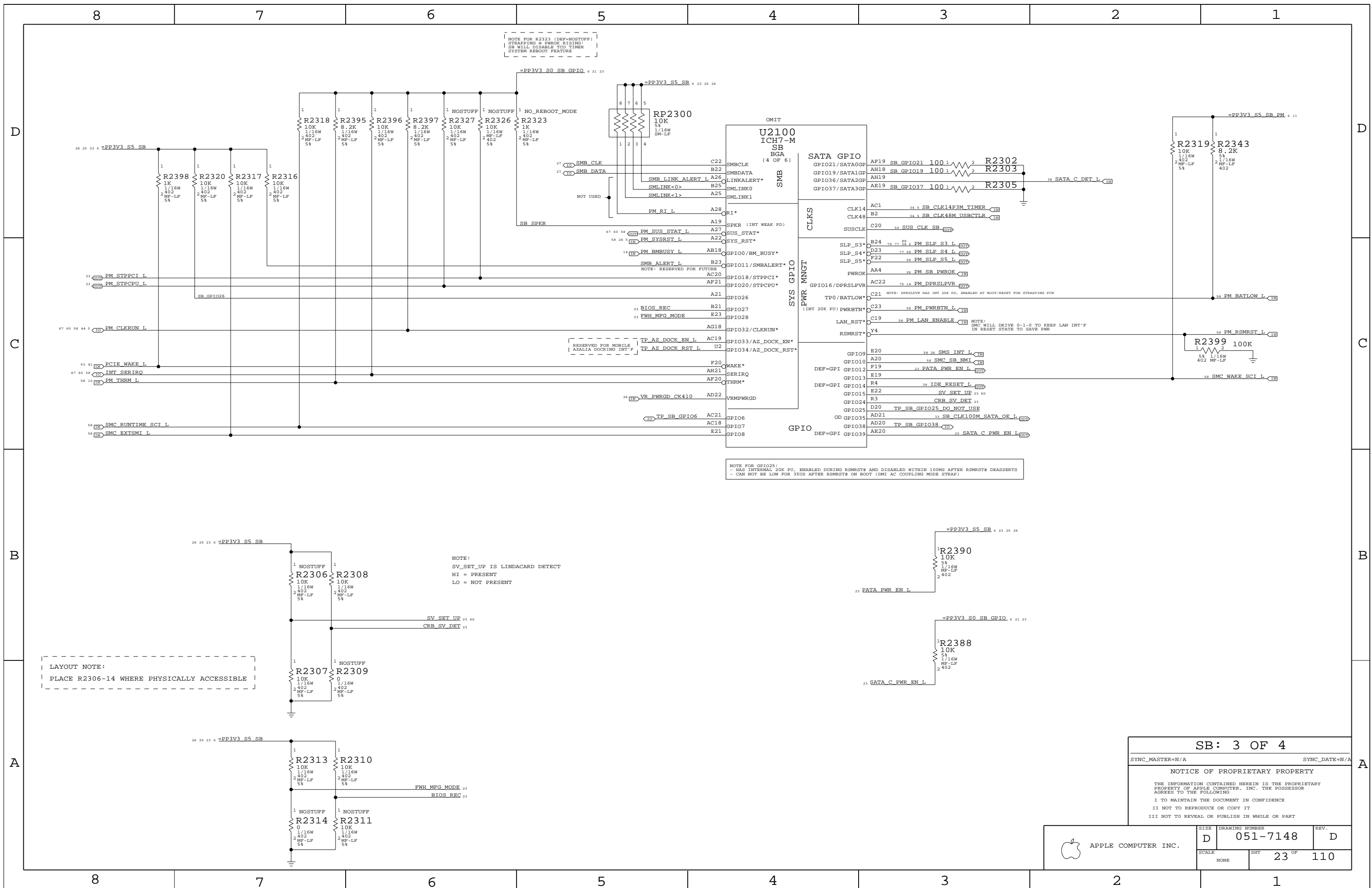
SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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SB: 3 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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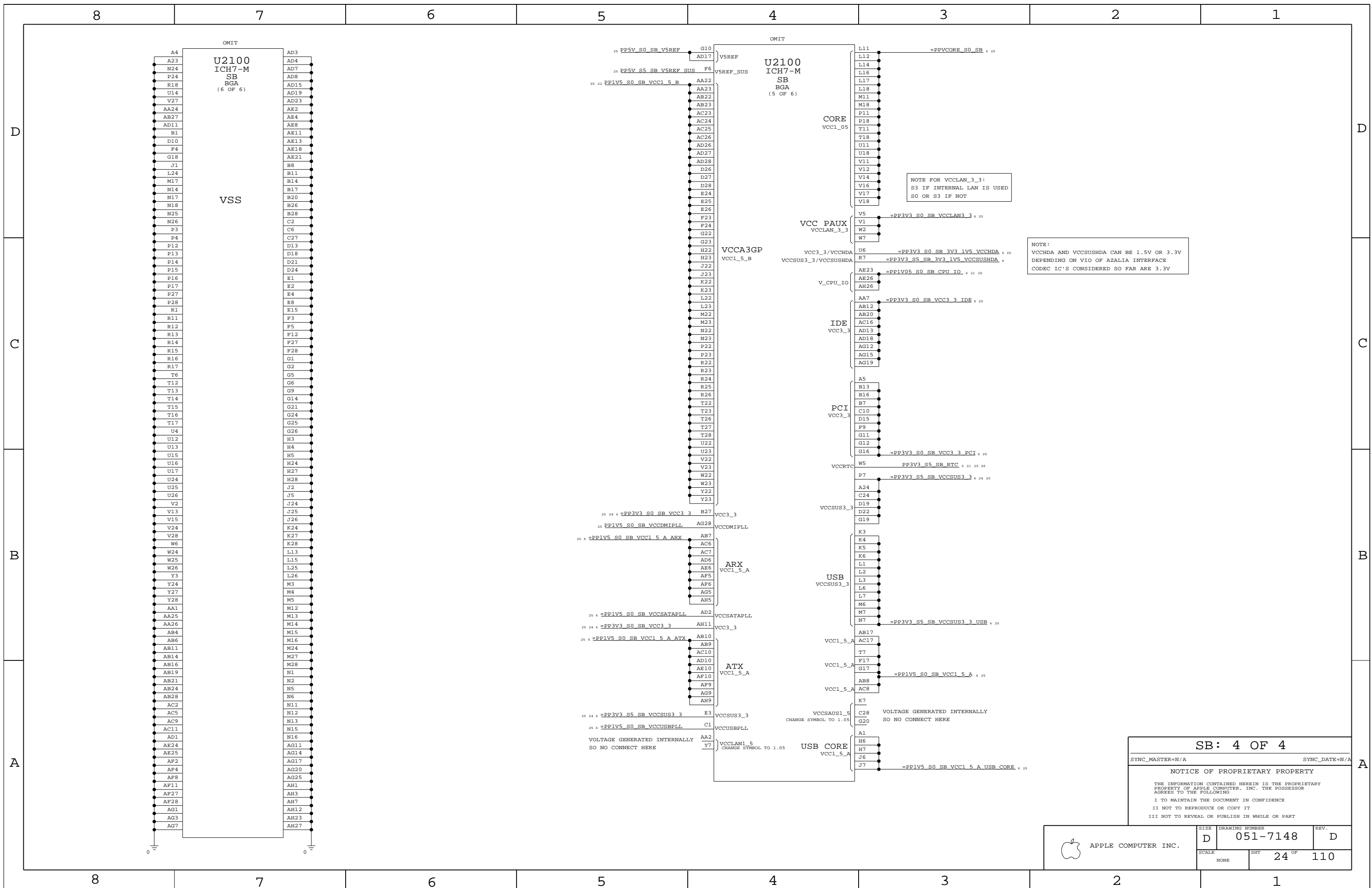
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	D	051-7148	D
SCALE	NONE	SHT	23 OF 110



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCC3_3/VCC3_3 IDE AND VCCSUS3_3/VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

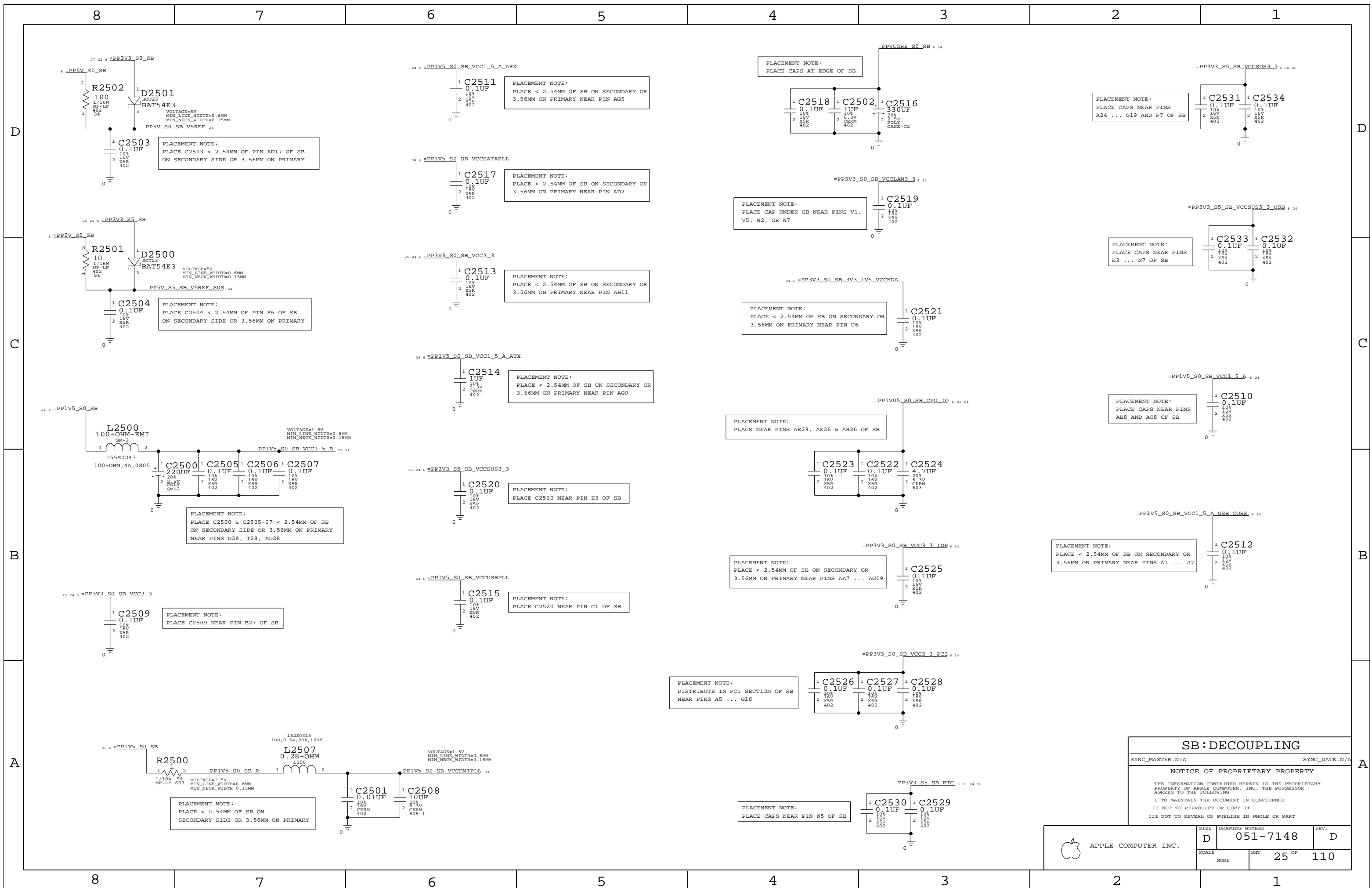
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	SCALE NONE	SHT 24 OF 110	



SB: DECOUPLING

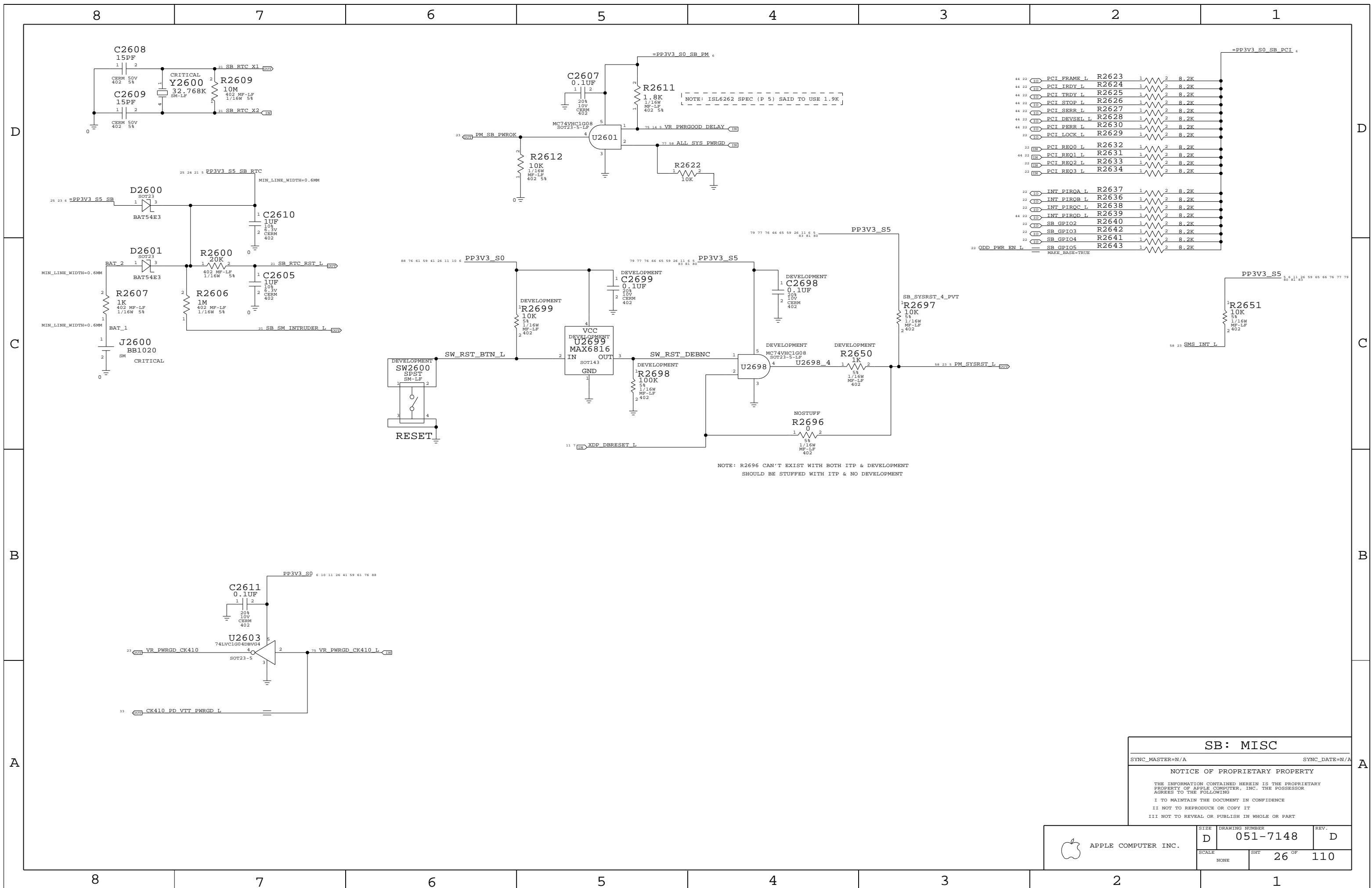
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SCALE	SHT	25 OF	110
NONE			



SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

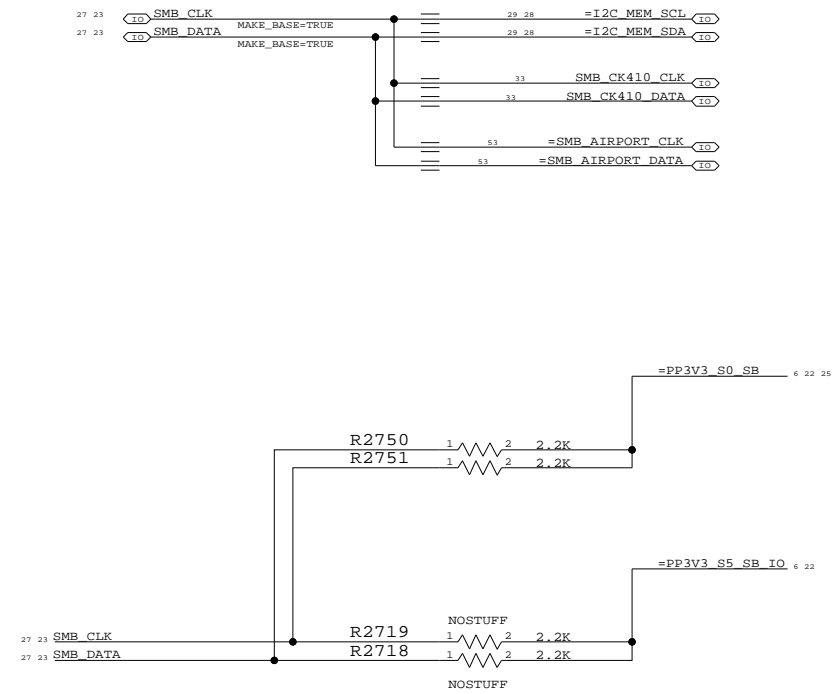
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	SCALE NONE	SHT 26 OF	110

SB I2C BUSSES



SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE D	DRAWING NUMBER 051-7148	REV. D
SCALE NONE	SHT 27 OF	110

Page Notes

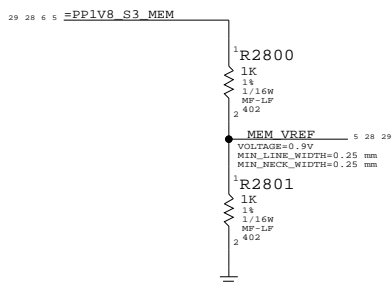
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

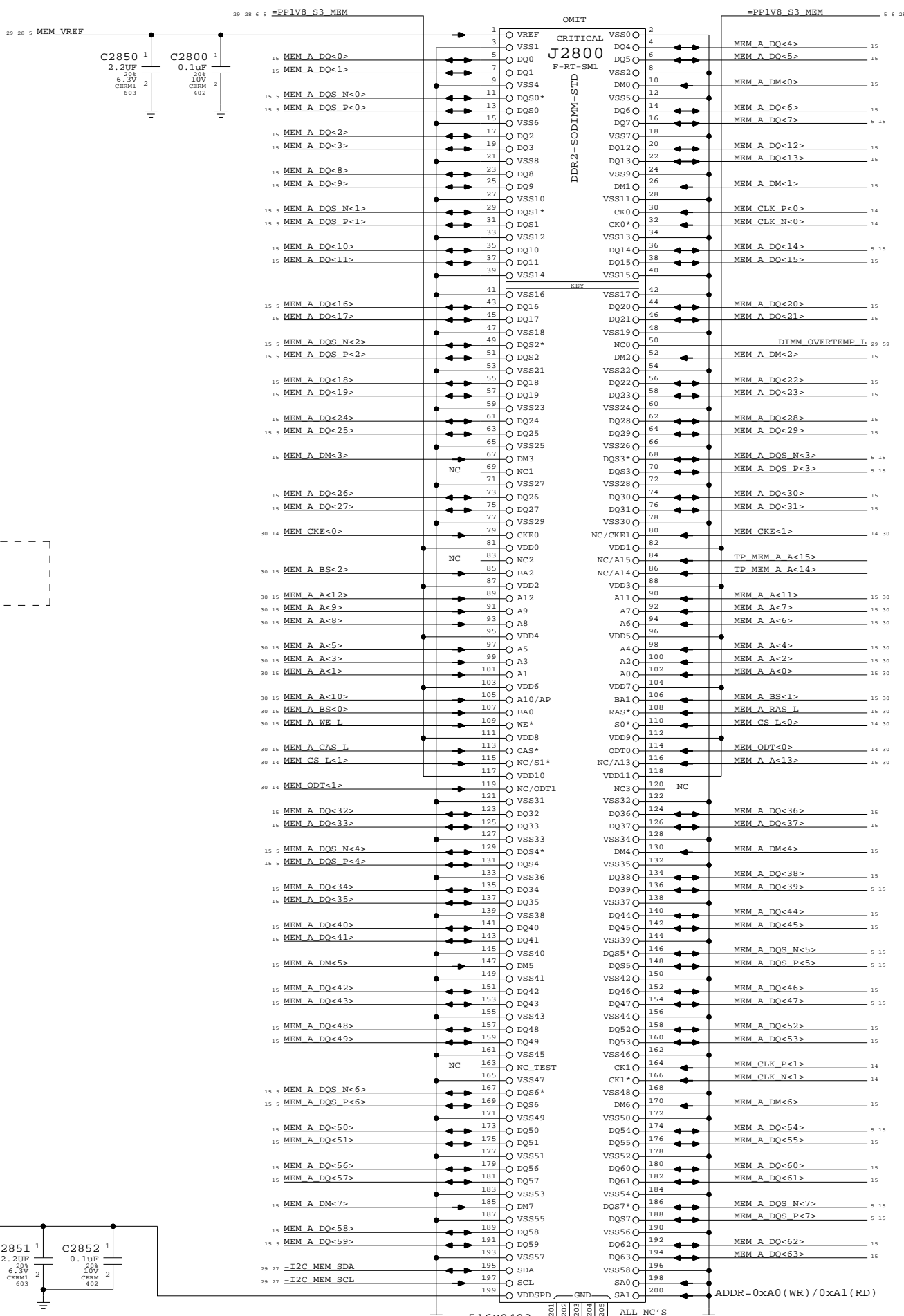
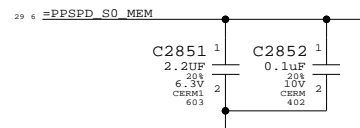
BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector



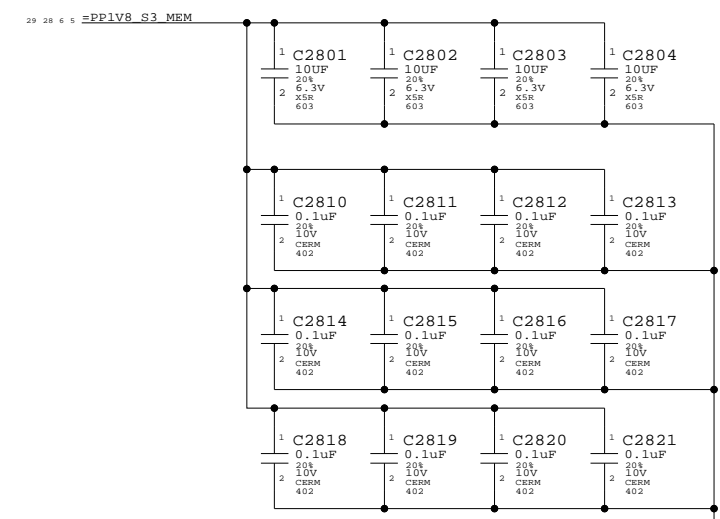
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
 (See Capell Valley pg 47)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0503	1	DDR2 SODIMM STD CONN	J2800	CRITICAL	

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7148	D
SCALE	SHT	OF	
NONE	28	110	

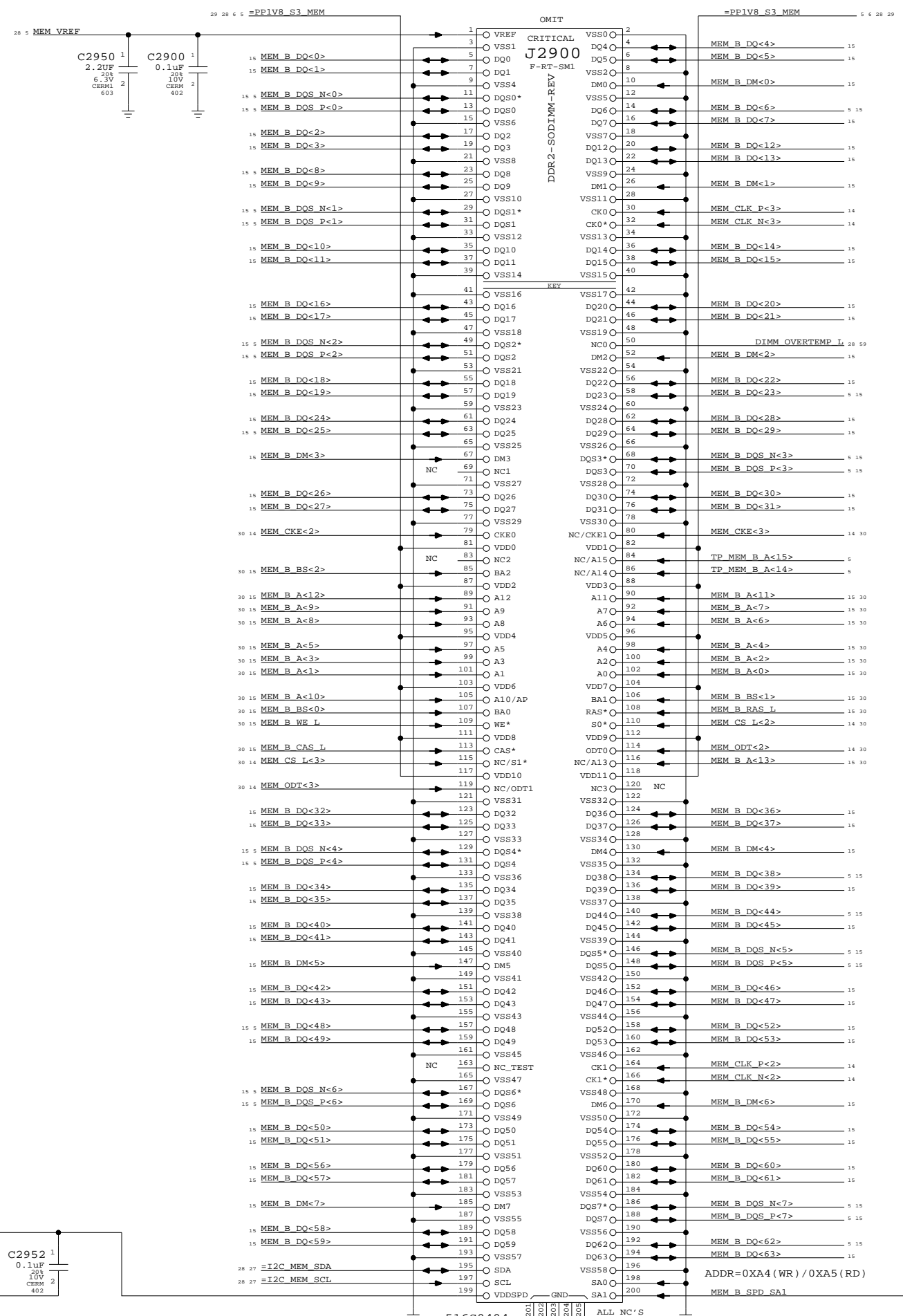
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
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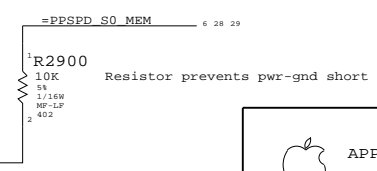
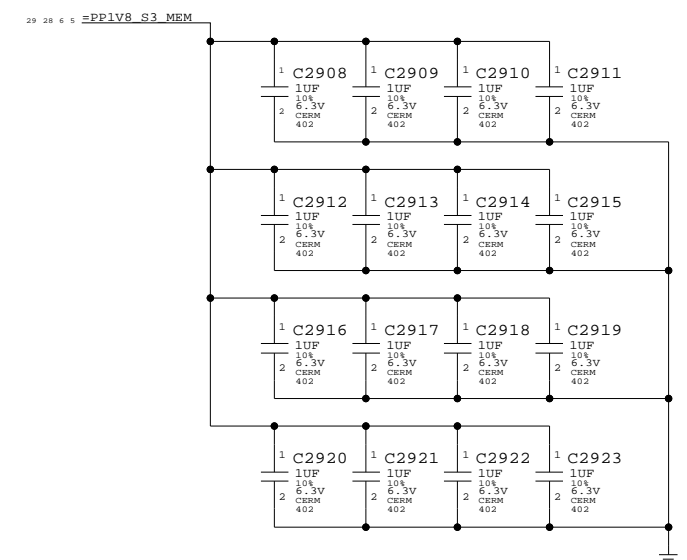
NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0504	1	DDR2 SODIMM REV CONN	J2900	CRITICAL	

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	29	110	

8

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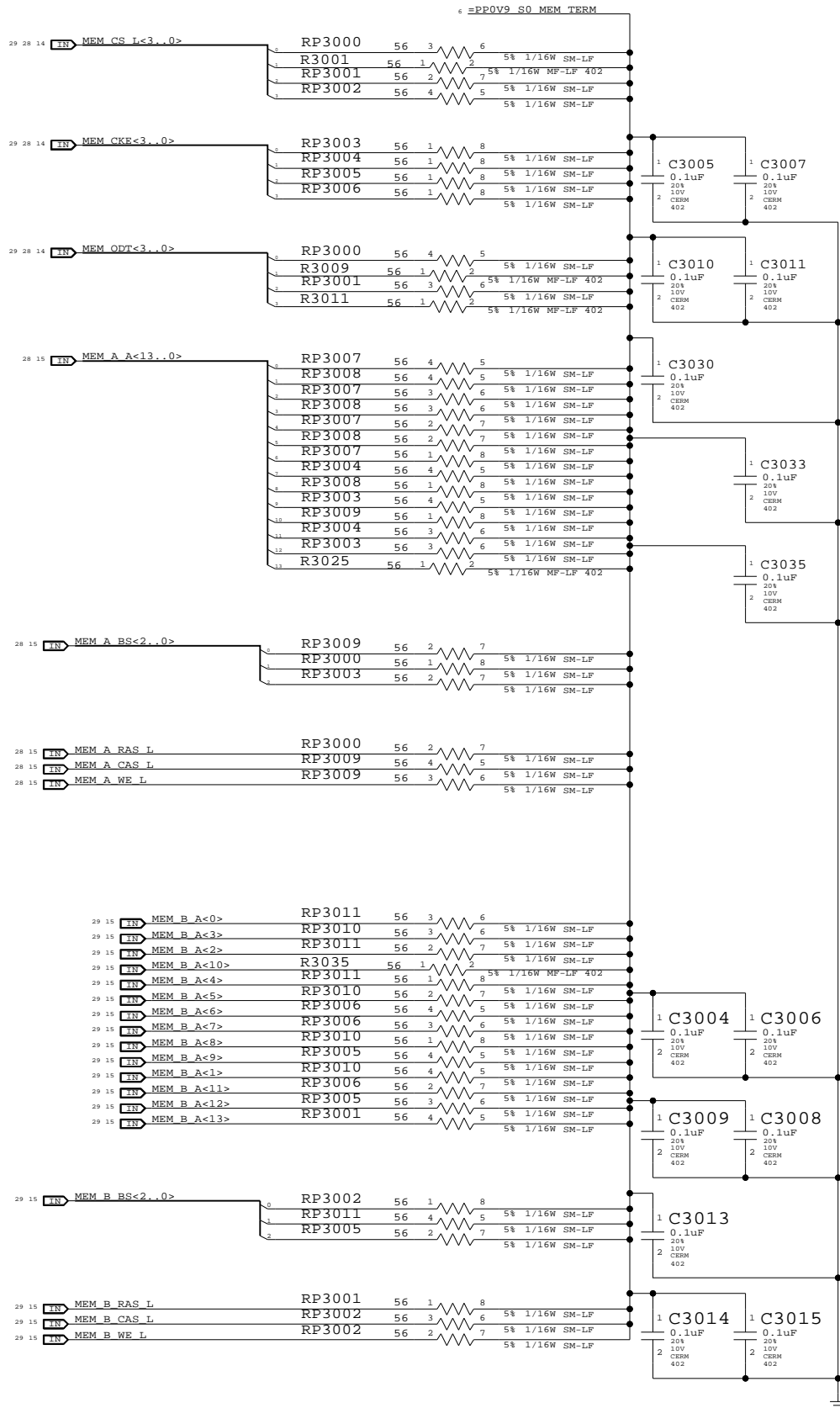
4

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2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	30	110	

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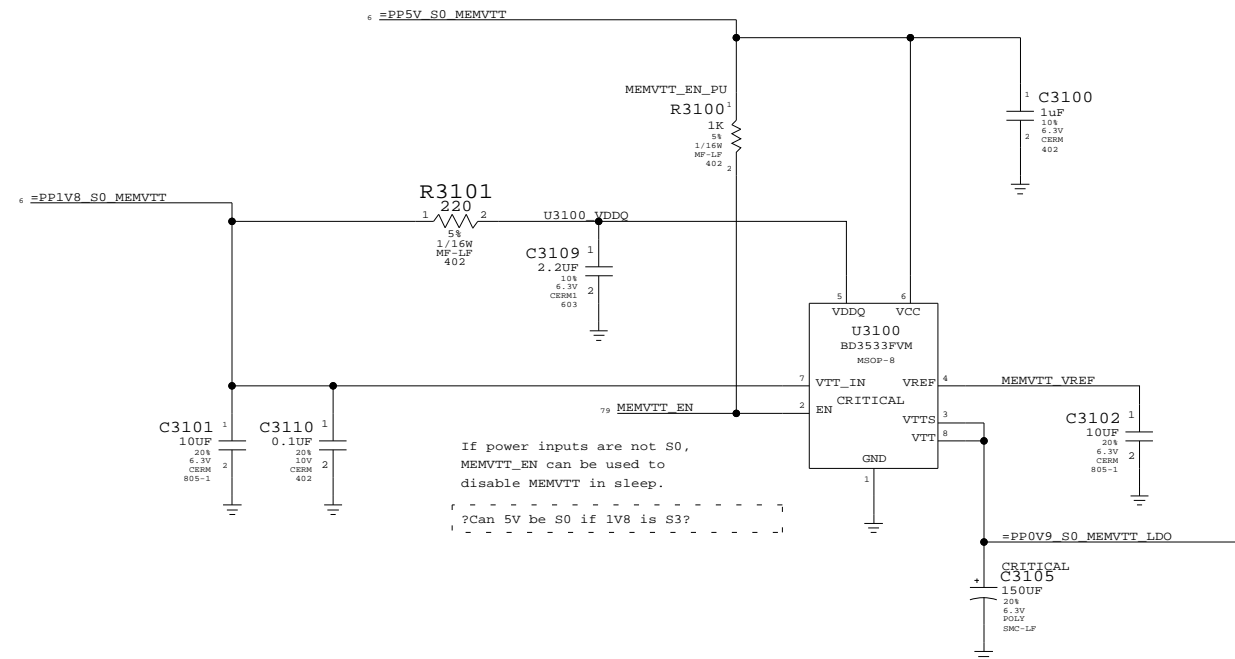
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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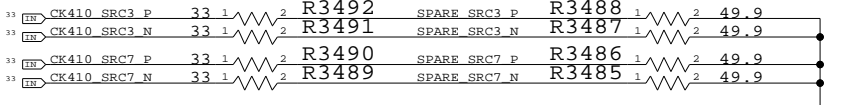
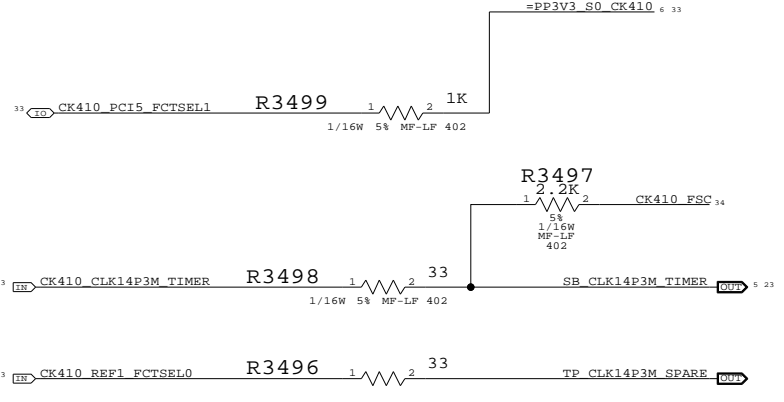
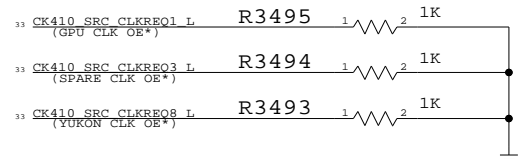
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

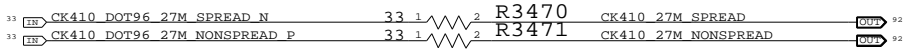
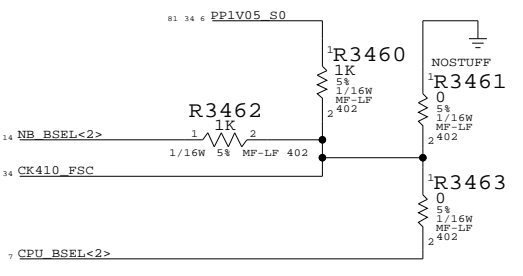
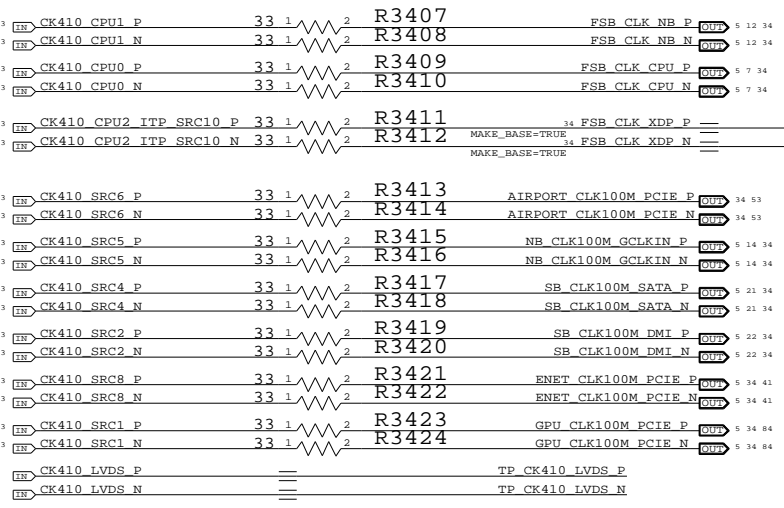
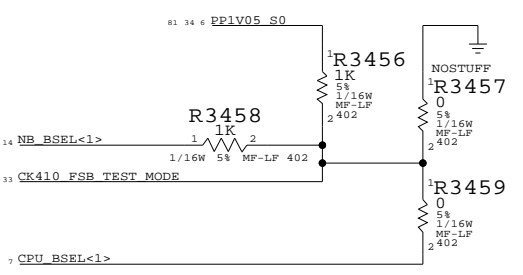
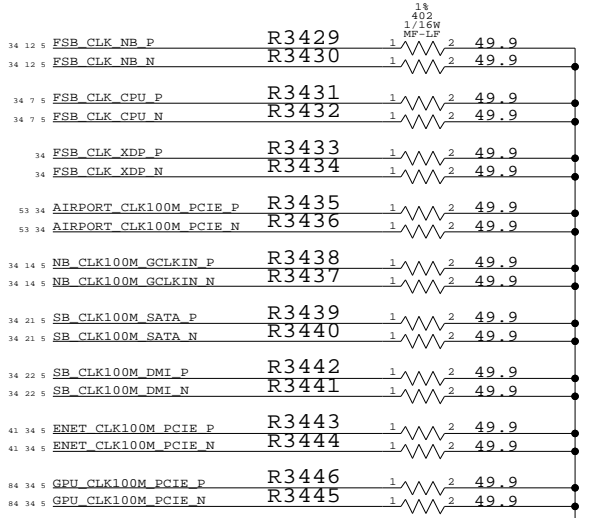
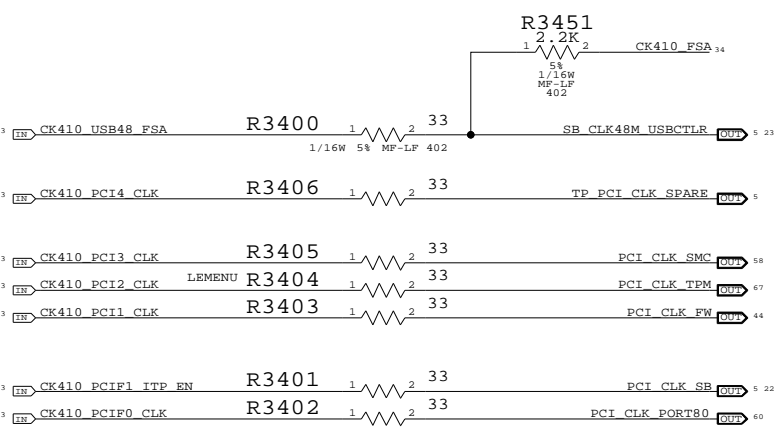
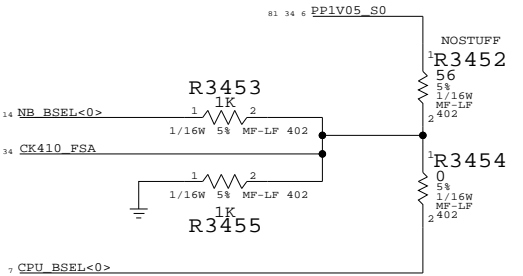
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	REV.
NONE	31	110	

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

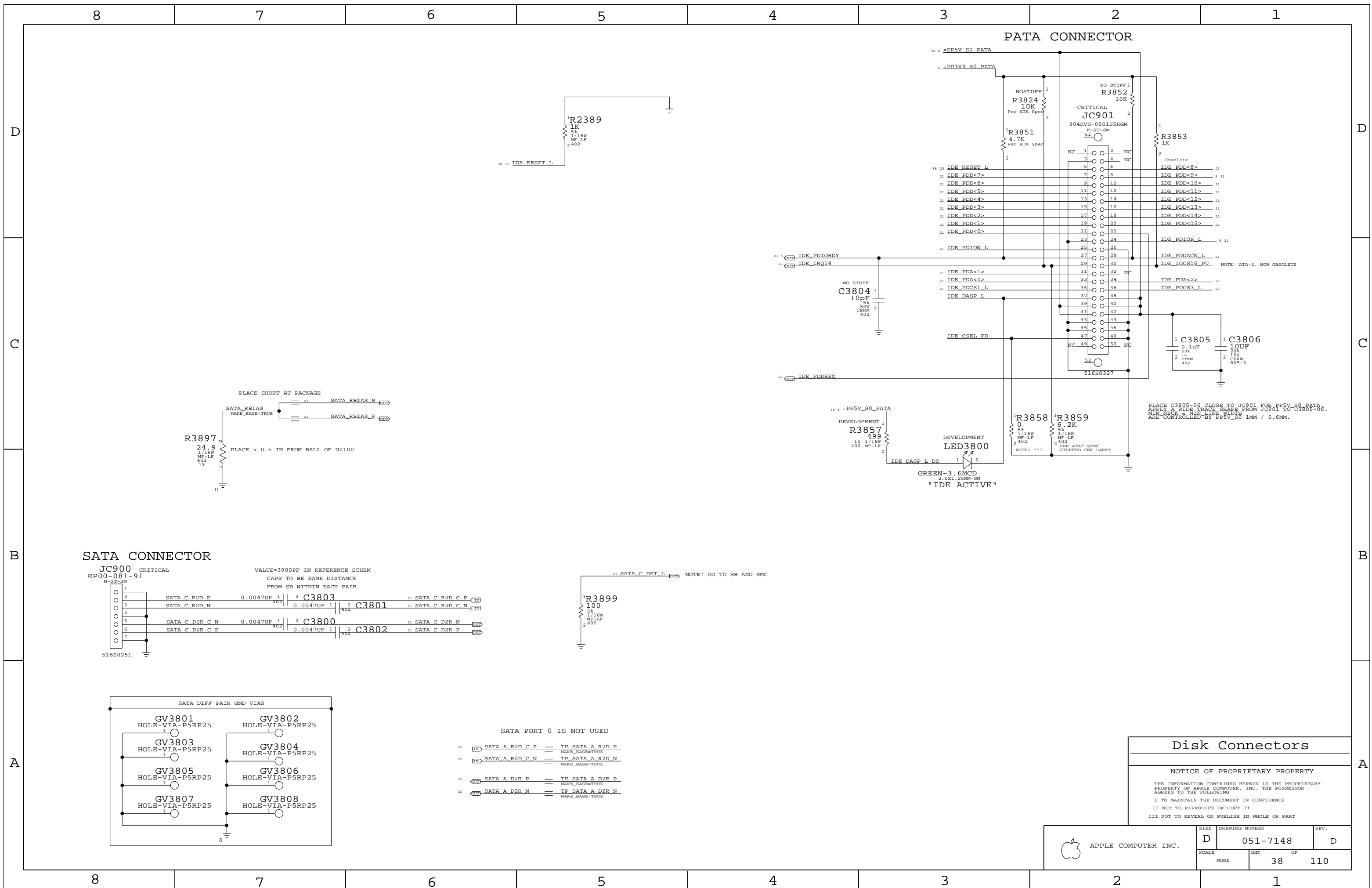
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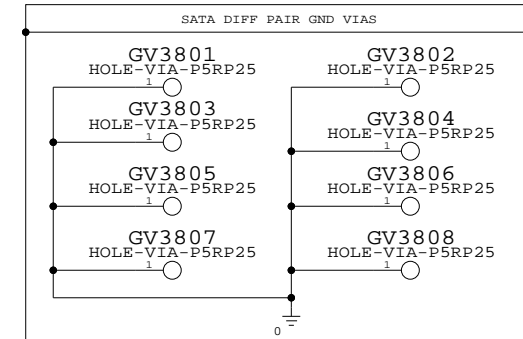
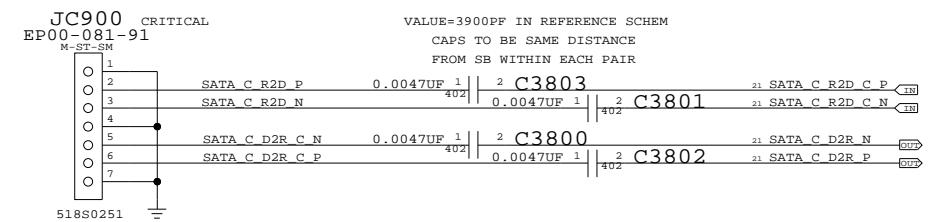
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	REV.
NONE	34	110	



SATA CONNECTOR



SATA PORT 0 IS NOT USED

IN	SATA A R2D C P	TP SATA A R2D P
		MAKE_BASE=TRUE
IN	SATA A R2D C N	TP SATA A R2D N
		MAKE_BASE=TRUE
OUT	SATA A D2R P	TP SATA A D2R P
		MAKE_BASE=TRUE
OUT	SATA A D2R N	TP SATA A D2R N
		MAKE_BASE=TRUE

Disk Connectors

NOTICE OF PROPRIETARY PROPERTY

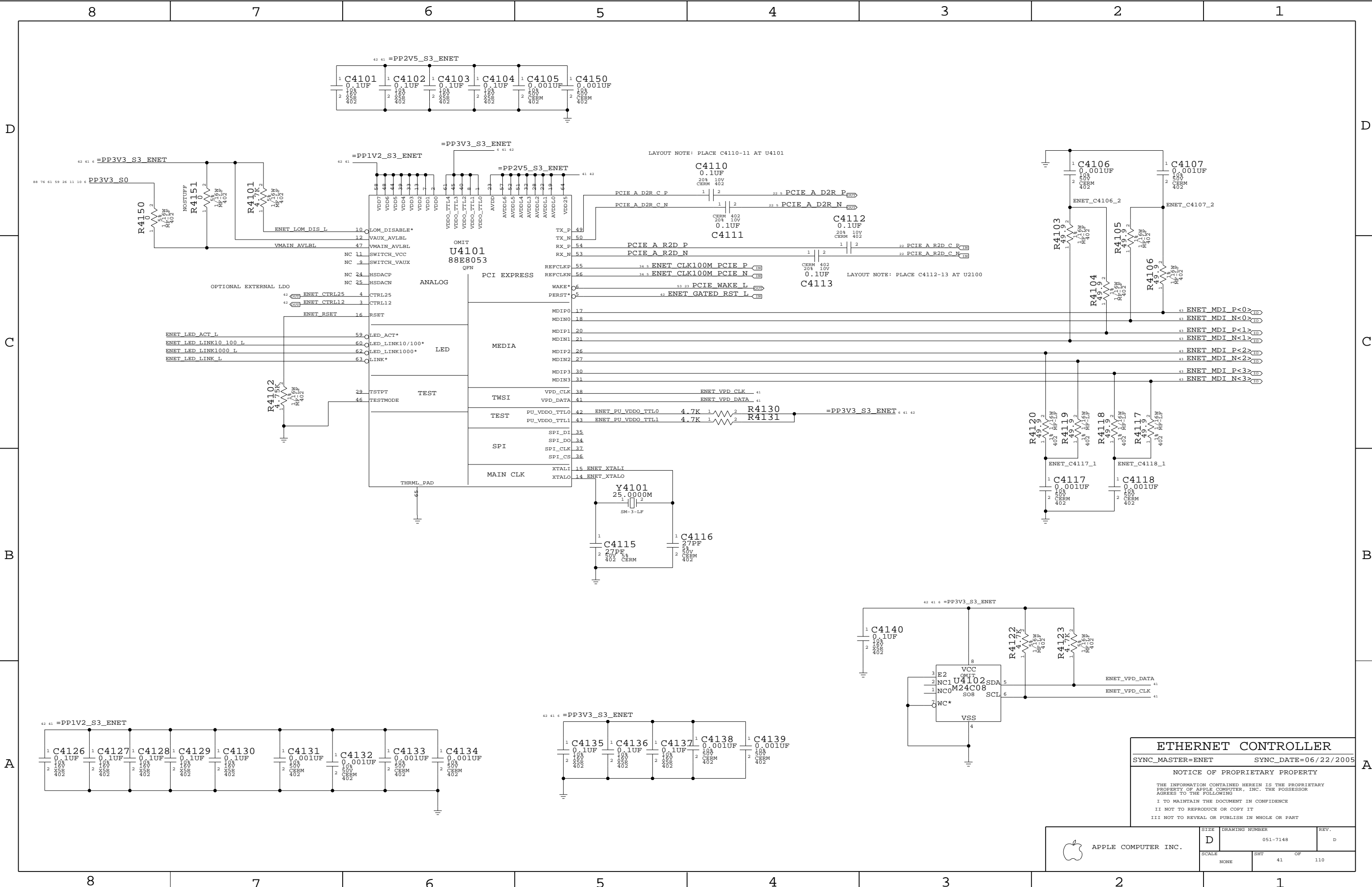
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	D	051-7148	D
SCALE	SHT OF		
NONE	38		110



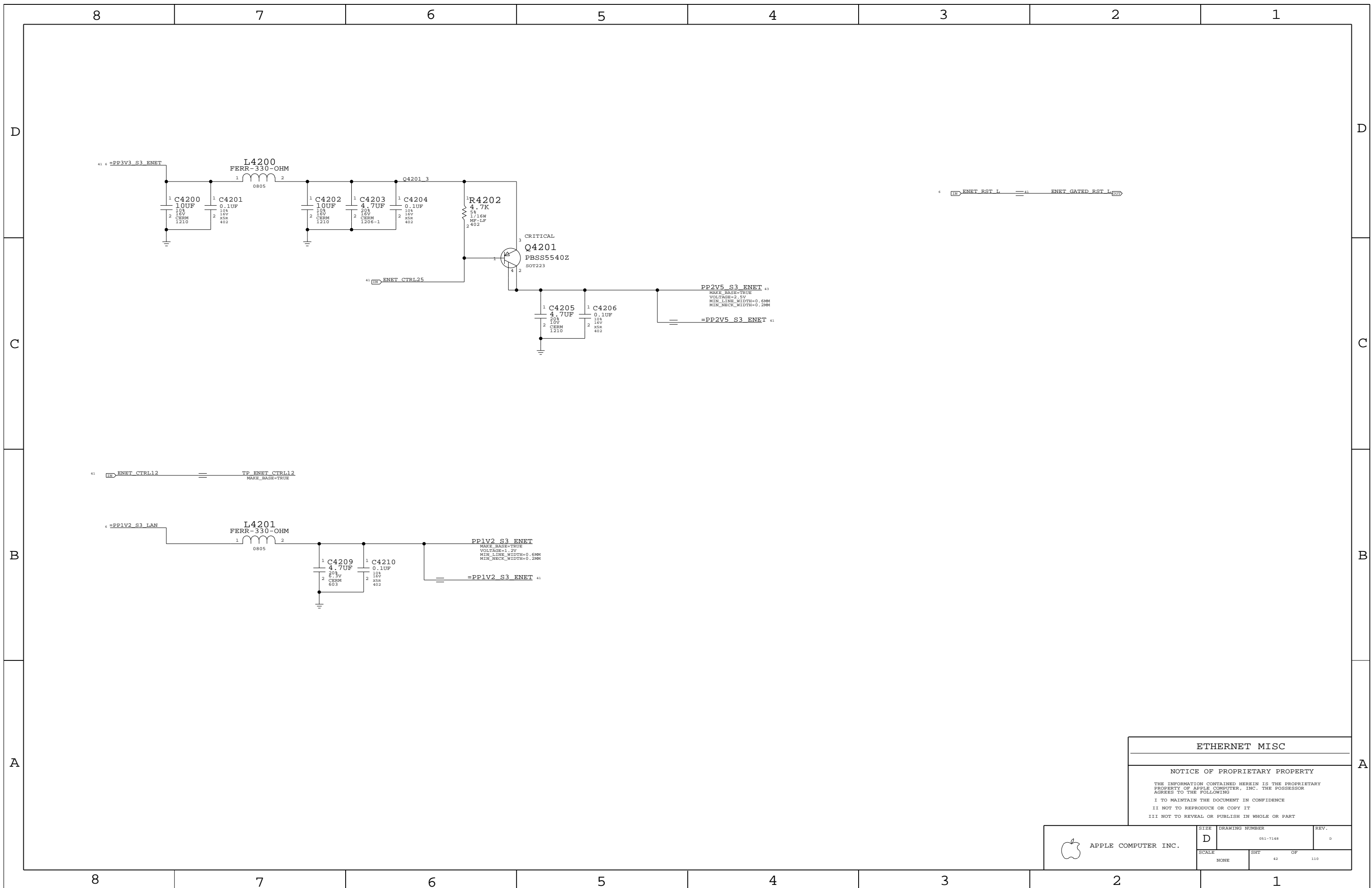
ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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	SCALE NONE	SHEET 41	OF 110



ETHERNET MISC

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. D
	SCALE NONE	SHT 42	OF 110

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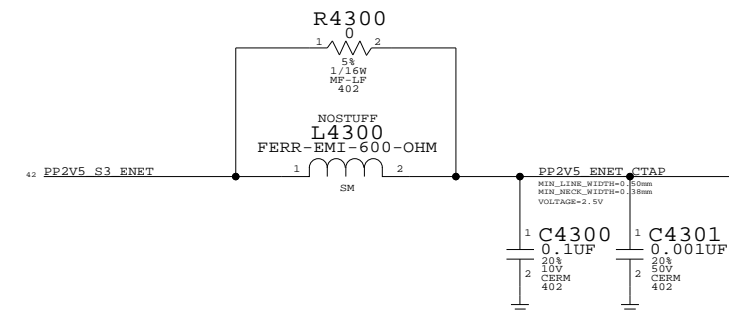
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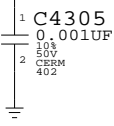
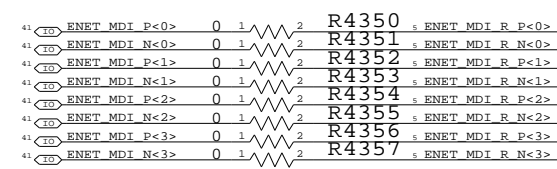
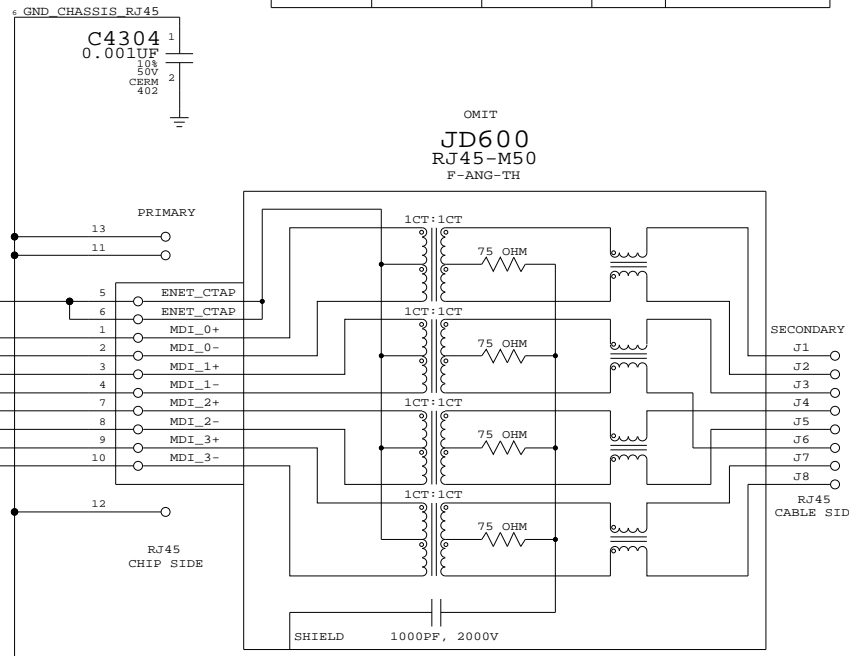
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0366	1	FOXCONN AND DELTA RJ45	JD600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:



ETHERNET CONNECTOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT OF		
NONE	43 OF 110		

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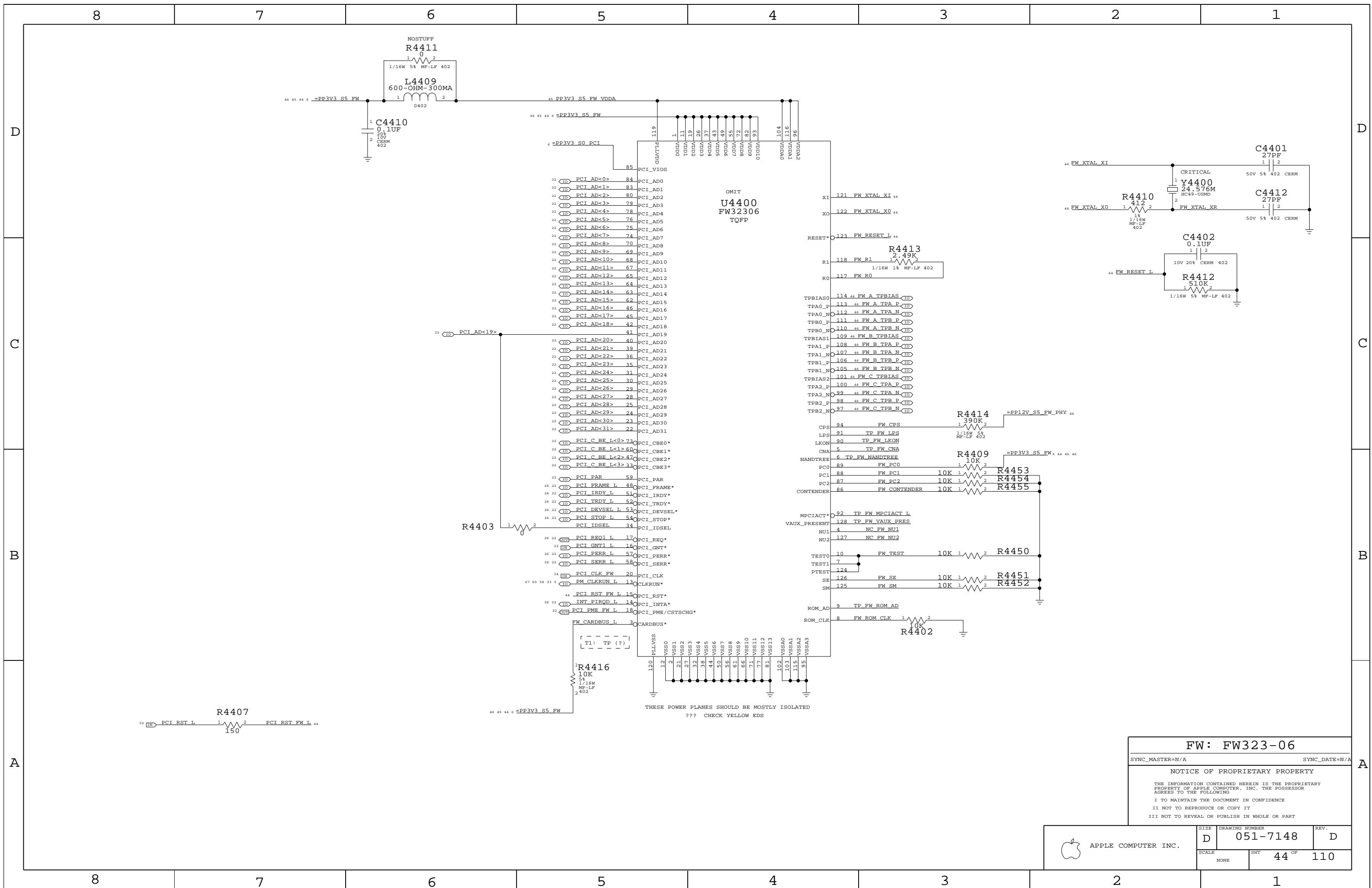
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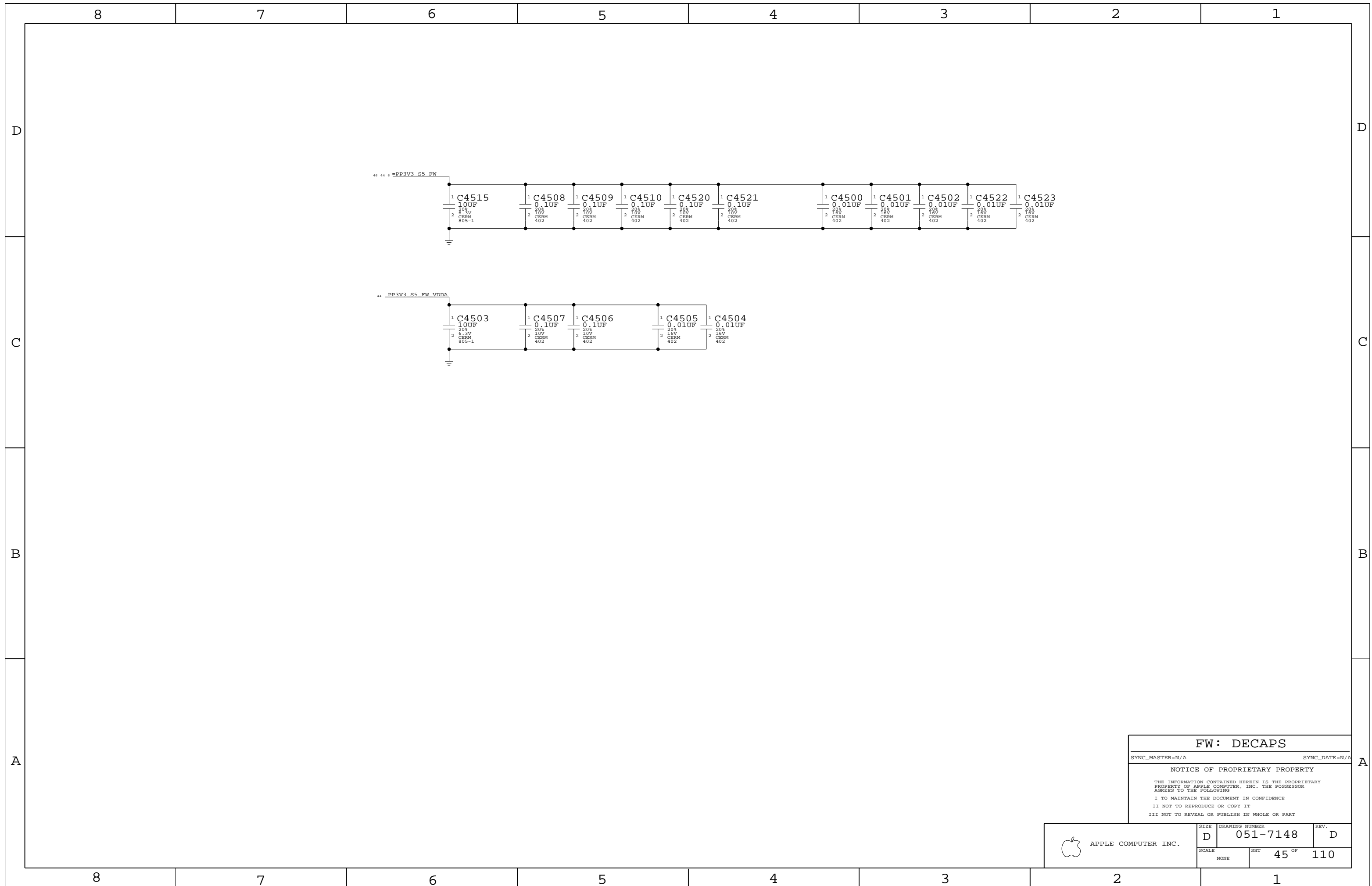
2

1



FW: FW323-06
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	44 OF	110
NONE			



FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

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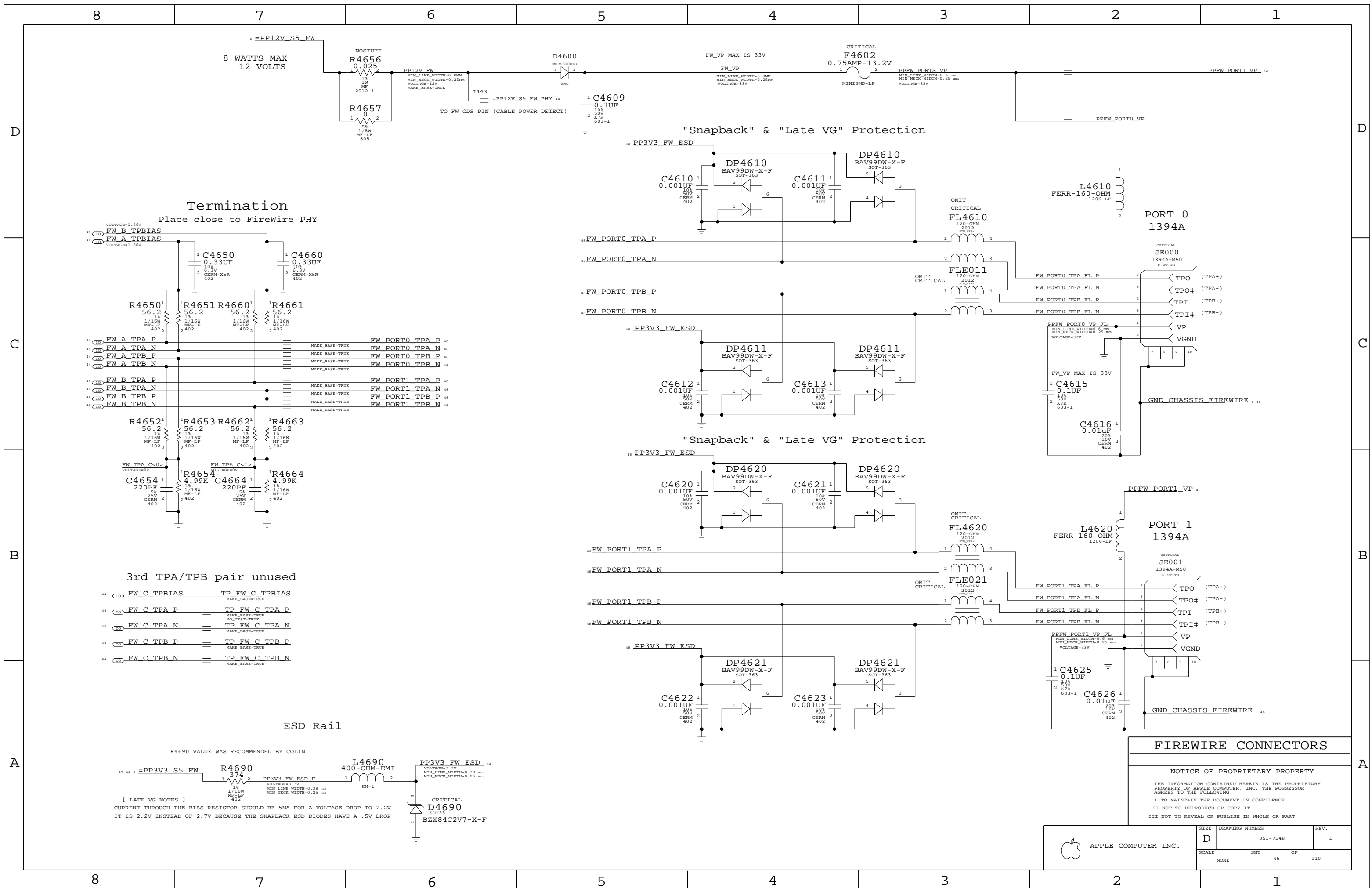
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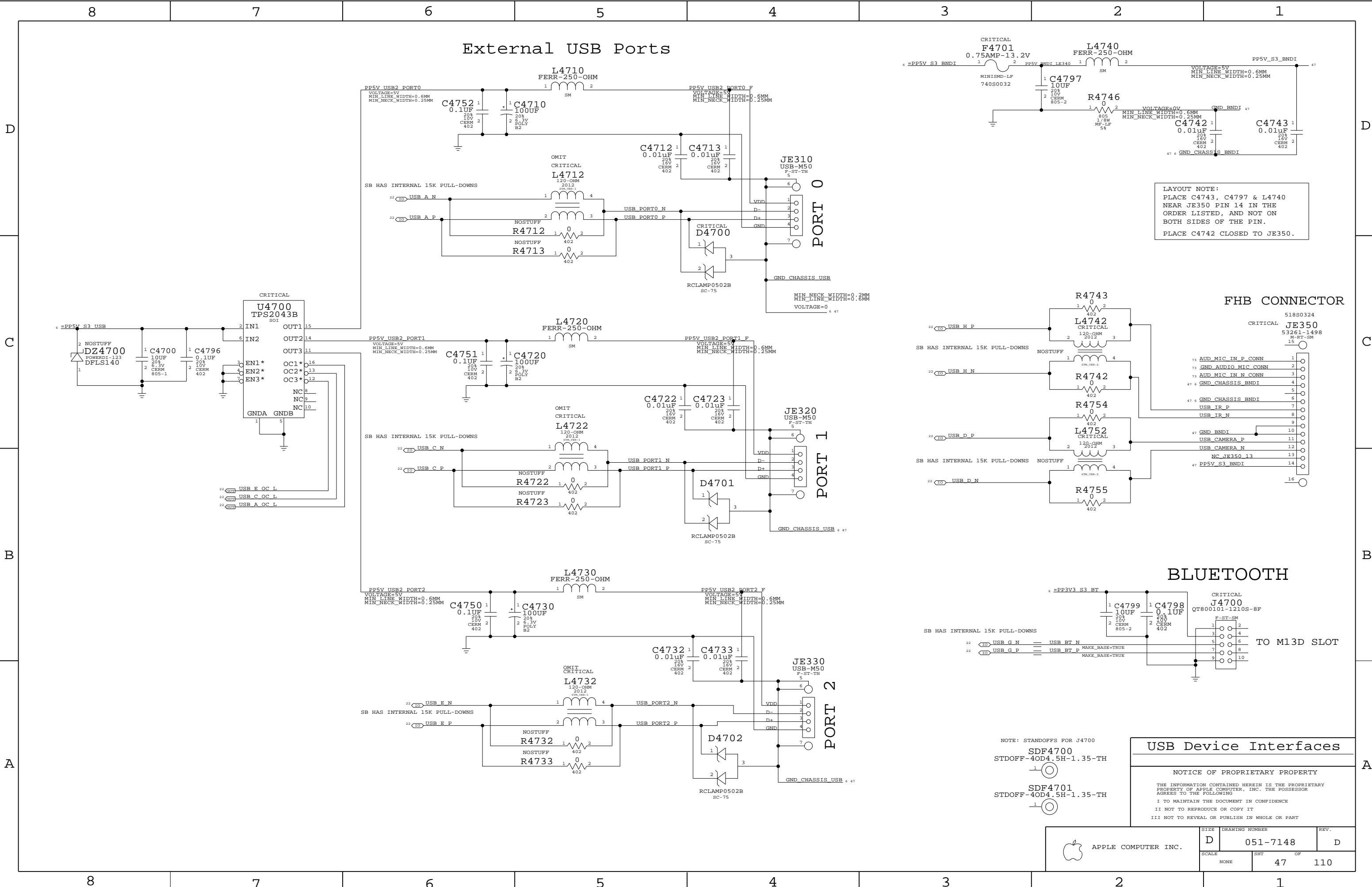
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

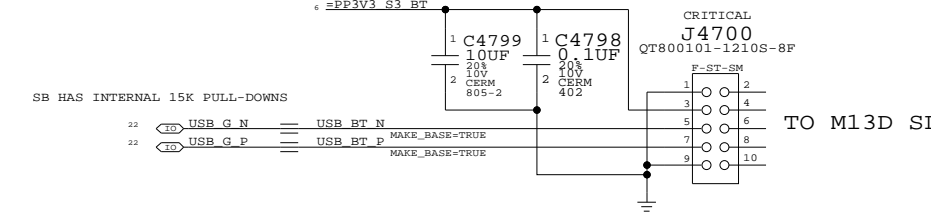
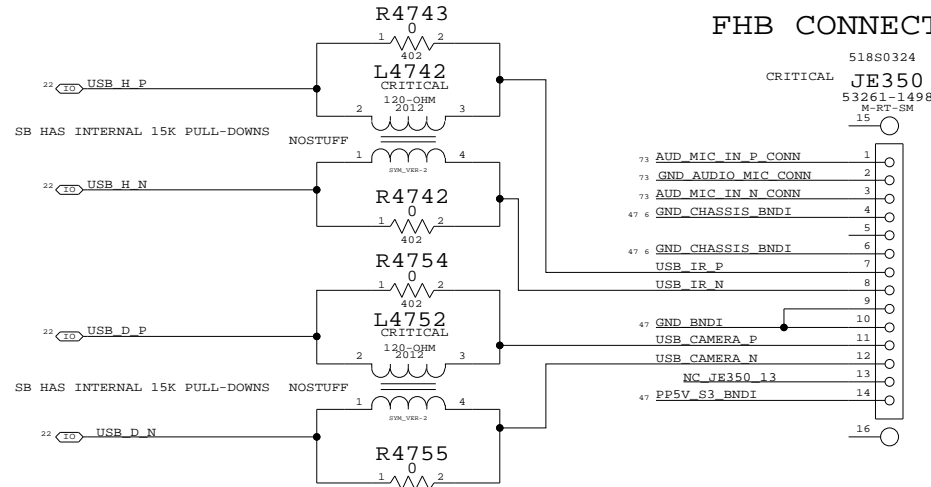
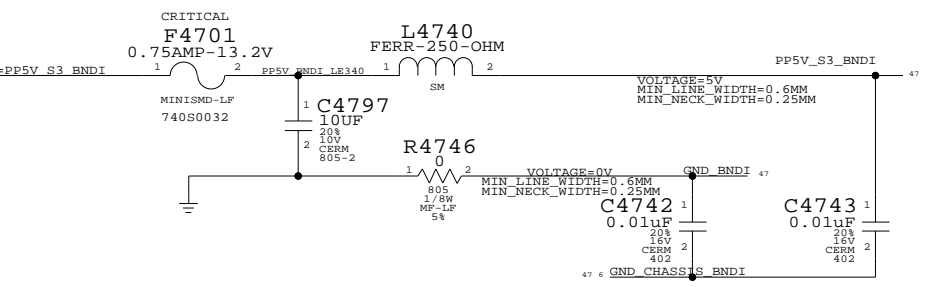
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. D
	SCALE NONE	SHIT 45 OF 110	



External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE350 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE350.



NOTE: STANDOFFS FOR J4700
 SDF4700
 STDOFF-40D4.5H-1.35-TH
 SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	NONE	SHT	OF
		47	110

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 APPLE COMPUTER INC.	<small>SIZE</small> D	<small>DRAWING NUMBER</small> 051-7148	<small>REV.</small> D
	<small>SCALE</small> NONE	<small>SHT</small> 48 OF	<small>110</small>

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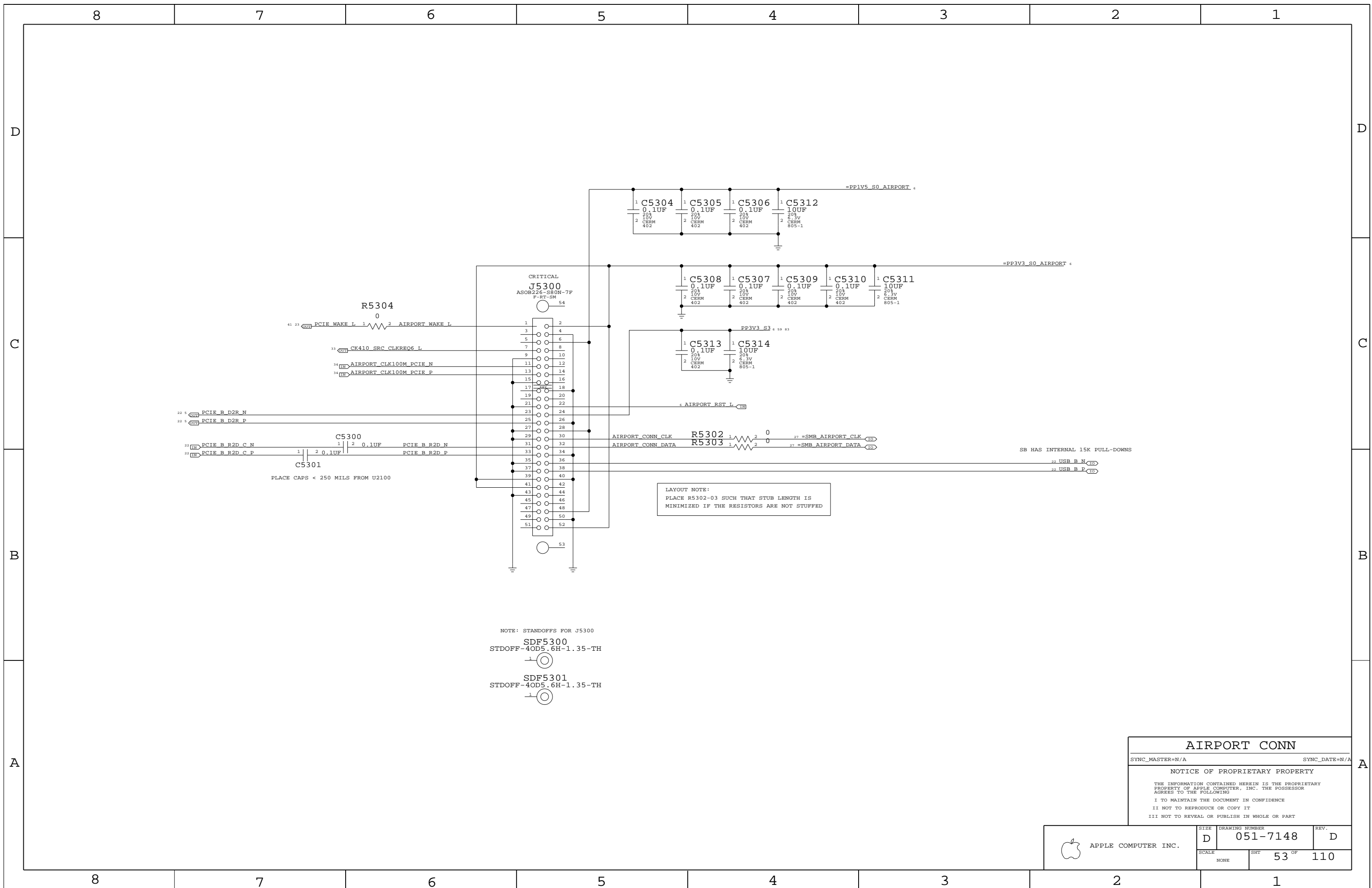
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PLACE CAPS < 250 MILS FROM U2100

LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
SDF5300
STDOFF-40D5.6H-1.35-TH
SDF5301
STDOFF-40D5.6H-1.35-TH

SB HAS INTERNAL 15K PULL-DOWNS

AIRPORT CONN
 SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	REV.	
NONE	53 OF	110	

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22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE

22 PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE

22 PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE

22 PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22 PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22 PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

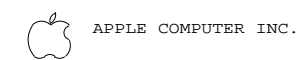
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SIZE	DRAWING NUMBER	REV.
D	051-7148	D
SCALE	SHT	OF
NONE	54	110

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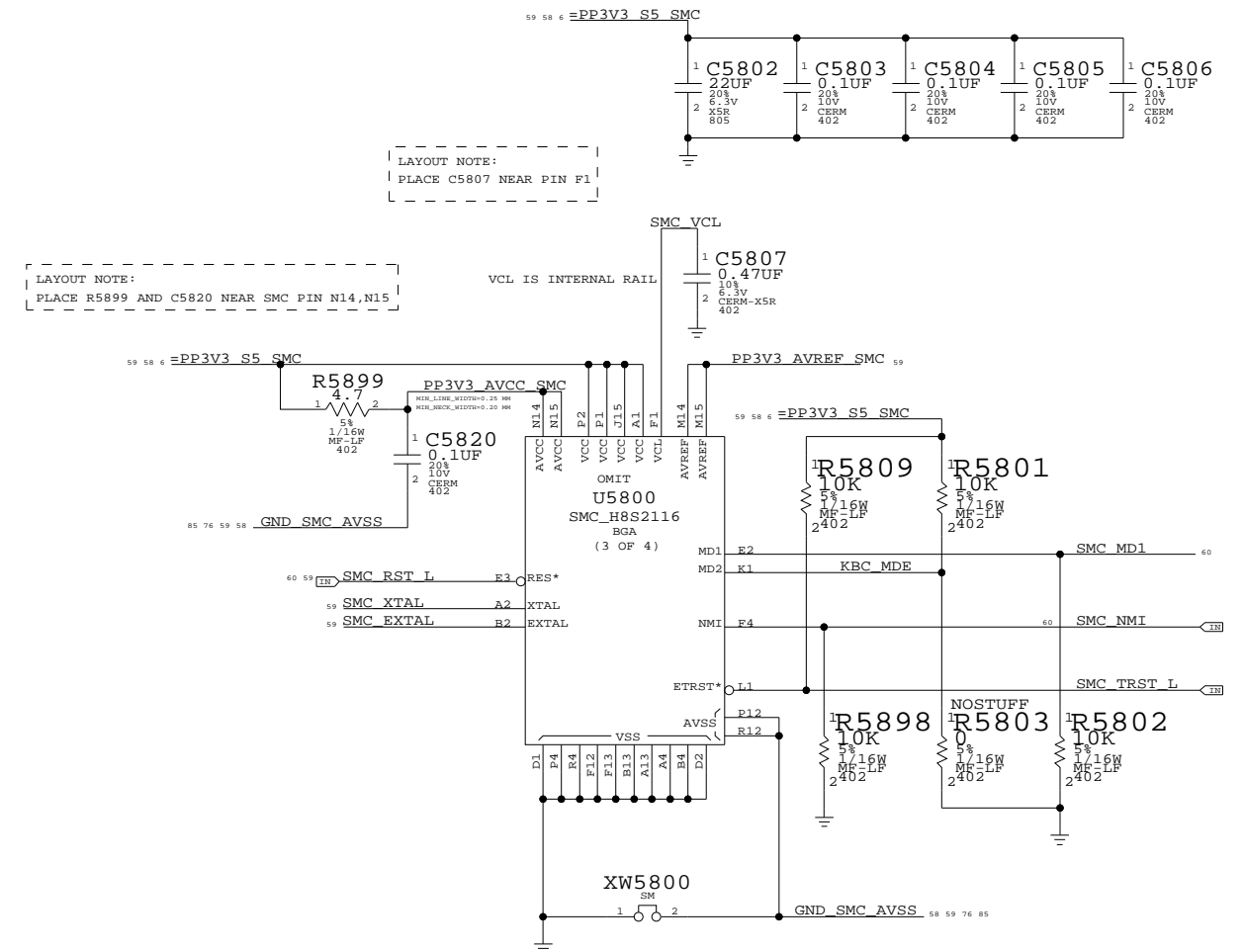
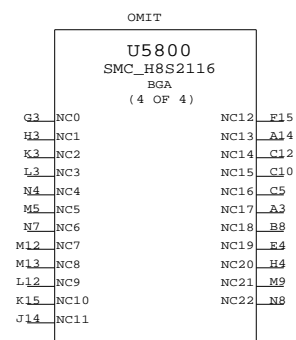
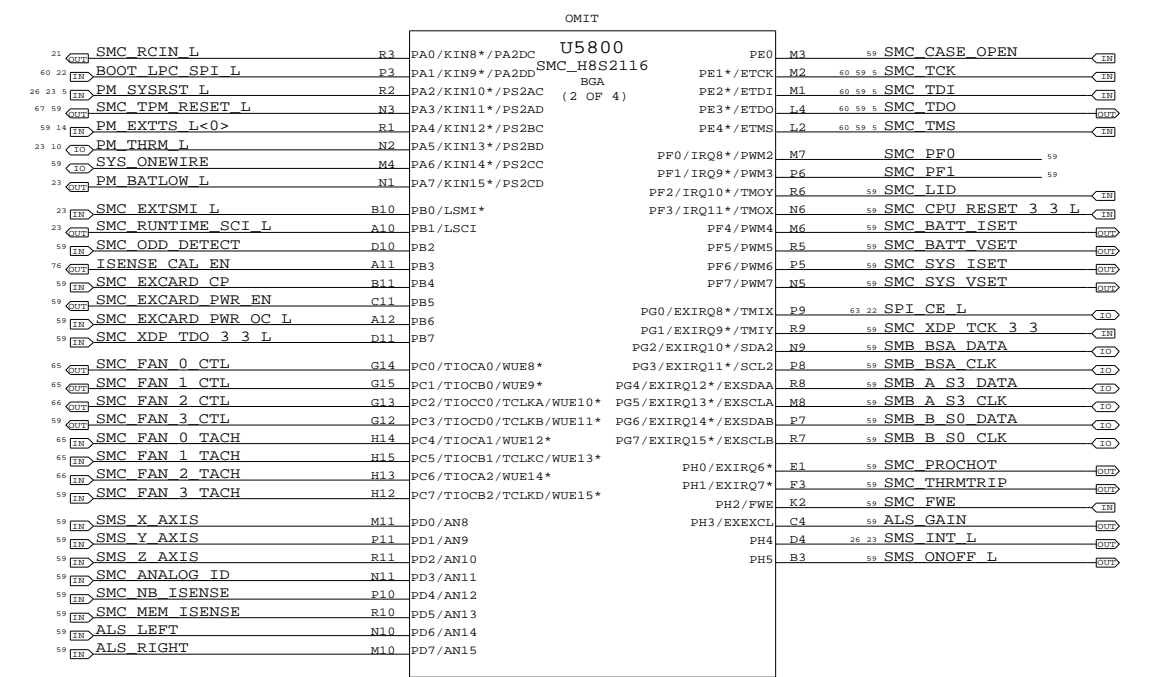
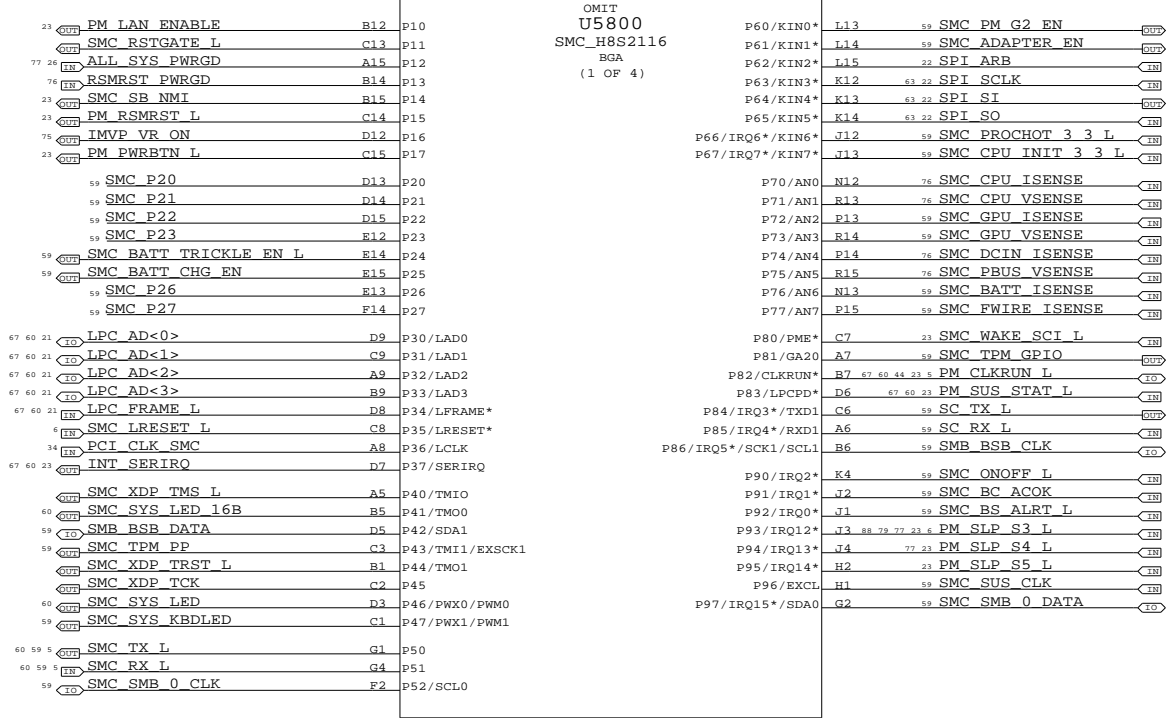
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UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

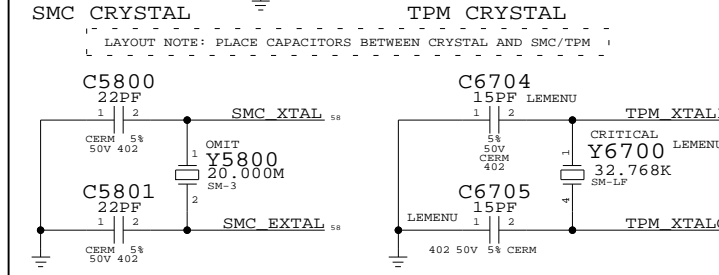
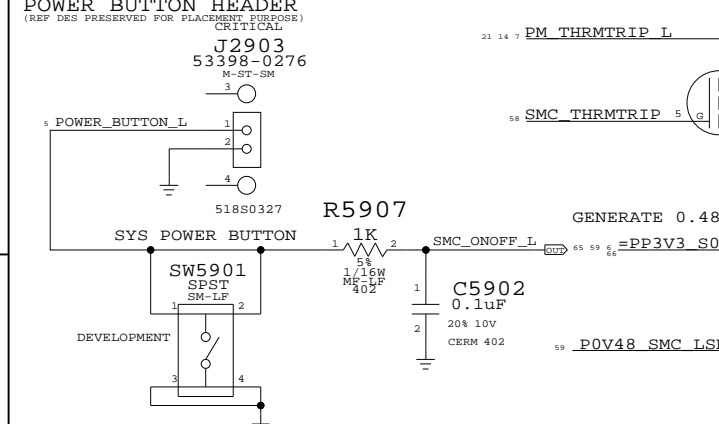
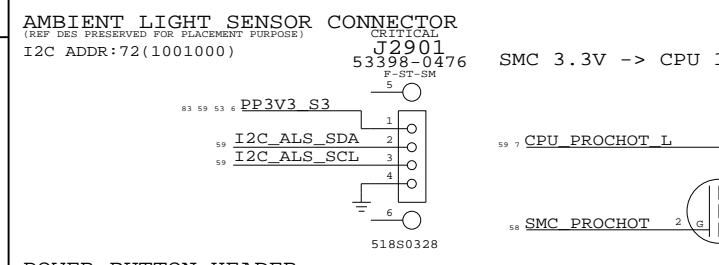
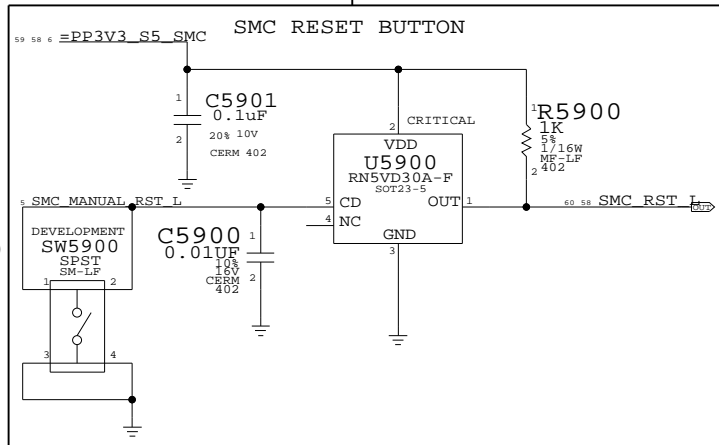
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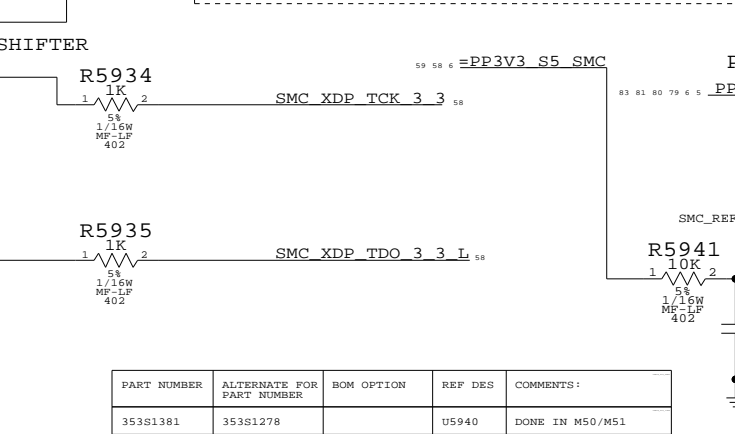
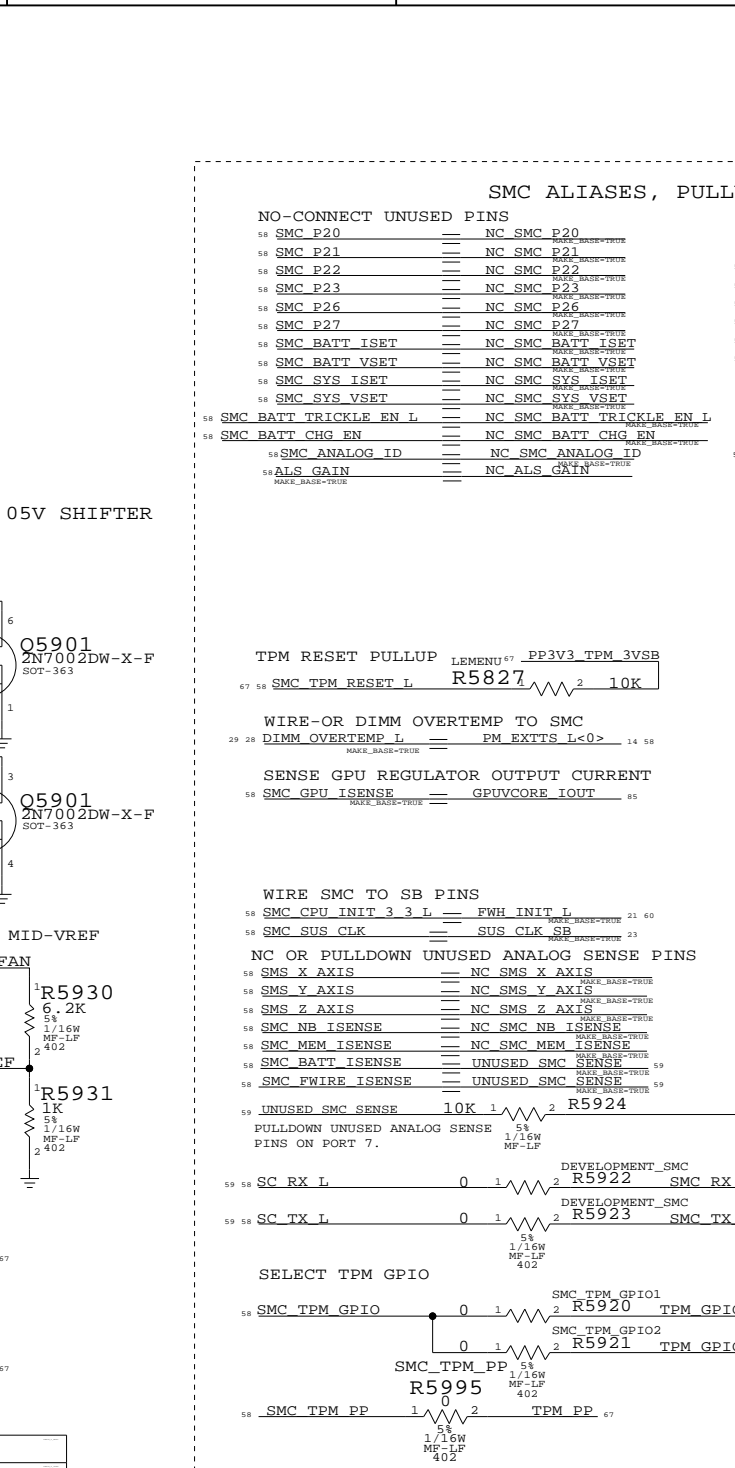
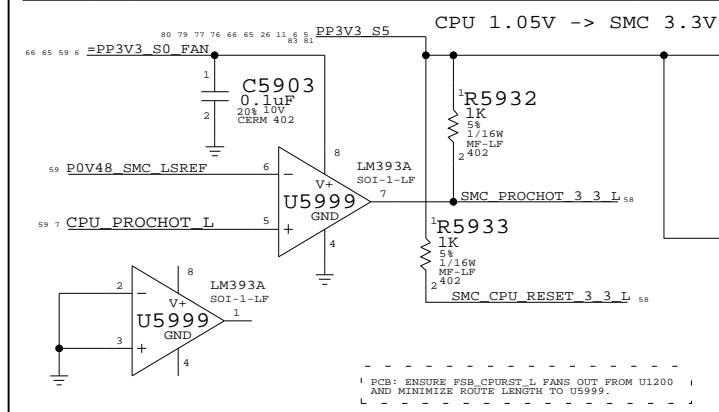
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II NOT TO REPRODUCE OR COPY IT

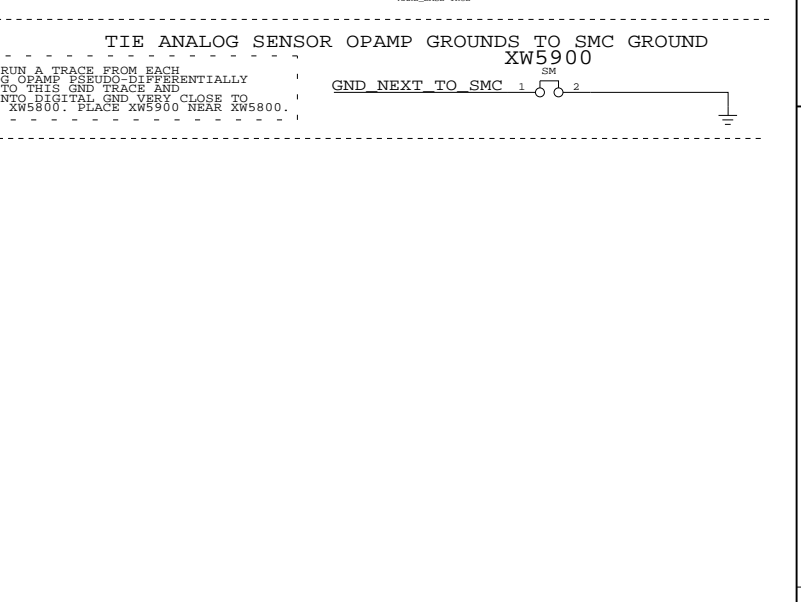
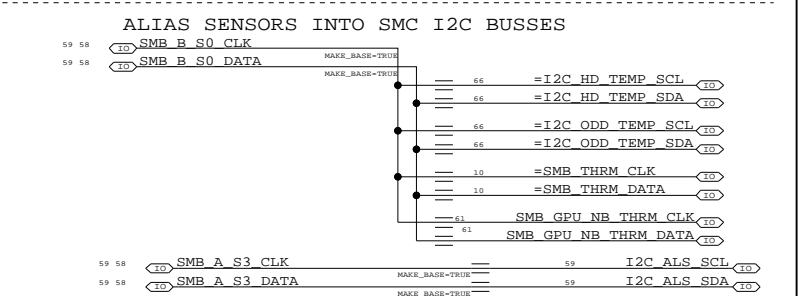
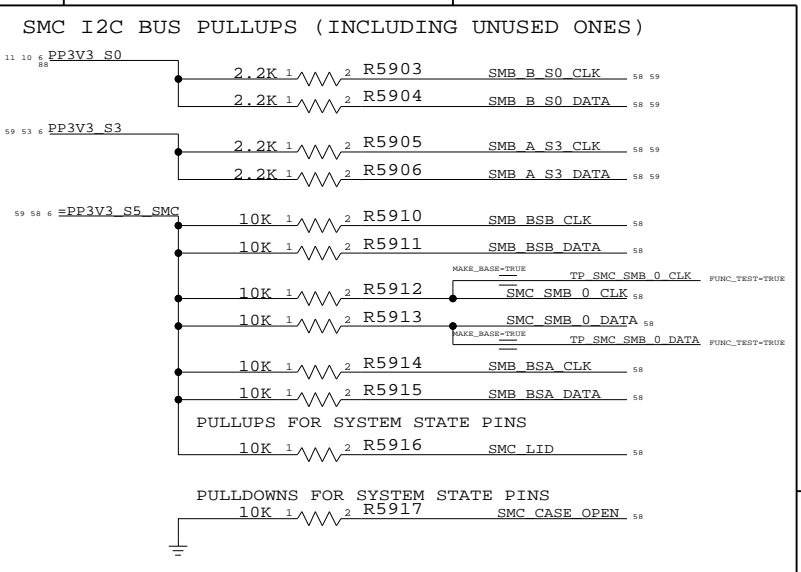
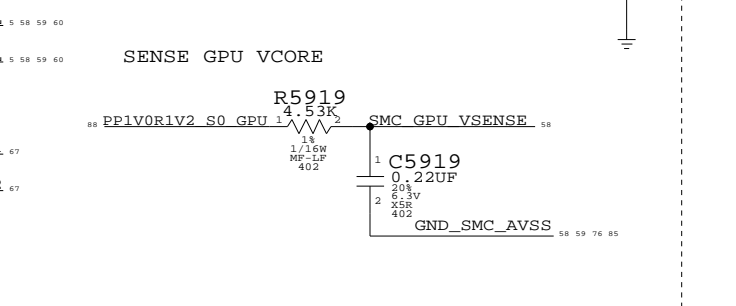
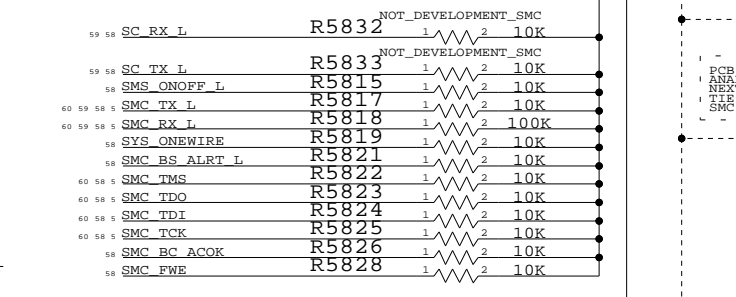
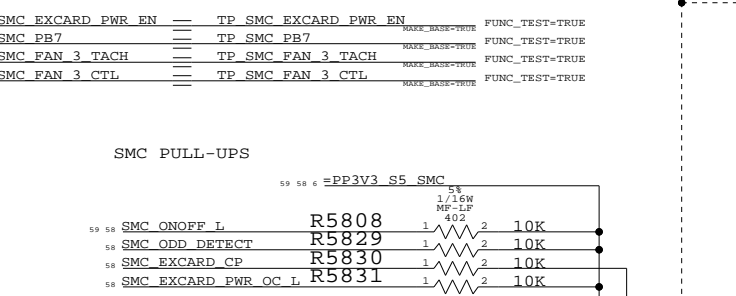
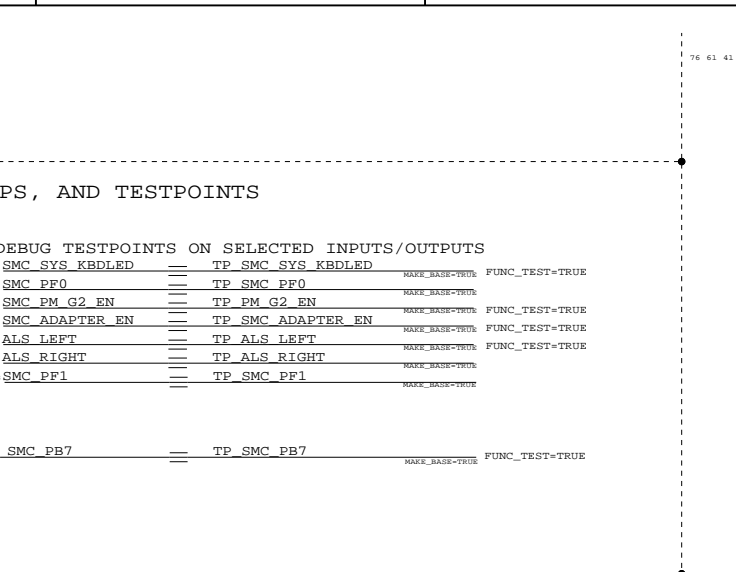
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
35381381	35381278		U5940	DONE IN M50/M51



SMC & TPM SUPPORT

NOTICE OF PROPRIETARY PROPERTY

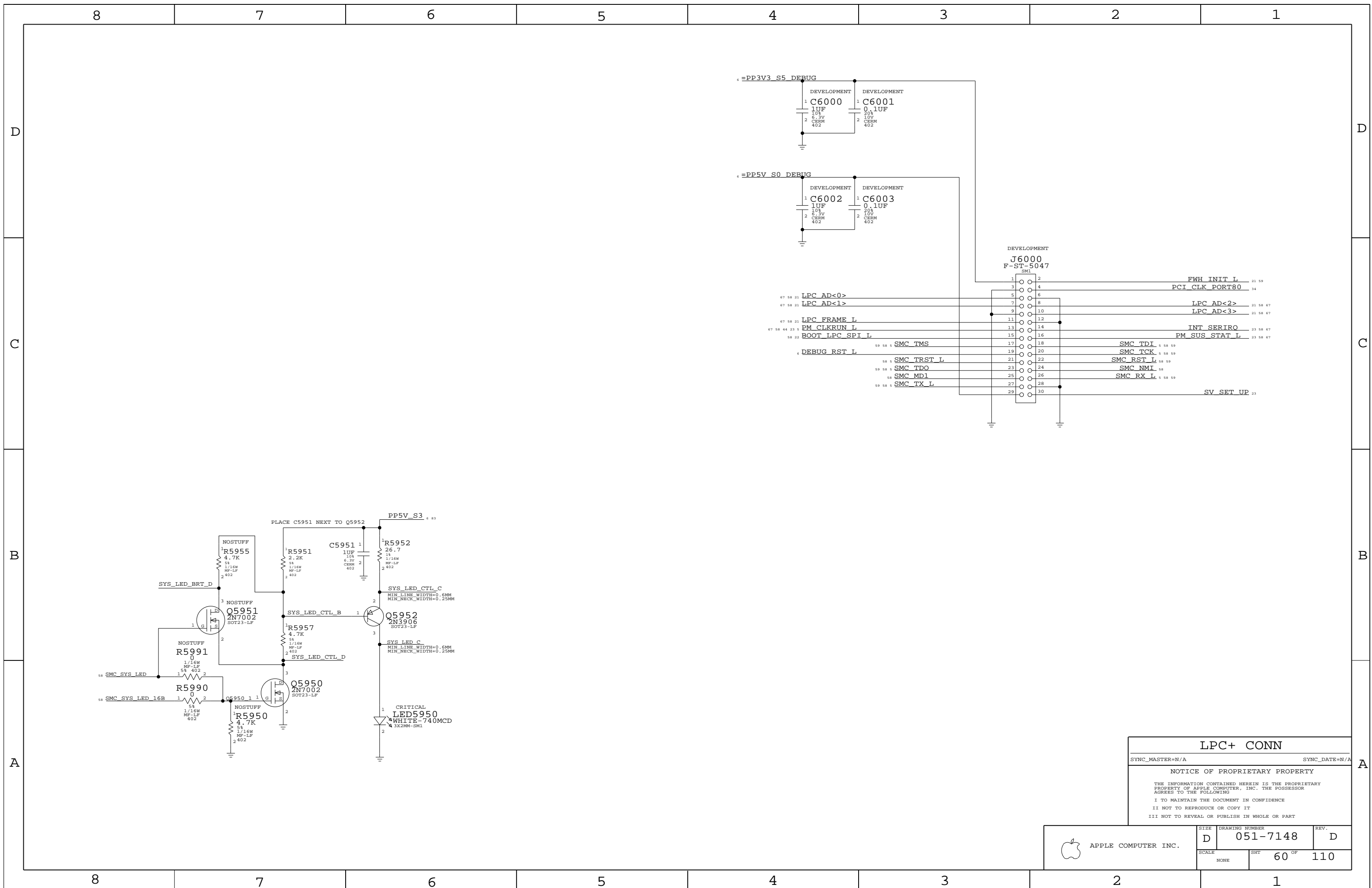
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SIZE	DRAWING NUMBER	REV.
D	051-7148	D
SCALE	SHT	OF
NONE	59	110



APPLE COMPUTER INC.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

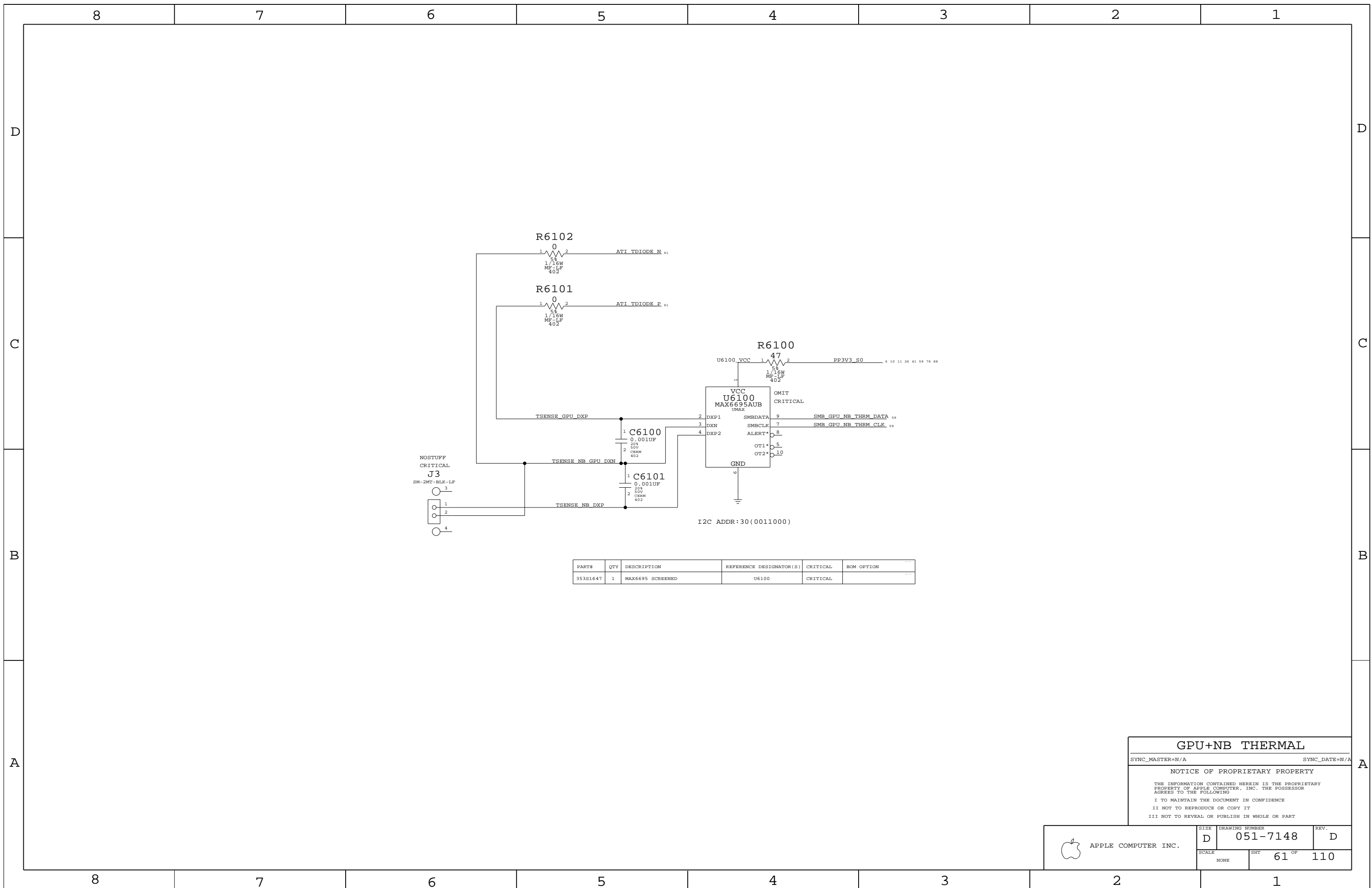
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. D
	SCALE NONE	SHEETS 60 OF 110	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1647	1	MAX6695 SCREENED	U6100	CRITICAL	

GPU+NB THERMAL

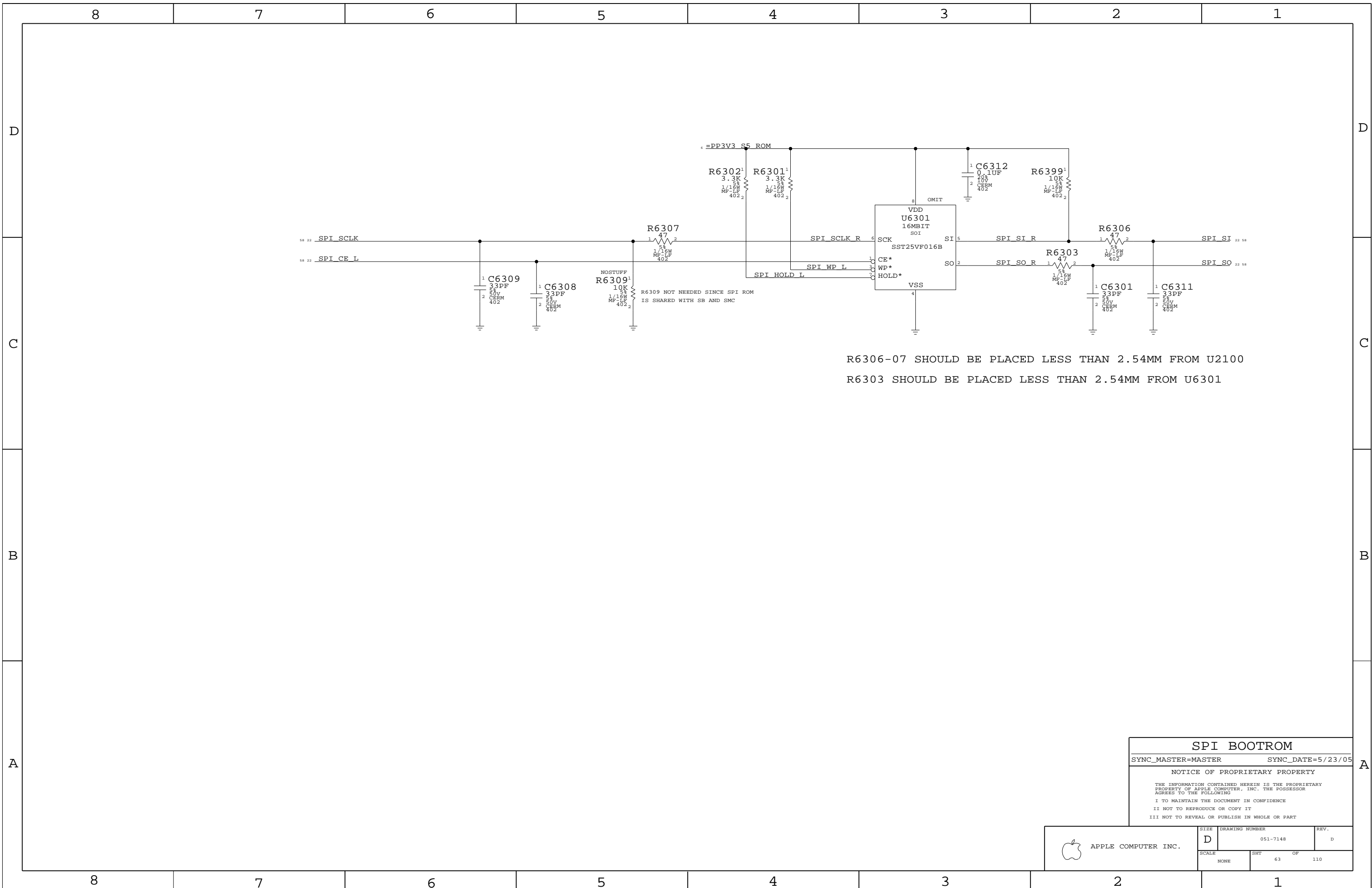
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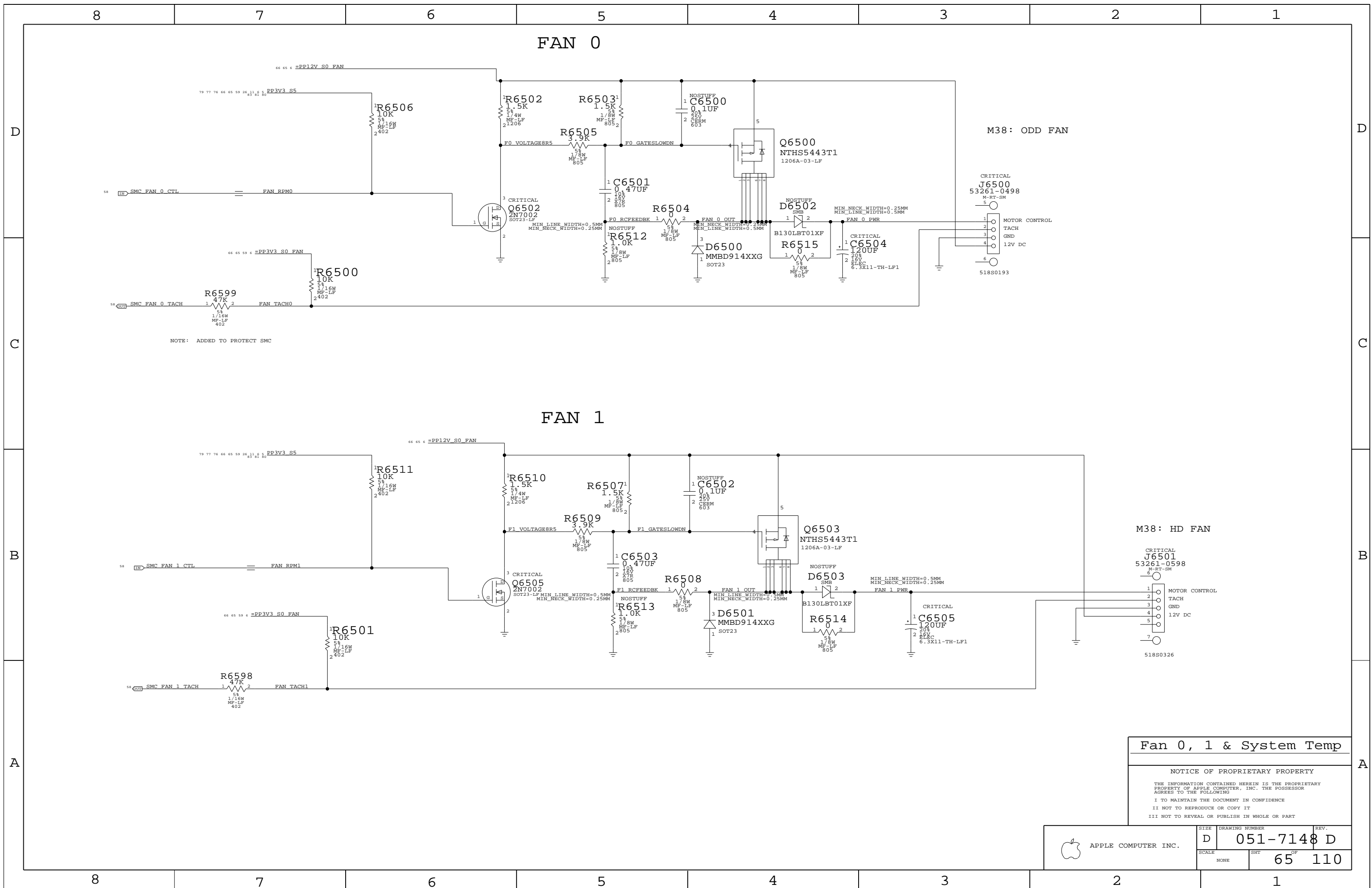
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	61 OF 110	
NONE			



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	63	110	




FAN 0

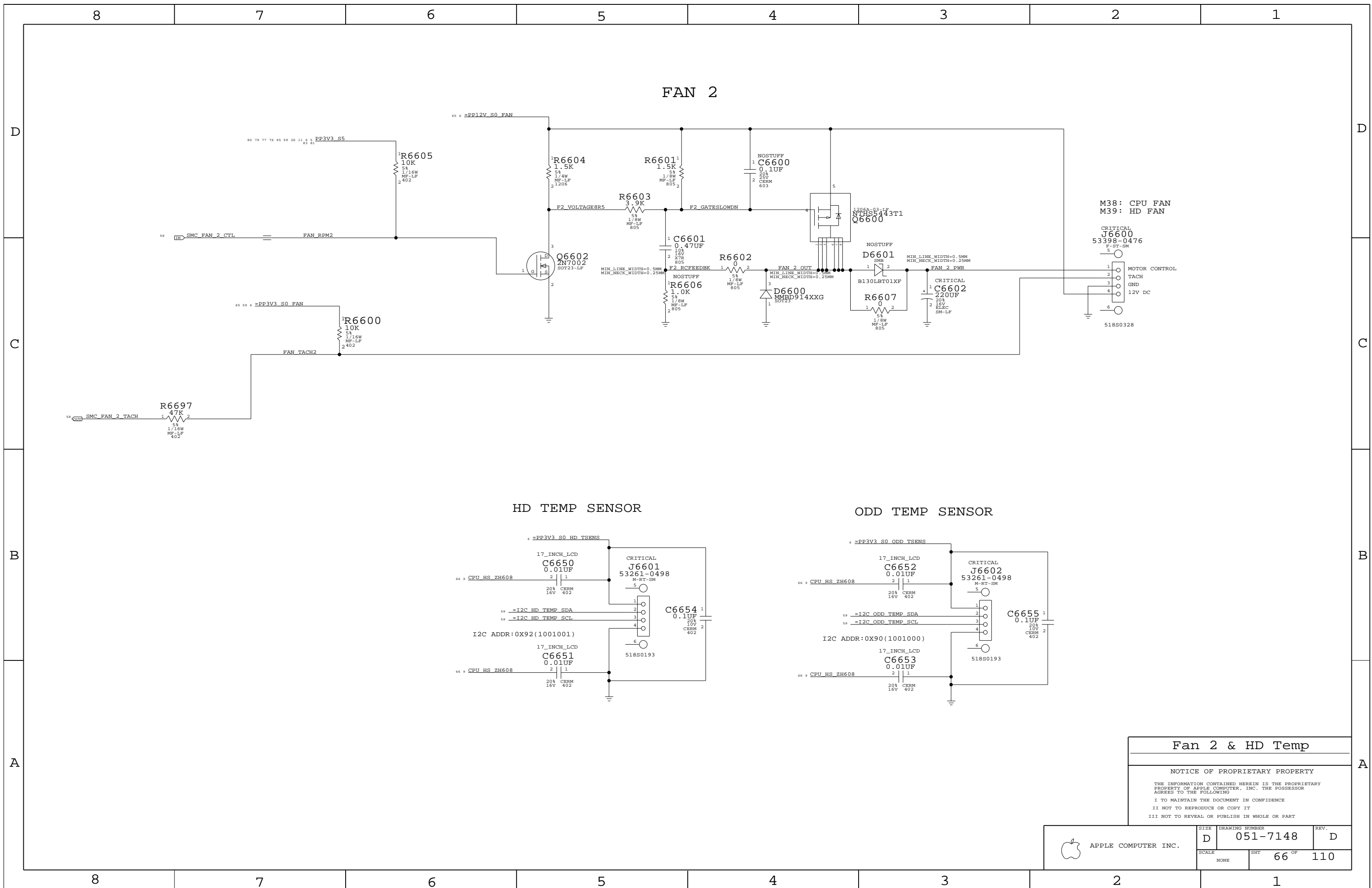
FAN 1

NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7148 D	
SCALE	SHT	OF	
	65	110	



FAN 2

HD TEMP SENSOR

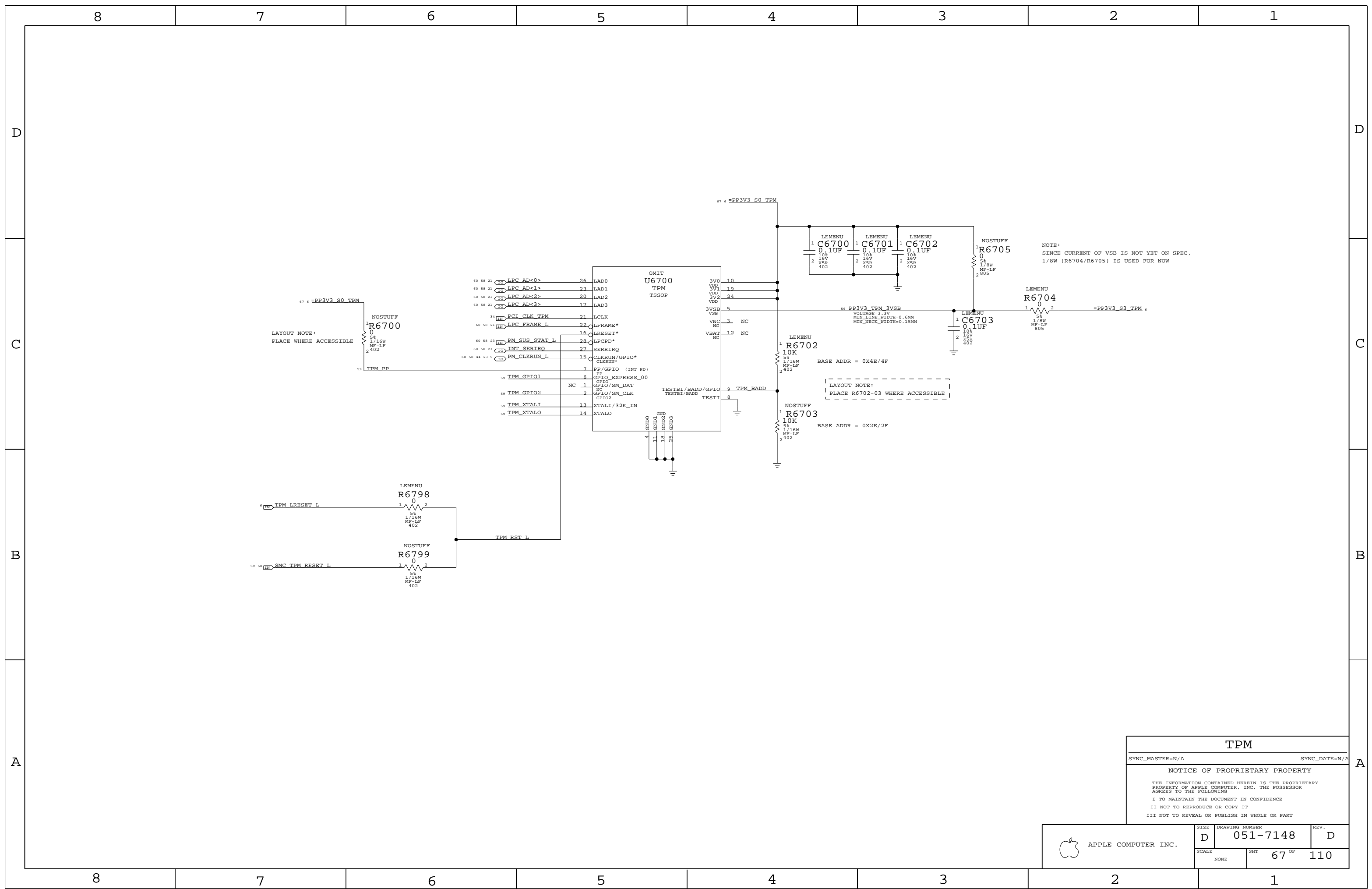
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	66 OF	110
NONE			



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

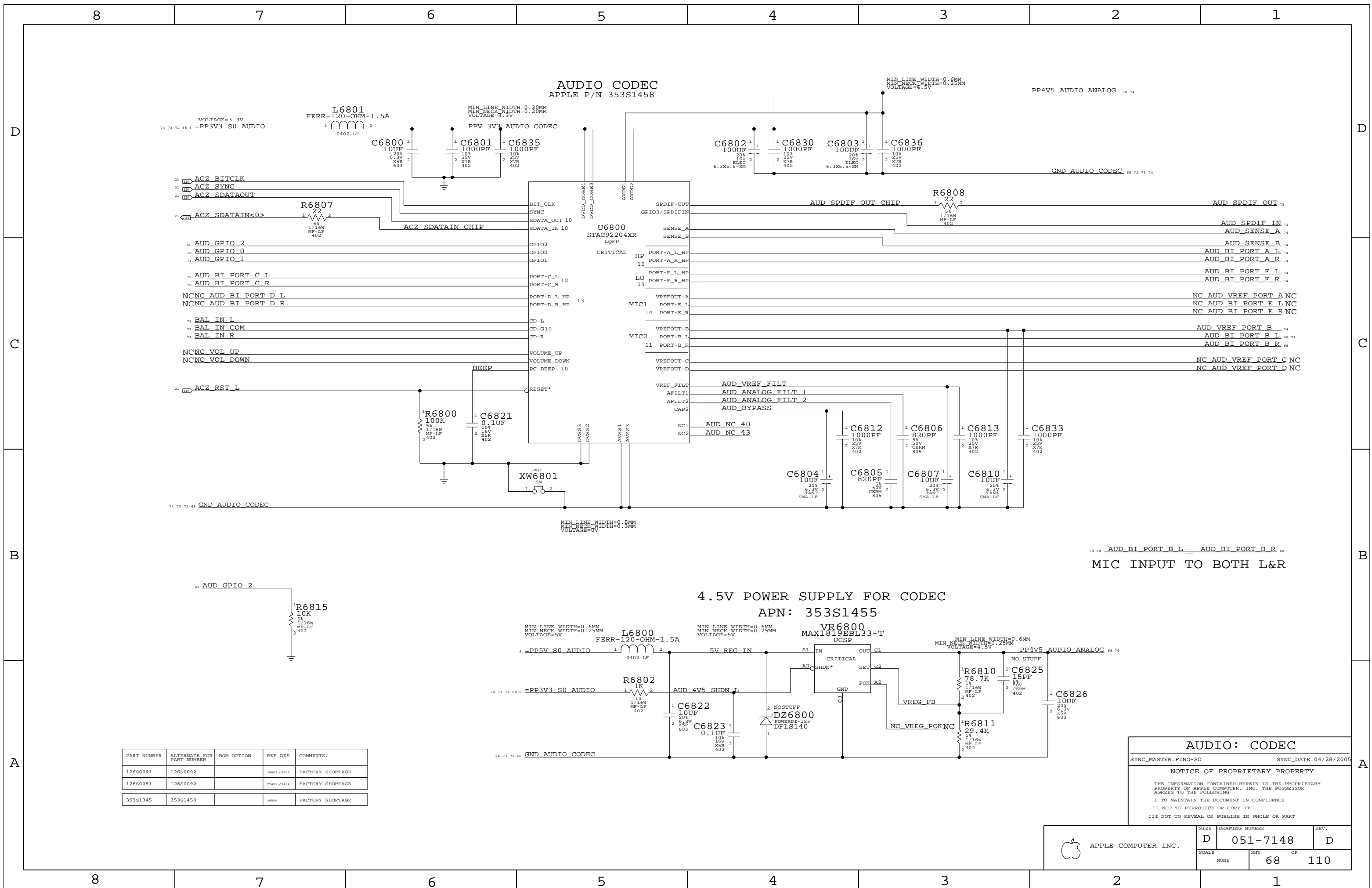
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	67 OF	110
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C6802, C6803	FACTORY SHORTAGE
126S0091	126S0092		C7403, C7404	FACTORY SHORTAGE
353S1345	353S1458		U6800	FACTORY SHORTAGE

AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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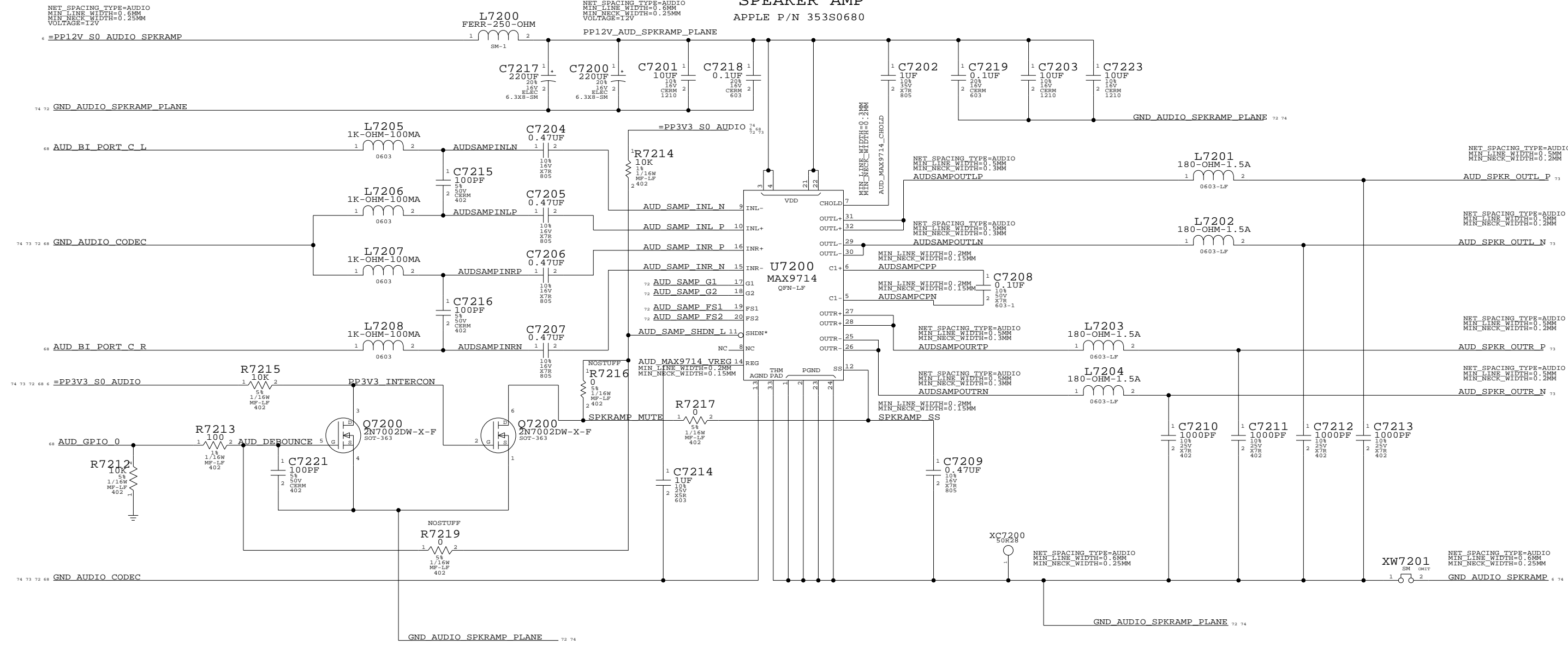
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II NOT TO REPRODUCE OR COPY IT

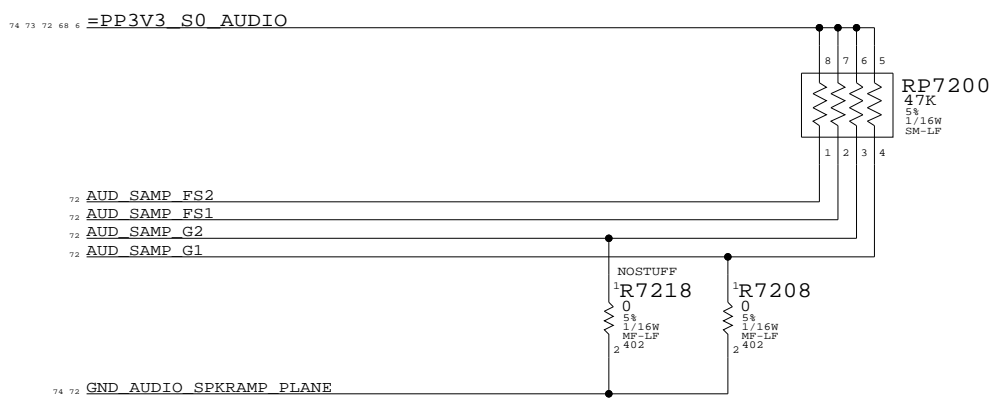
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	NONE	SHT OF	68 110

SPEAKER AMP
APPLE P/N 353S0680

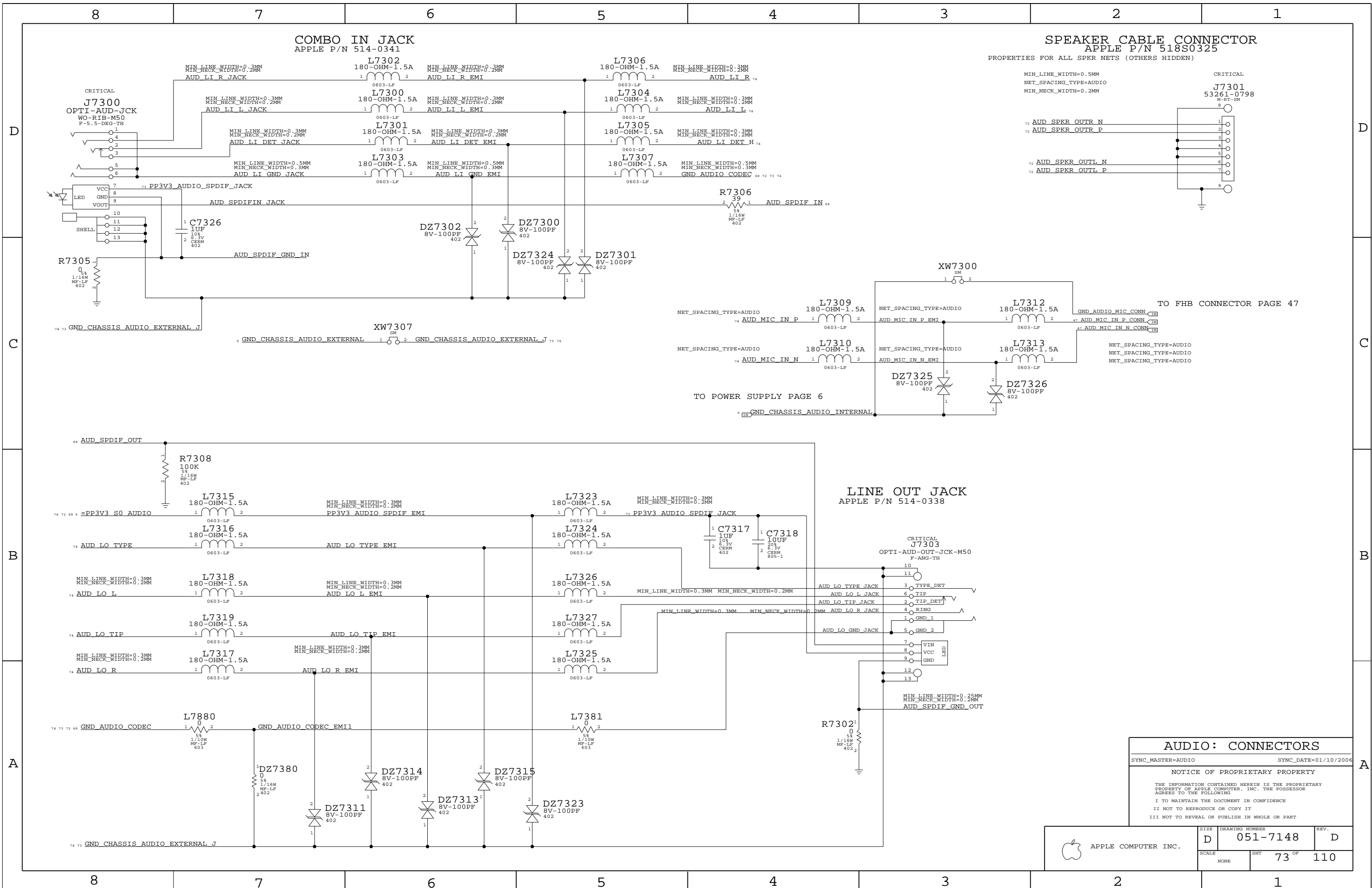


GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	NONE	SHT OF	72 OF 110



AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=01/10/2006

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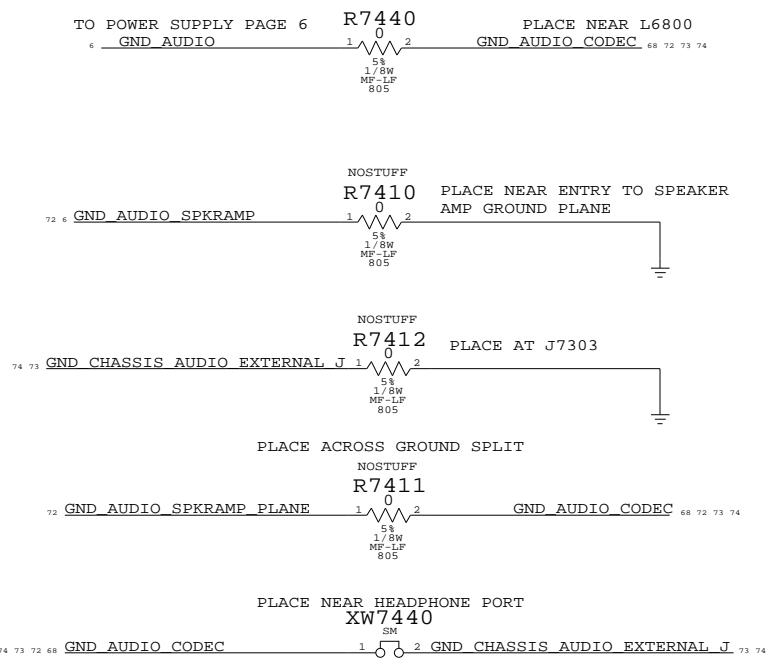
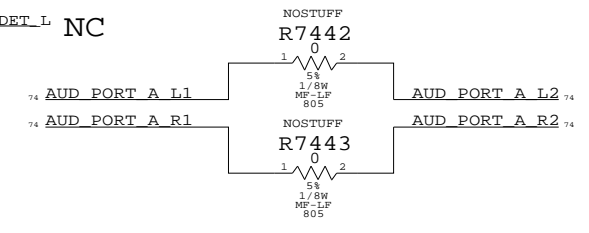
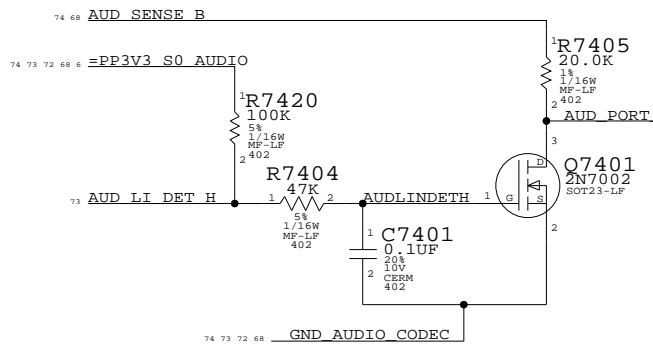
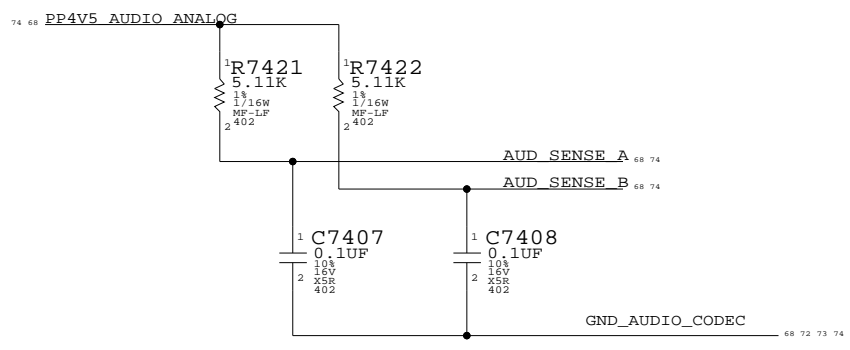
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	73 OF	110
NONE			

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

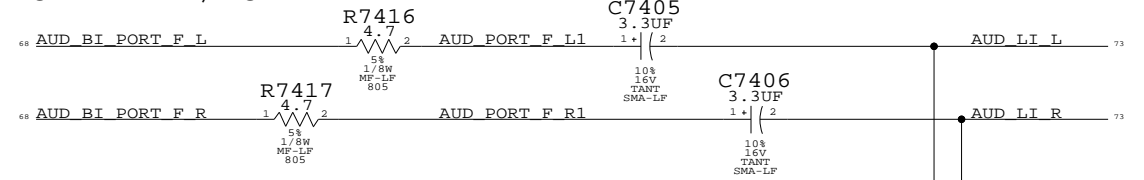
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



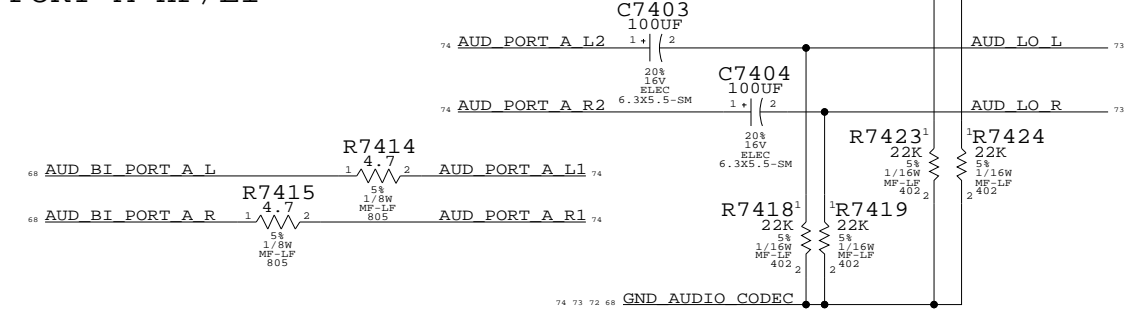
USED PORTS
 PORT A HP/LI
 PORT B MIC IN, VREF 80%
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E SPDIF OUT DELEGATE
 PORT D

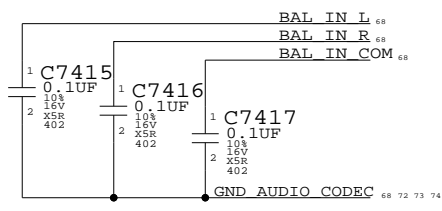
PORT F LI/LO



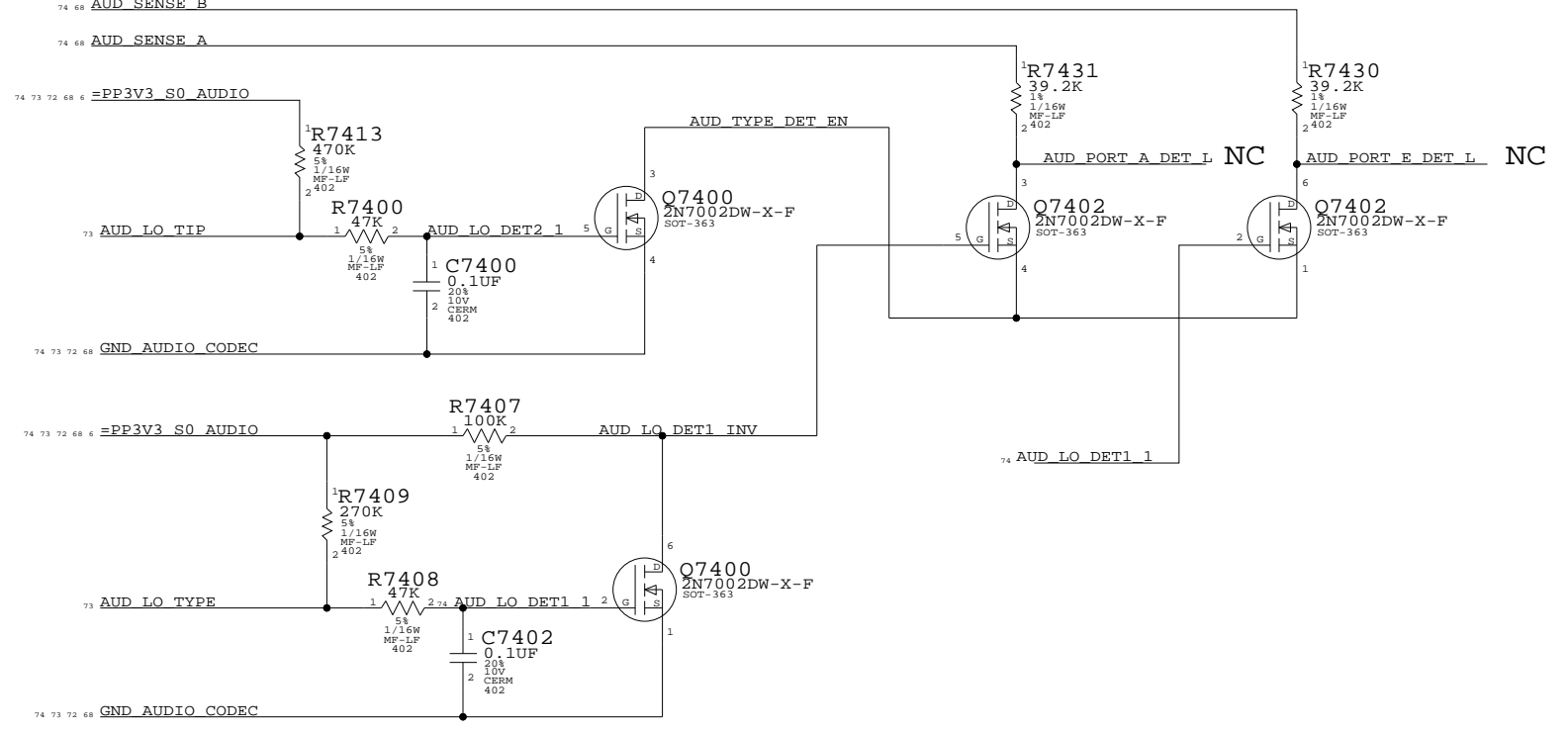
PORT A HP/LI



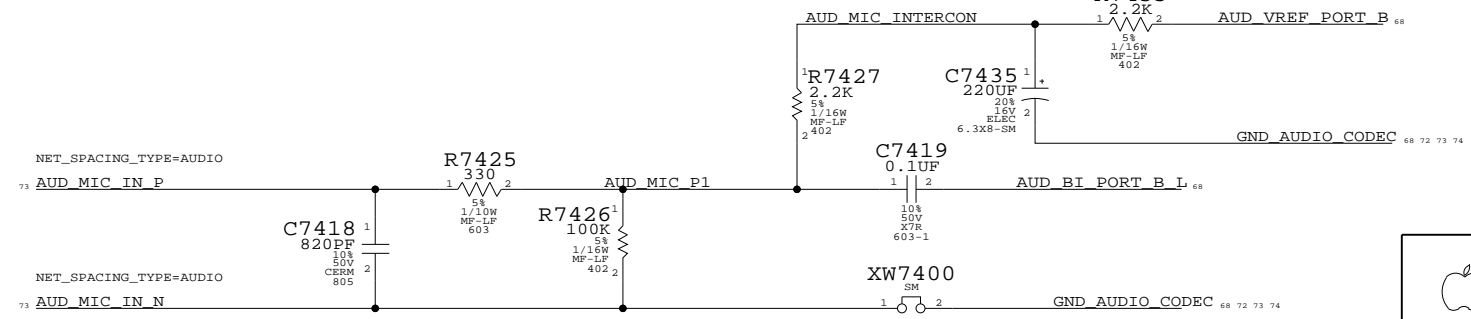
UNUSED PORT TERMINATION



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

NOTICE OF PROPRIETARY PROPERTY

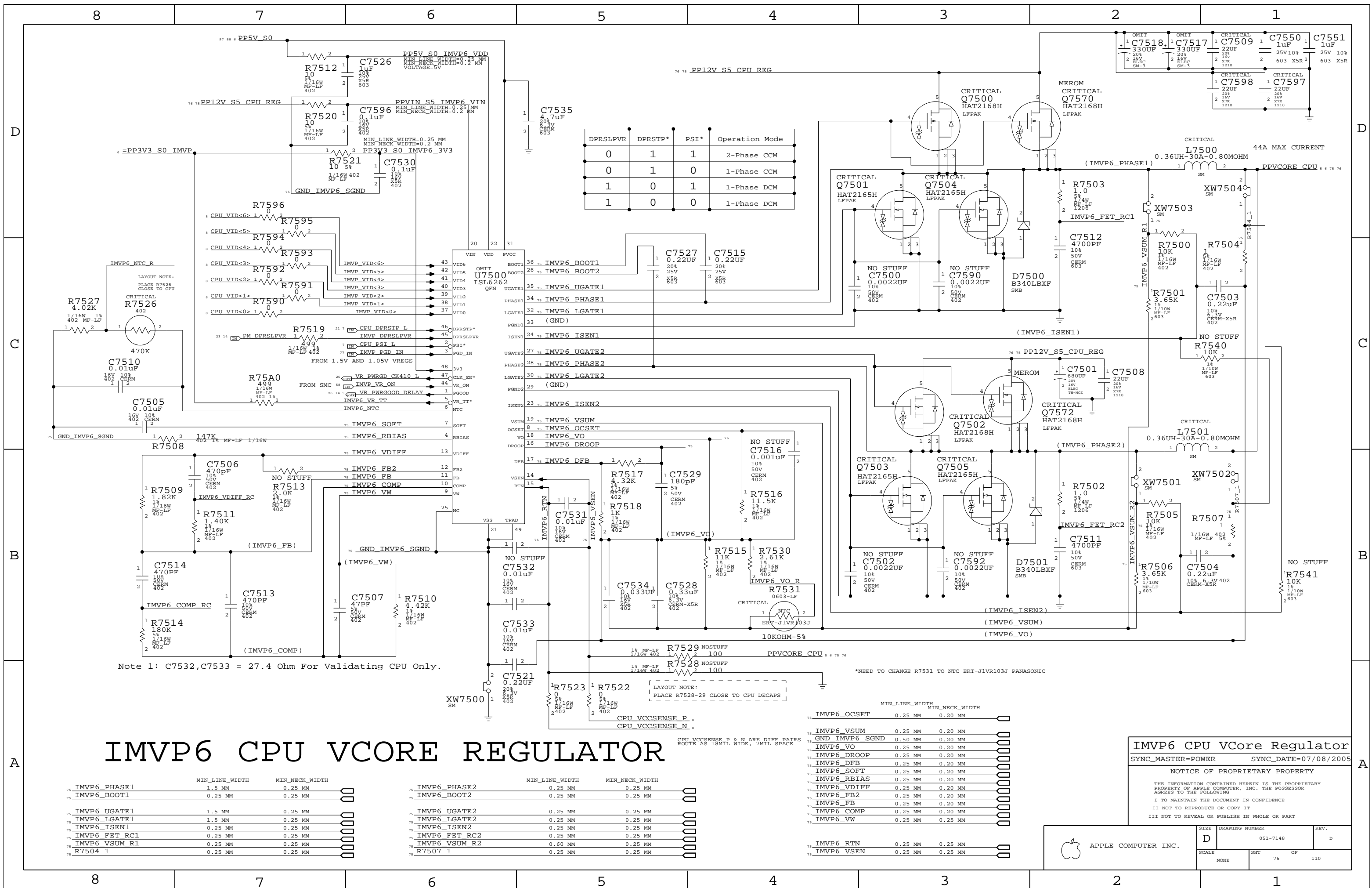
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	74 OF	110
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

IMVP6_PHASE1	IMVP6_PHASE2	IMVP6_VSUM	IMVP6_VO
NO STUFF	NO STUFF	NO STUFF	NO STUFF
C7500	C7502	C7503	C7504
0.0022UF	0.0022UF	0.22uF	0.22uF

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

LAYOUT NOTE:
PLACE R7528-29 CLOSE TO CPU DECAPS

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

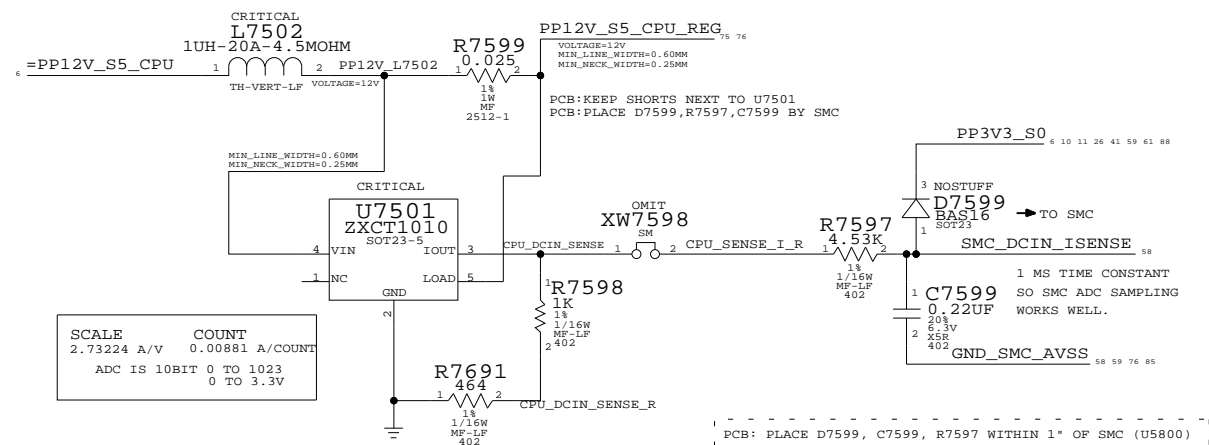
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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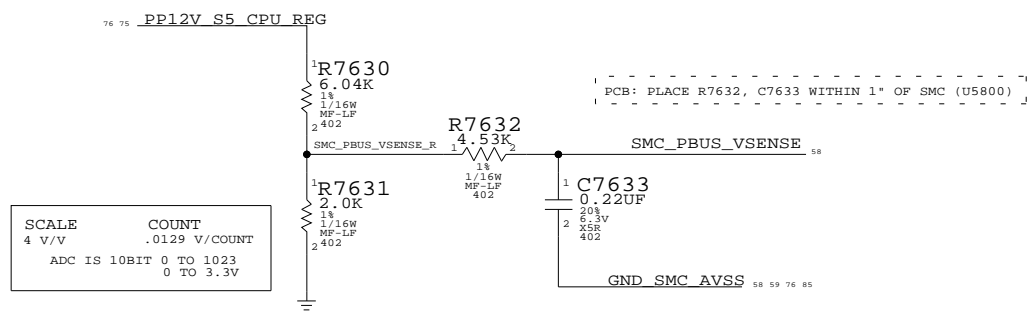
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHEET	OF	
NONE	75	110	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



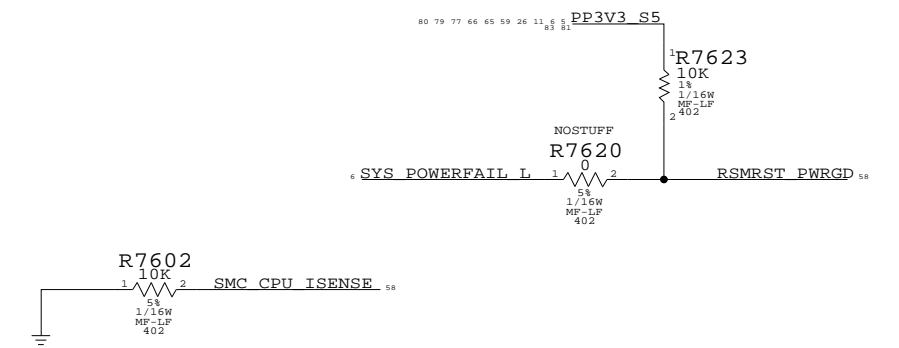
SCALE COUNT
2.73224 A/V 0.00881 A/COUNT
ADC IS 10BIT 0 TO 1023
 0 TO 3.3V

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

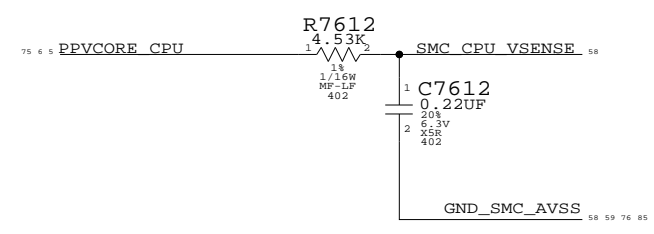


SCALE COUNT
4 V/V .0129 V/COUNT
ADC IS 10BIT 0 TO 1023
 0 TO 3.3V

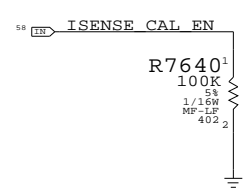
SMC PWRGD PULLUP



PROCESSOR VCORE SENSE



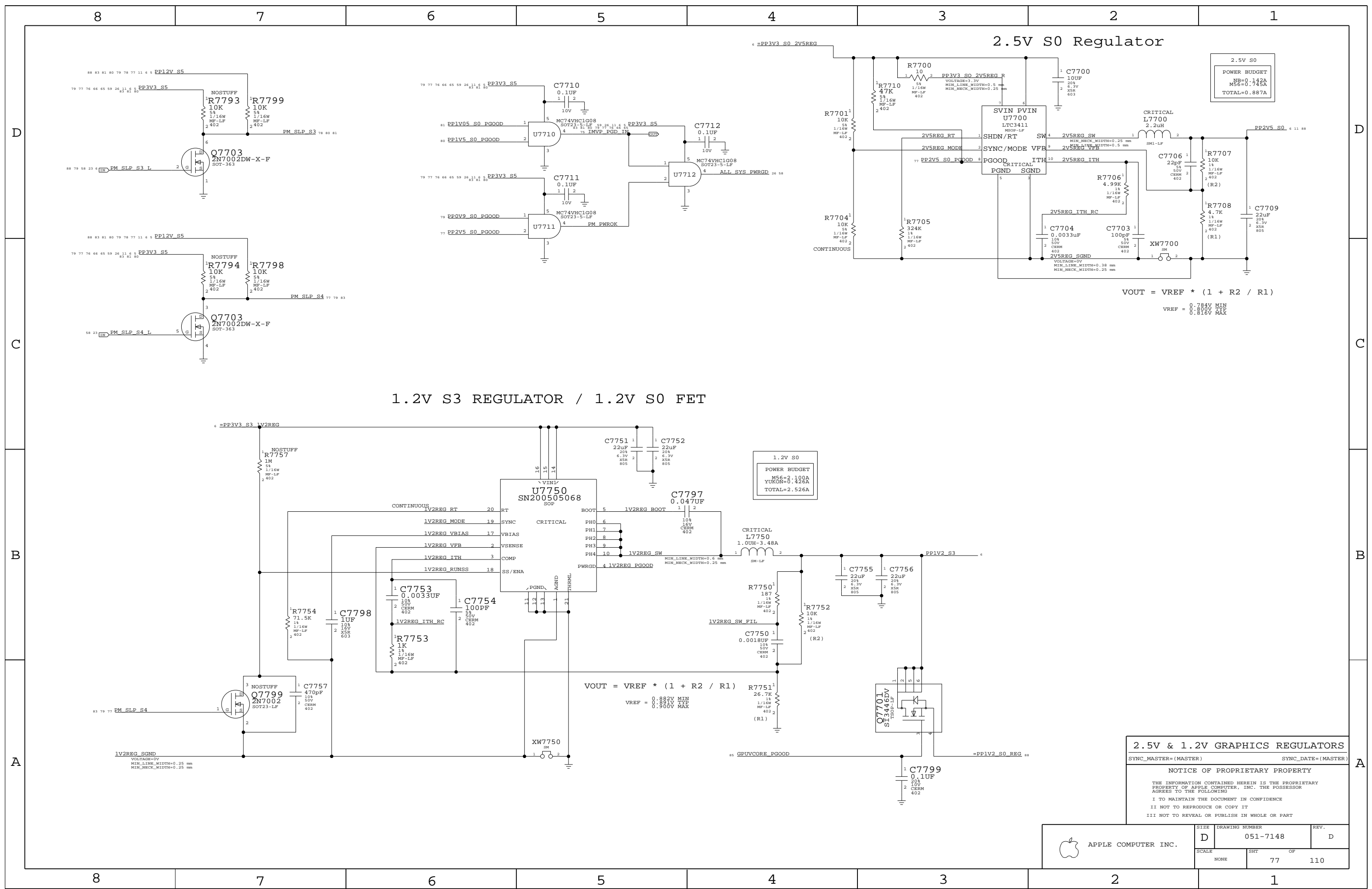
Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	76 OF	110
NONE			



2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

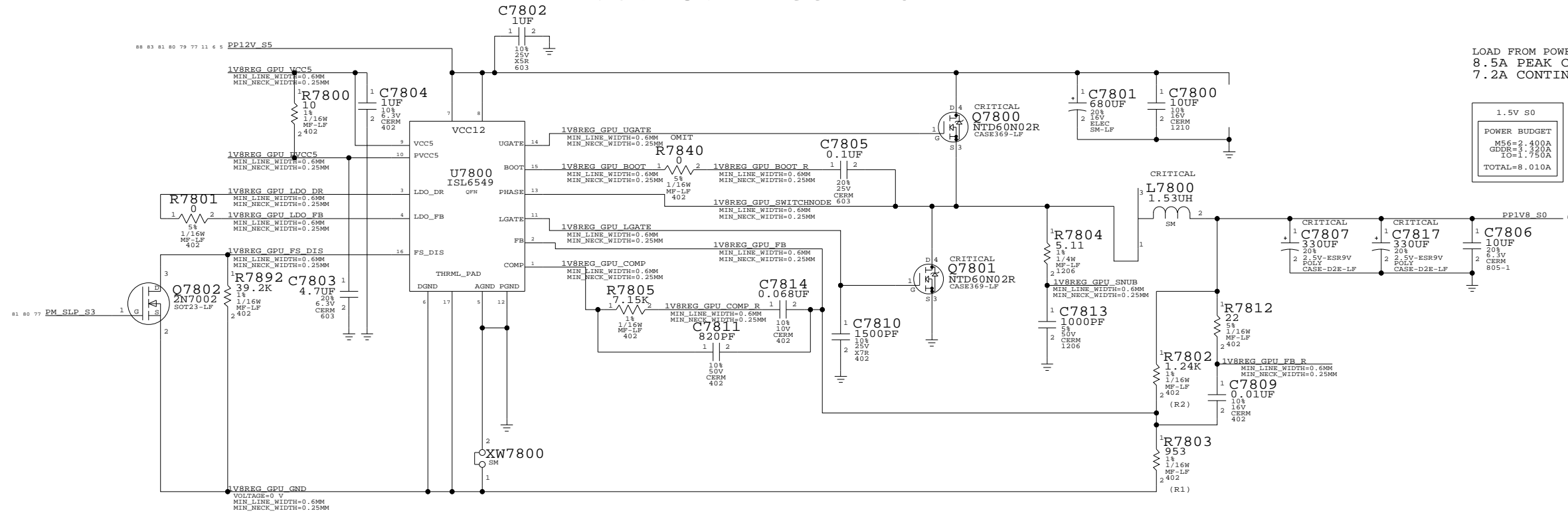
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	77	110	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480514	1	5.11 OHM 0402 1% 1/16W LF	R7840		

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0
POWER BUDGET
M56=2.400A
GDDR=3.320A
IO=1.750A
TOTAL=8.010A

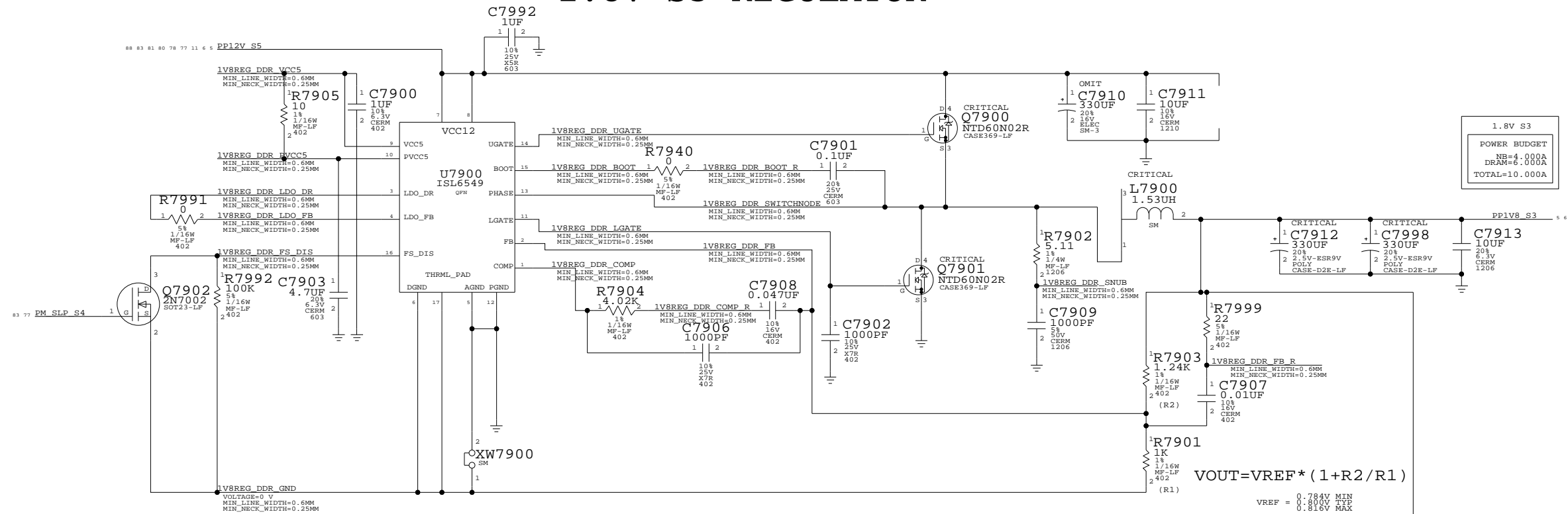
$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
VREF = 0.800V TYP
VREF = 0.816V MAX

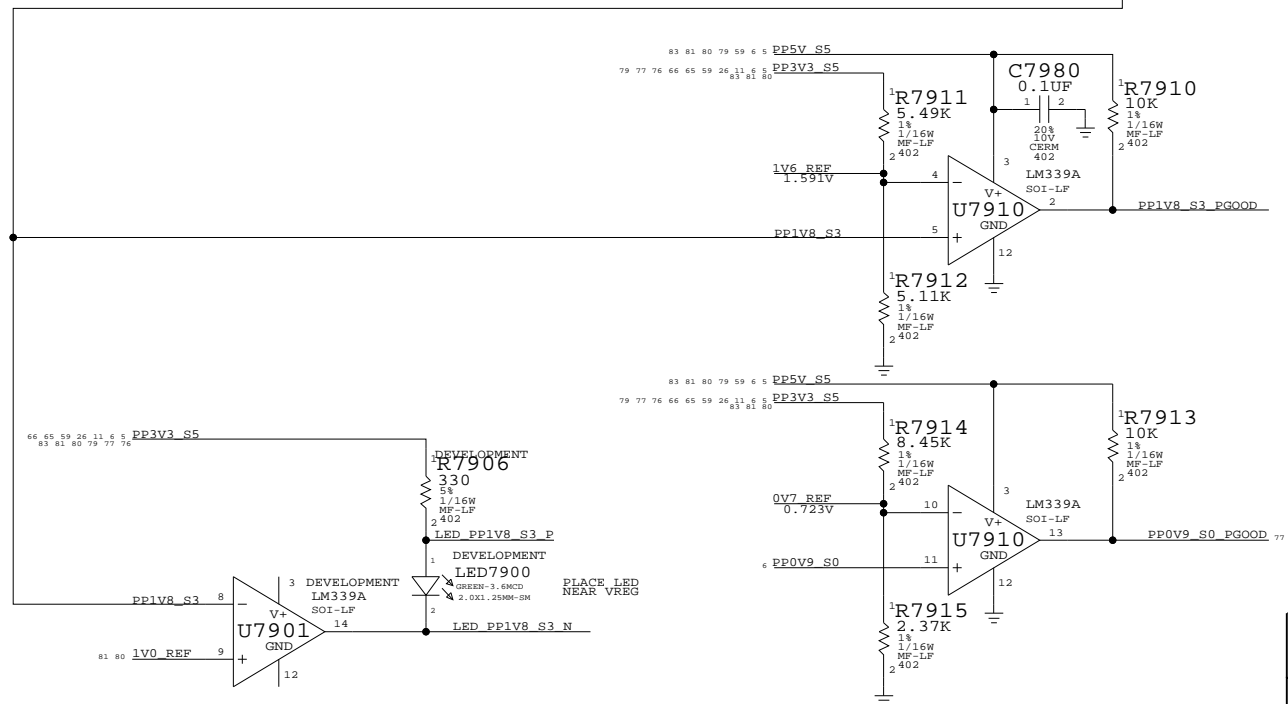
1.8V GDDR REGULATOR
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	REV.
NONE	78	110	

1.8V S3 REGULATOR



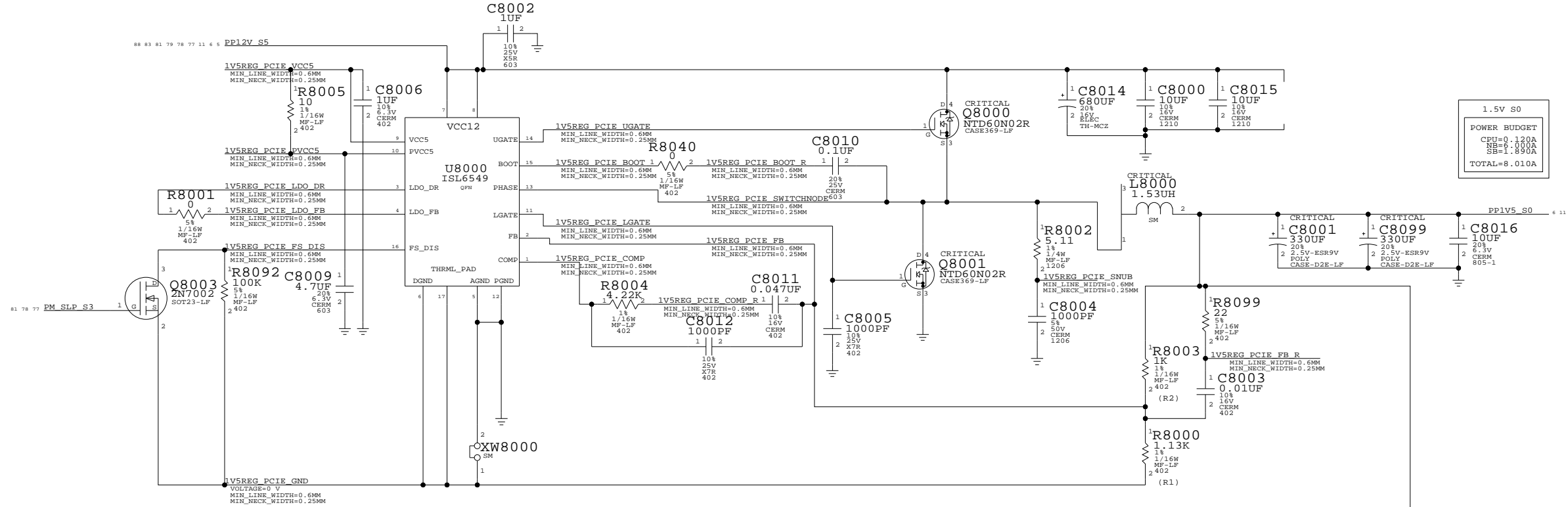
1.8V S3
POWER BUDGET
NB=4.000A
DRAM=5.000A
TOTAL=10.000A



1.8V Vreg
SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	79 OF	110
NONE			

1.5V S0 REGULATOR

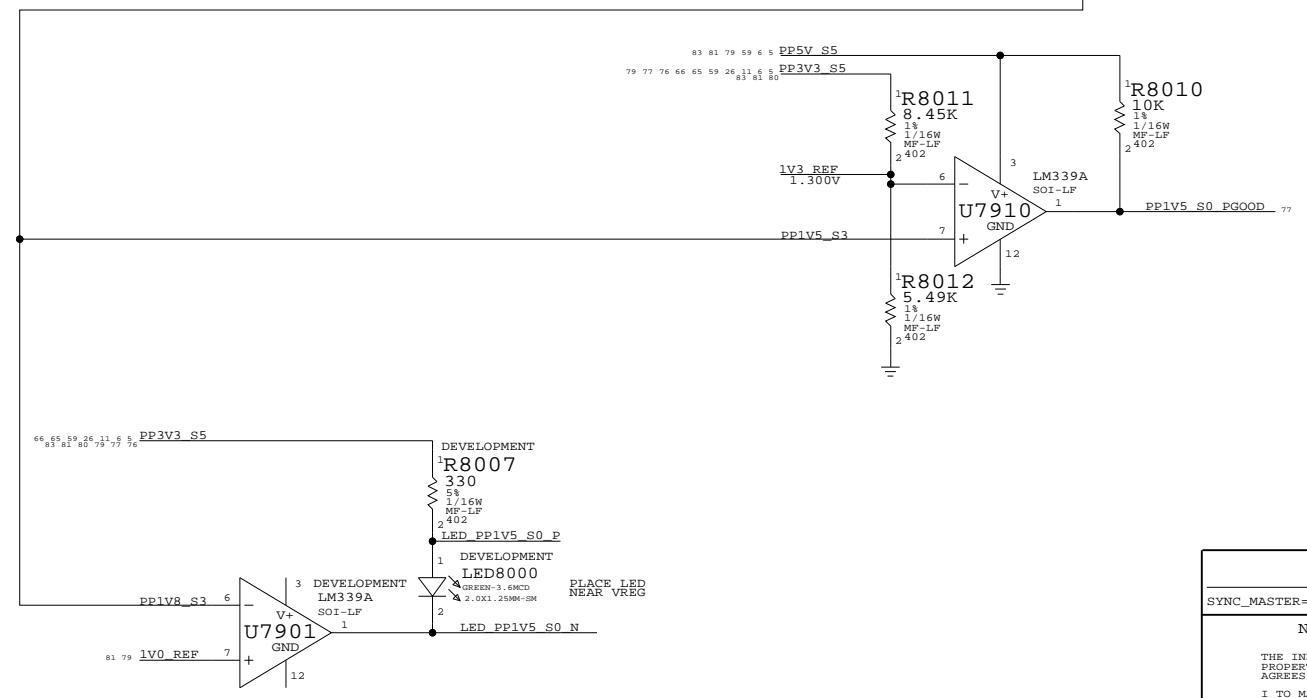


$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$V_{REF} = 0.800V \text{ TYP}$$

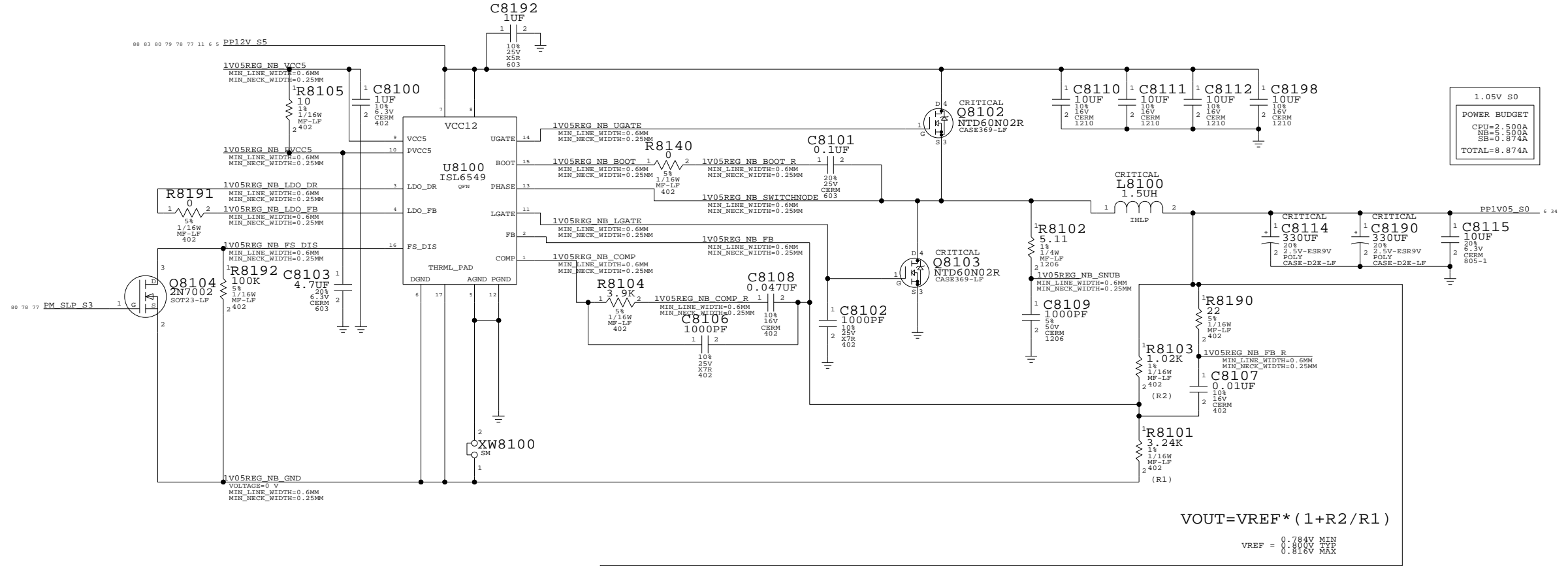
$$V_{REF} = 0.816V \text{ MAX}$$



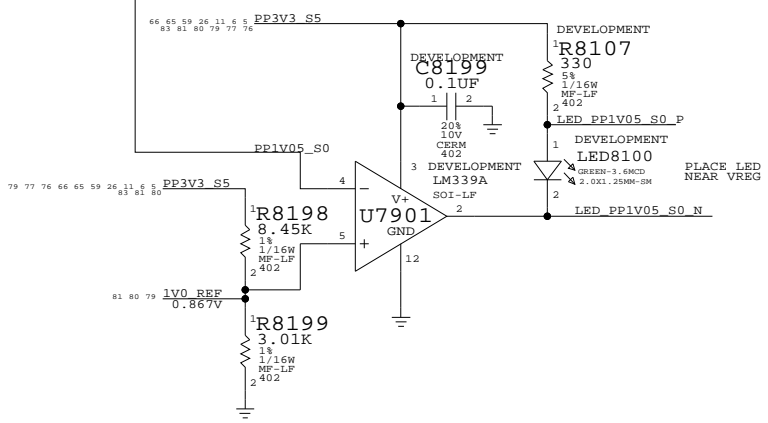
1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	80 OF	110
NONE			

1.05V S0 REGULATOR

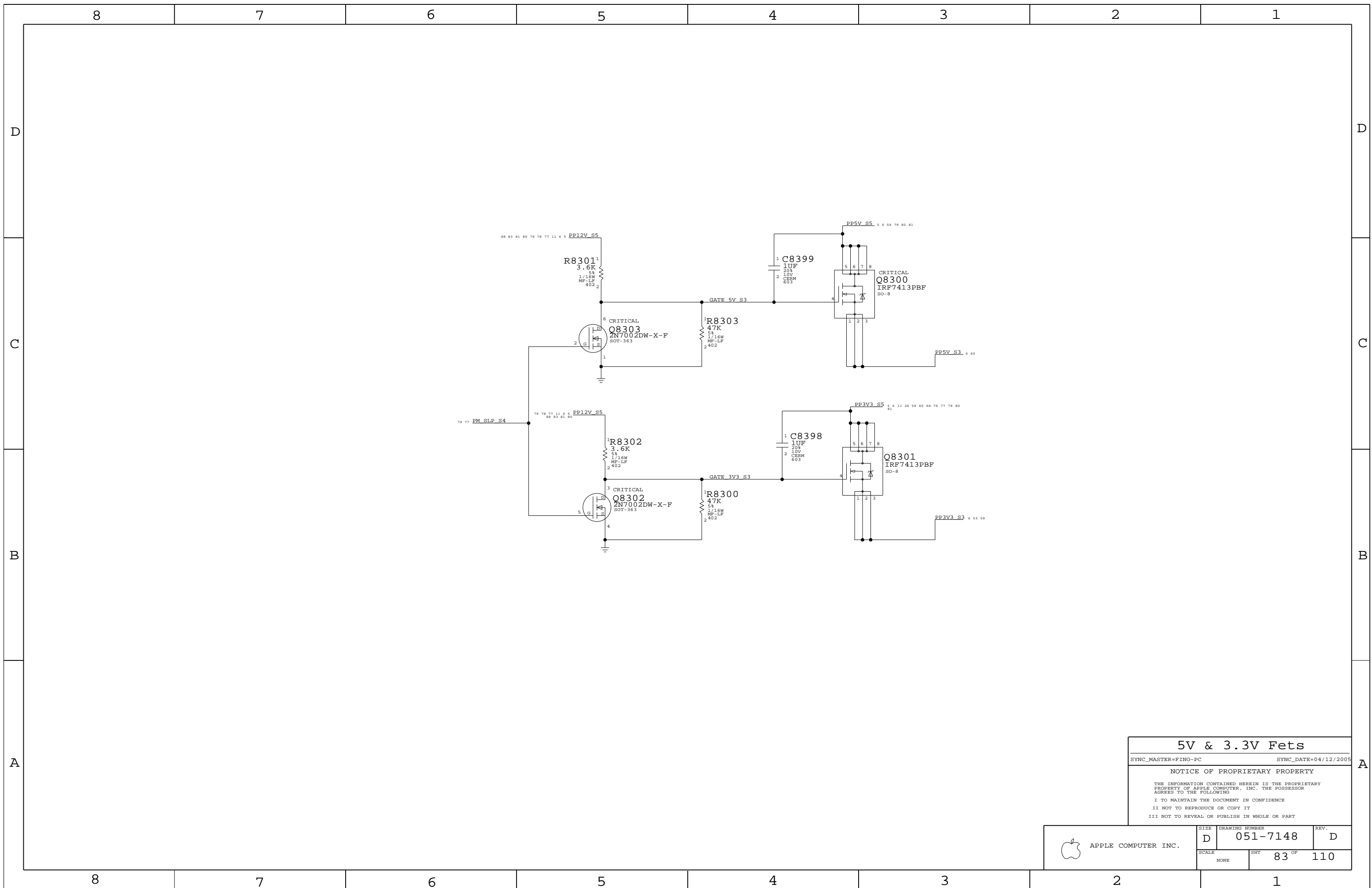


1.05V S0	
POWER BUDGET	
CPU=	2.500A
NB=	0.900A
SB=	0.874A
TOTAL=8.874A	



1.05V VREG	
SYNC_MASTER=M38-RT	SYNC_DATE=05/18/2005
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II NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	81 OF	110
NONE			




5V & 3.3V Fets

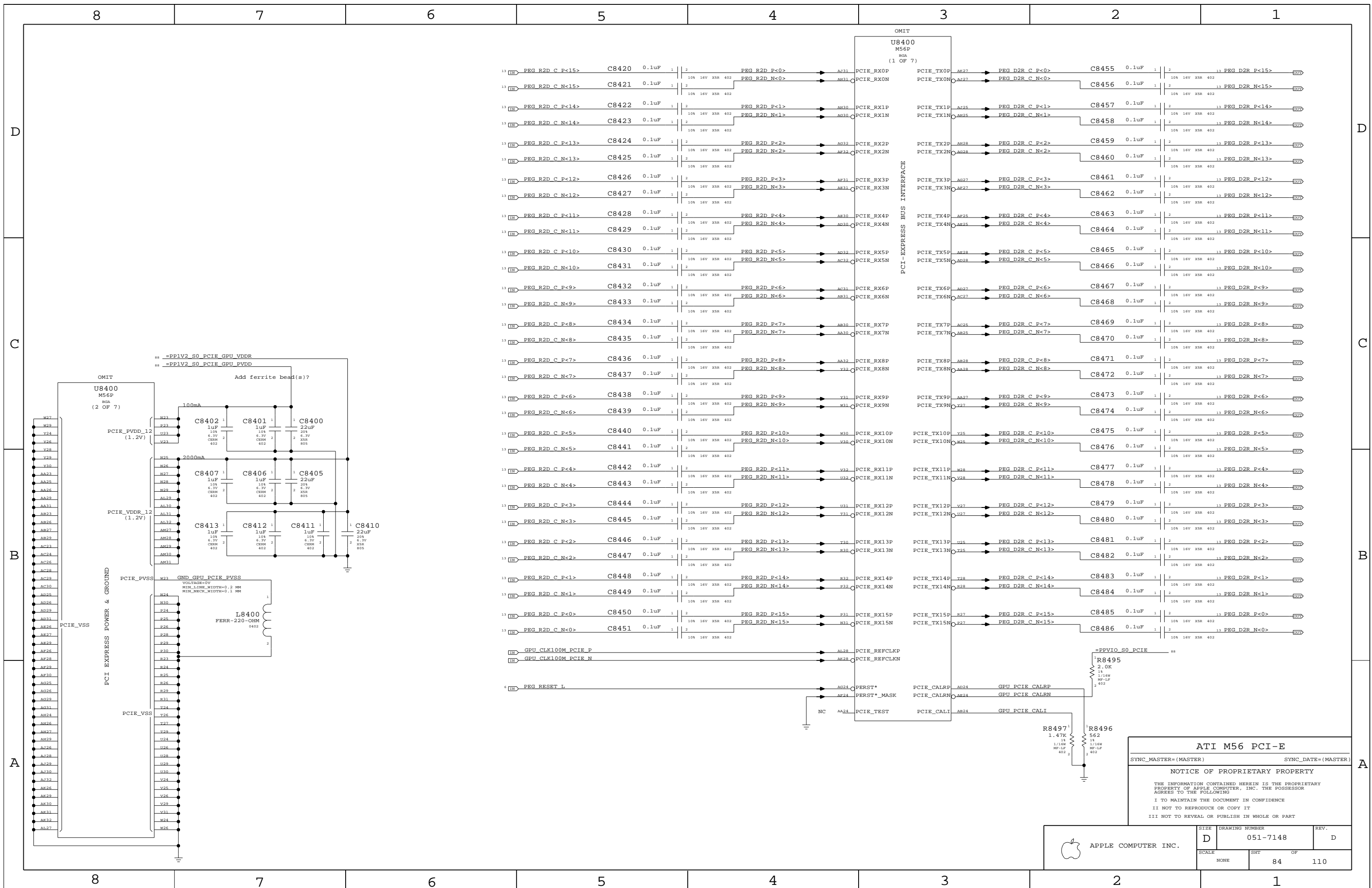
SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	83 OF 110	
NONE			



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

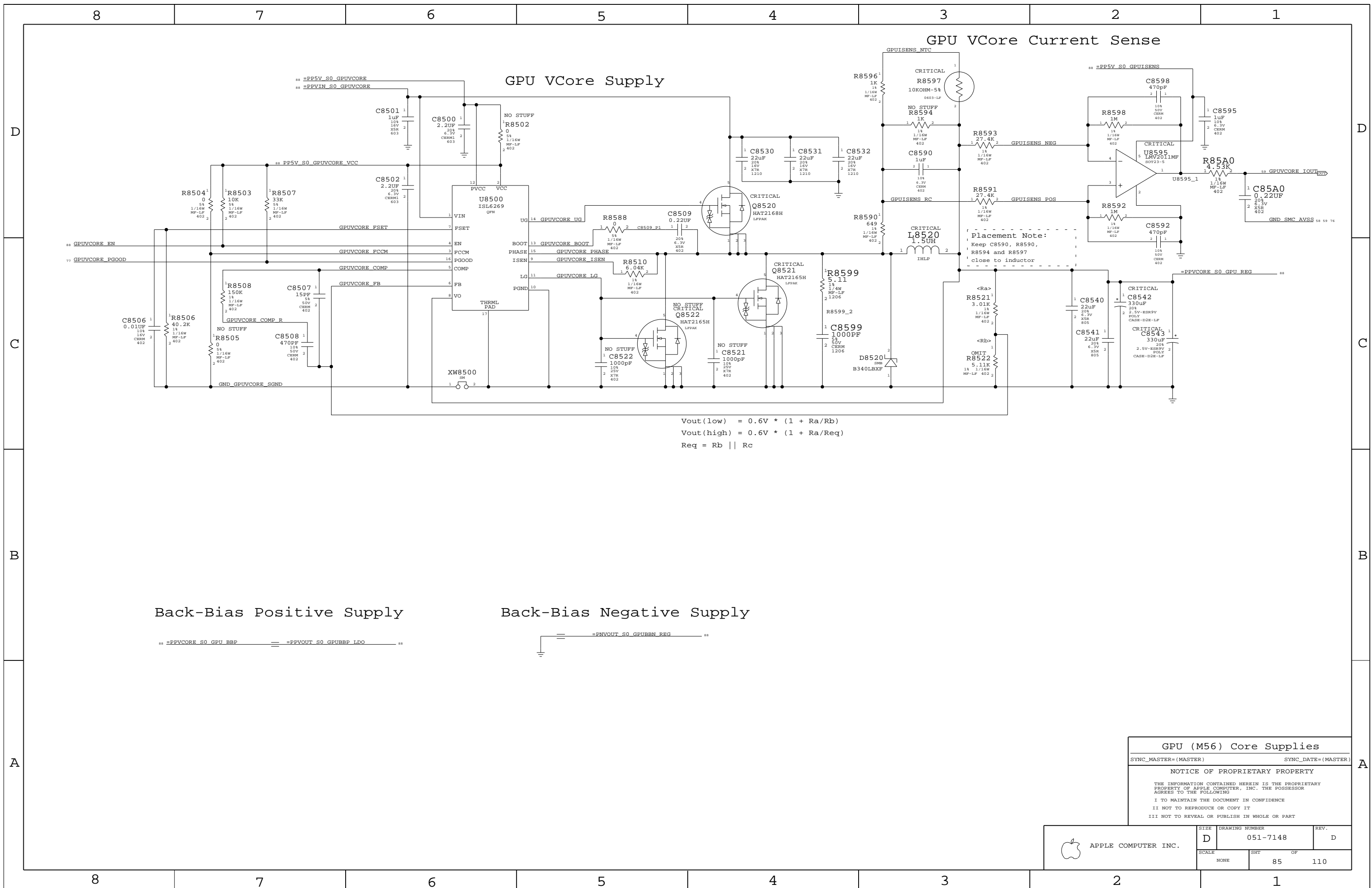
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	84	110	



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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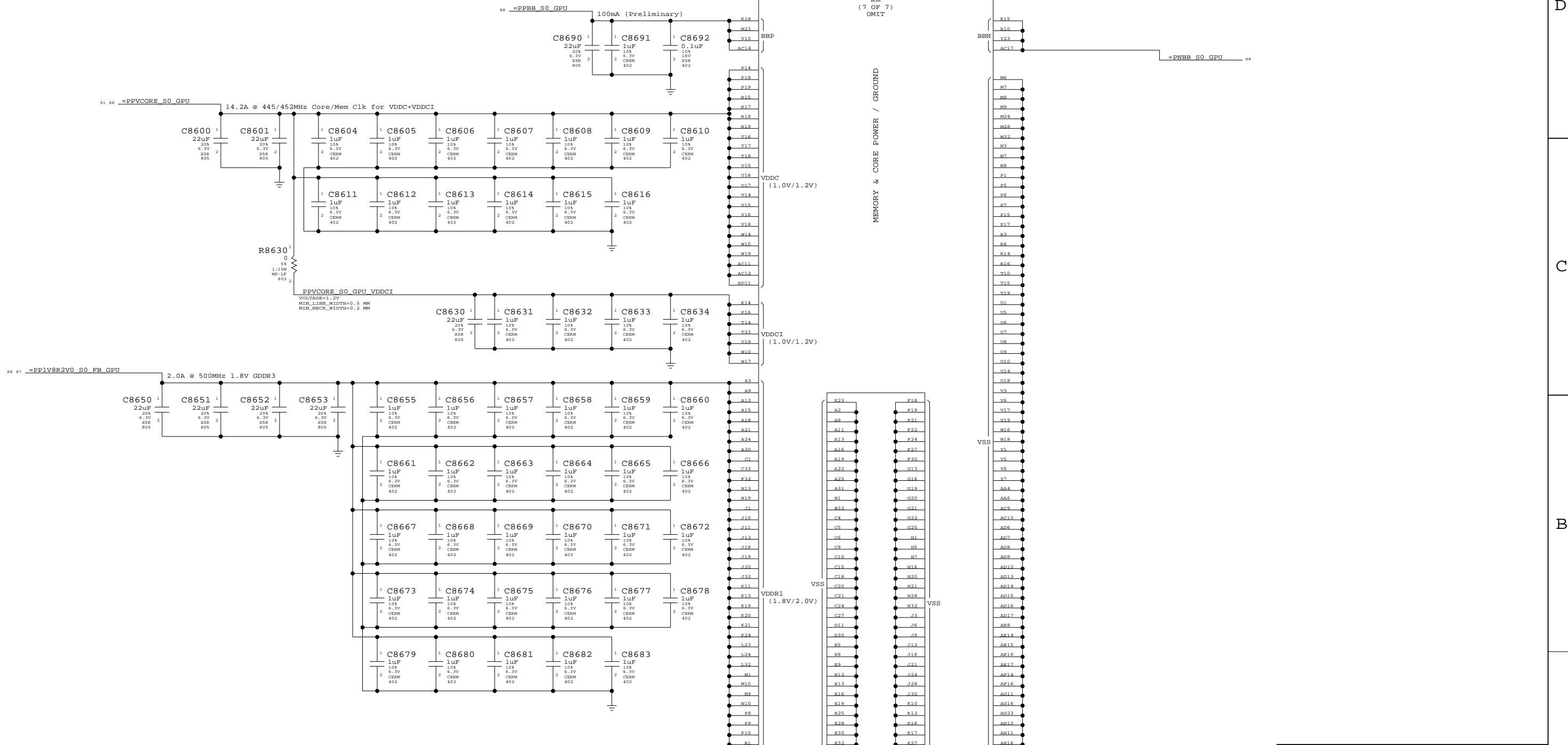
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	85	110	

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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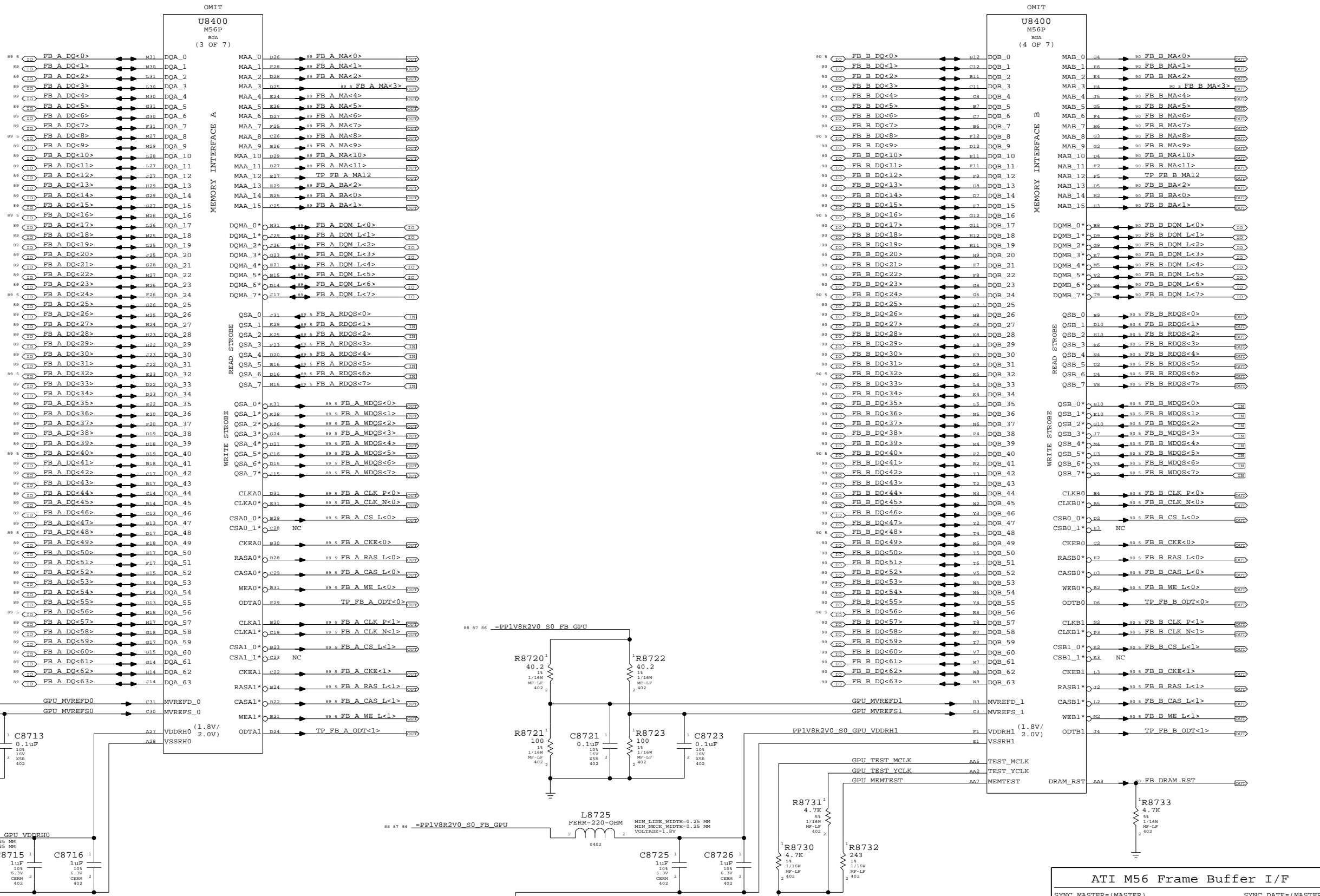
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	86	110	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Table with columns: SIZE (D), DRAWING NUMBER (051-7148), REV. (D), SCALE (NONE), SHEET (87 OF 110).



8

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"S0" GPU RAILS

ONLY ON IN RUN

59 EP1V0R1V2_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

85 PP5V_S0_GPUVCORE_VCC
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

PP1V2_GPU_IO_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PPBB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PPNB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.2MM
 VOLTAGE=0

76 61 59 41 26 11 10 6 PP3V3_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=3.3V

77 11 6 PP2V5_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=2.5V

PP1V8R2V0_S0_FB_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.8V

83 81 80 79 78 77 11 6 5 PP12V_S5
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=12V

6 PP12V_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=12V

97 76 6 PP5V_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

85 GPUVCORE_EN
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

97 FB_DRAM_RST
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

M56 GPIOs

94 91 GPU_GPIO_0
 10K 1/16W 2 R8813
 GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
 10K 1/16W 2 R8802
 GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
 NOSTUFF 2 R8803

91 GPU_GPIO_3
 NOSTUFF 2 R8804

91 GPU_GPIO_4
 NOSTUFF 2 R8805
 GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
 10K 1/16W 2 R8806

91 GPU_GPIO_6
 NOSTUFF 2 R8807

TP_GPU_GPIO_7
 MAKE_BASE=TRUE
 GPU_GPIO_7 91

91 GPU_GPIO_8
 NOSTUFF 2 R8808

NC_GPU_GPIO_10
 MAKE_BASE=TRUE
 GPU_GPIO_10 91

91 GPU_GPIO_9
 NOSTUFF 2 R8809

91 GPU_GPIO_13
 NOSTUFF 2 R8812

91 GPU_GPIO_12
 10K 1/16W 2 R8810
 ATI_FB_256M

91 GPU_GPIO_11
 NOSTUFF 2 R8811

GPIO 9,13,12,11 = ROM ID CFG
 INTERNAL PULL DOWN
 0010 = 256 M APERATURE SIZE

91 GPU_GPIO_24
 10K 1/16W 2 R8830
 ATI_FB_256M

91 GPU_GPIO_27
 10K 1/16W 2 R8831
 ATI_FB_HYNIX

91 GPU_GPIO_28
 10K 1/16W 2 R8832

91 GPU_GPIO_29
 TMD5_PANEL
 10K 1/16W 2 R8833

GPU_VCORE_LOW
 MAKE_BASE=TRUE
 GPU_GPIO_15 91
 10K 1/16W 2 R8850
 GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
 EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
 MAKE_BASE=TRUE
 GPU_GPIO_14 91

TP_GPU_GPIO_17
 MAKE_BASE=TRUE
 GPU_GPIO_17 91

TP_GPU_VGA_R
 MAKE_BASE=TRUE
 GPU_VGA_R 91

TP_GPU_VGA_G
 MAKE_BASE=TRUE
 GPU_VGA_G 91

TP_GPU_VGA_B
 MAKE_BASE=TRUE
 GPU_VGA_B 91

TP_GPU_VGA_HSYNC
 MAKE_BASE=TRUE
 GPU_VGA_HSYNC 91

TP_GPU_VGA_VSYNC
 MAKE_BASE=TRUE
 GPU_VGA_VSYNC 91

TP_GPU_TV_Y
 MAKE_BASE=TRUE
 GPU_TV_Y 91

TP_GPU_TV_COMP
 MAKE_BASE=TRUE
 GPU_TV_COMP 91

TP_GPU_TV_C
 MAKE_BASE=TRUE
 GPU_TV_C 91

TP_GPU_DDC_B_CLK
 MAKE_BASE=TRUE
 GPU_DDC_B_CLK 91

TP_GPU_DDC_B_DATA
 MAKE_BASE=TRUE
 GPU_DDC_B_DATA 91

GPU MISC

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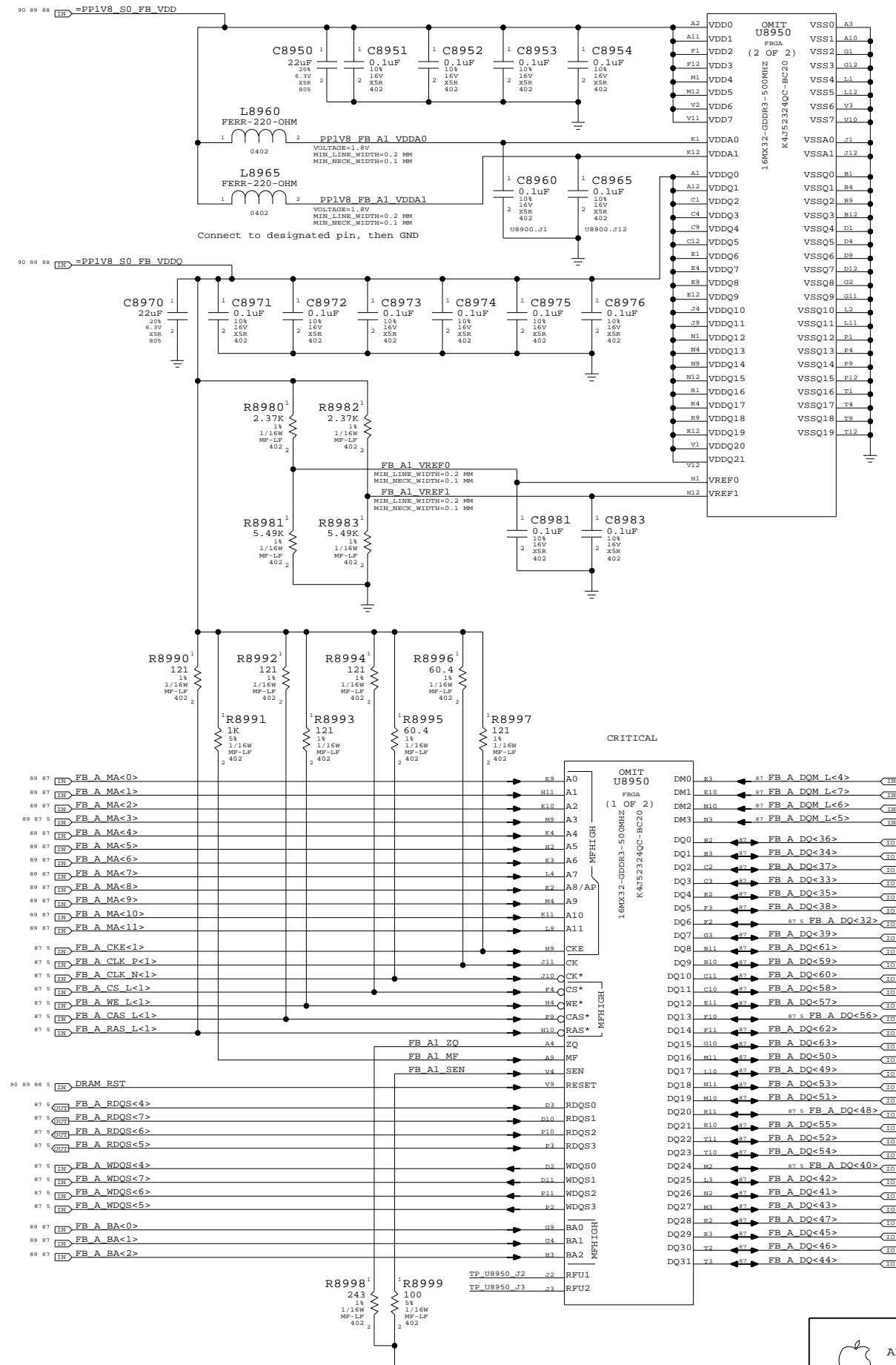
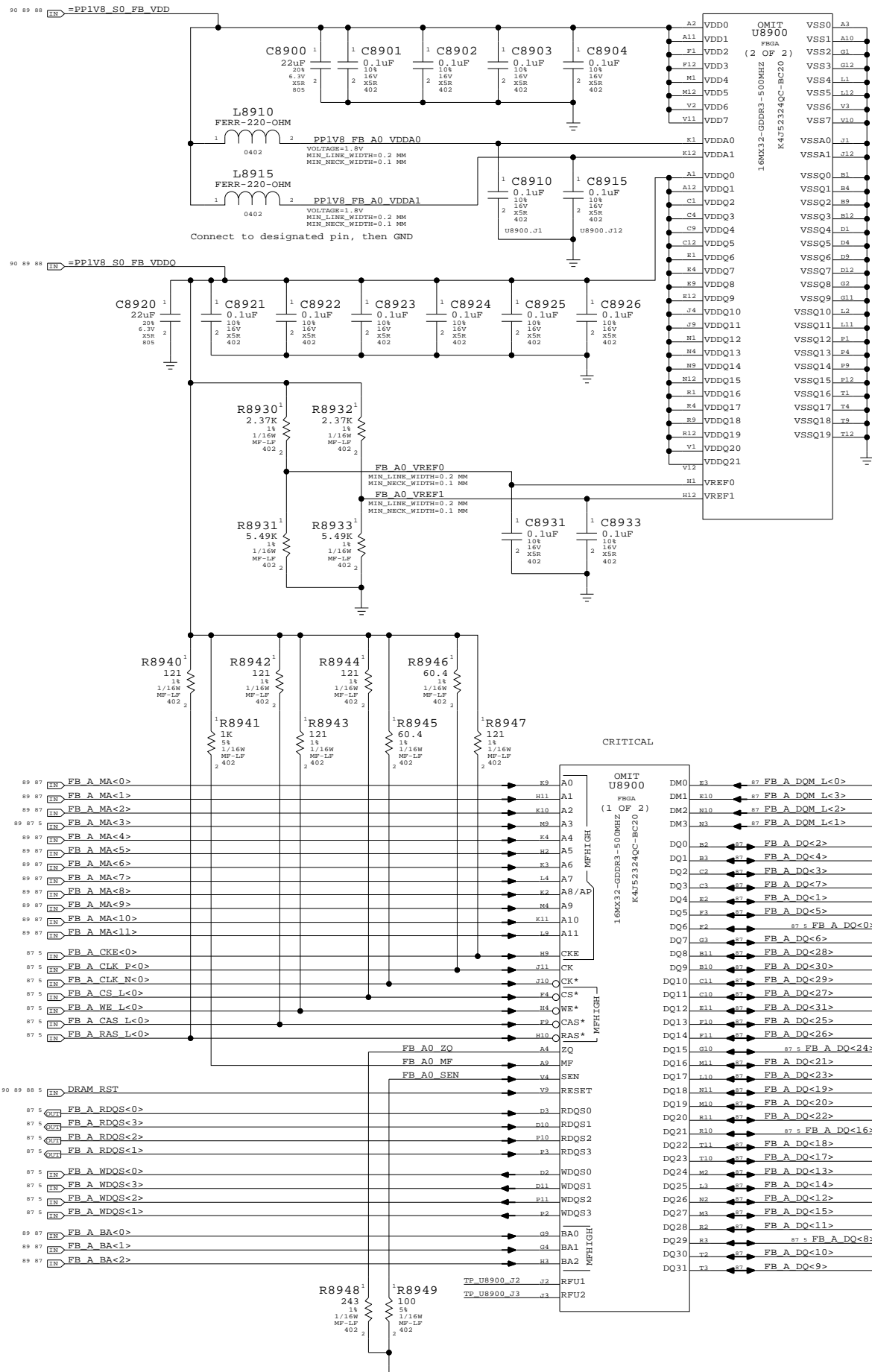
Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

CRITICAL

CRITICAL



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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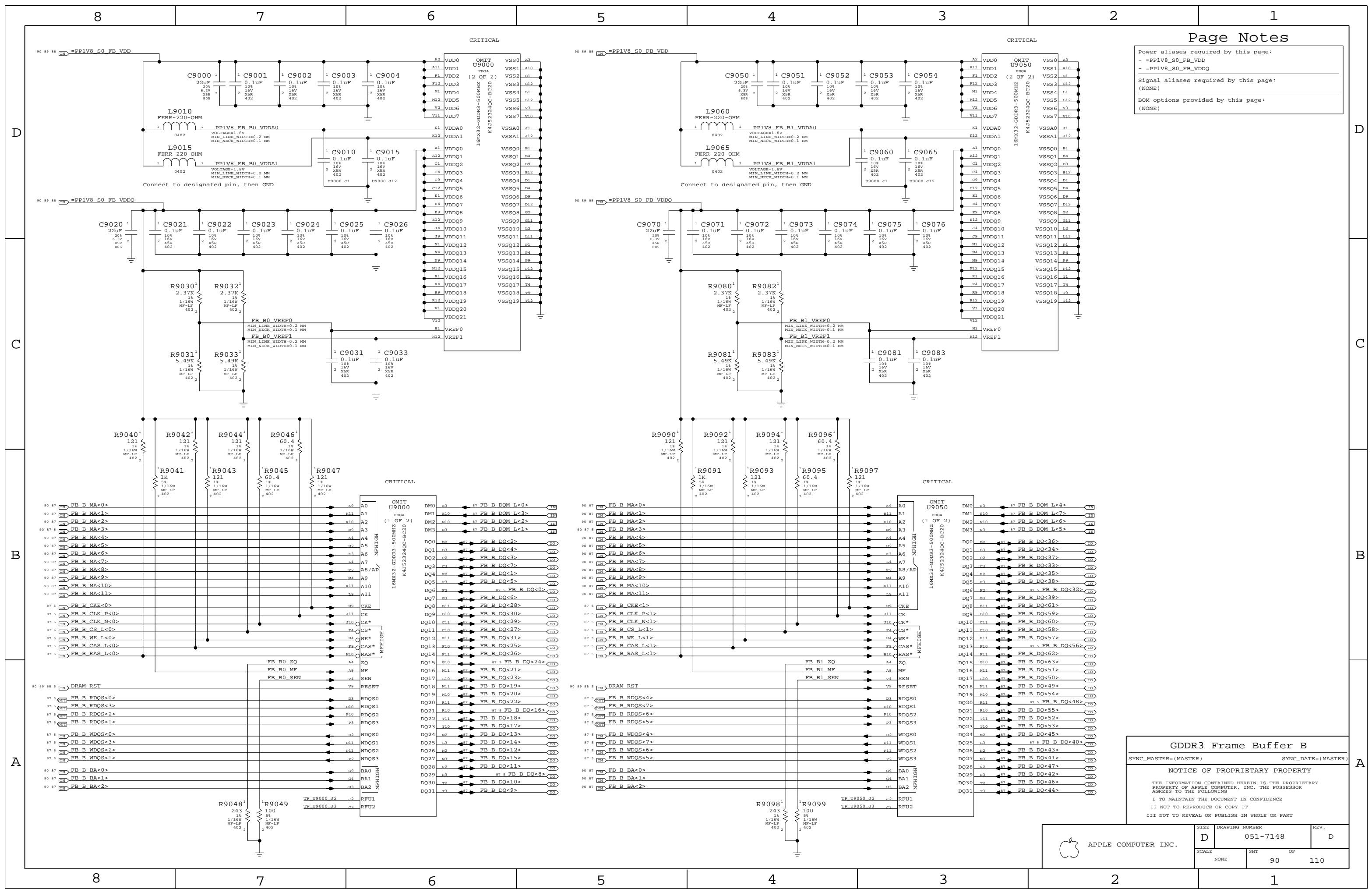
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Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Page Notes

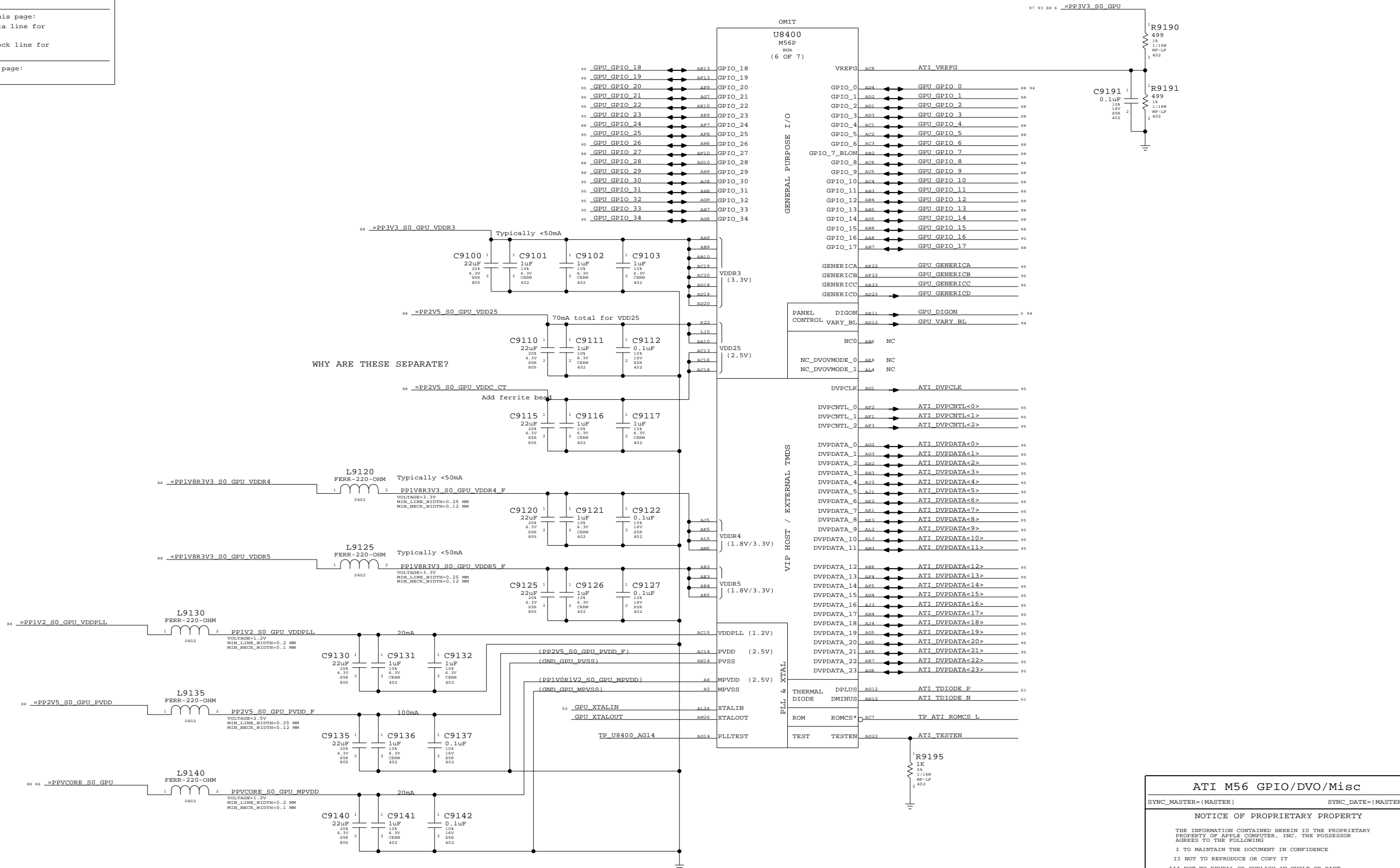
Power aliases required by this page:

- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	D
SCALE	SHT	OF	
NONE	91	110	

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Page Notes

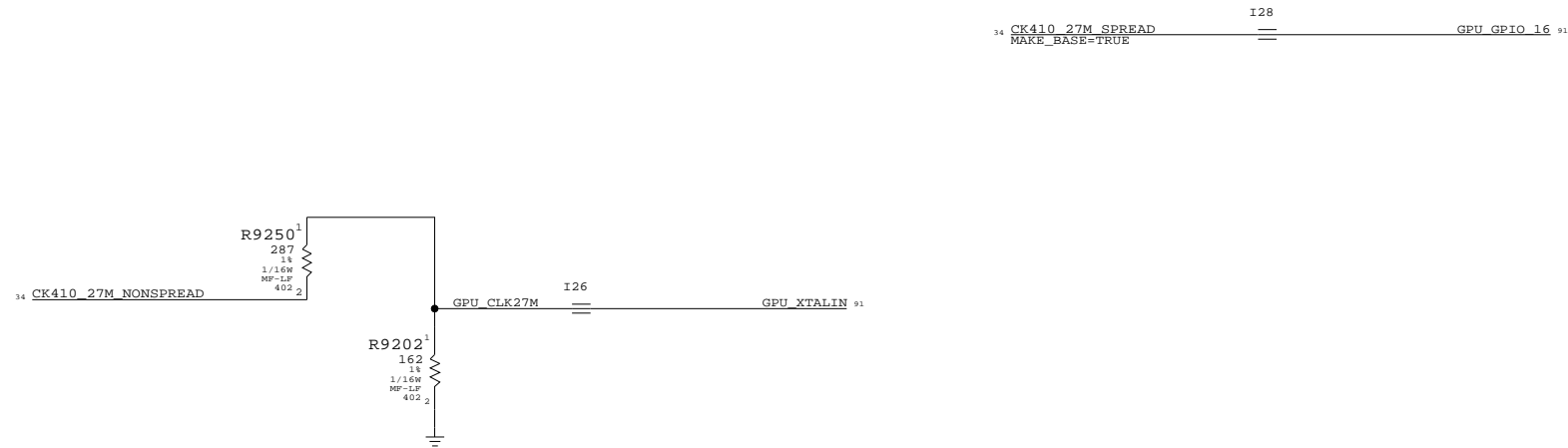
Power aliases required by this page:

- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8



GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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	SCALE	SHT	OF	REV.
	NONE	92	110	D

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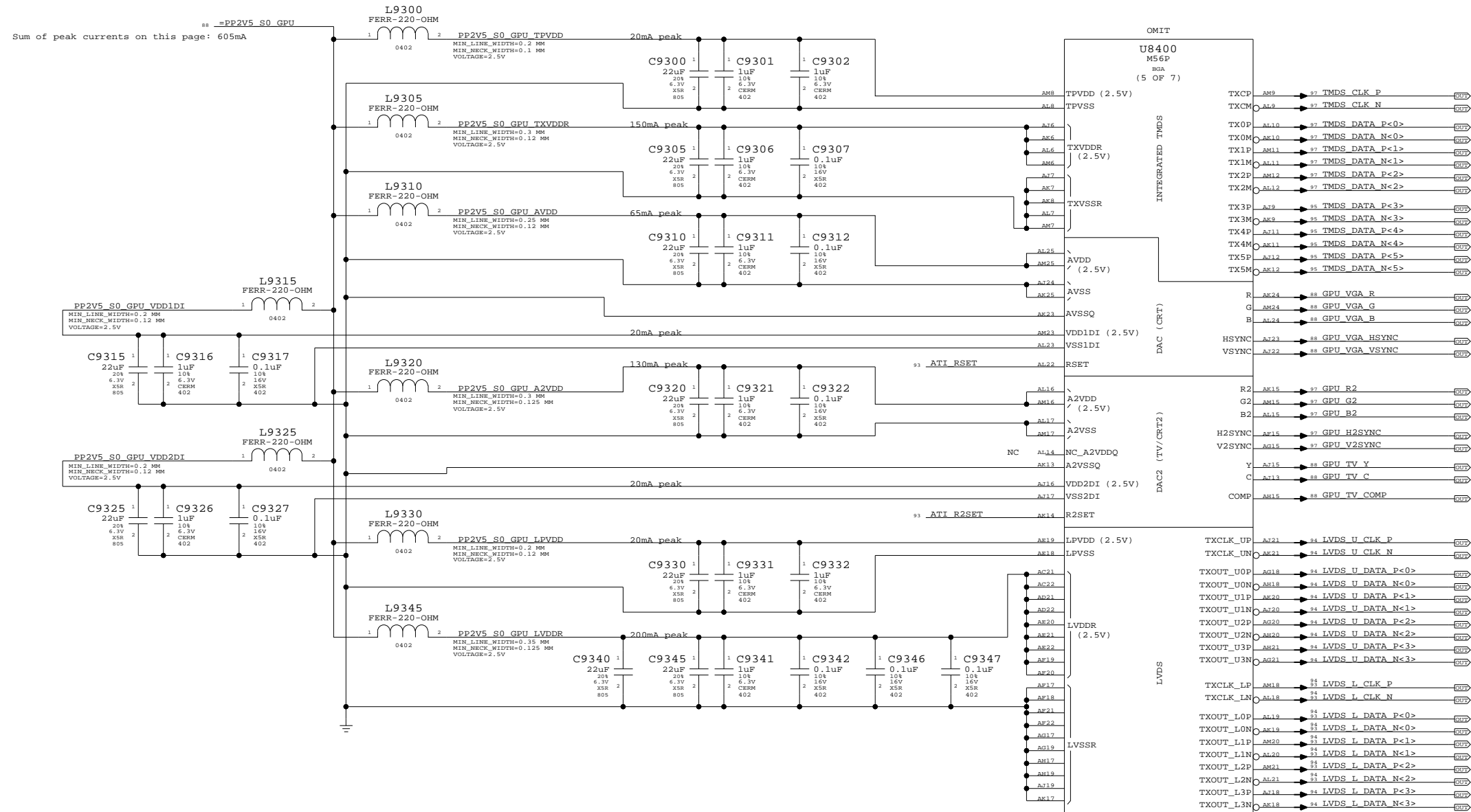
Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

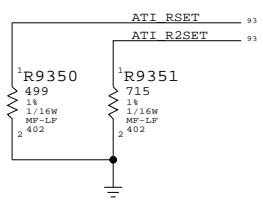
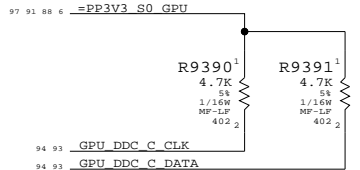
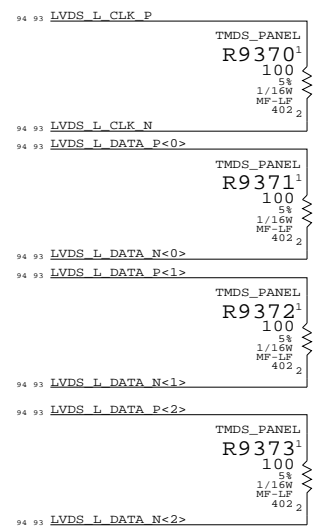
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

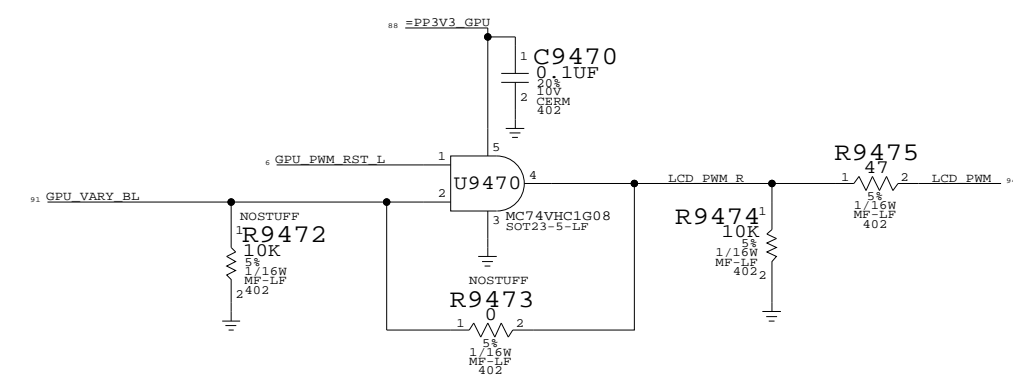
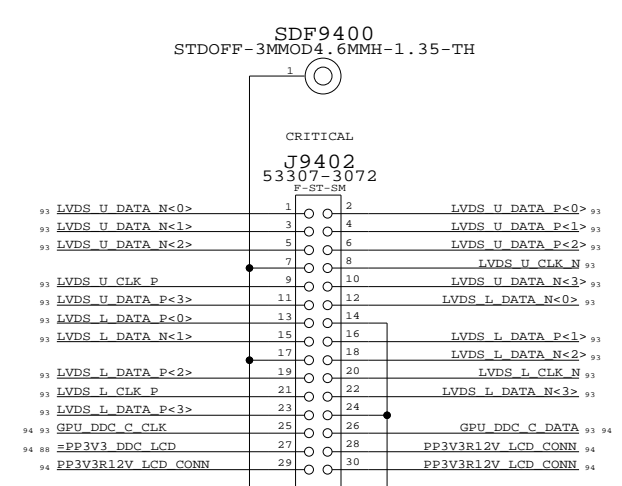
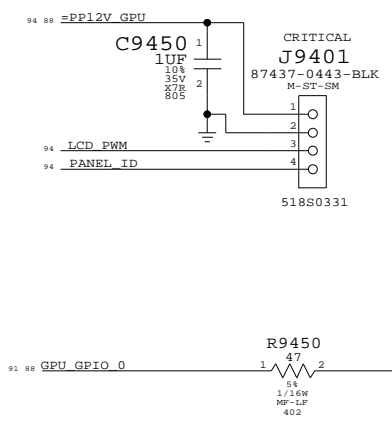
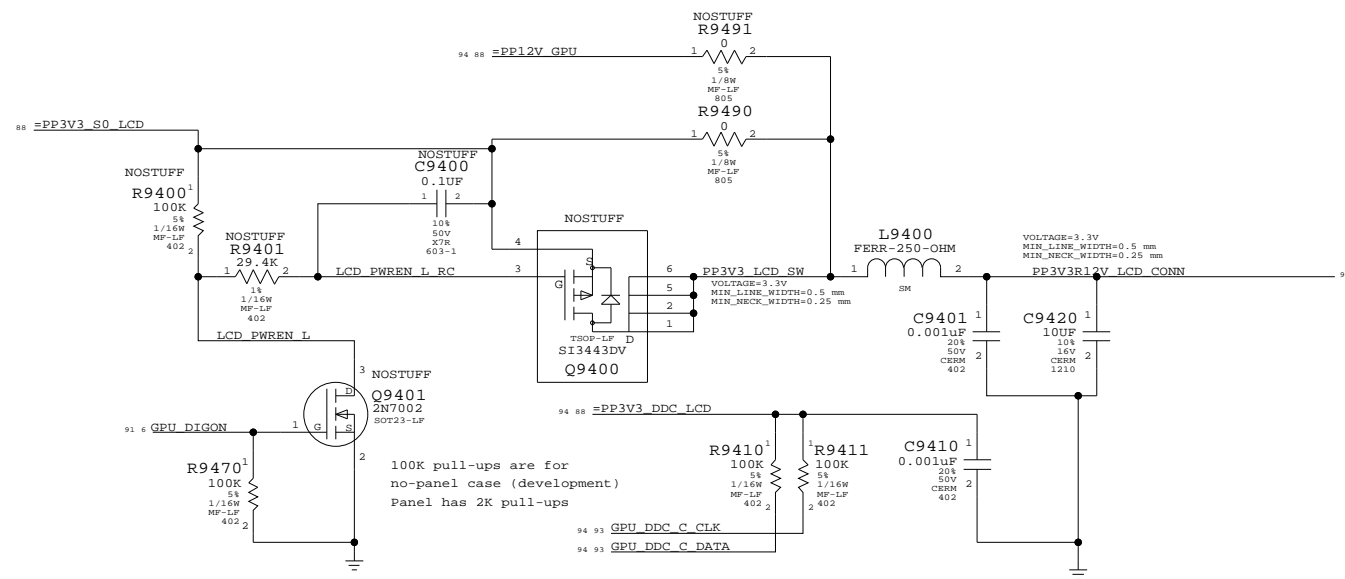
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	NONE	93	110	D

LCD (LVDS) INTERFACE

INVERTER INTERFACE



GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL

Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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	D	051-7148	D
SCALE	SHT	OF	
NONE	94	110	

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TP TMSD DATA P<3> == TMSD DATA P<3> 93
 MAKE_BASE=TRUE

TP TMSD DATA N<3> == TMSD DATA N<3> 93
 MAKE_BASE=TRUE

TP TMSD DATA P<4> == TMSD DATA P<4> 93
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TP TMSD DATA N<4> == TMSD DATA N<4> 93
 MAKE_BASE=TRUE

TP TMSD DATA P<5> == TMSD DATA P<5> 93
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TP ATI DVPDATA<22> == ATI DVPDATA<22> 91
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TP ATI DVPCNTL<2> == ATI DVPCNTL<2> 91
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TP GPU GPIO<34> == GPU_GPIO_34 91
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 MAKE_BASE=TRUE

TP GPU GPIO<32> == GPU_GPIO_32 91
 MAKE_BASE=TRUE

TP GPU GPIO<31> == GPU_GPIO_31 91
 MAKE_BASE=TRUE

TP GPU GPIO<30> == GPU_GPIO_30 91
 MAKE_BASE=TRUE
 NO_TEST=TRUE

TP GPU GPIO<26> == GPU_GPIO_26 91
 MAKE_BASE=TRUE

TP GPU GPIO<25> == GPU_GPIO_25 91
 MAKE_BASE=TRUE

TP GPU GPIO<23> == GPU_GPIO_23 91
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 MAKE_BASE=TRUE

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 MAKE_BASE=TRUE

TP GPU GPIO<20> == GPU_GPIO_20 91
 MAKE_BASE=TRUE

TP GPU GPIO<19> == GPU_GPIO_19 91
 MAKE_BASE=TRUE

TP GPU GPIO<18> == GPU_GPIO_18 91
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TP GPU GENERIC A == GPU_GENERIC A 91
 MAKE_BASE=TRUE

TP GPU GENERIC B == GPU_GENERIC B 91
 MAKE_BASE=TRUE

TP GPU GENERIC C == GPU_GENERIC C 91
 MAKE_BASE=TRUE

M56 TPS

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SCALE	SHT	OF
NONE	95	110

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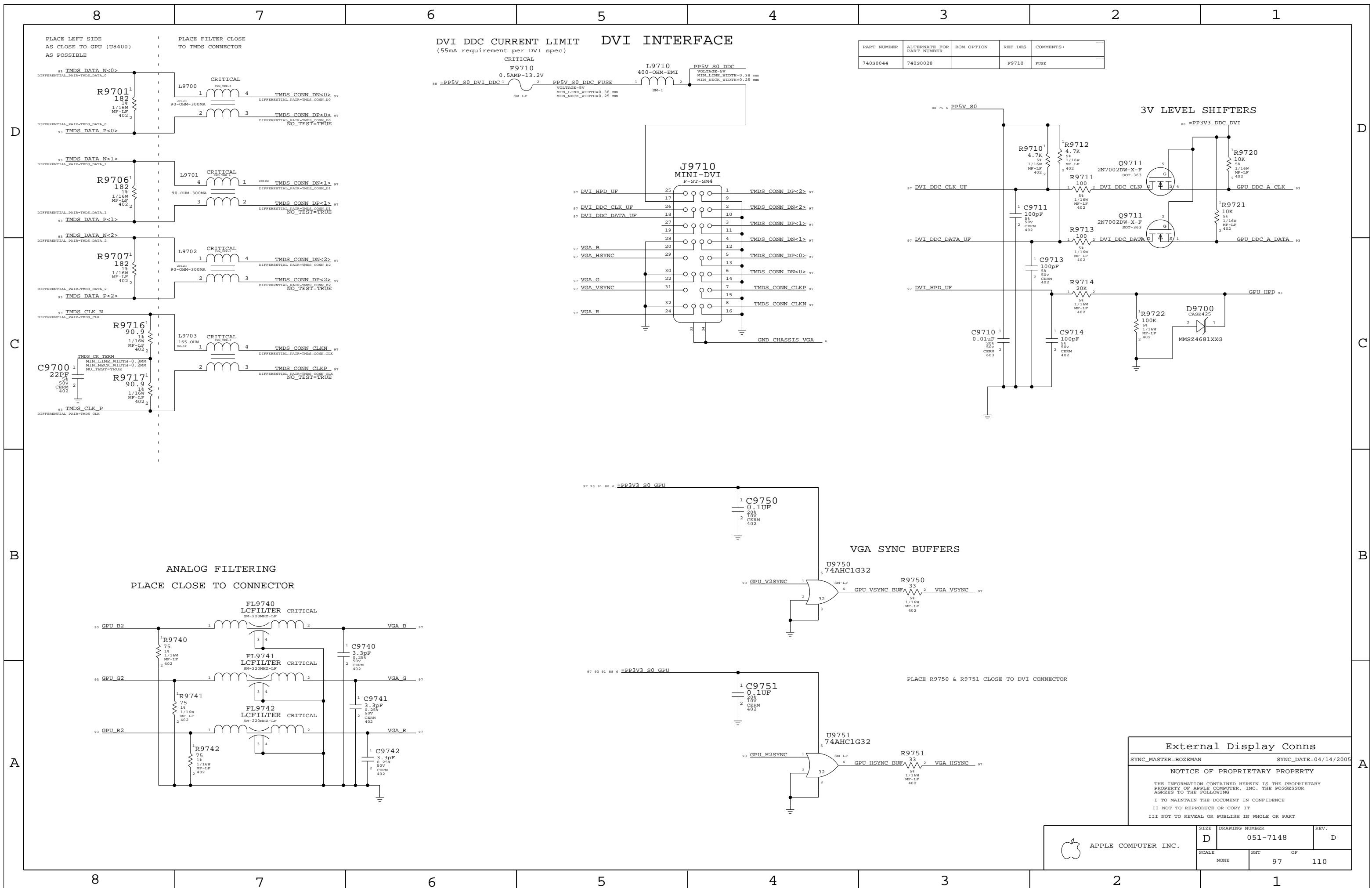
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
740S0044	740S0028		F9710	FUSE

DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

CRITICAL

F9710

0.5AMP-13.2V

L9710

400-OHM-EMI

PP5V S0 DDC

VOLTAGE=5V

MIN_LINE_WIDTH=0.38 mm

MIN_NECK_WIDTH=0.25 mm

PP5V S0 DDC FUSE

VOLTAGE=5V

MIN_LINE_WIDTH=0.38 mm

MIN_NECK_WIDTH=0.25 mm

J9710

MINI-DVI

F-ST-SM4

3V LEVEL SHIFTERS

PP3V3 DDC DVI

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

VGA SYNC BUFFERS

External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

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	D	051-7148	D
SCALE	SHT	OF	
NONE	97	110	

Table with 10 columns (labeled 1-10) and multiple rows. The table contains technical data including component names, addresses, and values. The columns are numbered 1 to 10 from right to left. The rows are grouped into sections A, B, C, and D.

Table with 10 columns (labeled 1-10) and multiple rows of data. Each row contains identifiers, addresses, and values. The table is organized into sections A, B, C, and D on both sides.

