

8

7

6

5

4

3

2

1

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# LINK

02/23/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
03		316008	ENGINEERING RELEASED	DATE	DATE
				02/23/04	?

## EVT1 BOM Option Table

630-4843  
630-4902  
PCBA, LINK, Q51

BOM Options	STUFF	NO STUFF
DEVELOPMENT	✓	
GPU_SS	✓	
MPIC_NB		✓
MPIC_SB	✓	
PATA_3V3_LOGIC		✓
PATA_5V_LOGIC	✓	
PCI_64BIT		✓
SMU_CPU_I2C	✓	
SMU_CPU_JTAG		✓
THERM_1	✓	
THERM_1B		✓
THERM_2	✓	
THERM_2B		✓
THERM_3	✓	
THERM_3B		✓
VESTA1V2_BURST		✓
VESTA1V2_PULSE		✓
VESTA_DS_ONLY_EN0	✓	
VESTA_PWR_CLASS_0		✓
AGP_BUSYSSTOP		✓
NO_SMU_I2C_D		✓
EI_3TO1	✓	
CPU_PLL_MEDIUM	✓	
CPU_AVDD_2V8	✓	
SB_HT_200M		✓
M11CSP64	630-4843	
M11CSP128	630-4902	
INT_TMDS	✓	
EXT_TMDS		✓

Module	Page	Contents	Sync
TOP	1	Table of Contents	N/A
	2	System Block Diagram	N/A
	3	Power Block Diagram	N/A
	4	Revision Notes	N/A
	5	Power & Signal Aliases	(Link)
	6	Functional Test Properties	N/A
	7	System Power Connectors	(Nimitz)
	8	Battery Charger	(Link)
	9	1.8V / 1.5V/ 1.2V Regulators	(Link)
	10	3.3V / 5V Regulators	(Link)
	11	2.5V / NB Vcore / PMU Regulators	(Link)
	12	Vesta Power / Misc	(Fizzy)
	13	System Management Unit (SMU)	(smu_real)
	14	Power Sequencing Connections	(Link)
	15	Thermal Sensor / Fans	(Link)
	16	Misc Internal Connectors	(Nimitz)
	17	Q51 Specific design/Connectors	N/A
	18	I2C Connections	(Gila)
	19	LMU Support	(Nimitz)
	20	U3Lite Core	(Gila)
	21	Shasta Core	(Fizzy)
	22	U3Lite Misc	Gila
	23	Shasta Misc	(Fizzy)
	24	Pulsar Core	Gila
	25	Pulsar Clocks	Gila
Processor Interface	26	U3Lite Processor Interface	U3Lite
	27	PPC970 Processor Interface	Gila
	28	PPC970 Pull-ups / Pull-downs	Gila
	29	PPC970 Core	Gila
	30	PPC970 Bypassing	Gila
	31	CPU VCore Regulator	(Link)
	32	CPU Temperature Monitoring	(Gila)
Main Memory	33	U3Lite Memory Interface	U3Lite
	34	Memory Series Termination	(Nimitz)
	35	SO-DIMM Connectors	(Nimitz)

Module	Page	Contents	Sync	
Graphics	36	U3Lite AGP Interface	Gila	
	37	M10-CSP64 AGP Interface	(Nimitz)	
	38	GPU VCore Regulator	(Link)	
	39	M10-CSP64 Core	(Nimitz)	
	40	M10-CSP64 Misc Power	(Nimitz)	
	41	TMDS Terminations	(Nimitz)	
	42	Video Connectors	(Nimitz)	
Hyper-Transport	43	U3Lite HyperTransport Interface	U3Lite	
	44	Shasta HyperTransport Interface	Fizzy	
PCI	45	South Bridge PCI Interface	(Fizzy)	
	46	BootROM	Fizzy	
	47	AirPort Extreme Connector	(Fizzy/Nimitz)	
	48	USB2 Controller PCI Interface	Fizzy	
	49	CardBus Controller & Connector	Fizzy	
	Disk	50	South Bridge Disk Interfaces	(Fizzy)
		51	Serial ATA to Parallel ATA Bridge	(Fizzy)
52		UATA/PATA Connectors	(Fizzy)	
Ethernet	53	South Bridge Ethernet	(Fizzy)	
	54	Vesta Ethernet	(Fizzy)	
FireWire	55	Ethernet Magnetics & Connector	(Fizzy/Nimitz)	
	56	South Bridge Firewire	(Fizzy)	
USB Modem	57	Vesta FireWire	(Fizzy)	
	58	FireWire Ports	(Fizzy/Nimitz)	
Audio	59	USB Interfaces	Fizzy	
	60	Modem Interface	(Fizzy)	
CRef	61	Audio Interface	(Fizzy)	
	62	End of Modules Placeholder	(Fizzy)	
	63	Signal Cross Reference (1 of 2)	N/A	
	64	Signal Cross Reference (2 of 2)	N/A	
	65	Component Cross Reference (1 of 2)	N/A	
	66	Component Cross Reference (2 of 2)	N/A	

### Module Components

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2835	1	IC, PPC970, 1.8GHz, 1.1V, 80C, 25W	576CBGA U2900	CRITICAL	
343S0284	1	IC, U3LITE, V1.1, 300MM, PBGA	U3	CRITICAL	
343S0283	1	IC, ASIC, SHASTA, V1.1, 484BALL, PBGA	U2300	CRITICAL	
338S0154	1	IC, ATI, M11-CSP64, NO HEATSPREADER	U4900	CRITICAL	M11CSP64
338S0158	1	IC, ATI, M11-CSP128, NO HEATSPREADER	U4900	CRITICAL	M11CSP128
343S0288	1	IC, ASIC, VESTA, V1.1	U8600	CRITICAL	
341S1340	1	BOOTROM, PROTO, Q51	U7500	CRITICAL	
341S1394	1	SMU, PROTO, Q51	U1300	CRITICAL	

### Alternates Components

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L, V1.1, 200MM, PBGA

### Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6532	1	SCHEM, LINK, Q51	SCH1	
820-1573	1	PCBF, LINK, Q51	PCB1	

DIMENSIONS ARE IN MILLIMETERS

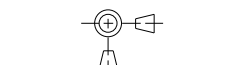
XX : \_\_\_\_\_

X.XX : \_\_\_\_\_

X.XXX : \_\_\_\_\_

ANGLES : \_\_\_\_\_

DO NOT SCALE DRAWING



THIRD ANGLE PROJECTION

### METRIC

DRAWER	DESIGN CK	ENG APPD	MFG APPD	QA APPD	DESIGNER	RELEASE	SCALE	NONE	MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D
--------	-----------	----------	----------	---------	----------	---------	-------	------	-------------------------------------	--------

Apple Computer Inc.

NOTICE OF PROPRIETARY PROPERTY  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II. NOT TO REPRODUCE OR COPY IT  
III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

### SCHEM, LINK, Q51

DRAWING NUMBER 051-6532 REV. 03  
SHEET 1 OF 103

DRAWING  
TITLE=LINK  
ABBREV=DRAWING  
LAST\_MODIFIED=Mon Feb 23 18:35:53 2004

8

7

6

5

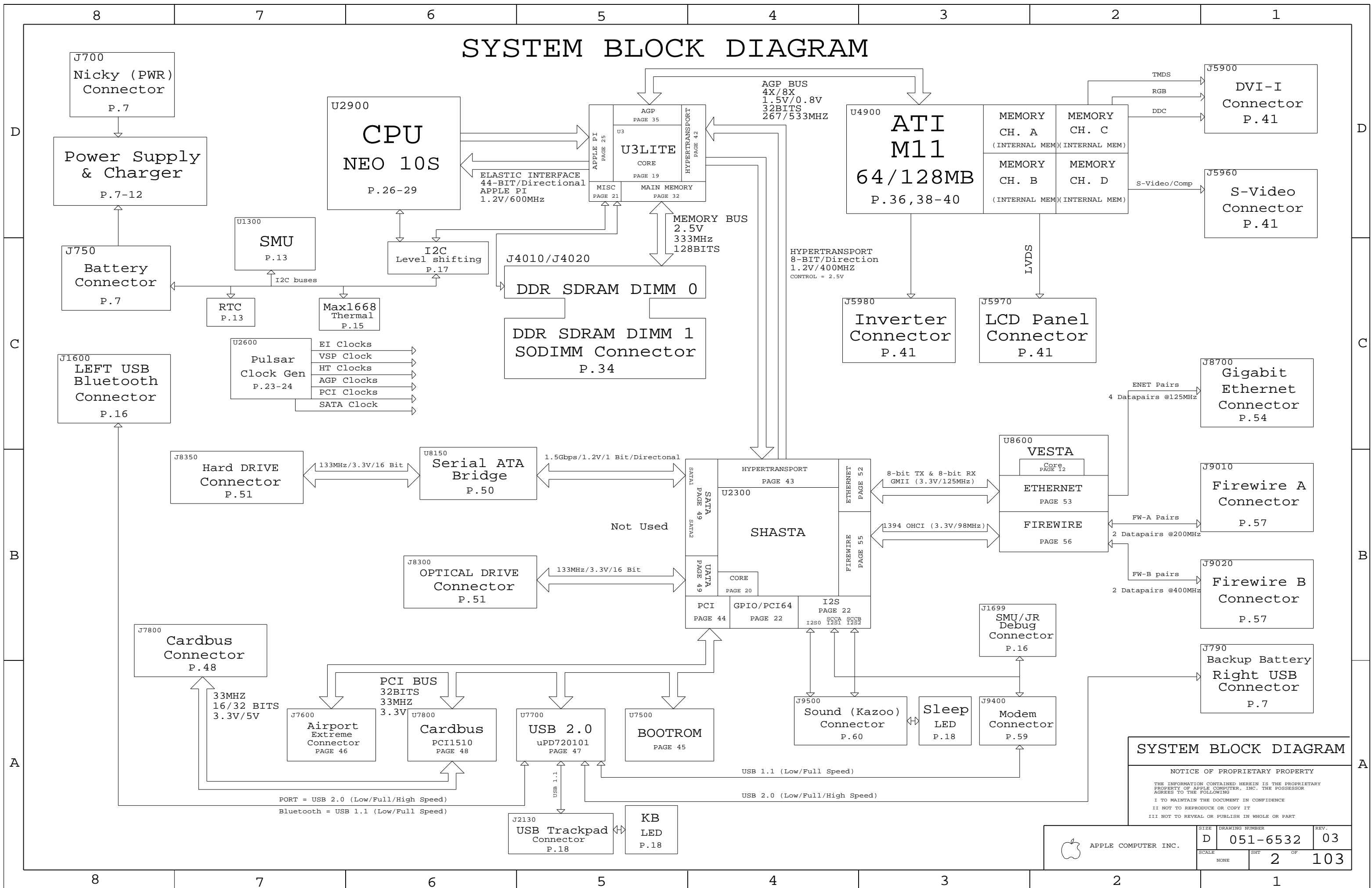
4

3

2

1

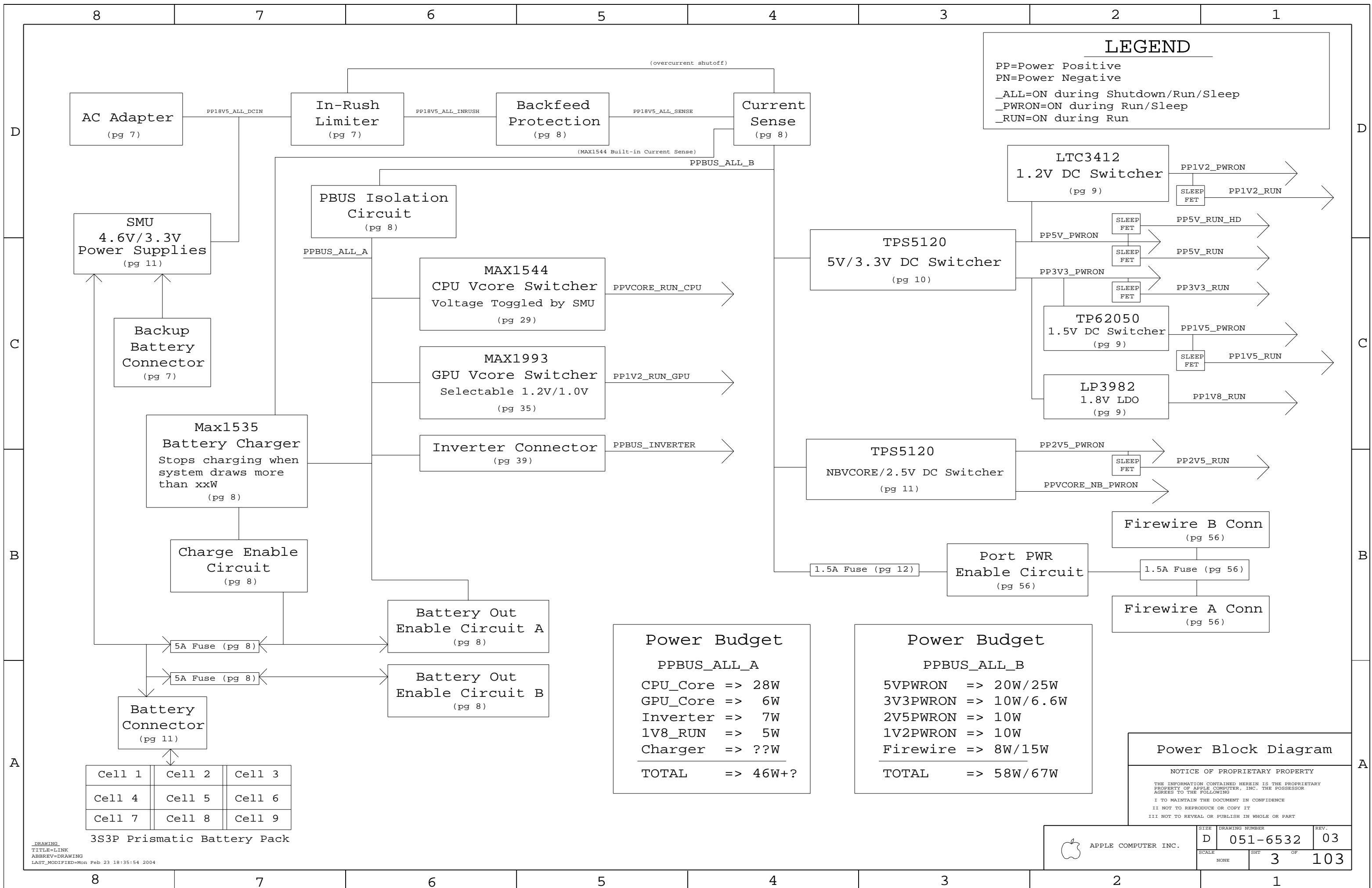
# SYSTEM BLOCK DIAGRAM



## SYSTEM BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	2	103	



AC Adapter  
(pg 7)

In-Rush Limiter  
(pg 7)

Backfeed Protection  
(pg 8)

Current Sense  
(pg 8)

LTC3412  
1.2V DC Switcher  
(pg 9)

TPS5120  
5V/3.3V DC Switcher  
(pg 10)

TP62050  
1.5V DC Switcher  
(pg 9)

LP3982  
1.8V LDO  
(pg 9)

TPS5120  
NBVCORE/2.5V DC Switcher  
(pg 11)

Firewire B Conn  
(pg 56)

Port PWR Enable Circuit  
(pg 56)

Firewire A Conn  
(pg 56)

PBUS Isolation Circuit  
(pg 8)

MAX1544  
CPU Vcore Switcher  
Voltage Toggled by SMU  
(pg 29)

MAX1993  
GPU Vcore Switcher  
Selectable 1.2V/1.0V  
(pg 35)

Inverter Connector  
(pg 39)

Battery Out Enable Circuit A  
(pg 8)

Battery Out Enable Circuit B  
(pg 8)

Max1535  
Battery Charger  
Stops charging when system draws more than xxW  
(pg 8)

Charge Enable Circuit  
(pg 8)

SMU  
4.6V/3.3V Power Supplies  
(pg 11)

Backup Battery Connector  
(pg 7)

Battery Connector  
(pg 11)

Cell 1	Cell 2	Cell 3
Cell 4	Cell 5	Cell 6
Cell 7	Cell 8	Cell 9


3S3P Prismatic Battery Pack

# Revision Notes

1/14/04  
 1) moved Q3001-Q3004,D3001,D3002,R3044,R3046,R3048,R3070,R3050,R3052,R3054 from Page 27 to page 16 to allow sync with Gila  
 2) moved AGP Vref (R4802,R4803,C4818) circuit to M11 specific page (49)  
 3) changed R2191 to pullup on SYS\_LED  
 4) sync with Gila \*\*pullup on SYS\_LED  
 1/20/04  
 1) added 10 mil MIN LINE WIDTH and MIN NECK WIDTH to BKFD\_PROT\_EN\_L  
 2) changed MIN LINE WIDTH of PP5V4 CHRG LDO to 10 mils  
 3) moved J790 (backup battery/R USB connector) to page 18 for syncing with Logic  
 4) moved C600 (BT/USB connector) to page 18 for syncing with Logic  
 5) moved C650 (bus hold-up caps) to page 18 for syncing with Logic  
 6) moved Z79900-Z79903 (EMI vias) to page 18 for syncing with Logic  
 7) moved S2500-S2505 and S2900 to (speaker wire clips) to page 18 for syncing with Logic  
 8) moved Z2500-Z2505 (Z7310 and Z7311 plated screw holes) to page 18 for syncing with Logic  
 9) moved S2510 to page 18 for syncing with Logic  
 10) moved J2130 (trackpad connector) to page 18 for syncing with Logic  
 11) changed C2150 to 20  
 12) added 10 mil MIN LINE WIDTH and MIN NECK WIDTH to KBDLED\_ANODE and KBDLED\_RETURN  
 13) changed C2115 to R2116 (3.32K 1% 402) to divide ALS output to 2.5V  
 14) sync with Logic \*\*\*  
 2/2/04  
 1) changed PCI from shasta to PCI\_SB to allow desktops to insert series R's  
 2) added eg\_73 to alias PCI\_SB nets back to PCI to reconnect  
 3) changed R2150 to 8.25 to reduce LED drive current to 20mA  
 4) changed Q2113 to second FET in Q5909  
 5) changed SMU\_ADAPTER\_ID to SMU\_ONEWIRE  
 6) added R1620 and R1621 to divide ALS output down to 2.5V  
 7) added alias from TP\_SATA\_CLK25M to SATA\_CLK25M  
 8) changed PPVCORE\_RUN\_CPU connection to KW592 to \_PP1V5\_RUN\_FET  
 9) changed C720 to 0.22uF  
 10) changed R800 and R810 to 1/2W 1206 10mohm  
 11) changed C1068 to NO STUFF  
 12) removed C1117 and C1114  
 13) changed R1115 to 2.0uH IMLP5050CE (152S0152)  
 14) changed C1121 to 680PF 402  
 15) changed R1102 to 20K 1% 402  
 16) added MIN LINE WIDTH and MIN NECK WIDTH properties to CPUVCORE\_CM\_N and CPUVCORE\_CS\_N  
 17) added MIN LINE WIDTH and MIN NECK WIDTH properties to ALS1\_PHOTODIODE and ALS1\_OP\_IN  
 3/7/04  
 1) changed R5019 to 26.7K 1% to increase GPU Vcore current limit (rdar://3510721)  
 2) sync with Gila (045) to fix several power disconnects  
 3) added aliases on page 5 to set unused CSE, CS, and MUX controls back to TP  
 4) sync with Logic (043) to get DVO constraints  
 10/04  
 1) changed R3671 to 100K 0.1% to adjust the Tdiode range  
 2) changed R3672 to 10uF 20% 6.3V to adjust the Tdiode range  
 3) changed R3673 to 40.2K 0.1% to adjust the Tdiode range  
 4) changed R3674 to 100K 0.1% to adjust the Tdiode range  
 5) changed R3675 to 100K 20% 6.3V to adjust the Tdiode range  
 6) changed R3676 to 40.2K 0.1% to adjust the Tdiode range  
 7) mirrored R3677 and R3678 to fix layout  
 11/04  
 1) changed L970 to 152S0154 (10uH) to reduce size  
 2/12/04  
 1) removed 197S0703 as alternate for 197S0037 (25MHz Vesta crystal)  
 4) changed all references to SMU\_MANUAL\_RESET\_L to SMU\_RESET\_L  
 2/19/04  
 1) removed DC current limit circuit (U870 and associated discretes)  
 4) added BOMOPTION for 2.8V CPU Avdd LDO  
 5) changed R4800 to 2.2 ohm 603, C4811 to 1uF 402, and C4816 to 0.1uF 402 in U3Lite AGP Avdd filter.  
 6) changed R1610 (series R on SMU\_ONEWIRE output) to 0 ohm  
 7) added R1611 (1k pullup to PP3V3\_ALL) on ADAPTER\_ID to power SMU\_ONEWIRE interface  
 5/23/04  
 1) changed C8160-C8160 (SATA AC coupling caps) to 0.01uF per Marvell recommendation  
 2) added NO\_TEST properties to CPUVCORE\_GNDSENSE and CPUVCORE\_SENSE

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	4		103

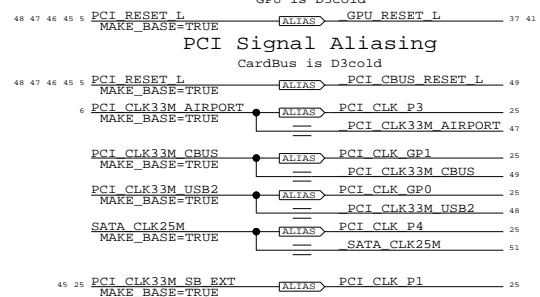
# Page Notes

Power aliases required by this page:  
N/A (Most aliases are on this page)

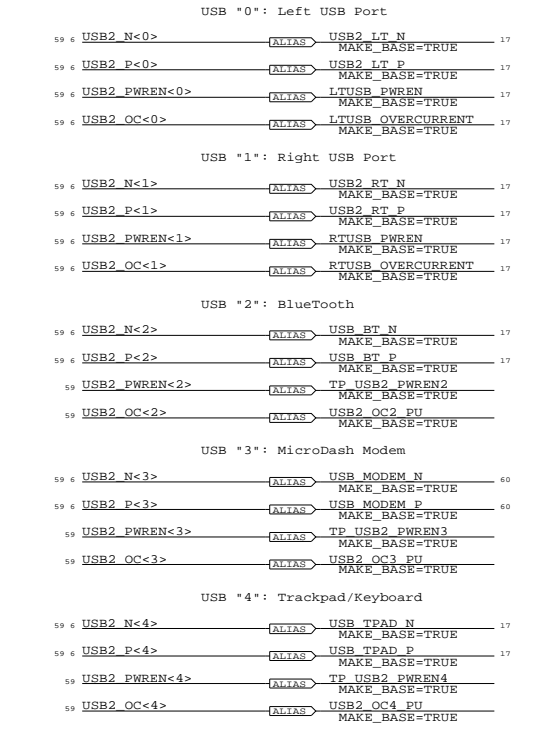
Signal aliases required by this page:  
N/A (Most aliases are on this page)

BOM options provided by this page:  
(NONE)

## AGP Signal Aliasing



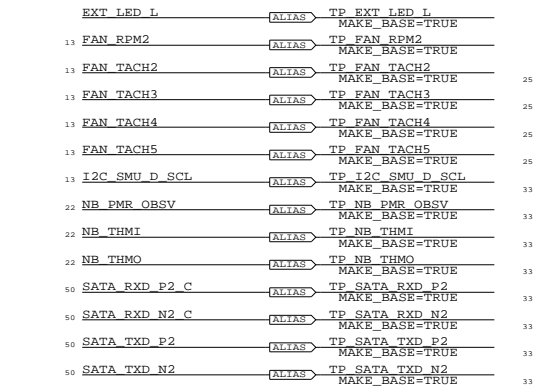
## USB Signal Aliasing



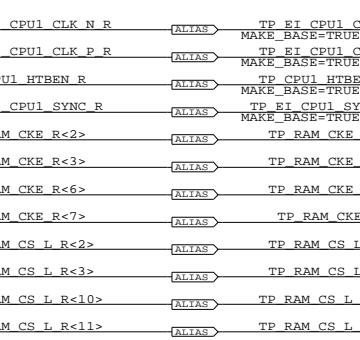
## SMU Signal Aliasing



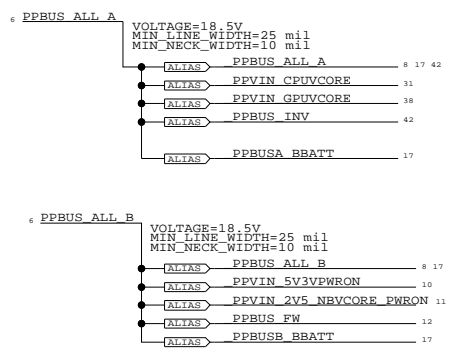
## Test Point Aliasing



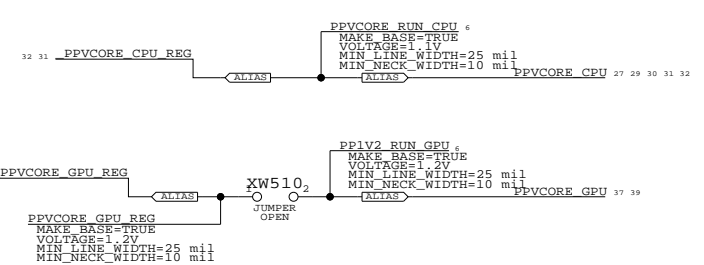
## More Test Point Aliasing



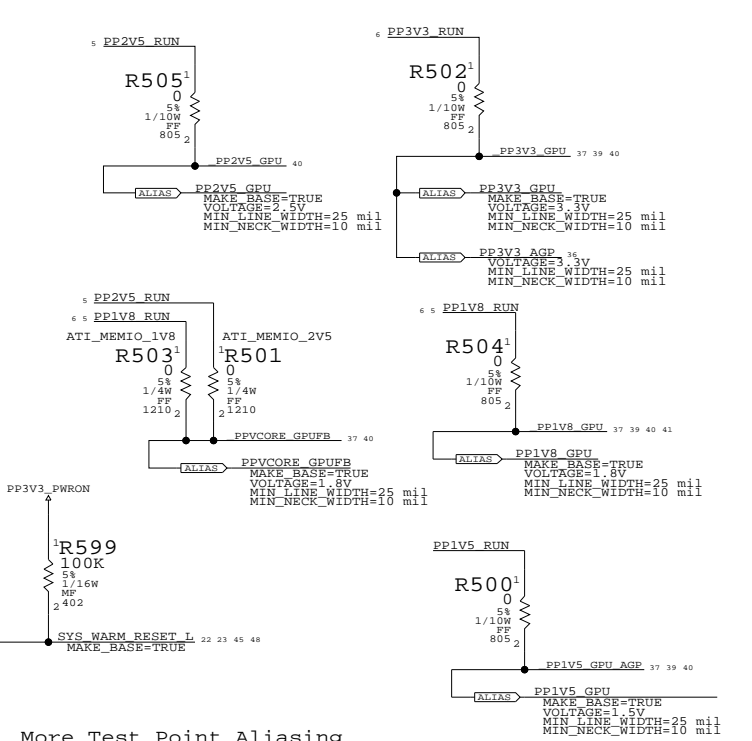
## PBUS PWR



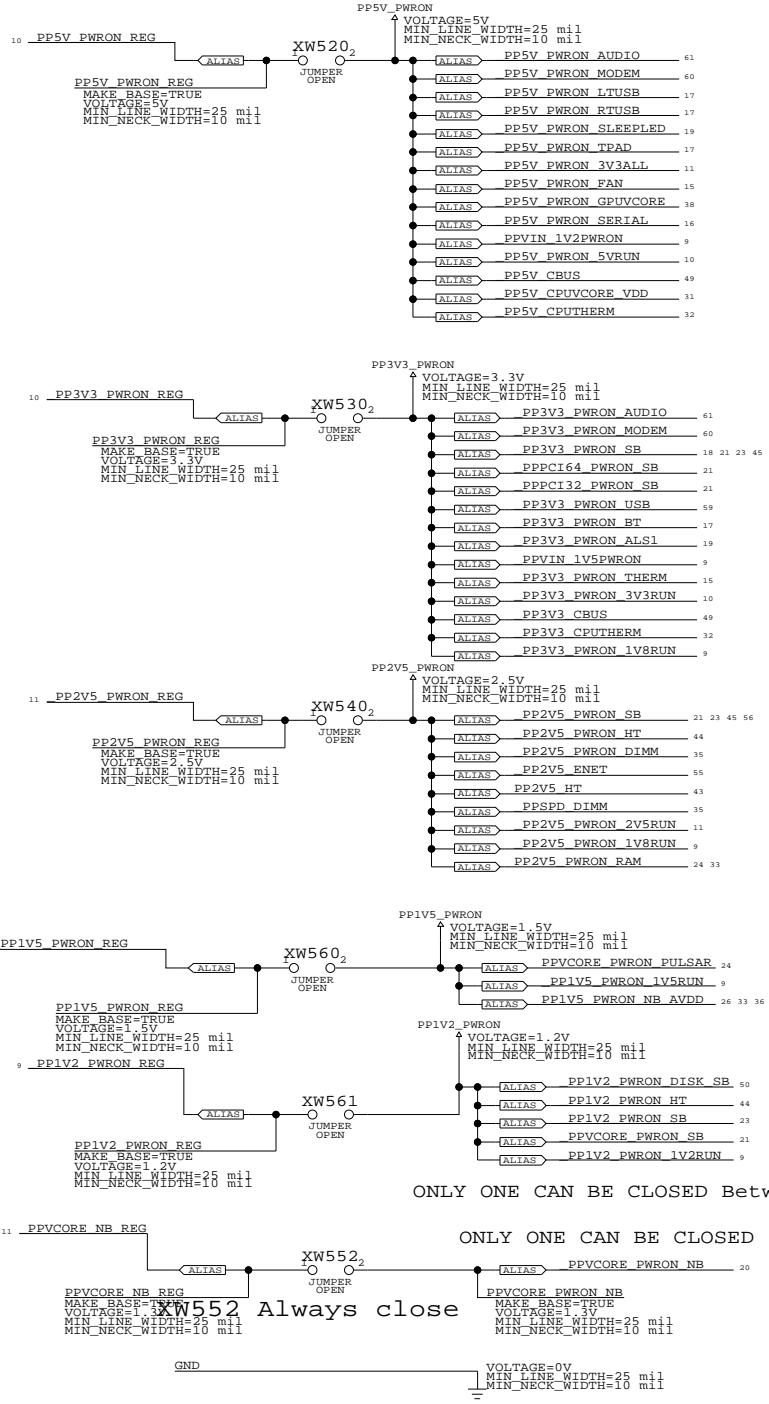
## CPU/GPU Core PWR



## Graphic PWR



## \_PWRON PWR

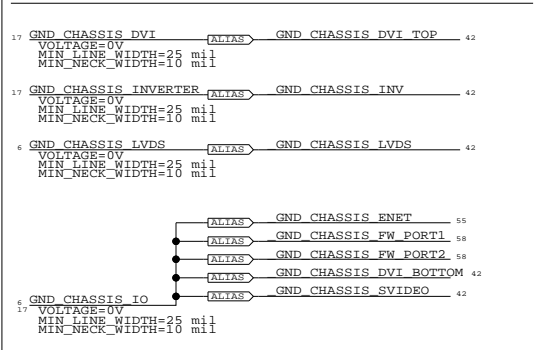


ONLY ONE CAN BE CLOSED Between XW560/XW561!!!

ONLY ONE CAN BE CLOSED Between XW550/XW551!!!

XW552 Always close

## Chassis Grounds



## \_RUN PWR



## Power Connections

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

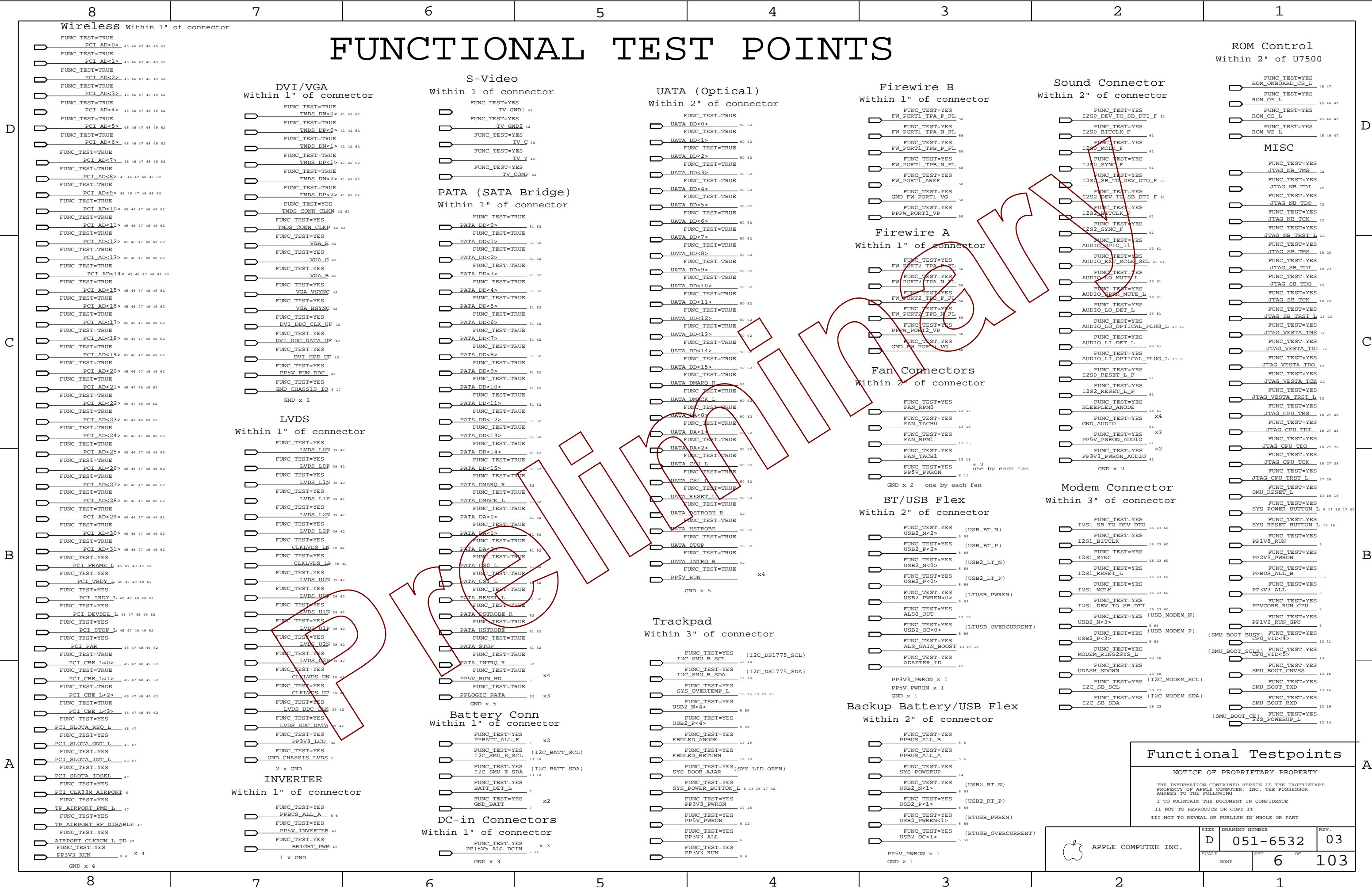
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	51-6532	03
SCALE		SIT	OF
NONE		5	103

# FUNCTIONAL TEST POINTS



## Functional Testpoints

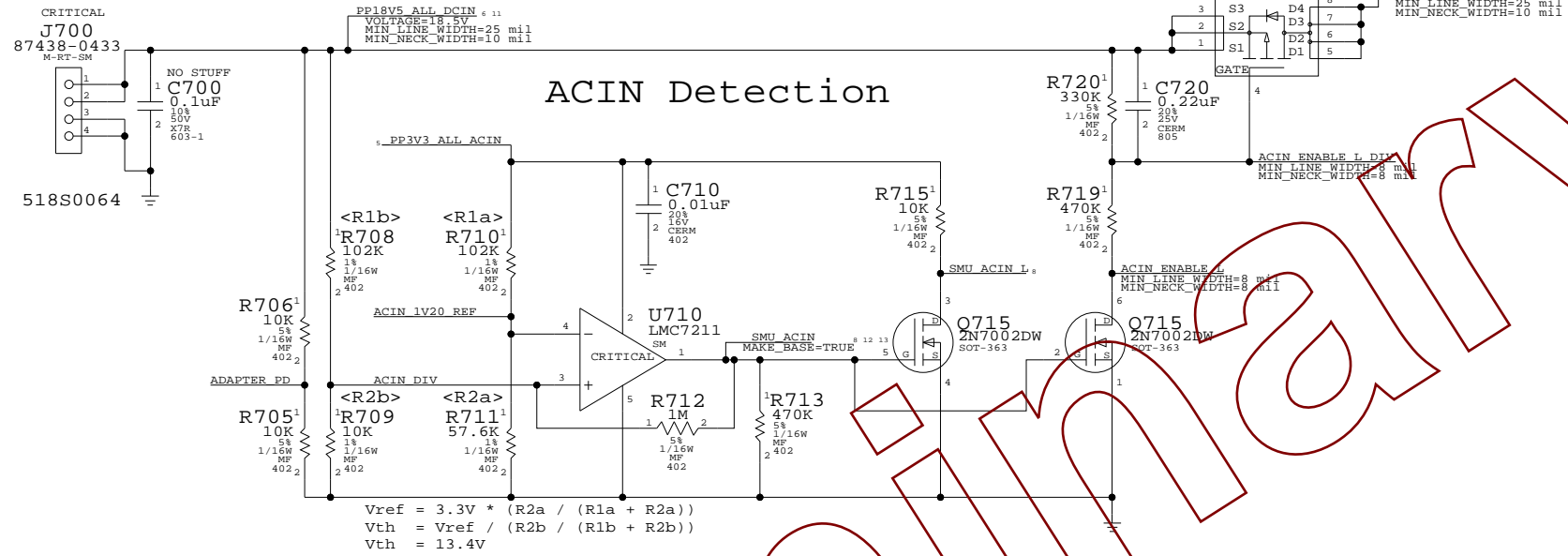
NOTICE OF PROPRIETARY PROPERTY  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHEET	OF	
NONE	6	103	

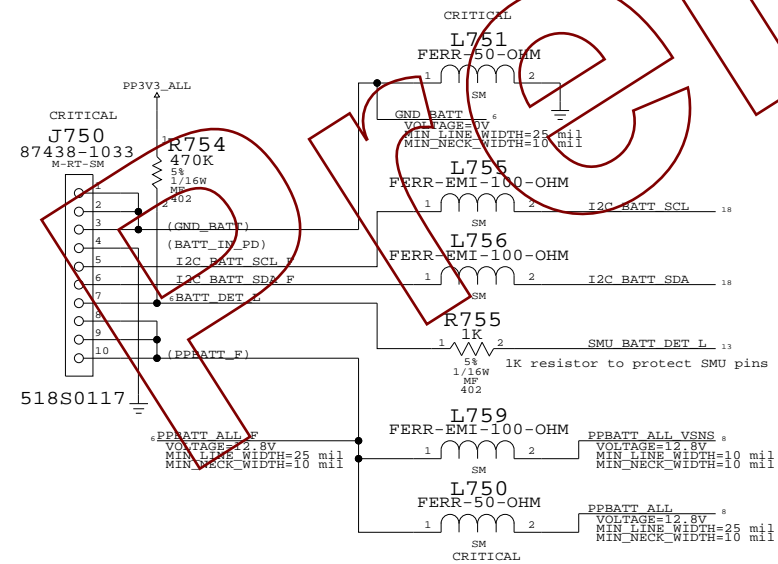
## DC Power Input

(DC-In jack and associated circuit are on separate board)

## DC Inrush Limiter



## Main Battery Connector



## Power Connectors

### NOTICE OF PROPRIETARY PROPERTY

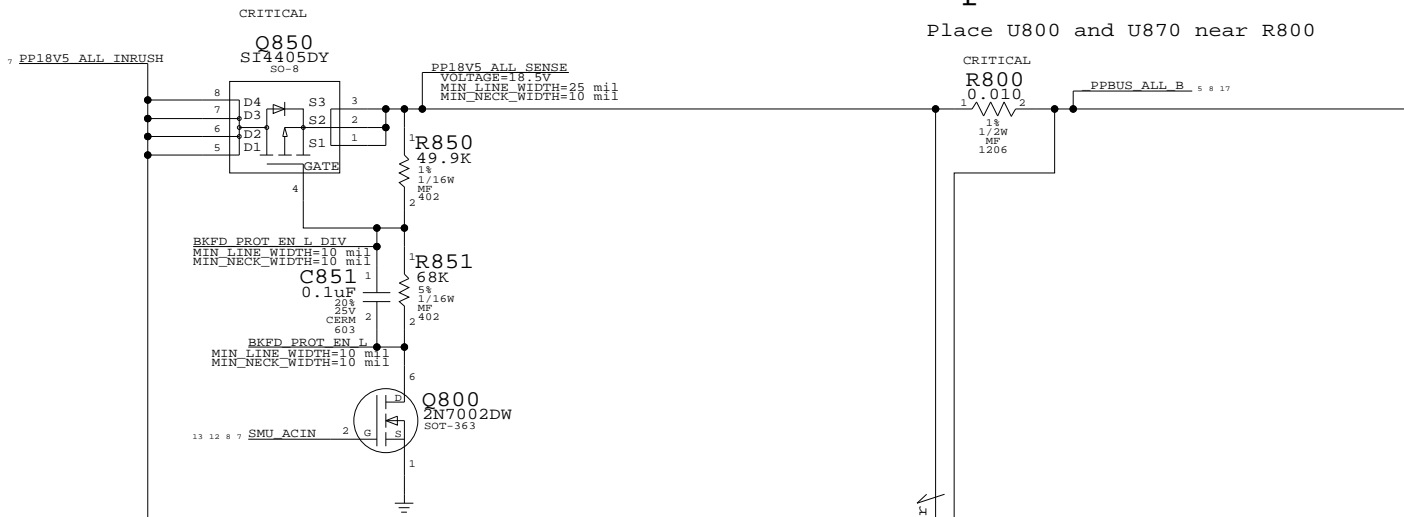
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	7 OF 103

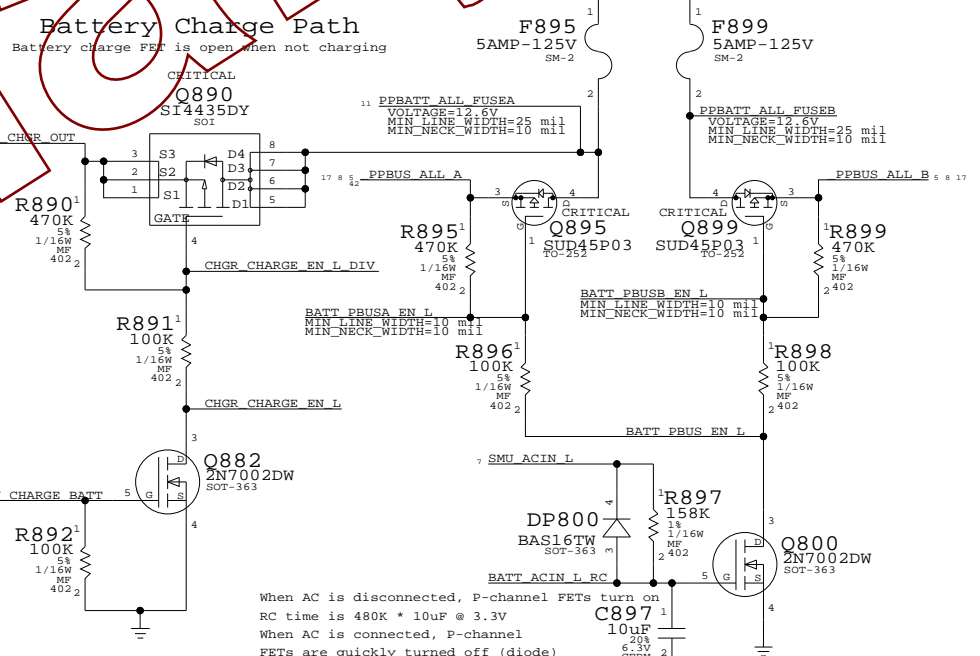


# DC-IN Input Current Limiter

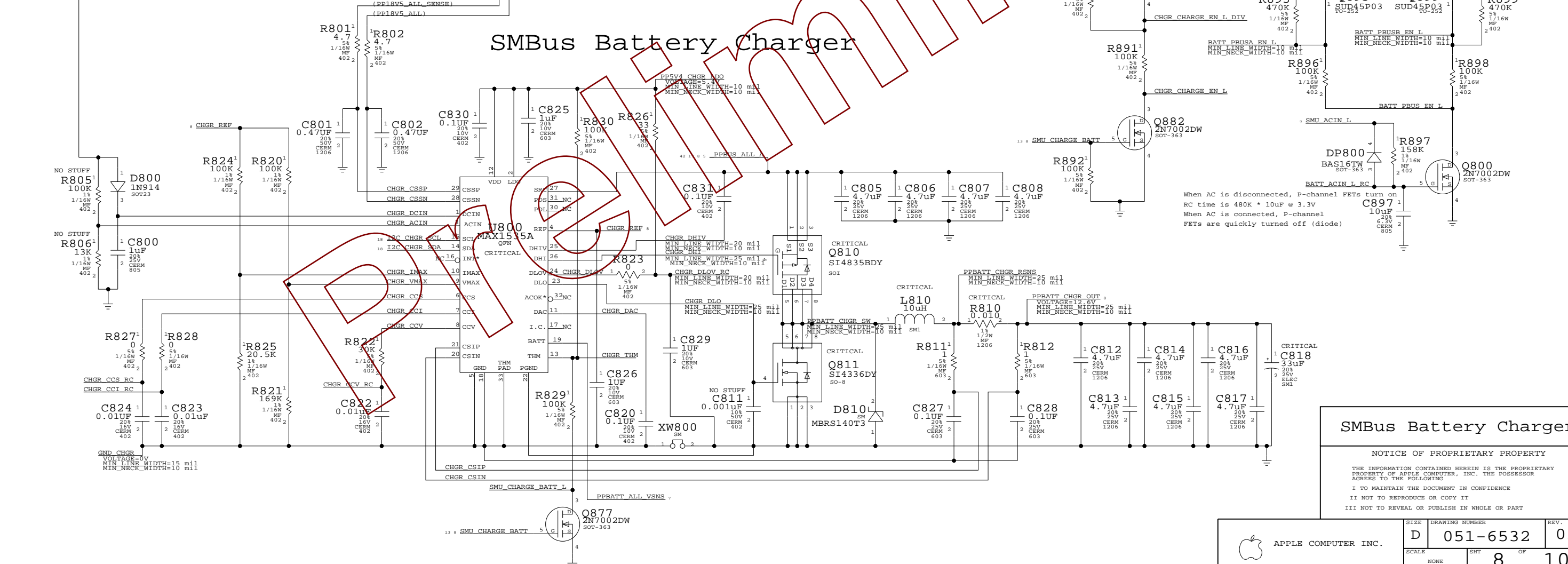
Place U800 and U870 near R800



# Battery Switch-over Circuit



# SMBus Battery Charger



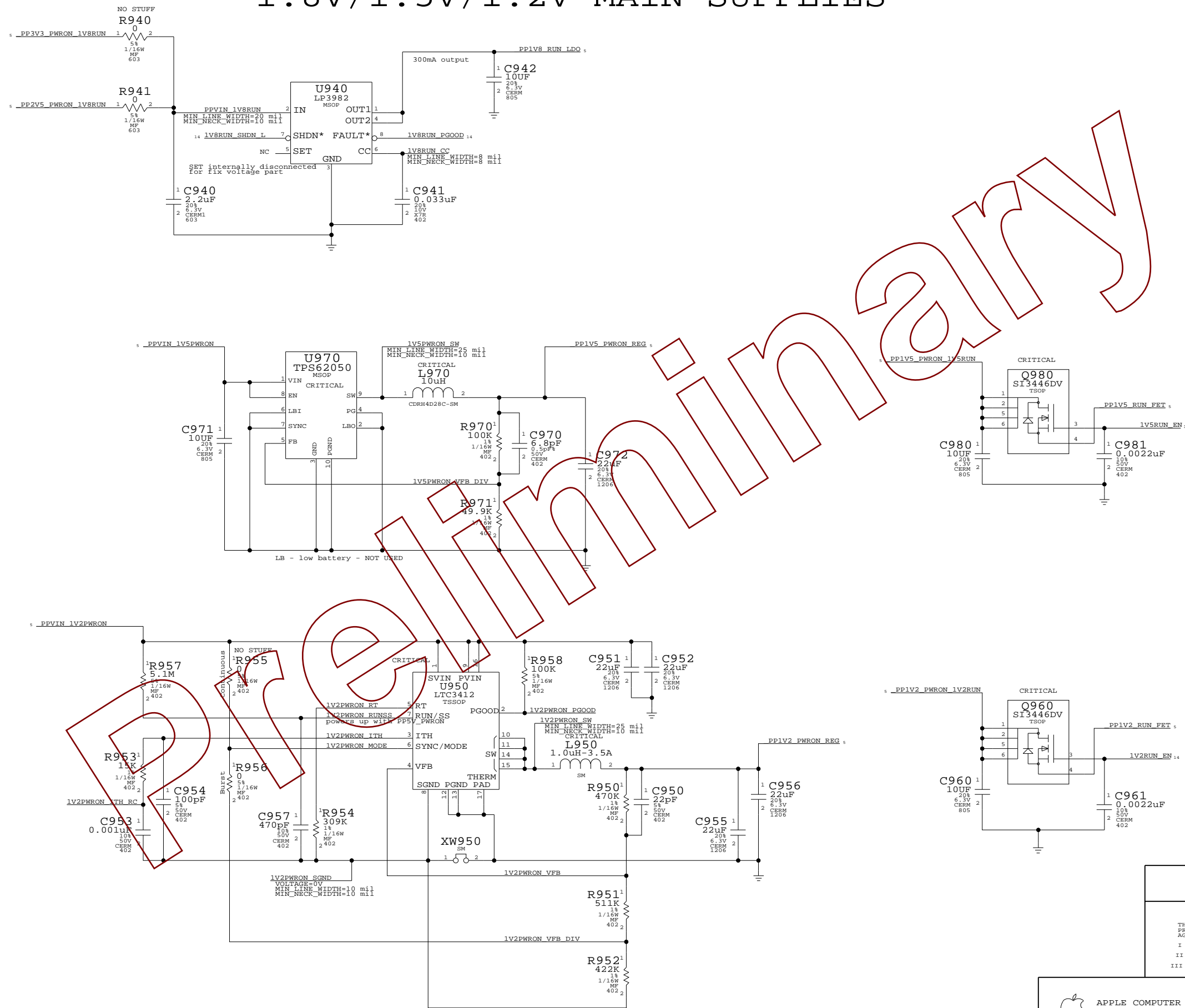
## SMBus Battery Charger

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	8 OF 103



# 1.8V/1.5V/1.2V MAIN SUPPLIES

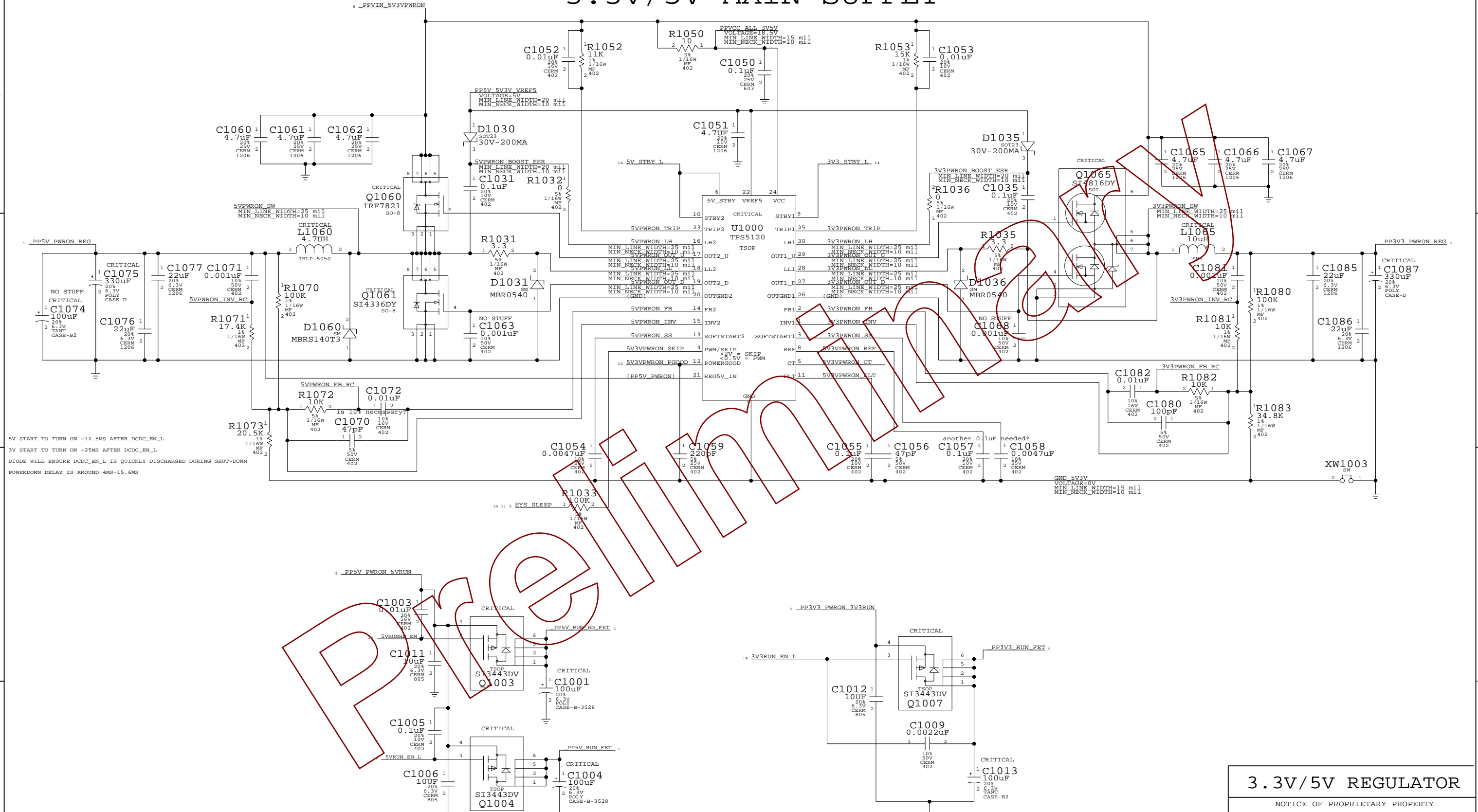


## 1.8V/1.5V Supplies

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	9 OF 103	03

# 3.3V/5V MAIN SUPPLY



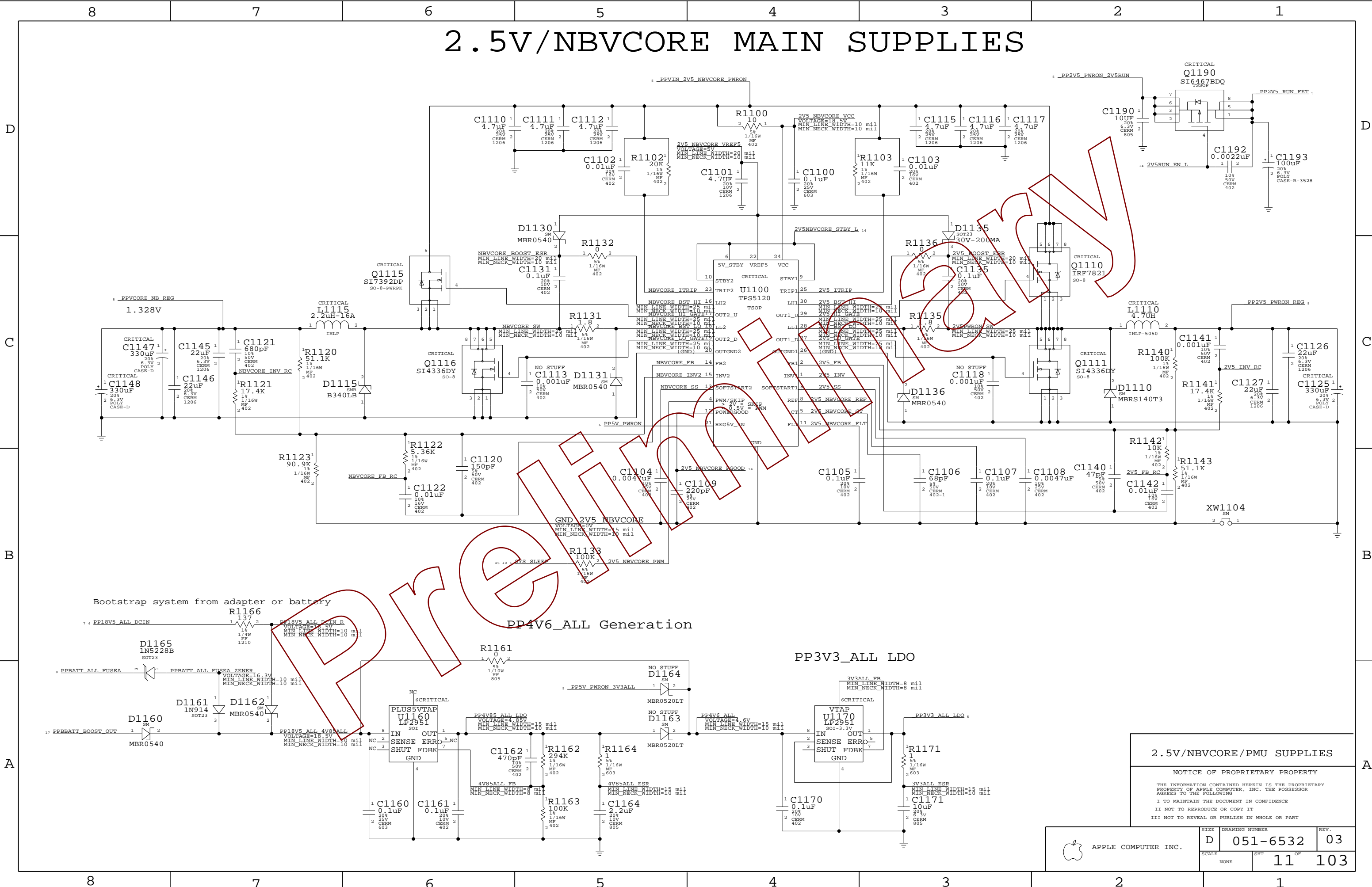
5V START TO TURN ON -12.5MS AFTER DCDC\_EN\_L  
 3V START TO TURN ON -25MS AFTER DCDC\_EN\_L  
 DIODE WILL ENSURE DCDC\_EN\_L IS QUICKLY DISCHARGED DURING SHUT-DOWN  
 POWERDOWN DELAY IS AROUND 4MS-15.6MS

## 3.3V/5V REGULATOR

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	OF
		10	103

# 2.5V/NBVCORE MAIN SUPPLIES



## 2.5V/NBVCORE/PMU SUPPLIES

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	11	103	

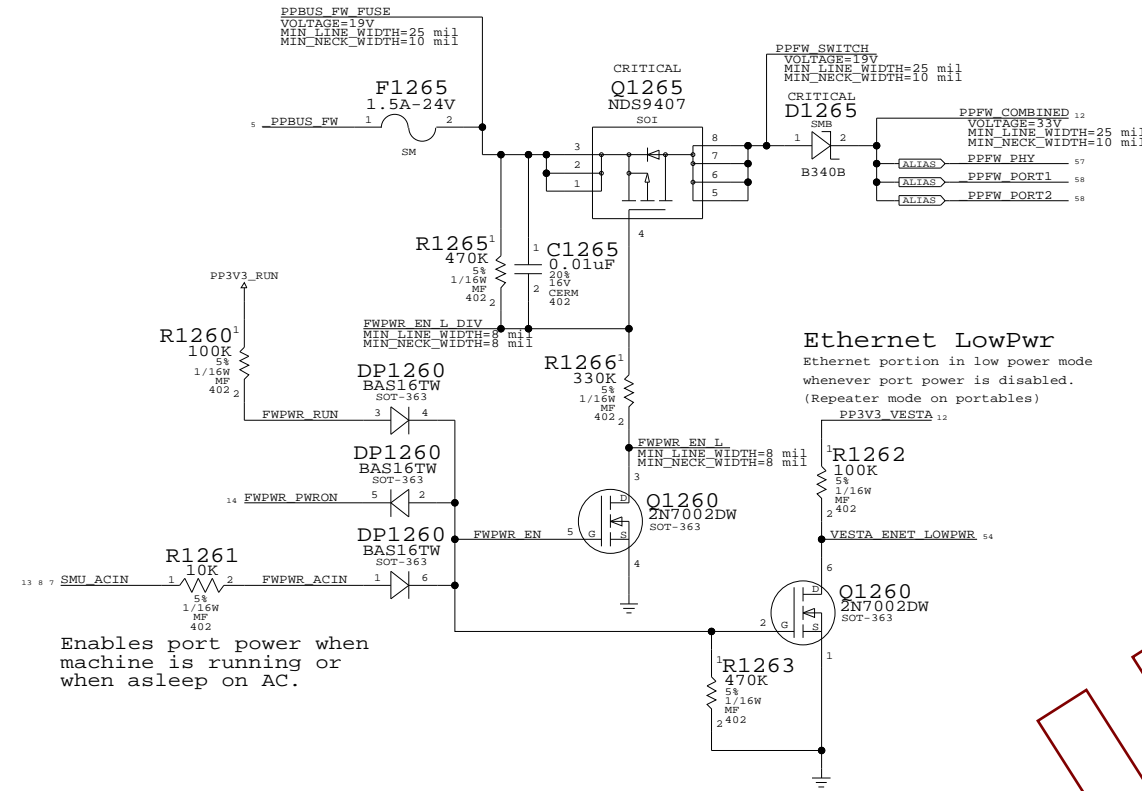
# Page Notes

Power aliases required by this page:  
 - \_PPBUS\_FW (system supply for bus power)  
 - \_PP12V\_RUN\_FW (backup PHY power)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - VESTALV2\_BURST / VESTALV2\_PULSE  
 Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

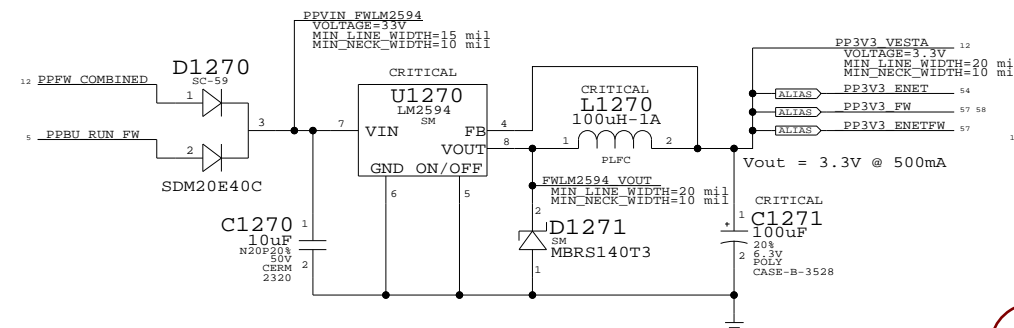
## Port Power Switch



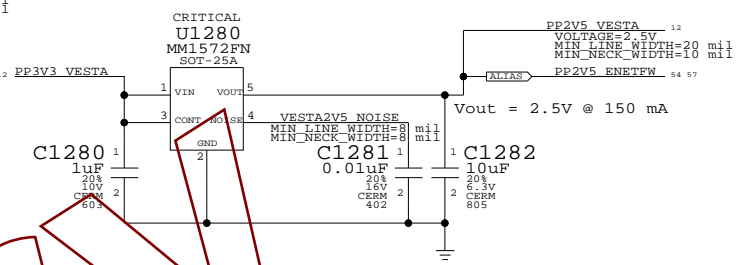
## Ethernet LowPwr

Ethernet portion in low power mode whenever port power is disabled. (Repeater mode on portables)

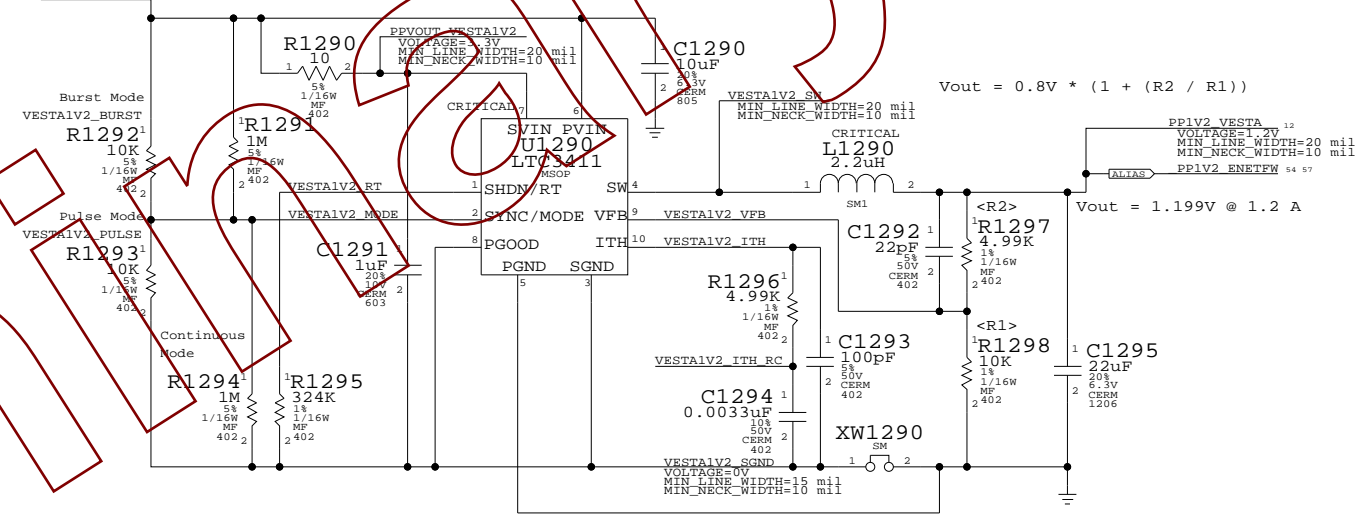
## 3.3V Regulator



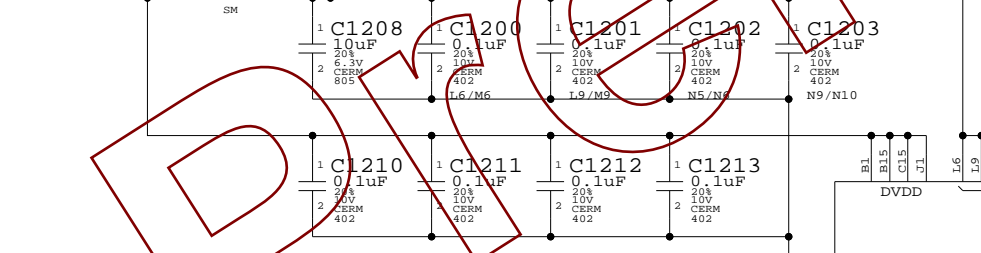
## 2.5V LDO



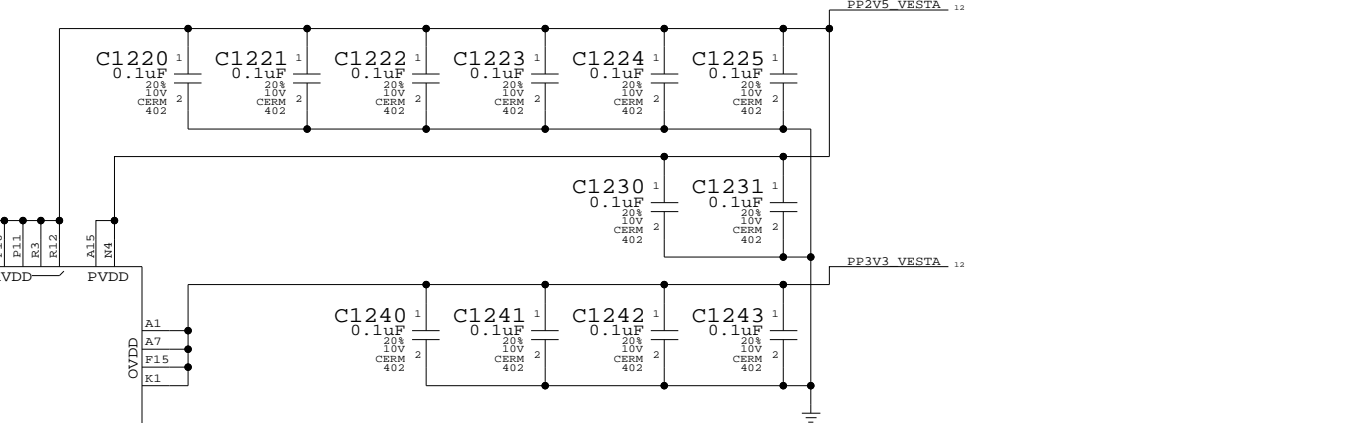
## 1.2V Regulator



## PP12V VESTA



## VESTA MISC



Master: Link

## Vesta Core / Misc

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	12 OF 103	
NONE			



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	15 MIL SPACING	SMU_CLK10M_XIN
	15 MIL SPACING	SMU_CLK10M_XOUT
	15 MIL SPACING	SMU_CLK10M_XOUT_B
RTC_CLK32K_XTAL	15 MIL SPACING	RTC_CLK32K_X1
	15 MIL SPACING	RTC_CLK32K_X2

### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_ALL\_SMU  
 - \_PP3V3\_ALL\_RTC  
 - \_PP3V3\_PWRON\_SMU  
 - \_PPVREF\_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

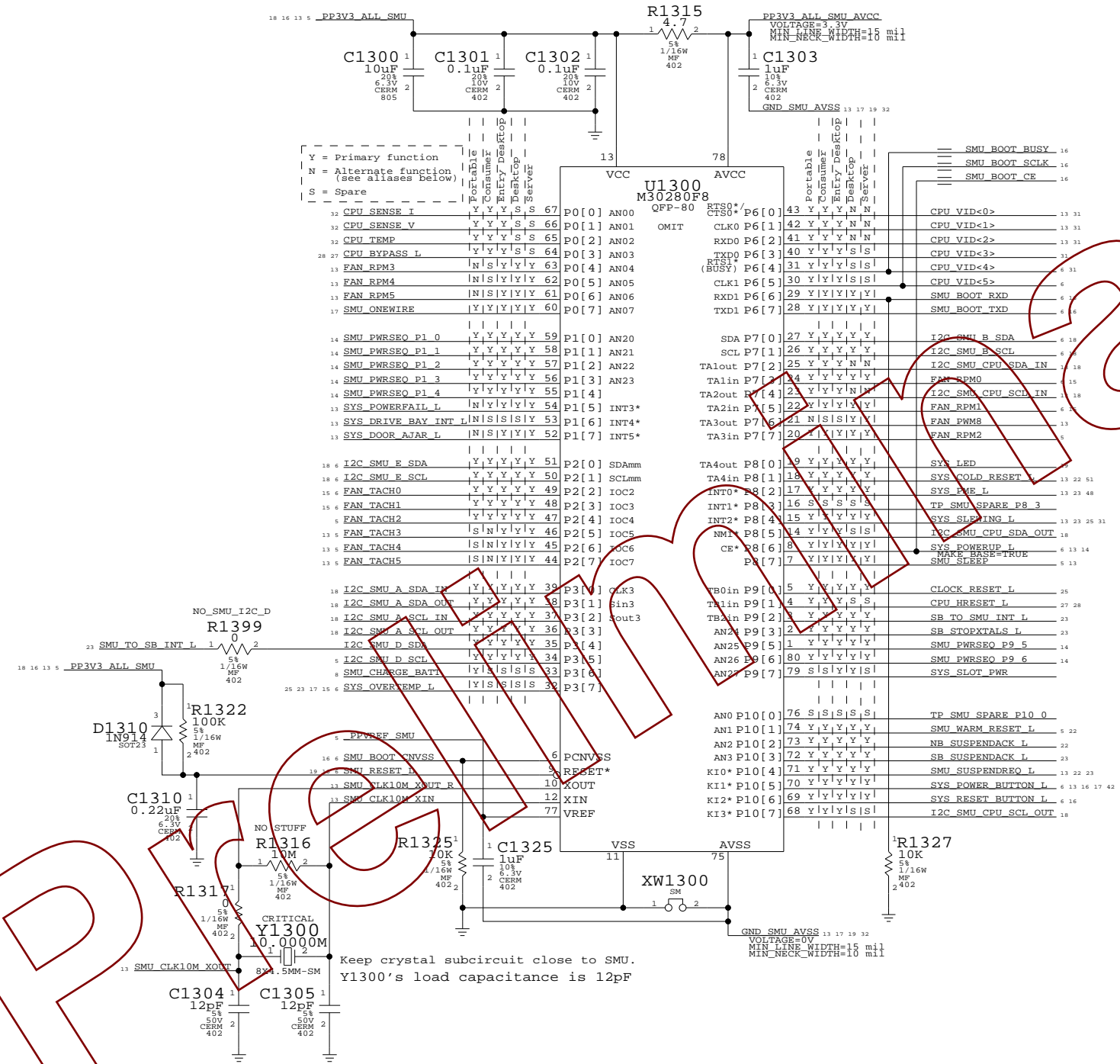
NOTE: CPU current/voltage monitoring (CPU\_SENSE\_I/CPU\_SENSE\_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND\_SMU\_AVSS. SMU\_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND\_SMU\_AVSS). None of those capacitors are provided on this page.

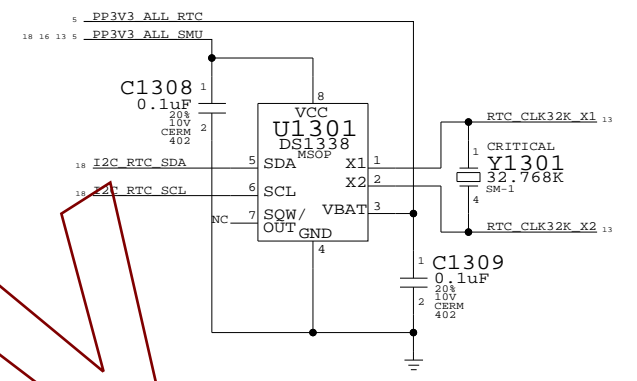
NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

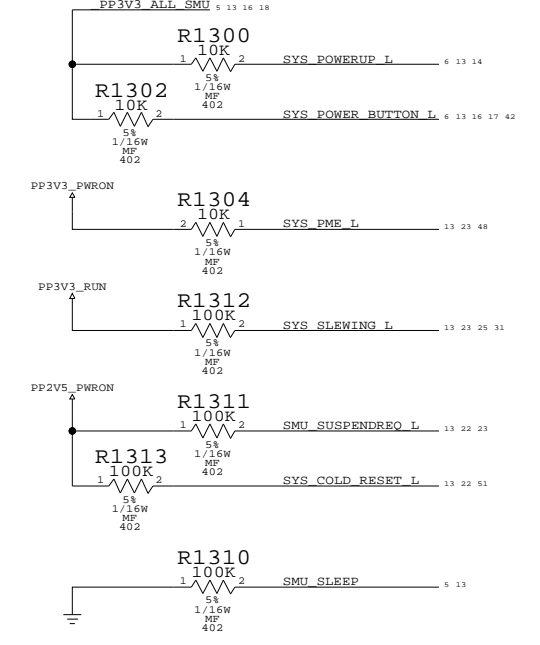
### System Management Unit



### Real Time Clock



### SMU Pull-ups / pull-down



P

### Alternate Functions

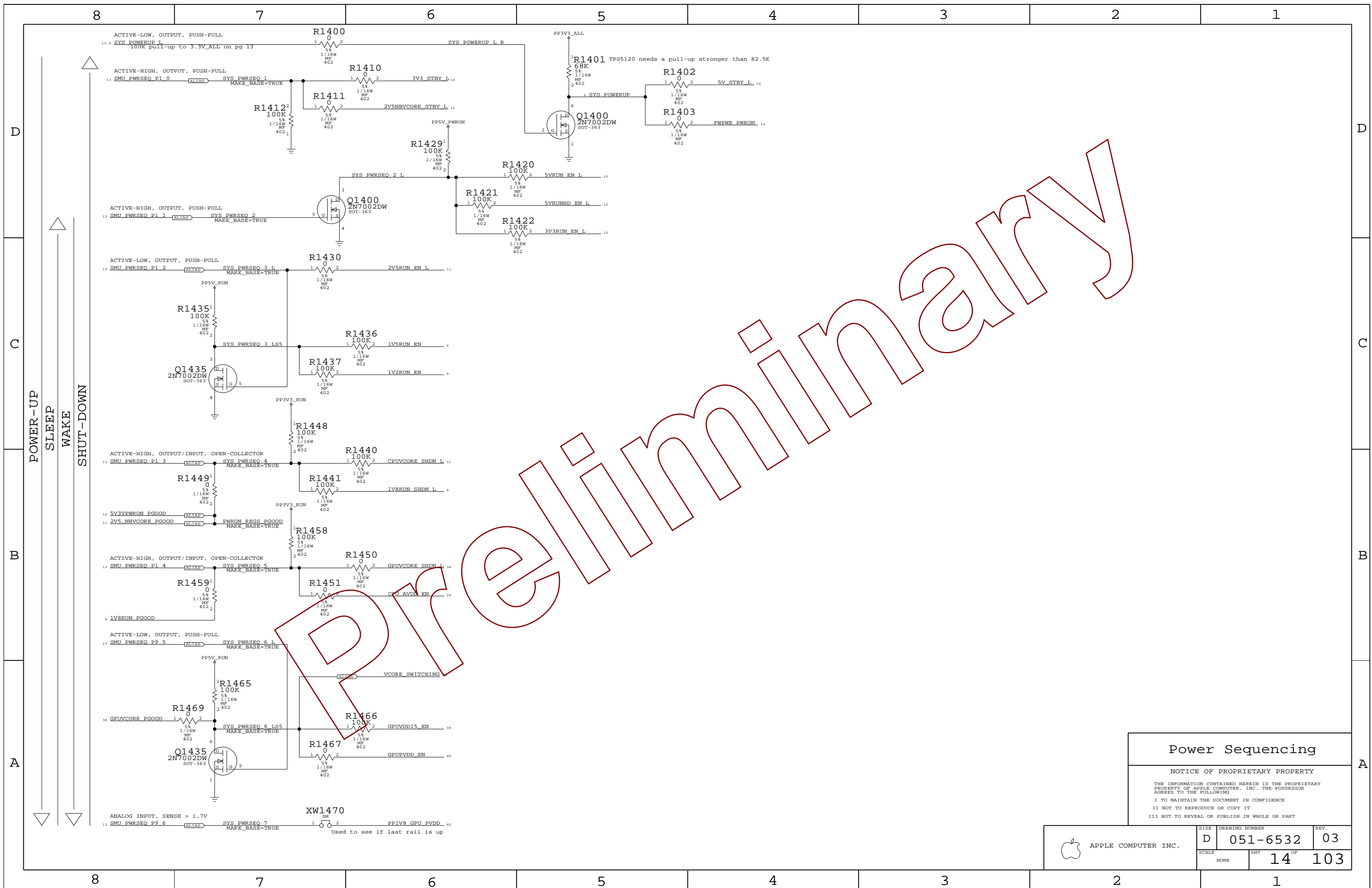
Portable		Consumer		Tower & Server	
Port	Signal	Port	Signal	Port	Signal
13	FAN_RPM3	0.4	ALSO OUT	6.17	FAN_TACH6
13	FAN_RPM4	0.5	ALS1 OUT	19	FAN_TACH7
13	FAN_RPM5	0.6	ALS_GAIN_BOOST	6.17	FAN_TACH8
13	SYS_POWERFAIL_L	1.5	SMU_ACIN	7.8	FAN_PMM6
13	SYS_DRIVE_BAY_INT_L	1.6	SMU_BATT_DET_L	7	FAN_PMM7
13	SYS_DOOR_AJAR_L	1.7	SYS_LID_OPEN	17	
13	FAN_PMM8	7.6	SYS_KBDLED	19	
13	FAN_RPM3	0.4		6.17	
13	FAN_RPM4	0.5		19	
13	FAN_RPM5	0.6		6.17	
13	SYS_POWERFAIL_L	1.5		7.8	
13	SYS_DRIVE_BAY_INT_L	1.6		7	
13	SYS_DOOR_AJAR_L	1.7		17	
13	FAN_PMM8	7.6		19	

Master: Link

### System Management Unit

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6532	03
		SHEET	OF
		13	103



**Power Sequencing**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	14 OF 103	03



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	THERM	MAX1989_D1	MAX1989_D1_P	15
	THERM	MAX1989_D1	MAX1989_D1_N	15
	THERM	MAX1989_D2	MAX1989_D2_P	15
	THERM	MAX1989_D2	MAX1989_D2_N	15
	THERM	MAX1989_D3	MAX1989_D3_P	15
	THERM	MAX1989_D3	MAX1989_D3_N	15
	THERM	MAX1989_D4	MAX1989_D4_P	15
	THERM	MAX1989_D4	MAX1989_D4_N	15
	THERM	THERM_1	THERM_1_P	15
	THERM	THERM_1	THERM_1_N	15
	THERM	THERM_2	THERM_2_P	15
	THERM	THERM_2	THERM_2_N	15
	THERM	THERM_3	THERM_3_P	15
	THERM	THERM_3	THERM_3_N	15
	THERM	THERM_1B	THERM_1B_P	15
	THERM	THERM_1B	THERM_1B_N	15
	THERM	THERM_2B	THERM_2B_P	15
	THERM	THERM_2B	THERM_2B_N	15
	THERM	THERM_3B	THERM_3B_P	15
	THERM	THERM_3B	THERM_3B_N	15

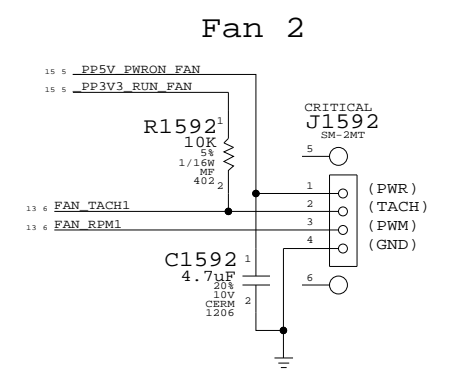
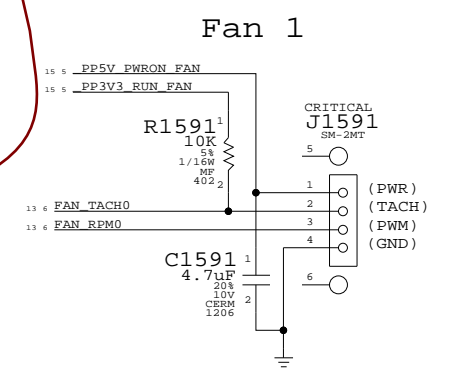
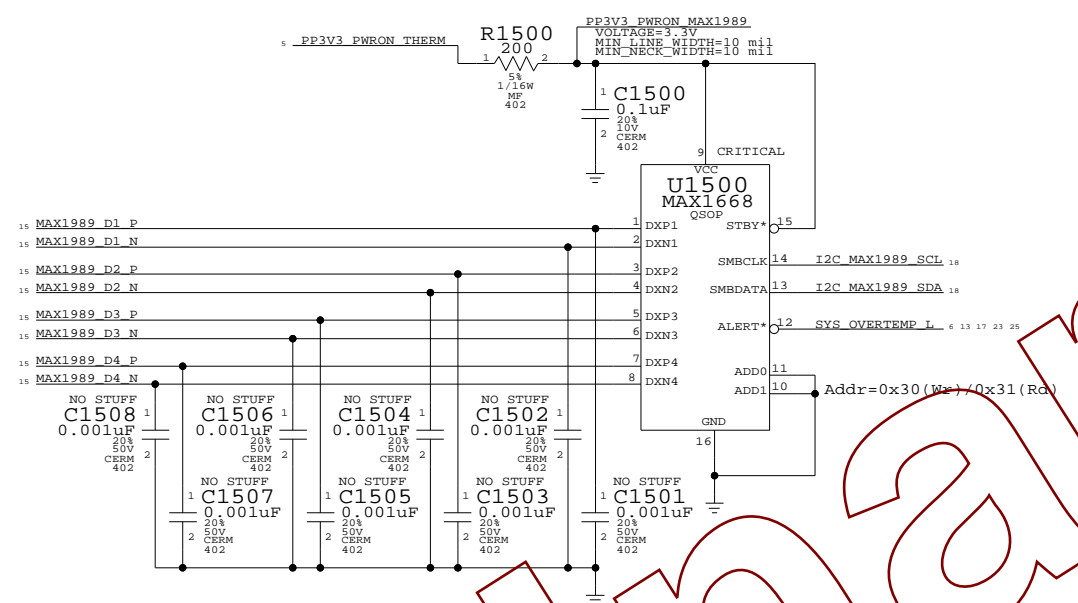
### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PWRON\_THERM  
 - \_PP5V\_PWRON\_FAN

Signal aliases required by this page:  
 (NONE)

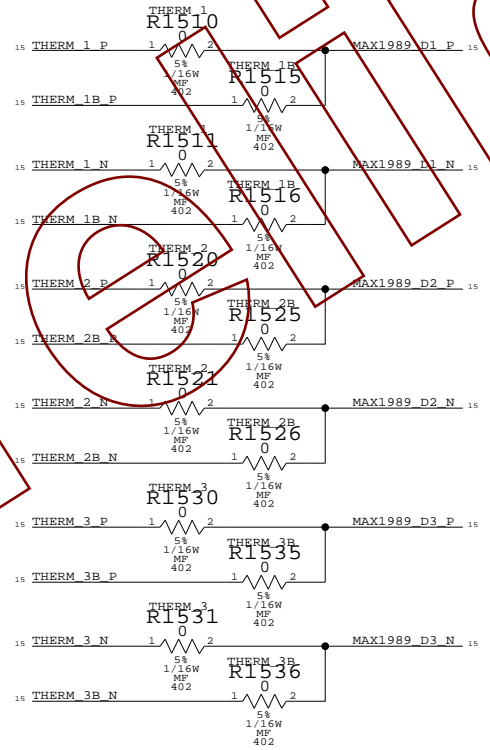
BOM options provided by this page:  
 - THERM\_x / THERM\_xB  
 Selects between primary and backup thermal sensors for each of the available remote sensor locations.

### MAX1989 Thermal Sensor



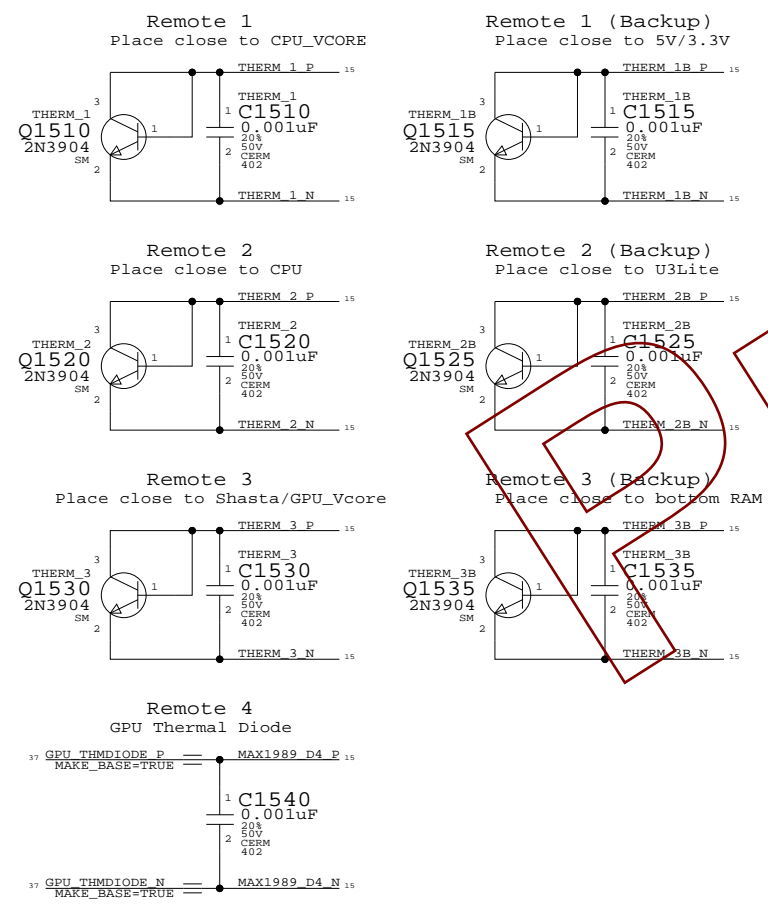
### Sensor Selection

First 3 MAX1668 inputs can connect to two different sensors. These resistors should be close to MAX1668, minimizing stubs.



### Remote Temperature Sensors

Place each cap close to associated transistor



### Thermal Sensor / Fans

NOTICE OF PROPRIETARY PROPERTY

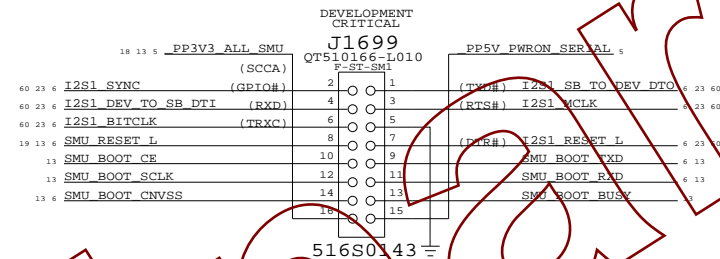
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

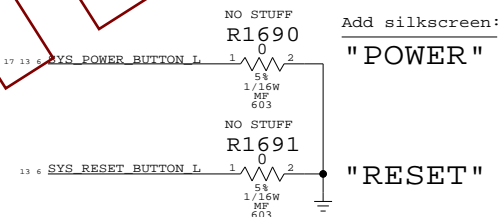
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	15 OF	103
NONE			

### SMU Download / Serial Debug Connector

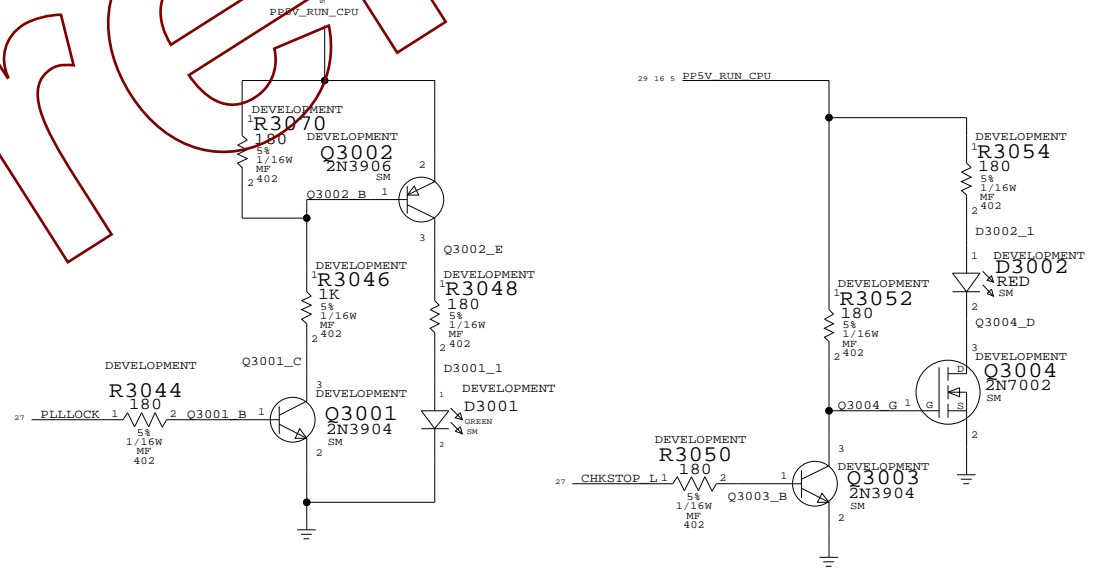
SCC same pins have pinout as modem connector to allow serial debug flex to use either connector



### Debug "Buttons"



### Debug LEDs



### INTERNAL I/O CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

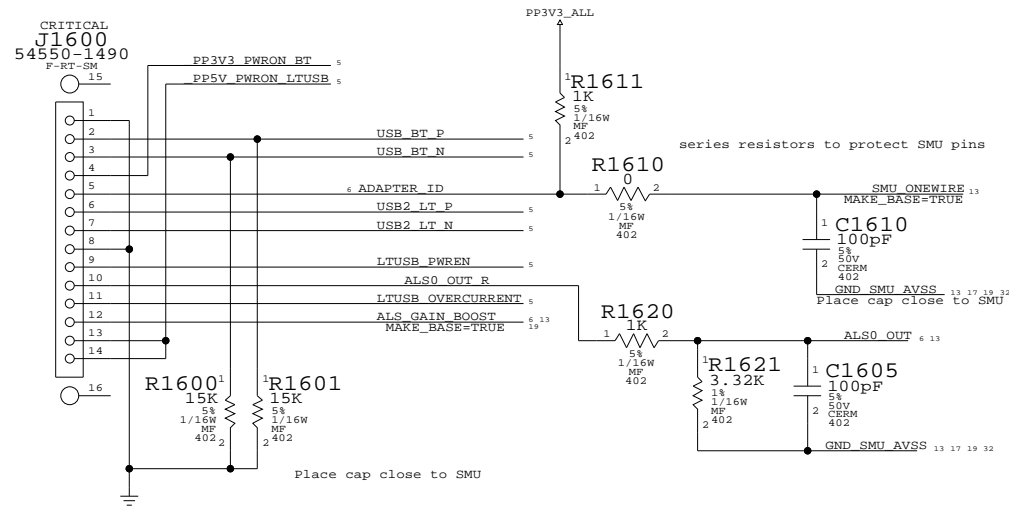
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

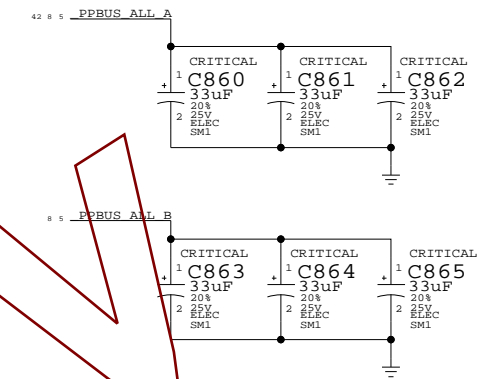
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT		OF
NONE	16		103

Preliminary

BlueTooth / Left USB Flex Connector

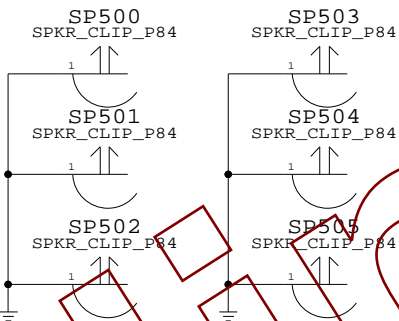
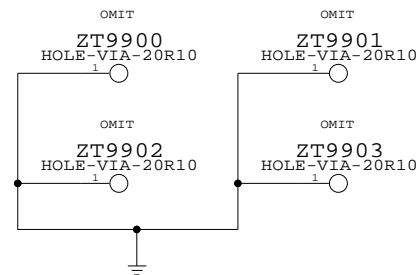


PPBUS Hold-Up Caps

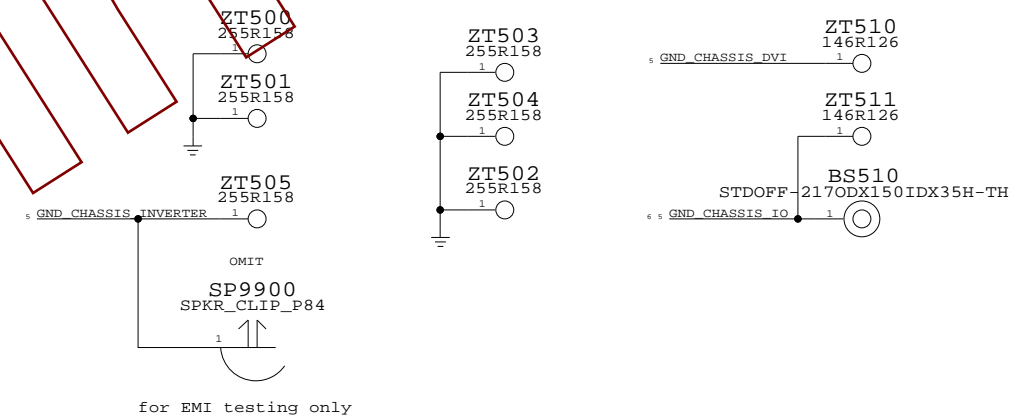


Speaker Clips

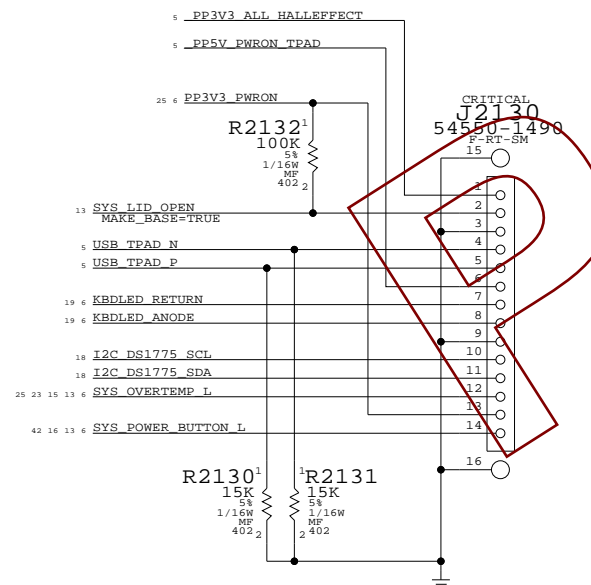
For EMI around ENET magnetic



CPU Heat Sink Graphic Heat Sink Right I/O area

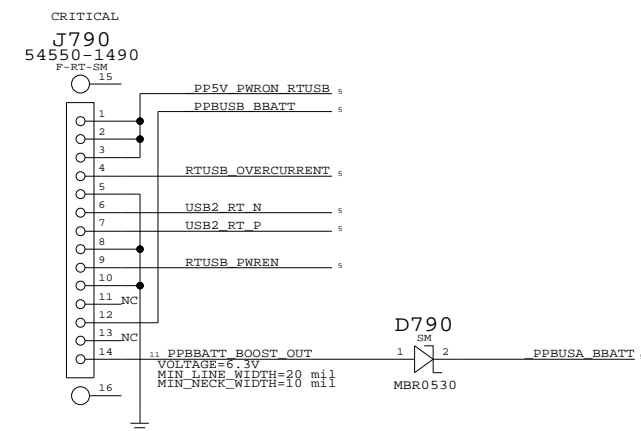


USB Trackpad Connector



overtemp may need pull-up resistor

Backup Battery / Right USB Flex Connector



\_PPBUS\_BBATT is both an input and an output for backup battery circuit. \_PPBUSA\_BBATT is an output only.

Q51 Specific connectors

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	103
NONE	18		

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
I2C_SMU_A_OUT	I2C	I2C_SMU_A_OUT	I2C_SMU_A_SCL_OUT
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SDA_OUT
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SCL_IN
I2C_SMU_A_IN	I2C	I2C_SMU_A_IN	I2C_SMU_A_SDA_IN
I2C_SMU_CPU_OUT	I2C	I2C_SMU_CPU_OUT	I2C_SMU_CPU_SCL_OUT
I2C_SMU_CPU_OUT	I2C	I2C_SMU_CPU_OUT	I2C_SMU_CPU_SDA_OUT
I2C_SMU_CPU_IN	I2C	I2C_SMU_CPU_IN	I2C_SMU_CPU_SCL_IN
I2C_SMU_CPU_IN	I2C	I2C_SMU_CPU_IN	I2C_SMU_CPU_SDA_IN
I2C_CPU_A_OUT	I2C	I2C_CPU_A_OUT	I2C_CPU_A_SCL
I2C_CPU_A_OUT	I2C	I2C_CPU_A_OUT	I2C_CPU_A_SDA
I2C_CPU_A_IN	I2C	I2C_CPU_A_IN	SMU_CPU_JTAG_OR_I2C
I2C_CPU_A_IN	I2C	I2C_CPU_A_IN	I2C_CPU_A_SDA_TO_SMU
I2C_SMU_B_OUT	I2C	I2C_SMU_B_OUT	I2C_SMU_B_SCL
I2C_SMU_B_OUT	I2C	I2C_SMU_B_OUT	I2C_SMU_B_SDA
I2C_NB_B_OUT	I2C	I2C_NB_B_OUT	I2C_NB_B_SCL
I2C_NB_B_OUT	I2C	I2C_NB_B_OUT	I2C_NB_B_SDA
I2C_NB_C_OUT	I2C	I2C_NB_C_OUT	I2C_NB_C_SCL
I2C_NB_C_OUT	I2C	I2C_NB_C_OUT	I2C_NB_C_SDA
I2C_SB_OUT	I2C	I2C_SB_OUT	I2C_SB_SCL
I2C_SB_OUT	I2C	I2C_SB_OUT	I2C_SB_SDA

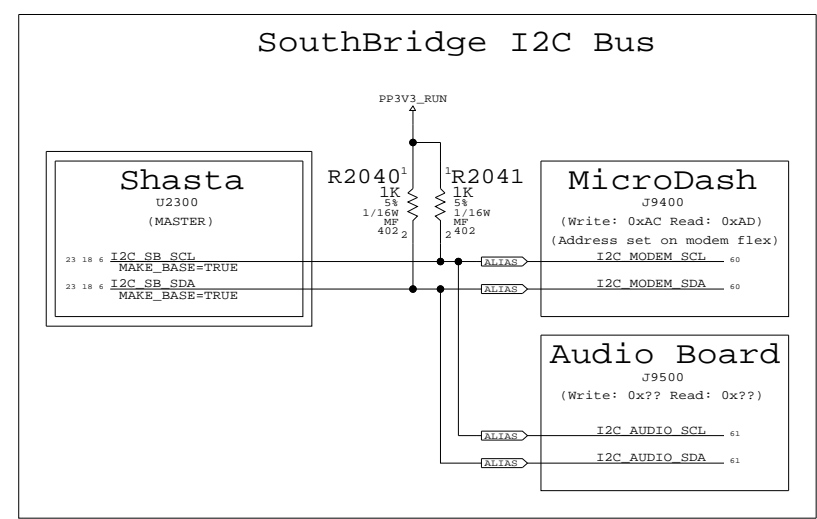
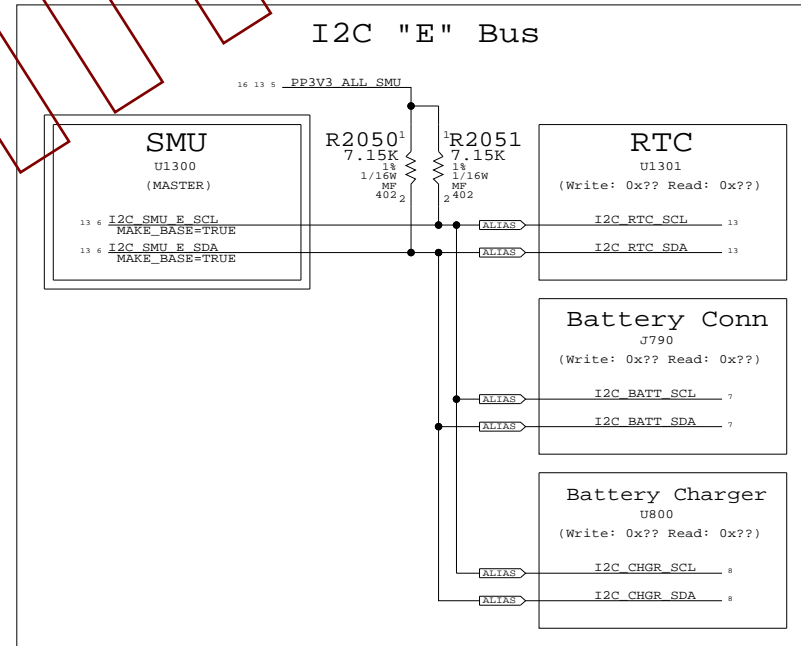
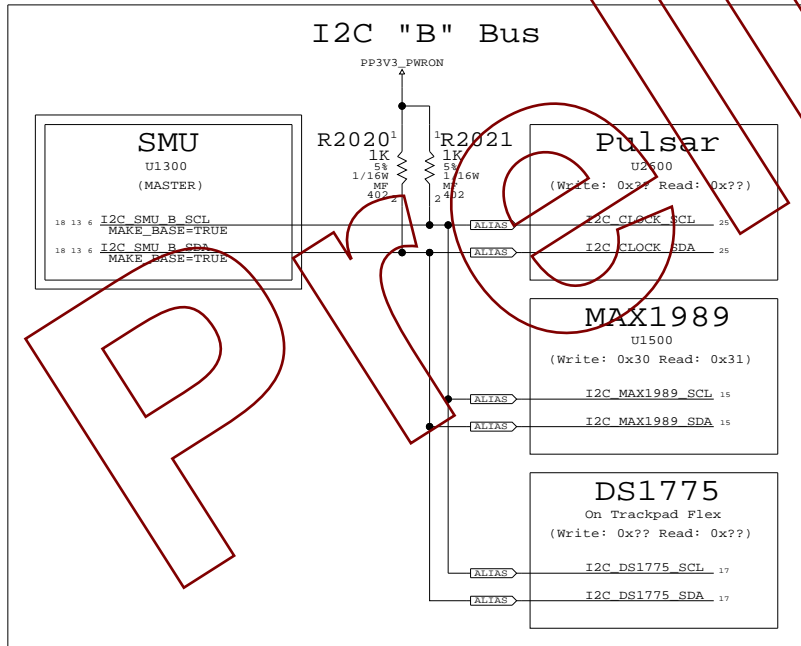
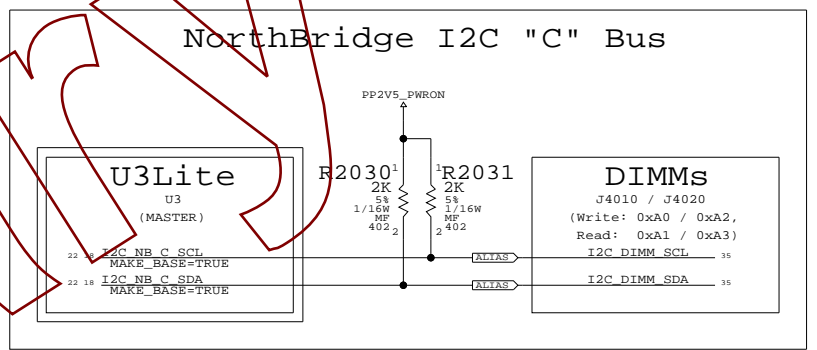
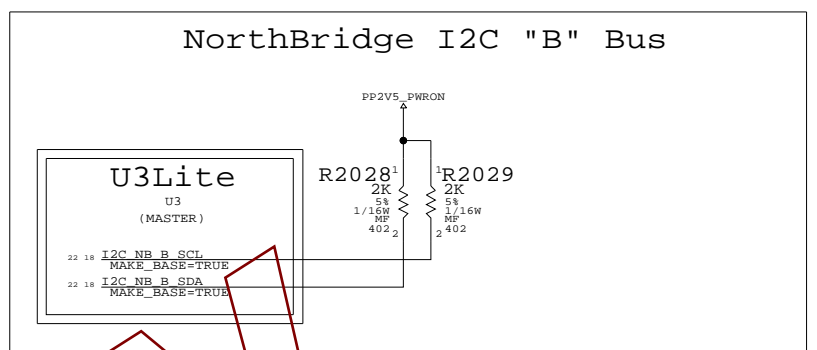
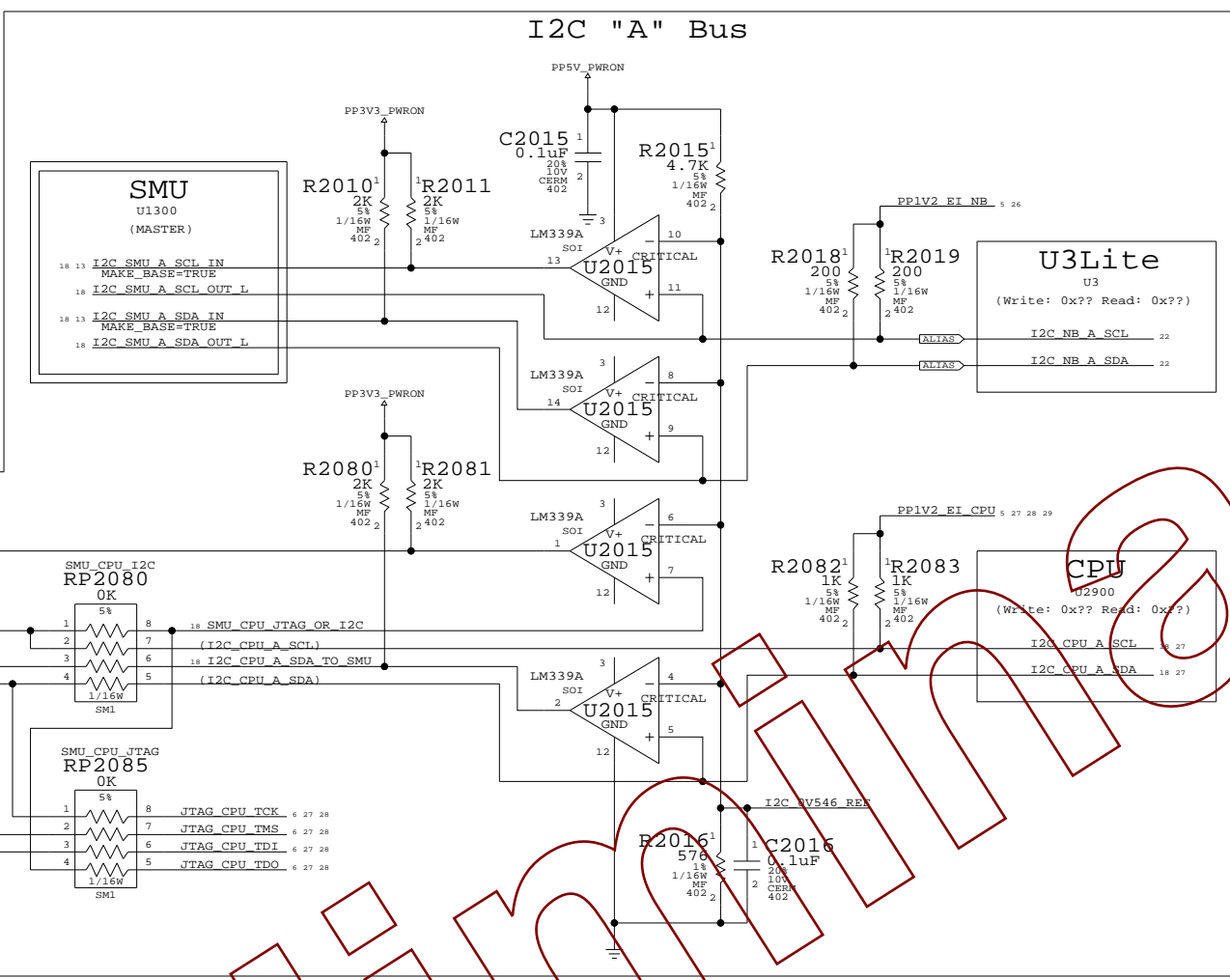
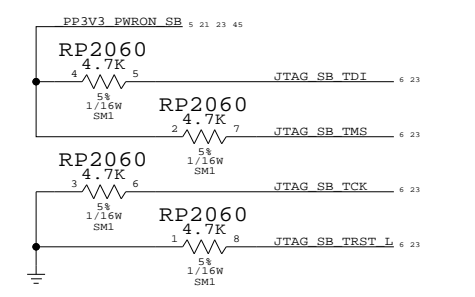
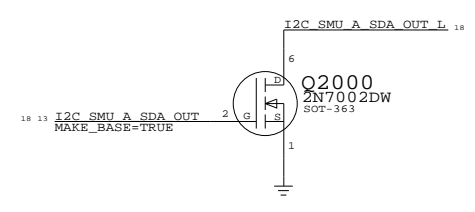
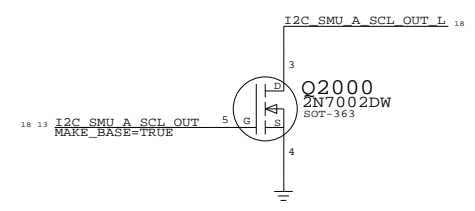
### Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

### U3 Lite I2C inversion



### I2C CONNECTIONS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

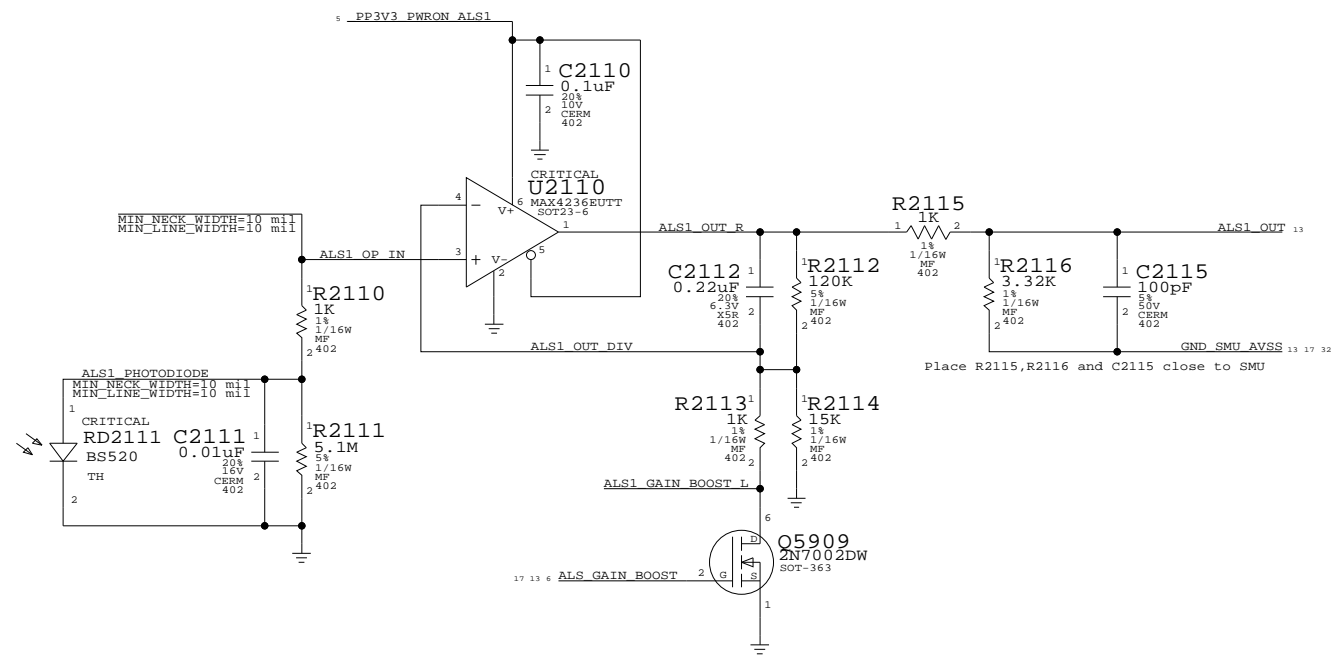
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	20	103	

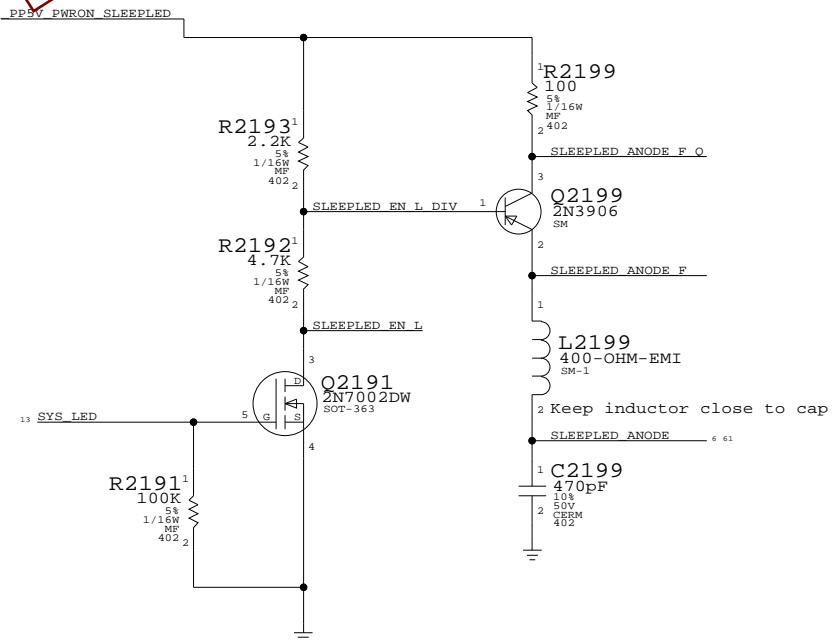
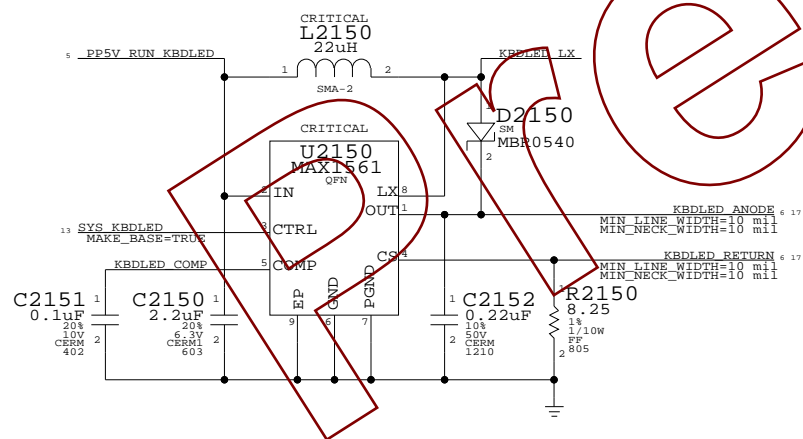
### Ambient Light Sensor #1



### SMU / System Reset Button

### Sleep LED Circuit

### Keyboard LED Driver



### SMU ALS/LEDs

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

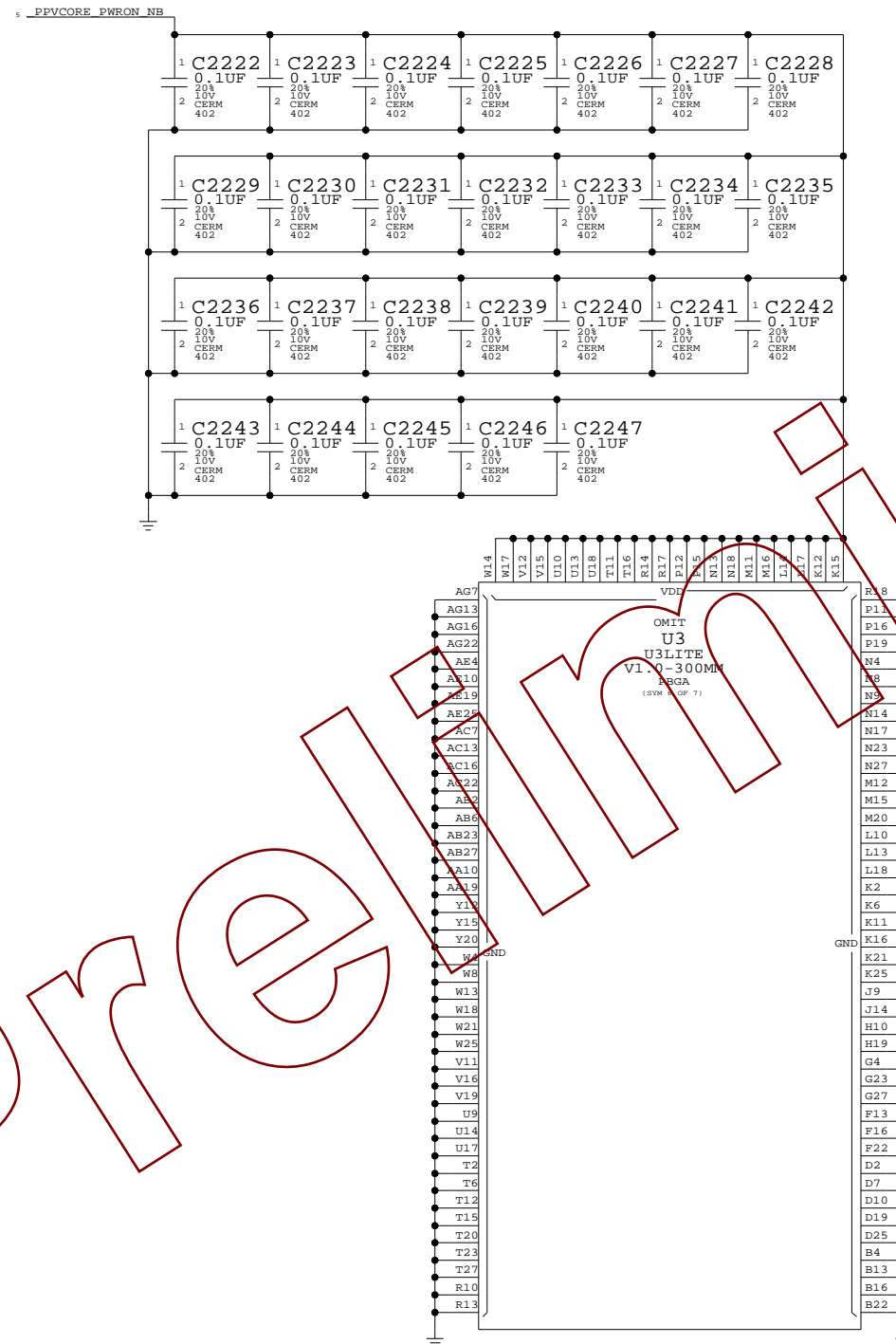
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6532	03
SCALE		SHT	OF
NONE		21	103

# Page Notes

Power aliases required by this page:  
 - \_PPVCORE\_PWRON\_NB

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



Preliminary

Master: Link

## U3Lite Core Power

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE NONE	SHT 22	OF 103



# Page Notes

Power aliases required by this page:

- \_PPPCI164\_PWRON\_SB (to 5V or 3.3V)
- \_PPPCI32\_PWRON\_SB (to 5V or 3.3V)
- \_PP3V3\_PWRON\_SB
- \_PP2V5\_PWRON\_SB
- \_PPVCORE\_PWRON\_SB (1.2V)

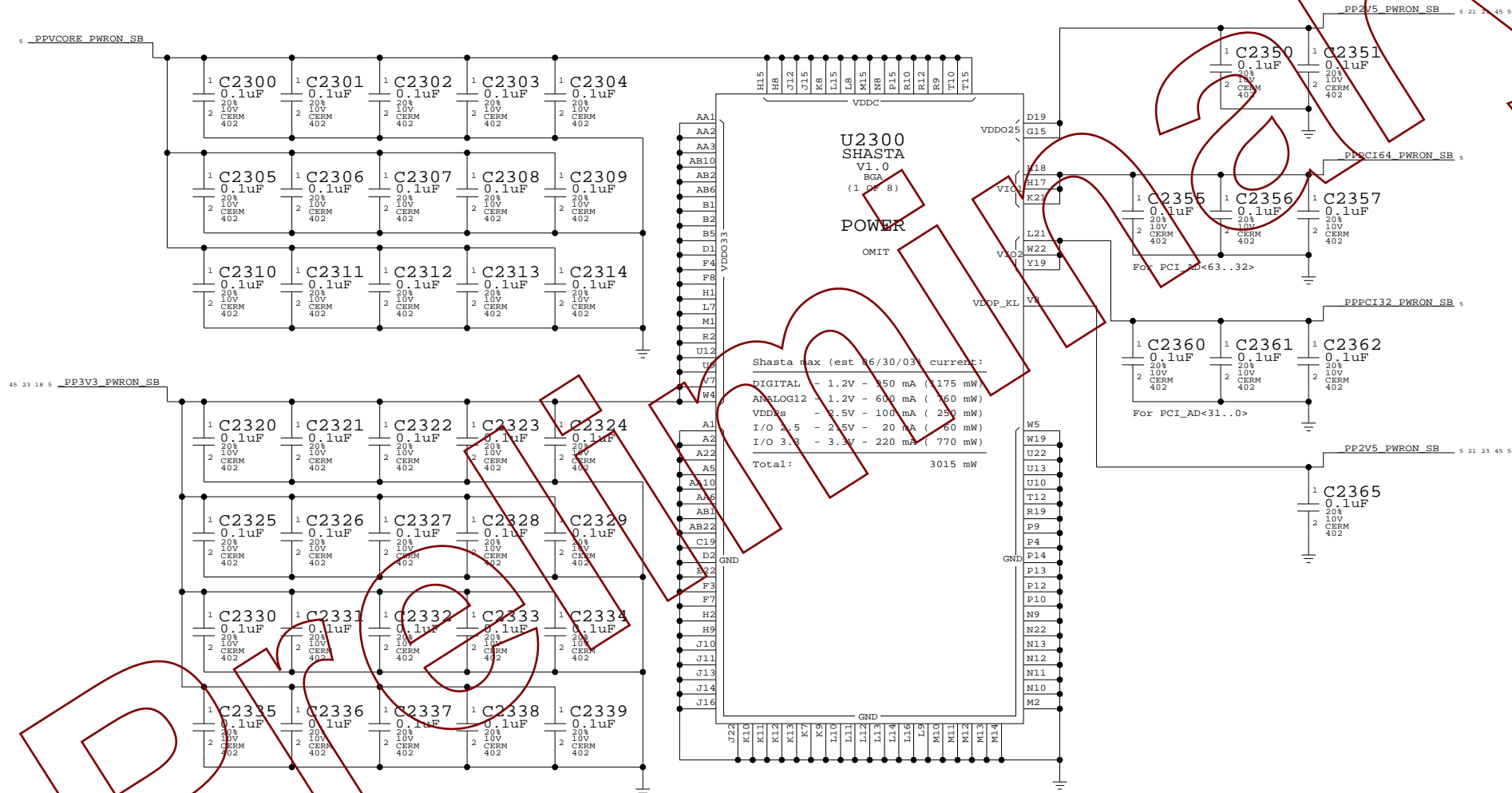
NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect \_PPPCI32\_PWRON\_SB to appropriate PCI bus voltage and \_PPPCI164\_PWRON\_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

**Power Sequencing:**

Must power Shasta VCore rail before any other Shasta supplies.



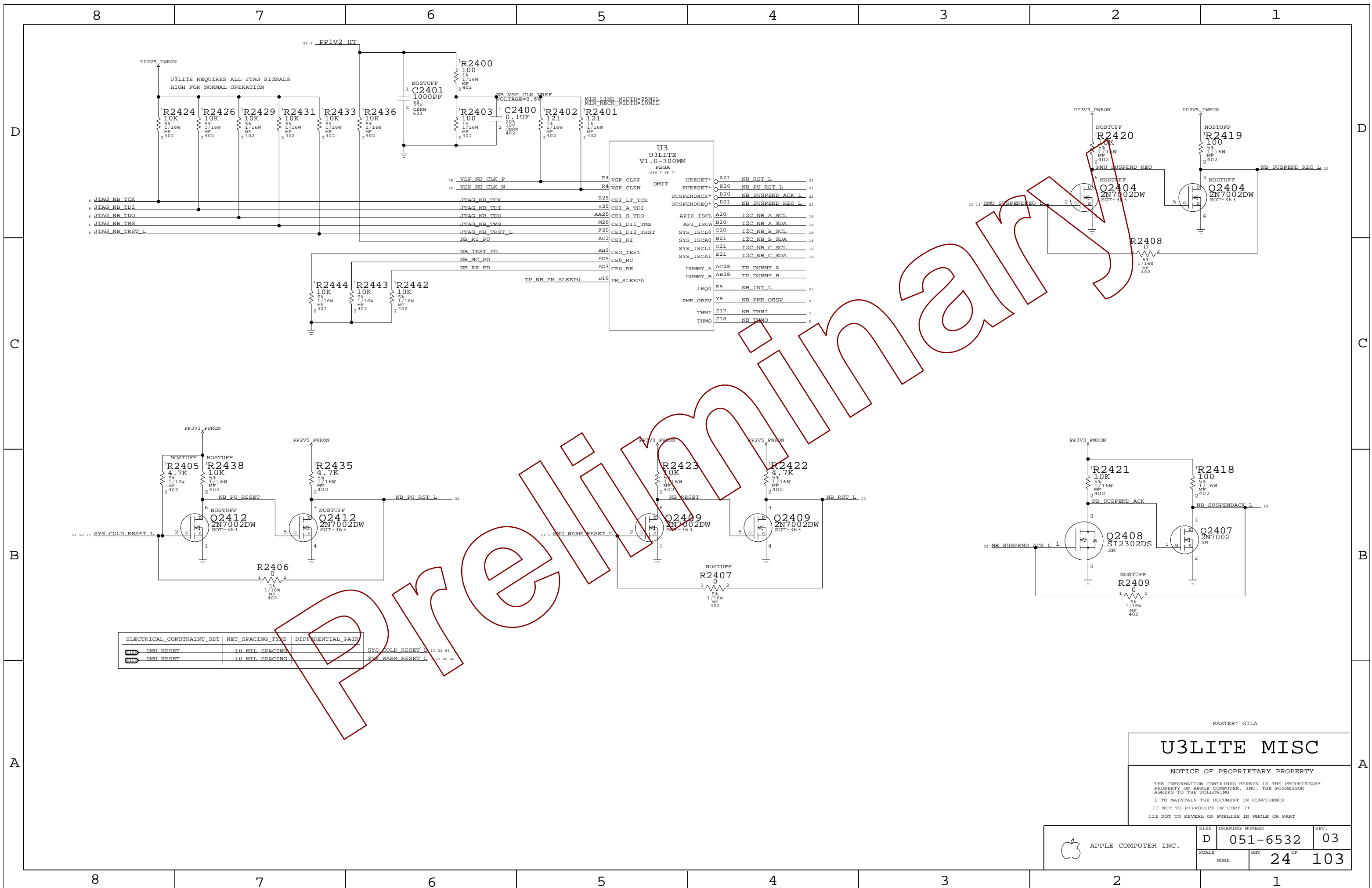
Master: Link

## Shasta Core Power

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6532	03
SCALE		SHT	OF
NONE		23	103



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	10 MIL SPACING	SYS_COLD RESET L 13 22 51
SMU_RESET	10 MIL SPACING	SYS_WARM RESET L 13 23 45 48

MASTER: GILA

**U3LITE MISC**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT		
NONE	24	OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		I2S0_DEV_TO_SB_DTI
I2S0_TO_DEV		I2S0_SB_TO_DEV_DTO
I2S0_TO_DEV	10 MIL SPACING	I2S0_MCLK
I2S0_BIDIR		I2S0_BITCLK
I2S0_BIDIR		I2S0_SYNC
I2S1_TO_SB		I2S1_DEV_TO_SB_DTI
I2S1_TO_DEV		I2S1_SB_TO_DEV_DTO
I2S1_TO_DEV	10 MIL SPACING	I2S1_MCLK
I2S1_BIDIR		I2S1_BITCLK
I2S1_BIDIR		I2S1_SYNC
I2S2_TO_SB		I2S2_DEV_TO_SB_DTI
I2S2_TO_DEV		I2S2_SB_TO_DEV_DTO
I2S2_TO_DEV	10 MIL SPACING	I2S2_MCLK
I2S2_BIDIR		I2S2_BITCLK
I2S2_BIDIR		I2S2_SYNC
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALI
	15 MIL SPACING	SB_CLK18M_XTALO
	15 MIL SPACING	SB_CLK18M_XTALO_R
SB_CLK25M_ATA	15 MIL SPACING	SB_CLK25M_ATA

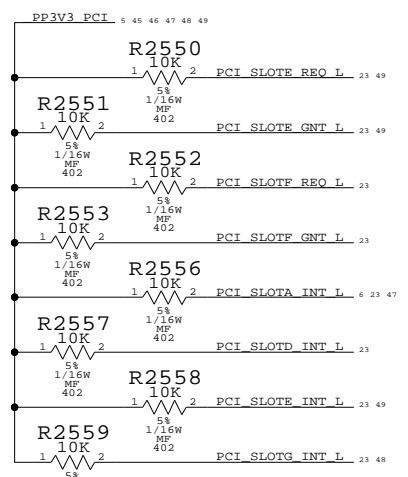
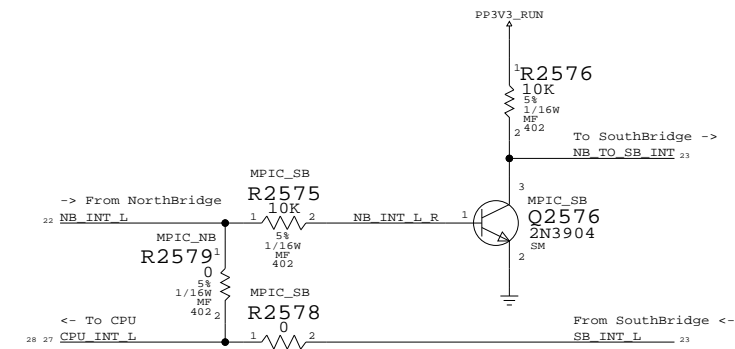
### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PCI  
 - \_PP3V3\_PWRON\_SB  
 - \_PP2V5\_PWRON\_SB  
 - \_PP1V2\_PWRON\_SB

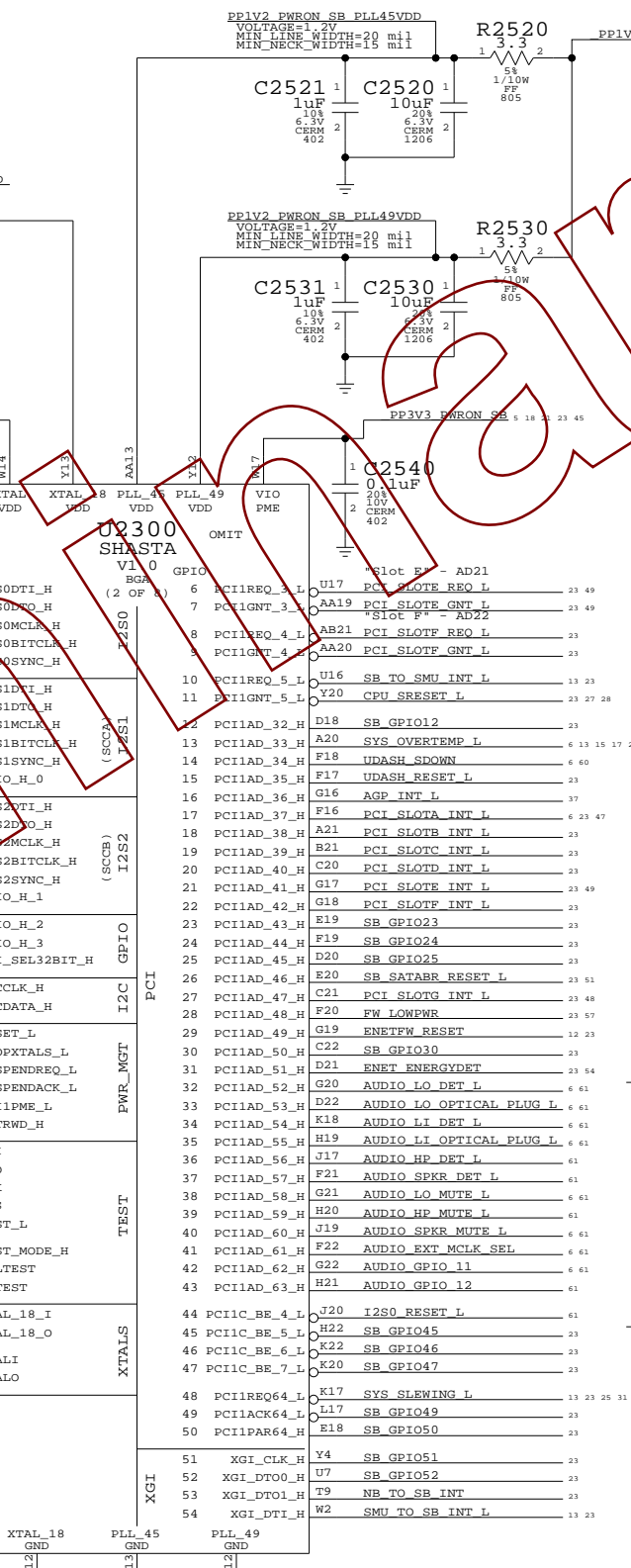
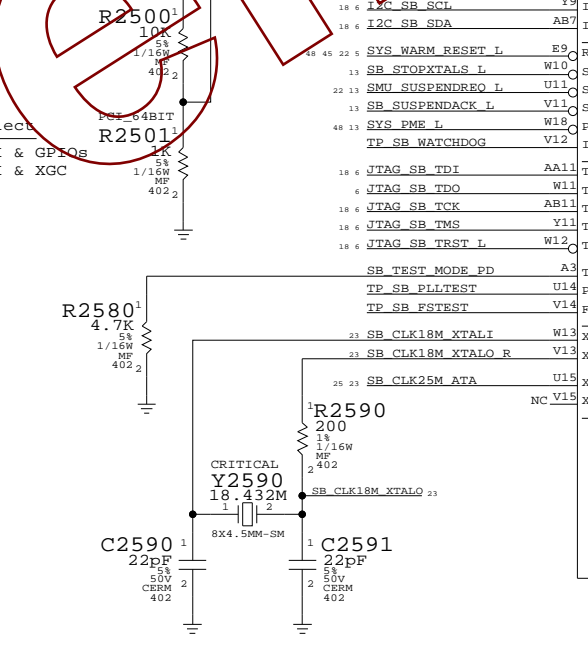
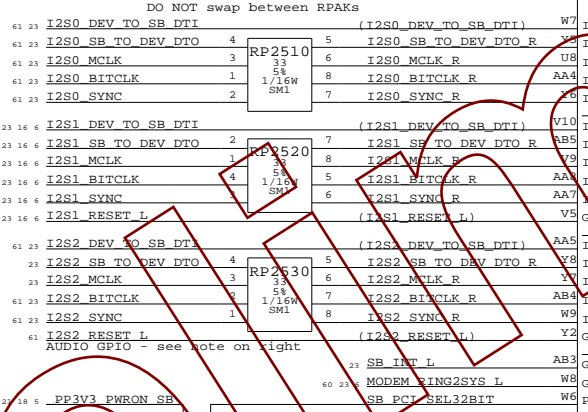
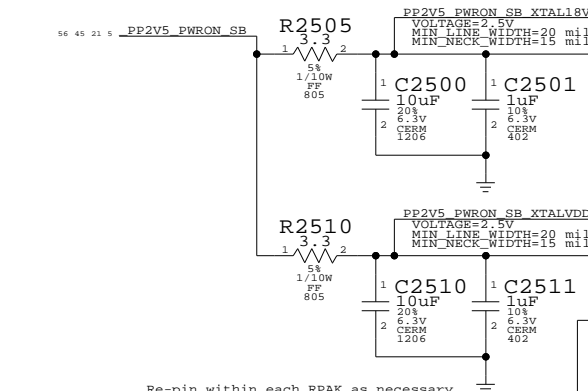
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - PCI\_64BIT  
 Configures Shasta for 64-bit PCI  
 NOTE: XGC required for Shasta GPIOs  
 - MPIC\_NB/MPIC\_SB  
 Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

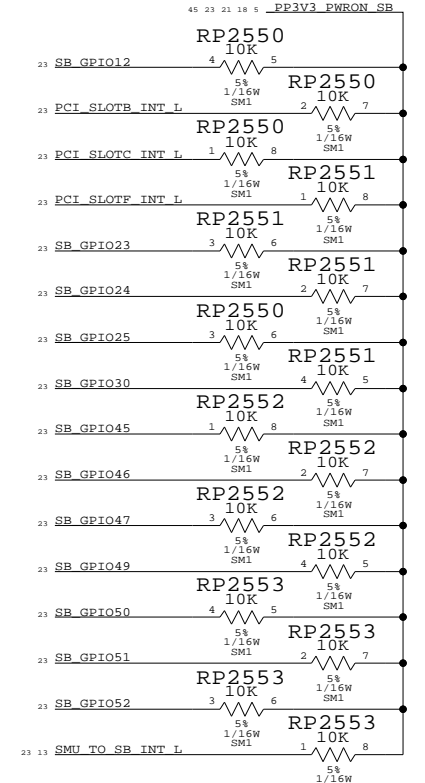
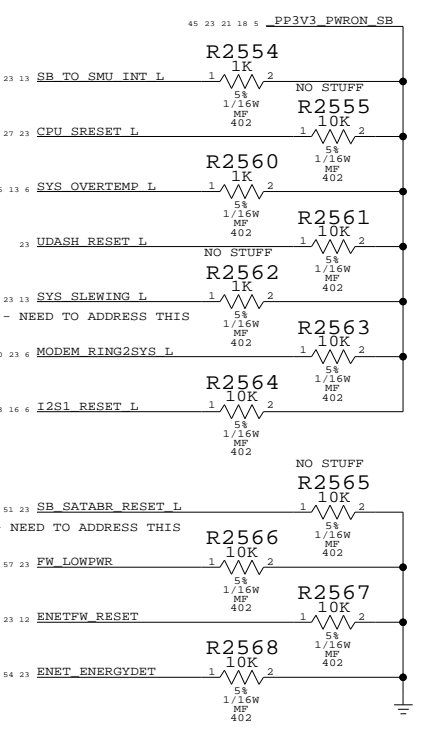
### NorthBridge / SouthBridge MPIC Routing



I2S0: Audio DAC  
 I2S1: Soft Modem  
 I2S2: S/P-DIF



**AUDIO GPIOs**  
 NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.



Master: Link

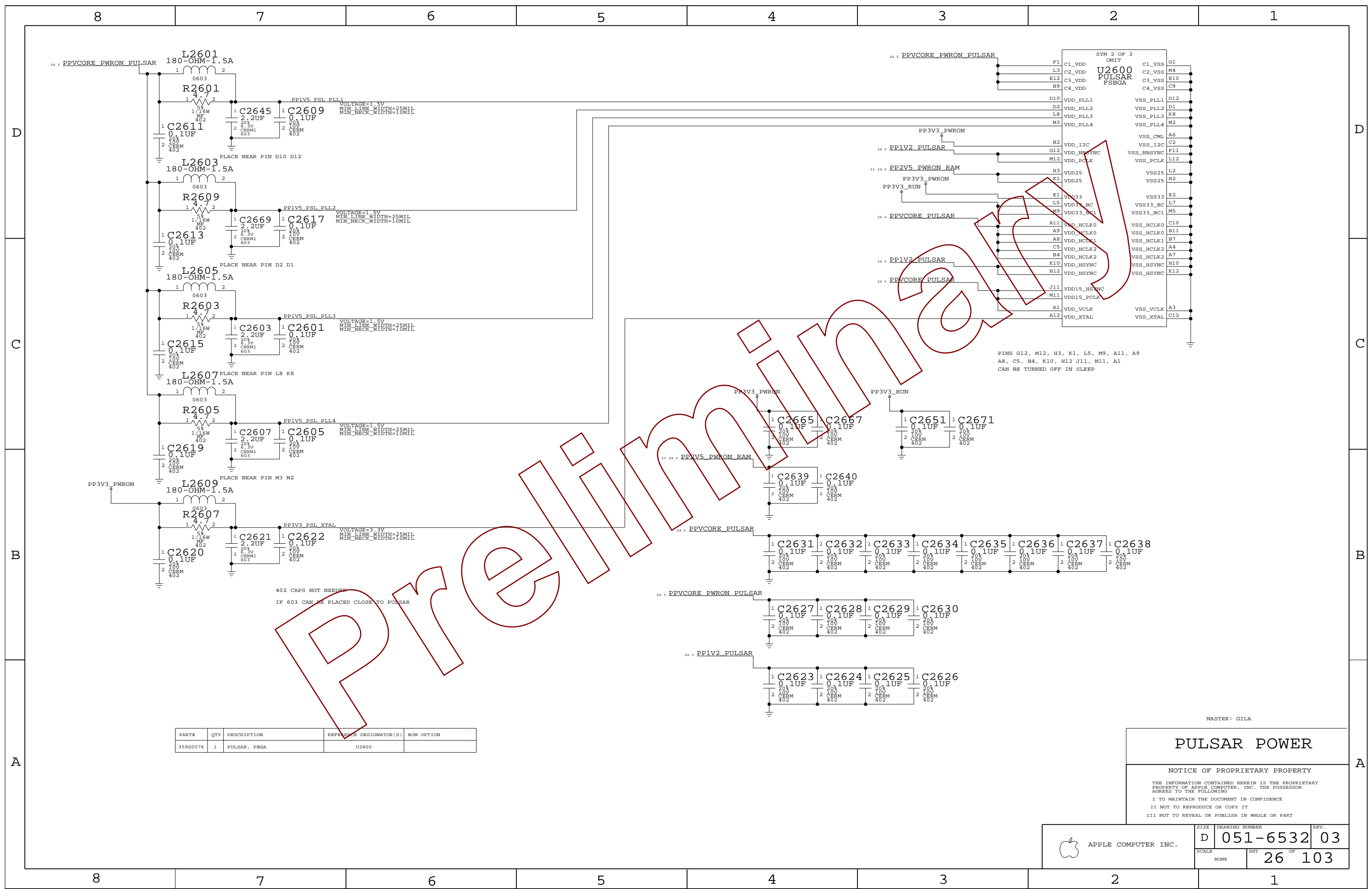
### Shasta Serial / Misc

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE	SHT	25 OF 103
NONE		



APPLE COMPUTER INC.



PINS G12, M12, H3, K1, L5, M9, A11, A9, A8, C5, B4, K10, H12, J11, M11, A1 CAN BE TURNED OFF IN SLEEP

Pre-Release

402 CAPS NOT NEEDED IF 603 CAN BE PLACED CLOSE TO PULSAR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, FBGA	U2600	

MASTER: GILA

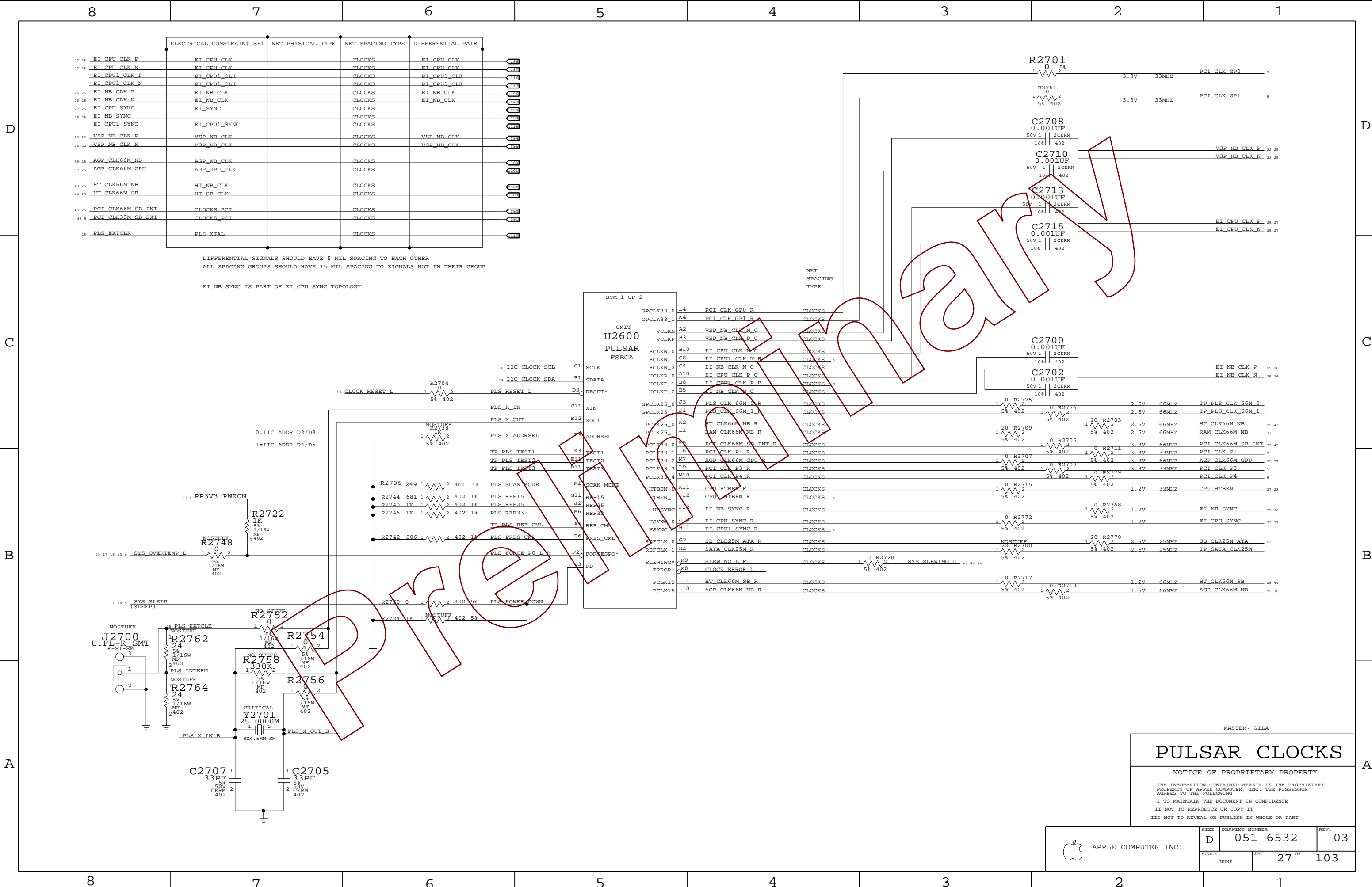
## PULSAR POWER

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	26	103	





	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
27 26	EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
27 25	EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
27 24	EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
27 23	EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
26 25	EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK
26 24	EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK
27 25	EI_CPU_SYNC	EI_SYNC	CLOCKS	
26 25	EI_NB_SYNC		CLOCKS	
26 25	EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	
25 22	VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
25 22	VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
36 25	AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	
37 25	AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	
43 25	HT_CLK66M_NB	HT_NB_CLK	CLOCKS	
44 25	HT_CLK66M_SB	HT_SB_CLK	CLOCKS	
45 25	PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	
45 5	PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	
25	PLS_EXTCLK	PLS_XTAL	CLOCKS	

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER  
 ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI\_NB\_SYNC IS PART OF EI\_CPU\_SYNC TOPOLOGY

SYM 1 OF 2

OMIT U2600 PULSAR FSBGA

GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS
HCLKN_1	C8	EI_CPU1_CLK_N_C	CLOCKS
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS
HCLKP_1	B8	EI_CPU1_CLK_P_C	CLOCKS
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS
PCLK33_0	M6	PCI_CLK66M_SB_INT_R	CLOCKS
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS
HTBEN_1	V12	CPU_HTBEN_R	CLOCKS
HSYNC_0	F12	EI_NB_SYNC_R	CLOCKS
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS
HSYNC_2	H11	EI_CPU1_SYNC_R	CLOCKS
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS
SLEWING_0	K9	SLEWING_L_R	CLOCKS
ERROR_0	M8	CLOCK_ERROR_L	CLOCKS
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS

MASTER: GILA

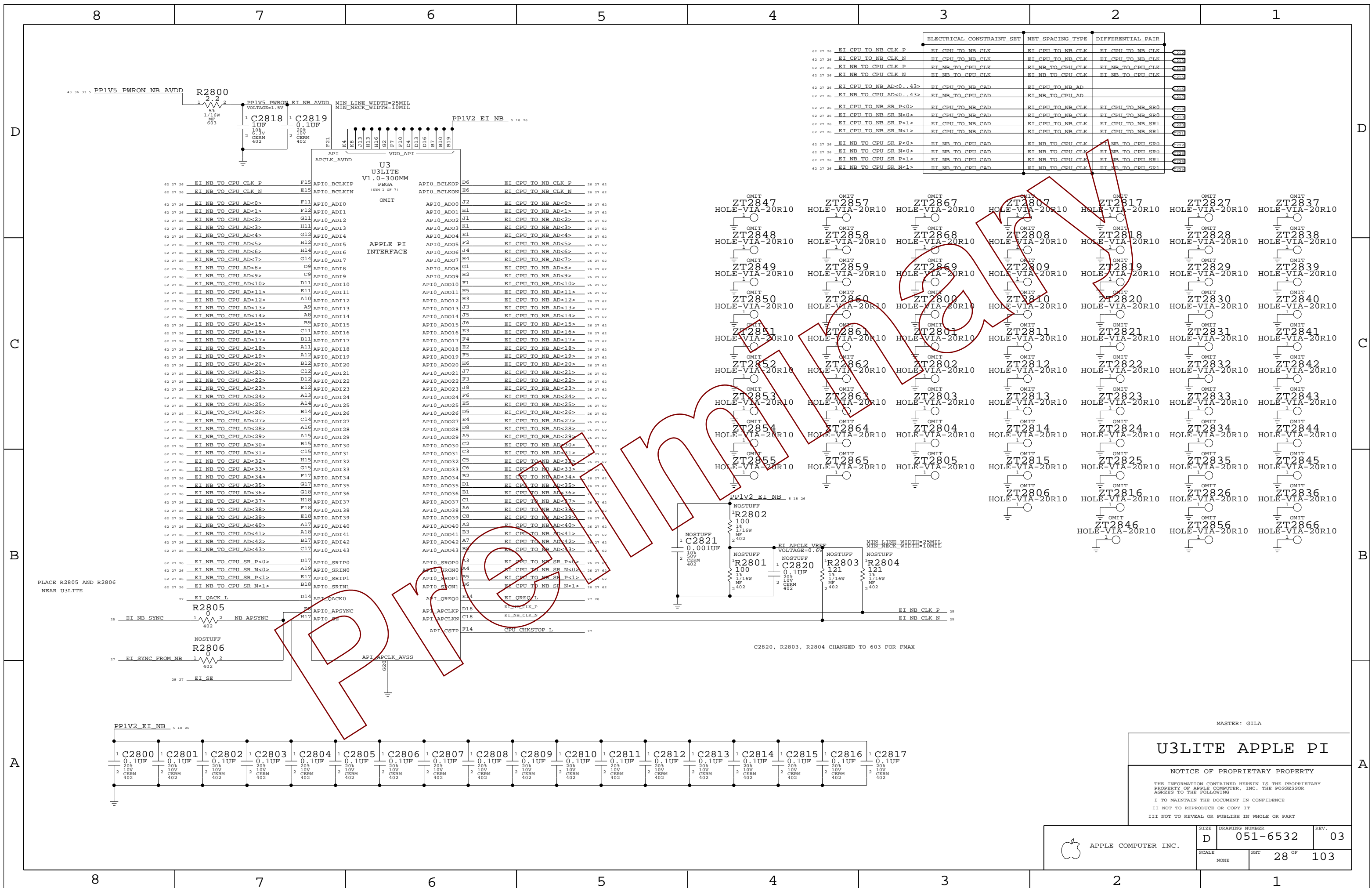
## PULSAR CLOCKS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	27 OF	103
NONE			



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK

PROTECTED  
 CONFIDENTIAL

C2820, R2803, R2804 CHANGED TO 603 FOR FMAX

### U3LITE APPLE PI

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

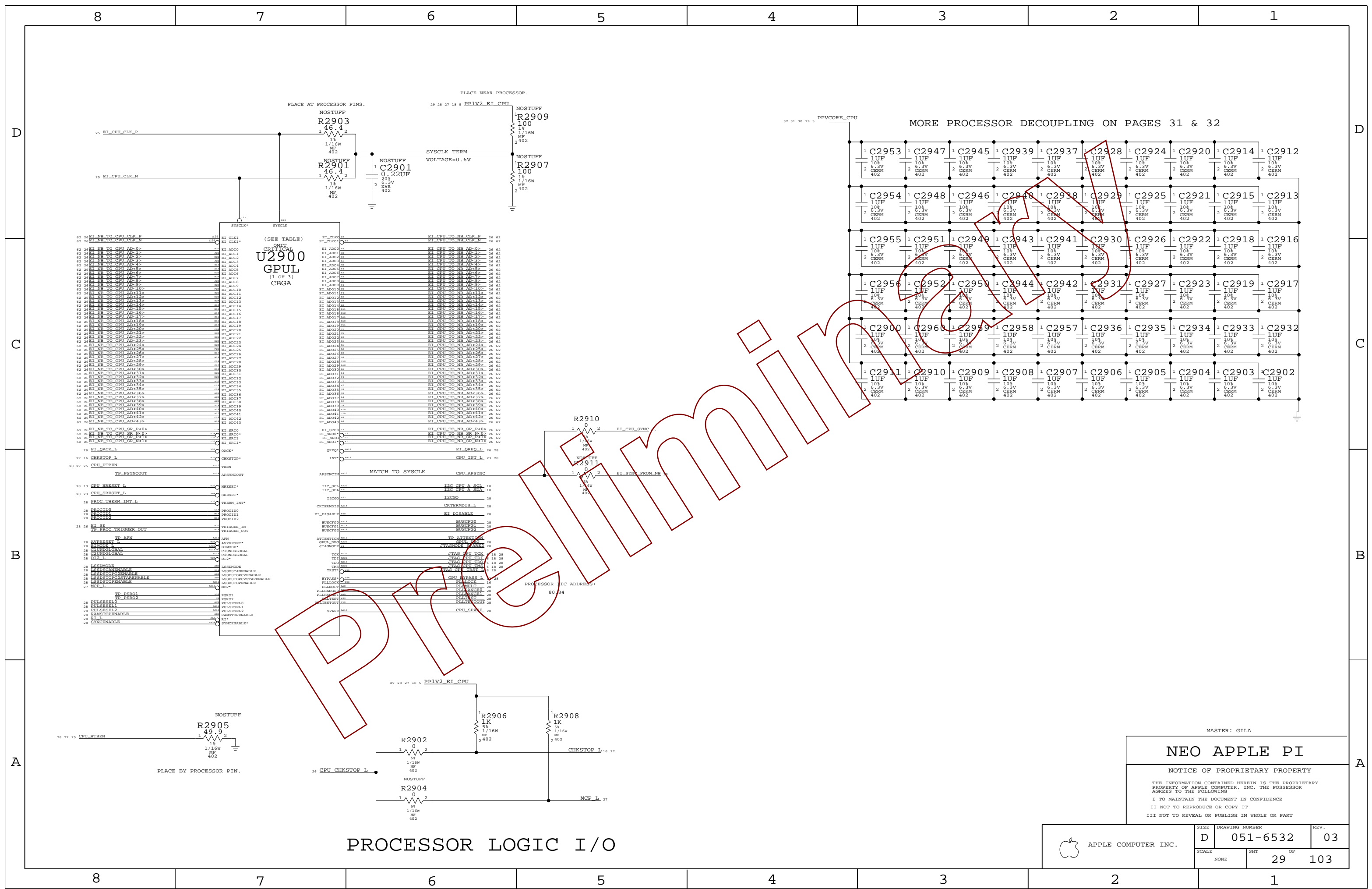
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	28 OF 103	
NONE			

MASTER: GILA





D

D

C

C

B

B

A

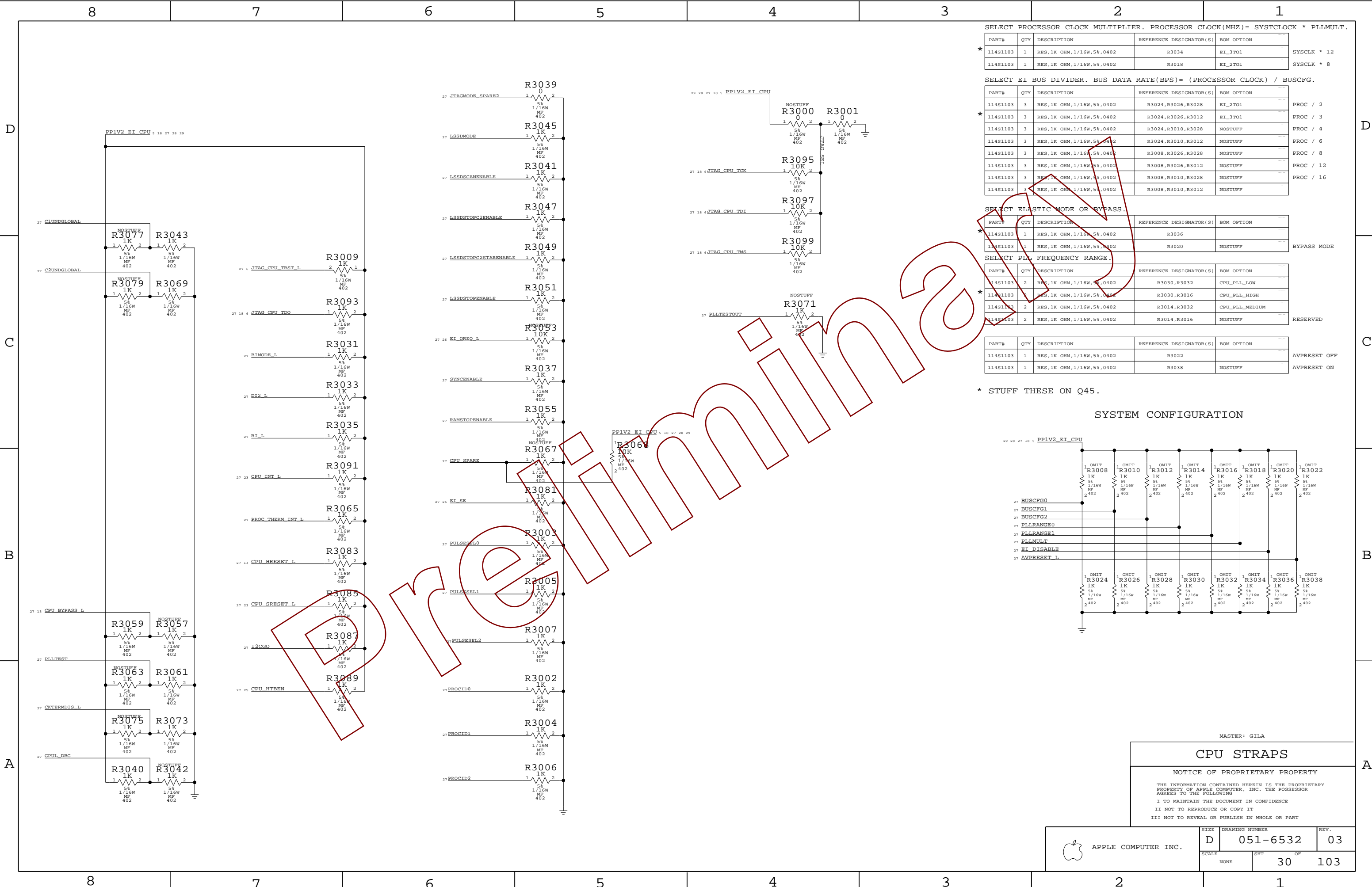
A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6532	03
SCALE		SHT	OF
NONE		29	103

PROCESSOR LOGIC I/O



SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK \* PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3T01
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2T01

SYSCLK \* 12  
SYSCLK \* 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2T01
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3T01
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF

PROC / 2  
PROC / 3  
PROC / 4  
PROC / 6  
PROC / 8  
PROC / 12  
PROC / 16

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF

BYPASS MODE

SELECT PLL FREQUENCY RANGE.

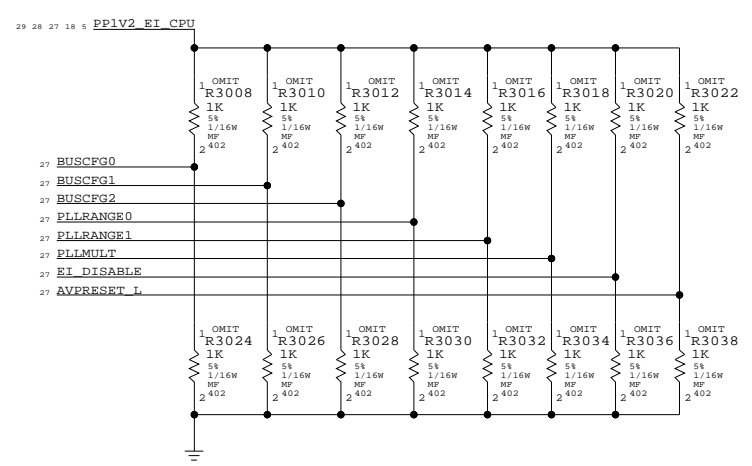
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF

RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022	AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	AVPRESET ON

\* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



MASTER: GILA

**CPU STRAPS**

NOTICE OF PROPRIETARY PROPERTY

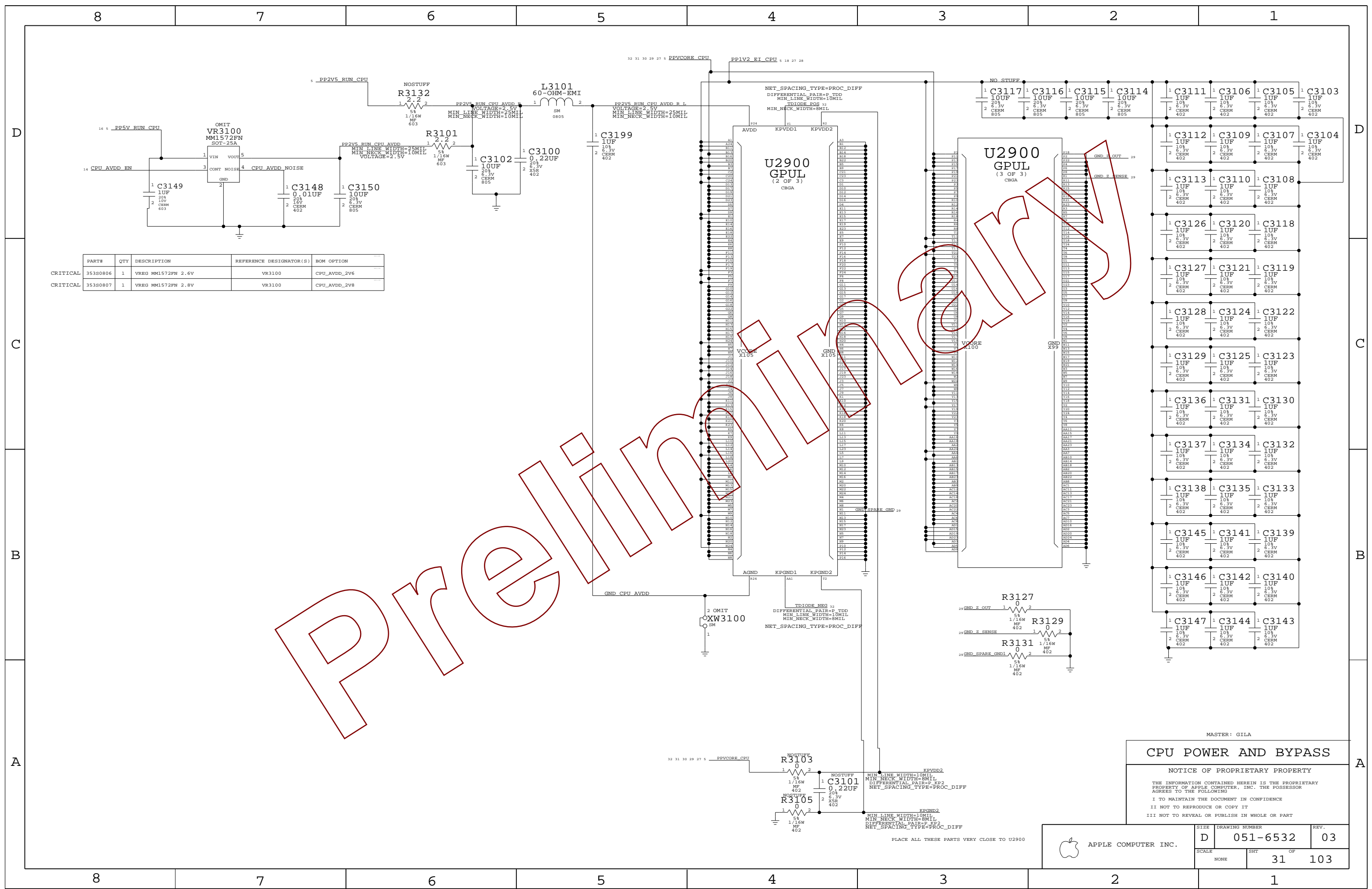
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	OF
		30	103



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572FN 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0807	1	VREG MM1572FN 2.8V	VR3100	CPU_AVDD_2V8

MASTER: GILA

**CPU POWER AND BYPASS**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

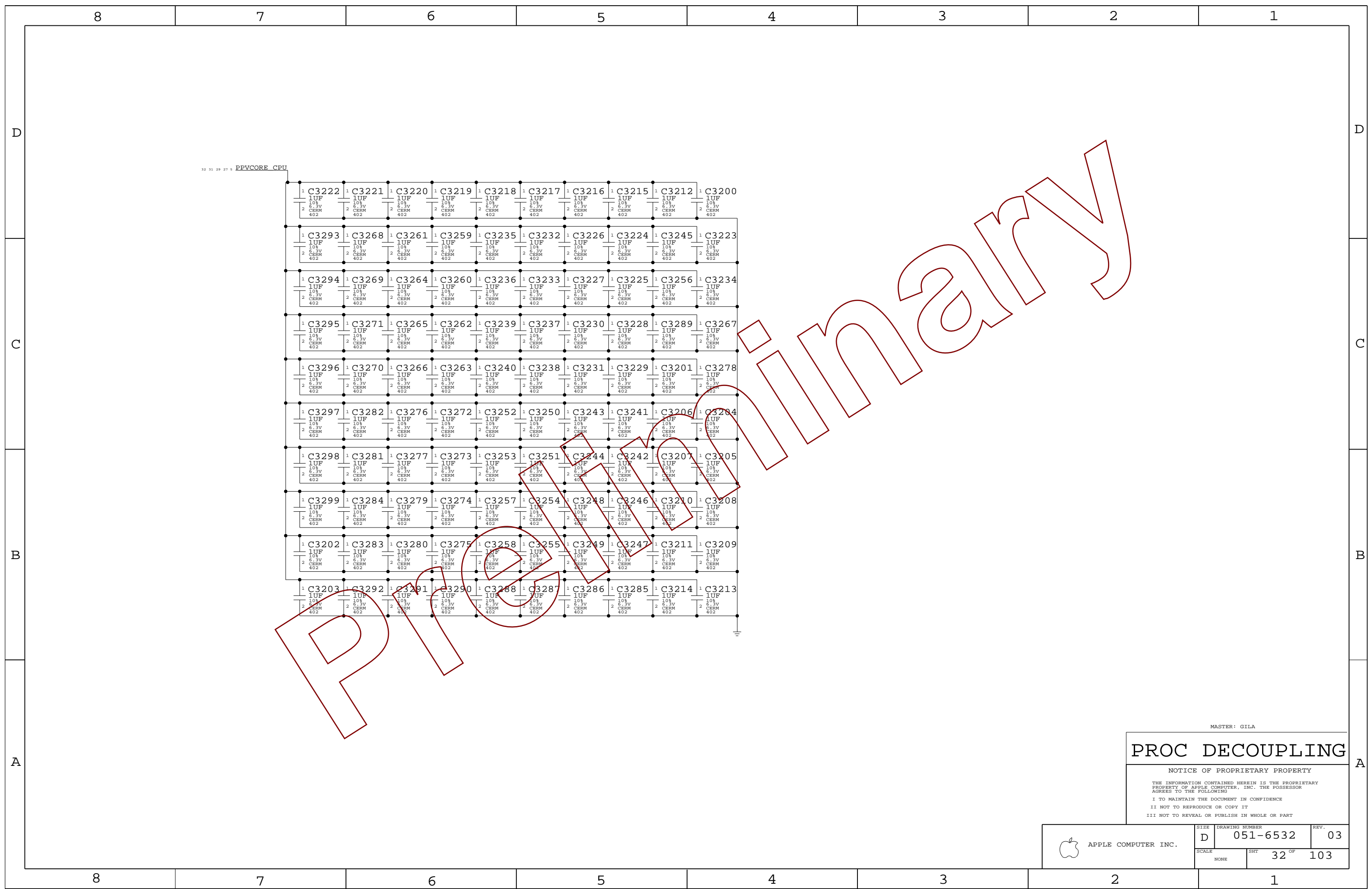
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	OF
		31	103

PLACE ALL THESE PARTS VERY CLOSE TO U2900



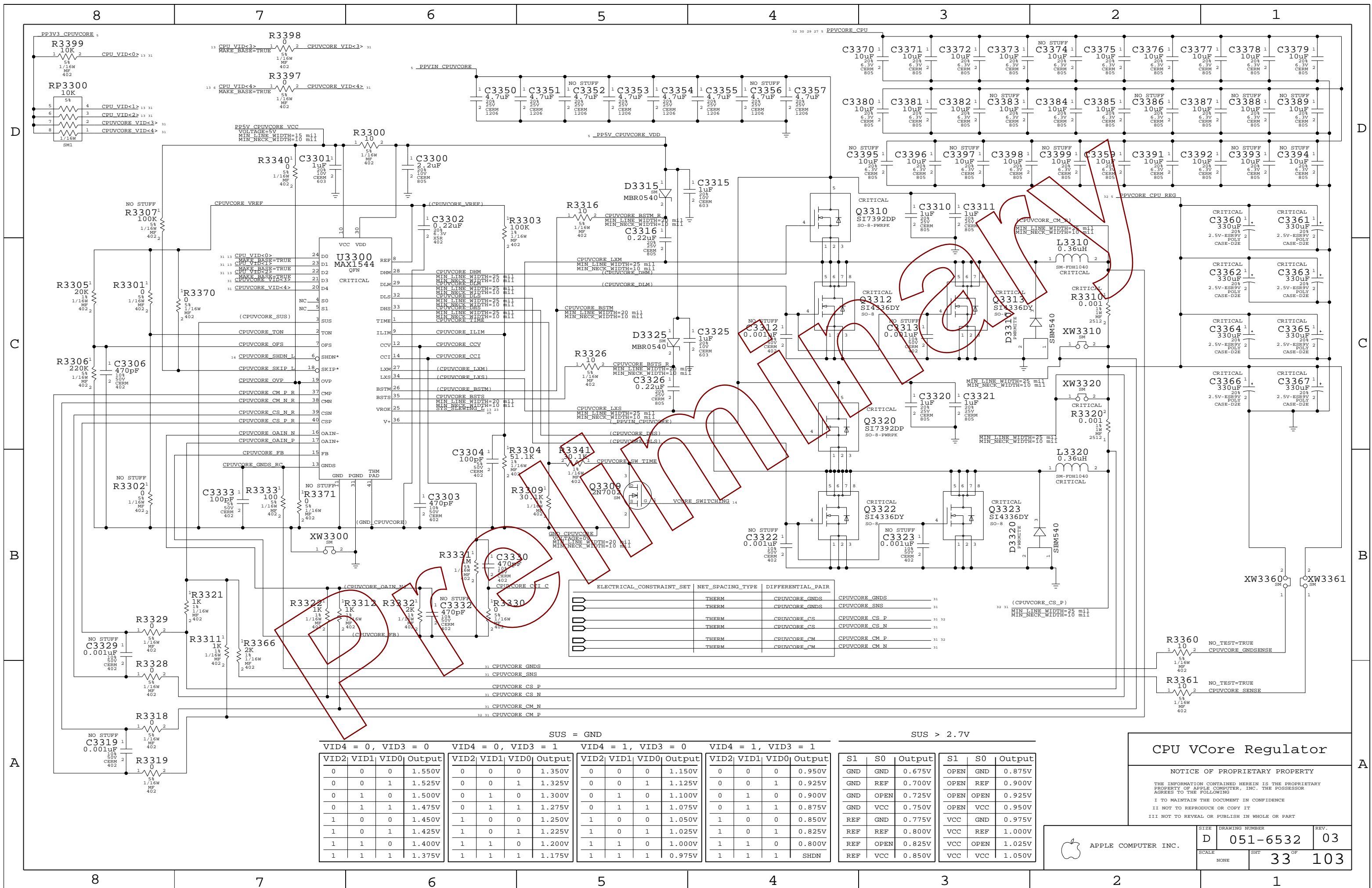
32 31 29 27 5 PPV CORE CPU

MASTER: GILA  
**PROC DECOUPLING**

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	REV.	
NONE	32 OF 103		





ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
THERM	CPUVCORE_GNDS	CPUVCORE_GNDS
THERM	CPUVCORE_GNDS	CPUVCORE_SNS
THERM	CPUVCORE_CS	CPUVCORE_CS_P
THERM	CPUVCORE_CS	CPUVCORE_CS_N
THERM	CPUVCORE_CM	CPUVCORE_CM_P
THERM	CPUVCORE_CM	CPUVCORE_CM_N

VID4 = 0, VID3 = 0					VID4 = 0, VID3 = 1					VID4 = 1, VID3 = 0					VID4 = 1, VID3 = 1					S1 S0 Output			S1 S0 Output		
VID2	VID1	VID0	Output		VID2	VID1	VID0	Output		VID2	VID1	VID0	Output		VID2	VID1	VID0	Output		S1	S0	Output	S1	S0	Output
0	0	0	1.550V		0	0	0	1.350V		0	0	0	1.150V		0	0	0	0.950V		GND	GND	0.675V	OPEN	GND	0.875V
0	0	1	1.525V		0	0	1	1.325V		0	0	1	1.125V		0	0	1	0.925V		GND	REF	0.700V	OPEN	REF	0.900V
0	1	0	1.500V		0	1	0	1.300V		0	1	0	1.100V		0	1	0	0.900V		GND	OPEN	0.725V	OPEN	OPEN	0.925V
0	1	1	1.475V		0	1	1	1.275V		0	1	1	1.075V		0	1	1	0.875V		GND	VCC	0.750V	OPEN	VCC	0.950V
1	0	0	1.450V		1	0	0	1.250V		1	0	0	1.050V		1	0	0	0.850V		REF	GND	0.775V	VCC	GND	0.975V
1	0	1	1.425V		1	0	1	1.225V		1	0	1	1.025V		1	0	1	0.825V		REF	REF	0.800V	VCC	REF	1.000V
1	1	0	1.400V		1	1	0	1.200V		1	1	0	1.000V		1	1	0	0.800V		REF	OPEN	0.825V	VCC	OPEN	1.025V
1	1	1	1.375V		1	1	1	1.175V		1	1	1	0.975V		1	1	1	SHDN		REF	VCC	0.850V	VCC	VCC	1.050V

### CPU VCore Regulator

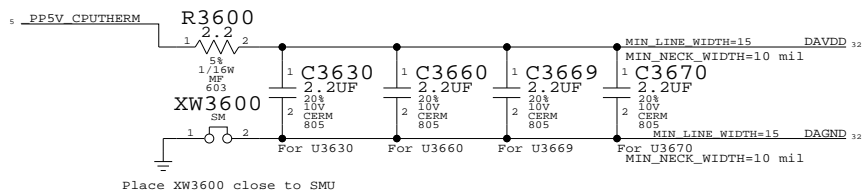
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE	SHT	OF
NONE	33	103

APPLE COMPUTER INC.

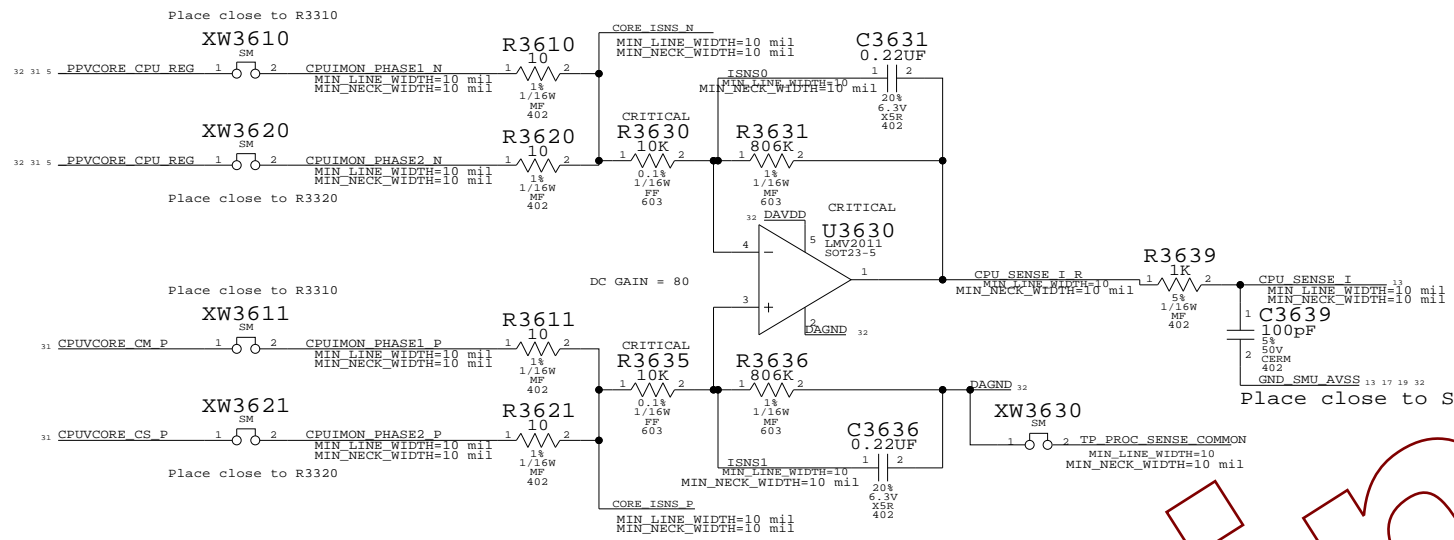


### CPU Current Monitoring

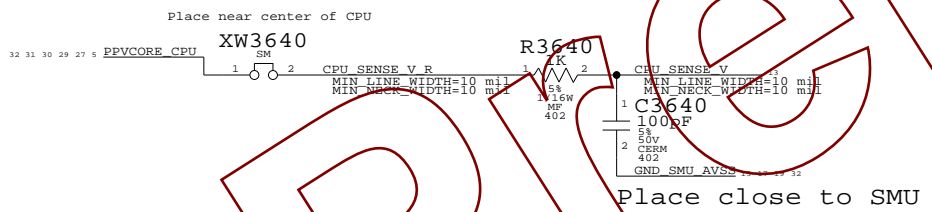
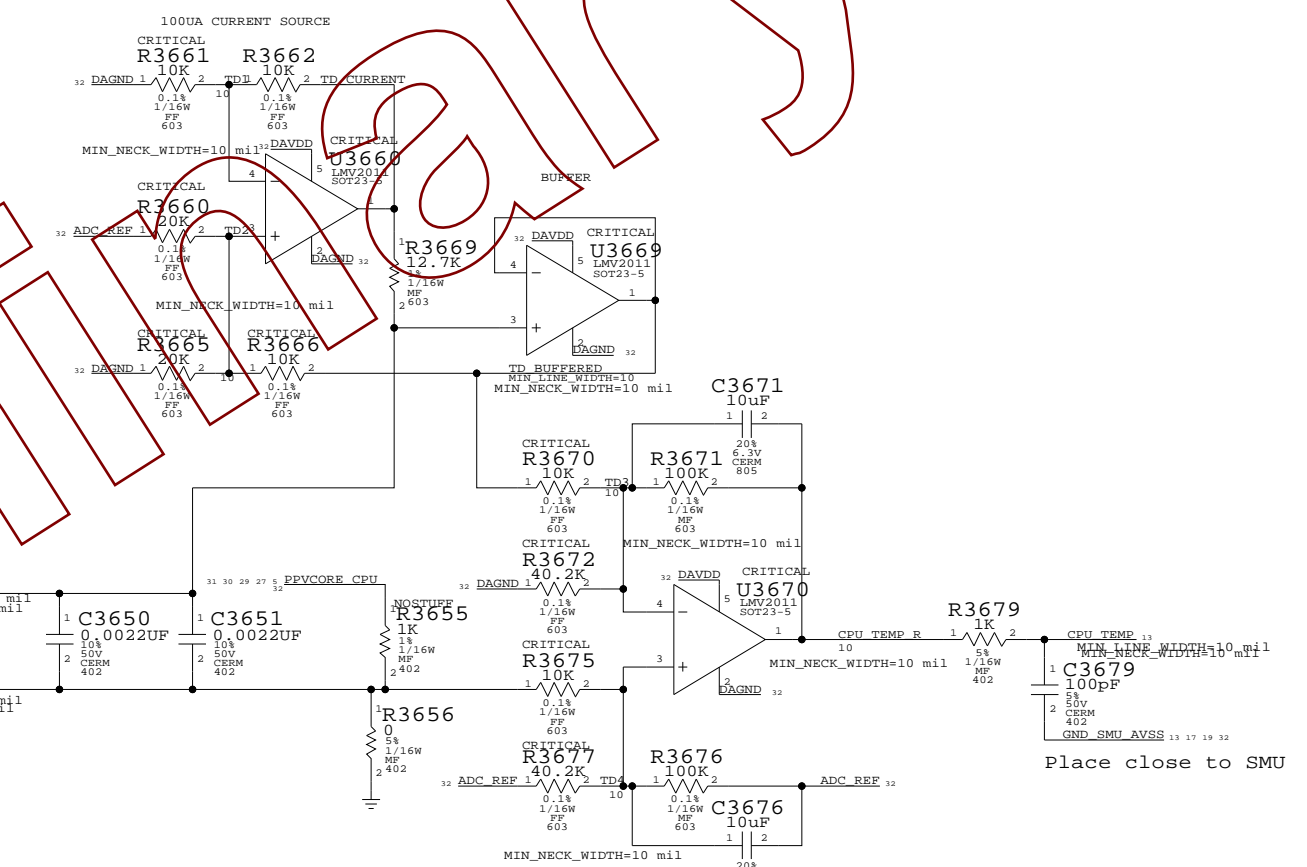
Place close to CPU Power Supply

### CPU Thermal Diode Circuit

Place close to CPU

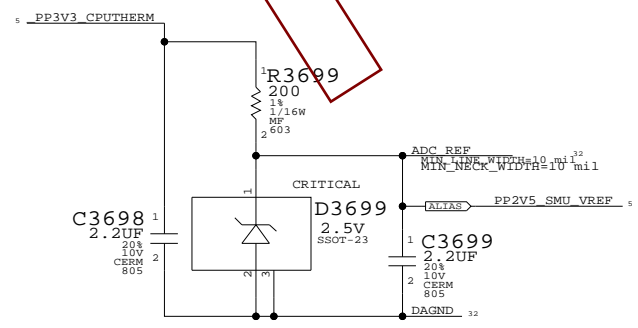


### CPU Voltage Monitoring



### SMU Voltage Reference

Place close to SMU

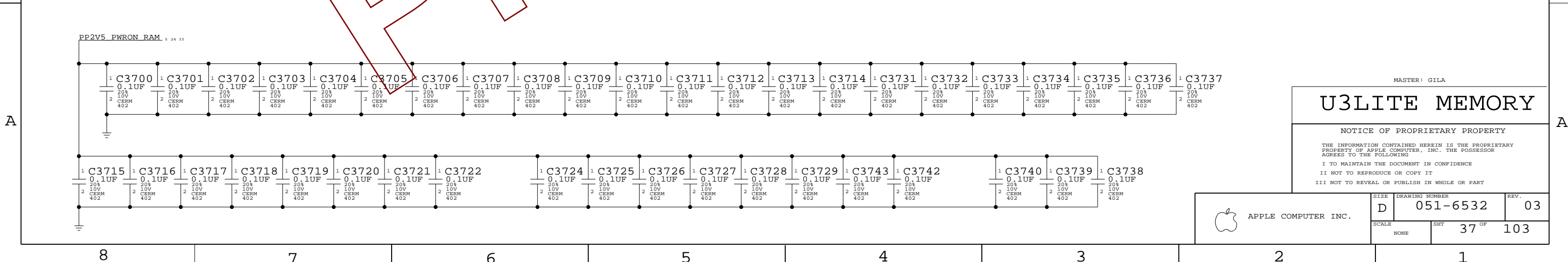
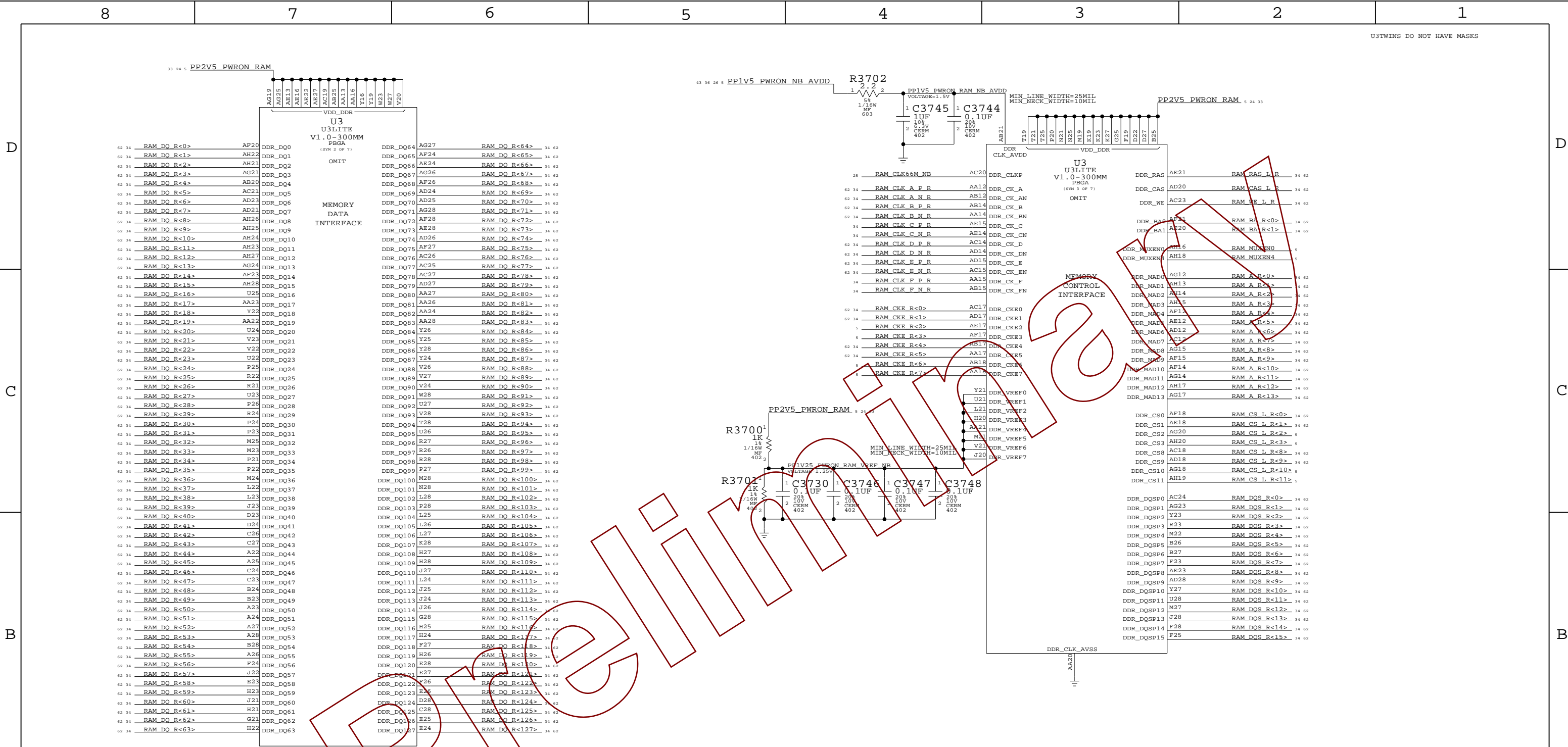


### CPU Temp Monitoring

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	36 OF 103





MASTER: GILA

## U3LITE MEMORY

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-6532</b>	REV. <b>03</b>
	SCALE NONE	SHIT 37 OF 103	

# Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

NOTE: SO-DIMMs only use 2 of the 3 clocks provided for each DIMM module. Unused clocks renamed below.

33	RAM CLK C P R	ALIAS	TP RAM CLK C P	MAKE_BASE=TRUE
33	RAM CLK C N R	ALIAS	TP RAM CLK C N	MAKE_BASE=TRUE
33	RAM CLK F P R	ALIAS	TP RAM CLK F P	MAKE_BASE=TRUE
33	RAM CLK F N R	ALIAS	TP RAM CLK F N	MAKE_BASE=TRUE

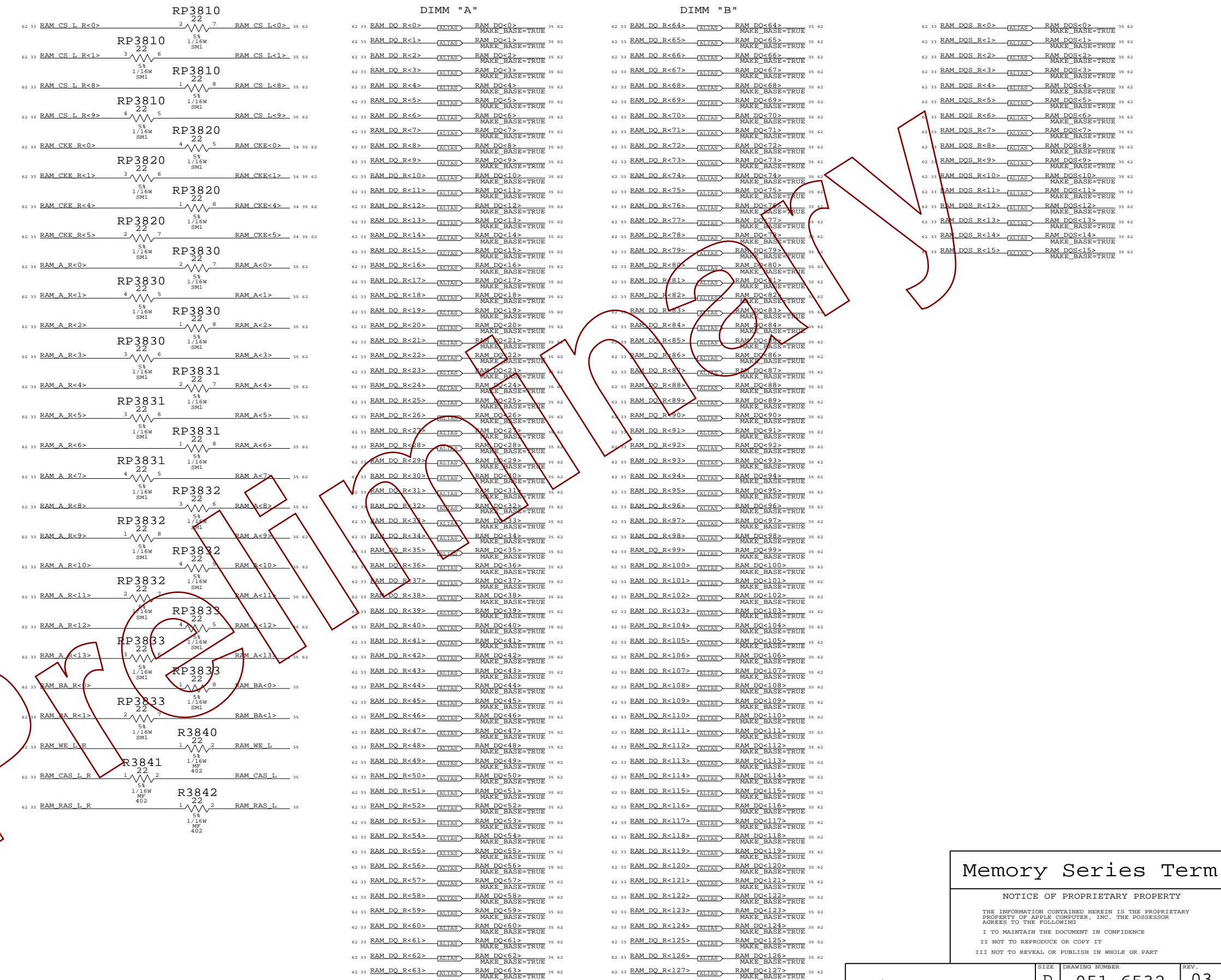
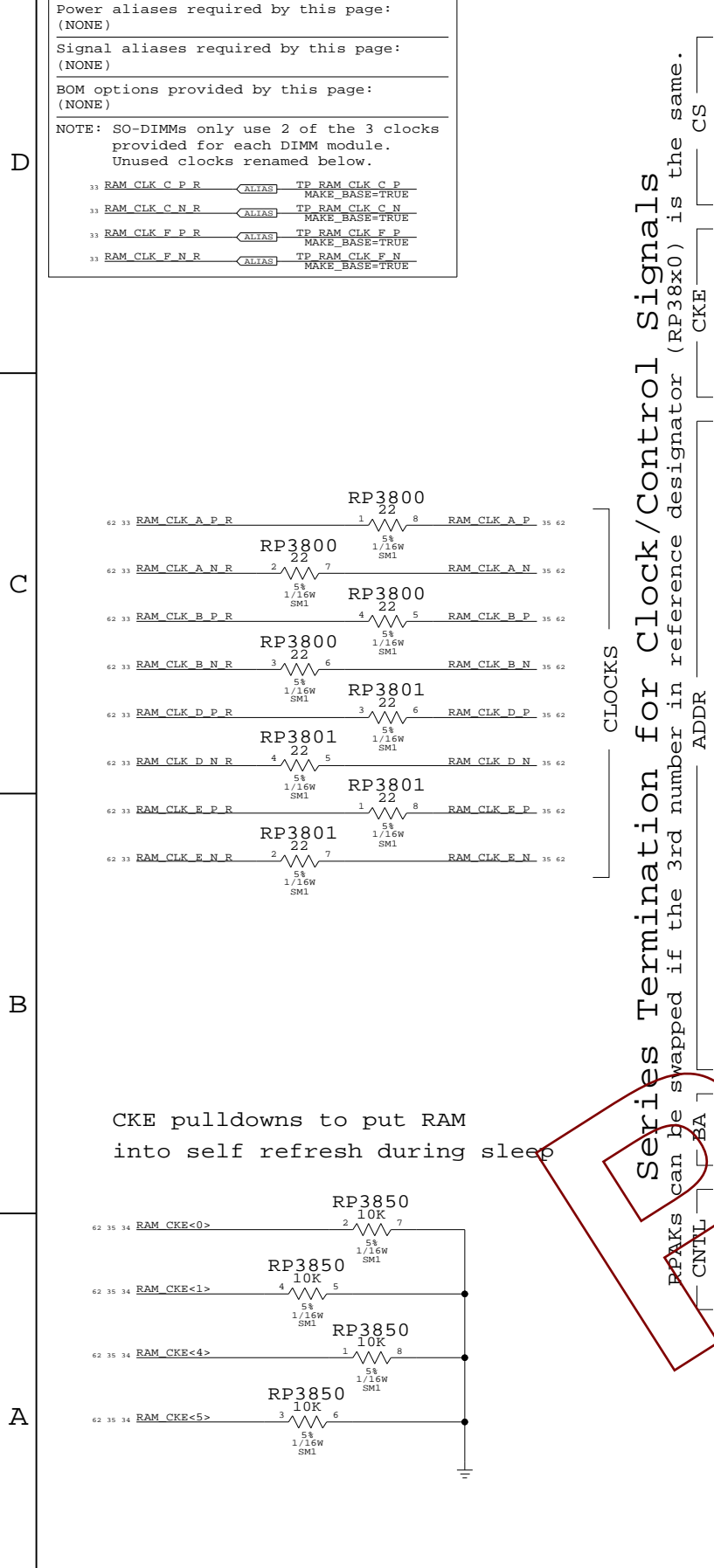
No series termination on data signals

No series termination on strobe signals

Series Termination for Clock/Control Signals  
RPAKs can be swapped if the 3rd number in reference designator (RP38x0) is the same.

D  
C  
B  
A

D  
C  
B  
A



**Memory Series Term**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	38 OF	103
NONE			

# Page Notes

Power aliases required by this page:  
 - \_PP2V5\_PWRON\_DIMM  
 - \_PPSPD\_DIMM (2.5V - 3.3V)

Signal aliases required by this page:  
 (NONE)

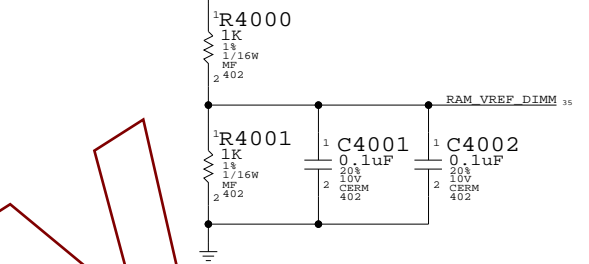
BOM options provided by this page:  
 (NONE)

Slot "A"  
 Standard  
 Factory Slot

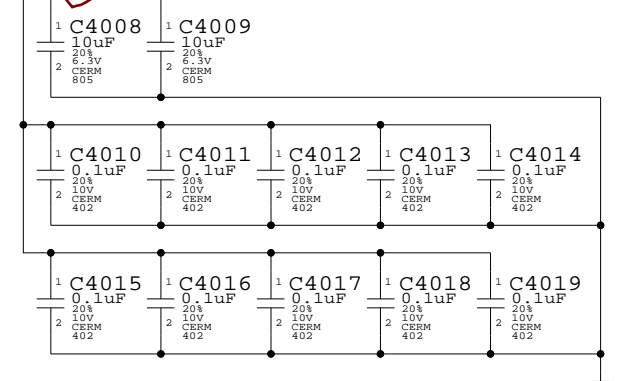
Slot "B"  
 Reversed  
 Customer Slot

## DDR VRef

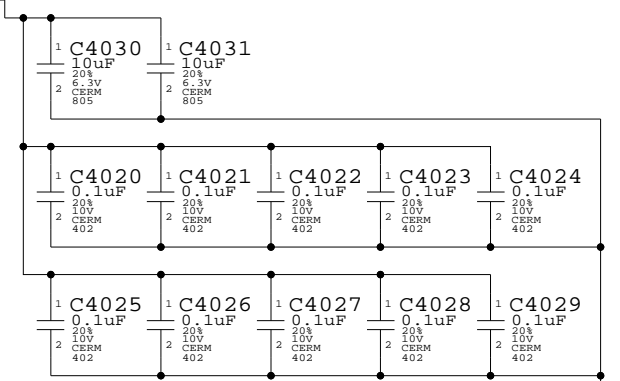
One 0.1uF per connector



## DDR Bypass Caps (For return current) Slot "A"



## Slot "B"

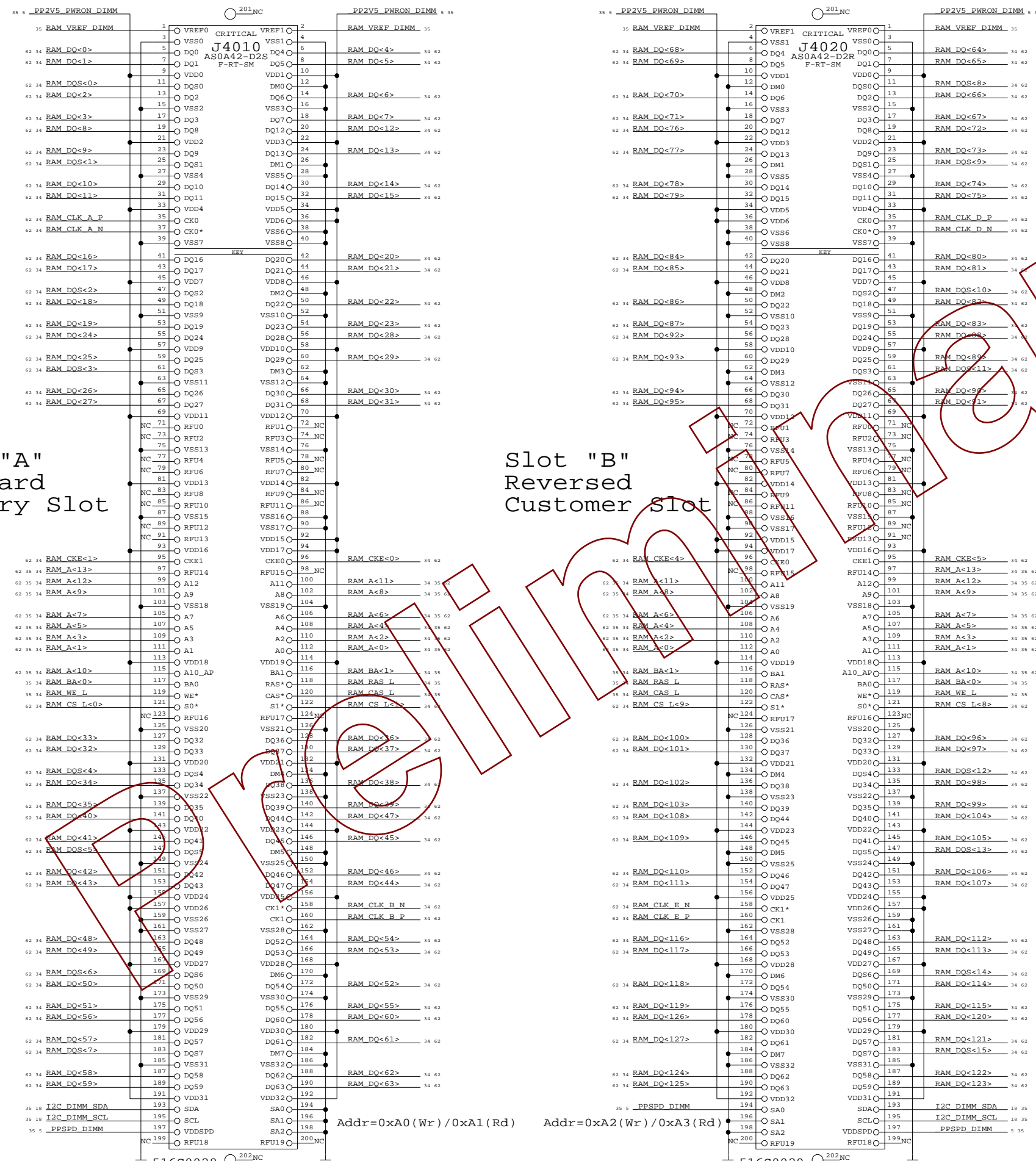


## DDR SODIMM CONNS

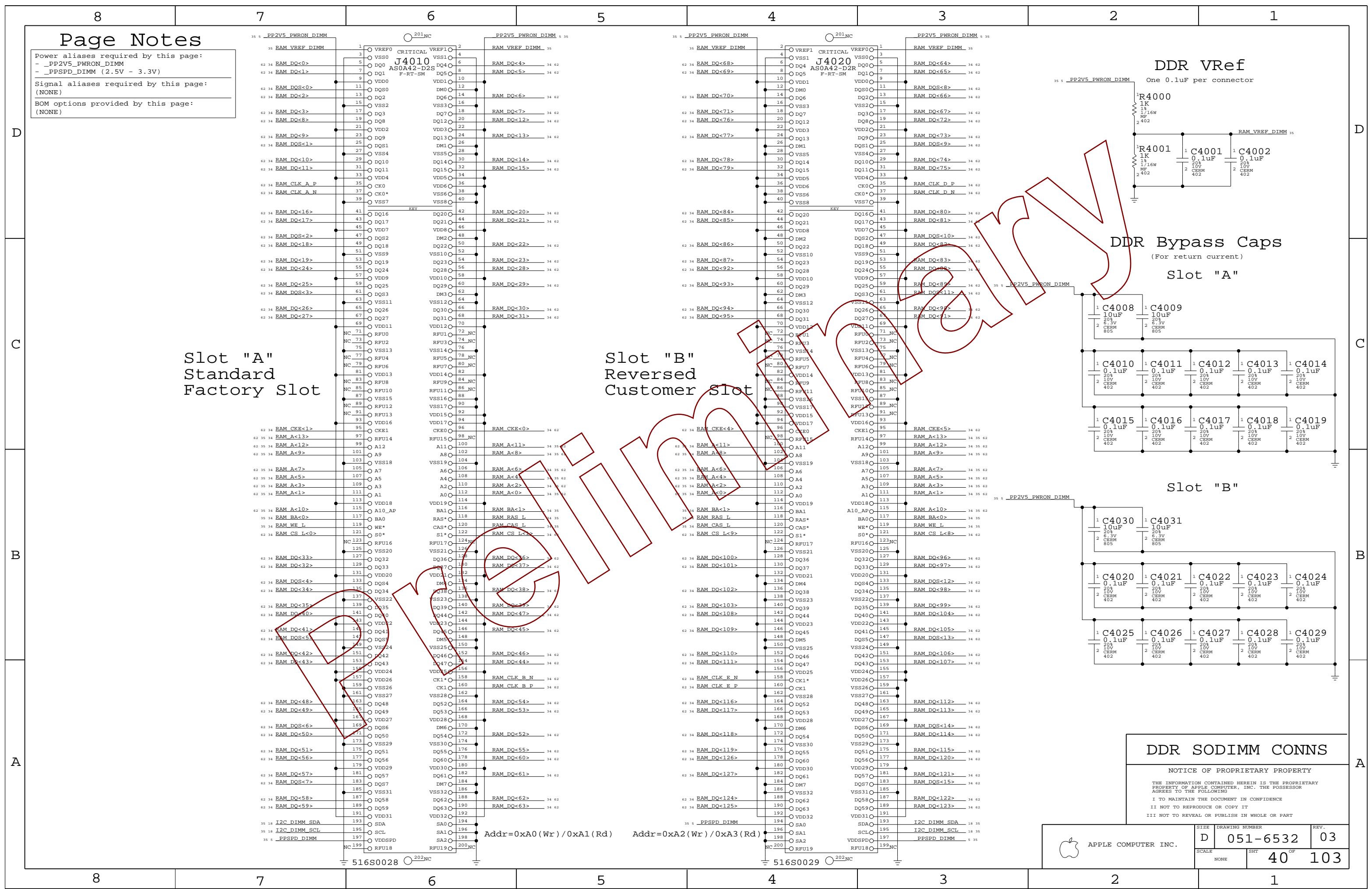
### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

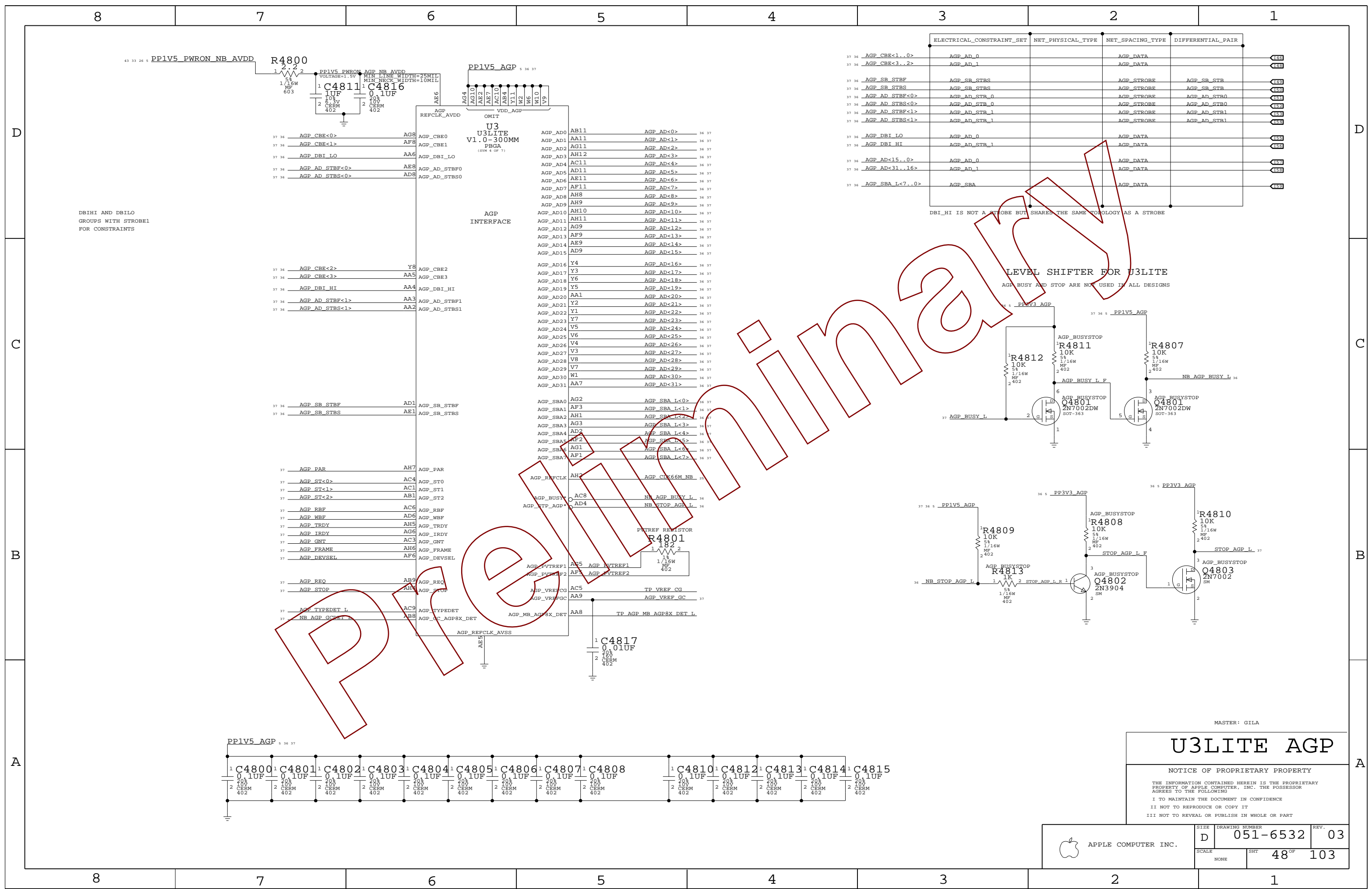
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHEET	OF	
NONE	40	103	



Addr=0xA0 (Wr) / 0xA1 (Rd)      Addr=0xA2 (Wr) / 0xA3 (Rd)







MASTER: GILA

**U3LITE AGP**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

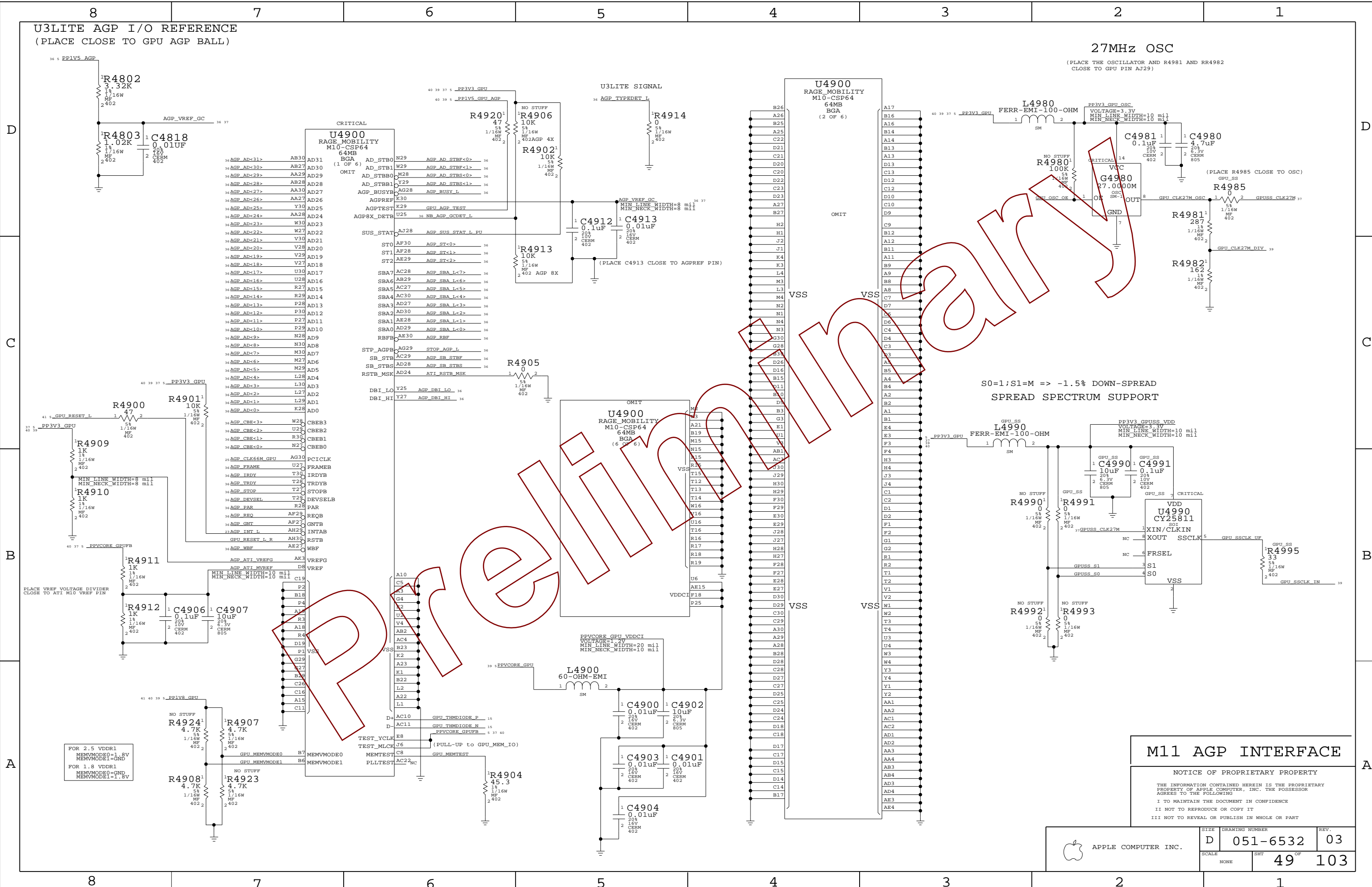
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	48" OF 103	
NONE			

# U3LITE AGP I/O REFERENCE (PLACE CLOSE TO GPU AGP BALL)

# 27MHz OSC

(PLACE THE OSCILLATOR AND R4981 AND RR4982 CLOSE TO GPU PIN AJ29)



CRITICAL

AGP AD<31>	AB30	AD31	BGA AD_STB0	N29	AGP_AD_STBF<0>	36
AGP AD<30>	AB27	AD30	AD_STB1	W29	AGP_AD_STBF<1>	36
AGP AD<29>	AA29	AD29	AD_STB0	M28	AGP_AD_STBF<0>	36
AGP AD<28>	AB28	AD28	AD_STB1	Y29	AGP_AD_STBF<1>	36
AGP AD<27>	AA30	AD27	AGP_BUSYB	AG28	AGP_BUSY L	36
AGP AD<26>	AA27	AD26	AGPREF	K30		
AGP AD<25>	Y30	AD25	AGPTEST	K29	GPU_AGP_TEST	
AGP AD<24>	AA28	AD24	AGPBX_DET	U25	NB_AGP_GCDET L	
AGP AD<23>	W30	AD23	SUS_STAT	AJ28	AGP_SUS_STAT L PU	
AGP AD<22>	W27	AD22	ST0	AF30	AGP_ST<0>	36
AGP AD<21>	V30	AD21	ST1	AF28	AGP_ST<1>	36
AGP AD<20>	V28	AD20	ST2	AE29	AGP_ST<2>	36
AGP AD<19>	V29	AD19	SBA7	AC28	AGP_SBA L<7>	36
AGP AD<18>	V27	AD18	SBA6	AB29	AGP_SBA L<6>	36
AGP AD<17>	U30	AD17	SBA5	AC27	AGP_SBA L<5>	36
AGP AD<16>	U28	AD16	SBA4	AC30	AGP_SBA L<4>	36
AGP AD<15>	R27	AD15	SBA3	AD27	AGP_SBA L<3>	36
AGP AD<14>	R29	AD14	SBA2	AD30	AGP_SBA L<2>	36
AGP AD<13>	P28	AD13	SBA1	AE28	AGP_SBA L<1>	36
AGP AD<12>	P30	AD12	SBA0	AD29	AGP_SBA L<0>	36
AGP AD<11>	P27	AD11	RBFB	AE30	AGP_EBF	36
AGP AD<10>	P29	AD10	STP_AGPB	AG29	STOP_AGP L	36
AGP AD<9>	N28	AD9	SB_STB	AC29	AGP_SB_STBF	36
AGP AD<8>	N30	AD8	SB_STBS	AD28	AGP_SB_STBS	36
AGP AD<7>	M30	AD7	RSTB_MSK	AD24	ATI_RSTB_MSK	36
AGP AD<6>	M27	AD6				
AGP AD<5>	M29	AD5				
AGP AD<4>	L28	AD4				
AGP AD<3>	L30	AD3				
AGP AD<2>	L27	AD2				
AGP AD<1>	L29	AD1				
AGP AD<0>	K28	AD0				
AGP CBE<3>	W28	CBEB3				
AGP CBE<2>	U29	CBEB2				
AGP CBE<1>	R30	CBEB1				
AGP CBE<0>	N29	CBEB0				
AGP CLK65M GPU	AG30	PCICLK				
AGP FRAME	U27	FRAMEB				
AGP IDY	T30	IRDYB				
AGP TRDY	T29	TRDYB				
AGP STOP	T29	STOPB				
AGP DEVSEL	T29	DEVSELB				
AGP PAR	R28	PAR				
AGP REQ	AF29	REQB				
AGP GNT	AF27	GNTB				
AGP INT L	AH29	INTAB				
GPU RESET L R	AH30	RSTB				
AGP WBF	AE29	WBF				
AGP ATI VREFG	AK3	VREFG				
AGP ATI MVREF	D8	VREF				

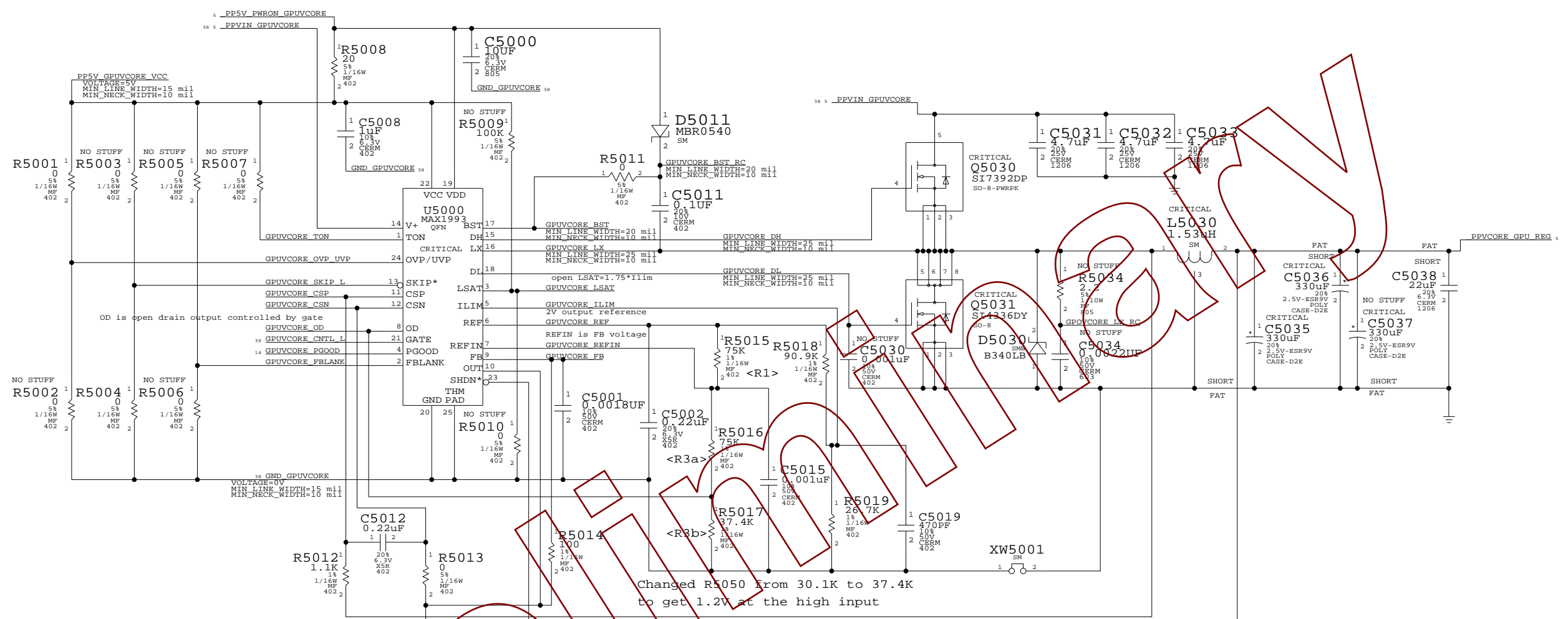
# Preliminary

## M11 AGP INTERFACE

NOTICE OF PROPRIETARY PROPERTY  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	NONE	SHT	49 OF 103





Changed R5050 from 30.1K to 37.4K  
to get 1.2V at the high input

When GPUTVCORE\_CNTL\_L = 1, Vout = 1.0V  
 $V_{out} = 2V * (R_2 / (R_1 + R_2)) = 1.0V$   
 When GPUTVCORE\_CNTL\_L = 0, Vout = 1.2V  
 $V_{out} = 2V * (R_{eq} / (R_1 + R_{eq})) = 1.2V$   
 $R_{eq} = R_{3a} + R_{3b}$

PRELIMINARY

### GPU VCore Regulator

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-6532	03
SCALE		SHT	OF
NONE		50	103

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
LVDS	LVDS	LVDS_I0
LVDS	LVDS	LVDS_I0P
LVDS	LVDS	LVDS_I0N
LVDS	LVDS	LVDS_I1
LVDS	LVDS	LVDS_I1P
LVDS	LVDS	LVDS_I1N
LVDS	LVDS	LVDS_I2
LVDS	LVDS	LVDS_I2P
LVDS	LVDS	LVDS_I2N
LVDS	LVDS	LVDS_ICLK
LVDS	LVDS	CLKLVDS_LP
LVDS	LVDS	CLKLVDS_LN
LVDS	LVDS	LVDS_U0P
LVDS	LVDS	LVDS_U0N
LVDS	LVDS	LVDS_U1P
LVDS	LVDS	LVDS_U1N
LVDS	LVDS	LVDS_U2P
LVDS	LVDS	LVDS_U2N
LVDS	LVDS	CLKLVDS_UP
LVDS	LVDS	CLKLVDS_UN
GPU_DVO_DATA	8 MIL SPACING	GPU DVOD<0..19>
GPU_DVO_DATA20	8 MIL SPACING	GPU DVOD<20>
GPU_DVO_DATA	8 MIL SPACING	GPU DVOD<21..23>
GPU_DVO_DATA	8 MIL SPACING	GPU DVO HSYNC
GPU_DVO_CTL	8 MIL SPACING	GPU DVO VSYNC
GPU_DVO_CTL	8 MIL SPACING	GPU DVO DE
GPU_DVO_CTL	8 MIL SPACING	GPU DVO CLKP

### Page Notes

Power aliases required by this page:  
 \_PP1V5\_GPU\_AGP, \_PP3V3\_GPU, PPVCORE\_GPU

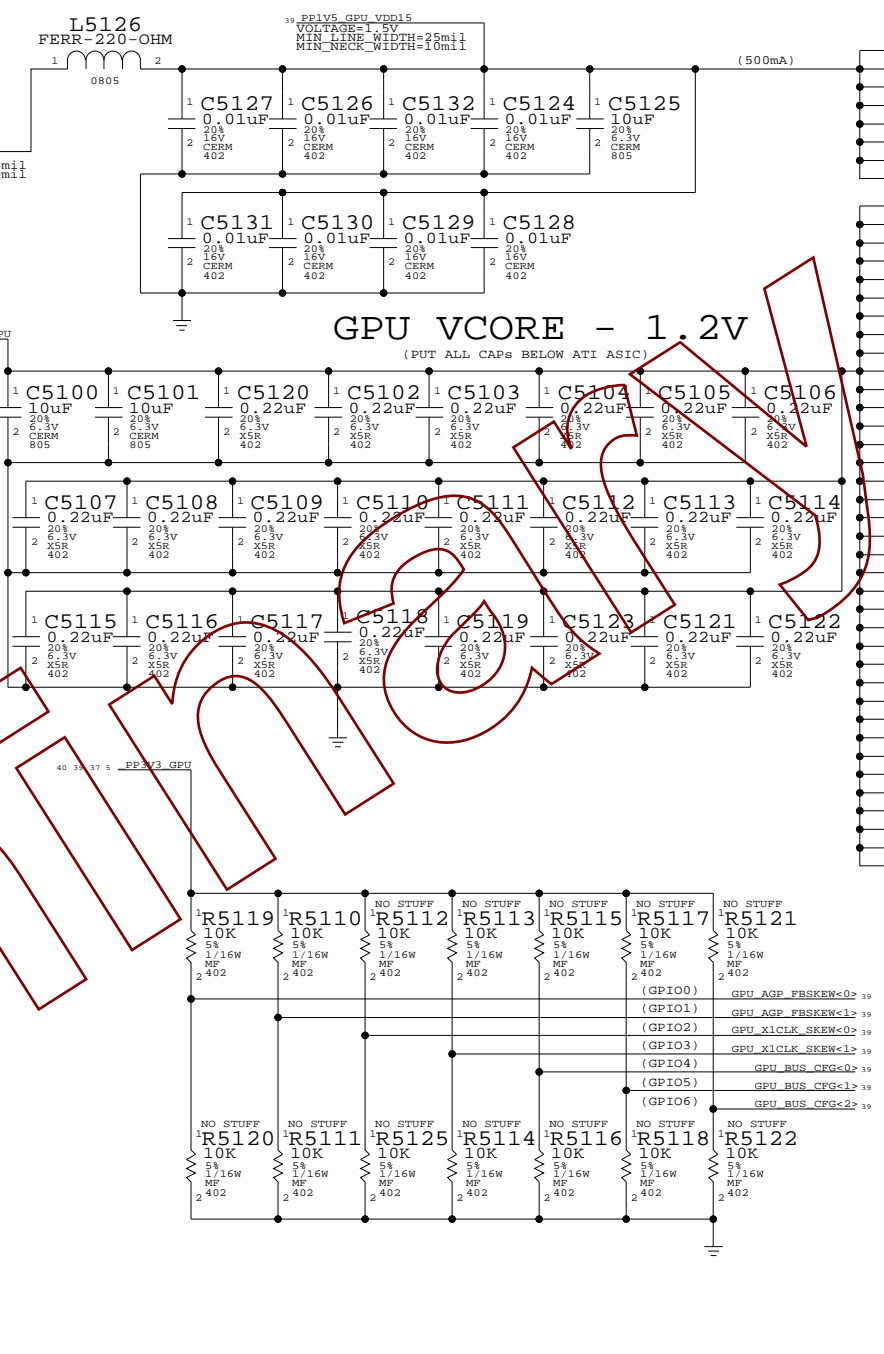
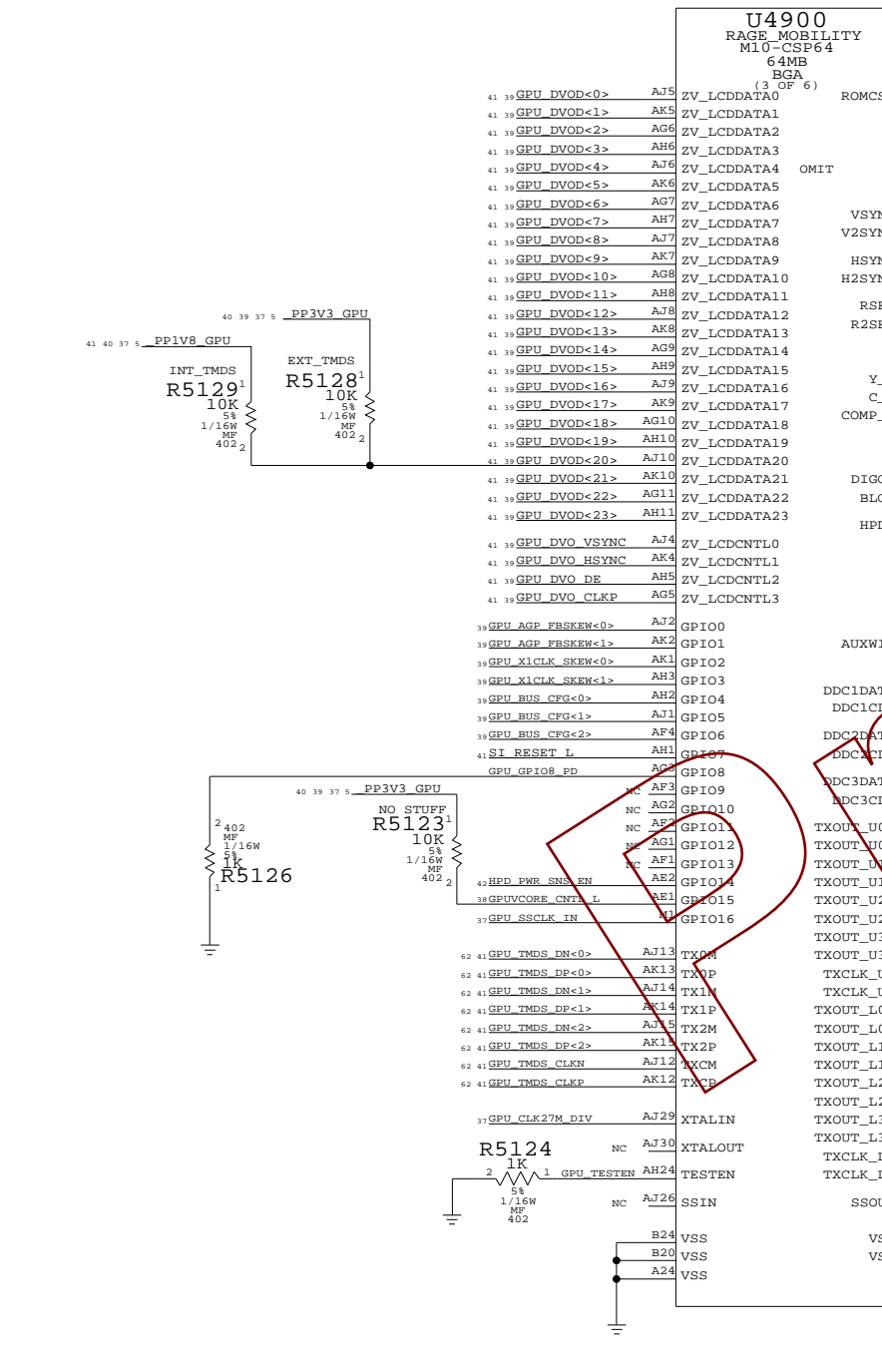
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

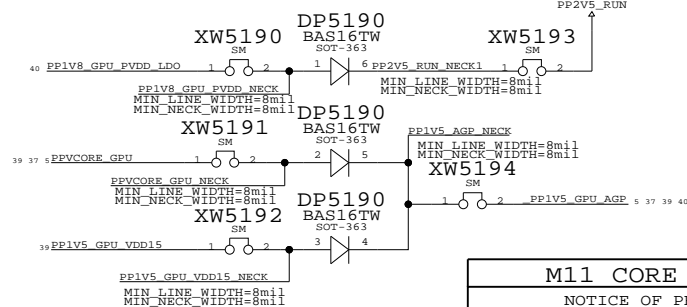
Net Spacing Type: LVDS

Line To Line: 15 mils  
 Length Tolerance: 50 mils  
 Primary Max Sep: 10 mils  
 Secondary Max Sep: 100 mils  
 Secondary Length: 250 mils

NOTE: Target differential impedance for LVDS data pairs is 100 ohms.



M10 Power Shut down Sequencing



**M11 CORE PWR/LVDS/TMDS**  
 NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6532	03
	SHEET	OF	
	51	103	

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---





# Page Notes

Power aliases required by this page:  
(None)

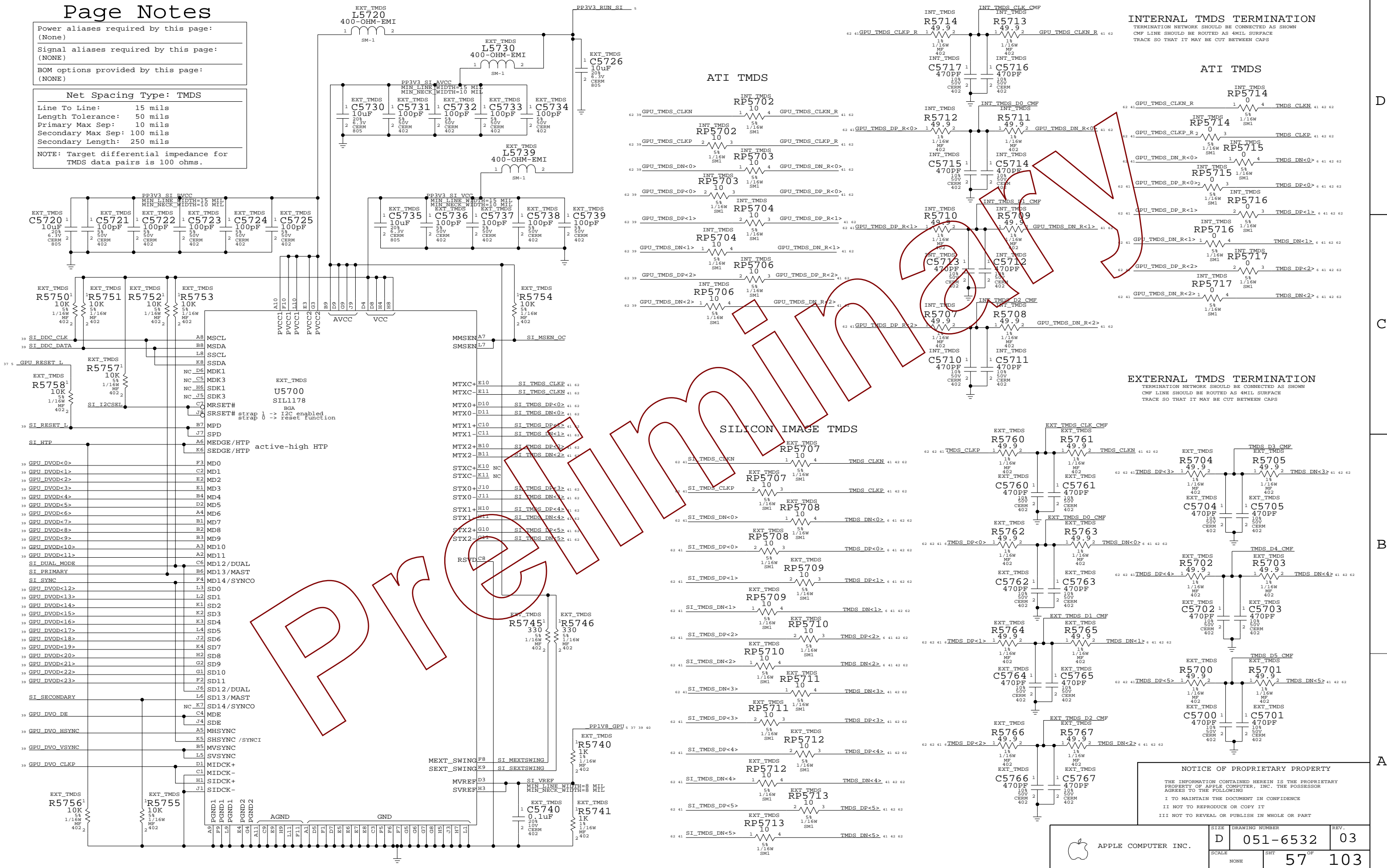
Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

## Net Spacing Type: TMSD

Line To Line: 15 mils  
Length Tolerance: 50 mils  
Primary Max Sep: 10 mils  
Secondary Max Sep: 100 mils  
Secondary Length: 250 mils

NOTE: Target differential impedance for TMSD data pairs is 100 ohms.



**INTERNAL TMSD TERMINATION**  
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN  
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE  
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

### ATI TMSD

### ATI TMSD

### SILICON IMAGE TMSD

**EXTERNAL TMSD TERMINATION**  
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN  
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE  
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHEET	OF	
NONE	57	103	

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

EXTERNAL VIDEO (DVI) INTERFACE

DVI POWER SWITCH

D

C

B

A

D

C

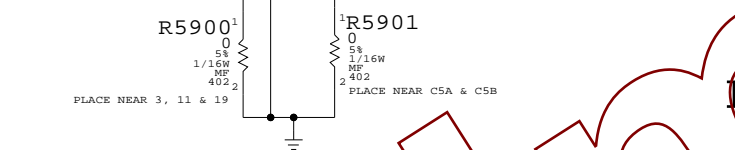
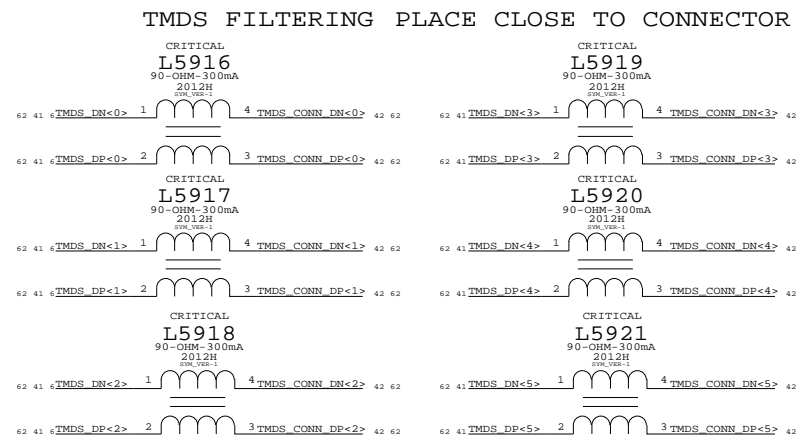
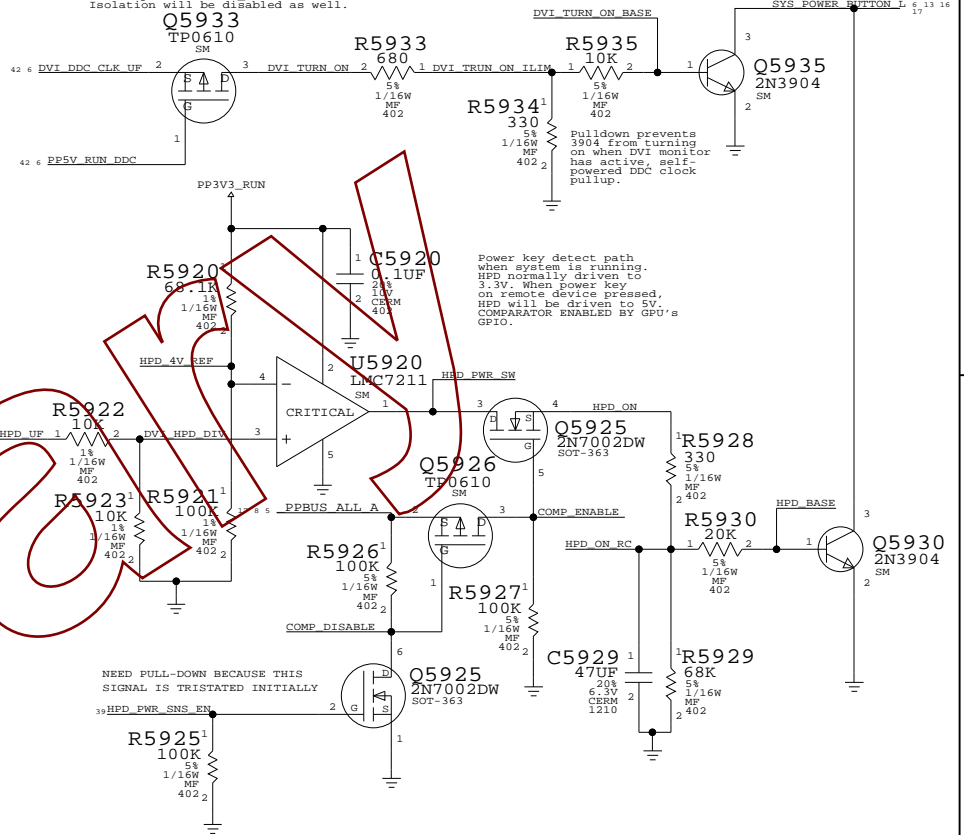
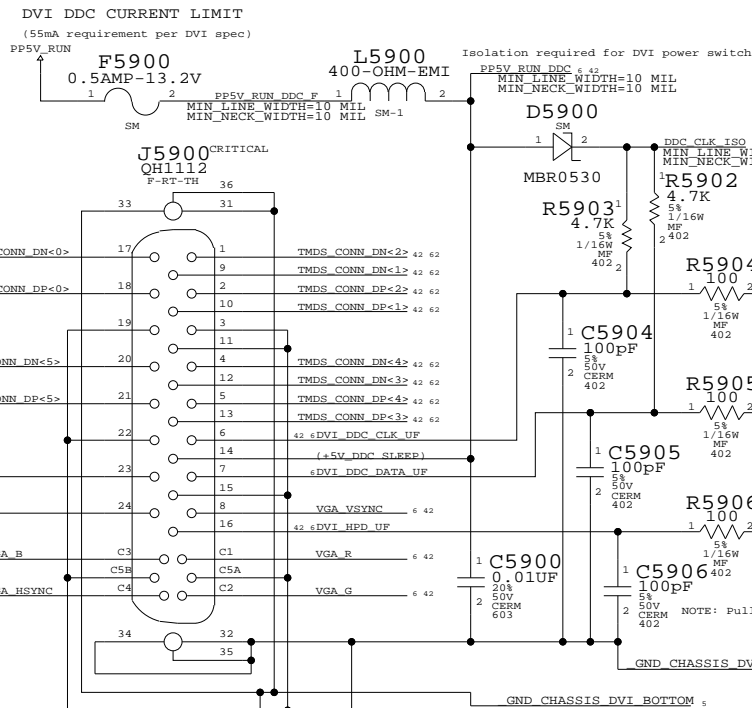
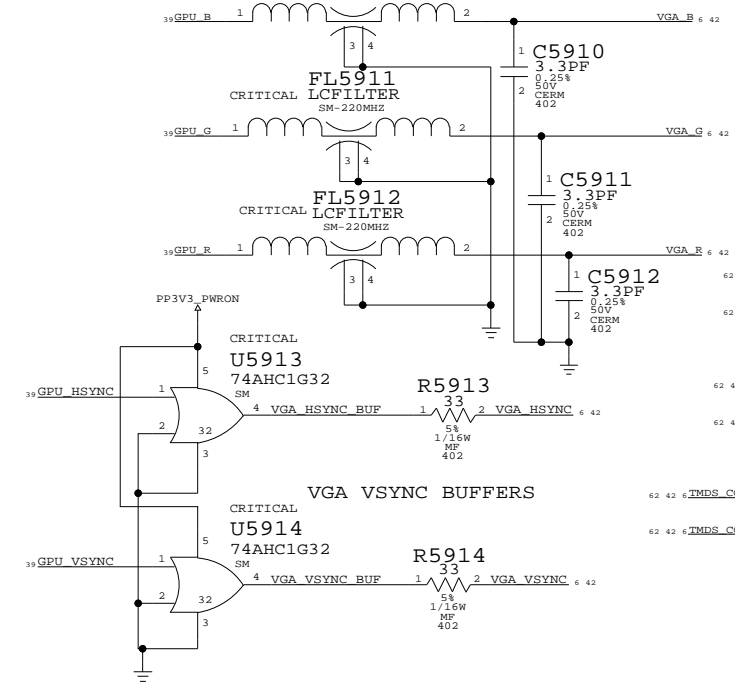
B

A

Power key detect path when system is shutdown or asleep... DDC CLK is isolated from GPU DURING SHUTDOWN. When power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT\_PWR\_ON low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

Power key detect path when system is running. HPD normally driven to 3.3v. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY GPU'S GPIO.

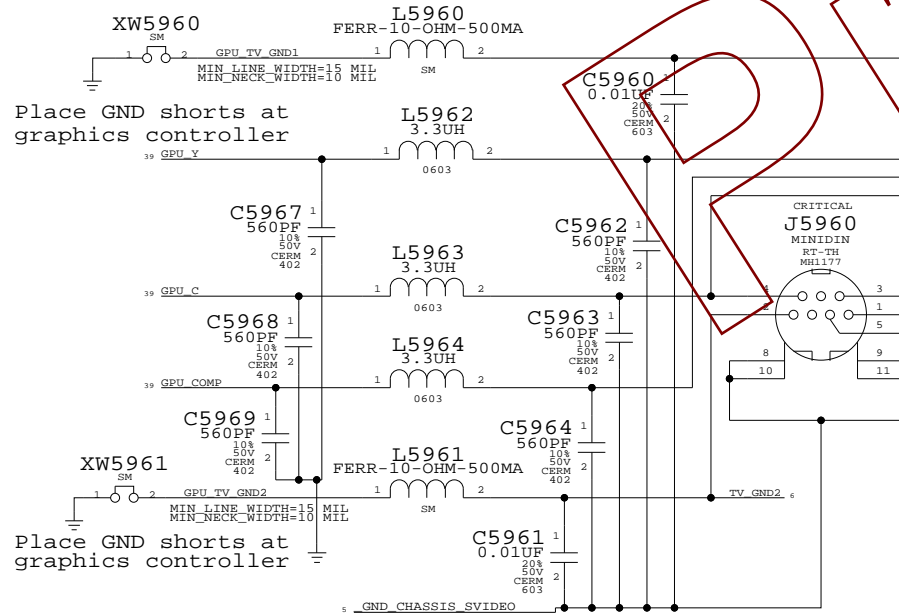
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY



LCD INTERFACE

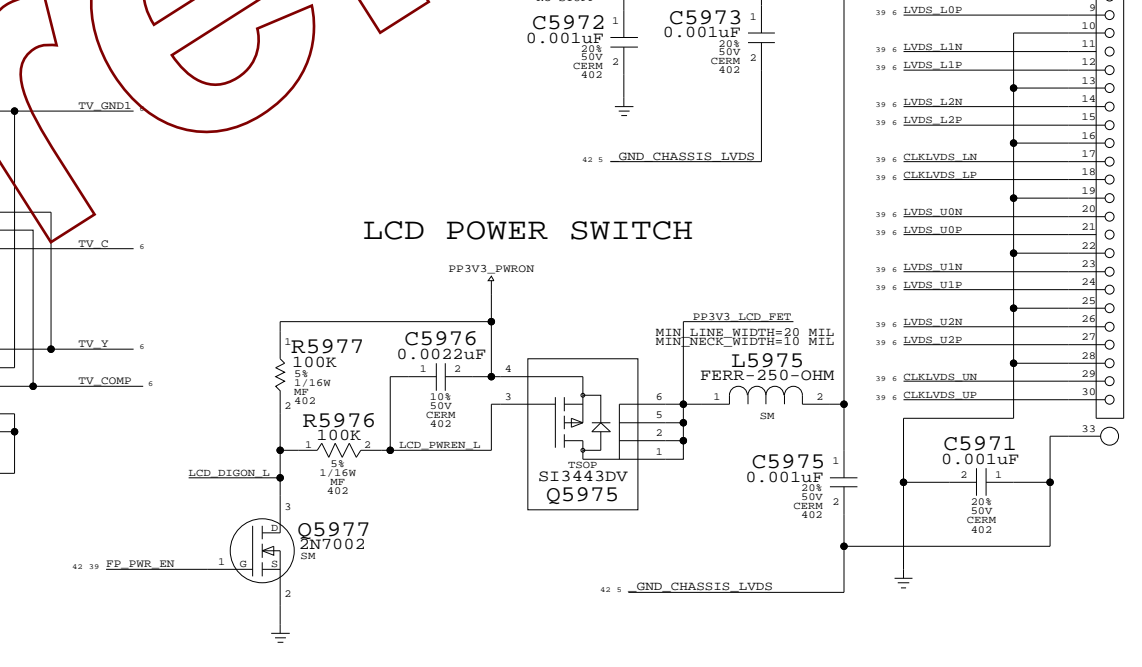
INVERTER INTERFACE

S-VIDEO/COMP OUT INTERFACE

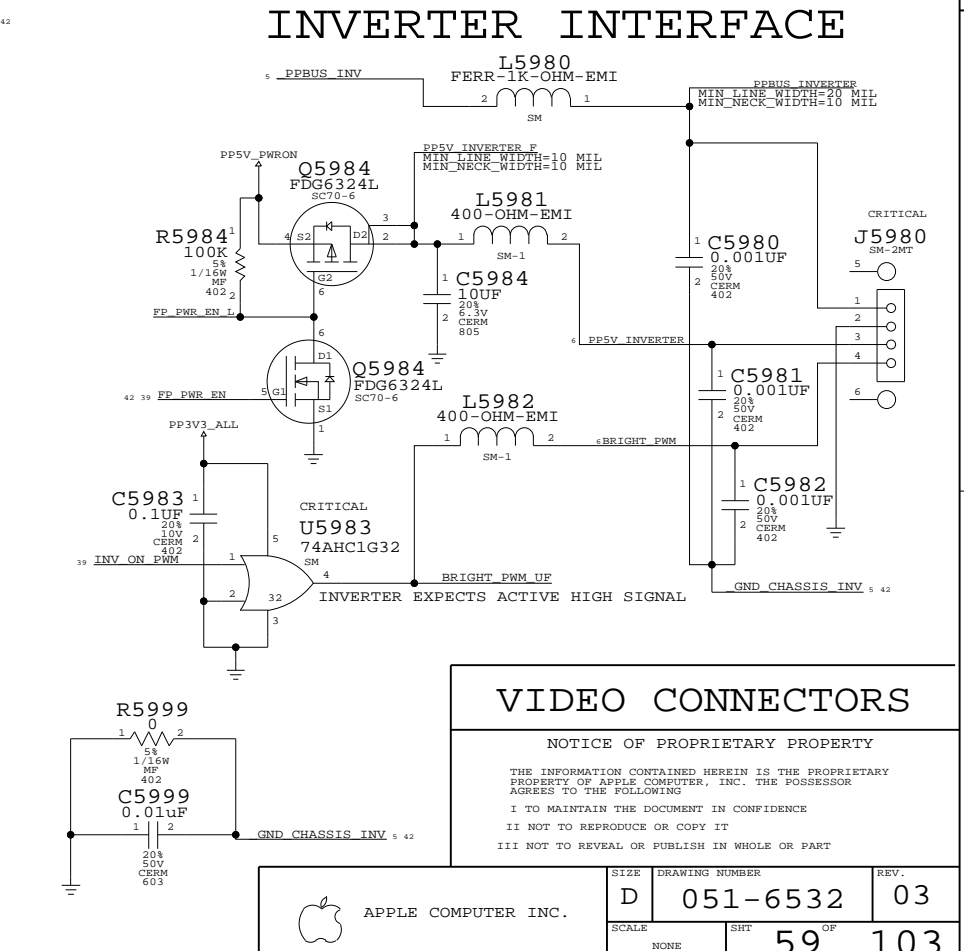


Place GND shorts at graphics controller

Place GND shorts at graphics controller



LCD POWER SWITCH



VIDEO CONNECTORS

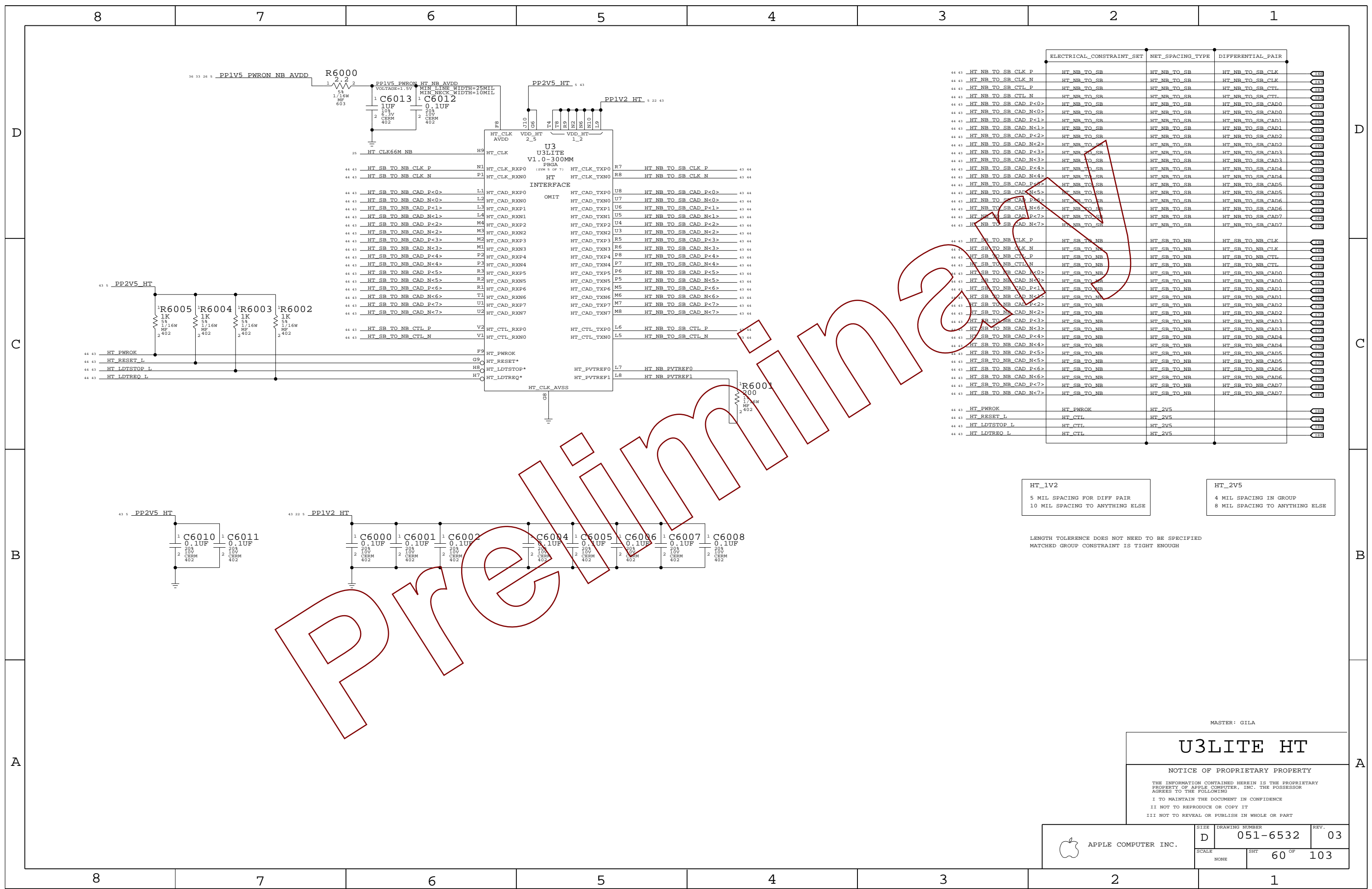
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF



APPLE COMPUTER INC. D 051-6532 03
SCALE NONE SHEET 59 OF 103





ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT NB TO SB CLK P	HT NB_TO_SB	HT NB_TO_SB_CLK
HT NB TO SB CLK N	HT NB_TO_SB	HT NB_TO_SB_CLK
HT NB TO SB CTL P	HT NB_TO_SB	HT NB_TO_SB_CTL
HT NB TO SB CTL N	HT NB_TO_SB	HT NB_TO_SB_CTL
HT NB TO SB CAD P<0>	HT NB_TO_SB	HT NB_TO_SB_CAD0
HT NB TO SB CAD N<0>	HT NB_TO_SB	HT NB_TO_SB_CAD0
HT NB TO SB CAD P<1>	HT NB_TO_SB	HT NB_TO_SB_CAD1
HT NB TO SB CAD N<1>	HT NB_TO_SB	HT NB_TO_SB_CAD1
HT NB TO SB CAD P<2>	HT NB_TO_SB	HT NB_TO_SB_CAD2
HT NB TO SB CAD N<2>	HT NB_TO_SB	HT NB_TO_SB_CAD2
HT NB TO SB CAD P<3>	HT NB_TO_SB	HT NB_TO_SB_CAD3
HT NB TO SB CAD N<3>	HT NB_TO_SB	HT NB_TO_SB_CAD3
HT NB TO SB CAD P<4>	HT NB_TO_SB	HT NB_TO_SB_CAD4
HT NB TO SB CAD N<4>	HT NB_TO_SB	HT NB_TO_SB_CAD4
HT NB TO SB CAD P<5>	HT NB_TO_SB	HT NB_TO_SB_CAD5
HT NB TO SB CAD N<5>	HT NB_TO_SB	HT NB_TO_SB_CAD5
HT NB TO SB CAD P<6>	HT NB_TO_SB	HT NB_TO_SB_CAD6
HT NB TO SB CAD N<6>	HT NB_TO_SB	HT NB_TO_SB_CAD6
HT NB TO SB CAD P<7>	HT NB_TO_SB	HT NB_TO_SB_CAD7
HT NB TO SB CAD N<7>	HT NB_TO_SB	HT NB_TO_SB_CAD7
HT SB TO NB CLK P	HT SB_TO_NB	HT SB_TO_NB_CLK
HT SB TO NB CLK N	HT SB_TO_NB	HT SB_TO_NB_CLK
HT SB TO NB CTL P	HT SB_TO_NB	HT SB_TO_NB_CTL
HT SB TO NB CTL N	HT SB_TO_NB	HT SB_TO_NB_CTL
HT SB TO NB CAD P<0>	HT SB_TO_NB	HT SB_TO_NB_CAD0
HT SB TO NB CAD N<0>	HT SB_TO_NB	HT SB_TO_NB_CAD0
HT SB TO NB CAD P<1>	HT SB_TO_NB	HT SB_TO_NB_CAD1
HT SB TO NB CAD N<1>	HT SB_TO_NB	HT SB_TO_NB_CAD1
HT SB TO NB CAD P<2>	HT SB_TO_NB	HT SB_TO_NB_CAD2
HT SB TO NB CAD N<2>	HT SB_TO_NB	HT SB_TO_NB_CAD2
HT SB TO NB CAD P<3>	HT SB_TO_NB	HT SB_TO_NB_CAD3
HT SB TO NB CAD N<3>	HT SB_TO_NB	HT SB_TO_NB_CAD3
HT SB TO NB CAD P<4>	HT SB_TO_NB	HT SB_TO_NB_CAD4
HT SB TO NB CAD N<4>	HT SB_TO_NB	HT SB_TO_NB_CAD4
HT SB TO NB CAD P<5>	HT SB_TO_NB	HT SB_TO_NB_CAD5
HT SB TO NB CAD N<5>	HT SB_TO_NB	HT SB_TO_NB_CAD5
HT SB TO NB CAD P<6>	HT SB_TO_NB	HT SB_TO_NB_CAD6
HT SB TO NB CAD N<6>	HT SB_TO_NB	HT SB_TO_NB_CAD6
HT SB TO NB CAD P<7>	HT SB_TO_NB	HT SB_TO_NB_CAD7
HT SB TO NB CAD N<7>	HT SB_TO_NB	HT SB_TO_NB_CAD7
HT PWROK	HT_PWROK	HT_2V5
HT RESET L	HT_CTL	HT_2V5
HT LDTSTOP L	HT_CTL	HT_2V5
HT LDTREQ L	HT_CTL	HT_2V5

HT\_1V2  
5 MIL SPACING FOR DIFF PAIR  
10 MIL SPACING TO ANYTHING ELSE

HT\_2V5  
4 MIL SPACING IN GROUP  
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERANCE DOES NOT NEED TO BE SPECIFIED  
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: GILA

# U3LITE HT

## NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

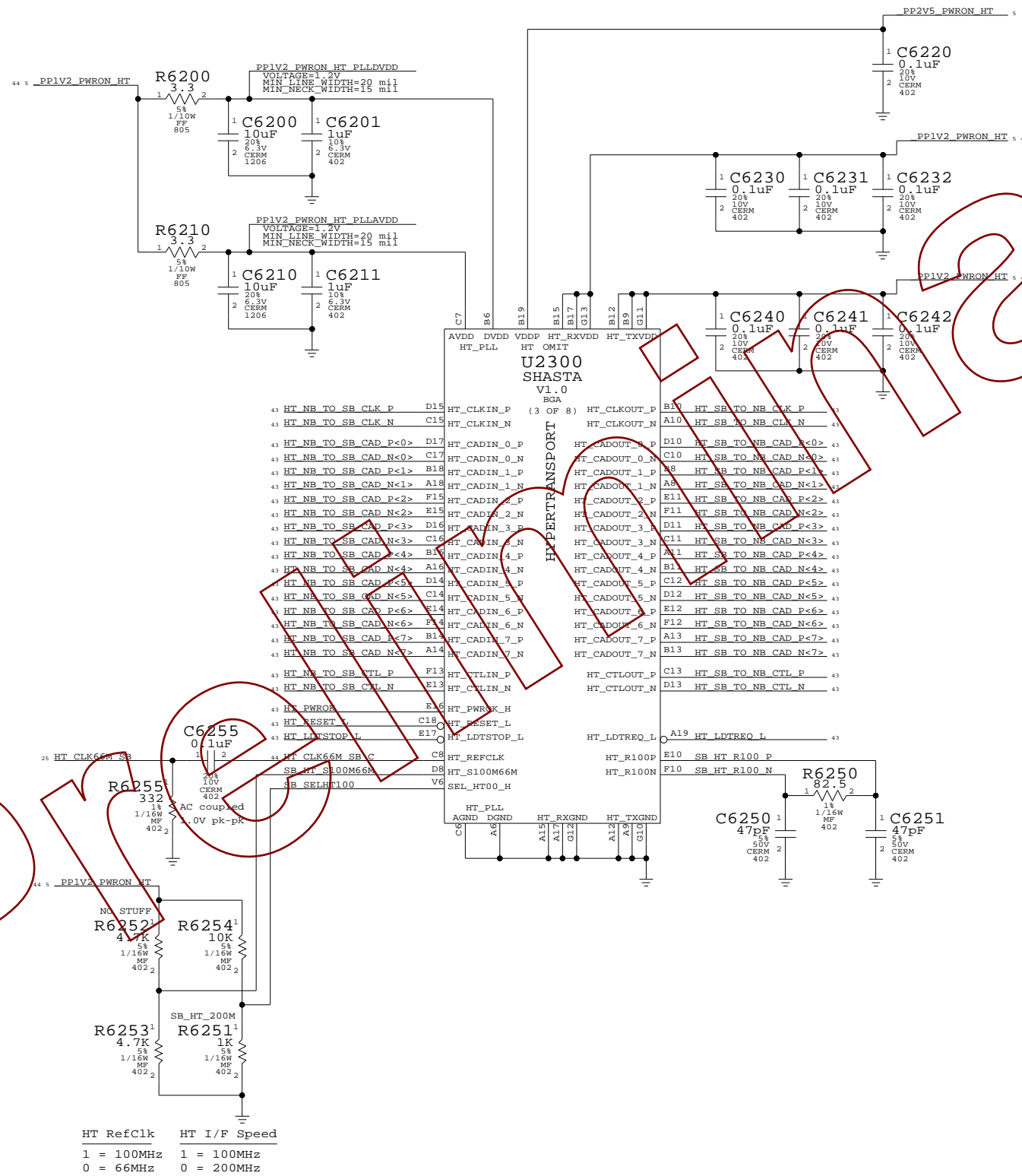
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	60 OF 103	
NONE			

### Page Notes

Power aliases required by this page:  
 - \_PP2V5\_PWRON\_HT  
 - \_PP1V2\_PWRON\_HT

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - SB\_HT\_200M  
 Stuffs resistor to select 200MHz HT I/F.



HT RefClk    HT I/F Speed  
 1 = 100MHz    1 = 100MHz  
 0 = 66MHz     0 = 200MHz

Master: Fizzy

### Shasta HyperTransport

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	62	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_AD		
PCI_AD27		
PCI_AD		
PCI_AD23		
PCI_AD22		
PCI_AD21		
PCI_AD20		
PCI_AD		
PCI_AD17		
PCI_AD		
PCI		
PCI		
PCI_CTL		
PCI_CTL		
PCI_CTL		
PCI_CTL		
PCI_CTL		
PCI_CTL		

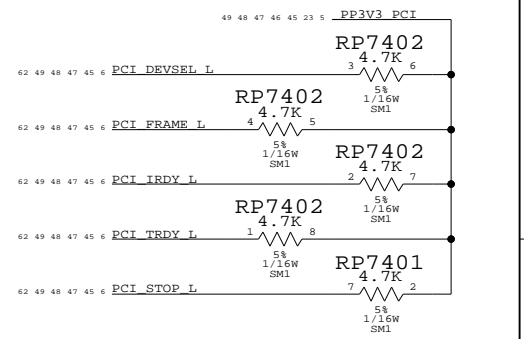
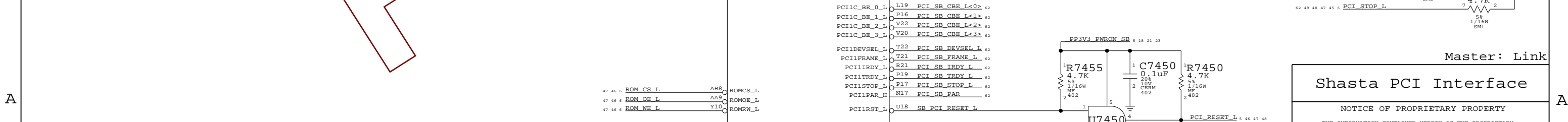
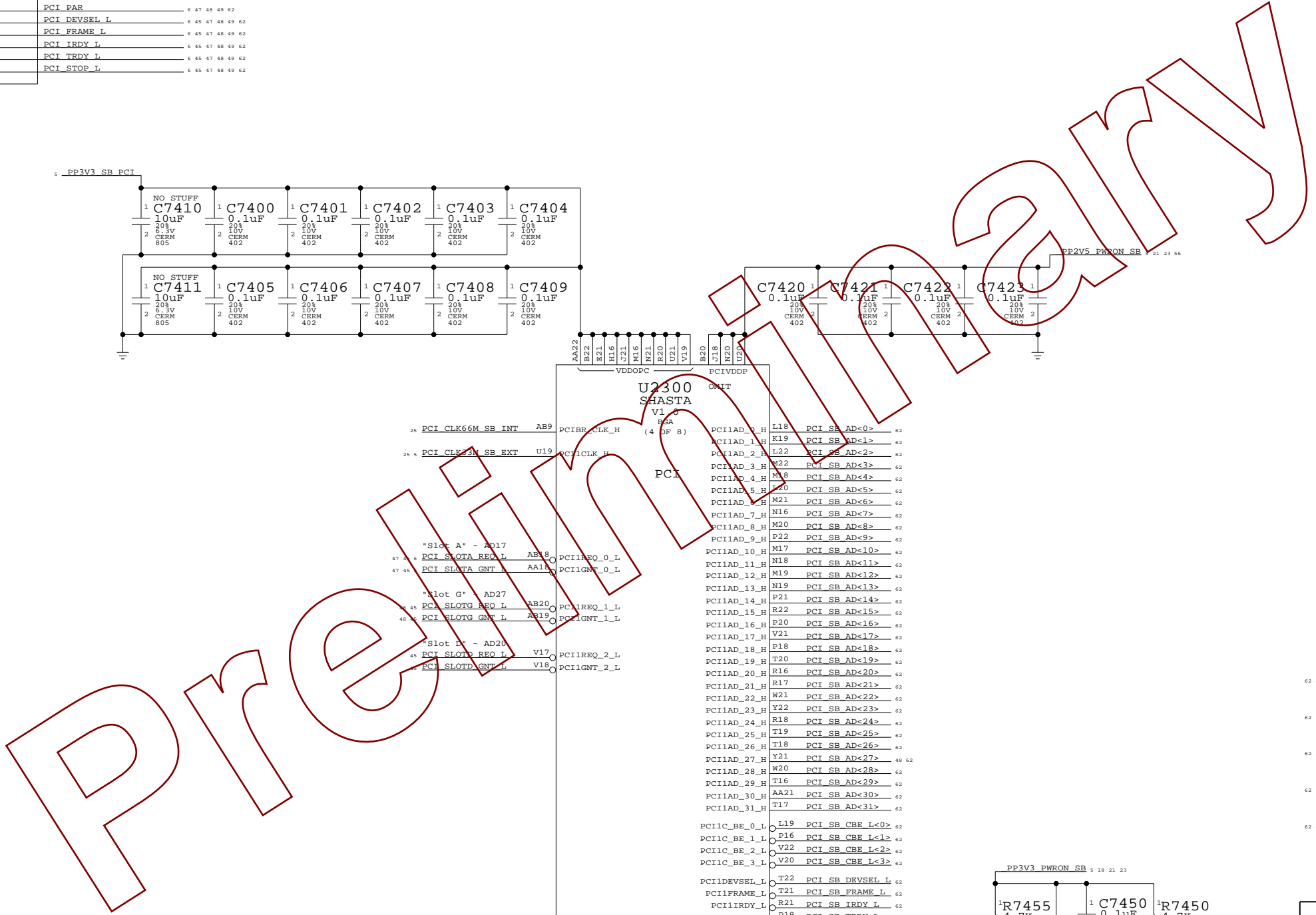
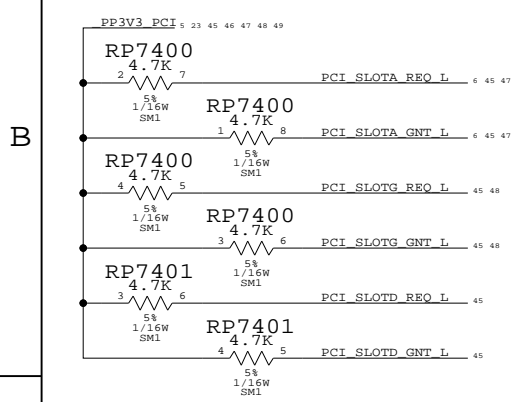
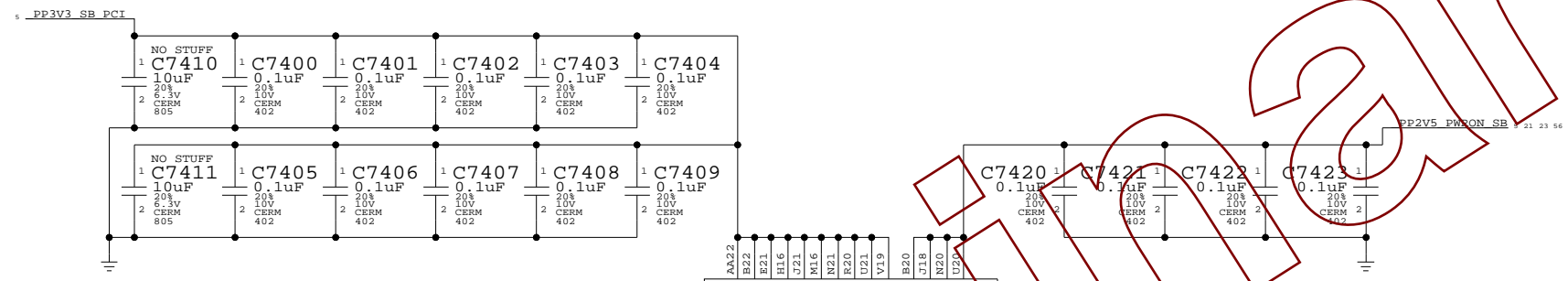
Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PCI  
 - \_PP3V3\_SB\_PCI (can be \_PP3V3\_PCI)  
 - \_PP3V3\_PWRON\_SB  
 - \_PP2V5\_PWRON\_SB

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

PCI Devices implemented on this page:  
 AD11 - PCI0 (0x106B/0x0053)  
 AD11 - PCI1 (0x106B/0x0054)  
 AD11 - PCI2 (0x106B/0x0055)  
 AD23 - KeyLargo (0x106B/0x004F, PCI1)  
 AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)  
 AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)  
 AD30 - FireWire (0x106B/0x0052, PCI0 or 2)  
 AD31 - Ethernet (0x106B/0x0051, PCI0)



Master: Link  
**Shasta PCI Interface**

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

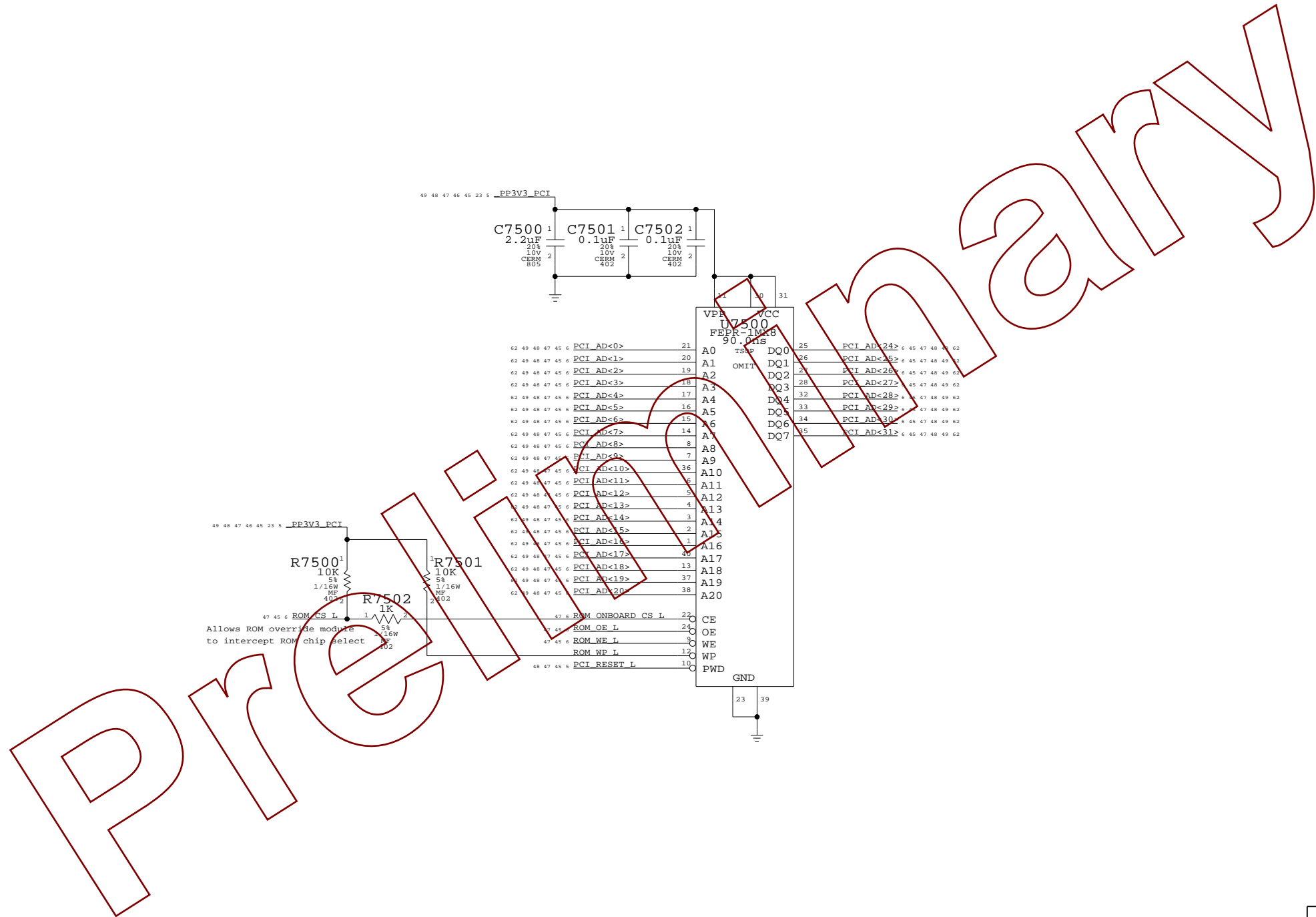
# Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PCI

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE\_x\_ITEM symbol to declare U7500 part number.



Pre-Announcement

Master: Fizzy

## BootROM

### NOTICE OF PROPRIETARY PROPERTY


THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

\_DRAWING  
 TITLE=FIZZY  
 ABBREV=DRAWING  
 LAST\_MODIFIED=Mon Feb 23 19:06:47 2004

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	75	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT

## Page Notes

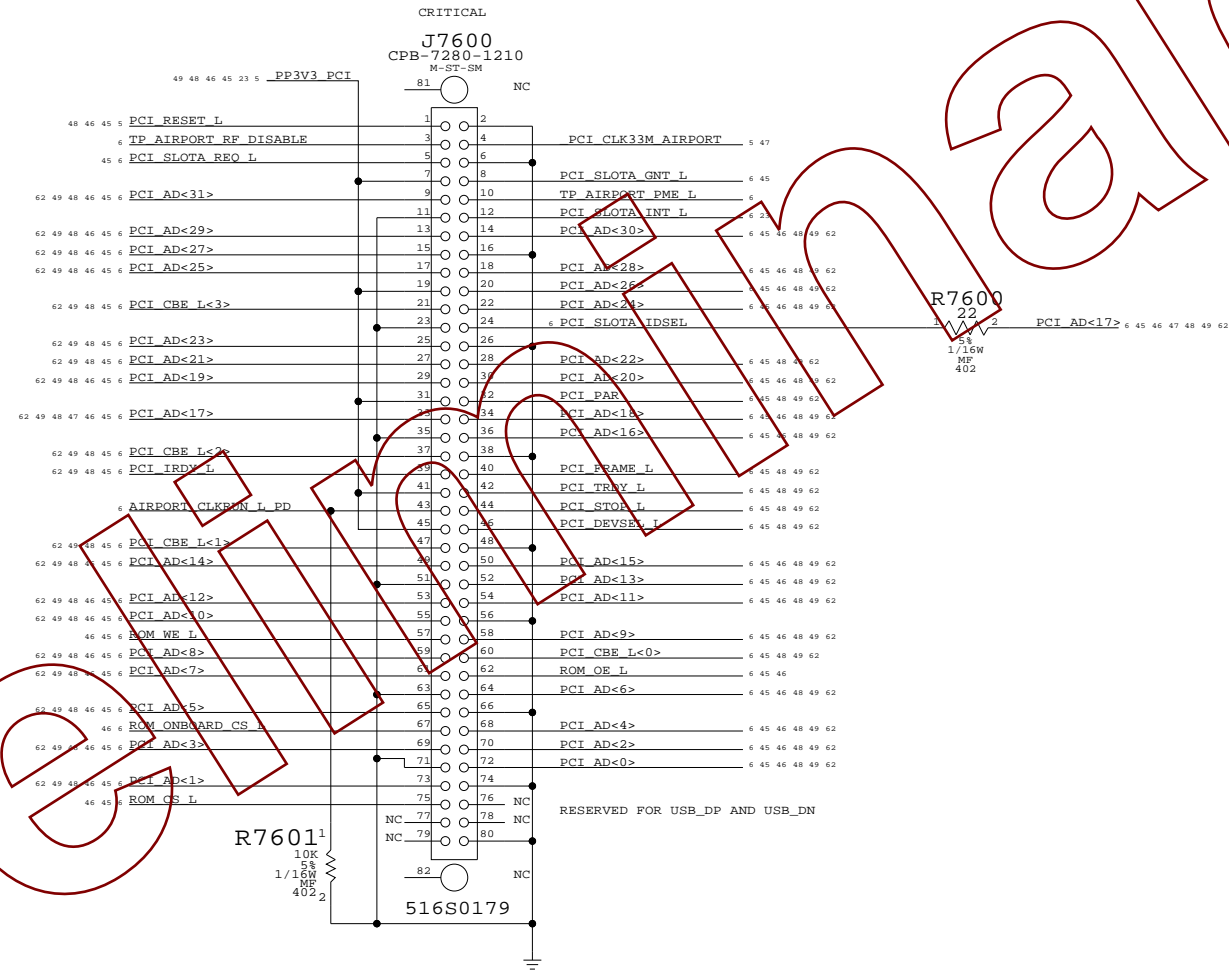
Power aliases required by this page:  
 - \_PP3V3\_PCI

Signal aliases required by this page:  
 - \_PCI\_CLK33M\_AIRPORT (33MHz PCI clock)

BOM options provided by this page:  
 (NONE)

PCI Devices implemented on this page:  
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



Pre-Announcement

### AirPort Extreme

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE	SHT	OF
NONE	76	103



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	PCI_CLK33M_USB2

# Page Notes

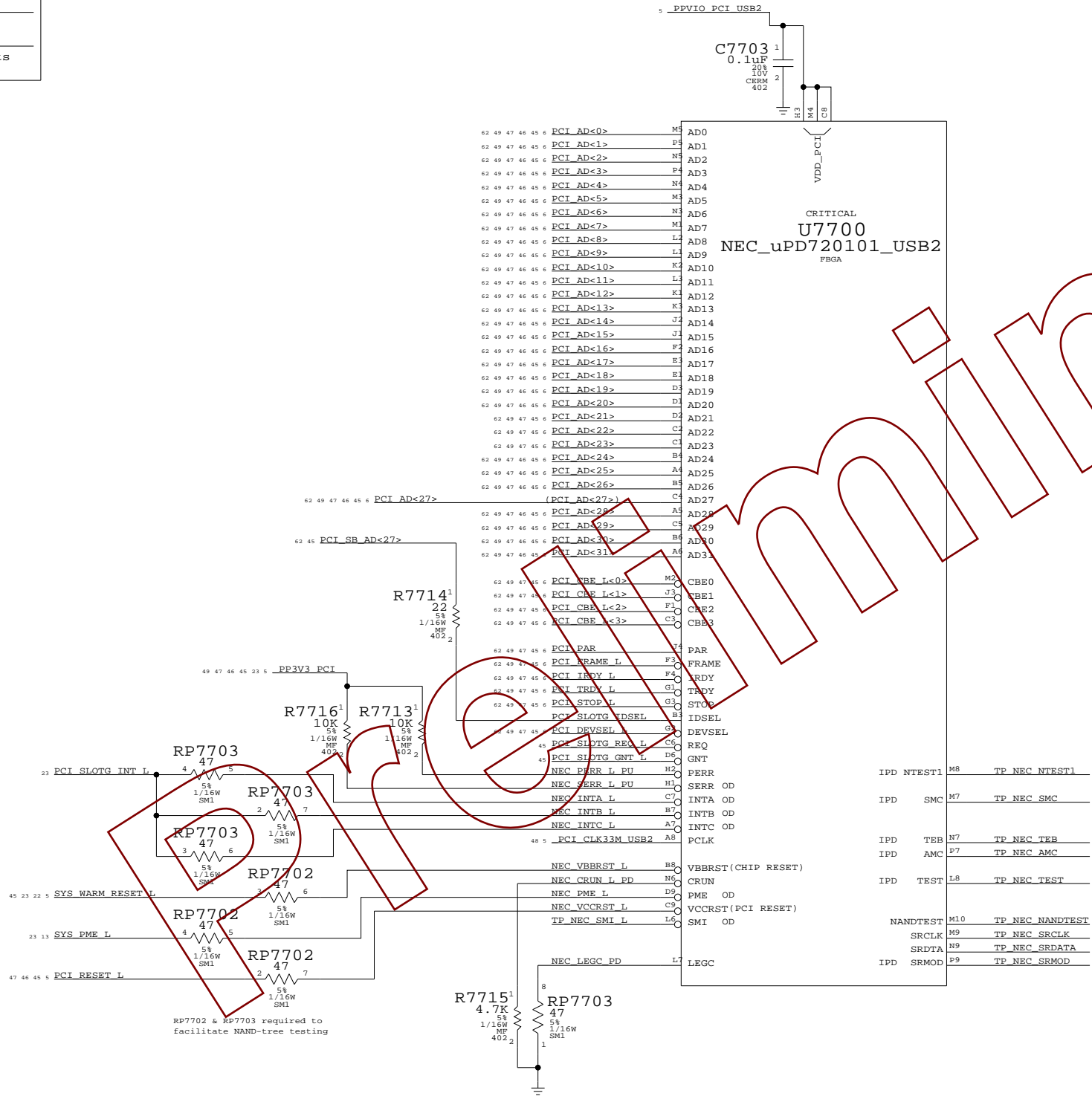
Power aliases required by this page:  
 - \_PPVIO\_PCI (to 3.3V or 5V)

Signal aliases required by this page:  
 - \_PCI\_CLK33M\_USB2 (33MHz PCI clock)

BOM options provided by this page:  
 (NONE)

PCI Devices implemented on this page:  
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



RP7702 & RP7703 required to facilitate NAND-tree testing

Master: Fizzy

## USB 2.0 PCI Interface

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	77	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_CBUS	CLOCKS	PCI_CLK33M_CBUS

# Page Notes

Power aliases required by this page:  
 - \_PP5V\_CBUS  
 - \_PP3V3\_CBUS  
 - \_PP3V3\_PCI  
 - \_PP2V5\_PCI  
 - \_PPVIO\_PCI (to \_PP5V\_PCI or \_PP3V3\_PCI)  
 NOTE: All 4 rails MUST implement the same power state (PWRON or RUN). For PWRON must alias \_PCI\_CBUS\_RESET\_L to SYS\_WARM\_RESET\_L. For RUN must alias to PCI\_RESET\_L instead.

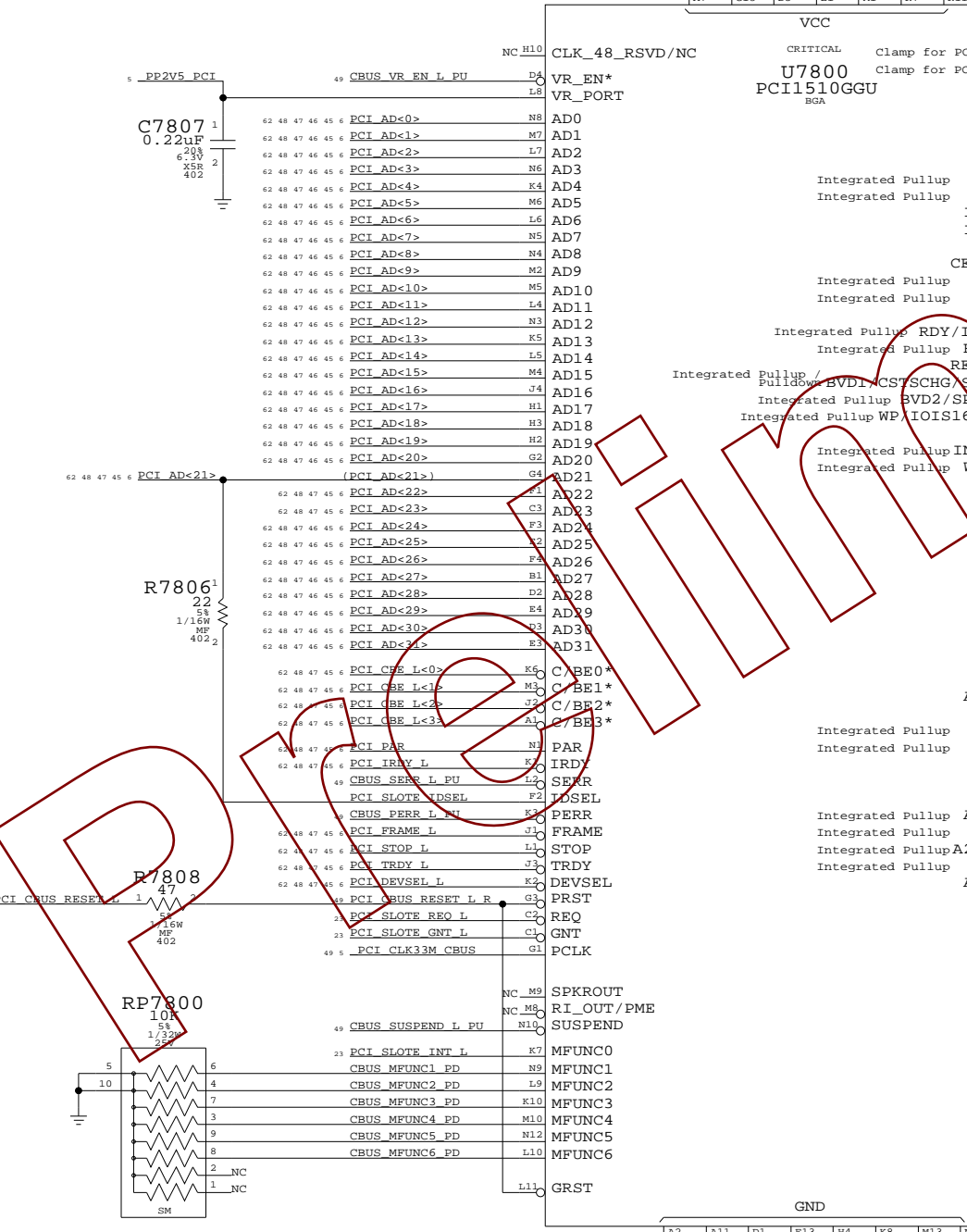
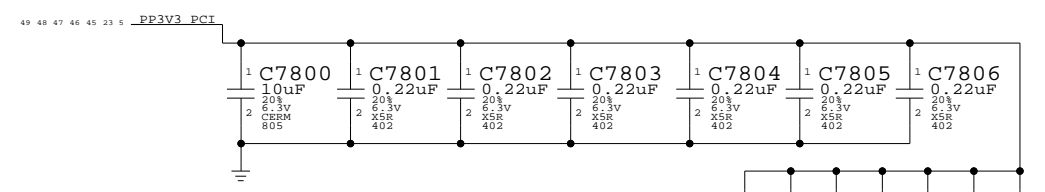
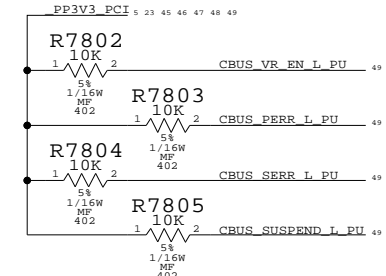
Signal aliases required by this page:  
 - \_PCI\_CBUS\_RESET\_L (see note above)  
 - \_PCI\_CLK33M\_CBUS (33MHz PCI clock)

BOM options provided by this page:  
 (NONE)

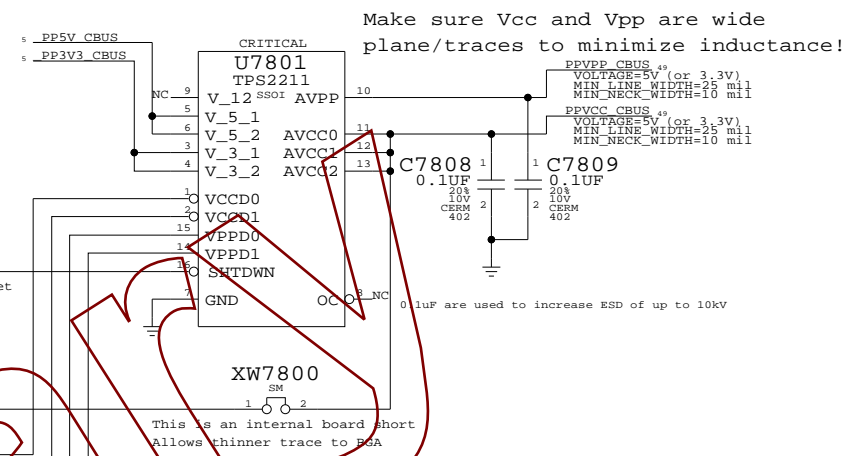
PCI Devices implemented on this page:  
 AD21 (Slot "E") - CardBus (0x104C/0xAC56)

Power Sequencing:  
 Power Up                      Power Down  
 1. Assert RESET            1. Assert RESET  
 2. \_PP3V3\_PCI              2. \_PPVIO\_PCI  
 3. \_PPVIO\_PCI              3. \_PP3V3\_PCI  
 (\_PPVIO\_PCI can be same as \_PP3V3\_PCI)

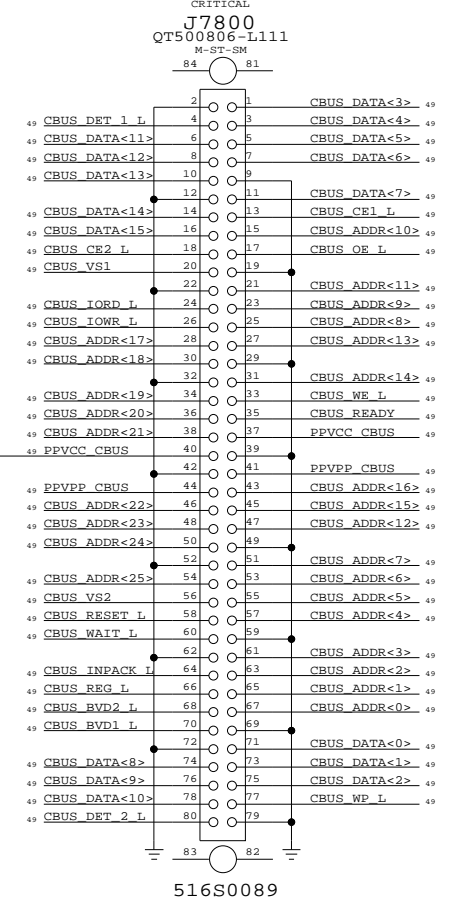
NOTE: This CardBus implementation does not provide PME# or 12V Vpp support.



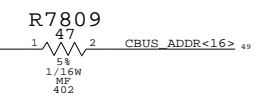
## PC Card Power Switch



## PC Card/CardBus Connector



TI reference schematic does not have bulk on PPVCC\_CBUS



516S0089

Master: Fizzy

**CardBus Interface**

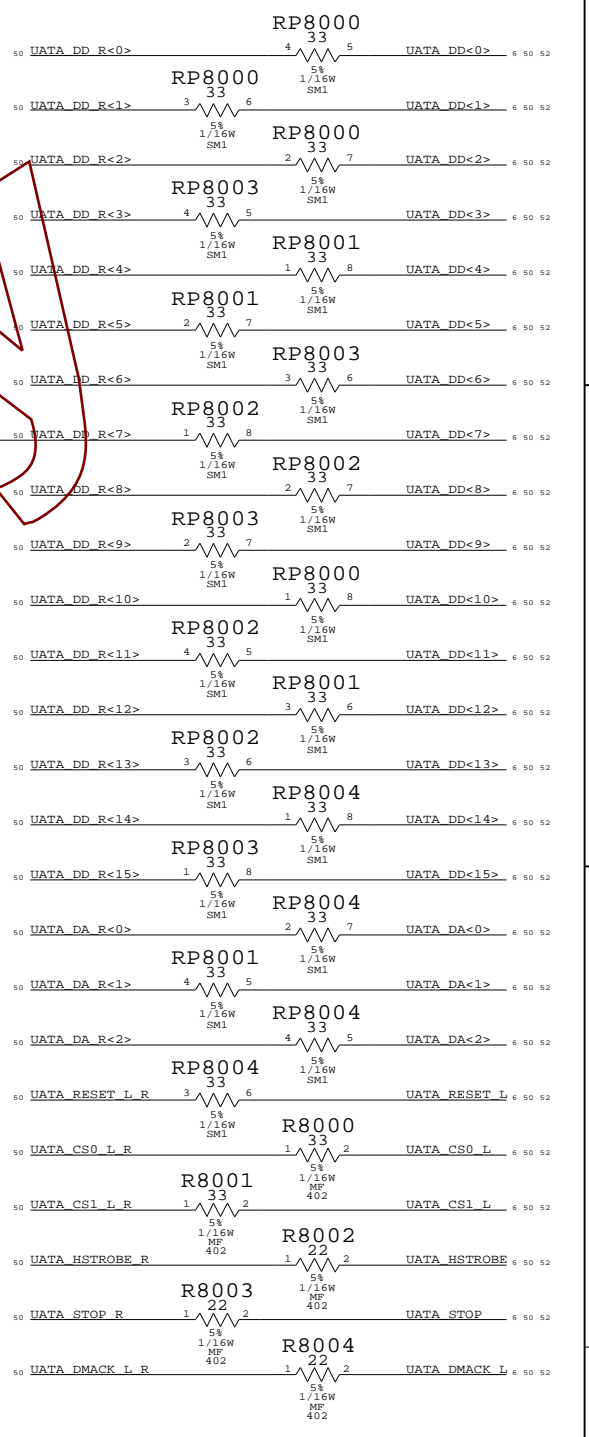
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C 50 51
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C 50 51
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1 50 51
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1 50 51
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C 5 50
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C 5 50
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2 5 50
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2 5 50
UATA_DD		UATA_DD<15..8>	6 50 52
UATA_DD7		UATA_DD<7>	6 50 52
UATA_DD		UATA_DD<6..0>	6 50 52
UATA_HOST		UATA_DA<2..0>	6 50 52
UATA_HOST		UATA_CS0_L	6 50 52
UATA_HOST		UATA_CS1_L	6 50 52
UATA_HOST		UATA_HSTROBE	6 50 52
UATA_HOST		UATA_STOP	6 50 52
UATA_HOST_R		UATA_DMACK_L	6 50 52
UATA_HOST_R		UATA_RESET_L	6 50 52
UATA_DEV_R_C		UATA_DSTROBE	50 52
UATA_DEV_R		UATA_DMARQ	50 52
UATA_DEV_R		UATA_INTRO	50 52

UATA Termination



Page Notes

Power aliases required by this page:  
 - \_PP1V2\_PWRON\_DISK

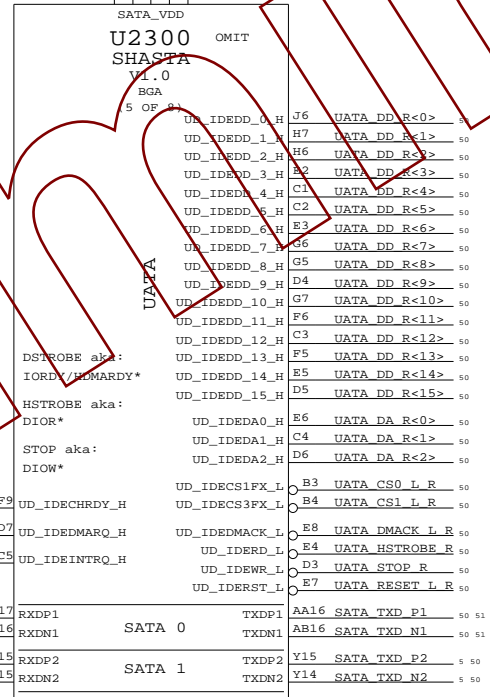
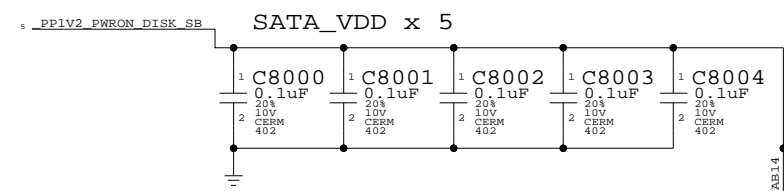
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

Net Spacing Type: SATA

Line To Line: 15 mils  
 Length Tolerance: 50 mils  
 Primary Max Sep: 10 mils outer  
 Primary Max Sep: 9 mils inner  
 Secondary Max Sep: 100 mils  
 Secondary Length: 500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.



AC coupling required for any SATA pair used.  
 Recommend 0.1uF cap placed close to Shasta.  
 (Caps provided by device page)



Master: Link

Shasta Disk

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	80	103	

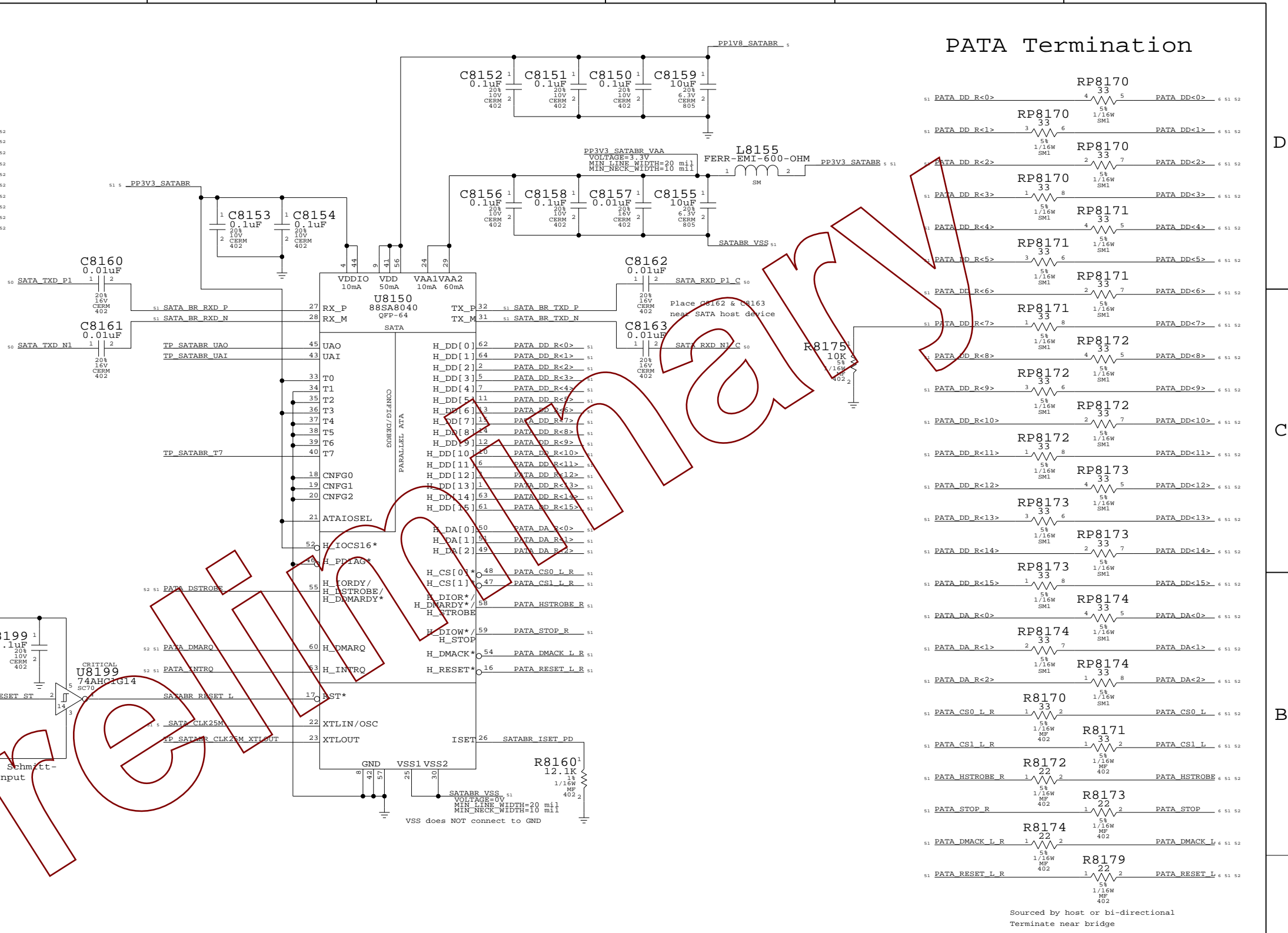
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PROVIDED BY	SATA	SATA_BR_RXD
SATA CONTROLLER	SATA	SATA_BR_TXD
	CLOCKS	SATA_CLK25M

### Page Notes

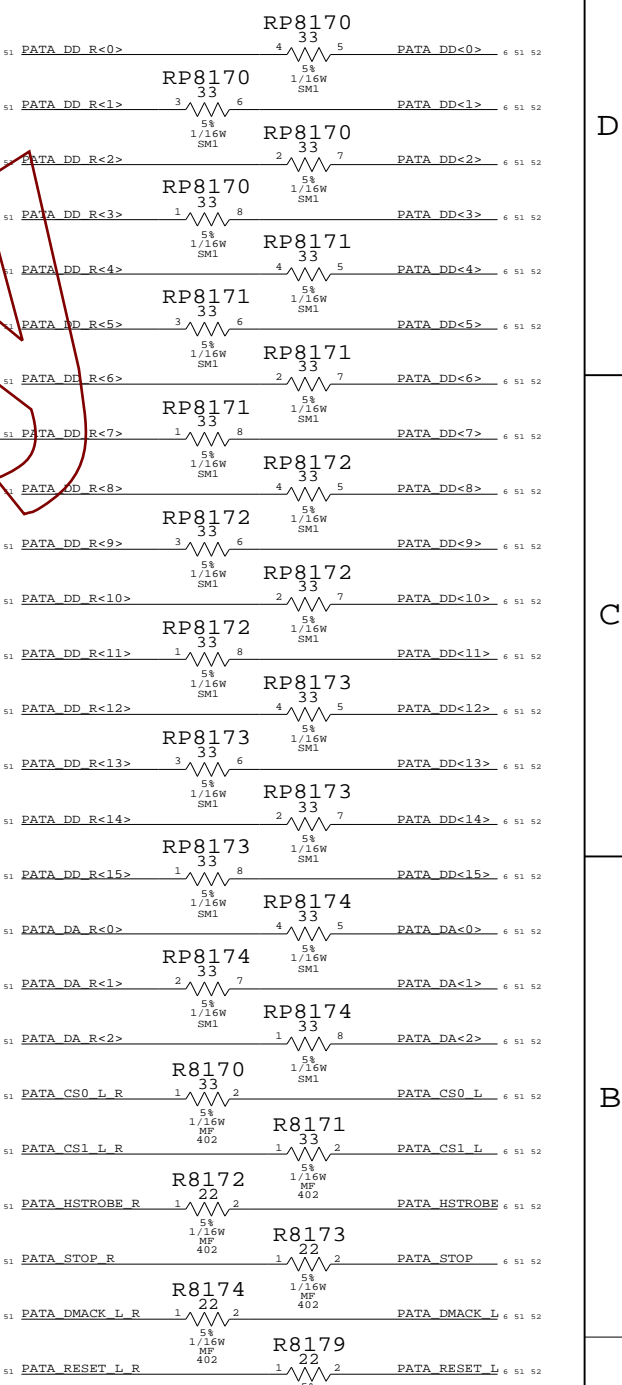
Power aliases required by this page:  
 - PP3V3\_SATABR  
 - PP1V8\_SATABR

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - SATA\_1\_BRIDGE (/ SATA\_1\_CONN)  
 Selects whether 88SA8040 SATA Bridge or SATA connector is connected to Shasta SATA port 1.



### PATA Termination



#### 88SA8040 Config Straps (Device Mode):

T<1..0> - Vendor Unique (VU) and Read/Write Long	T<4..3> - Reference Clock Configuration	T6 - Power Mode Enable	CNFG<2..0> - Mode Configuration	H_IOCS16_N - DMA_EN
T<1..0> VU Type R/W Long Type	T<4..3> Clock Frequency	1 - Enable translation of ATA power management commands into SATA Partial or Slumber mode	CNFG<2..0> Mode	1 - Good status on Set Features to set DMA
00 1 1	00 20 MHz	0 - Disable translation (Internal Pull-down)	000 Device Mode - 100MB/s	0 - Error status on Set Features to set DMA (Internal Pull-up)
01 1 2	01 25 MHz	T7 - Plug-in (output)	001 Device Mode - 133MB/s	H_PDIAQ_N - PATA_ORDER
10 1 1 (default)	10 30 MHz	1 - SATA cable plugged in	010 Device Mode - 150MB/s (default)	1 - Reverse Order mode for Parallel ATA pins
11 2 2	11 40 MHz	0 - SATA cable unplugged (Internal Pull-down)	100 Host Mode - 100MB/s	0 - Normal Order mode
T2 - SSC Enable	T5 - Fixed UDMA		101 Host Mode - 133MB/s	ATAIOSEL - ATA I/O Enable
1 - Enable SATA Spread Spectrum Clocking	1 - UDMA mode fixed by CNFG<2..0> pins		110 Host Mode - 150MB/s	1 - Enable output to ATA bus
0 - Disable SATA Spread Spectrum Clocking (Internal Pull-down)	0 - UDMA mode adjustable with Set Features (Internal Pull-up)		011 Reserved	0 - Disable output to ATA bus (Internal Pull-up)

Master: Link

### Serial ATA Bridge

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



# Page Notes

Power aliases required by this page:

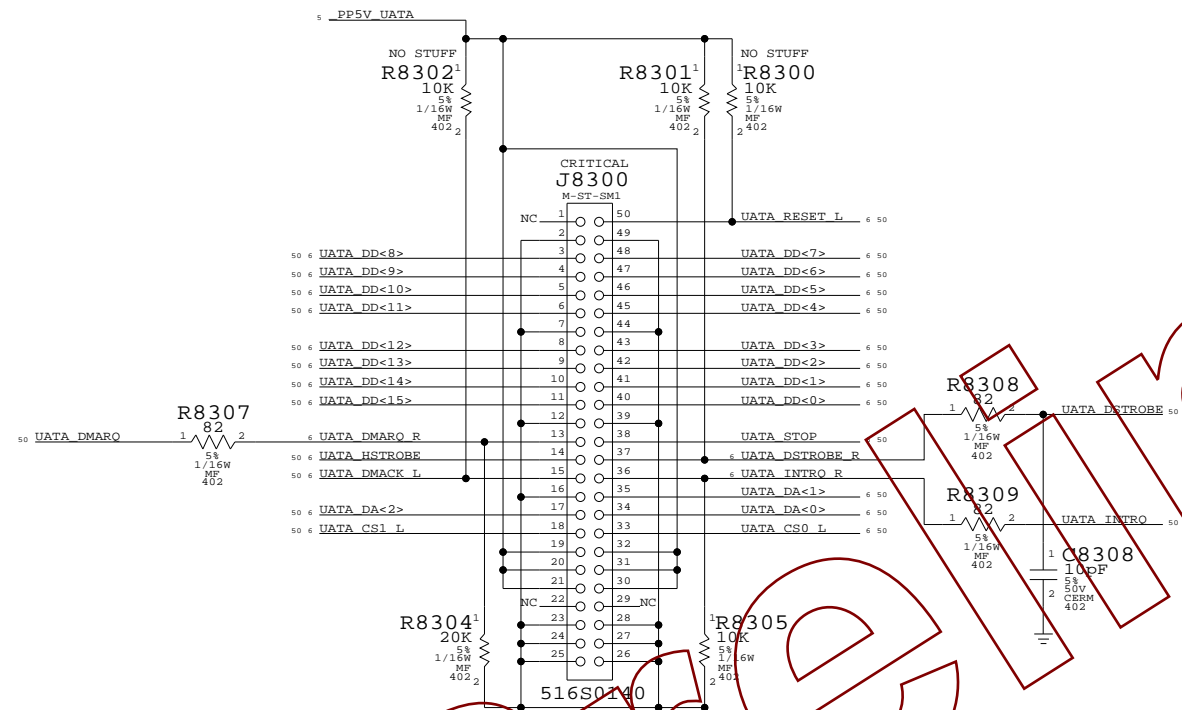
- \_PP5V\_PATA
- \_PP5V\_UATA
- \_PP3V3\_PATA
- \_PP3V3\_UATA

Signal aliases required by this page:  
(NONE)

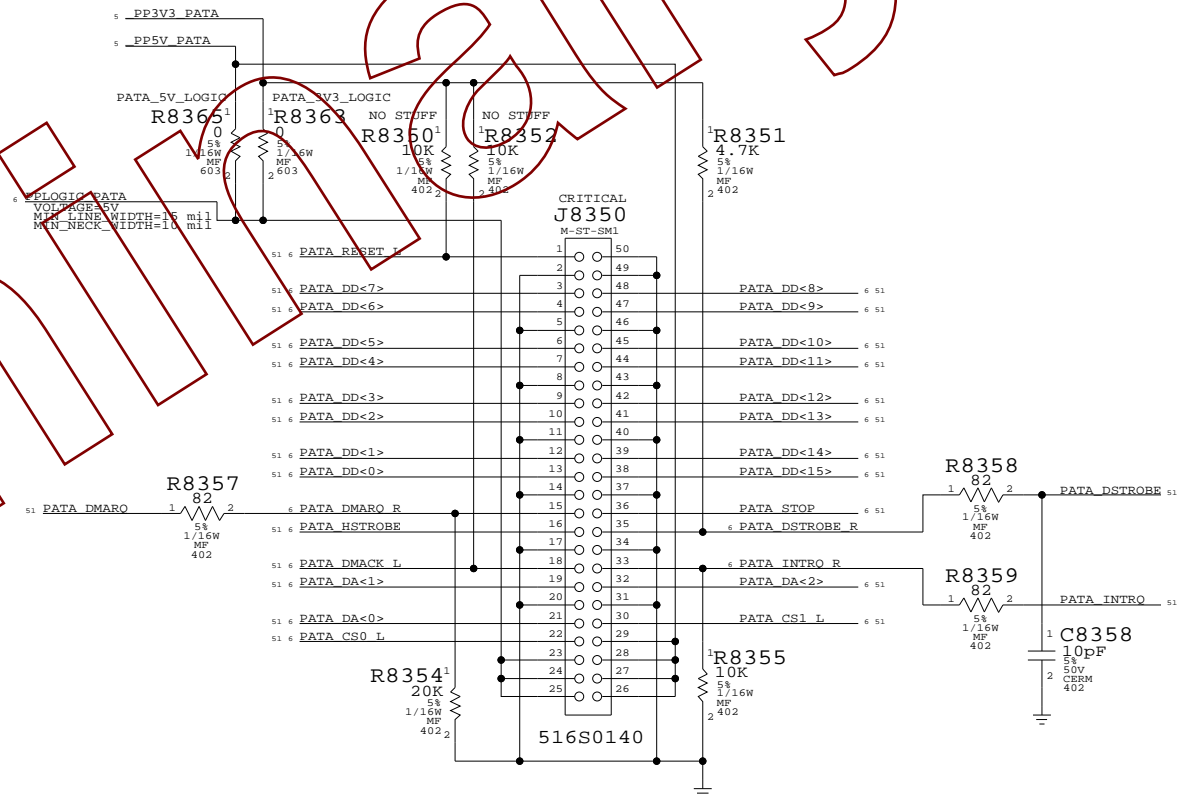
BOM options provided by this page:  
(NONE)

NOTE: ATA constraints are expected to be defined on another page (ATA host) and apply to this page via XNets.

## UATA (SouthBridge) Connector



## PATA (SATA Bridge) Connector



### IDE Connectors

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE	SHT	OF
NONE	83	103



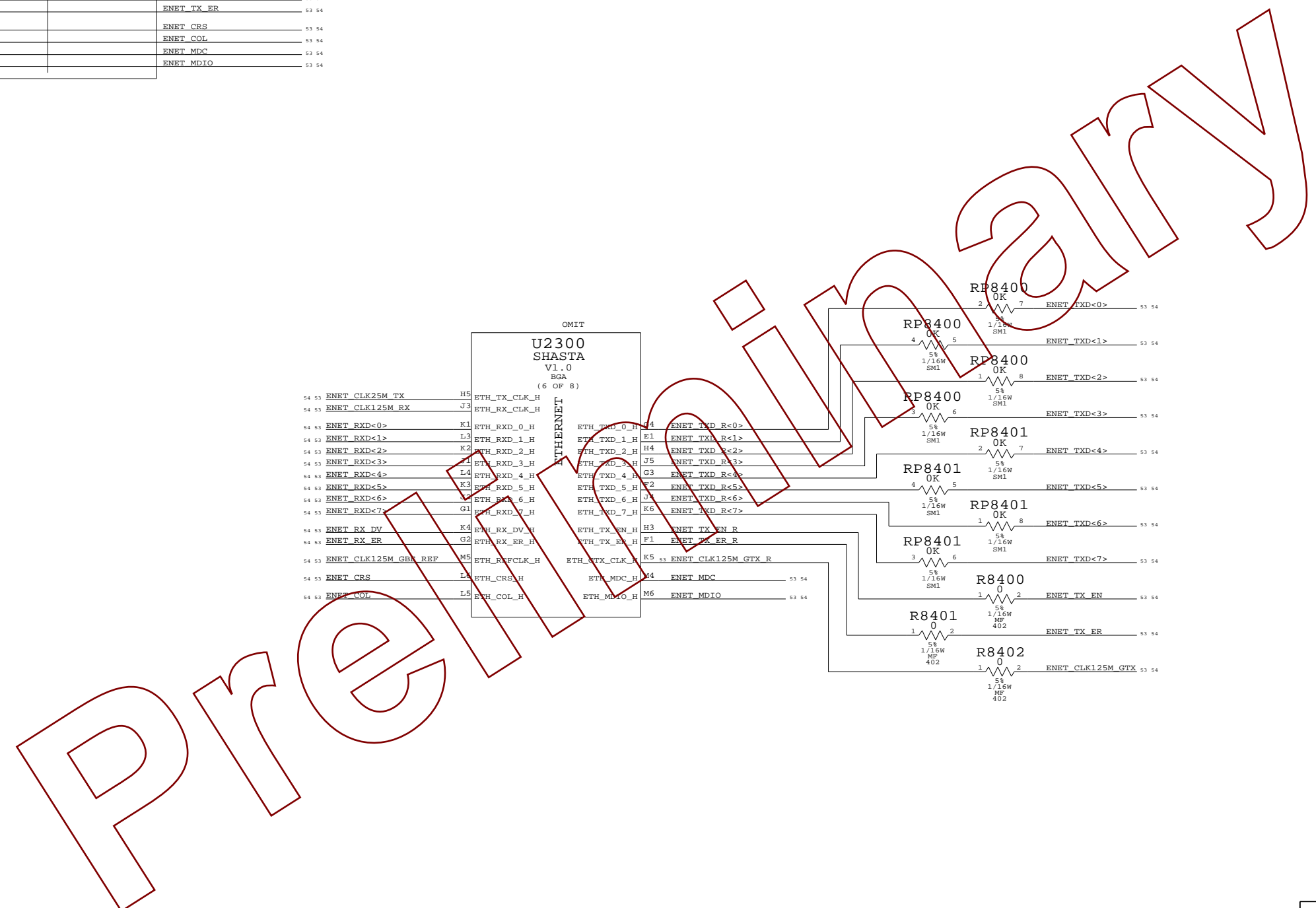
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK	ENET	15 MIL SPACING	ENET_CLK25M_TX
ENET_RX_CLK	ENET	15 MIL SPACING	ENET_CLK125M_RX
ENET_GBE_REF	ENET	15 MIL SPACING	ENET_CLK125M_GBE_REF
ENET_TX_CLK	ENET	15 MIL SPACING	ENET_CLK125M_GTX
	ENET	15 MIL SPACING	ENET_CLK125M_GTX_R
ENET_RX	ENET		ENET_RXD<7..0>
ENET_RX_CTL	ENET		ENET_RX_DV
ENET_RX_CTL	ENET		ENET_RX_ER
ENET_TX	ENET		ENET_TXD<7..0>
ENET_TX_CTL	ENET		ENET_TX_EN
ENET_TX_CTL	ENET		ENET_TX_ER
ENET_RX_CTL	ENET		ENET_CR5
ENET_RX_CTL	ENET		ENET_COL
ENET_MDC	ENET		ENET_MDC
ENET_MDIO	ENET		ENET_MDIO

Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



Master: Link

Shasta Ethernet

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	84	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	15 MIL SPACING	ENET_CLK125M_GBE_REF_R
	15 MIL SPACING	ENET_CLK125M_RX_R
	15 MIL SPACING	ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET_MDI0
ENET_MDI	ENET	ENET_MDI1
ENET_MDI	ENET	ENET_MDI2
ENET_MDI	ENET	ENET_MDI3
ENET_MDI	ENET	ENET_MDI0
ENET_MDI	ENET	ENET_MDI1
ENET_MDI	ENET	ENET_MDI2
ENET_MDI	ENET	ENET_MDI3
ENET_MDI	ENET	ENET_MDI0
ENET_MDI	ENET	ENET_MDI1
ENET_MDI	ENET	ENET_MDI2
ENET_MDI	ENET	ENET_MDI3
VESTA_CLK25M_XTAL	15 MIL SPACING	VESTA_CLK25M_XTALI
	15 MIL SPACING	VESTA_CLK25M_XTALO
	15 MIL SPACING	VESTA_CLK25M_XTALO_R

### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_ENET  
 - \_PP2V5\_ENETFW  
 - \_PPLV2\_ENETFW

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

Net Spacing Type: ENET  
 Line To Line: 15 mils  
 Length Tolerance: 50 mils  
 Primary Max Sep: 5 mils  
 Secondary Max Sep: 100 mils  
 Secondary Length: 500 mils

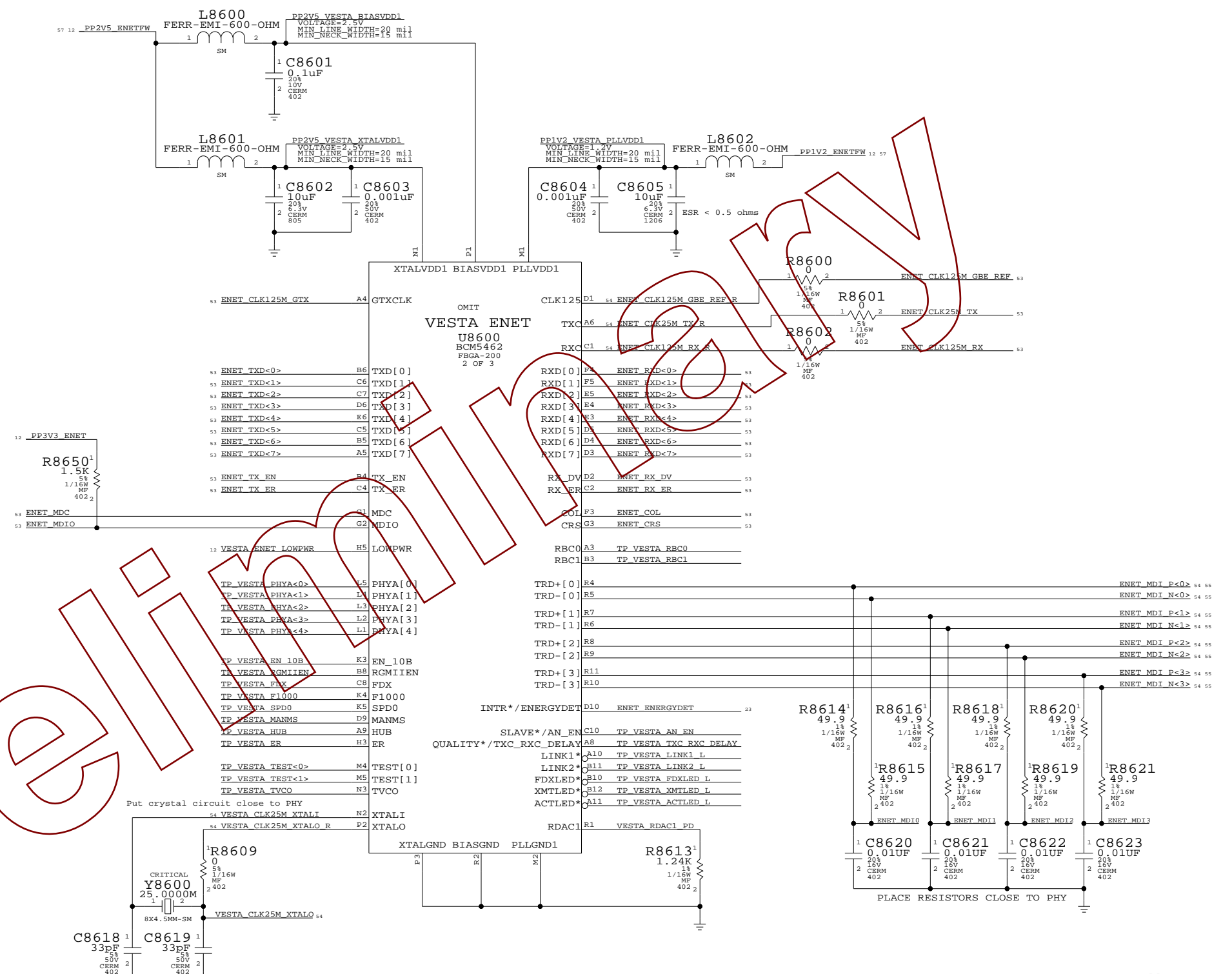
NOTE: Target differential impedance for ENET data pairs is 100 ohms.

#### Vesta Config Straps:

PHYA<4..0> - PHY Address Select (Internal Pull-downs)	MANMS - Manual Master/Slave Configuration Select Sets manual master/slave configuration enable bit (Internal Pull-down)
EN_10B - TBI Interface Select 1 - TBI/RTBI Mode 0 - GMII/RGMII Mode (Internal Pull-down)	HUB - Repeater Select Sets Hub/DTE bit and master/slave configuration value bit (Internal Pull-down)
RGMIIEN - RGMII Enable 1 - RGMII/RTBI Mode 0 - GMII/TBI Mode (Internal Pull-down)	ER - Edge Rate Select 1 - Rise time approx. 5 ns 0 - Rise time approx. 4 ns (Internal Pull-down)
FDX - Full-Duplex Select Sets manual duplex mode bit (Internal Pull-up)	AN_EN - Auto-Negotiation Select 1 - Auto-negotiation enabled 0 - Auto-negotiation disabled (Internal Pull-up)
F1000 - Speed Select See table below (Internal Pull-up)	TXC_RXC_DELAY 1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns 0 - No clock delay (Internal Pull-down)
SPD0 - Speed Select See table below (Internal Pull-down)	

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T



Master: Link

**Vesta Ethernet PHY**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	86	103	

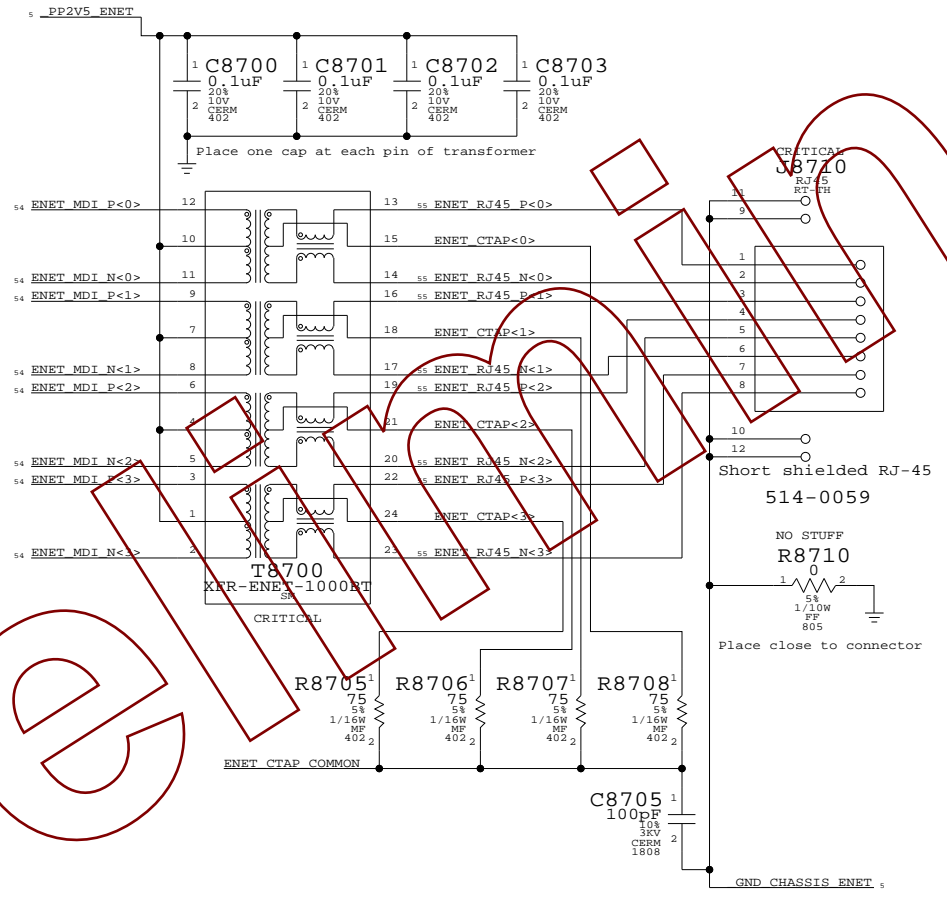
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PROVIDED	ENET	ENET_RJ45_0
	ENET	ENET_RJ45_1
	ENET	ENET_RJ45_2
BY	ENET	ENET_RJ45_3
	ENET	ENET_RJ45_4
	ENET	ENET_RJ45_5
ETHERNET	ENET	ENET_RJ45_6
	ENET	ENET_RJ45_7
	ENET	ENET_RJ45_8
PHY	ENET	ENET_RJ45_9
	ENET	ENET_RJ45_10
	ENET	ENET_RJ45_11

## Page Notes

Power aliases required by this page:  
 - \_PP2V5\_ENET  
 - \_GND\_CHASSIS\_ENET

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



Preview

## Ethernet Connector

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE		SHT	OF
NONE		87	103

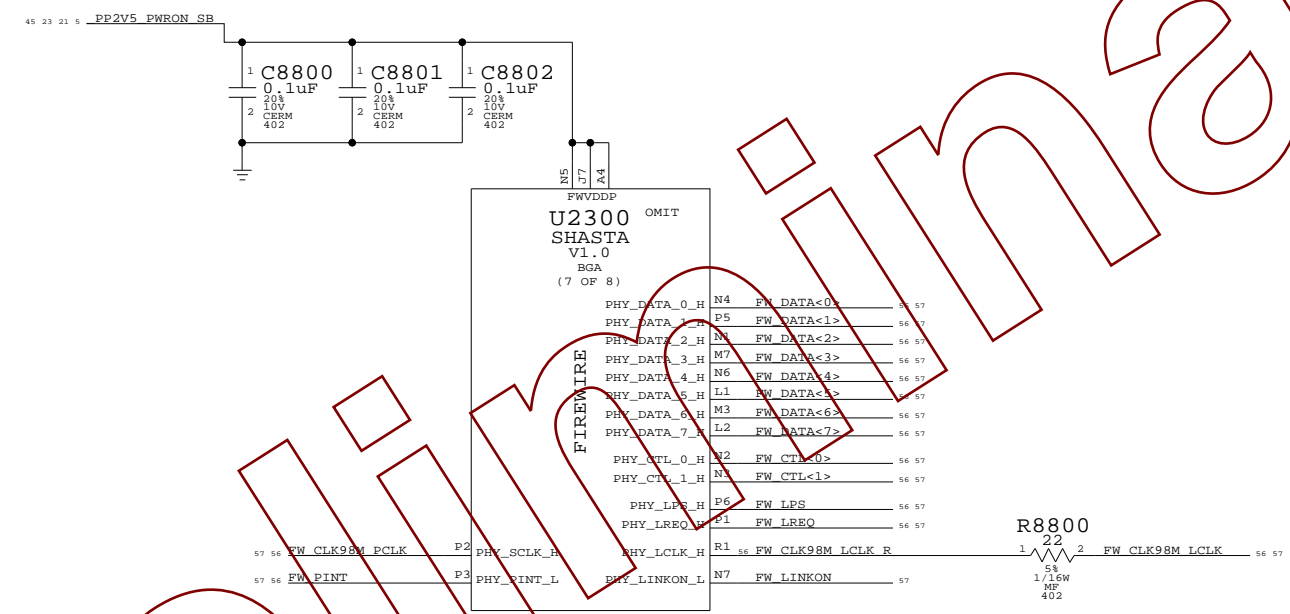
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW	FW		FW_DATA<7..0>
FW	FW		FW_CTL<1..0>
FW_LPS	FW		FW LPS
FW_LREQ	FW		FW LREQ
FW_PINT	FW		FW PINT
FW_LCLK	FW	15 MIL SPACING	FW CLK98M LCLK
FW_PCLK	FW	15 MIL SPACING	FW CLK98M PCLK
		15 MIL SPACING	FW CLK98M LCLK R

### Page Notes

Power aliases required by this page:  
 - \_PP2V5\_PWRON\_SB

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



Preliminary

Master: Link

### Shasta FireWire

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

\_DRAWING  
 TITLE=FIZZY  
 ABBREV=DRAWING  
 LAST\_MODIFIED=Mon Feb 23 19:08:06 2004

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6532	03
SCALE	SHT	OF	
NONE	88	103	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	15 MIL SPACING		FW_CLK98M_PCLK_R
FW_TPA1	FW	FW_TPA0	FW_TPA_P<0>
FW_TPA1	FW	FW_TPA0	FW_TPA_N<0>
FW_TPB1	FW	FW_TPB0	FW_TPB_P<0>
FW_TPB1	FW	FW_TPB0	FW_TPB_N<0>
FW_TPA2	FW	FW_TPA1	FW_TPA_P<1>
FW_TPA2	FW	FW_TPA1	FW_TPA_N<1>
FW_TPB2	FW	FW_TPB1	FW_TPB_P<1>
FW_TPB2	FW	FW_TPB1	FW_TPB_N<1>
FW_TPA3	FW	FW_TPA2	FW_TPA_P<2>
FW_TPA3	FW	FW_TPA2	FW_TPA_N<2>
FW_TPB3	FW	FW_TPB2	FW_TPB_P<2>
FW_TPB3	FW	FW_TPB2	FW_TPB_N<2>
VESTA_CLK24M_XTAL	15 MIL SPACING		VESTA_CLK24M_XTALI
	15 MIL SPACING		VESTA_CLK24M_XTALO
	15 MIL SPACING		VESTA_CLK24M_XTALO_R

### Page Notes

Power aliases required by this page:  
 - \_PPFW\_PHY  
 - \_PP3V3\_FW  
 - \_PP3V3\_ENETFW  
 - \_PP2V5\_ENETFW  
 - \_PP1V2\_ENETFW

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - VESTA\_DS\_ONLY\_EN0  
 If stuffed, adds external pull-up to counter internal pull-down in Vesta.  
 See straps table for more information.  
 - VESTA\_PWR\_CLASS\_0  
 If stuffed, adds external pull-down to counter internal pull-up in Vesta.  
 See straps table for more information.

**Net Spacing Type: FW**

Line To Line: 15 mils  
 Length Tolerance: 100 mils  
 Primary Max Sep: 7.5 mils  
 Secondary Max Sep: 100 mils  
 Secondary Length: 500 mils

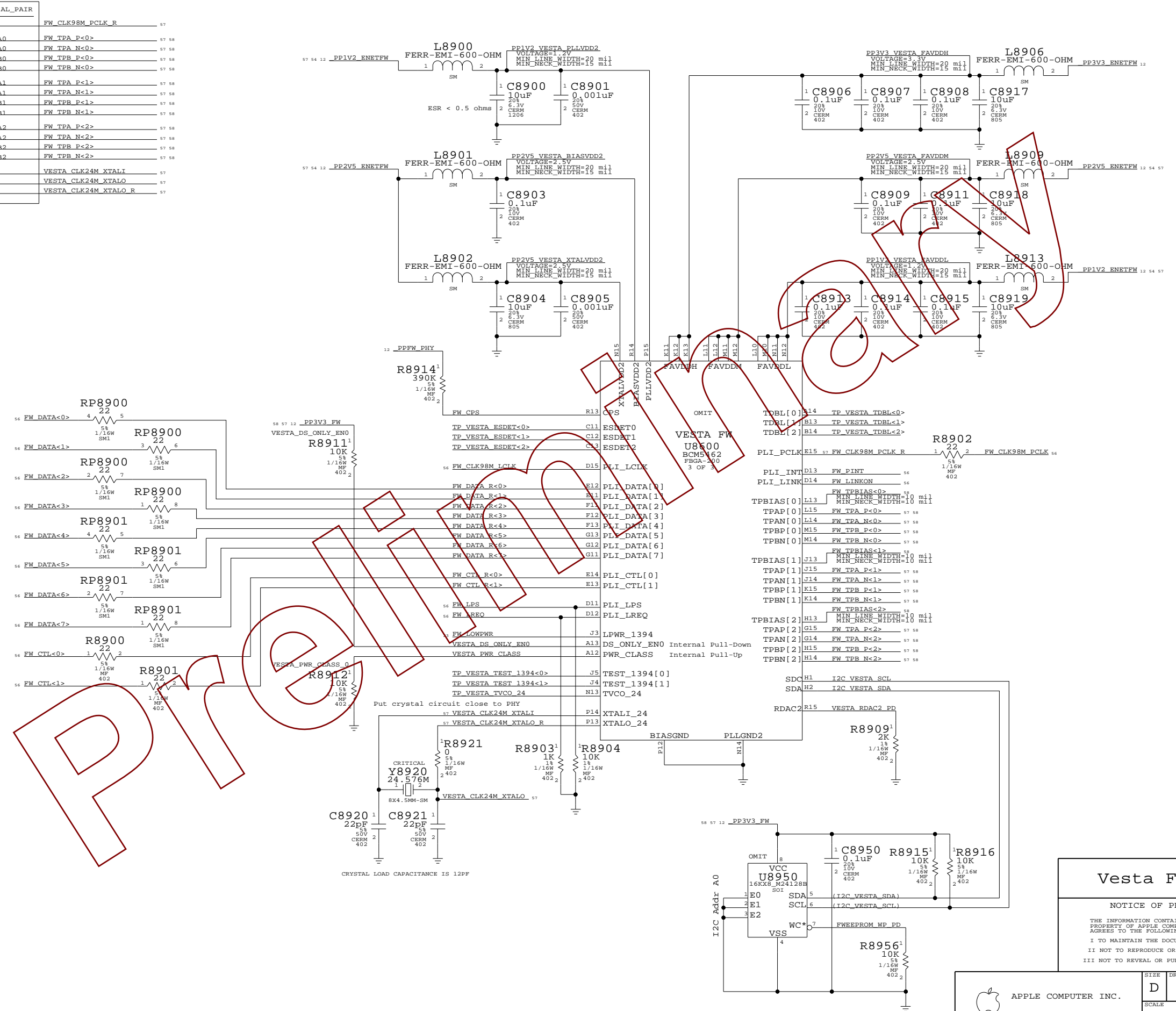
NOTE: Target differential impedance for FW data pairs is 110 ohms.

**Vesta Config Straps:**

PWR\_CLASS - FireWire Power Class  
 1 - Sets Power Class to 0x4  
 0 - Sets Power Class to 0x0  
 (Internal Pull-up)

DS\_ONLY\_EN0 - Port 0 Data/Strobe  
 1 - Port 0 Data/Strobe mode only  
 0 - Port 0 Bilingual mode  
 (Internal Pull-down)

\_DRAWING  
 TITLE=PIZZY  
 ABBREV=DRAWING  
 LAST\_MODIFIED=Mon Feb 23 19:08:14 2004



Master: Link

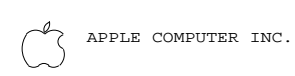
**Vesta FireWire PHY**

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE	SHT	OF
NONE	89	103



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PROVIDED	FW	FW_PORT1_TPA_FL, FW_PORT1_TPA_P_FL, FW_PORT1_TPA_N_FL, FW_PORT1_TPA_P_FL
BY	FW	FW_PORT1_TPB_FL, FW_PORT1_TPB_P_FL, FW_PORT1_TPB_N_FL, FW_PORT1_TPB_P_FL
PHY	FW	FW_PORT2_TPA_FL, FW_PORT2_TPA_P_FL, FW_PORT2_TPA_N_FL, FW_PORT2_TPA_P_FL
PAGE	FW	FW_PORT2_TPB_FL, FW_PORT2_TPB_P_FL, FW_PORT2_TPB_N_FL, FW_PORT2_TPB_P_FL

### Page Notes

Power aliases required by this page:  
 - \_PPFW\_PORT1  
 - \_PPFW\_PORT2  
 - \_PPFW\_PORT3  
 - \_PP3V3\_FW  
 - \_GND\_CHASSIS\_FW\_PORT1  
 - \_GND\_CHASSIS\_FW\_PORT2  
 - \_GND\_CHASSIS\_FW\_PORT3

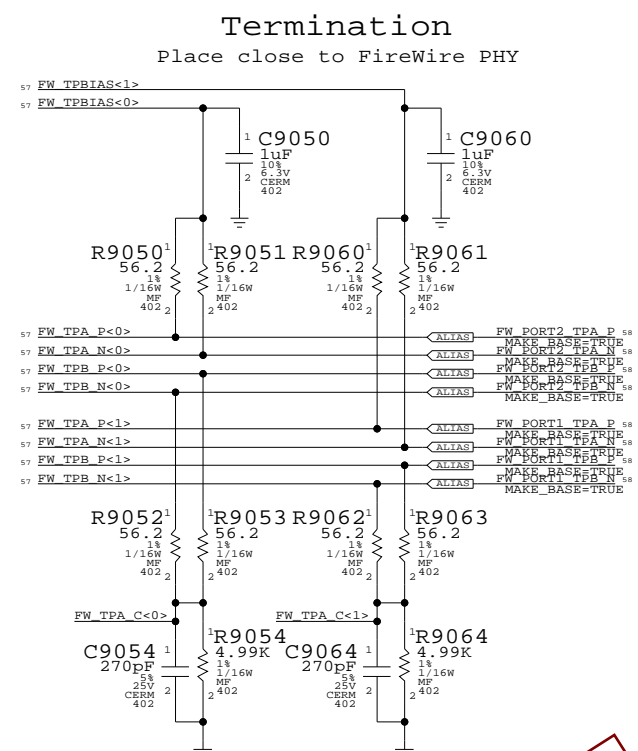
Signal aliases required by this page:  
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

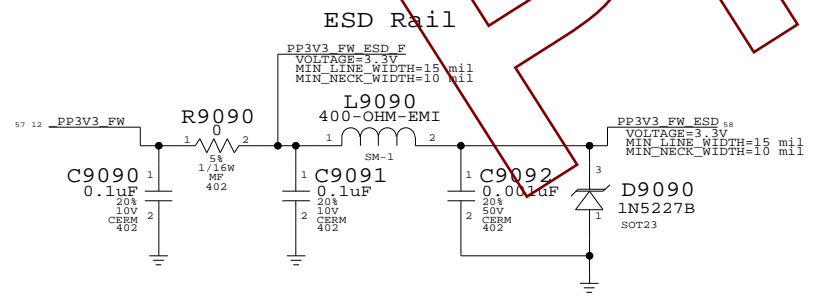
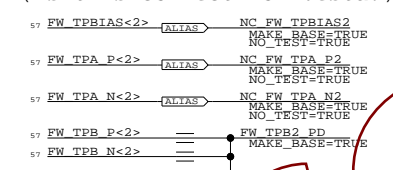
BOM options provided by this page:  
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

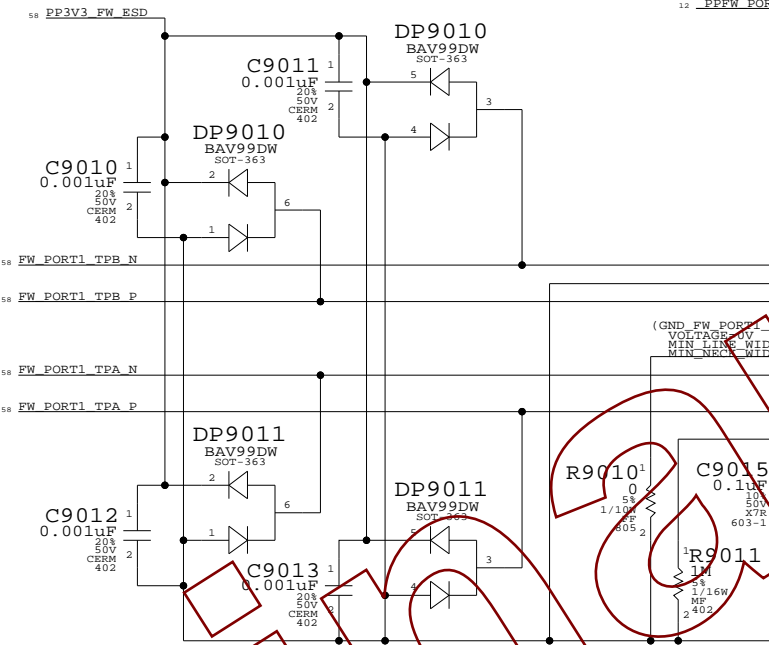
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



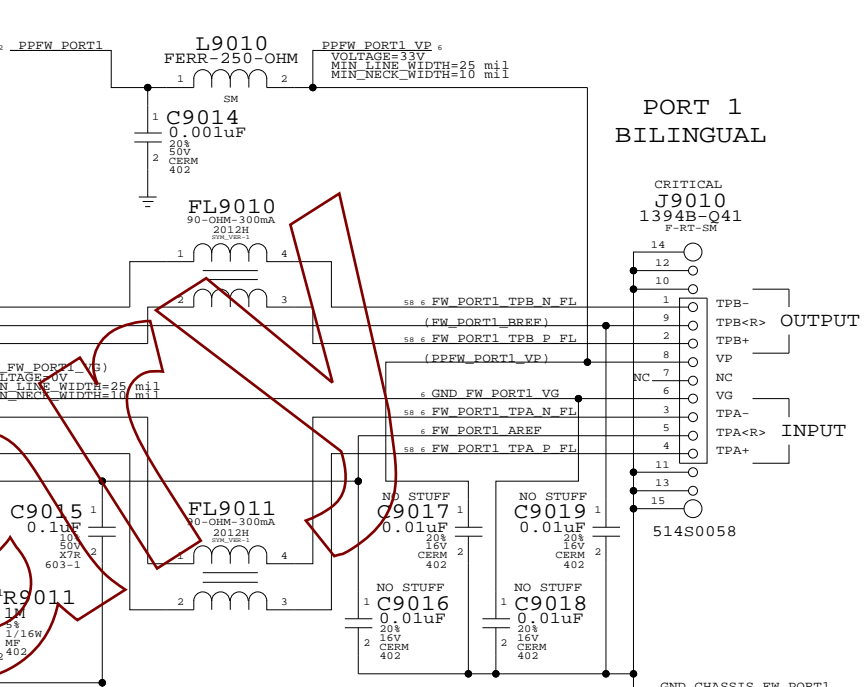
3rd TPA/TPB pair unused  
 (Is this correct for Vesta?)



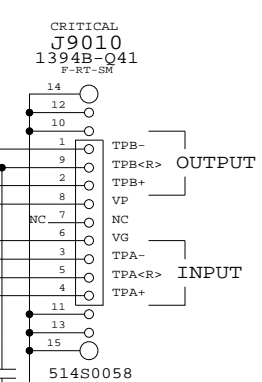
### "Snapback" & "Late VG" Protection



### Cable Power



### PORT 1 BILINGUAL

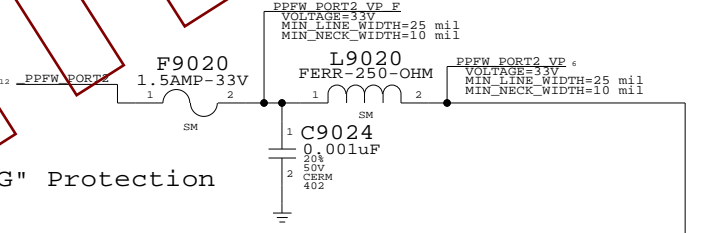


AREF needs to be isolated from all local grounds per 1394b spec

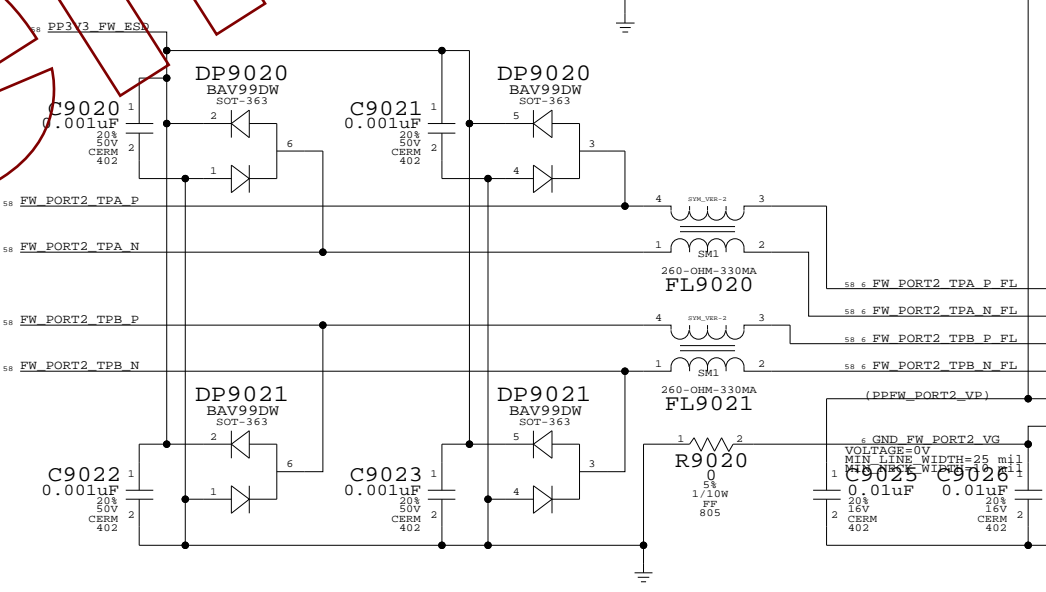
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

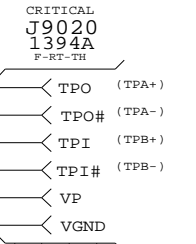
### Cable Power



### "Snapback" & "Late VG" Protection



### PORT 2 1394A



### FireWire Ports

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
USB2_0	USB2	USB2	USB2_P<0>
USB2_0	USB2	USB2	USB2_N<0>
USB2_1	USB2	USB2	USB2_P<1>
USB2_1	USB2	USB2	USB2_N<1>
USB2_2	USB2	USB2	USB2_P<2>
USB2_2	USB2	USB2	USB2_N<2>
USB2_3	USB2	USB2	USB2_P<3>
USB2_3	USB2	USB2	USB2_N<3>
USB2_4	USB2	USB2	USB2_P<4>
USB2_4	USB2	USB2	USB2_N<4>
USB2_NEC_XTAL	15 MIL SPACING	NEC_CLK30M_XT1	
	15 MIL SPACING	NEC_CLK30M_XT2	
	15 MIL SPACING	NEC_CLK30M_XT2_R	

### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PWRON\_USB

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

**Net Spacing Type: USB2**

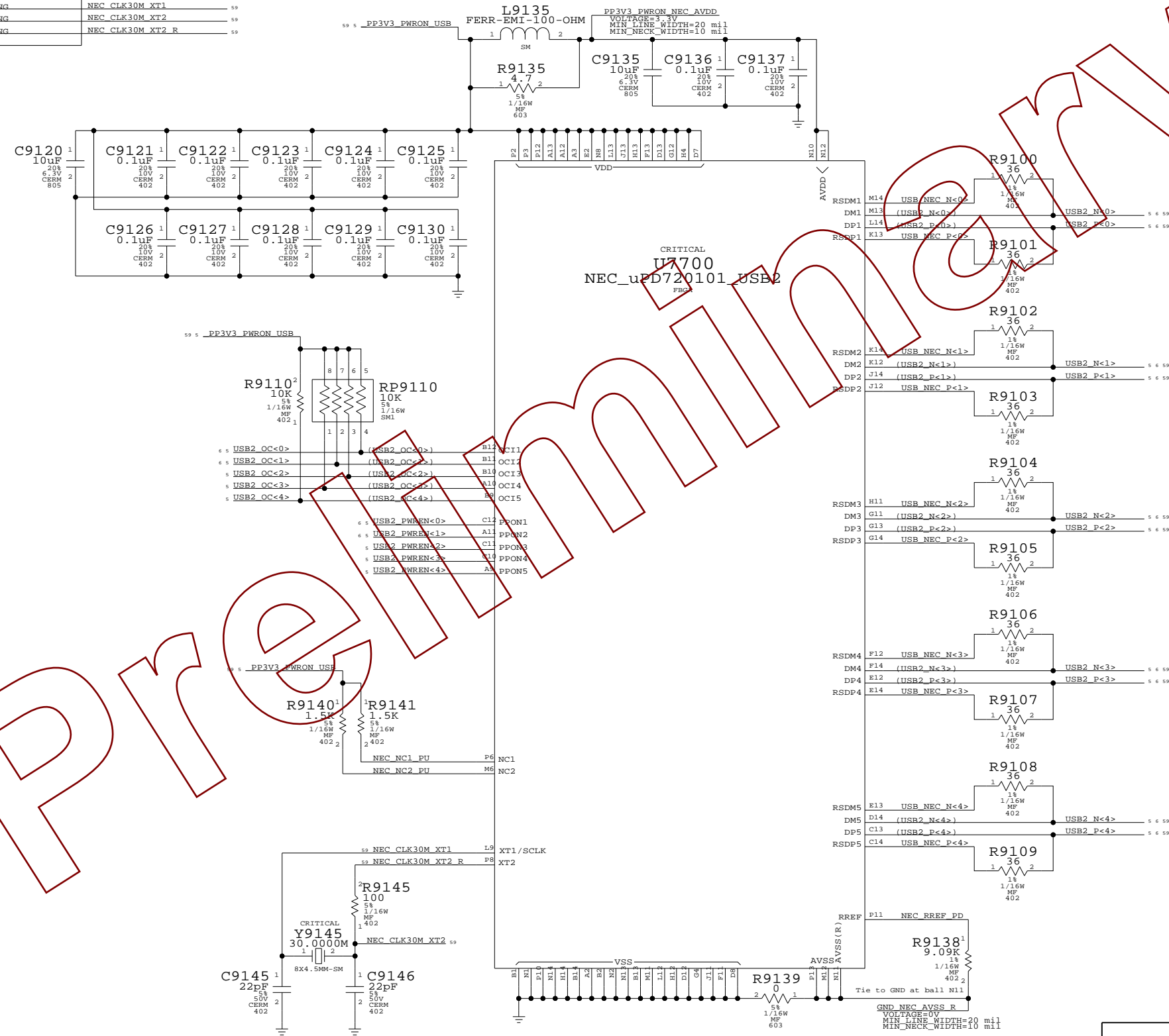
Line To Line: 19.5 mils  
 Length Tolerance: 50 mils  
 Primary Max Sep: 7.5 mils  
 Secondary Max Sep: 100 mils  
 Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

### U2300 SHASTA V1.0

BGA (8 OF 8)  
 OMIT

NC0	P7	TP_SB_NC_P7
NC1	P8	TP_SB_NC_P8
NC2	R3	TP_SB_NC_R3
NC3	R4	TP_SB_NC_R4
NC4	R5	TP_SB_NC_R5
NC5	R6	TP_SB_NC_R6
NC6	R7	TP_SB_NC_R7
NC7	R8	TP_SB_NC_R8
NC8	T1	TP_SB_NC_T1
NC9	T2	TP_SB_NC_T2
NC10	T3	TP_SB_NC_T3
NC11	T4	TP_SB_NC_T4
NC12	T5	TP_SB_NC_T5
NC13	T6	TP_SB_NC_T6
NC14	T7	TP_SB_NC_T7
NC15	T8	TP_SB_NC_T8
NC16	U1	TP_SB_NC_U1
NC17	U2	TP_SB_NC_U2
NC18	U3	TP_SB_NC_U3
NC19	U4	TP_SB_NC_U4
NC20	U5	TP_SB_NC_U5
NC21	U6	TP_SB_NC_U6
NC22	V1	TP_SB_NC_V1
NC23	V2	TP_SB_NC_V2
NC24	V3	TP_SB_NC_V3
NC25	V4	TP_SB_NC_V4
NC26	W1	TP_SB_NC_W1
NC27	W3	TP_SB_NC_W3
NC28	Y1	TP_SB_NC_Y1
NC29	Y3	TP_SB_NC_Y3



Preview

Master: Fizzy

### USB Host Interfaces

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

# Page Notes

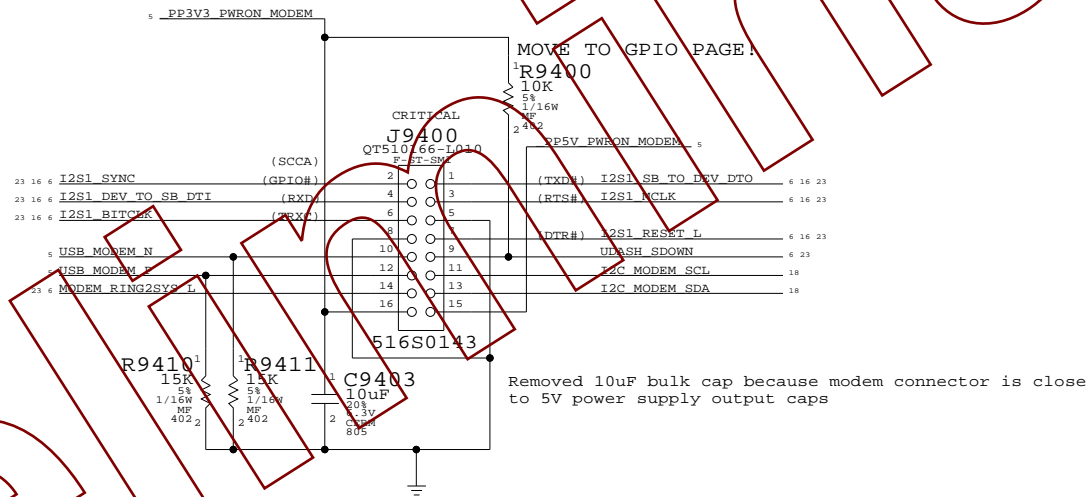
Power aliases required by this page:  
 - \_PP3V3\_PWRON\_MODEM  
 Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

## Modem Connector

Supports both The Last Dash and Q52 Modems



Preliminary

### Modem Interface

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-6532	03
SCALE	SHT	OF
NONE	94	103



# Page Notes

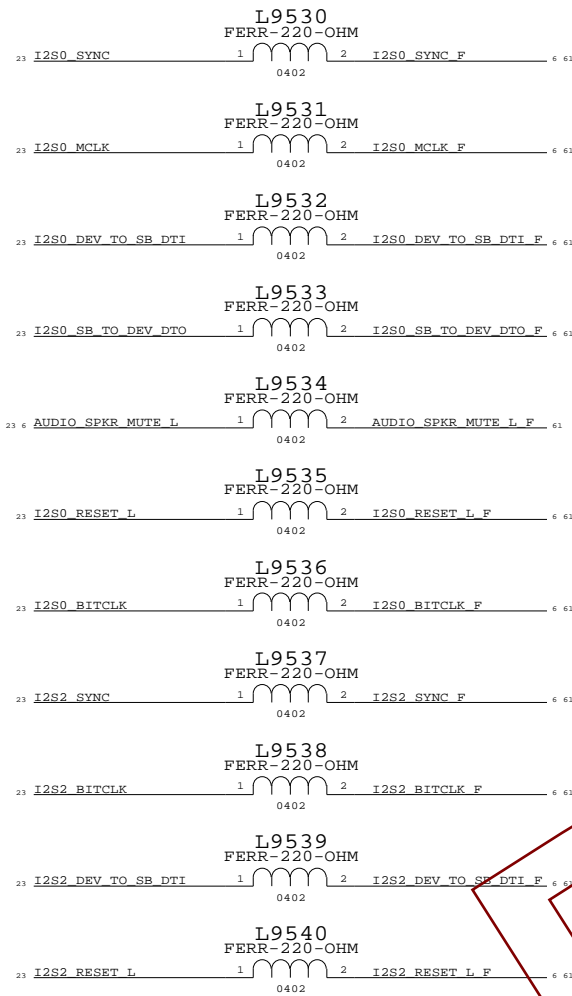
Power aliases required by this page:  
 - \_PP5V\_PWRON\_AUDIO  
 - \_PP3V3\_PWRON\_AUDIO

Signal aliases required by this page:  
 (NONE)

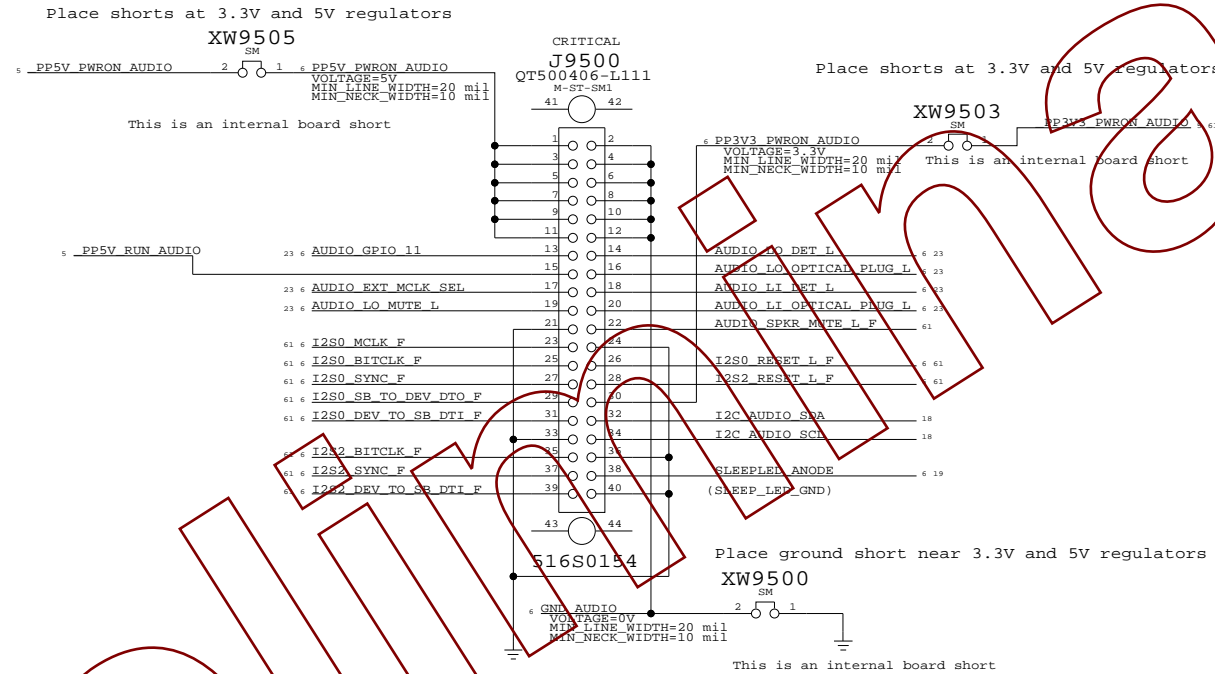
BOM options provided by this page:  
 (NONE)

NOTE: It is considered the responsibility of the audio section to provide the appropriate pull-ups and pull-downs for ALL audio GPIOs.

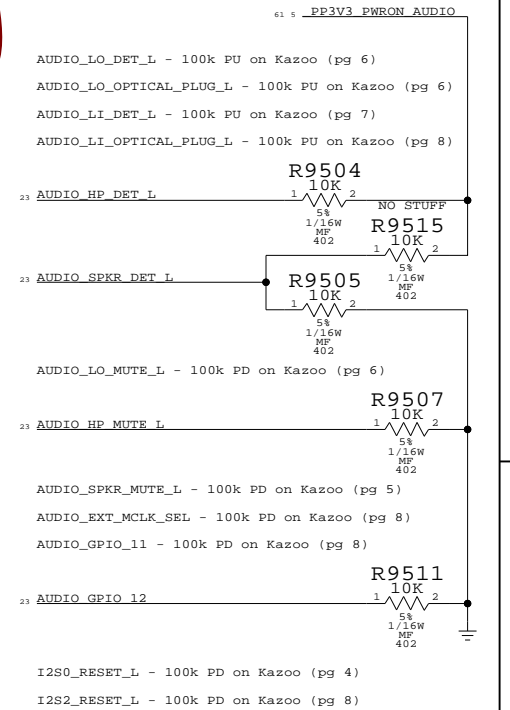
## EMI Filtering



## Sound Board Connector



## Audio GPIO Pull-ups & Pull-downs



## Audio Interface

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



# Electrical Constraints

No series termination on PCI signals

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	RAM_CAD	RAM_DQS_R<15..0>
	RAM_CAD	RAM_DQ_R<127..0>
	RAM_CAD	RAM_DQS<0>
RAM_DQS0	RAM_CAD	RAM_DQ<7..0>
RAM_DQS0	RAM_CAD	RAM_DQS<1>
RAM_DQS1	RAM_CAD	RAM_DQ<15..8>
RAM_DQS2	RAM_CAD	RAM_DQS<2>
RAM_DQS2	RAM_CAD	RAM_DQ<23..16>
RAM_DQS3	RAM_CAD	RAM_DQS<3>
RAM_DQS3	RAM_CAD	RAM_DQ<31..24>
RAM_DQS4	RAM_CAD	RAM_DQS<4>
RAM_DQS4	RAM_CAD	RAM_DQ<39..32>
RAM_DQS5	RAM_CAD	RAM_DQS<5>
RAM_DQS5	RAM_CAD	RAM_DQ<47..40>
RAM_DQS6	RAM_CAD	RAM_DQS<6>
RAM_DQS6	RAM_CAD	RAM_DQ<55..48>
RAM_DQS7	RAM_CAD	RAM_DQS<7>
RAM_DQS7	RAM_CAD	RAM_DQ<63..56>
RAM_DQS8	RAM_CAD	RAM_DQS<8>
RAM_DQS8	RAM_CAD	RAM_DQ<71..64>
RAM_DQS9	RAM_CAD	RAM_DQS<9>
RAM_DQS9	RAM_CAD	RAM_DQ<79..72>
RAM_DQS10	RAM_CAD	RAM_DQS<10>
RAM_DQS10	RAM_CAD	RAM_DQ<87..80>
RAM_DQS11	RAM_CAD	RAM_DQS<11>
RAM_DQS11	RAM_CAD	RAM_DQ<95..88>
RAM_DQS12	RAM_CAD	RAM_DQS<12>
RAM_DQS12	RAM_CAD	RAM_DQ<103..96>
RAM_DQS13	RAM_CAD	RAM_DQS<13>
RAM_DQS13	RAM_CAD	RAM_DQ<111..104>
RAM_DQS14	RAM_CAD	RAM_DQS<14>
RAM_DQS14	RAM_CAD	RAM_DQ<119..112>
RAM_DQS15	RAM_CAD	RAM_DQS<15>
RAM_DQS15	RAM_CAD	RAM_DQ<127..120>

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	RAM_CLK	RAM_CLK_A_P_R
	RAM_CLK	RAM_CLK_A_N_R
	RAM_CLK	RAM_CLK_B_P_R
	RAM_CLK	RAM_CLK_B_N_R
	RAM_CLK	RAM_CLK_D_P_R
	RAM_CLK	RAM_CLK_D_N_R
	RAM_CLK	RAM_CLK_E_P_R
	RAM_CLK	RAM_CLK_E_N_R
RAM_CLK0	RAM_CLK	RAM_CLK_A_P
RAM_CLK0	RAM_CLK	RAM_CLK_A_N
RAM_CLK0	RAM_CLK	RAM_CLK_B_P
RAM_CLK0	RAM_CLK	RAM_CLK_B_N
RAM_CLK1	RAM_CLK	RAM_CLK_D_P
RAM_CLK1	RAM_CLK	RAM_CLK_D_N
RAM_CLK1	RAM_CLK	RAM_CLK_E_P
RAM_CLK1	RAM_CLK	RAM_CLK_E_N
	RAM_CAD	RAM_CKE_R<1..0>
	RAM_CAD	RAM_CKE_R<5..4>
RAM_CKE0	RAM_CAD	RAM_CKE<0>
RAM_CKE0	RAM_CAD	RAM_CKE<1>
RAM_CKE1	RAM_CAD	RAM_CKE<4>
RAM_CKE1	RAM_CAD	RAM_CKE<5>
	RAM_CAD	RAM_CS_L_R<1..0>
	RAM_CAD	RAM_CS_L_R<9..8>
RAM_CS0	RAM_CAD	RAM_CS_L<0>
RAM_CS0	RAM_CAD	RAM_CS_L<1>
RAM_CS1	RAM_CAD	RAM_CS_L<8>
RAM_CS1	RAM_CAD	RAM_CS_L<9>
	RAM_CAD	RAM_A_R<13..0>
RAM_A_CTL	RAM_CAD	RAM_BA_R<1..0>
RAM_A_CTL	RAM_CAD	RAM_RAS_L_R
RAM_A_CTL	RAM_CAD	RAM_CAS_L_R
RAM_A_CTL	RAM_CAD	RAM_WE_L_R
RAM_A_CTL	RAM_CAD	RAM_A<13..0>
RAM_A_CTL	RAM_CAD	RAM_BA_R<1..0>
RAM_A_CTL	RAM_CAD	RAM_RAS_L_R
RAM_A_CTL	RAM_CAD	RAM_CAS_L_R
RAM_A_CTL	RAM_CAD	RAM_WE_L_R

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	TMDS	TMDS_D0
	TMDS	TMDS_DP<0>
	TMDS	TMDS_DN<0>
	TMDS	TMDS_D1
	TMDS	TMDS_DP<1>
	TMDS	TMDS_DN<1>
	TMDS	TMDS_D2
	TMDS	TMDS_DP<2>
	TMDS	TMDS_DN<2>
	TMDS	TMDS_CLK
	TMDS	TMDS_CLKP
	TMDS	TMDS_CLKN
	TMDS	TMDS_D3
	TMDS	TMDS_DP<3>
	TMDS	TMDS_DN<3>
	TMDS	TMDS_D4
	TMDS	TMDS_DP<4>
	TMDS	TMDS_DN<4>
	TMDS	TMDS_D5
	TMDS	TMDS_DP<5>
	TMDS	TMDS_DN<5>
	CONN_TMDS	CONN_TMDS_D0
	CONN_TMDS	CONN_TMDS_DP<0>
	CONN_TMDS	CONN_TMDS_DN<0>
	CONN_TMDS	CONN_TMDS_D1
	CONN_TMDS	CONN_TMDS_DP<1>
	CONN_TMDS	CONN_TMDS_DN<1>
	CONN_TMDS	CONN_TMDS_D2
	CONN_TMDS	CONN_TMDS_DP<2>
	CONN_TMDS	CONN_TMDS_DN<2>
	CONN_TMDS	CONN_TMDS_D3
	CONN_TMDS	CONN_TMDS_DP<3>
	CONN_TMDS	CONN_TMDS_DN<3>
	CONN_TMDS	CONN_TMDS_D4
	CONN_TMDS	CONN_TMDS_DP<4>
	CONN_TMDS	CONN_TMDS_DN<4>
	CONN_TMDS	CONN_TMDS_D5
	CONN_TMDS	CONN_TMDS_DP<5>
	CONN_TMDS	CONN_TMDS_DN<5>
	SI_TMDS	SI_TMDS_D0
	SI_TMDS	SI_TMDS_DP<0>
	SI_TMDS	SI_TMDS_DN<0>
	SI_TMDS	SI_TMDS_D1
	SI_TMDS	SI_TMDS_DP<1>
	SI_TMDS	SI_TMDS_DN<1>
	SI_TMDS	SI_TMDS_D2
	SI_TMDS	SI_TMDS_DP<2>
	SI_TMDS	SI_TMDS_DN<2>
	SI_TMDS	SI_TMDS_CLK
	SI_TMDS	SI_TMDS_CLKP
	SI_TMDS	SI_TMDS_CLKN
	SI_TMDS	SI_TMDS_D3
	SI_TMDS	SI_TMDS_DP<3>
	SI_TMDS	SI_TMDS_DN<3>
	SI_TMDS	SI_TMDS_D4
	SI_TMDS	SI_TMDS_DP<4>
	SI_TMDS	SI_TMDS_DN<4>
	SI_TMDS	SI_TMDS_D5
	SI_TMDS	SI_TMDS_DP<5>
	SI_TMDS	SI_TMDS_DN<5>
	GPU_TMDS	GPU_TMDS_D0
	GPU_TMDS	GPU_TMDS_DP<0>
	GPU_TMDS	GPU_TMDS_DN<0>
	GPU_TMDS	GPU_TMDS_D1
	GPU_TMDS	GPU_TMDS_DP<1>
	GPU_TMDS	GPU_TMDS_DN<1>
	GPU_TMDS	GPU_TMDS_D2
	GPU_TMDS	GPU_TMDS_DP<2>
	GPU_TMDS	GPU_TMDS_DN<2>
	GPU_TMDS	GPU_TMDS_CLK
	GPU_TMDS	GPU_TMDS_CLKP
	GPU_TMDS	GPU_TMDS_CLKN
	GPU_TMDS	GPU_TMDS_D0_R
	GPU_TMDS	GPU_TMDS_DP_R<0>
	GPU_TMDS	GPU_TMDS_DN_R<0>
	GPU_TMDS	GPU_TMDS_D1_R
	GPU_TMDS	GPU_TMDS_DP_R<1>
	GPU_TMDS	GPU_TMDS_DN_R<1>
	GPU_TMDS	GPU_TMDS_D2_R
	GPU_TMDS	GPU_TMDS_DP_R<2>
	GPU_TMDS	GPU_TMDS_DN_R<2>
	GPU_TMDS	GPU_TMDS_CLK_R
	GPU_TMDS	GPU_TMDS_CLKP_R
	GPU_TMDS	GPU_TMDS_CLKN_R

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK		EI_CPU_TO_NB_CLK_P
EI_CPU_TO_NB_CLK		EI_CPU_TO_NB_CLK_N
EI_NB_TO_CPU_CLK		EI_NB_TO_CPU_CLK_P
EI_NB_TO_CPU_CLK		EI_NB_TO_CPU_CLK_N
EI_CPU_NB_DATA		EI_CPU_TO_NB_AD<43..0>
EI_NB_CPU_DATA		EI_NB_TO_CPU_AD<43..0>
EI_CPU_TO_NB_CAD		EI_CPU_TO_NB_SR_P<0>
EI_CPU_TO_NB_CAD		EI_CPU_TO_NB_SR_N<0>
EI_CPU_TO_NB_CAD		EI_CPU_TO_NB_SR_P<1>
EI_CPU_TO_NB_CAD		EI_CPU_TO_NB_SR_N<1>
EI_NB_TO_CPU_CAD		EI_NB_TO_CPU_SR_P<0>
EI_NB_TO_CPU_CAD		EI_NB_TO_CPU_SR_N<0>
EI_NB_TO_CPU_CAD		EI_NB_TO_CPU_SR_P<1>
EI_NB_TO_CPU_CAD		EI_NB_TO_CPU_SR_N<1>

PCI_SB_AD<0>	ALIAS	PCI_AD<0>	MAKE_BASE=TRUE
PCI_SB_AD<1>	ALIAS	PCI_AD<1>	MAKE_BASE=TRUE
PCI_SB_AD<2>	ALIAS	PCI_AD<2>	MAKE_BASE=TRUE
PCI_SB_AD<3>	ALIAS	PCI_AD<3>	MAKE_BASE=TRUE
PCI_SB_AD<4>	ALIAS	PCI_AD<4>	MAKE_BASE=TRUE
PCI_SB_AD<5>	ALIAS	PCI_AD<5>	MAKE_BASE=TRUE
PCI_SB_AD<6>	ALIAS	PCI_AD<6>	MAKE_BASE=TRUE
PCI_SB_AD<7>	ALIAS	PCI_AD<7>	MAKE_BASE=TRUE
PCI_SB_AD<8>	ALIAS	PCI_AD<8>	MAKE_BASE=TRUE
PCI_SB_AD<9>	ALIAS	PCI_AD<9>	MAKE_BASE=TRUE
PCI_SB_AD<10>	ALIAS	PCI_AD<10>	MAKE_BASE=TRUE
PCI_SB_AD<11>	ALIAS	PCI_AD<11>	MAKE_BASE=TRUE
PCI_SB_AD<12>	ALIAS	PCI_AD<12>	MAKE_BASE=TRUE
PCI_SB_AD<13>	ALIAS	PCI_AD<13>	MAKE_BASE=TRUE
PCI_SB_AD<14>	ALIAS	PCI_AD<14>	MAKE_BASE=TRUE
PCI_SB_AD<15>	ALIAS	PCI_AD<15>	MAKE_BASE=TRUE
PCI_SB_AD<16>	ALIAS	PCI_AD<16>	MAKE_BASE=TRUE
PCI_SB_AD<17>	ALIAS	PCI_AD<17>	MAKE_BASE=TRUE
PCI_SB_AD<18>	ALIAS	PCI_AD<18>	MAKE_BASE=TRUE
PCI_SB_AD<19>	ALIAS	PCI_AD<19>	MAKE_BASE=TRUE
PCI_SB_AD<20>	ALIAS	PCI_AD<20>	MAKE_BASE=TRUE
PCI_SB_AD<21>	ALIAS	PCI_AD<21>	MAKE_BASE=TRUE
PCI_SB_AD<22>	ALIAS	PCI_AD<22>	MAKE_BASE=TRUE
PCI_SB_AD<23>	ALIAS	PCI_AD<23>	MAKE_BASE=TRUE
PCI_SB_AD<24>	ALIAS	PCI_AD<24>	MAKE_BASE=TRUE
PCI_SB_AD<25>	ALIAS	PCI_AD<25>	MAKE_BASE=TRUE
PCI_SB_AD<26>	ALIAS	PCI_AD<26>	MAKE_BASE=TRUE
PCI_SB_AD<27>	ALIAS	PCI_AD<27>	MAKE_BASE=TRUE
PCI_SB_AD<28>	ALIAS	PCI_AD<28>	MAKE_BASE=TRUE
PCI_SB_AD<29>	ALIAS	PCI_AD<29>	MAKE_BASE=TRUE
PCI_SB_AD<30>	ALIAS	PCI_AD<30>	MAKE_BASE=TRUE
PCI_SB_AD<31>	ALIAS	PCI_AD<31>	MAKE_BASE=TRUE
PCI_SB_CBE_L<0>	ALIAS	PCI_CBE_L<0>	MAKE_BASE=TRUE
PCI_SB_CBE_L<1>	ALIAS	PCI_CBE_L<1>	MAKE_BASE=TRUE
PCI_SB_CBE_L<2>	ALIAS	PCI_CBE_L<2>	MAKE_BASE=TRUE
PCI_SB_CBE_L<3>	ALIAS	PCI_CBE_L<3>	MAKE_BASE=TRUE
PCI_SB_DEVSEL_L		PCI_DEVSEL_L	MAKE_BASE=TRUE
PCI_SB_FRAME_L		PCI_FRAME_L	MAKE_BASE=TRUE
PCI_SB_IRDY_L		PCI_IRDY_L	MAKE_BASE=TRUE
PCI_SB_TRDY_L		PCI_TRDY_L	MAKE_BASE=TRUE
PCI_SB_STOP_L		PCI_STOP_L	MAKE_BASE=TRUE
PCI_SB_PAR		PCI_PAR	MAKE_BASE=TRUE



**Electrical Constraints**

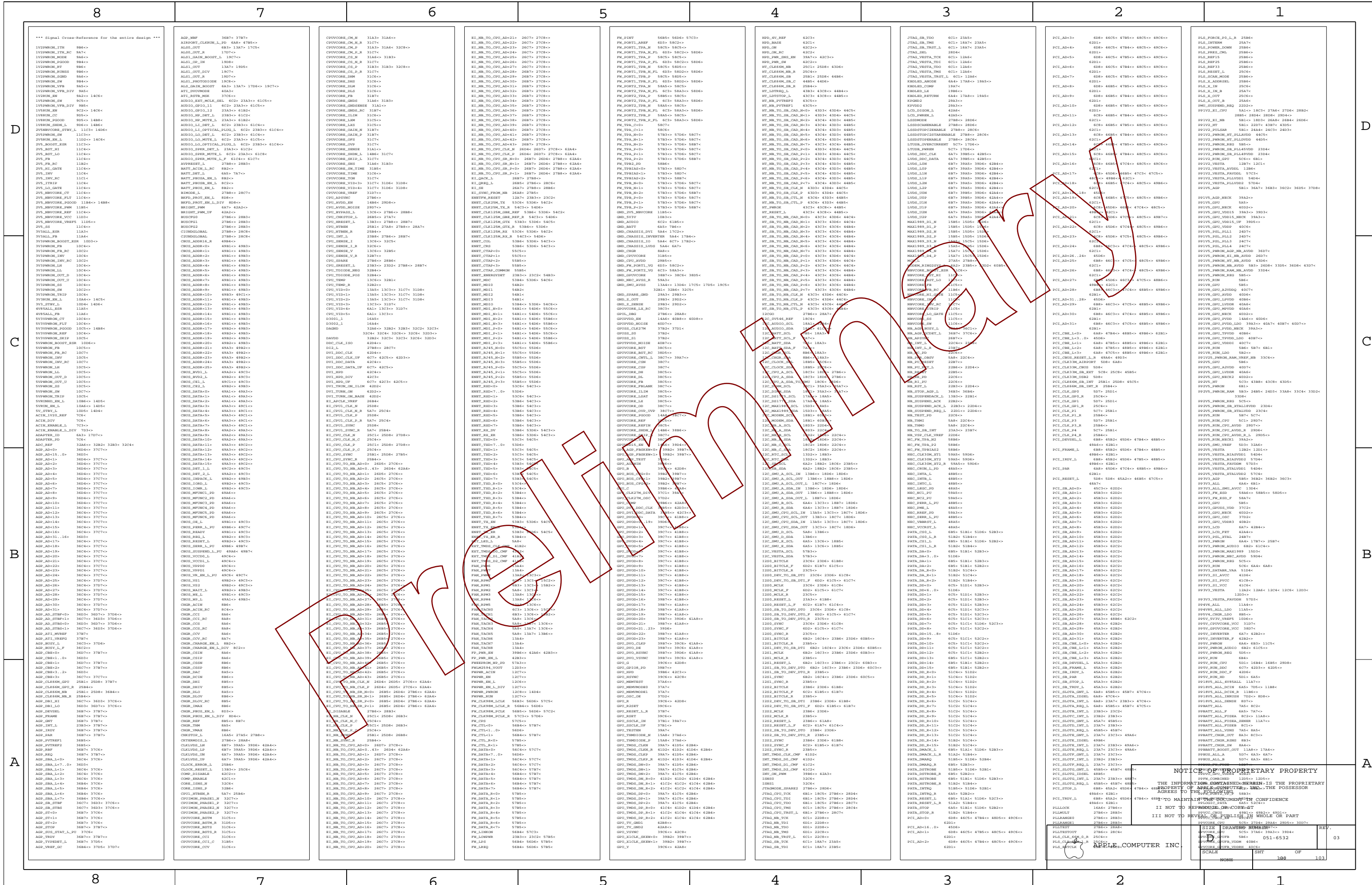
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC., THE POSSESSOR OF WHICH IS

III NOT TO REPRODUCE OR COPIE IT IN ANY MANNER WITHOUT THE WRITTEN PERMISSION OF APPLE COMPUTER, INC.

SCALE SHEET OF 103

A

A

B

B

C

C

D

D

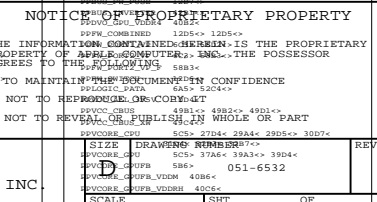
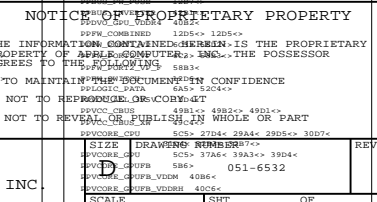




Table with 8 columns and 26 rows. Each cell contains alphanumeric codes and symbols. A large red watermark 'APPLE' is oriented diagonally across the center of the page.

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

Table with 3 columns: SIZE, DRAWING NUMBER, REV.
Row 1: D, 051-6532, 03
Row 2: SCALE, NONE; SHEET, 101; OF, 103



APPLE COMPUTER, INC.



Main grid with columns 8 to 1 and rows A to D. Each cell contains a list of component identifiers (e.g., 85510 PCB\_STANDOFF 17, C1280 CAP 12) and their corresponding quantities. A large diagonal watermark 'SAMPLE' is overlaid across the grid.

NOTICE OF PROPRIETARY PROPERTY  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF ARBOR COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

Scale and Drawing Information Table

SCALE	SHEET	OF	REV.
NONE	102	103	03

