

8

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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IMAC 5,2 -- REV A

7/25/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
A		451207	PRODUCTION RELEASED		
				DATE	DATE
				07/26/06	06/22/04

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
5	5	FUNC TEST 1 OF 2	MASTER	MASTER	
6	6	Power Conn / Alias	MASTER	MASTER	
7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006	
12	12	NB CPU Interface	M1	01/05/2006	
13	13	NB PEG / Video Interfaces	M1	01/05/2006	
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1	01/05/2006	
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40	01/05/2006	
18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector	AMASTER	MASTER	
29	29	DDR2 SO-DIMM Connector	BMASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUI	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	



DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTR	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		TITLE		DRAWING NUMBER	
				051-7199	
				REV. A	
				SHT 1 OF 97	

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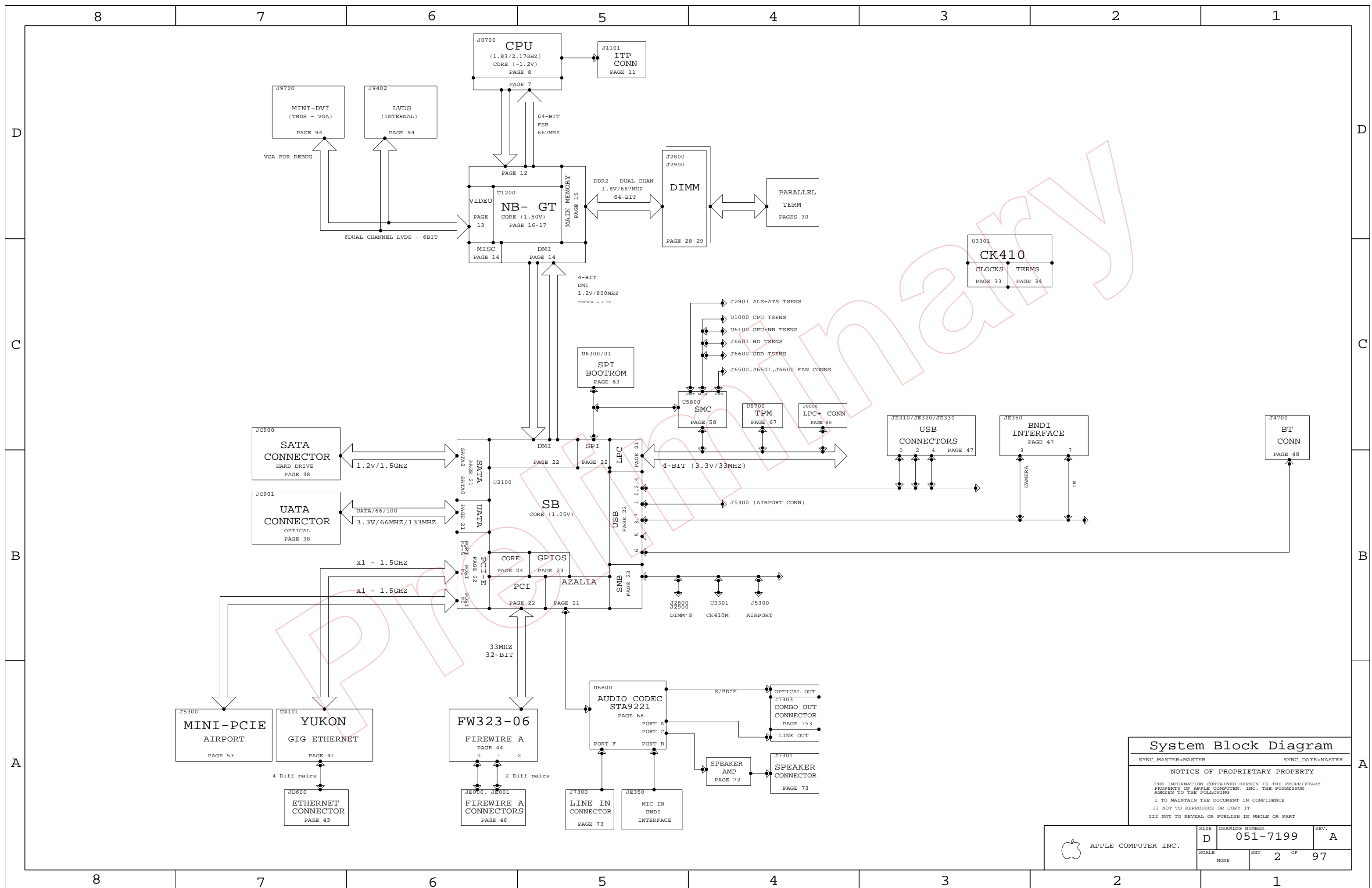
5

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1



System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

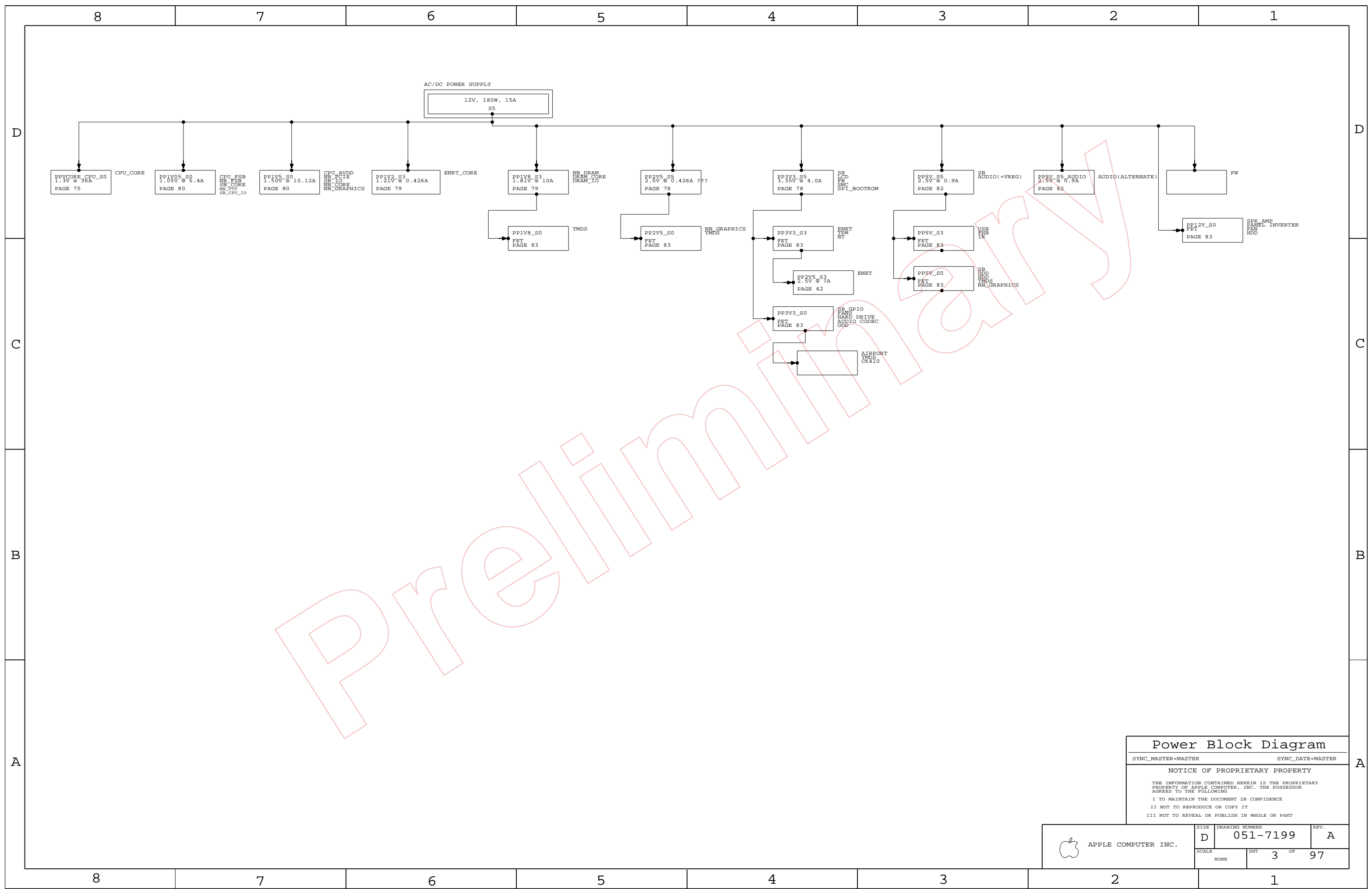
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	D	051-7199	A
SCALE	SHT	OF	REV.
NONE	2	97	



Preliminary

Power Block Diagram

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 3	OF 97

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1461	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7199	1	PCB,SCHEM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0042	1	EFI ROM,M50A	U6301	CRITICAL	
337S3386	1	M50 MEROM CPU	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1465	353S1461		U7500	CPU VREG, OLD DIE, SCREENED PART
124-0338	124-0333		C7953,C7954	FOR SUPPLY

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50A	[EEE:WJ9]	CRITICAL	MEROM

Pre-internal

Table Items

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SCALE	SHT	OF	
NONE	4	97	

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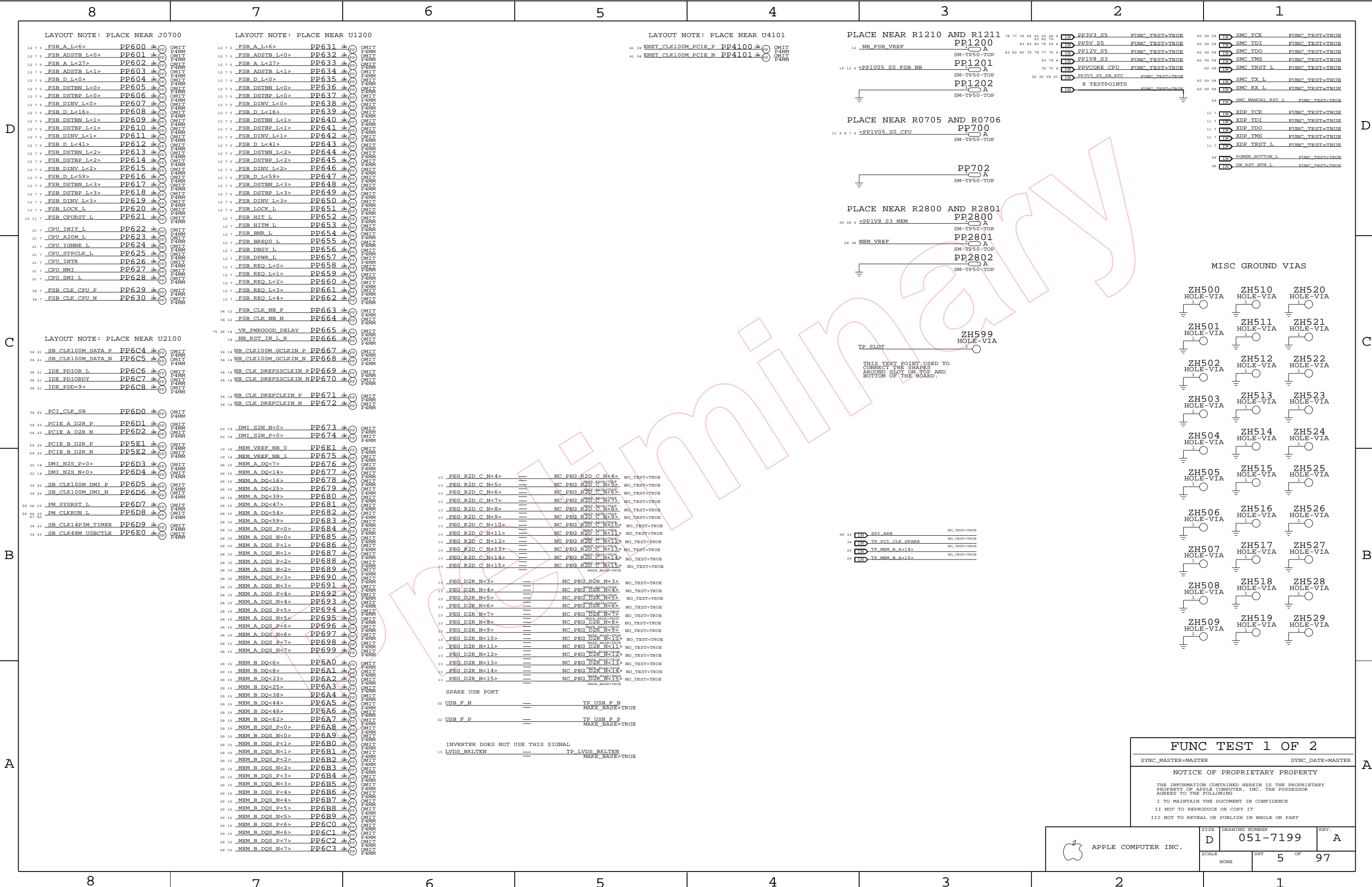
5

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1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

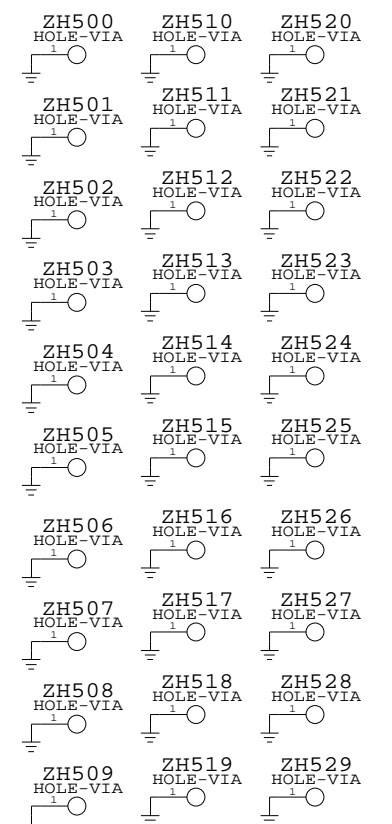
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

FUNC TEST 1 OF 2

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHEET	OF	
NONE	5	97	

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11	PEG_R2D_C_N<5>	NC_PEG_R2D_C_N<5>	NO_TEST=TRUE
11	PEG_R2D_C_N<6>	NC_PEG_R2D_C_N<6>	NO_TEST=TRUE
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11	PEG_R2D_C_N<8>	NC_PEG_R2D_C_N<8>	NO_TEST=TRUE
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11	PEG_R2D_C_N<10>	NC_PEG_R2D_C_N<10>	NO_TEST=TRUE
11	PEG_R2D_C_N<11>	NC_PEG_R2D_C_N<11>	NO_TEST=TRUE
11	PEG_R2D_C_N<12>	NC_PEG_R2D_C_N<12>	NO_TEST=TRUE
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11	PEG_D2R_N<13>	NC_PEG_D2R_N<13>	NO_TEST=TRUE
11	PEG_D2R_N<14>	NC_PEG_D2R_N<14>	NO_TEST=TRUE
11	PEG_D2R_N<15>	NC_PEG_D2R_N<15>	NO_TEST=TRUE

SPARE USB PORT

22 USB_F_N TP_USB_F_N
MAKE_BASE=TRUE

22 USB_F_P TP_USB_F_P
MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL

13 LVDS_BKLTEN TP_LVDS_BKLTEN
MAKE_BASE=TRUE

"S0" RAILS

ONLY ON IN RUN

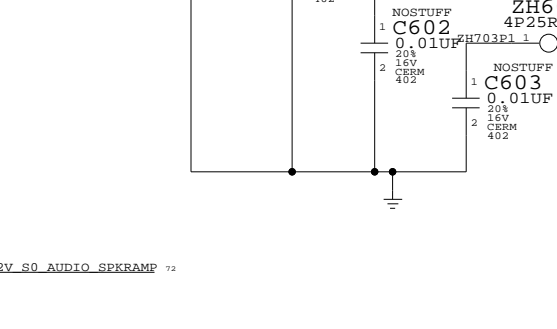
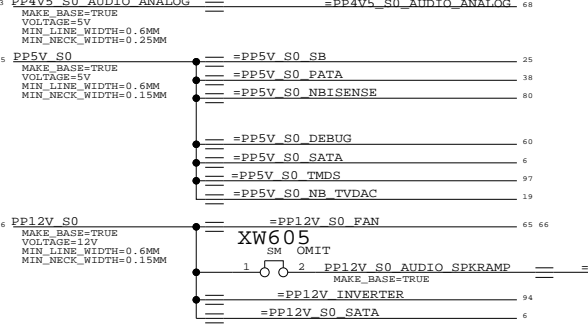
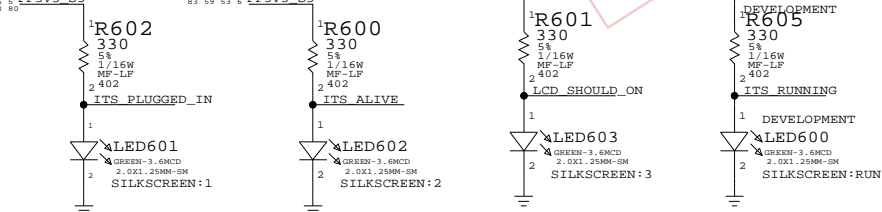
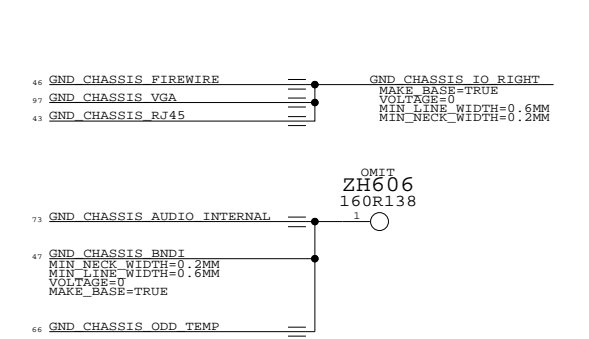
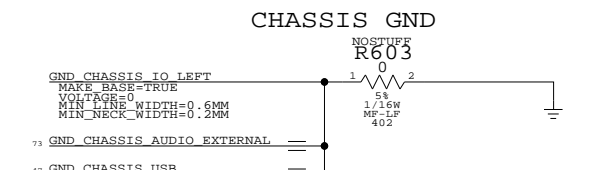
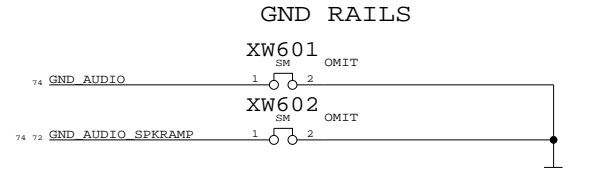
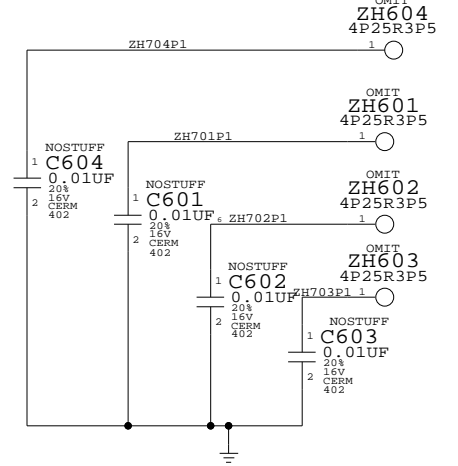
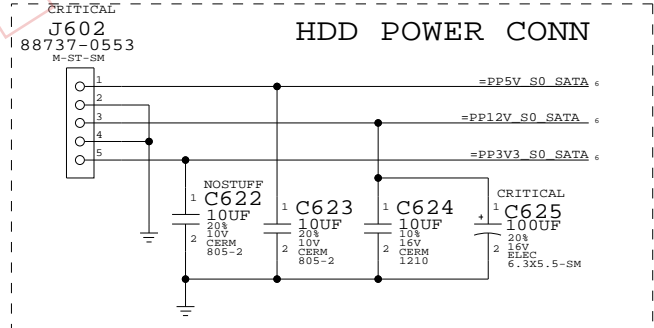
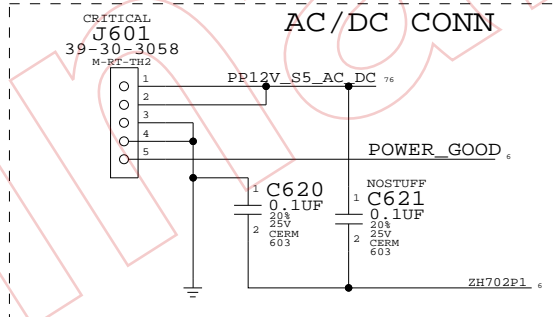
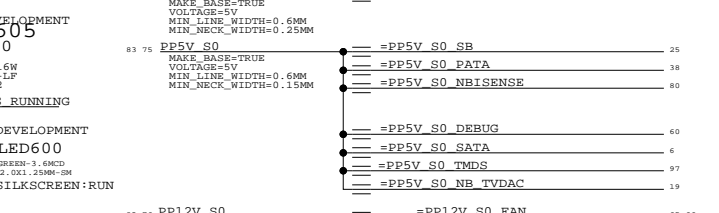
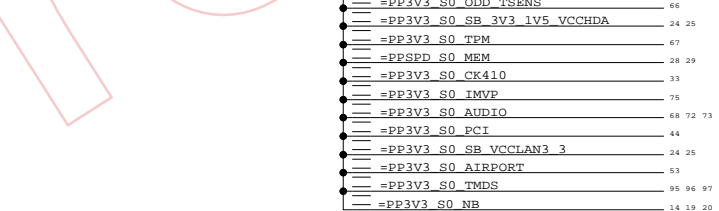
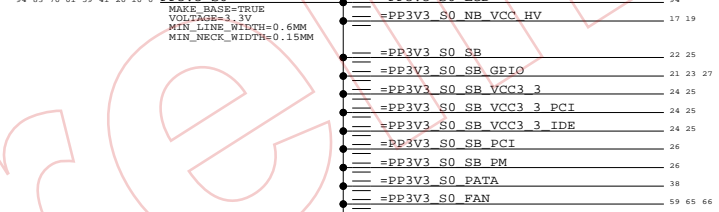
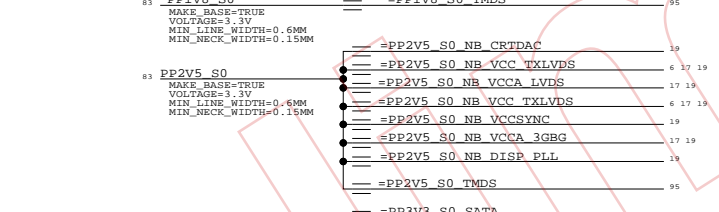
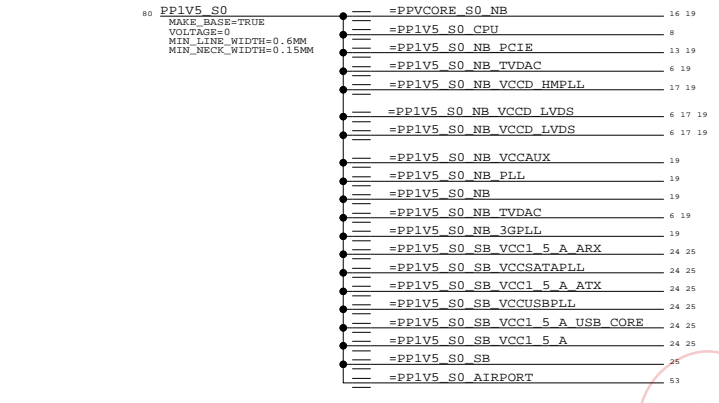
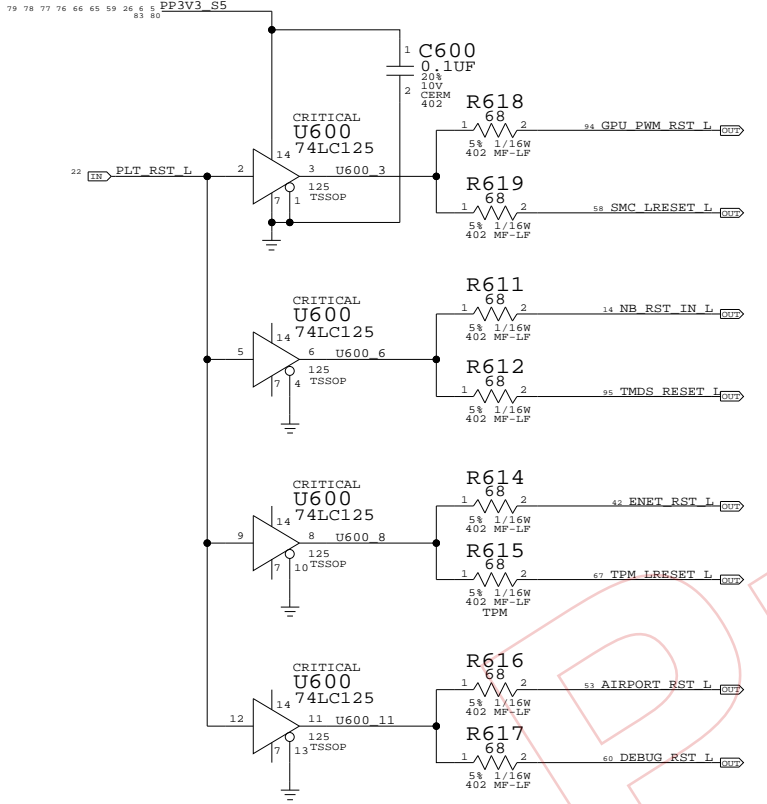
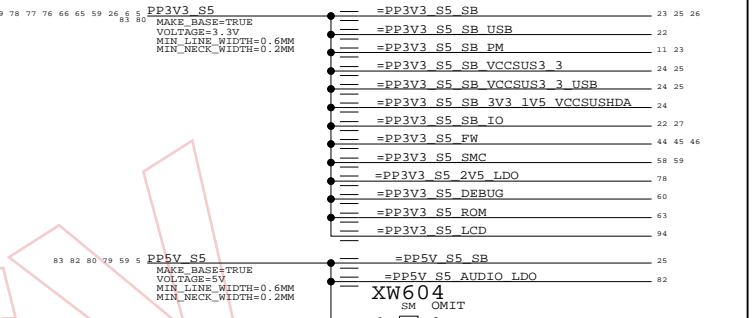
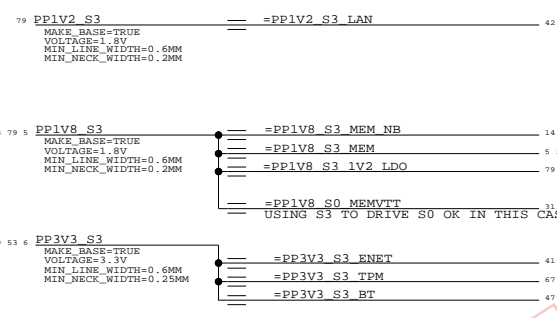
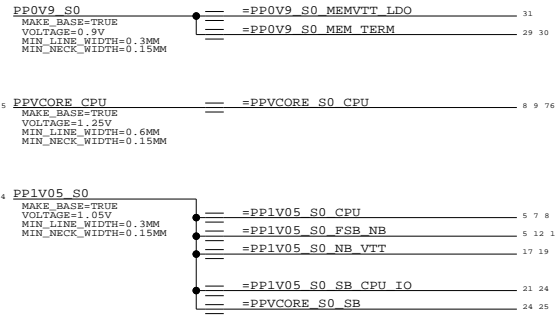
"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

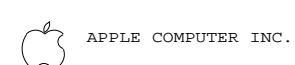
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

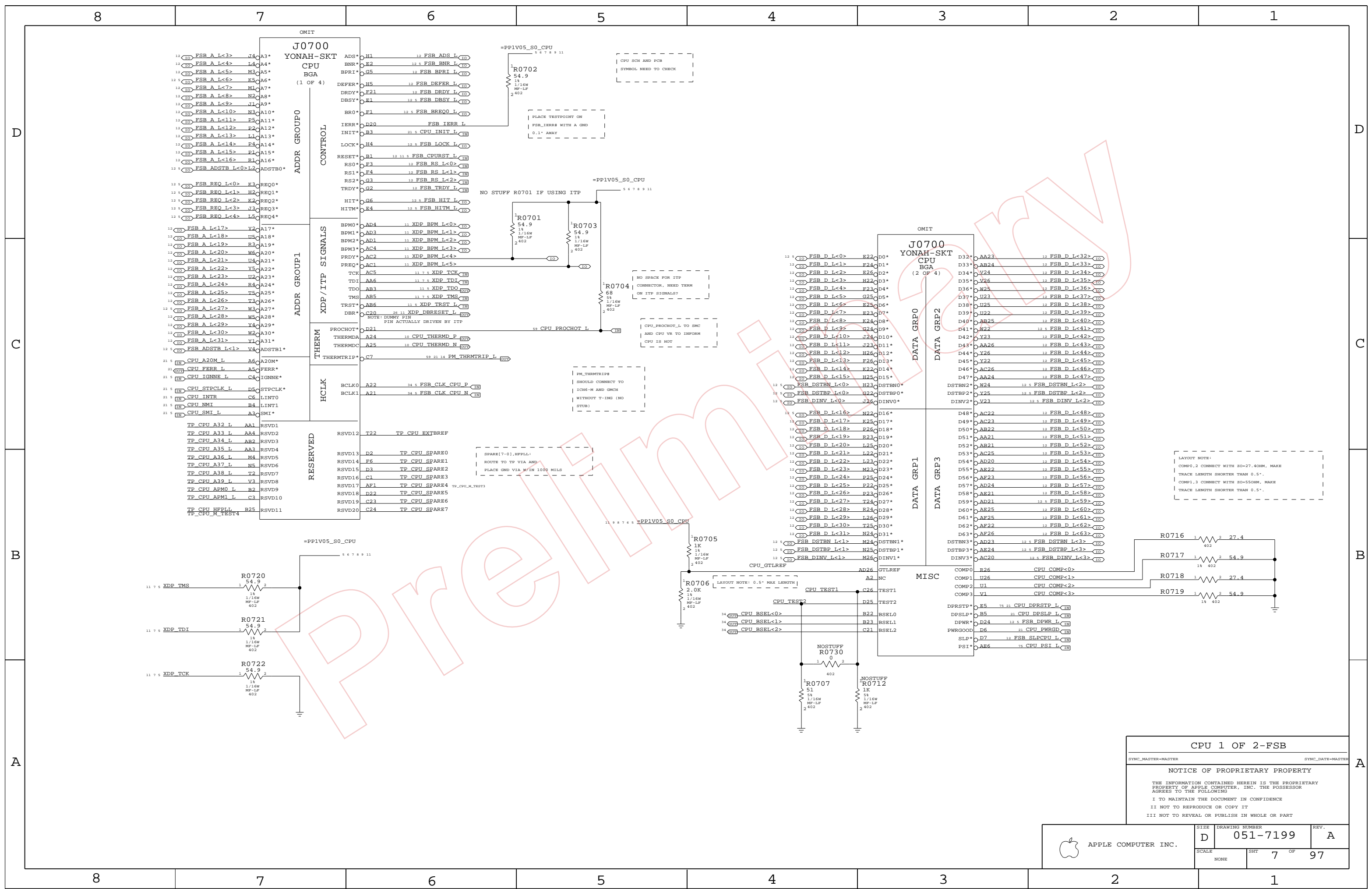
82 78 76 SYS POWERFAIL L I632 POWER_GOOD



Power Conn / Alias
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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Table with columns: SIZE (D), DRAWING NUMBER (051-7199), REV. (A), SCALE (NONE), SHEET (6 OF 97).





CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATA-MASTER

NOTICE OF PROPRIETARY PROPERTY

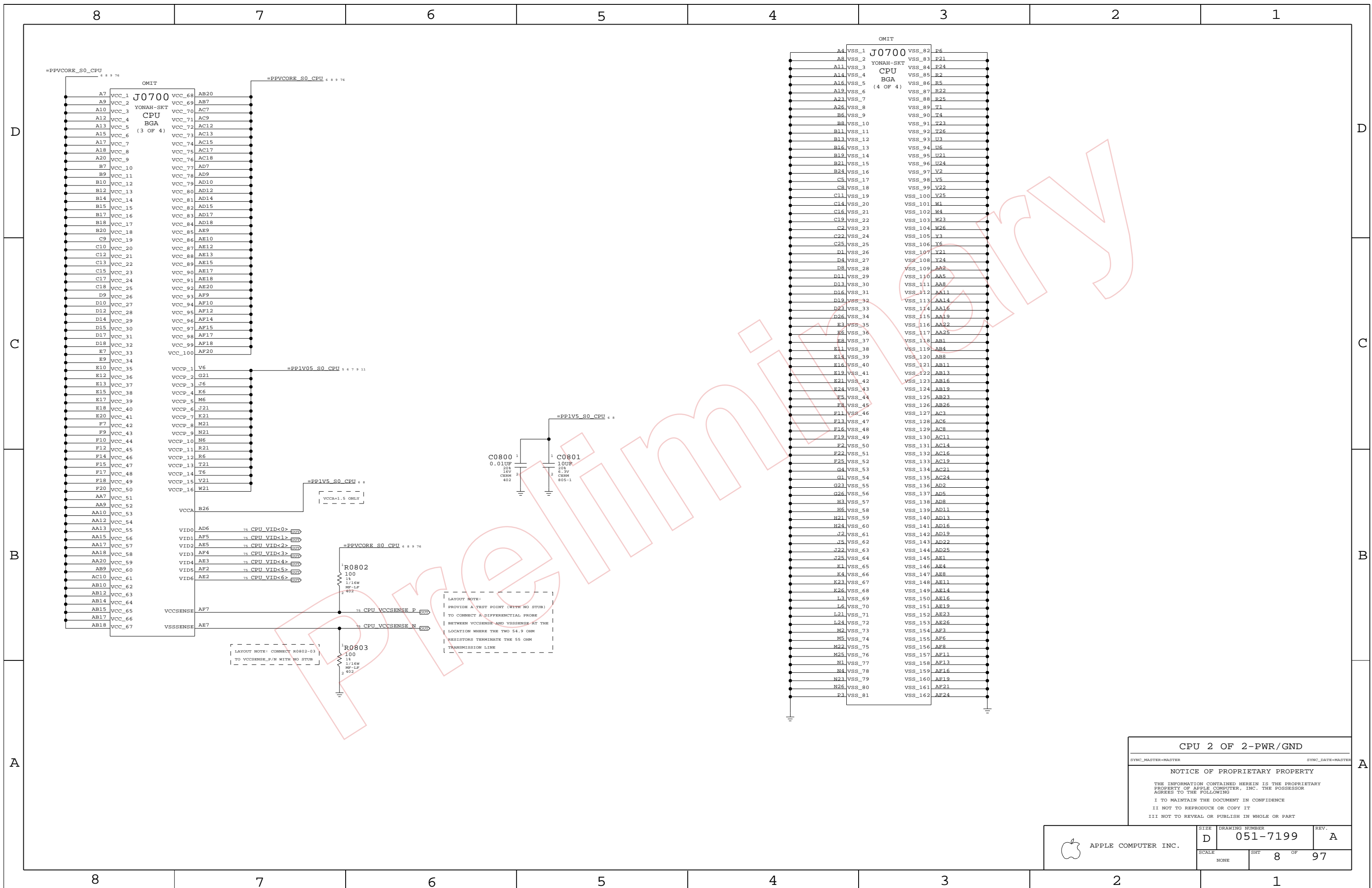
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SCALE		SHT	OF
NONE		7	97



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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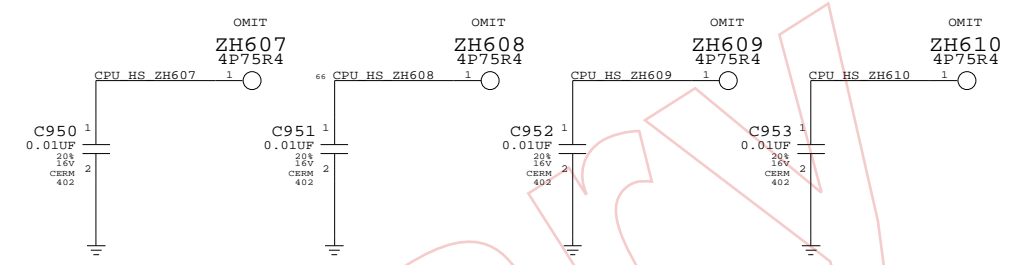
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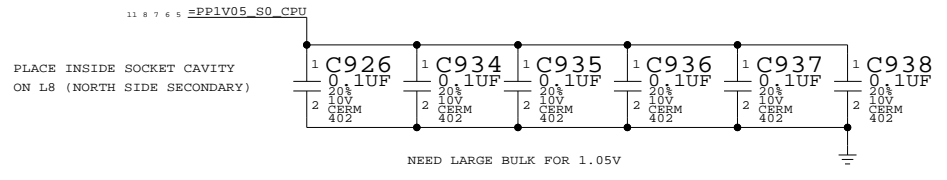
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 8	OF 97

CPU HEATSINK MOUNTING HOLES



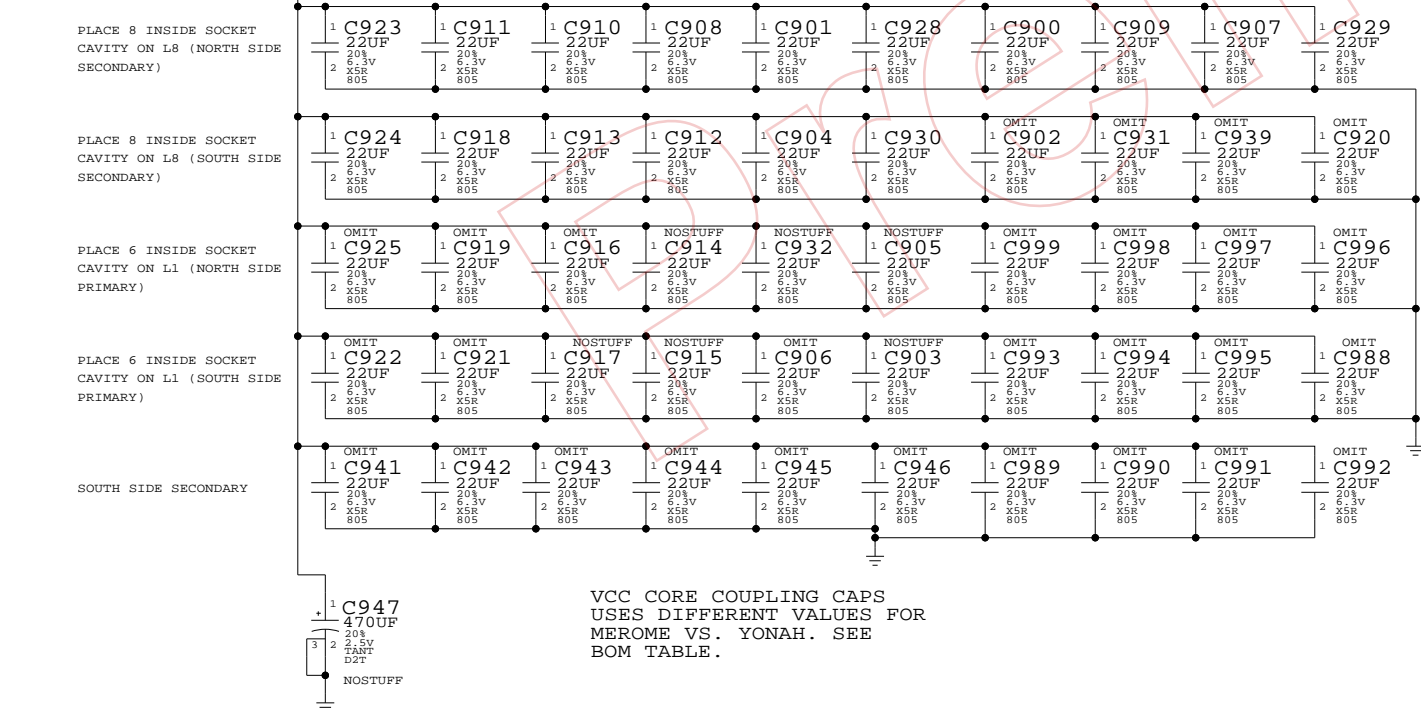
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20k, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20k, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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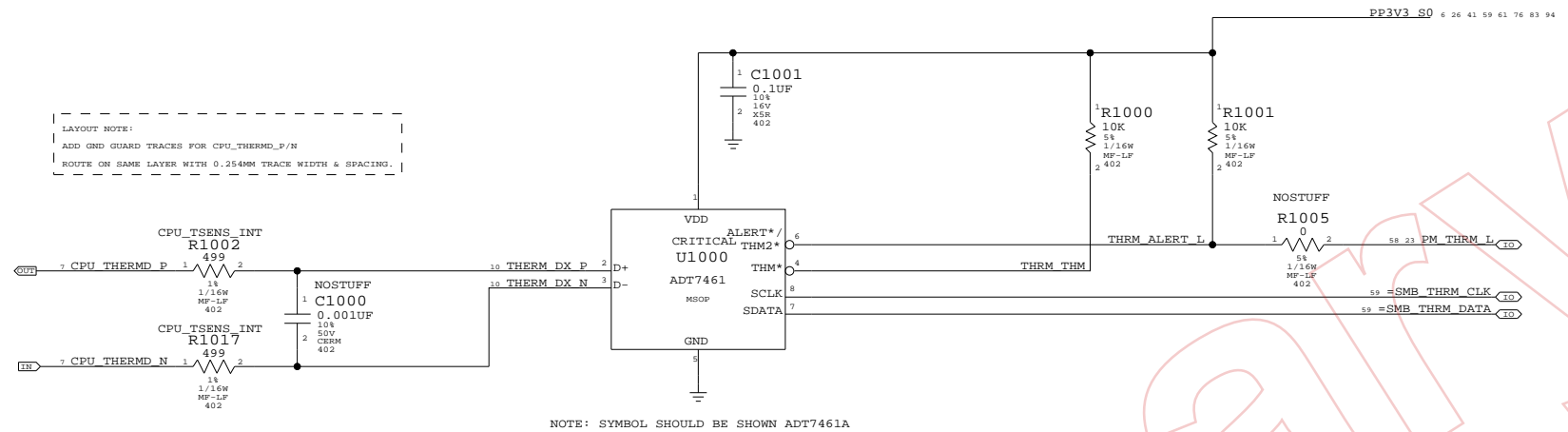
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	9 OF	97
NONE			

CPU THERMAL SENSOR

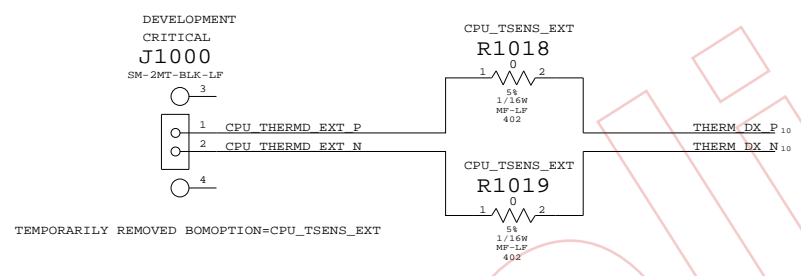
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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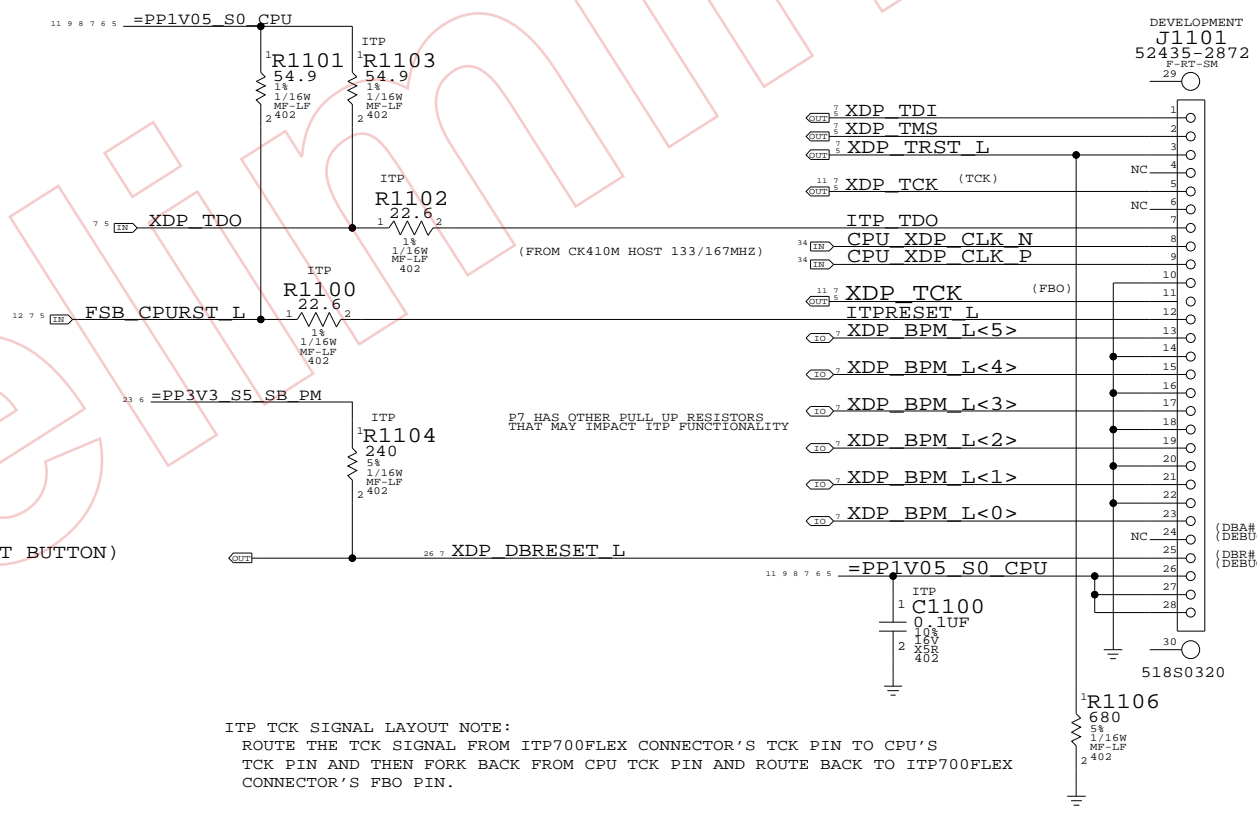
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	D	051-7199	A
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



DEVELOPMENT
 J1101
 52435-2872
 P-ST-SM
 29

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
 (DEBUG PORT ACTIVE)
 (DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
 (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
 CONNECTOR'S FBO PIN.

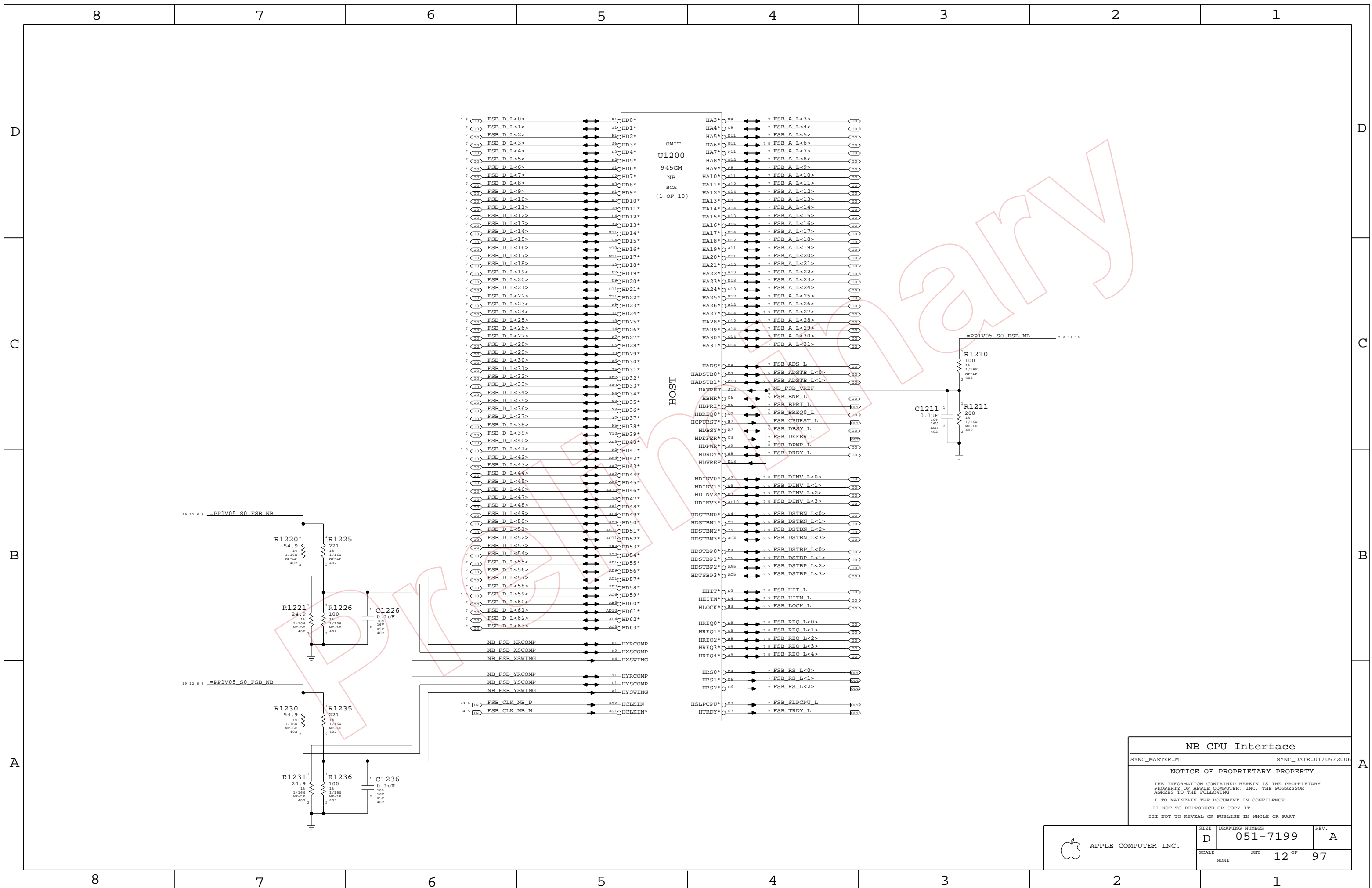
(AND WITH RESET BUTTON)

P7 HAS OTHER PULL UP RESISTORS
 THAT MAY IMPACT ITP FUNCTIONALITY

CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

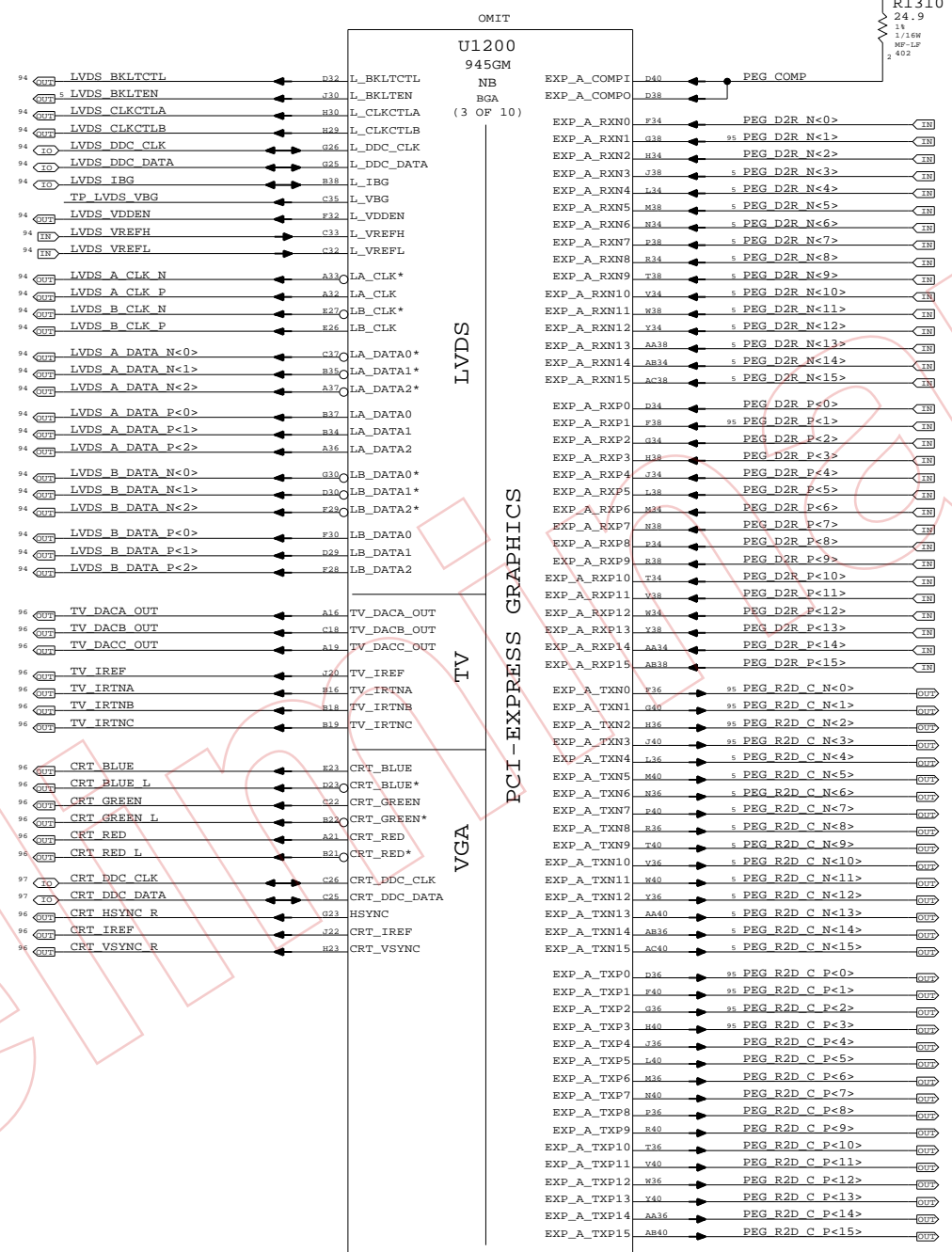
LVDS Disable
Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable
Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function
SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

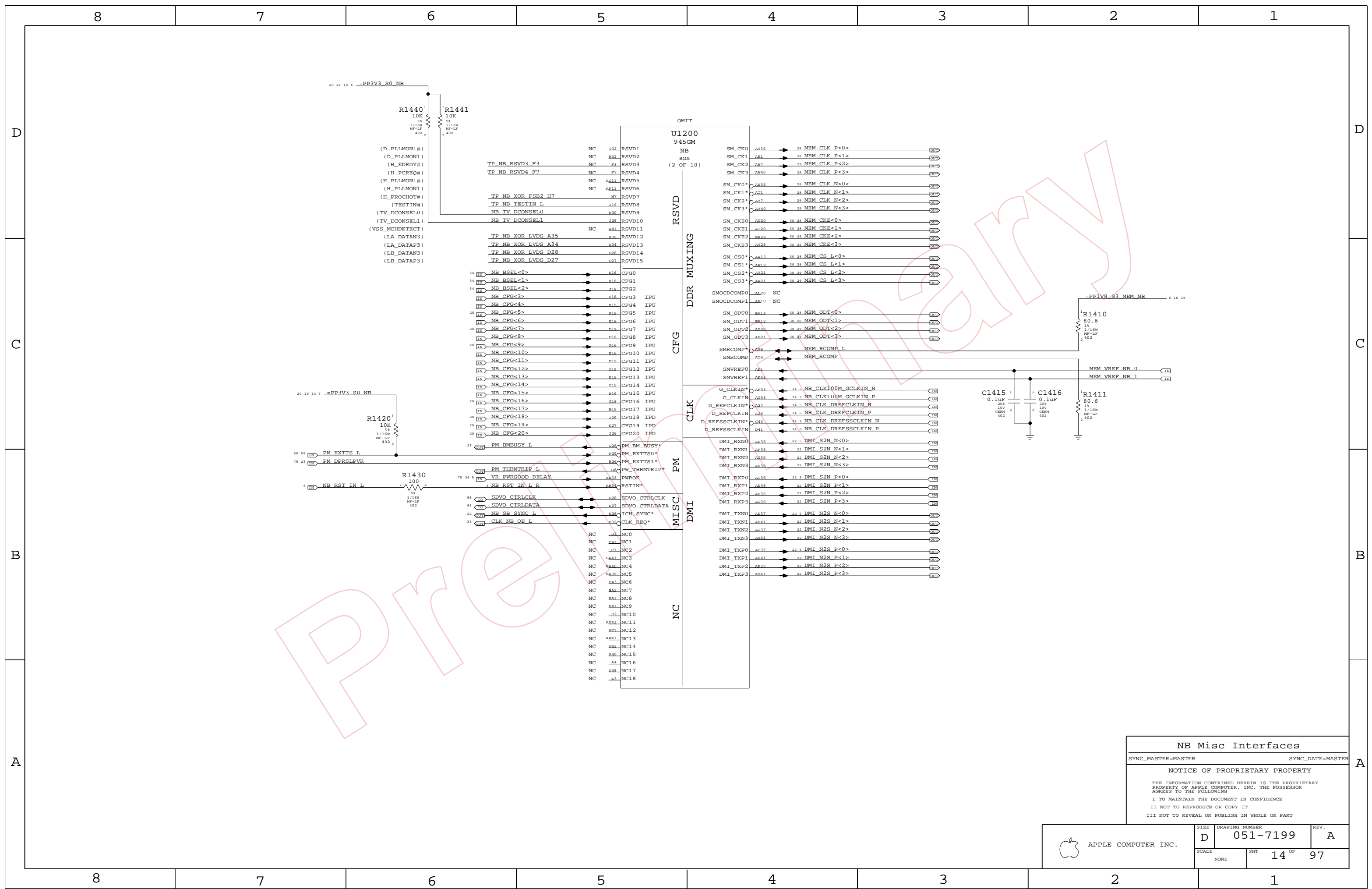
SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

Pre-release

NB PEG / Video Interfaces
SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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SCALE	SHT	13 OF	97
NONE			



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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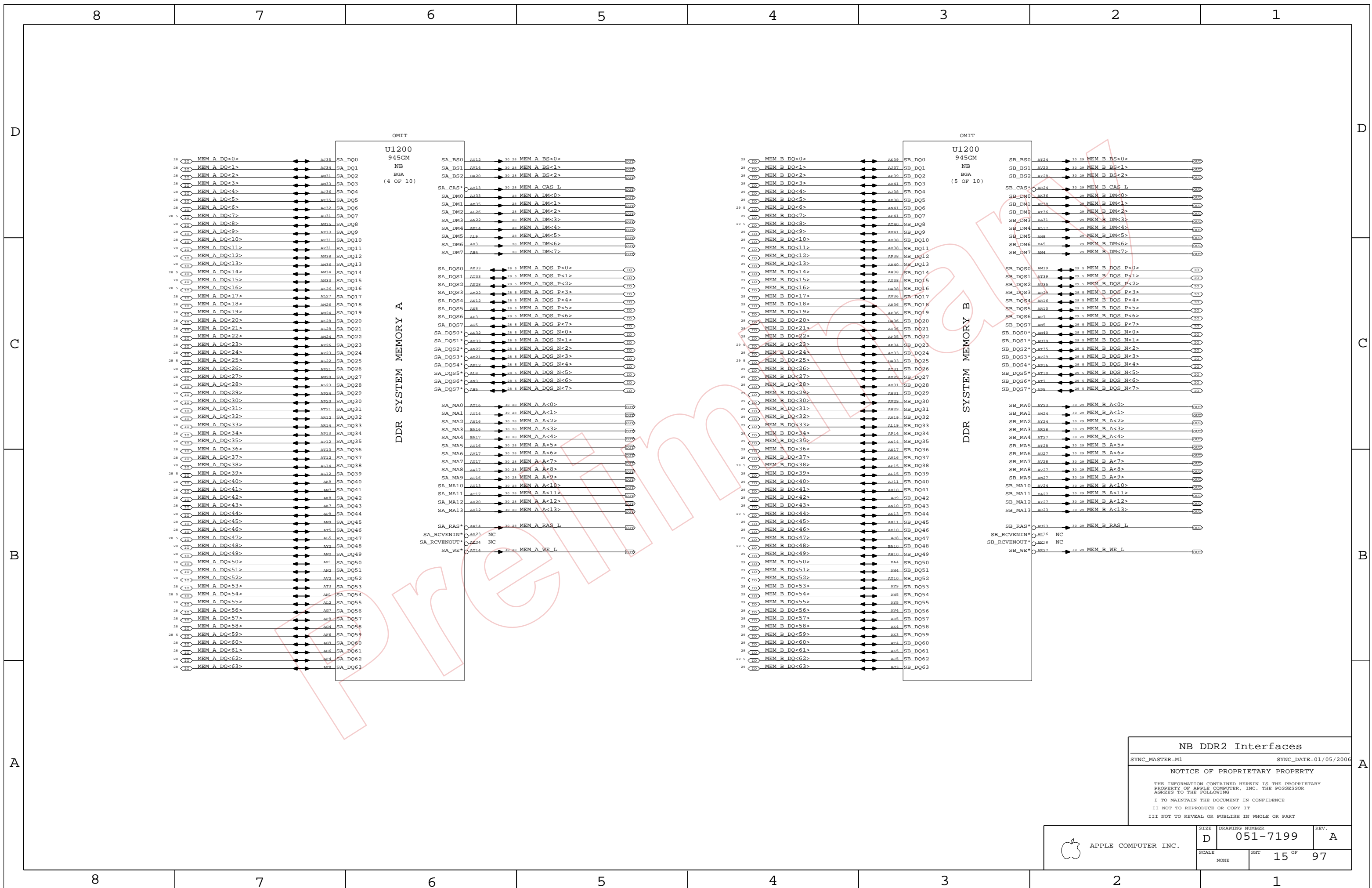
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NB DDR2 Interfaces

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	SCALE NONE	SHEET 15 OF 97	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT

D

D

C

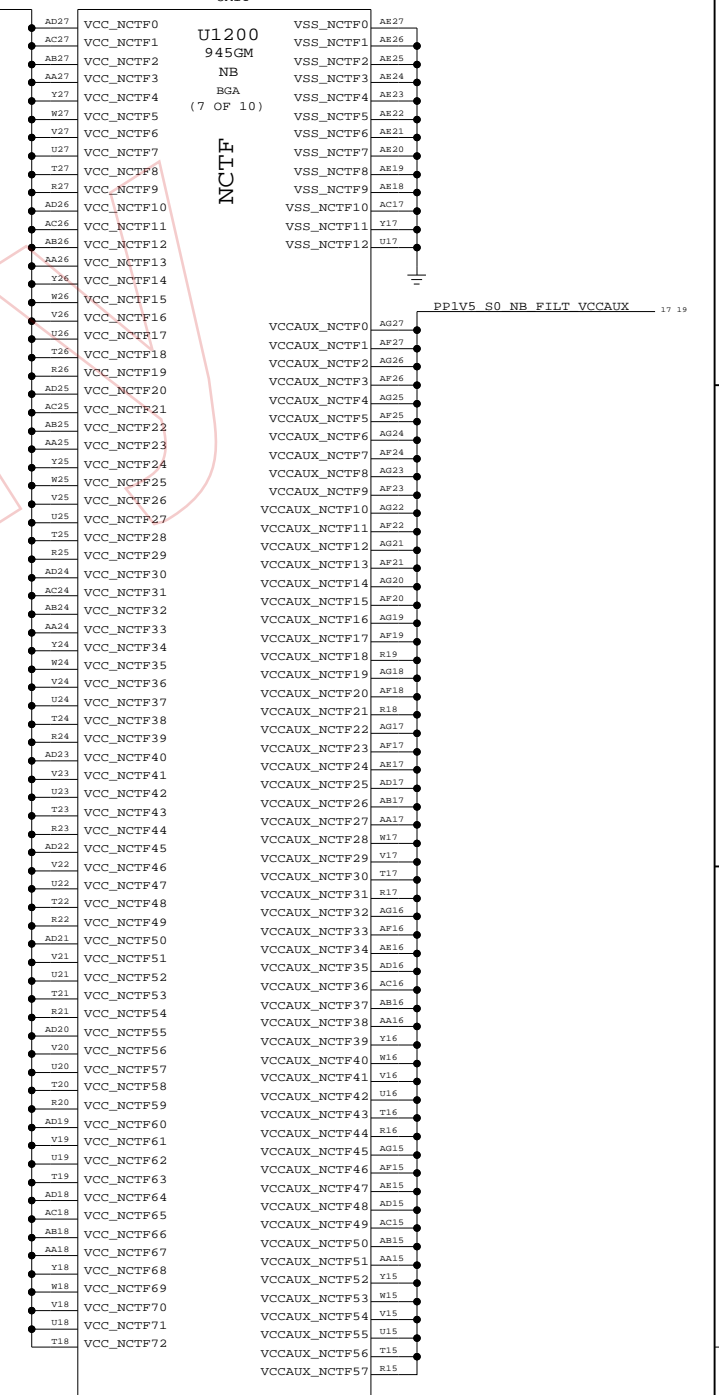
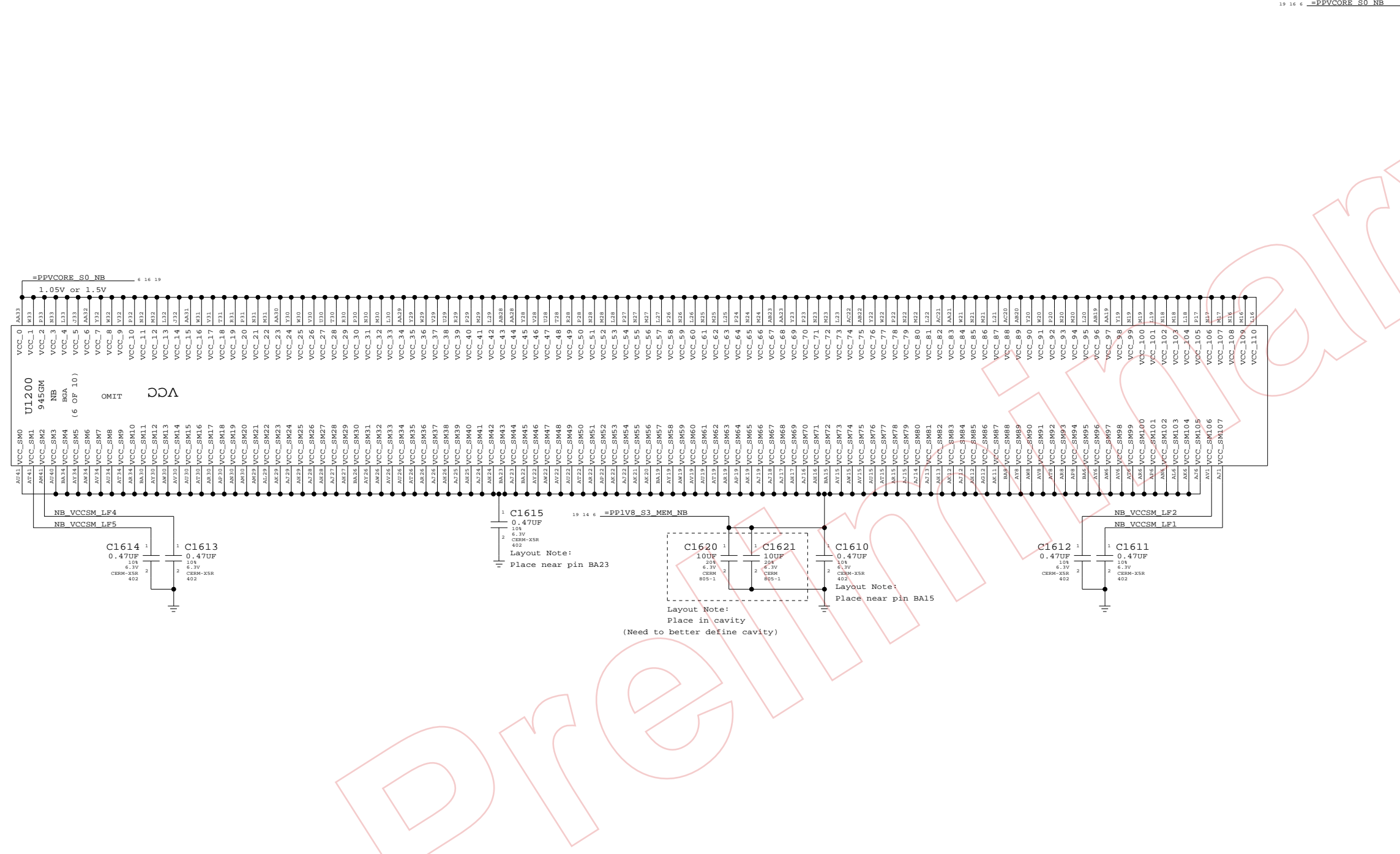
C

B

B

A

A



NB Power 1

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

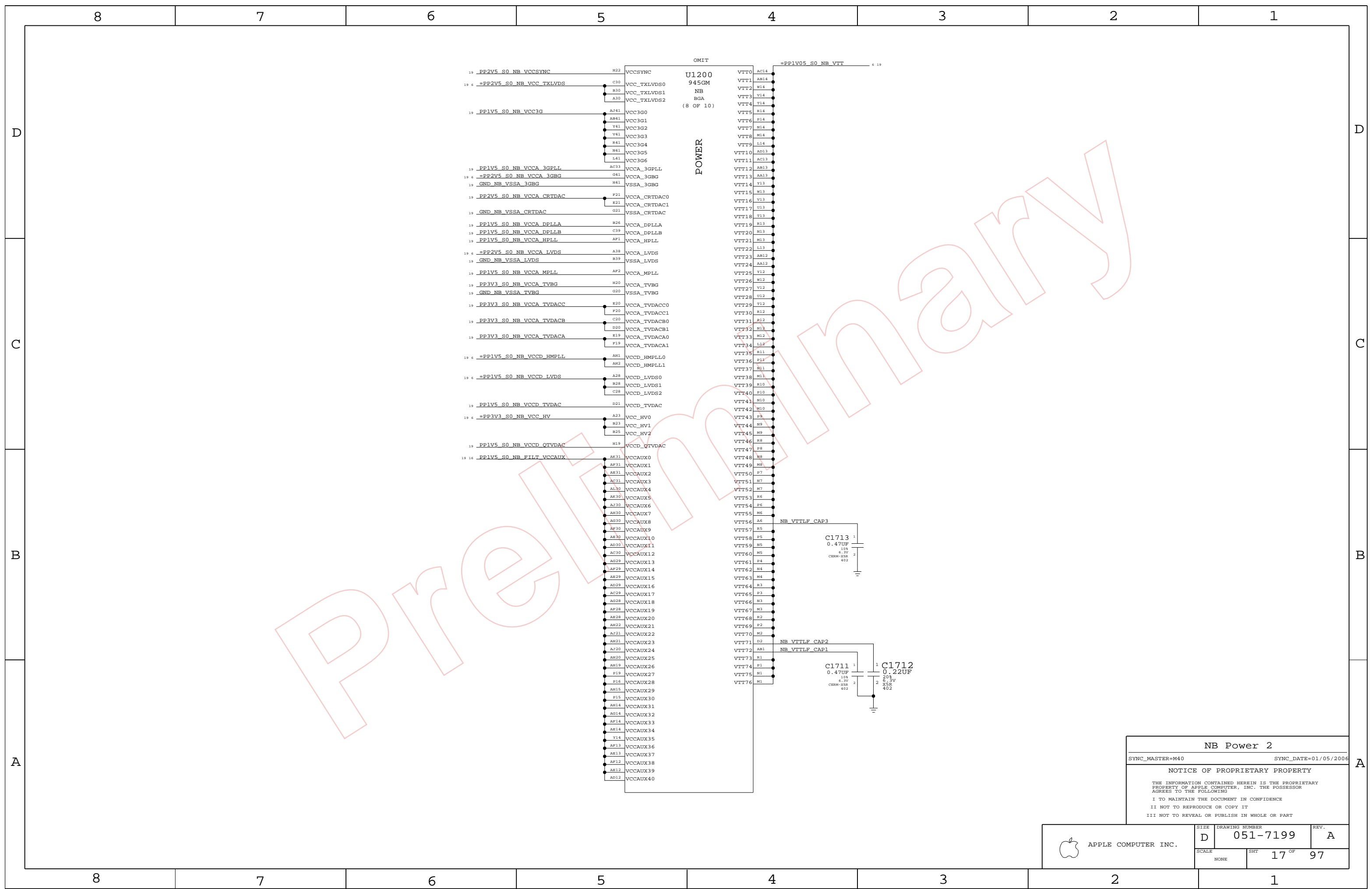
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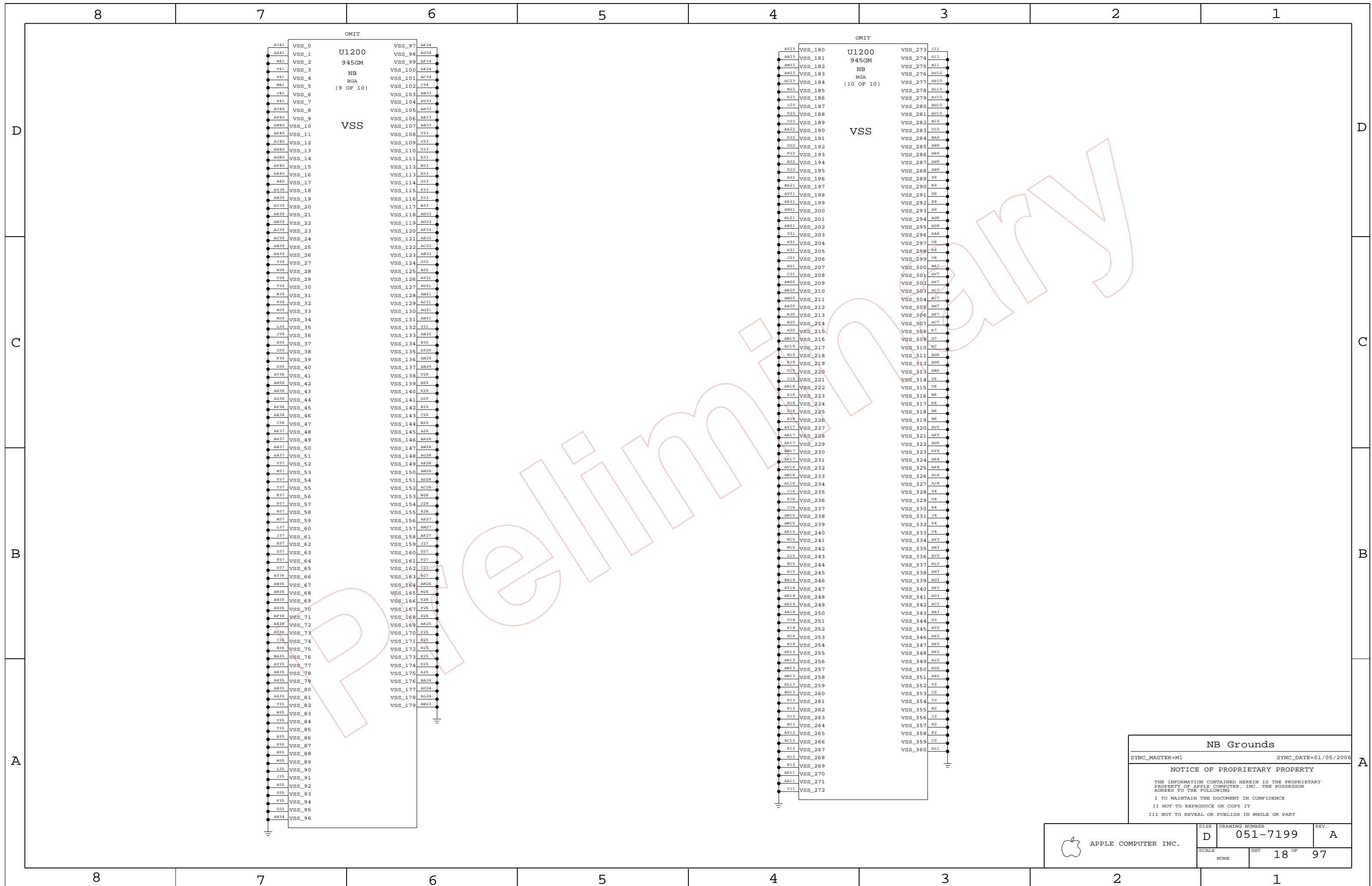
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	16 OF	97
NONE			



NB Power 2
 SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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	D	051-7199	A
SCALE	NONE	SHT	17 OF 97



NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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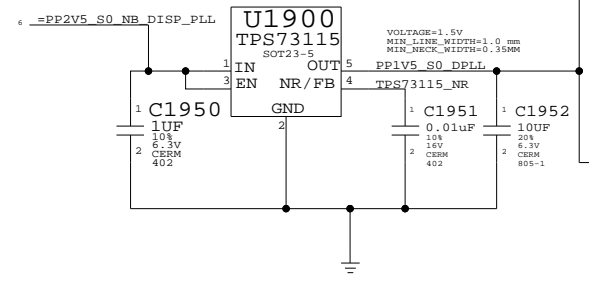
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 18 OF 97	

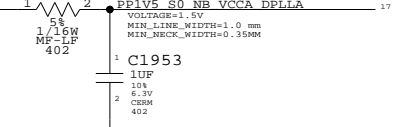
Power Interface
These are the power signals that leave the NB "block"

- =PP1V05_S0_FSB_NB 5 6 12
- =PPVCORE_S0_NB 6 16 19
- =PP1V05_S0_NB_VTT 6 17 19
- =PP1V5_S0_NB 6 19
- =PP1V5_S0_NB_PCIE 6 13
- =PP1V5_S0_NB_PLL 6 19
- =PP1V5_S0_NB_TVDAC 6 19
- =PP1V5_S0_NB_VCCD_HMPLL 6 17
- =PP1V5_S0_NB_VCCD_LVDS 6 17 19
- =PP1V5_S0_NB_VCCAUX 6 19
- =PP1V8_S3_MEM_NB 6 14 16 19
- =PP2V5_S0_NB_VCCSYNC 19 6
- =PP2V5_S0_NB_VCC_TXLVDS 6 17 19
- =PP2V5_S0_NB_VCCA_3GBG 6 17 19
- =PP2V5_S0_NB_VCCA_LVDS 6 17 19
- =PP3V3_S0_NB 6 14 20
- =PP3V3_S0_NB_VCC_HV 6 17 19
- =PP5V_S0_NB_TVDAC 6 19

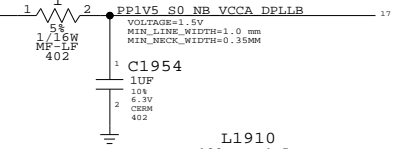
MCH DISPLAY PLL POWER LDO



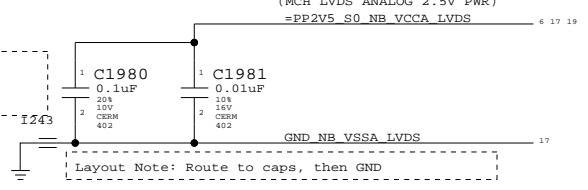
MCH VCCA_DPLL_A FILTER (MCH DISPLAY A PLL 1.5V PWR)



GMCH VCCA_DPLL_B FILTER (MCH DISPLAY B PLL 1.5V PWR)



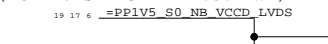
MCH VCCA_LVDS FILTER (MCH LVDS ANALOG 2.5V PWR)



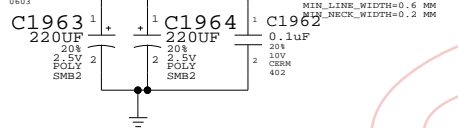
Layout Note: This 0.1uF cap should be within 5 mm of NB edge

Layout Note: Route to caps, then GND

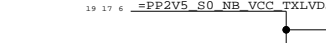
GMCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)



FILTERING REQUIRED FOR INTEGRATED GFX (PG. 333)

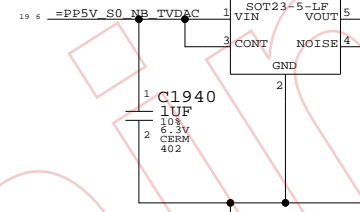


GMCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)

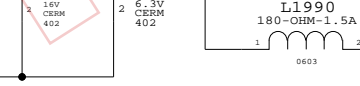


945 EDS: 1210?

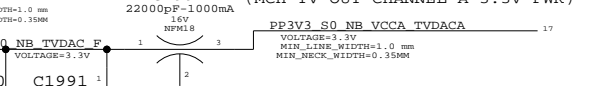
MCH VCCD_TV DAC FILTER (MCH TV OUT CHANNEL A 3.3V PWR)



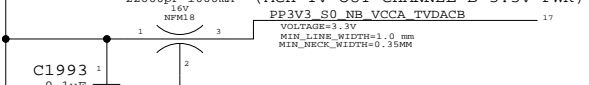
MCH VCCA_TV DAC FILTER (MCH TV OUT CHANNEL A 3.3V PWR)



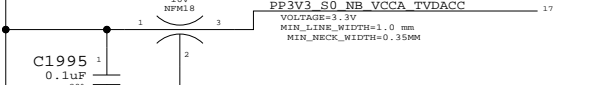
MCH VCCA_TV DAC FILTER (MCH TV OUT CHANNEL B 3.3V PWR)



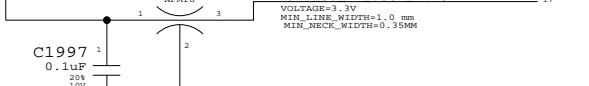
MCH VCCA_TV DAC FILTER (MCH TV OUT CHANNEL B 3.3V PWR)



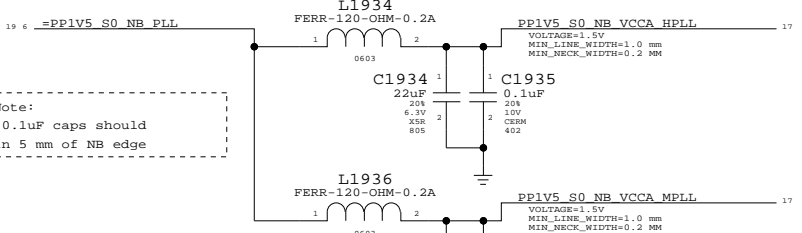
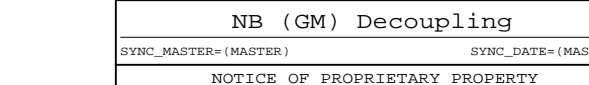
MCH VCCA_TV DAC FILTER (MCH TV OUT CHANNEL C 3.3V PWR)



MCH VCCA_TV DAC FILTER (MCH TV OUT CHANNEL C 3.3V PWR)

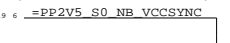


MCH VCCA_TV DAC FILTER (MCH TV DAC BAND GAP 3.3V PWR)



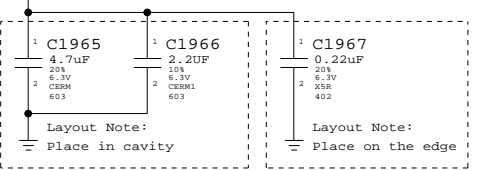
Layout Note: These 4 0.1uF caps should be within 5 mm of NB edge

MCH VCCSYNC BYPASS (MCH H/V SYNC 2.5V PWR)



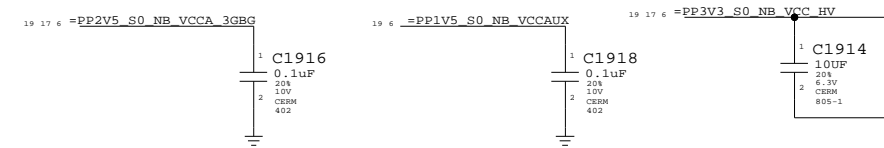
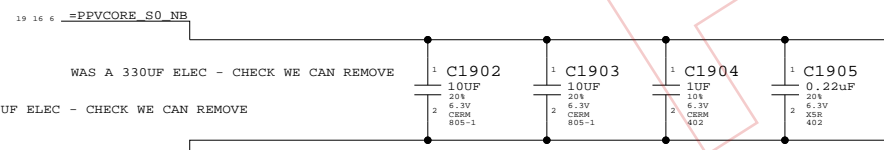
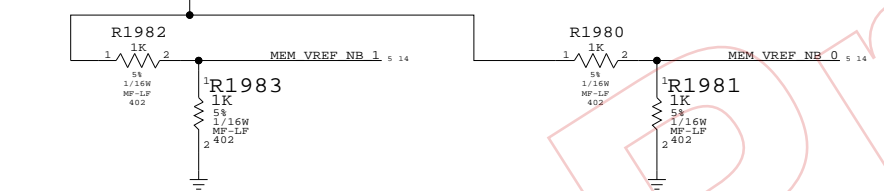
Layout Note: PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

Layout Note: These 8 caps should be within 6.35 mm of NB edge

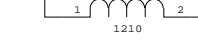


Layout Note: Place in cavity

Layout Note: Place on the edge



MCH VCC3G FILTER (MCH TV OUT CHANNEL C 3.3V PWR)



Layout Note: Place L and C close to MCH

Layout Note: 10uF caps should be close to MCH on opposite side.

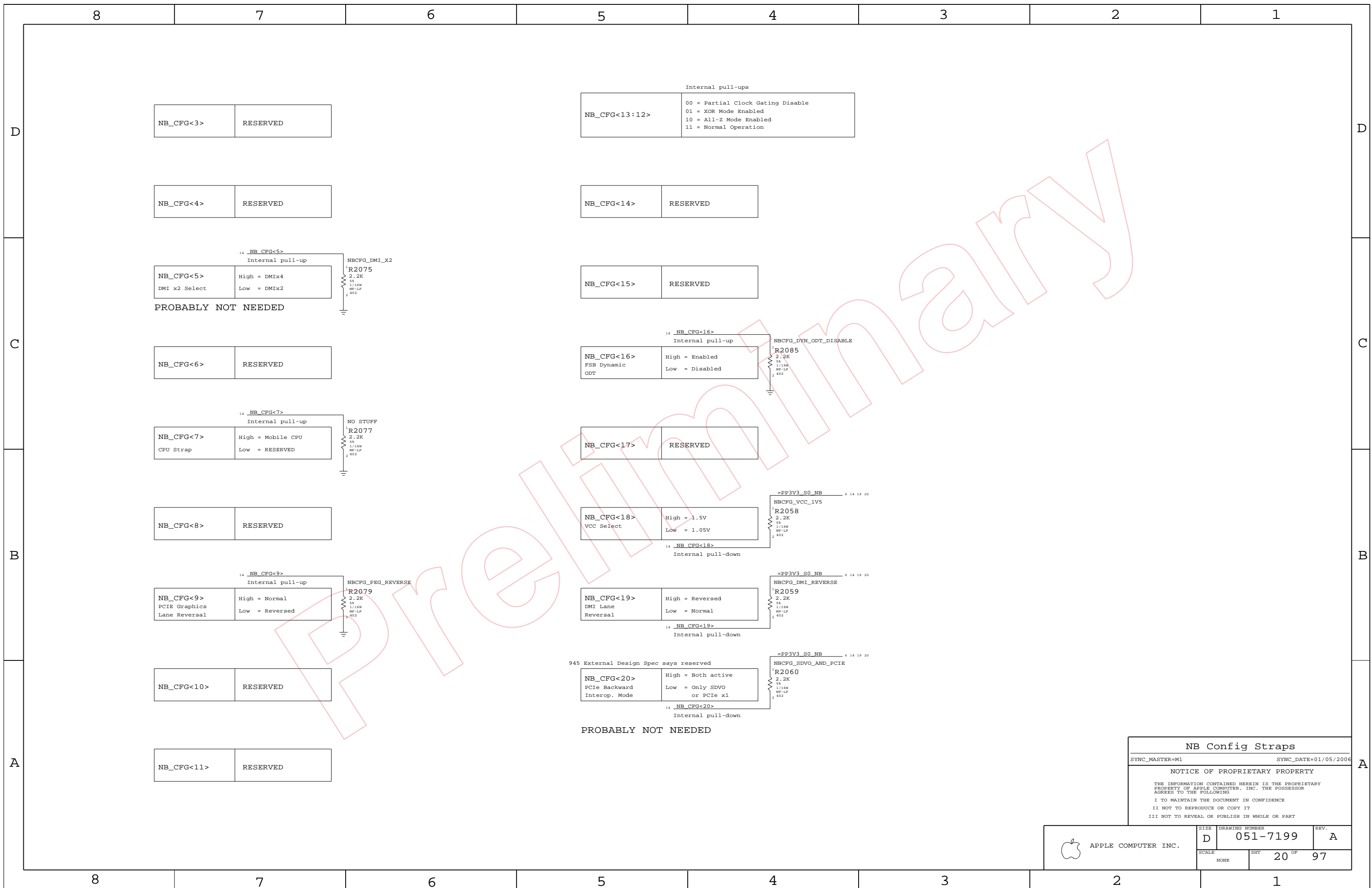
NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7199	A
SCALE	SHT	19 OF 97	
NONE			



NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

NB_CFG<10>	RESERVED
------------	----------

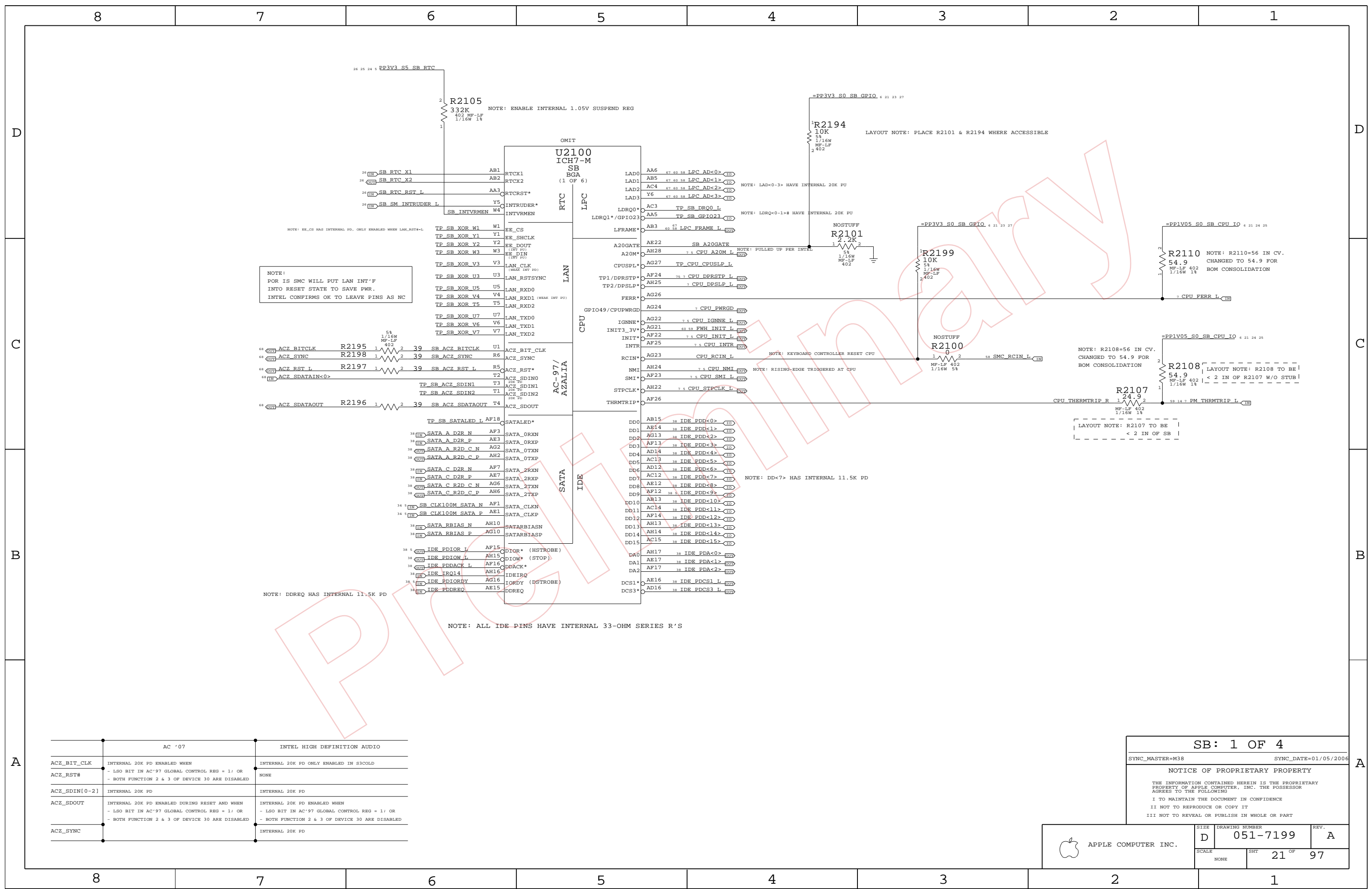
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

NB Config Straps
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	D	051-7199	A
SCALE	SHT	20 OF 97	
NONE			



NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

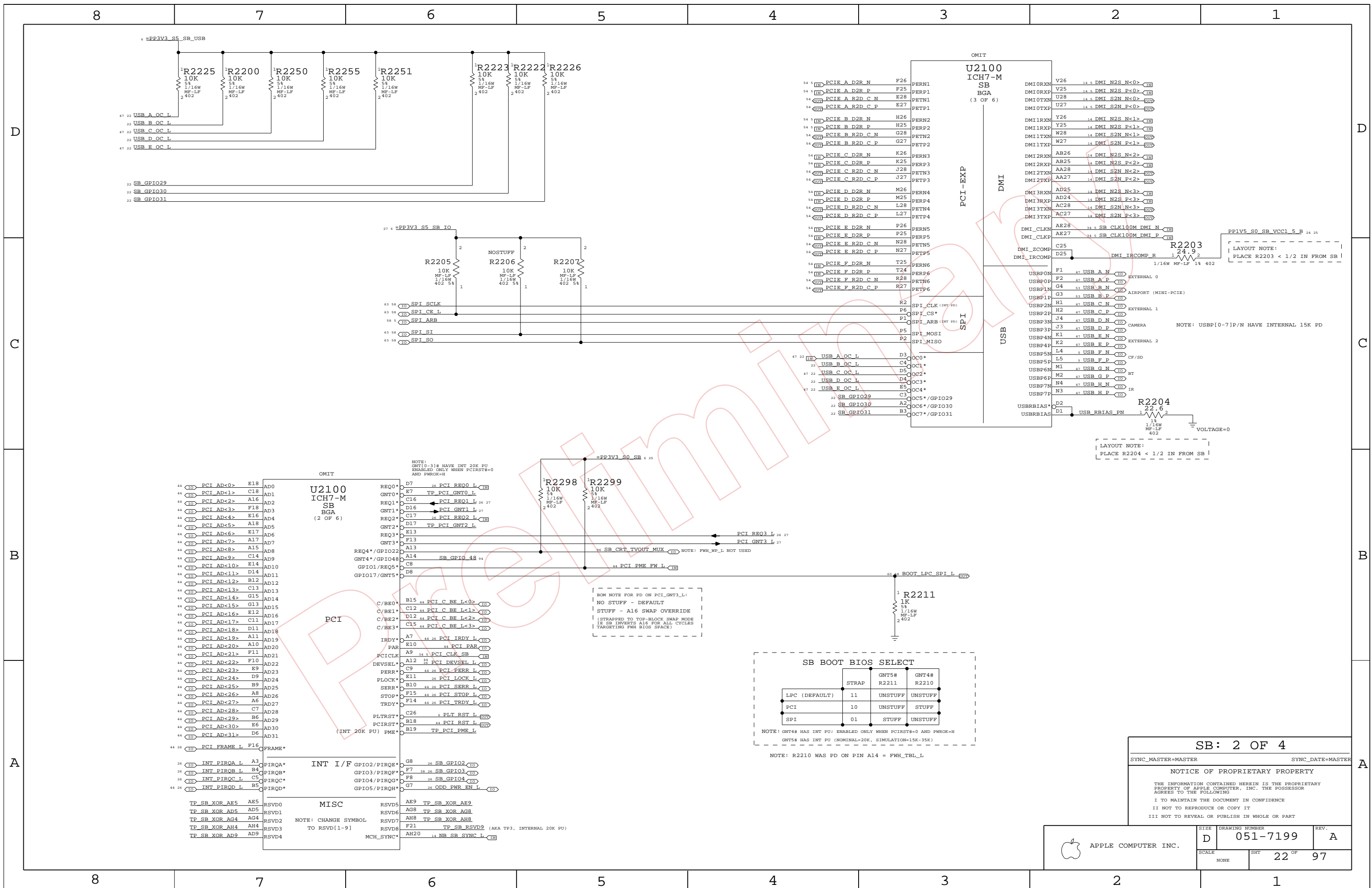
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7199	A
SCALE	SHT	21 OF 97	
NONE			



Pin	Signal	Function
54	PCIE A D2R N	F26 PERN1
54	PCIE A D2R P	F25 PERP1
54	PCIE A R2D C N	E28 PETN1
54	PCIE A R2D C P	E27 PETP1
54	PCIE B D2R N	H26 PERN2
54	PCIE B D2R P	H25 PERP2
54	PCIE B R2D C N	G28 PETN2
54	PCIE B R2D C P	G27 PETP2
54	PCIE C D2R N	K26 PERN3
54	PCIE C D2R P	K25 PERP3
54	PCIE C R2D C N	J28 PETN3
54	PCIE C R2D C P	J27 PETP3
54	PCIE D D2R N	M26 PERN4
54	PCIE D D2R P	M25 PERP4
54	PCIE D R2D C N	L28 PETN4
54	PCIE D R2D C P	L27 PETP4
54	PCIE E D2R N	P26 PERN5
54	PCIE E D2R P	P25 PERP5
54	PCIE E R2D C N	N28 PETN5
54	PCIE E R2D C P	N27 PETP5
54	PCIE F D2R N	T26 PERN6
54	PCIE F D2R P	T24 PERP6
54	PCIE F R2D C N	R28 PETN6
54	PCIE F R2D C P	R27 PETP6

SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST#=0 AND FWR0K=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

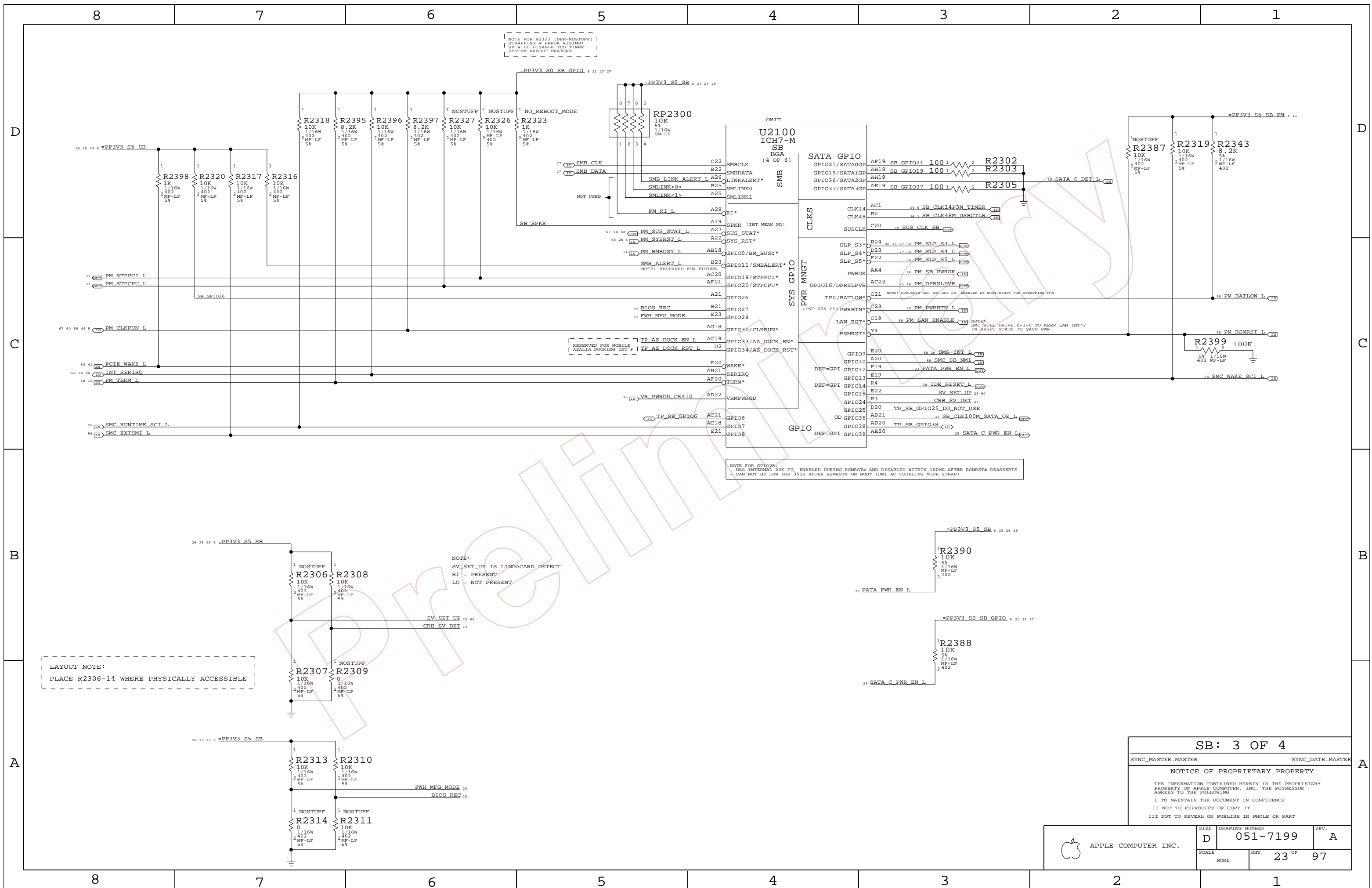
SB: 2 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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NOTE FOR R2333 (DEF=NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

NOTE FOR GPIO25: * HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS * CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOTE: SV_SET_UP IS LINDACARD DETECT HI = PRESENT LO = NOT PRESENT

LAYOUT NOTE: PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT		23 OF 97
NONE			

8

7

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C

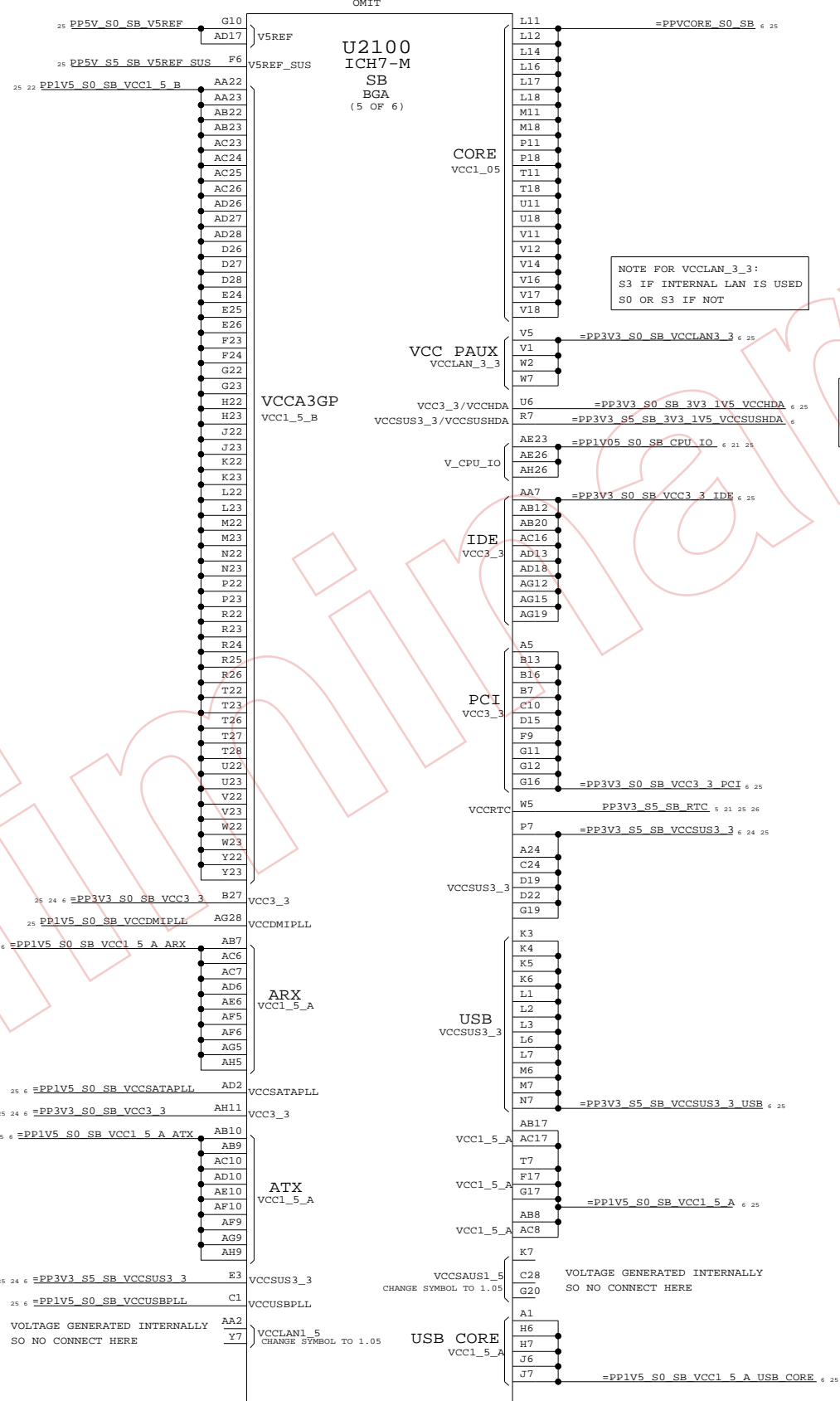
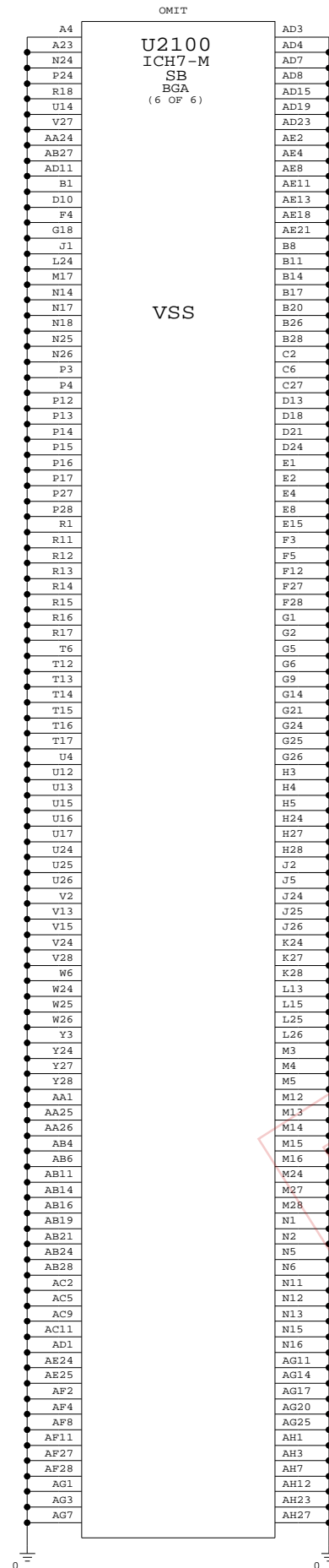
C

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SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

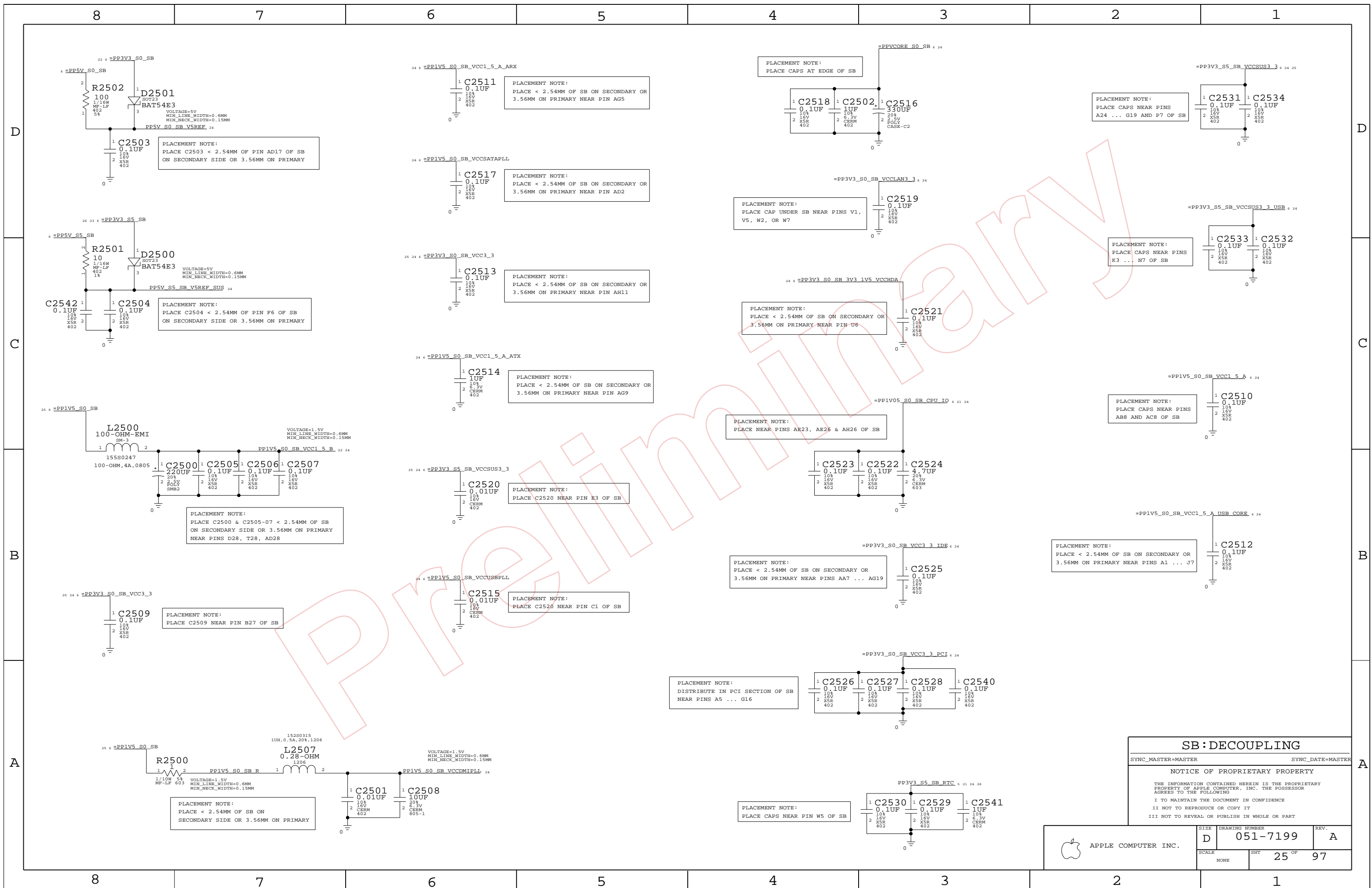
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	24 OF 97	
NONE			



SB: DECOUPLING

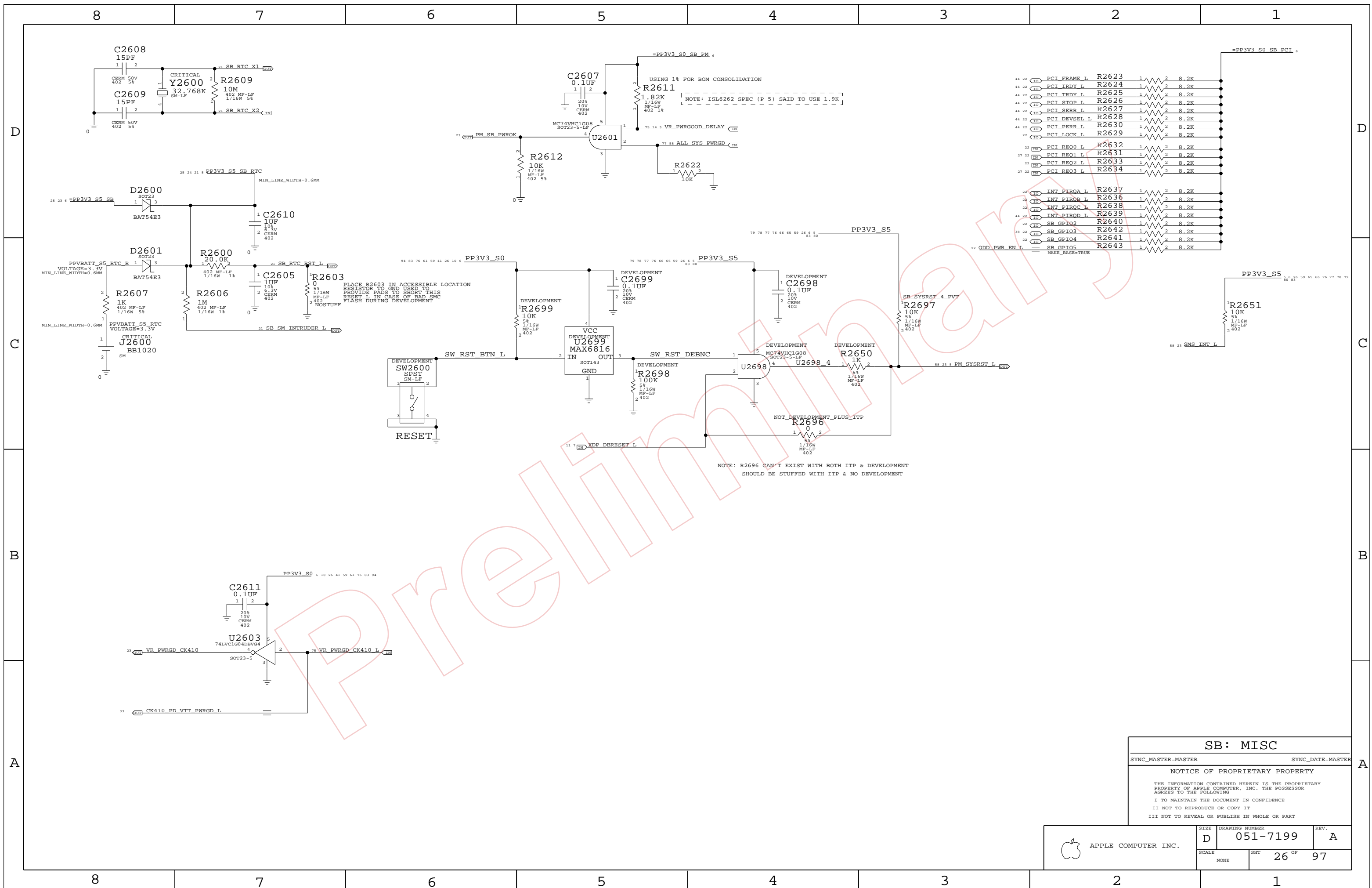
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	25 OF	97
NONE			



SB: MISC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	26 OF	97
NONE			

8

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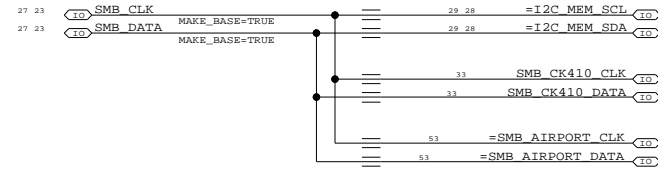
2

1

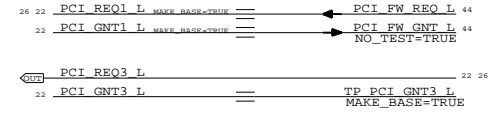
D

D

SB I2C BUSSES

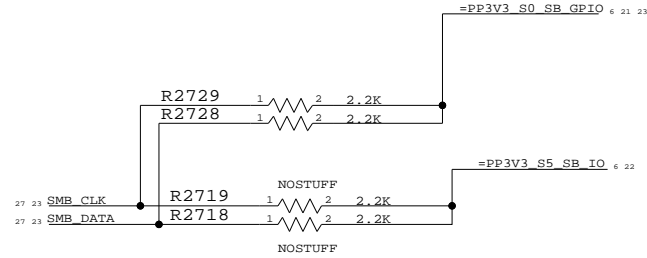


PCI CONTROL



C

C



B

B

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A

Preliminary

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	NONE	SHT	27 OF 97

8

7

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1

Page Notes

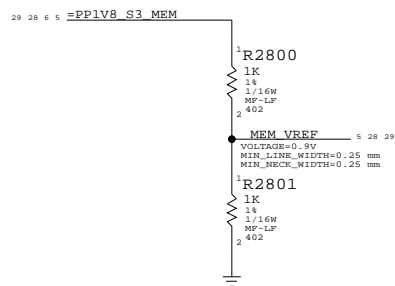
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

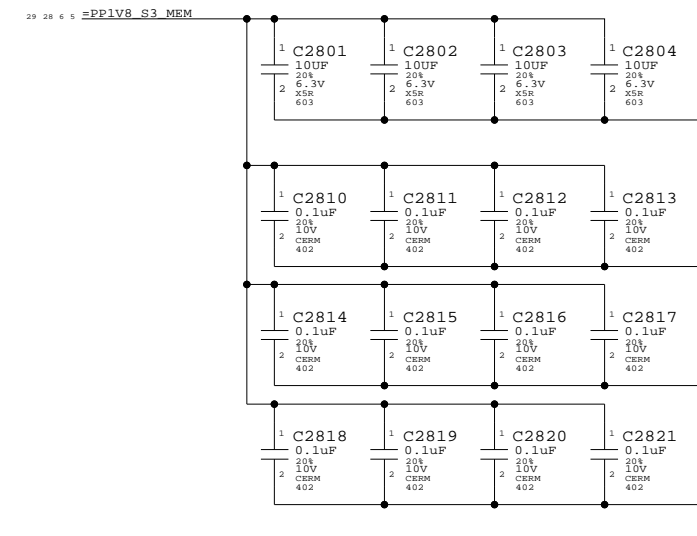
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 28 OF 97	

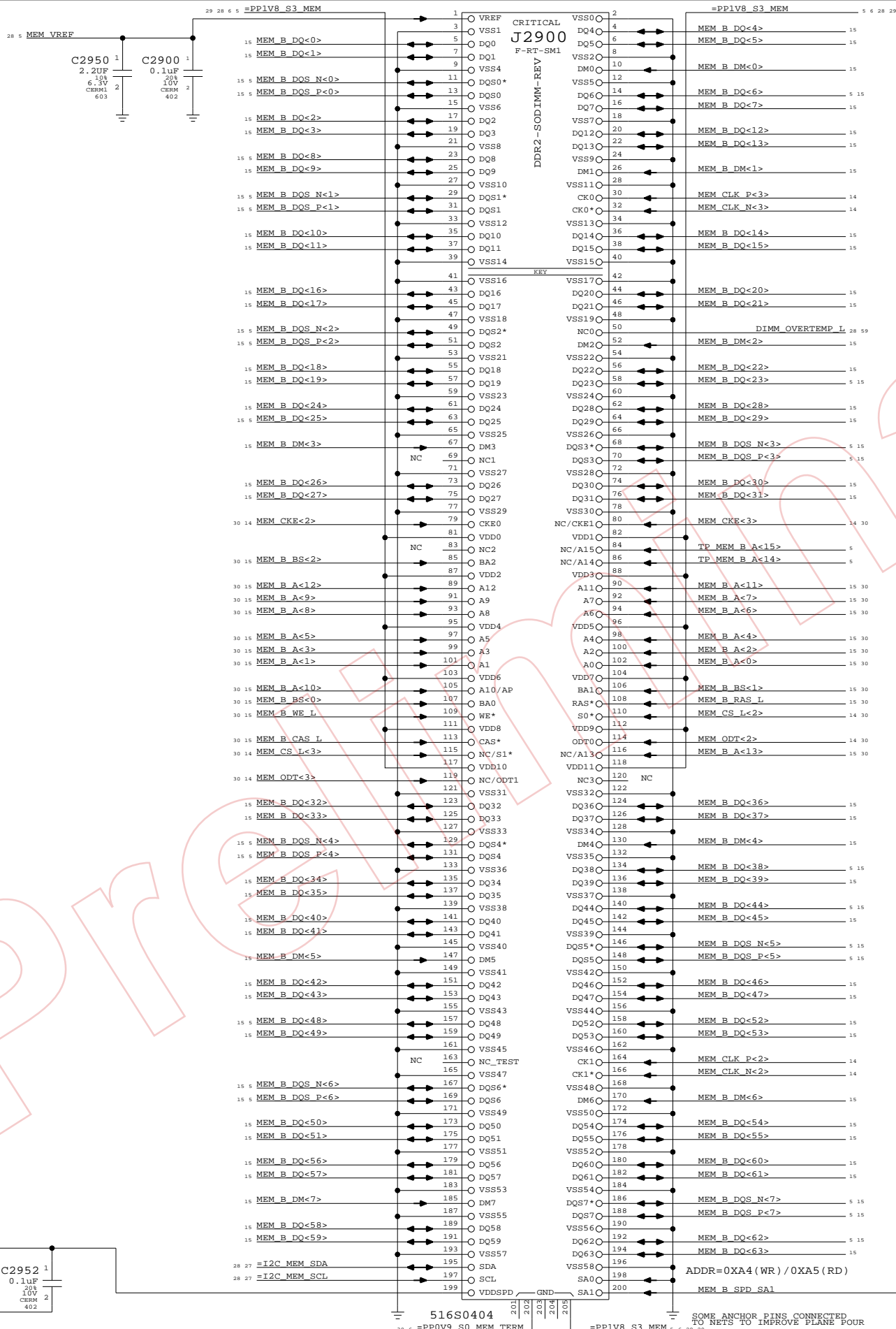
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

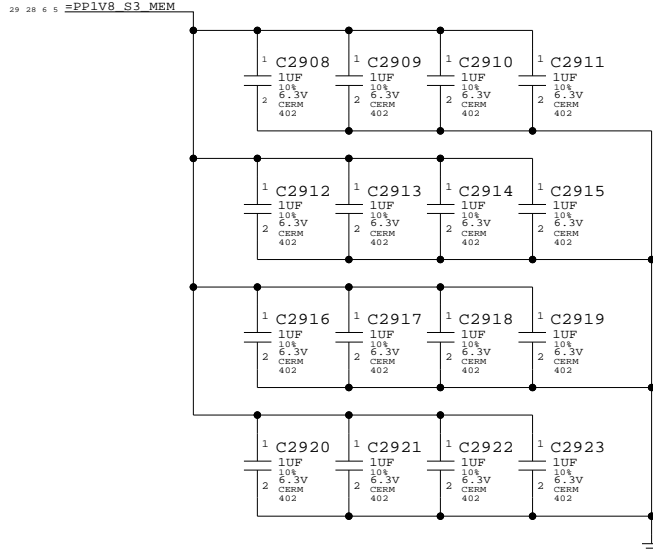
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.

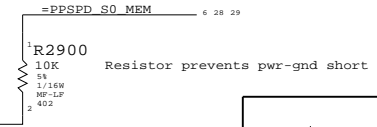


DDR2 Bypass Caps
 (For return current)



DDR2 SO-DIMM Connector B	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	

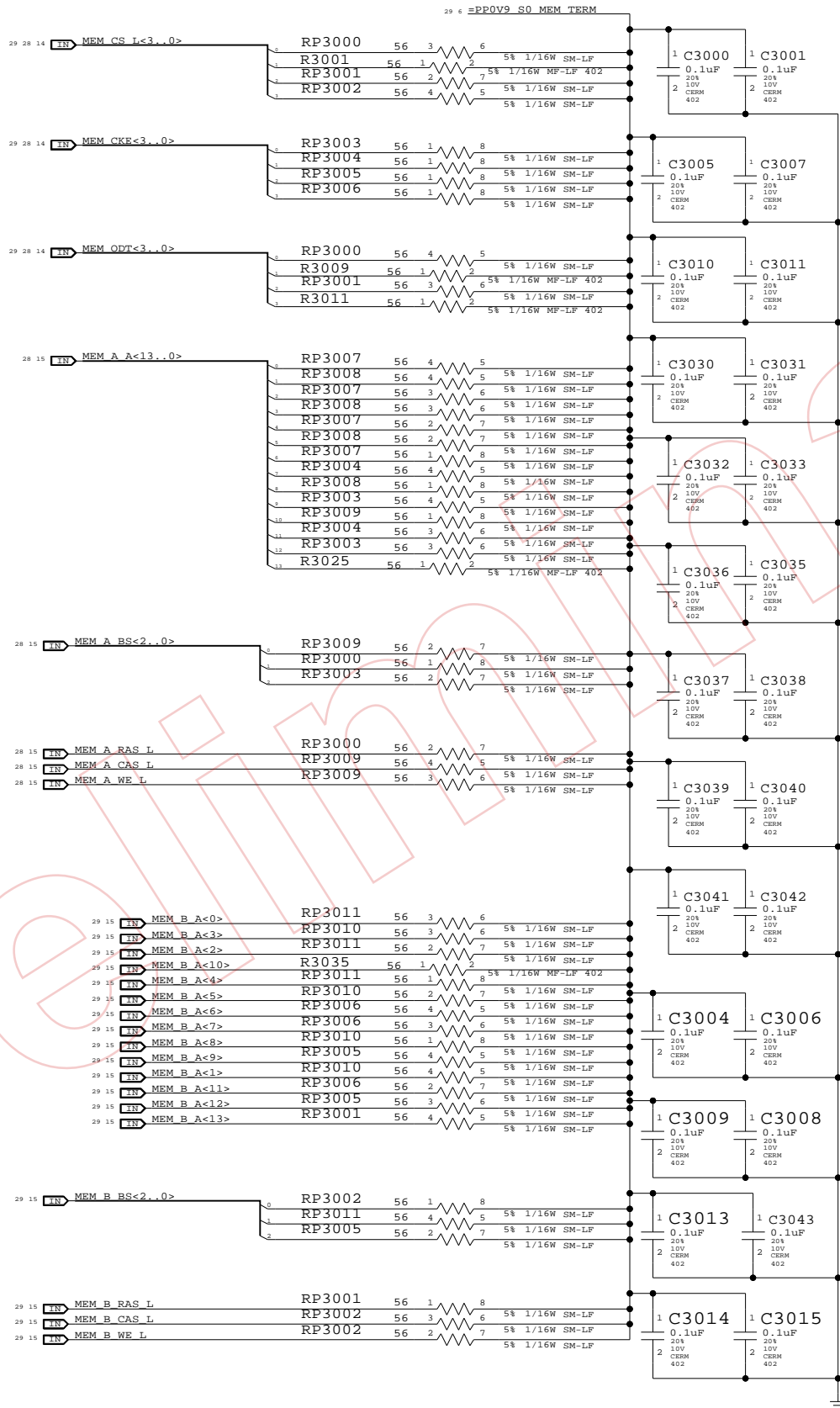
	SCALE	SHEET	REV.
	NONE	29 OF 97	A



D
C
B
A

D
C
B
A

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



PRELIMINARY

Memory Active Termination

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	30 OF 97	
NONE			

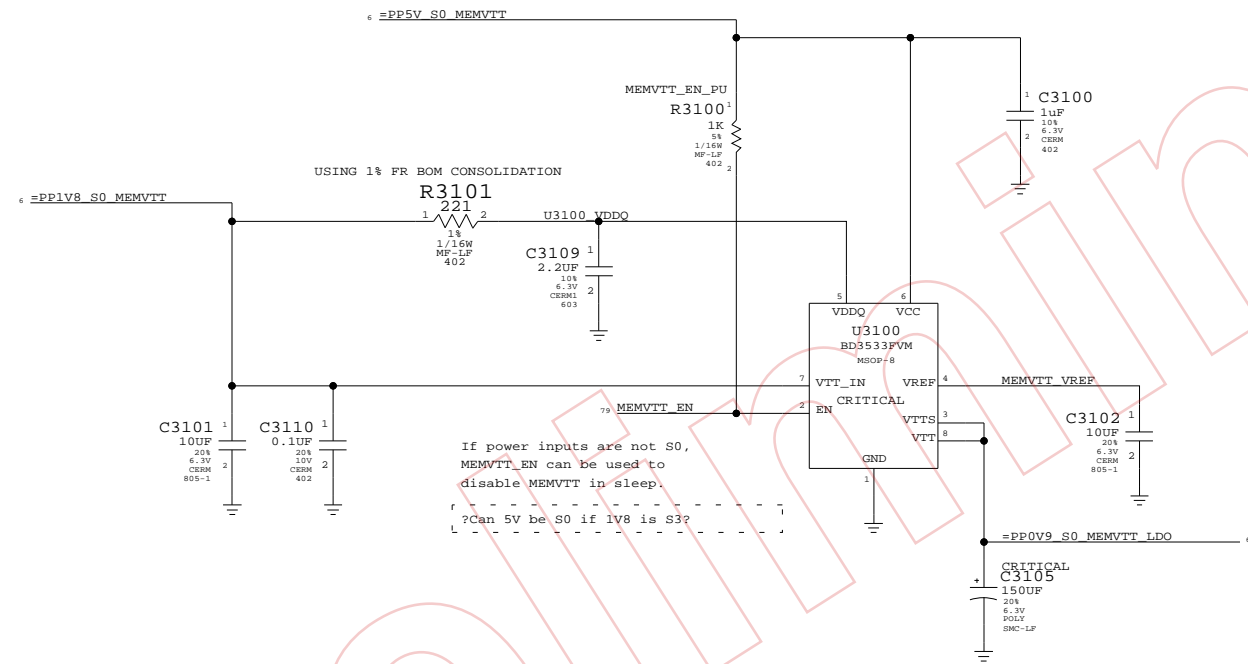
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

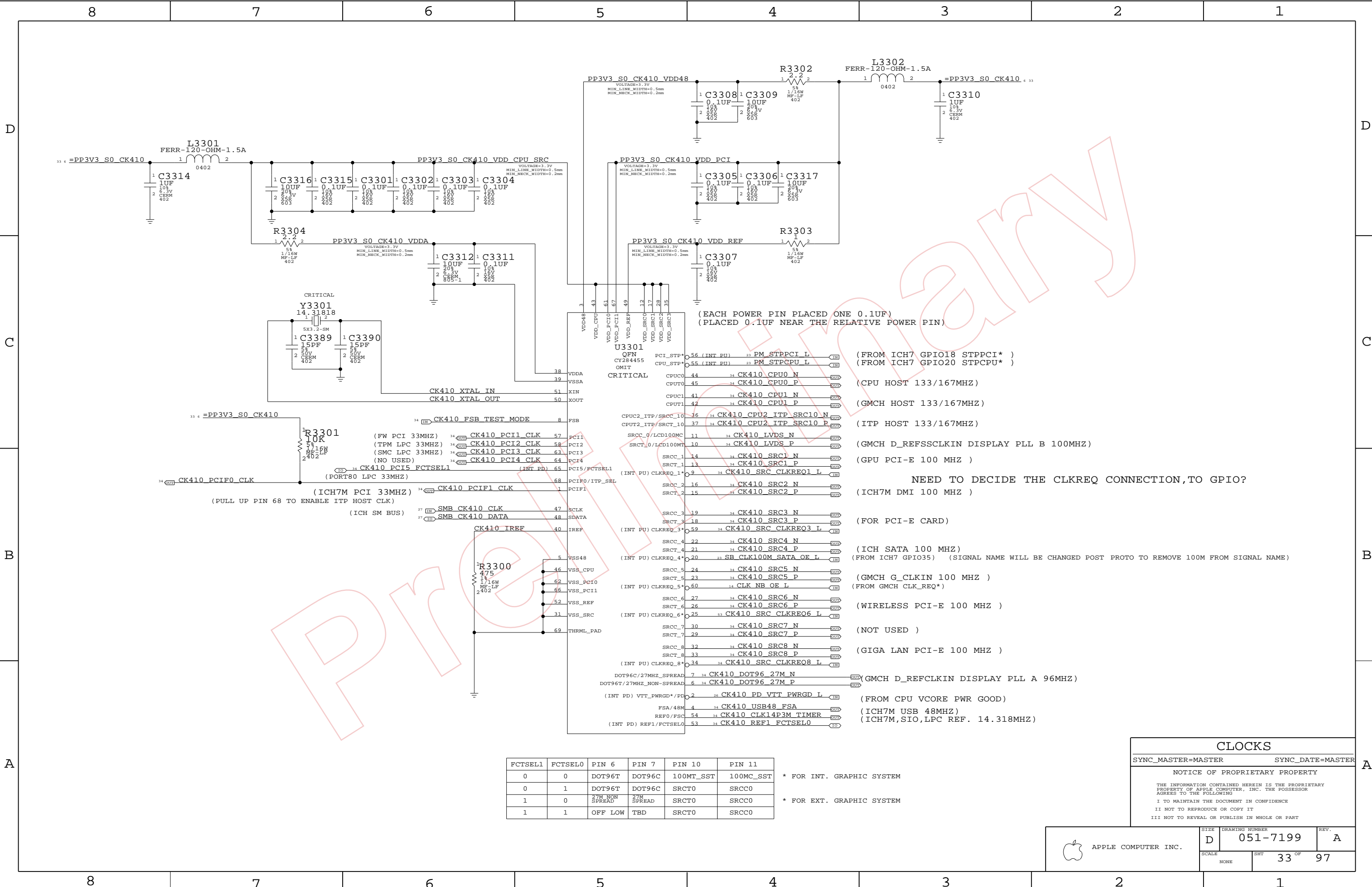
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	31 OF 97	
NONE			



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

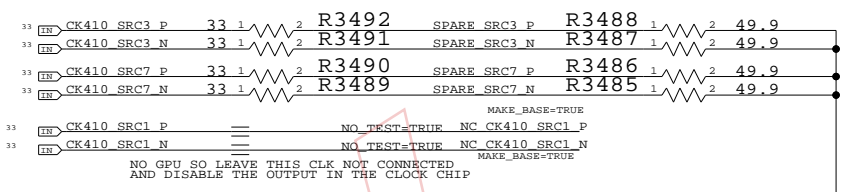
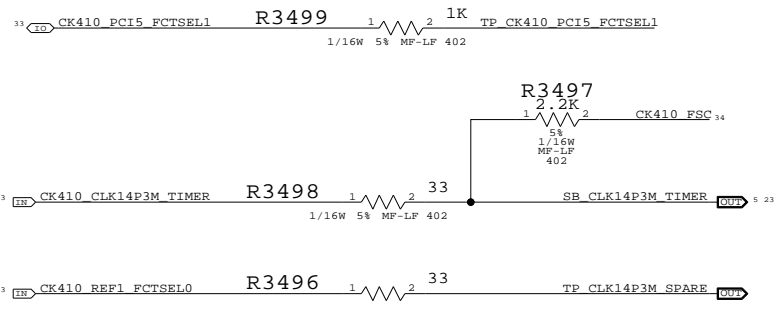
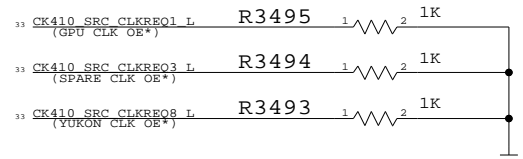
* FOR EXT. GRAPHIC SYSTEM

CLOCKS
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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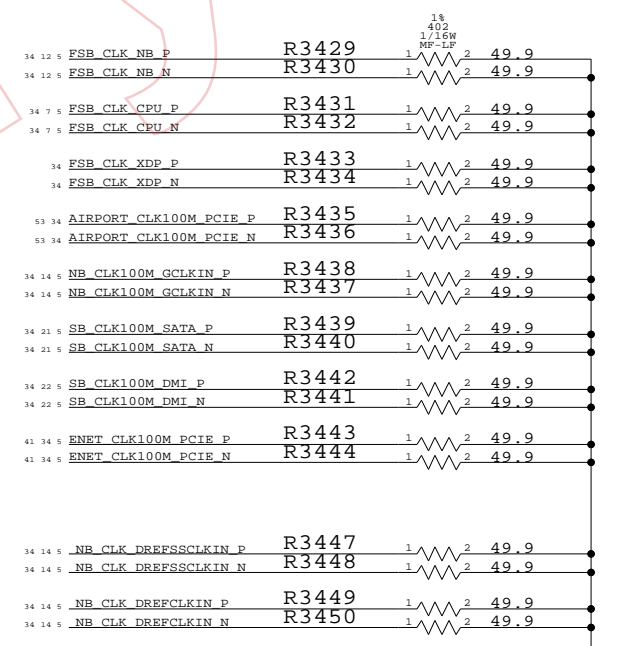
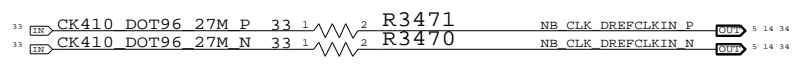
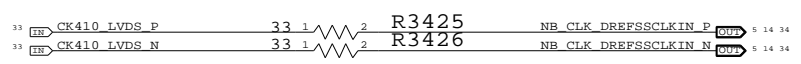
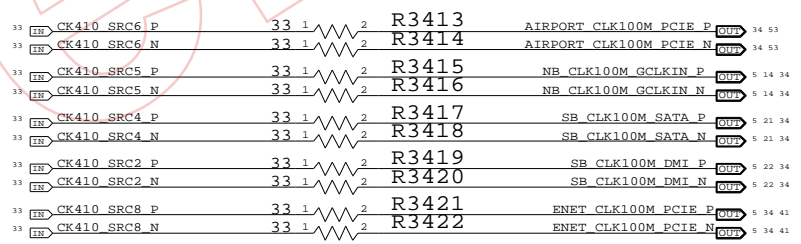
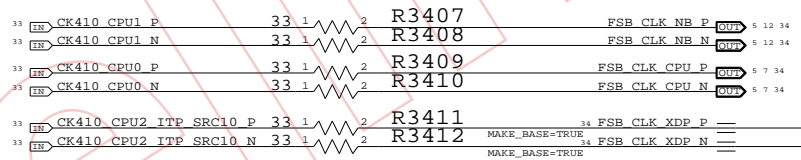
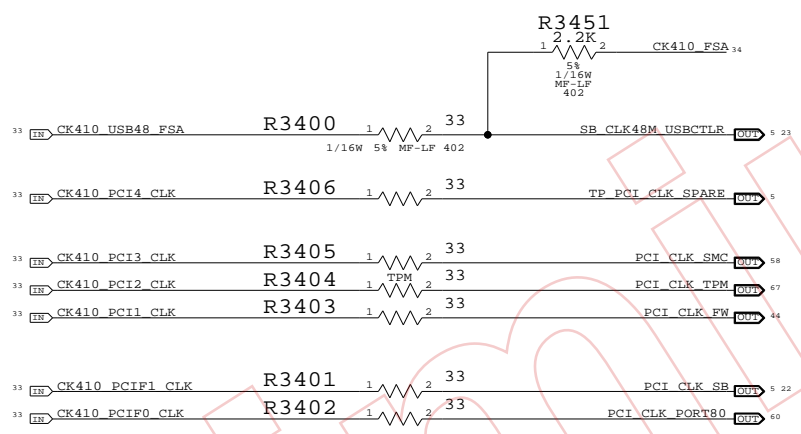
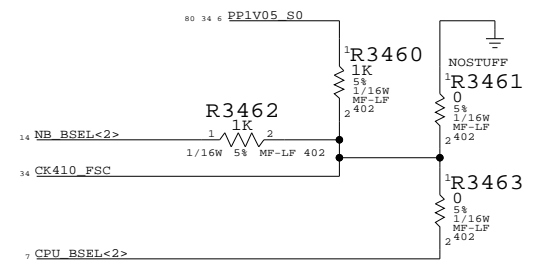
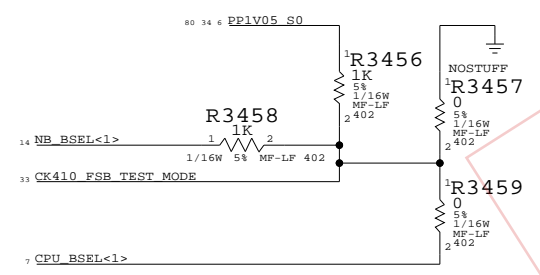
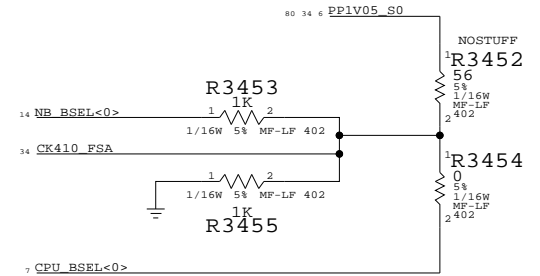
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7199	REV.: A
	SCALE: NONE	SHT: 33 OF 97	

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3452 R3453 R3454 R3455	R3456 R3457 R3458 R3459
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3456 R3457 R3458 R3459
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3456 R3457 R3458 R3459



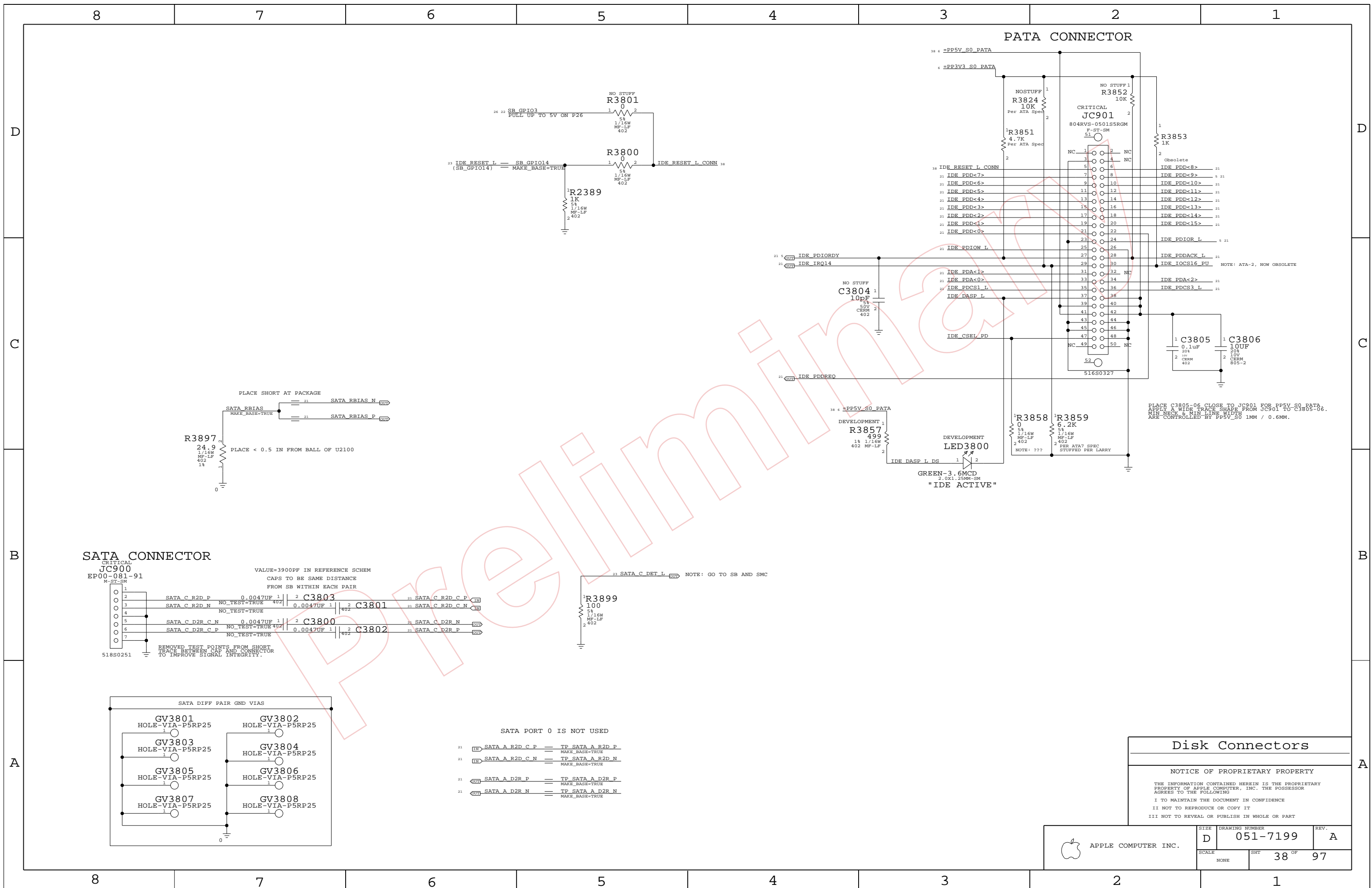
CLOCKS: TERMINATIONS

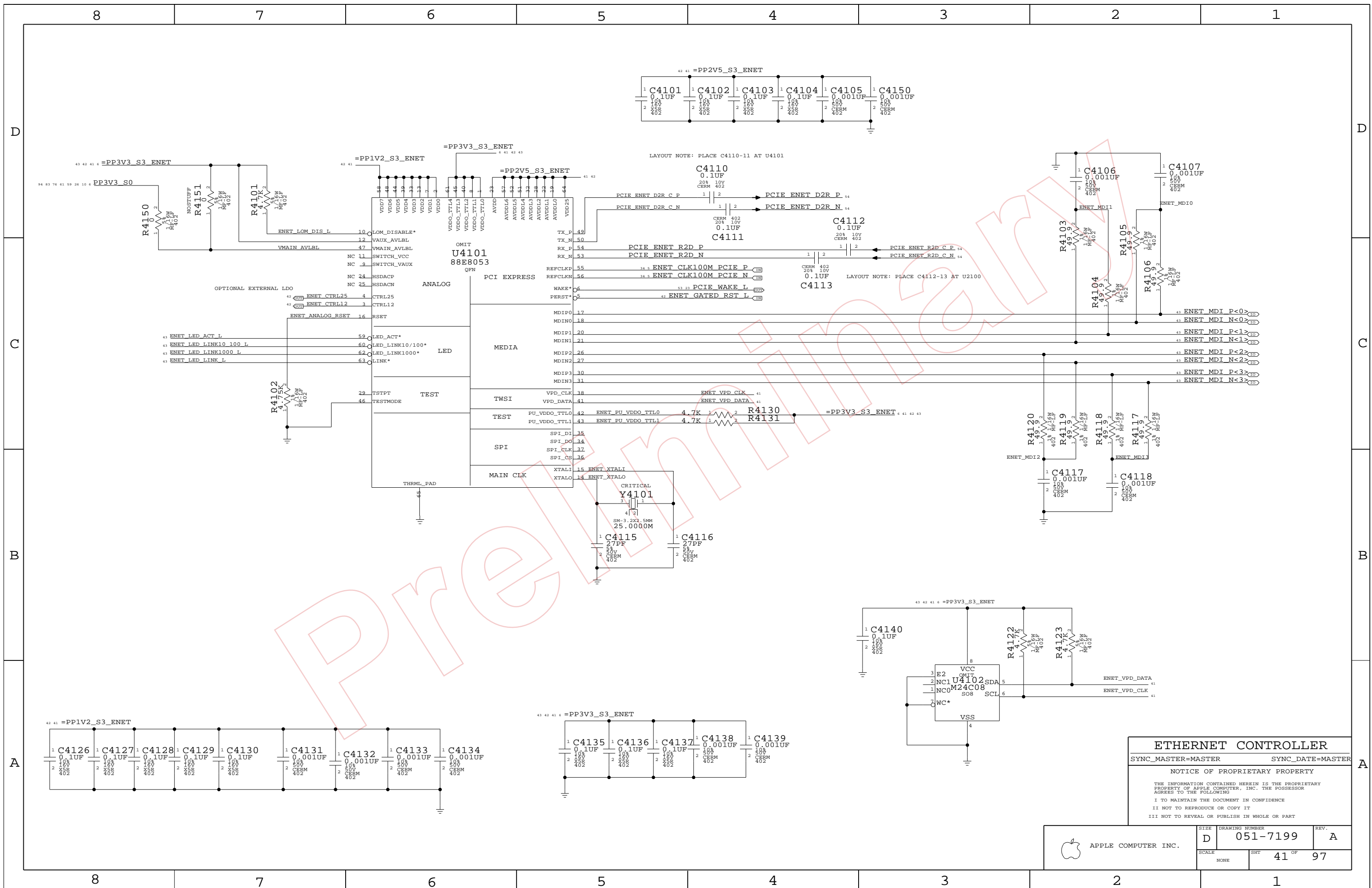
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	34 OF	97
NONE			





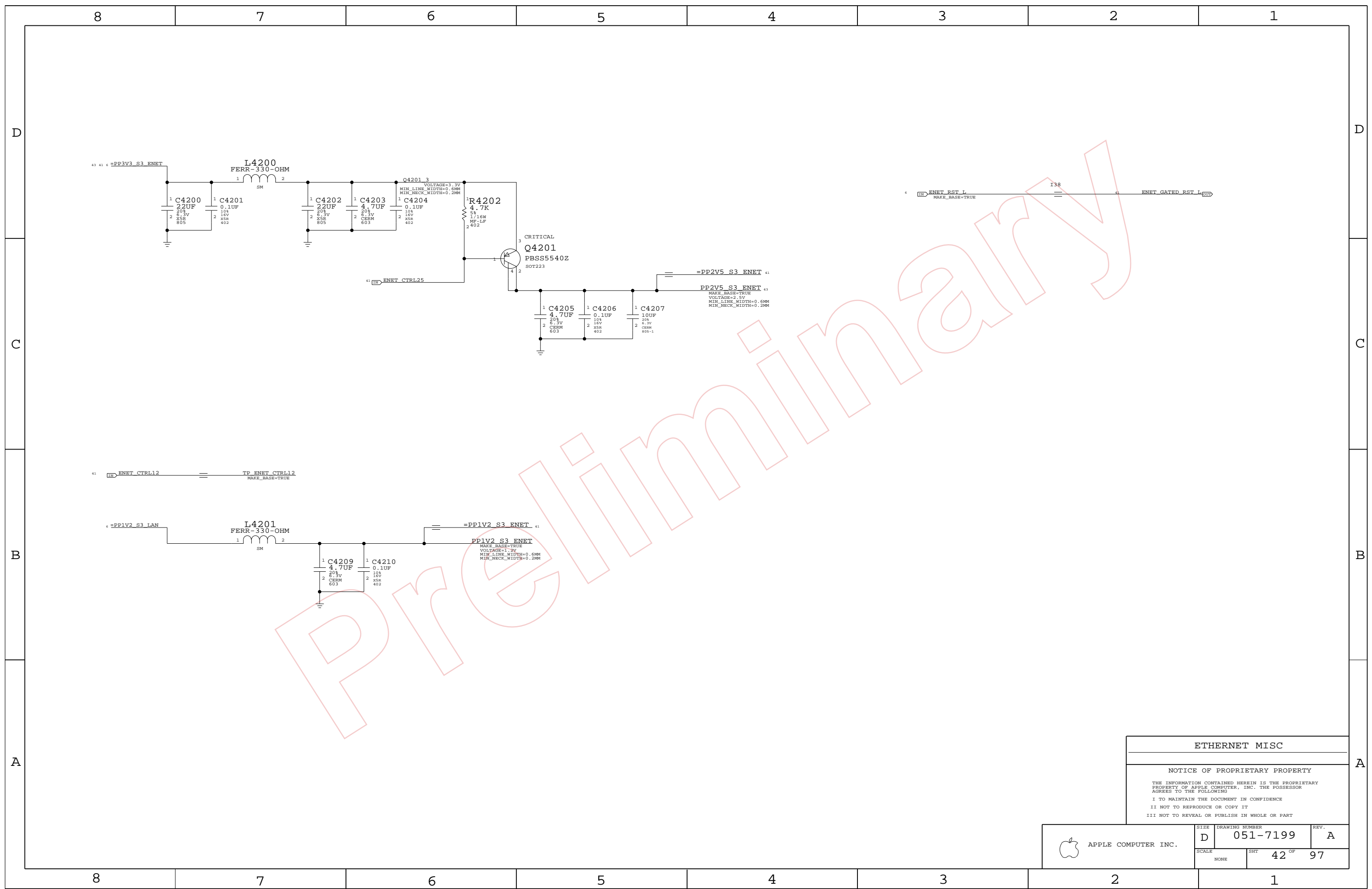
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

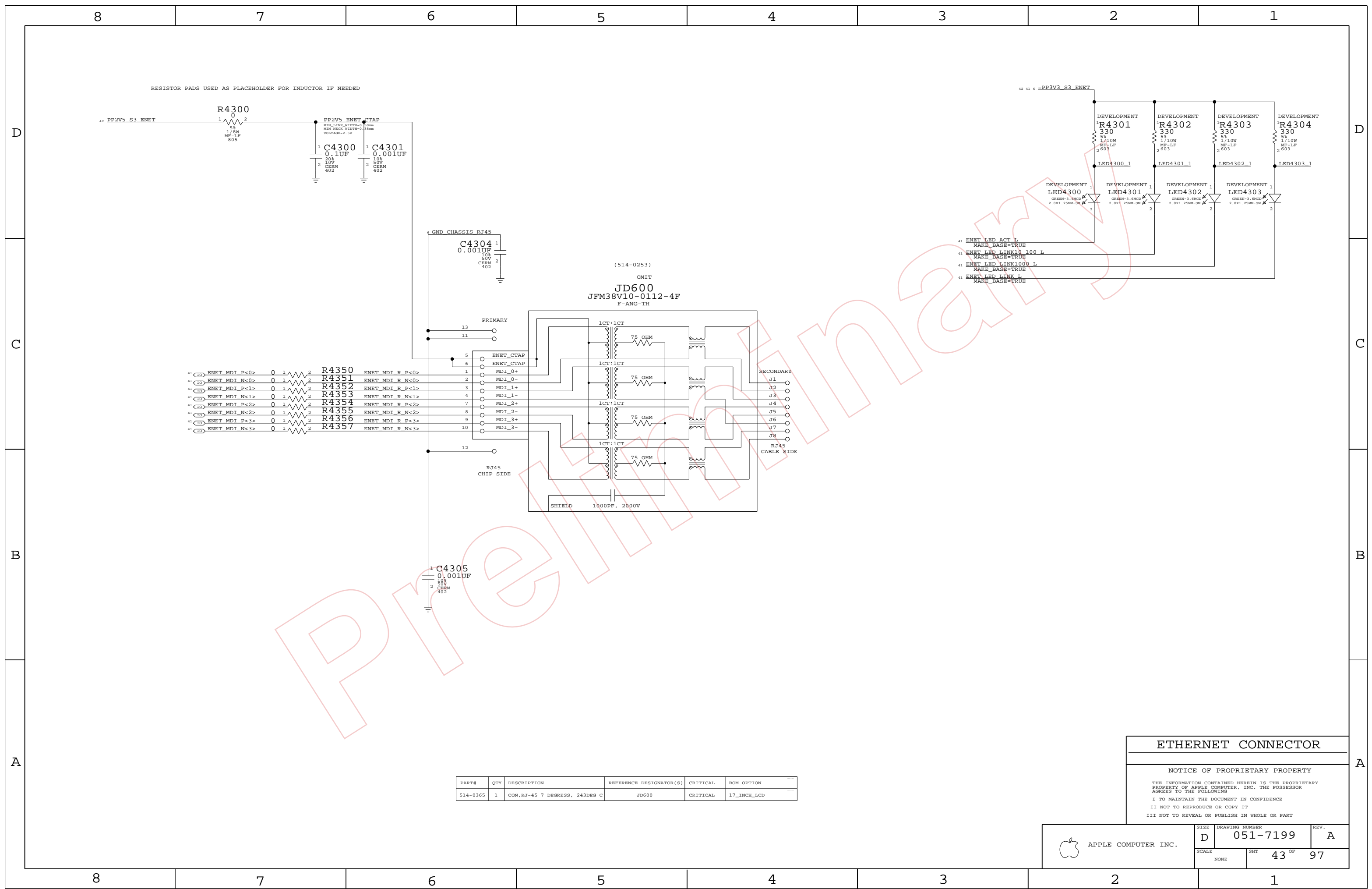
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	42 OF	97
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

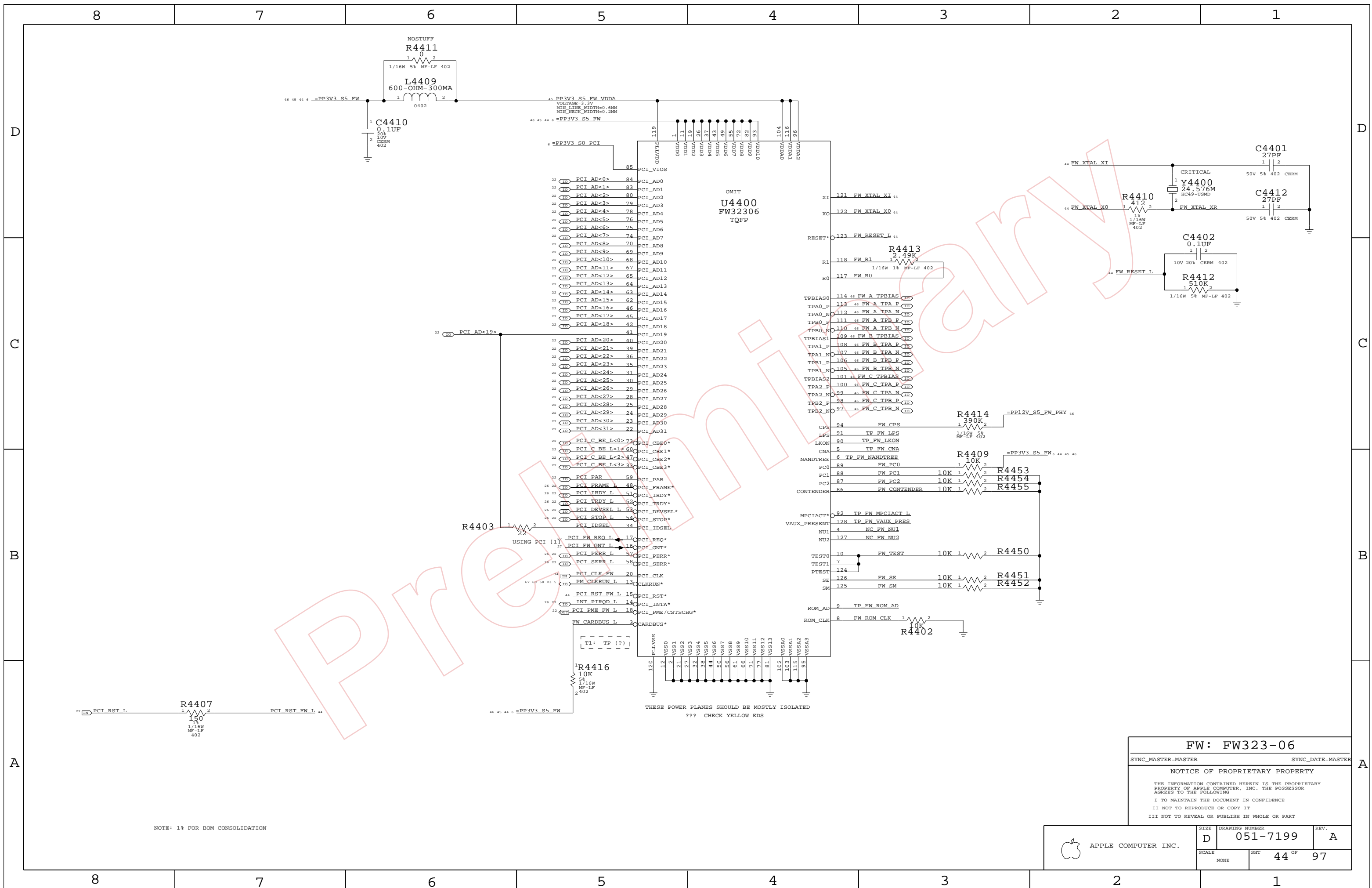
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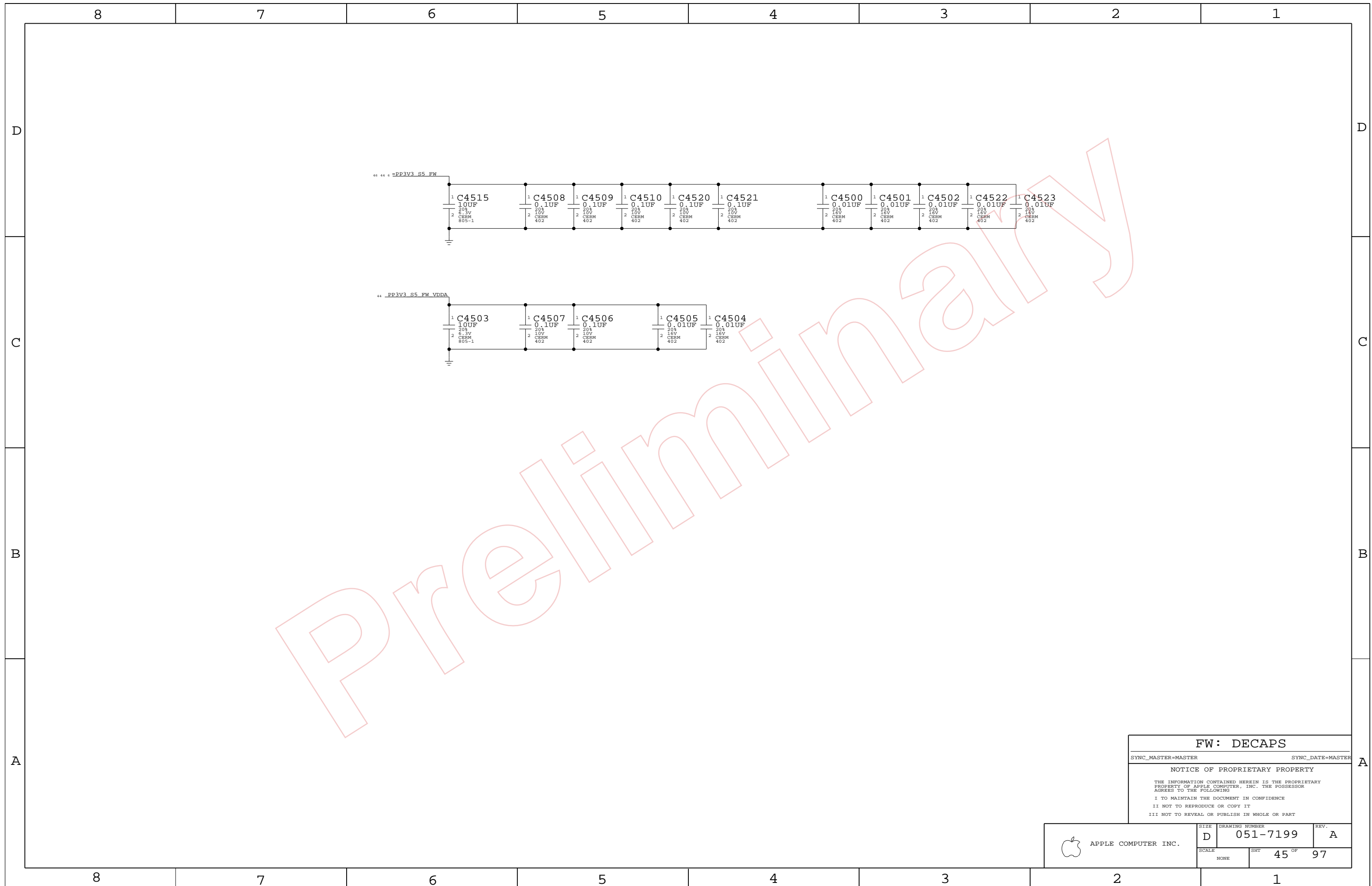
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	43 OF 97	
NONE			



NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	44 OF 97	
NONE			



Preliminary

FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

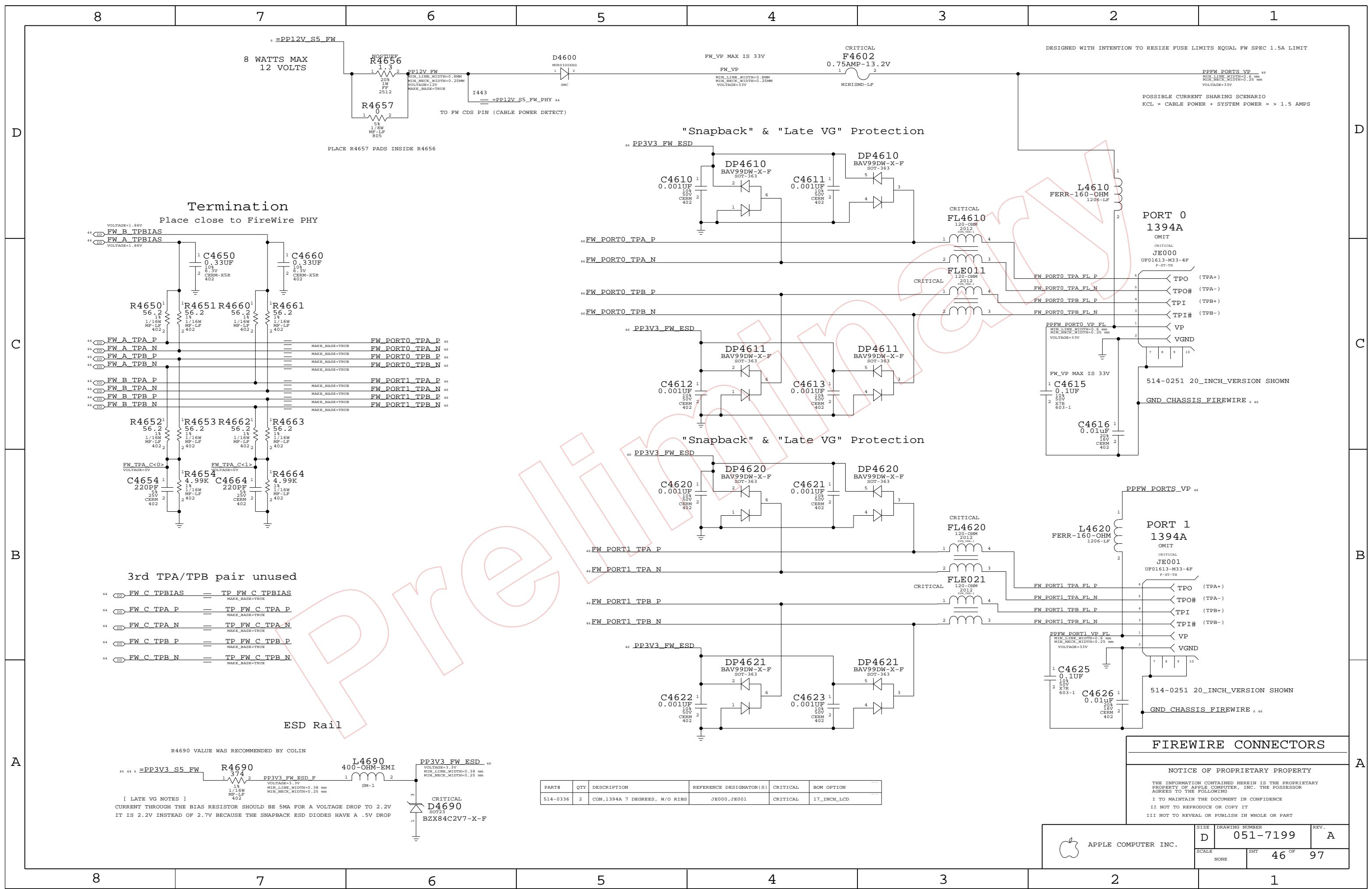
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHIT 45 OF 97	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

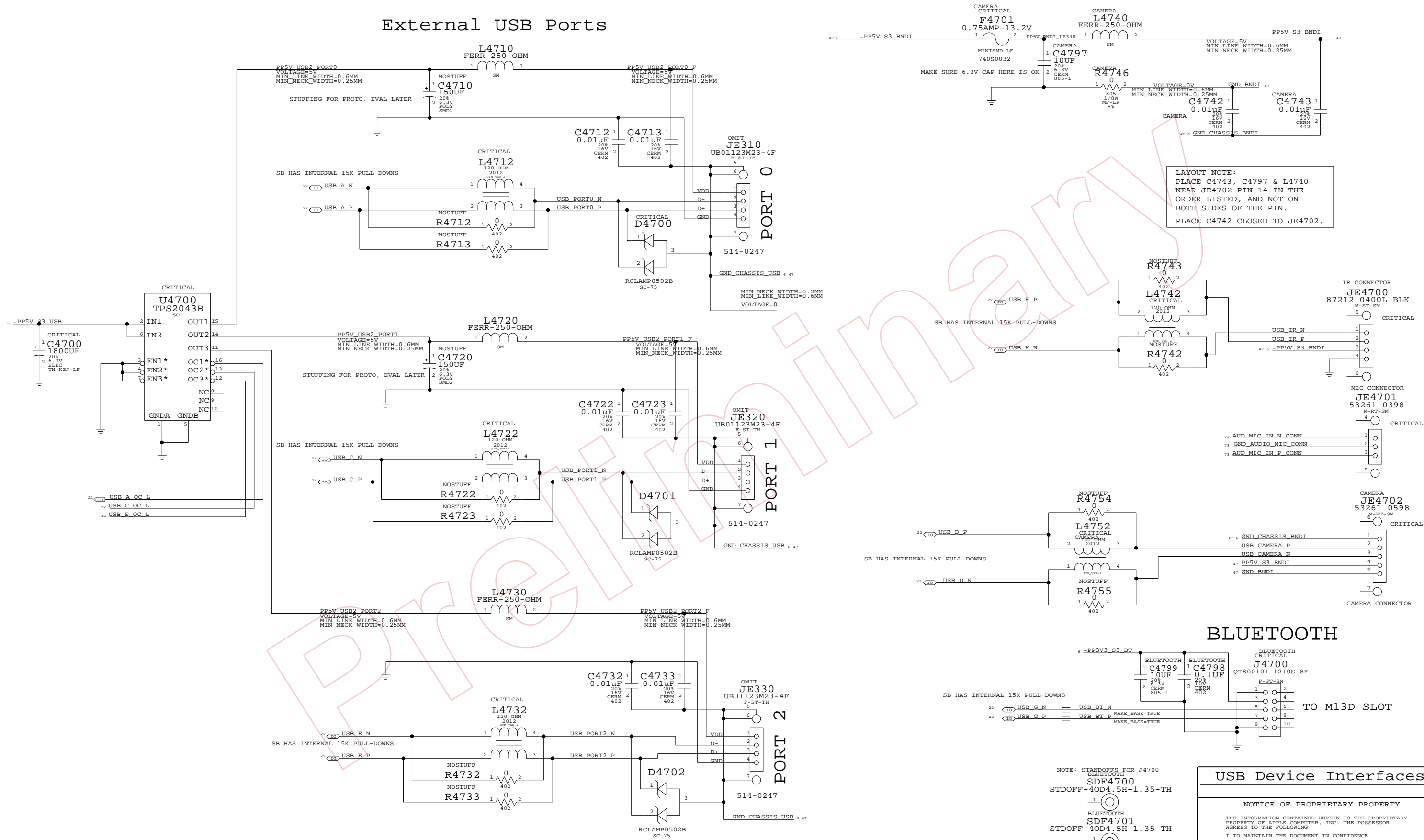
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 46 OF 97	

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE4702 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE4702.

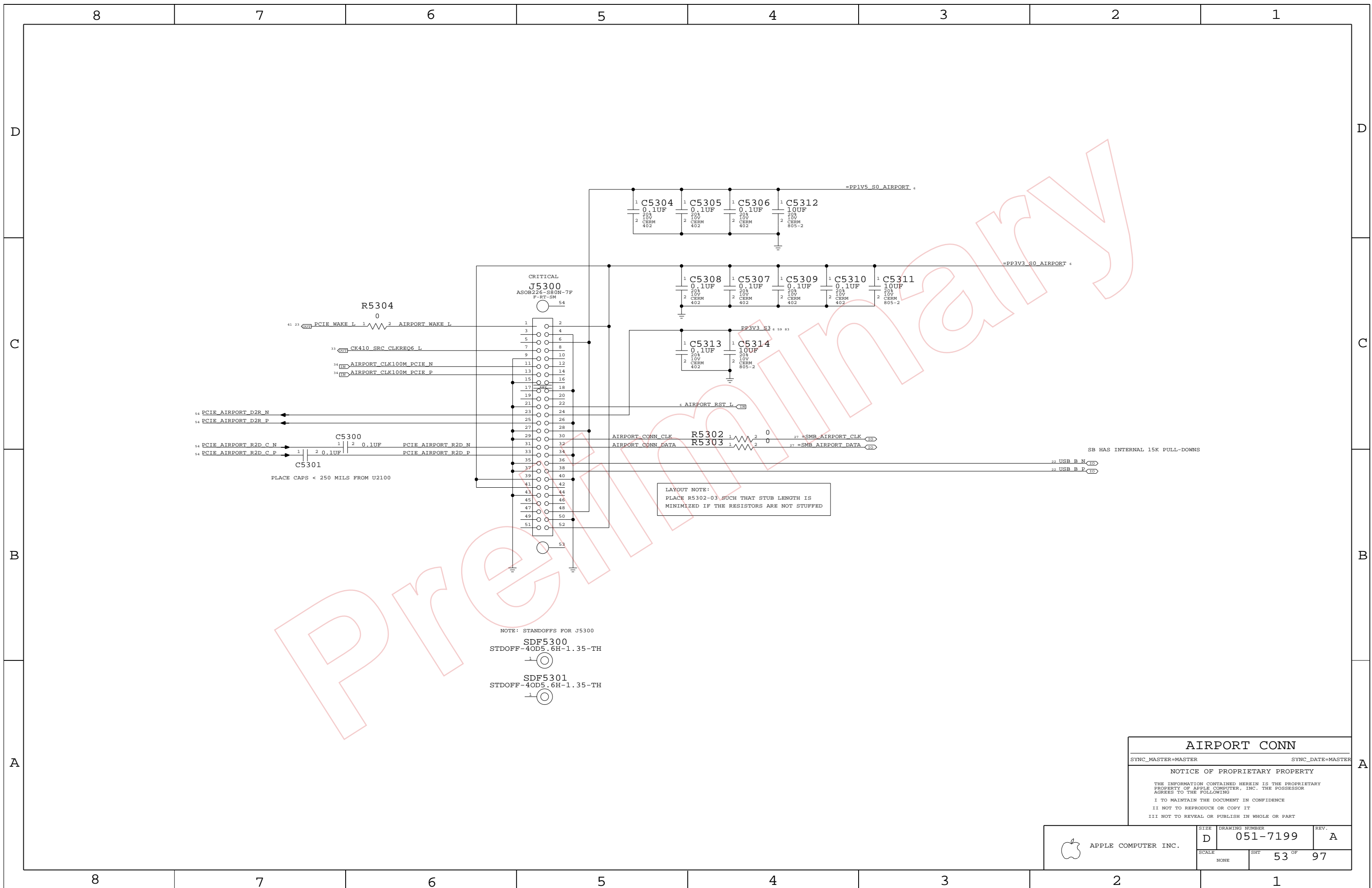
BLUETOOTH

USB Device Interfaces

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
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 47 OF 97	



PROTOTYPE

LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH

 SDF5301
 STDOFF-40D5.6H-1.35-TH


PLACE CAPS < 250 MILS FROM U2100

SB HAS INTERNAL 15K PULL-DOWNS

AIRPORT CONN

SYNC_MASTER=MASTER SYNC_DATE=MASTER


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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 53 OF 97	

D

D

C

C

B

B

A

A

22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
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22 PCIE E R2D C N == TP PCIE E R2D C N
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MAKE_BASE=TRUE

22 PCIE E D2R P == TP PCIE E D2R P
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MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

USED PCIE PORTS

22 PCIE A R2D C N == PCIE AIRPORT R2D C N 53
MAKE_BASE=TRUE

22 PCIE A R2D C P == PCIE AIRPORT R2D C P 53
MAKE_BASE=TRUE

22 5 PCIE A D2R N == PCIE AIRPORT D2R N 53
MAKE_BASE=TRUE

22 5 PCIE A D2R P == PCIE AIRPORT D2R P 53
MAKE_BASE=TRUE

22 PCIE B R2D C N == PCIE ENET R2D C N 41
MAKE_BASE=TRUE

22 PCIE B R2D C P == PCIE ENET R2D C P 41
MAKE_BASE=TRUE

22 5 PCIE B D2R N == PCIE ENET D2R N 41
MAKE_BASE=TRUE

22 5 PCIE B D2R P == PCIE ENET D2R P 41
MAKE_BASE=TRUE

Preliminary

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	54 OF 97	
NONE			

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

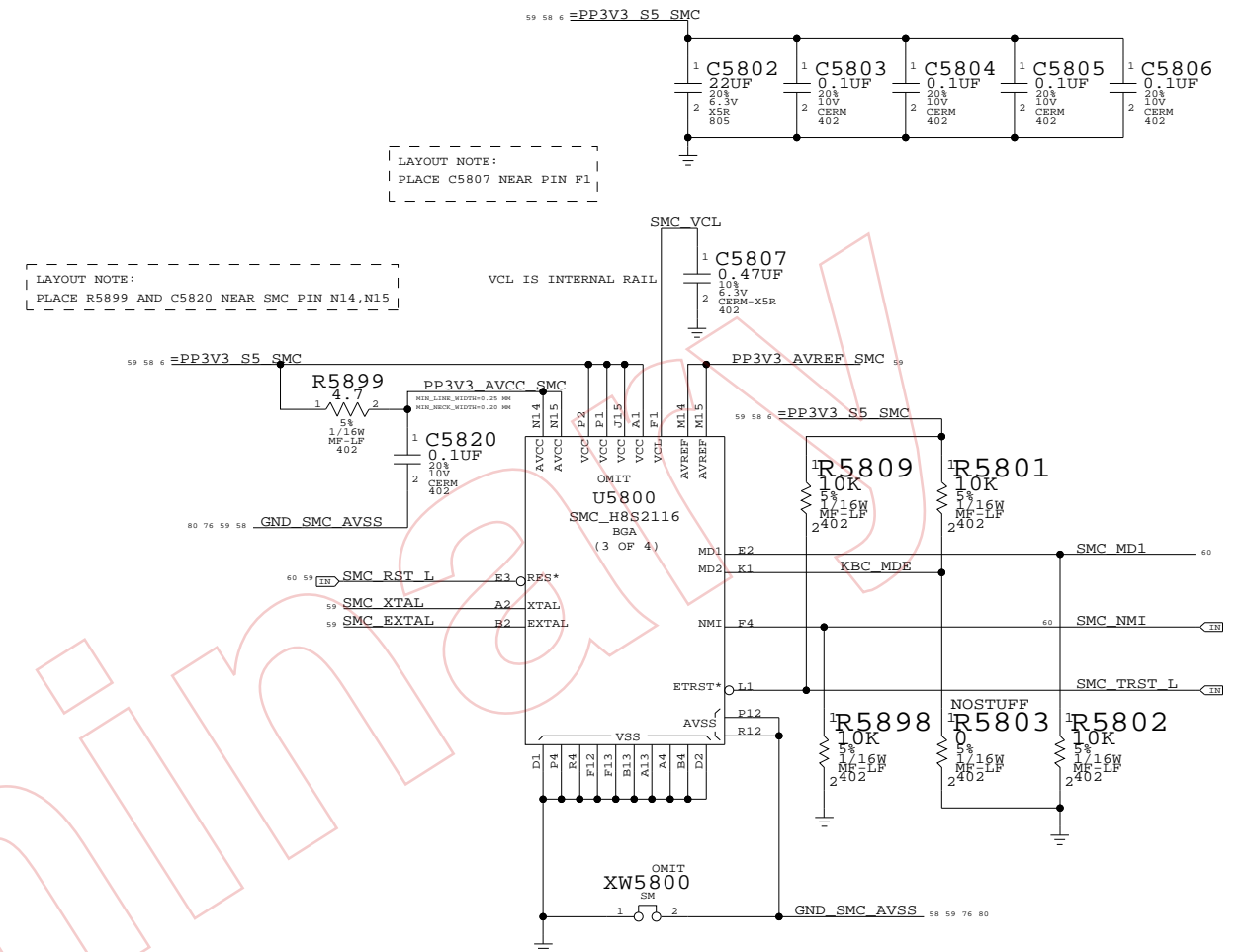
SMC_H8S2116 (1 OF 4)		SMC_H8S2116 (2 OF 4)	
PM LAN ENABLE	B12 P10	PA0/KIN8*/PA2DC	PR0 M3
SMC_RSTGATE_L	C13 P11	PA1/KIN9*/PA2DD	PR1*/ETCK M2
ALL_SYS_PWRGD	A15 P12	PM SYRST L	R2 PA2/KIN10*/PS2AC
RSMRST_PWRGD	B14 P13	SMC_TPM_RESET_L	N3 PA3/KIN11*/PS2AD
SMC_SB_NMI	B15 P14	PM_EXITS_L	R1 PA4/KIN12*/PS2BC
PM_RSMRST_L	C14 P15	PM_THRM_L	N2 PA5/KIN13*/PS2BD
IMVP_VR_ON	D12 P16	SYS_ONEWIRE	M4 PA6/KIN14*/PS2CC
PM_PWRBTN_L	C15 P17	PM_BATLOW_L	N1 PA7/KIN15*/PS2CD
SMC_P20	D13 P20	SMC_EXTSMI_L	B10 PB0/LSMI*
SMC_P21	D14 P21	SMC_RUNTIME_SCI_L	A10 PB1/LSCI
SMC_P22	D15 P22	SMC_ODD_DETECT	D10 PB2
SMC_P23	E12 P23	ISENSE_CAL_EN	A11 PB3
SMC_BATT_TRICKLE_EN_L	E14 P24	SMC_EXCARD_CP	B11 PB4
SMC_BATT_CHG_EN	E15 P25	SMC_EXCARD_PWR_EN	C11 PB5
SMC_P26	E13 P26	SMC_EXCARD_OC_L	A12 PB6
SMC_P27	F14 P27	SMC_XDP_TDO_3_3	D11 PB7
LPC_AD<0>	D9 P30/LAD0	SMC_FAN_0_CTL	G14 PC0/TIOCA0/WUE8*
LPC_AD<1>	C9 P31/LAD1	SMC_FAN_1_CTL	G15 PC1/TIOC0/WUE9*
LPC_AD<2>	A9 P32/LAD2	SMC_FAN_2_CTL	G13 PC2/TIOCC0/TCLKA/WUE10*
LPC_AD<3>	B9 P33/LAD3	SMC_FAN_3_CTL	G12 PC3/TIOC0/TCLKB/WUE11*
LPC_FRAME_L	D8 P34/LFRAME*	SMC_FAN_0_TACH	H14 PC4/TIOCA1/WUE12*
SMC_LRESET_L	C8 P35/LRESET*	SMC_FAN_1_TACH	H15 PC5/TIOCB1/TCLKC/WUE13*
PCI_CLK_SMC	A8 P36/LCLK	SMC_FAN_2_TACH	H13 PC6/TIOCA2/WUE14*
INT_SERIRQ	D7 P37/SERIRQ	SMC_FAN_3_TACH	H12 PC7/TIOCB2/TCLKD/WUE15*
SMC_XDP_TMS	A5 P40/TMIO	SMS_X_AXIS	M11 PD0/AN8
SMC_SYS_LED_16B	B5 P41/TMO0	SMS_Y_AXIS	P11 PD1/AN9
SMB_BSB_DATA	D5 P42/SDA1	SMS_Z_AXIS	R11 PD2/AN10
SMC_TPM_PP	C3 P43/TM11/EXSCK1	SMC_ANALOG_ID	N11 PD3/AN11
SMC_XDP_TRST_L	B1 P44/TMO1	SMC_NB_ISENSE	P10 PD4/AN12
SMC_XDP_TCK	C2 P45	SMC_MEM_ISENSE	R10 PD5/AN13
SMC_SYS_LED	D3 P46/PWX0/PWM0	ALS_LEFT	N10 PD6/AN14
SMC_SYS_KBDLED	C1 P47/PWX1/PWM1	ALS_RIGHT	M10 PD7/AN15
SMC_TX_L	G1 P50		
SMC_RX_L	G4 P51		
SMB_0_S0_CLK	F2 P52/SCL0		

SMC_H8S2116 (3 OF 4)		SMC_H8S2116 (4 OF 4)	
SMC_PM_G2_EN	L12	SMC_CASE_OPEN	M3
SMC_ADAPTER_EN	L14	SMC_TCK	M2
SPI_ARB	L15	SMC_TDI	M1
SPI_SCLK	K12	SMC_TDO	L4
SPI_SI	K13	SMC_TMS	L2
SPI_SO	K14	SMC_PF0	M7
SMC_PROCHOT_3_3_L	J12	SMC_PF1	P6
SMC_CPU_INIT_3_3_L	J13	SMC_LID	R6
SMC_CPU_ISENSE	N12	SMC_CPU_RESET_3_3_L	N6
SMC_CPU_VSENSE	R13	SMC_BATT_ISET	M6
SMC_GPU_ISENSE	P13	SMC_BATT_VSET	R5
SMC_GPU_VSENSE	R14	SMC_SYS_ISET	P5
SMC_PBUS_VSENSE	R15	SMC_SYS_VSET	N5
SMC_BATT_ISENSE	N13	SPI_CE_L	P9
SMC_FWIRE_ISENSE	P15	SMC_XDP_TCK_3_3	R9
SMC_WAKE_SCI_L	C7	SMB_BSA_DATA	N9
SMC_TPM_GPIO	A7	SMB_BSA_CLK	P8
PM_CLKRUN_L	B7	SMB_A_S3_DATA	R8
PM_CLKRUN_2	B7	SMB_A_S3_CLK	MB
PM_SUS_STAT_L	D6	SMB_B_S0_DATA	R7
SC_TX_L	C6	SMB_B_S0_CLK	R7
SMC_RX_L	A6	SMC_PROCHOT	R1
SMB_BSB_CLK	B6	SMC_THRMTRIP	E3
SMC_ONOFF_L	K4	SMC_FWE	K2
SMC_BC_ACOK	J2	ALS_GAIN	C4
SMC_BS_ALRT_L	J1	SMS_INT_L	D4
PM_SLP_S3_L	J3	SMC_ONOFF_L	B3
PM_SLP_S4_L	J4		
PM_SLP_S5_L	H2		
SMC_SUS_CLK	H1		
SMB_0_S0_DATA	G2		

OMIT

U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
M3	NC4	NC16	C5
N3	NC5	NC17	A3
P3	NC6	NC18	B8
R3	NC7	NC19	E4
S3	NC8	NC20	H4
T3	NC9	NC21	M9
V3	NC10	NC22	N8
W3	NC11		



SMC

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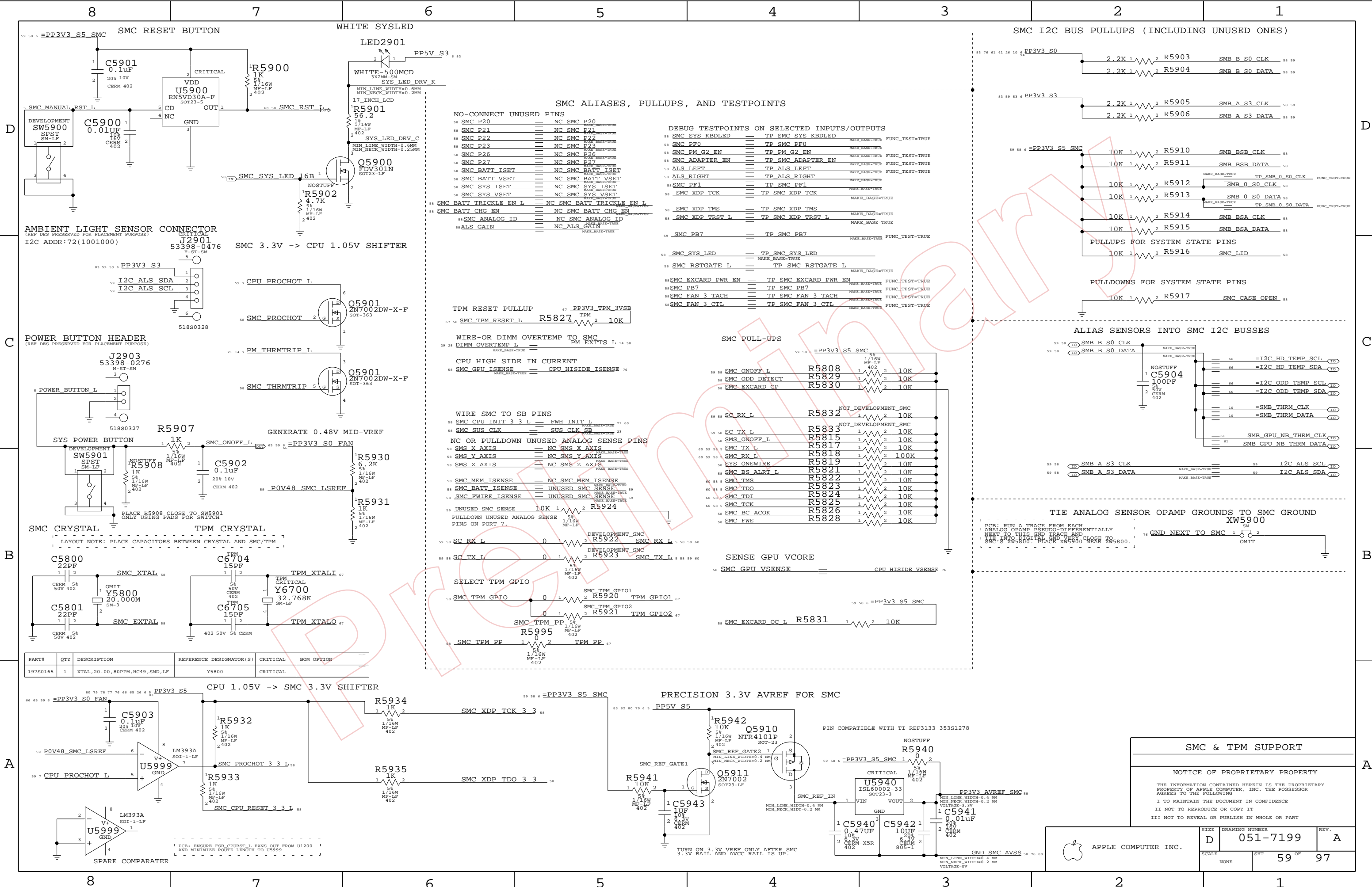
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	D	051-7199	A
SCALE	SHT	58 OF 97	
NONE			



AMBIENT LIGHT SENSOR CONNECTOR
(REF DES RESERVED FOR PLACEMENT PURPOSE)
I2C ADDR:72(1001000)

POWER BUTTON HEADER
(REF DES RESERVED FOR PLACEMENT PURPOSE)

SMC CRYSTAL
LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	TPM RESET PULLUP	WIRE-OR DIMM OVERTEMP TO SMC	CPU HIGH SIDE IN CURRENT	WIRE SMC TO SB PINS	NC OR PULLDOWN UNUSED ANALOG SENSE PINS	SMC MEM ISENSE	SMC BATT ISENSE	SMC FWIRE ISENSE	UNUSED SMC SENSE	PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7	SC RX L	SC TX L	SELECT TPM GPIO	SMC TPM PP	SMC XDP TCK 3 3	SMC XDP TDO 3 3
SMC P20	R5827	PM_EXITS_L	SMC GPU ISENSE	SMC CPU INIT 3 3 L	SMC SMS X AXIS	SMC MEM ISENSE	SMC BATT ISENSE	SMC FWIRE ISENSE	UNUSED SMC SENSE	SMC XDP TCK 3 3	SC RX L	SC TX L	SMC TPM GPIO	SMC TPM PP	SMC XDP TCK 3 3	SMC XDP TDO 3 3

ALIAS SENSORS INTO SMC I2C BUSES

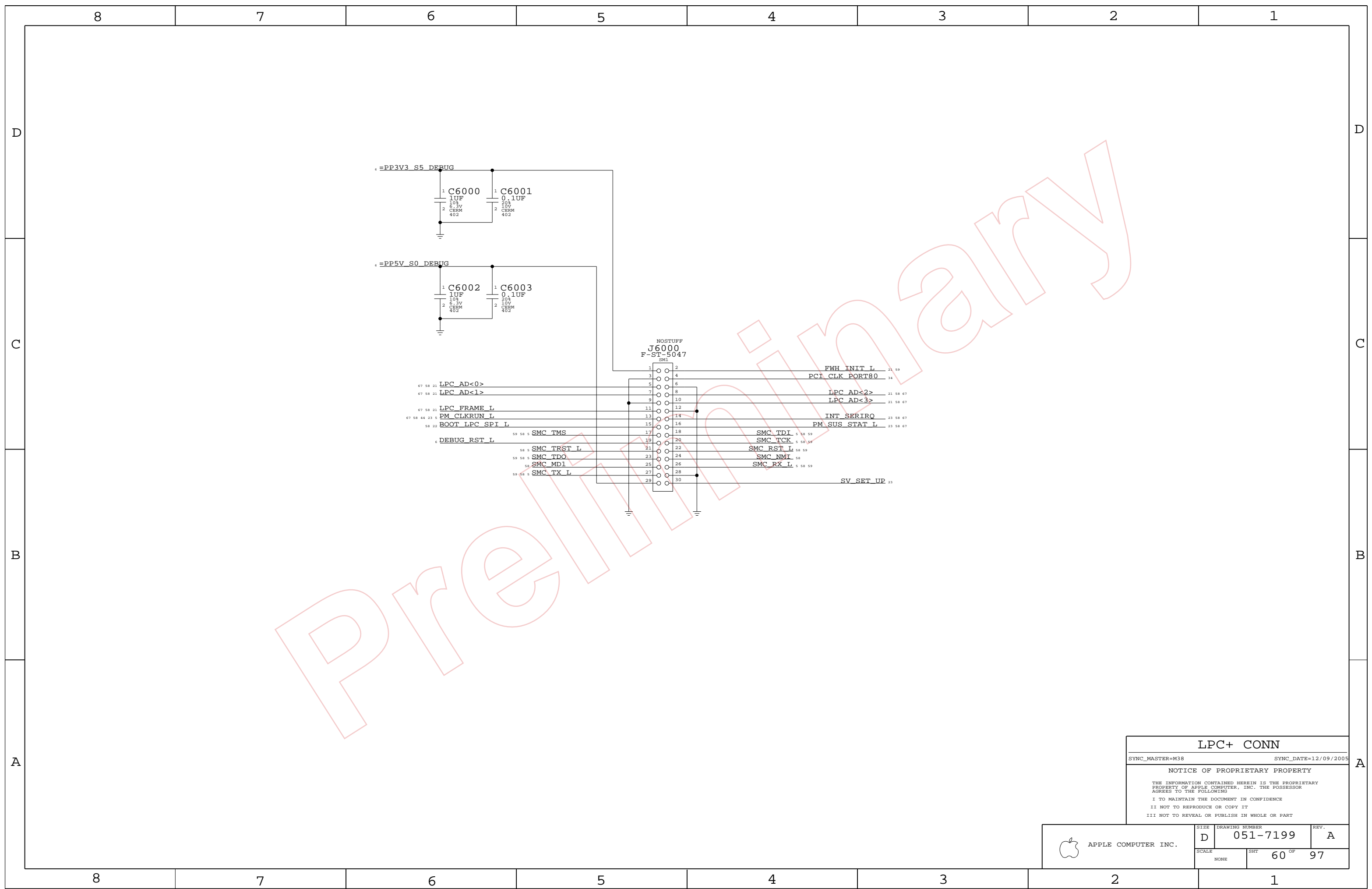
TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND
XW5900
GND NEXT TO SMC 1

SMC & TPM SUPPORT

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SCALE NONE	SHEET 59 OF 97	REV. A	SIZE D	DRAWING NUMBER 051-7199
			APPLE COMPUTER INC.	



Pre-release

LPC+ CONN

SYNC_MASTER=M38 SYNC_DATE=12/09/2005

NOTICE OF PROPRIETARY PROPERTY

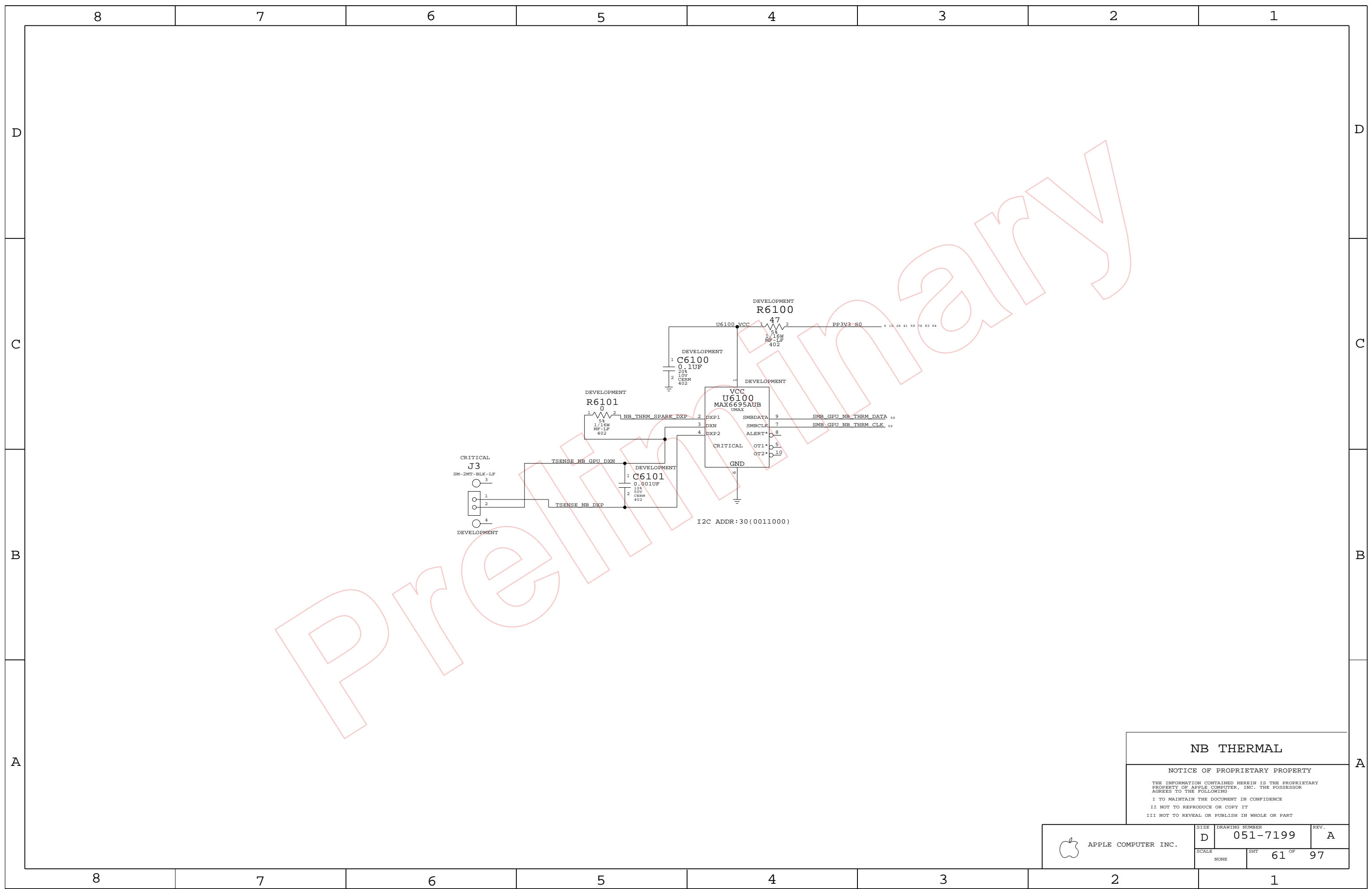
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHIT 60 OF 97	



Pre-release

NB THERMAL

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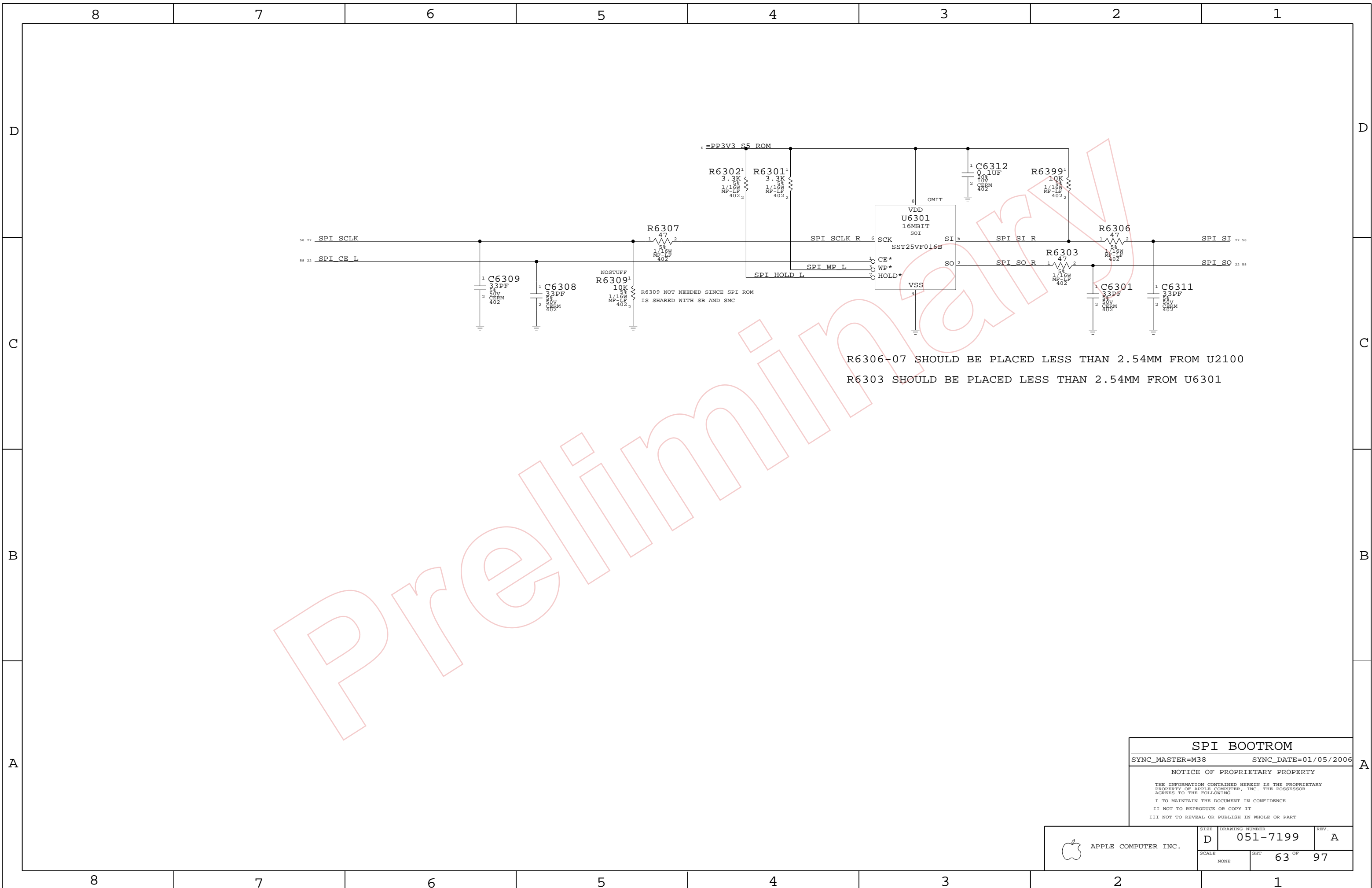
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	SCALE NONE	SHT 61 OF 97	

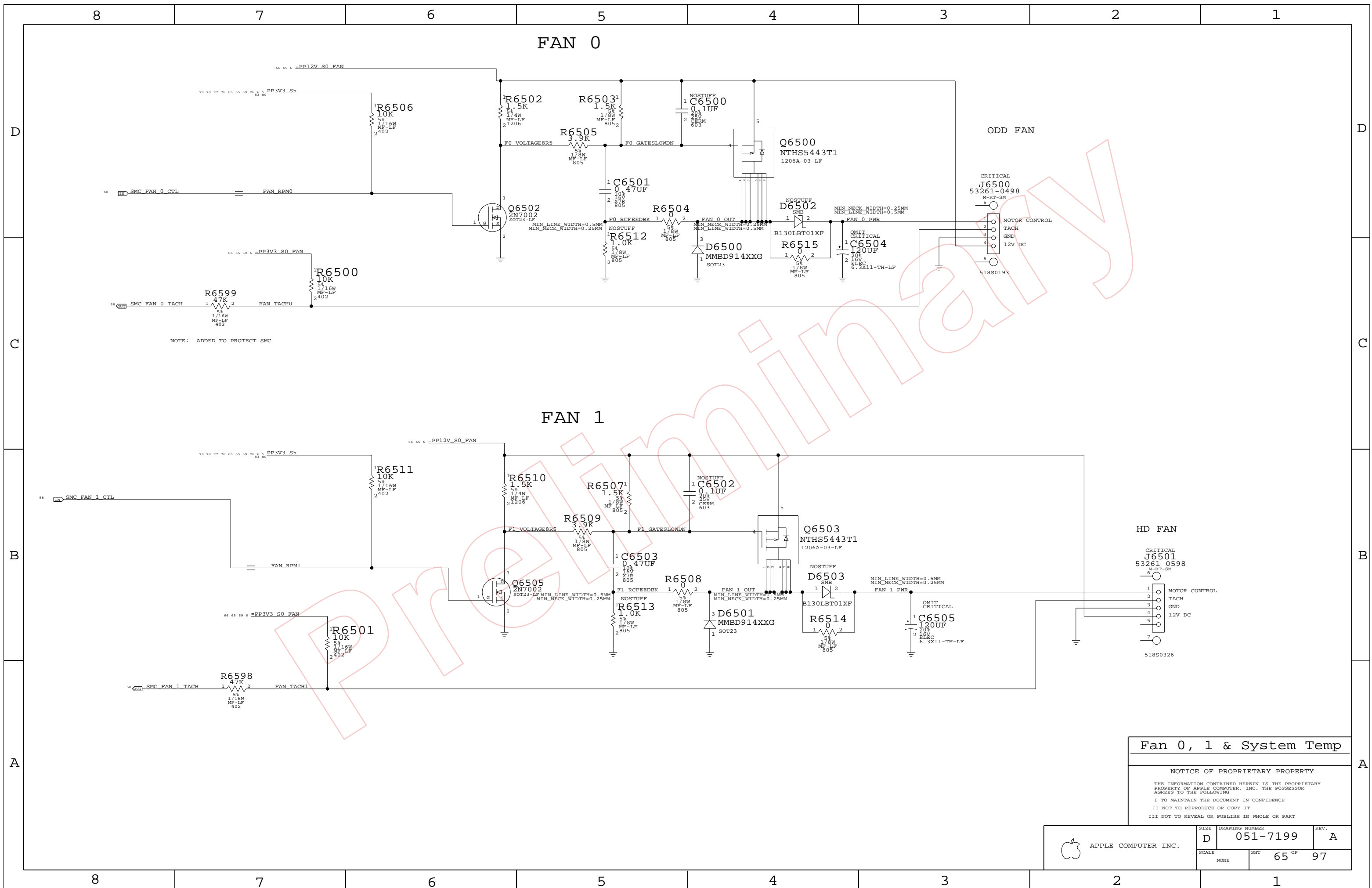


R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7199	A
SCALE	SHT		
NONE	63 OF		97

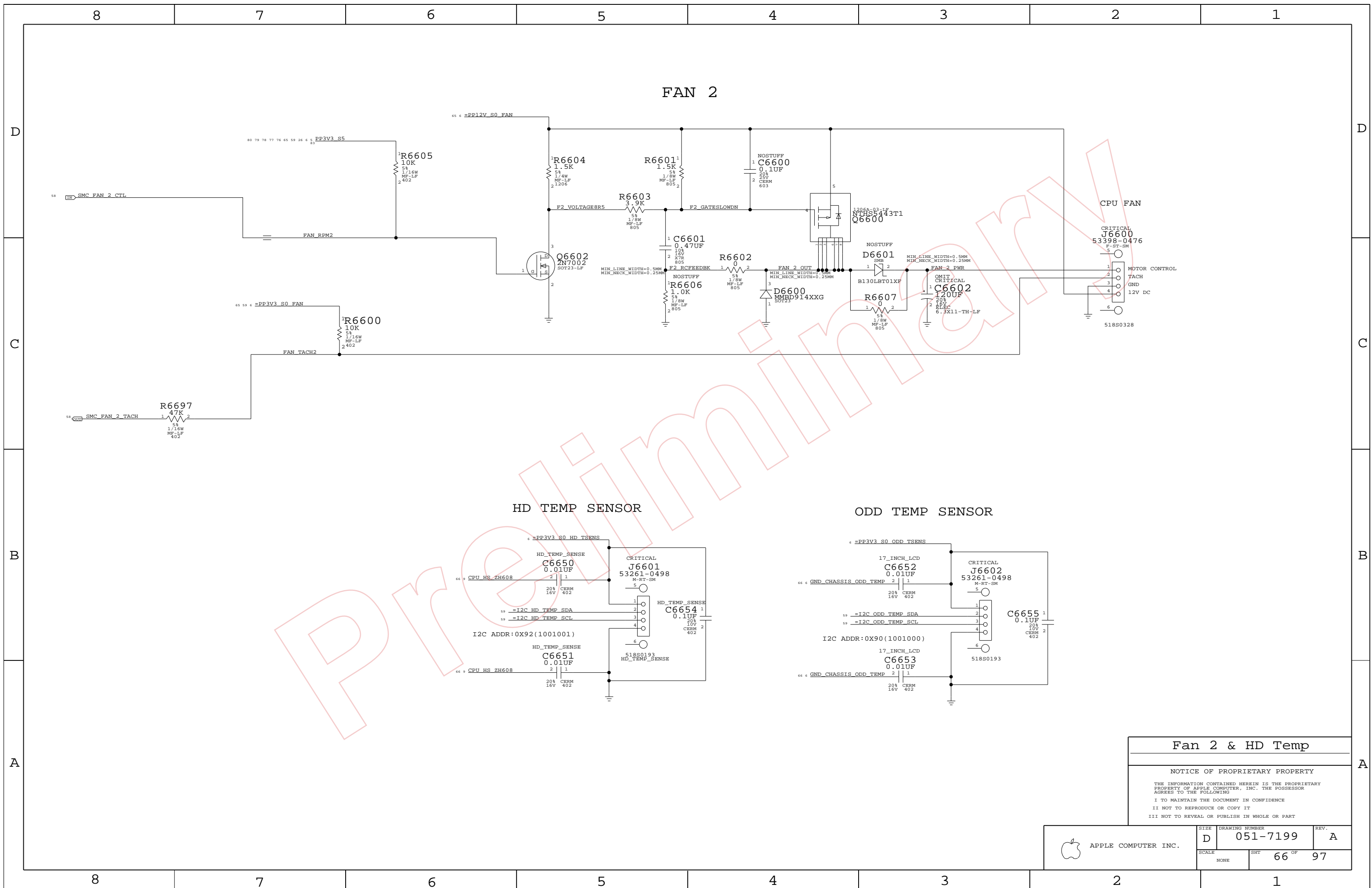


Fan 0, 1 & System Temp

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	D	051-7199	A
SCALE	SHT	65 OF	97
NONE			



FAN 2

HD TEMP SENSOR

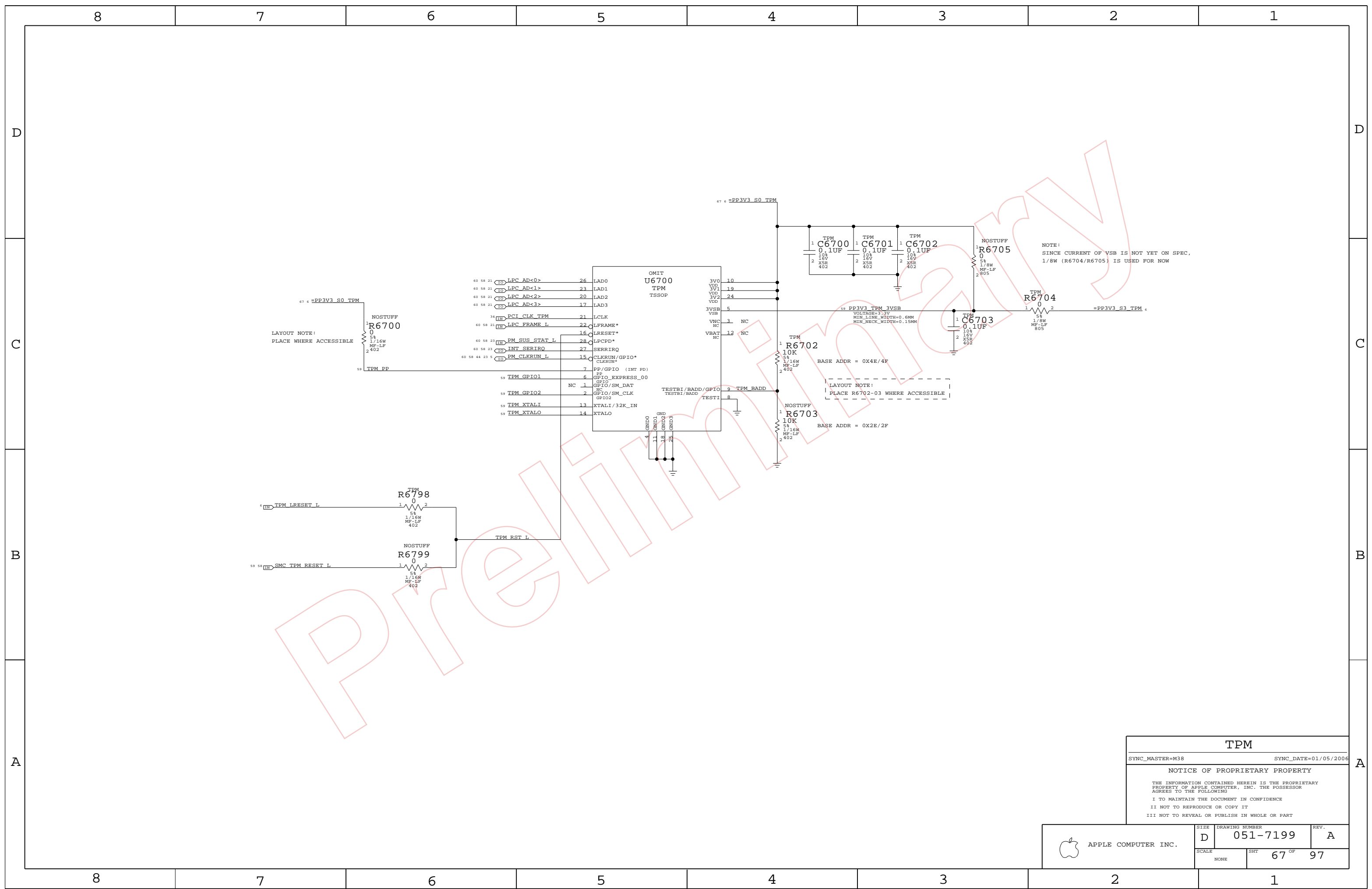
ODD TEMP SENSOR

Fan 2 & HD Temp

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	D	051-7199	A
SCALE	SHT	66 OF	97
NONE			



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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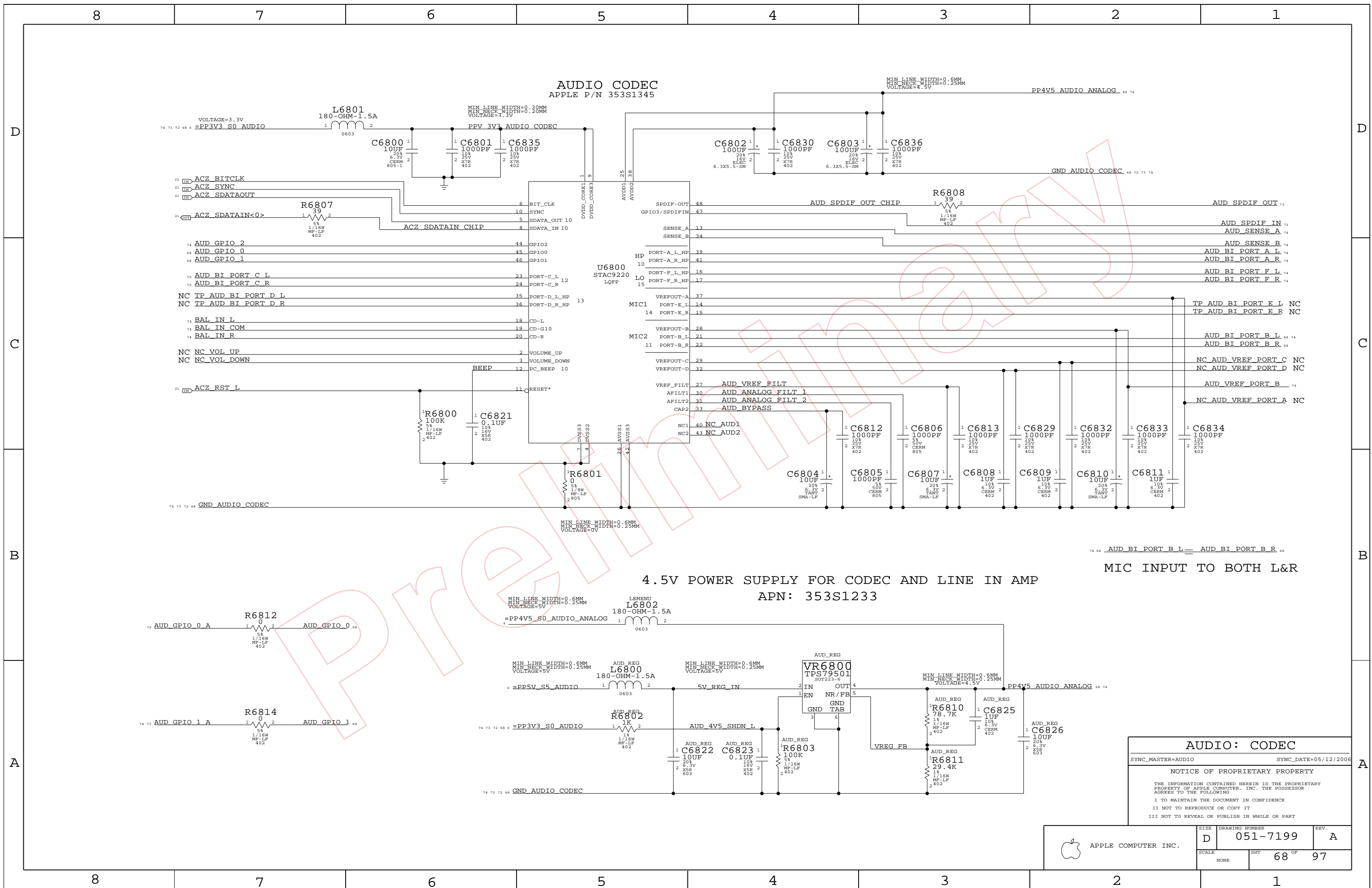
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	67 OF 97	
NONE			



AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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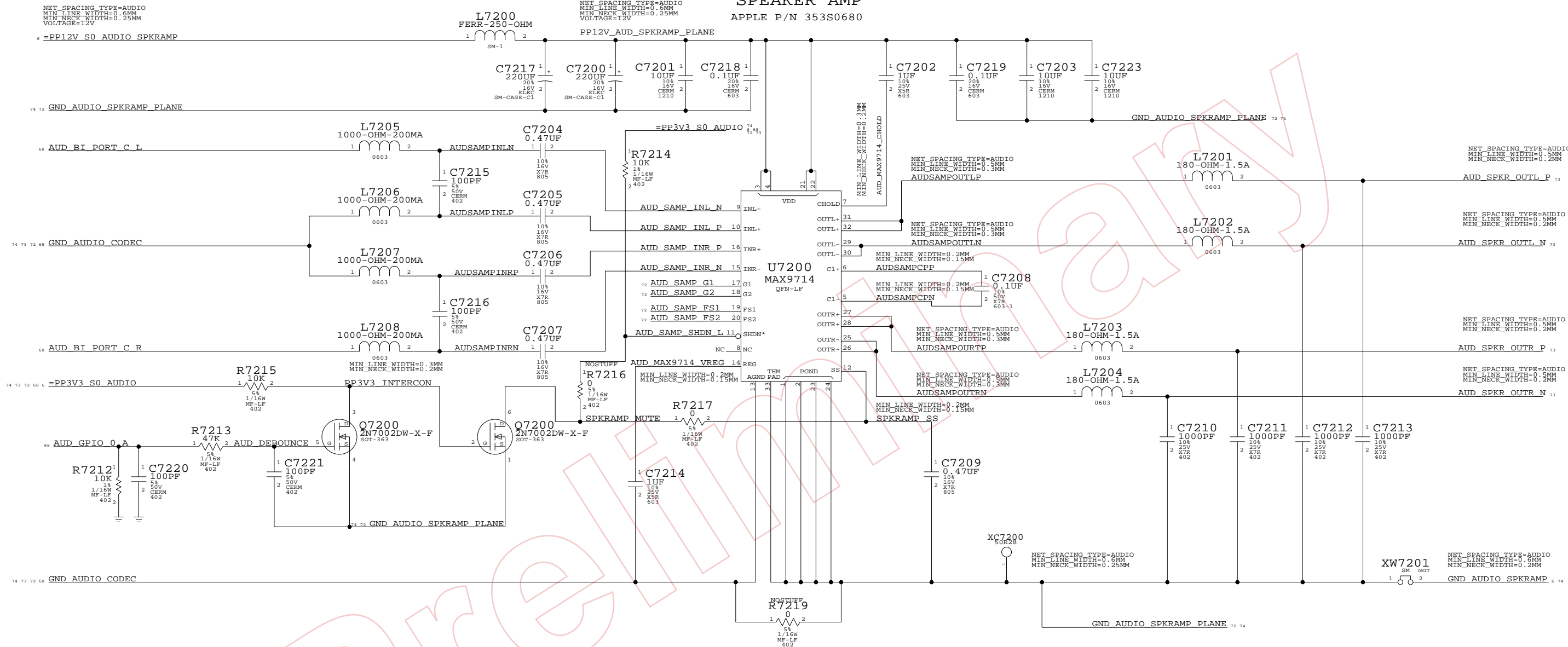
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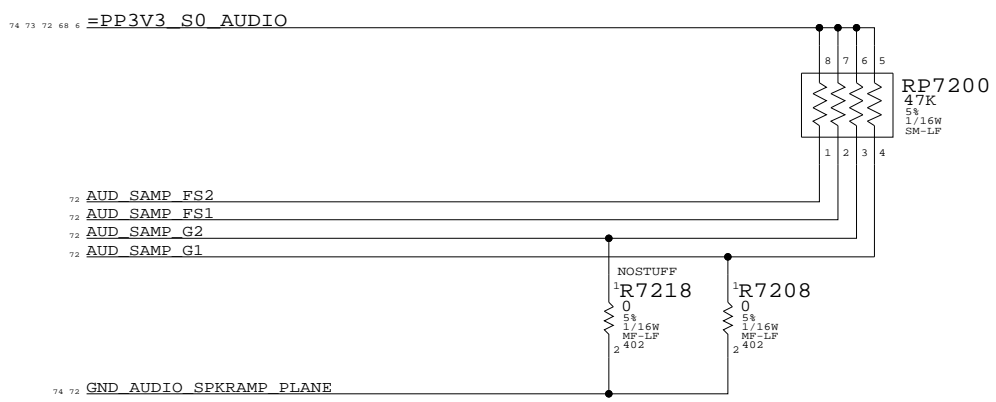
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 68 OF 97	

SPEAKER AMP
APPLE P/N 353S0680



GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

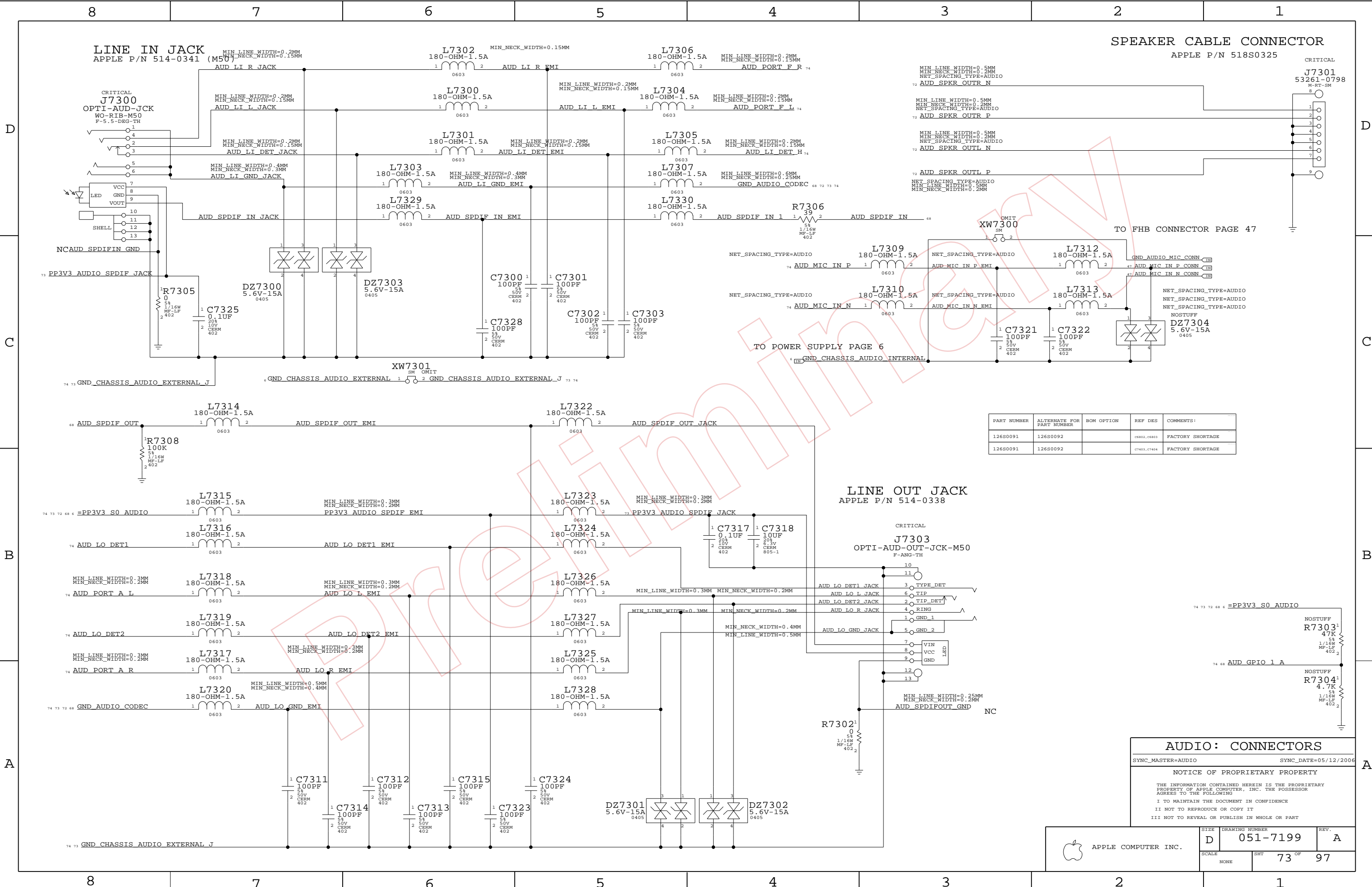


AUDIO: SPEAKER AMP
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	D	051-7199	A
SCALE	SHT		72 OF 97
NONE			

LINE IN JACK
APPLE P/N 514-0341 (M50)

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

LINE OUT JACK
APPLE P/N 514-0338

AUDIO: CONNECTORS
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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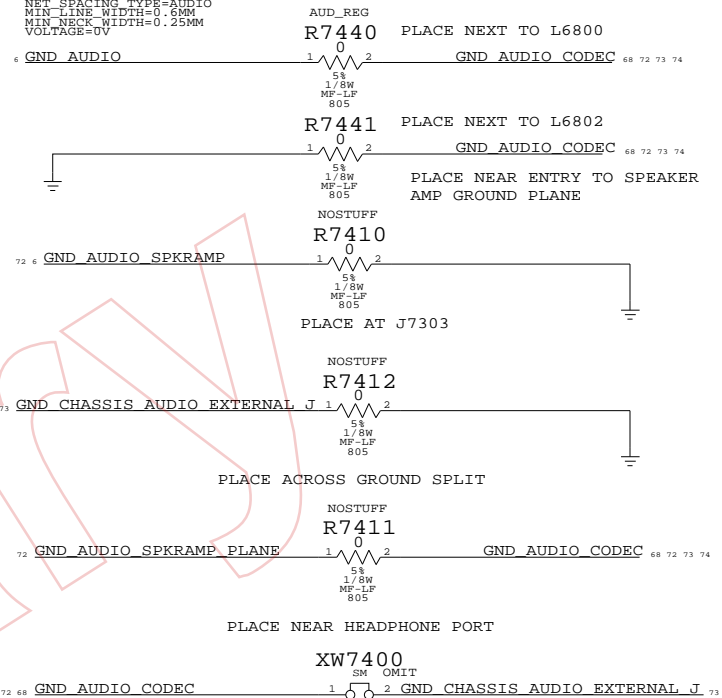
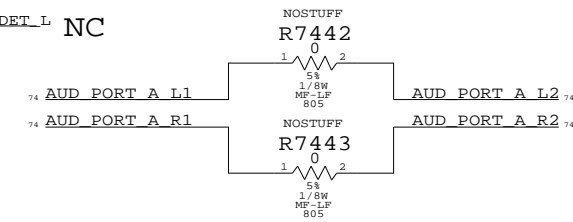
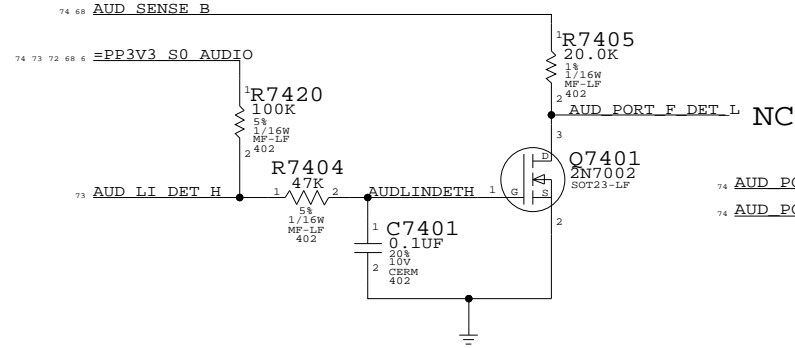
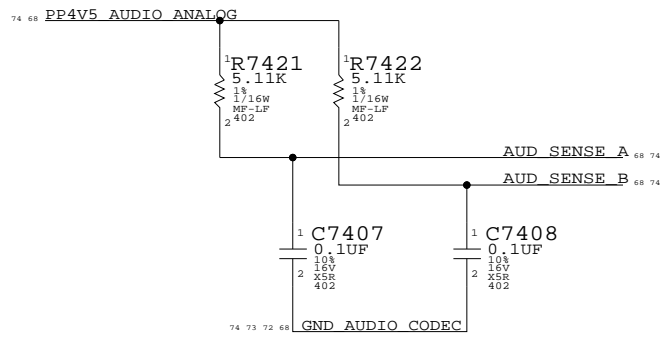
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	73 OF	97
NONE			

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

NET SPACING TYPE=AUDIO
MIN LINE WIDTH=0.6MM
MIN SPC WIDTH=0.25MM
VOLTAGE=0V

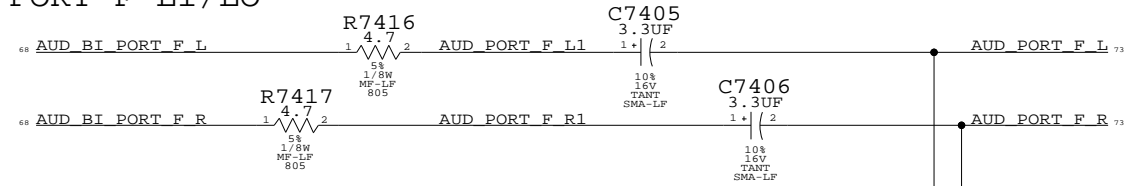
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



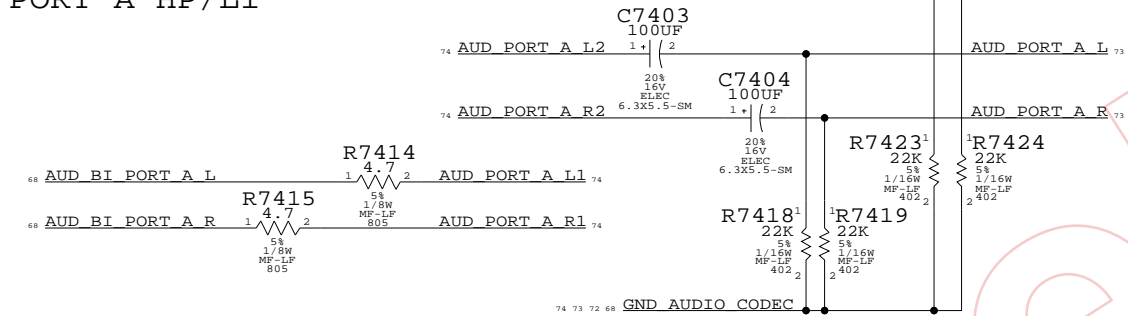
USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E
PORT D

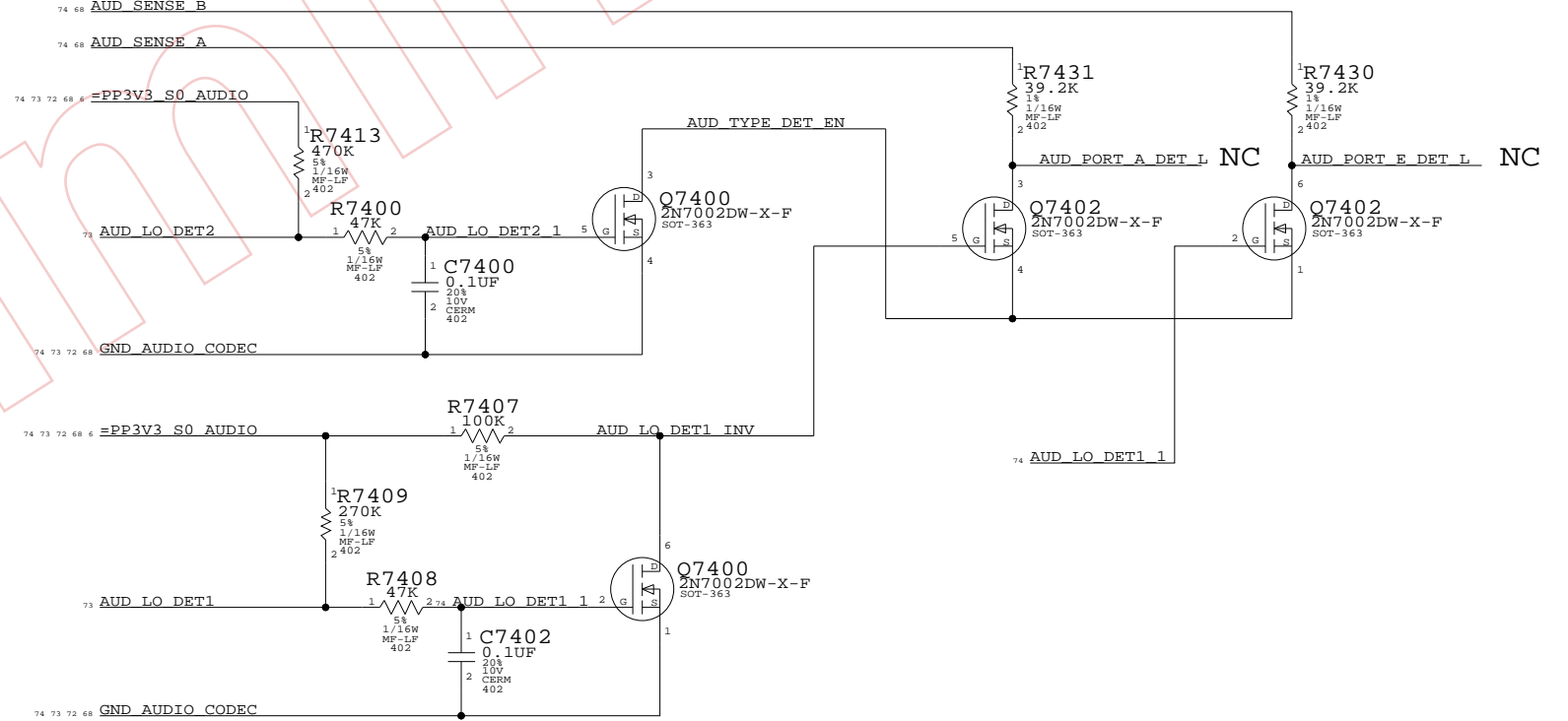
PORT F LI/LO



PORT A HP/LI

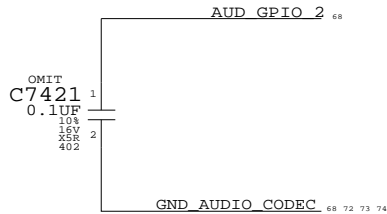


PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

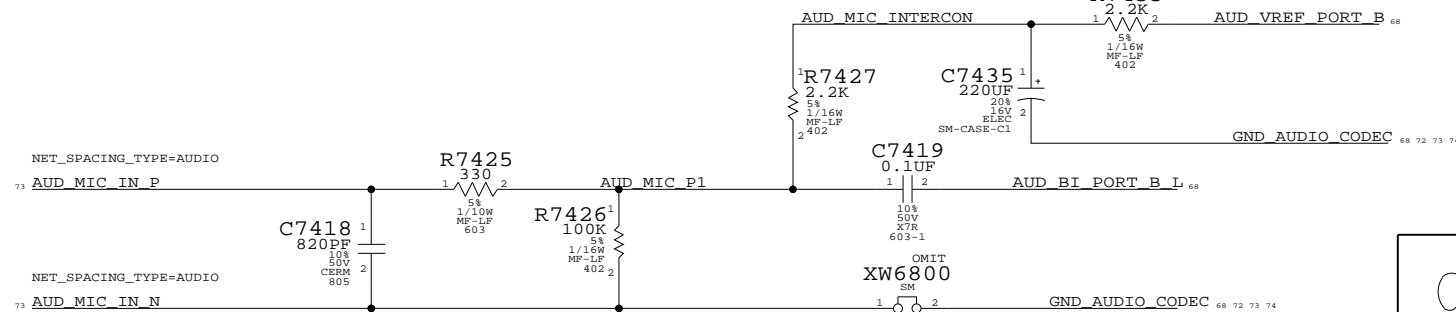


UNUSED PORT TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA



MICROPHONE IMPEDANCE MATCHING CIRCUIT



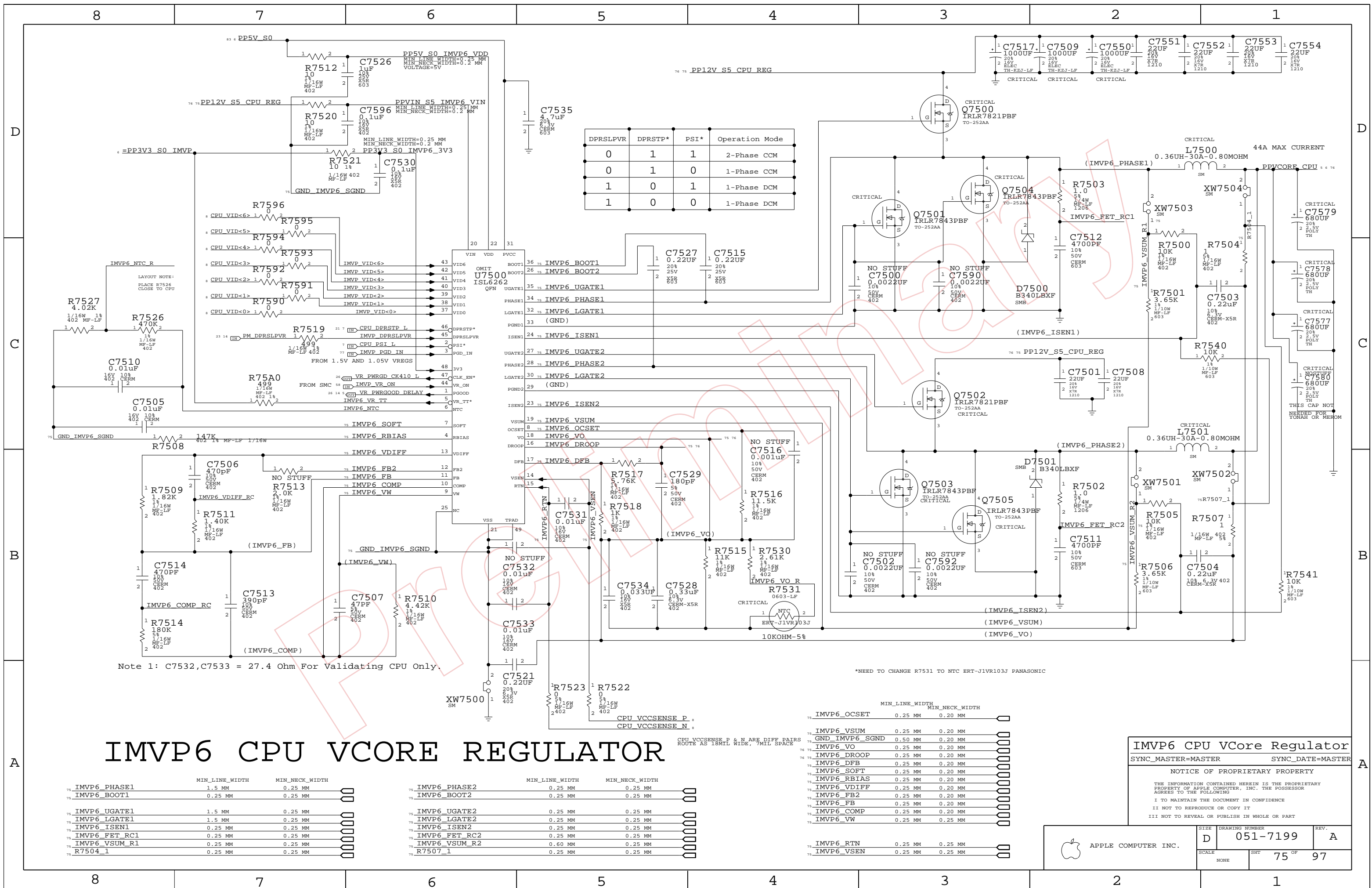
AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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	D	051-7199	A
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

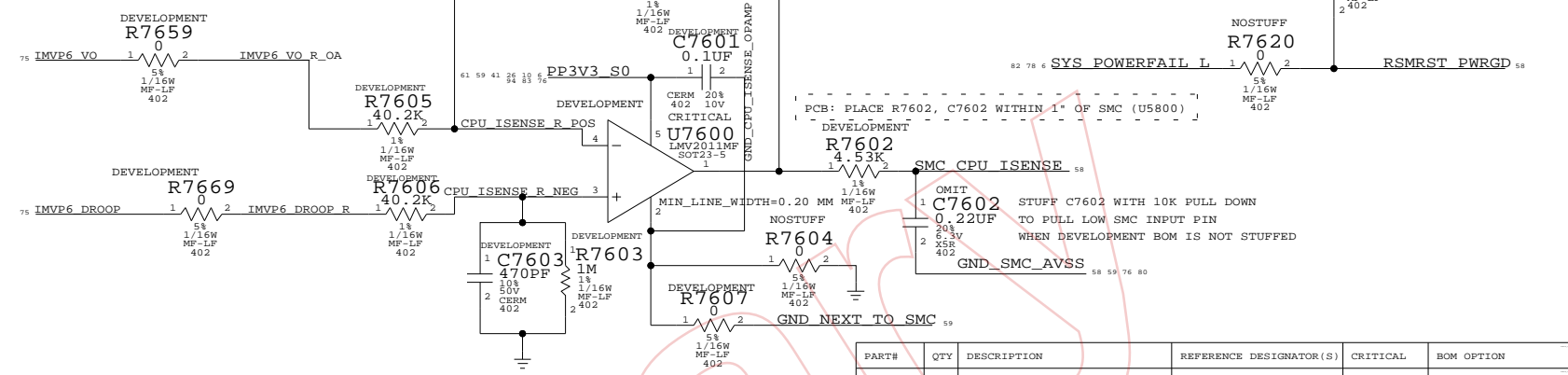
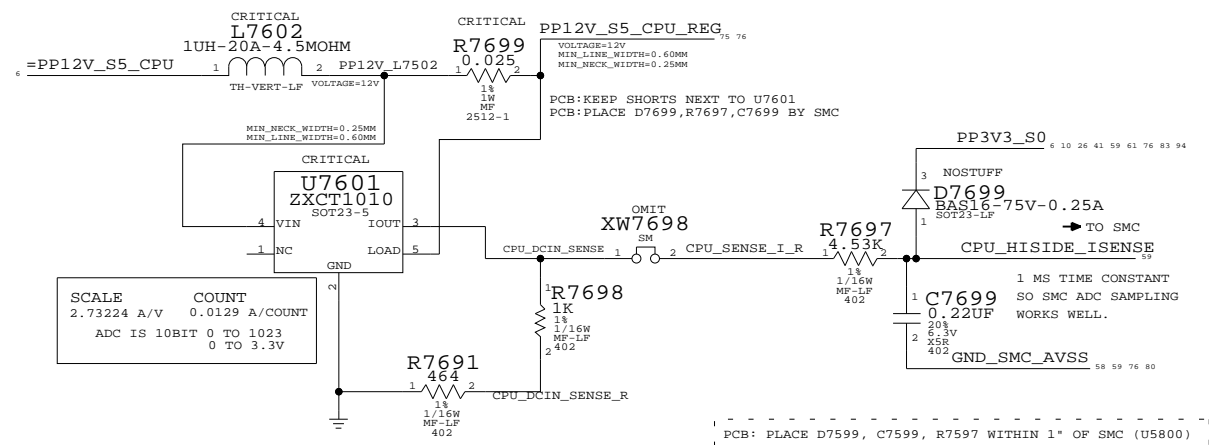
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7199	REV.: A
	SCALE: NONE	SHEET: 75 OF 97	

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

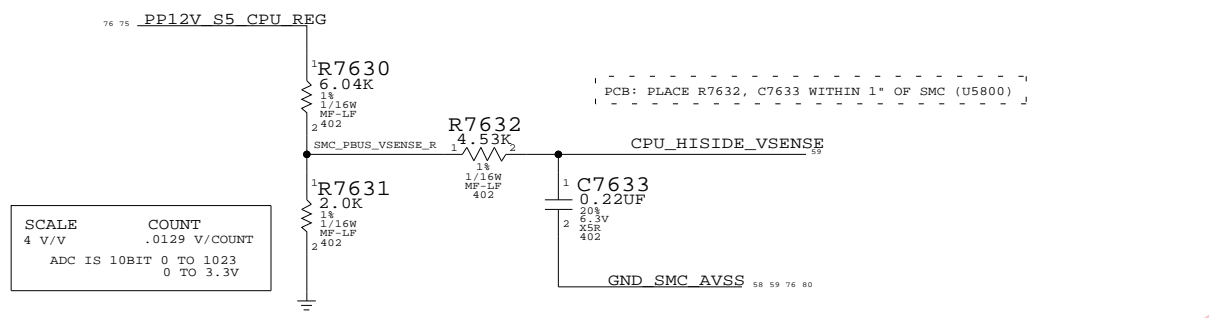
SMC PWRGD PULLUP

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

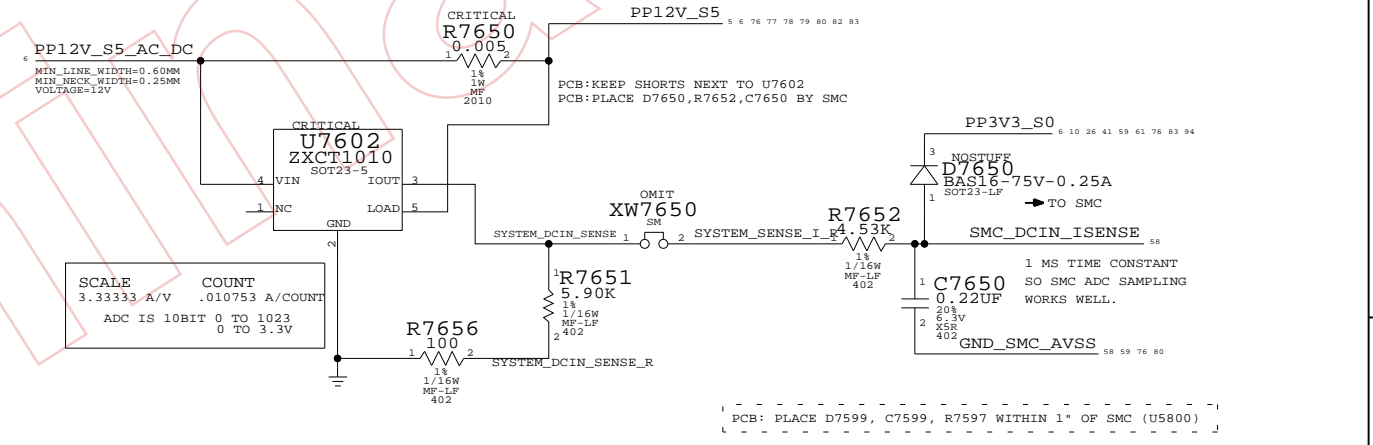


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP,0.22UF,6.3V,20%,0402	C7602		DEVELOPMENT
116S0090	1	RES,10K,5%,0402	C7602		NOT_DEVELOPMENT

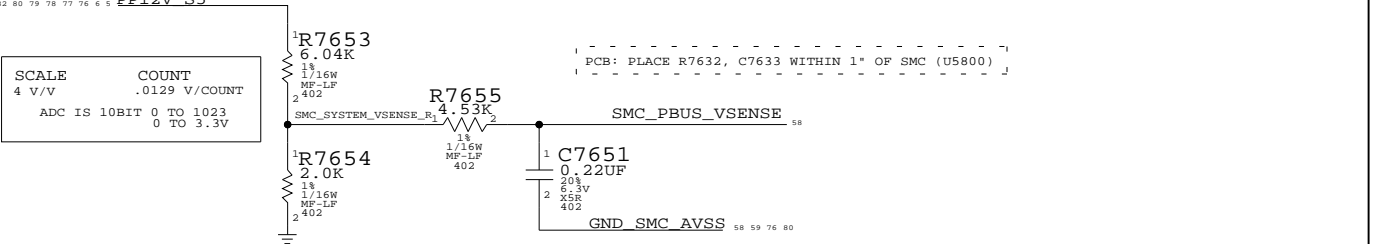
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



SYSTEM CURRENT SENSE

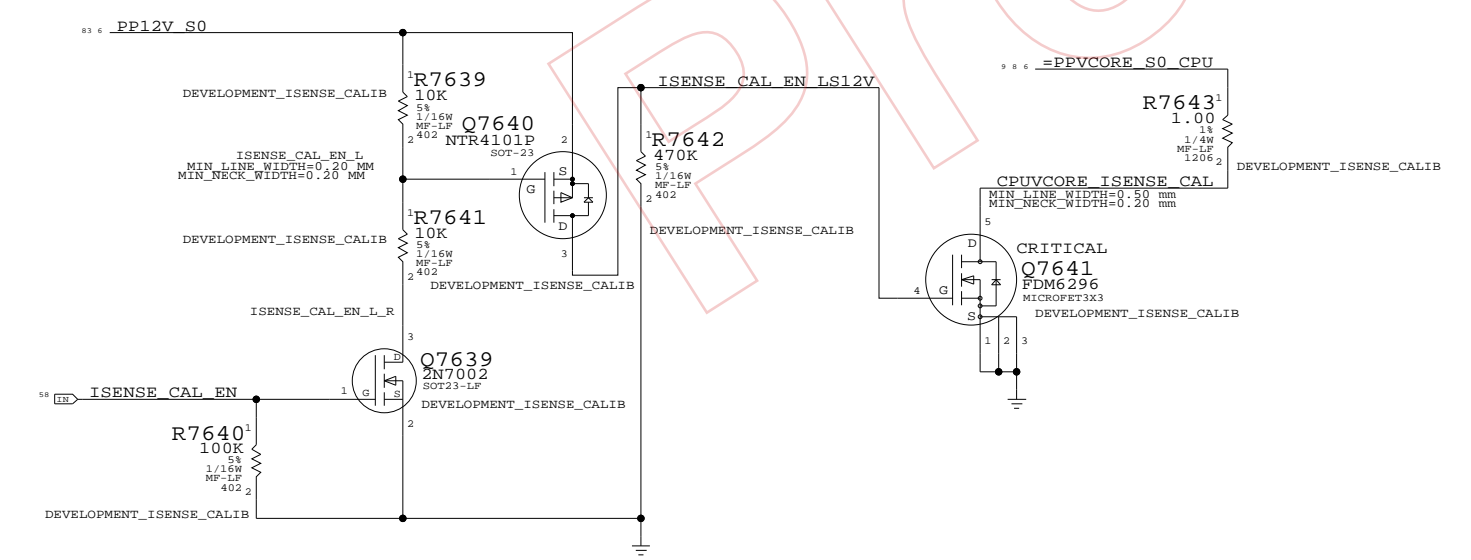


SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

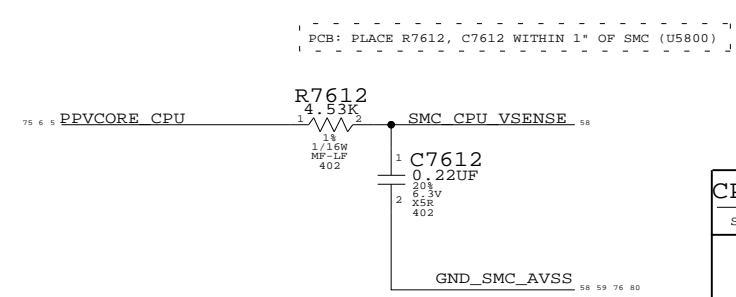


Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

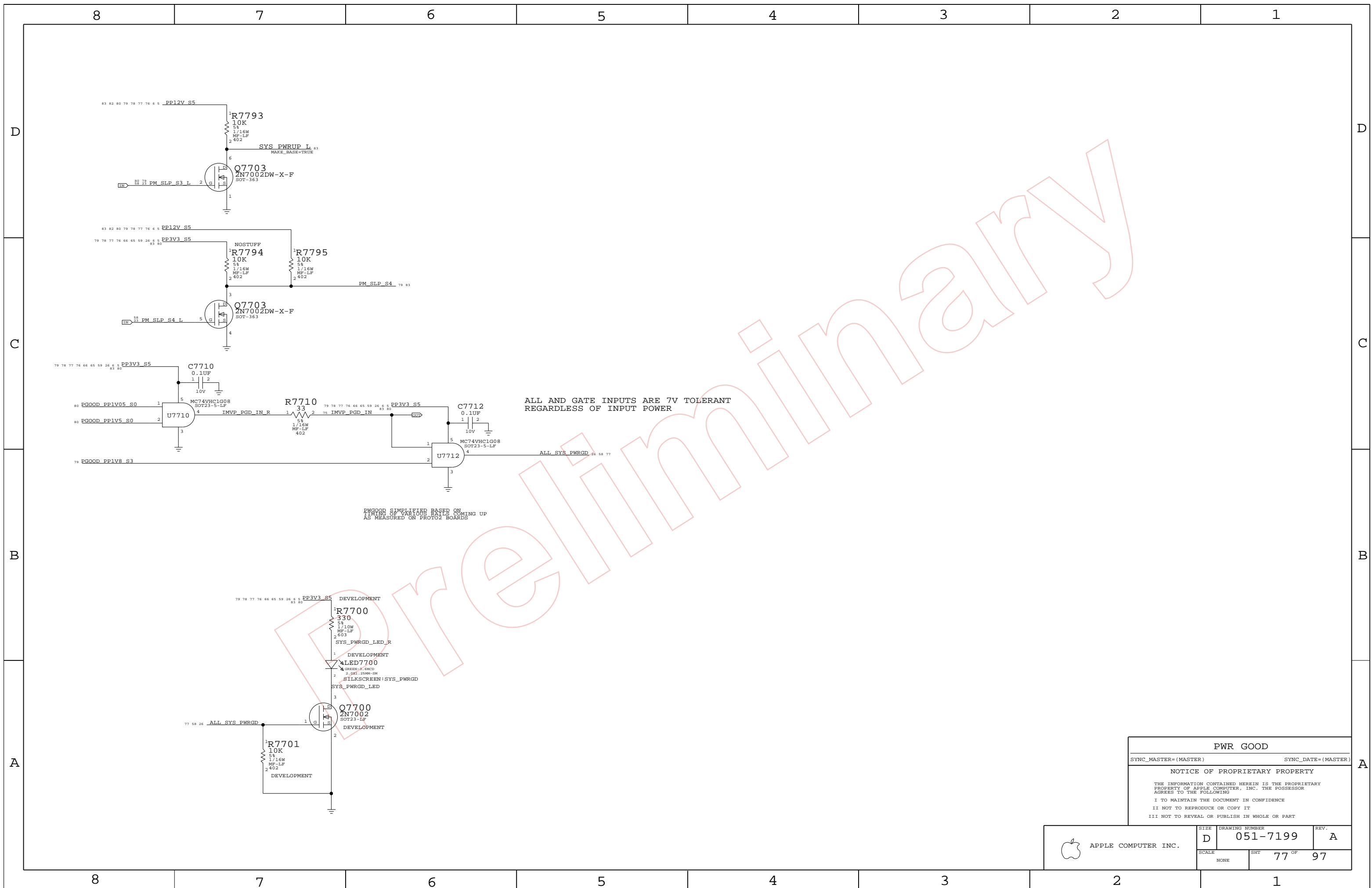
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ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWRGOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS


PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

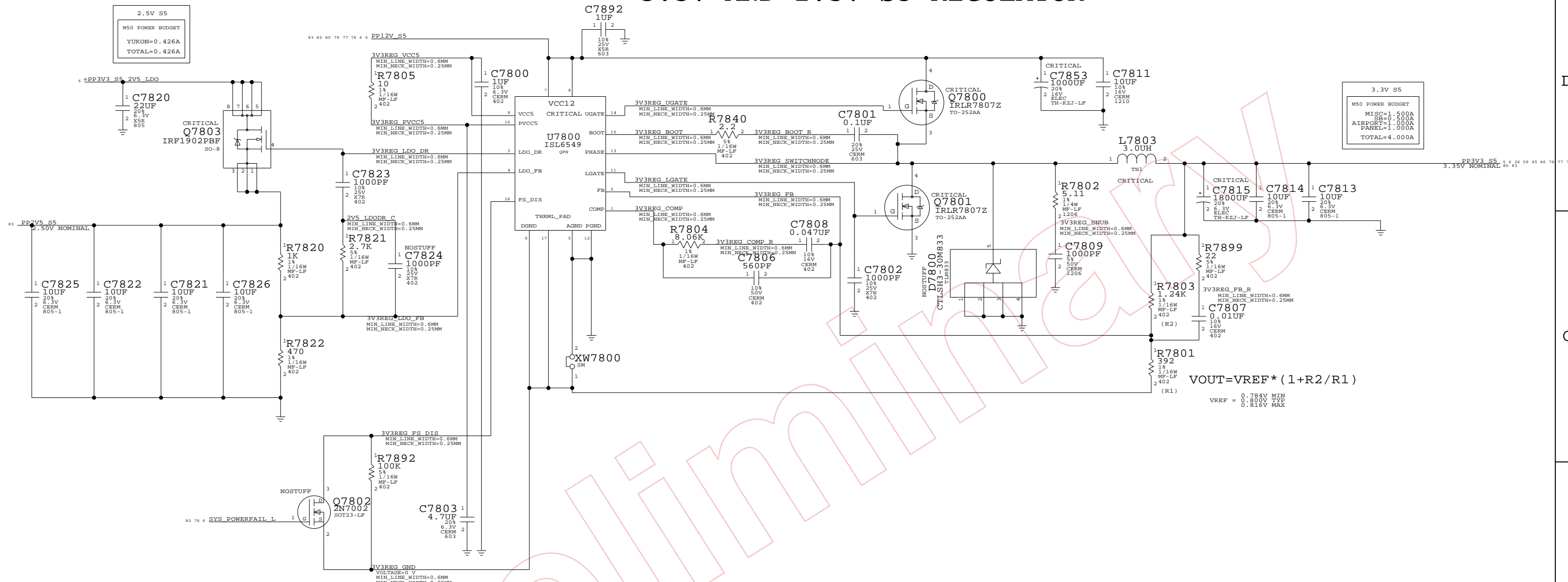
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	SCALE NONE	SHT 77 OF	97

3.3V AND 2.5V S5 REGULATOR



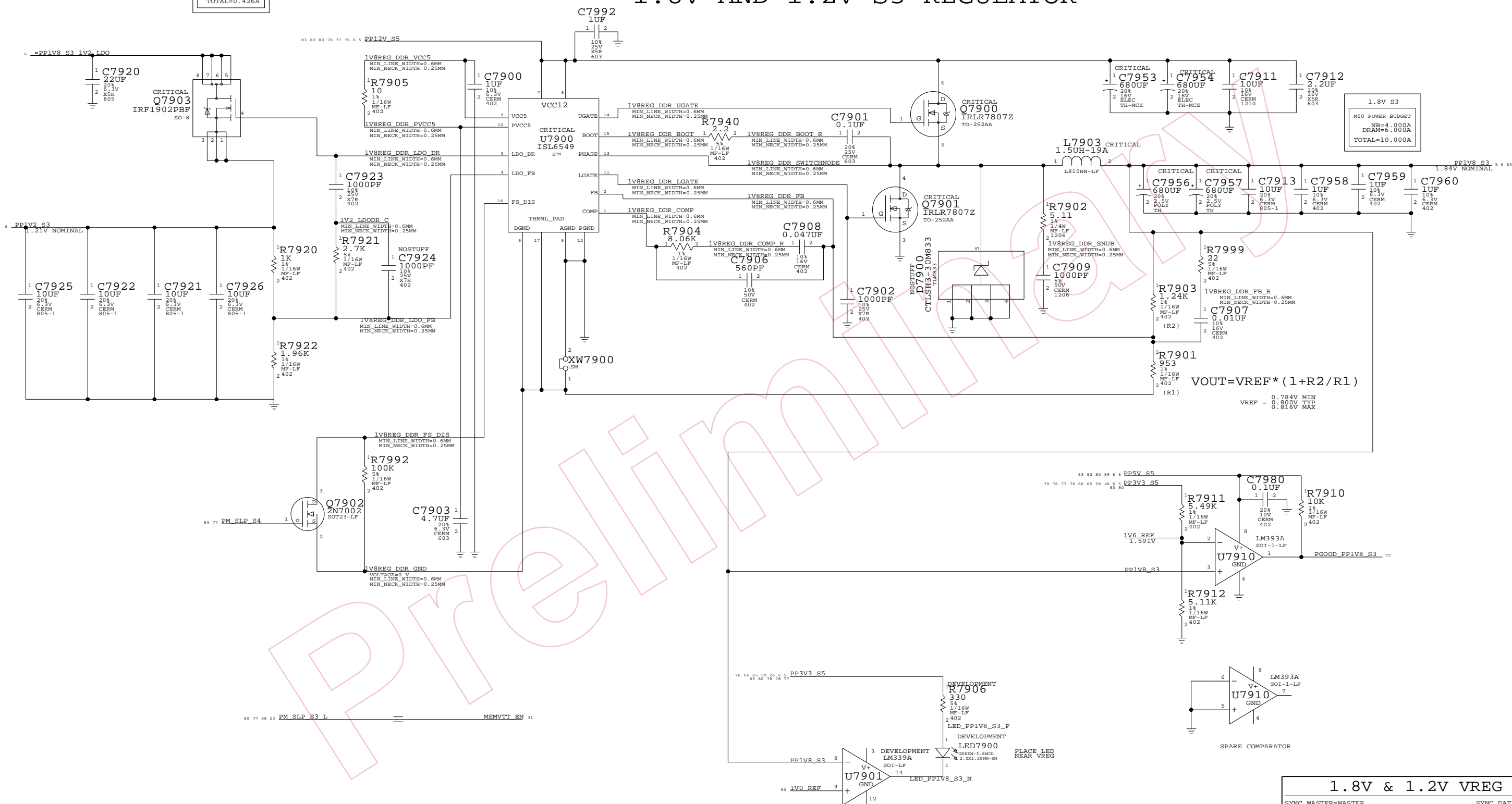
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	78 OF 97	
NONE			

TRUE 1

1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NE=4.000A
DRAM=6.000A
TOTAL=10.000A



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

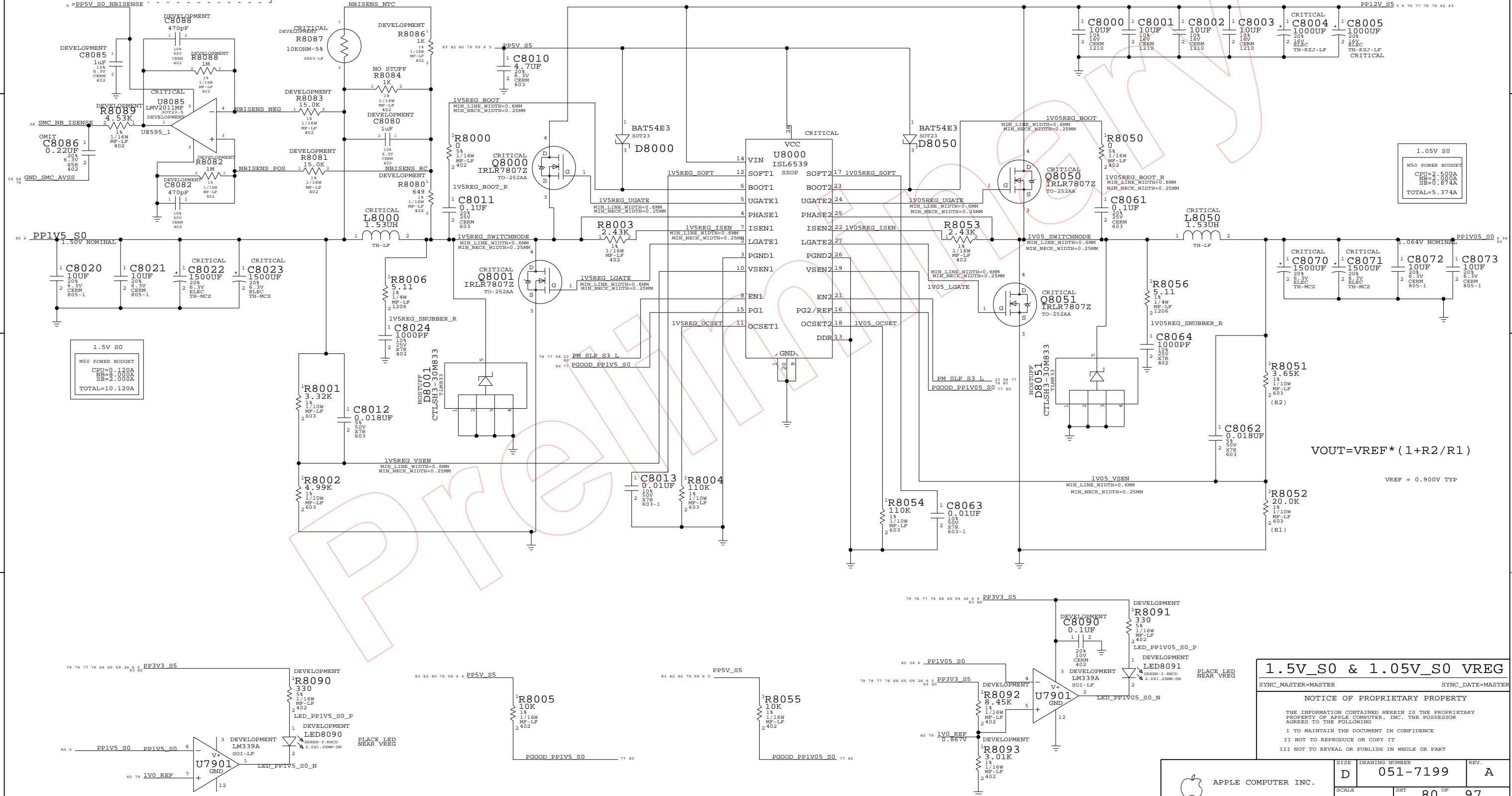
1.8V & 1.2V VREG
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7199	A
SCALE	SHT	79 OF	97
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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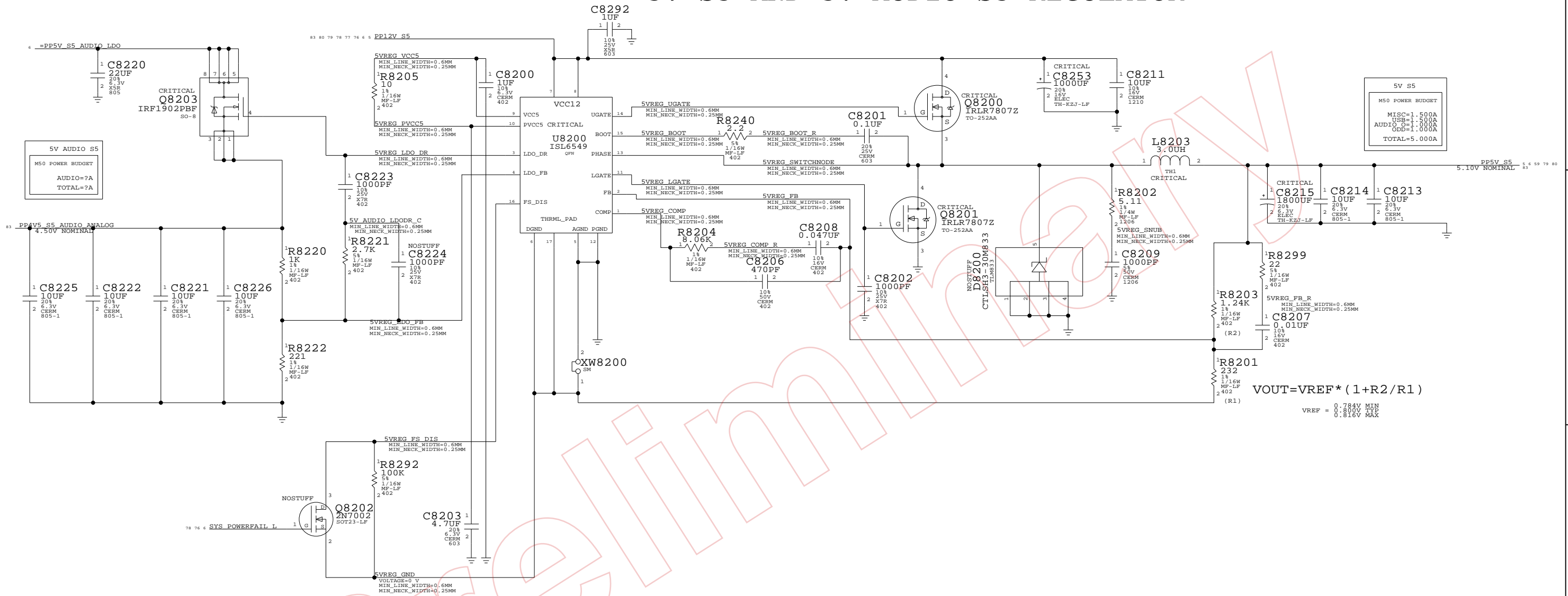
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



5V AUDIO S5
M50 POWER BUDGET
AUDIO=7A
TOTAL=7A

5V S5
M50 POWER BUDGET
MISC=1.500A
USB=1.500A
AUDIO_O=1.000A
ODD=1.000A
TOTAL=5.000A

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

POWER SUPPLY 3.3V/5V MAIN SWITCH

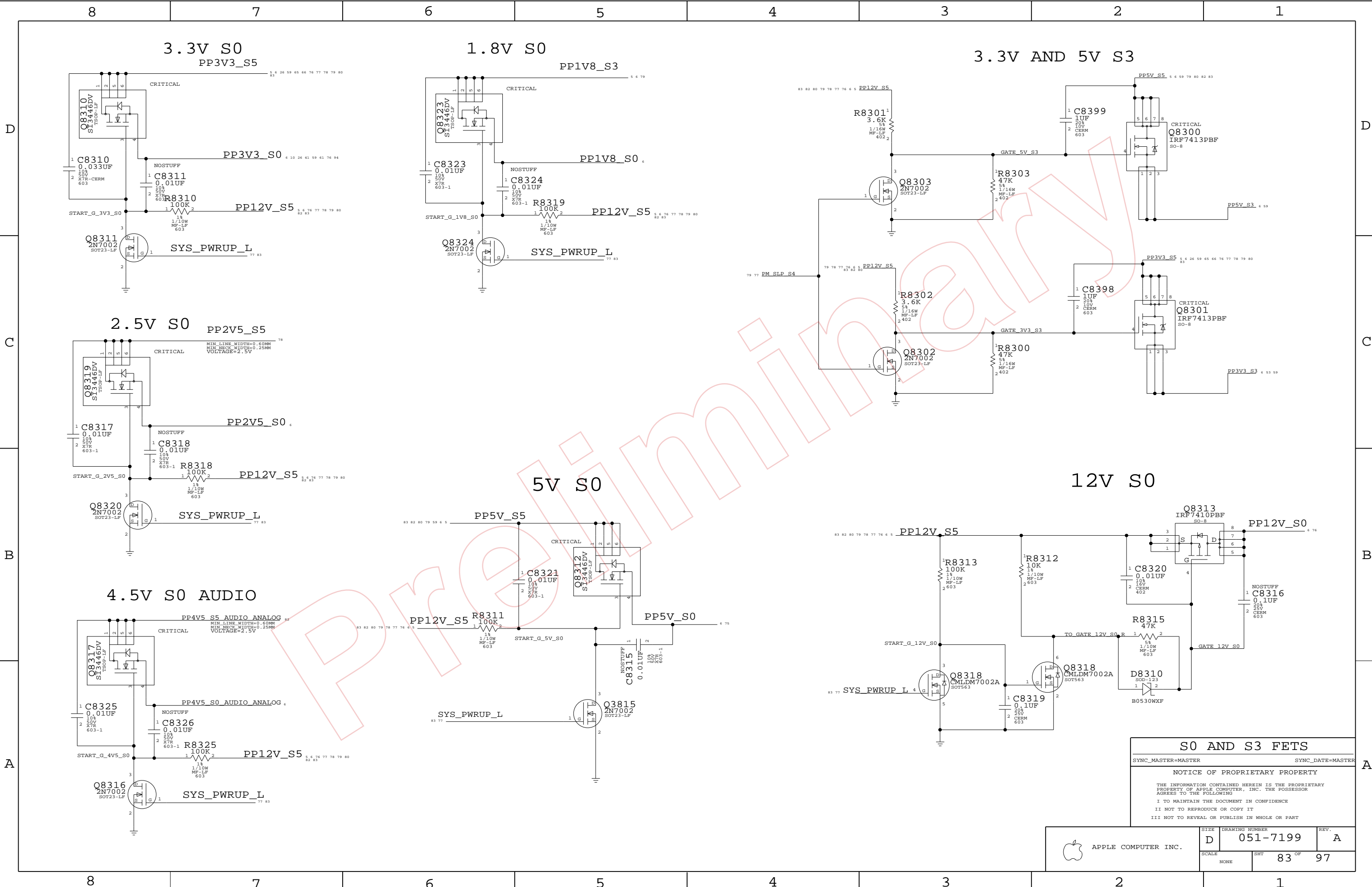
5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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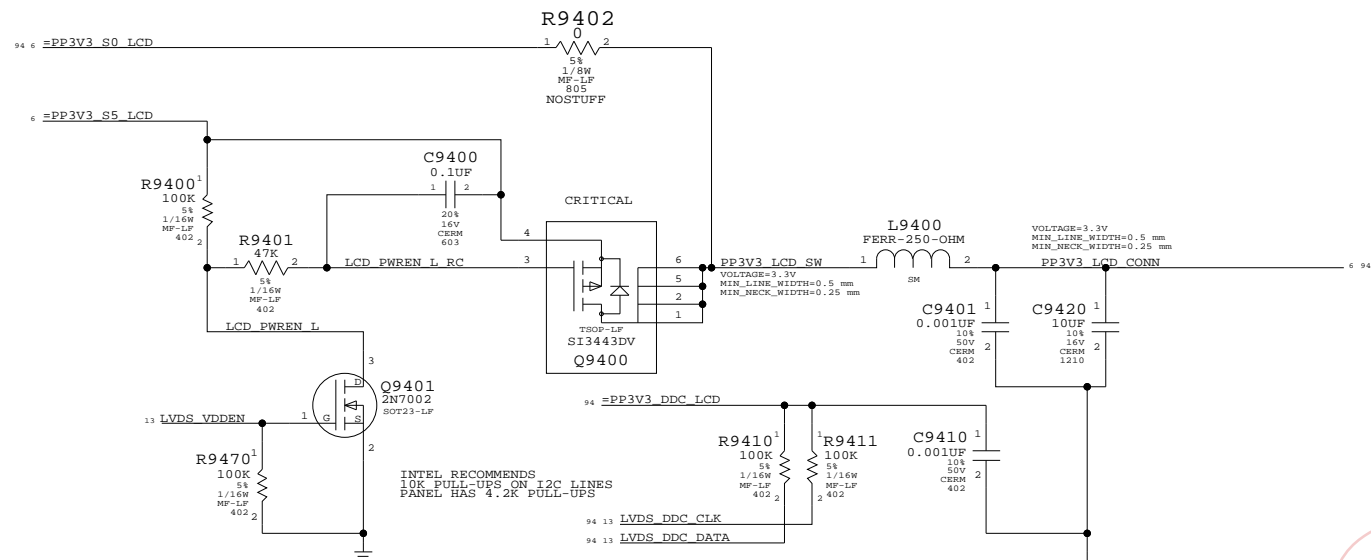
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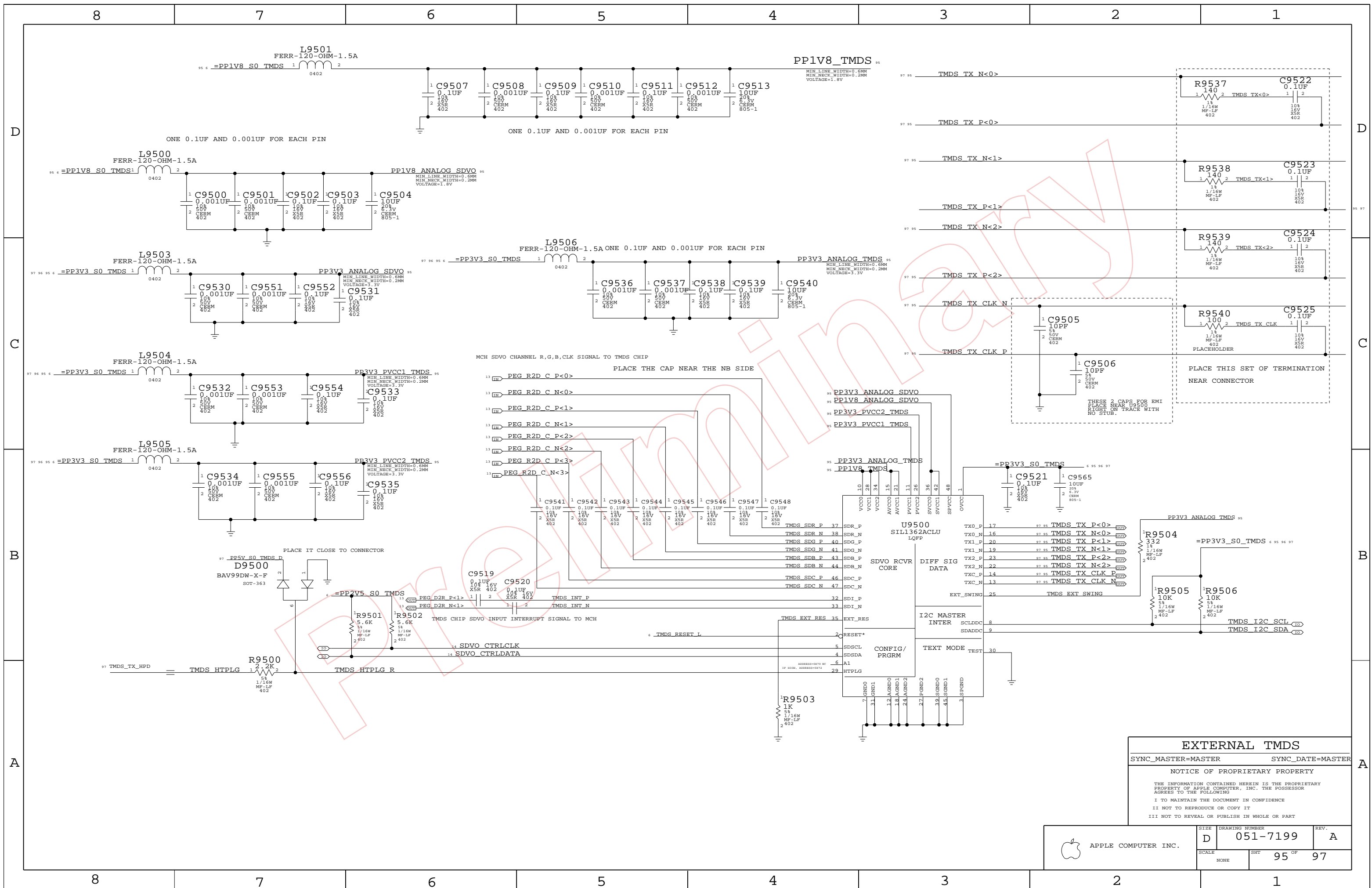
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 83 OF 97	

LCD (LVDS) INTERFACE

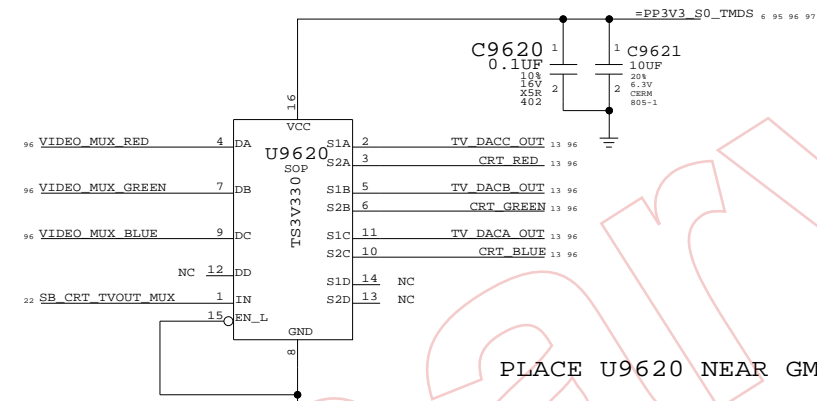
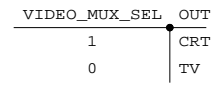
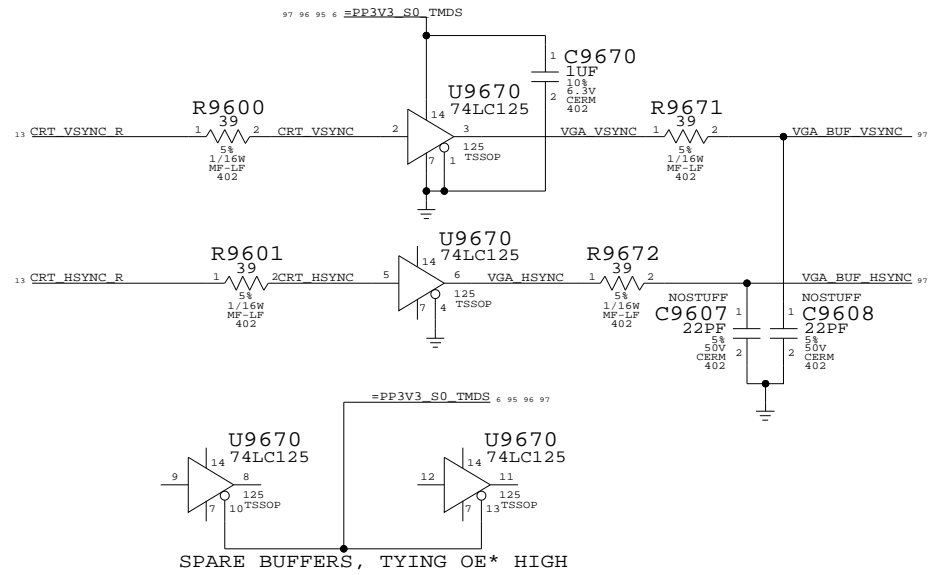
INVERTER INTERFACE



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	94 OF	97
NONE			

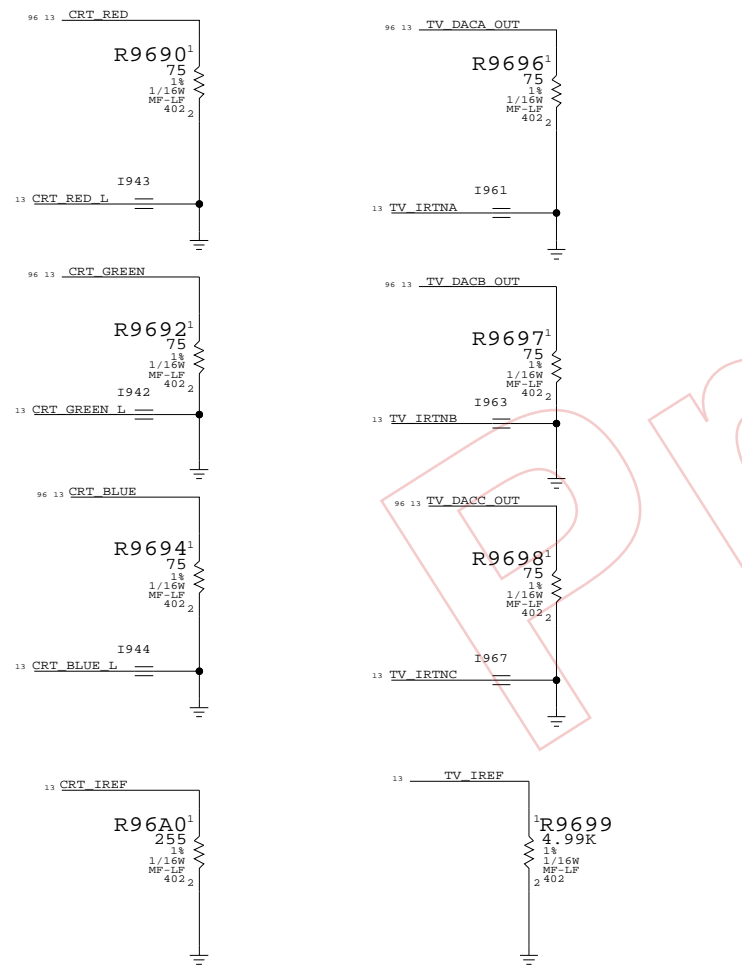


VGA SYNC BUFFERS

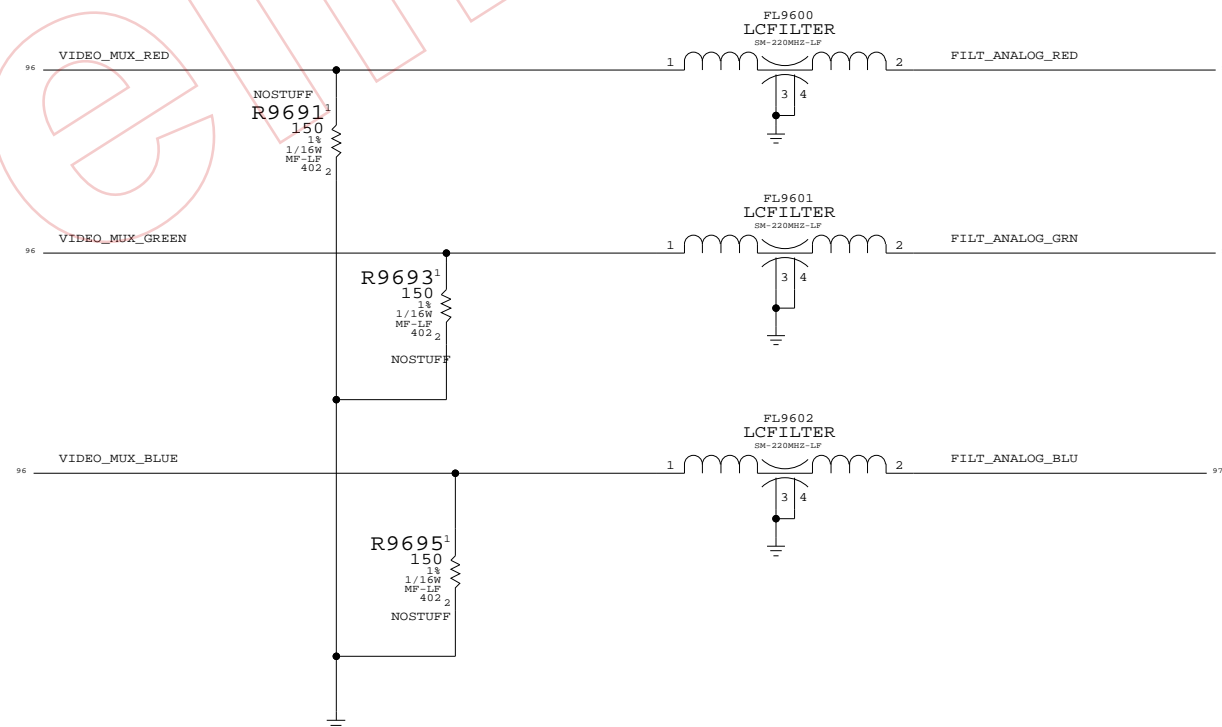


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE



ANALOG FILTERING PLACE BY CONNECTOR

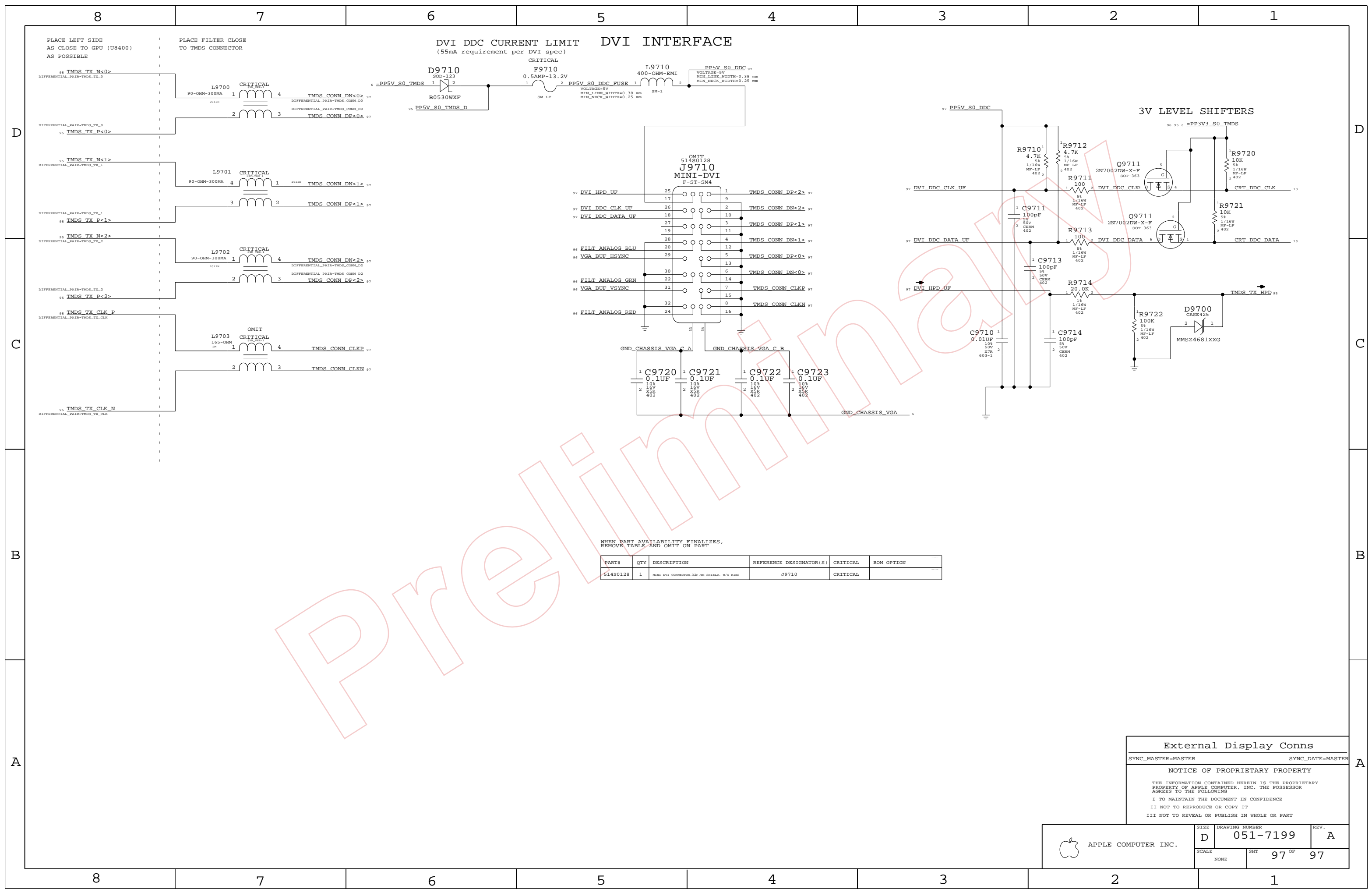


TMDS/Inverter/ExtVGA
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

DVI INTERFACE

514S0128
J9710
MINI-DVI
F-ST-SM4

3V LEVEL SHIFTERS

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 32P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	97 OF	97
NONE			