1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M60 - EVT

05/12/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
06		400374	ENGINEERING RELEASED	09/16/05	06/22/04

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

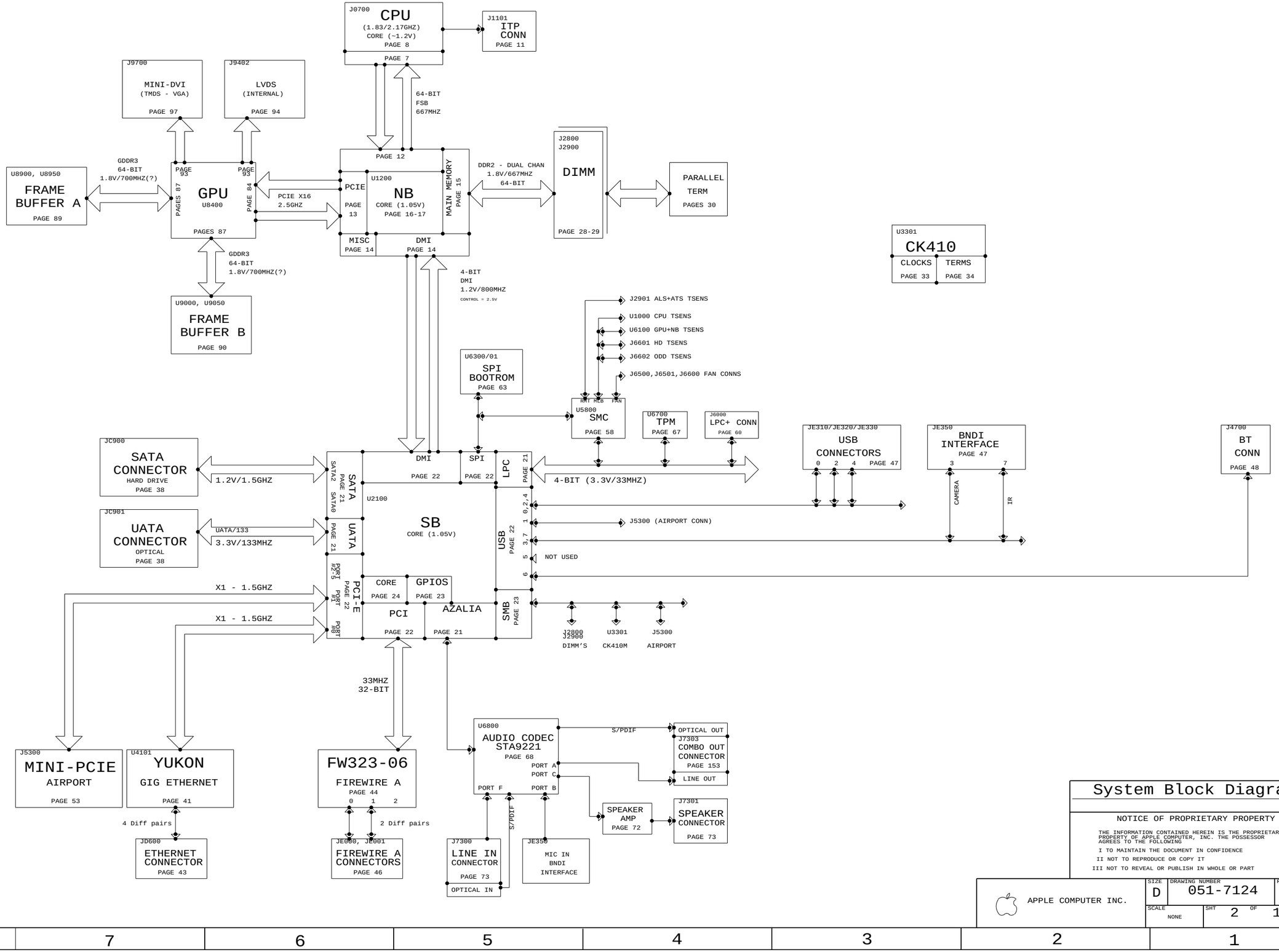
SIZE D

Apple Computer Inc.

TITLE: SCH,MLB,M60

DRAWING NUMBER 051-7124 REV. 13

SHT 1 OF 110

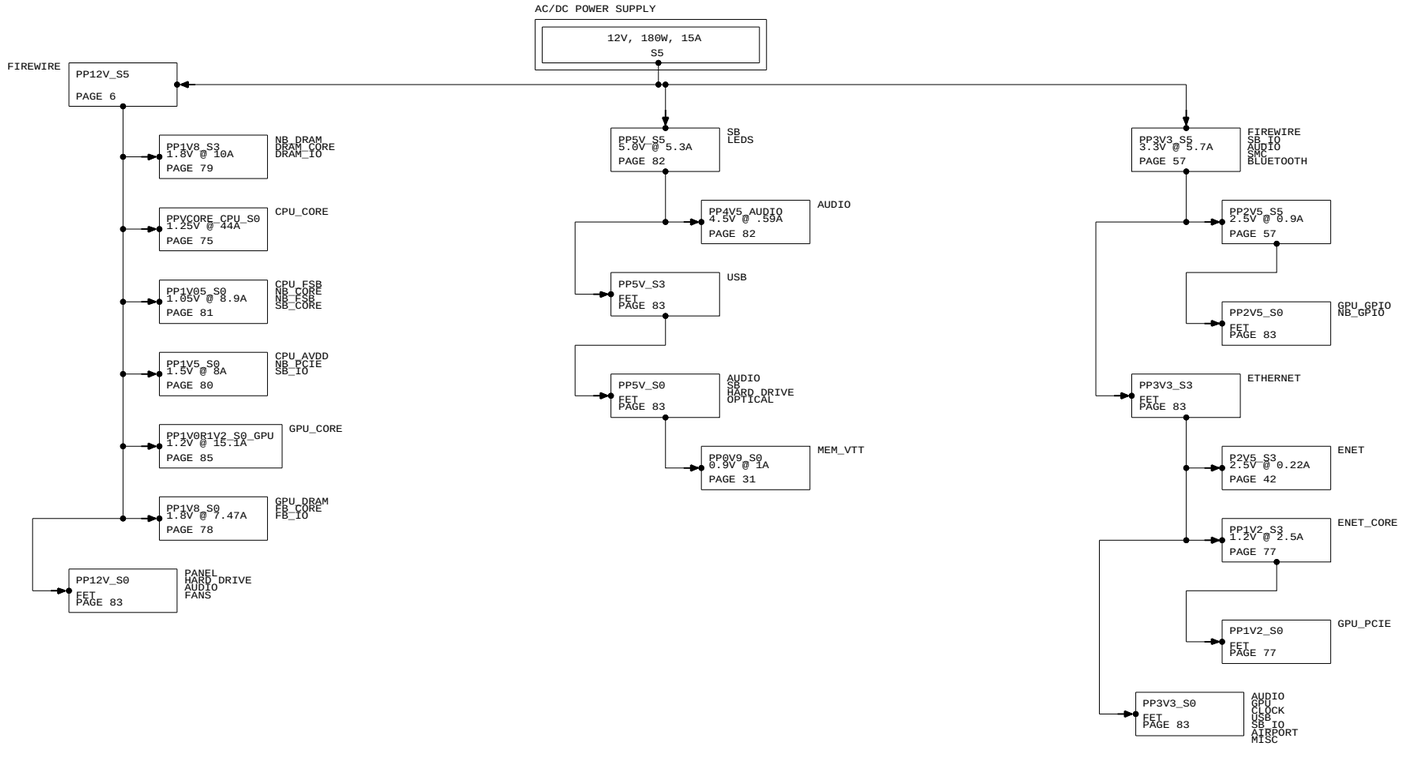


System Block Diagram

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 2 OF 110	



Power Block Diagram

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	3	110

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
	338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
	343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
	338S0345	1	IC,ATI,M56D,GRAFIXCTLR,880BGA,LF	U8400	CRITICAL	
	359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
	338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
	338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
	341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1235	353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	
	128S0078	2	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518	CRITICAL	
	825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		C940,C1900,C1901,C1968	SANYO W6CE330FS 330UF 6.3V LF
128S0080	128S0078		C7517,C7518	SANYO 16SVP330M 330UF 16V SMD LF
124-0338	124-0333			CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
353S1321	353S1105		U7910	LM339
338S0344	338S0345		U8400	M56 B26 P - DIFF P/N
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7124	1	PCB,SCHEM,MLB,M60	SCH1		20_INCH_LCD
	820-2031	1	PCB,FAB,MLB,M60	MLB1		20_INCH_LCD
(341S1904 - DEV) (341S1905 - PVT) (335S0384 - BLNK)	341T0036	1	EFI ROM,M60	U6301	CRITICAL	20_INCH_LCD
(341S1903 - PROG) (338S0274 - BLNK)	341T0035	1	IC,SMC,M60	U5800	CRITICAL	20_INCH_LCD
	338S0315	1	IC,ATI,M56LP,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
	114S0264	1	3.01K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P2V
	337S3293	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU
	337S3292	1	2.33GHZ MEROM	CPU	CRITICAL	2P33_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

Table Items

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7124 | REV. 13

SCALE NONE | SHT 4 OF 110

LAYOUT NOTE: PLACE NEAR J0700

12 7 5	FSB_A_L<6>	PP600	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP601	OMIT P4MM
12 7 5	FSB_A_L<27>	PP602	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP603	OMIT P4MM
12 7 5	FSB_D_L<0>	PP604	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP605	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP606	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP607	OMIT P4MM
12 7 5	FSB_D_L<16>	PP608	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP609	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP610	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP611	OMIT P4MM
12 7 5	FSB_D_L<41>	PP612	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP613	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP614	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP615	OMIT P4MM
12 7 5	FSB_D_L<59>	PP616	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP617	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP618	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP619	OMIT P4MM
12 7 5	FSB_LOCK_L	PP620	OMIT P4MM
12 11 7	FSB_CPURST_L	PP621	OMIT P4MM
21 7	CPU_INIT_L	PP622	OMIT P4MM
21 7	CPU_A20M_L	PP623	OMIT P4MM
21 7	CPU_IGNNE_L	PP624	OMIT P4MM
21 7	CPU_STPCLK_L	PP625	OMIT P4MM
21 7	CPU_INTR	PP626	OMIT P4MM
21 7	CPU_NMI	PP627	OMIT P4MM
21 7	CPU_SMI_L	PP628	OMIT P4MM
34 7	FSB_CLK_CPU_P	PP629	OMIT P4MM
34 7	FSB_CLK_CPU_N	PP630	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

34 21	SB_CLK100M_SATA_P	PP6C4	OMIT P4MM
34 21	SB_CLK100M_SATA_N	PP6C5	OMIT P4MM
38 21	IDE_PDIOR_L	PP6C6	OMIT P4MM
38 21	IDE_PDIORDY	PP6C7	OMIT P4MM
38 21	IDE_PDD<9>	PP6C8	OMIT P4MM
34 22	PCI_CLK_SB	PP6D0	OMIT P4MM
41 22	PCIE_A_D2R_P	PP6D1	OMIT P4MM
41 22	PCIE_A_D2R_N	PP6D2	OMIT P4MM
53 22	PCIE_B_D2R_P	PP5E1	OMIT P4MM
53 22	PCIE_B_D2R_N	PP5E2	OMIT P4MM
22 14	DMI_N2S_P<0>	PP6D3	OMIT P4MM
22 14	DMI_N2S_N<0>	PP6D4	OMIT P4MM
34 22	SB_CLK100M_DMI_P	PP6D5	OMIT P4MM
34 22	SB_CLK100M_DMI_N	PP6D6	OMIT P4MM
58 26 23	PM_SYSRST_L	PP6D7	OMIT P4MM
58 44 23 67 60	PM_CLKRUN_L	PP6D8	OMIT P4MM
34 23	SB_CLK14P3M_TIMER	PP6D9	OMIT P4MM
34 23	SB_CLK48M_USBCTLR	PP6E0	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1200

12 7 5	FSB_A_L<6>	PP631	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP632	OMIT P4MM
12 7 5	FSB_A_L<27>	PP633	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP634	OMIT P4MM
12 7 5	FSB_D_L<0>	PP635	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP636	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP637	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP638	OMIT P4MM
12 7 5	FSB_D_L<16>	PP639	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP640	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP641	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP642	OMIT P4MM
12 7 5	FSB_D_L<41>	PP643	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP644	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP645	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP646	OMIT P4MM
12 7 5	FSB_D_L<59>	PP647	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP648	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP649	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP650	OMIT P4MM
12 7 5	FSB_LOCK_L	PP651	OMIT P4MM
12 7	FSB_HIT_L	PP652	OMIT P4MM
12 7	FSB_HITM_L	PP653	OMIT P4MM
12 7	FSB_BNR_L	PP654	OMIT P4MM
12 7	FSB_BREQ0_L	PP655	OMIT P4MM
12 7	FSB_DBSY_L	PP656	OMIT P4MM
12 7	FSB_DPWR_L	PP657	OMIT P4MM
12 7	FSB_REQ_L<0>	PP658	OMIT P4MM
12 7	FSB_REQ_L<1>	PP659	OMIT P4MM
12 7	FSB_REQ_L<2>	PP660	OMIT P4MM
12 7	FSB_REQ_L<3>	PP661	OMIT P4MM
12 7	FSB_REQ_L<4>	PP662	OMIT P4MM
34 12	FSB_CLK_NB_P	PP663	OMIT P4MM
34 12	FSB_CLK_NB_N	PP664	OMIT P4MM
75 26 14	VR_PWRGOOD_DELAY	PP665	OMIT P4MM
14	NB_RST_IN_L_R	PP666	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_P	PP667	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_N	PP668	OMIT P4MM
22 14	DMI_S2N_N<0>	PP673	OMIT P4MM
22 14	DMI_S2N_P<0>	PP674	OMIT P4MM
19 14	MEM_VREF_NB_0	PP6E1	OMIT P4MM
19 14	MEM_VREF_NB_1	PP675	OMIT P4MM
28 15	MEM_A_DQ<7>	PP676	OMIT P4MM
28 15	MEM_A_DQ<14>	PP677	OMIT P4MM
28 15	MEM_A_DQ<16>	PP678	OMIT P4MM
28 15	MEM_A_DQ<25>	PP679	OMIT P4MM
28 15	MEM_A_DQ<39>	PP680	OMIT P4MM
28 15	MEM_A_DQ<47>	PP681	OMIT P4MM
28 15	MEM_A_DQ<54>	PP682	OMIT P4MM
28 15	MEM_A_DQ<59>	PP683	OMIT P4MM
29 15	MEM_A_DQS_P<0>	PP684	OMIT P4MM
29 15	MEM_A_DQS_N<0>	PP685	OMIT P4MM
28 15	MEM_A_DQS_P<1>	PP686	OMIT P4MM
28 15	MEM_A_DQS_N<1>	PP687	OMIT P4MM
28 15	MEM_A_DQS_P<2>	PP688	OMIT P4MM
28 15	MEM_A_DQS_N<2>	PP689	OMIT P4MM
28 15	MEM_A_DQS_P<3>	PP690	OMIT P4MM
28 15	MEM_A_DQS_N<3>	PP691	OMIT P4MM
28 15	MEM_A_DQS_P<4>	PP692	OMIT P4MM
28 15	MEM_A_DQS_N<4>	PP693	OMIT P4MM
28 15	MEM_A_DQS_P<5>	PP694	OMIT P4MM
28 15	MEM_A_DQS_N<5>	PP695	OMIT P4MM
28 15	MEM_A_DQS_P<6>	PP696	OMIT P4MM
28 15	MEM_A_DQS_N<6>	PP697	OMIT P4MM
28 15	MEM_A_DQS_P<7>	PP698	OMIT P4MM
28 15	MEM_A_DQS_N<7>	PP699	OMIT P4MM
29 15	MEM_B_DQ<6>	PP6A0	OMIT P4MM
29 15	MEM_B_DQ<8>	PP6A1	OMIT P4MM
29 15	MEM_B_DQ<23>	PP6A2	OMIT P4MM
29 15	MEM_B_DQ<25>	PP6A3	OMIT P4MM
29 15	MEM_B_DQ<38>	PP6A4	OMIT P4MM
29 15	MEM_B_DQ<44>	PP6A5	OMIT P4MM
29 15	MEM_B_DQ<48>	PP6A6	OMIT P4MM
29 15	MEM_B_DQ<62>	PP6A7	OMIT P4MM
29 15	MEM_B_DQS_P<0>	PP6A8	OMIT P4MM
29 15	MEM_B_DQS_N<0>	PP6A9	OMIT P4MM
29 15	MEM_B_DQS_P<1>	PP6B0	OMIT P4MM
29 15	MEM_B_DQS_N<1>	PP6B1	OMIT P4MM
29 15	MEM_B_DQS_P<2>	PP6B2	OMIT P4MM
29 15	MEM_B_DQS_N<2>	PP6B3	OMIT P4MM
29 15	MEM_B_DQS_P<3>	PP6B4	OMIT P4MM
29 15	MEM_B_DQS_N<3>	PP6B5	OMIT P4MM
29 15	MEM_B_DQS_P<4>	PP6B6	OMIT P4MM
29 15	MEM_B_DQS_N<4>	PP6B7	OMIT P4MM
29 15	MEM_B_DQS_P<5>	PP6B8	OMIT P4MM
29 15	MEM_B_DQS_N<5>	PP6B9	OMIT P4MM
29 15	MEM_B_DQS_P<6>	PP6C0	OMIT P4MM
29 15	MEM_B_DQS_N<6>	PP6C1	OMIT P4MM
29 15	MEM_B_DQS_P<7>	PP6C2	OMIT P4MM
29 15	MEM_B_DQS_N<7>	PP6C3	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U8400

89 87 5	FB_A_DQ<0>	PP8700	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8701	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8702	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8703	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8704	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8705	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8706	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8707	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8708	OMIT P4MM
89 87	FB_A_RDQS<0>	PP8709	OMIT P4MM
89 87	FB_A_RDQS<1>	PP8710	OMIT P4MM
89 87	FB_A_RDQS<2>	PP8711	OMIT P4MM
89 87	FB_A_RDQS<3>	PP8712	OMIT P4MM
89 87	FB_A_RDQS<4>	PP8713	OMIT P4MM
89 87	FB_A_RDQS<5>	PP8714	OMIT P4MM
89 87	FB_A_RDQS<6>	PP8715	OMIT P4MM
89 87	FB_A_RDQS<7>	PP8716	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP8720	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP8721	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP8722	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP8723	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP8724	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP8725	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP8726	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP8727	OMIT P4MM
90 87 5	FB_B_MA<3>	PP8728	OMIT P4MM
90 87	FB_B_RDQS<0>	PP8729	OMIT P4MM
90 87	FB_B_RDQS<1>	PP8730	OMIT P4MM
90 87	FB_B_RDQS<2>	PP8731	OMIT P4MM
90 87	FB_B_RDQS<3>	PP8732	OMIT P4MM
90 87	FB_B_RDQS<4>	PP8733	OMIT P4MM
90 87	FB_B_RDQS<5>	PP8734	OMIT P4MM
90 87	FB_B_RDQS<6>	PP8735	OMIT P4MM
90 87	FB_B_RDQS<7>	PP8736	OMIT P4MM
84 34	GPU_CLK100M_PCIE_P	PP8400	OMIT P4MM
84 34	GPU_CLK100M_PCIE_N	PP8401	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4101

41 34	ENET_CLK100M_PCIE_P	PP4100	OMIT P4MM
41 34	ENET_CLK100M_PCIE_N	PP4101	OMIT P4MM

PLACE NEAR U8900

89 87	FB_A_CKE<0>	PP8900	OMIT P4MM
89 87	FB_A_CLK_P<0>	PP8901	OMIT P4MM
89 87	FB_A_CLK_N<0>	PP8902	OMIT P4MM
89 87	FB_A_CS_L<0>	PP8903	OMIT P4MM
89 87	FB_A_WE_L<0>	PP8904	OMIT P4MM
89 87	FB_A_CAS_L<0>	PP8905	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8906	OMIT P4MM
89 87	FB_A_RAS_L<0>	PP8907	OMIT P4MM
90 89 88 5	DRAM_RST	PP8908	OMIT P4MM
89 87	FB_A_WDQS<0>	PP8909	OMIT P4MM
89 87	FB_A_WDQS<1>	PP8910	OMIT P4MM
89 87	FB_A_WDQS<3>	PP8911	OMIT P4MM
89 87	FB_A_WDQS<2>	PP8912	OMIT P4MM
89 87 5	FB_A_DQ<0>	PP8913	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8914	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8915	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8916	OMIT P4MM

PLACE NEAR U8950

89 87	FB_A_CKE<1>	PP8920	OMIT P4MM
89 87	FB_A_CLK_P<1>	PP8921	OMIT P4MM
89 87	FB_A_CLK_N<1>	PP8922	OMIT P4MM
89 87	FB_A_CS_L<1>	PP8923	OMIT P4MM
89 87	FB_A_WE_L<1>	PP8924	OMIT P4MM
89 87	FB_A_CAS_L<1>	PP8925	OMIT P4MM
89 87	FB_A_RAS_L<1>	PP8926	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8927	OMIT P4MM
90 89 88 5	DRAM_RST	PP8928	OMIT P4MM
89 87	FB_A_WDQS<5>	PP8929	OMIT P4MM
89 87	FB_A_WDQS<6>	PP8930	OMIT P4MM
89 87	FB_A_WDQS<4>	PP8931	OMIT P4MM
89 87	FB_A_WDQS<7>	PP8932	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8933	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8934	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8935	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8936	OMIT P4MM

PLACE NEAR U9000

90 87	FB_B_CKE<0>	PP9000	OMIT P4MM
90 87	FB_B_CLK_P<0>	PP9001	OMIT P4MM
90 87	FB_B_CLK_N<0>	PP9002	OMIT P4MM
90 87	FB_B_CS_L<0>	PP9003	OMIT P4MM
90 87	FB_B_WE_L<0>	PP9004	OMIT P4MM
90 87	FB_B_CAS_L<0>	PP9005	OMIT P4MM
90 87	FB_B_RAS_L<0>	PP9006	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9007	OMIT P4MM
90 89 88 5	DRAM_RST	PP9008	OMIT P4MM
90 87	FB_B_WDQS<0>	PP9009	OMIT P4MM
90 87	FB_B_WDQS<1>	PP9010	OMIT P4MM
90 87	FB_B_WDQS<3>	PP9011	OMIT P4MM
90 87	FB_B_WDQS<2>	PP9012	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP9013	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP9014	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP9015	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP9016	OMIT P4MM

PLACE NEAR U9050

90 87	FB_B_CKE<1>	PP9020	OMIT P4MM
90 87	FB_B_CLK_P<1>	PP9021	OMIT P4MM
90 87	FB_B_CLK_N<1>	PP9022	OMIT P4MM
90 87	FB_B_CS_L<1>	PP9023	OMIT P4MM
90 87	FB_B_WE_L<1>	PP9024	OMIT P4MM
90 87	FB_B_CAS_L<1>	PP9025	OMIT P4MM
90 87	FB_B_RAS_L<1>	PP9026	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9027	OMIT P4MM
90 89 88 5	DRAM_RST	PP9028	OMIT P4MM
90 87	FB_B_WDQS<5>	PP9029	OMIT P4MM
90 87	FB_B_WDQS<6>	PP9030	OMIT P4MM
90 87	FB_B_WDQS<7>	PP9031	OMIT P4MM
90 87	FB_B_WDQS<4>	PP9032	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP9033	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP9034	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP9035	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP9036	OMIT P4MM

PLACE NEAR R1210 AND R1211

12	NB_FSB_VREF	PP1200	SM-TP50-TOP
19 12 6	=PP1V05_S0_FSB_NB	PP1201	SM-TP50-TOP
		PP1202	SM-TP50-TOP

PLACE NEAR R0705 AND R0706

11 9 8 7 6	=PP1V05_S0_CPU	PP700	SM-TP50-TOP
7	CPU_GTLREF	PP701	SM-TP50-TOP
		PP702	SM-TP50-TOP

PLACE NEAR R2800 AND R2801

29 28 6	=PP1V8_S3_MEM	PP2800	SM-TP50-TOP
29 28	MEM_VREF	PP2801	SM-TP50-TOP
		PP2802	SM-TP50-TOP

77 76 66 65 59 57 26 6	PP3V3_S5	FUNC_TEST=TRUE
83 82 81 80 79 59 6	PP5V_S5	FUNC_TEST=TRUE
83 82 81 80 79 78 77 57 6	PP12V_S5	FUNC_TEST=TRUE
79 6	PP1V8_S3	FUNC_TEST=TRUE
76 75 6	PPVCORE_CPU	FUNC_TEST=TRUE
26 25 24 21	PP3V3_S5_S8_RTC	FUNC_TEST=TRUE
	8 TESTPOINTS	FUNC_TEST=TRUE

60 59 58	SMC_TCK	FUNC_TEST=TRUE
60 59 58	SMC_TDI	FUNC_TEST=TRUE
60 59 58	SMC_TDO	FUNC_TEST=TRUE
60 59 58	SMC_TMS	FUNC_TEST=TRUE
60 58	SMC_TRST_L	FUNC_TEST=TRUE
60 59 58	SMC_TX_L	FUNC_TEST=TRUE
60 59 58	SMC_RX_L	FUNC_TEST=TRUE
59	SMC_MANUAL_RST_L	FUNC_TEST=TRUE
11 7	XDP_TCK	FUNC_TEST=TRUE
11 7	XDP_TDI	FUNC_TEST=TRUE
11 7	XDP_TDO	FUNC_TEST=TRUE
11 7	XDP_TMS	FUNC_TEST=TRUE
11 7	XDP_TRST_L	FUNC_TEST=TRUE
59	POWER_BUTTON_L	FUNC_TEST=TRUE
26	SW_RST_BTN_L	FUNC_TEST=TRUE

34	TP_PCI_CLK_SPARE	NO_TEST=TRUE
29	TP_MEM_B_A<14>	NO_TEST=TRUE
29	TP_MEM_B_A<15>	NO_TEST=TRUE
43	ENET_MDI_R_N<0>	NO_TEST=TRUE
43	ENET_MDI_R_N<1>	NO_TEST=TRUE
43	ENET_MDI_R_N<2>	NO_TEST=TRUE
43	ENET_MDI_R_N<3>	NO_TEST=TRUE
43	ENET_MDI_R_P<0>	NO_TEST=TRUE
43	ENET_MDI_R_P<1>	NO_TEST=TRUE
43	ENET_MDI_R_P<2>	NO_TEST=TRUE
43	ENET_MDI_R_P<3>	NO_TEST=TRUE

MISC GROUND VIAS

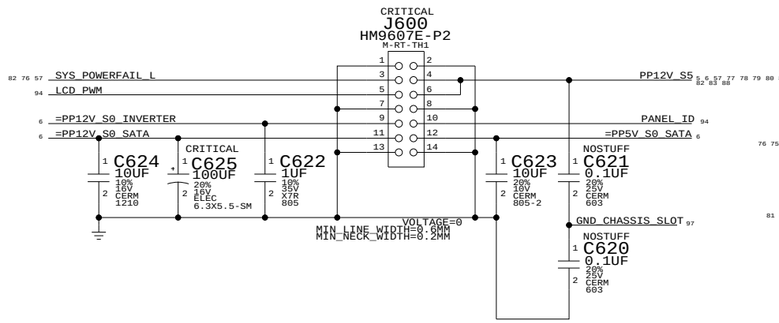
ZH500	HOLE-VIA	ZH510	HOLE-VIA
ZH501	HOLE-VIA	ZH511	HOLE-VIA
ZH502	HOLE-VIA	ZH512	HOLE-VIA
ZH503	HOLE-VIA	ZH513	HOLE-VIA
ZH504	HOLE-VIA	ZH514	HOLE-VIA
ZH505	HOLE-VIA	ZH515	HOLE-VIA
ZH506	HOLE-VIA	ZH516	HOLE-VIA
ZH507	HOLE-VIA	ZH517	HOLE-VIA
ZH508	HOLE-VIA	ZH518	HOLE-VIA
ZH509	HOLE-VIA	ZH519	HOLE-VIA

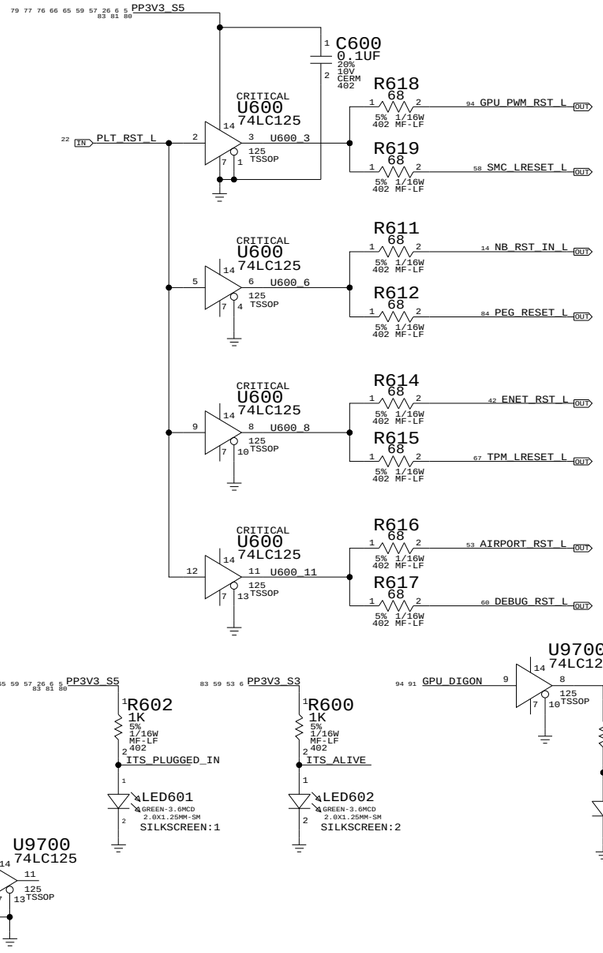
	ZH520	HOLE-VIA
	ZH521	HOLE-VIA
	ZH522	HOLE-VIA
	ZH523	HOLE-VIA
	ZH524	HOLE-VIA
	ZH525	HOLE-VIA
	ZH526	HOLE-VIA
	ZH527	HOLE-VIA
	ZH528	HOLE-VIA
	ZH529	HOLE-VIA

FUNC TEST 1 OF 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 5 OF 110	





"S0" RAILS

ONLY ON IN RUN

- PP0V9_S0 — MAKE_BASE=TRUE, VOLTAGE=0.9V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM
  - =PP0V9_S0_MEMVTT_LDO
  - =PP0V9_S0_MEM_TERM
- PPVCORE_CPU — MAKE_BASE=TRUE, VOLTAGE=1.25V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM
  - =PPVCORE_S0_CPU
- PP1V05_S0 — MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM
  - =PPVCORE_S0_NB
  - =PP1V05_S0_CPU
  - =PP1V05_S0_FSB_NB
  - =PP1V05_S0_NB_VTT
  - =PP1V05_S0_NB
  - =PP1V05_S0_SB_CPU_IO
  - =PPVCORE_S0_SB
- PP1V5_S0 — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM
  - =PP1V5_S0_CPU
  - =PP1V5_S0_NB_PCIE
  - =PP1V5_S0_NB_VCCAUX
  - =PP1V5_S0_NB_VCCD_HMPLL
  - =PP1V5_S0_NB_VCCAUX
  - =PP1V5_S0_NB_PLL
  - =PP1V5_S0_NB
  - =PP1V5_S0_NB_TVDAC
  - =PP1V5_S0_NB_3GPLL
  - =PP1V5_S0_SB_VCC1_5_A_ARX
  - =PP1V5_S0_SB_VCCSATAPLL
  - =PP1V5_S0_SB_VCC1_5_A_ATX
  - =PP1V5_S0_SB_VCCUSBPLL
  - =PP1V5_S0_SB_VCC1_5_A_USB_CORE
  - =PP1V5_S0_SB_VCC1_5_A
  - =PP1V5_S0_SB
  - =PP1V5_S0_AIRPORT
- PP2V5_S0 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM
  - =PP2V5_S0_NB_VCCA_3GBG
- PP3V3_S0 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.30MM, MIN_NECK_WIDTH=0.20MM
  - =PP3V3_S0_NB_VCC_HV
  - =PP3V3_S0_NB_TVDAC
  - =PP3V3_S0_SB
  - =PP3V3_S0_SB_GPIO
  - =PP3V3_S0_SB_VCC3_3
  - =PP3V3_S0_SB_VCC3_3_PCI
  - =PP3V3_S0_SB_VCC3_3_IDE
  - =PP3V3_S0_SB_PCI
  - =PP3V3_S0_SB_PM
  - =PP3V3_S0_PATA
  - =PP3V3_S0_FAN
  - =PP3V3_S0_HD_TSENS
  - =PP3V3_S0_ODD_TSENS
  - =PP3V3_S0_SB_3V3_1V5_VCCHDA
  - =PP3V3_S0_TPM
  - =PPSPD_S0_MEM
  - =PP3V3_S0_CK410
  - =PP3V3_S0_IMVP
  - =PP3V3_S0_AUDIO
  - =PP3V3_S0_PCI
  - =PP3V3_S0_SB_VCCLAN3_3
  - =PP3V3_S0_AIRPORT
  - =PP3V3_S0_NB
- PP4V5_S0_AUDIO_ANALOG — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
  - =PP4V5_S0_AUDIO_ANALOG
- PP5V_S0 — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM
  - =PP5V_S0_SB
  - =PP5V_S0_PATA
  - =PP5V_S0_DEBUG
  - =PP5V_S0_SATA
- PP12V_S0 — MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM
  - =PP12V_S0_FAN
  - XW605 SM OMIT — PP12V_S0_AUDIO_SPKRAMP (MAKE_BASE=TRUE) → =PP12V_S0_AUDIO_SPKRAMP
  - =PP12V_S0_INVERTER
  - =PP12V_S0_SATA

"S3" RAILS

ON IN RUN AND SLEEP

- PP1V2_S3 — MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - =PP1V2_S3_LAN
- PP1V8_S3 — MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - =PP1V8_S3_MEM_NB
  - =PP1V8_S3_MEM_NB
  - =PP1V8_S3_MEM
  - =PP1V8_S0_MEMVTT
- PP3V3_S3 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
  - =PP3V3_S3_ENET
  - =PP3V3_S3_TPM
  - =PP3V3_S3_1V2REG
  - =PP3V3_S3_BT
  - =PP3V3_S3_VGASYNC
- PP5V_S3 — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
  - =PP5V_S3_USB
  - =PP5V_S3_BNDI
  - =PP5V_S0_MEMVTT

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

- PP3V3_S5 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - =PP3V3_S5_SB
  - =PP3V3_S5_SB_USB
  - =PP3V3_S5_SB_PM
  - =PP3V3_S5_SB_VCCSUS3_3
  - =PP3V3_S5_SB_VCCSUS3_3_USB
  - =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
  - =PP3V3_S5_SB_IO
  - =PP3V3_S5_FW
  - =PP3V3_S5_SMC
  - =PP3V3_S5_2V5_LDO
  - =PP3V3_S5_DEBUG
  - =PP3V3_S5_ROM
- PP5V_S5 — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - =PP5V_S5_SB
  - =PP5V_S5_AUDIO_LDO
- PP12V_S5 — MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - =PP12V_S5_FW
  - =PP12V_S5_CPU

GND RAILS

XW602 SM NOSTUFF — GND_AUDIO_SPKRAMP

CHASSIS GND

R603 0 5% 1/16W MF-LF 402 NOSTUFF

- GND_CHASSIS_IO_LEFT — MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - GND_CHASSIS_AUDIO_EXTERNAL
  - GND_CHASSIS_USB
- GND_CHASSIS_IO_RIGHT — MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM
  - GND_CHASSIS_FIREWIRE
  - GND_CHASSIS_VGA
  - GND_CHASSIS_RJ45
- GND_CHASSIS_AUDIO_INTERNAL — ZH606 160R138 OMIT
- GND_CHASSIS_BNDI — MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0, MAKE_BASE=TRUE

ZH601 4P25R3P5 OMIT — ZH701P1
ZH602 4P25R3P5 OMIT — ZH702P1
ZH603 4P25R3P5 OMIT — ZH703P1
C601 0.01UF 20% 16V CERM 402 NOSTUFF
C602 0.01UF 20% 16V CERM 402 NOSTUFF
C603 0.01UF 20% 16V CERM 402 NOSTUFF

Power Conn / Alias

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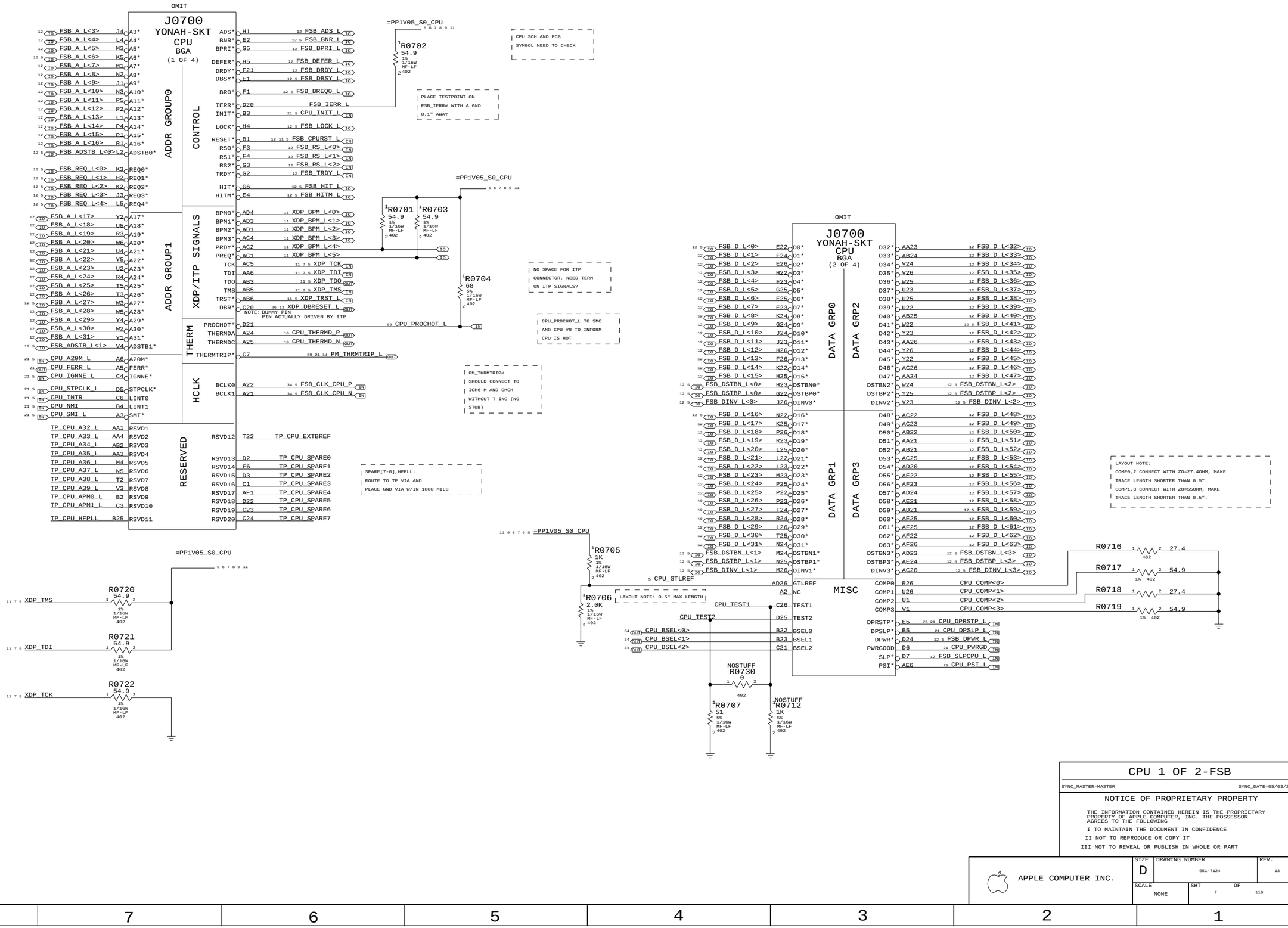
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
	SCALE: NONE	SHT 6 OF 110	



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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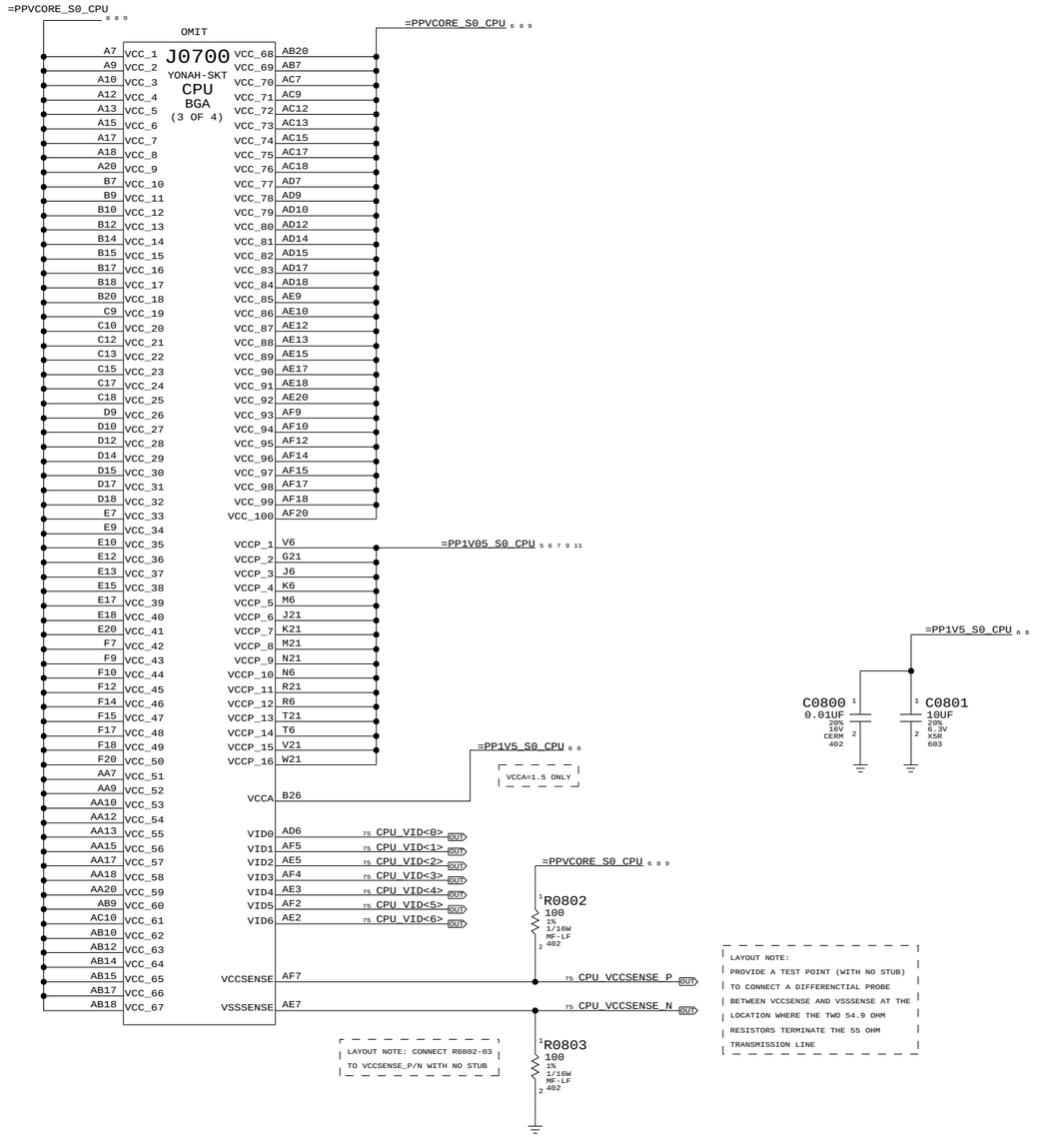
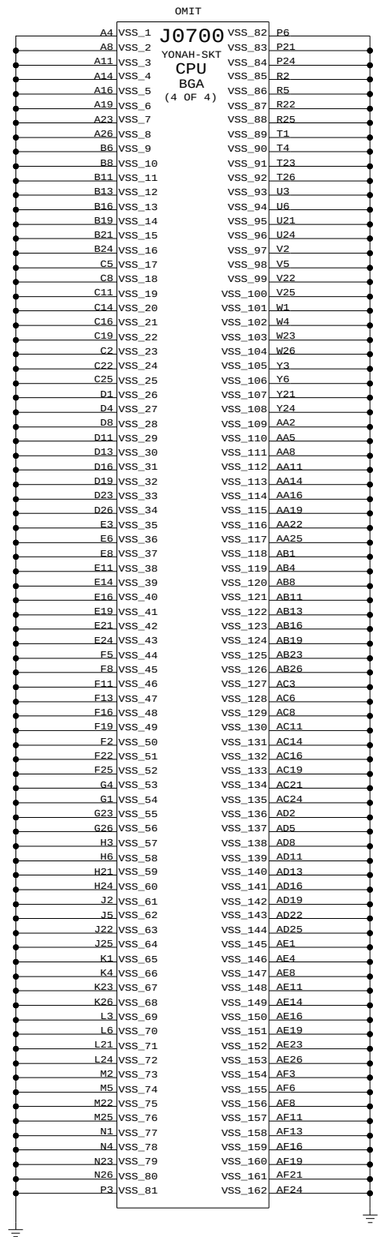
D	051-7124	13
SCALE: NONE	SHT 7 OF 110	





CPU 2 OF 2-PWR/GND

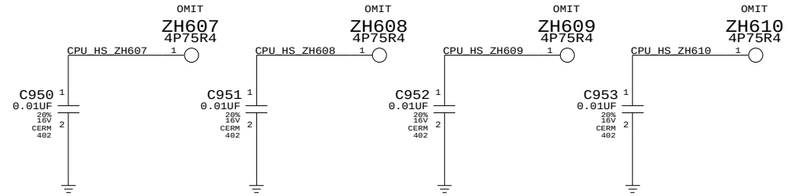
SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

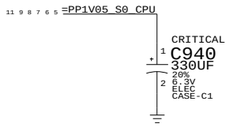
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

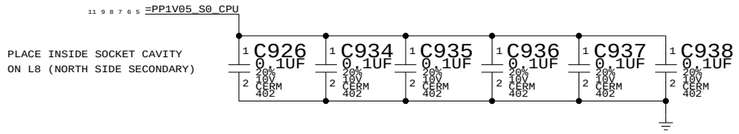
SCALE	SHT	OF
NONE	8	110

CPU HEATSINK MOUNTING HOLES

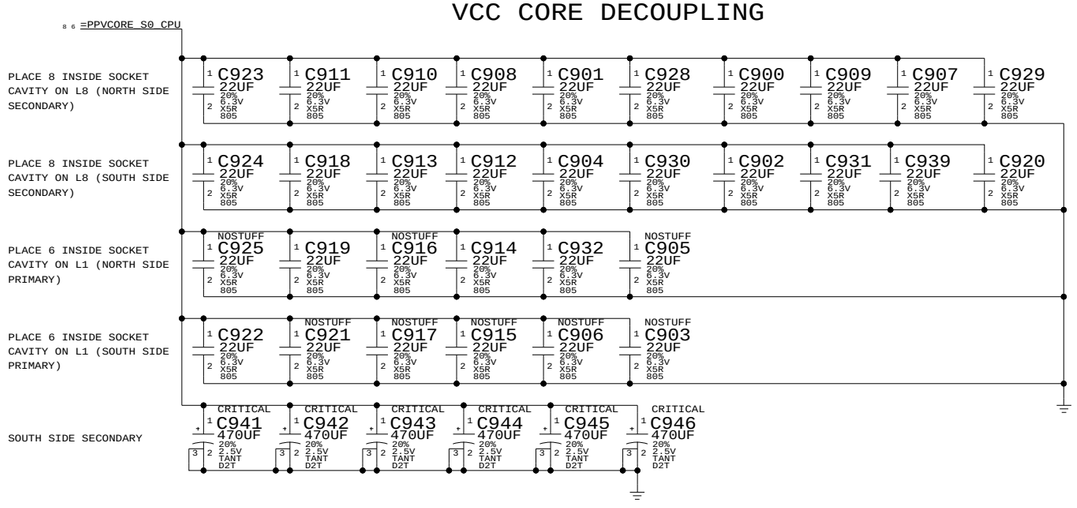




VCCP CORE DECOUPLING



VCC CORE DECOUPLING



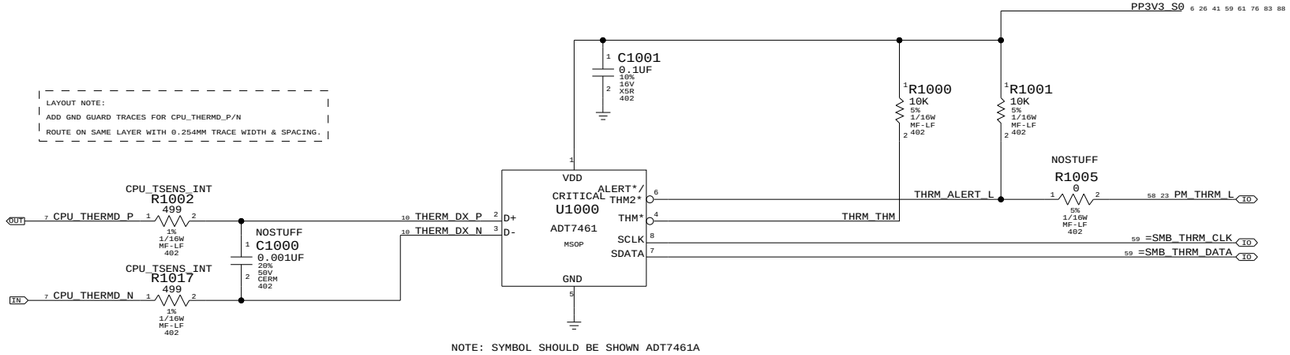
CPU DECAPS & VID<>

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 9 OF 110	

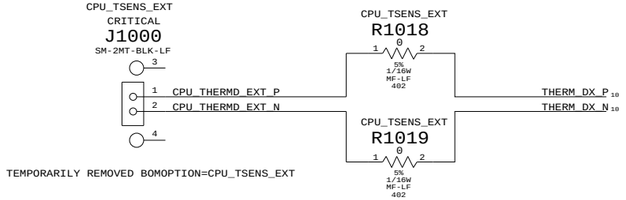
CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

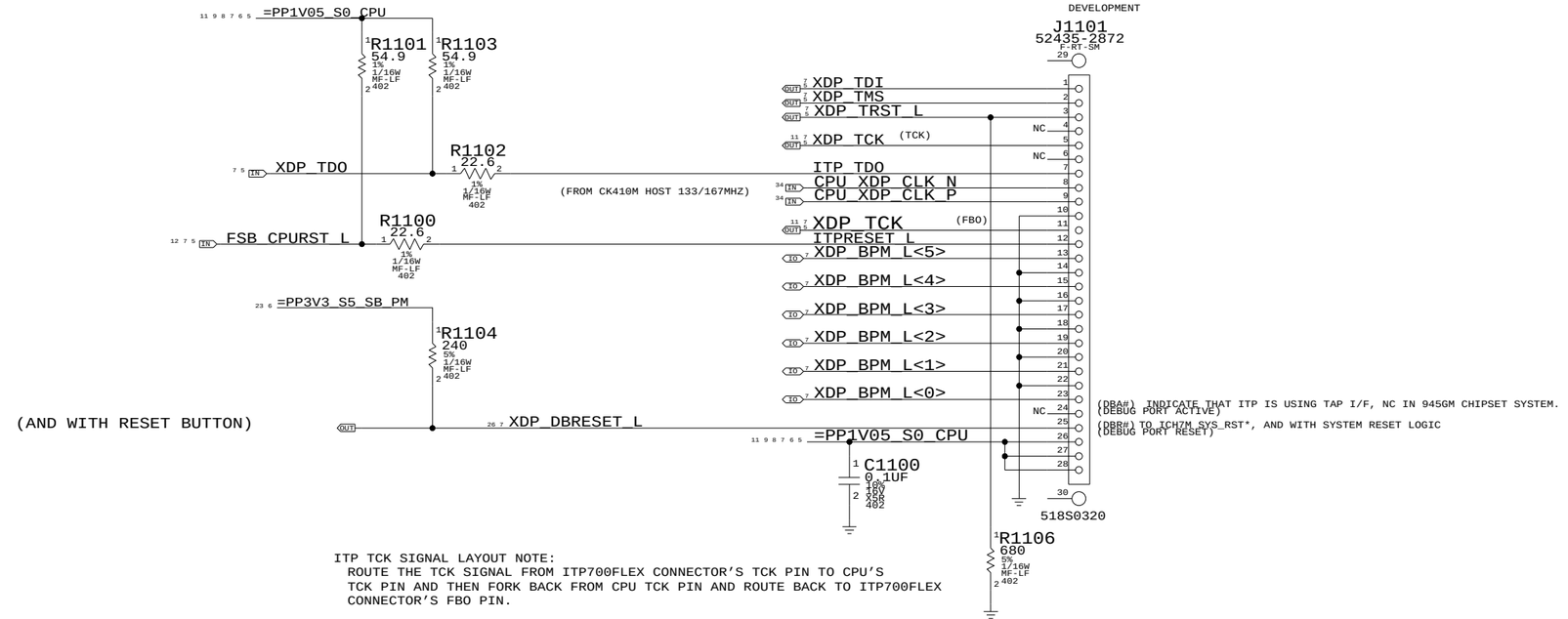
CPU TEMP SENSOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	10	110

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

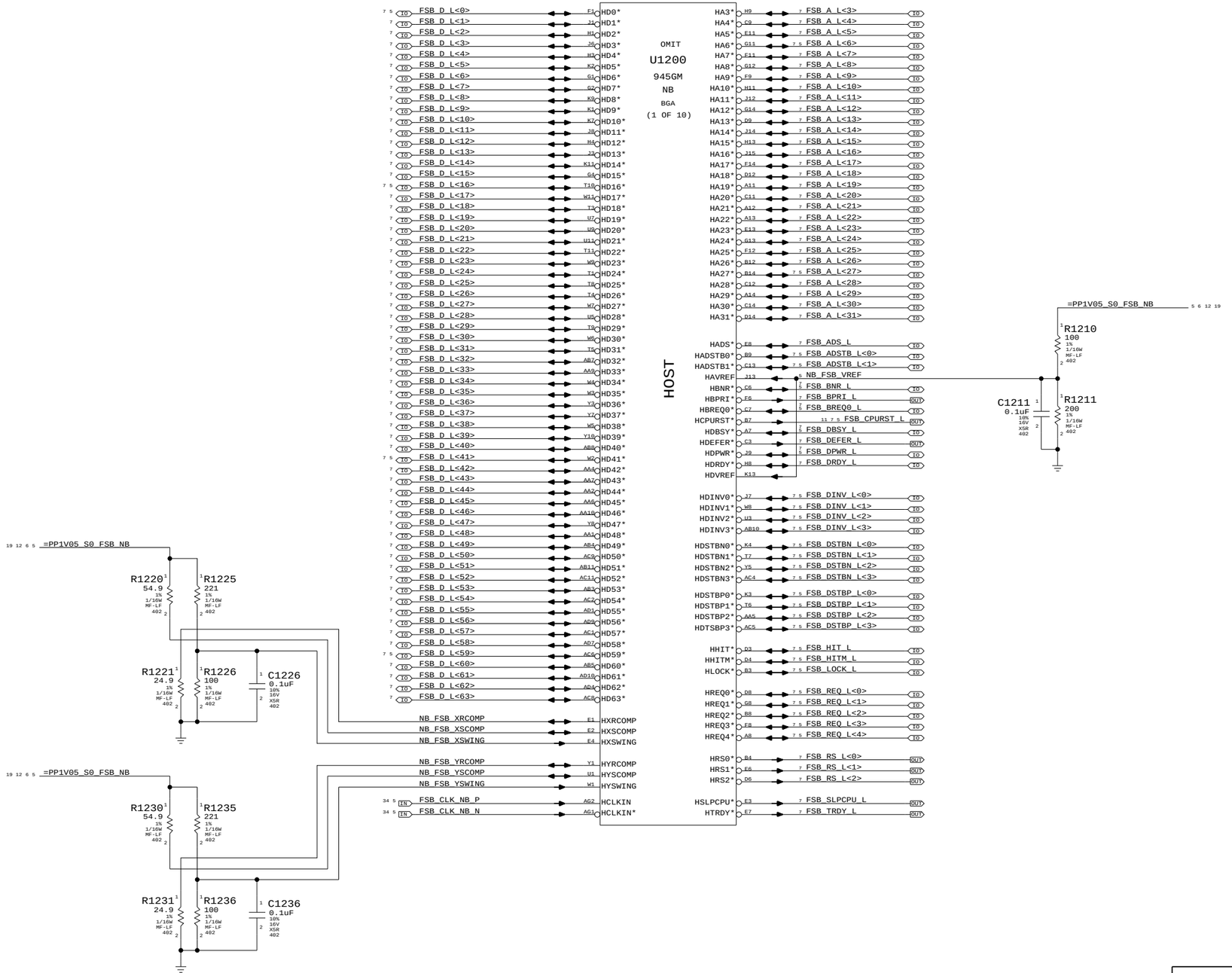
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	11	110



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	12	110

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

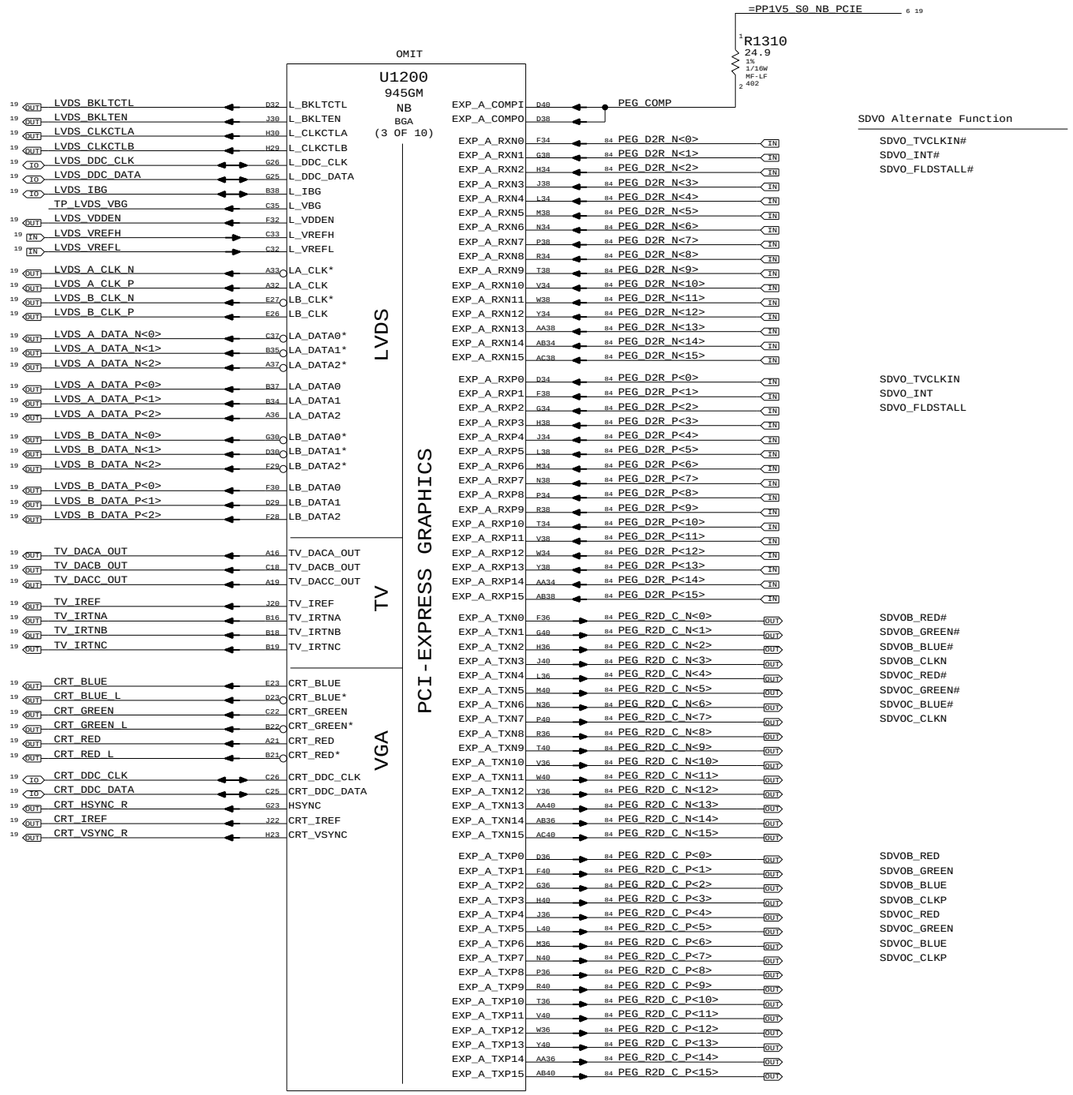
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

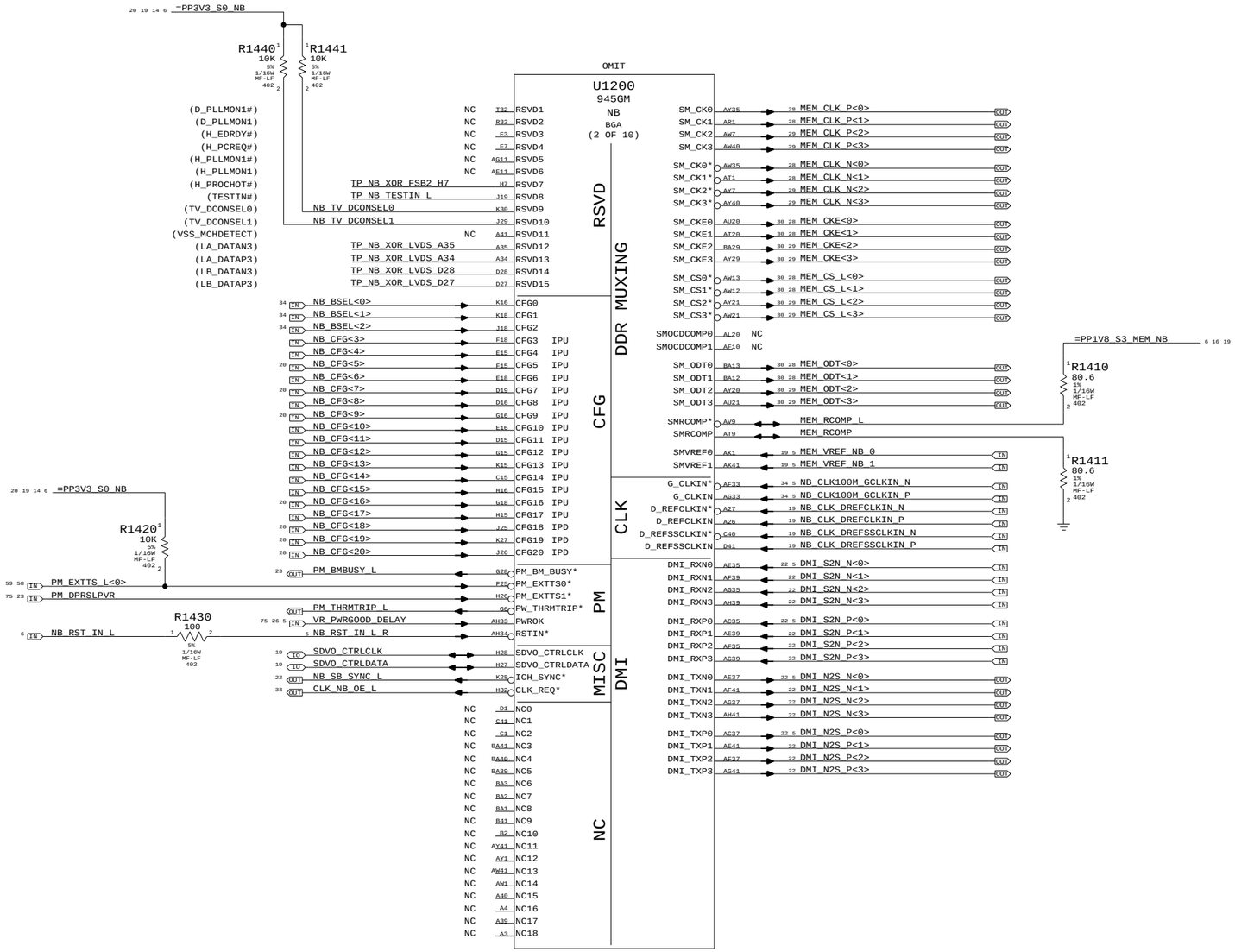
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	13	110

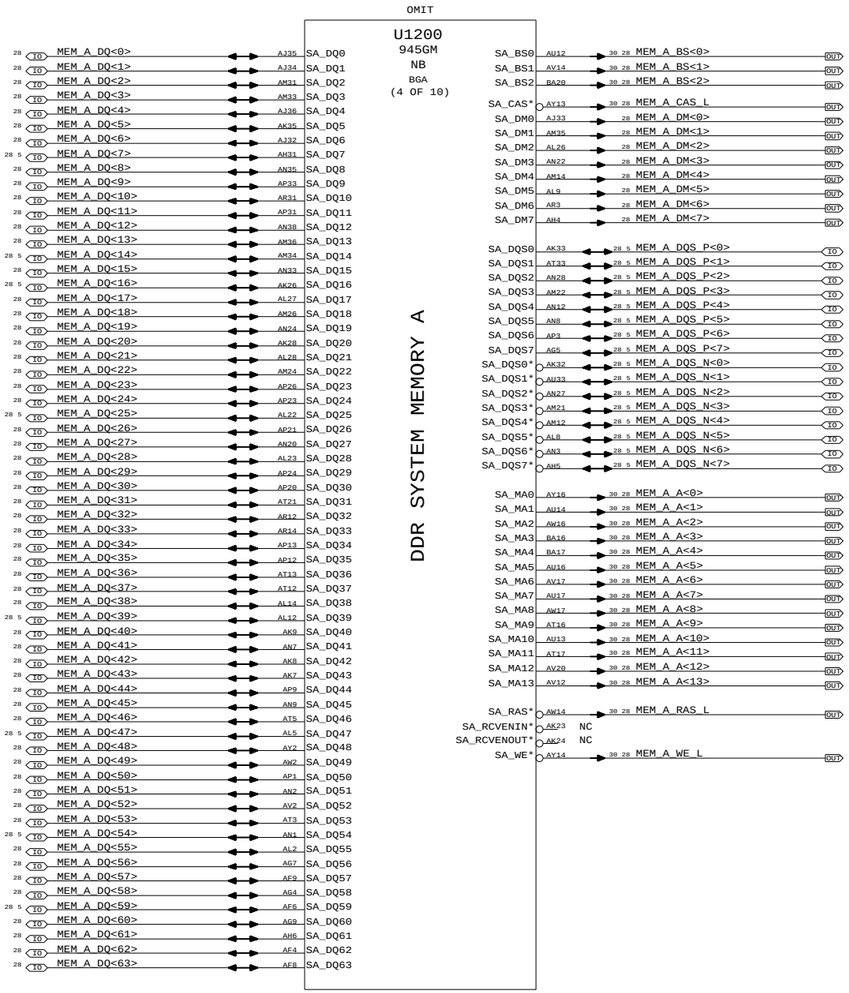


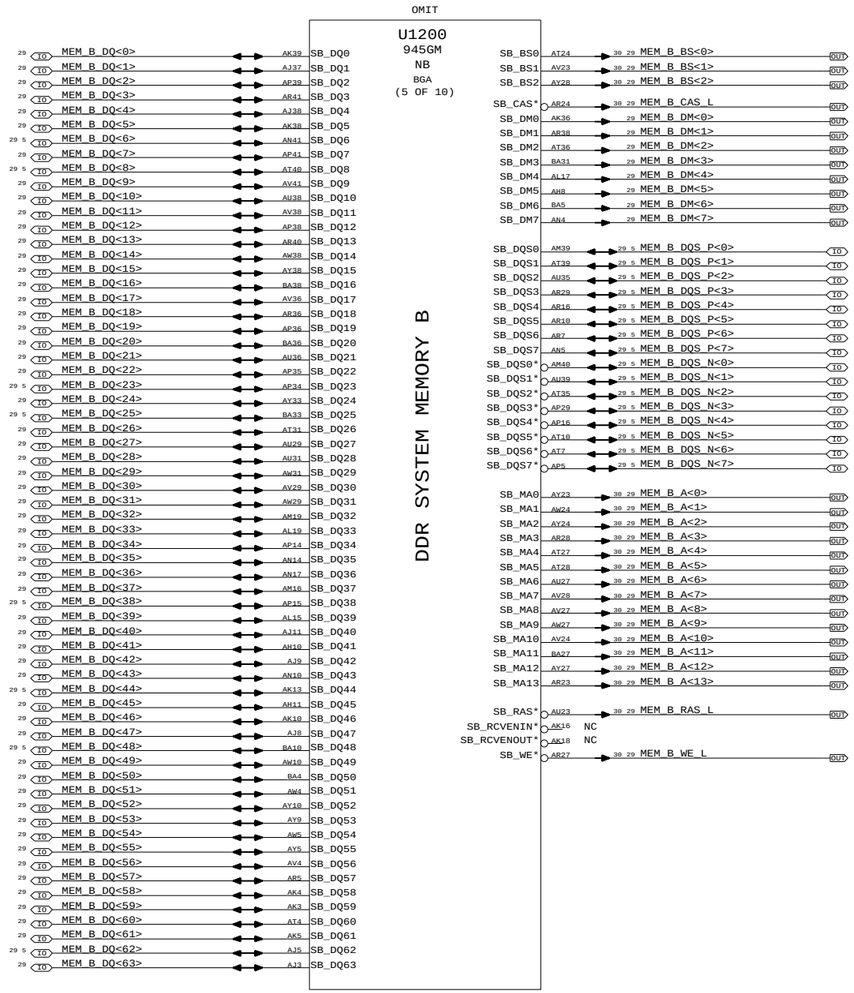
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 14 OF 110	





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE

SHT 15 OF 110

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 6 16 19

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) OMIT VCC

VCC_0 AA33, VCC_1 AK3, VCC_2 P33, VCC_3 N33, VCC_4 L33, VCC_5 J33, VCC_6 AA32, VCC_7 Y32, VCC_8 W32, VCC_9 V32, VCC_10 P32, VCC_11 N32, VCC_12 M32, VCC_13 L32, VCC_14 J32, VCC_15 AA31, VCC_16 W31, VCC_17 V31, VCC_18 T31, VCC_19 R31, VCC_20 P31, VCC_21 N31, VCC_22 M31, VCC_23 AA30, VCC_24 W30, VCC_25 V30, VCC_26 U30, VCC_27 T30, VCC_28 R30, VCC_29 P30, VCC_30 N30, VCC_31 M30, VCC_32 L30, VCC_33 AA29, VCC_34 Y29, VCC_35 W29, VCC_36 V29, VCC_37 U29, VCC_38 P29, VCC_39 M29, VCC_40 L29, VCC_41 AB28, VCC_42 AB23, VCC_43 AB20, VCC_44 AA28, VCC_45 Y28, VCC_46 V28, VCC_47 U28, VCC_48 T28, VCC_49 R28, VCC_50 P28, VCC_51 N28, VCC_52 M28, VCC_53 L28, VCC_54 P27, VCC_55 M27, VCC_56 L27, VCC_57 P26, VCC_58 N26, VCC_59 L26, VCC_60 M25, VCC_61 L25, VCC_62 P24, VCC_63 M24, VCC_64 L24, VCC_65 AB23, VCC_66 AB20, VCC_67 AA23, VCC_68 Y23, VCC_69 P23, VCC_70 N23, VCC_71 M23, VCC_72 L23, VCC_73 AC22, VCC_74 AB22, VCC_75 Y22, VCC_76 W22, VCC_77 P22, VCC_78 N22, VCC_79 M22, VCC_80 L22, VCC_81 AC21, VCC_82 AA21, VCC_83 Y21, VCC_84 W21, VCC_85 N21, VCC_86 L21, VCC_87 AC20, VCC_88 AB20, VCC_89 Y20, VCC_90 W20, VCC_91 P20, VCC_92 N20, VCC_93 M20, VCC_94 L20, VCC_95 AB19, VCC_96 AA19, VCC_97 Y19, VCC_98 W19, VCC_99 N19, VCC_100 L19, VCC_101 N18, VCC_102 L18, VCC_103 P17, VCC_104 L17, VCC_105 N17, VCC_106 M17, VCC_107 N16, VCC_108 M16, VCC_109 L16, VCC_110

VCC_SM0 AU41, VCC_SM1 AT41, VCC_SM2 AM41, VCC_SM3 AU40, VCC_SM4 BA34, VCC_SM5 AW34, VCC_SM6 AV34, VCC_SM7 AU34, VCC_SM8 AT34, VCC_SM9 AR34, VCC_SM10 BA30, VCC_SM11 AY30, VCC_SM12 AW30, VCC_SM13 AV30, VCC_SM14 AU30, VCC_SM15 AT30, VCC_SM16 AR30, VCC_SM17 AP30, VCC_SM18 AN30, VCC_SM19 AM30, VCC_SM20 AM29, VCC_SM21 AL29, VCC_SM22 AK29, VCC_SM23 AJ29, VCC_SM24 AH29, VCC_SM25 AJ28, VCC_SM26 AH28, VCC_SM27 AJ27, VCC_SM28 AH27, VCC_SM29 BA26, VCC_SM30 AY26, VCC_SM31 AW26, VCC_SM32 AV26, VCC_SM33 AU26, VCC_SM34 AT26, VCC_SM35 AR26, VCC_SM36 AJ26, VCC_SM37 AH26, VCC_SM38 AJ25, VCC_SM39 AH25, VCC_SM40 AJ24, VCC_SM41 AH24, VCC_SM42 BA23, VCC_SM43 AJ23, VCC_SM44 BA22, VCC_SM45 AY22, VCC_SM46 AM22, VCC_SM47 AV22, VCC_SM48 AU22, VCC_SM49 AT22, VCC_SM50 AR22, VCC_SM51 AP22, VCC_SM52 AK22, VCC_SM53 AJ22, VCC_SM54 AK21, VCC_SM55 AK20, VCC_SM56 BA19, VCC_SM57 AY19, VCC_SM58 AW19, VCC_SM59 AV19, VCC_SM60 AT19, VCC_SM61 AU19, VCC_SM62 AK19, VCC_SM63 AR19, VCC_SM64 AK18, VCC_SM65 AJ18, VCC_SM66 AJ17, VCC_SM67 AH17, VCC_SM68 AJ16, VCC_SM69 AH16, VCC_SM70 BA15, VCC_SM71 AY15, VCC_SM72 AM15, VCC_SM73 AV15, VCC_SM74 AU15, VCC_SM75 AT15, VCC_SM76 AR15, VCC_SM77 AJ15, VCC_SM78 AJ14, VCC_SM79 AJ13, VCC_SM80 AH13, VCC_SM81 AK12, VCC_SM82 AJ12, VCC_SM83 AH12, VCC_SM84 AG12, VCC_SM85 AK11, VCC_SM86 AJ11, VCC_SM87 BA8, VCC_SM88 AY8, VCC_SM89 AW8, VCC_SM90 AV8, VCC_SM91 AU8, VCC_SM92 AT8, VCC_SM93 AR8, VCC_SM94 AP8, VCC_SM95 BA6, VCC_SM96 AY6, VCC_SM97 AV6, VCC_SM98 AU6, VCC_SM99 AT6, VCC_SM100 AR6, VCC_SM101 AP6, VCC_SM102 AN6, VCC_SM103 AL6, VCC_SM104 AJ6, VCC_SM105 AV1, VCC_SM106 AJ1, VCC_SM107

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402

C1613 0.47uF 20% 6.3V CERM-X5R 402

1 C1615 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA23

19 14 6 =PP1V8_S3_MEM_NB

C1620 10UF 20% 6.3V CERM 805-1

C1621 10UF 20% 6.3V CERM 805-1

C1610 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA15

Layout Note: Place in cavity (Need to better define cavity)

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 0.47uF 20% 6.3V CERM-X5R 402

C1611 0.47uF 20% 6.3V CERM-X5R 402

19 16 6 =PPVCORE_S0_NB

U1200 945GM NB BGA (7 OF 10) OMIT NCTF

VCC_NCTF0 AD27, VCC_NCTF1 AC27, VCC_NCTF2 AB27, VCC_NCTF3 AA27, VCC_NCTF4 Y27, VCC_NCTF5 W27, VCC_NCTF6 V27, VCC_NCTF7 U27, VCC_NCTF8 T27, VCC_NCTF9 R27, VCC_NCTF10 AD26, VCC_NCTF11 AC26, VCC_NCTF12 AB26, VCC_NCTF13 AA26, VCC_NCTF14 Y26, VCC_NCTF15 W26, VCC_NCTF16 V26, VCC_NCTF17 U26, VCC_NCTF18 T26, VCC_NCTF19 R26, VCC_NCTF20 AD25, VCC_NCTF21 AC25, VCC_NCTF22 AB25, VCC_NCTF23 AA25, VCC_NCTF24 Y25, VCC_NCTF25 W25, VCC_NCTF26 V25, VCC_NCTF27 U25, VCC_NCTF28 T25, VCC_NCTF29 R25, VCC_NCTF30 AD24, VCC_NCTF31 AC24, VCC_NCTF32 AB24, VCC_NCTF33 AA24, VCC_NCTF34 Y24, VCC_NCTF35 W24, VCC_NCTF36 V24, VCC_NCTF37 U24, VCC_NCTF38 T24, VCC_NCTF39 R24, VCC_NCTF40 AD23, VCC_NCTF41 U23, VCC_NCTF42 T23, VCC_NCTF43 R23, VCC_NCTF44 AD22, VCC_NCTF45 V22, VCC_NCTF46 U22, VCC_NCTF47 T22, VCC_NCTF48 R22, VCC_NCTF49 AD21, VCC_NCTF50 V21, VCC_NCTF51 U21, VCC_NCTF52 T21, VCC_NCTF53 R21, VCC_NCTF54 AD20, VCC_NCTF55 V20, VCC_NCTF56 U20, VCC_NCTF57 T20, VCC_NCTF58 R20, VCC_NCTF59 AD19, VCC_NCTF60 V19, VCC_NCTF61 U19, VCC_NCTF62 T19, VCC_NCTF63 AD18, VCC_NCTF64 AC18, VCC_NCTF65 AB18, VCC_NCTF66 AA18, VCC_NCTF67 Y18, VCC_NCTF68 W18, VCC_NCTF69 V18, VCC_NCTF70 U18, VCC_NCTF71 T18, VCC_NCTF72

VSS_NCTF0 AE27, VSS_NCTF1 AE26, VSS_NCTF2 AE25, VSS_NCTF3 AE24, VSS_NCTF4 AE23, VSS_NCTF5 AE22, VSS_NCTF6 AE21, VSS_NCTF7 AE20, VSS_NCTF8 AE19, VSS_NCTF9 AE18, VSS_NCTF10 AC17, VSS_NCTF11 Y17, VSS_NCTF12 U17

=PP1V5_S0_NB_VCCAUX 6 17 19

VCCAUX_NCTF0 AG27, VCCAUX_NCTF1 AF27, VCCAUX_NCTF2 AG26, VCCAUX_NCTF3 AF26, VCCAUX_NCTF4 AG25, VCCAUX_NCTF5 AF25, VCCAUX_NCTF6 AG24, VCCAUX_NCTF7 AF24, VCCAUX_NCTF8 AG23, VCCAUX_NCTF9 AF23, VCCAUX_NCTF10 AG22, VCCAUX_NCTF11 AF22, VCCAUX_NCTF12 AG21, VCCAUX_NCTF13 AF21, VCCAUX_NCTF14 AG20, VCCAUX_NCTF15 AF20, VCCAUX_NCTF16 AG19, VCCAUX_NCTF17 AF19, VCCAUX_NCTF18 R19, VCCAUX_NCTF19 AG18, VCCAUX_NCTF20 AF18, VCCAUX_NCTF21 R18, VCCAUX_NCTF22 AG17, VCCAUX_NCTF23 AF17, VCCAUX_NCTF24 AE17, VCCAUX_NCTF25 AD17, VCCAUX_NCTF26 AB17, VCCAUX_NCTF27 AA17, VCCAUX_NCTF28 W17, VCCAUX_NCTF29 V17, VCCAUX_NCTF30 T17, VCCAUX_NCTF31 R17, VCCAUX_NCTF32 AG16, VCCAUX_NCTF33 AF16, VCCAUX_NCTF34 AE16, VCCAUX_NCTF35 AD16, VCCAUX_NCTF36 AC16, VCCAUX_NCTF37 AB16, VCCAUX_NCTF38 AA16, VCCAUX_NCTF39 Y16, VCCAUX_NCTF40 W16, VCCAUX_NCTF41 V16, VCCAUX_NCTF42 U16, VCCAUX_NCTF43 T16, VCCAUX_NCTF44 R16, VCCAUX_NCTF45 AG15, VCCAUX_NCTF46 AF15, VCCAUX_NCTF47 AE15, VCCAUX_NCTF48 AD15, VCCAUX_NCTF49 AC15, VCCAUX_NCTF50 AB15, VCCAUX_NCTF51 AA15, VCCAUX_NCTF52 Y15, VCCAUX_NCTF53 W15, VCCAUX_NCTF54 V15, VCCAUX_NCTF55 U15, VCCAUX_NCTF56 T15, VCCAUX_NCTF57 R15

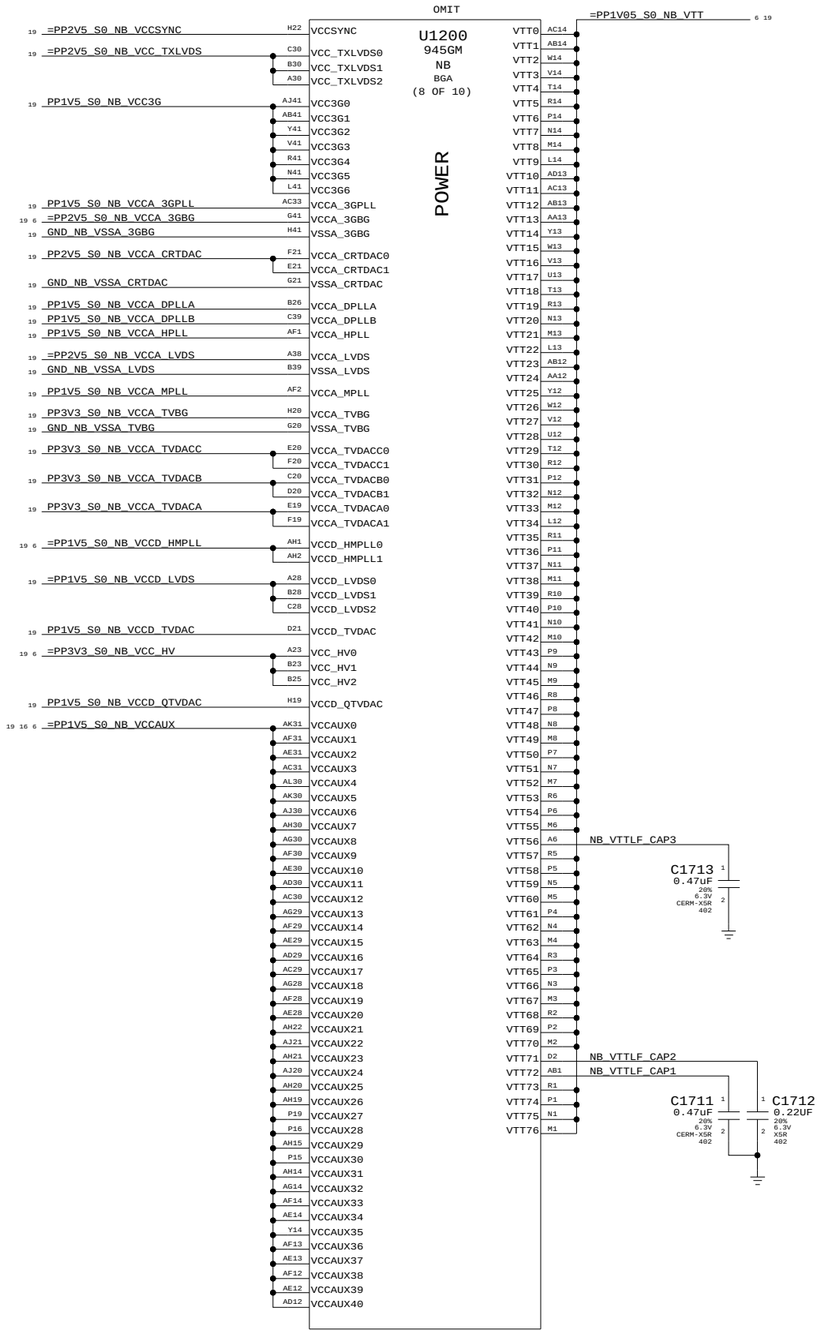
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	16	110



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	17	110

OMIT

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	18	110

Power Interface

These are the power signals that leave the NB "block"

=PP1V05_S0_FSB_NB — 5 6 12
=PPVCORE_S0_NB — 6 16 19
=PP1V05_S0_NB — 6
=PP1V05_S0_NB_VTT — 6 17 19
=PP1V5_S0_NB — 6 19
=PP1V5_S0_NB_PCIE — 6 13
=PP1V5_S0_NB_PLL — 6 19
=PP1V5_S0_NB_TVDAC — 6 19
=PP1V5_S0_NB_VCCD_HMPLL — 6 17
=PP1V5_S0_NB_VCCD_LVDS — 17 19
=PP1V5_S0_NB_VCCAUX — 6 16 17 19
=PP1V8_S3_MEM_NB — 6 14 16 19

=PP2V5_S0_NB_VCCSYNC — 17 19
=PP2V5_S0_NB_VCC_TXLVDS — 17 19
=PP2V5_S0_NB_VCCA_3GBG — 6 17 19
=PP2V5_S0_NB_VCCA_LVDS — 17 19

=PP3V3_S0_NB — 6 14 20
=PP3V3_S0_NB_TVDAC — 6
=PP3V3_S0_NB_VCC_HV — 6 17 19

=PP1V5_S0_NB_PLL — 19 6
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL — 17
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=0.2 MM
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402

Layout Note:
These 4 0.1uF caps should
be within 5 mm of NB edge

L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL — 17
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=0.2 MM
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402

=PP1V05_S0_NB_VTT — 19 17 6
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 10% 6.3V CERM1 603

Layout Note:
Place in cavity

C1967 0.22uF 20% 6.3V X5R 402
NOSTUFF C1968 330UF 20% 6.3V ELEC CASE-C1

Layout Note:
Place on the edge

=PP1V8_S3_MEM_NB — 19 16 14 6
R1982 1K 5% 1/16W MF-LF 402
MEM_VREF_NB_1 — 5 14
R1983 1K 5% 1/16W MF-LF 402
C1982 0.1UF 20% 16V CERM 603

R1980 1K 5% 1/16W MF-LF 402
MEM_VREF_NB_0 — 5 14
R1981 1K 5% 1/16W MF-LF 402
C1981 0.1UF 20% 16V CERM 603

=PP3V3_S0_NB_VCC_HV — 19 17 6
C1914 10UF 20% 6.3V CERM 805-1
C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG — 19 17 6
C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX — 19 17 16 6
C1918 0.1uF 20% 10V CERM 402

TVOUT DISABLE

=PPVCORE_S0_NB — 16 6 19
PP2V5_S0_NB_VCCA_CRTDAC — 17
CRT_RED — 13
CRT_RED_L — 13
CRT_GREEN — 13
CRT_GREEN_L — 13
CRT_BLUE — 13
CRT_BLUE_L — 13
CRT_IREF — 13

CRT_VSYNC_R — 13
CRT_HSYNC_R — 13
=PP2V5_S0_NB_VCCSYNC — 17 19
GND_NB_VSSA_CRTDAC — 17

TP_CRT_DDC_CLK TRUE — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA TRUE — CRT_DDC_DATA — 13

DISPLAY DISABLE

TP_NB_VCCA_DPLLA TRUE — PP1V5_S0_NB_VCCA_DPLLA — 17
TP_NB_VCCA_DPLLB TRUE — PP1V5_S0_NB_VCCA_DPLLB — 17

NB_CLK_DREFCLKIN_N (IN) — 14
NB_CLK_DREFCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_N (OUT) — 14

=PPVCORE_S0_NB — 19 16 6
C1900 330UF 20% 6.3V ELEC CASE-C1
C1901 330UF 20% 6.3V ELEC CASE-C1
C1902 10UF 20% 6.3V CERM 805-1
C1903 10UF 20% 6.3V CERM 805-1
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

=PP1V5_S0_NB_3GPLL — 19 6
L1970 91NH 1210
Layout Note:
Place L and C
close to MCH
C1970 220UF 20% 2.5V POLY SMD2
C1971 10UF 20% 6.3V CERM 805-1
C1972 10UF 20% 6.3V CERM 805-1
PP1V5_S0_NB_VCC3G — 17
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=0.2 MM
Layout Note:
10uF caps should
be close to MCH
on opposite side.

1uH, 20%
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=0.2 MM
Should be 1%
R1975 0.51 1% 1/16W MF-LF 402
C1975 10UF 20% 6.3V CERM 805-1
C1976 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_3GPLL — 17
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=0.2 MM
GND_NB_VSSA_3GBG — 17
Layout Note: Route to caps, then GND
Layout Note:
3GPLL 10uF cap should
be placed in cavity

LVDS DISABLE

LVDS_A_CLK_N (TO) — TRUE — TP_LVDS_A_CLK_N — 13
LVDS_A_CLK_P (TO) — TRUE — TP_LVDS_A_CLK_P — 13
LVDS_B_CLK_N (TO) — TRUE — TP_LVDS_B_CLK_N — 13
LVDS_B_CLK_P (TO) — TRUE — TP_LVDS_B_CLK_P — 13

LVDS_A_DATA_N<0> (TO) — TRUE — TP_LVDS_A_DATA_N<0> — 13
LVDS_A_DATA_N<1> (TO) — TRUE — TP_LVDS_A_DATA_N<1> — 13
LVDS_A_DATA_N<2> (TO) — TRUE — TP_LVDS_A_DATA_N<2> — 13

LVDS_A_DATA_P<0> (TO) — TRUE — TP_LVDS_A_DATA_P<0> — 13
LVDS_A_DATA_P<1> (TO) — TRUE — TP_LVDS_A_DATA_P<1> — 13
LVDS_A_DATA_P<2> (TO) — TRUE — TP_LVDS_A_DATA_P<2> — 13

LVDS_B_DATA_N<0> (TO) — TRUE — TP_LVDS_B_DATA_N<0> — 13
LVDS_B_DATA_N<1> (TO) — TRUE — TP_LVDS_B_DATA_N<1> — 13
LVDS_B_DATA_N<2> (TO) — TRUE — TP_LVDS_B_DATA_N<2> — 13

LVDS_B_DATA_P<0> (TO) — TRUE — TP_LVDS_B_DATA_P<0> — 13
LVDS_B_DATA_P<1> (TO) — TRUE — TP_LVDS_B_DATA_P<1> — 13
LVDS_B_DATA_P<2> (TO) — TRUE — TP_LVDS_B_DATA_P<2> — 13

LVDS_BKLTEN (IN) — TRUE — TP_LVDS_BKLTEN — 13
LVDS_VDDEN (IN) — TRUE — TP_LVDS_VDDEN — 13
LVDS_IBG (IN) — TRUE — TP_LVDS_IBG — 13
GND_NB_VSSA_LVDS (IN) — TRUE — TP_GND_NB_VSSA_LVDS — 17
LVDS_VREFH (OUT) — TRUE — TP_LVDS_VREFH — 13
LVDS_VREFL (OUT) — TRUE — TP_LVDS_VREFL — 13

=PP2V5_S0_NB_VCCA_LVDS — 19 17
=PP1V5_S0_NB_VCCD_LVDS — 19 17
=PP2V5_S0_NB_VCC_TXLVDS — 19 17

LVDS_BKLTCTL (IN) — TRUE — TP_LVDS_BKLTCTL — 13
LVDS_CLKCTLA (IN) — TRUE — TP_LVDS_CLKCTLA — 13
LVDS_CLKCTLB (IN) — TRUE — TP_LVDS_CLKCTLB — 13
LVDS_DDC_CLK (IN) — TRUE — TP_LVDS_DDC_CLK — 13
LVDS_DDC_DATA (IN) — TRUE — TP_LVDS_DDC_DATA — 13

TVOUT DISABLE

=PP1V5_S0_NB — 19 6
PP3V3_S0_NB_VCCA_TVDACA — 17
PP3V3_S0_NB_VCCA_TVDACB — 17
PP3V3_S0_NB_VCCA_TVDACC — 17
PP3V3_S0_NB_VCCA_TVBG — 17
TV_DACA_OUT (IN) — 13
TV_DACB_OUT (IN) — 13
TV_DACC_OUT (IN) — 13
TV_IREF (IN) — 13
TV_IRTNA (IN) — 13
TV_IRTNB (IN) — 13
TV_IRTNC (IN) — 13

GND_NB_VSSA_TVBG — 17

=PP1V5_S0_NB_TVDAC — 19 6
PP1V5_S0_NB_VCCD_TVDAC — 17
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
PP1V5_S0_NB_VCCD_QTVDAC — 17

Layout Note:
THESE 2 CAPS SHOULD BE
within 6.35 mm of NB edge

SDVO_CTRLCLK (IN) — 14 — TP_SDVO_CTRLCLK
SDVO_CTRLDATA (IN) — 14 — TP_SDVO_CTRLDATA

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	19	110

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 6 14 19 20
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 6 14 19 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 6 14 19 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

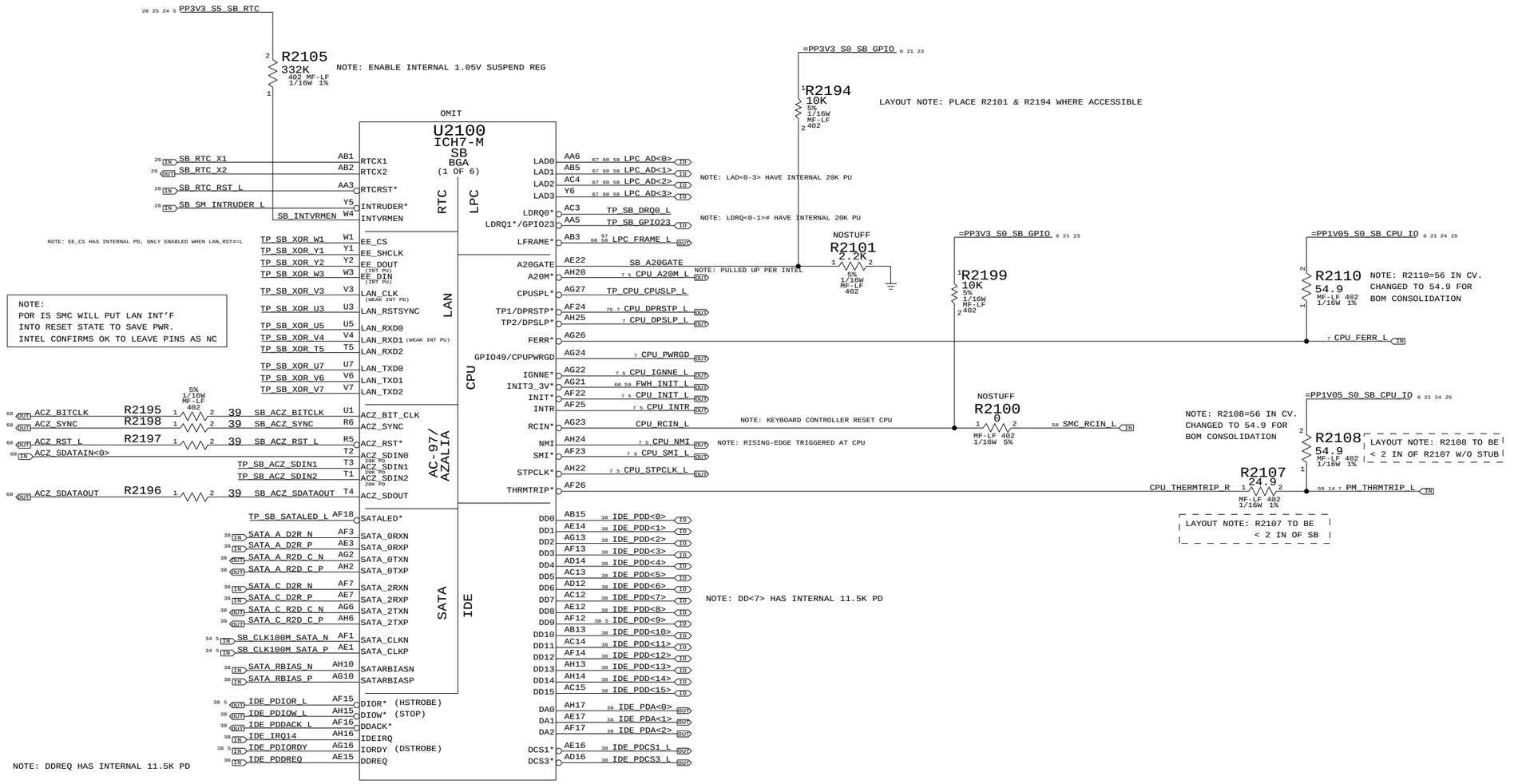
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT: 20	OF: 110



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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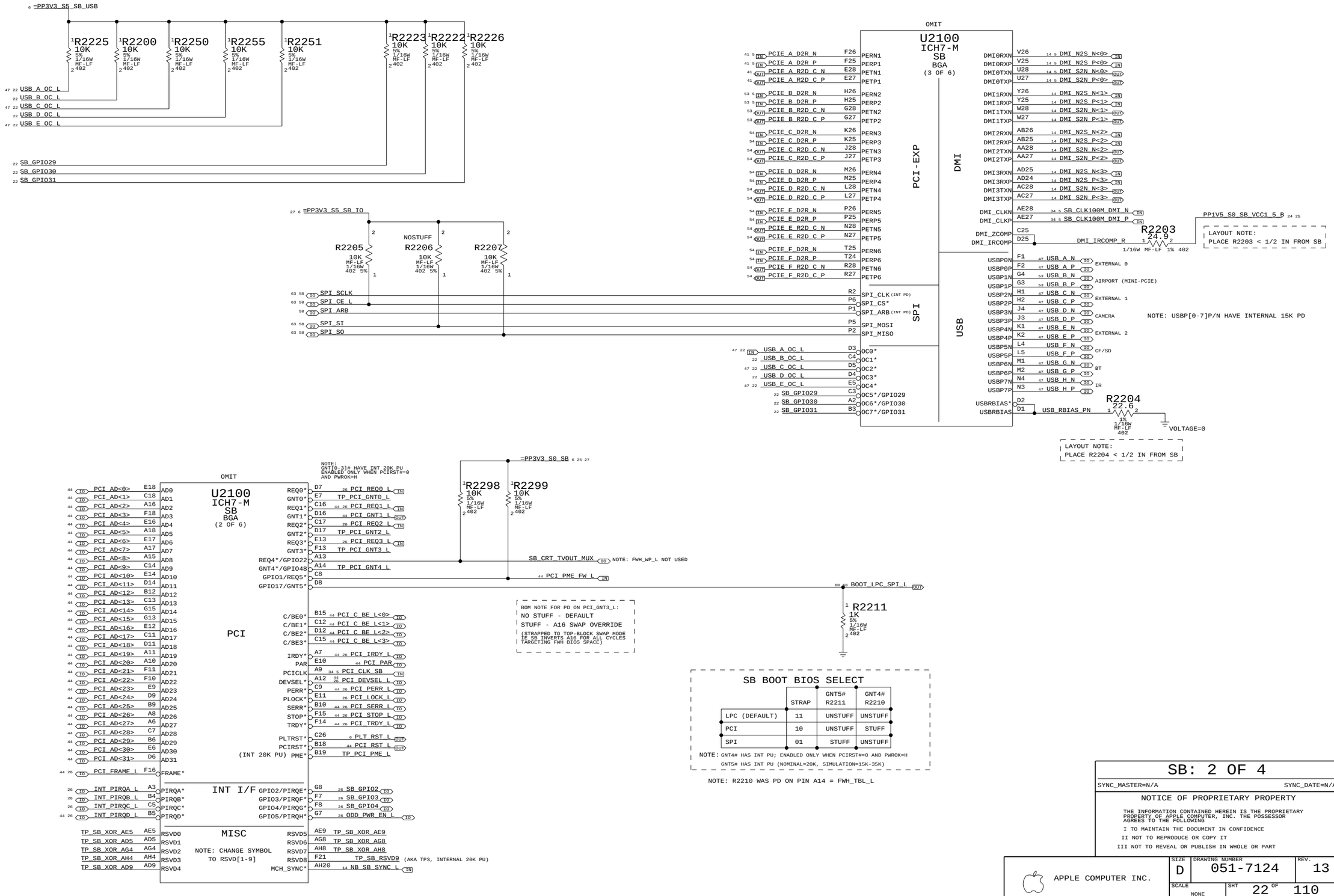
SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 21 OF 110	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2222 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCI-EXP
PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N E28
PCIE_A_R2D_C_P E27
PCIE_B_D2R_N H26
PCIE_B_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_C_D2R_N K26
PCIE_C_D2R_P K25
PCIE_C_R2D_C_N J28
PCIE_C_R2D_C_P J27
PCIE_D_D2R_N M26
PCIE_D_D2R_P M25
PCIE_D_R2D_C_N L28
PCIE_D_R2D_C_P L27
PCIE_E_D2R_N P26
PCIE_E_D2R_P P25
PCIE_E_R2D_C_N N28
PCIE_E_R2D_C_P N27
PCIE_F_D2R_N T25
PCIE_F_D2R_P T24
PCIE_F_R2D_C_N R28
PCIE_F_R2D_C_P R27
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
DMI
DMI0RXN V26
DMI0RXP V25
DMI0TXN U28
DMI0TXP U27
DMI1RXN Y26
DMI1RXP Y25
DMI1TXN W28
DMI1TXP W27
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA28
DMI2TXP AA27
DMI3RXN AD25
DMI3RXP AD24
DMI3TXN AC28
DMI3TXP AC27
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_CLKN AE28
DMI_CLKP AE27
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_ZCOMP C25
DMI_IRCOMP D25
DMI_IRCOMP_R
R2203 24.9 1% 1/16W MF-LF 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N F1
USBP0P F2
USBP1N G4
USBP1P G3
USBP2N H1
USBP2P H2
USBP3N J4
USBP3P J3
USBP4N K1
USBP4P K2
USBP5N L4
USBP5P L5
USBP6N M1
USBP6P M2
USBP7N N4
USBP7P N3
USB_A_N
USB_A_P
USB_B_N
USB_B_P
USB_C_N
USB_C_P
USB_D_N
USB_D_P
USB_E_N
USB_E_P
USB_F_N
USB_F_P
USB_G_N
USB_G_P
USB_H_N
USB_H_P
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
USBRBIAS* D2
USBRBIAS D1
USB_RBIAS_PN
R2204 22.6 1% 1/16W MF-LF 402
VOLTAGE=0
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
SPI
SPI_CLK (INT PD) R2
SPI_CS* P6
SPI_ARB (INT PD) P1
SPI_MOSI P5
SPI_MISO P2
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
=PP3V3_S5_SB_IO
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
USB_A_OC_L D3
USB_B_OC_L C4
USB_C_OC_L D5
USB_D_OC_L D4
USB_E_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
SB_GPIO31 B3
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
OMIT
U2100
ICH7-M
SB
BGA
(2 OF 6)
PCI
PCI_AD<0> E18
PCI_AD<1> C18
PCI_AD<2> A16
PCI_AD<3> F18
PCI_AD<4> E16
PCI_AD<5> A18
PCI_AD<6> E17
PCI_AD<7> A17
PCI_AD<8> A15
PCI_AD<9> C14
PCI_AD<10> E14
PCI_AD<11> D14
PCI_AD<12> B12
PCI_AD<13> C13
PCI_AD<14> G15
PCI_AD<15> G13
PCI_AD<16> E12
PCI_AD<17> C11
PCI_AD<18> D11
PCI_AD<19> A11
PCI_AD<20> A10
PCI_AD<21> F11
PCI_AD<22> F10
PCI_AD<23> E9
PCI_AD<24> D9
PCI_AD<25> B9
PCI_AD<26> A8
PCI_AD<27> A6
PCI_AD<28> C7
PCI_AD<29> B6
PCI_AD<30> E6
PCI_AD<31> D6
PCI_FRAME_L F16
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
FRAME*
REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 TP_PCI_GNT3_L
REQ4*/GPIO22 A13
GNT4*/GPIO48 A14 TP_PCI_GNT4_L
GPIO1/REQ5* C8 PCI_PME_FW_L
GPIO17/GNT5* D8 BOOT_LPC_SPI_L
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IE SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY_L
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL_L
PERR* C9 PCI_PERR_L
PLOCK* E11 PCI_LOCK_L
SERR* B10 PCI_SERR_L
STOP* F15 PCI_STOP_L
TRDY* F14 PCI_TRDY_L
PLTRST* C26 PLT_RST_L
PCIRST* B18 PCI_RST_L
(INT 20K PU) PME* B19 TP_PCI_PME_L
INT I/F
PIRQA* INT_PIRQA_L A3
PIRQB* INT_PIRQB_L B4
PIRQC* INT_PIRQC_L C5
PIRQD* INT_PIRQD_L B5
GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 ODD_PWR_EN_L
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
RSVD0 AE5 TP_SB_XOR_AE5
RSVD1 AD5 TP_SB_XOR_AD5
RSVD2 AG4 TP_SB_XOR_AG4
RSVD3 AH4 TP_SB_XOR_AH4
RSVD4 AD9 TP_SB_XOR_AD9
RSVD5 AE9 TP_SB_XOR_AE9
RSVD6 AG8 TP_SB_XOR_AG8
RSVD7 AH8 TP_SB_XOR_AH8
RSVD8 F21 TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
MCH_SYNC* AH20 NB_SB_SYNC_L
SB BOOT BIOS SELECT
STRAP | GNT5# R2211 | GNT4# R2210
LPC (DEFAULT) | 11 | UNSTUFF | UNSTUFF
PCI | 10 | UNSTUFF | STUFF
SPI | 01 | STUFF | UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
SYNC_MASTER=N/A
SYNC_DATE=N/A
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SIZE D
DRAWING NUMBER 051-7124
REV. 13
SCALE NONE
SHT 22 OF 110

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 6 21 23

=PP3V3_S5_SB 6 23 25 26

26 25 23 6 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 SMB_CLK → C22 SMBCLK
27 SMB_DATA → B22 SMBDATA
SMB_LINK_ALERT_L → A26 LINKALERT*
SMLINK<0> → B25 SMLINK0
SMLINK<1> → A25 SMLINK1
NOT USED
PM_RI_L → A28 RI*
SB_SPKR → A19 SPKR (INT WEAK PD)
67 60 58 PM_SUS_STAT_L → A27 SUS_STAT*
58 26 5 PM_SYSRST_L → A22 SYS_RST*
14 PM_BMBUSY_L → AB18 GPIO0/BM_BUSY*
SMB_ALERT_L → B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
33 PM_STPPCI_L → AC20 GPIO18/STPPCI*
33 PM_STPCPU_L → AF21 GPIO20/STPCPU*
SB_GPIO26 → A21 GPIO26
23 BIOS_REC → B21 GPIO27
23 FWH_MFG_MODE → E23 GPIO28
67 60 58 44 5 PM_CLKRUN_L → AG18 GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L → AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L → U2 GPIO34/AZ_DOCK_RST*
53 41 PCIE_WAKE_L → F20 WAKE*
67 60 58 INT_SERIRQ → AH21 SERIRQ
58 10 PM_THRM_L → AF20 THRM*
26 VR_PWRGD_CK410 → AD22 VRMPWRGD
TP_SB_GPIO6 → AC21 GPIO6
AC18 GPIO7
58 SMC_RUNTIME_SCI_L → E21 GPIO8
58 SMC_EXTSMI_L

SATA GPIO
GPIO21/SATA0GP AF19 SB_GPIO21 100 R2302
GPIO19/SATA1GP AH18 SB_GPIO19 100 R2303
GPIO36/SATA2GP AH19
GPIO37/SATA3GP AE19 SB_GPIO37 100 R2305
38 SATA_C_DET_L

CLKS
CLK14 AC1 34 5 SB_CLK14P3M_TIMER
CLK48 B2 34 5 SB_CLK48M_USBCTLR
SUSCLK C20 59 SUS_CLK_SB

SYS GPIO
PWR MNGT
SLP_S3* B24 88 79 77 58 PM_SLP_S3_L
SLP_S4* D23 77 58 PM_SLP_S4_L
SLP_S5* F22 58 PM_SLP_S5_L
PWROK AA4 26 PM_SB_PWROK
GPIO16/DPRSLPVR AC22 75 14 PM_DPRSLPVR
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* C23 58 PM_PWRBTN_L
LAN_RST* C19 58 PM_LAN_ENABLE NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4

GPIO
GPIO9 E20 58 26 SMS_INT_L
GPIO10 A20 58 SMC_SB_NMI
DEF=GPI GPIO12 F19 23 PATA_PWR_EN_L
GPIO13 E19
DEF=GPI GPIO14 R4 38 IDE_RESET_L
GPIO15 E22 SV_SET_UP 23 60
GPIO24 R3 CRB_SV_DET 23
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 33 SB_CLK100M_SATA_OE_L
GPIO38 AD20 TP_SB_GPIO38
DEF=GPI GPIO39 AE20 23 SATA_C_PWR_EN_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 6 11

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L
58 PM_RSMRST_L
58 SMC_WAKE_SCI_L

R2399 100K 5% 1/16W 402 MF-LF

26 25 23 6 =PP3V3_S5_SB

R2306 10K 1/16W 402 MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 0 1/16W 402 MF-LF 5% NOSTUFF

SV_SET_UP 23 60
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 6 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 0 1/16W 402 MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 MF-LF 5% NOSTUFF

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 6 23 25 26

R2390 10K 5% 1/16W MF-LF 402
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 6 21 23

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L

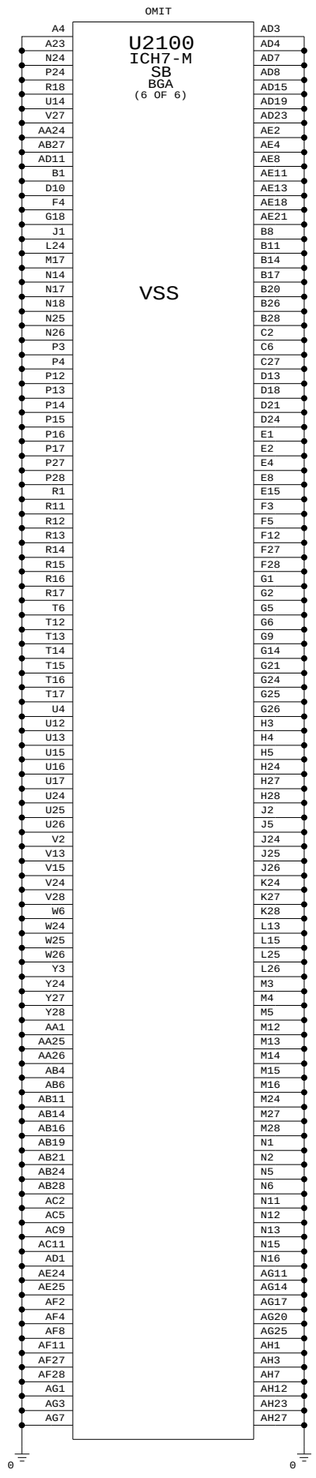
SB: 3 OF 4

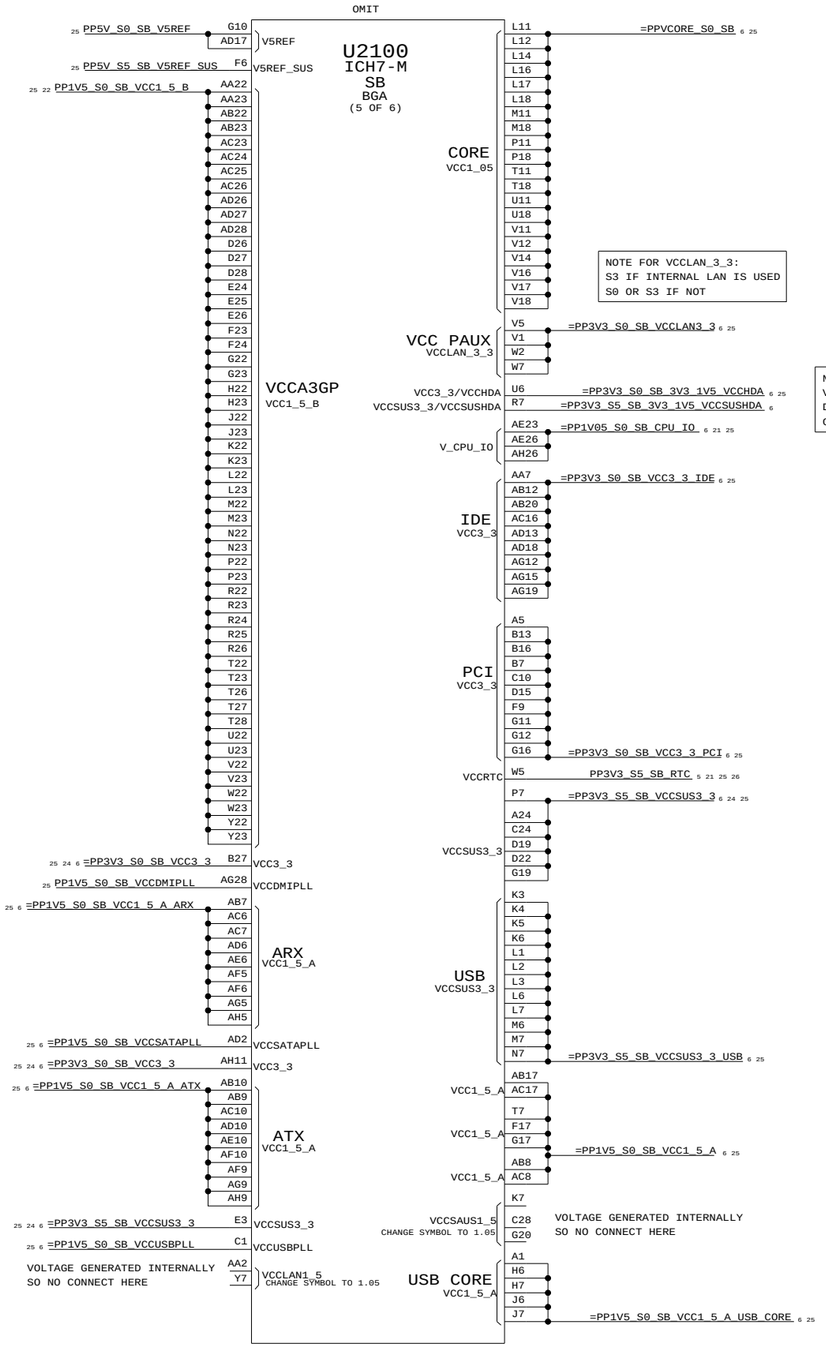
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT
NONE	23 OF 110





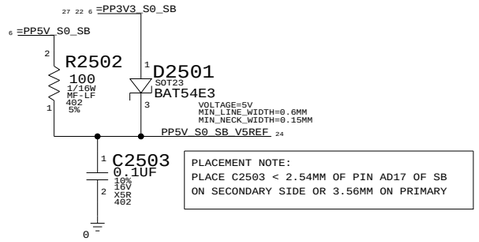
SB: 4 OF 4

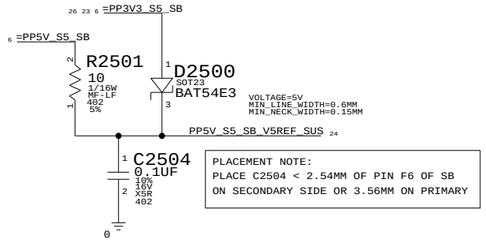
SYNC_MASTER=N/A SYNC_DATE=N/A

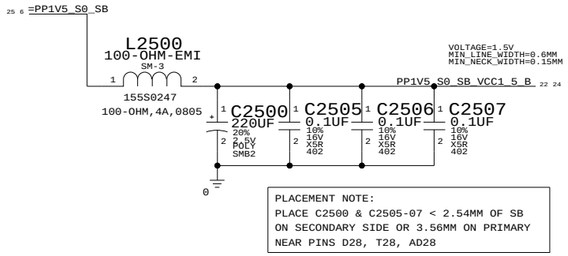
APPLE COMPUTER INC.

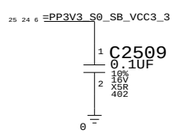
SIZE	DRAWING NUMBER	REV.
D	051-7124	13

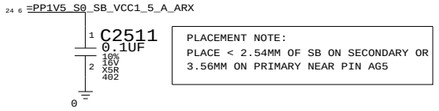
SCALE	SHT
NONE	24 OF 110

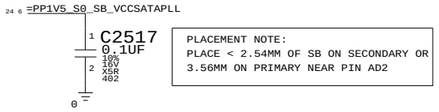


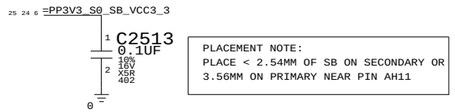


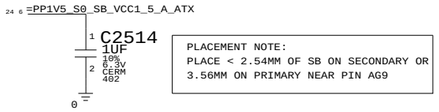


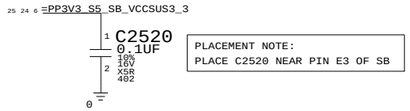


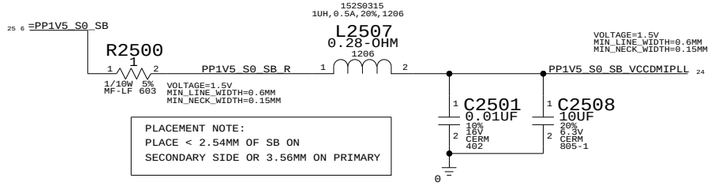


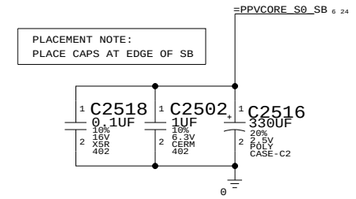


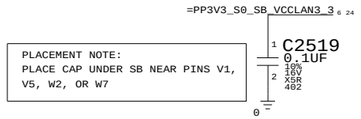


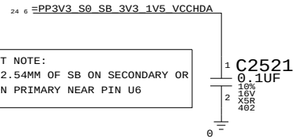


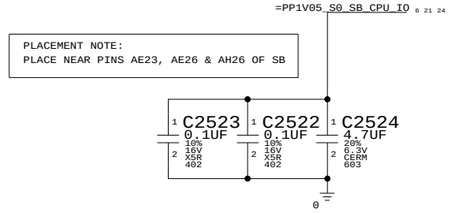


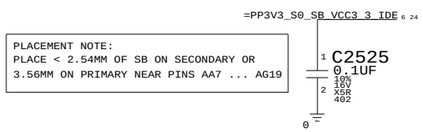


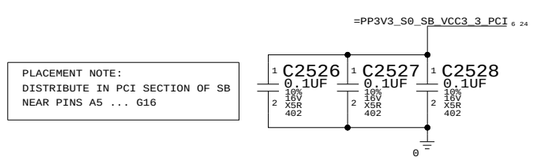


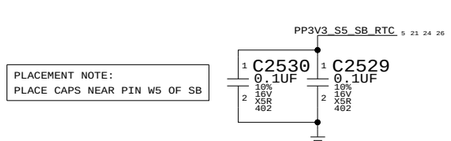


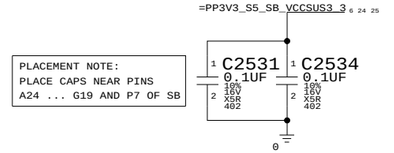


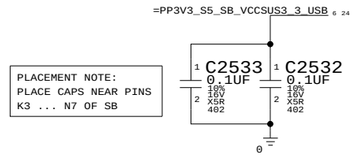


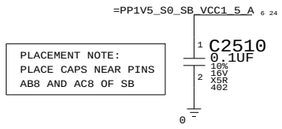


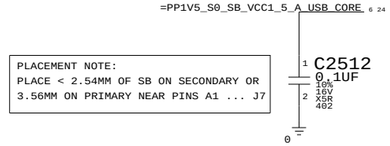










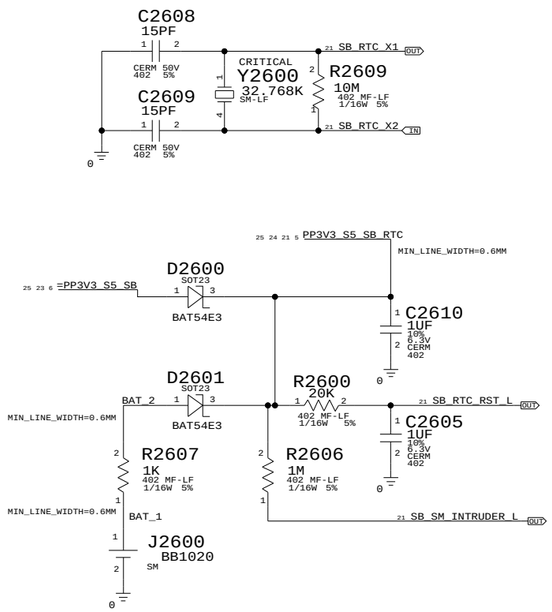


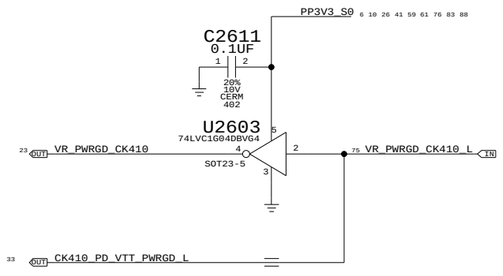
SB:DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 25 OF 110	





SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

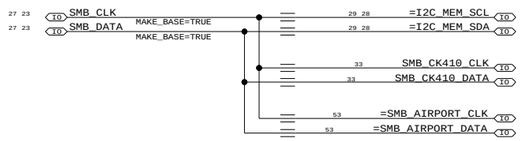
APPLE COMPUTER INC.

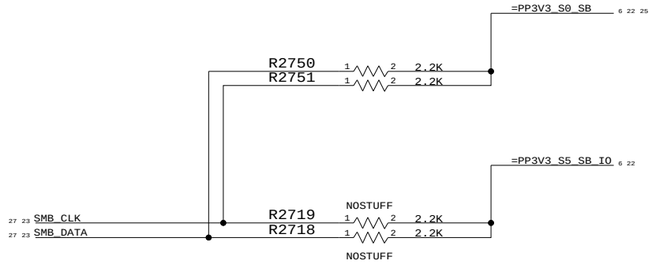
SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE

SHT 26 OF 110

SB I2C BUSSES





SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT
NONE	27 OF 110

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

29 28 6 5 =PP1V8_S3_MEM

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF 5 28 29
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

29 28 5 MEM_VREF

C2850 2.2UF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

29 28 6 5 =PP1V8_S3_MEM

CRITICAL
J2800
F-RT-SM1
DDR2-SODIMM-STD

	1	VREF			2	VSS0	
	3	VSS1			4	DQ4	MEM_A_DQ<4> 15
15	5	DQ0	MEM_A_DQ<0>		6	DQ5	MEM_A_DQ<5> 15
15	7	DQ1	MEM_A_DQ<1>		8	VSS2	
	9	VSS4			10	DM0	MEM_A_DM<0> 15
15 5	11	DQS0*	MEM_A_DQS_N<0>		12	VSS5	
15 5	13	DQS0	MEM_A_DQS_P<0>		14	DQ6	MEM_A_DQ<6> 15
	15	VSS6			16	DQ7	MEM_A_DQ<7> 5 15
15	17	DQ2	MEM_A_DQ<2>		18	VSS7	
15	19	DQ3	MEM_A_DQ<3>		20	DQ12	MEM_A_DQ<12> 15
	21	VSS8			22	DQ13	MEM_A_DQ<13> 15
15	23	DQ8	MEM_A_DQ<8>		24	VSS9	
15	25	DQ9	MEM_A_DQ<9>		26	DM1	MEM_A_DM<1> 15
	27	VSS10			28	VSS11	
15 5	29	DQS1*	MEM_A_DQS_N<1>		30	CK0	MEM_CLK_P<0> 14
15 5	31	DQS1	MEM_A_DQS_P<1>		32	CK0*	MEM_CLK_N<0> 14
	33	VSS12			34	VSS13	
15	35	DQ10	MEM_A_DQ<10>		36	DQ14	MEM_A_DQ<14> 5 15
15	37	DQ11	MEM_A_DQ<11>		38	DQ15	MEM_A_DQ<15> 15
	39	VSS14			40	VSS15	
		KEY					
	41	VSS16			42	VSS17	
15 5	43	DQ16	MEM_A_DQ<16>		44	DQ20	MEM_A_DQ<20> 15
15	45	DQ17	MEM_A_DQ<17>		46	DQ21	MEM_A_DQ<21> 15
	47	VSS18			48	VSS19	
15 5	49	DQS2*	MEM_A_DQS_N<2>		50	NC0	DIMM_OVERTEMP_L 29 59
15 5	51	DQS2	MEM_A_DQS_P<2>		52	DM2	MEM_A_DM<2> 15
	53	VSS21			54	VSS22	
15	55	DQ18	MEM_A_DQ<18>		56	DQ22	MEM_A_DQ<22> 15
15	57	DQ19	MEM_A_DQ<19>		58	DQ23	MEM_A_DQ<23> 15
	59	VSS23			60	VSS24	
15	61	DQ24	MEM_A_DQ<24>		62	DQ28	MEM_A_DQ<28> 15
15 5	63	DQ25	MEM_A_DQ<25>		64	DQ29	MEM_A_DQ<29> 15
	65	VSS25			66	VSS26	
15	67	DM3	MEM_A_DM<3>		68	DQS3*	MEM_A_DQS_N<3> 5 15
NC	69	NC1			70	DQS3	MEM_A_DQS_P<3> 5 15
	71	VSS27			72	VSS28	
15	73	DQ26	MEM_A_DQ<26>		74	DQ30	MEM_A_DQ<30> 15
15	75	DQ27	MEM_A_DQ<27>		76	DQ31	MEM_A_DQ<31> 15
	77	VSS29			78	VSS30	
30 14	79	CKE0	MEM_CKE<0>		80	NC/CKE1	MEM_CKE<1> 14 30
	81	VDD0			82	VDD1	
NC	83	NC2			84	NC/A15	TP_MEM_A_A<15>
30 15	85	BA2	MEM_A_BS<2>		86	NC/A14	TP_MEM_A_A<14>
	87	VDD2			88	VDD3	
30 15	89	A12	MEM_A_A<12>		90	A11	MEM_A_A<11> 15 30
30 15	91	A9	MEM_A_A<9>		92	A7	MEM_A_A<7> 15 30
30 15	93	A8	MEM_A_A<8>		94	A6	MEM_A_A<6> 15 30
	95	VDD4			96	VDD5	
30 15	97	A5	MEM_A_A<5>		98	A4	MEM_A_A<4> 15 30
30 15	99	A3	MEM_A_A<3>		100	A2	MEM_A_A<2> 15 30
30 15	101	A1	MEM_A_A<1>		102	A0	MEM_A_A<0> 15 30
	103	VDD6			104	VDD7	
30 15	105	A10/AP	MEM_A_A<10>		106	BA1	MEM_A_BS<1> 15 30
30 15	107	BA0	MEM_A_BS<0>		108	RAS*	MEM_A_RAS_L 15 30
30 15	109	WE*	MEM_A_WE_L		110	S0*	MEM_CS_L<0> 14 30
	111	VDD8			112	VDD9	
30 15	113	CAS*	MEM_A_CAS_L		114	ODT0	MEM_ODT<0> 14 30
30 14	115	NC/S1*	MEM_CS_L<1>		116	NC/A13	MEM_A_A<13> 15 30
	117	VDD10			118	VDD11	
30 14	119	NC/ODT1	MEM_ODT<1>		120	NC3	NC
	121	VSS31			122	VSS32	
15	123	DQ32	MEM_A_DQ<32>		124	DQ36	MEM_A_DQ<36> 15
15	125	DQ33	MEM_A_DQ<33>		126	DQ37	MEM_A_DQ<37> 15
	127	VSS33			128	VSS34	
15 5	129	DQS4*	MEM_A_DQS_N<4>		130	DM4	MEM_A_DM<4> 15
15 5	131	DQS4	MEM_A_DQS_P<4>		132	VSS35	
	133	VSS36			134	DQ38	MEM_A_DQ<38> 15
15	135	DQ34	MEM_A_DQ<34>		136	DQ39	MEM_A_DQ<39> 5 15
15	137	DQ35	MEM_A_DQ<35>		138	VSS37	
	139	VSS38			140	DQ44	MEM_A_DQ<44> 15
15	141	DQ40	MEM_A_DQ<40>		142	DQ45	MEM_A_DQ<45> 15
15	143	DQ41	MEM_A_DQ<41>		144	VSS39	
	145	VSS40			146	DQS5*	MEM_A_DQS_N<5> 5 15
15	147	DM5	MEM_A_DM<5>		148	DQS5	MEM_A_DQS_P<5> 5 15
	149	VSS41			150	VSS42	
15	151	DQ42	MEM_A_DQ<42>		152	DQ46	MEM_A_DQ<46> 15
15	153	DQ43	MEM_A_DQ<43>		154	DQ47	MEM_A_DQ<47> 5 15
	155	VSS43			156	VSS44	
15	157	DQ48	MEM_A_DQ<48>		158	DQ52	MEM_A_DQ<52> 15
15	159	DQ49	MEM_A_DQ<49>		160	DQ53	MEM_A_DQ<53> 15
	161	VSS45			162	VSS46	
NC	163	NC_TEST			164	CK1	MEM_CLK_P<1> 14
	165	VSS47			166	CK1*	MEM_CLK_N<1> 14
15 5	167	DQS6*	MEM_A_DQS_N<6>		168	VSS48	
15 5	169	DQS6	MEM_A_DQS_P<6>		170	DM6	MEM_A_DM<6> 15
	171	VSS49			172	VSS50	
15	173	DQ50	MEM_A_DQ<50>		174	DQ54	MEM_A_DQ<54> 5 15
15	175	DQ51	MEM_A_DQ<51>		176	DQ55	MEM_A_DQ<55> 15
	177	VSS51			178	VSS52	
15	179	DQ56	MEM_A_DQ<56>		180	DQ60	MEM_A_DQ<60> 15
15	181	DQ57	MEM_A_DQ<57>		182	DQ61	MEM_A_DQ<61> 15
	183	VSS53			184	VSS54	
15	185	DM7	MEM_A_DM<7>		186	DQS7*	MEM_A_DQS_N<7> 5 15
	187	VSS55			188	DQS7	MEM_A_DQS_P<7> 5 15
15	189	DQ58	MEM_A_DQ<58>		190	VSS56	
15 5	191	DQ59	MEM_A_DQ<59>		192	DQ62	MEM_A_DQ<62> 15
	193	VSS57			194	DQ63	MEM_A_DQ<63> 15
29 27	195	SDA	=I2C_MEM_SDA		196	VSS58	
29 27	197	SCL	=I2C_MEM_SCL		198	SA0	
	199	VDDSPD		GND	200	SA1	ADDR=0xA0(WR)/0xA1(RD)
	201	202	203	204	205	ALL NC'S	

516S0403

29 6 =PPSPD_S0_MEM

C2851 2.2UF 20% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

DDR2 Bypass Caps

(For return current)

29 28 6 5 =PP1V8_S3_MEM

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT: 28	OF: 110

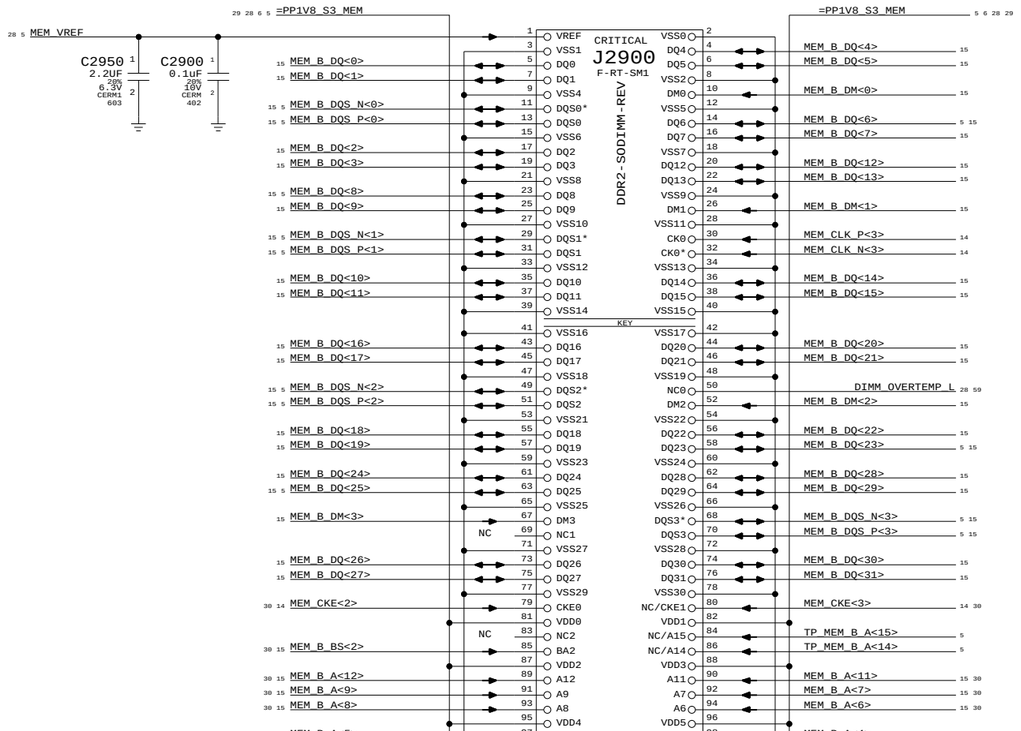
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

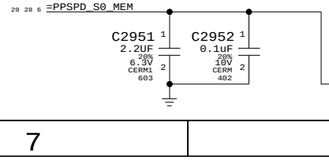
BOM options provided by this page:
(NONE)

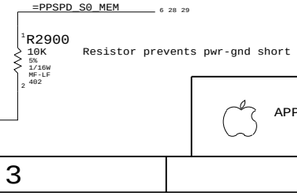
NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)





Resistor prevents pwr-gnd short

DDR2 SO-DIMM Connector B

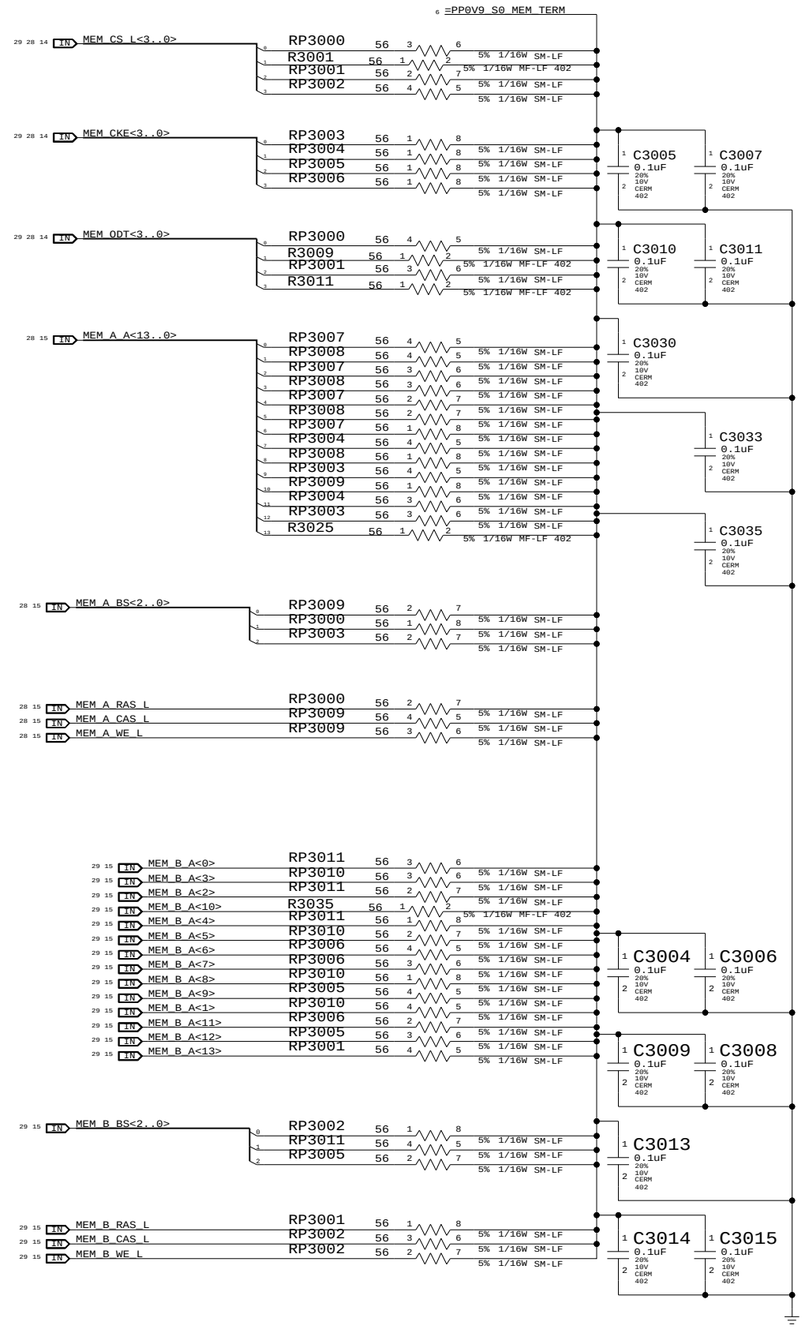
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	29	110

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	30	110

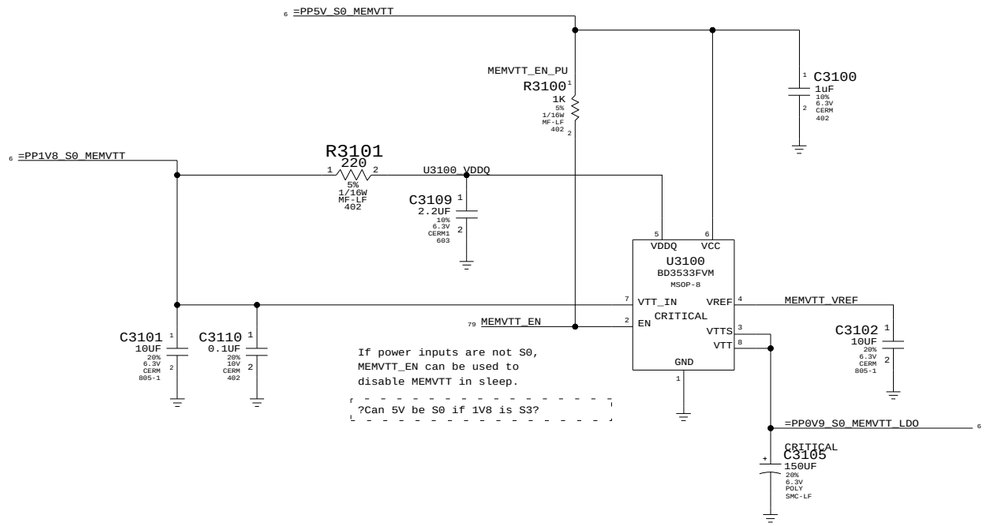
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



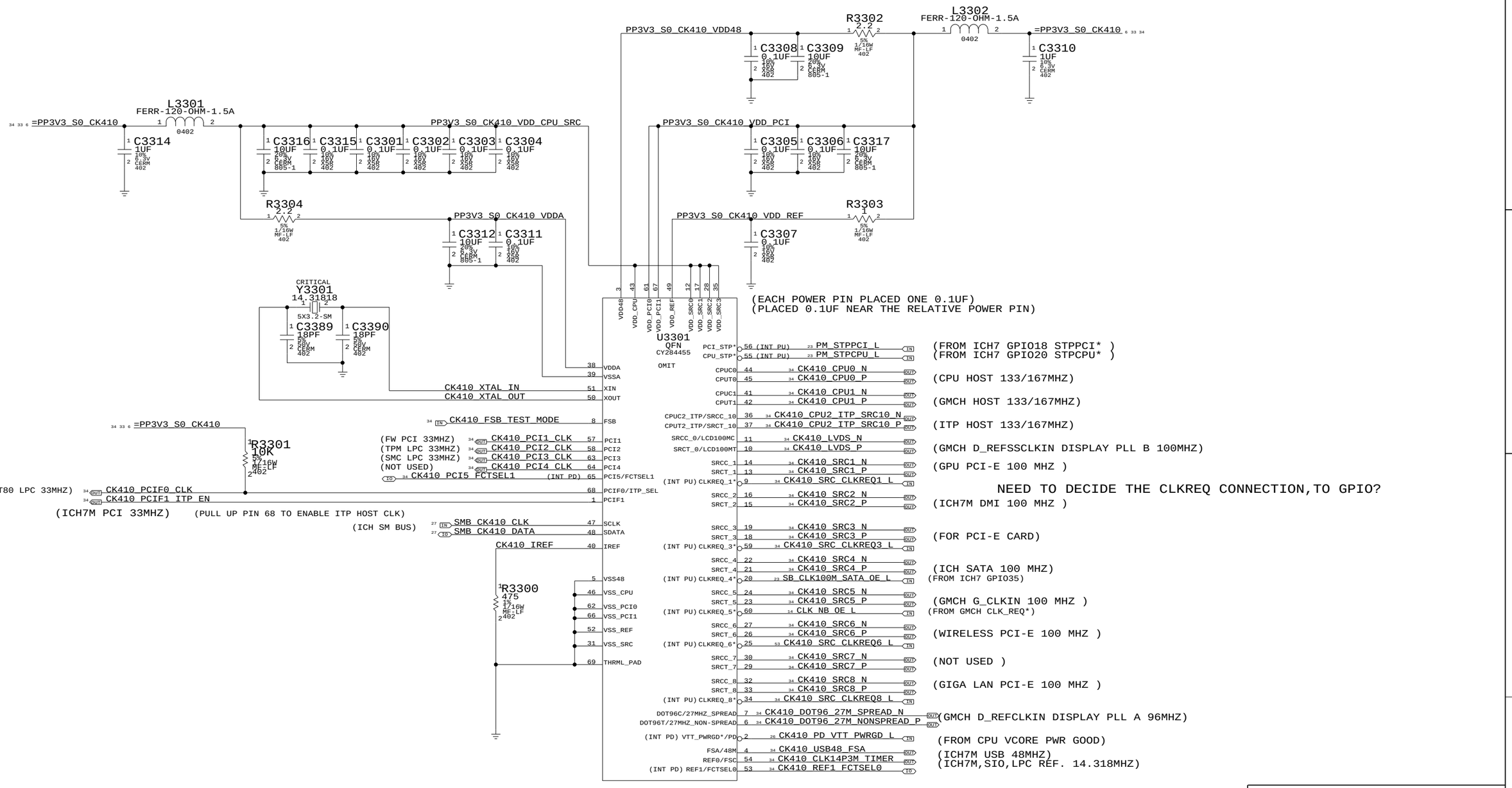
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	31	110



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE SHT 33 OF 110

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) R3495 1K
33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) R3494 1K
33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) R3493 1K

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

81 34 6 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402
14 NB_BSEL<0>
34 CK410_FSA
R3455 1K 1/16W 5% MF-LF 402
7 CPU_BSEL<0>

NOSTUFF R3452 56 5% 1/16W MF-LF 402
R3454 0 5% 1/16W MF-LF 402

81 34 6 PP1V05_S0

R3458 1K 1/16W 5% MF-LF 402
14 NB_BSEL<1>
33 CK410_FSB_TEST_MODE
7 CPU_BSEL<1>

R3456 1K 5% 1/16W MF-LF 402
NOSTUFF R3457 0 5% 1/16W MF-LF 402
R3459 0 5% 1/16W MF-LF 402

81 34 6 PP1V05_S0

R3462 1K 1/16W 5% MF-LF 402
14 NB_BSEL<2>
34 CK410_FSC
7 CPU_BSEL<2>

R3460 1K 5% 1/16W MF-LF 402
NOSTUFF R3461 0 5% 1/16W MF-LF 402
R3463 0 5% 1/16W MF-LF 402

=PP3V3_S0_CK410 6 33

33 IO CK410_PCI5_FCTSEL1 R3499 1K 1/16W 5% MF-LF 402

R3497 2.2K 5% 1/16W MF-LF 402 CK410_FSC 34

33 IN CK410_CLK14P3M_TIMER R3498 33 1/16W 5% MF-LF 402 SB_CLK14P3M_TIMER OUT 5 23

33 IN CK410_REF1_FCTSEL0 R3496 33 TP_CLK14P3M_SPARE OUT

R3451 2.2K 5% 1/16W MF-LF 402 CK410_FSA 34

33 IN CK410_USB48_FSA R3400 33 1/16W 5% MF-LF 402 SB_CLK48M_USBCTLR OUT 5 23
33 IN CK410_PCI4_CLK R3406 33 TP_PCI_CLK_SPARE OUT 9
33 IN CK410_PCI3_CLK R3405 33 PCI_CLK_SMC OUT 58
33 IN CK410_PCI2_CLK R3404 33 PCI_CLK_TPM OUT 67
33 IN CK410_PCI1_CLK R3403 33 PCI_CLK_FW OUT 44
33 IN CK410_PCIF1_ITP_EN R3401 33 PCI_CLK_SB OUT 5 22
33 IN CK410_PCIF0_CLK R3402 33 PCI_CLK_PORT80 OUT 60

33 IN CK410_CPU1_P R3407 33
33 IN CK410_CPU1_N R3408 33 FSB_CLK_NB_P OUT 5 12 34 / FSB_CLK_NB_N OUT 5 12 34
33 IN CK410_CPU0_P R3409 33
33 IN CK410_CPU0_N R3410 33 FSB_CLK_CPU_P OUT 5 7 34 / FSB_CLK_CPU_N OUT 5 7 34
33 IN CK410_CPU2_ITP_SRC10_P R3411 33
33 IN CK410_CPU2_ITP_SRC10_N R3412 33 MAKE_BASE=TRUE
34 FSB_CLK_XDP_P — CPU_XDP_CLK_P 11
34 FSB_CLK_XDP_N — CPU_XDP_CLK_N 11

33 IN CK410_SRC6_P R3413 33 AIRPORT_CLK100M_PCIE_P OUT 34 53
33 IN CK410_SRC6_N R3414 33 AIRPORT_CLK100M_PCIE_N OUT 34 53
33 IN CK410_SRC5_P R3415 33 NB_CLK100M_GCLKIN_P OUT 5 14 34
33 IN CK410_SRC5_N R3416 33 NB_CLK100M_GCLKIN_N OUT 5 14 34
33 IN CK410_SRC4_P R3417 33 SB_CLK100M_SATA_P OUT 5 21 34
33 IN CK410_SRC4_N R3418 33 SB_CLK100M_SATA_N OUT 5 21 34
33 IN CK410_SRC2_P R3419 33 SB_CLK100M_DMI_P OUT 5 22 34
33 IN CK410_SRC2_N R3420 33 SB_CLK100M_DMI_N OUT 5 22 34
33 IN CK410_SRC8_P R3421 33 ENET_CLK100M_PCIE_P OUT 5 34 41
33 IN CK410_SRC8_N R3422 33 ENET_CLK100M_PCIE_N OUT 5 34 41
33 IN CK410_SRC1_P R3423 33 GPU_CLK100M_PCIE_P OUT 5 34 84
33 IN CK410_SRC1_N R3424 33 GPU_CLK100M_PCIE_N OUT 5 34 84
33 IN CK410_LVDS_P — TP_CK410_LVDS_P
33 IN CK410_LVDS_N — TP_CK410_LVDS_N

33 IN CK410_DOT96_27M_SPREAD_N R3470 33 CK410_27M_SPREAD OUT 92
33 IN CK410_DOT96_27M_NONSPREAD_P R3471 33 CK410_27M_NONSPREAD OUT 92

33 IN CK410_SRC3_P R3492 33 SPARE_SRC3_P R3488 49.9
33 IN CK410_SRC3_N R3491 33 SPARE_SRC3_N R3487 49.9
33 IN CK410_SRC7_P R3490 33 SPARE_SRC7_P R3486 49.9
33 IN CK410_SRC7_N R3489 33 SPARE_SRC7_N R3485 49.9

1% 402 1/16W MF-LF

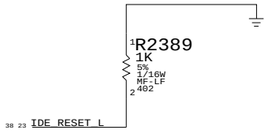
34 12 5 FSB_CLK_NB_P R3429 49.9
34 12 5 FSB_CLK_NB_N R3430 49.9
34 7 5 FSB_CLK_CPU_P R3431 49.9
34 7 5 FSB_CLK_CPU_N R3432 49.9
34 FSB_CLK_XDP_P R3433 49.9
34 FSB_CLK_XDP_N R3434 49.9
53 34 AIRPORT_CLK100M_PCIE_P R3435 49.9
53 34 AIRPORT_CLK100M_PCIE_N R3436 49.9
34 14 5 NB_CLK100M_GCLKIN_P R3438 49.9
34 14 5 NB_CLK100M_GCLKIN_N R3437 49.9
34 21 5 SB_CLK100M_SATA_P R3439 49.9
34 21 5 SB_CLK100M_SATA_N R3440 49.9
34 22 5 SB_CLK100M_DMI_P R3442 49.9
34 22 5 SB_CLK100M_DMI_N R3441 49.9
41 34 5 ENET_CLK100M_PCIE_P R3443 49.9
41 34 5 ENET_CLK100M_PCIE_N R3444 49.9
84 34 5 GPU_CLK100M_PCIE_P R3446 49.9
84 34 5 GPU_CLK100M_PCIE_N R3445 49.9

CLOCKS: TERMINATIONS

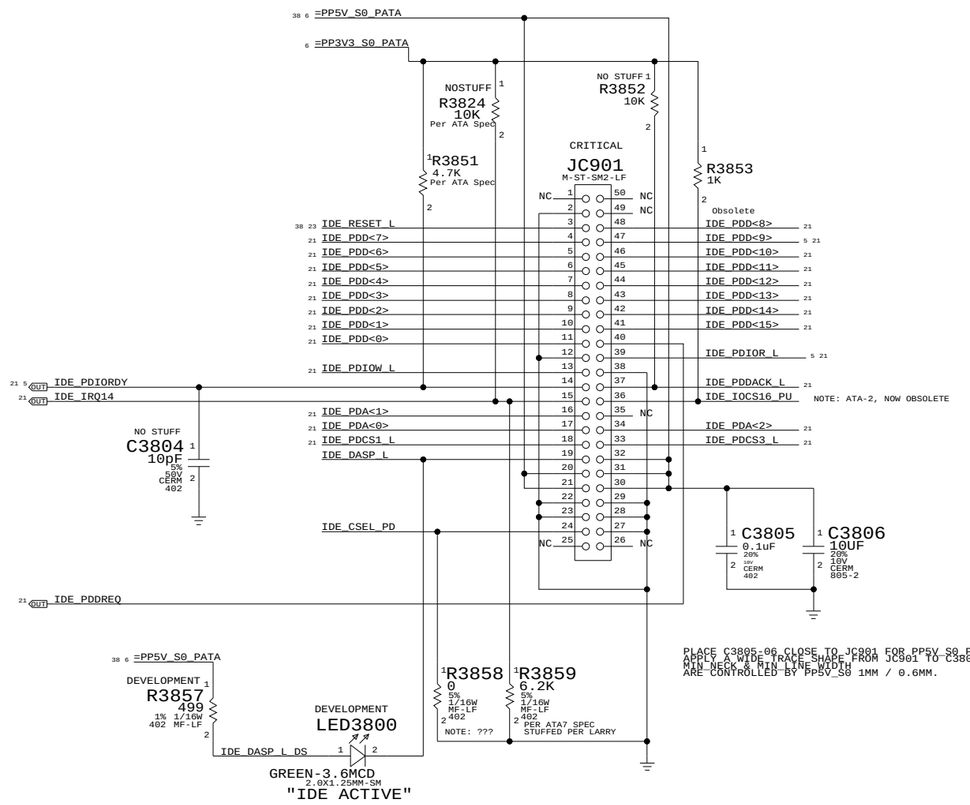
SYNC_MASTER=N/A SYNC_DATE=N/A

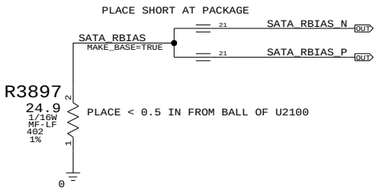
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 34 OF 110	

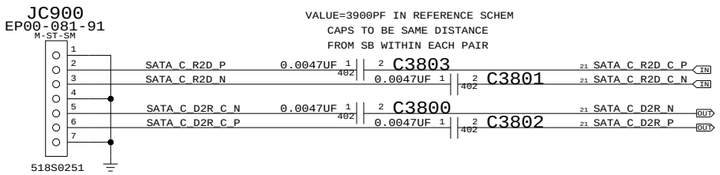


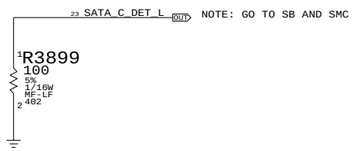
PATA CONNECTOR





SATA CONNECTOR

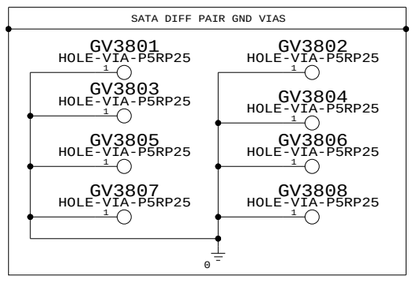




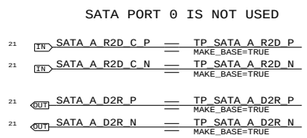
SMT NUTS FOR ODD ADAPTER

SDF3800
STDOFF-3.5OD1.35H-1.55-TH

SDF3801
STDOFF-3.5OD1.35H-1.55-TH



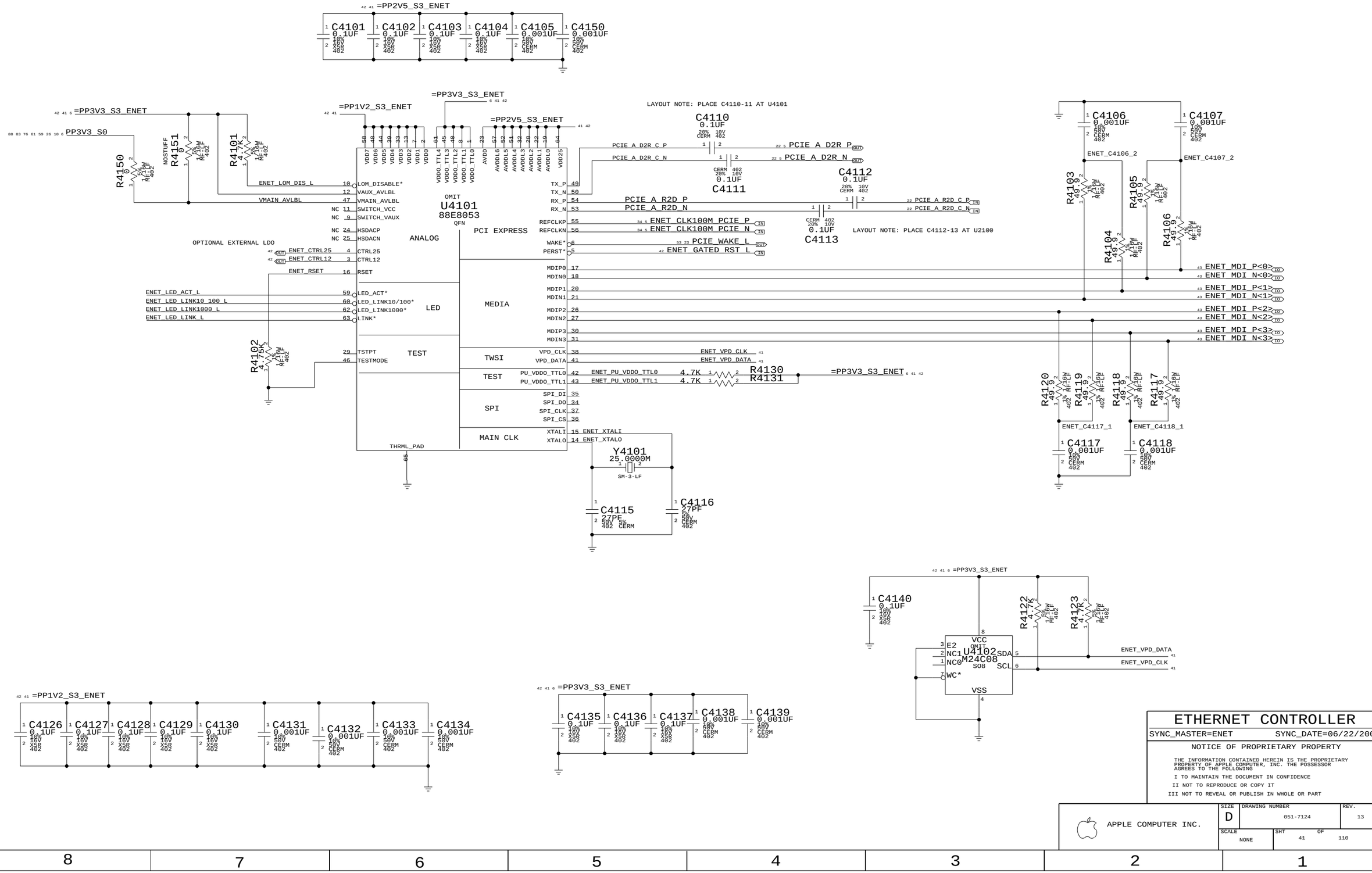
SATA PORT 0 IS NOT USED



Disk Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 38 OF 110	



ETHERNET CONTROLLER

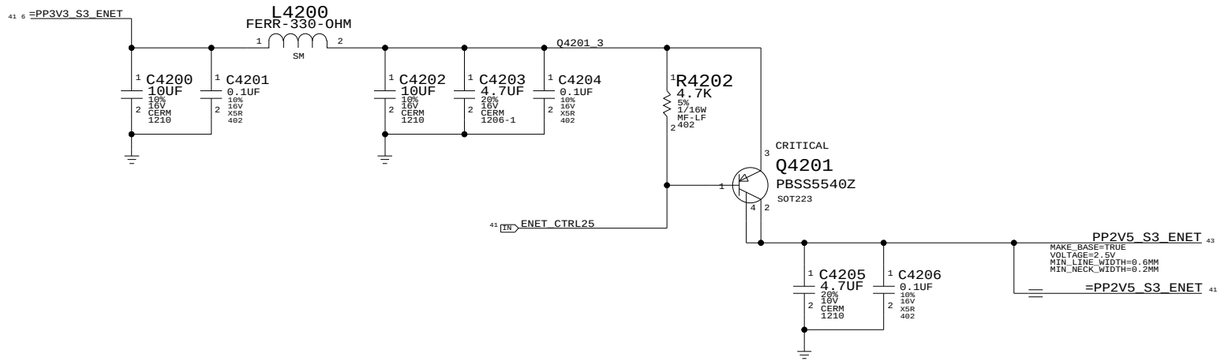
SYNC_MASTER=ENET SYNC_DATE=06/22/2005

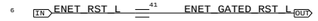
NOTICE OF PROPRIETARY PROPERTY

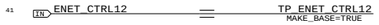
APPLE COMPUTER INC.

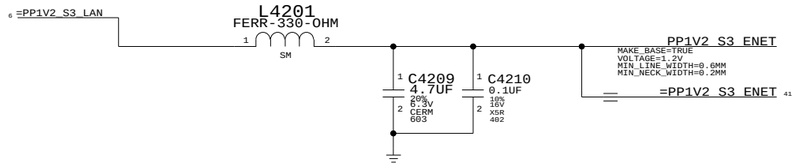
SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE SHT 41 OF 110





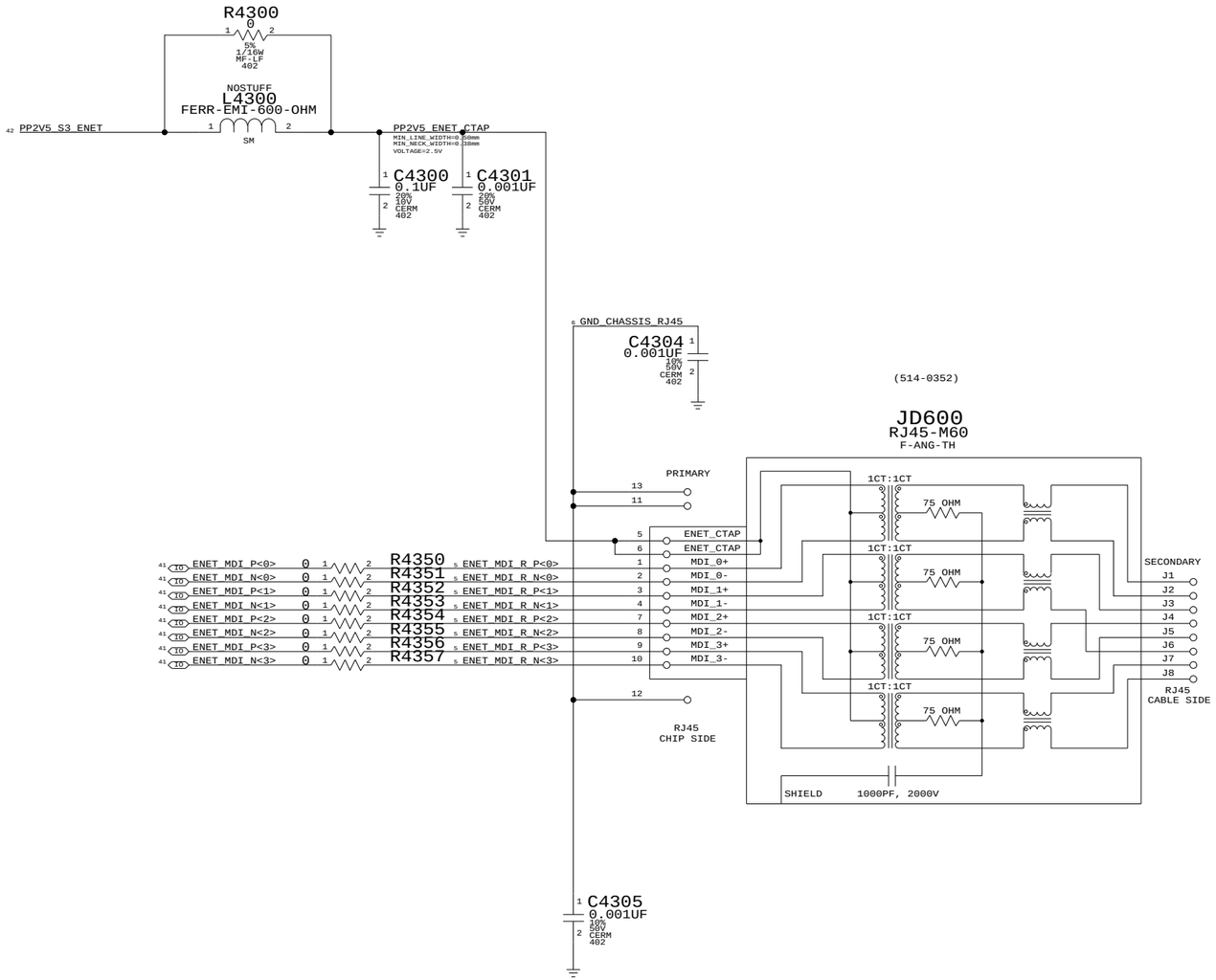




ETHERNET MISC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE	SHT	OF
NONE	42	110

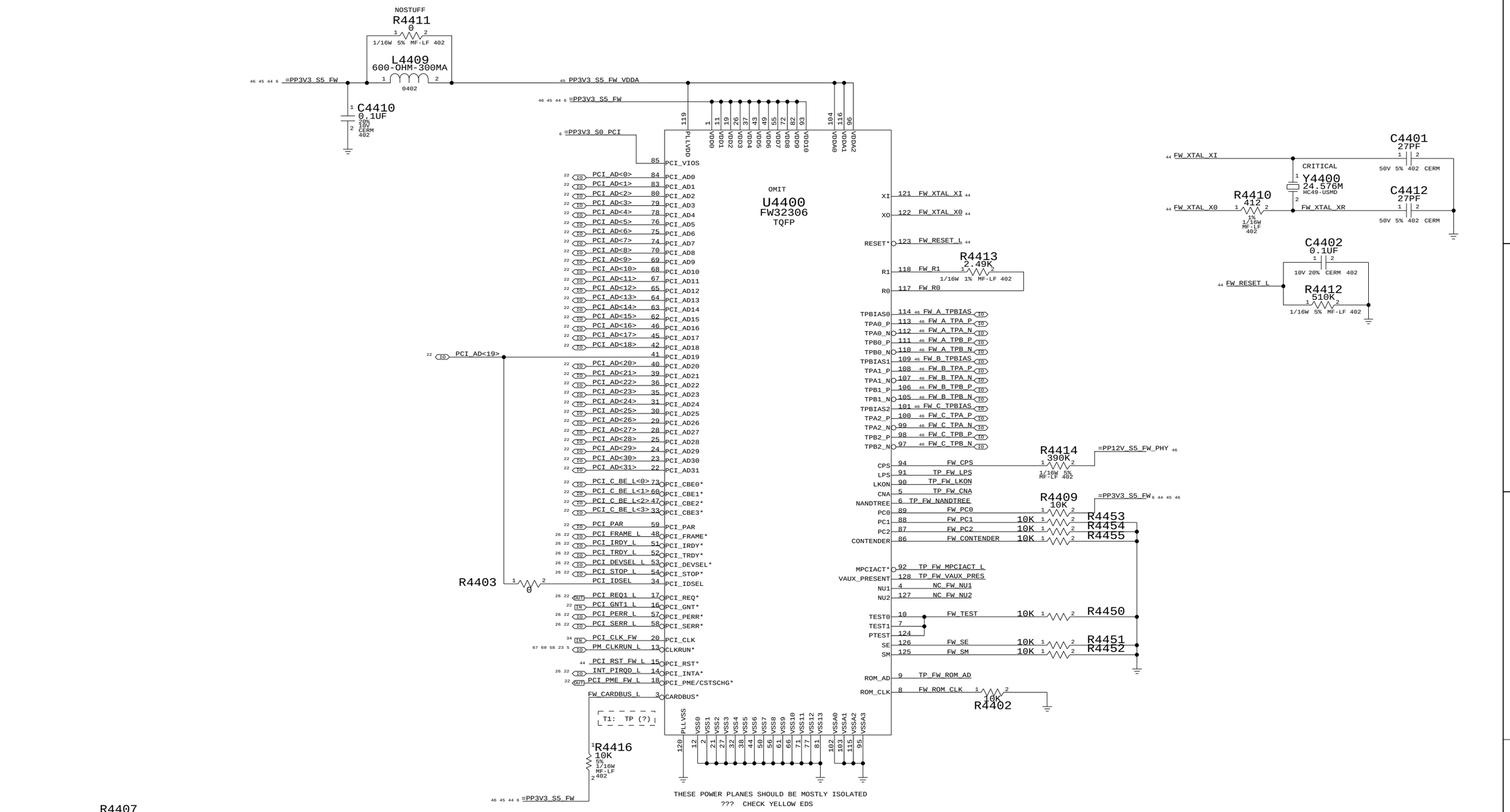


ETHERNET CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

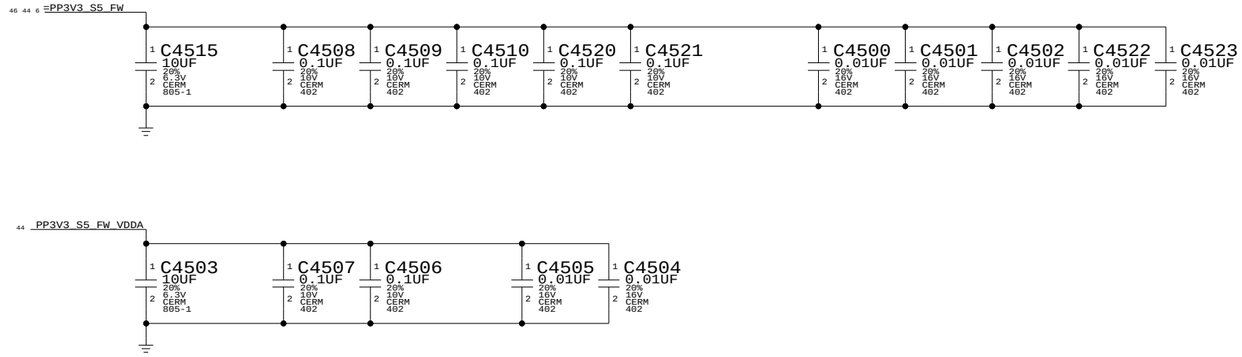
SCALE	SHT	OF
NONE	43	110



FW:	FW323-06
SYNC_MASTER=N/A	SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 44 OF 110	



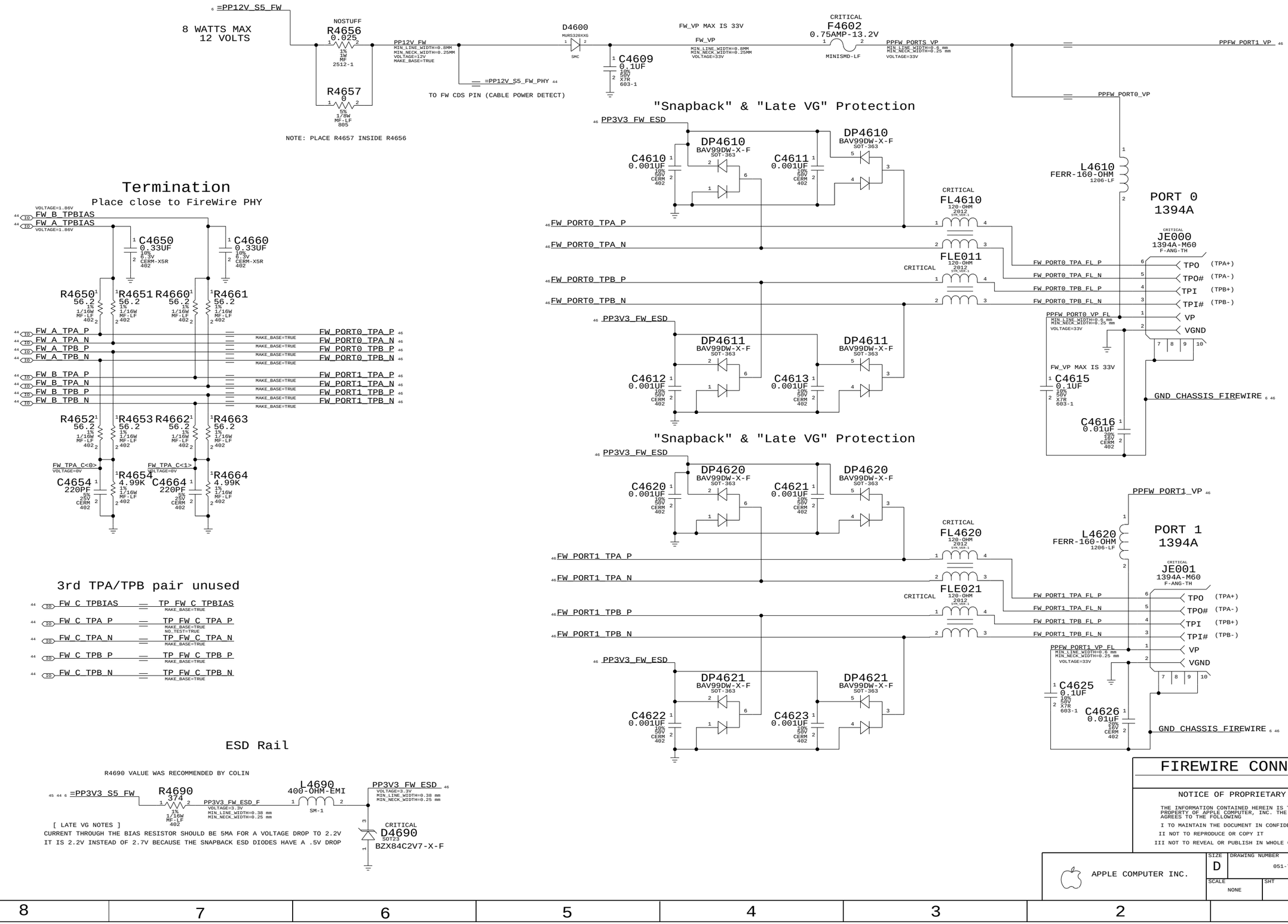
FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT
NONE	45 OF 110


=PP12V_S5_FW
8 WATTS MAX
12 VOLTS
NOSTUFF
R4656
0.025
1%
1W
MF
2512-1
R4657
0
5%
1/8W
MF-LF
805
NOTE: PLACE R4657 INSIDE R4656
PP12V_FW
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V
MAKE_BASE=TRUE
=PP12V_S5_FW_PHY
TO FW CDS PIN (CABLE POWER DETECT)
D4600
MURS320XXG
SMC
C4609
0.1UF
10%
50V
X7R
603-1
FW_VP MAX IS 33V
FW_VP
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V
CRITICAL
F4602
0.75AMP-13.2V
MINISMD-LF
PPFW_PORTS_VP
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
PPFW_PORT1_VP
PPFW_PORT0_VP
Termination
Place close to FireWire PHY
VOLTAGE=1.86V
FW_B_TPBIAS
FW_A_TPBIAS
C4650
0.33UF
10%
6.3V
CERM-X5R
402
C4660
0.33UF
10%
6.3V
CERM-X5R
402
R4650
56.2
1%
1/10W
MF-LF
402
R4651
56.2
1%
1/16W
MF-LF
402
R4660
56.2
1%
1/10W
MF-LF
402
R4661
56.2
1%
1/16W
MF-LF
402
FW_A_TPA_P
FW_A_TPA_N
FW_A_TPB_P
FW_A_TPB_N
FW_B_TPA_P
FW_B_TPA_N
FW_B_TPB_P
FW_B_TPB_N
MAKE_BASE=TRUE
FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N
FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N
R4652
56.2
1%
1/10W
MF-LF
402
R4653
56.2
1%
1/16W
MF-LF
402
R4662
56.2
1%
1/10W
MF-LF
402
R4663
56.2
1%
1/16W
MF-LF
402
FW_TPA_C<0>
VOLTAGE=0V
FW_TPA_C<1>
VOLTAGE=0V
C4654
220PF
5%
25V
CERM
402
R4654
4.99K
1%
1/16W
MF-LF
402
C4664
220PF
5%
25V
CERM
402
R4664
4.99K
1%
1/16W
MF-LF
402
3rd TPA/TPB pair unused
FW_C_TPBIAS
TP_FW_C_TPBIAS
FW_C_TPA_P
TP_FW_C_TPA_P
NO_TEST=TRUE
FW_C_TPA_N
TP_FW_C_TPA_N
FW_C_TPB_P
TP_FW_C_TPB_P
FW_C_TPB_N
TP_FW_C_TPB_N
ESD Rail
R4690 VALUE WAS RECOMMENDED BY COLIN
=PP3V3_S5_FW
R4690
374
1%
1/16W
MF-LF
402
PP3V3_FW_ESD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
L4690
400-OHM-EMI
SM-1
PP3V3_FW_ESD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
CRITICAL
D4690
SOT23
BZX84C2V7-X-F
[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP
"Snapback" & "Late VG" Protection
PP3V3_FW_ESD
DP4610
BAV99DW-X-F
SOT-363
C4610
0.001UF
10%
50V
CERM
402
C4611
0.001UF
10%
50V
CERM
402
CRITICAL
FL4610
120-OHM
2012
SYM_VER-1
FLE011
120-OHM
2012
SYM_VER-1
DP4611
BAV99DW-X-F
SOT-363
C4612
0.001UF
10%
50V
CERM
402
C4613
0.001UF
10%
50V
CERM
402
L4610
FERR-160-OHM
1206-LF
PORT 0
1394A
CRITICAL
JE000
1394A-M60
F-ANG-TH
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
PPFW_PORT0_VP_FL
C4615
0.1UF
10%
50V
X7R
603-1
C4616
0.01uF
20%
16V
CERM
402
GND_CHASSIS_FIREWIRE
"Snapback" & "Late VG" Protection
DP4620
BAV99DW-X-F
SOT-363
C4620
0.001UF
10%
50V
CERM
402
C4621
0.001UF
10%
50V
CERM
402
FL4620
120-OHM
2012
SYM_VER-1
FLE021
120-OHM
2012
SYM_VER-1
DP4621
BAV99DW-X-F
SOT-363
C4622
0.001UF
10%
50V
CERM
402
C4623
0.001UF
10%
50V
CERM
402
L4620
FERR-160-OHM
1206-LF
PORT 1
1394A
JE001
1394A-M60
F-ANG-TH
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
PPFW_PORT1_VP_FL
C4625
0.1UF
10%
50V
X7R
603-1
C4626
0.01uF
20%
16V
CERM
402
GND_CHASSIS_FIREWIRE
FIREWIRE CONNECTORS
NOTICE OF PROPRIETARY PROPERTY
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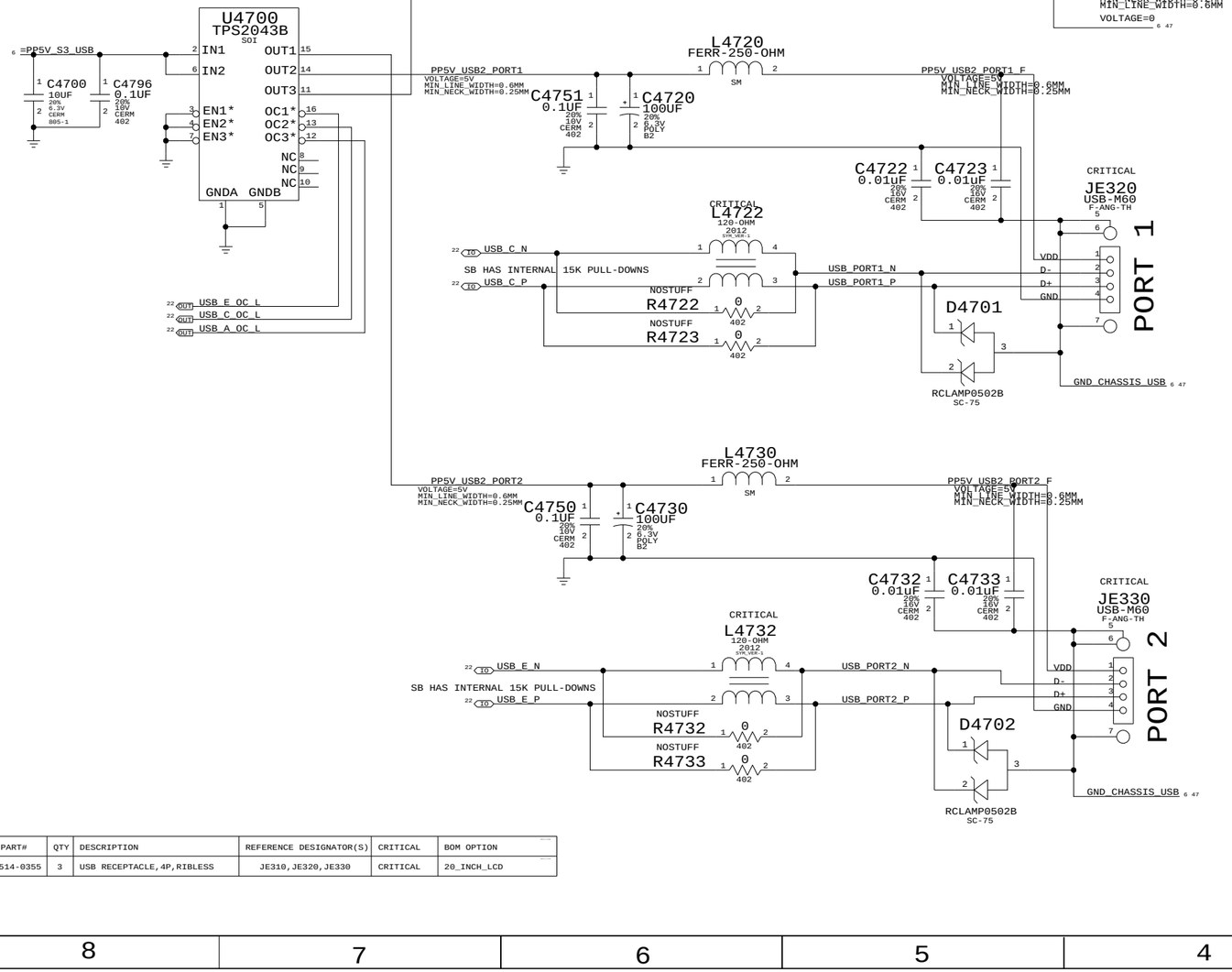
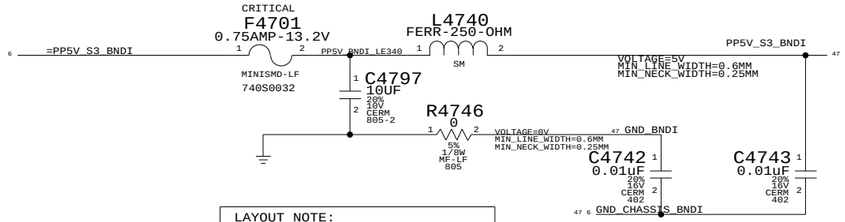
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7124
REV. 13
SCALE NONE
SHT 46 OF 110

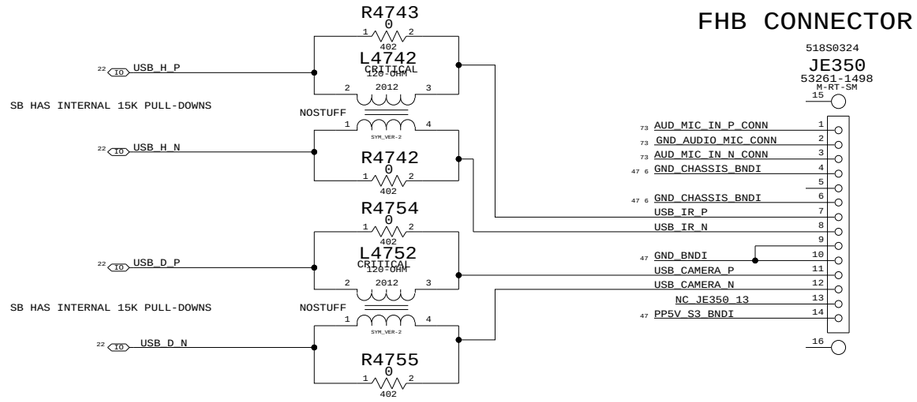
External USB Ports

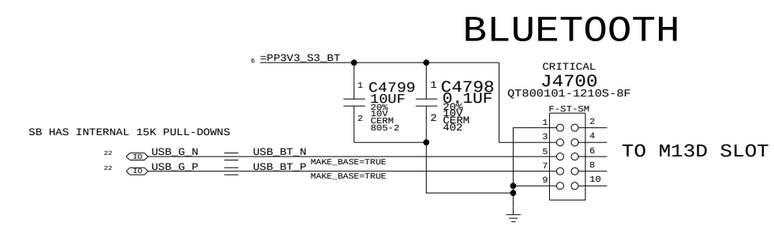




LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO JE350.





NOTE: STANDOFFS FOR J4700

SDF4700
STDOFF-40D4.5H-1.35-TH

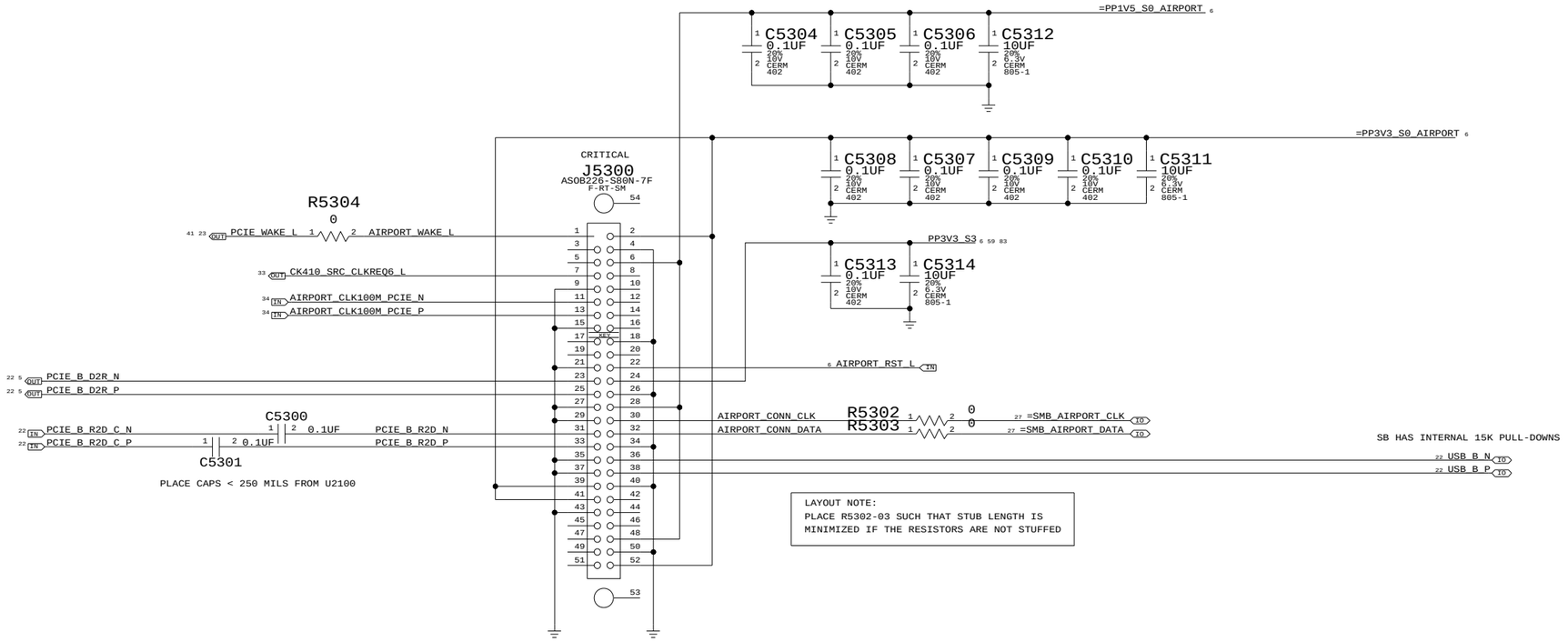
SDF4701
STDOFF-40D4.5H-1.35-TH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0355	3	USB RECEPTACLE,4P,RIBLESS	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

USB Device Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 47 OF 110	



AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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D	051-7124	13
SCALE: NONE	SHT 53 OF 110	

22 IN PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N — TP_PCIE_C_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_C_D2R_P — TP_PCIE_C_D2R_P MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N — TP_PCIE_D_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_D_D2R_P — TP_PCIE_D_D2R_P MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N — TP_PCIE_E_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_E_D2R_P — TP_PCIE_E_D2R_P MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N — TP_PCIE_F_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_F_D2R_P — TP_PCIE_F_D2R_P MAKE_BASE=TRUE

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE NONE SHT 54 OF 110

3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
NB=0.142A
MS5=0.745A
TOTAL=0.887A

3.3V S5
POWER BUDGET
3.3V S0=1.755A
MISC=2.470A
MS5=2.100A
3.3V S5=0.296A
TOTAL=5.686A

PP12V_S5
=PP3V3_S5_2V5_LDO
PP2V5_S5
2.50V NOMINAL
PP3V3_S5
3.35V NOMINAL
SYS_POWERFAIL_L

C5792 1UF 10% 25V X5R 603
C5700 1UF 10% 6.3V CERM 402
C5720 22UF 20% 6.3V X5R 805
C5723 1000PF 10% 25V X7R 402
C5724 1000PF 10% 25V X7R 402
C5725 10UF 20% 6.3V CERM 805-1
C5722 10UF 20% 6.3V CERM 805-1
C5721 10UF 20% 6.3V CERM 805-1
C5726 10UF 20% 6.3V CERM 805-1
C5753 10UF 10% 16V CERM 1210
C5711 10UF 10% 16V CERM 1210
C5799 10UF 10% 16V CERM 1210
C5798 10UF 10% 16V CERM 1210
C5797 10UF 10% 16V CERM 1210
C5715 1800UF 20% 6.3V ELEC TH-NZJ-LF
C5714 10UF 20% 6.3V CERM 805-1
C5713 10UF 20% 6.3V CERM 805-1
C5701 0.1UF 20% 25V CERM 603
C5702 1000PF 10% 25V X7R 402
C5706 560PF 10% 16V CERM 402
C5708 0.047UF 10% 16V CERM 402
C5709 1000PF 5% 50V CERM 1206
C5707 0.01UF 10% 16V CERM 402
C5703 4.7UF 20% 6.3V CERM 603

R5705 10 1% 1/16W MF-LF 402
R5720 1K 1% 1/16W MF-LF 402
R5721 2.7K 5% 1/16W MF-LF 402
R5722 470 1% 1/16W MF-LF 402
R5740 2.2 5% 1/16W MF-LF 402
R5704 8.06K 1% 1/16W MF-LF 402
R5702 5.11 1% 1/4W MF-LF 1206
R5799 22 5% 1/16W MF-LF 402
R5703 1.24K 1% 1/16W MF-LF 402 (R2)
R5701 392 1% 1/16W MF-LF 402 (R1)
R5792 39.2K 1% 1/16W MF-LF 402

L5703 3.3UH IHLP CRITICAL

U5700 ISL6549 QFN
VCC12
VCC5
PVCC5
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND
AGND PGND
UGATE
BOOT
PHASE
LGATE
FB
COMP

Q5703 IRF1902PBF SO-8 CRITICAL
Q5700 IRLR7807Z TO-252AA CRITICAL
Q5701 IRLR7807Z TO-252AA CRITICAL
Q5702 2N7002 SOT23-LF NOSTUFF
D5700 CTLSH3-30M833 TLM833 NOSTUFF

3V3REG_VCC5
3V3REG_PVCC5
3V3REG_LDO_DR
2V5_LDODR_C
3V3REG_LDO_FB
3V3REG_FS_DIS
3V3REG_UGATE
3V3REG_BOOT
3V3REG_BOOT_R
3V3REG_SWITCHNODE
3V3REG_LGATE
3V3REG_FB
3V3REG_COMP
3V3REG_COMP_R
3V3REG_SNUB
3V3REG_FB_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

3.3V DC/DC 2.5V

APPLE COMPUTER INC.

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D	051-7124	13
SCALE: NONE	SHT 57 OF 110	

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	
SMC_RSTGATE_L	C13	P11	
ALL_SYS_PWRGD	A15	P12	
RSMRST_PWRGD	B14	P13	
SMC_SB_NMI	B15	P14	
PM_RSMRST_L	C14	P15	
IMVP_VR_ON	D12	P16	
PM_PWRBTN_L	C15	P17	
SMC_P20	D13	P20	
SMC_P21	D14	P21	
SMC_P22	D15	P22	
SMC_P23	E12	P23	
SMC_BATT_TRICKLE_EN_L	E14	P24	
SMC_BATT_CHG_EN	E15	P25	
SMC_P26	E13	P26	
SMC_P27	F14	P27	
LPC_AD<0>	D9	P30/LAD0	
LPC_AD<1>	C9	P31/LAD1	
LPC_AD<2>	A9	P32/LAD2	
LPC_AD<3>	B9	P33/LAD3	
LPC_FRAME_L	D8	P34/LFRAME*	
SMC_LRESET_L	C8	P35/LRESET*	
PCI_CLK_SMC	A8	P36/LCLK	
INT_SERIRQ	D7	P37/SERIRQ	
SMC_XDP_TMS_L	A5	P40/TMI0	
SMC_SYS_LED_16B	B5	P41/TMO0	
SMB_BSB_DATA	D5	P42/SDA1	
SMC_TPM_PP	C3	P43/TMI1/EXSCKI	
SMC_XDP_TRST_L	B1	P44/TMO1	
SMC_XDP_TCK	C2	P45	
SMC_SYS_LED	D3	P46/PWX0/PWM0	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	
SMC_TX_L	G1	P50	
SMC_RX_L	G4	P51	
SMC_SMB_0_CLK	F2	P52/SCL0	
	L13	P60/KIN0*	SMC_PM_G2_EN
	L14	P61/KIN1*	SMC_ADAPTER_EN
	L15	P62/KIN2*	SPI_ARB
	K12	P63/KIN3*	SPI_SCLK
	K13	P64/KIN4*	SPI_SI
	K14	P65/KIN5*	SPI_SO
	J12	P66/IRQ6*/KIN6*	SMC_PROCHOT_3_3_L
	J13	P67/IRQ7*/KIN7*	SMC_CPU_INIT_3_3_L
	N12	P70/AN0	SMC_CPU_ISENSE
	R13	P71/AN1	SMC_CPU_VSENSE
	P13	P72/AN2	SMC_GPU_ISENSE
	R14	P73/AN3	SMC_GPU_VSENSE
	P14	P74/AN4	SMC_DCIN_ISENSE
	R15	P75/AN5	SMC_PBUS_VSENSE
	N13	P76/AN6	SMC_BATT_ISENSE
	P15	P77/AN7	SMC_FWIRE_ISENSE
	C7	P80/PME*	SMC_WAKE_SCI_L
	A7	P81/GA20	SMC_TPM_GPIO
	B7	P82/CLKRUN*	PM_CLKRUN_L
	D6	P83/LPCPD*	PM_SUS_STAT_L
	C6	P84/IRQ3*/TXD1	SC_TX_L
	A6	P85/IRQ4*/RXD1	SC_RX_L
	B6	P86/IRQ5*/SCK1/SCL1	SMB_BSB_CLK
	K4	P90/IRQ2*	SMC_ONOFF_L
	J2	P91/IRQ1*	SMC_BC_ACOK
	J1	P92/IRQ0*	SMC_BS_ALRT_L
	J3	P93/IRQ12*	PM_SLP_S3_L
	J4	P94/IRQ13*	PM_SLP_S4_L
	H2	P95/IRQ14*	PM_SLP_S5_L
	H1	P96/EXCL	SMC_SUS_CLK
	G2	P97/IRQ15*/SDA0	SMC_SMB_0_DATA

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	
SMC_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	
SMC_EXTSMI_L	B10	PB0/LSMI*	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	
SMC_ODD_DETECT	D10	PB2	
ISENSE_CAL_EN	A11	PB3	
SMC_EXCARD_CP	B11	PB4	
SMC_EXCARD_PWR_EN	C11	PB5	
SMC_EXCARD_PWR_OC_L	A12	PB6	
SMC_XDP_TDO_3_3_L	D11	PB7	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	
SMS_X_AXIS	M11	PD0/AN8	
SMS_Y_AXIS	P11	PD1/AN9	
SMS_Z_AXIS	R11	PD2/AN10	
SMC_ANALOG_ID	N11	PD3/AN11	
SMC_NB_ISENSE	P10	PD4/AN12	
SMC_MEM_ISENSE	R10	PD5/AN13	
ALS_LEFT	N10	PD6/AN14	
ALS_RIGHT	M10	PD7/AN15	
	M3	PE0	SMC_CASE_OPEN
	M2	PE1*/ETCK	SMC_TCK
	M1	PE2*/ETDI	SMC_TDI
	L4	PE3*/ETDO	SMC_TDO
	L2	PE4*/ETMS	SMC_TMS
	M7	PF0/IRQ8*/PWM2	SMC_PF0
	P6	PF1/IRQ9*/PWM3	SMC_PF1
	R6	PF2/IRQ10*/TMOY	SMC_LID
	N6	PF3/IRQ11*/TMOX	SMC_CPU_RESET_3_3_L
	M6	PF4/PWM4	SMC_BATT_ISET
	R5	PF5/PWM5	SMC_BATT_VSET
	P5	PF6/PWM6	SMC_SYS_ISET
	N5	PF7/PWM7	SMC_SYS_VSET
	P9	PG0/EXIRQ8*/TMIX	SPI_CE_L
	R9	PG1/EXIRQ9*/TMIY	SMC_XDP_TCK_3_3
	N9	PG2/EXIRQ10*/SDA2	SMB_BSA_DATA
	P8	PG3/EXIRQ11*/SCL2	SMB_BSA_CLK
	R8	PG4/EXIRQ12*/EXSDAA	SMB_A_S3_DATA
	M8	PG5/EXIRQ13*/EXSCLA	SMB_A_S3_CLK
	P7	PG6/EXIRQ14*/EXSDAB	SMB_B_S0_DATA
	R7	PG7/EXIRQ15*/EXSCLB	SMB_B_S0_CLK
	E1	PH0/EXIRQ6*	SMC_PROCHOT
	F3	PH1/EXIRQ7*	SMC_THRMTRIP
	K2	PH2/FWE	SMC_FWE
	C4	PH3/EXEXCL	ALS_GAIN
	D4	PH4	SMS_INT_L
	B3	PH5	SMS_ONOFF_L

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

=PP3V3_S5_SMC
C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

=PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
=PP3V3_S5_SMC
R5809 10K 5% 1/16W MF-LF 2402
R5801 10K 5% 1/16W MF-LF 2402

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

SMC_RST_L	E3	RES*	
SMC_XTAL	A2	XTAL	
SMC_EXTAL	B2	EXTAL	
	F2	MD1	SMC_MD1
	K1	MD2	KBC_MDE
	F4	NMI	SMC_NMI
	L1	ETRST*	SMC_TRST_L
	P12	AVSS	
	R12	AVSS	
	D1	VSS	
	F4	VSS	
	R4	VSS	
	F12	VSS	
	F13	VSS	
	B13	VSS	
	A13	VSS	
	A4	VSS	
	B4	VSS	
	D2	VSS	

NOSTUFF
R5898 10K 5% 1/16W MF-LF 2402
R5803 0 5% 1/16W MF-LF 2402
R5802 10K 5% 1/16W MF-LF 2402

XW5800
SM
GND_SMC_AVSS

SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 58 OF 110	

SMC RESET BUTTON

=PP3V3_S5_SMC

C5901 0.1uF 20% 10V CERM 402

CRITICAL

U5900 RN5VD30A-F SOT23-5 (VDD, CD, NC, GND, OUT)

R5900 1K 5% 1/16W MF-LF 402

SMC_MANUAL_RST_L

DEVELOPMENT SW5900 SPST SM-LF

C5900 0.01UF 10% 16V CERM 402

SMC_RST_L (OUT)

AMBIENT LIGHT SENSOR CONNECTOR

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

I2C ADDR:72(1001000)

CRITICAL J2901 53398-0476 F-ST-SM

PP3V3_S3

I2C_ALS_SDA

I2C_ALS_SCL

518S0328

SMC 3.3V -> CPU 1.05V SHIFTER

CPU_PROCHOT_L

Q5901 2N7002DW-X-F SOT-363

SMC_PROCHOT

PM_THRMTRIP_L

Q5901 2N7002DW-X-F SOT-363

SMC_THRMTRIP

POWER BUTTON HEADER

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

J2903 53398-0276 M-ST-SM

POWER_BUTTON_L

518S0327

R5907 1K 5% 1/16W MF-LF 402

SYS POWER BUTTON

SW5901 SPST SM-LF

DEVELOPMENT

SMC_ONOFF_L (OUT)

C5902 0.1uF 20% 10V CERM 402

GENERATE 0.48V MID-VREF

=PP3V3_S0_FAN

R5930 6.2K 5% 1/16W MF-LF 402

P0V48_SMC_LSREF

R5931 1K 5% 1/16W MF-LF 402

SMC CRYSTAL

C5800 22PF CERM 5% 50V 402

SMC_XTAL

OMIT Y5800 20.000M SM-3

C5801 22PF CERM 5% 50V 402

SMC_EXTAL

TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

C6704 15PF 5% 50V CERM 402

TPM_XTALI

CRITICAL Y6700 32.768K SM-LF

C6705 15PF 5% 50V CERM 402

TPM_XTALO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL,20.00,80PPM,HC49,SMD,LF	Y5800	CRITICAL	

CPU 1.05V -> SMC 3.3V SHIFTER

PP3V3_S5

=PP3V3_S0_FAN

C5903 0.1UF 20% 10V CERM 402

P0V48_SMC_LSREF

CPU_PROCHOT_L

U5999 LM393A SOI-1-LF

R5932 1K 5% 1/16W MF-LF 402

SMC_PROCHOT_3_3_L

R5933 1K 5% 1/16W MF-LF 402

SMC_CPU_RESET_3_3_L

R5934 1K 5% 1/16W MF-LF 402

SMC_XDP_TCK_3_3

R5935 1K 5% 1/16W MF-LF 402

SMC_XDP_TDO_3_3_L

U5999 LM393A SOI-1-LF

PCB: ENSURE FSB_CPURST_L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	DONE IN M50/M51

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20	MAKE_BASE=TRUE
SMC_P21	NC_SMC_P21	MAKE_BASE=TRUE
SMC_P22	NC_SMC_P22	MAKE_BASE=TRUE
SMC_P23	NC_SMC_P23	MAKE_BASE=TRUE
SMC_P26	NC_SMC_P26	MAKE_BASE=TRUE
SMC_P27	NC_SMC_P27	MAKE_BASE=TRUE
SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE
SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE
SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE
SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE	
SMC_PM_G2_EN	TP_PM_G2_EN	MAKE_BASE=TRUE	FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE	FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE	FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE	
SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE	
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE	FUNC_TEST=TRUE
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE	FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE	FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE	FUNC_TEST=TRUE

TPM RESET PULLUP

PP3V3_TPM_3VSB — R5827 10K — SMC_TPM_RESET_L

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L<0> (MAKE_BASE=TRUE)

SENSE GPU REGULATOR OUTPUT CURRENT

SMC_GPU_ISENSE — GPUVCORE_IOUT (MAKE_BASE=TRUE)

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L	MAKE_BASE=TRUE
SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE
SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE
SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE
SMC_NB_ISENSE	NC_SMC_NB_ISENSE	MAKE_BASE=TRUE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE

UNUSED_SMC_SENSE — R5924 10K 5% 1/16W MF-LF

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SMC_EXCARD_CP	R5830	10K
SMC_EXCARD_PWR_OC_L	R5831	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K

NOT_DEVELOPMENT_SMC

DEVELOPMENT_SMC

SC_RX_L — 0 — R5922 — SMC_RX_L

SC_TX_L — 0 — R5923 — SMC_TX_L

SELECT TPM GPIO

SMC_TPM_GPIO — 0 — R5920 — TPM_GPIO1

SMC_TPM_GPIO2 — 0 — R5921 — TPM_GPIO2

SMC_TPM_PP — R5995 0 — SMC_TPM_PP — TPM_PP

SENSE GPU VCORE

PP1V0R1V2_S0_GPU — R5919 4.53K 1% 1/16W MF-LF 402 — SMC_GPU_VSENSE

C5919 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS

PRECISION 3.3V AVREF FOR SMC

PP5V_S5

R5942 10K 5% 1/16W MF-LF 402

Q5910 NTR4101P SOT-23

SMC_REF_GATE2

SMC_REF_GATE1

R5941 10K 5% 1/16W MF-LF 402

Q5911 2N7002 SOT23-LF

C5943 1UF 10% 6.3V CERM 402

SMC_REF_IN

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDT=0.2 MM

NOSTUFF R5940 0 5% 1/16W MF-LF 402

=PP3V3_S5_SMC

CRITICAL U5940 REF3133 SOT23-3 (IN, TI, OUT, GND)

PP3V3_AVREF_SMC (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V)

C5940 0.47UF 20% 6.3V CERM-X5R 402

C5942 10UF 20% 6.3V CERM 805-1

C5941 0.01UF 10% 16V CERM 402

GND_SMC_AVSS (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0V)

TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

SMC I2C BUS PULLUPS (INCLUDING UNUSED ONES)

PP3V3_S0

2.2K	R5903	SMB_B_S0_CLK
2.2K	R5904	SMB_B_S0_DATA

PP3V3_S3

2.2K	R5905	SMB_A_S3_CLK
2.2K	R5906	SMB_A_S3_DATA

=PP3V3_S5_SMC

10K	R5910	SMB_BSB_CLK
10K	R5911	SMB_BSB_DATA
10K	R5912	TP_SMC_SMB_0_CLK (MAKE_BASE=TRUE, FUNC_TEST=TRUE) / SMC_SMB_0_CLK
10K	R5913	SMC_SMB_0_DATA / TP_SMC_SMB_0_DATA (MAKE_BASE=TRUE, FUNC_TEST=TRUE)
10K	R5914	SMB_BSA_CLK
10K	R5915	SMB_BSA_DATA

PULLUPS FOR SYSTEM STATE PINS

10K R5916 SMC_LID

PULLDOWNS FOR SYSTEM STATE PINS

10K R5917 SMC_CASE_OPEN

ALIAS SENSORS INTO SMC I2C BUSSES

SMB_B_S0_CLK — SMB_B_S0_DATA (MAKE_BASE=TRUE)

=I2C_HD_TEMP_SCL

=I2C_HD_TEMP_SDA

=I2C_ODD_TEMP_SCL

=I2C_ODD_TEMP_SDA

=SMB_THRM_CLK

=SMB_THRM_DATA

SMB_GPU_NB_THRM_CLK

SMB_GPU_NB_THRM_DATA

SMB_A_S3_CLK — I2C_ALS_SCL

SMB_A_S3_DATA — I2C_ALS_SDA

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

XW5900 SM

GND_NEXT_TO_SMC

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

PP5V_S3

PLACE C5951 NEXT TO Q5952

R5955 4.7K 5% 1/16W MF-LF 402

SYS_LED_BRT_D

R5951 2.2K 5% 1/16W MF-LF 402

C5951 1UF 10% 6.3V CERM 402

R5952 43 5% 1/16W MF-LF 402

SYS_LED_CTL_C

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q5952 2N3906 SOT23-LF

SYS_LED_CTL_B

Q5951 2N7002 SOT23-LF

R5957 4.7K 5% 1/16W MF-LF 402

SYS_LED_CTL_D

NOSTUFF R5991 0 1/16W MF-LF 5% 402

SMC_SYS_LED

SYS_LED_C MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

R5990 0 5% 1/16W MF-LF 402

SMC_SYS_LED_16B

Q5950 2N7002 SOT23-LF

CRITICAL LED5950 WHITE-740MCD 3X2MM-SM 378S0169

NOSTUFF R5950 4.7K 1% 1/16W MF-LF 402

SMC & TPM SUPPORT

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II NOT TO REPRODUCE OR COPY IT

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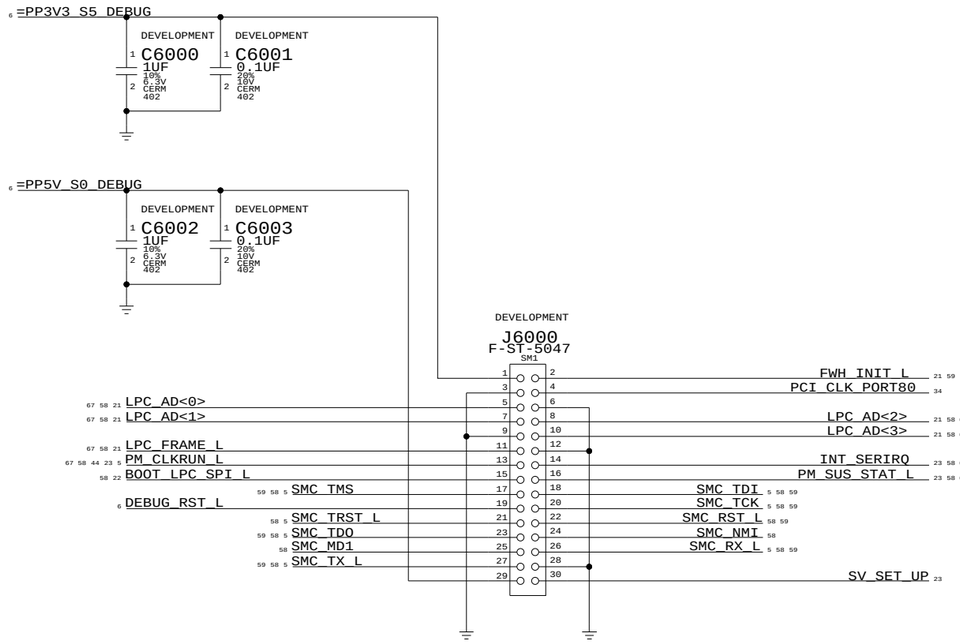
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 59 OF 110	



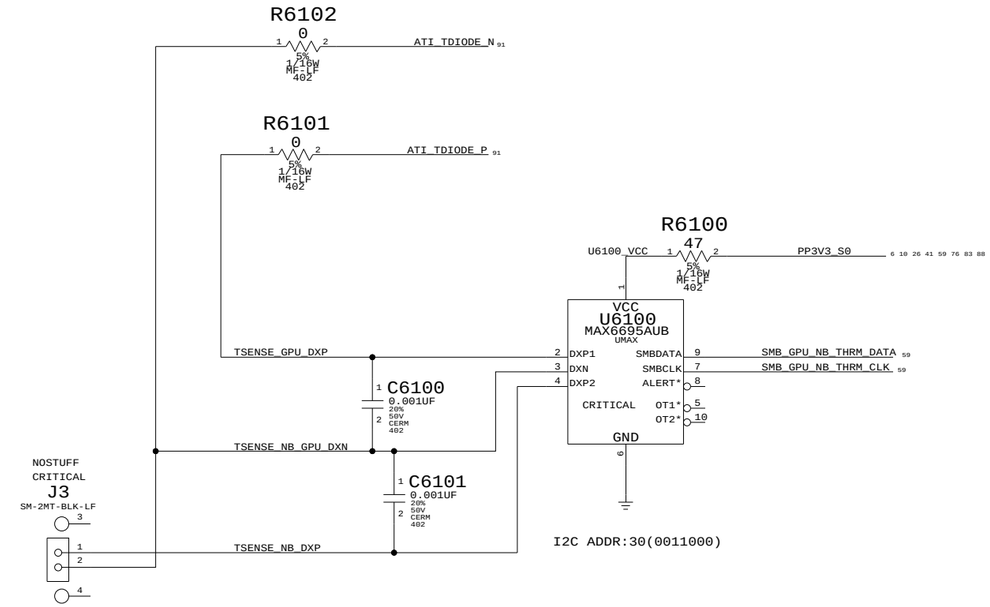
LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT
NONE	60 OF 110



GPU+NB THERMAL

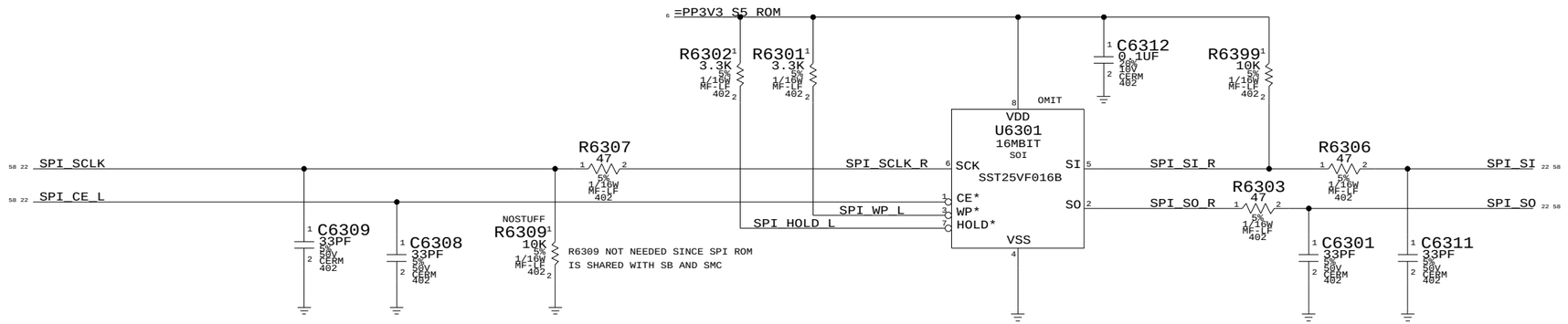
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE

SHT 61 OF 110



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

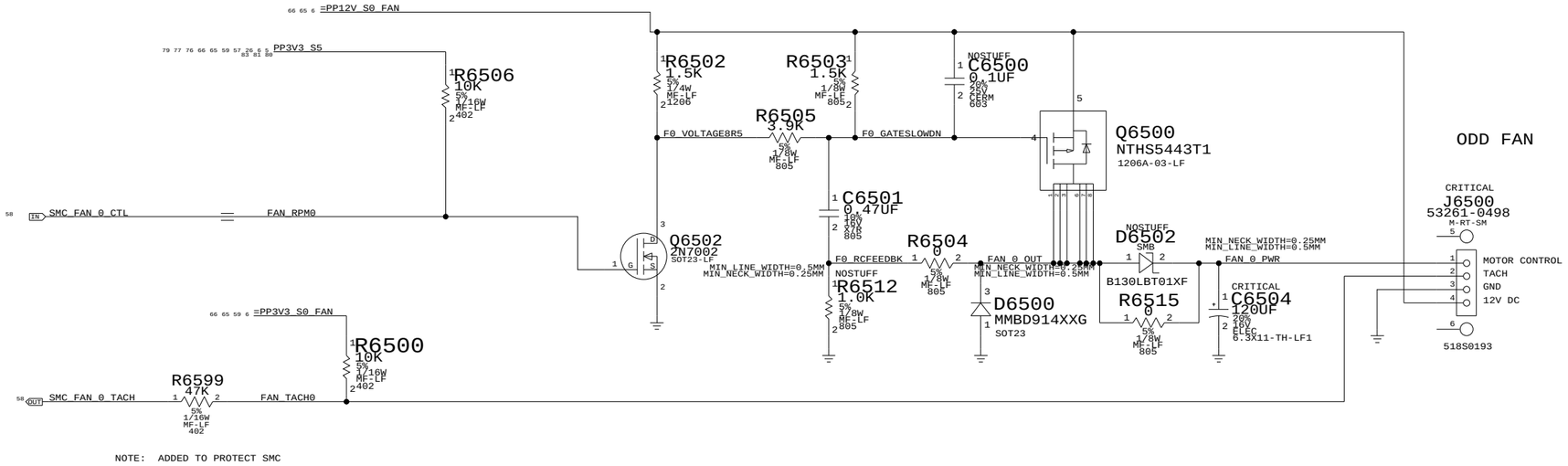
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

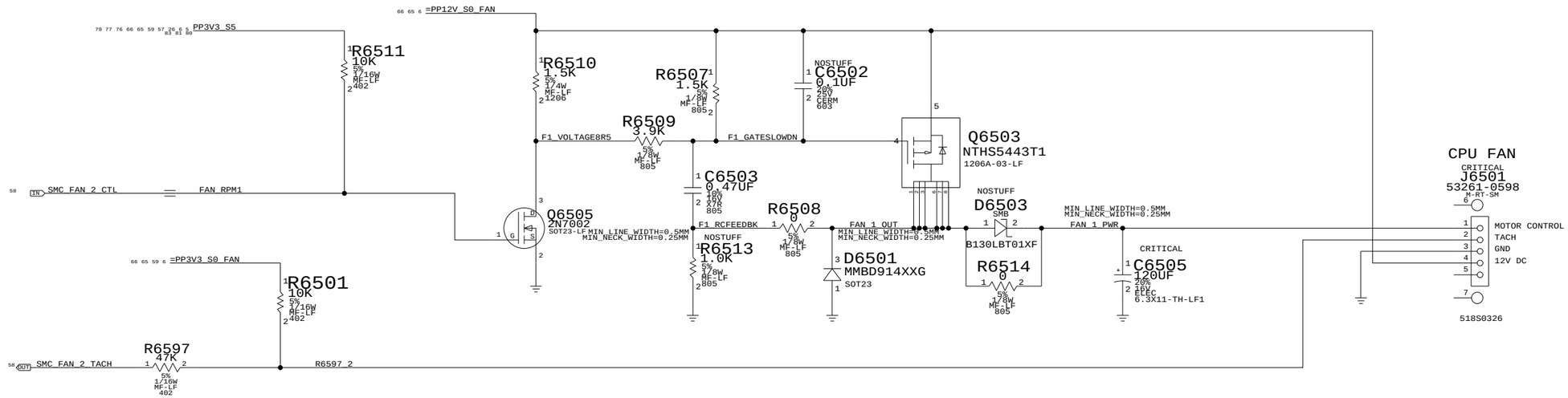
SCALE	SHT	OF
NONE	63	110

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1

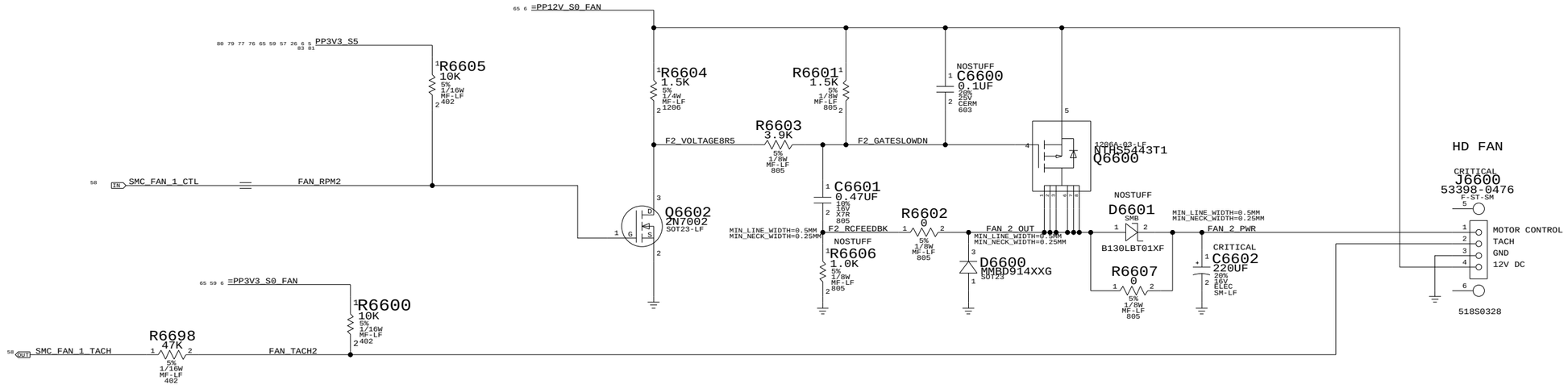


Fan 0, 1 & System Temp

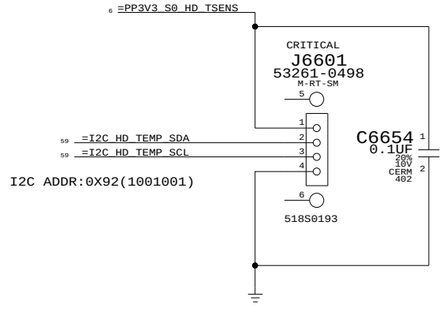
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 65 OF 110	

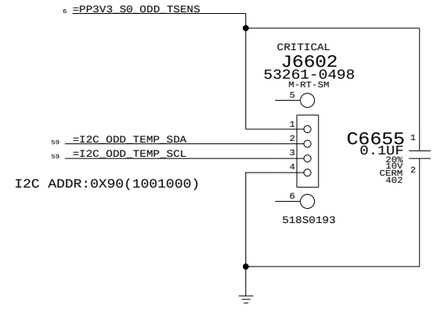
FAN 2



HD TEMP SENSOR



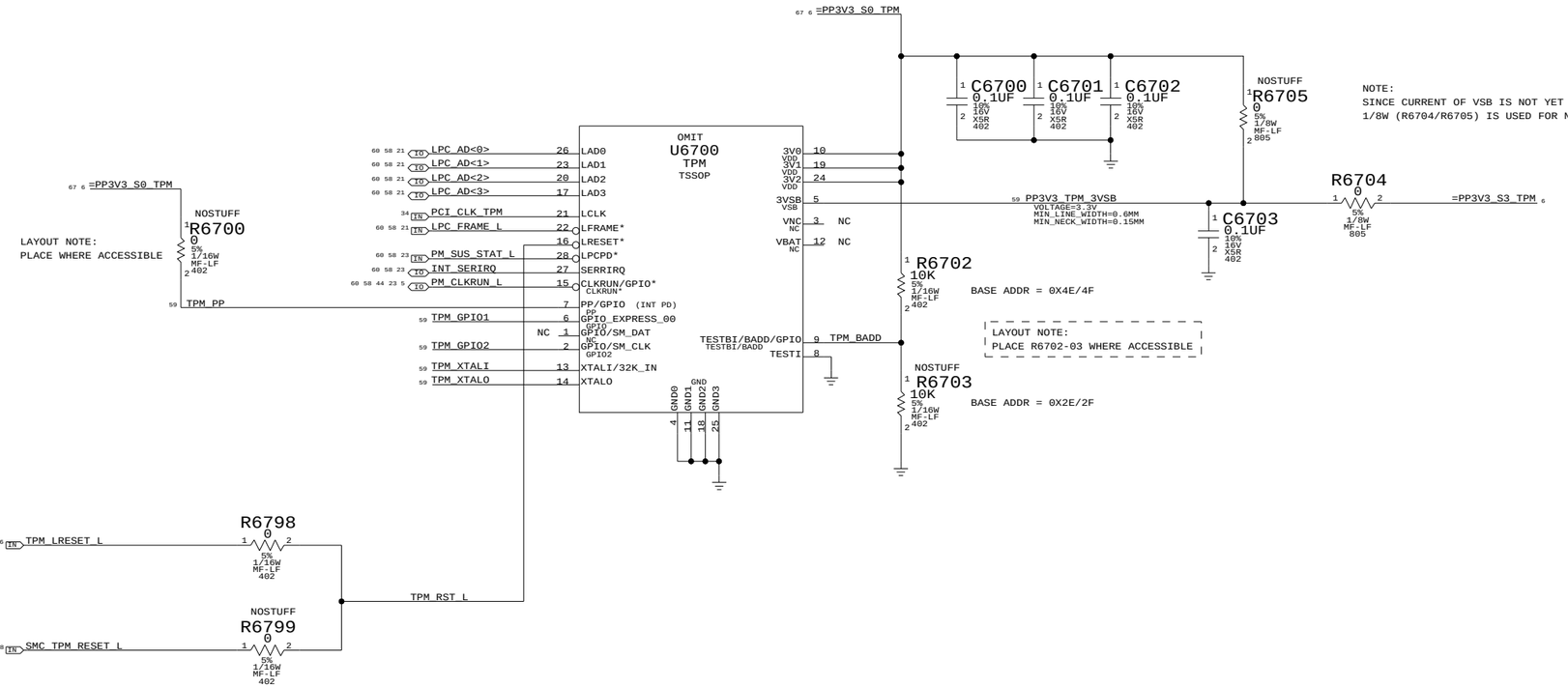
ODD TEMP SENSOR



Fan 2 & HD Temp

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 66 OF 110	



TPM

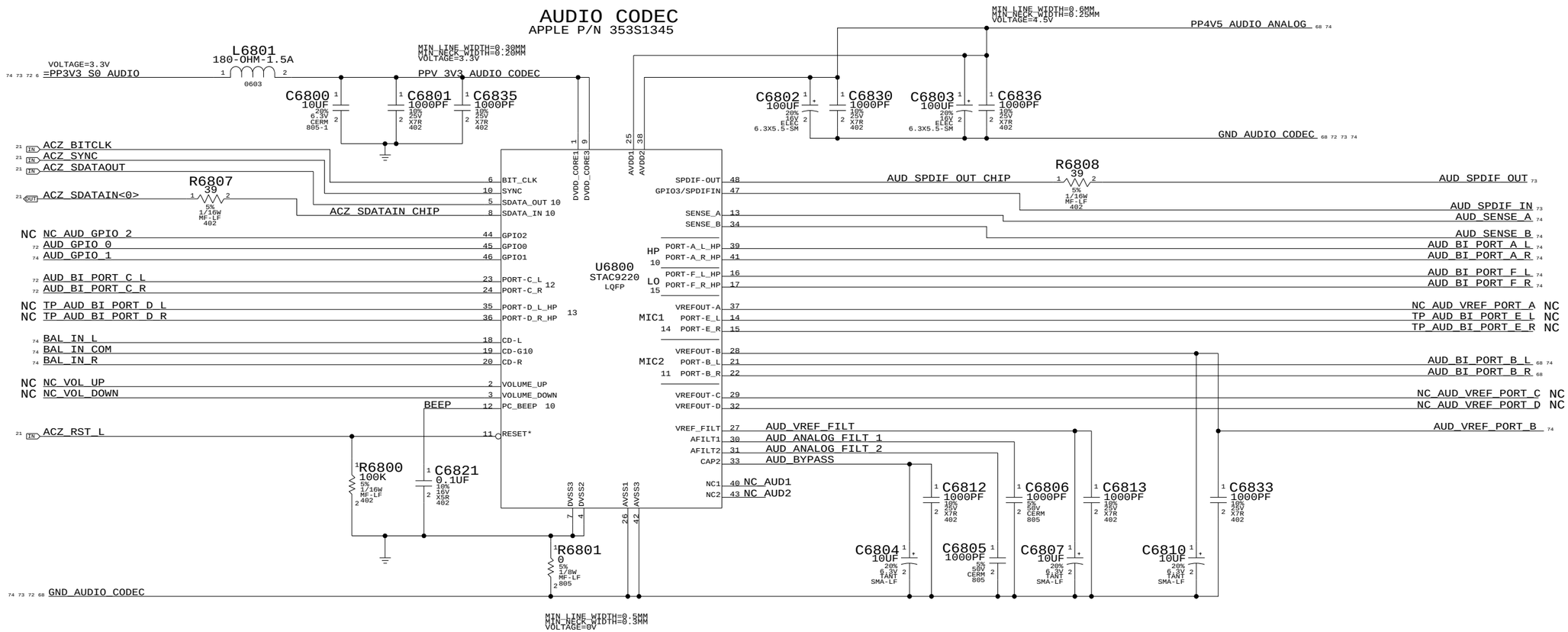
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT
NONE	67 OF 110

AUDIO CODEC
APPLE P/N 353S1345



AUD_BI_PORT_B_L = AUD_BI_PORT_B_R

MIC INPUT TO BOTH L&R

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
=PP4V5_S0_AUDIO_ANALOG

L6802
180-OHM-1.5A
0603

PP4V5_AUDIO_ANALOG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C6802,C6803	FACTORY SHORTAGE
126S0091	126S0092		C7403,C7404	FACTORY SHORTAGE

AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	13
SCALE: NONE	SHT 68 OF 110	

SPEAKER AMP
APPLE P/N 353S0680

=PP12V_S0_AUDIO_SPKRAMP
L7200 FERR-250-OHM
PP12V_AUD_SPKRAMP_PLANE
C7217 220UF
C7200 220UF
C7201 10UF
C7218 0.1UF
C7202 1UF
C7219 0.1UF
C7203 10UF
C7223 10UF
GND_AUDIO_SPKRAMP_PLANE
GND_AUDIO_CODEC
=PP3V3_S0_AUDIO
L7205 1000-OHM-200MA
L7206 1000-OHM-200MA
L7207 1000-OHM-200MA
L7208 1000-OHM-200MA
AUD_BI_PORT_C_L
AUD_BI_PORT_C_R
AUDSAMPINLN
AUDSAMPINLP
AUDSAMPINRP
AUDSAMPINRN
C7204 0.47UF
C7205 0.47UF
C7206 0.47UF
C7207 0.47UF
C7215 100PF
C7216 100PF
R7214 10K
AUD_SAMP_INL_N
AUD_SAMP_INL_P
AUD_SAMP_INR_P
AUD_SAMP_INR_N
AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2
AUD_SAMP_SHDN_L
AUD_MAX9714_VREG
U7200 MAX9714 QFN-LF
VDD
CHOLD
INL- INL+ INR+ INR- G1 G2 FS1 FS2 SHDN* NC REG
OUTL+ OUTL+ OUTL- OUTL- C1+ C1- OUTR+ OUTR+ OUTR- OUTR-
AGND PAD THM PGND SS
AUD_MAX9714_CHOLD
AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPCPP
AUDSAMPCPN
AUDSAMPOURTP
AUDSAMPOUTRN
C7208 0.1UF
L7201 180-OHM-1.5A
L7202 180-OHM-1.5A
L7203 180-OHM-1.5A
L7204 180-OHM-1.5A
AUD_SPKR_OUTL_P
AUD_SPKR_OUTL_N
AUD_SPKR_OUTR_P
AUD_SPKR_OUTR_N
R7215 10K
PP3V3_INTERCON
R7216 0
R7217 0
SPKRAMP_MUTE
SPKRAMP_SS
AUD_GPIO_0
R7213 100
AUD_DEBOUNCE
Q7200 2N7002DW-X-F SOT-363
C7221 100PF
R7212 10K
C7214 1UF
R7219 0
C7209 0.47UF
C7210 1000PF
C7211 1000PF
C7212 1000PF
C7213 1000PF
XC7200 50H28
XW7201 SM OMIT
GND_AUDIO_SPKRAMP

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO
RP7200 47K
AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1
R7218 0
R7208 0
GND_AUDIO_SPKRAMP_PLANE

NET SPACING TYPE=AUDIO
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V

NET SPACING TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM

NET SPACING TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

NET SPACING TYPE=AUDIO
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM

NET SPACING TYPE=AUDIO
MIN_NECK_WIDTH=0.25MM

TITLE	AUDIO: SPEAKER AMP
SYNC_MASTER	FINO-SO
SYNC_DATE	04/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 72 OF 110	

COMBO IN JACK
APPLE P/N 514-0349

OMIT
CRITICAL

J7300
OPTI-AUD-IN-JCK-M60
F-ANG-TH

NC_AUD_LI_TYPE_JACK NC
AUD_LI_L_JACK
AUD_LI_DET_JACK
AUD_LI_R_JACK
AUD_LI_GND_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_SPDIFIN_JACK
AUD_SPDIF_GND_IN NC
GND_CHASSIS_AUDIO_EXTERNAL_J

L7300 180-OHM-1.5A 0603 — AUD_LI_L_EMI
L7301 180-OHM-1.5A 0603 — AUD_LI_DET_EMI
L7302 180-OHM-1.5A 0603 — AUD_LI_R_EMI
L7303 180-OHM-1.5A 0603 — AUD_LI_GND_EMI
L7304 180-OHM-1.5A 0603 — AUD_LI_L
L7305 180-OHM-1.5A 0603 — AUD_LI_DET_H
L7306 180-OHM-1.5A 0603 — AUD_LI_R
L7307 180-OHM-1.5A 0603 — GND_AUDIO_CODEC

R7306 39 5% 1/16W MF-LF 402 — AUD_SPDIF_IN
R7305 5% 1/16W MF-LF 402
R7307 0 5% 1/8W MF-LF 805 — GND_CHASSIS_AUDIO_EXTERNAL
C7326 1UF 10% 6.3V CERM 402

DZ7300 8V-100PF 402
DZ7301 8V-100PF 402
DZ7302 8V-100PF 402
DZ7324 8V-100PF 402

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325

PROPERTIES FOR ALL SPKR NETS (OTHERS HIDDEN)
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO

J7301
53261-0798
M-RT-SM

AUD_SPKR_OUTR_N
AUD_SPKR_OUTR_P
AUD_SPKR_OUTL_N
AUD_SPKR_OUTL_P

XW7300
SM

L7309 180-OHM-1.5A 0603 — AUD_MIC_IN_P_EMI — AUD_MIC_IN_P
L7310 180-OHM-1.5A 0603 — AUD_MIC_IN_N_EMI — AUD_MIC_IN_N
L7312 180-OHM-1.5A 0603 — GND_AUDIO_MIC_CONN — AUD_MIC_IN_P_CONN
L7313 180-OHM-1.5A 0603 — AUD_MIC_IN_N_CONN

DZ7325 8V-100PF 402
DZ7326 8V-100PF 402

TO FHB CONNECTOR PAGE 47
TO POWER SUPPLY PAGE 6
GND_CHASSIS_AUDIO_INTERNAL

LINE OUT JACK
APPLE P/N 514-0354

OMIT
CRITICAL

J7303
OPTI-AUD-OUT-JCK-M60
F-ANG-TH

AUD_SPDIF_OUT
AUD_LO_TYPE_JACK
AUD_LO_L_JACK
AUD_LO_TIP_JACK
AUD_LO_R_JACK
AUD_LO_GND_JACK
AUD_SPDIF_GND_OUT NC
GND_CHASSIS_AUDIO_EXTERNAL_J

R7308 100K 5% 1/16W MF-LF 402
R7302 0 5% 1/16W MF-LF 402

L7315 180-OHM-1.5A 0603 — =PP3V3_S0_AUDIO — PP3V3_AUDIO_SPDIF_EMI
L7316 180-OHM-1.5A 0603 — AUD_LO_TYPE — AUD_LO_TYPE_EMI
L7317 180-OHM-1.5A 0603 — AUD_LO_R — AUD_LO_R_EMI
L7318 180-OHM-1.5A 0603 — AUD_LO_L — AUD_LO_L_EMI
L7319 180-OHM-1.5A 0603 — AUD_LO_TIP — AUD_LO_TIP_EMI
L7323 180-OHM-1.5A 0603 — PP3V3_AUDIO_SPDIF_JACK
L7324 180-OHM-1.5A 0603
L7325 180-OHM-1.5A 0603
L7326 180-OHM-1.5A 0603
L7327 180-OHM-1.5A 0603
L7381 180-OHM-1.5A 0603 — GND_AUDIO_CODEC
L7880 180-OHM-1.5A 0603 — GND_AUDIO_CODEC — GND_AUDIO_CODEC_EMI1

C7317 1UF 10% 6.3V CERM 402
C7318 10UF 20% 6.3V CERM 805-1

DZ7311 8V-100PF 402
DZ7313 8V-100PF 402
DZ7314 8V-100PF 402
DZ7315 8V-100PF 402
DZ7323 8V-100PF 402
DZ7380 8V-100PF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0349	1	COMBO INPUT CONNECTOR M60	J7300	CRITICAL	
514-0354	1	COMBO OUTPUT CONNECTOR M60	J7303	CRITICAL	

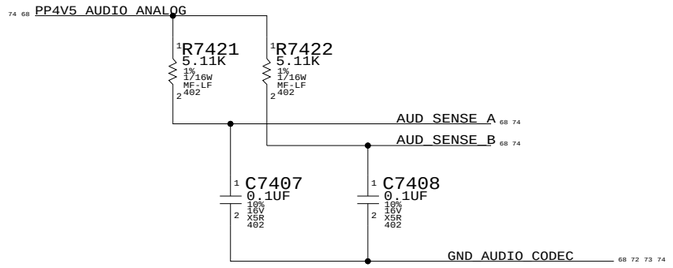
AUDIO: INPUT/OUTPUT

SYNC_MASTER=AUDIO
SYNC_DATE=02/23/2006

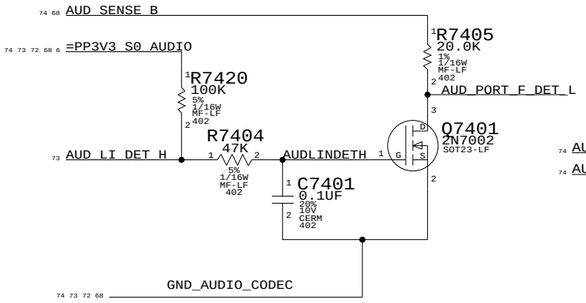
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	13
SCALE: NONE	SHT 73 OF 110	

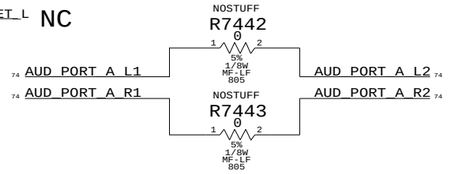
JACK SENSE PULL UPS(PLACE NEXT TO CODEC)

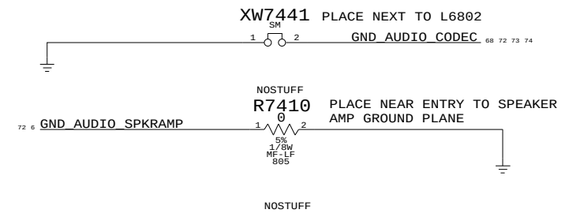


PORT F (LI) PLUG DETECT



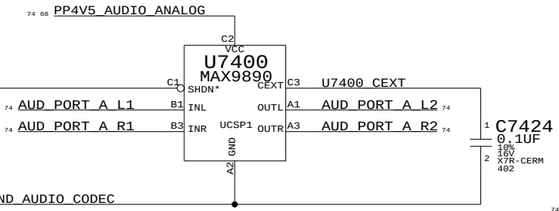
AUDIO GROUND RETURNS



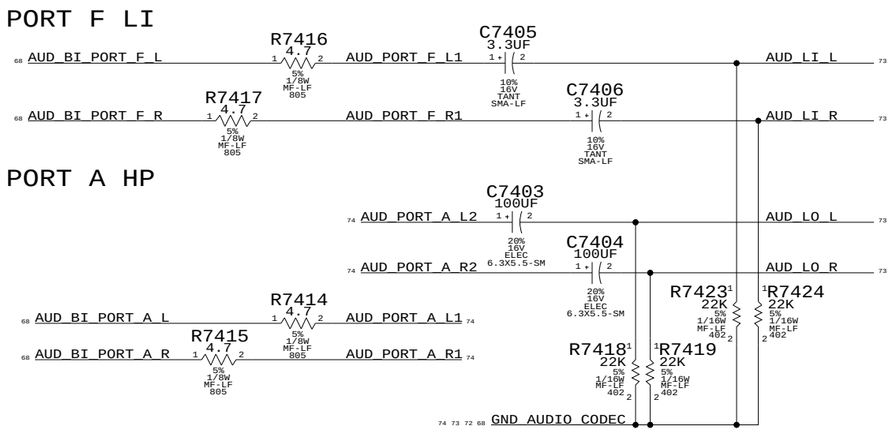


USED PORTS
PORT A HP
PORT B MIC IN VREF =80%
PORT C BI SPEAKERS
PORT F LI

UNUSED PORTS
PORT E DETECT DELEGATE
PORT D

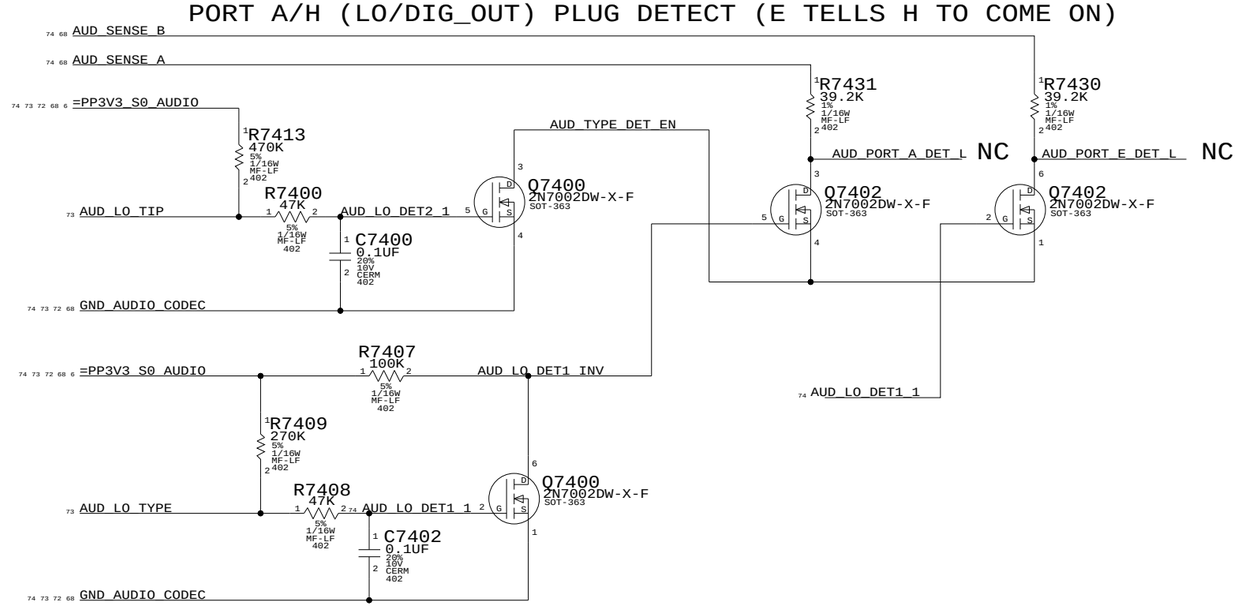


PORT F LI

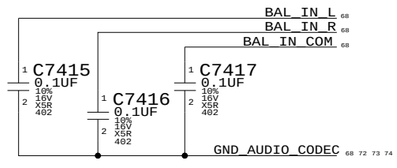


PORT A HP

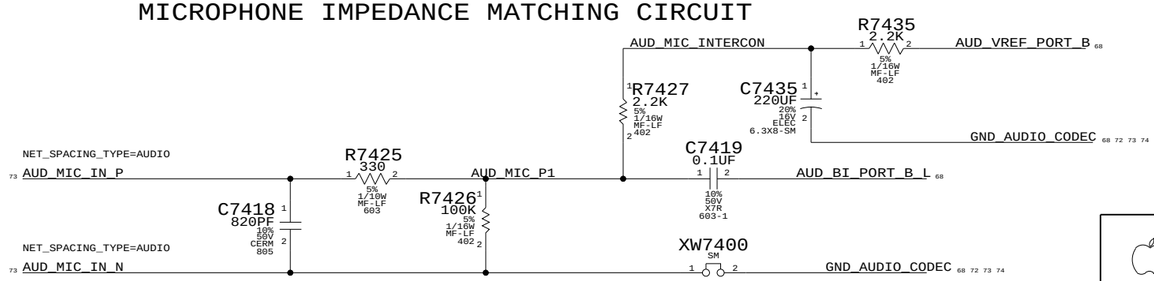
PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



UNUSED PORT TERMINATION



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: JACK DETECT

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	13
SCALE: NONE	SHT 74 OF 110	

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator	
SYNC_MASTER=POWER	SYNC_DATE=07/08/2005

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APPLE COMPUTER INC.

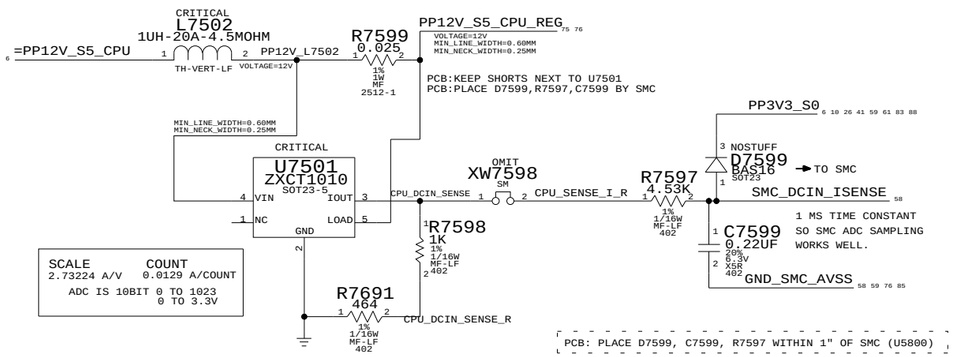
SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 75 OF 110	

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

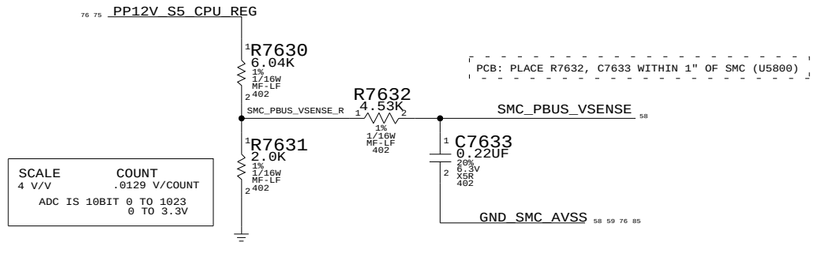
PROCESSOR VCORE CURRENT SENSE

(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

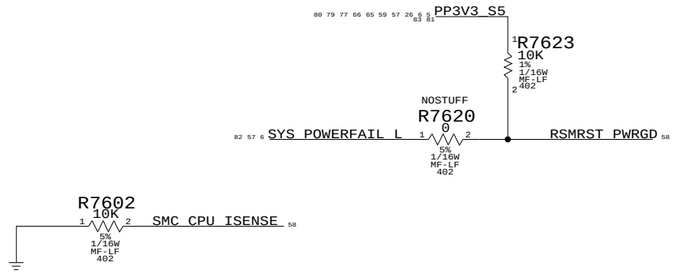


PROCESSOR DCIN VOLTAGE SENSE

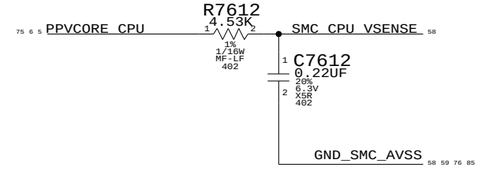
(SCALING 12V INPUT VOLTAGE TO SMC)

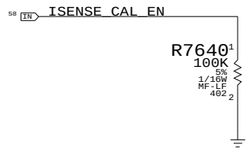


SMC PWRGD PULLUP



PROCESSOR VCORE SENSE



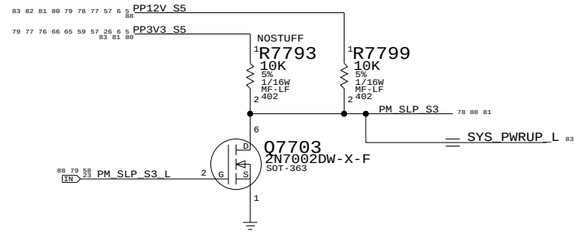


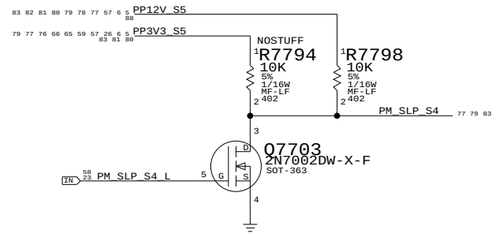
CPU SENSE CIRCUITRIES

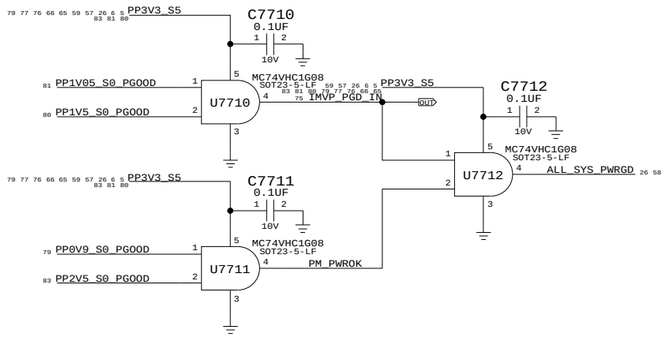
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

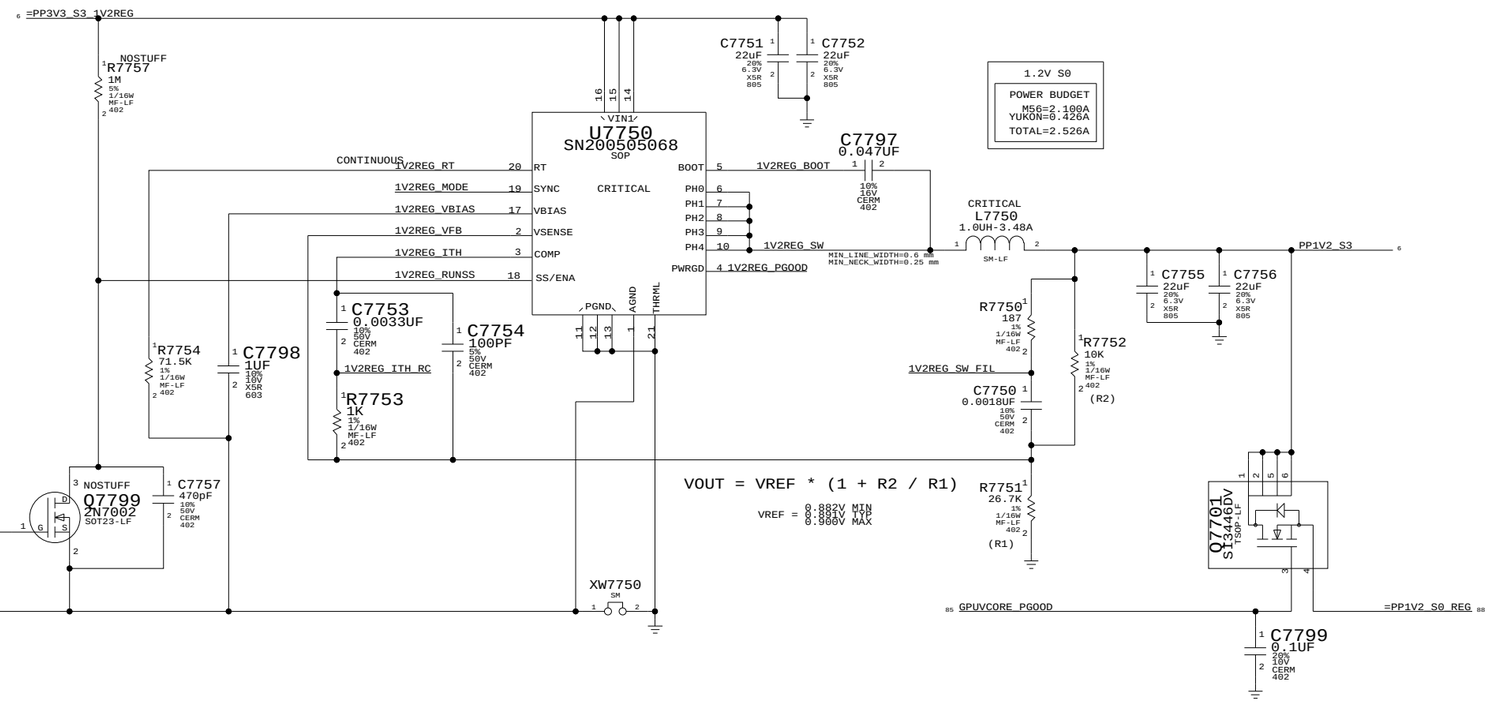
SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 76 OF 110	







1.2V S3 REGULATOR / 1.2V S0 FET



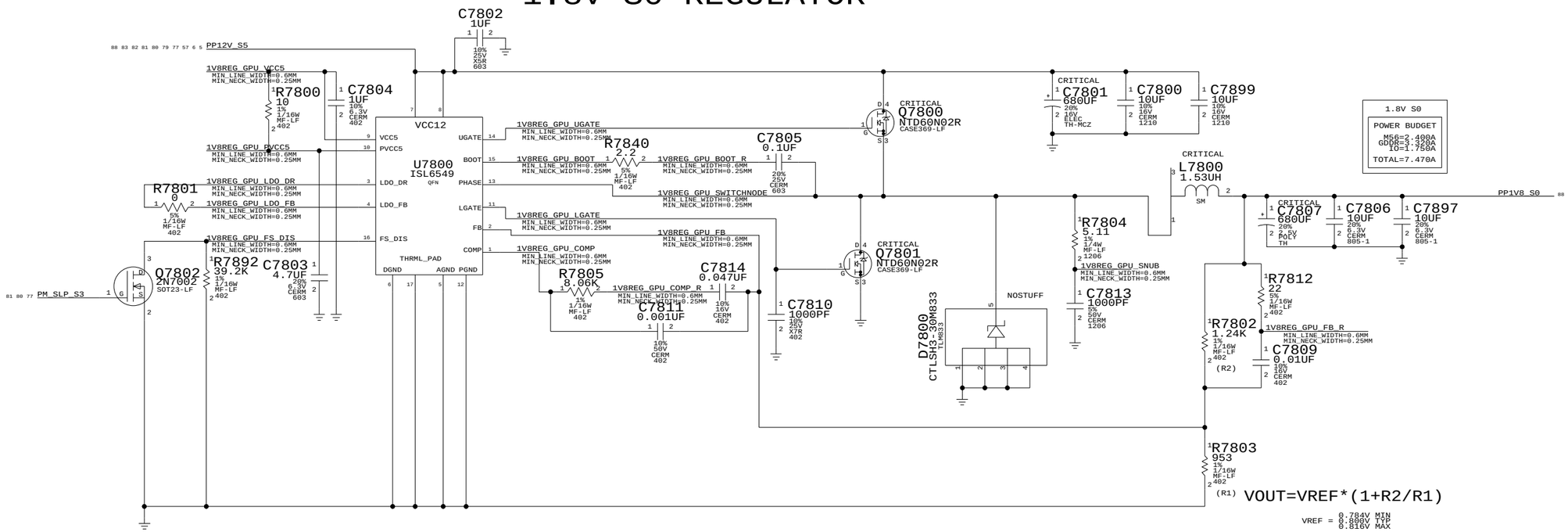
2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 77 OF 110	

1.8V S0 REGULATOR



1.8V GDDR REGULATOR

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

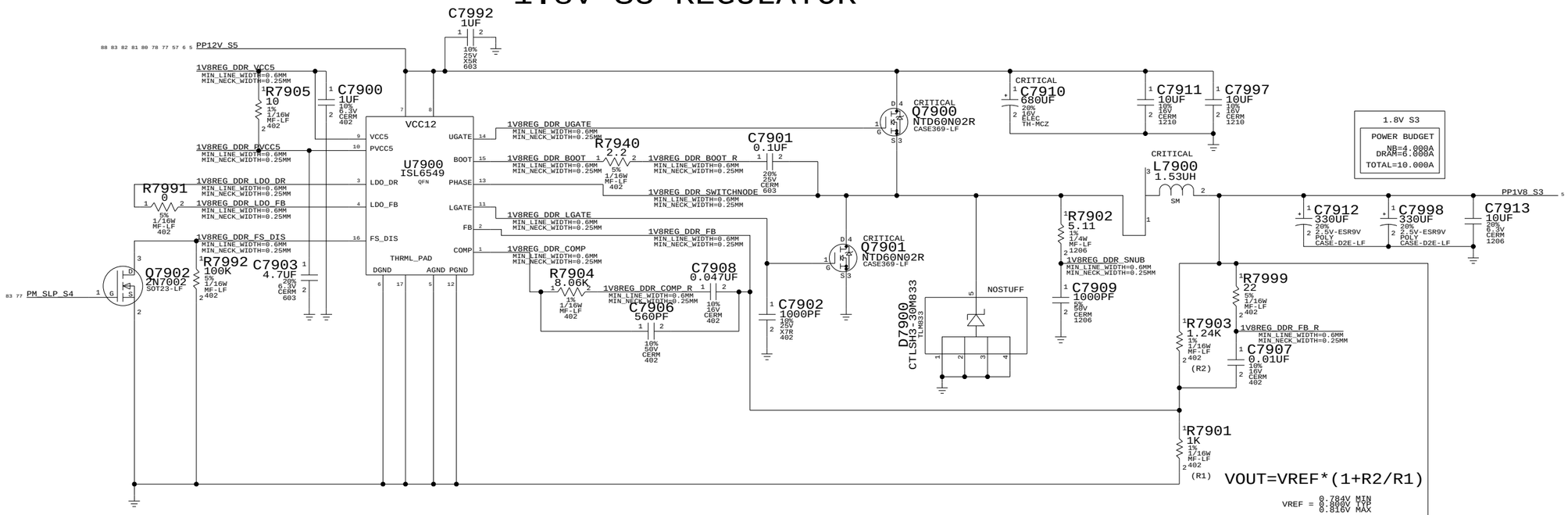
SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE

SHT 78 OF 110

TRUE

1.8V S3 REGULATOR



1.8V Vreg

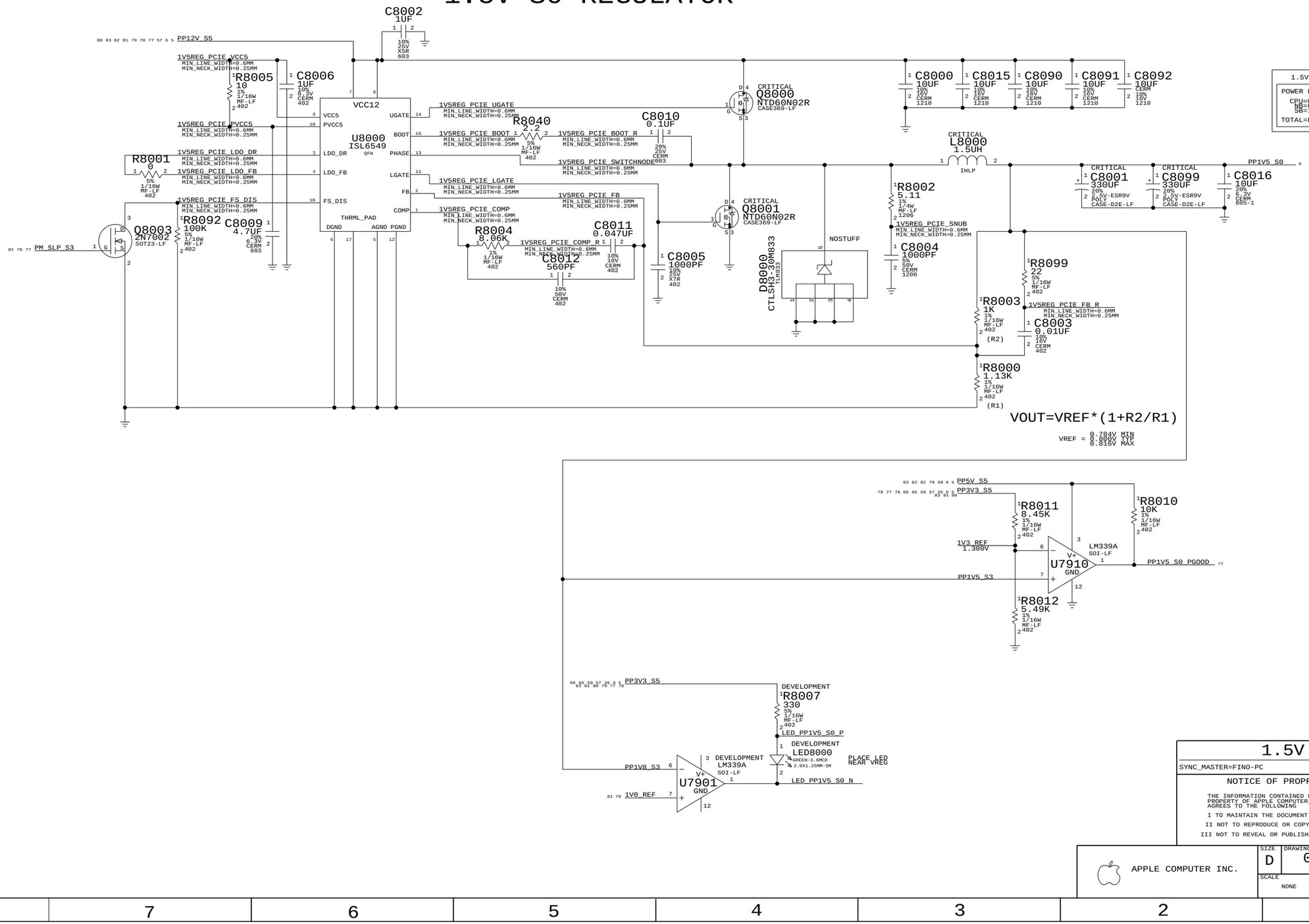
SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT
NONE	79 OF 110

1.5V S0 REGULATOR



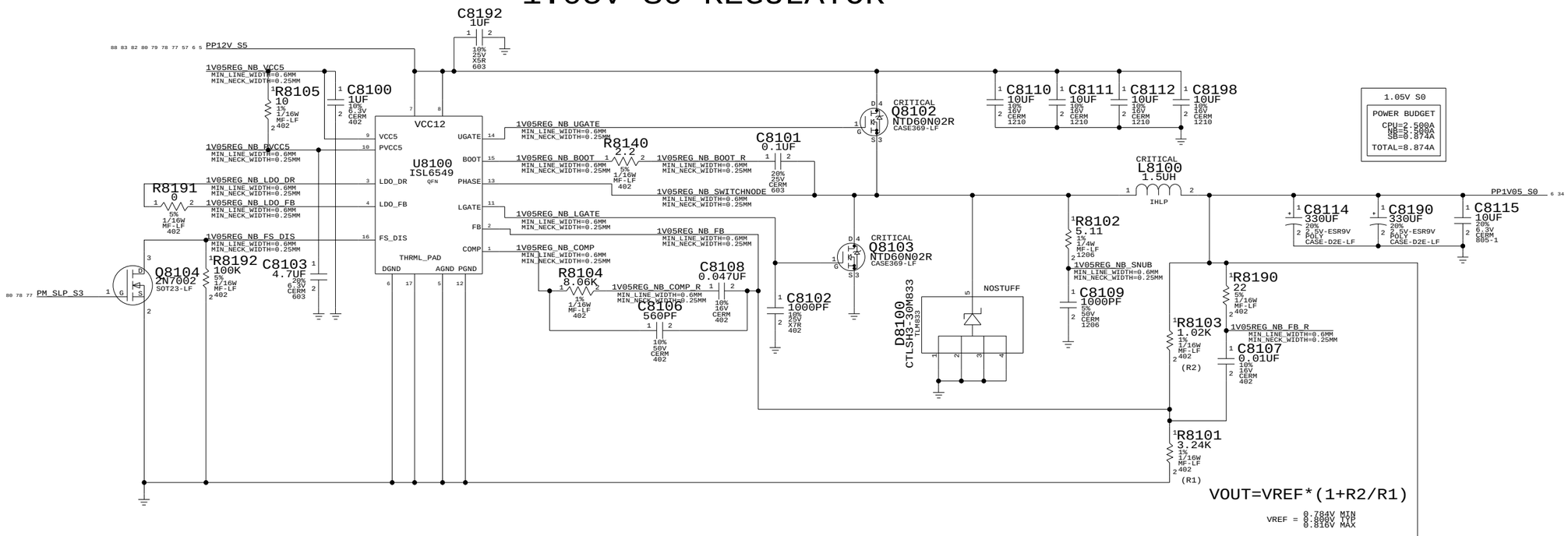
1.5V Vreg

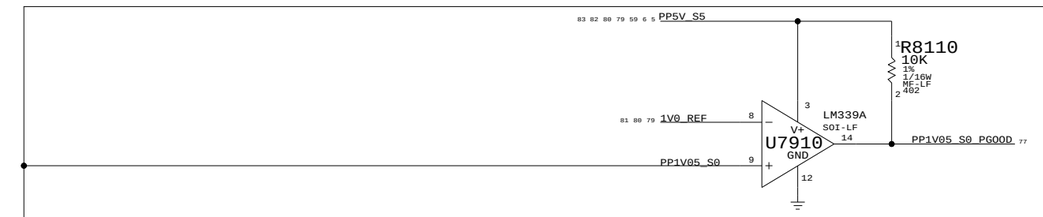
SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

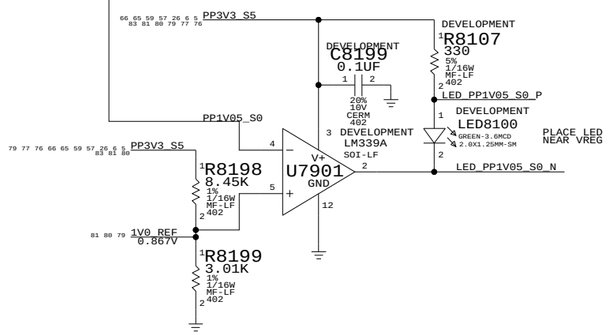
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 80 OF 110	

1.05V S0 REGULATOR







1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 81 OF 110	

5V S5 AND 5V AUDIO S5 REGULATOR

=PP5V_S5_AUDIO_LDO
C8220 22UF 20% 6.3V X5R 805
CRITICAL Q8203 IRF1902PBF SO-8

5V AUDIO S5
M50 POWER BUDGET
AUDIO=0.059A
TOTAL=0.059A

PP4V5_S5_AUDIO_ANALOG 4.50V NOMINAL
C8225 10UF 20% 6.3V CERM 805-1
C8222 10UF 20% 6.3V CERM 805-1
C8221 10UF 20% 6.3V CERM 805-1
C8226 10UF 20% 6.3V CERM 805-1
R8220 1K 1% 1/16W MF-LF 402
R8222 215 1% 1/16W MF-LF 402

PP12V_S5
C8292 1UF 10% 25V X5R 603
C8200 1UF 10% 25V CERM 402
R8205 10 1% 1/16W MF-LF 402
5VREG_VCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_PVCC5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LDO_DR MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8223 1000PF 10% 25V X7R 402
5V_AUDIO_LDODR_C MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8221 2.7K 5% 1/16W MF-LF 402
NOSTUFF C8224 1000PF 10% 25V X7R 402
5VREG_LDO_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

U8200 ISL6549 QFN
VCC12
VCC5
PVCC5 CRITICAL
LDO_DR
LDO_FB
FS_DIS
THRML_PAD
DGND
AGND PGND
UGATE
BOOT
PHASE
LGATE
FB
COMP

5VREG_UGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_BOOT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8240 2.2 5% 1/16W MF-LF 402
5VREG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8201 0.1UF 20% 25V CERM 603
5VREG_SWITCHNODE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_LGATE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_FB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
5VREG_COMP MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8204 8.06K 1% 1/16W MF-LF 402
5VREG_COMP_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8208 0.047UF 10% 16V CERM 402
C8206 470PF 10% 50V CERM 402

CRITICAL Q8200 IRLR7807Z TO-252AA
CRITICAL Q8201 IRLR7807Z TO-252AA
C8202 1000PF 10% 25V X7R 402
D8200 CTLSH3-30M833 TLM833
NOSTUFF

CRITICAL C8253 1000UF 20% 16V ELEC TH-KZJ-LF
C8211 10UF 20% 6.3V CERM 1210
L8203 3.3UH IHLP CRITICAL
R8202 5.11 1% 1/4W MF-LF 1206
5VREG_SNUB MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8209 1000PF 5% 50V CERM 1206

5V S5
M50 POWER BUDGET
5V S0=3.544A
5V S3=1.600A
MISC=0.164A
TOTAL=5.317A

CRITICAL C8215 1800UF 20% 6.3V ELEC TH-KZJ-LF
C8214 10UF 20% 6.3V CERM 805-1
C8213 10UF 20% 6.3V CERM 805-1
PP5V_S5 5.10V NOMINAL

R8299 22 5% 1/16W MF-LF 402
R8203 1.24K 1% 1/16W MF-LF 402 (R2)
5VREG_FB_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C8207 0.01UF 10% 16V CERM 402
R8201 232 1% 1/16W MF-LF 402 (R1)

VOUT=VREF*(1+R2/R1)
VREF = 0.784V MIN
0.800V TYP
0.816V MAX

5VREG_FS_DIS MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R8292 39.2K 1% 1/16W MF-LF 402
NOSTUFF Q8202 2N7002 SOT23-LF
SYS_POWERFAIL_L
C8203 4.7UF 20% 6.3V CERM 603

5V DC/DC 4.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

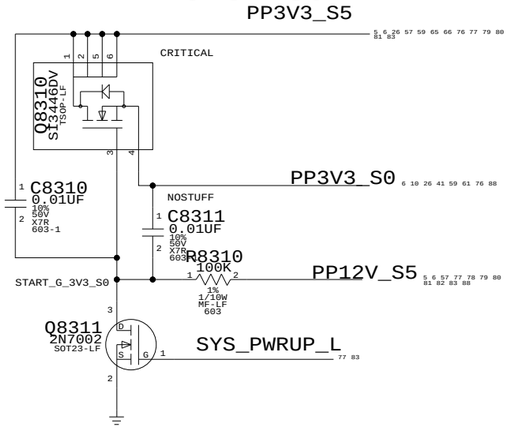
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

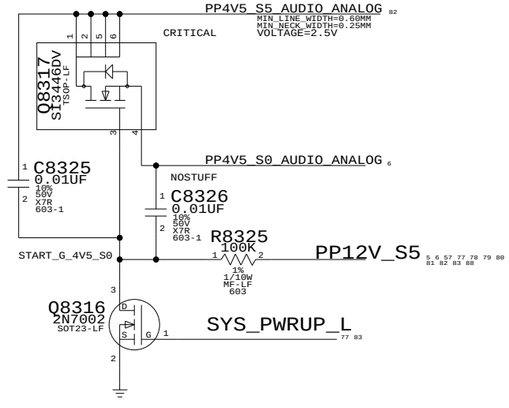
SCALE: NONE

SHT 82 OF 110

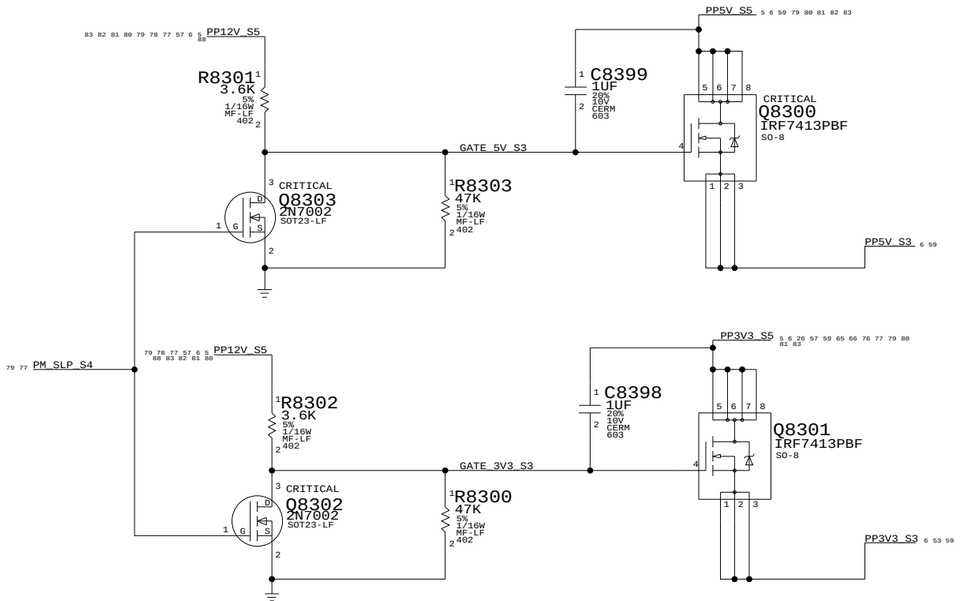
3.3V S0



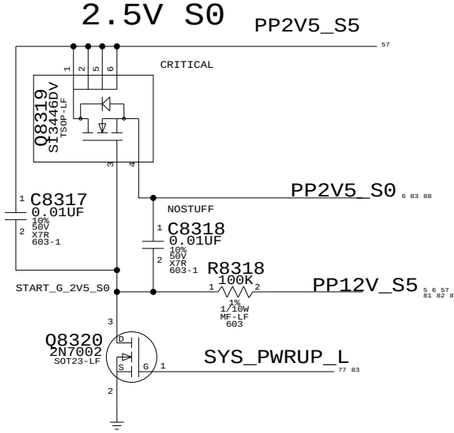
4.5V S0 AUDIO



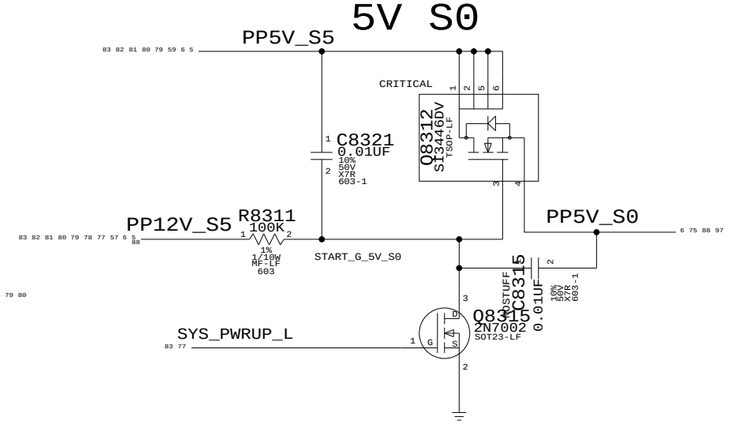
3.3V AND 5V S3



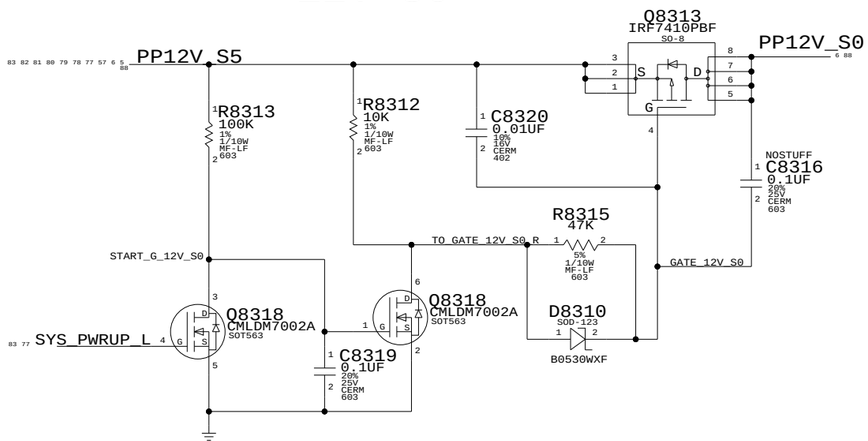
2.5V S0

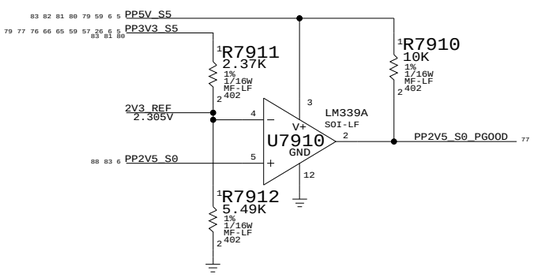


5V S0



12V S0





S0 AND S3 FETS

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

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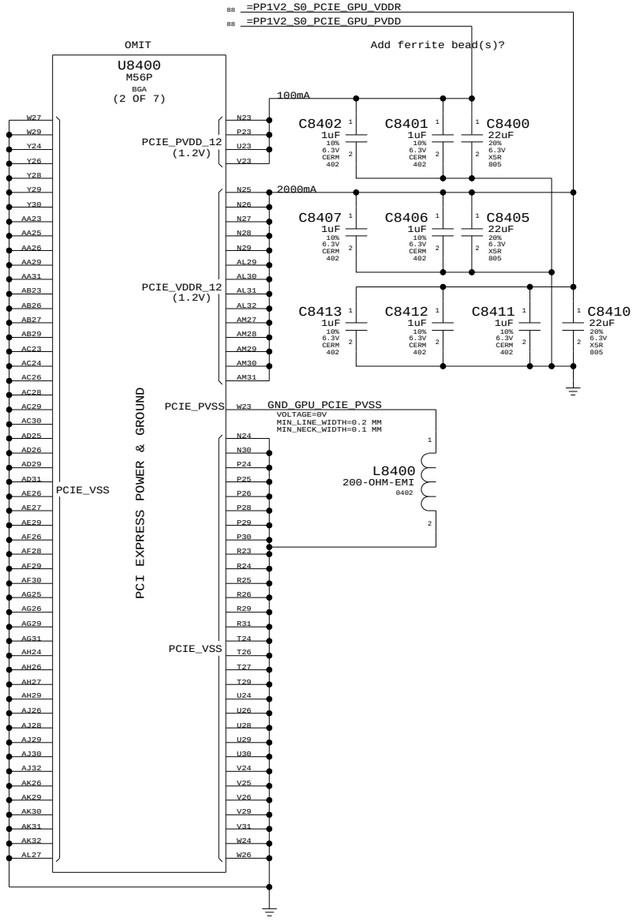
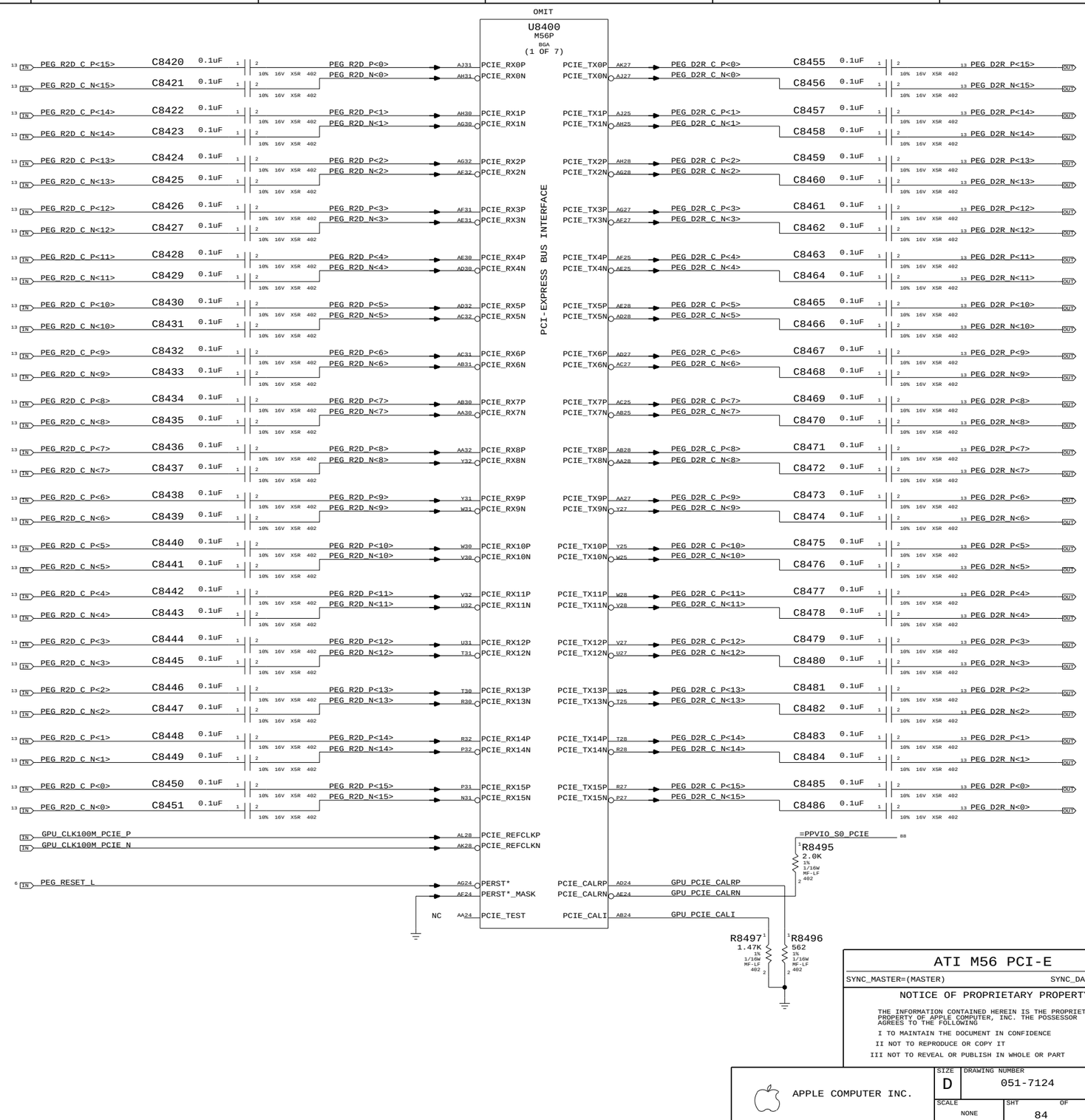
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE

SHT 83 OF 110





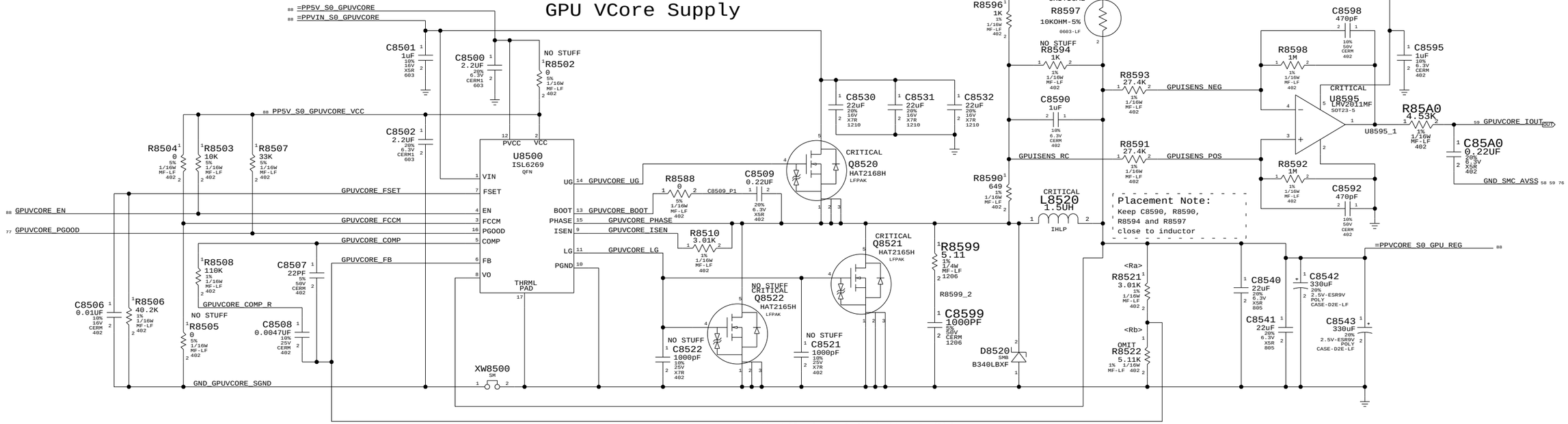
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 84 OF 110	

GPU VCore Supply



Vout(low) = 0.6V * (1 + Ra/Rb)
Vout(high) = 0.6V * (1 + Ra/Req)
Req = Rb || Rc

GPU VCore Current Sense

Back-Bias Positive Supply

=PPVCORE_S0_GPU_BBP — =PPVOUT_S0_GPUBBP_LDO

Back-Bias Negative Supply

=PNVOUT_S0_GPUBBN_REG

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

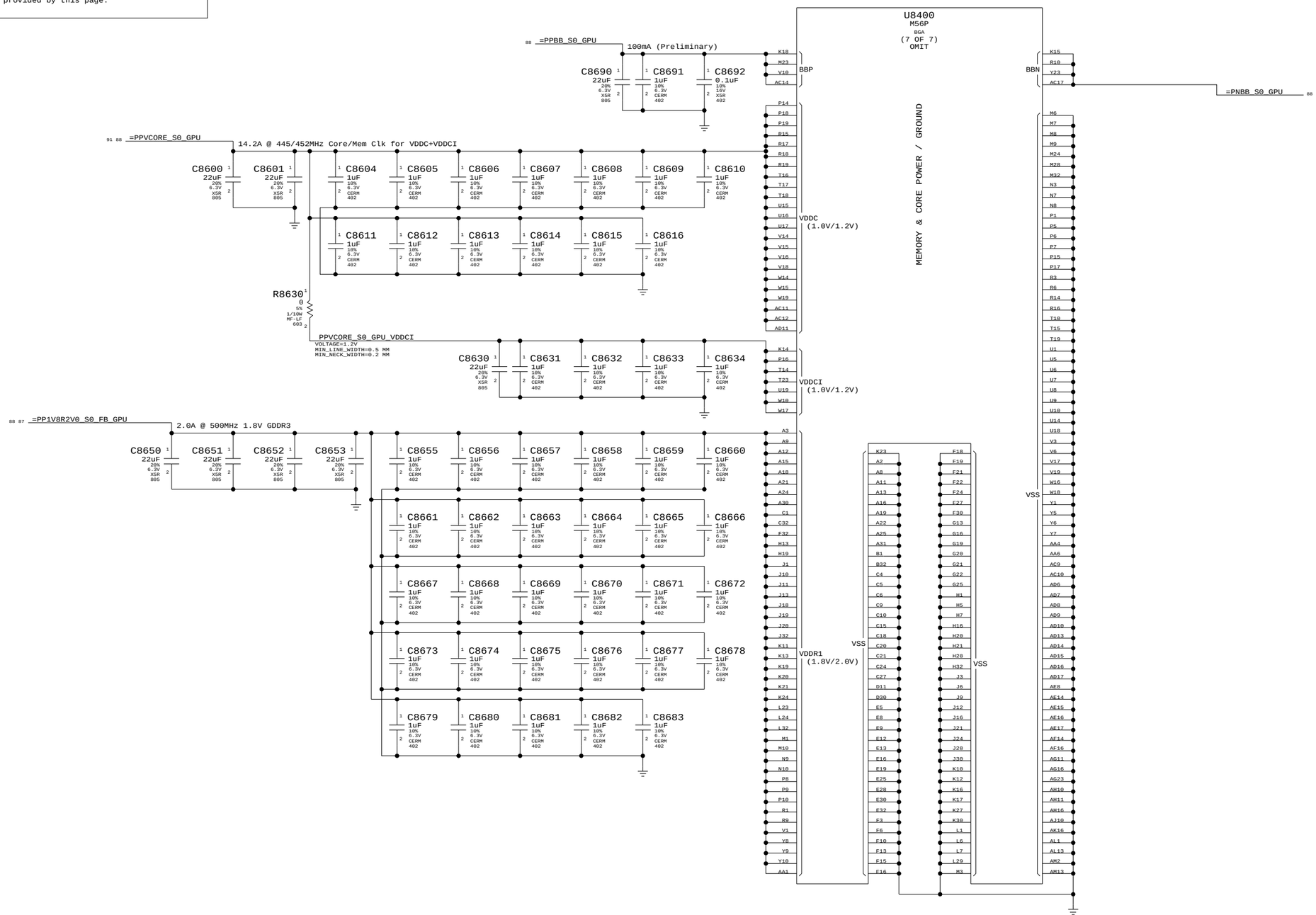
SCALE	SHT	OF
NONE	85	110

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

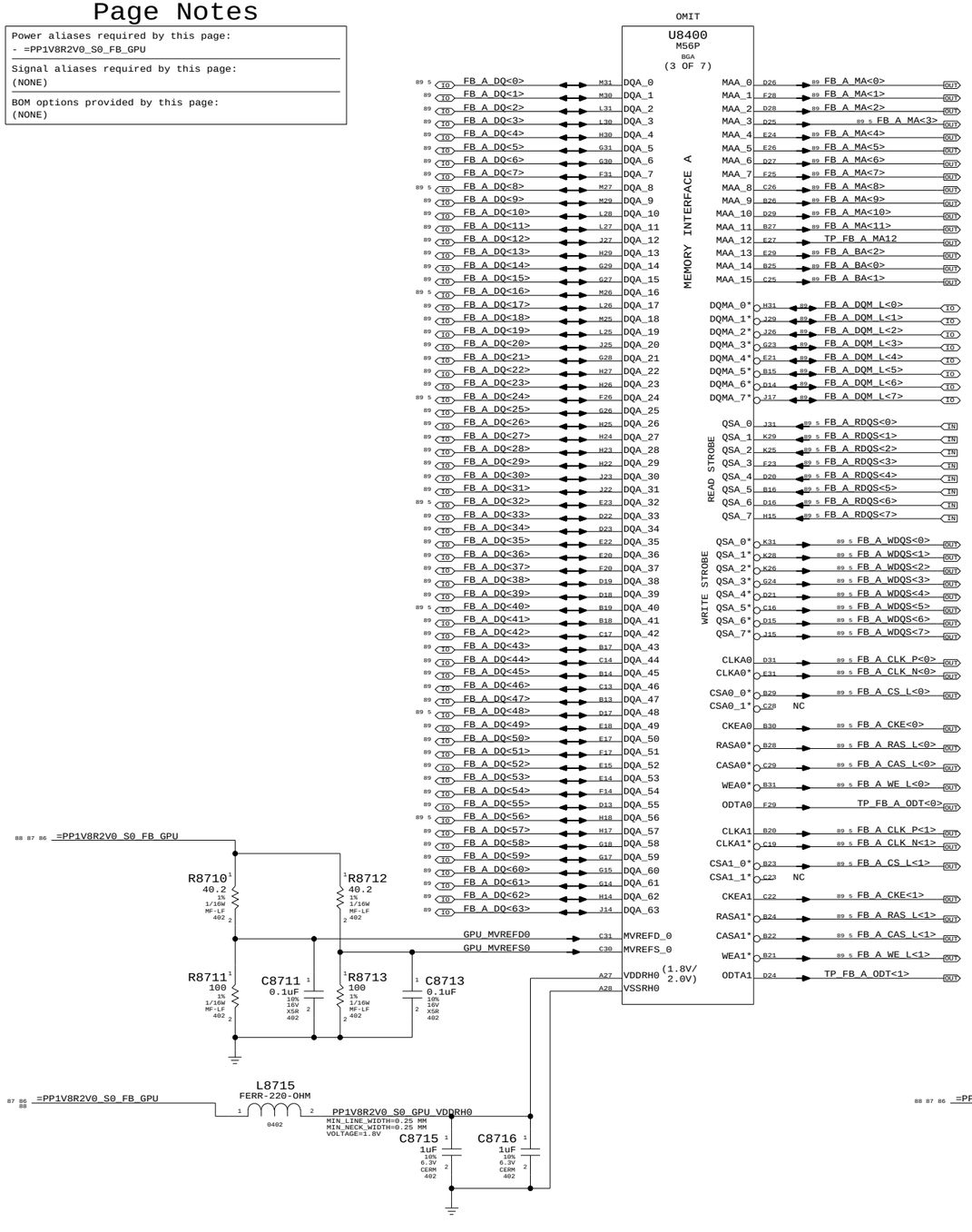
SCALE	SHT	OF
NONE	86	110

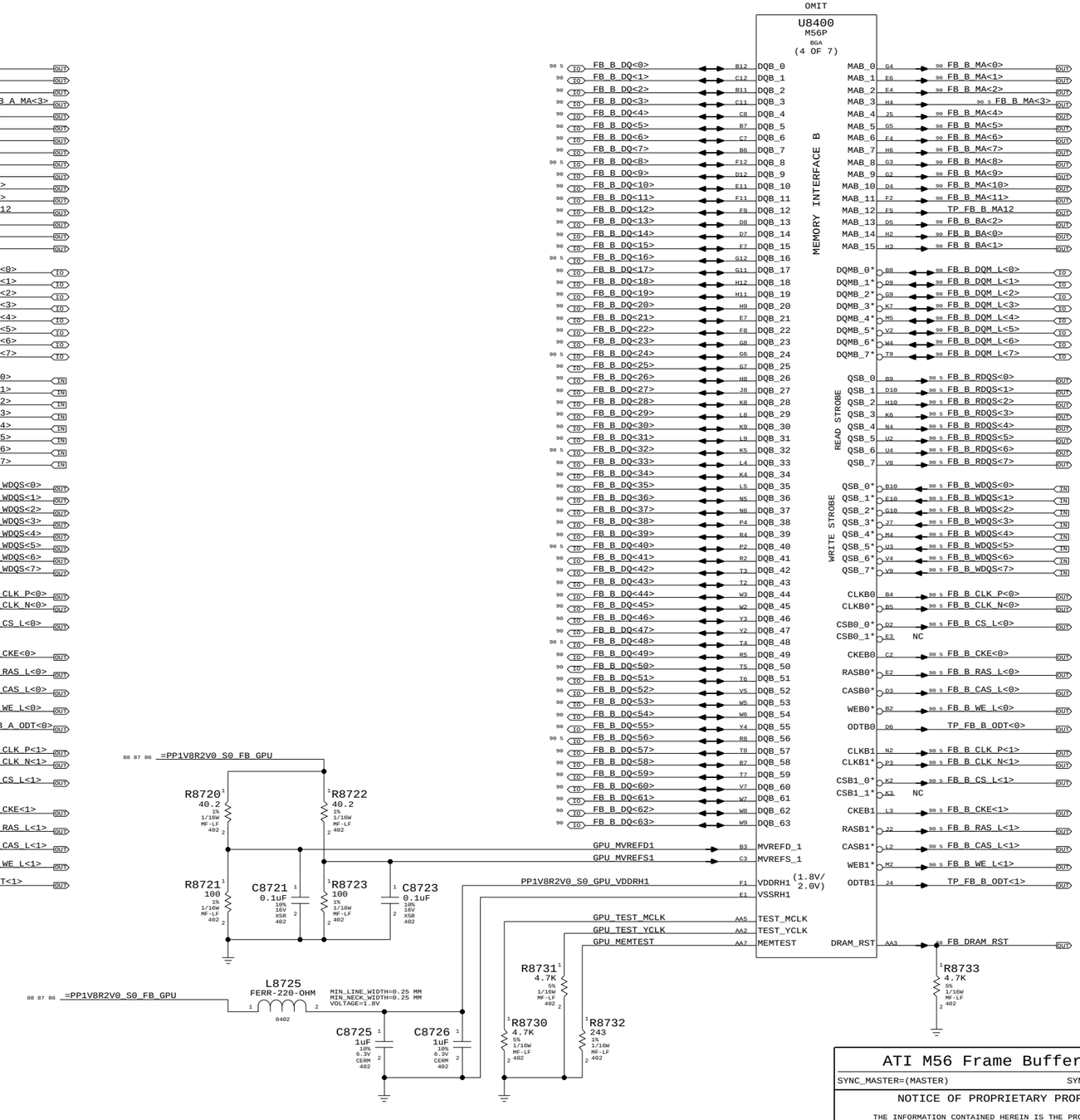
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 87 OF 110	

"S0" GPU RAILS

ONLY ON IN RUN

PP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVCORE_S0_GPU_REG 85
=PPVCORE_S0_GPU 86 91
=PPVCORE_S0_GPU_BBP 85

PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V
10 1/16W R8800 2 603 MF-LF 5%
=PP5V_S0_GPUVCORE 85
GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PP1V2_S0_PCIE_GPU_VDDR 84
=PP1V2_S0_PCIE_GPU_PVDD 84
=PPVIO_S0_PCIE 84
=PP1V2_S0_REG 77
=PP1V2_S0_GPU_VDDPLL 91

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVOUT_S0_GPUBBP_LDO 85
=PPBB_S0_GPU 86

PNBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0
=PNVOUT_S0_GPUBBN_REG 85
=PNBB_S0_GPU 86

83 76 61 59 41 26 10 6 PP3V3_S0
=PP3V3_S0_GPUBBP
=PP3V3_S0_GPUBBCTL
=PP3V3_DDC_DVI 97
=PP3V3_S0_LCD 94
=PP3V3_S0_GPU_VDDR3 88 91
=PP3V3_S0_GPU 91 93 97
=PP3V3_S0_GPUBBN
=PP3V3_S0_GPU_CLOCKS
=PP3V3_DDC_LCD 94
=PP3V3_GPU 94

83 6 PP2V5_S0
=PP2V5_S0_GPU_PVDD 91
=PP2V5_S0_GPU_VDD25 91
=PP2V5_S0_GPU_VDDC_CT 91
=PP2V5_S0_GPU 93

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V
=PP1V8_S0_FB_VDD 89 90
=PP1V8R3V3_S0_GPU_VDDR4 91
=PP1V8R3V3_S0_GPU_VDDR5 91
=PP1V8_S0_FB_VDDQ 89 90
PP1V8_S0 78
=PP1V8R2V0_S0_FB_GPU 86 87

83 82 81 80 79 78 77 57 6 5 PP12V_S5
=PPVIN_S0_GPUVCORE 85

83 6 PP12V_S0
=PP12V_GPU 94

97 83 75 6 PP5V_S0
=PP5V_S0_GPUBBCTL
=PP5V_S0_DVI_DDC 97
=PP5V_S0_GPUISENS 85

85 GPUVCORE_EN
33 1/16W R8801 2 402 MF-LF 5%
PM_SLP_S3_L 23 58 77 79

87 FB_DRAM_RST
MAKE_BASE=TRUE
DRAM_RST 5 89 90

M56 GPIOS

=PP3V3_S0_GPU_VDDR3 88 91

94 91 GPU_GPIO_0
10K 1/16W R8813 2 402 MF-LF 5%

GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
10K 1/16W R8802 2 402 MF-LF 5%

GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
NOSTUFF 10K 1/16W R8803 2 402 MF-LF 5%

91 GPU_GPIO_3
NOSTUFF 10K 1/16W R8804 2 402 MF-LF 5%

91 GPU_GPIO_4
NOSTUFF 10K 1/16W R8805 2 402 MF-LF 5%

GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
10K 1/16W R8806 2 402 MF-LF 5%

91 GPU_GPIO_6
NOSTUFF 10K 1/16W R8807 2 402 MF-LF 5%

TP_GPU_GPIO_7
MAKE_BASE=TRUE
GPU_GPIO_7 91

91 GPU_GPIO_8
NOSTUFF 10K 1/16W R8808 2 402 MF-LF 5%

NC_GPU_GPIO_10
MAKE_BASE=TRUE
GPU_GPIO_10 91

91 GPU_GPIO_9
NOSTUFF 10K 1/16W R8809 2 402 MF-LF 5%

91 GPU_GPIO_13
NOSTUFF 10K 1/16W R8812 2 402 MF-LF 5%
ATI_FB_256M

91 GPU_GPIO_12
10K 1/16W R8810 2 402 MF-LF 5%

91 GPU_GPIO_11
NOSTUFF 10K 1/16W R8811 2 402 MF-LF 5%

GPIO 9,13,12,11 = ROM ID CFG
INTERNAL PULL DOWN
0010 = 256 M APERATURE SIZE

ATI_FB_256M
91 GPU_GPIO_24
10K 1/16W R8830 2 402 MF-LF 5%

ATI_FB_HYNIX
91 GPU_GPIO_27
10K 1/16W R8831 2 402 MF-LF 5%

91 GPU_GPIO_28
10K 1/16W R8832 2 402 MF-LF 5%

TMDS_PANEL
91 GPU_GPIO_29
10K 1/16W R8833 2 402 MF-LF 5%

GPU_VCORE_LOW
MAKE_BASE=TRUE
GPU_GPIO_15 91

10K 1/16W R8850 2 402 MF-LF 5%

GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
MAKE_BASE=TRUE
GPU_GPIO_14 91

TP_GPU_GPIO_17
MAKE_BASE=TRUE
GPU_GPIO_17 91

TP_GPU_VGA_R
MAKE_BASE=TRUE
GPU_VGA_R 93

TP_GPU_VGA_G
MAKE_BASE=TRUE
GPU_VGA_G 93

TP_GPU_VGA_B
MAKE_BASE=TRUE
GPU_VGA_B 93

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE
GPU_VGA_HSYNC 93

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE
GPU_VGA_VSYNC 93

TP_GPU_TV_Y
MAKE_BASE=TRUE
GPU_TV_Y 93

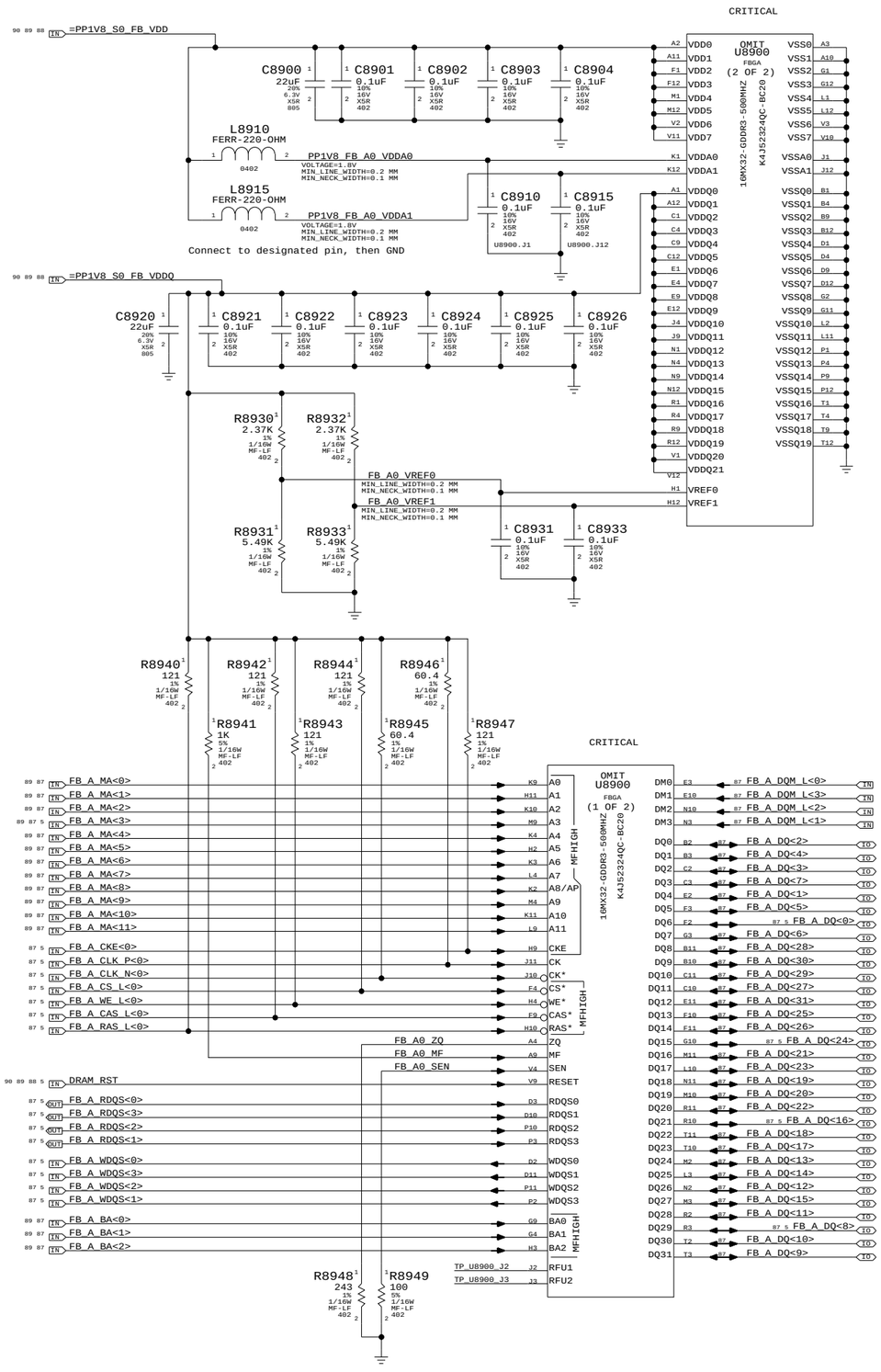
TP_GPU_TV_COMP
MAKE_BASE=TRUE
GPU_TV_COMP 93

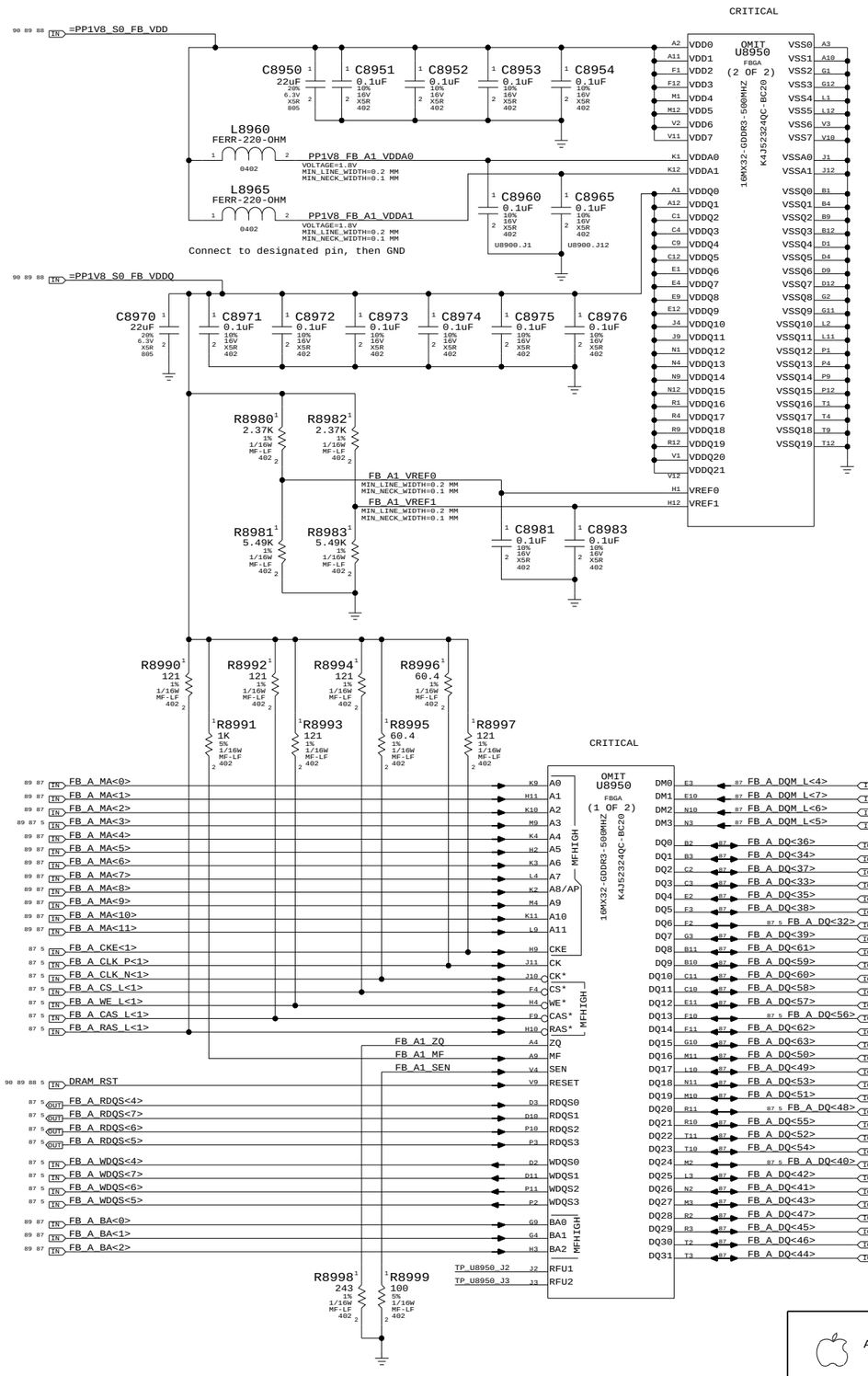
TP_GPU_TV_C
MAKE_BASE=TRUE
GPU_TV_C 93

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE
GPU_DDC_B_CLK 93

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE
GPU_DDC_B_DATA 93

GPU MISC





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

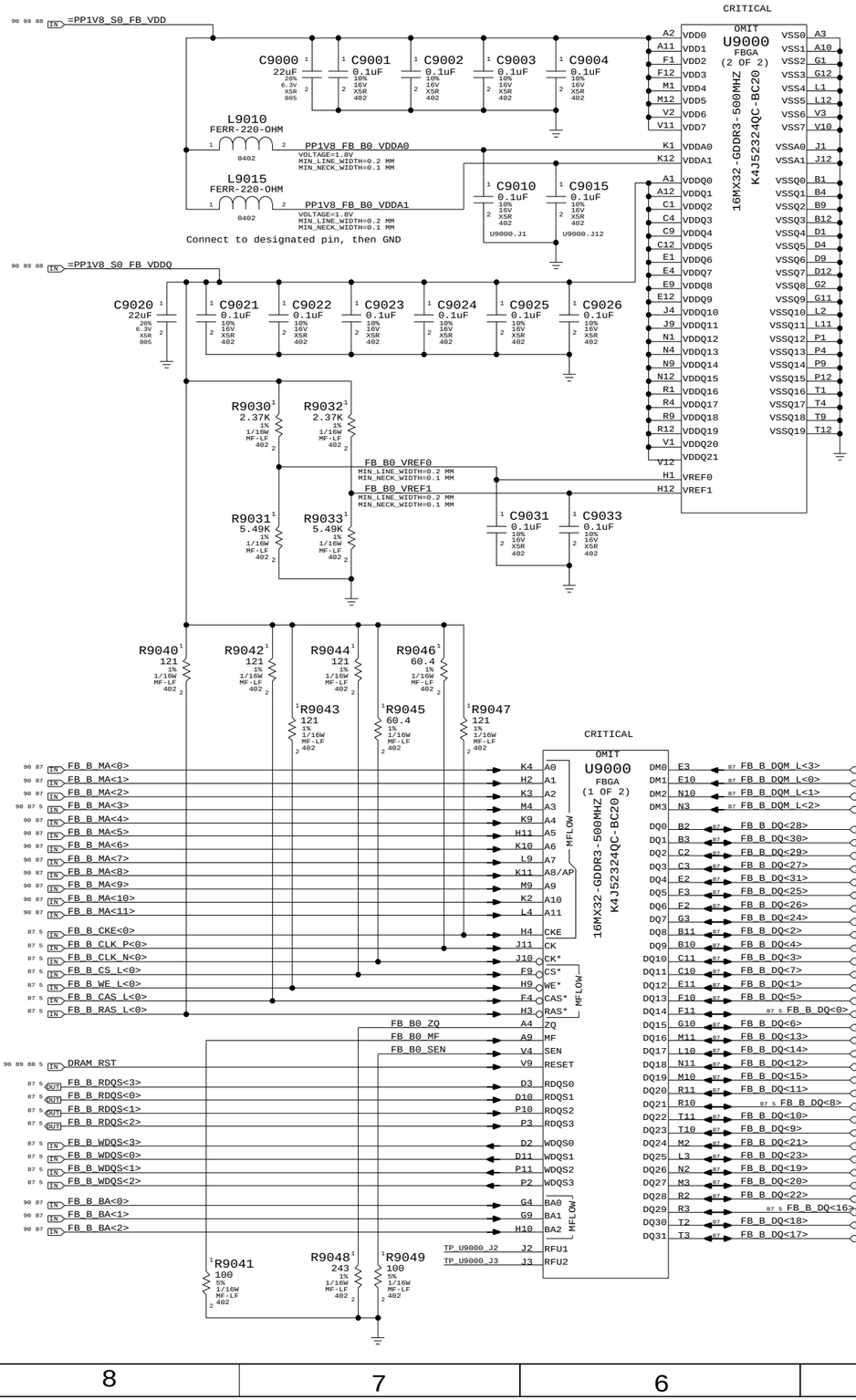
GDDR3 Frame Buffer A

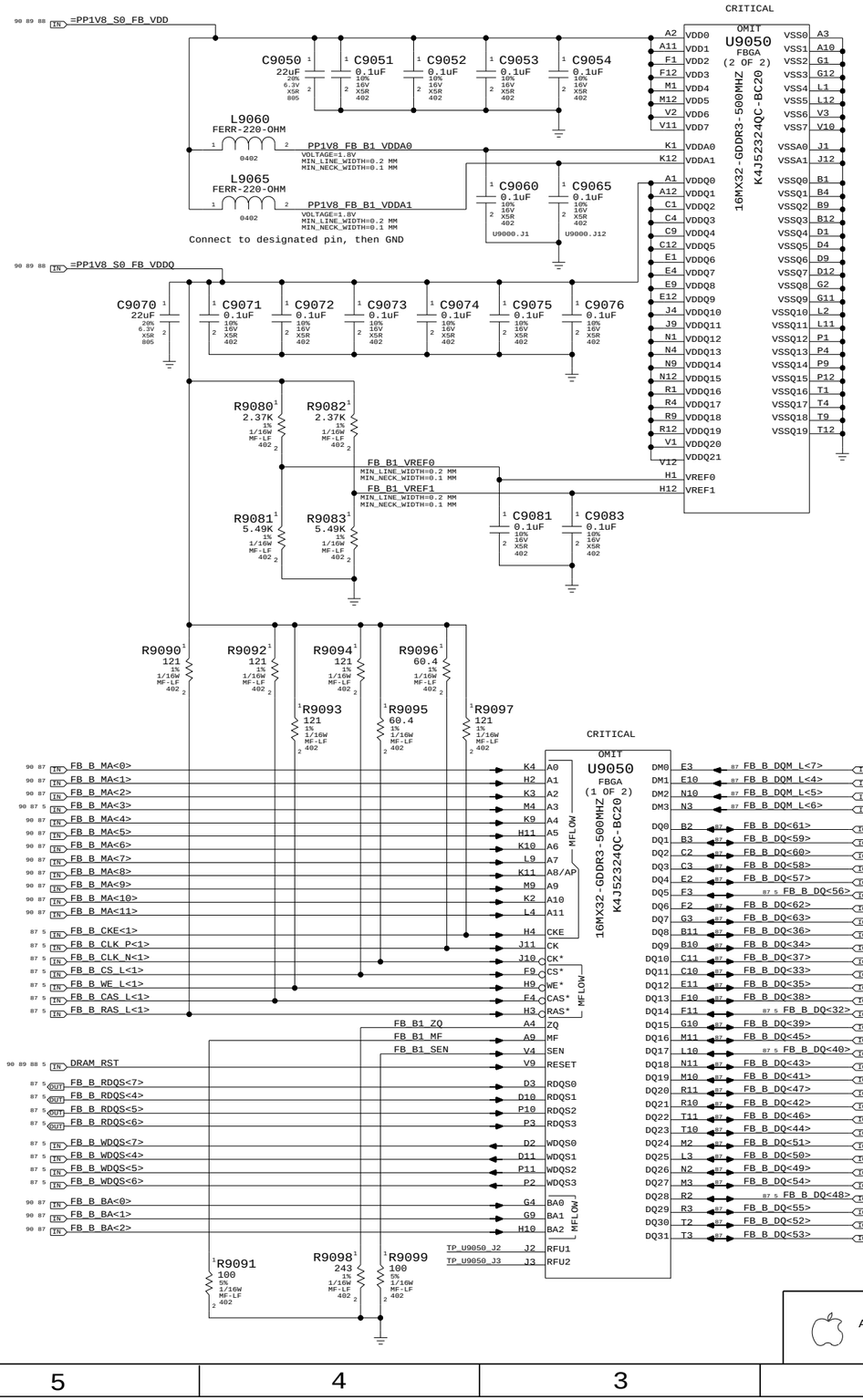
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	89	110





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

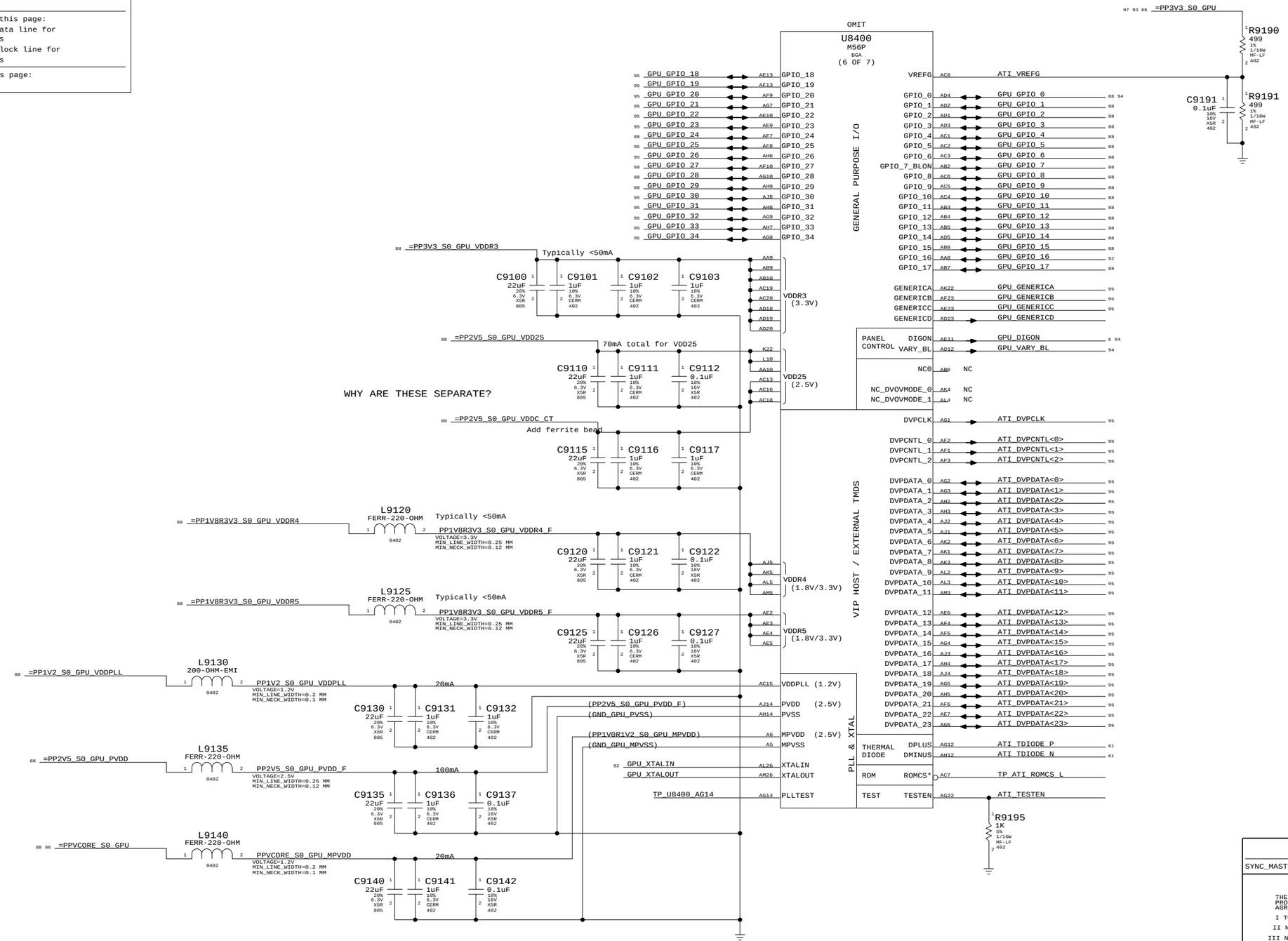
SCALE	SHT	OF
NONE	90	110

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

ATI M56 GPIO/DVO/Misc

APPLE COMPUTER INC.

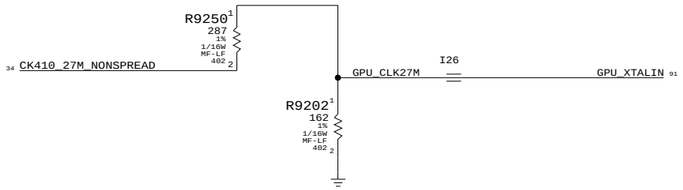
SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 91	OF 110

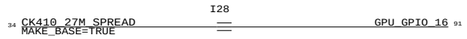
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8





GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	92	110

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents on this page: 605mA

88 =PP2V5_S0_GPU

L9300 FERR-220-OHM 0402
PP2V5_S0_GPU_TPVDD
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=2.5V
20mA peak
C9300 22uF 20% 6.3V X5R 805
C9301 1uF 10% 6.3V CERM 402
C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402
PP2V5_S0_GPU_TXVDDR
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.12 MM
VOLTAGE=2.5V
150mA peak
C9305 22uF 20% 6.3V X5R 805
C9306 1uF 10% 6.3V CERM 402
C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402
PP2V5_S0_GPU_AVDD
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.12 MM
VOLTAGE=2.5V
65mA peak
C9310 22uF 20% 6.3V X5R 805
C9311 1uF 10% 6.3V CERM 402
C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402
PP2V5_S0_GPU_VDD1DI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.12 MM
VOLTAGE=2.5V
20mA peak
C9315 22uF 20% 6.3V X5R 805
C9316 1uF 10% 6.3V CERM 402
C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402
PP2V5_S0_GPU_A2VDD
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.125 MM
VOLTAGE=2.5V
130mA peak
C9320 22uF 20% 6.3V X5R 805
C9321 1uF 10% 6.3V CERM 402
C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402
PP2V5_S0_GPU_VDD2DI
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.12 MM
VOLTAGE=2.5V
20mA peak
C9325 22uF 20% 6.3V X5R 805
C9326 1uF 10% 6.3V CERM 402
C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402
PP2V5_S0_GPU_LPVDD
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.12 MM
VOLTAGE=2.5V
20mA peak
C9330 22uF 20% 6.3V X5R 805
C9331 1uF 10% 6.3V CERM 402
C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402
PP2V5_S0_GPU_LVDDR
MIN_LINE_WIDTH=0.35 MM
MIN_NECK_WIDTH=0.125 MM
VOLTAGE=2.5V
200mA peak
C9340 22uF 20% 6.3V X5R 805
C9345 22uF 20% 6.3V X5R 805
C9341 1uF 10% 6.3V CERM 402
C9342 0.1uF 10% 16V X5R 402
C9346 0.1uF 10% 16V X5R 402
C9347 0.1uF 10% 16V X5R 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
AM8 TPVDD (2.5V)
AL8 TPVSS
AJ6 AK6 AL6 AM6 TXVDDR (2.5V)
AJ7 AK7 AK8 AL7 AM7 TXVSSR
AL25 AM25 AVDD (2.5V)
AJ24 AK25 AVSS
AK23 AVSSQ

DAC (CRT)
AM23 VDD1DI (2.5V)
AL23 VSS1DI
93 ATI_RSET AL22 RSET

DAC2 (TV/CRT2)
AL16 AM16 A2VDD (2.5V)
AL17 AM17 A2VSS
NC AL14 NC_A2VDDQ
AK13 A2VSSQ
AJ16 VDD2DI (2.5V)
AJ17 VSS2DI
93 ATI_R2SET AK14 R2SET

LVDS
AE19 LVDDR (2.5V)
AE18 LVPVSS
AC21 AC22 AD21 AD22 AE20 AE21 AE22 AE19 AE20 AE17 AE18 AE21 AE22 AG17 AG19 AH17 AH19 AJ19 AK17 LVSSR

MONITOR IDENTIFICATION
97 IN GPU_HPD AE11 HPD1

TMDS
TXCP AM9 → 97 TMDS_CLK_P OUT
TXCM AL9 → 97 TMDS_CLK_N OUT
TX0P AL10 → 97 TMDS_DATA_P<0> OUT
TX0M AK10 → 97 TMDS_DATA_N<0> OUT
TX1P AM11 → 97 TMDS_DATA_P<1> OUT
TX1M AL11 → 97 TMDS_DATA_N<1> OUT
TX2P AM12 → 97 TMDS_DATA_P<2> OUT
TX2M AL12 → 97 TMDS_DATA_N<2> OUT
TX3P AJ9 → 95 TMDS_DATA_P<3> OUT
TX3M AK9 → 95 TMDS_DATA_N<3> OUT
TX4P AJ11 → 95 TMDS_DATA_P<4> OUT
TX4M AK11 → 95 TMDS_DATA_N<4> OUT
TX5P AJ12 → 95 TMDS_DATA_P<5> OUT
TX5M AK12 → 95 TMDS_DATA_N<5> OUT

DAC (CRT)
R AK24 → 88 GPU_VGA_R OUT
G AM24 → 88 GPU_VGA_G OUT
B AL24 → 88 GPU_VGA_B OUT
HSYNC AJ23 → 88 GPU_VGA_HSYNC OUT
VSYNC AJ22 → 88 GPU_VGA_VSYNC OUT

DAC2 (TV/CRT2)
R2 AK15 → 97 GPU_R2 OUT
G2 AM15 → 97 GPU_G2 OUT
B2 AL15 → 97 GPU_B2 OUT
H2SYNC AE15 → 97 GPU_H2SYNC OUT
V2SYNC AG15 → 97 GPU_V2SYNC OUT
Y AJ15 → 88 GPU_TV_Y OUT
C AJ13 → 88 GPU_TV_C OUT
COMP AH15 → 88 GPU_TV_COMP OUT

LVDS
TXCLK_UP AJ21 → 94 LVDS_U_CLK_P OUT
TXCLK_UN AK21 → 94 LVDS_U_CLK_N OUT
TXOUT_U0P AG18 → 94 LVDS_U_DATA_P<0> OUT
TXOUT_U0N AH18 → 94 LVDS_U_DATA_N<0> OUT
TXOUT_U1P AK20 → 94 LVDS_U_DATA_P<1> OUT
TXOUT_U1N AJ20 → 94 LVDS_U_DATA_N<1> OUT
TXOUT_U2P AG20 → 94 LVDS_U_DATA_P<2> OUT
TXOUT_U2N AH20 → 94 LVDS_U_DATA_N<2> OUT
TXOUT_U3P AH21 → 94 LVDS_U_DATA_P<3> OUT
TXOUT_U3N AG21 → 94 LVDS_U_DATA_N<3> OUT
TXCLK_LP AM18 → 94 93 LVDS_L_CLK_P OUT
TXCLK_LN AL18 → 94 93 LVDS_L_CLK_N OUT
TXOUT_L0P AL19 → 94 93 LVDS_L_DATA_P<0> OUT
TXOUT_L0N AK19 → 94 93 LVDS_L_DATA_N<0> OUT
TXOUT_L1P AM20 → 94 93 LVDS_L_DATA_P<1> OUT
TXOUT_L1N AL20 → 94 93 LVDS_L_DATA_N<1> OUT
TXOUT_L2P AM21 → 94 93 LVDS_L_DATA_P<2> OUT
TXOUT_L2N AL21 → 94 93 LVDS_L_DATA_N<2> OUT
TXOUT_L3P AJ18 → 94 LVDS_L_DATA_P<3> OUT
TXOUT_L3N AK18 → 94 LVDS_L_DATA_N<3> OUT

MONITOR IDENTIFICATION
DDC1CLK AH23 → 97 GPU_DDC_A_CLK IO
DDC1DATA AH22 → 97 GPU_DDC_A_DATA IO
DDC2CLK AG13 → 88 GPU_DDC_B_CLK IO
DDC2DATA AH13 → 88 GPU_DDC_B_DATA IO
DDC3CLK AF12 → 94 93 GPU_DDC_C_CLK IO
DDC3DATA AE12 → 94 93 GPU_DDC_C_DATA IO

ATI_RSET 93
ATI_R2SET 93
R9350 499 1% 1/16W MF-LF 402
R9351 715 1% 1/16W MF-LF 402

TERMINATION FOR TMDS USAGE OF LVDS PINS
PLACE CLOSE TO GPU (U8400)

94 93 LVDS_L_CLK_P → TMDS_PANEL R9370 100 5% 1/10W MF-LF 402
94 93 LVDS_L_CLK_N
94 93 LVDS_L_DATA_P<0> → TMDS_PANEL R9371 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<0>
94 93 LVDS_L_DATA_P<1> → TMDS_PANEL R9372 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<1>
94 93 LVDS_L_DATA_P<2> → TMDS_PANEL R9373 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<2>

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

97 91 88 =PP3V3_S0_GPU
R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402
94 93 GPU_DDC_C_CLK
94 93 GPU_DDC_C_DATA

ATI M56 Video Interfaces

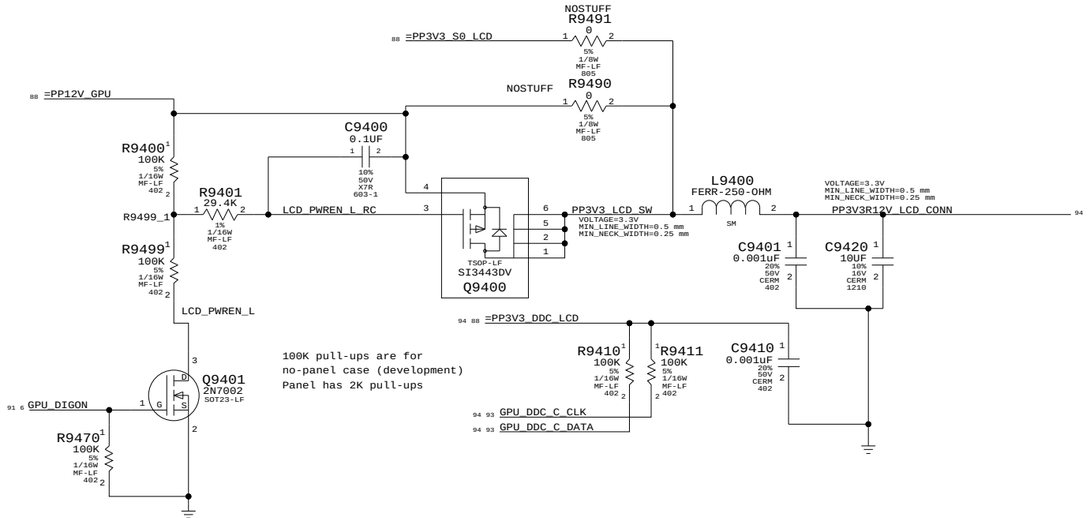
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

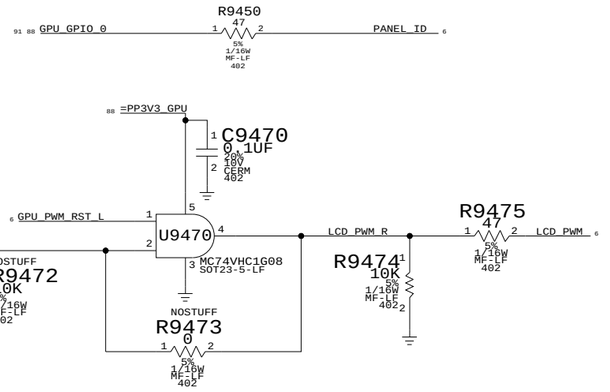
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE	SHT	OF
NONE	93	110

LCD (LVDS) INTERFACE





Internal Display Conns			
SYNC_MASTER=BOZEMAN	SYNC_DATE=04/27/2005		

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	13
	SCALE	SHT	OF
	NONE	94	110

TP_TMDS_DATA_P<3> == TMDS_DATA_P<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<3> == TMDS_DATA_N<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<4> == TMDS_DATA_P<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<4> == TMDS_DATA_N<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<5> == TMDS_DATA_P<5> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<5> == TMDS_DATA_N<5> 93
MAKE_BASE=TRUE

TP_ATI_DVPDATA<23> == ATI_DVPDATA<23> 91
MAKE_BASE=TRUE

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MAKE_BASE=TRUE

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MAKE_BASE=TRUE

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MAKE_BASE=TRUE

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MAKE_BASE=TRUE

TP_ATI_DVPDATA<6> == ATI_DVPDATA<6> 91
MAKE_BASE=TRUE

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MAKE_BASE=TRUE

TP_ATI_DVPDATA<4> == ATI_DVPDATA<4> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<3> == ATI_DVPDATA<3> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<2> == ATI_DVPDATA<2> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<1> == ATI_DVPDATA<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<0> == ATI_DVPDATA<0> 91
MAKE_BASE=TRUE

TP_ATI_DVPCLK == ATI_DVPCLK 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<0> == ATI_DVPCNTL<0> 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<1> == ATI_DVPCNTL<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<2> == ATI_DVPCNTL<2> 91
MAKE_BASE=TRUE

TP_GPU_GPIO<34> == GPU_GPIO_34 91
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TP_GPU_GPIO<33> == GPU_GPIO_33 91
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TP_GPU_GPIO<32> == GPU_GPIO_32 91
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TP_GPU_GPIO<31> == GPU_GPIO_31 91
MAKE_BASE=TRUE

TP_GPU_GPIO<30> == GPU_GPIO_30 91
MAKE_BASE=TRUE

TP_GPU_GPIO<26> == GPU_GPIO_26 91
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TP_GPU_GPIO<25> == GPU_GPIO_25 91
MAKE_BASE=TRUE

TP_GPU_GPIO<23> == GPU_GPIO_23 91
MAKE_BASE=TRUE

TP_GPU_GPIO<22> == GPU_GPIO_22 91
MAKE_BASE=TRUE

TP_GPU_GPIO<21> == GPU_GPIO_21 91
MAKE_BASE=TRUE

TP_GPU_GPIO<20> == GPU_GPIO_20 91
MAKE_BASE=TRUE

TP_GPU_GPIO<19> == GPU_GPIO_19 91
MAKE_BASE=TRUE

TP_GPU_GPIO<18> == GPU_GPIO_18 91
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TP_GPU_GENERICA == GPU_GENERICA 91
MAKE_BASE=TRUE

TP_GPU_GENERICB == GPU_GENERICB 91
MAKE_BASE=TRUE

TP_GPU_GENERICC == GPU_GENERICC 91
MAKE_BASE=TRUE

M56 TPS

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13
SCALE: NONE	SHT 95 OF 110	

DVI INTERFACE

PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

PLACE FILTER CLOSE
TO TMDS CONNECTOR

TMDS_DATA_N<0> — R9701 182 1% 1/10W MF-LF 402 — TMDS_DATA_P<0>
TMDS_DATA_N<1> — R9706 182 1% 1/10W MF-LF 402 — TMDS_DATA_P<1>
TMDS_DATA_N<2> — R9707 182 1% 1/10W MF-LF 402 — TMDS_DATA_P<2>
TMDS_CLK_N — R9716 90.9 1% 1/10W MF-LF 402 — R9717 90.9 1% 1/10W MF-LF 402 — TMDS_CLK_P
TMDS_CK_TERM: C9700 22PF 5% 50V CERM 402
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

TMDS_DATA_N<0>	L9700 SYM_VER-1	TMDS_CONN_DN<0>
TMDS_DATA_P<0>	2012M 90-OHM-300MA	TMDS_CONN_DP<0>
TMDS_DATA_N<1>	L9701 SYM_VER-1	TMDS_CONN_DN<1>
TMDS_DATA_P<1>	2012M 90-OHM-300MA	TMDS_CONN_DP<1>
TMDS_DATA_N<2>	L9702 SYM_VER-1	TMDS_CONN_DN<2>
TMDS_DATA_P<2>	2012M 90-OHM-300MA	TMDS_CONN_DP<2>
TMDS_CLK_N	L9703 165-OHM SM	TMDS_CONN_CLKN
TMDS_CLK_P		TMDS_CONN_CLKP

All L97xx: CRITICAL. All TMDS_CONN_*: DIFFERENTIAL_PAIR=TMDS_CONN_*, NO_TEST=TRUE.

NOSTUFF R9700 0 — NOSTUFF R9702 0 — NOSTUFF R9703 0 — NOSTUFF R9705 0 — NOSTUFF R9704 0 — NOSTUFF R9709 0 — NOSTUFF R9708 0 — NOSTUFF R9715 0

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC — CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL
J9710
MINI-DVI-M60
F-ST-SM

DVI_HPD_UF	25	1	TMDS_CONN_DP<2>
	17	9	
DVI_DDC_CLK_UF	26	2	TMDS_CONN_DN<2>
DVI_DDC_DATA_UF	18	10	
	27	3	TMDS_CONN_DP<1>
	19	11	
	28	4	TMDS_CONN_DN<1>
VGA_B	20	12	
VGA_HSYNC	29	5	TMDS_CONN_DP<0>
		13	
	30	6	TMDS_CONN_DN<0>
VGA_G	22	14	
VGA_VSYNC	31	7	TMDS_CONN_CLKP
		15	
	32	8	TMDS_CONN_CLKN
VGA_R	24	16	
GND_CHASSIS_SLOT	33	34	GND_CHASSIS_VGA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION

3V LEVEL SHIFTERS

PP5V_S0 — R9710 4.7K — R9712 4.7K — =PP3V3_DDC_DVI — R9720 10K

DVI_DDC_CLK_UF — R9711 100 — DVI_DDC_CLK — Q9711 2N7002DW-X-F SOT-363 — GPU_DDC_A_CLK
C9711 100PF 5% 50V CERM 402

DVI_DDC_DATA_UF — R9713 100 — DVI_DDC_DATA — Q9711 2N7002DW-X-F SOT-363 — GPU_DDC_A_DATA — R9721 10K
C9713 100PF 5% 50V CERM 402

DVI_HPD_UF — R9714 20K — GPU_HPD — R9722 100K — D9700 CASE425 MMSZ4681XXG
C9710 0.01UF 20% 50V CERM 603
C9714 100PF 5% 50V CERM 402

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

GPU_B2	FL9740 LCFILTER CRITICAL SM-220MHZ-LF	VGA_B	R9740 75 1% 1/10W MF-LF 402 — C9740 3.3PF 0.25% 50V CERM 402
GPU_G2	FL9741 LCFILTER CRITICAL SM-220MHZ-LF	VGA_G	R9741 75 1% 1/10W MF-LF 402 — C9741 3.3PF 0.25% 50V CERM 402
GPU_R2	FL9742 LCFILTER CRITICAL SM-220MHZ-LF	VGA_R	R9742 75 1% 1/10W MF-LF 402 — C9742 3.3PF 0.25% 50V CERM 402

VGA SYNC BUFFERS

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

=PP3V3_S0_GPU — C9750 0.1UF 20% 10V CERM 402

U9700 74LC125 125 TSSOP

GPU_V2SYNC — GPU_VSYNC_BUF — R9750 33 5% 1/10W MF-LF 402 — VGA_VSYNC

GPU_H2SYNC — GPU_HSYNC_BUF — R9751 33 5% 1/10W MF-LF 402 — VGA_HSYNC (NO_TEST=TRUE)

External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	13

SCALE: NONE — SHT 97 OF 110

```
Title:        Basenet Report
Design:       m60
Date:         May 12 10:16:43 2006

Base nets and synonyms for m60_lib.M60(@m60_lib.m60(sch_1))
Base Signal           Synonyms                               Location([Zone][dir])

0V7_REF               0V7_REF - @m60_lib.M60                 79A3
1V0_REF               1V0_REF - @m60_lib.M60                 79A5 80A5 81A5 81B3
1V2REG_BOOT           1V2REG_BOOT - @m60_lib.M60             77C3
1V2REG_ITH            1V2REG_ITH - @m60_lib.M60              77B4
1V2REG_ITH_RC         1V2REG_ITH_RC - @m60_lib.M60           77B4
1V2REG_MODE           1V2REG_MODE - @m60_lib.M60             77C4
1V2REG_PGOOD          1V2REG_PGOOD - @m60_lib.M60            77B3
1V2REG_RT             1V2REG_RT - @m60_lib.M60               77C4
1V2REG_RUNSS          1V2REG_RUNSS - @m60_lib.M60            77B4
1V2REG_SGND           1V2REG_SGND - @m60_lib.M60             77A6
1V2REG_SW             1V2REG_SW - @m60_lib.M60               77B3
1V2REG_SW_FIL         1V2REG_SW_FIL - @m60_lib.M60           77B3
1V2REG_VBIAS          1V2REG_VBIAS - @m60_lib.M60            77C4
1V2REG_VFB            1V2REG_VFB - @m60_lib.M60              77B4
1V3_REF               1V3_REF - @m60_lib.M60                 80B3
1V05REG_NB_BOOT       1V05REG_NB_BOOT - @m60_lib.M60         81C6
1V05REG_NB_BOOT_R     1V05REG_NB_BOOT_R - @m60_lib.M60       81C5
1V05REG_NB_COMP       1V05REG_NB_COMP - @m60_lib.M60         81C6
1V05REG_NB_COMP_R     1V05REG_NB_COMP_R - @m60_lib.M60       81C5
1V05REG_NB_FB         1V05REG_NB_FB - @m60_lib.M60           81C5
1V05REG_NB_FB_R       1V05REG_NB_FB_R - @m60_lib.M60         81C2
1V05REG_NB_FS_DIS     1V05REG_NB_FS_DIS - @m60_lib.M60       81C7
1V05REG_NB_LDO_DR     1V05REG_NB_LDO_DR - @m60_lib.M60       81C7
1V05REG_NB_LDO_FB     1V05REG_NB_LDO_FB - @m60_lib.M60       81C7
1V05REG_NB_LGATE      1V05REG_NB_LGATE - @m60_lib.M60        81C6
1V05REG_NB_PVCC5      1V05REG_NB_PVCC5 - @m60_lib.M60        81D7
1V05REG_NB_SNUB       1V05REG_NB_SNUB - @m60_lib.M60         81C3
1V05REG_NB_SWITCHNOD  1V05REG_NB_SWITCHNODE -                81C5
E                     @m60_lib.M60
1V05REG_NB_UGATE      1V05REG_NB_UGATE - @m60_lib.M60        81D6
1V05REG_NB_VCC5       1V05REG_NB_VCC5 - @m60_lib.M60         81D7
1V5REG_PCIE_BOOT      1V5REG_PCIE_BOOT - @m60_lib.M60        80C6
1V5REG_PCIE_BOOT_R    1V5REG_PCIE_BOOT_R - @m60_lib.M60      80C5
1V5REG_PCIE_COMP      1V5REG_PCIE_COMP - @m60_lib.M60        80C6
1V5REG_PCIE_COMP_R    1V5REG_PCIE_COMP_R - @m60_lib.M60      80C5
1V5REG_PCIE_FB        1V5REG_PCIE_FB - @m60_lib.M60          80C5
1V5REG_PCIE_FB_R      1V5REG_PCIE_FB_R - @m60_lib.M60        80C2
1V5REG_PCIE_FS_DIS    1V5REG_PCIE_FS_DIS - @m60_lib.M60      80C7
1V5REG_PCIE_LDO_DR    1V5REG_PCIE_LDO_DR - @m60_lib.M60      80C7
1V5REG_PCIE_LDO_FB    1V5REG_PCIE_LDO_FB - @m60_lib.M60      80C7
1V5REG_PCIE_LGATE     1V5REG_PCIE_LGATE - @m60_lib.M60       80C6
1V5REG_PCIE_PVCC5     1V5REG_PCIE_PVCC5 - @m60_lib.M60       80D7
1V5REG_PCIE_SNUB      1V5REG_PCIE_SNUB - @m60_lib.M60        80C3
1V5REG_PCIE_SWITCHNO  1V5REG_PCIE_SWITCHNODE -               80C5
DE                    @m60_lib.M60
1V5REG_PCIE_UGATE     1V5REG_PCIE_UGATE - @m60_lib.M60       80D6
1V5REG_PCIE_VCC5      1V5REG_PCIE_VCC5 - @m60_lib.M60        80D7
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1V8REG_DDR_BOOT_R     1V8REG_DDR_BOOT_R - @m60_lib.M60       79D5
1V8REG_DDR_COMP       1V8REG_DDR_COMP - @m60_lib.M60         79C6
1V8REG_DDR_COMP_R     1V8REG_DDR_COMP_R - @m60_lib.M60       79C5
1V8REG_DDR_FB         1V8REG_DDR_FB - @m60_lib.M60           79C5
1V8REG_DDR_FB_R       1V8REG_DDR_FB_R - @m60_lib.M60         79C2
1V8REG_DDR_FS_DIS     1V8REG_DDR_FS_DIS - @m60_lib.M60       79C7
1V8REG_DDR_LDO_DR     1V8REG_DDR_LDO_DR - @m60_lib.M60       79C7
1V8REG_DDR_LDO_FB     1V8REG_DDR_LDO_FB - @m60_lib.M60       79C7
1V8REG_DDR_LGATE      1V8REG_DDR_LGATE - @m60_lib.M60        79C6
1V8REG_DDR_PVCC5      1V8REG_DDR_PVCC5 - @m60_lib.M60        79D7
1V8REG_DDR_SNUB       1V8REG_DDR_SNUB - @m60_lib.M60         79C3
1V8REG_DDR_SWITCHNOD  1V8REG_DDR_SWITCHNODE -                79C5
E                     @m60_lib.M60
1V8REG_DDR_UGATE      1V8REG_DDR_UGATE - @m60_lib.M60        79D6
1V8REG_DDR_VCC5       1V8REG_DDR_VCC5 - @m60_lib.M60         79D7
1V8REG_GPU_BOOT       1V8REG_GPU_BOOT - @m60_lib.M60         78C6
1V8REG_GPU_BOOT_R     1V8REG_GPU_BOOT_R - @m60_lib.M60       78C5
1V8REG_GPU_COMP       1V8REG_GPU_COMP - @m60_lib.M60         78B6
1V8REG_GPU_COMP_R     1V8REG_GPU_COMP_R - @m60_lib.M60       78B6
1V8REG_GPU_FB         1V8REG_GPU_FB - @m60_lib.M60           78B5
1V8REG_GPU_FB_R       1V8REG_GPU_FB_R - @m60_lib.M60         78B2
1V8REG_GPU_FS_DIS     1V8REG_GPU_FS_DIS - @m60_lib.M60       78B7
1V8REG_GPU_LDO_DR     1V8REG_GPU_LDO_DR - @m60_lib.M60       78C7
1V8REG_GPU_LDO_FB     1V8REG_GPU_LDO_FB - @m60_lib.M60       78B7
1V8REG_GPU_LGATE      1V8REG_GPU_LGATE - @m60_lib.M60        78B6
1V8REG_GPU_PVCC5      1V8REG_GPU_PVCC5 - @m60_lib.M60        78C7
1V8REG_GPU_SNUB       1V8REG_GPU_SNUB - @m60_lib.M60         78B3
1V8REG_GPU_SWITCHNOD  1V8REG_GPU_SWITCHNODE -                78C5
E                     @m60_lib.M60
1V8REG_GPU_UGATE      1V8REG_GPU_UGATE - @m60_lib.M60        78C6
1V8REG_GPU_VCC5       1V8REG_GPU_VCC5 - @m60_lib.M60         78C7
2V3_REF               2V3_REF - @m60_lib.M60                 83B3
2V5_LDODR_C           2V5_LDODR_C - @m60_lib.M60             57C7
3V3REG_BOOT           3V3REG_BOOT - @m60_lib.M60             57D5
3V3REG_BOOT_R         3V3REG_BOOT_R - @m60_lib.M60           57D5
3V3REG_COMP           3V3REG_COMP - @m60_lib.M60             57C5
3V3REG_COMP_R         3V3REG_COMP_R - @m60_lib.M60           57C5
3V3REG_FB             3V3REG_FB - @m60_lib.M60               57D5
3V3REG_FB_R           3V3REG_FB_R - @m60_lib.M60             57C2
3V3REG_FS_DIS         3V3REG_FS_DIS - @m60_lib.M60           57C6
3V3REG_LDO_DR         3V3REG_LDO_DR - @m60_lib.M60           57D6
3V3REG_LDO_FB         3V3REG_LDO_FB - @m60_lib.M60           57C7
3V3REG_LGATE          3V3REG_LGATE - @m60_lib.M60            57D5
3V3REG_PVCC5          3V3REG_PVCC5 - @m60_lib.M60            57D6
3V3REG_SNUB           3V3REG_SNUB - @m60_lib.M60             57C3
3V3REG_SWITCHNODE     3V3REG_SWITCHNODE - @m60_lib.M60       57D5
3V3REG_UGATE          3V3REG_UGATE - @m60_lib.M60            57D5
3V3REG_VCC5           3V3REG_VCC5 - @m60_lib.M60             57D6
5VREG_BOOT            5VREG_BOOT - @m60_lib.M60              82D5
5VREG_BOOT_R          5VREG_BOOT_R - @m60_lib.M60            82D5
5VREG_COMP            5VREG_COMP - @m60_lib.M60              82C5
5VREG_COMP_R          5VREG_COMP_R - @m60_lib.M60            82C5
5VREG_FB              5VREG_FB - @m60_lib.M60                82D5
5VREG_FB_R            5VREG_FB_R - @m60_lib.M60              82C2
5VREG_FS_DIS          5VREG_FS_DIS - @m60_lib.M60            82C6
5VREG_LDO_DR          5VREG_LDO_DR - @m60_lib.M60            82D6
5VREG_LDO_FB          5VREG_LDO_FB - @m60_lib.M60            82C7
5VREG_LGATE           5VREG_LGATE - @m60_lib.M60             82D5
5VREG_PVCC5           5VREG_PVCC5 - @m60_lib.M60             82D6
5VREG_SNUB            5VREG_SNUB - @m60_lib.M60              82C3
5VREG_SWITCHNODE      5VREG_SWITCHNODE - @m60_lib.M60        82D5
5VREG_UGATE           5VREG_UGATE - @m60_lib.M60             82D5
5VREG_VCC5            5VREG_VCC5 - @m60_lib.M60              82D6
5V_AUDIO_LDODR_C      5V_AUDIO_LDODR_C - @m60_lib.M60        82C7
=I2C_HD_TEMP_SCL      =I2C_HD_TEMP_SCL - @m60_lib.M60        59C1 66B6
                      =I2C_ODD_TEMP_SCL - @m60_lib.M60       59C1 66B4
                      =SMB_THRM_CLK - @m60_lib.M60           10C3 59C1
                      SMB_B_S0_CLK - @m60_lib.M60            58B5 59C2 59D1
                      SMB_GPU_NB_THRM_CLK - @m60_lib.M60     59C1 61C3
                      SMB_B_S0_CLK - @m60_lib.M60            58B5 59C2 59D1
                      =SMB_THRM_CLK - @m60_lib.M60           10C3 59C1
                      =I2C_ODD_TEMP_SCL - @m60_lib.M60       59C1 66B4
=I2C_HD_TEMP_SDA      =I2C_HD_TEMP_SDA - @m60_lib.M60        59C1 66B6
                      =I2C_ODD_TEMP_SDA - @m60_lib.M60       59C1 66B4
                      =SMB_THRM_DATA - @m60_lib.M60          10C3 59C1
                      SMB_B_S0_DATA - @m60_lib.M60           58B5 59C2 59D1
                      SMB_GPU_NB_THRM_DATA - @m60_lib.M60    59C1 61C3
                      SMB_B_S0_DATA - @m60_lib.M60           58B5 59C2 59D1
                      =SMB_THRM_DATA - @m60_lib.M60          10C3 59C1
                      =I2C_ODD_TEMP_SDA - @m60_lib.M60       59C1 66B4
=I2C_MEM_SCL          =I2C_MEM_SCL - @m60_lib.M60            27D6 28A6 29A6
                      =SMB_AIRPORT_CLK - @m60_lib.M60        27D6 53B4
                      SMB_CK410_CLK - @m60_lib.M60           27D6 33B6
                      SMB_CLK - @m60_lib.M60                 23D5 27B8 27D7
                      SMB_CK410_CLK - @m60_lib.M60           27D6 33B6
                      =SMB_AIRPORT_CLK - @m60_lib.M60        27D6 53B4
=I2C_MEM_SDA          =I2C_MEM_SDA - @m60_lib.M60            27D6 28A6 29A6
                      =SMB_AIRPORT_DATA - @m60_lib.M60       27C6 53B4
                      SMB_CK410_DATA - @m60_lib.M60          27D6 33B6
                      SMB_DATA - @m60_lib.M60                23D5 27B8 27D7
                      SMB_CK410_DATA - @m60_lib.M60          27D6 33B6
                      =SMB_AIRPORT_DATA - @m60_lib.M60       27C6 53B4
=PP0V9_S0_MEMVTT_LDO  =PP0V9_S0_MEMVTT_LDO - @m60_lib.M60    6D4 31B3
                      =PP0V9_S0_MEM_TERM - @m60_lib.M60      6D4 30D4
                      PP0V9_S0 - @m60_lib.M60                6D6 79A3
                      =PP0V9_S0_MEM_TERM - @m60_lib.M60      6D4 30D4
=PP1V2_S0_GPU_VDDPLL  =PP1V2_S0_GPU_VDDPLL - @m60_lib.M60    88C6 91B8
                      =PPVIO_S0_PCIE - @m60_lib.M60          84A2 88C6
                      =PP1V2_S0_REG - @m60_lib.M60           77A1 88C6
                      =PP1V2_S0_PCIE_GPU_PVDD -              84C8 88D6
                      @m60_lib.M60
                      =PP1V2_S0_PCIE_GPU_VDDR -              84C8 88D6
                      @m60_lib.M60
                      PP1V2_GPU_IO_S0 - @m60_lib.M60         88D8
                      =PPVIO_S0_PCIE - @m60_lib.M60          84A2 88C6
                      =PP1V2_S0_REG - @m60_lib.M60           77A1 88C6
                      =PP1V2_S0_PCIE_GPU_VDDR -              84C8 88D6
                      @m60_lib.M60
                      =PP1V2_S0_PCIE_GPU_PVDD -              84C8 88D6
                      @m60_lib.M60
=PP1V2_S3_ENET        =PP1V2_S3_ENET - @m60_lib.M60          41A8 41D6 42B5
                      PP1V2_S3_ENET - @m60_lib.M60           42B5
=PP1V2_S3_LAN         =PP1V2_S3_LAN - @m60_lib.M60           6D3 42B8
                      PP1V2_S3 - @m60_lib.M60                6D4 77B1
=PP1V8_S0_FB_VDD      =PP1V8_S0_FB_VDD - @m60_lib.M60        88B6 89D5 89D8 90D5 90D8
                      =PP1V8_S0_FB_VDDQ - @m60_lib.M60       88B6 89D5 89D8 90D5 90D8
                      =PP1V8R2V0_S0_FB_GPU - @m60_lib.M60    86B8 87A5 87A8 87B5 87B8
                                                             88B6
                      PP1V8_S0 - @m60_lib.M60                78C2 88B6
                      =PP1V8R3V3_S0_GPU_VDDR5 -              88B6 91B7
                      @m60_lib.M60
                      =PP1V8R3V3_S0_GPU_VDDR4 -              88B6 91B7
                      @m60_lib.M60
                      PP1V8_S0 - @m60_lib.M60                78C2 88B6
                      PP1V8R2V0_S0_FB_GPU - @m60_lib.M60     88B8
                      =PP1V8_S0_FB_VDDQ - @m60_lib.M60       88B6 89D5 89D8 90D5 90D8
                      =PP1V8R3V3_S0_GPU_VDDR5 -              88B6 91B7
                      @m60_lib.M60
                      =PP1V8R3V3_S0_GPU_VDDR4 -              88B6 91B7
                      @m60_lib.M60
                      =PP1V8R2V0_S0_FB_GPU - @m60_lib.M60    86B8 87A5 87A8 87B5 87B8
                                                             88B6
=PP1V8_S3_MEM_NB      =PP1V8_S3_MEM_NB - @m60_lib.M60        6D3 6D3 14C2 16B6 19B8
                                                             19D7
                      =PP1V8_S0_MEMVTT - @m60_lib.M60        6D3 31C7
                      PP1V8_S3 - @m60_lib.M60                5D2 6D4 79C1
                      =PP1V8_S3_MEM - @m60_lib.M60           5C4 6D3 28B2 28C8 28D3
                                                             28D6 29B2 29D3 29D6
                      PP1V8_S3 - @m60_lib.M60                5D2 6D4 79C1
                      =PP1V8_S3_MEM - @m60_lib.M60           5C4 6D3 28B2 28C8 28D3
                                                             28D6 29B2 29D3 29D6
                      =PP1V8_S0_MEMVTT - @m60_lib.M60        6D3 31C7
=PP2V5_S0_NB_VCCA_3G  =PP2V5_S0_NB_VCCA_3GBG -               6B4 17D6 19A8 19C7
BG                    @m60_lib.M60
                      =PP2V5_S0_GPU - @m60_lib.M60           88B6 93C8
                      PP2V5_S0 - @m60_lib.M60                6B6 83A3 83B7 88C8
                      =PP2V5_S0_GPU_VDD25 - @m60_lib.M60     88B6 91C6
                      =PP2V5_S0_GPU_VDDC_CT -                88B6 91C6
                      @m60_lib.M60
                      =PP2V5_S0_GPU_PVDD - @m60_lib.M60      88B6 91A8
                      PP2V5_S0 - @m60_lib.M60                6B6 83A3 83B7 88C8
                      =PP2V5_S0_GPU_VDDC_CT -                88B6 91C6
                      @m60_lib.M60
                      =PP2V5_S0_GPU_VDD25 - @m60_lib.M60     88B6 91C6
                      =PP2V5_S0_GPU_PVDD - @m60_lib.M60      88B6 91A8
                      =PP2V5_S0_GPU - @m60_lib.M60           88B6 93C8
=PP2V5_S3_ENET        =PP2V5_S3_ENET - @m60_lib.M60          41D5 41D6 42C4
                      PP2V5_S3_ENET - @m60_lib.M60           42C4 43D8
=PP3V3_S0_NB          =PP3V3_S0_NB - @m60_lib.M60            6A4 14C7 14D6 19C7 20A4
                                                             20B4 20B4
                      =PP3V3_DDC_DVI - @m60_lib.M60          88C6 97D2
                      =PP3V3_DDC_LCD - @m60_lib.M60          88C6 94A7 94C7
                      =PP3V3_GPU - @m60_lib.M60              88C6 94B3
                      PP3V3_S0 - @m60_lib.M60                6B6 10D2 26B7 26C6 41D8
                                                             59D3 61C3 76D6 83D7 88C8
                      =PP3V3_S0_GPU - @m60_lib.M60           88C6 91D2 93A1 97B5
                      =PP3V3_S0_GPU_VDDR3 - @m60_lib.M60     88C6 88D3 91C6
                      =PP3V3_S0_LCD - @m60_lib.M60           88C6 94D7
                      =PP3V3_S0_AIRPORT - @m60_lib.M60       6A4 53C2
                      =PP3V3_S0_PCI - @m60_lib.M60           6A4 44D5
                      =PP3V3_S0_AUDIO - @m60_lib.M60         6A4 68D7 72A6 72C8 72D5
                                                             73B8 74B5 74C5 74D6
                      =PP3V3_S0_IMVP - @m60_lib.M60          6A4 75D8
                      =PP3V3_S0_CK410 - @m60_lib.M60         6A4 33C8 33D3 33D8 34D4
                      =PPSPD_S0_MEM - @m60_lib.M60           6A4 28A7 29A3 29A7
                      =PP3V3_S0_TPM - @m60_lib.M60           6B4 67C7 67D4
                      =PP3V3_S0_SB_3V3_1V5_VCCHDA -          6B4 24C3 25C4
                      @m60_lib.M60
                      =PP3V3_S0_ODD_TSENS - @m60_lib.M60     6B4 66B4
                      =PP3V3_S0_HD_TSENS - @m60_lib.M60      6B4 66B5
                      =PP3V3_S0_FAN - @m60_lib.M60           6B4 59A8 59B7 65B7 65C7
                                                             66C7
                      =PP3V3_S0_PATA - @m60_lib.M60          6B4 38D3
                      =PP3V3_S0_SB_PM - @m60_lib.M60         6B4 26D4
                      =PP3V3_S0_SB_PCI - @m60_lib.M60        6B4 26D1
                      =PP3V3_S0_SB_VCC3_3_IDE -              6B4 24C3 25B3
                      @m60_lib.M60
                      =PP3V3_S0_SB_VCC3_3_PCI -              6B4 24B3 25A3
                      @m60_lib.M60
                      =PP3V3_S0_SB_VCC3_3 - @m60_lib.M60     6B4 24B5 24B5 25B8 25C6
                      =PP3V3_S0_NB_VCC_HV - @m60_lib.M60     6B4 17C6 19A8 19C7
                      =PP3V3_S0_SB_GPIO - @m60_lib.M60       6B4 21C3 21D3 23B3 23D5
                      =PP3V3_S0_SB_VCCLAN3_3 -               6A4 24D3 25D3
                      @m60_lib.M60
                      =PP3V3_S0_SB - @m60_lib.M60            6B4 22B5 25D8 27C6
                      PP3V3_S0 - @m60_lib.M60                6B6 10D2 26B7 26C6 41D8
                                                             59D3 61C3 76D6 83D7 88C8
                      =PPSPD_S0_MEM - @m60_lib.M60           6A4 28A7 29A3 29A7
                      =PP3V3_S0_TPM - @m60_lib.M60           6B4 67C7 67D4
                      =PP3V3_S0_SB_VCCLAN3_3 -               6A4 24D3 25D3
                      @m60_lib.M60
                      =PP3V3_S0_SB_VCC3_3_PCI -              6B4 24B3 25A3
                      @m60_lib.M60
                      =PP3V3_S0_SB_VCC3_3_IDE -              6B4 24C3 25B3
                      @m60_lib.M60
                      =PP3V3_S0_SB_VCC3_3 - @m60_lib.M60     6B4 24B5 24B5 25B8 25C6
                      =PP3V3_S0_SB_PM - @m60_lib.M60         6B4 26D4
                      =PP3V3_S0_SB_PCI - @m60_lib.M60        6B4 26D1
                      =PP3V3_S0_SB_GPIO - @m60_lib.M60       6B4 21C3 21D3 23B3 23D5
                      =PP3V3_S0_SB_3V3_1V5_VCCHDA -          6B4 24C3 25C4
                      @m60_lib.M60
                      =PP3V3_S0_SB - @m60_lib.M60            6B4 22B5 25D8 27C6
                      =PP3V3_S0_PCI - @m60_lib.M60           6A4 44D5
                      =PP3V3_S0_PATA - @m60_lib.M60          6B4 38D3
                      =PP3V3_S0_ODD_TSENS - @m60_lib.M60     6B4 66B4
                      =PP3V3_S0_NB_VCC_HV - @m60_lib.M60     6B4 17C6 19A8 19C7
                      =PP3V3_S0_NB_TVDAC - @m60_lib.M60      6B4 19C7
                      =PP3V3_S0_LCD - @m60_lib.M60           88C6 94D7
                      =PP3V3_S0_IMVP - @m60_lib.M60          6A4 75D8
                      =PP3V3_S0_HD_TSENS - @m60_lib.M60      6B4 66B5
                      =PP3V3_S0_GPU_CLOCKS - @m60_lib.M60    88C6
                      =PP3V3_S0_GPUBBP - @m60_lib.M60        88C6
                      =PP3V3_S0_GPUBBN - @m60_lib.M60        88C6
                      =PP3V3_S0_GPUBBCTL - @m60_lib.M60      88C6
                      =PP3V3_S0_GPU - @m60_lib.M60           88C6 91D2 93A1 97B5
                      =PP3V3_S0_FAN - @m60_lib.M60           6B4 59A8 59B7 65B7 65C7
                                                             66C7
                      =PP3V3_S0_CK410 - @m60_lib.M60         6A4 33C8 33D3 33D8 34D4
                      =PP3V3_S0_AUDIO - @m60_lib.M60         6A4 68D7 72A6 72C8 72D5
                                                             73B8 74B5 74C5 74D6
                      =PP3V3_S0_AIRPORT - @m60_lib.M60       6A4 53C2
                      =PP3V3_GPU - @m60_lib.M60              88C6 94B3
                      =PP3V3_DDC_LCD - @m60_lib.M60          88C6 94A7 94C7
                      =PP3V3_DDC_DVI - @m60_lib.M60          88C6 97D2
=PP3V3_S3_1V2REG      =PP3V3_S3_1V2REG - @m60_lib.M60        6D3 77C6
                      PP3V3_S3 - @m60_lib.M60                6A7 6D4 53C4 59C8 59D3
                                                             83C1
                      =PP3V3_S3_BT - @m60_lib.M60            6D3 47B3
                      =PP3V3_S3_TPM - @m60_lib.M60           6D3 67C2
                      =PP3V3_S3_ENET - @m60_lib.M60          6D3 41A5 41B3 41C3 41D6
                                                             41D8 42D8
                      PP3V3_S3 - @m60_lib.M60                6A7 6D4 53C4 59C8 59D3
                                                             83C1
                      =PP3V3_S3_VGASYNC - @m60_lib.M60       6C3
                      =PP3V3_S3_TPM - @m60_lib.M60           6D3 67C2
                      =PP3V3_S3_ENET - @m60_lib.M60          6D3 41A5 41B3 41C3 41D6
                                                             41D8 42D8
                      =PP3V3_S3_BT - @m60_lib.M60            6D3 47B3
=PP3V3_S5_2V5_LDO     =PP3V3_S5_2V5_LDO - @m60_lib.M60       6D1 57D8
                      PP3V3_S5 - @m60_lib.M60                5D2 6A8 6C8 6D2 26C1 26C4
                                                             26C4 57D1 59A8 65B7 65D7
                                                             66D7 76D2 77B8 77C7 77C8
                                                             77C8 77D8 79A3 79A5 80A5
                                                             80B3 81A5 81A5 83B3 83C1
                                                             83D7
                      =PP3V3_S5_ROM - @m60_lib.M60           6D1 63D4
                      =PP3V3_S5_DEBUG - @m60_lib.M60         6D1 60D6
                      =PP3V3_S5_SMC - @m60_lib.M60           6D1 58C2 58D3 58D4 59A4
                                                             59A5 59C4 59D3 59D8
                      =PP3V3_S5_FW - @m60_lib.M60            6D1 44A6 44B2 44D5 44D7
                                                             45D6 46A8
                      =PP3V3_S5_SB_IO - @m60_lib.M60         6D1 22C6 27C6
                      =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA -       6D1 24C3
                      @m60_lib.M60
                      =PP3V3_S5_SB_VCCSUS3_3_USB -           6D1 24B3 25D1
                      @m60_lib.M60
                      =PP3V3_S5_SB_VCCSUS3_3 -               6D1 24A5 24B3 25B6 25D1
                      @m60_lib.M60
                      =PP3V3_S5_SB_PM - @m60_lib.M60         6D1 11B5 23D1
                      =PP3V3_S5_SB_USB - @m60_lib.M60        6D1 22D8
                      =PP3V3_S5_SB - @m60_lib.M60            6D1 23A7 23B3 23B7 23D4
                                                             23D8 25C8 26D8
                      PP3V3_S5 - @m60_lib.M60                5D2 6A8 6C8 6D2 26C1 26C4
                                                             26C4 57D1 59A8 65B7 65D7
                                                             66D7 76D2 77B8 77C7 77C8
                                                             77C8 77D8 79A3 79A5 80A5
                                                             80B3 81A5 81A5 83B3 83C1
                                                             83D7
                      =PP3V3_S5_SMC - @m60_lib.M60           6D1 58C2 58D3 58D4 59A4
                                                             59A5 59C4 59D3 59D8
                      =PP3V3_S5_SB_VCCSUS3_3_USB -           6D1 24B3 25D1
                      @m60_lib.M60
                      =PP3V3_S5_SB_VCCSUS3_3 -               6D1 24A5 24B3 25B6 25D1
                      @m60_lib.M60
                      =PP3V3_S5_SB_USB - @m60_lib.M60        6D1 22D8
                      =PP3V3_S5_SB_PM - @m60_lib.M60         6D1 11B5 23D1
                      =PP3V3_S5_SB_IO - @m60_lib.M60         6D1 22C6 27C6
                      =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA -       6D1 24C3
                      @m60_lib.M60
                      =PP3V3_S5_SB - @m60_lib.M60            6D1 23A7 23B3 23B7 23D4
                                                             23D8 25C8 26D8
                      =PP3V3_S5_ROM - @m60_lib.M60           6D1 63D4
                      =PP3V3_S5_FW - @m60_lib.M60            6D1 44A6 44B2 44D5 44D7
                                                             45D6 46A8
                      =PP3V3_S5_DEBUG - @m60_lib.M60         6D1 60D6
=PP4V5_S0_AUDIO_ANAL  =PP4V5_S0_AUDIO_ANALOG -               6A4 68A6
OG                    @m60_lib.M60
                      PP4V5_S0_AUDIO_ANALOG -                6A6 83D5
                      @m60_lib.M60
=PP5V_S0_DEBUG        =PP5V_S0_DEBUG - @m60_lib.M60          6A4 60C6
                      =PP5V_S0_DVI_DDC - @m60_lib.M60        88A6 97D6
                      =PP5V_S0_GPUISENS - @m60_lib.M60       85D2 88A6
                      PP5V_S0 - @m60_lib.M60                 6A6 75D7 83B4 88B8 97D3
                      =PP5V_S0_SATA - @m60_lib.M60           6A4 6D6
                      =PP5V_S0_SB - @m60_lib.M60             6A4 25D8
                      =PP5V_S0_PATA - @m60_lib.M60           6A4 38C4 38D3
                      PP5V_S0 - @m60_lib.M60                 6A6 75D7 83B4 88B8 97D3
                      =PP5V_S0_SB - @m60_lib.M60             6A4 25D8
                      =PP5V_S0_PATA - @m60_lib.M60           6A4 38C4 38D3
                      =PP5V_S0_GPUISENS - @m60_lib.M60       85D2 88A6
                      =PP5V_S0_GPUBBCTL - @m60_lib.M60       88B6
                      =PP5V_S0_DVI_DDC - @m60_lib.M60        88A6 97D6
=PP5V_S0_GPUVCORE     =PP5V_S0_GPUVCORE - @m60_lib.M60       85D7 88D6
                      GPUVCORE_VCC - @m60_lib.M60            88D6
=PP5V_S0_MEMVTT       =PP5V_S0_MEMVTT - @m60_lib.M60         6C3 31C6
                      PP5V_S3 - @m60_lib.M60                 6C4 59B1 83C1
                      =PP5V_S3_BNDI - @m60_lib.M60           6C3 47D4
                      =PP5V_S3_USB - @m60_lib.M60            6C3 47C8
                      PP5V_S3 - @m60_lib.M60                 6C4 59B1 83C1
                      =PP5V_S3_USB - @m60_lib.M60            6C3 47C8
                      =PP5V_S3_BNDI - @m60_lib.M60           6C3 47D4
=PP5V_S5_AUDIO_LDO    =PP5V_S5_AUDIO_LDO - @m60_lib.M60      6D1 82D8
                      PP5V_S5 - @m60_lib.M60                 5D2 6D2 59A5 79B3 80B3
                                                             81B3 82D1 83B3 83C6 83D1
                      =PP5V_S5_SB - @m60_lib.M60             6D1 25C8
                      PP5V_S5 - @m60_lib.M60                 5D2 6D2 59A5 79B3 80B3
                                                             81B3 82D1 83B3 83C6 83D1
                      =PP5V_S5_SB - @m60_lib.M60             6D1 25C8
=PP12V_GPU            =PP12V_GPU - @m60_lib.M60              88B6 94C8
                      PP12V_S0 - @m60_lib.M60                6A6 83B5 88B8
                      =PP12V_S0_INVERTER - @m60_lib.M60      6A4 6D8
                      =PP12V_S0_SATA - @m60_lib.M60          6A4 6D8
                      =PP12V_S0_FAN - @m60_lib.M60           6A4 65B6 65D7 66D6
                      PP12V_S0 - @m60_lib.M60                6A6 83B5 88B8
                      =PP12V_S0_FAN - @m60_lib.M60           6A4 65B6 65D7 66D6
=PP12V_S0_AUDIO_SPKR  =PP12V_S0_AUDIO_SPKRAMP -              6A4 72D8
AMP                   @m60_lib.M60
                      PP12V_S0_AUDIO_SPKRAMP -               6A5
                      @m60_lib.M60
=PP12V_S5_CPU         =PP12V_S5_CPU - @m60_lib.M60           6C1 76D8
                      =PPVIN_S0_GPUVCORE - @m60_lib.M60      85D7 88B6
                      PP12V_S5 - @m60_lib.M60                5D2 6C2 6D6 57D6 77C8
                                                             77D8 78C7 79D7 80D7 81D7
                                                             82D6 83B6 83B7 83B8 83C3
                                                             83D3 83D5 83D7 88B8
                      =PP12V_S5_FW - @m60_lib.M60            6C1 46D7
                      PP12V_S5 - @m60_lib.M60                5D2 6C2 6D6 57D6 77C8
                                                             77D8 78C7 79D7 80D7 81D7
                                                             82D6 83B6 83B7 83B8 83C3
                                                             83D3 83D5 83D7 88B8
                      =PPVIN_S0_GPUVCORE - @m60_lib.M60      85D7 88B6
                      =PP12V_S5_FW - @m60_lib.M60            6C1 46D7
=PP12V_S5_FW_PHY      =PP12V_S5_FW_PHY - @m60_lib.M60        44C2 46D5
                      PP12V_FW - @m60_lib.M60                46D6
=PPBB_S0_GPU          =PPBB_S0_GPU - @m60_lib.M60            86D6 88C6
                      =PPVCORE_S0_GPU - @m60_lib.M60         86D8 88D6 91A7
                      PP1V0R1V2_S0_GPU - @m60_lib.M60        59B4 88D8
                      =PPVCORE_S0_GPU_REG - @m60_lib.M60     85C1 88D6
                      PPBB_S0_GPU - @m60_lib.M60             88C8
                      PP1V0R1V2_S0_GPU - @m60_lib.M60        59B4 88D8
                      =PPVOUT_S0_GPUBBP_LDO -                85A6 88C6
                      @m60_lib.M60
                      =PPVCORE_S0_GPU_REG - @m60_lib.M60     85C1 88D6
                      =PPVCORE_S0_GPU_BBP - @m60_lib.M60     85A8 88D6
                      =PPVCORE_S0_GPU - @m60_lib.M60         86D8 88D6 91A7
=PPVCORE_S0_CPU       =PPVCORE_S0_CPU - @m60_lib.M60         6D4 8B6 8D7 8D8 9B8
                      PPVCORE_CPU - @m60_lib.M60             5D2 6D6 75A4 75D1 76B3
ACZ_BITCLK            ACZ_BITCLK - @m60_lib.M60              21C7 68D7
ACZ_RST_L             ACZ_RST_L - @m60_lib.M60               21C7 68C7
ACZ_SDATAIN<0>        ACZ_SDATAIN<0> - @m60_lib.M60          21C7 68D7
ACZ_SDATAIN_CHIP      ACZ_SDATAIN_CHIP - @m60_lib.M60        68C6
ACZ_SDATAOUT          ACZ_SDATAOUT - @m60_lib.M60            21C7 68D7
ACZ_SYNC              ACZ_SYNC - @m60_lib.M60                21C7 68D7
AIRPORT_CLK100M_PCIE  AIRPORT_CLK100M_PCIE_N -               34B4 34C2 53C6
_N                    @m60_lib.M60
AIRPORT_CLK100M_PCIE  AIRPORT_CLK100M_PCIE_P -               34B4 34C2 53C6
_P                    @m60_lib.M60
AIRPORT_CONN_CLK      AIRPORT_CONN_CLK - @m60_lib.M60        53B5
AIRPORT_CONN_DATA     AIRPORT_CONN_DATA - @m60_lib.M60       53B5
AIRPORT_RST_L         AIRPORT_RST_L - @m60_lib.M60           6A7 53C5
AIRPORT_WAKE_L        AIRPORT_WAKE_L - @m60_lib.M60          53C6
ALL_SYS_PWRGD         ALL_SYS_PWRGD - @m60_lib.M60           26D5 58D7 77B6
ALS_GAIN              ALS_GAIN - @m60_lib.M60                58B5 59C6
                      NC_ALS_GAIN - @m60_lib.M60             59C5
ALS_LEFT              ALS_LEFT - @m60_lib.M60                58A7 59D5
                      TP_ALS_LEFT - @m60_lib.M60             59D3
ALS_RIGHT             ALS_RIGHT - @m60_lib.M60               58A7 59D5
                      TP_ALS_RIGHT - @m60_lib.M60            59D3
ATI_DVPCLK            ATI_DVPCLK - @m60_lib.M60              91C3 95A6
                      TP_ATI_DVPCLK - @m60_lib.M60           95A8
ATI_DVPCNTL<0>        ATI_DVPCNTL<0> - @m60_lib.M60          91C3 95A6
ATI_DVPCNTL<1>        ATI_DVPCNTL<1> - @m60_lib.M60          91B3 95A6
ATI_DVPCNTL<2>        ATI_DVPCNTL<2> - @m60_lib.M60          91B3 95A6
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ATI_RSET              ATI_RSET - @m60_lib.M60                93A8 93B5
ATI_TDIODE_N          ATI_TDIODE_N - @m60_lib.M60            61C5 91A3
ATI_TDIODE_P          ATI_TDIODE_P - @m60_lib.M60            61C5 91A3
ATI_TESTEN            ATI_TESTEN - @m60_lib.M60              91A3
ATI_VREFG             ATI_VREFG - @m60_lib.M60               91D3
AUDLINDETH            AUDLINDETH - @m60_lib.M60              74D5
AUDSAMPCPN            AUDSAMPCPN - @m60_lib.M60              72C4
AUDSAMPCPP            AUDSAMPCPP - @m60_lib.M60              72C4
AUDSAMPINLN           AUDSAMPINLN - @m60_lib.M60             72D6
AUDSAMPINLP           AUDSAMPINLP - @m60_lib.M60             72C6
AUDSAMPINRN           AUDSAMPINRN - @m60_lib.M60             72C6
AUDSAMPINRP           AUDSAMPINRP - @m60_lib.M60             72C6
AUDSAMPOURTP          AUDSAMPOURTP - @m60_lib.M60            72C4
AUDSAMPOUTLN          AUDSAMPOUTLN - @m60_lib.M60            72C4
AUDSAMPOUTLP          AUDSAMPOUTLP - @m60_lib.M60            72C4
AUDSAMPOUTRN          AUDSAMPOUTRN - @m60_lib.M60            72C4
AUD_ANALOG_FILT_1     AUD_ANALOG_FILT_1 - @m60_lib.M60       68C4
AUD_ANALOG_FILT_2     AUD_ANALOG_FILT_2 - @m60_lib.M60       68C4
AUD_BI_PORT_A_L       AUD_BI_PORT_A_L - @m60_lib.M60         68C1 74B8
AUD_BI_PORT_A_R       AUD_BI_PORT_A_R - @m60_lib.M60         68C1 74B8
AUD_BI_PORT_B_L       AUD_BI_PORT_B_L - @m60_lib.M60         68B2 68C1 74A3
                      AUD_BI_PORT_B_R - @m60_lib.M60         68B1 68C1
AUD_BI_PORT_C_L       AUD_BI_PORT_C_L - @m60_lib.M60         68C7 72D8
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AUD_BI_PORT_C_R	AUD_BI_PORT_C_R - @m60_lib.M60	68C7 72C8
AUD_BI_PORT_F_L	AUD_BI_PORT_F_L - @m60_lib.M60	68C1 74C8
AUD_BI_PORT_F_R	AUD_BI_PORT_F_R - @m60_lib.M60	68C1 74C8
AUD_BYPASS	AUD_BYPASS - @m60_lib.M60	68C4
AUD_DEBOUNCE	AUD_DEBOUNCE - @m60_lib.M60	72B7
AUD_GPIO_0	AUD_GPIO_0 - @m60_lib.M60	68C7 72B8
AUD_GPIO_1	AUD_GPIO_1 - @m60_lib.M60	68C7 74C5
AUD_LI_DET_EMI	AUD_LI_DET_EMI - @m60_lib.M60	73D6
AUD_LI_DET_H	AUD_LI_DET_H - @m60_lib.M60	73D4 74D6
AUD_LI_DET_JACK	AUD_LI_DET_JACK - @m60_lib.M60	73D8
AUD_LI_GND_EMI	AUD_LI_GND_EMI - @m60_lib.M60	73D6
AUD_LI_GND_JACK	AUD_LI_GND_JACK - @m60_lib.M60	73D8
AUD_LI_L	AUD_LI_L - @m60_lib.M60	73D4 74C5
AUD_LI_L_EMI	AUD_LI_L_EMI - @m60_lib.M60	73D6
AUD_LI_L_JACK	AUD_LI_L_JACK - @m60_lib.M60	73D8
AUD_LI_R	AUD_LI_R - @m60_lib.M60	73D4 74C5
AUD_LI_R_EMI	AUD_LI_R_EMI - @m60_lib.M60	73D6
AUD_LI_R_JACK	AUD_LI_R_JACK - @m60_lib.M60	73D8
AUD_LO_DET1_1	AUD_LO_DET1_1 - @m60_lib.M60	74A4 74B2
AUD_LO_DET1_INV	AUD_LO_DET1_INV - @m60_lib.M60	74B3
AUD_LO_DET2_1	AUD_LO_DET2_1 - @m60_lib.M60	74B4
AUD_LO_GND_JACK	AUD_LO_GND_JACK - @m60_lib.M60	73A4
AUD_LO_L	AUD_LO_L - @m60_lib.M60	73B8 74B5
AUD_LO_L_EMI	AUD_LO_L_EMI - @m60_lib.M60	73B7
AUD_LO_L_JACK	AUD_LO_L_JACK - @m60_lib.M60	73B4
AUD_LO_R	AUD_LO_R - @m60_lib.M60	73A8 74B5
AUD_LO_R_EMI	AUD_LO_R_EMI - @m60_lib.M60	73A7
AUD_LO_R_JACK	AUD_LO_R_JACK - @m60_lib.M60	73B4
AUD_LO_TIP	AUD_LO_TIP - @m60_lib.M60	73A8 74B5
AUD_LO_TIP_EMI	AUD_LO_TIP_EMI - @m60_lib.M60	73A7
AUD_LO_TIP_JACK	AUD_LO_TIP_JACK - @m60_lib.M60	73B4
AUD_LO_TYPE	AUD_LO_TYPE - @m60_lib.M60	73B8 74A5
AUD_LO_TYPE_EMI	AUD_LO_TYPE_EMI - @m60_lib.M60	73B7
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AUD_MAX9714_VREG	AUD_MAX9714_VREG - @m60_lib.M60	72C5
AUD_MIC_INTERCON	AUD_MIC_INTERCON - @m60_lib.M60	74A4
AUD_MIC_IN_N	AUD_MIC_IN_N - @m60_lib.M60	73C4 74A6
AUD_MIC_IN_N_CONN	AUD_MIC_IN_N_CONN - @m60_lib.M60	47C2 73C2
AUD_MIC_IN_N_EMI	AUD_MIC_IN_N_EMI - @m60_lib.M60	73C3
AUD_MIC_IN_P	AUD_MIC_IN_P - @m60_lib.M60	73C4 74A6
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AUD_MIC_P1	AUD_MIC_P1 - @m60_lib.M60	74A4
AUD_PORT_A_DET_L	AUD_PORT_A_DET_L - @m60_lib.M60	74B2
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AUD_PORT_A_L2	AUD_PORT_A_L2 - @m60_lib.M60	74B7 74C3 74D3
AUD_PORT_A_R1	AUD_PORT_A_R1 - @m60_lib.M60	74B7 74C4 74D4
AUD_PORT_A_R2	AUD_PORT_A_R2 - @m60_lib.M60	74B7 74C3 74D3
AUD_PORT_E_DET_L	AUD_PORT_E_DET_L - @m60_lib.M60	74B1
AUD_PORT_F_DET_L	AUD_PORT_F_DET_L - @m60_lib.M60	74D4
AUD_PORT_F_L1	AUD_PORT_F_L1 - @m60_lib.M60	74C7
AUD_PORT_F_R1	AUD_PORT_F_R1 - @m60_lib.M60	74C7
AUD_SAMP_FS1	AUD_SAMP_FS1 - @m60_lib.M60	72A6 72C5
AUD_SAMP_FS2	AUD_SAMP_FS2 - @m60_lib.M60	72A6 72C5
AUD_SAMP_G1	AUD_SAMP_G1 - @m60_lib.M60	72A6 72C5
AUD_SAMP_G2	AUD_SAMP_G2 - @m60_lib.M60	72A6 72C5
AUD_SAMP_INL_N	AUD_SAMP_INL_N - @m60_lib.M60	72C5
AUD_SAMP_INL_P	AUD_SAMP_INL_P - @m60_lib.M60	72C5
AUD_SAMP_INR_N	AUD_SAMP_INR_N - @m60_lib.M60	72C5
AUD_SAMP_INR_P	AUD_SAMP_INR_P - @m60_lib.M60	72C5
AUD_SAMP_SHDN_L	AUD_SAMP_SHDN_L - @m60_lib.M60	72C5
AUD_SENSE_A	AUD_SENSE_A - @m60_lib.M60	68C1 74C5 74D7
AUD_SENSE_B	AUD_SENSE_B - @m60_lib.M60	68C1 74C5 74D6 74D7
AUD_SPDIFIN_JACK	AUD_SPDIFIN_JACK - @m60_lib.M60	73D7
AUD_SPDIF_GND_IN	AUD_SPDIF_GND_IN - @m60_lib.M60	73C7
AUD_SPDIF_GND_OUT	AUD_SPDIF_GND_OUT - @m60_lib.M60	73A3
AUD_SPDIF_IN	AUD_SPDIF_IN - @m60_lib.M60	68C1 73D4
AUD_SPDIF_OUT	AUD_SPDIF_OUT - @m60_lib.M60	68D1 73B8
AUD_SPDIF_OUT_CHIP	AUD_SPDIF_OUT_CHIP - @m60_lib.M60	68D4
AUD_SPKR_OUTL_N	AUD_SPKR_OUTL_N - @m60_lib.M60	72C1 73C3
AUD_SPKR_OUTL_P	AUD_SPKR_OUTL_P - @m60_lib.M60	72C1 73C3
AUD_SPKR_OUTR_N	AUD_SPKR_OUTR_N - @m60_lib.M60	72C1 73D3
AUD_SPKR_OUTR_P	AUD_SPKR_OUTR_P - @m60_lib.M60	72C1 73C3
AUD_TYPE_DET_EN	AUD_TYPE_DET_EN - @m60_lib.M60	74B3
AUD_VREF_FILT	AUD_VREF_FILT - @m60_lib.M60	68C4
AUD_VREF_PORT_B	AUD_VREF_PORT_B - @m60_lib.M60	68C1 74A2
BAL_IN_COM	BAL_IN_COM - @m60_lib.M60	68C7 74A7
BAL_IN_L	BAL_IN_L - @m60_lib.M60	68C7 74A7
BAL_IN_R	BAL_IN_R - @m60_lib.M60	68C7 74A7
BAT_1	BAT_1 - @m60_lib.M60	26C8
BAT_2	BAT_2 - @m60_lib.M60	26C8
BEEP	BEEP - @m60_lib.M60	68C6
BIOS_REC	BIOS_REC - @m60_lib.M60	23A6 23C5
BOOT_LPC_SPI_L	BOOT_LPC_SPI_L - @m60_lib.M60	22B3 58C7 60C6
C8509_P1	C8509_P1 - @m60_lib.M60	85C5
CK410_27M_NONSPREAD	CK410_27M_NONSPREAD - @m60_lib.M60	34A4 92C7
CK410_27M_SPREAD	CK410_27M_SPREAD - @m60_lib.M60	34A4 92C5
	GPU_GPIO_16 - @m60_lib.M60	91C3 92C3
CK410_CLK14P3M_TIMER	CK410_CLK14P3M_TIMER - @m60_lib.M60	33A4 34D6
CK410_CPU0_N	CK410_CPU0_N - @m60_lib.M60	33C4 34B6
CK410_CPU0_P	CK410_CPU0_P - @m60_lib.M60	33C4 34B6
CK410_CPU1_N	CK410_CPU1_N - @m60_lib.M60	33C4 34B6
CK410_CPU1_P	CK410_CPU1_P - @m60_lib.M60	33C4 34B6
CK410_CPU2_ITP_SRC10_N	CK410_CPU2_ITP_SRC10_N - @m60_lib.M60	33C4 34B6
CK410_CPU2_ITP_SRC10_P	CK410_CPU2_ITP_SRC10_P - @m60_lib.M60	33C4 34B6
CK410_DOT96_27M_NONSPREAD_P	CK410_DOT96_27M_NONSPREAD_P - @m60_lib.M60	33A4 34A6
CK410_DOT96_27M_SPREAD_N	CK410_DOT96_27M_SPREAD_N - @m60_lib.M60	33A4 34A6
CK410_FSA	CK410_FSA - @m60_lib.M60	34B8 34C4
CK410_FSB_TEST_MODE	CK410_FSB_TEST_MODE - @m60_lib.M60	33C6 34A8
CK410_FSC	CK410_FSC - @m60_lib.M60	34A8 34D4
CK410_IREF	CK410_IREF - @m60_lib.M60	33B6
CK410_LVDS_N	CK410_LVDS_N - @m60_lib.M60	33B4 34A6
	TP_CK410_LVDS_N - @m60_lib.M60	34A4
CK410_LVDS_P	CK410_LVDS_P - @m60_lib.M60	33B4 34A6
	TP_CK410_LVDS_P - @m60_lib.M60	34A4
CK410_PCI1_CLK	CK410_PCI1_CLK - @m60_lib.M60	33B6 34C6
CK410_PCI2_CLK	CK410_PCI2_CLK - @m60_lib.M60	33B6 34C6
CK410_PCI3_CLK	CK410_PCI3_CLK - @m60_lib.M60	33B6 34C6
CK410_PCI4_CLK	CK410_PCI4_CLK - @m60_lib.M60	33B6 34C6
CK410_PCI5_FCTSEL1	CK410_PCI5_FCTSEL1 - @m60_lib.M60	33B6 34D6
CK410_PCIF0_CLK	CK410_PCIF0_CLK - @m60_lib.M60	33B8 34B6
CK410_PCIF1_ITP_EN	CK410_PCIF1_ITP_EN - @m60_lib.M60	33B8 34B6
CK410_PD_VTT_PWRGD_L	CK410_PD_VTT_PWRGD_L - @m60_lib.M60	26A8 33A4
	VR_PWRGD_CK410_L - @m60_lib.M60	26A7 75C6
CK410_REF1_FCTSEL0	CK410_REF1_FCTSEL0 - @m60_lib.M60	33A4 34C6
CK410_SRC1_N	CK410_SRC1_N - @m60_lib.M60	33B4 34A6
CK410_SRC1_P	CK410_SRC1_P - @m60_lib.M60	33B4 34A6
CK410_SRC2_N	CK410_SRC2_N - @m60_lib.M60	33B4 34A6
CK410_SRC2_P	CK410_SRC2_P - @m60_lib.M60	33B4 34A6
CK410_SRC3_N	CK410_SRC3_N - @m60_lib.M60	33B4 34D3
CK410_SRC3_P	CK410_SRC3_P - @m60_lib.M60	33B4 34D3
CK410_SRC4_N	CK410_SRC4_N - @m60_lib.M60	33B4 34B6
CK410_SRC4_P	CK410_SRC4_P - @m60_lib.M60	33B4 34B6
CK410_SRC5_N	CK410_SRC5_N - @m60_lib.M60	33B4 34B6
CK410_SRC5_P	CK410_SRC5_P - @m60_lib.M60	33B4 34B6
CK410_SRC6_N	CK410_SRC6_N - @m60_lib.M60	33B4 34B6
CK410_SRC6_P	CK410_SRC6_P - @m60_lib.M60	33B4 34B6
CK410_SRC7_N	CK410_SRC7_N - @m60_lib.M60	33B4 34D3
CK410_SRC7_P	CK410_SRC7_P - @m60_lib.M60	33B4 34D3
CK410_SRC8_N	CK410_SRC8_N - @m60_lib.M60	33A4 34A6
CK410_SRC8_P	CK410_SRC8_P - @m60_lib.M60	33A4 34A6
CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L - @m60_lib.M60	33B4 34D8
CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L - @m60_lib.M60	33B4 34D8
CK410_SRC_CLKREQ6_L	CK410_SRC_CLKREQ6_L - @m60_lib.M60	33B4 53C6
CK410_SRC_CLKREQ8_L	CK410_SRC_CLKREQ8_L - @m60_lib.M60	33A4 34D8
CK410_USB48_FSA	CK410_USB48_FSA - @m60_lib.M60	33A4 34C6
CK410_XTAL_IN	CK410_XTAL_IN - @m60_lib.M60	33C6
CK410_XTAL_OUT	CK410_XTAL_OUT - @m60_lib.M60	33C6
CLK_NB_OE_L	CLK_NB_OE_L - @m60_lib.M60	14B6 33B4
CPU_A20M_L	CPU_A20M_L - @m60_lib.M60	5C8 7C7 21C4
CPU_BSEL<0>	CPU_BSEL<0> - @m60_lib.M60	7B4 34B8
CPU_BSEL<1>	CPU_BSEL<1> - @m60_lib.M60	7B4 34A8
CPU_BSEL<2>	CPU_BSEL<2> - @m60_lib.M60	7B4 34A8
CPU_COMP<0>	CPU_COMP<0> - @m60_lib.M60	7B2
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CPU_COMP<2>	CPU_COMP<2> - @m60_lib.M60	7B2
CPU_COMP<3>	CPU_COMP<3> - @m60_lib.M60	7B2
CPU_DCIN_SENSE	CPU_DCIN_SENSE - @m60_lib.M60	76D7
CPU_DCIN_SENSE_R	CPU_DCIN_SENSE_R - @m60_lib.M60	76C7
CPU_DPRSTP_L	CPU_DPRSTP_L - @m60_lib.M60	7B3 21C4 75C6
CPU_DPSLP_L	CPU_DPSLP_L - @m60_lib.M60	7B3 21C4
CPU_FERR_L	CPU_FERR_L - @m60_lib.M60	7C7 21C2
CPU_GTLREF	CPU_GTLREF - @m60_lib.M60	5D4 7B4
CPU_HS_ZH607	CPU_HS_ZH607 - @m60_lib.M60	9D4
CPU_HS_ZH608	CPU_HS_ZH608 - @m60_lib.M60	9D3
CPU_HS_ZH609	CPU_HS_ZH609 - @m60_lib.M60	9D3
CPU_HS_ZH610	CPU_HS_ZH610 - @m60_lib.M60	9D2
CPU_IGNNE_L	CPU_IGNNE_L - @m60_lib.M60	5C8 7C7 21C4
CPU_INIT_L	CPU_INIT_L - @m60_lib.M60	5C8 7D6 21C4
CPU_INTR	CPU_INTR - @m60_lib.M60	5C8 7C7 21C4
CPU_NMI	CPU_NMI - @m60_lib.M60	5C8 7C7 21C4
CPU_PROCHOT_L	CPU_PROCHOT_L - @m60_lib.M60	7C6 59A8 59C7
CPU_PSI_L	CPU_PSI_L - @m60_lib.M60	7A3 75C6
CPU_PWRGD	CPU_PWRGD - @m60_lib.M60	7B3 21C4
CPU_RCIN_L	CPU_RCIN_L - @m60_lib.M60	21C4
CPU_SENSE_I_R	CPU_SENSE_I_R - @m60_lib.M60	76D7
CPU_SMI_L	CPU_SMI_L - @m60_lib.M60	5C8 7C7 21C4
CPU_STPCLK_L	CPU_STPCLK_L - @m60_lib.M60	5C8 7C7 21C4
CPU_TEST1	CPU_TEST1 - @m60_lib.M60	7B4
CPU_TEST2	CPU_TEST2 - @m60_lib.M60	7B4
CPU_THERMD_EXT_N	CPU_THERMD_EXT_N - @m60_lib.M60	10B6
CPU_THERMD_EXT_P	CPU_THERMD_EXT_P - @m60_lib.M60	10B6
CPU_THERMD_N	CPU_THERMD_N - @m60_lib.M60	7C6 10C6
CPU_THERMD_P	CPU_THERMD_P - @m60_lib.M60	7C6 10C6
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @m60_lib.M60	21C2
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @m60_lib.M60	8B6 75A4
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @m60_lib.M60	8B6 75A4
CPU_VID<0>	CPU_VID<0> - @m60_lib.M60	8B7 75C7
CPU_VID<1>	CPU_VID<1> - @m60_lib.M60	8B7 75C7
CPU_VID<2>	CPU_VID<2> - @m60_lib.M60	8B7 75C7
CPU_VID<3>	CPU_VID<3> - @m60_lib.M60	8B7 75C7
CPU_VID<4>	CPU_VID<4> - @m60_lib.M60	8B7 75C7
CPU_VID<5>	CPU_VID<5> - @m60_lib.M60	8B7 75C7
CPU_VID<6>	CPU_VID<6> - @m60_lib.M60	8B7 75D7
CPU_XDP_CLK_N	CPU_XDP_CLK_N - @m60_lib.M60	11B3 34B3
	FSB_CLK_XDP_N - @m60_lib.M60	34B4 34C2
CPU_XDP_CLK_P	CPU_XDP_CLK_P - @m60_lib.M60	11B3 34B3
	FSB_CLK_XDP_P - @m60_lib.M60	34B4 34C2
CRB_SV_DET	CRB_SV_DET - @m60_lib.M60	23B6 23C3
CRT_BLUE	CRT_BLUE - @m60_lib.M60	13B5 19D4
	=PPVCORE_S0_NB - @m60_lib.M60	6D4 16C8 16D3 19B6 19D5 19D7
	CRT_BLUE_L - @m60_lib.M60	13B5 19D4
	CRT_IREF - @m60_lib.M60	13B5 19D4
	CRT_GREEN_L - @m60_lib.M60	13B5 19D4
	CRT_GREEN - @m60_lib.M60	13B5 19D4
	PP2V5_S0_NB_VCCA_CRTDAC - @m60_lib.M60	17D6 19D4
	CRT_RED - @m60_lib.M60	13B5 19D4
	CRT_RED_L - @m60_lib.M60	13B5 19D4
	PP1V05_S0 - @m60_lib.M60	6D6 34A8 34B8 34C7 81C1
	=PP1V05_S0_CPU - @m60_lib.M60	5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 9C8 11B3 11C5
	=PPVCORE_S0_SB - @m60_lib.M60	6D4 24D3 25D3
	=PP1V05_S0_SB_CPU_IO - @m60_lib.M60	6D4 21C1 21C1 24C3 25C3
	=PP1V05_S0_NB_VTT - @m60_lib.M60	6D4 17D3 19B8 19D7
	=PP1V05_S0_FSB_NB - @m60_lib.M60	5D4 6D4 12A7 12B7 12C2 19D7
	PP2V5_S0_NB_VCCA_CRTDAC - @m60_lib.M60	17D6 19D4
	PP1V05_S0 - @m60_lib.M60	6D6 34A8 34B8 34C7 81C1
	CRT_RED_L - @m60_lib.M60	13B5 19D4
	CRT_RED - @m60_lib.M60	13B5 19D4
	CRT_IREF - @m60_lib.M60	13B5 19D4
	CRT_GREEN_L - @m60_lib.M60	13B5 19D4
	CRT_GREEN - @m60_lib.M60	13B5 19D4
	CRT_BLUE_L - @m60_lib.M60	13B5 19D4
	=PPVCORE_S0_SB - @m60_lib.M60	6D4 24D3 25D3
	=PPVCORE_S0_NB - @m60_lib.M60	6D4 16C8 16D3 19B6 19D5 19D7
	=PP1V05_S0_SB_CPU_IO - @m60_lib.M60	6D4 21C1 21C1 24C3 25C3
	=PP1V05_S0_NB_VTT - @m60_lib.M60	6D4 17D3 19B8 19D7
	=PP1V05_S0_NB - @m60_lib.M60	6D4 19D7
	=PP1V05_S0_FSB_NB - @m60_lib.M60	5D4 6D4 12A7 12B7 12C2 19D7
	=PP1V05_S0_CPU - @m60_lib.M60	5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 9C8 11B3 11C5
CRT_DDC_CLK	CRT_DDC_CLK - @m60_lib.M60	13B5 19C4
	TP_CRT_DDC_CLK - @m60_lib.M60	19C5
CRT_DDC_DATA	CRT_DDC_DATA - @m60_lib.M60	13B5 19C4
	TP_CRT_DDC_DATA - @m60_lib.M60	19C5
DEBUG_RST_L	DEBUG_RST_L - @m60_lib.M60	6A7 60B6
DMI_IRCOMP_R	DMI_IRCOMP_R - @m60_lib.M60	22C2
DMI_N2S_N<0>	DMI_N2S_N<0> - @m60_lib.M60	5B8 14B4 22D2
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DVI_DDC_DATA	DVI_DDC_DATA - @m60_lib.M60	97C2
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DVI_HPD_UF	DVI_HPD_UF - @m60_lib.M60	97C3 97D5
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ENET_C4107_2	ENET_C4107_2 - @m60_lib.M60	41D2
ENET_C4117_1	ENET_C4117_1 - @m60_lib.M60	41B2
ENET_C4118_1	ENET_C4118_1 - @m60_lib.M60	41B2
ENET_CLK100M_PCIE_N	ENET_CLK100M_PCIE_N - @m60_lib.M60	5D5 34A4 34B2 41C5
ENET_CLK100M_PCIE_P	ENET_CLK100M_PCIE_P - @m60_lib.M60	5D5 34A4 34B2 41C5
ENET_CTRL12	ENET_CTRL12 - @m60_lib.M60	41C7 42B8
	TP_ENET_CTRL12 - @m60_lib.M60	42B7
ENET_CTRL25	ENET_CTRL25 - @m60_lib.M60	41C7 42C6
ENET_GATED_RST_L	ENET_GATED_RST_L - @m60_lib.M60	41C5 42D2
	ENET_RST_L - @m60_lib.M60	6B7 42D3
ENET_LED_ACT_L	ENET_LED_ACT_L - @m60_lib.M60	41C8
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m60_lib.M60	41C8
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m60_lib.M60	41C8
ENET_LED_LINK_L	ENET_LED_LINK_L - @m60_lib.M60	41C8
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m60_lib.M60	41C7
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ENET_PU_VDDO_TTL1	ENET_PU_VDDO_TTL1 - @m60_lib.M60	41C5
ENET_RSET	ENET_RSET - @m60_lib.M60	41C7
ENET_VPD_CLK	ENET_VPD_CLK - @m60_lib.M60	41A2 41C4
ENET_VPD_DATA	ENET_VPD_DATA - @m60_lib.M60	41A2 41C4
ENET_XTALI	ENET_XTALI - @m60_lib.M60	41B5
ENET_XTALO	ENET_XTALO - @m60_lib.M60	41B5
F0_GATESLOWDN	F0_GATESLOWDN - @m60_lib.M60	65D5
F0_RCFEEDBK	F0_RCFEEDBK - @m60_lib.M60	65C5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @m60_lib.M60	65D6
F1_GATESLOWDN	F1_GATESLOWDN - @m60_lib.M60	65B5
F1_RCFEEDBK	F1_RCFEEDBK - @m60_lib.M60	65B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @m60_lib.M60	65B6
F2_GATESLOWDN	F2_GATESLOWDN - @m60_lib.M60	66D4
F2_RCFEEDBK	F2_RCFEEDBK - @m60_lib.M60	66C5
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @m60_lib.M60	66D5
FAN_0_OUT	FAN_0_OUT - @m60_lib.M60	65C4
FAN_0_PWR	FAN_0_PWR - @m60_lib.M60	65C4
FAN_1_OUT	FAN_1_OUT - @m60_lib.M60	65B4
FAN_1_PWR	FAN_1_PWR - @m60_lib.M60	65B3
FAN_2_OUT	FAN_2_OUT - @m60_lib.M60	66C4
FAN_2_PWR	FAN_2_PWR - @m60_lib.M60	66C3
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FSB_D_L<39>	FSB_D_L<39> - @m60_lib.M60	7C2 12B6
FSB_D_L<40>	FSB_D_L<40> - @m60_lib.M60	7C2 12B6
FSB_D_L<41>	FSB_D_L<41> - @m60_lib.M60	5D7 5D8 7C2 12B6
FSB_D_L<42>	FSB_D_L<42> - @m60_lib.M60	7C2 12B6
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FSB_D_L<59>	FSB_D_L<59> - @m60_lib.M60	5D7 5D8 7B2 12B6
FSB_D_L<60>	FSB_D_L<60> - @m60_lib.M60	7B2 12B6
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FSB_D_L<63>	FSB_D_L<63> - @m60_lib.M60	7B2 12B6
FSB_HITM_L	FSB_HITM_L - @m60_lib.M60	5C7 7D6 12B4
FSB_HIT_L	FSB_HIT_L - @m60_lib.M60	5C7 7D6 12B4
FSB_IERR_L	FSB_IERR_L - @m60_lib.M60	7D6
FSB_LOCK_L	FSB_LOCK_L - @m60_lib.M60	5D7 5D8 7D6 12B4
FSB_REQ_L<0>	FSB_REQ_L<0> - @m60_lib.M60	5C7 7D7 12B4
FSB_REQ_L<1>	FSB_REQ_L<1> - @m60_lib.M60	5C7 7D7 12B4
FSB_REQ_L<2>	FSB_REQ_L<2> - @m60_lib.M60	5C7 7D7 12A4
FSB_REQ_L<3>	FSB_REQ_L<3> - @m60_lib.M60	5C7 7D7 12A4
FSB_REQ_L<4>	FSB_REQ_L<4> - @m60_lib.M60	5C7 7D7 12A4
FSB_RS_L<0>	FSB_RS_L<0> - @m60_lib.M60	7D6 12A4
FSB_RS_L<1>	FSB_RS_L<1> - @m60_lib.M60	7D6 12A4
FSB_RS_L<2>	FSB_RS_L<2> - @m60_lib.M60	7D6 12A4
FSB_SLPCPU_L	FSB_SLPCPU_L - @m60_lib.M60	7A3 12A4
FSB_TRDY_L	FSB_TRDY_L - @m60_lib.M60	7D6 12A4
FWH_INIT_L	FWH_INIT_L - @m60_lib.M60	21C4 59C5 60C3
	SMC_CPU_INIT_3_3_L - @m60_lib.M60	58D5 59C6
FWH_MFG_MODE	FWH_MFG_MODE - @m60_lib.M60	23A6 23C5
FW_A_TPA_N	FW_A_TPA_N - @m60_lib.M60	44C3 46C8
	FW_PORT0_TPA_N - @m60_lib.M60	46C5 46C6
FW_A_TPA_P	FW_A_TPA_P - @m60_lib.M60	44C3 46C8
	FW_PORT0_TPA_P - @m60_lib.M60	46C5 46C6
FW_A_TPBIAS	FW_A_TPBIAS - @m60_lib.M60	44C4 46C8
FW_A_TPB_N	FW_A_TPB_N - @m60_lib.M60	44C3 46C8
	FW_PORT0_TPB_N - @m60_lib.M60	46C5 46C6
FW_A_TPB_P	FW_A_TPB_P - @m60_lib.M60	44C3 46C8
	FW_PORT0_TPB_P - @m60_lib.M60	46C5 46C6
FW_B_TPA_N	FW_B_TPA_N - @m60_lib.M60	44C3 46C8
	FW_PORT1_TPA_N - @m60_lib.M60	46B5 46C6
FW_B_TPA_P	FW_B_TPA_P - @m60_lib.M60	44C3 46C8
	FW_PORT1_TPA_P - @m60_lib.M60	46B5 46C6
FW_B_TPBIAS	FW_B_TPBIAS - @m60_lib.M60	44C4 46C8
FW_B_TPB_N	FW_B_TPB_N - @m60_lib.M60	44C3 46C8
	FW_PORT1_TPB_N - @m60_lib.M60	46B5 46C6
FW_B_TPB_P	FW_B_TPB_P - @m60_lib.M60	44C3 46C8
	FW_PORT1_TPB_P - @m60_lib.M60	46B5 46C6
FW_CARDBUS_L	FW_CARDBUS_L - @m60_lib.M60	44B5
FW_CONTENDER	FW_CONTENDER - @m60_lib.M60	44B3
FW_CPS	FW_CPS - @m60_lib.M60	44C3
FW_C_TPA_N	FW_C_TPA_N - @m60_lib.M60	44C3 46B8
	TP_FW_C_TPA_N - @m60_lib.M60	46B7
FW_C_TPA_P	FW_C_TPA_P - @m60_lib.M60	44C3 46B8
	TP_FW_C_TPA_P - @m60_lib.M60	46B7
FW_C_TPBIAS	FW_C_TPBIAS - @m60_lib.M60	44C4 46B8
	TP_FW_C_TPBIAS - @m60_lib.M60	46B7
FW_C_TPB_N	FW_C_TPB_N - @m60_lib.M60	44C3 46A8
	TP_FW_C_TPB_N - @m60_lib.M60	46A7
FW_C_TPB_P	FW_C_TPB_P - @m60_lib.M60	44C3 46A8
	TP_FW_C_TPB_P - @m60_lib.M60	46A7
FW_PC0	FW_PC0 - @m60_lib.M60	44B3
FW_PC1	FW_PC1 - @m60_lib.M60	44B3
FW_PC2	FW_PC2 - @m60_lib.M60	44B3
FW_PORT0_TPA_FL_N	FW_PORT0_TPA_FL_N - @m60_lib.M60	46C2
FW_PORT0_TPA_FL_P	FW_PORT0_TPA_FL_P - @m60_lib.M60	46C2
FW_PORT0_TPB_FL_N	FW_PORT0_TPB_FL_N - @m60_lib.M60	46C2
FW_PORT0_TPB_FL_P	FW_PORT0_TPB_FL_P - @m60_lib.M60	46C2
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m60_lib.M60	46B2
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m60_lib.M60	46B2
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m60_lib.M60	46B2
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m60_lib.M60	46B2
FW_R0	FW_R0 - @m60_lib.M60	44C4
FW_R1	FW_R1 - @m60_lib.M60	44C4
FW_RESET_L	FW_RESET_L - @m60_lib.M60	44C2 44C3
FW_ROM_CLK	FW_ROM_CLK - @m60_lib.M60	44B4
FW_SE	FW_SE - @m60_lib.M60	44B3
FW_SM	FW_SM - @m60_lib.M60	44B3
FW_TEST	FW_TEST - @m60_lib.M60	44B3
FW_TPA_C<0>	FW_TPA_C<0> - @m60_lib.M60	46B8
FW_TPA_C<1>	FW_TPA_C<1> - @m60_lib.M60	46B7
FW_VP	FW_VP - @m60_lib.M60	46D4
FW_XTAL_X0	FW_XTAL_X0 - @m60_lib.M60	44D2 44D3
FW_XTAL_XI	FW_XTAL_XI - @m60_lib.M60	44D2 44D3
FW_XTAL_XR	FW_XTAL_XR - @m60_lib.M60	44D2
GATE_3V3_S3	GATE_3V3_S3 - @m60_lib.M60	83C2
GATE_5V_S3	GATE_5V_S3 - @m60_lib.M60	83D2
GATE_12V_S0	GATE_12V_S0 - @m60_lib.M60	83A6
GND_AUDIO_CODEC	GND_AUDIO_CODEC - @m60_lib.M60	68B7 68D2 72B8 72C8 73A8
		73D4 74A2 74A3 74A5 74A7
		74B5 74B7 74C1 74C3 74C5
		74C6 74C6 74D1
GND_AUDIO_CODEC_EMI1	GND_AUDIO_CODEC_EMI1 - @m60_lib.M60	73A7
GND_AUDIO_MIC_CONN	GND_AUDIO_MIC_CONN - @m60_lib.M60	47C2 73C2
GND_AUDIO_SPKRAMP	GND_AUDIO_SPKRAMP - @m60_lib.M60	6C2 72B1 74D3
GND_AUDIO_SPKRAMP_PL	GND_AUDIO_SPKRAMP_PLANE -	72A6 72B2 72B5 72D2 72D8
ANE	@m60_lib.M60	74C3
GND_BNDI	GND_BNDI - @m60_lib.M60	47B2 47D2
GND_CHASSIS_AUDIO_EX	GND_CHASSIS_AUDIO_EXTERNAL -	6B2 73C7
TERNAL	@m60_lib.M60	
	GND_CHASSIS_IO_LEFT - @m60_lib.M60	6B2
	GND_CHASSIS_USB - @m60_lib.M60	6B2 47A4 47B4 47C4
	GND_CHASSIS_IO_LEFT - @m60_lib.M60	6B2
GND_CHASSIS_AUDIO_EX	GND_CHASSIS_AUDIO_EXTERNAL_J -	73A8 73C5 73C8 74C1 74C3
TERNAL_J	@m60_lib.M60	
GND_CHASSIS_AUDIO_IN	GND_CHASSIS_AUDIO_INTERNAL -	6A2 73C4
TERNAL	@m60_lib.M60	
	GND_CHASSIS_BNDI - @m60_lib.M60	6A2 47C2 47C2 47D2
GND_CHASSIS_FIREWIRE	GND_CHASSIS_FIREWIRE - @m60_lib.M60	6B2 46A1 46C1
	GND_CHASSIS_RJ45 - @m60_lib.M60	6B2 43C6
	GND_CHASSIS_VGA - @m60_lib.M60	6B2 97C4
	GND_CHASSIS_RJ45 - @m60_lib.M60	6B2 43C6
	GND_CHASSIS_IO_RIGHT - @m60_lib.M60	6B1
GND_CHASSIS_SLOT	GND_CHASSIS_SLOT - @m60_lib.M60	6D6 97C5
GND_GPUVCORE_SGND	GND_GPUVCORE_SGND - @m60_lib.M60	85C7
GND_GPU_PCIE_PVSS	GND_GPU_PCIE_PVSS - @m60_lib.M60	84B8
GND_IMVP6_SGND	GND_IMVP6_SGND - @m60_lib.M60	75A4 75B6 75B8 75D7
GND_NB_VSSA_LVDS	GND_NB_VSSA_LVDS - @m60_lib.M60	17C6 19C2
	TP_GND_NB_VSSA_LVDS - @m60_lib.M60	19C1
GND_NEXT_TO_SMC	GND_NEXT_TO_SMC - @m60_lib.M60	59B2
GND_SMC_AVSS	GND_SMC_AVSS - @m60_lib.M60	58B2 58C4 59A3 59B3 76B2
		76B6 76C5 85C1
GPUISENS_NEG	GPUISENS_NEG - @m60_lib.M60	85D3
GPUISENS_NTC	GPUISENS_NTC - @m60_lib.M60	85D3
GPUISENS_POS	GPUISENS_POS - @m60_lib.M60	85D3
GPUISENS_RC	GPUISENS_RC - @m60_lib.M60	85D3
GPUVCORE_BOOT	GPUVCORE_BOOT - @m60_lib.M60	85C5
GPUVCORE_COMP	GPUVCORE_COMP - @m60_lib.M60	85C7
GPUVCORE_COMP_R	GPUVCORE_COMP_R - @m60_lib.M60	85C7
GPUVCORE_EN	GPUVCORE_EN - @m60_lib.M60	85C8 88A8
GPUVCORE_FB	GPUVCORE_FB - @m60_lib.M60	85C7
GPUVCORE_FCCM	GPUVCORE_FCCM - @m60_lib.M60	85C7
GPUVCORE_FSET	GPUVCORE_FSET - @m60_lib.M60	85C7
GPUVCORE_IOUT	GPUVCORE_IOUT - @m60_lib.M60	59C5 85D1
	SMC_GPU_ISENSE - @m60_lib.M60	58D5 59C6
GPUVCORE_ISEN	GPUVCORE_ISEN - @m60_lib.M60	85C5
GPUVCORE_LG	GPUVCORE_LG - @m60_lib.M60	85C5
GPUVCORE_PGOOD	GPUVCORE_PGOOD - @m60_lib.M60	77A3 85C8
GPUVCORE_PHASE	GPUVCORE_PHASE - @m60_lib.M60	85C5
GPUVCORE_UG	GPUVCORE_UG - @m60_lib.M60	85C5
GPU_B2	GPU_B2 - @m60_lib.M60	93B3 97B8
GPU_CLK27M	GPU_CLK27M - @m60_lib.M60	92C6
	GPU_XTALIN - @m60_lib.M60	91A5 92C5
GPU_CLK100M_PCIE_N	GPU_CLK100M_PCIE_N - @m60_lib.M60	5C6 34A4 34B2 84A5
GPU_CLK100M_PCIE_P	GPU_CLK100M_PCIE_P - @m60_lib.M60	5C6 34A4 34B2 84A5
GPU_DDC_A_CLK	GPU_DDC_A_CLK - @m60_lib.M60	93A3 97D1
GPU_DDC_A_DATA	GPU_DDC_A_DATA - @m60_lib.M60	93A3 97C1
GPU_DDC_B_CLK	GPU_DDC_B_CLK - @m60_lib.M60	88B1 93A3
	TP_GPU_DDC_B_CLK - @m60_lib.M60	88B3
GPU_DDC_B_DATA	GPU_DDC_B_DATA - @m60_lib.M60	88B1 93A3
	TP_GPU_DDC_B_DATA - @m60_lib.M60	88B3
GPU_DDC_C_CLK	GPU_DDC_C_CLK - @m60_lib.M60	93A1 93A3 94A7 94C7
GPU_DDC_C_DATA	GPU_DDC_C_DATA - @m60_lib.M60	93A1 93A3 94A6 94C7
GPU_DIGON	GPU_DIGON - @m60_lib.M60	6A7 91C3 94C8
GPU_G2	GPU_G2 - @m60_lib.M60	93B3 97A8
GPU_GENERICA	GPU_GENERICA - @m60_lib.M60	91C3 95B4
	TP_GPU_GENERICA - @m60_lib.M60	95B6
GPU_GENERICB	GPU_GENERICB - @m60_lib.M60	91C3 95B4
	TP_GPU_GENERICB - @m60_lib.M60	95B6
GPU_GENERICC	GPU_GENERICC - @m60_lib.M60	91C3 95B4
	TP_GPU_GENERICC - @m60_lib.M60	95B6
GPU_GENERICD	GPU_GENERICD - @m60_lib.M60	91C3
GPU_GPIO_0	GPU_GPIO_0 - @m60_lib.M60	88D5 91D3 94C3
GPU_GPIO_1	GPU_GPIO_1 - @m60_lib.M60	88D5 91D3
GPU_GPIO_2	GPU_GPIO_2 - @m60_lib.M60	88D5 91D3
GPU_GPIO_3	GPU_GPIO_3 - @m60_lib.M60	88D5 91D3
GPU_GPIO_4	GPU_GPIO_4 - @m60_lib.M60	88C5 91D3
GPU_GPIO_5	GPU_GPIO_5 - @m60_lib.M60	88C5 91D3
GPU_GPIO_6	GPU_GPIO_6 - @m60_lib.M60	88C5 91D3
GPU_GPIO_7	GPU_GPIO_7 - @m60_lib.M60	88C3 91D3
	TP_GPU_GPIO_7 - @m60_lib.M60	88C5
GPU_GPIO_8	GPU_GPIO_8 - @m60_lib.M60	88C5 91D3
GPU_GPIO_9	GPU_GPIO_9 - @m60_lib.M60	88C5 91C3
GPU_GPIO_10	GPU_GPIO_10 - @m60_lib.M60	88C3 91C3
	NC_GPU_GPIO_10 - @m60_lib.M60	88C5
GPU_GPIO_11	GPU_GPIO_11 - @m60_lib.M60	88B5 91C3
GPU_GPIO_12	GPU_GPIO_12 - @m60_lib.M60	88C5 91C3
GPU_GPIO_13	GPU_GPIO_13 - @m60_lib.M60	88C5 91C3
GPU_GPIO_14	GPU_GPIO_14 - @m60_lib.M60	88C1 91C3
	TP_GPU_GPIO_14 - @m60_lib.M60	88C3
GPU_GPIO_15	GPU_GPIO_15 - @m60_lib.M60	88B4 91C3
	GPU_VCORE_LOW - @m60_lib.M60	88B5
GPU_GPIO_17	GPU_GPIO_17 - @m60_lib.M60	88C1 91C3
	TP_GPU_GPIO_17 - @m60_lib.M60	88C3
GPU_GPIO_18	GPU_GPIO_18 - @m60_lib.M60	91D5 95B4
GPU_GPIO_19	GPU_GPIO_19 - @m60_lib.M60	91D5 95B4
GPU_GPIO_20	GPU_GPIO_20 - @m60_lib.M60	91D5 95B4
GPU_GPIO_21	GPU_GPIO_21 - @m60_lib.M60	91D5 95B4
GPU_GPIO_22	GPU_GPIO_22 - @m60_lib.M60	91D5 95B4
GPU_GPIO_23	GPU_GPIO_23 - @m60_lib.M60	91D5 95B4
GPU_GPIO_24	GPU_GPIO_24 - @m60_lib.M60	88B5 91D5
GPU_GPIO_25	GPU_GPIO_25 - @m60_lib.M60	91D5 95C4
GPU_GPIO_26	GPU_GPIO_26 - @m60_lib.M60	91D5 95C4
GPU_GPIO_27	GPU_GPIO_27 - @m60_lib.M60	88B5 91D5
GPU_GPIO_28	GPU_GPIO_28 - @m60_lib.M60	88B5 91D5
GPU_GPIO_29	GPU_GPIO_29 - @m60_lib.M60	88B5 91C5
GPU_GPIO_30	GPU_GPIO_30 - @m60_lib.M60	91C5 95C4
GPU_GPIO_31	GPU_GPIO_31 - @m60_lib.M60	91C5 95C4
GPU_GPIO_32	GPU_GPIO_32 - @m60_lib.M60	91C5 95C4
GPU_GPIO_33	GPU_GPIO_33 - @m60_lib.M60	91C5 95C4
GPU_GPIO_34	GPU_GPIO_34 - @m60_lib.M60	91C5 95C4
GPU_H2SYNC	GPU_H2SYNC - @m60_lib.M60	93B3 97A4
GPU_HPD	GPU_HPD - @m60_lib.M60	93A5 97C1
GPU_HSYNC_BUF	GPU_HSYNC_BUF - @m60_lib.M60	97A4
GPU_MEMTEST	GPU_MEMTEST - @m60_lib.M60	87A3
GPU_MVREFD0	GPU_MVREFD0 - @m60_lib.M60	87B7
GPU_MVREFD1	GPU_MVREFD1 - @m60_lib.M60	87B3
GPU_MVREFS0	GPU_MVREFS0 - @m60_lib.M60	87B7
GPU_MVREFS1	GPU_MVREFS1 - @m60_lib.M60	87B3
GPU_PCIE_CALI	GPU_PCIE_CALI - @m60_lib.M60	84A3
GPU_PCIE_CALRN	GPU_PCIE_CALRN - @m60_lib.M60	84A3
GPU_PCIE_CALRP	GPU_PCIE_CALRP - @m60_lib.M60	84A3
GPU_PWM_RST_L	GPU_PWM_RST_L - @m60_lib.M60	6C7 94B3
GPU_R2	GPU_R2 - @m60_lib.M60	93B3 97A8
GPU_TEST_MCLK	GPU_TEST_MCLK - @m60_lib.M60	87A3
GPU_TEST_YCLK	GPU_TEST_YCLK - @m60_lib.M60	87A3
GPU_TV_C	GPU_TV_C - @m60_lib.M60	88B1 93B3
	TP_GPU_TV_C - @m60_lib.M60	88B3
GPU_TV_COMP	GPU_TV_COMP - @m60_lib.M60	88B1 93B3
	TP_GPU_TV_COMP - @m60_lib.M60	88B3
GPU_TV_Y	GPU_TV_Y - @m60_lib.M60	88B1 93B3
	TP_GPU_TV_Y - @m60_lib.M60	88B3
GPU_V2SYNC	GPU_V2SYNC - @m60_lib.M60	93B3 97A4
GPU_VARY_BL	GPU_VARY_BL - @m60_lib.M60	91C3 94B3
GPU_VGA_B	GPU_VGA_B - @m60_lib.M60	88C1 93C3
	TP_GPU_VGA_B - @m60_lib.M60	88C3
GPU_VGA_G	GPU_VGA_G - @m60_lib.M60	88C1 93C3
	TP_GPU_VGA_G - @m60_lib.M60	88C3
GPU_VGA_HSYNC	GPU_VGA_HSYNC - @m60_lib.M60	88B1 93B3
	TP_GPU_VGA_HSYNC - @m60_lib.M60	88B3
GPU_VGA_R	GPU_VGA_R - @m60_lib.M60	88C1 93C3
	TP_GPU_VGA_R - @m60_lib.M60	88C3
GPU_VGA_VSYNC	GPU_VGA_VSYNC - @m60_lib.M60	88B1 93B3
	TP_GPU_VGA_VSYNC - @m60_lib.M60	88B3
GPU_VSYNC_BUF	GPU_VSYNC_BUF - @m60_lib.M60	97A4
GPU_XTALOUT	GPU_XTALOUT - @m60_lib.M60	91A5
I2C_ALS_SCL	I2C_ALS_SCL - @m60_lib.M60	59C1 59C8
	SMB_A_S3_CLK - @m60_lib.M60	58B5 59C2 59D1
I2C_ALS_SDA	I2C_ALS_SDA - @m60_lib.M60	59C1 59C8
	SMB_A_S3_DATA - @m60_lib.M60	58B5 59C2 59D1
IDE_CSEL_PD	IDE_CSEL_PD - @m60_lib.M60	38C3
IDE_DASP_L	IDE_DASP_L - @m60_lib.M60	38C3
IDE_DASP_L_DS	IDE_DASP_L_DS - @m60_lib.M60	38B3
IDE_IOCS16_PU	IDE_IOCS16_PU - @m60_lib.M60	38C1
IDE_IRQ14	IDE_IRQ14 - @m60_lib.M60	21B6 38C4
IDE_PDA<0>	IDE_PDA<0> - @m60_lib.M60	21B5 38C3
IDE_PDA<1>	IDE_PDA<1> - @m60_lib.M60	21B5 38C3
IDE_PDA<2>	IDE_PDA<2> - @m60_lib.M60	21B5 38C1
IDE_PDCS1_L	IDE_PDCS1_L - @m60_lib.M60	21B5 38C3
IDE_PDCS3_L	IDE_PDCS3_L - @m60_lib.M60	21B5 38C1
IDE_PDD<0>	IDE_PDD<0> - @m60_lib.M60	21C5 38C3
IDE_PDD<1>	IDE_PDD<1> - @m60_lib.M60	21B5 38C3
IDE_PDD<2>	IDE_PDD<2> - @m60_lib.M60	21B5 38D3
IDE_PDD<3>	IDE_PDD<3> - @m60_lib.M60	21B5 38D3
IDE_PDD<4>	IDE_PDD<4> - @m60_lib.M60	21B5 38D3
IDE_PDD<5>	IDE_PDD<5> - @m60_lib.M60	21B5 38D3
IDE_PDD<6>	IDE_PDD<6> - @m60_lib.M60	21B5 38D3
IDE_PDD<7>	IDE_PDD<7> - @m60_lib.M60	21B5 38D3
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IDE_PDD<9>	IDE_PDD<9> - @m60_lib.M60	5C8 21B5 38D1
IDE_PDD<10>	IDE_PDD<10> - @m60_lib.M60	21B5 38D1
IDE_PDD<11>	IDE_PDD<11> - @m60_lib.M60	21B5 38D1
IDE_PDD<12>	IDE_PDD<12> - @m60_lib.M60	21B5 38D1
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IDE_PDD<14>	IDE_PDD<14> - @m60_lib.M60	21B5 38D1
IDE_PDD<15>	IDE_PDD<15> - @m60_lib.M60	21B5 38C1
IDE_PDDACK_L	IDE_PDDACK_L - @m60_lib.M60	21B6 38C1
IDE_PDDREQ	IDE_PDDREQ - @m60_lib.M60	21B6 38C4
IDE_PDIORDY	IDE_PDIORDY - @m60_lib.M60	5C8 21B6 38C4
IDE_PDIOR_L	IDE_PDIOR_L - @m60_lib.M60	5C8 21B6 38C1
IDE_PDIOW_L	IDE_PDIOW_L - @m60_lib.M60	21B6 38C3
IDE_RESET_L	IDE_RESET_L - @m60_lib.M60	23C3 38D3 38D5
IMVP6_BOOT1	IMVP6_BOOT1 - @m60_lib.M60	75A8 75C5
IMVP6_BOOT2	IMVP6_BOOT2 - @m60_lib.M60	75A6 75C5
IMVP6_COMP	IMVP6_COMP - @m60_lib.M60	75A4 75B6
IMVP6_COMP_RC	IMVP6_COMP_RC - @m60_lib.M60	75B7
IMVP6_DFB	IMVP6_DFB - @m60_lib.M60	75A4 75B5
IMVP6_DROOP	IMVP6_DROOP - @m60_lib.M60	75A4 75B4
IMVP6_FB	IMVP6_FB - @m60_lib.M60	75A4 75B6
IMVP6_FB2	IMVP6_FB2 - @m60_lib.M60	75A4 75B6
IMVP6_FET_RC1	IMVP6_FET_RC1 - @m60_lib.M60	75A8 75C2
IMVP6_FET_RC2	IMVP6_FET_RC2 - @m60_lib.M60	75A6 75B2
IMVP6_ISEN1	IMVP6_ISEN1 - @m60_lib.M60	75A8 75C5
IMVP6_ISEN2	IMVP6_ISEN2 - @m60_lib.M60	75A6 75C5
IMVP6_LGATE1	IMVP6_LGATE1 - @m60_lib.M60	75A8 75C5
IMVP6_LGATE2	IMVP6_LGATE2 - @m60_lib.M60	75A6 75C5
IMVP6_NTC	IMVP6_NTC - @m60_lib.M60	75C7
IMVP6_NTC_R	IMVP6_NTC_R - @m60_lib.M60	75C7
IMVP6_OCSET	IMVP6_OCSET - @m60_lib.M60	75A4 75B5
IMVP6_PHASE1	IMVP6_PHASE1 - @m60_lib.M60	75A8 75C5
IMVP6_PHASE2	IMVP6_PHASE2 - @m60_lib.M60	75A6 75C5
IMVP6_RBIAS	IMVP6_RBIAS - @m60_lib.M60	75A4 75B6
IMVP6_RTN	IMVP6_RTN - @m60_lib.M60	75A4 75B5
IMVP6_SOFT	IMVP6_SOFT - @m60_lib.M60	75A4 75C6
IMVP6_UGATE1	IMVP6_UGATE1 - @m60_lib.M60	75A8 75C5
IMVP6_UGATE2	IMVP6_UGATE2 - @m60_lib.M60	75A6 75C5
IMVP6_VDIFF	IMVP6_VDIFF - @m60_lib.M60	75A4 75B6
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m60_lib.M60	75B7
IMVP6_VO	IMVP6_VO - @m60_lib.M60	75A4 75B4
IMVP6_VO_R	IMVP6_VO_R - @m60_lib.M60	75B4
IMVP6_VR_TT	IMVP6_VR_TT - @m60_lib.M60	75C7
IMVP6_VSEN	IMVP6_VSEN - @m60_lib.M60	75A4 75B5
IMVP6_VSUM	IMVP6_VSUM - @m60_lib.M60	75A4 75C5
IMVP6_VSUM_R1	IMVP6_VSUM_R1 - @m60_lib.M60	75A8 75C2
IMVP6_VSUM_R2	IMVP6_VSUM_R2 - @m60_lib.M60	75A6 75B2
IMVP6_VW	IMVP6_VW - @m60_lib.M60	75A4 75B6
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m60_lib.M60	75C6
IMVP_PGD_IN	IMVP_PGD_IN - @m60_lib.M60	75C6 77C7
IMVP_VID<0>	IMVP_VID<0> - @m60_lib.M60	75C6
IMVP_VID<1>	IMVP_VID<1> - @m60_lib.M60	75C7

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IMVP_VID<2>          IMVP_VID<2> - @m60_lib.M60          75C7
IMVP_VID<3>          IMVP_VID<3> - @m60_lib.M60          75C7
IMVP_VID<4>          IMVP_VID<4> - @m60_lib.M60          75C7
IMVP_VID<5>          IMVP_VID<5> - @m60_lib.M60          75C7
IMVP_VID<6>          IMVP_VID<6> - @m60_lib.M60          75C7
IMVP_VR_ON           IMVP_VR_ON - @m60_lib.M60           58D7 75C6
INT_PIRQA_L          INT_PIRQA_L - @m60_lib.M60          22A7 26D2
INT_PIRQB_L          INT_PIRQB_L - @m60_lib.M60          22A7 26D2
INT_PIRQC_L          INT_PIRQC_L - @m60_lib.M60          22A7 26D2
INT_PIRQD_L          INT_PIRQD_L - @m60_lib.M60          22A7 26D2 44B5
INT_SERIRQ           INT_SERIRQ - @m60_lib.M60           23C8 58C7 60C3 67C6
ISENSE_CAL_EN        ISENSE_CAL_EN - @m60_lib.M60        58B7 76A7
ITPRESET_L           ITPRESET_L - @m60_lib.M60           11B3
ITP_TDO              ITP_TDO - @m60_lib.M60              11B3
ITS_ALIVE            ITS_ALIVE - @m60_lib.M60            6A7
ITS_PLUGGED_IN       ITS_PLUGGED_IN - @m60_lib.M60       6A8
KBC_MDE              KBC_MDE - @m60_lib.M60              58C2
LCD_PWM              LCD_PWM - @m60_lib.M60              6D8 94B1
LCD_PWM_R            LCD_PWM_R - @m60_lib.M60            94B2
LCD_PWREN_L          LCD_PWREN_L - @m60_lib.M60          94C8
LCD_PWREN_L_RC       LCD_PWREN_L_RC - @m60_lib.M60       94C7
LCD_SHOULD_ON        LCD_SHOULD_ON - @m60_lib.M60        6A6
LED_PP1V05_S0_N      LED_PP1V05_S0_N - @m60_lib.M60      81A4
LED_PP1V05_S0_P      LED_PP1V05_S0_P - @m60_lib.M60      81A4
LED_PP1V5_S0_N       LED_PP1V5_S0_N - @m60_lib.M60       80A3
LED_PP1V5_S0_P       LED_PP1V5_S0_P - @m60_lib.M60       80A4
LED_PP1V8_S3_N       LED_PP1V8_S3_N - @m60_lib.M60       79A4
LED_PP1V8_S3_P       LED_PP1V8_S3_P - @m60_lib.M60       79A4
LPC_AD<0>            LPC_AD<0> - @m60_lib.M60            21D4 58D7 60C6 67C6
LPC_AD<1>            LPC_AD<1> - @m60_lib.M60            21D4 58D7 60C6 67C6
LPC_AD<2>            LPC_AD<2> - @m60_lib.M60            21D4 58C7 60C3 67C6
LPC_AD<3>            LPC_AD<3> - @m60_lib.M60            21D4 58C7 60C3 67C6
LPC_FRAME_L          LPC_FRAME_L - @m60_lib.M60          21C5 58C7 60C6 67C6
LVDS_A_CLK_N         LVDS_A_CLK_N - @m60_lib.M60         13D5 19D2
                     TP_LVDS_A_CLK_N - @m60_lib.M60      19D1
LVDS_A_CLK_P         LVDS_A_CLK_P - @m60_lib.M60         13C5 19D2
                     TP_LVDS_A_CLK_P - @m60_lib.M60      19D1
LVDS_A_DATA_N<0>     LVDS_A_DATA_N<0> - @m60_lib.M60     13C5 19D2
LVDS_A_DATA_N<1>     LVDS_A_DATA_N<1> - @m60_lib.M60     13C5 19D2
LVDS_A_DATA_N<2>     LVDS_A_DATA_N<2> - @m60_lib.M60     13C5 19D2
LVDS_A_DATA_P<0>     LVDS_A_DATA_P<0> - @m60_lib.M60     13C5 19D2
LVDS_A_DATA_P<1>     LVDS_A_DATA_P<1> - @m60_lib.M60     13C5 19D2
LVDS_A_DATA_P<2>     LVDS_A_DATA_P<2> - @m60_lib.M60     13C5 19D2
LVDS_BKLTCTL         LVDS_BKLTCTL - @m60_lib.M60         13D5 19C2
                     TP_LVDS_BKLTCTL - @m60_lib.M60      19C1
LVDS_BKLTEN          LVDS_BKLTEN - @m60_lib.M60          13D5 19C2
                     TP_LVDS_BKLTEN - @m60_lib.M60       19C1
LVDS_B_CLK_N         LVDS_B_CLK_N - @m60_lib.M60         13C5 19D2
                     TP_LVDS_B_CLK_N - @m60_lib.M60      19D1
LVDS_B_CLK_P         LVDS_B_CLK_P - @m60_lib.M60         13C5 19D2
                     TP_LVDS_B_CLK_P - @m60_lib.M60      19D1
LVDS_B_DATA_N<0>     LVDS_B_DATA_N<0> - @m60_lib.M60     13C5 19D2
LVDS_B_DATA_N<1>     LVDS_B_DATA_N<1> - @m60_lib.M60     13C5 19D2
LVDS_B_DATA_N<2>     LVDS_B_DATA_N<2> - @m60_lib.M60     13C5 19D2
LVDS_B_DATA_P<0>     LVDS_B_DATA_P<0> - @m60_lib.M60     13C5 19D2
LVDS_B_DATA_P<1>     LVDS_B_DATA_P<1> - @m60_lib.M60     13C5 19D2
LVDS_B_DATA_P<2>     LVDS_B_DATA_P<2> - @m60_lib.M60     13C5 19D2
LVDS_CLKCTLA         LVDS_CLKCTLA - @m60_lib.M60         13D5 19C2
                     TP_LVDS_CLKCTLA - @m60_lib.M60      19C1
LVDS_CLKCTLB         LVDS_CLKCTLB - @m60_lib.M60         13D5 19C2
                     TP_LVDS_CLKCTLB - @m60_lib.M60      19C1
LVDS_DDC_CLK         LVDS_DDC_CLK - @m60_lib.M60         13D5 19C2
                     TP_LVDS_DDC_CLK - @m60_lib.M60      19C1
LVDS_DDC_DATA        LVDS_DDC_DATA - @m60_lib.M60        13D5 19C2
                     TP_LVDS_DDC_DATA - @m60_lib.M60     19C1
LVDS_IBG             LVDS_IBG - @m60_lib.M60             13D5 19C2
                     TP_LVDS_IBG - @m60_lib.M60          19C1
LVDS_L_CLK_N         LVDS_L_CLK_N - @m60_lib.M60         93A3 93D2 94A6
LVDS_L_CLK_P         LVDS_L_CLK_P - @m60_lib.M60         93A3 93D2 94A7
LVDS_L_DATA_N<0>     LVDS_L_DATA_N<0> - @m60_lib.M60     93A3 93C2 94A6
LVDS_L_DATA_N<1>     LVDS_L_DATA_N<1> - @m60_lib.M60     93A3 93C2 94A7
LVDS_L_DATA_N<2>     LVDS_L_DATA_N<2> - @m60_lib.M60     93A3 93C2 94A6
LVDS_L_DATA_N<3>     LVDS_L_DATA_N<3> - @m60_lib.M60     93A3 94A6
LVDS_L_DATA_P<0>     LVDS_L_DATA_P<0> - @m60_lib.M60     93A3 93D2 94A7
LVDS_L_DATA_P<1>     LVDS_L_DATA_P<1> - @m60_lib.M60     93A3 93C2 94A6
LVDS_L_DATA_P<2>     LVDS_L_DATA_P<2> - @m60_lib.M60     93A3 93C2 94A7
LVDS_L_DATA_P<3>     LVDS_L_DATA_P<3> - @m60_lib.M60     93A3 94A7
LVDS_U_CLK_N         LVDS_U_CLK_N - @m60_lib.M60         93B3 94B6
LVDS_U_CLK_P         LVDS_U_CLK_P - @m60_lib.M60         93B3 94A7
LVDS_U_DATA_N<0>     LVDS_U_DATA_N<0> - @m60_lib.M60     93B3 94B7
LVDS_U_DATA_N<1>     LVDS_U_DATA_N<1> - @m60_lib.M60     93B3 94B7
LVDS_U_DATA_N<2>     LVDS_U_DATA_N<2> - @m60_lib.M60     93B3 94B7
LVDS_U_DATA_N<3>     LVDS_U_DATA_N<3> - @m60_lib.M60     93B3 94A6
LVDS_U_DATA_P<0>     LVDS_U_DATA_P<0> - @m60_lib.M60     93B3 94B6
LVDS_U_DATA_P<1>     LVDS_U_DATA_P<1> - @m60_lib.M60     93B3 94B6
LVDS_U_DATA_P<2>     LVDS_U_DATA_P<2> - @m60_lib.M60     93B3 94B6
LVDS_U_DATA_P<3>     LVDS_U_DATA_P<3> - @m60_lib.M60     93B3 94A7
LVDS_VDDEN           LVDS_VDDEN - @m60_lib.M60           13D5 19C2
                     TP_LVDS_VDDEN - @m60_lib.M60        19C1
LVDS_VREFH           LVDS_VREFH - @m60_lib.M60           13D5 19C2
                     TP_LVDS_VREFH - @m60_lib.M60        19C1
LVDS_VREFL           LVDS_VREFL - @m60_lib.M60           13D5 19C2
                     TP_LVDS_VREFL - @m60_lib.M60        19C1
MEMVTT_VREF          MEMVTT_VREF - @m60_lib.M60          31B4
MEM_A_A<0>           MEM_A_A<0> - @m60_lib.M60           15C5 28B3
MEM_A_A<13..0>       MEM_A_A<13..0> - @m60_lib.M60       30C6
MEM_A_A<1>           MEM_A_A<1> - @m60_lib.M60           15C5 28B6
MEM_A_A<2>           MEM_A_A<2> - @m60_lib.M60           15C5 28B3
MEM_A_A<3>           MEM_A_A<3> - @m60_lib.M60           15B5 28B6
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MEM_A_A<5>           MEM_A_A<5> - @m60_lib.M60           15B5 28B6
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MEM_A_A<9>           MEM_A_A<9> - @m60_lib.M60           15B5 28C6
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MEM_A_A<13>          MEM_A_A<13> - @m60_lib.M60          15B5 28B3
MEM_A_BS<0>          MEM_A_BS<0> - @m60_lib.M60          15D5 28B6
MEM_A_BS<2..0>       MEM_A_BS<2..0> - @m60_lib.M60       30C6
MEM_A_BS<1>          MEM_A_BS<1> - @m60_lib.M60          15D5 28B3
MEM_A_BS<2>          MEM_A_BS<2> - @m60_lib.M60          15D5 28C6
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MEM_A_DM<2>          MEM_A_DM<2> - @m60_lib.M60          15D5 28C3
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MEM_A_DQ<17>         MEM_A_DQ<17> - @m60_lib.M60         15C7 28C6
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NB_VTTLF_CAP3        NB_VTTLF_CAP3 - @m60_lib.M60        17B4
NC_AUD1              NC_AUD1 - @m60_lib.M60              68C4
NC_AUD2              NC_AUD2 - @m60_lib.M60              68B4
NC_AUD_GPIO_2        NC_AUD_GPIO_2 - @m60_lib.M60        68C7
NC_AUD_LI_TYPE_JACK  NC_AUD_LI_TYPE_JACK - @m60_lib.M60  73D7
NC_AUD_VREF_PORT_A   NC_AUD_VREF_PORT_A - @m60_lib.M60   68C1
NC_AUD_VREF_PORT_C   NC_AUD_VREF_PORT_C - @m60_lib.M60   68C1
NC_AUD_VREF_PORT_D   NC_AUD_VREF_PORT_D - @m60_lib.M60   68C1
NC_FW_NU1            NC_FW_NU1 - @m60_lib.M60            44B3
NC_FW_NU2            NC_FW_NU2 - @m60_lib.M60            44B3
NC_JE350_13          NC_JE350_13 - @m60_lib.M60          47B1
NC_SMC_P20           NC_SMC_P20 - @m60_lib.M60           59D5
                     SMC_P20 - @m60_lib.M60              58D7 59D6
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                     SMC_P21 - @m60_lib.M60              58D7 59D6
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                     SMC_P22 - @m60_lib.M60              58D7 59D6
NC_SMC_P23           NC_SMC_P23 - @m60_lib.M60           59D5
                     SMC_P23 - @m60_lib.M60              58D7 59D6
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                     SMC_P26 - @m60_lib.M60              58D7 59D6
NC_SMC_P27           NC_SMC_P27 - @m60_lib.M60           59D5
                     SMC_P27 - @m60_lib.M60              58D7 59D6
NC_VOL_DOWN          NC_VOL_DOWN - @m60_lib.M60          68C7
NC_VOL_UP            NC_VOL_UP - @m60_lib.M60            68C7
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                     SB_GPIO5 - @m60_lib.M60             26C2
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PANEL_ID             PANEL_ID - @m60_lib.M60             6D6 94C2
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PCIE_A_D2R_C_P       PCIE_A_D2R_C_P - @m60_lib.M60       41D5
PCIE_A_D2R_N         PCIE_A_D2R_N - @m60_lib.M60         5B8 22D4 41D4
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PCIE_B_R2D_C_N       PCIE_B_R2D_C_N - @m60_lib.M60       22D4 53B7
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PCI_CLK_PORT80       PCI_CLK_PORT80 - @m60_lib.M60       34B4 60C3
PCI_CLK_SB           PCI_CLK_SB - @m60_lib.M60           5C8 22A6 34B4
PCI_CLK_SMC          PCI_CLK_SMC - @m60_lib.M60          34C4 58C7
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PCI_FRAME_L	PCI_FRAME_L - @m60_lib.M60	22A7 26D2 44B5
PCI_GNT1_L	PCI_GNT1_L - @m60_lib.M60	22B6 44B5
PCI_IDSEL	PCI_IDSEL - @m60_lib.M60	44B5
PCI_IRDY_L	PCI_IRDY_L - @m60_lib.M60	22A6 26D2 44B5
PCI_LOCK_L	PCI_LOCK_L - @m60_lib.M60	22A6 26D2
PCI_PAR	PCI_PAR - @m60_lib.M60	22A6 44B5
PCI_PERR_L	PCI_PERR_L - @m60_lib.M60	22A6 26D2 44B5
PCI_PME_FW_L	PCI_PME_FW_L - @m60_lib.M60	22B5 44B5
PCI_REQ0_L	PCI_REQ0_L - @m60_lib.M60	22B6 26D2
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PCI_REQ3_L	PCI_REQ3_L - @m60_lib.M60	22B6 26D2
PCI_RST_FW_L	PCI_RST_FW_L - @m60_lib.M60	44A7 44B5
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PCI_STOP_L	PCI_STOP_L - @m60_lib.M60	22A6 26D2 44B5
PCI_TRDY_L	PCI_TRDY_L - @m60_lib.M60	22A6 26D2 44B5
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PEG_R2D_C_P<9>	PEG_R2D_C_P<9> - @m60_lib.M60	13B3 84C5
PEG_R2D_C_P<10>	PEG_R2D_C_P<10> - @m60_lib.M60	13B3 84C5
PEG_R2D_C_P<11>	PEG_R2D_C_P<11> - @m60_lib.M60	13B3 84D5
PEG_R2D_C_P<12>	PEG_R2D_C_P<12> - @m60_lib.M60	13A3 84D5
PEG_R2D_C_P<13>	PEG_R2D_C_P<13> - @m60_lib.M60	13A3 84D5
PEG_R2D_C_P<14>	PEG_R2D_C_P<14> - @m60_lib.M60	13A3 84D5
PEG_R2D_C_P<15>	PEG_R2D_C_P<15> - @m60_lib.M60	13A3 84D5
PEG_R2D_N<0>	PEG_R2D_N<0> - @m60_lib.M60	84D4
PEG_R2D_N<1>	PEG_R2D_N<1> - @m60_lib.M60	84D4
PEG_R2D_N<2>	PEG_R2D_N<2> - @m60_lib.M60	84D4
PEG_R2D_N<3>	PEG_R2D_N<3> - @m60_lib.M60	84D4
PEG_R2D_N<4>	PEG_R2D_N<4> - @m60_lib.M60	84C4
PEG_R2D_N<5>	PEG_R2D_N<5> - @m60_lib.M60	84C4
PEG_R2D_N<6>	PEG_R2D_N<6> - @m60_lib.M60	84C4
PEG_R2D_N<7>	PEG_R2D_N<7> - @m60_lib.M60	84C4
PEG_R2D_N<8>	PEG_R2D_N<8> - @m60_lib.M60	84C4
PEG_R2D_N<9>	PEG_R2D_N<9> - @m60_lib.M60	84C4
PEG_R2D_N<10>	PEG_R2D_N<10> - @m60_lib.M60	84B4
PEG_R2D_N<11>	PEG_R2D_N<11> - @m60_lib.M60	84B4
PEG_R2D_N<12>	PEG_R2D_N<12> - @m60_lib.M60	84B4
PEG_R2D_N<13>	PEG_R2D_N<13> - @m60_lib.M60	84B4
PEG_R2D_N<14>	PEG_R2D_N<14> - @m60_lib.M60	84B4
PEG_R2D_N<15>	PEG_R2D_N<15> - @m60_lib.M60	84B4
PEG_R2D_P<0>	PEG_R2D_P<0> - @m60_lib.M60	84D4
PEG_R2D_P<1>	PEG_R2D_P<1> - @m60_lib.M60	84D4
PEG_R2D_P<2>	PEG_R2D_P<2> - @m60_lib.M60	84D4
PEG_R2D_P<3>	PEG_R2D_P<3> - @m60_lib.M60	84D4
PEG_R2D_P<4>	PEG_R2D_P<4> - @m60_lib.M60	84D4
PEG_R2D_P<5>	PEG_R2D_P<5> - @m60_lib.M60	84C4
PEG_R2D_P<6>	PEG_R2D_P<6> - @m60_lib.M60	84C4
PEG_R2D_P<7>	PEG_R2D_P<7> - @m60_lib.M60	84C4
PEG_R2D_P<8>	PEG_R2D_P<8> - @m60_lib.M60	84C4
PEG_R2D_P<9>	PEG_R2D_P<9> - @m60_lib.M60	84C4
PEG_R2D_P<10>	PEG_R2D_P<10> - @m60_lib.M60	84B4
PEG_R2D_P<11>	PEG_R2D_P<11> - @m60_lib.M60	84B4
PEG_R2D_P<12>	PEG_R2D_P<12> - @m60_lib.M60	84B4
PEG_R2D_P<13>	PEG_R2D_P<13> - @m60_lib.M60	84B4
PEG_R2D_P<14>	PEG_R2D_P<14> - @m60_lib.M60	84B4
PEG_R2D_P<15>	PEG_R2D_P<15> - @m60_lib.M60	84B4
PEG_RESET_L	PEG_RESET_L - @m60_lib.M60	6B7 84A5
PLT_RST_L	PLT_RST_L - @m60_lib.M60	6C8 22A6
PM_BATLOW_L	PM_BATLOW_L - @m60_lib.M60	23C1 58B7
PM_BMBUSY_L	PM_BMBUSY_L - @m60_lib.M60	14B6 23C5
PM_CLKRUN_L	PM_CLKRUN_L - @m60_lib.M60	5B8 23C8 44B5 58C5 60C6 67C6
PM_DPRSLPVR	PM_DPRSLPVR - @m60_lib.M60	14B7 23C3 75C7
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @m60_lib.M60	14B7 58B7 59C5
	DIMM_OVERTEMP_L - @m60_lib.M60	28C3 29C3 59C6
PM_LAN_ENABLE	PM_LAN_ENABLE - @m60_lib.M60	23C3 58D7
PM_PWRBTN_L	PM_PWRBTN_L - @m60_lib.M60	23C3 58D7
PM_PWROK	PM_PWROK - @m60_lib.M60	77B7
PM_RI_L	PM_RI_L - @m60_lib.M60	23D5
PM_RSMRST_L	PM_RSMRST_L - @m60_lib.M60	23C1 58D7
PM_SB_PWROK	PM_SB_PWROK - @m60_lib.M60	23C3 26D6
PM_SLP_S3	PM_SLP_S3 - @m60_lib.M60	77D7 78B8 80C8 81C8
	SYS_PWRUP_L - @m60_lib.M60	77D6 83A8 83B6 83B7 83C5 83C7
PM_SLP_S3_L	PM_SLP_S3_L - @m60_lib.M60	23C3 58C5 77D8 79A7 88A6
	MEMVTT_EN - @m60_lib.M60	31B5 79A6
PM_SLP_S4	PM_SLP_S4 - @m60_lib.M60	77B6 77C7 79C8 83C4
PM_SLP_S4_L	PM_SLP_S4_L - @m60_lib.M60	23C3 58C5 77C8
PM_SLP_S5_L	PM_SLP_S5_L - @m60_lib.M60	23C3 58C5
PM_STPCPU_L	PM_STPCPU_L - @m60_lib.M60	23C8 33C4
PM_STPPCI_L	PM_STPPCI_L - @m60_lib.M60	23C8 33C4
PM_SUS_STAT_L	PM_SUS_STAT_L - @m60_lib.M60	23C5 58C5 60C3 67C6
PM_SYSRST_L	PM_SYSRST_L - @m60_lib.M60	5B8 23C5 26C3 58B7
PM_THRMTRIP_L	PM_THRMTRIP_L - @m60_lib.M60	7C6 14B6 21C2 59C7
PM_THRM_L	PM_THRM_L - @m60_lib.M60	10D3 23C8 58B7
POWER_BUTTON_L	POWER_BUTTON_L - @m60_lib.M60	5D1 59C8
PP0V9_S0_PGOOD	PP0V9_S0_PGOOD - @m60_lib.M60	77B8 79A2
PP1V2_S0_GPU_VDDPLL	PP1V2_S0_GPU_VDDPLL - @m60_lib.M60	91B6
PP1V05_S0_PGOOD	PP1V05_S0_PGOOD - @m60_lib.M60	77C8 81B2
PP1V5_S0_NB_3GPLL_F	PP1V5_S0_NB_3GPLL_F - @m60_lib.M60	19A5
PP1V5_S0_NB_VCC3G	PP1V5_S0_NB_VCC3G - @m60_lib.M60	17D6 19A3
PP1V5_S0_NB_VCCA_3GPLL	PP1V5_S0_NB_VCCA_3GPLL - @m60_lib.M60	17D6 19A3
PP1V5_S0_NB_VCCA_DPLLA	PP1V5_S0_NB_VCCA_DPLLA - @m60_lib.M60	17C6 19C4
	TP_NB_VCCA_DPLLA - @m60_lib.M60	19C5
PP1V5_S0_NB_VCCA_DPLLB	PP1V5_S0_NB_VCCA_DPLLB - @m60_lib.M60	17C6 19C4
	TP_NB_VCCA_DPLLB - @m60_lib.M60	19C5
PP1V5_S0_NB_VCCA_HPLL	PP1V5_S0_NB_VCCA_HPLL - @m60_lib.M60	17C6 19C6
PP1V5_S0_NB_VCCA_MPLL	PP1V5_S0_NB_VCCA_MPLL - @m60_lib.M60	17C6 19C6
PP1V5_S0_PGOOD	PP1V5_S0_PGOOD - @m60_lib.M60	77C8 80B2
PP1V5_S0_SB_R	PP1V5_S0_SB_R - @m60_lib.M60	25A7
PP1V5_S0_SB_VCC1_5_B	PP1V5_S0_SB_VCC1_5_B - @m60_lib.M60	22C1 24D5 25B7
PP1V5_S0_SB_VCCDMIPLL	PP1V5_S0_SB_VCCDMIPLL - @m60_lib.M60	24B5 25A6
PP1V8R2V0_S0_GPU_VDDRH0	PP1V8R2V0_S0_GPU_VDDRH0 - @m60_lib.M60	87A7
PP1V8R2V0_S0_GPU_VDDRH1	PP1V8R2V0_S0_GPU_VDDRH1 - @m60_lib.M60	87B3
PP1V8R3V3_S0_GPU_VDDR4_F	PP1V8R3V3_S0_GPU_VDDR4_F - @m60_lib.M60	91B6
PP1V8R3V3_S0_GPU_VDDR5_F	PP1V8R3V3_S0_GPU_VDDR5_F - @m60_lib.M60	91B6
PP1V8_FB_A0_VDDA0	PP1V8_FB_A0_VDDA0 - @m60_lib.M60	89D7
PP1V8_FB_A0_VDDA1	PP1V8_FB_A0_VDDA1 - @m60_lib.M60	89D7
PP1V8_FB_A1_VDDA0	PP1V8_FB_A1_VDDA0 - @m60_lib.M60	89D4
PP1V8_FB_A1_VDDA1	PP1V8_FB_A1_VDDA1 - @m60_lib.M60	89D4
PP1V8_FB_B0_VDDA0	PP1V8_FB_B0_VDDA0 - @m60_lib.M60	90D7
PP1V8_FB_B0_VDDA1	PP1V8_FB_B0_VDDA1 - @m60_lib.M60	90D7
PP1V8_FB_B1_VDDA0	PP1V8_FB_B1_VDDA0 - @m60_lib.M60	90D4
PP1V8_FB_B1_VDDA1	PP1V8_FB_B1_VDDA1 - @m60_lib.M60	90D4
PP2V5_ENET_CTAP	PP2V5_ENET_CTAP - @m60_lib.M60	43D7
PP2V5_S0_GPU_A2VDD	PP2V5_S0_GPU_A2VDD - @m60_lib.M60	93B7
PP2V5_S0_GPU_AVDD	PP2V5_S0_GPU_AVDD - @m60_lib.M60	93C7
PP2V5_S0_GPU_LPVDD	PP2V5_S0_GPU_LPVDD - @m60_lib.M60	93B7
PP2V5_S0_GPU_LVDDR	PP2V5_S0_GPU_LVDDR - @m60_lib.M60	93B7
PP2V5_S0_GPU_PVDD_F	PP2V5_S0_GPU_PVDD_F - @m60_lib.M60	91A6
PP2V5_S0_GPU_TPVDD	PP2V5_S0_GPU_TPVDD - @m60_lib.M60	93C7
PP2V5_S0_GPU_TXVDDR	PP2V5_S0_GPU_TXVDDR - @m60_lib.M60	93C7
PP2V5_S0_GPU_VDD1DI	PP2V5_S0_GPU_VDD1DI - @m60_lib.M60	93C8
PP2V5_S0_GPU_VDD2DI	PP2V5_S0_GPU_VDD2DI - @m60_lib.M60	93B8
PP2V5_S0_PGOOD	PP2V5_S0_PGOOD - @m60_lib.M60	77B8 83B2
PP2V5_S5	PP2V5_S5 - @m60_lib.M60	57C8 83C7
PP3V3R12V_LCD_CONN	PP3V3R12V_LCD_CONN - @m60_lib.M60	94A6 94A6 94A7 94C5
PP3V3_AUDIO_SPDIF_EMI	PP3V3_AUDIO_SPDIF_EMI - @m60_lib.M60	73B7
PP3V3_AUDIO_SPDIF_JACK	PP3V3_AUDIO_SPDIF_JACK - @m60_lib.M60	73B5 73D8
PP3V3_AVCC_SMC	PP3V3_AVCC_SMC - @m60_lib.M60	58D3
PP3V3_AVREF_SMC	PP3V3_AVREF_SMC - @m60_lib.M60	58D2 59A3
PP3V3_FW_ESD	PP3V3_FW_ESD - @m60_lib.M60	46A5 46A6 46B5 46C5 46D5
PP3V3_FW_ESD_F	PP3V3_FW_ESD_F - @m60_lib.M60	46A7
PP3V3_INTERCON	PP3V3_INTERCON - @m60_lib.M60	72C7
PP3V3_LCD_SW	PP3V3_LCD_SW - @m60_lib.M60	94C6
PP3V3_S0_CK410_VDD48	PP3V3_S0_CK410_VDD48 - @m60_lib.M60	33D5
PP3V3_S0_CK410_VDDA	PP3V3_S0_CK410_VDDA - @m60_lib.M60	33C6
PP3V3_S0_CK410_VDD_CPU_SRC	PP3V3_S0_CK410_VDD_CPU_SRC - @m60_lib.M60	33D6
PP3V3_S0_CK410_VDD_PCI	PP3V3_S0_CK410_VDD_PCI - @m60_lib.M60	33D5
PP3V3_S0_CK410_VDD_REF	PP3V3_S0_CK410_VDD_REF - @m60_lib.M60	33C5
PP3V3_S0_IMVP6_3V3	PP3V3_S0_IMVP6_3V3 - @m60_lib.M60	75D6
PP3V3_S5_FW_VDDA	PP3V3_S5_FW_VDDA - @m60_lib.M60	44D5 45C6
PP3V3_S5_SB_RTC	PP3V3_S5_SB_RTC - @m60_lib.M60	5D2 21D6 24B3 25A3 26D7
PP3V3_TPM_3VSB	PP3V3_TPM_3VSB - @m60_lib.M60	59C5 67C4
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @m60_lib.M60	68A2 68D2 74C4 74D8
PP4V5_S5_AUDIO_ANALOG	PP4V5_S5_AUDIO_ANALOG - @m60_lib.M60	82C8 83D5
PP5V_BNDI_LE340	PP5V_BNDI_LE340 - @m60_lib.M60	47D3
PP5V_S0_DDC	PP5V_S0_DDC - @m60_lib.M60	97D4
PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @m60_lib.M60	97D5
PP5V_S0_GPUVCORE_VCC	PP5V_S0_GPUVCORE_VCC - @m60_lib.M60	85D7 88D8
PP5V_S0_IMVP6_VDD	PP5V_S0_IMVP6_VDD - @m60_lib.M60	75D6
PP5V_S0_SB_V5REF	PP5V_S0_SB_V5REF - @m60_lib.M60	24D5 25D7
PP5V_S3_BNDI	PP5V_S3_BNDI - @m60_lib.M60	47B2 47D1
PP5V_S5_SB_V5REF_SUS	PP5V_S5_SB_V5REF_SUS - @m60_lib.M60	24D5 25C7
PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @m60_lib.M60	47D7
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @m60_lib.M60	47D5
PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @m60_lib.M60	47C7
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @m60_lib.M60	47C5
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @m60_lib.M60	47B7
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @m60_lib.M60	47B5
PP12V_AUD_SPKRAMP_PLANE	PP12V_AUD_SPKRAMP_PLANE - @m60_lib.M60	72D5
PP12V_L7502	PP12V_L7502 - @m60_lib.M60	76D7
PP12V_S5_CPU_REG	PP12V_S5_CPU_REG - @m60_lib.M60	75C3 75D4 75D7 76C8 76D6
PPFW_PORT0_VP	PPFW_PORT0_VP - @m60_lib.M60	46D2
	PPFW_PORT1_VP - @m60_lib.M60	46B2 46D1
	PPFW_PORTS_VP - @m60_lib.M60	46D3
PPFW_PORT0_VP_FL	PPFW_PORT0_VP_FL - @m60_lib.M60	46C2
PPFW_PORT1_VP_FL	PPFW_PORT1_VP_FL - @m60_lib.M60	46B2
PPVCORE_S0_GPU_MPVDD	PPVCORE_S0_GPU_MPVDD - @m60_lib.M60	91A6
PPVCORE_S0_GPU_VDDCI	PPVCORE_S0_GPU_VDDCI - @m60_lib.M60	86C7
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @m60_lib.M60	75D6
PPV_3V3_AUDIO_CODEC	PPV_3V3_AUDIO_CODEC - @m60_lib.M60	68D6
Q4201_3	Q4201_3 - @m60_lib.M60	42D6
Q5950_1	Q5950_1 - @m60_lib.M60	59A2
R6597_2	R6597_2 - @m60_lib.M60	65A6
R7504_1	R7504_1 - @m60_lib.M60	75A8 75C1
R7507_1	R7507_1 - @m60_lib.M60	75A6 75B1
R8599_2	R8599_2 - @m60_lib.M60	85C4
R9499_1	R9499_1 - @m60_lib.M60	94C8
RSMRST_PWRGD	RSMRST_PWRGD - @m60_lib.M60	58D7 76D1
SATA_A_D2R_N	SATA_A_D2R_N - @m60_lib.M60	21B6 38A6
	TP_SATA_A_D2R_N - @m60_lib.M60	38A5
SATA_A_D2R_P	SATA_A_D2R_P - @m60_lib.M60	21B6 38A6
	TP_SATA_A_D2R_P - @m60_lib.M60	38A5
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @m60_lib.M60	21B6 38A6
	TP_SATA_A_R2D_N - @m60_lib.M60	38A5
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @m60_lib.M60	21B6 38A6
	TP_SATA_A_R2D_P - @m60_lib.M60	38A5
SATA_C_D2R_C_N	SATA_C_D2R_C_N - @m60_lib.M60	38B8
SATA_C_D2R_C_P	SATA_C_D2R_C_P - @m60_lib.M60	38B8
SATA_C_D2R_N	SATA_C_D2R_N - @m60_lib.M60	21B6 38B6
SATA_C_D2R_P	SATA_C_D2R_P - @m60_lib.M60	21B6 38B6
SATA_C_DET_L	SATA_C_DET_L - @m60_lib.M60	23D2 38B5
SATA_C_PWR_EN_L	SATA_C_PWR_EN_L - @m60_lib.M60	23A3 23B3
SATA_C_R2D_C_N	SATA_C_R2D_C_N - @m60_lib.M60	21B6 38B6
SATA_C_R2D_C_P	SATA_C_R2D_C_P - @m60_lib.M60	21B6 38B6
SATA_C_R2D_N	SATA_C_R2D_N - @m60_lib.M60	38B8
SATA_C_R2D_P	SATA_C_R2D_P - @m60_lib.M60	38B8
SATA_RBIAS_N	SATA_RBIAS_N - @m60_lib.M60	21B6 38C7
	SATA_RBIAS_P - @m60_lib.M60	21B6 38C7
	SATA_RBIAS - @m60_lib.M60	38C7
	SATA_RBIAS_P - @m60_lib.M60	21B6 38C7
	SATA_RBIAS - @m60_lib.M60	38C7
SB_A20GATE	SB_A20GATE - @m60_lib.M60	21C4
SB_ACZ_BITCLK	SB_ACZ_BITCLK - @m60_lib.M60	21C6
SB_ACZ_RST_L	SB_ACZ_RST_L - @m60_lib.M60	21C6
SB_ACZ_SDATAOUT	SB_ACZ_SDATAOUT - @m60_lib.M60	21C6
SB_ACZ_SYNC	SB_ACZ_SYNC - @m60_lib.M60	21C6
SB_CLK14P3M_TIMER	SB_CLK14P3M_TIMER - @m60_lib.M60	5B8 23D3 34D4
SB_CLK48M_USBCTLR	SB_CLK48M_USBCTLR - @m60_lib.M60	5B8 23D3 34C4
SB_CLK100M_DMI_N	SB_CLK100M_DMI_N - @m60_lib.M60	5B8 22C2 34A4 34C2
SB_CLK100M_DMI_P	SB_CLK100M_DMI_P - @m60_lib.M60	5B8 22C2 34A4 34C2
SB_CLK100M_SATA_N	SB_CLK100M_SATA_N - @m60_lib.M60	5C8 21B6 34B4 34C2
SB_CLK100M_SATA_OE_L	SB_CLK100M_SATA_OE_L - @m60_lib.M60	23C3 33B4
SB_CLK100M_SATA_P	SB_CLK100M_SATA_P - @m60_lib.M60	5C8 21B6 34B4 34C2
SB_CRT_TVOUT_MUX	SB_CRT_TVOUT_MUX - @m60_lib.M60	22B5
SB_GPIO2	SB_GPIO2 - @m60_lib.M60	22A6 26C2
SB_GPIO3	SB_GPIO3 - @m60_lib.M60	22A6 26C2
SB_GPIO4	SB_GPIO4 - @m60_lib.M60	22A6 26C2
SB_GPIO19	SB_GPIO19 - @m60_lib.M60	23D3
SB_GPIO21	SB_GPIO21 - @m60_lib.M60	23D3
SB_GPIO26	SB_GPIO26 - @m60_lib.M60	23C7
SB_GPIO29	SB_GPIO29 - @m60_lib.M60	22C4 22D8
SB_GPIO30	SB_GPIO30 - @m60_lib.M60	22C4 22D8
SB_GPIO31	SB_GPIO31 - @m60_lib.M60	22C4 22D8
SB_GPIO37	SB_GPIO37 - @m60_lib.M60	23D3
SB_INTVRMEN	SB_INTVRMEN - @m60_lib.M60	21D6
SB_RTC_RST_L	SB_RTC_RST_L - @m60_lib.M60	21D6 26C7
SB_RTC_X1	SB_RTC_X1 - @m60_lib.M60	21D6 26D7
SB_RTC_X2	SB_RTC_X2 - @m60_lib.M60	21D6 26D7
SB_SM_INTRUDER_L	SB_SM_INTRUDER_L - @m60_lib.M60	21D6 26C7
SB_SPKR	SB_SPKR - @m60_lib.M60	23C5
SC_RX_L	SC_RX_L - @m60_lib.M60	58C5 59B6 59C4
SC_TX_L	SC_TX_L - @m60_lib.M60	58C5 59B4 59B6
SDVO_CTRLCLK	SDVO_CTRLCLK - @m60_lib.M60	14B6 19A2
	TP_SDVO_CTRLCLK - @m60_lib.M60	19A1
SDVO_CTRLDATA	SDVO_CTRLDATA - @m60_lib.M60	14B6 19A2
	TP_SDVO_CTRLDATA - @m60_lib.M60	19A1
SMB_ALERT_L	SMB_ALERT_L - @m60_lib.M60	23C5
SMB_BSA_CLK	SMB_BSA_CLK - @m60_lib.M60	58B5 59D1
SMB_BSA_DATA	SMB_BSA_DATA - @m60_lib.M60	58B5 59D1
SMB_BSB_CLK	SMB_BSB_CLK - @m60_lib.M60	58C5 59D1
SMB_BSB_DATA	SMB_BSB_DATA - @m60_lib.M60	58C7 59D1
SMB_LINK_ALERT_L	SMB_LINK_ALERT_L - @m60_lib.M60	23D5
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @m60_lib.M60	58D5 59D5
	TP_SMC_ADAPTER_EN - @m60_lib.M60	59D3
SMC_ANALOG_ID	SMC_ANALOG_ID - @m60_lib.M60	58A7 59C6
	NC_SMC_ANALOG_ID - @m60_lib.M60	59C5
SMC_BATT_CHG_EN	SMC_BATT_CHG_EN - @m60_lib.M60	58D7 59D6
	NC_SMC_BATT_CHG_EN - @m60_lib.M60	59D5
SMC_BATT_ISENSE	SMC_BATT_ISENSE - @m60_lib.M60	58D5 59B6
	UNUSED_SMC_SENSE - @m60_lib.M60	59B5 59B5 59B6
	SMC_FWIRE_ISENSE - @m60_lib.M60	58D5 59B6
	UNUSED_SMC_SENSE - @m60_lib.M60	59B5 59B5 59B6
	SMC_FWIRE_ISENSE - @m60_lib.M60	58D5 59B6
SMC_BATT_ISET	SMC_BATT_ISET - @m60_lib.M60	58B5 59D6
	NC_SMC_BATT_ISET - @m60_lib.M60	59D5
SMC_BATT_TRICKLE_EN_L	SMC_BATT_TRICKLE_EN_L - @m60_lib.M60	58D7 59D6
	NC_SMC_BATT_TRICKLE_EN_L - @m60_lib.M60	59D5
SMC_BATT_VSET	SMC_BATT_VSET - @m60_lib.M60	58B5 59D6
	NC_SMC_BATT_VSET - @m60_lib.M60	59D5
SMC_BC_ACOK	SMC_BC_ACOK - @m60_lib.M60	58C5 59B4
SMC_BS_ALRT_L	SMC_BS_ALRT_L - @m60_lib.M60	58C5 59B4
SMC_CASE_OPEN	SMC_CASE_OPEN - @m60_lib.M60	58C5 59C1
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @m60_lib.M60	58D5 76D2
SMC_CPU_RESET_3_3_L	SMC_CPU_RESET_3_3_L - @m60_lib.M60	58B5 59A7
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @m60_lib.M60	58D5 76B2
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE - @m60_lib.M60	58D5 76D5
SMC_EXCARD_CP	SMC_EXCARD_CP - @m60_lib.M60	58B7 59C4
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @m60_lib.M60	58B7 59C5
	TP_SMC_EXCARD_PWR_EN - @m60_lib.M60	59C3
SMC_EXCARD_PWR_OC_L	SMC_EXCARD_PWR_OC_L - @m60_lib.M60	58B7 59C4
SMC_EXTAL	SMC_EXTAL - @m60_lib.M60	58C3 59B8
SMC_EXTSMI_L	SMC_EXTSMI_L - @m60_lib.M60	23B8 58B7
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @m60_lib.M60	58B7 65D8
	FAN_RPM0 - @m60_lib.M60	65D7
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @m60_lib.M60	58B7 65C8
SMC_FAN_1_CTL	SMC_FAN_1_CTL - @m60_lib.M60	58B7 66C7
	FAN_RPM2 - @m60_lib.M60	66C7
SMC_FAN_1_TACH	SMC_FAN_1_TACH - @m60_lib.M60	58B7 66C8
SMC_FAN_2_CTL	SMC_FAN_2_CTL - @m60_lib.M60	58B7 65B8
	FAN_RPM1 - @m60_lib.M60	65B7
SMC_FAN_2_TACH	SMC_FAN_2_TACH - @m60_lib.M60	58B7 65A8
SMC_FAN_3_CTL	SMC_FAN_3_CTL - @m60_lib.M60	58B7 59C5
	TP_SMC_FAN_3_CTL - @m60_lib.M60	59C3
SMC_FAN_3_TACH	SMC_FAN_3_TACH - @m60_lib.M60	58B7 59C5
	TP_SMC_FAN_3_TACH - @m60_lib.M60	59C3
SMC_FWE	SMC_FWE - @m60_lib.M60	58B5 59B4
SMC_GPU_VSENSE	SMC_GPU_VSENSE - @m60_lib.M60	58D5 59B3
SMC_LID	SMC_LID - @m60_lib.M60	58B5 59C1
SMC_LRESET_L	SMC_LRESET_L - @m60_lib.M60	6B7 58C7
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @m60_lib.M60	5D1 59D8
SMC_MD1	SMC_MD1 - @m60_lib.M60	58C1 60B5
SMC_MEM_ISENSE	SMC_MEM_ISENSE - @m60_lib.M60	58A7 59B6
	NC_SMC_MEM_ISENSE - @m60_lib.M60	59B5
SMC_NB_ISENSE	SMC_NB_ISENSE - @m60_lib.M60	58A7 59B6
	NC_SMC_NB_ISENSE - @m60_lib.M60	59B5
SMC_NMI	SMC_NMI - @m60_lib.M60	58C1 60B4
SMC_ODD_DETECT	SMC_ODD_DETECT - @m60_lib.M60	58B7 59C4
SMC_ONOFF_L	SMC_ONOFF_L - @m60_lib.M60	58C5 59B7 59C4
SMC_PB7	SMC_PB7 - @m60_lib.M60	59C5 59C5
	TP_SMC_PB7 - @m60_lib.M60	59C3 59C3
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE - @m60_lib.M60	58D5 76C6
SMC_PBUS_VSENSE_R	SMC_PBUS_VSENSE_R - @m60_lib.M60	76C8
SMC_PF0	SMC_PF0 - @m60_lib.M60	58B5 59D5
	TP_SMC_PF0 - @m60_lib.M60	59D3
SMC_PF1	SMC_PF1 - @m60_lib.M60	58B5 59D5
	TP_SMC_PF1 - @m60_lib.M60	59D3
SMC_PM_G2_EN	SMC_PM_G2_EN - @m60_lib.M60	58D5 59D5
	TP_PM_G2_EN - @m60_lib.M60	59D3
SMC_PROCHOT	SMC_PROCHOT - @m60_lib.M60	58B5 59C7
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @m60_lib.M60	58D5 59A7
SMC_RCIN_L	SMC_RCIN_L - @m60_lib.M60	21C3 58C7
SMC_REF_GATE1	SMC_REF_GATE1 - @m60_lib.M60	59A5
SMC_REF_GATE2	SMC_REF_GATE2 - @m60_lib.M60	59A4
SMC_REF_IN	SMC_REF_IN - @m60_lib.M60	59A4
SMC_RSTGATE_L	SMC_RSTGATE_L - @m60_lib.M60	58D7
SMC_RST_L	SMC_RST_L - @m60_lib.M60	58C3 59D7 60B4
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @m60_lib.M60	23C8 58B7
SMC_RX_L	SMC_RX_L - @m60_lib.M60	5D1 58C7 59B4 59B5 60B4
SMC_SB_NMI	SMC_SB_NMI - @m60_lib.M60	23C3 58D7
SMC_SMB_0_CLK	SMC_SMB_0_CLK - @m60_lib.M60	58C7 59D1
	TP_SMC_SMB_0_CLK - @m60_lib.M60	59D1
SMC_SMB_0_DATA	SMC_SMB_0_DATA - @m60_lib.M60	58C5 59D1
	TP_SMC_SMB_0_DATA - @m60_lib.M60	59D1
SMC_SYS_ISET	SMC_SYS_ISET - @m60_lib.M60	58B5 59D6
	NC_SMC_SYS_ISET - @m60_lib.M60	59D5
SMC_SYS_KBDLED	SMC_SYS_KBDLED - @m60_lib.M60	58C7 59D5
	TP_SMC_SYS_KBDLED - @m60_lib.M60	59D3
SMC_SYS_LED	SMC_SYS_LED - @m60_lib.M60	58C7 59A3
SMC_SYS_LED_16B	SMC_SYS_LED_16B - @m60_lib.M60	58C7 59A3
SMC_SYS_VSET	SMC_SYS_VSET - @m60_lib.M60	58B5 59D6
	NC_SMC_SYS_VSET - @m60_lib.M60	59D5
SMC_TCK	SMC_TCK - @m60_lib.M60	5D1 58C5 59B4 60B4
SMC_TDI	SMC_TDI - @m60_lib.M60	5D1 58B5 59B4 60B4
SMC_TDO	SMC_TDO - @m60_lib.M60	5D1 58B5 59B4 60B5
SMC_THRMTRIP	SMC_THRMTRIP - @m60_lib.M60	58B5 59C7
SMC_TMS	SMC_TMS - @m60_lib.M60	5D1 58B5 59B4 60B5
SMC_TPM_GPIO	SMC_TPM_GPIO - @m60_lib.M60	58D5 59B6
SMC_TPM_PP	SMC_TPM_PP - @m60_lib.M60	58C7 59A6
SMC_TPM_RESET_L	SMC_TPM_RESET_L - @m60_lib.M60	58B7 59C6 67B7
SMC_TRST_L	SMC_TRST_L - @m60_lib.M60	5D1 58C1 60B5
SMC_TX_L	SMC_TX_L - @m60_lib.M60	5D1 58C7 59B4 59B5 60B5
SMC_VCL	SMC_VCL - @m60_lib.M60	58D3
SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @m60_lib.M60	23C1 58D5
SMC_XDP_TCK	SMC_XDP_TCK - @m60_lib.M60	58C7
SMC_XDP_TCK_3_3	SMC_XDP_TCK_3_3 - @m60_lib.M60	58B5 59A5
SMC_XDP_TDO_3_3_L	SMC_XDP_TDO_3_3_L - @m60_lib.M60	58B7 59A5
SMC_XDP_TMS_L	SMC_XDP_TMS_L - @m60_lib.M60	58C7
SMC_XDP_TRST_L	SMC_XDP_TRST_L - @m60_lib.M60	58C7
SMC_XTAL	SMC_XTAL - @m60_lib.M60	58C3 59B8
SMLINK<0>	SMLINK<0> - @m60_lib.M60	23D5
SMLINK<1>	SMLINK<1> - @m60_lib.M60	23D5
SMS_INT_L	SMS_INT_L - @m60_lib.M60	23C3 26C2 58B5
SMS_ONOFF_L	SMS_ONOFF_L - @m60_lib.M60	58A5 59B4
SMS_X_AXIS	SMS_X_AXIS - @m60_lib.M60	58B7 59B6
	NC_SMS_X_AXIS - @m60_lib.M60	59B5
SMS_Y_AXIS	SMS_Y_AXIS - @m60_lib.M60	58B7 59B6
	NC_SMS_Y_AXIS - @m60_lib.M60	59B5
SMS_Z_AXIS	SMS_Z_AXIS - @m60_lib.M60	58A7 59B6
	NC_SMS_Z_AXIS - @m60_lib.M60	59B5
SPARE_SRC3_N	SPARE_SRC3_N - @m60_lib.M60	34D2
SPARE_SRC3_P	SPARE_SRC3_P - @m60_lib.M60	34D2
SPARE_SRC7_N	SPARE_SRC7_N - @m60_lib.M60	34D2
SPARE_SRC7_P	SPARE_SRC7_P - @m60_lib.M60	34D2
SPI_ARB	SPI_ARB - @m60_lib.M60	22C6 58D5
SPI_CE_L	SPI_CE_L - @m60_lib.M60	22C6 58B5 63C7
SPI_HOLD_L	SPI_HOLD_L - @m60_lib.M60	63C4
SPI_SCLK	SPI_SCLK - @m60_lib.M60	22C6 58D5 63C7
SPI_SCLK_R	SPI_SCLK_R - @m60_lib.M60	63C4
SPI_SI	SPI_SI - @m60_lib.M60	22C6 58D5 63C1
SPI_SI_R	SPI_SI_R - @m60_lib.M60	63C3
SPI_SO	SPI_SO - @m60_lib.M60	22C6 58D5 63C1
SPI_SO_R	SPI_SO_R - @m60_lib.M60	63C3
SPI_WP_L	SPI_WP_L - @m60_lib.M60	63C4
SPKRAMP_MUTE	SPKRAMP_MUTE - @m60_lib.M60	72B5
SPKRAMP_SS	SPKRAMP_SS - @m60_lib.M60	72B4
START_G_2V5_S0	START_G_2V5_S0 - @m60_lib.M60	83B8
START_G_3V3_S0	START_G_3V3_S0 - @m60_lib.M60	83C8
START_G_4V5_S0	START_G_4V5_S0 - @m60_lib.M60	83D6
START_G_5V_S0	START_G_5V_S0 - @m60_lib.M60	83B5

8 7 6 5 4 3 2 1

START_G_12V_S0	START_G_12V_S0 - @m60_lib.M60	83A8
SUS_CLK_SB	SUS_CLK_SB - @m60_lib.M60	23C3 59B5
	SMC_SUS_CLK - @m60_lib.M60	58C5 59B6
SV_SET_UP	SV_SET_UP - @m60_lib.M60	23B6 23C3 60B3
SW_RST_BTN_L	SW_RST_BTN_L - @m60_lib.M60	5D1 26C6
SW_RST_DEBNC	SW_RST_DEBNC - @m60_lib.M60	26C4
SYS_LED_BRT_D	SYS_LED_BRT_D - @m60_lib.M60	59B2
SYS_LED_C	SYS_LED_C - @m60_lib.M60	59B1
SYS_LED_CTL_B	SYS_LED_CTL_B - @m60_lib.M60	59B2
SYS_LED_CTL_C	SYS_LED_CTL_C - @m60_lib.M60	59B1
SYS_LED_CTL_D	SYS_LED_CTL_D - @m60_lib.M60	59B1
SYS_ONEWIRE	SYS_ONEWIRE - @m60_lib.M60	58B7 59B4
SYS_POWERFAIL_L	SYS_POWERFAIL_L - @m60_lib.M60	6D8 57B7 76D2 82B7
THERM_DX_N	THERM_DX_N - @m60_lib.M60	10B5 10C5
THERM_DX_P	THERM_DX_P - @m60_lib.M60	10B5 10C5
THRM_ALERT_L	THRM_ALERT_L - @m60_lib.M60	10D3
THRM_THM	THRM_THM - @m60_lib.M60	10C4
TMDS_CK_TERM	TMDS_CK_TERM - @m60_lib.M60	97C8
TMDS_CLK_N	TMDS_CLK_N - @m60_lib.M60	93C3 97C8
TMDS_CLK_P	TMDS_CLK_P - @m60_lib.M60	93C3 97C8
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @m60_lib.M60	97C4 97C7
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @m60_lib.M60	97C4 97C7
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @m60_lib.M60	97C4 97D7
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @m60_lib.M60	97C4 97D7
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @m60_lib.M60	97C7 97D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @m60_lib.M60	97C4 97D7
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @m60_lib.M60	97C4 97D7
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @m60_lib.M60	97C7 97D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @m60_lib.M60	93C3 97D8
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @m60_lib.M60	93C3 97D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @m60_lib.M60	93C3 97C8
TMDS_DATA_N<3>	TMDS_DATA_N<3> - @m60_lib.M60	93C3 95D6
TMDS_DATA_N<4>	TMDS_DATA_N<4> - @m60_lib.M60	93C3 95D6
TMDS_DATA_N<5>	TMDS_DATA_N<5> - @m60_lib.M60	93C3 95D6
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @m60_lib.M60	93C3 97D8
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @m60_lib.M60	93C3 97C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @m60_lib.M60	93C3 97C8
TMDS_DATA_P<3>	TMDS_DATA_P<3> - @m60_lib.M60	93C3 95D6
TMDS_DATA_P<4>	TMDS_DATA_P<4> - @m60_lib.M60	93C3 95D6
TMDS_DATA_P<5>	TMDS_DATA_P<5> - @m60_lib.M60	93C3 95D6
TO_GATE_12V_S0_R	TO_GATE_12V_S0_R - @m60_lib.M60	83A7
TPM_BADD	TPM_BADD - @m60_lib.M60	67C4
TPM_GPIO1	TPM_GPIO1 - @m60_lib.M60	59B5 67C6
TPM_GPIO2	TPM_GPIO2 - @m60_lib.M60	59B5 67C6
TPM_LRESET_L	TPM_LRESET_L - @m60_lib.M60	6B7 67B7
TPM_PP	TPM_PP - @m60_lib.M60	59A5 67C6
TPM_RST_L	TPM_RST_L - @m60_lib.M60	67B6
TPM_XTALI	TPM_XTALI - @m60_lib.M60	59B7 67C6
TPM_XTALO	TPM_XTALO - @m60_lib.M60	59B7 67C6
TP_ATI_ROMCS_L	TP_ATI_ROMCS_L - @m60_lib.M60	43A3
TP_AUD_BI_PORT_D_L	TP_AUD_BI_PORT_D_L - @m60_lib.M60	68C7
TP_AUD_BI_PORT_D_R	TP_AUD_BI_PORT_D_R - @m60_lib.M60	68C7
TP_AUD_BI_PORT_E_L	TP_AUD_BI_PORT_E_L - @m60_lib.M60	68C1
TP_AUD_BI_PORT_E_R	TP_AUD_BI_PORT_E_R - @m60_lib.M60	68C1
TP_AZ_DOCK_EN_L	TP_AZ_DOCK_EN_L - @m60_lib.M60	23C5
TP_AZ_DOCK_RST_L	TP_AZ_DOCK_RST_L - @m60_lib.M60	23C5
TP_CLK14P3M_SPARE	TP_CLK14P3M_SPARE - @m60_lib.M60	34C4
TP_CPU_A32_L	TP_CPU_A32_L - @m60_lib.M60	7C7
TP_CPU_A33_L	TP_CPU_A33_L - @m60_lib.M60	7B7
TP_CPU_A34_L	TP_CPU_A34_L - @m60_lib.M60	7B7
TP_CPU_A35_L	TP_CPU_A35_L - @m60_lib.M60	7B7
TP_CPU_A36_L	TP_CPU_A36_L - @m60_lib.M60	7B7
TP_CPU_A37_L	TP_CPU_A37_L - @m60_lib.M60	7B7
TP_CPU_A38_L	TP_CPU_A38_L - @m60_lib.M60	7B7
TP_CPU_A39_L	TP_CPU_A39_L - @m60_lib.M60	7B7
TP_CPU_APM0_L	TP_CPU_APM0_L - @m60_lib.M60	7B7
TP_CPU_APM1_L	TP_CPU_APM1_L - @m60_lib.M60	7B7
TP_CPU_CPUSLP_L	TP_CPU_CPUSLP_L - @m60_lib.M60	21C4
TP_CPU_EXTBREF	TP_CPU_EXTBREF - @m60_lib.M60	7B6
TP_CPU_HFPLL	TP_CPU_HFPLL - @m60_lib.M60	7B7
TP_CPU_SPARE0	TP_CPU_SPARE0 - @m60_lib.M60	7B6
TP_CPU_SPARE1	TP_CPU_SPARE1 - @m60_lib.M60	7B6
TP_CPU_SPARE2	TP_CPU_SPARE2 - @m60_lib.M60	7B6
TP_CPU_SPARE3	TP_CPU_SPARE3 - @m60_lib.M60	7B6
TP_CPU_SPARE4	TP_CPU_SPARE4 - @m60_lib.M60	7B6
TP_CPU_SPARE5	TP_CPU_SPARE5 - @m60_lib.M60	7B6
TP_CPU_SPARE6	TP_CPU_SPARE6 - @m60_lib.M60	7B6
TP_CPU_SPARE7	TP_CPU_SPARE7 - @m60_lib.M60	7B6
TP_FB_A_MA12	TP_FB_A_MA12 - @m60_lib.M60	87D5
TP_FB_A_ODT<0>	TP_FB_A_ODT<0> - @m60_lib.M60	87B5
TP_FB_A_ODT<1>	TP_FB_A_ODT<1> - @m60_lib.M60	87B5
TP_FB_B_MA12	TP_FB_B_MA12 - @m60_lib.M60	87D1
TP_FB_B_ODT<0>	TP_FB_B_ODT<0> - @m60_lib.M60	87B1
TP_FB_B_ODT<1>	TP_FB_B_ODT<1> - @m60_lib.M60	87B1
TP_FW_CNA	TP_FW_CNA - @m60_lib.M60	44B3
TP_FW_LKON	TP_FW_LKON - @m60_lib.M60	44B3
TP_FW_LPS	TP_FW_LPS - @m60_lib.M60	44B3
TP_FW_MPCIACT_L	TP_FW_MPCIACT_L - @m60_lib.M60	44B3
TP_FW_NANDTREE	TP_FW_NANDTREE - @m60_lib.M60	44B3
TP_FW_ROM_AD	TP_FW_ROM_AD - @m60_lib.M60	44B3
TP_FW_VAUX_PRES	TP_FW_VAUX_PRES - @m60_lib.M60	44B3
TP_LVDS_VBG	TP_LVDS_VBG - @m60_lib.M60	13D5
TP_MEM_A_A<14>	TP_MEM_A_A<14> - @m60_lib.M60	28C3
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @m60_lib.M60	28C3
TP_MEM_B_A<14>	TP_MEM_B_A<14> - @m60_lib.M60	5B4 29C3
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @m60_lib.M60	5B4 29C3
TP_NB_TESTIN_L	TP_NB_TESTIN_L - @m60_lib.M60	14D6
TP_NB_XOR_FSB2_H7	TP_NB_XOR_FSB2_H7 - @m60_lib.M60	14D6
TP_NB_XOR_LVDS_A34	TP_NB_XOR_LVDS_A34 - @m60_lib.M60	14C6
TP_NB_XOR_LVDS_A35	TP_NB_XOR_LVDS_A35 - @m60_lib.M60	14C6
TP_NB_XOR_LVDS_D27	TP_NB_XOR_LVDS_D27 - @m60_lib.M60	14C6
TP_NB_XOR_LVDS_D28	TP_NB_XOR_LVDS_D28 - @m60_lib.M60	14C6
TP_PCI_CLK_SPARE	TP_PCI_CLK_SPARE - @m60_lib.M60	5B4 34C4
TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m60_lib.M60	22B6
TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m60_lib.M60	22B6
TP_PCI_GNT3_L	TP_PCI_GNT3_L - @m60_lib.M60	22B6
TP_PCI_GNT4_L	TP_PCI_GNT4_L - @m60_lib.M60	22B6
TP_PCI_PME_L	TP_PCI_PME_L - @m60_lib.M60	22A6
TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m60_lib.M60	21C6
TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m60_lib.M60	21C6
TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m60_lib.M60	21D4
TP_SB_GPIO6	TP_SB_GPIO6 - @m60_lib.M60	23C5
TP_SB_GPIO23	TP_SB_GPIO23 - @m60_lib.M60	21D5
TP_SB_GPIO25_DO_NOT_USE	TP_SB_GPIO25_DO_NOT_USE - @m60_lib.M60	23C3
TP_SB_GPIO38	TP_SB_GPIO38 - @m60_lib.M60	23C3
TP_SB_RSVD9	TP_SB_RSVD9 - @m60_lib.M60	22A6
TP_SB_SATALED_L	TP_SB_SATALED_L - @m60_lib.M60	21C6
TP_SB_XOR_AD5	TP_SB_XOR_AD5 - @m60_lib.M60	22A7
TP_SB_XOR_AD9	TP_SB_XOR_AD9 - @m60_lib.M60	22A7
TP_SB_XOR_AE5	TP_SB_XOR_AE5 - @m60_lib.M60	22A7
TP_SB_XOR_AE9	TP_SB_XOR_AE9 - @m60_lib.M60	22A6
TP_SB_XOR_AG4	TP_SB_XOR_AG4 - @m60_lib.M60	22A7
TP_SB_XOR_AG8	TP_SB_XOR_AG8 - @m60_lib.M60	22A6
TP_SB_XOR_AH4	TP_SB_XOR_AH4 - @m60_lib.M60	22A7
TP_SB_XOR_AH8	TP_SB_XOR_AH8 - @m60_lib.M60	22A6
TP_SB_XOR_T5	TP_SB_XOR_T5 - @m60_lib.M60	21C6
TP_SB_XOR_U3	TP_SB_XOR_U3 - @m60_lib.M60	21C6
TP_SB_XOR_U5	TP_SB_XOR_U5 - @m60_lib.M60	21C6
TP_SB_XOR_U7	TP_SB_XOR_U7 - @m60_lib.M60	21C6
TP_SB_XOR_V3	TP_SB_XOR_V3 - @m60_lib.M60	21C6
TP_SB_XOR_V4	TP_SB_XOR_V4 - @m60_lib.M60	21C6
TP_SB_XOR_V6	TP_SB_XOR_V6 - @m60_lib.M60	21C6
TP_SB_XOR_V7	TP_SB_XOR_V7 - @m60_lib.M60	21C6
TP_SB_XOR_W1	TP_SB_XOR_W1 - @m60_lib.M60	21C6
TP_SB_XOR_W3	TP_SB_XOR_W3 - @m60_lib.M60	21C6
TP_SB_XOR_Y1	TP_SB_XOR_Y1 - @m60_lib.M60	21C6
TP_SB_XOR_Y2	TP_SB_XOR_Y2 - @m60_lib.M60	21C6
TP_U8400_AG14	TP_U8400_AG14 - @m60_lib.M60	91A5
TP_U8900_J2	TP_U8900_J2 - @m60_lib.M60	89A7
TP_U8900_J3	TP_U8900_J3 - @m60_lib.M60	89A7
TP_U8950_J2	TP_U8950_J2 - @m60_lib.M60	89A4
TP_U8950_J3	TP_U8950_J3 - @m60_lib.M60	89A4
TP_U9000_J2	TP_U9000_J2 - @m60_lib.M60	90A7
TP_U9000_J3	TP_U9000_J3 - @m60_lib.M60	90A7
TP_U9050_J2	TP_U9050_J2 - @m60_lib.M60	90A4
TP_U9050_J3	TP_U9050_J3 - @m60_lib.M60	90A4
TSENSE_GPU_DXP	TSENSE_GPU_DXP - @m60_lib.M60	61C5
TSENSE_NB_DXP	TSENSE_NB_DXP - @m60_lib.M60	61B5
TSENSE_NB_GPU_DXN	TSENSE_NB_GPU_DXN - @m60_lib.M60	61B5
TV_DACA_OUT	TV_DACA_OUT - @m60_lib.M60	13C5 19B1
	TV_DACB_OUT - @m60_lib.M60	13C5 19B1
	TV_DACC_OUT - @m60_lib.M60	13C5 19B1
	TV_IRTNA - @m60_lib.M60	13C5 19B1
	TV_IRTNB - @m60_lib.M60	13C5 19B1
	TV_IRTNC - @m60_lib.M60	13C5 19B1
	TV_IREF - @m60_lib.M60	13C5 19B1
	PP3V3_S0_NB_VCCA_TVBG - @m60_lib.M60	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACC - @m60_lib.M60	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACB - @m60_lib.M60	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACA - @m60_lib.M60	17C6 19B1
	PP1V5_S0_NB_VCCD_TVDAC - @m60_lib.M60	17C6 19B1
	PP1V5_S0_NB_VCCD_QTVDAC - @m60_lib.M60	17B6 19B1
	=PP1V5_S0_AIRPORT - @m60_lib.M60	6C4 53D3
	PP1V5_S0 - @m60_lib.M60	6C6 80C1
	=PP1V5_S0_SB - @m60_lib.M60	6C4 25A8 25C8
	=PP1V5_S0_SB_VCC1_5_A - @m60_lib.M60	6C4 24A3 25C1
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m60_lib.M60	6C4 24A3 25B1
	=PP1V5_S0_SB_VCCUSBPLL - @m60_lib.M60	6C4 24A5 25B6
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m60_lib.M60	6C4 24A5 25C6
	=PP1V5_S0_SB_VCCSATAPLL - @m60_lib.M60	6C4 24B5 25D6
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m60_lib.M60	6C4 24B5 25D6
	=PP1V5_S0_NB_3GPLL - @m60_lib.M60	6C4 19A6 19A6
	=PP1V5_S0_NB_PLL - @m60_lib.M60	6C4 19C8 19D7
	=PP1V5_S0_NB_VCCAUX - @m60_lib.M60	6C4 6C4 16D1 17B6 19A7 19D7
	=PP1V5_S0_NB_VCCD_HMPLL - @m60_lib.M60	6C4 17C6 19D7
	=PP1V5_S0_NB_PCIE - @m60_lib.M60	6C4 13D2 19D7
	=PP1V5_S0_CPU - @m60_lib.M60	6C4 8B6 8C5
	TV_IRTNC - @m60_lib.M60	13C5 19B1
	TV_IRTNB - @m60_lib.M60	13C5 19B1
	TV_IRTNA - @m60_lib.M60	13C5 19B1
	TV_IREF - @m60_lib.M60	13C5 19B1
	TV_DACC_OUT - @m60_lib.M60	13C5 19B1
	TV_DACB_OUT - @m60_lib.M60	13C5 19B1
	PP3V3_S0_NB_VCCA_TVDACC - @m60_lib.M60	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACB - @m60_lib.M60	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACA - @m60_lib.M60	17C6 19B1
	PP3V3_S0_NB_VCCA_TVBG - @m60_lib.M60	17C6 19B1
	PP1V5_S0_NB_VCCD_TVDAC - @m60_lib.M60	17C6 19B1
	PP1V5_S0_NB_VCCD_QTVDAC - @m60_lib.M60	17B6 19B1
	PP1V5_S0 - @m60_lib.M60	6C6 80C1
	=PP1V5_S0_SB_VCCUSBPLL - @m60_lib.M60	6C4 24A5 25B6
	=PP1V5_S0_SB_VCCSATAPLL - @m60_lib.M60	6C4 24B5 25D6
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m60_lib.M60	6C4 24A3 25B1
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m60_lib.M60	6C4 24A5 25C6
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m60_lib.M60	6C4 24B5 25D6
	=PP1V5_S0_SB_VCC1_5_A - @m60_lib.M60	6C4 24A3 25C1
	=PP1V5_S0_SB - @m60_lib.M60	6C4 25A8 25C8
	=PP1V5_S0_NB_VCCD_HMPLL - @m60_lib.M60	6C4 17C6 19D7
	=PP1V5_S0_NB_VCCAUX - @m60_lib.M60	6C4 6C4 16D1 17B6 19A7 19D7
	=PP1V5_S0_NB_TVDAC - @m60_lib.M60	6C4 19B2 19D7
	=PP1V5_S0_NB_PLL - @m60_lib.M60	6C4 19C8 19D7
	=PP1V5_S0_NB_PCIE - @m60_lib.M60	6C4 13D2 19D7
	=PP1V5_S0_NB_3GPLL - @m60_lib.M60	6C4 19A6 19A6
	=PP1V5_S0_NB - @m60_lib.M60	6C4 19B2 19D7
	=PP1V5_S0_CPU - @m60_lib.M60	6C4 8B6 8C5
	=PP1V5_S0_AIRPORT - @m60_lib.M60	6C4 53D3
U600_3	U600_3 - @m60_lib.M60	6C7
U600_6	U600_6 - @m60_lib.M60	6B7
U600_8	U600_8 - @m60_lib.M60	6B7
U600_11	U600_11 - @m60_lib.M60	6A7
U2698_4	U2698_4 - @m60_lib.M60	26C4
U3100_VDDQ	U3100_VDDQ - @m60_lib.M60	31C5
U6100_VCC	U6100_VCC - @m60_lib.M60	61C4
U7400_CEXT	U7400_CEXT - @m60_lib.M60	74C4
U8595_1	U8595_1 - @m60_lib.M60	85D2
U9700_8	U9700_8 - @m60_lib.M60	6A6
USB_A_N	USB_A_N - @m60_lib.M60	22C2 47D7
USB_A_OC_L	USB_A_OC_L - @m60_lib.M60	22C4 22D8 47B8
USB_A_P	USB_A_P - @m60_lib.M60	22C2 47C7
USB_B_N	USB_B_N - @m60_lib.M60	22C2 53B2
USB_B_OC_L	USB_B_OC_L - @m60_lib.M60	22C4 22D8
USB_B_P	USB_B_P - @m60_lib.M60	22C2 53B2
USB_CAMERA_N	USB_CAMERA_N - @m60_lib.M60	47B2
USB_CAMERA_P	USB_CAMERA_P - @m60_lib.M60	47B2
USB_C_N	USB_C_N - @m60_lib.M60	22C2 47B7
USB_C_OC_L	USB_C_OC_L - @m60_lib.M60	22C4 22D8 47B8
USB_C_P	USB_C_P - @m60_lib.M60	22C2 47B7
USB_D_N	USB_D_N - @m60_lib.M60	22C2 47B3
USB_D_OC_L	USB_D_OC_L - @m60_lib.M60	22C4 22D8
USB_D_P	USB_D_P - @m60_lib.M60	22C2 47B3
USB_E_N	USB_E_N - @m60_lib.M60	22C2 47A7
USB_E_OC_L	USB_E_OC_L - @m60_lib.M60	22C4 22D8 47B8
USB_E_P	USB_E_P - @m60_lib.M60	22C2 47A7
USB_F_N	USB_F_N - @m60_lib.M60	22C2
USB_F_P	USB_F_P - @m60_lib.M60	22C2
USB_G_N	USB_G_N - @m60_lib.M60	22C2 47A3
	USB_BT_N - @m60_lib.M60	47A3
USB_G_P	USB_G_P - @m60_lib.M60	22C2 47A3
	USB_BT_P - @m60_lib.M60	47A3
USB_H_N	USB_H_N - @m60_lib.M60	22C2 47C3
USB_H_P	USB_H_P - @m60_lib.M60	22C2 47C3
USB_IR_N	USB_IR_N - @m60_lib.M60	47C2
USB_IR_P	USB_IR_P - @m60_lib.M60	47C2
USB_PORT0_N	USB_PORT0_N - @m60_lib.M60	47D5
USB_PORT0_P	USB_PORT0_P - @m60_lib.M60	47C5
USB_PORT1_N	USB_PORT1_N - @m60_lib.M60	47B5
USB_PORT1_P	USB_PORT1_P - @m60_lib.M60	47B5
USB_PORT2_N	USB_PORT2_N - @m60_lib.M60	47A5
USB_PORT2_P	USB_PORT2_P - @m60_lib.M60	47A5
USB_RBIAS_PN	USB_RBIAS_PN - @m60_lib.M60	22C2
VGA_B	VGA_B - @m60_lib.M60	97B6 97C5
VGA_G	VGA_G - @m60_lib.M60	97A6 97C5
VGA_HSYNC	VGA_HSYNC - @m60_lib.M60	97A3 97C5
VGA_R	VGA_R - @m60_lib.M60	97A6 97C5
VGA_VSYNC	VGA_VSYNC - @m60_lib.M60	97A3 97C5
VMAIN_AVLBL	VMAIN_AVLBL - @m60_lib.M60	41C7
VR_PWRGD_CK410	VR_PWRGD_CK410 - @m60_lib.M60	23C5 26A8
VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m60_lib.M60	5C7 14B6 26D5 75C6
XDP_BPM_L<0>	XDP_BPM_L<0> - @m60_lib.M60	7C6 11B3
XDP_BPM_L<1>	XDP_BPM_L<1> - @m60_lib.M60	7C6 11B3
XDP_BPM_L<2>	XDP_BPM_L<2> - @m60_lib.M60	7C6 11B3
XDP_BPM_L<3>	XDP_BPM_L<3> - @m60_lib.M60	7C6 11B3
XDP_BPM_L<4>	XDP_BPM_L<4> - @m60_lib.M60	7C6 11B3
XDP_BPM_L<5>	XDP_BPM_L<5> - @m60_lib.M60	7C6 11B3
XDP_DBRESET_L	XDP_DBRESET_L - @m60_lib.M60	7C6 11B4 26B5
XDP_TCK	XDP_TCK - @m60_lib.M60	5D1 7A8 7C6 11B3 11B3
XDP_TDI	XDP_TDI - @m60_lib.M60	5D1 7B8 7C6 11B3
XDP_TDO	XDP_TDO - @m60_lib.M60	5D1 7C6 11B5
XDP_TMS	XDP_TMS - @m60_lib.M60	5D1 7B8 7C6 11B3
XDP_TRST_L	XDP_TRST_L - @m60_lib.M60	5D1 7C6 11B3
ZH701P1	ZH701P1 - @m60_lib.M60	6A3
ZH702P1	ZH702P1 - @m60_lib.M60	6A3
ZH703P1	ZH703P1 - @m60_lib.M60	6A3

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C85A0	CAP_402	m60[85D1]
C600	CAP_402	m60[6C7]
C601	CAP_402	m60[6A3]
C602	CAP_402	m60[6A3]
C603	CAP_402	m60[6A3]
C620	CAP_603	m60[6D6]
C621	CAP_603	m60[6D6]
C622	CAP_805	m60[6D7]
C623	CAP_805-2	m60[6D7]
C624	CAP_1210	m60[6D8]
C625	CAP_P_6.3X5.5-SM	m60[6D8]
C0800	CAP_402	m60[8B5]
C0801	CAP_603	m60[8B5]
C900	CAP_805	m60[9B6]
C901	CAP_805	m60[9B6]
C902	CAP_805	m60[9A6]
C903	CAP_805	m60[9A6]
C904	CAP_805	m60[9A6]
C905	CAP_805	m60[9A6]
C906	CAP_805	m60[9A6]
C907	CAP_805	m60[9B5]
C908	CAP_805	m60[9B7]
C909	CAP_805	m60[9B5]
C910	CAP_805	m60[9B7]
C911	CAP_805	m60[9B7]
C912	CAP_805	m60[9A7]
C913	CAP_805	m60[9A7]
C914	CAP_805	m60[9A7]
C915	CAP_805	m60[9A7]
C916	CAP_805	m60[9A7]
C917	CAP_805	m60[9A7]
C918	CAP_805	m60[9A7]
C919	CAP_805	m60[9A7]
C920	CAP_805	m60[9A5]
C921	CAP_805	m60[9A7]
C922	CAP_805	m60[9A7]
C923	CAP_805	m60[9B7]
C924	CAP_805	m60[9A7]
C925	CAP_805	m60[9A7]
C926	CAP_402	m60[9B7]
C928	CAP_805	m60[9B6]
C929	CAP_805	m60[9B5]
C930	CAP_805	m60[9A6]
C931	CAP_805	m60[9A5]
C932	CAP_805	m60[9A6]
C934	CAP_402	m60[9B7]
C935	CAP_402	m60[9B7]
C936	CAP_402	m60[9B7]
C937	CAP_402	m60[9B6]
C938	CAP_402	m60[9B6]
C939	CAP_805	m60[9A5]
C940	CAP_P_CASE-C1	m60[9C7]
C941	CAP_P_3P_D2T	m60[9A7]
C942	CAP_P_3P_D2T	m60[9A7]
C943	CAP_P_3P_D2T	m60[9A7]
C944	CAP_P_3P_D2T	m60[9A7]
C945	CAP_P_3P_D2T	m60[9A6]
C946	CAP_P_3P_D2T	m60[9A6]
C950	CAP_402	m60[9D4]
C951	CAP_402	m60[9D3]
C952	CAP_402	m60[9D3]
C953	CAP_402	m60[9D2]
C1000	CAP_402	m60[10C6]
C1001	CAP_402	m60[10D4]
C1100	CAP_402	m60[11A3]
C1211	CAP_402	m60[12C3]
C1226	CAP_402	m60[12B6]
C1236	CAP_402	m60[12A6]
C1610	CAP_402	m60[16B5]
C1611	CAP_402	m60[16B4]
C1612	CAP_402	m60[16B4]
C1613	CAP_402	m60[16B8]
C1614	CAP_402	m60[16B8]
C1615	CAP_402	m60[16B6]
C1620	CAP_805-1	m60[16B5]
C1621	CAP_805-1	m60[16B5]
C1711	CAP_402	m60[17A3]
C1712	CAP_402	m60[17A3]
C1713	CAP_402	m60[17B3]
C1900	CAP_P_CASE-C1	m60[19B5]
C1901	CAP_P_CASE-C1	m60[19B5]
C1902	CAP_805-1	m60[19B5]
C1903	CAP_805-1	m60[19B4]
C1904	CAP_402	m60[19B4]
C1905	CAP_402	m60[19B4]
C1906	CAP_402	m60[19B3]
C1907	CAP_402	m60[19B3]
C1914	CAP_805-1	m60[19A8]
C1915	CAP_402	m60[19A7]
C1916	CAP_402	m60[19A8]
C1918	CAP_402	m60[19A7]
C1934	CAP_805	m60[19C7]
C1935	CAP_402	m60[19C7]
C1936	CAP_805	m60[19C7]
C1937	CAP_402	m60[19C7]
C1965	CAP_603	m60[19B8]
C1966	CAP_603	m60[19B7]
C1967	CAP_402	m60[19B7]
C1968	CAP_P_CASE-C1	m60[19B7]
C1970	CAP_P_SMB2	m60[19A5]
C1971	CAP_805-1	m60[19A4]
C1972	CAP_805-1	m60[19A4]
C1975	CAP_805-1	m60[19A4]
C1976	CAP_402	m60[19A4]
C1981	CAP_603	m60[19B6]
C1982	CAP_603	m60[19B8]
C2500	CAP_P_SMB2	m60[25B8]
C2501	CAP_402	m60[25A6]
C2502	CAP_402	m60[25D4]
C2503	CAP_402	m60[25D8]
C2504	CAP_402	m60[25C8]
C2505	CAP_402	m60[25B7]
C2506	CAP_402	m60[25B7]
C2507	CAP_402	m60[25B7]
C2508	CAP_805-1	m60[25A6]
C2509	CAP_402	m60[25B8]
C2510	CAP_402	m60[25C1]
C2511	CAP_402	m60[25D6]
C2512	CAP_402	m60[25B1]
C2513	CAP_402	m60[25C6]
C2514	CAP_402	m60[25C6]
C2515	CAP_402	m60[25B6]
C2516	CAP_P_CASE-C2	m60[25D3]
C2517	CAP_402	m60[25D6]
C2518	CAP_402	m60[25D4]
C2519	CAP_402	m60[25D3]
C2520	CAP_402	m60[25B6]
C2521	CAP_402	m60[25C3]
C2522	CAP_402	m60[25B3]
C2523	CAP_402	m60[25B4]
C2524	CAP_603	m60[25B3]
C2525	CAP_402	m60[25B3]
C2526	CAP_402	m60[25A4]
C2527	CAP_402	m60[25A3]
C2528	CAP_402	m60[25A3]
C2529	CAP_402	m60[25A3]
C2530	CAP_402	m60[25A3]
C2531	CAP_402	m60[25D1]
C2532	CAP_402	m60[25C1]
C2533	CAP_402	m60[25C1]
C2534	CAP_402	m60[25D1]
C2605	CAP_402	m60[26C7]
C2607	CAP_402	m60[26D5]
C2608	CAP_402	m60[26D8]
C2609	CAP_402	m60[26D8]
C2610	CAP_402	m60[26C7]
C2611	CAP_402	m60[26B7]
C2698	CAP_402	m60[26C4]
C2699	CAP_402	m60[26C5]
C2800	CAP_402	m60[28D6]
C2801	CAP_603	m60[28B2]
C2802	CAP_603	m60[28B2]
C2803	CAP_603	m60[28B1]
C2804	CAP_603	m60[28B1]
C2810	CAP_402	m60[28B2]
C2811	CAP_402	m60[28B2]
C2812	CAP_402	m60[28B1]
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C2814	CAP_402	m60[28B2]
C2815	CAP_402	m60[28B2]
C2816	CAP_402	m60[28B1]
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C2818	CAP_402	m60[28B2]
C2819	CAP_402	m60[28B2]
C2820	CAP_402	m60[28B1]
C2821	CAP_402	m60[28B1]
C2850	CAP_603	m60[28D6]
C2851	CAP_603	m60[28A6]
C2852	CAP_402	m60[28A6]
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C2911	CAP_402	m60[29B1]
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C2922	CAP_402	m60[29B1]
C2923	CAP_402	m60[29B1]
C2950	CAP_603	m60[29D6]
C2951	CAP_603	m60[29A7]
C2952	CAP_402	m60[29A6]
C3004	CAP_402	m60[30B4]
C3005	CAP_402	m60[30D4]
C3006	CAP_402	m60[30B3]
C3007	CAP_402	m60[30D3]
C3008	CAP_402	m60[30A3]
C3009	CAP_402	m60[30A4]
C3010	CAP_402	m60[30D4]
C3011	CAP_402	m60[30D3]
C3013	CAP_402	m60[30A4]
C3014	CAP_402	m60[30A4]
C3015	CAP_402	m60[30A3]
C3030	CAP_402	m60[30C4]
C3033	CAP_402	m60[30C3]
C3035	CAP_402	m60[30C3]
C3100	CAP_402	m60[31C4]
C3101	CAP_805-1	m60[31B6]
C3102	CAP_805-1	m60[31B4]
C3105	CAP_P_SMC-LF	m60[31B4]
C3109	CAP_603	m60[31C5]
C3110	CAP_402	m60[31B6]
C3301	CAP_402	m60[33D6]
C3302	CAP_402	m60[33D6]
C3303	CAP_402	m60[33D6]
C3304	CAP_402	m60[33D6]
C3305	CAP_402	m60[33D4]
C3306	CAP_402	m60[33D4]
C3307	CAP_402	m60[33C4]
C3308	CAP_402	m60[33D4]
C3309	CAP_805-1	m60[33D4]
C3310	CAP_402	m60[33D3]
C3311	CAP_402	m60[33C6]
C3312	CAP_805-1	m60[33C6]
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C3315	CAP_402	m60[33D7]
C3316	CAP_805-1	m60[33D7]
C3317	CAP_805-1	m60[33D4]
C3389	CAP_402	m60[33C7]
C3390	CAP_402	m60[33C7]
C3800	CAP_402	m60[38B7]
C3801	CAP_402	m60[38B7]
C3802	CAP_402	m60[38B7]
C3803	CAP_402	m60[38B7]
C3804	CAP_402	m60[38C3]
C3805	CAP_402	m60[38C2]
C3806	CAP_805-2	m60[38C1]
C4101	CAP_402	m60[41D7]
C4102	CAP_402	m60[41D6]
C4103	CAP_402	m60[41D6]
C4104	CAP_402	m60[41D6]
C4105	CAP_402	m60[41D5]
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C4117	CAP_402	m60[41B2]
C4118	CAP_402	m60[41B2]
C4126	CAP_402	m60[41A8]
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C4128	CAP_402	m60[41A8]
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C4130	CAP_402	m60[41A7]
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C4140	CAP_402	m60[41B3]
C4150	CAP_402	m60[41D5]
C4200	CAP_1210	m60[42D8]
C4201	CAP_402	m60[42D7]
C4202	CAP_1210	m60[42D7]
C4203	CAP_1206-1	m60[42D6]
C4204	CAP_402	m60[42D6]
C4205	CAP_1210	m60[42C5]
C4206	CAP_402	m60[42C5]
C4209	CAP_603	m60[42B7]
C4210	CAP_402	m60[42B6]
C4300	CAP_402	m60[43D7]
C4301	CAP_402	m60[43D6]
C4304	CAP_402	m60[43C6]
C4305	CAP_402	m60[43B6]
C4401	CAP_402	m60[44D1]
C4402	CAP_402	m60[44C1]
C4410	CAP_402	m60[44D6]
C4412	CAP_402	m60[44D1]
C4500	CAP_402	m60[45D4]
C4501	CAP_402	m60[45D3]
C4502	CAP_402	m60[45D3]
C4503	CAP_805-1	m60[45C6]
C4504	CAP_402	m60[45C4]
C4505	CAP_402	m60[45C5]
C4506	CAP_402	m60[45C5]
C4507	CAP_402	m60[45C5]
C4508	CAP_402	m60[45D5]
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C4519	CAP_402	m60[45D5]
C4515	CAP_805-1	m60[45D6]
C4520	CAP_402	m60[45D5]
C4521	CAP_402	m60[45D4]
C4522	CAP_402	m60[45D3]
C4523	CAP_402	m60[45D3]
C4609	CAP_603-1	m60[46D5]
C4610	CAP_402	m60[46D4]
C4611	CAP_402	m60[46D4]
C4612	CAP_402	m60[46C4]
C4613	CAP_402	m60[46C4]
C4615	CAP_603-1	m60[46C2]
C4616	CAP_402	m60[46B2]
C4620	CAP_402	m60[46B4]
C4621	CAP_402	m60[46B4]
C4622	CAP_402	m60[46A4]
C4623	CAP_402	m60[46A4]
C4625	CAP_603-1	m60[46A2]
C4626	CAP_402	m60[46A2]
C4650	CAP_402	m60[46C7]
C4654	CAP_402	m60[46B8]
C4660	CAP_402	m60[46C7]
C4664	CAP_402	m60[46B7]
C4700	CAP_805-1	m60[47C8]
C4710	CAP_P_B2	m60[47D6]
C4712	CAP_402	m60[47D5]
C4713	CAP_402	m60[47D5]
C4720	CAP_P_B2	m60[47C6]
C4722	CAP_402	m60[47C5]
C4723	CAP_402	m60[47C5]
C4730	CAP_P_B2	m60[47B6]
C4732	CAP_402	m60[47A5]
C4733	CAP_402	m60[47A5]
C4742	CAP_402	m60[47D2]
C4743	CAP_402	m60[47D1]
C4750	CAP_402	m60[47B6]
C4751	CAP_402	m60[47C6]
C4752	CAP_402	m60[47D6]
C4796	CAP_402	m60[47C8]
C4797	CAP_805-2	m60[47D3]
C4798	CAP_402	m60[47A2]
C4799	CAP_805-2	m60[47A2]
C5300	CAP_402	m60[53B7]
C5301	CAP_402	m60[53B7]
C5304	CAP_402	m60[53D5]
C5305	CAP_402	m60[53D5]
C5306	CAP_402	m60[53D4]
C5307	CAP_402	m60[53C4]
C5308	CAP_402	m60[53C5]
C5309	CAP_402	m60[53C4]
C5310	CAP_402	m60[53C4]
C5311	CAP_805-1	m60[53C3]
C5312	CAP_805-1	m60[53D4]
C5313	CAP_402	m60[53C5]
C5314	CAP_805-1	m60[53C4]
C5700	CAP_402	m60[57D6]
C5701	CAP_603	m60[57D4]
C5702	CAP_402	m60[57C4]
C5703	CAP_603	m60[57B6]
C5706	CAP_402	m60[57C5]
C5707	CAP_402	m60[57C2]
C5708	CAP_402	m60[57C4]
C5709	CAP_1206	m60[57C3]
C5711	CAP_1210	m60[57D3]
C5713	CAP_805-1	m60[57D2]
C5714	CAP_805-1	m60[57D2]
C5715	CAP_P_TH-KZJ-LF	m60[57D2]
C5720	CAP_805	m60[57D8]
C5721	CAP_805-1	m60[57C8]
C5722	CAP_805-1	m60[57C8]
C5723	CAP_402	m60[57D7]
C5724	CAP_402	m60[57C6]
C5725	CAP_805-1	m60[57C8]
C5726	CAP_805-1	m60[57C7]
C5753	CAP_1210	m60[57D3]
C5792	CAP_603	m60[57D5]
C5797	CAP_1210	m60[57D2]
C5798	CAP_1210	m60[57D2]
C5799	CAP_1210	m60[57D3]
C5800	CAP_402	m60[59B8]
C5801	CAP_402	m60[59B8]
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C5803	CAP_402	m60[58D2]
C5804	CAP_402	m60[58D2]
C5805	CAP_402	m60[58D2]
C5806	CAP_402	m60[58D1]
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C5901	CAP_402	m60[59D8]
C5902	CAP_402	m60[59B7]
C5903	CAP_402	m60[59A8]
C5919	CAP_402	m60[59B4]
C5940	CAP_402	m60[59A4]
C5941	CAP_402	m60[59A3]
C5942	CAP_805-1	m60[59A3]
C5943	CAP_402	m60[59A5]
C5951	CAP_402	m60[59B1]
C6000	CAP_402	m60[60D6]
C6001	CAP_402	m60[60D6]
C6002	CAP_402	m60[60C6]
C6003	CAP_402	m60[60C6]
C6100	CAP_402	m60[61B5]
C6101	CAP_402	m60[61B5]
C6301	CAP_402	m60[63C2]
C6308	CAP_402	m60[63C5]
C6309	CAP_402	m60[63C6]
C6311	CAP_402	m60[63C2]
C6312	CAP_402	m60[63D3]
C6500	CAP_603	m60[65D5]
C6501	CAP_805	m60[65D5]
C6502	CAP_603	m60[65B4]
C6503	CAP_805	m60[65B5]
C6504	CAP_P_6.3X11-TH-LF1	m60[65C4]
C6505	CAP_P_6.3X11-TH-LF1	m60[65B3]
C6600	CAP_603	m60[66D4]
C6601	CAP_805	m60[66C5]
C6602	CAP_P_SM-LF	m60[66C3]
C6654	CAP_402	m60[66B4]
C6655	CAP_402	m60[66B2]
C6700	CAP_402	m60[67C4]
C6701	CAP_402	m60[67C4]
C6702	CAP_402	m60[67C3]
C6703	CAP_402	m60[67C3]
C6704	CAP_402	m60[59B7]
C6705	CAP_402	m60[59B7]
C6800	CAP_805-1	m60[68D6]
C6801	CAP_402	m60[68D6]
C6802	CAP_P_6.3X5.5-SM	m60[68D4]
C6803	CAP_P_6.3X5.5-SM	m60[68D3]
C6804	CAP_P_SMA-LF	m60[68B4]
C6805	CAP_805	m60[68B3]
C6806	CAP_805	m60[68B3]
C6807	CAP_P_SMA-LF	m60[68B3]
C6810	CAP_P_SMA-LF	m60[68B2]
C6812	CAP_402	m60[68B4]
C6813	CAP_402	m60[68B3]
C6821	CAP_402	m60[68C6]
C6830	CAP_402	m60[68D4]
C6833	CAP_402	m60[68B2]
C6835	CAP_402	m60[68D6]
C6836	CAP_402	m60[68D3]
C7200	CAP_P_6.3X8-SM	m60[72D5]
C7201	CAP_1210	m60[72D5]
C7202	CAP_805	m60[72D4]
C7203	CAP_1210	m60[72D3]
C7204	CAP_805	m60[72D6]
C7205	CAP_805	m60[72C6]
C7206	CAP_805	m60[72C6]
C7207	CAP_805	m60[72C6]
C7208	CAP_603-1	m60[72C4]
C7209	CAP_805	m60[72B4]
C7210	CAP_402	m60[72B3]
C7211	CAP_402	m60[72B2]
C7212	CAP_402	m60[72B2]
C7213	CAP_402	m60[72B2]
C7214	CAP_603	m60[72B5]
C7215	CAP_402	m60[72C6]
C7216	CAP_402	m60[72C6]
C7217	CAP_P_6.3X8-SM	m60[72D6]
C7218	CAP_603	m60[72D5]
C7219	CAP_603	m60[72D4]
C7221	CAP_402	m60[72B7]
C7223	CAP_1210	m60[72D3]
C7317	CAP_402	m60[73B4]
C7318	CAP_805-1	m60[73B4]
C7326	CAP_402	m60[73D8]
C7400	CAP_402	m60[74B4]
C7401	CAP_402	m60[74D5]
C7402	CAP_402	m60[74A4]
C7403	CAP_P_6.3X5.5-SM	m60[74B7]
C7404	CAP_P_6.3X5.5-SM	m60[74B6]
C7405	CAP_P_SMA-LF	m60[74C7]
C7406	CAP_P_SMA-LF	m60[74C6]
C7407	CAP_402	m60[74D8]
C7408	CAP_402	m60[74D7]
C7415	CAP_402	m60[74A8]
C7416	CAP_402	m60[74A8]
C7417	CAP_402	m60[74A8]
C7418	CAP_805	m60[74A5]
C7419	CAP_603-1	m60[74A4]
C7424	CAP_402	m60[74C3]
C7435	CAP_P_6.3X8-SM	m60[74A3]
C7500	CAP_402	m60[75C4]
C7501	CAP_P_TH-MCZ	m60[75C2]
C7502	CAP_402	m60[75B4]
C7503	CAP_402	m60[75C1]
C7504	CAP_402	m60[75B1]
C7505	CAP_402	m60[75C8]
C7506	CAP_402	m60[75B7]
C7507	CAP_402	m60[75B7]
C7508	CAP_1210	m60[75C2]
C7509	CAP_1210	m60[75D1]
C7510	CAP_402	m60[75C8]
C7511	CAP_603	m60[75B2]
C7512	CAP_603	m60[75C2]
C7513	CAP_402	m60[75B7]
C7514	CAP_402	m60[75B8]
C7515	CAP_603	m60[75C4]

C7516	CAP_402	m60[75B4]
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C7518	CAP_P_SM-3	m60[75D2]
C7521	CAP_402	m60[75A6]
C7526	CAP_603	m60[75D6]
C7527	CAP_603	m60[75C5]
C7528	CAP_402	m60[75B5]
C7529	CAP_402	m60[75B5]
C7530	CAP_402	m60[75D6]
C7531	CAP_402	m60[75B5]
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C7533	CAP_402	m60[75B6]
C7534	CAP_402	m60[75B5]
C7535	CAP_603	m60[75D5]
C7550	CAP_603	m60[75D1]
C7551	CAP_603	m60[75D1]
C7590	CAP_402	m60[75C3]
C7592	CAP_402	m60[75B3]
C7596	CAP_402	m60[75D6]
C7597	CAP_1210	m60[75D1]
C7598	CAP_1210	m60[75D1]
C7599	CAP_402	m60[76D6]
C7612	CAP_402	m60[76B2]
C7633	CAP_402	m60[76C7]
C7710	CAP_402	m60[77C7]
C7711	CAP_402	m60[77B7]
C7712	CAP_402	m60[77C7]
C7750	CAP_402	m60[77B2]
C7751	CAP_805	m60[77C3]
C7752	CAP_805	m60[77C3]
C7753	CAP_402	m60[77B5]
C7754	CAP_402	m60[77B4]
C7755	CAP_805	m60[77B2]
C7756	CAP_805	m60[77B2]
C7757	CAP_402	m60[77B5]
C7797	CAP_402	m60[77C3]
C7798	CAP_603	m60[77B5]
C7799	CAP_402	m60[77A2]
C7800	CAP_1210	m60[78C3]
C7801	CAP_P_TH-MCZ	m60[78C4]
C7802	CAP_603	m60[78C6]
C7803	CAP_603	m60[78B7]
C7804	CAP_402	m60[78C7]
C7805	CAP_603	m60[78C5]
C7806	CAP_805-1	m60[78B3]
C7807	CAP_P_TH	m60[78B3]
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C7810	CAP_402	m60[78B5]
C7811	CAP_402	m60[78B5]
C7813	CAP_1206	m60[78B4]
C7814	CAP_402	m60[78B5]
C7897	CAP_805-1	m60[78B2]
C7899	CAP_1210	m60[78C3]
C7900	CAP_402	m60[79D6]
C7901	CAP_603	m60[79D5]
C7902	CAP_402	m60[79C5]
C7903	CAP_603	m60[79C7]
C7906	CAP_402	m60[79C5]
C7907	CAP_402	m60[79C3]
C7908	CAP_402	m60[79C5]
C7909	CAP_1206	m60[79C3]
C7910	CAP_P_TH-MCZ	m60[79D4]
C7911	CAP_1210	m60[79D3]
C7912	CAP_P_CASE-D2E-LF	m60[79C2]
C7913	CAP_1206	m60[79C2]
C7980	CAP_402	m60[79A3]
C7992	CAP_603	m60[79D6]
C7997	CAP_1210	m60[79D3]
C7998	CAP_P_CASE-D2E-LF	m60[79C2]
C8000	CAP_1210	m60[80D3]
C8001	CAP_P_CASE-D2E-LF	m60[80C2]
C8002	CAP_603	m60[80D6]
C8003	CAP_402	m60[80C3]
C8004	CAP_1206	m60[80C3]
C8005	CAP_402	m60[80C4]
C8006	CAP_402	m60[80D6]
C8009	CAP_603	m60[80C6]
C8010	CAP_603	m60[80C4]
C8011	CAP_402	m60[80C5]
C8012	CAP_402	m60[80C5]
C8015	CAP_1210	m60[80D3]
C8016	CAP_805-1	m60[80C2]
C8090	CAP_1210	m60[80D3]
C8091	CAP_1210	m60[80D2]
C8092	CAP_1210	m60[80D2]
C8099	CAP_P_CASE-D2E-LF	m60[80C2]
C8100	CAP_402	m60[81D6]
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C8102	CAP_402	m60[81C5]
C8103	CAP_603	m60[81C7]
C8106	CAP_402	m60[81C5]
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C8108	CAP_402	m60[81C5]
C8109	CAP_1206	m60[81C3]
C8110	CAP_1210	m60[81D4]
C8111	CAP_1210	m60[81D3]
C8112	CAP_1210	m60[81D3]
C8114	CAP_P_CASE-D2E-LF	m60[81C2]
C8115	CAP_805-1	m60[81C2]
C8190	CAP_P_CASE-D2E-LF	m60[81C2]
C8192	CAP_603	m60[81D6]
C8198	CAP_1210	m60[81D3]
C8199	CAP_402	m60[81A5]
C8200	CAP_402	m60[82D6]
C8201	CAP_603	m60[82D4]
C8202	CAP_402	m60[82C4]
C8203	CAP_603	m60[82B6]
C8206	CAP_402	m60[82C5]
C8207	CAP_402	m60[82C2]
C8208	CAP_402	m60[82C4]
C8209	CAP_1206	m60[82C3]
C8211	CAP_1210	m60[82D3]
C8213	CAP_805-1	m60[82D2]
C8214	CAP_805-1	m60[82D2]
C8215	CAP_P_TH-KZJ-LF	m60[82D2]
C8220	CAP_805	m60[82D8]
C8221	CAP_805-1	m60[82C8]
C8222	CAP_805-1	m60[82C8]
C8223	CAP_402	m60[82D7]
C8224	CAP_402	m60[82C6]
C8225	CAP_805-1	m60[82C8]
C8226	CAP_805-1	m60[82C7]
C8253	CAP_P_TH-KZJ-LF	m60[82D3]
C8292	CAP_603	m60[82D5]

C8310	CAP_603-1	m60[83D8]
C8311	CAP_603-1	m60[83D7]
C8315	CAP_603-1	m60[83B5]
C8316	CAP_603	m60[83A6]
C8317	CAP_603-1	m60[83B8]
C8318	CAP_603-1	m60[83B7]
C8319	CAP_603	m60[83A7]
C8320	CAP_402	m60[83A7]
C8321	CAP_603-1	m60[83C5]
C8325	CAP_603-1	m60[83D6]
C8326	CAP_603-1	m60[83D5]
C8398	CAP_603	m60[83C2]
C8399	CAP_603	m60[83D2]
C8400	CAP_805	m60[84C7]
C8401	CAP_402	m60[84C7]
C8402	CAP_402	m60[84C7]
C8405	CAP_805	m60[84B7]
C8406	CAP_402	m60[84B7]
C8407	CAP_402	m60[84B7]
C8410	CAP_805	m60[84B6]
C8411	CAP_402	m60[84B7]
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C8502	CAP_603	m60[85D6]
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C8507	CAP_402	m60[85C7]
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C8521	CAP_402	m60[85C4]
C8522	CAP_402	m60[85C5]
C8530	CAP_1210	m60[85D4]
C8531	CAP_1210	m60[85D4]
C8532	CAP_1210	m60[85D4]
C8540	CAP_805	m60[85C2]
C8541	CAP_805	m60[85C2]
C8542	CAP_P_CASE-D2E-LF	m60[85C2]
C8543	CAP_P_CASE-D2E-LF	m60[85C2]
C8590	CAP_402	m60[85D3]
C8592	CAP_402	m60[85C2]
C8595	CAP_402	m60[85D1]
C8598	CAP_402	m60[85D2]
C8599	CAP_1206	m60[85C4]
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C8616	CAP_402	m60[86C5]
C8630	CAP_805	m60[86C6]

C8631	CAP_402	m60[86C6]
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C8634	CAP_402	m60[86C5]
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C8723	CAP_402	m60[87B4]
C8725	CAP_402	m60[87A4]
C8726	CAP_402	m60[87A3]
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C8902	CAP_402	m60[89D7]
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C8973	CAP_402	m60[89C4]
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C8983	CAP_402	m60[89C3]
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C9065	CAP_402	m60[90D3]
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C9081	CAP_402	m60[90C3]
C9083	CAP_402	m60[90C3]
C9100	CAP_805	m60[91C5]
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C9103	CAP_402	m60[91C5]
C9110	CAP_805	m60[91C5]
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C9115	CAP_805	m60[91B5]
C9116	CAP_402	m60[91B5]
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C9127	CAP_402	m60[91B5]
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C9137	CAP_402	m60[91A5]
C9140	CAP_805	m60[91A6]
C9141	CAP_402	m60[91A6]
C9142	CAP_402	m60[91A5]
C9191	CAP_402	m60[91D2]
C9300	CAP_805	m60[93C6]
C9301	CAP_402	m60[93C6]
C9302	CAP_402	m60[93C5]
C9305	CAP_805	m60[93C6]
C9306	CAP_402	m60[93C6]
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C9327	CAP_402	m60[93B7]
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C9340	CAP_805	m60[93A6]
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C9342	CAP_402	m60[93A5]
C9345	CAP_805	m60[93A6]
C9346	CAP_402	m60[93A5]
C9347	CAP_402	m60[93A5]
C9400	CAP_603-1	m60[94C7]
C9401	CAP_402	m60[94C6]
C9410	CAP_402	m60[94C6]
C9420	CAP_1210	m60[94C5]
C9470	CAP_402	m60[94B2]
C9700	CAP_402	m60[97C8]
C9710	CAP_603	m60[97C3]
C9711	CAP_402	m60[97D3]
C9713	CAP_402	m60[97C2]
C9714	CAP_402	m60[97C2]
C9740	CAP_402	m60[97A7]
C9741	CAP_402	m60[97A6]
C9742	CAP_402	m60[97A6]
C9750	CAP_402	m60[97B4]
D2500	DIODE_SCHOT_SOT23	m60[25C8]
D2501	DIODE_SCHOT_SOT23	m60[25D8]
D2600	DIODE_SCHOT_SOT23	m60[26D8]
D2601	DIODE_SCHOT_SOT23	m60[26C8]
D4600	DIODE_SMC	m60[46D5]
D4690	ZENER_SOT23	m60[46A6]
D4700	DIODE_SCHOT_3P_A_SC-75	m60[47C5]
D4701	DIODE_SCHOT_3P_A_SC-75	m60[47B5]
D4702	DIODE_SCHOT_3P_A_SC-75	m60[47A5]
D5700	DIODE_SCHOT_5P_TLM83	m60[57C4]
D6500	DIODE_SOT23	m60[65C4]
D6501	DIODE_SOT23	m60[65B4]
D6502	DIODE_SCHOT_SMB	m60[65C4]
D6503	DIODE_SCHOT_SMB	m60[65B4]
D6600	DIODE_SOT23	m60[66C4]
D6601	DIODE_SCHOT_SMB	m60[66C3]
D7500	DIODE_SCHOT_SMB	m60[75C3]
D7501	DIODE_SCHOT_SMB	m60[75B2]
D7599	DIODE_SOT23	m60[76D6]
D7800	DIODE_SCHOT_5P_TLM83	m60[78B4]
D7900	DIODE_SCHOT_5P_TLM83	m60[79C4]
D8000	DIODE_SCHOT_5P_TLM83	m60[80C4]
D8100	DIODE_SCHOT_5P_TLM83	m60[81C4]
D8200	DIODE_SCHOT_5P_TLM83	m60[82C3]
D8310	DIODE_SCHOT_SOD-123	m60[83A6]
D8520	DIODE_SCHOT_SMB	m60[85C3]
D9700	ZENER_CASE425	m60[97C1]
DP4610	DIODE_DUAL_6P_SOT-36	m60[46D4 46D3]
DP4611	DIODE_DUAL_6P_SOT-36	m60[46C4 46C3]
DP4620	DIODE_DUAL_6P_SOT-36	m60[46B4 46B3]
DP4621	DIODE_DUAL_6P_SOT-36	m60[46A4 46A3]
DZ7300	SUPPR_TRANSIENT1_402	m60[73D6]
DZ7301	SUPPR_TRANSIENT1_402	m60[73C6]
DZ7302	SUPPR_TRANSIENT1_402	m60[73C6]
DZ7311	SUPPR_TRANSIENT1_402	m60[73A7]
DZ7313	SUPPR_TRANSIENT1_402	m60[73A6]
DZ7314	SUPPR_TRANSIENT1_402	m60[73A6]
DZ7315	SUPPR_TRANSIENT1_402	m60[73A6]
DZ7323	SUPPR_TRANSIENT1_402	m60[73A5]
DZ7324	SUPPR_TRANSIENT1_402	m60[73C5]
DZ7325	SUPPR_TRANSIENT1_402	m60[73C3]
DZ7326	SUPPR_TRANSIENT1_402	m60[73C3]
DZ7380	SUPPR_TRANSIENT1_402	m60[73A7]
F4602	FUSE_MINISMD-LF	m60[46D3]
F4701	FUSE_MINISMD-LF	m60[47D3]
F9710	FUSE_SM-LF	m60[97D5]
FL4610	FILTER_4P_2012	m60[46C3]
FL4620	FILTER_4P_2012	m60[46B3]
FL9740	FILTER_LC_SM-220MHZ-LF	m60[97B7]
FL9741	FILTER_LC_SM-220MHZ-LF	m60[97A7]
FL9742	FILTER_LC_SM-220MHZ-LF	m60[97A7]
FLE011	FILTER_4P_2012	m60[46C3]
FLE021	FILTER_4P_2012	m60[46B3]

GV3801	HOLE_VIA	m60[38A8]	
GV3802	HOLE_VIA	m60[38A7]	
GV3803	HOLE_VIA	m60[38A8]	
GV3804	HOLE_VIA	m60[38A7]	
GV3805	HOLE_VIA	m60[38A8]	
GV3806	HOLE_VIA	m60[38A7]	
GV3807	HOLE_VIA	m60[38A8]	
GV3808	HOLE_VIA	m60[38A7]	
J3	CON_2RTSM_125_SM-2MT-BLK-LF	m60[61B6]	
J600	CON_M14RT_D_THA_M-RT-TH1	m60[6D7]	
J0700	CPU_YONAH_SKT_BGA	m60[7C3 7D7]	
J0700	CPU_YONAH_SKT_BGA	m60[8D4 8D8]	
J1000	CON_2RTSM_125_SM-2MT-BLK-LF	m60[10B7]	
J1101	CON_F28RT_S2MT_SM_F-RT-SM	m60[11C2]	
J2600	BATTERY_2P_SM	m60[26C8]	
J2800	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m60[28D5]	
J2900	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m60[29D5]	
J2901	CON_F4ST_S2MT_SM_F-ST-SM	m60[59C7]	
J2903	CON_M2ST_S2MT_SM_M-ST-SM	m60[59C8]	
J4700	CON_F10ST_D_SMA_F-ST-SM	m60[47A2]	
J5300	CON_F52RT_D2MT_SM_F-RT-SM	m60[53C5]	
J6000	CON_F30STSM_5047_SM1	m60[60B5]	
J6500	CON_M4RT_S2MT_SM_M-RT-SM	m60[65D3]	
J6501	CON_M5RT_S2MT_SMA_M-RT-SM	m60[65B2]	
J6600	CON_F4ST_S2MT_SM_F-ST-SM	m60[66C2]	
J6601	CON_M4RT_S2MT_SM_M-RT-SM	m60[66B5]	
J6602	CON_M4RT_S2MT_SM_M-RT-SM	m60[66B3]	
J7300	CON_F9ANG_S4MT_TH3_F-ANG-TH	m60[73D8]	
J7301	CON_M7RT_S2MT_SM_M-RT-SM	m60[73C1]	
J7303	CON_F9ANG_S4MT_TH1_F-ANG-TH	m60[73B3]	
J9402	CON_F30ST_D_SM_F-ST-SM	m60[94B6]	
J9710	CON_DVI_F32ST_Q2MT_S-M_F-ST-SM	m60[97D5]	
JC900	CON_M7ST_SATA_SM_M-S-T-SM	m60[38B8]	
JC901	CON_M50SM_5MM_M-ST-S-M2-LF	m60[38C2]	
JD600	CON_RJ45_10ANG_S3MT_TH1_F-ANG-TH	m60[43C6]	
JE000	CON_F6ANG_S4MT_TH1_F-ANG-TH	m60[46C2]	
JE001	CON_F6ANG_S4MT_TH1_F-ANG-TH	m60[46B2]	
JE310	CON_F4ANG_3MT_USB_TH1_F-ANG-TH	m60[47D4]	
JE320	CON_F4ANG_3MT_USB_TH1_F-ANG-TH	m60[47B4]	
JE330	CON_F4ANG_3MT_USB_TH1_F-ANG-TH	m60[47A4]	
JE350	CON_M14RT_S2MT_SM_M-RT-SM	m60[47C1]	
L1934	IND_0603	m60[19C7]	
L1936	IND_0603	m60[19C7]	
L1970	IND_1210	m60[19A5]	
L1975	IND_0805	m60[19A5]	
L2500	IND_SM-3	m60[25B8]	
L2507	IND_1206	m60[25A7]	
L3301	IND_0402	m60[33D7]	
L3302	IND_0402	m60[33D3]	
L4200	IND_SM	m60[42D7]	
L4201	IND_SM	m60[42B7]	
L4300	IND_SM	m60[43D7]	
L4409	IND_0402	m60[44D6]	
L4610	IND_1206-LF	m60[46D2]	
L4620	IND_1206-LF	m60[46B2]	
L4690	IND_SM-1	m60[46A6]	
L4710	IND_SM	m60[47D6]	
L4712	FILTER_4P_2012	m60[47C6]	
L4720	IND_SM	m60[47C6]	
L4722	FILTER_4P_2012	m60[47B6]	
L4730	IND_SM	m60[47B6]	
L4732	FILTER_4P_2012	m60[47A6]	
L4740	IND_SM	m60[47D2]	
L4742	FILTER_4P_2012	m60[47C2]	
L4752	FILTER_4P_2012	m60[47B2]	
L5703	IND_IHLP	m60[57D3]	
L6801	IND_0603	m60[68D6]	
L6802	IND_0603	m60[68A4]	
L7200	IND_SM-1	m60[72D6]	
L7201	IND_0603	m60[72C2]	
L7202	IND_0603	m60[72C2]	
L7203	IND_0603	m60[72C3]	
L7204	IND_0603	m60[72C3]	
L7205	IND_0603	m60[72D6]	
L7206	IND_0603	m60[72C6]	
L7207	IND_0603	m60[72C6]	
L7208	IND_0603	m60[72C6]	
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L7301	IND_0603	m60[73D6]	
L7302	IND_0603	m60[73D6]	
L7303	IND_0603	m60[73D6]	
L7304	IND_0603	m60[73D5]	
L7305	IND_0603	m60[73D5]	
L7306	IND_0603	m60[73D5]	
L7307	IND_0603	m60[73D5]	
L7309	IND_0603	m60[73C4]	
L7310	IND_0603	m60[73C4]	
L7312	IND_0603	m60[73C3]	
L7313	IND_0603	m60[73C3]	
L7315	IND_0603	m60[73B7]	
L7316	IND_0603	m60[73B7]	
L7317	IND_0603	m60[73A7]	
L7318	IND_0603	m60[73B7]	
L7319	IND_0603	m60[73A7]	
L7323	IND_0603	m60[73B5]	
L7324	IND_0603	m60[73B5]	
L7325	IND_0603	m60[73A5]	
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L7327	IND_0603	m60[73A5]	
L7381	IND_0603	m60[73A5]	
L7500	IND_SM	m60[75D1]	
L7501	IND_SM	m60[75B2]	
L7502	IND_TH-VERT-LF	m60[76D8]	
L7750	IND_SM-LF	m60[77B2]	
L7800	IND_3P_SM	m60[78C3]	
L7880	IND_0603	m60[73A7]	
L7900	IND_3P_SM	m60[79C3]	
L8000	IND_IHLP	m60[80C3]	
L8100	IND_IHLP	m60[81C3]	
L8203	IND_IHLP	m60[82D3]	
L8400	IND_0402	m60[84B7]	
L8520	IND_IHLP	m60[85C3]	
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L9305	IND_0402	m60[93C7]	
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L9315	IND_0402	m60[93C7]	
L9320	IND_0402	m60[93B7]	
L9325	IND_0402	m60[93B7]	
L9330	IND_0402	m60[93B7]	
L9345	IND_0402	m60[93B7]	
L9400	IND_SM	m60[94C6]	
L9700	FILTER_4P_2012H	m60[97D7]	
L9701	FILTER_4P_2012H	m60[97D7]	
L9702	FILTER_4P_2012H	m60[97C7]	
L9703	FILTER_4P_SM	m60[97C7]	
L9710	IND_SM-1	m60[97D5]	
LED601	LED_2.0X1.25MM-SM	m60[6A8]	
LED602	LED_2.0X1.25MM-SM	m60[6A7]	
LED603	LED_2.0X1.25MM-SM	m60[6A6]	
LED3800	LED_2.0X1.25MM-SM	m60[38B3]	
LED5950	LED_3X2MM-SM	m60[59A1]	
LED7900	LED_2.0X1.25MM-SM	m60[79A4]	
LED8000	LED_2.0X1.25MM-SM	m60[80A4]	
LED8100	LED_2.0X1.25MM-SM	m60[81A4]	
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PP702	TP_SM-TP50-TOP	m60[5D3]	
PP1200	TP_SM-TP50-TOP	m60[5D3]	
PP1201	TP_SM-TP50-TOP	m60[5D3]	
PP1202	TP_SM-TP50-TOP	m60[5D3]	
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PP2802	TP_SM-TP50-TOP	m60[5C3]	
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PP9036	PROBEPOINT_SM	m60[5A4]	
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Q5700	TRA_IRLR7807Z_TO-252-AA	m60[57D4]	
Q5701	TRA_IRLR7807Z_TO-252-AA	m60[57C4]	
Q5702	TRA_2N7002_SOT23-LF	m60[57B7]	
Q5703	TRA_IRF1902PBF_SO-8	m60[57D7]	
Q5901	TRA_2N7002DW_SOT-363	m60[59C7 59C7]	
Q5910	TRA_SINGLE_MOSFET_PC-HN_SOT-23	m60[59A4]	
Q5911	TRA_2N7002_SOT23-LF	m60[59A4]	
Q5950	TRA_2N7002_SOT23-LF	m60[59A2]	
Q5951	TRA_2N7002_SOT23-LF	m60[59B2]	
Q5952	TRA_2N3906_SOT23-LF	m60[59B1]	
Q6500	TRA_NTHS5443T1_1206A-03-LF	m60[65D4]	
Q6502	TRA_2N7002_SOT23-LF	m60[65D6]	
Q6503	TRA_NTHS5443T1_1206A-03-LF	m60[65B4]	
Q6505	TRA_2N7002_SOT23-LF	m60[65B6]	
Q6600	TRA_NTHS5443T1_1206A-03-LF	m60[66D4]	
Q6602	TRA_2N7002_SOT23-LF	m60[66C5]	
Q7200	TRA_2N7002DW_SOT-363	m60[72B6 72B7]	
Q7400	TRA_2N7002DW_SOT-363	m60[74B3 74B3]	
Q7401	TRA_2N7002_SOT23-LF	m60[74D5]	
Q7402	TRA_2N7002DW_SOT-363	m60[74B2 74B2]	
Q7500	TRA_HAT2168H_LFPAK	m60[75D3]	
Q7501	TRA_HAT2165H_LFPAK	m60[75D3]	
Q7502	TRA_HAT2168H_LFPAK	m60[75C3]	
Q7503	TRA_HAT2165H_LFPAK	m60[75B3]	
Q7504	TRA_HAT2165H_LFPAK	m60[75D3]	
Q7505	TRA_HAT2165H_LFPAK	m60[75B3]	
Q7570	TRA_HAT2168H_LFPAK	m60[75D2]	
Q7572	TRA_HAT2168H_LFPAK	m60[75C3]	
Q7701	TRA_SI3446DV_TSOP-LF	m60[77B2]	
Q7703	TRA_2N7002DW_SOT-363	m60[77C7 77D7]	
Q7799	TRA_2N7002_SOT23-LF	m60[77B6]	
Q7800	TRA_NTD60N02R_CASE36-9-LF	m60[78C4]	
Q7801	TRA_NTD60N02R_CASE36-9-LF	m60[78B5]	
Q7802	TRA_2N7002_SOT23-LF	m60[78B8]	
Q7900	TRA_NTD60N02R_CASE36-9-LF	m60[79D4]	
Q7901	TRA_NTD60N02R_CASE36-9-LF	m60[79C4]	
Q7902	TRA_2N7002_SOT23-LF	m60[79C7]	
Q8000	TRA_NTD60N02R_CASE36-9-LF	m60[80D4]	
Q8001	TRA_NTD60N02R_CASE36-9-LF	m60[80C4]	
Q8003	TRA_2N7002_SOT23-LF	m60[80C7]	
Q8102	TRA_NTD60N02R_CASE36-9-LF	m60[81D4]	
Q8103	TRA_NTD60N02R_CASE36-9-LF	m60[81C4]	
Q8104	TRA_2N7002_SOT23-LF	m60[81C7]	
Q8200	TRA_IRLR7807Z_TO-252-AA	m60[82D4]	
Q8201	TRA_IRLR7807Z_TO-252-AA	m60[82C4]	
Q8202	TRA_2N7002_SOT23-LF	m60[82B7]	
Q8203	TRA_IRF1902PBF_SO-8	m60[82D7]	

Q8300	TRA_IRF7413_SO-8	m60[83D2]
Q8301	TRA_IRF7413_SO-8	m60[83C2]
Q8302	TRA_2N7002_SOT23-LF	m60[83C3]
Q8303	TRA_2N7002_SOT23-LF	m60[83D3]
Q8310	TRA_SI3446DV_TSOP-LF	m60[83D8]
Q8311	TRA_2N7002_SOT23-LF	m60[83C7]
Q8312	TRA_SI3446DV_TSOP-LF	m60[83C5]
Q8313	TRA_IRF7410_SO-8	m60[83B6]
Q8315	TRA_2N7002_SOT23-LF	m60[83B5]
Q8316	TRA_2N7002_SOT23-LF	m60[83C5]
Q8317	TRA_SI3446DV_TSOP-LF	m60[83D5]
Q8318	TRA_DUAL_2N7002A_SOT 563	m60[83A8 83A7]
Q8319	TRA_SI3446DV_TSOP-LF	m60[83C8]
Q8320	TRA_2N7002_SOT23-LF	m60[83B7]
Q8520	TRA_HAT2168H_LFPAK	m60[85D4]
Q8521	TRA_HAT2165H_LFPAK	m60[85C4]
Q8522	TRA_HAT2165H_LFPAK	m60[85C5]
Q9400	TRA_SI3443DV_TSOP-LF	m60[94C7]
Q9401	TRA_2N7002_SOT23-LF	m60[94C8]
Q9711	TRA_2N7002DW_SOT-363	m60[97D2 97C2]
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R603	RES_402	m60[6B1]
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R2502	RES_402	m60[25D8]
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R6606	RES_805	m60[66C5]
R6607	RES_805	m60[66C3]
R6698	RES_402	m60[66C7]
R6700	RES_402	m60[67C6]
R6702	RES_402	m60[67C4]
R6703	RES_402	m60[67C4]
R6704	RES_805	m60[67C2]
R6705	RES_805	m60[67C3]
R6798	RES_402	m60[67B6]
R6799	RES_402	m60[67B6]
R6800	RES_402	m60[68C6]
R6801	RES_805	m60[68B5]
R6807	RES_402	m60[68D7]
R6808	RES_402	m60[68D3]
R7208	RES_402	m60[72A4]
R7212	RES_402	m60[72B7]
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R7214	RES_402	m60[72C5]
R7215	RES_402	m60[72C7]
R7216	RES_402	m60[72C5]
R7217	RES_402	m60[72B5]
R7218	RES_402	m60[72A5]
R7219	RES_402	m60[72B6]
R7302	RES_402	m60[73A4]
R7305	RES_402	m60[73C8]
R7306	RES_402	m60[73D4]
R7307	RES_805	m60[73C6]
R7308	RES_402	m60[73B8]
R7400	RES_402	m60[74B4]
R7404	RES_402	m60[74D5]
R7405	RES_402	m60[74D5]
R7407	RES_402	m60[74B4]
R7408	RES_402	m60[74A4]

R7409	RES_402	m60[74B4]
R7410	RES_805	m60[74D2]
R7411	RES_805	m60[74C2]
R7412	RES_805	m60[74C2]
R7413	RES_402	m60[74B4]
R7414	RES_805	m60[74B7]
R7415	RES_805	m60[74B8]
R7416	RES_805	m60[74C7]
R7417	RES_805	m60[74C8]
R7418	RES_402	m60[74B6]
R7419	RES_402	m60[74B6]
R7420	RES_402	m60[74D5]
R7421	RES_402	m60[74D8]
R7422	RES_402	m60[74D7]
R7423	RES_402	m60[74B6]
R7424	RES_402	m60[74B6]
R7425	RES_603	m60[74A5]
R7426	RES_402	m60[74A4]
R7427	RES_402	m60[74A4]
R7430	RES_402	m60[74C1]
R7431	RES_402	m60[74C2]
R7435	RES_402	m60[74A3]
R7437	RES_402	m60[74C5]
R7442	RES_805	m60[74D3]
R7443	RES_805	m60[74D3]
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R7501	RES_603	m60[75C2]
R7502	RES_1206	m60[75B2]
R7503	RES_1206	m60[75D2]
R7504	RES_402	m60[75C1]
R7505	RES_402	m60[75B2]
R7506	RES_603	m60[75B2]
R7507	RES_402	m60[75B1]
R7508	RES_402	m60[75B8]
R7509	RES_402	m60[75B8]
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R7511	RES_402	m60[75B7]
R7512	RES_402	m60[75D7]
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R7518	RES_402	m60[75B5]
R7519	RES_402	m60[75C7]
R7520	RES_402	m60[75D7]
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R7523	RES_402	m60[75A5]
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R7527	RES_402	m60[75C8]
R7528	RES_402	m60[75A5]
R7529	RES_402	m60[75A5]
R7530	RES_402	m60[75B4]
R7531	THERMISTER_0603-LF	m60[75B4]
R7540	RES_603	m60[75C1]
R7541	RES_603	m60[75B1]
R7590	RES_402	m60[75C7]
R7591	RES_402	m60[75C7]
R7592	RES_402	m60[75C7]
R7593	RES_402	m60[75C7]
R7594	RES_402	m60[75C7]
R7595	RES_402	m60[75C7]
R7596	RES_402	m60[75D7]
R7597	RES_402	m60[76D6]
R7598	RES_402	m60[76D7]
R7599	RES_2512-1	m60[76D7]
R7602	RES_402	m60[76D3]
R7612	RES_402	m60[76B2]
R7620	RES_402	m60[76D2]
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R7640	RES_402	m60[76A6]
R7691	RES_402	m60[76C7]
R7750	RES_402	m60[77B2]
R7751	RES_402	m60[77B2]
R7752	RES_402	m60[77B2]
R7753	RES_402	m60[77B5]
R7754	RES_402	m60[77B5]
R7757	RES_402	m60[77C5]
R7793	RES_402	m60[77D7]
R7794	RES_402	m60[77C7]
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R7800	RES_402	m60[78C7]
R7801	RES_402	m60[78B7]
R7802	RES_402	m60[78B3]
R7803	RES_402	m60[78B3]
R7804	RES_1206	m60[78B4]
R7805	RES_402	m60[78B6]
R7812	RES_402	m60[78B3]
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R7902	RES_1206	m60[79C3]
R7903	RES_402	m60[79C3]
R7904	RES_402	m60[79C5]
R7905	RES_402	m60[79D7]
R7906	RES_402	m60[79A4]
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R7991	RES_402	m60[79C7]
R7992	RES_402	m60[79C7]
R7999	RES_402	m60[79C3]
R8000	RES_402	m60[80B3]
R8001	RES_402	m60[80C7]
R8002	RES_1206	m60[80C3]
R8003	RES_402	m60[80C3]
R8004	RES_402	m60[80C5]
R8005	RES_402	m60[80D7]
R8007	RES_402	m60[80A4]
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R8012	RES_402	m60[80B3]
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R8092	RES_402	m60[80C7]
R8099	RES_402	m60[80C3]
R8101	RES_402	m60[81B3]
R8102	RES_1206	m60[81C3]
R8103	RES_402	m60[81C3]
R8104	RES_402	m60[81C5]
R8105	RES_402	m60[81D7]
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R8191	RES_402	m60[81C7]
R8192	RES_402	m60[81C7]
R8198	RES_402	m60[81A5]
R8199	RES_402	m60[81A5]
R8201	RES_402	m60[82C2]
R8202	RES_1206	m60[82C3]
R8203	RES_402	m60[82C2]
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R8222	RES_402	m60[82C7]
R8240	RES_402	m60[82D5]
R8292	RES_402	m60[82B6]
R8299	RES_402	m60[82C2]
R8300	RES_402	m60[83C3]
R8301	RES_402	m60[83D3]
R8302	RES_402	m60[83C3]
R8303	RES_402	m60[83D3]
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R8593	RES_402	m60[85D3]
R8594	RES_402	m60[85D3]
R8596	RES_402	m60[85D3]
R8597	THERMISTER_0603-LF	m60[85D3]
R8598	RES_402	m60[85D2]
R8599	RES_1206	m60[85C4]
R8630	RES_603	m60[86C7]
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R8713	RES_402	m60[87A7]
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R8722	RES_402	m60[87B4]
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R8732	RES_402	m60[87A3]
R8733	RES_402	m60[87A1]
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R8804	RES_402	m60[88D4]
R8805	RES_402	m60[88C4]
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R8809	RES_402	m60[88C4]
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R8811	RES_402	m60[88B4]
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R8947	RES_402	m60[89B7]
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R8949	RES_402	m60[89A7]
R8980	RES_402	m60[89C4]
R8981	RES_402	m60[89C4]
R8982	RES_402	m60[89C4]
R8983	RES_402	m60[89C4]
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R9033	RES_402	m60[90C7]
R9040	RES_402	m60[90B8]
R9041	RES_402	m60[90A8]
R9042	RES_402	m60[90B7]
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R9044	RES_402	m60[90B7]
R9045	RES_402	m60[90B7]
R9046	RES_402	m60[90B7]
R9047	RES_402	m60[90B7]
R9048	RES_402	m60[90A7]
R9049	RES_402	m60[90A7]
R9080	RES_402	m60[90C4]
R9081	RES_402	m60[90C4]
R9082	RES_402	m60[90C4]
R9083	RES_402	m60[90C4]
R9090	RES_402	m60[90B5]
R9091	RES_402	m60[90A4]
R9092	RES_402	m60[90B4]
R9093	RES_402	m60[90B4]
R9094	RES_402	m60[90B4]
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R9099	RES_402	m60[90A4]
R9190	RES_402	m60[91D2]
R9191	RES_402	m60[91D2]
R9195	RES_402	m60[91A3]
R9202	RES_402	m60[92C6]
R9250	RES_402	m60[92C6]
R9350	RES_402	m60[93A8]
R9351	RES_402	m60[93A8]
R9370	RES_402	m60[93D1]
R9371	RES_402	m60[93D1]
R9372	RES_402	m60[93C1]
R9373	RES_402	m60[93C1]
R9390	RES_402	m60[93A1]
R9391	RES_402	m60[93A1]
R9400	RES_402	m60[94C8]
R9401	RES_402	m60[94C7]
R9410	RES_402	m60[94C6]
R9411	RES_402	m60[94C6]
R9450	RES_402	m60[94C2]
R9470	RES_402	m60[94B8]
R9472	RES_402	m60[94B3]
R9473	RES_402	m60[94B2]
R9474	RES_402	m60[94B2]
R9475	RES_402	m60[94B1]
R9490	RES_805	m60[94C6]
R9491	RES_805	m60[94D6]
R9499	RES_402	m60[94C8]
R9700	RES_402	m60[97D7]
R9701	RES_402	m60[97D8]
R9702	RES_402	m60[97D7]
R9703	RES_402	m60[97D7]
R9704	RES_402	m60[97C7]
R9705	RES_402	m60[97C7]
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R9707	RES_402	m60[97C8]
R9708	RES_402	m60[97C7]
R9709	RES_402	m60[97C7]
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R9711	RES_402	m60[97D2]
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R9714	RES_402	m60[97C2]
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R9716	RES_402	m60[97C8]
R9717	RES_402	m60[97C8]
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R9722	RES_402	m60[97C2]
R9740	RES_402	m60[97A8]
R9741	RES_402	m60[97A8]
R9742	RES_402	m60[97A7]
R9750	RES_402	m60[97A3]
R9751	RES_402	m60[97A3]
RP2300	RPAK4P_SM-LF	m60[23D5]
RP3000	RPAK4P_SM-LF	m60[30B4 30C4 30D4 30D4]
RP3001	RPAK4P_SM-LF	m60[30C4 30A4 30A4 30D4]
RP3002	RPAK4P_SM-LF	m60[30A4 30A4 30A4 30D4]
RP3003	RPAK4P_SM-LF	m60[30C4 30C4 30C4 30D4]
RP3004	RPAK4P_SM-LF	m60[30C4 30C4 30D4]
RP3005	RPAK4P_SM-LF	m60[30B4 30A4 30A4 30D4]
RP3006	RPAK4P_SM-LF	m60[30B4 30B4 30A4 30D4]
RP3007	RPAK4P_SM-LF	m60[30C4 30C4 30C4 30C4]
RP3008	RPAK4P_SM-LF	m60[30C4 30C4 30C4 30C4]
RP3009	RPAK4P_SM-LF	m60[30B4 30B4 30C4 30C4]
RP3010	RPAK4P_SM-LF	m60[30B4 30B4 30B4 30B4]
RP3011	RPAK4P_SM-LF	m60[30B4 30A4 30B4 30B4]
RP7200	RPAK4P_SM-LF	m60[72A4]
SDF3800	PCB_STANDOFF	m60[38B2]
SDF3801	PCB_STANDOFF	m60[38A2]
SDF4700	PCB_STANDOFF	m60[47A2]
SDF4701	PCB_STANDOFF	m60[47A2]
SDF5300	PCB_STANDOFF	m60[53A5]
SDF5301	PCB_STANDOFF	m60[53A5]
SDF9400	PCB_STANDOFF	m60[94B6]
SDF9401	PCB_STANDOFF	m60[94A6]
SW2600	SWI_TACT_4SM_EVQPH_S M-LF	m60[26C6]
SW5900	SWI_TACT_4SM_EVQPH_S M-LF	m60[59D8]
SW5901	SWI_TACT_4SM_EVQPH_S M-LF	m60[59B8]
U600	74LC125_TSSOP	m60[6A7 6B7 6B7 6C7]
U1000	ADT7461_MSOP	m60[10D5]
U1200	NB_945GM_BGA	m60[12D5]
U1200	NB_945GM_BGA	m60[13D4]
U1200	NB_945GM_BGA	m60[14D5]
U1200	NB_945GM_BGA	m60[15D3 15D7]
U1200	NB_945GM_BGA	m60[16D2 16C8]
U1200	NB_945GM_BGA	m60[17D5]
U1200	NB_945GM_BGA	m60[18D4 18D7]
U2100	SB_ICH7M_BGA	m60[21D6]
U2100	SB_ICH7M_BGA	m60[22B7 22D3]
U2100	SB_ICH7M_BGA	m60[23D4]
U2100	SB_ICH7M_BGA	m60[24D4 24D7]
U2601	MC74VHC1G08_SOT23-5-LF	m60[26D5]
U2603	SN74LVC1G04_SOT23-5	m60[26A7]
U2698	MC74VHC1G08_SOT23-5-LF	m60[26C4]
U2699	MAX6816_SOT143	m60[26C5]
U3100	LREG_BD3533FVM_MSOP-8	m60[31C5]
U3301	CLK_GEN_CY284455_QFN	m60[33C5]
U4101	88E8053_QFN	m60[41D5]
U4102	EEPROM_M24C08_SO8	m60[41A3]
U4400	FW32306_TQFP	m60[44D5]
U4700	SWI_TPS2043_SOI	m60[47C8]
U5700	ISL6549_QFN	m60[57D6]
U5800	SMC_H8S2116_BGA	m60[58A8 58C3 58C6 58D6]
U5900	VDET_RN5VD_SOT23-5	m60[59D8]
U5940	VREF_REF3133_SOT23-3	m60[59A4]
U5999	COMPARATOR_LM393_SOI -1-LF	m60[59A8 59A8]
U6100	MAX6695_UMAX	m60[61C4]
U6301	FLASH_SST25VF016B_SOI	m60[63D3]
U6700	TPM_TSSOP	m60[67C5]
U6800	AUDIO_STAC9220_LQFP	m60[68D5]
U7200	MAX9714_QFN-LF	m60[72C5]
U7400	MAX9890_UCSP1	m60[74C4]
U7500	ISL6262_QFN	m60[75C6]
U7501	ZXCT1010_SOT23-5	m60[76D7]
U7710	MC74VHC1G08_SOT23-5-LF	m60[77C7]
U7711	MC74VHC1G08_SOT23-5-LF	m60[77B7]
U7712	MC74VHC1G08_SOT23-5-LF	m60[77B7]
U7750	SN200505068_SOP	m60[77C4]
U7800	ISL6549_QFN	m60[78C7]
U7900	ISL6549_QFN	m60[79D6]
U7901	COMPARATOR_LM339A_SO I-LF	m60[79A5]
U7901	COMPARATOR_LM339A_SO I-LF	m60[80A4]
U7901	COMPARATOR_LM339A_SO I-LF	m60[81A5]
U7910	COMPARATOR_LM339A_SO I-LF	m60[79A3]
U7910	COMPARATOR_LM339A_SO I-LF	m60[80B2]
U7910	COMPARATOR_LM339A_SO I-LF	m60[81B3]
U7910	COMPARATOR_LM339A_SO I-LF	m60[83B3]
U8000	ISL6549_QFN	m60[80D6]
U8100	ISL6549_QFN	m60[81D6]
U8200	ISL6549_QFN	m60[82D6]
U8400	ATI_M56P_BGA	m60[84C8 84D4]
U8400	ATI_M56P_BGA	m60[86D4]
U8400	ATI_M56P_BGA	m60[87D2 87D6]
U8400	ATI_M56P_BGA	m60[91D4]
U8400	ATI_M56P_BGA	m60[93C4]
U8500	ISL6269_QFN	m60[85D6]
U8595	OPAMP_LMV2011_SOT23-5	m60[85D2]
U8900	SGRAM_16MX32_GDDR3_1 36H_FBGA	m60[89D6 89B6]
U8950	SGRAM_16MX32_GDDR3_1 36H_FBGA	m60[89D3 89B3]
U9000	SGRAM_16MX32_GDDR3_1 36_FBGA	m60[90D6 90B6]
U9050	SGRAM_16MX32_GDDR3_1 36_FBGA	m60[90D3 90B3]
U9470	MC74VHC1G08_SOT23-5-LF	m60[94B2]
U9700	74LC125_TSSOP	m60[6A8 6A6]
U9700	74LC125_TSSOP	m60[97A4 97A4]
XC7200	MTGHOLE	m60[72B3]
XW602	SHORT_SM	m60[6C2]
XW605	SHORT_SM	m60[6A5]
XW5800	SHORT_SM	m60[58B3]
XW5900	SHORT_SM	m60[59B1]
XW7201	SHORT_SM	m60[72B2]
XW7300	SHORT_SM	m60[73C3]
XW7400	SHORT_SM	m60[74A4]
XW7429	SHORT_SM	m60[74C2]
XW7441	SHORT_SM	m60[74D2]
XW7500	SHORT_SM	m60[75A6]
XW7501	SHORT_SM	m60[75B2]
XW7502	SHORT_SM	m60[75B1]
XW7503	SHORT_SM	m60[75D2]
XW7504	SHORT_SM	m60[75D1]
XW7598	SHORT_SM	m60[76D7]
XW7750	SHORT_SM	m60[77A4]
XW8500	SHORT_SM	m60[85C6]
Y2600	CRYSTAL_4PIN_SM-LF	m60[26D8]
Y3301	CRYSTAL_5X3.2-SM	m60[33C7]
Y4101	CRYSTAL_SM-3-LF	m60[41B5]
Y4400	CRYSTAL_HC49-USMD	m60[44D2]
Y5800	CRYSTAL_SM-3	m60[59B8]
Y6700	CRYSTAL_4PIN_SM-LF	m60[59B7]
ZH500	HOLE_VIA	m60[5C1]
ZH501	HOLE_VIA	m60[5C1]
ZH502	HOLE_VIA	m60[5C1]
ZH503	HOLE_VIA	m60[5C1]
ZH504	HOLE_VIA	m60[5B1]
ZH505	HOLE_VIA	m60[5B1]
ZH506	HOLE_VIA	m60[5B1]
ZH507	HOLE_VIA	m60[5B1]
ZH508	HOLE_VIA	m60[5B1]
ZH509	HOLE_VIA	m60[5B1]
ZH510	HOLE_VIA	m60[5C1]
ZH511	HOLE_VIA	m60[5C1]
ZH512	HOLE_VIA	m60[5C1]
ZH513	HOLE_VIA	m60[5C1]
ZH514	HOLE_VIA	m60[5B1]
ZH515	HOLE_VIA	m60[5B1]
ZH516	HOLE_VIA	m60[5B1]
ZH517	HOLE_VIA	m60[5B1]
ZH518	HOLE_VIA	m60[5B1]
ZH519	HOLE_VIA	m60[5B1]
ZH520	HOLE_VIA	m60[5C1]
ZH521	HOLE_VIA	m60[5C1]
ZH522	HOLE_VIA	m60[5C1]
ZH523	HOLE_VIA	m60[5C1]
ZH524	HOLE_VIA	m60[5B1]
ZH525	HOLE_VIA	m60[5B1]
ZH526	HOLE_VIA	m60[5B1]
ZH527	HOLE_VIA	m60[5B1]
ZH528	HOLE_VIA	m60[5B1]
ZH529	HOLE_VIA	m60[5B1]
ZH601	MTGHOLE	m60[6A3]
ZH602	MTGHOLE	m60[6A3]
ZH603	MTGHOLE	m60[6A3]
ZH606	MTGHOLE	m60[6A1]
ZH607	MTGHOLE	m60[9D4]

ZH608	MTGHOLE	m60[9D3]
ZH609	MTGHOLE	m60[9D2]
ZH610	MTGHOLE	m60[9D2]