

M39 - DVT

12/07/05

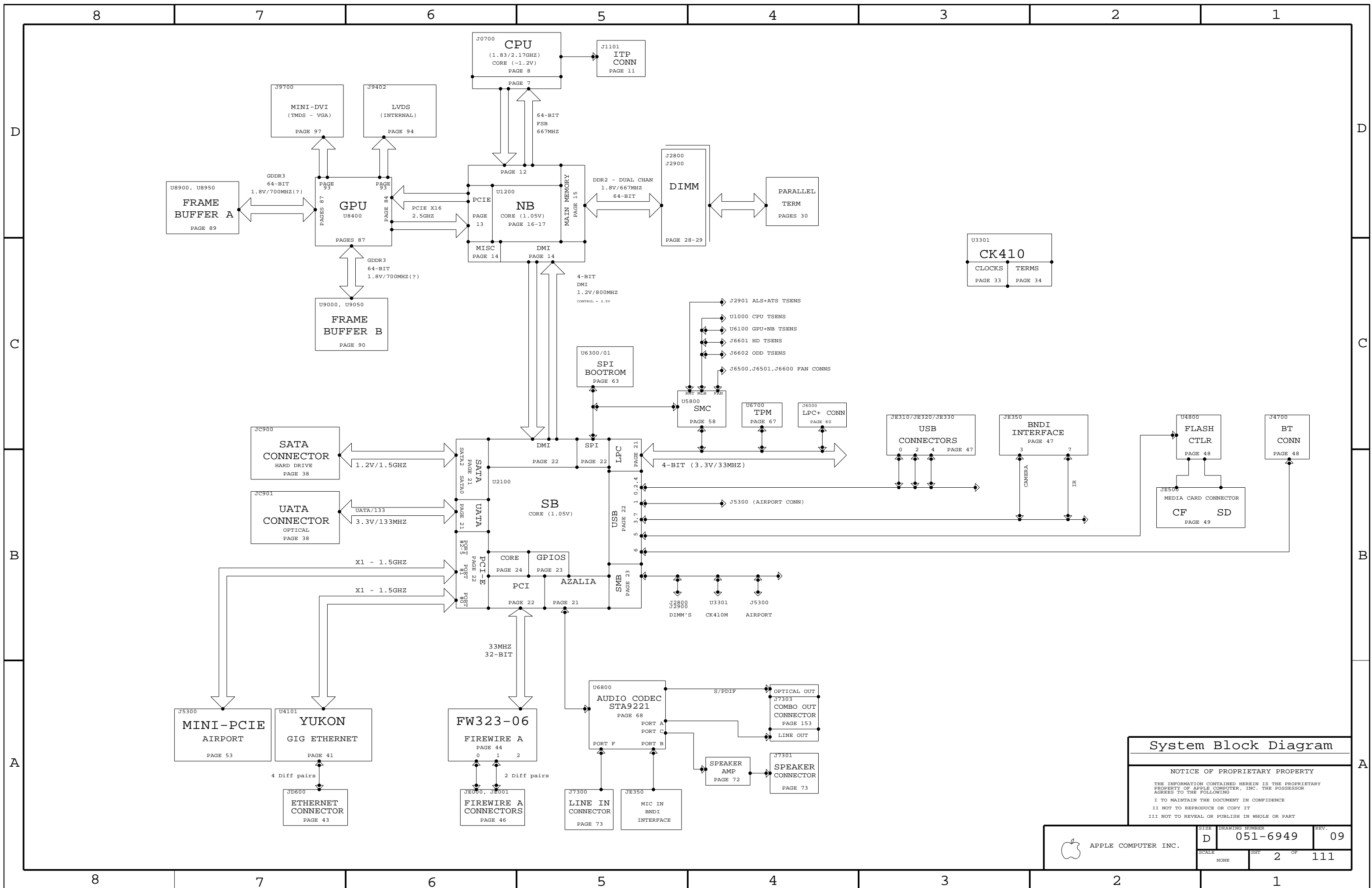
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
06		400374	ENGINEERING RELEASED	09/16/05	06/22/04

PAGE	DRI	PDF	CIRCUIT
1	JD	JD	1 TABLE OF CONTENTS
2	JD	JD	2 SYSTEM BLOCK DIAGRAM
3	RT	RT	3 POWER BLOCK DIAGRAM
4	JD	JD	4 TABLE ITEMS & REVISION HISTORY
5	JD	JD	5 FUNC TEST
6	RT	RT	6 POWER CONNECTOR / POWER ALIAS
(M42) 7	MS	JD	7 CPU - BUS INTERFACE
(M42) 8	MS	JD	8 CPU - PWR & GND
9	MS	JD	9 CPU - DECAPS
(M42) 10	MS	JD	10 CPU - THERMAL SENSOR
M42 11	MS	JD	11 CPU - ITP CONN
M1 12	PS	JH	12 NB - CPU INTERFACE
M1 13	PS	JH	13 NB - VIDEO INTERFACE
14	PS	JH	14 NB - MISC INTERFACES
M1 15	PS	JH	15 NB - DDR2 INTERFACE
M1 16	PS	JH	16 NB - POWER 1
M1 17	PS	JH	17 NB - POWER 2
M1 18	PS	JH	18 NB - GROUNDS
19	PS	JH	19 NB - DECAPS
M1 20	PS	JH	20 NB - CONFIG STRAPS
21	JD	JD	21 SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	JD	22 SB - PCIE, SPI, USB, DMI, PCI
23	JD	JD	23 SB - SMB, GPIO, PM, CLKS
24	JD	JD	24 SB - POWERS AND GROUNDS
25	JD	JD	25 SB - DECAPS
26	JD	JD	26 SB - MISC
27	JD	JD	27 SB - SMB BUS CONNECTIONS
28	PS	JD	28 DDR2 - SO-DIMM CONN A
29	PS	JD	29 DDR2 - SO-DIMM CONN B (REVERSED)
30	PS	JD	30 DDR2 - TERMINATION
M1 31	RT	RT	31 DDR2 - VTT SUPPLY
M42 33	JD	JD	33 CLOCKS - GENERATOR
34	JD	JD	34 CLOCKS - TERMINATIONS
38	JD	JD	38 ATA (SATA AND IDE) CONN'S
(M42) 41	JD	JD	41 LAN - YUKON'S PCIE INTERFACE
42	JD	JD	42 LAN - YUKON'S PWR, MISC
43	JD	JD	43 LAN - CONN
44	JD	JD	44 FIREWIRE - FW323-06
45	JD	JD	45 FIREWIRE - DECAPS
46	JD	JD	46 FIREWIRE - CONN'S
47	JD	JD	47 USB - CONN'S
49	JD	JD	49 USB - FLASH CONN

PAGE	DRI	PDF	CIRCUIT
53	JD	JD	43 PCI-E - AIRPORT MINI-PCIE CONN
54	JD	JD	44 PCI-E - UNUSED PORTS
58	MS	MS	45 SMC - H8S2116
59	MS	MS	46 SMC - SMB BUSSES, MISC
60	MS	MS	47 SMC - LPC+ CONN
61	JH	JH	48 SMC - GPU/NB THERMAL SENSOR
RX 63	MS	JD	49 SMC - SPI BOOTROM
65	MS	MS	50 SMC - FANS
66	MS	MS	51 SMC - FANS
67	JD	JD	52 SMC - TPM
SO 68	PT	JD	53 AUDIO - CODEC, VREG, MIC BIAS
SO 72	PT	JD	54 AUDIO - INTERNAL SPEAKER AMP
SO 73	PT	JD	55 AUDIO - I/O CONN'S, EMC
SO 74	PT	JD	56 AUDIO - DETECT TRANSLATORS
RP 75	RT	RT	57 VR - CPU CORE
RP 76	RT	RT	58 VR - CPU I-V SENSE CKT
RP 77	RT	RT	59 VR - "S0" 1.2V & 2.5V (GRAFIX)
RP 78	RT	RT	60 VR - "S0" 1.8V
RP 79	RT	RT	61 VR - "S3" 1.8V
RP 80	RT	RT	62 VR - "S0" 1.5V
RP 81	RT	RT	63 VR - "S0" 1.05V
RP 83	RT	RT	64 VR - "S3" 3.3V AND 5V
JH 84	JH	JH	65 GPU - M56 PCI-E
M1 85	JH	JH	66 GPU - VCORE SUPPLY
M1 86	JH	JH	67 GPU - M56 CORE PWR
M1 87	JH	JH	68 GPU - M56 FRAME BUFFER
M1 88	JH	JH	69 GPU - MISC
M1 89	JH	JH	70 GPU - GDDR SDRAM A
M1 90	JH	JH	71 GPU - GDDR SDRAM B
M1 91	JH	JH	72 GPU - M56 GPIO, DVO, MISC
M1 92	JH	JH	73 GPU - M56 CLOCKS
M1 93	JH	JH	74 GPU - M56 VIDEO INTERFACES
JH 94	JH	JH	75 GPU - INTERNAL DISPLAY CONN'S
JH 95	JH	JH	76 GPU - TP'S
JH 96	JH	JH	77 GPU - TMDS, INVERTER, EXT VGA
JH 97	JH	JH	78 GPU - EXTERNAL DISPLAY CONN'S

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center; font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<p>Apple Computer Inc.</p>																
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<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAFTER</td> <td style="width: 25%;">DESIGN CR</td> <td style="width: 25%;">MFG APPD</td> <td style="width: 25%;">TITLE</td> </tr> <tr> <td style="width: 25%;">ENG APPD</td> <td style="width: 25%;">DESIGNER</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">NONE</td> </tr> <tr> <td style="width: 25%;">QA APPD</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">NONE</td> <td style="width: 25%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> </tr> <tr> <td style="width: 25%;">RELEASE</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">NONE</td> <td style="width: 25%;">SIZE D</td> </tr> </table>		DRAFTER	DESIGN CR	MFG APPD	TITLE	ENG APPD	DESIGNER	SCALE	NONE	QA APPD	SCALE	NONE	MATERIAL/FINISH NOTED AS APPLICABLE	RELEASE	SCALE	NONE	SIZE D	<p style="font-size: large; font-weight: bold;">SCHEM, M39</p>
DRAFTER	DESIGN CR	MFG APPD	TITLE															
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QA APPD	SCALE	NONE	MATERIAL/FINISH NOTED AS APPLICABLE															
RELEASE	SCALE	NONE	SIZE D															
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">DRAWING NUMBER</td> <td style="width: 30%;">REV.</td> </tr> <tr> <td style="text-align: center; font-size: large;">051-6950</td> <td style="text-align: center; font-size: large;">06</td> </tr> </table>		DRAWING NUMBER	REV.	051-6950	06	<p>SHT 1 OF 111</p>												
DRAWING NUMBER	REV.																	
051-6950	06																	



System Block Diagram

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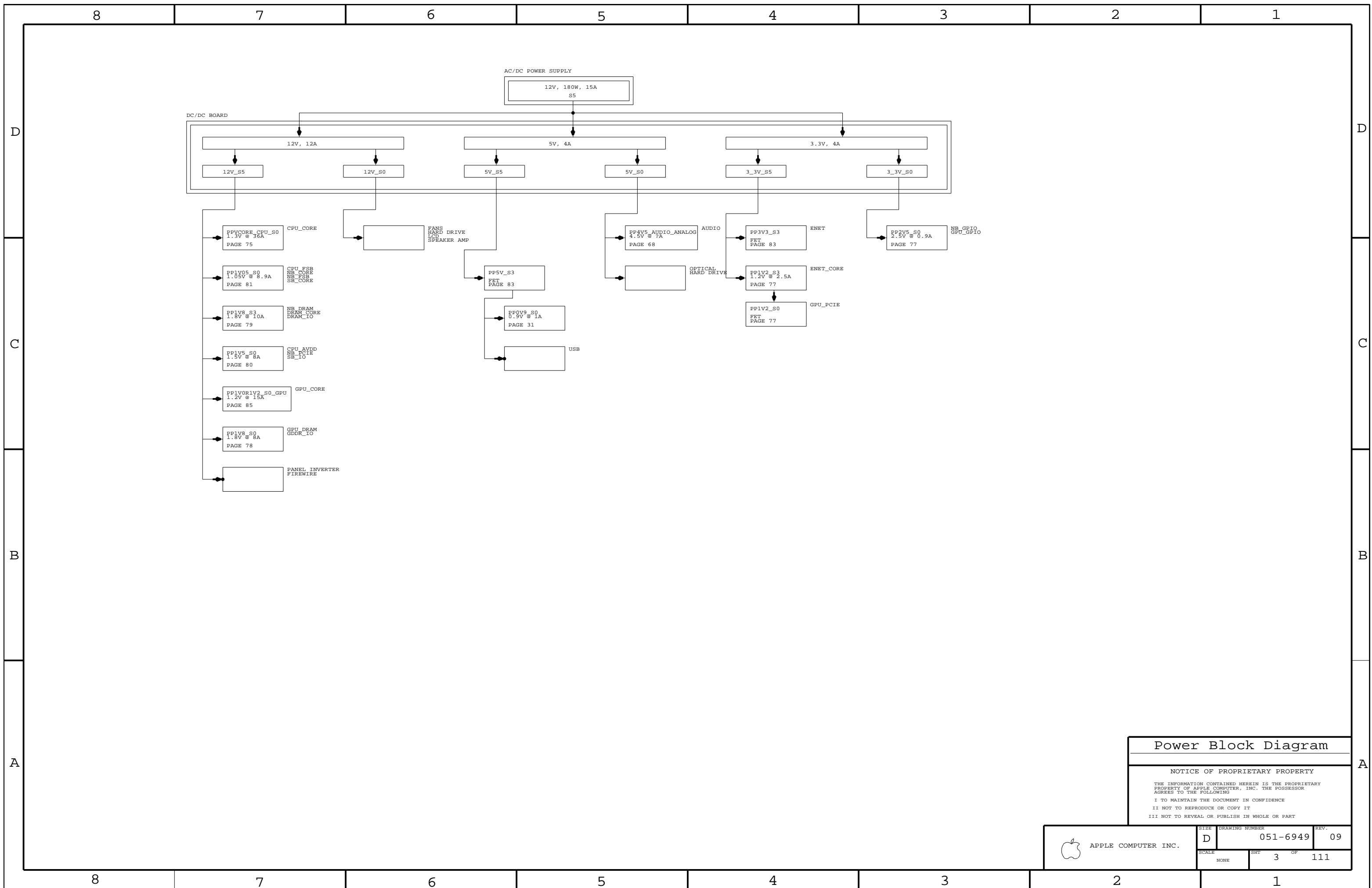
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Power Block Diagram

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NONE	3	111	

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1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,888053,1GIGABIT ETH XVR,64P QFN,BD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274	1	IC,SMC,HSS/2116,BLANK	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	
338S0266	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_B24
338S0305	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_A24
128S0078	3	CAP,EL,AL,330UF,20A,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	
825-6402	1	LBL,SERIAL NUMBER	X14	CRITICAL	

M38

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6949	1	PCB,SCHEM,MLB,M38	SCH1		17_INCH_LCD
820-1919	1	PCB,FAB,MLB,M38	MLB1		17_INCH_LCD
(335S0384) 341T0003	1	EFI ROM,M38	U6301	CRITICAL	17_INCH_LCD
114S0287	1	5.11K,1%,1/16W,402,MF-LF	R8522		17_INCH_LCD
337S3242	1	M00-SPEED CPU (QINZ)	CPU	CRITICAL	CPU_M00
337S3241	1	M38/M39 LOW-SPEED CPU (QINY)	CPU	CRITICAL	CPU_M38

M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6950	1	PCB,SCHEM,MLB,M39	SCH1		20_INCH_LCD
820-1888	1	PCB,FAB,MLB,M39	MLB1		20_INCH_LCD
(335S0384) 341T0004	1	EFI ROM,M39	U6301	CRITICAL	20_INCH_LCD
114S0276	1	4.02K,1%,1/16W,402,MF-LF	R8522		20_INCH_LCD
337S3243	1	M39 HI-SPEED CPU (QHJY)	CPU	CRITICAL	CPU_M39

M38 / M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX

M39 - CTO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16C680EX 680UF 16V LFP
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330F8 330UF 6.3V LFP
128S0080	128S0078		C7517,C7518,C7910	SANYO 160VP330W 330UF 16V SMD LFP
338S0309	338S0266		U8400	IC,ATI,M56LP,GRAFIX CTLR,880PBGA,LF
197S0177	197S0020		Y4101	XTAL,25MHZ,50PFM,16PF,3.2X2.5 SMD,LF

124-0338 124-0333 C7501,C8014 CAP,AL,EL,680UF,16V,RAD,10X12.5MM

Table Items

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SCALE	SHT		OF
NONE	4		111

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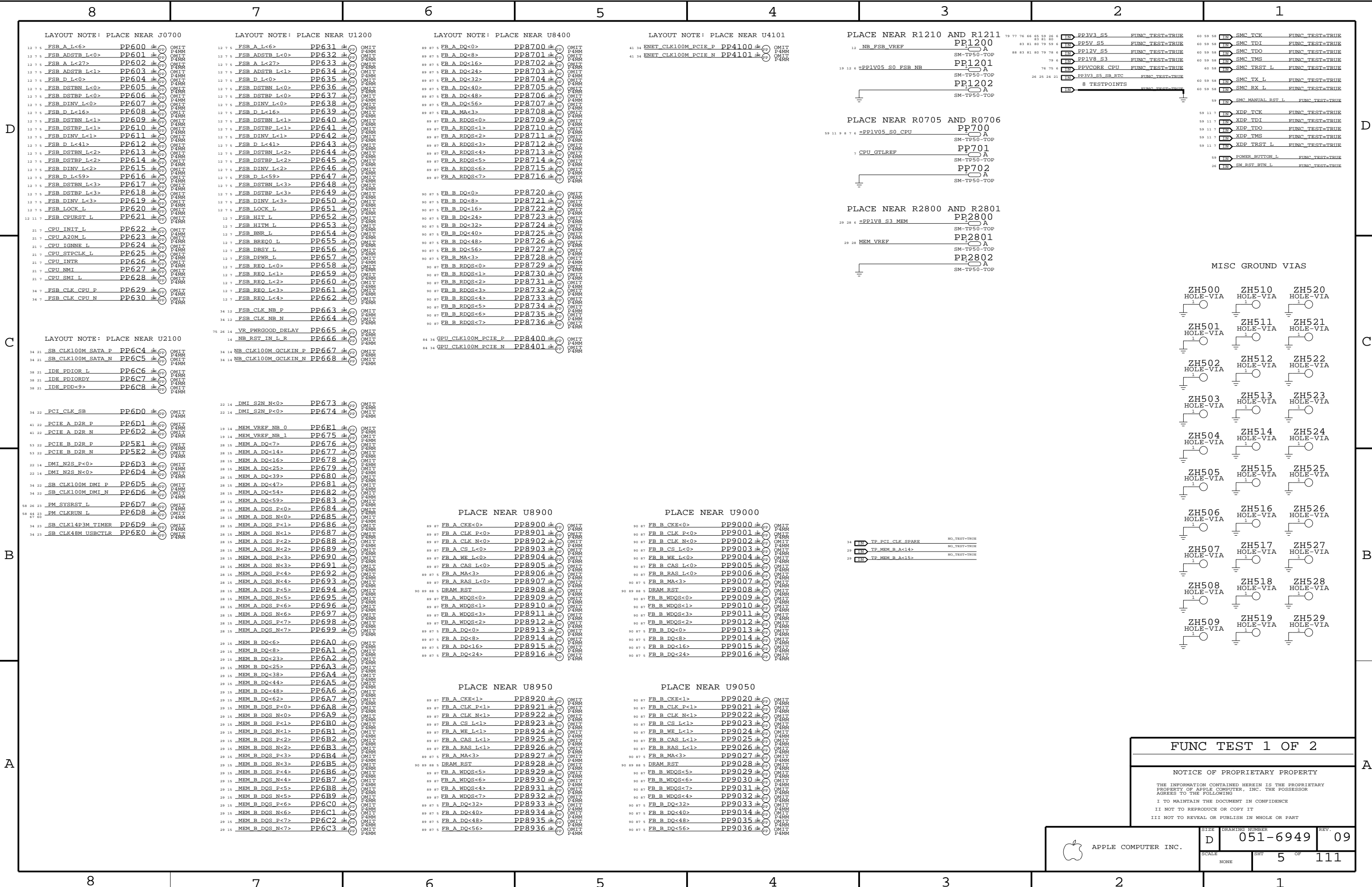
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1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS

LAYOUT NOTE: PLACE NEAR U2100

PLACE NEAR U8900

PLACE NEAR U9000

PLACE NEAR U8950

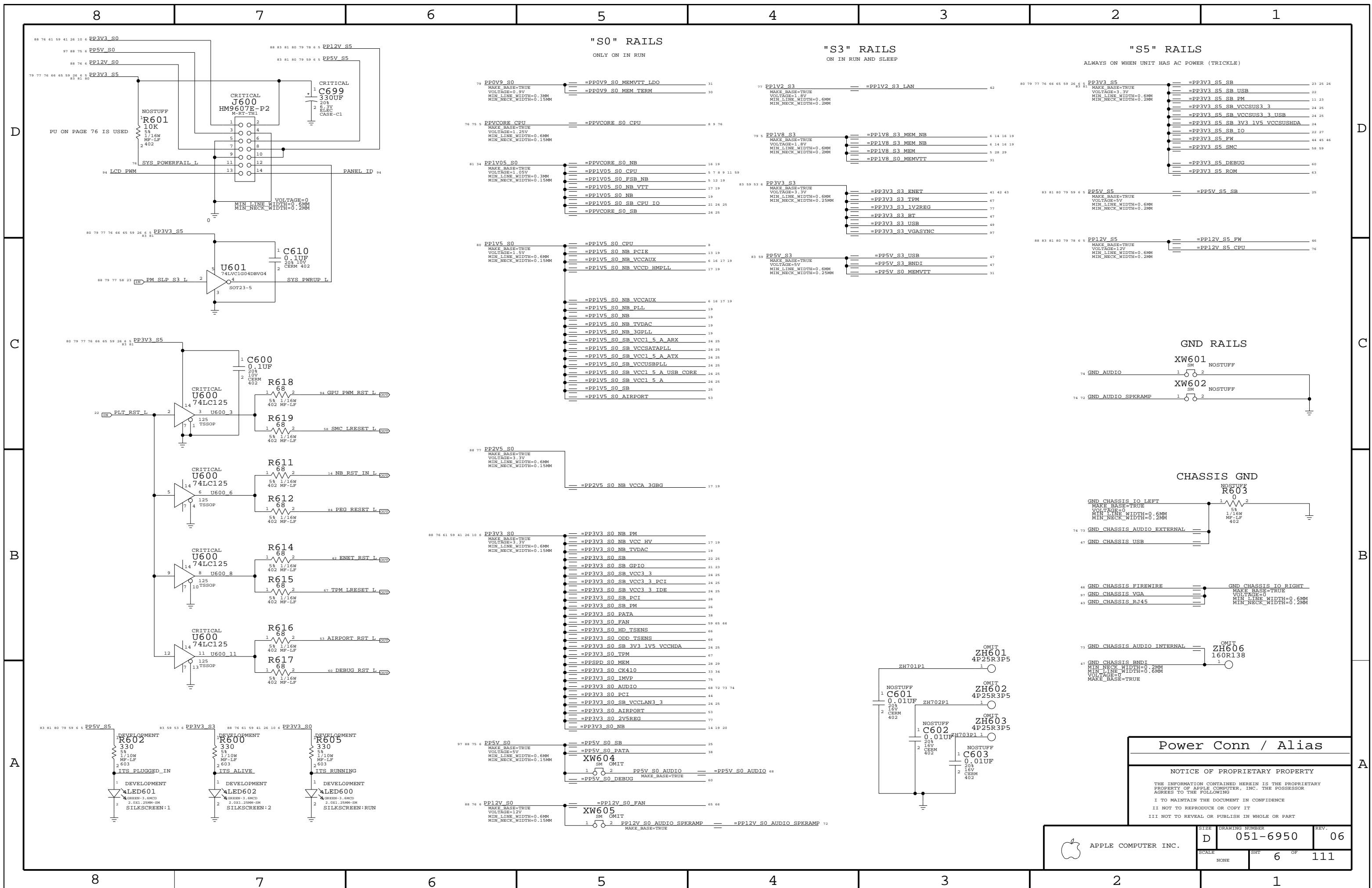
PLACE NEAR U9050

FUNC TEST 1 OF 2

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"S0" RAILS
ONLY ON IN RUN

"S3" RAILS
ON IN RUN AND SLEEP

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

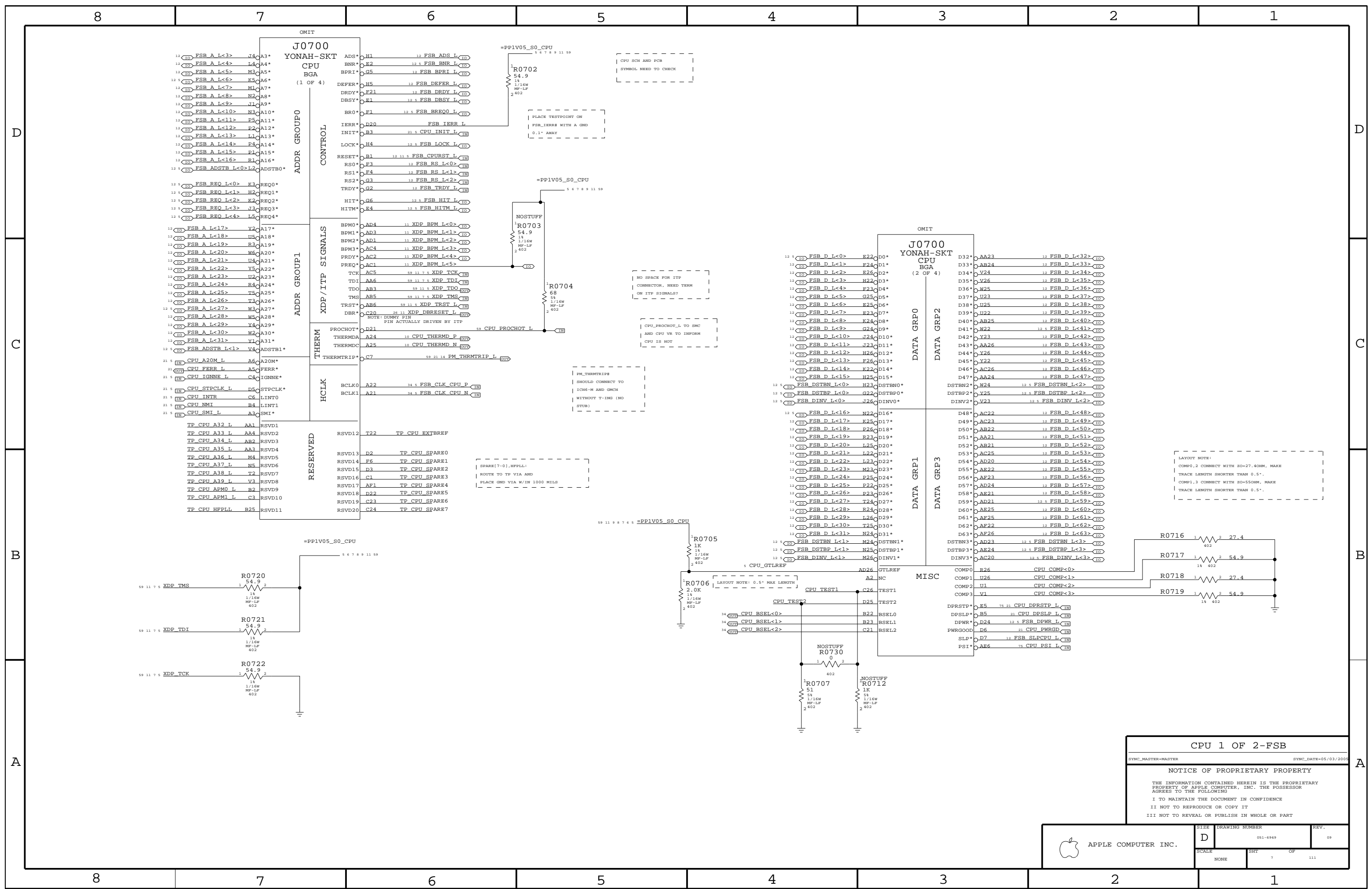
CHASSIS GND

Power Conn / Alias

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NONE			



CPU 1 OF 2-FSB

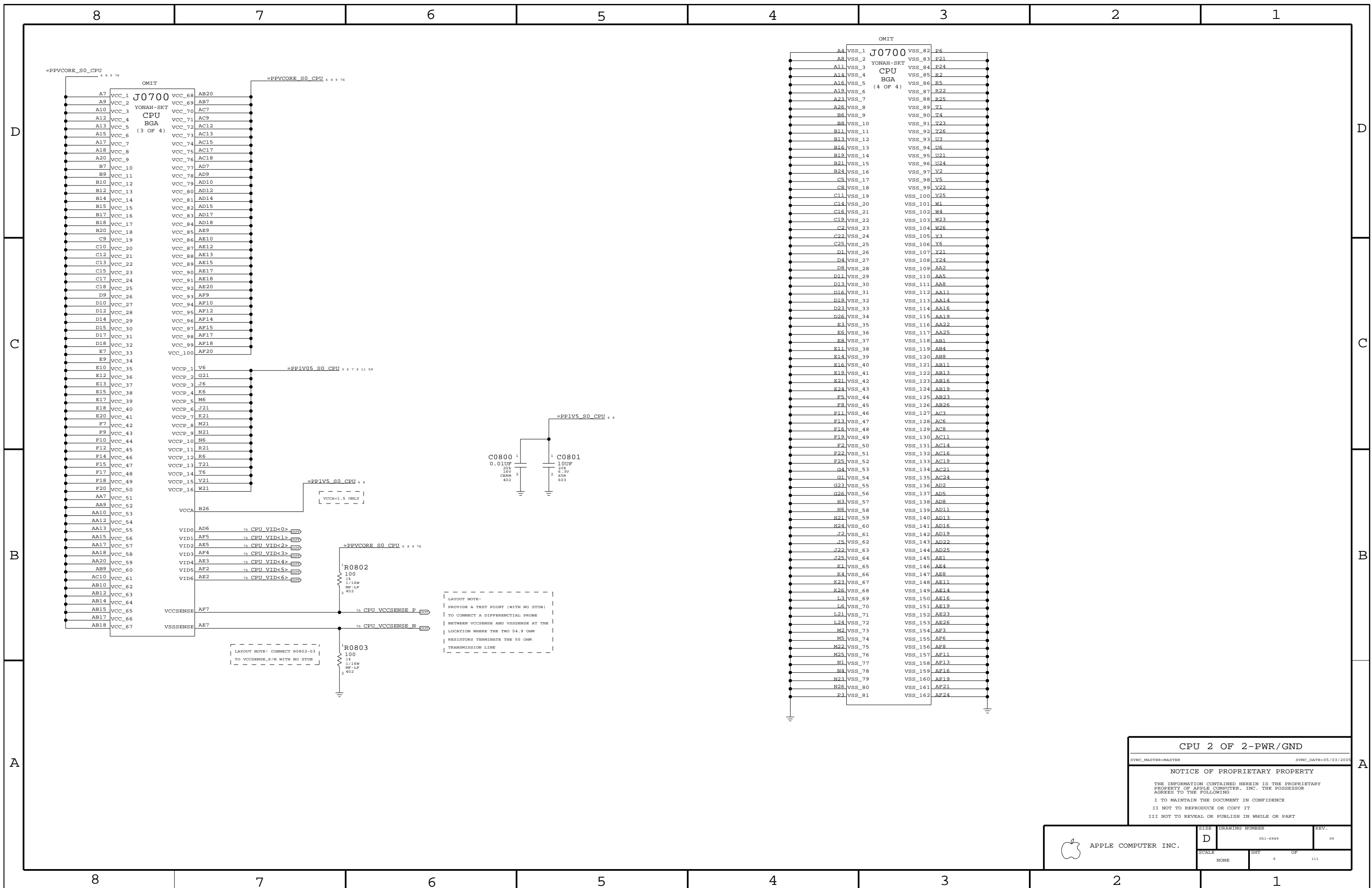
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NONE		7	111



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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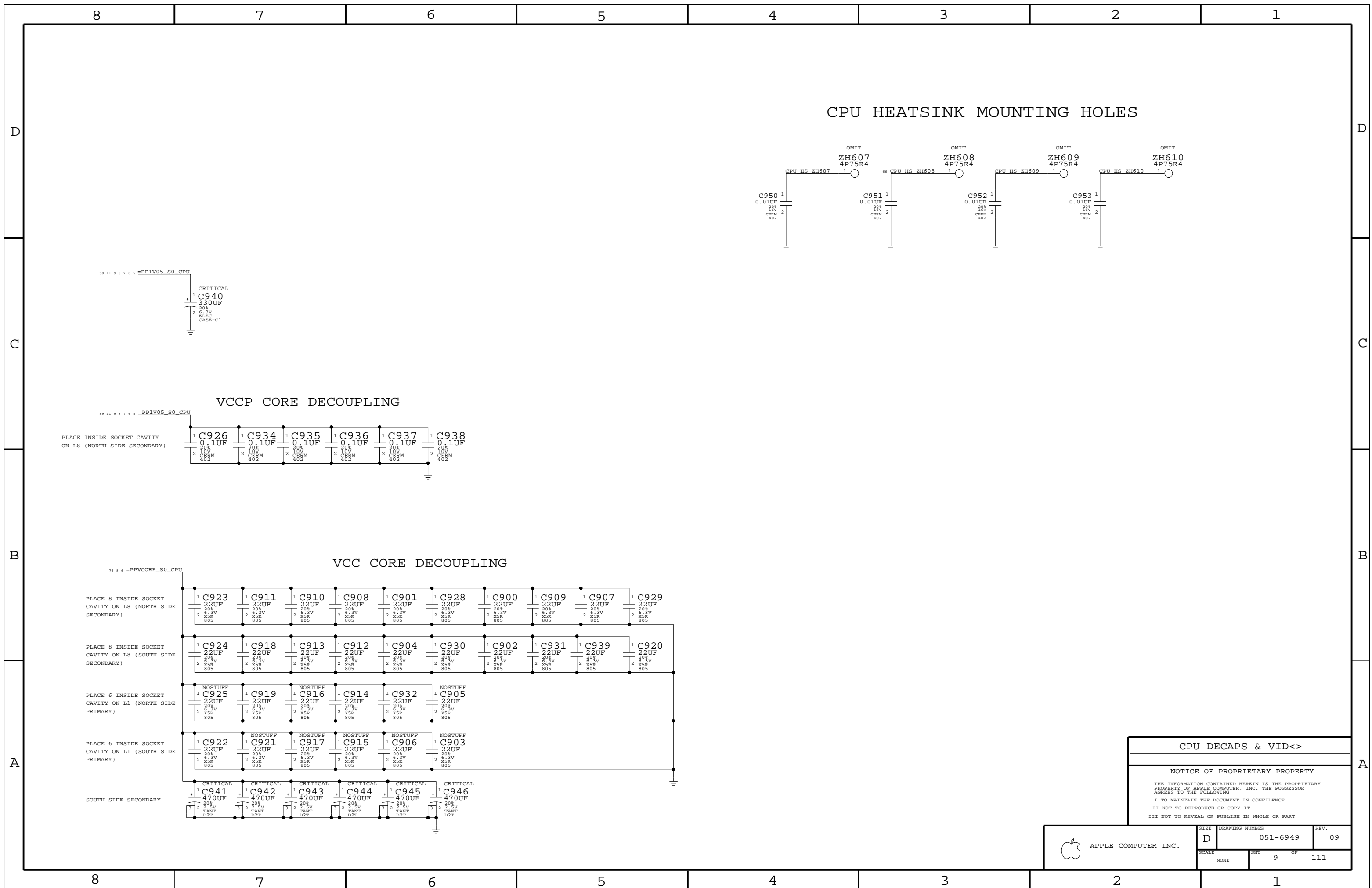
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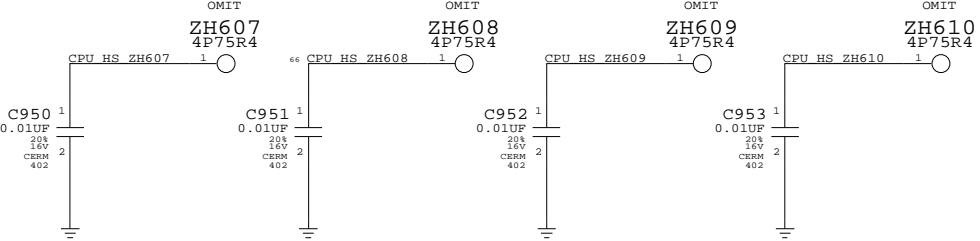
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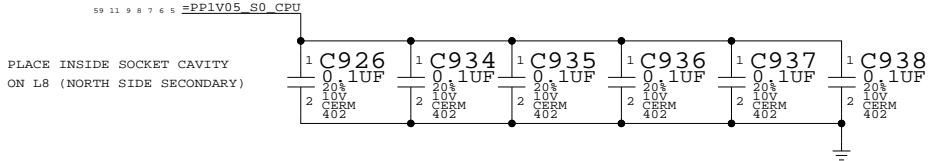
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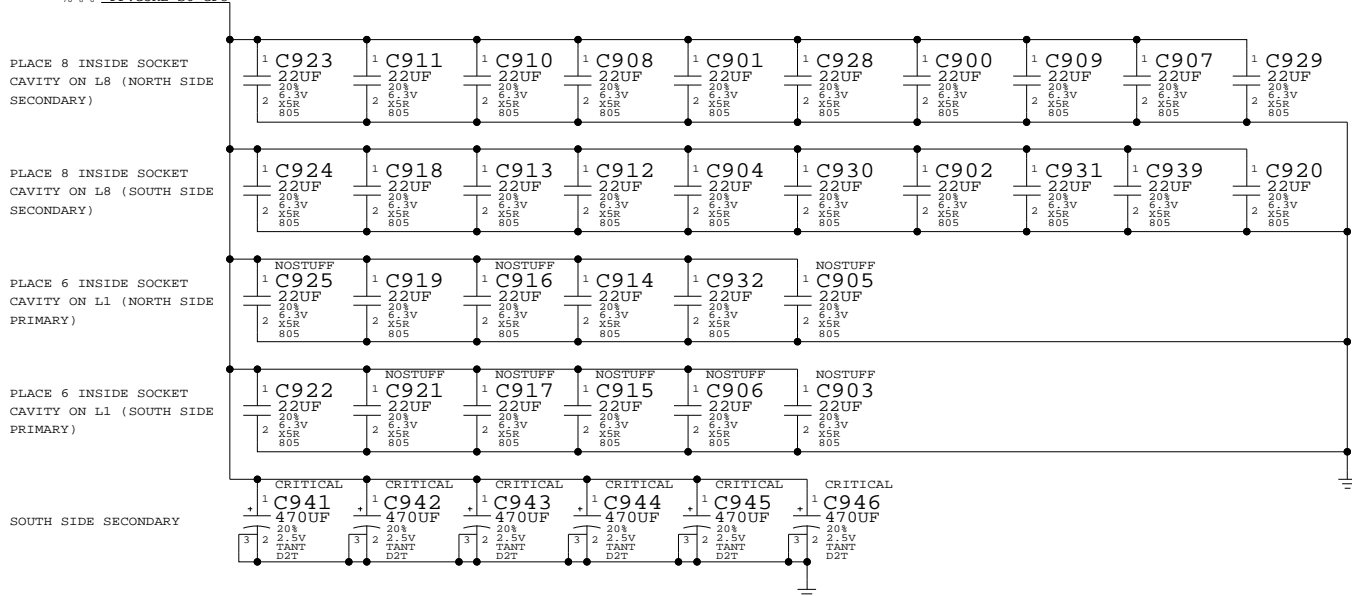
CPU HEATSINK MOUNTING HOLES



VCC CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

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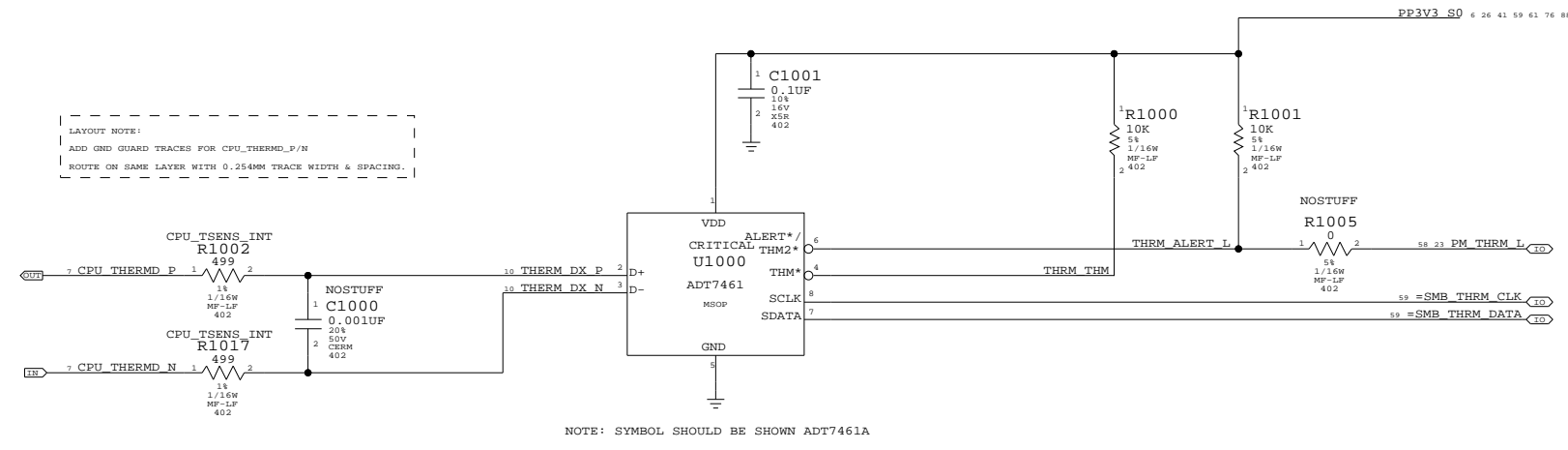
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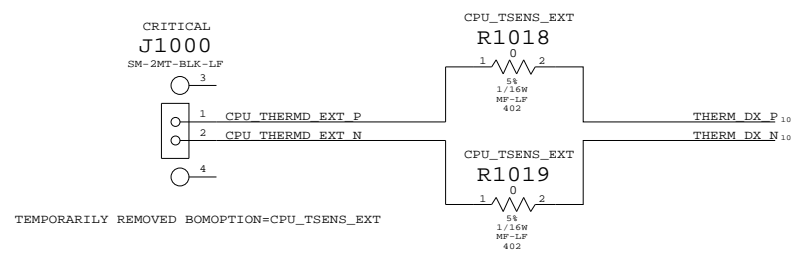
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT 9 OF 111		
NONE			

CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

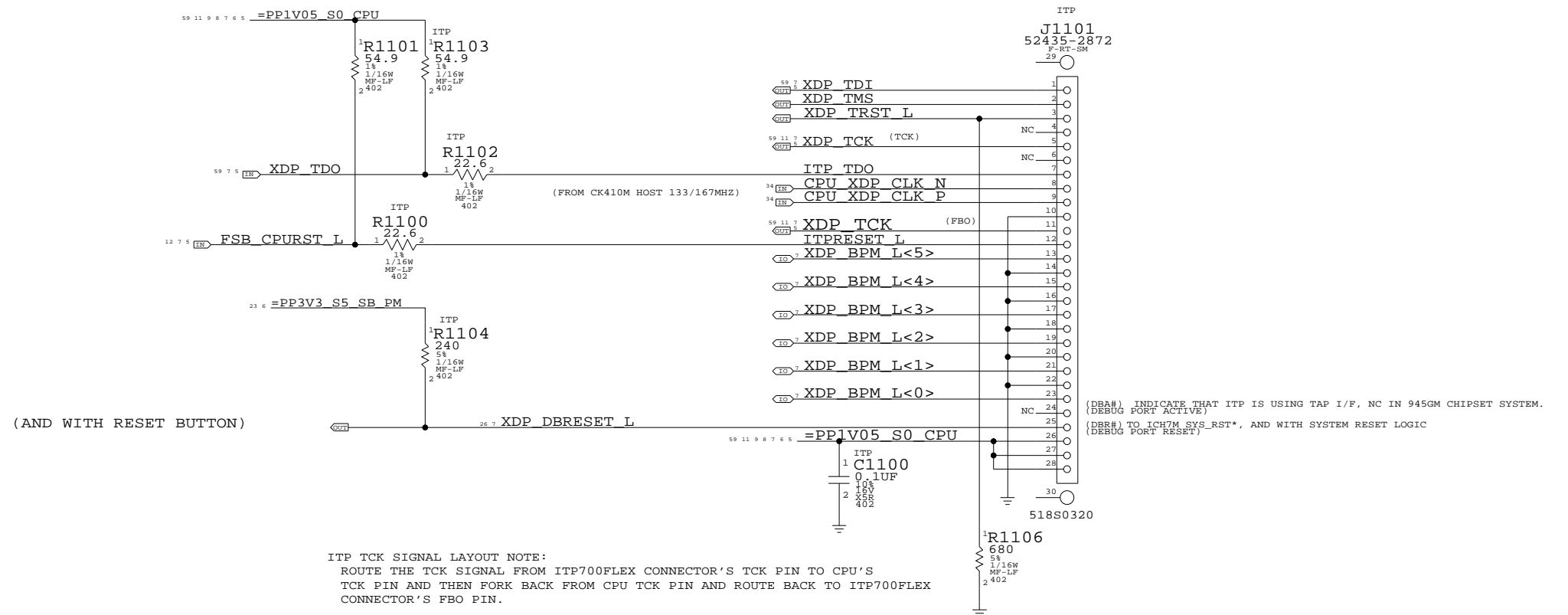
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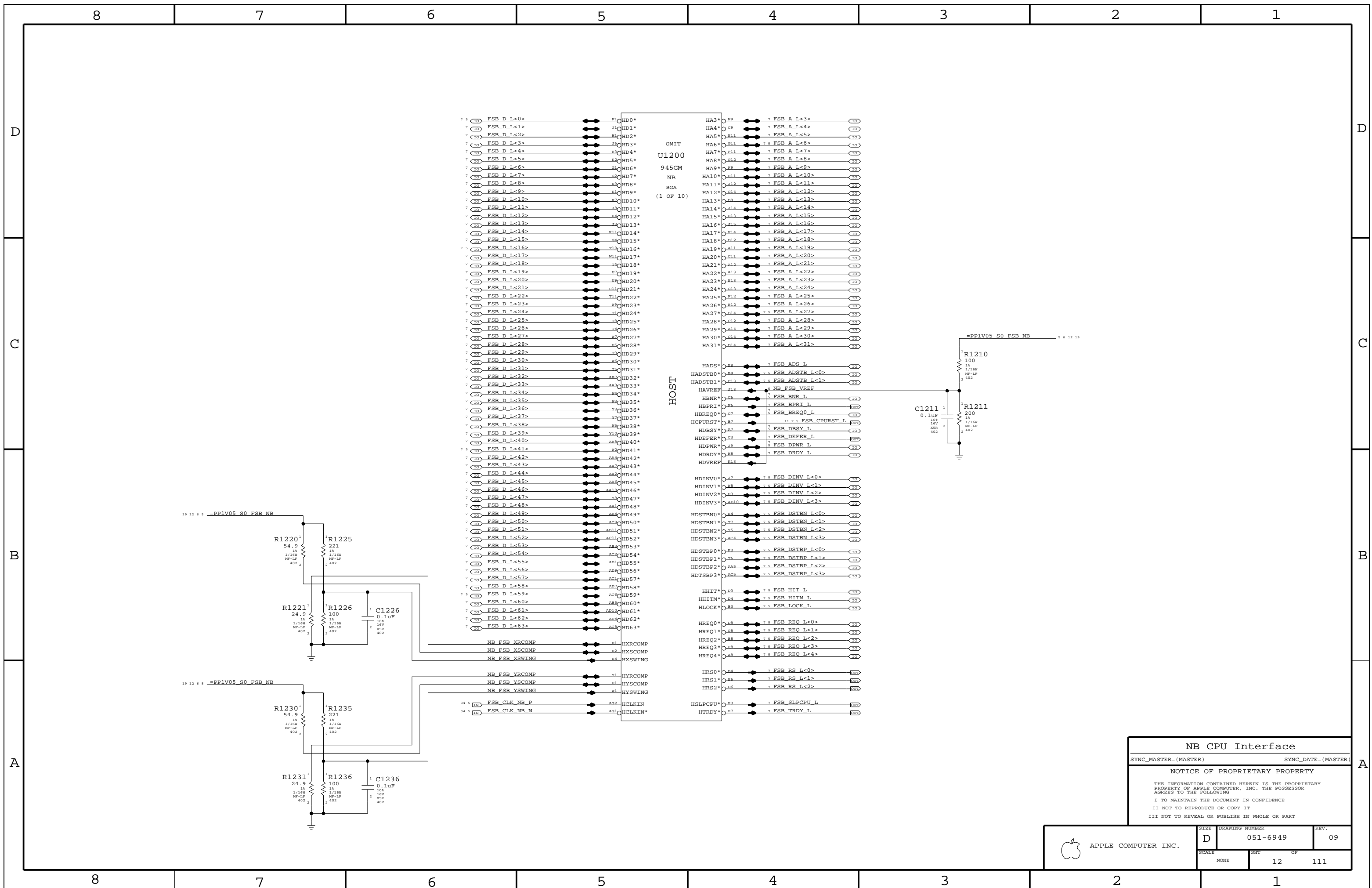
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NONE	10		

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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SCALE	SHT	OF	111
NONE	11		



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

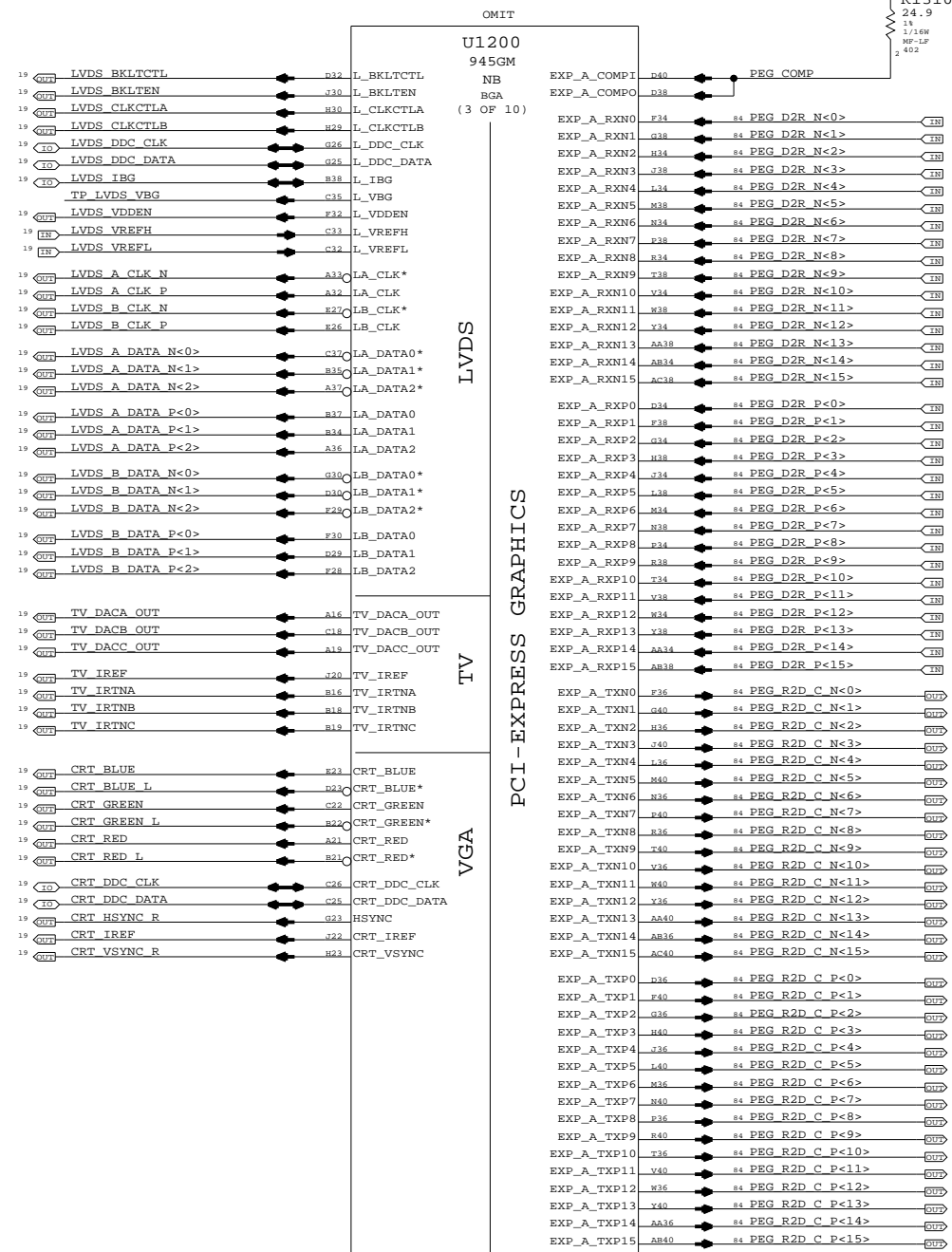
Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_RED#
 SDVO_GREEN#
 SDVO_BLUE#
 SDVO_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

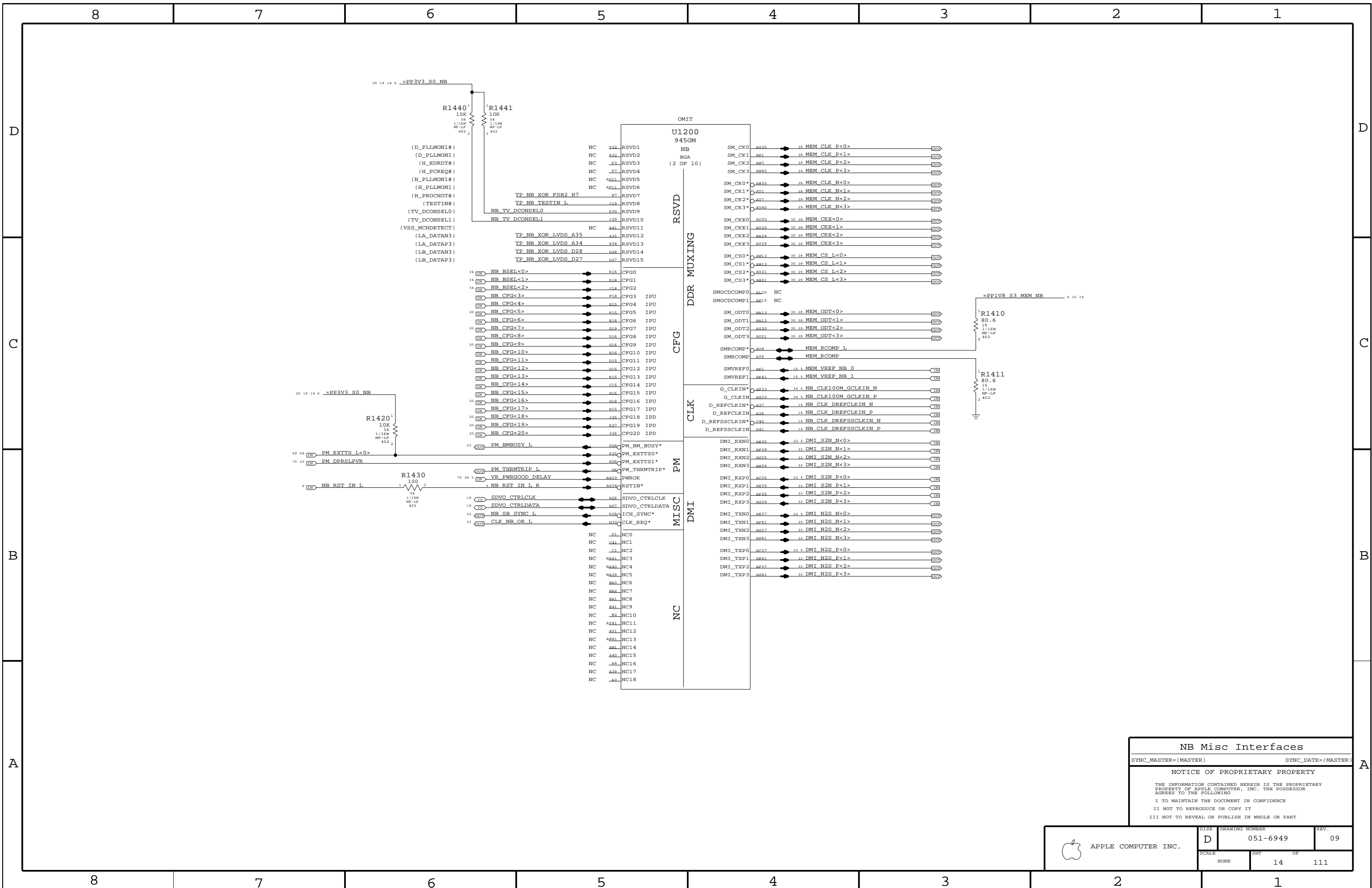
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	13	111	



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

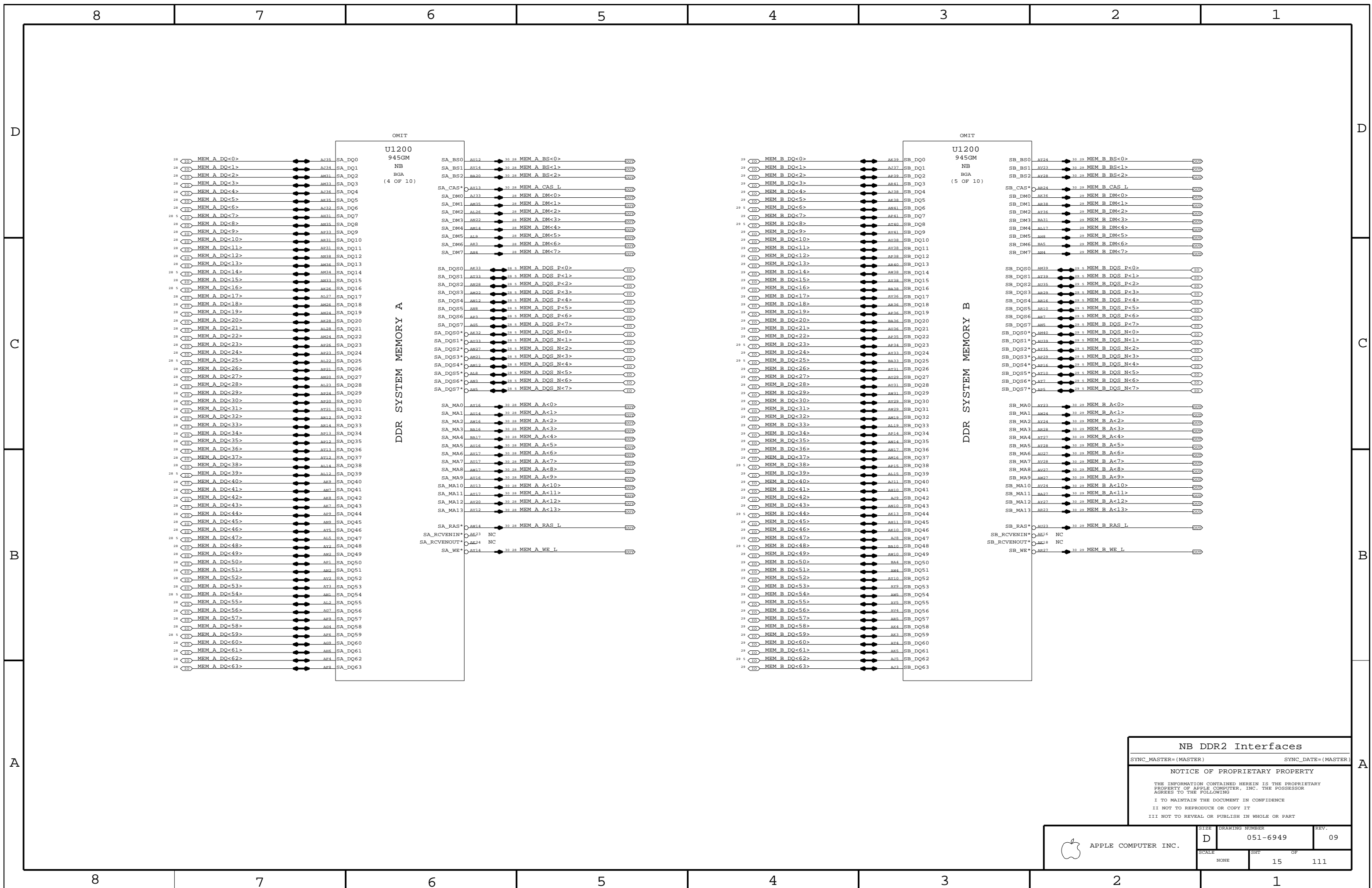
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6949	REV.: 09
	SCALE: NONE	SHEET: 14	OF: 111



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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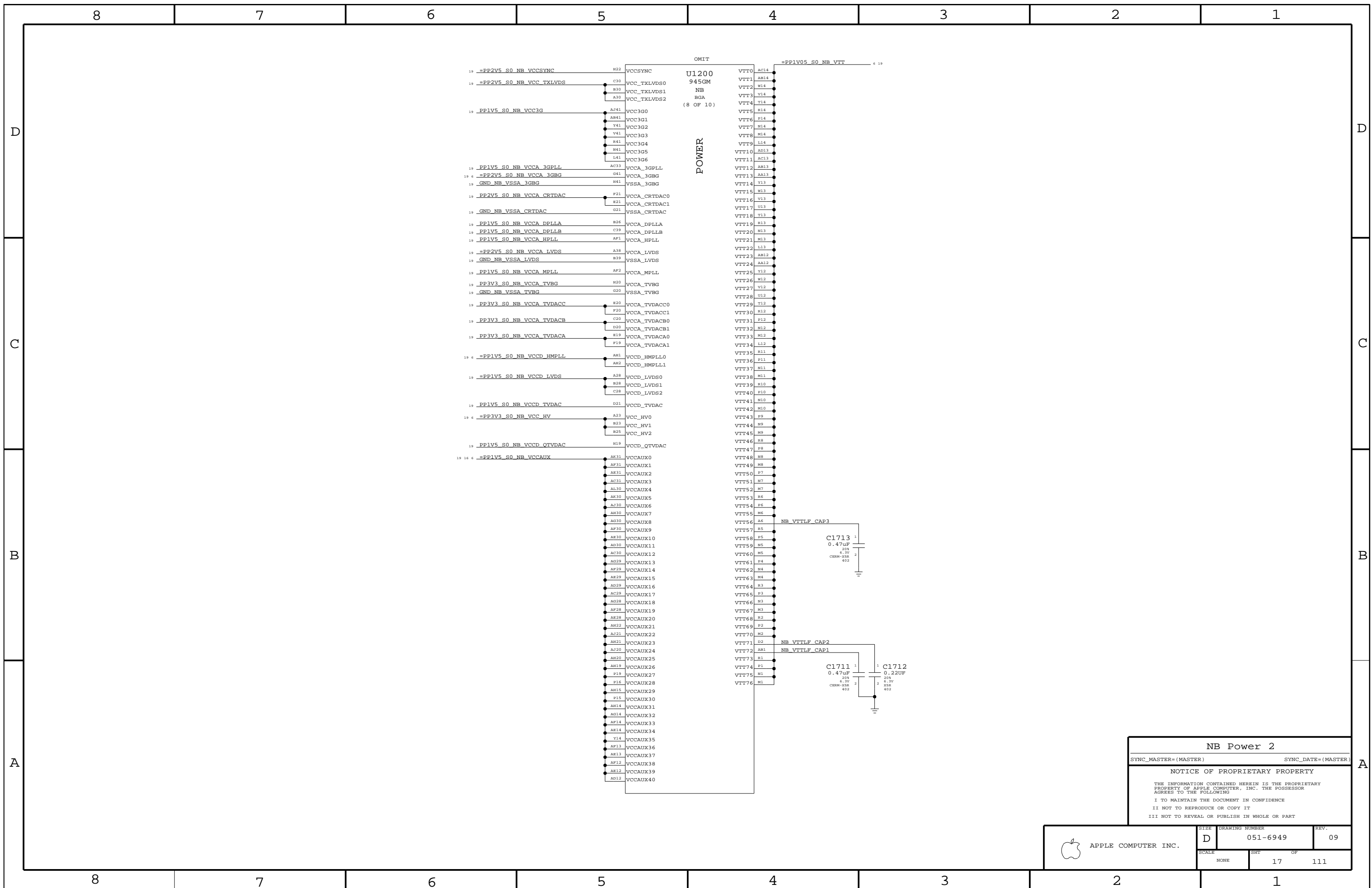
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	SCALE: NONE	SHEET: 15	OF: 111



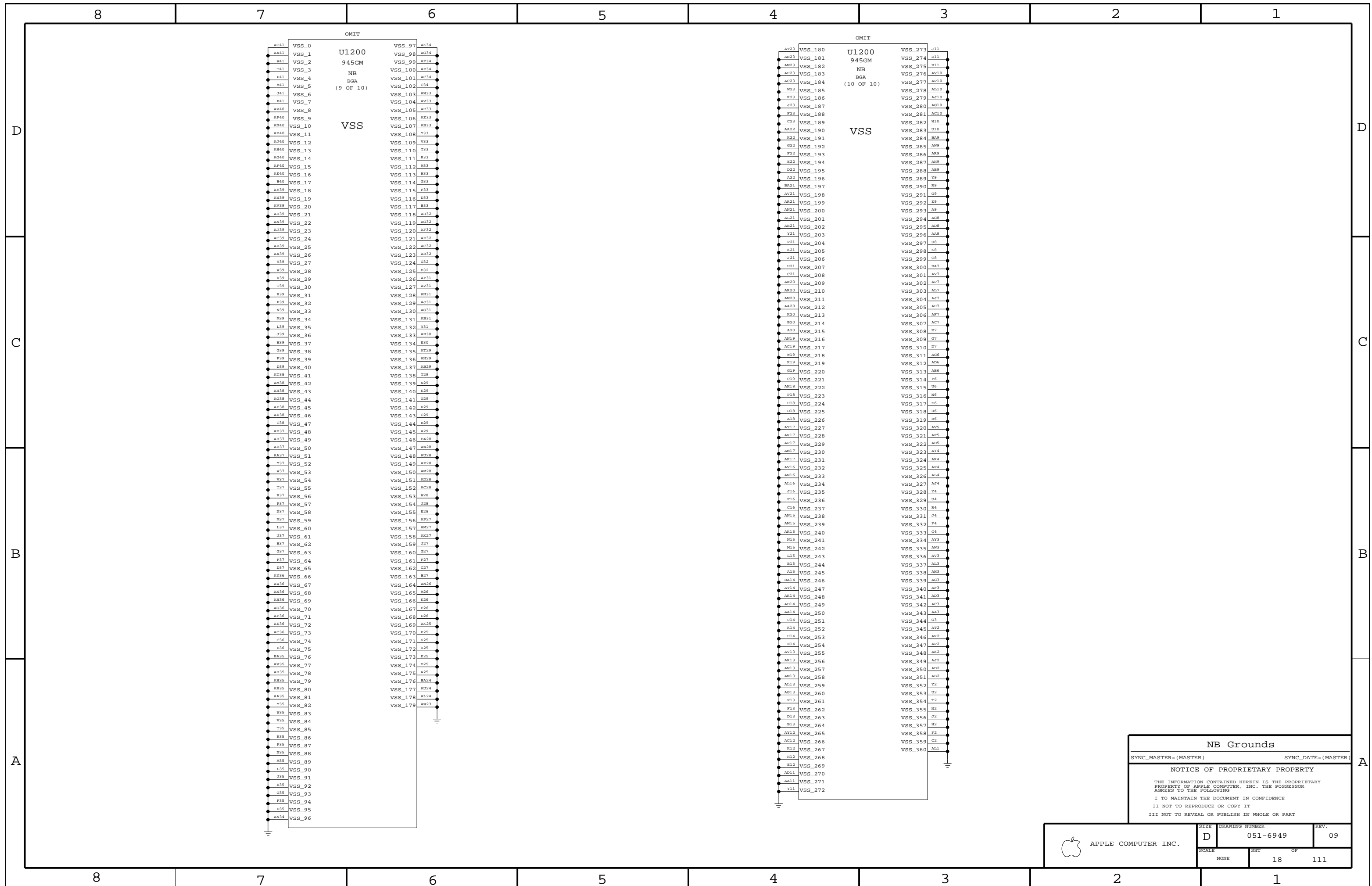
NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	17	111	



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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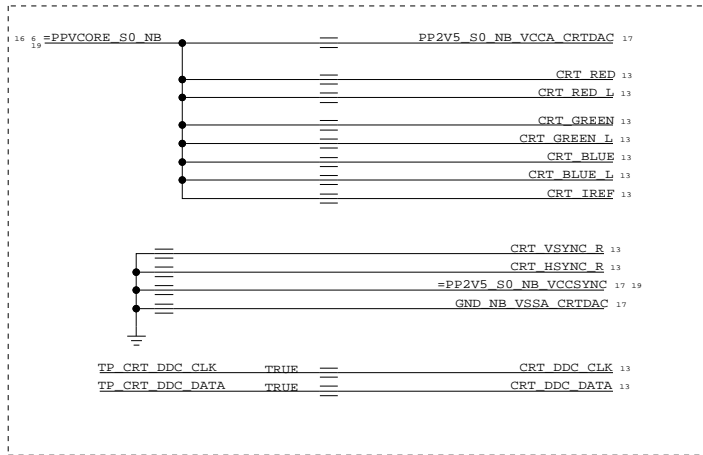
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 18	OF 111

Power Interface

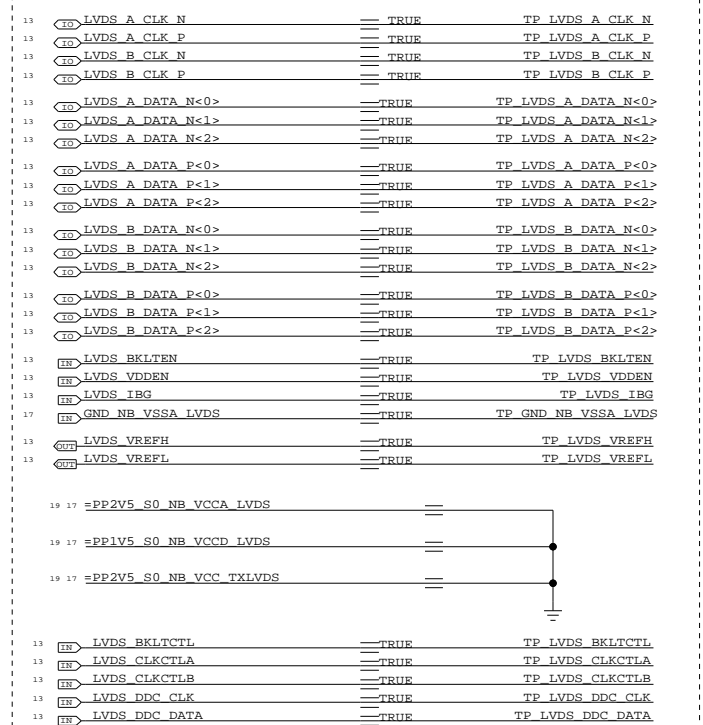
These are the power signals that leave the NB "block"

PP1V05_S0_FSB_NB	5 6 12
PPVCORE_S0_NB	6 16 19
PP1V05_S0_NB	6
PP1V05_S0_NB_VTT	6 17 19
PP1V5_S0_NB	6 19
PP1V5_S0_NB_PCIE	6 13
PP1V5_S0_NB_PLL	6 19
PP1V5_S0_NB_TVDAC	6 19
PP1V5_S0_NB_VCCD_HMPLL	6 17
PP1V5_S0_NB_VCCD_LVDS	17 19
PP1V5_S0_NB_VCCAUX	6 16 17 19
PP1V8_S3_MEM_NB	6 14 16 19
PP2V5_S0_NB_VCCSYNCR	17 19
PP2V5_S0_NB_VCC_TXLVDS	17 19
PP2V5_S0_NB_VCCA_3GBG	6 17 19
PP2V5_S0_NB_VCCA_LVDS	17 19
PP3V3_S0_NB	6 14 20
PP3V3_S0_NB_TVDAC	6
PP3V3_S0_NB_VCC_HV	6 17 19

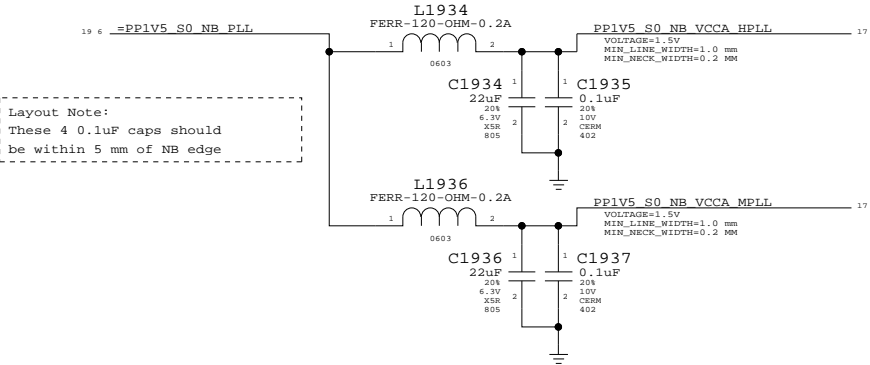
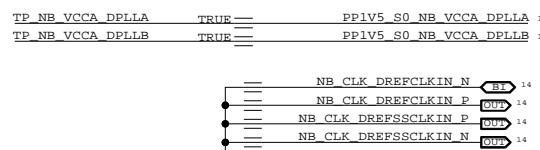
TVOUT DISABLE



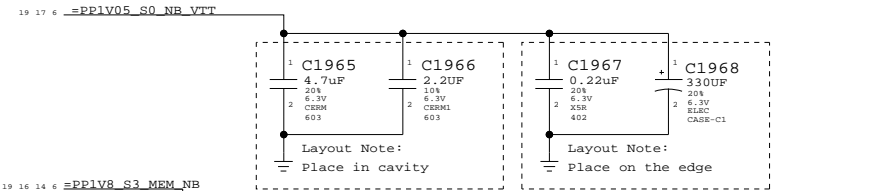
LVDS DISABLE



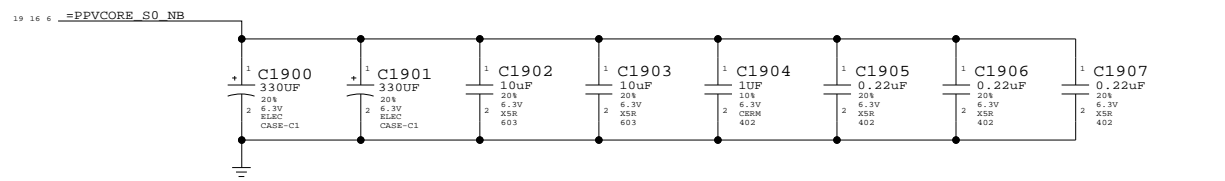
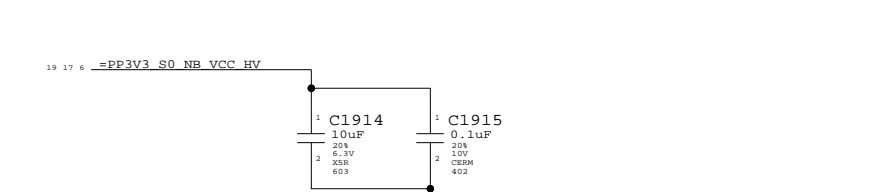
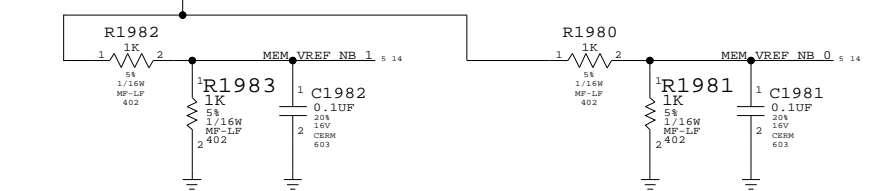
DISPLAY DISABLE



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge

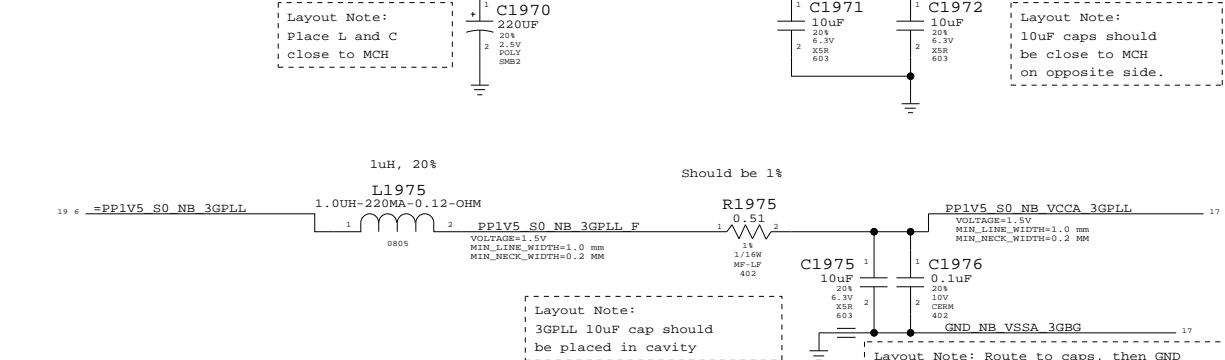


Layout Note:
Place in cavity



Layout Note:
Place L and C close to MCH

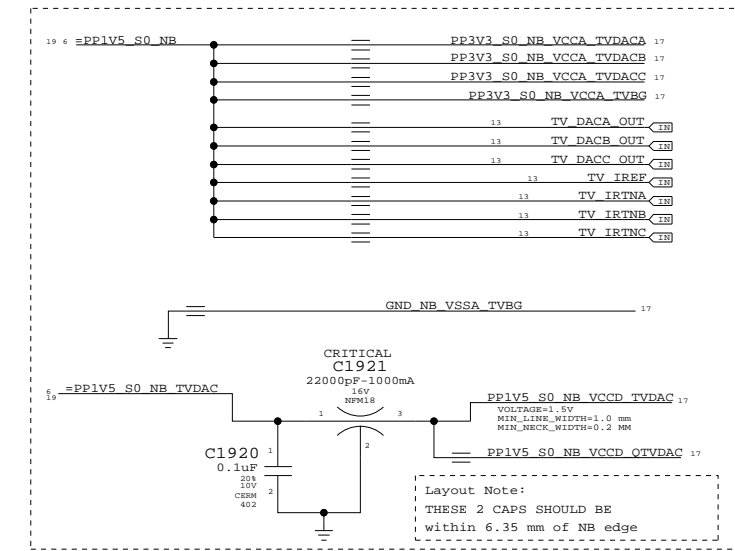
Layout Note:
10uF caps should be close to MCH on opposite side.



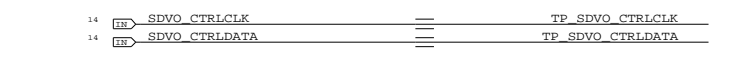
Layout Note:
3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

TVOUT DISABLE



Layout Note:
THESE 2 CAPS SHOULD BE within 6.35 mm of NB edge



NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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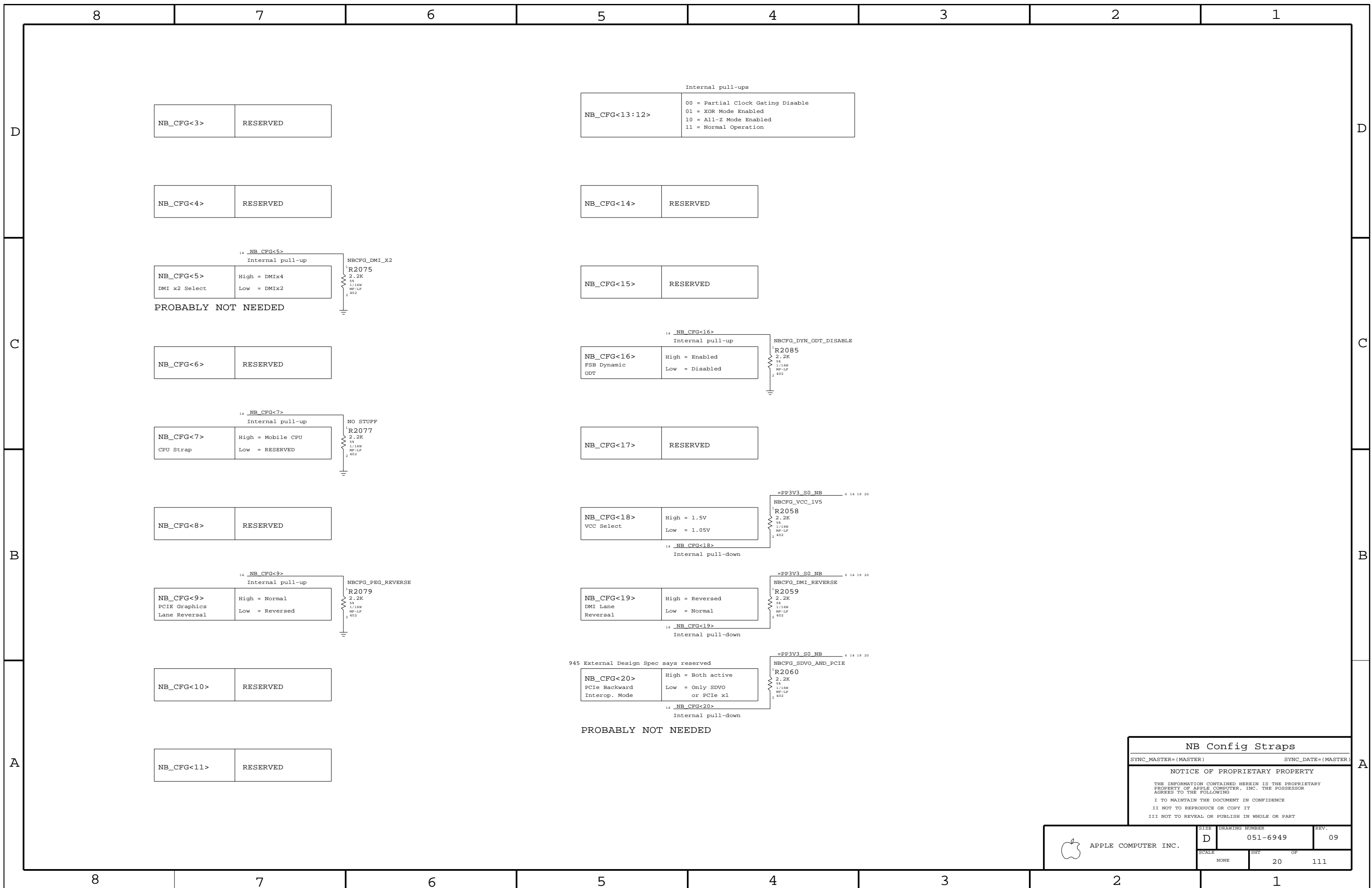
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		SHEET	OF
		19	111



NB Config Straps

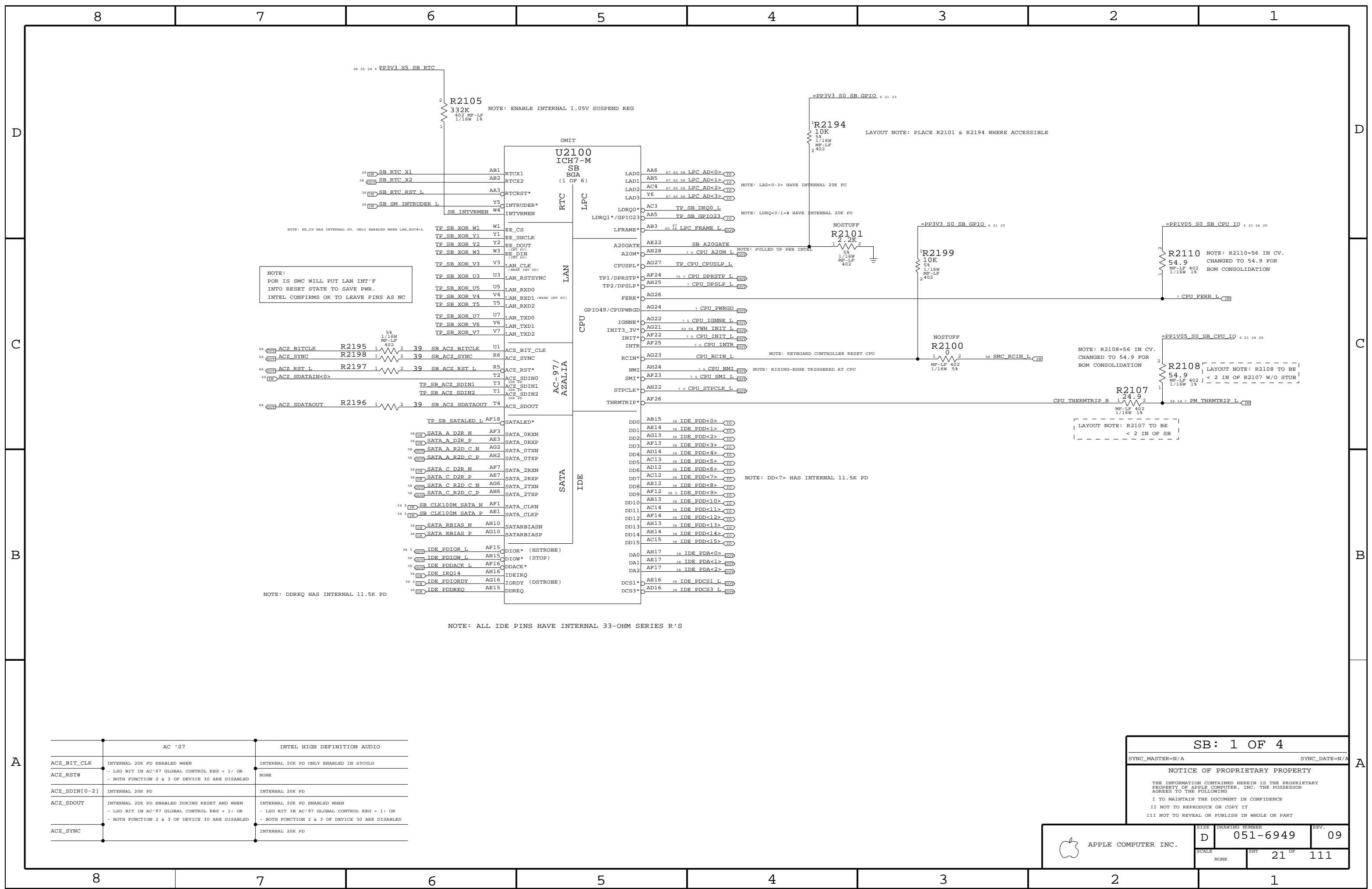
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SCALE	SHT	OF	
NONE	20	111	



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

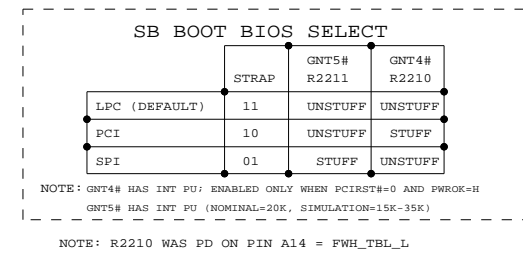
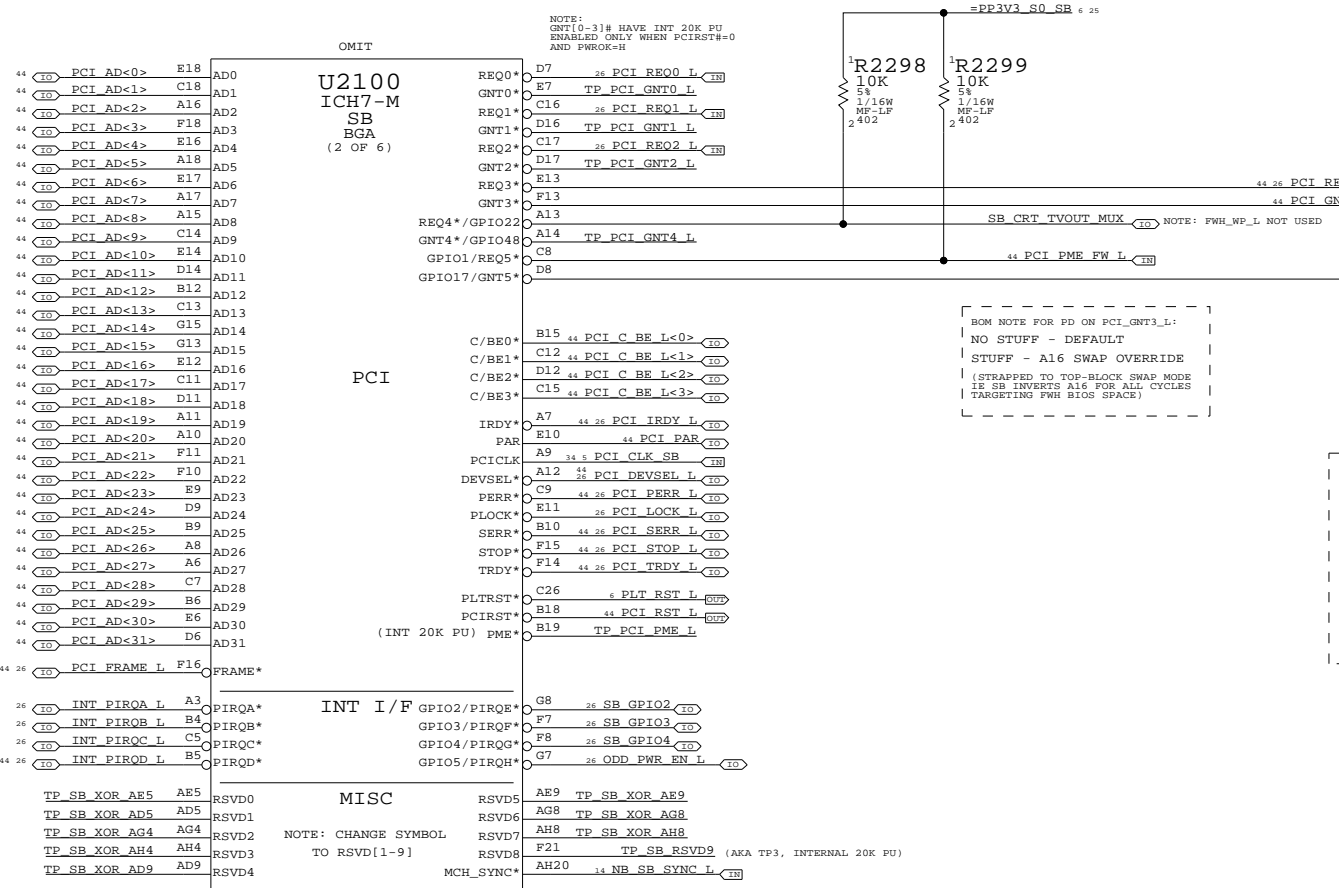
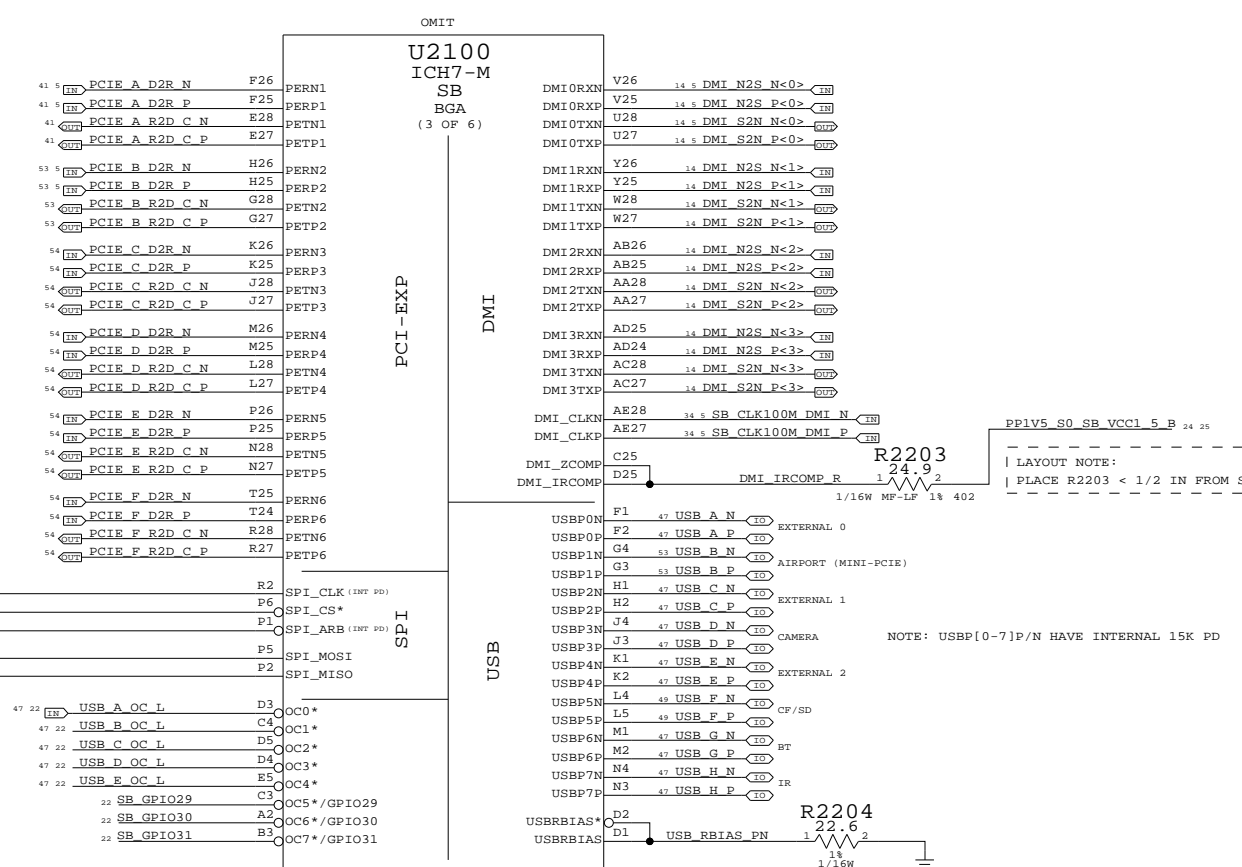
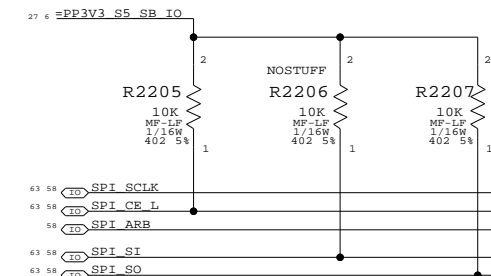
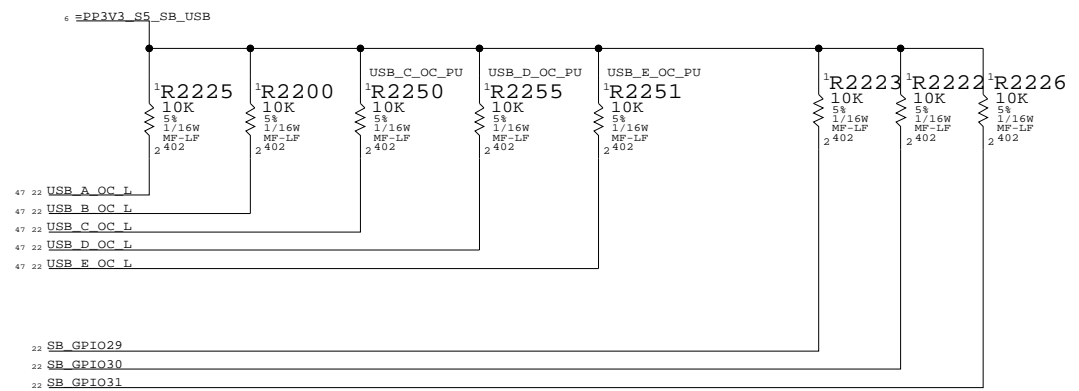
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	D	051-6949	09
SCALE	SHT	21 OF	111
NONE			



SB: 2 OF 4

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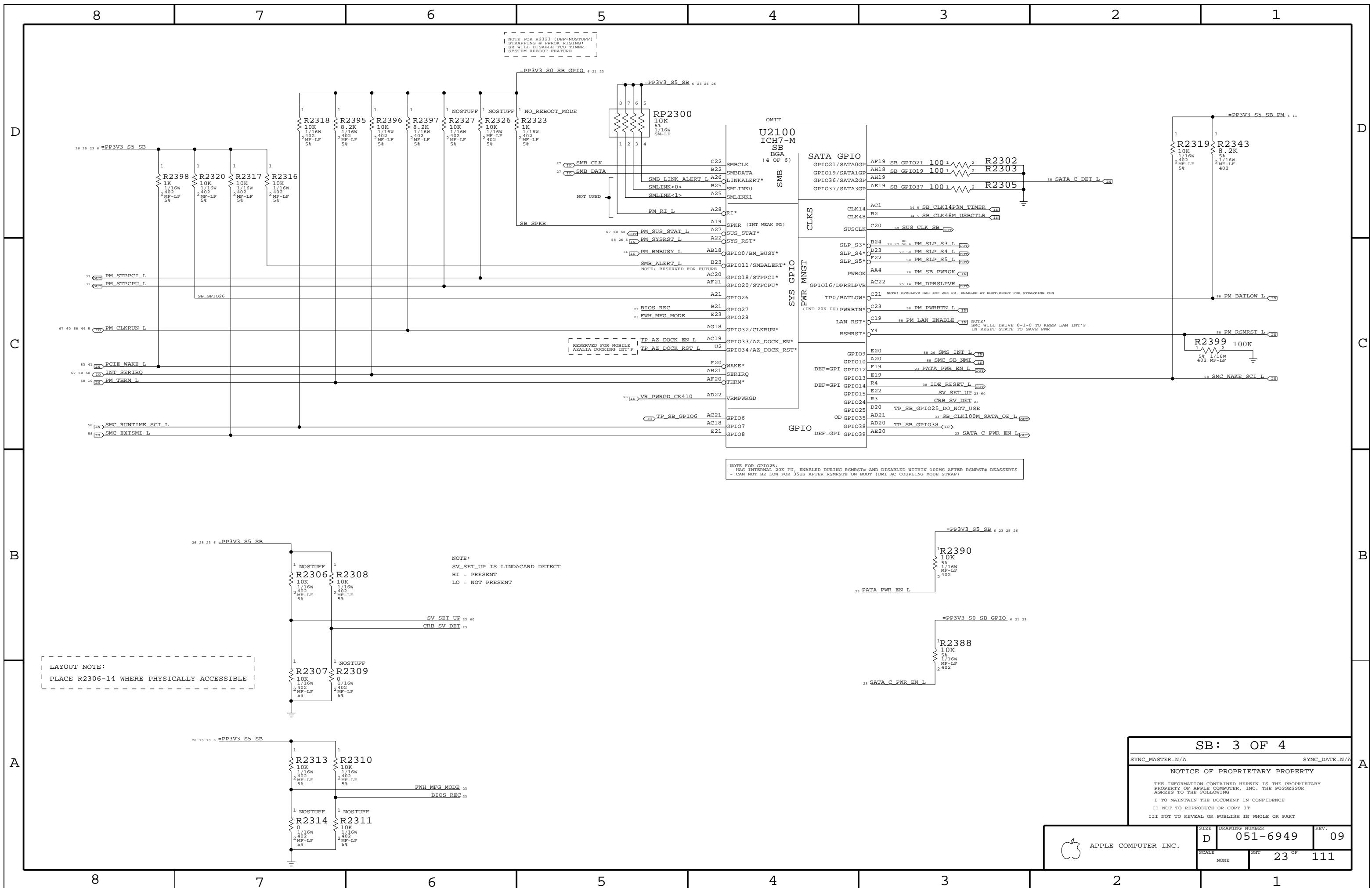
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NOTE FOR R2323 (DEF-NOSTUFF)
STRAPPING # PWROK RISING:
SB WILL DISABLE TOO TIMER
SYSTEM REBOOT FEATURE

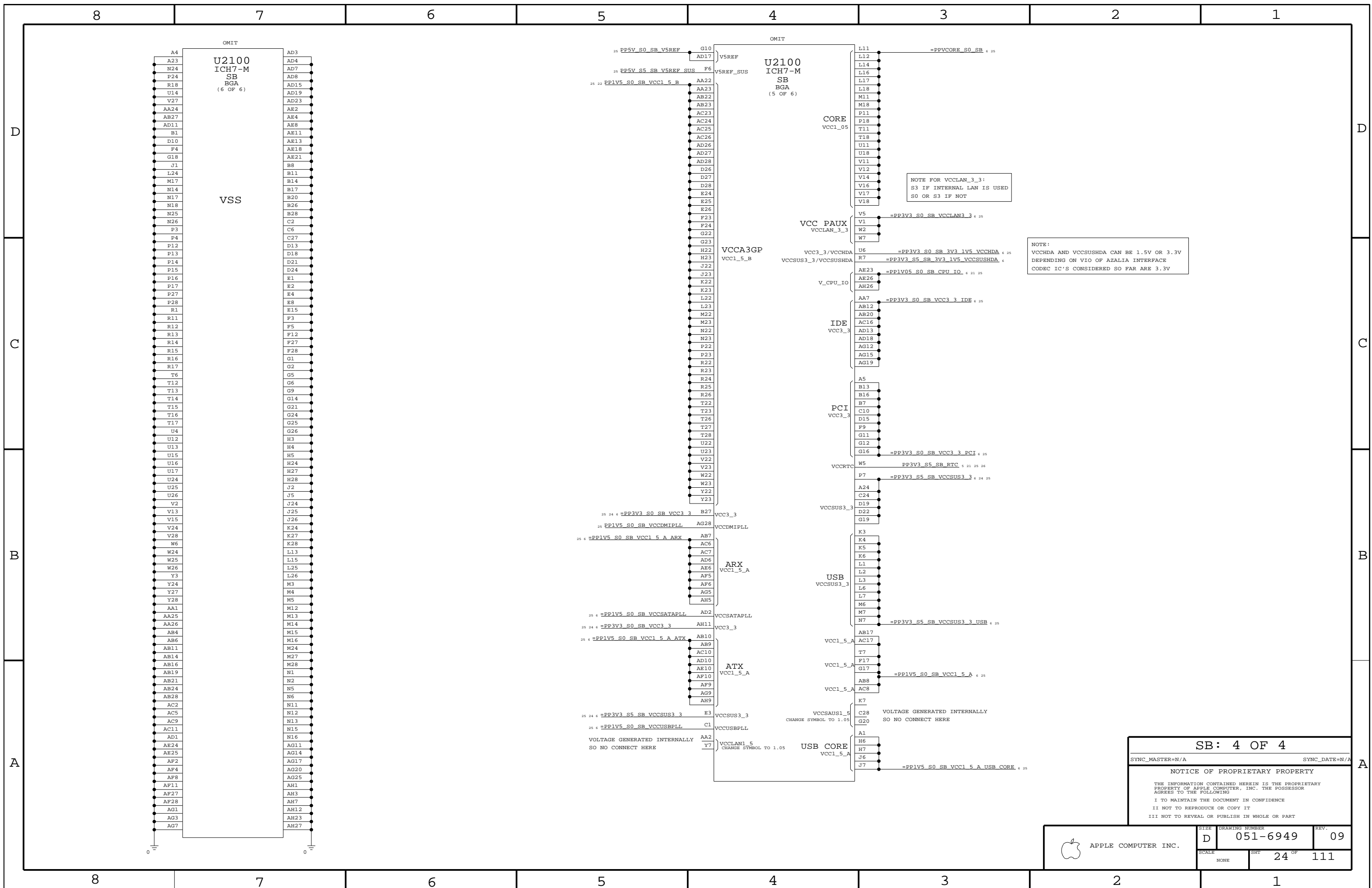
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-6949	09
SCALE	NONE	SHT	23 OF 111



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCCHDA AND VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

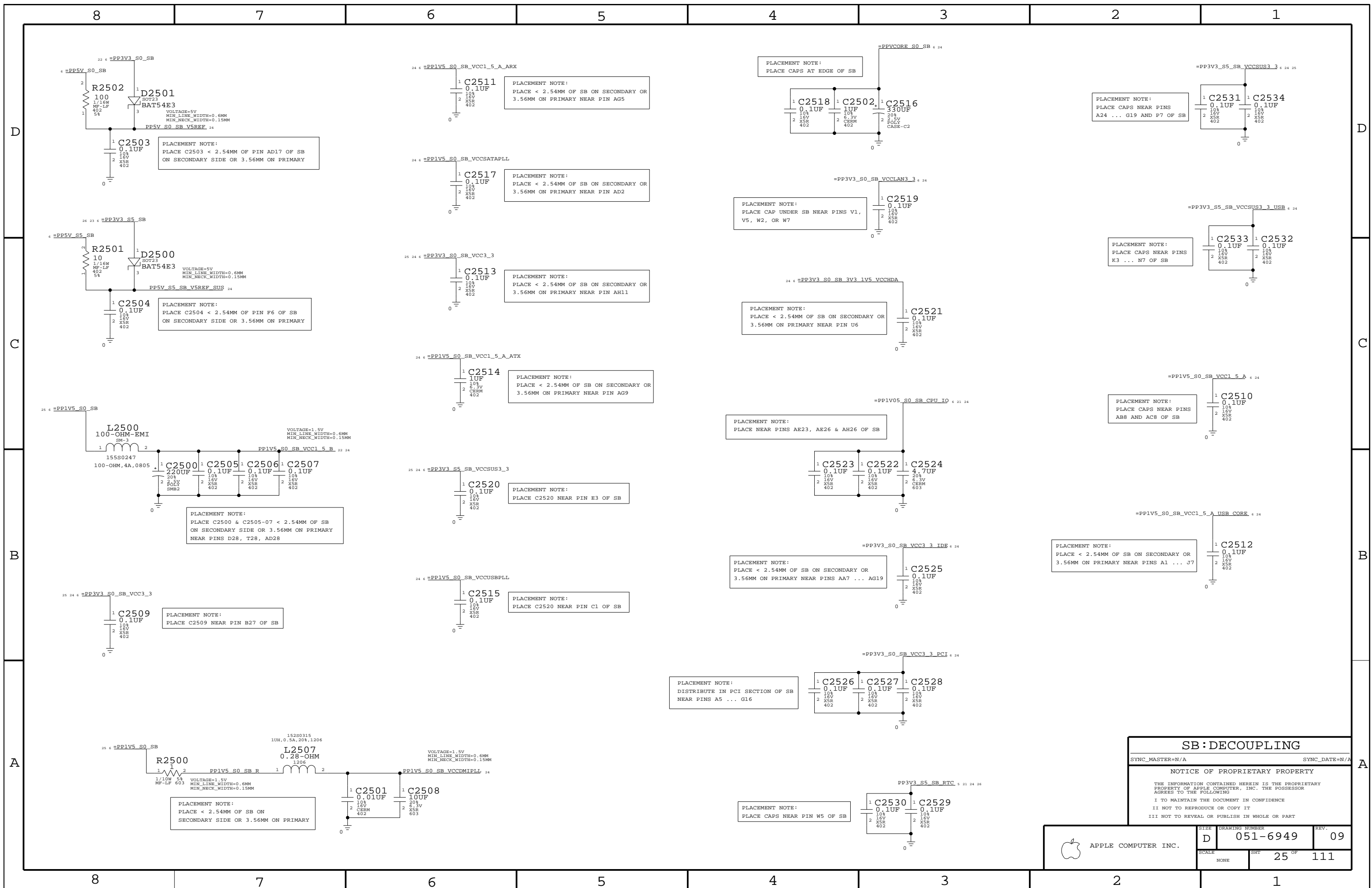
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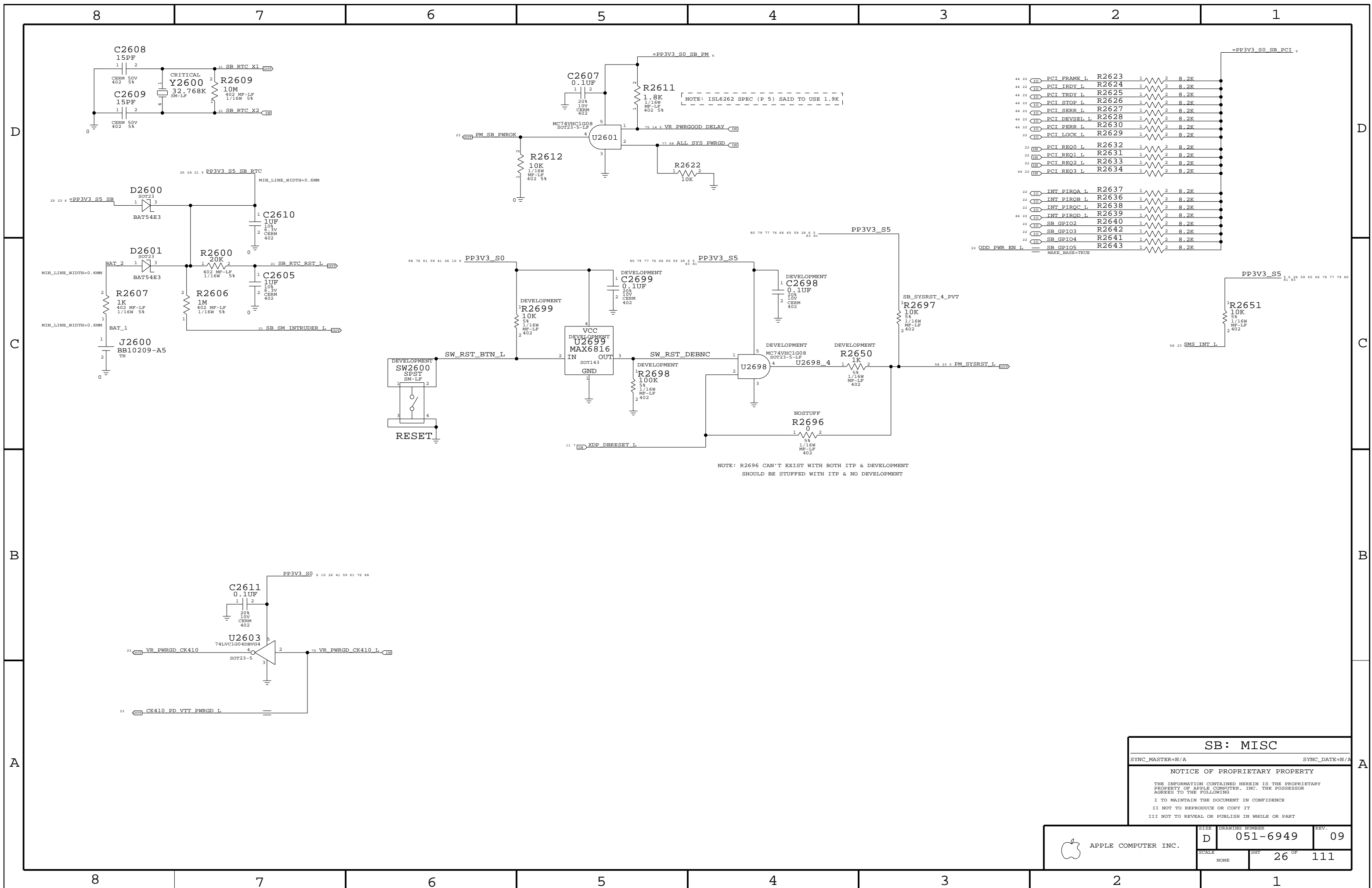
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	D	051-6949	09
SCALE	SHT	REV.	
NONE	24 OF 111		





SB: MISC

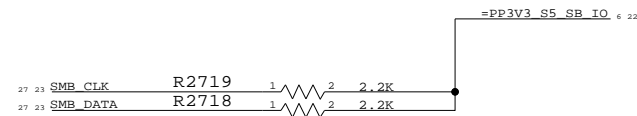
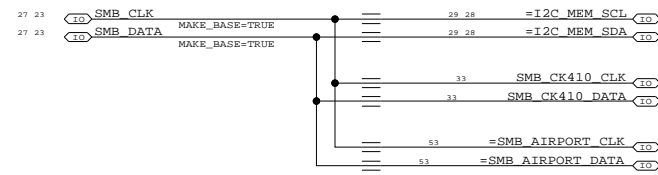
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	D	051-6949	09
SCALE	NONE	SHT	26 OF 111

SB I2C BUSSES



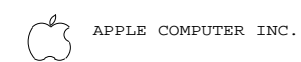
SB: SMB HUB

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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	27	111

Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

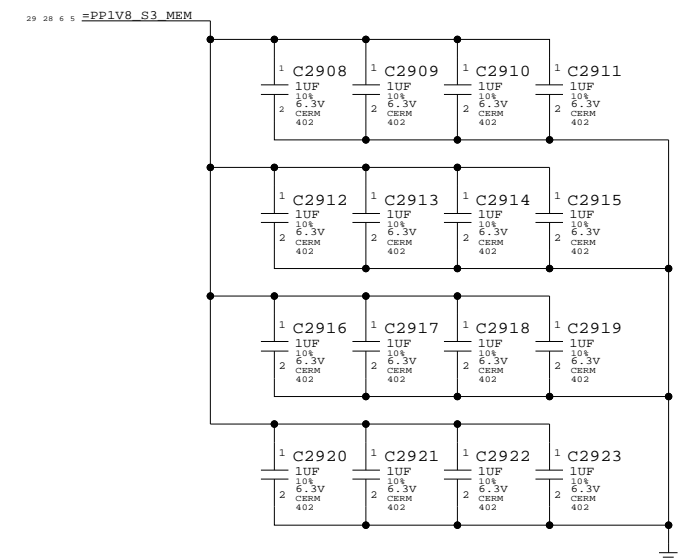
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	SHT	OF	
	29	111	

8

7

6

5

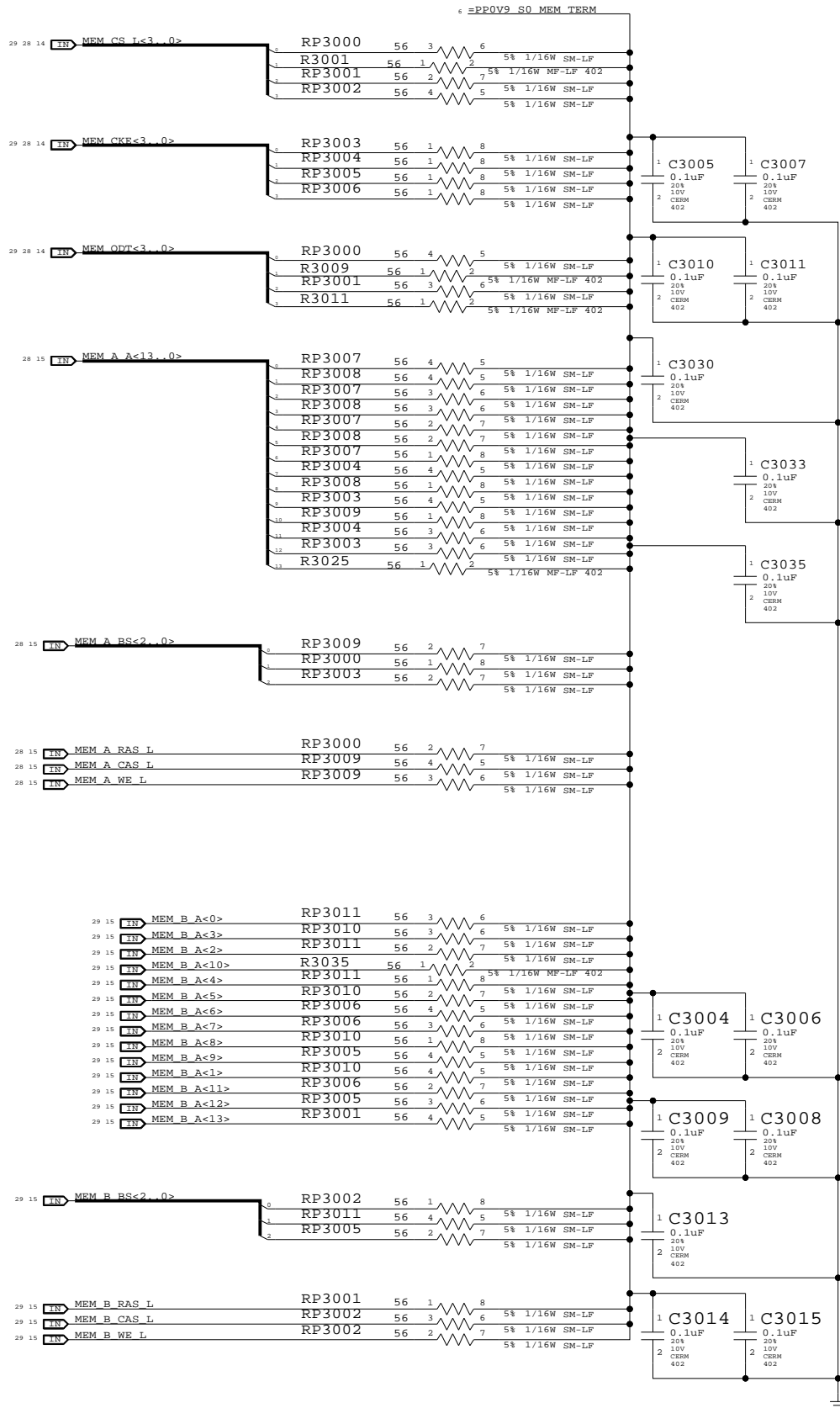
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6949 09

SCALE SHEET OF

NONE 30 111

8

7

6

5

4

3

2

1

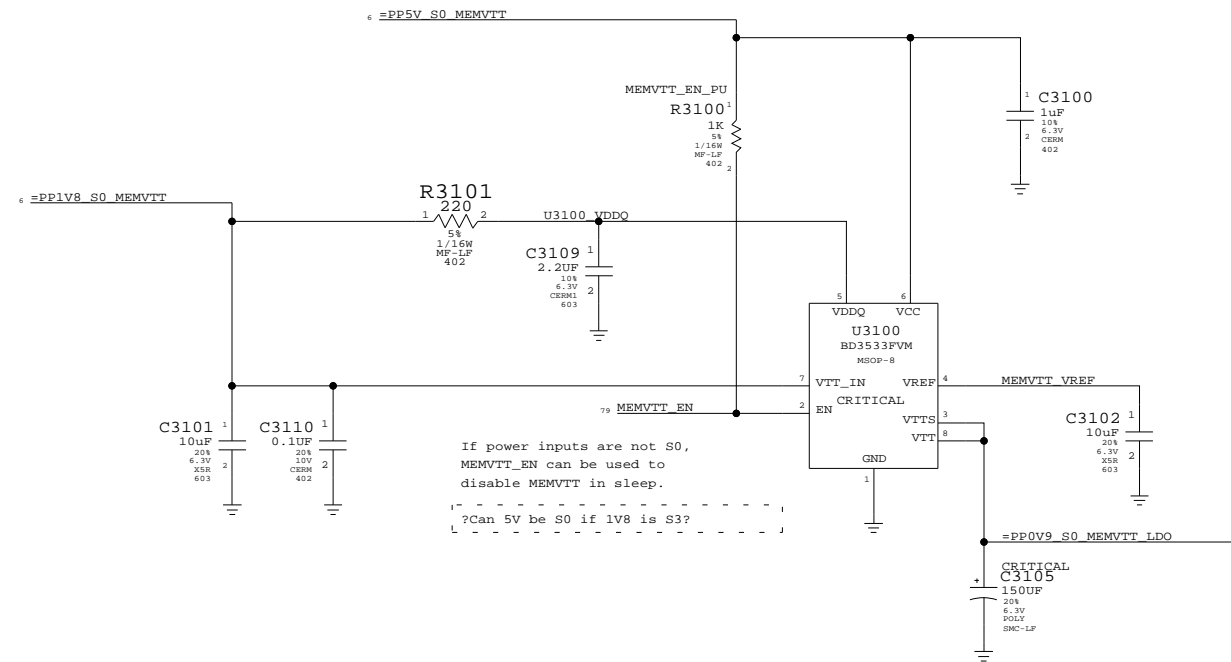
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

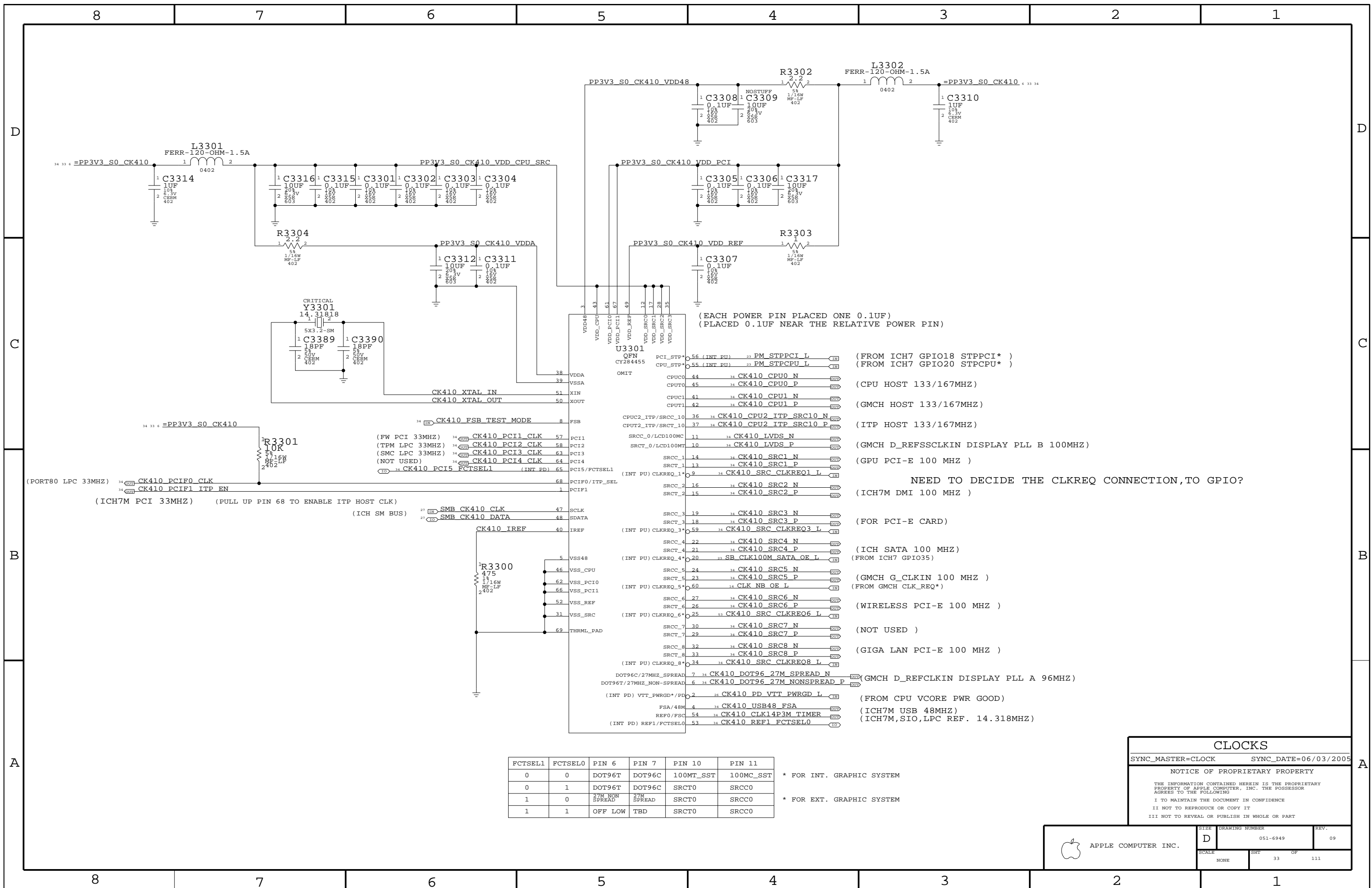
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	D	051-6949	09
SCALE		SHT	OF
NONE		31	111



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)

(FROM ICH7 GPIO35)

(GMCH G_CLKIN 100 MHZ)

(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

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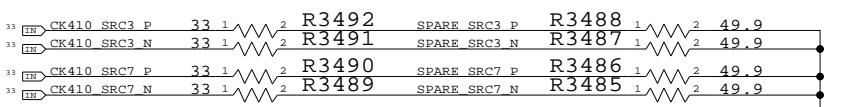
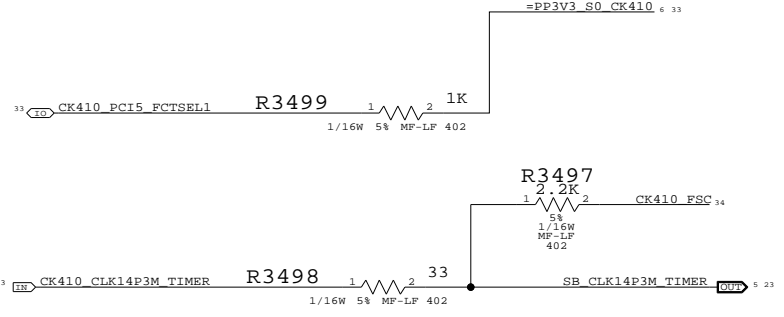
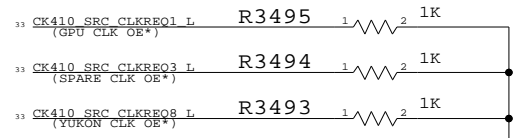
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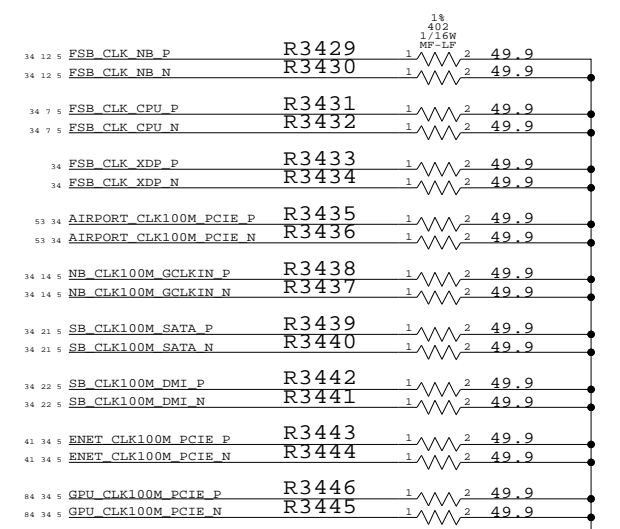
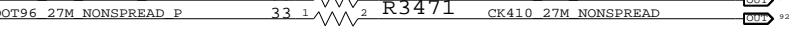
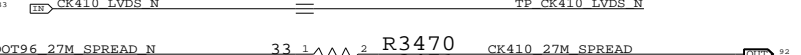
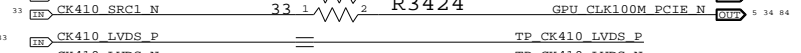
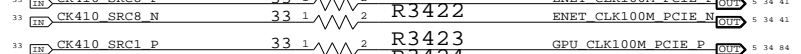
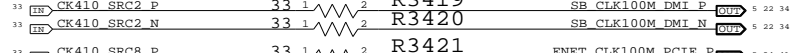
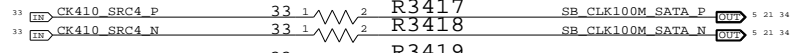
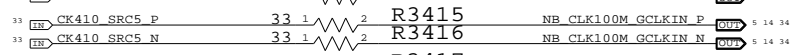
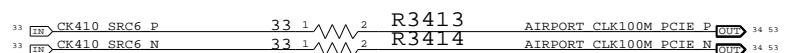
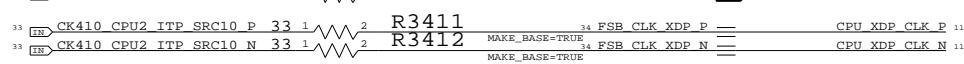
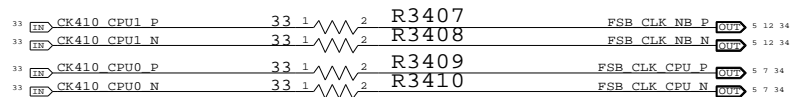
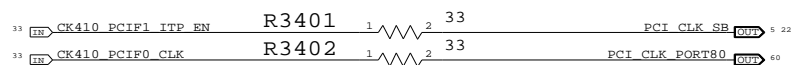
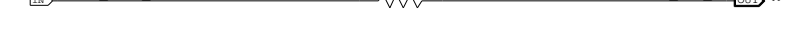
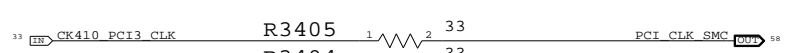
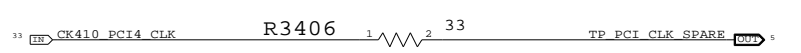
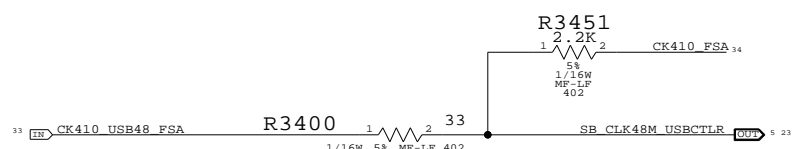
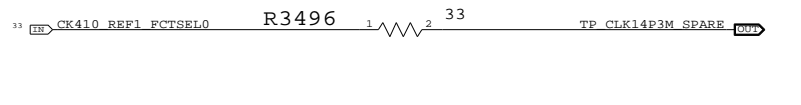
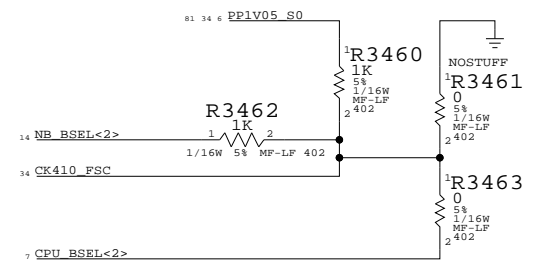
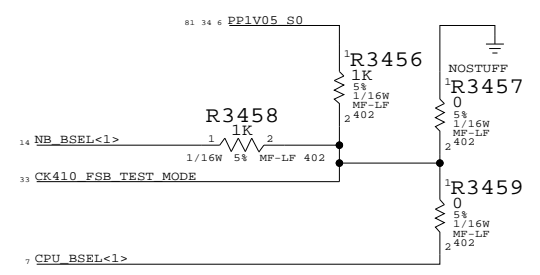
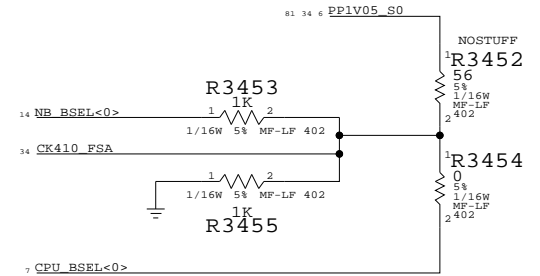
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	33	111

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457 R3458
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458



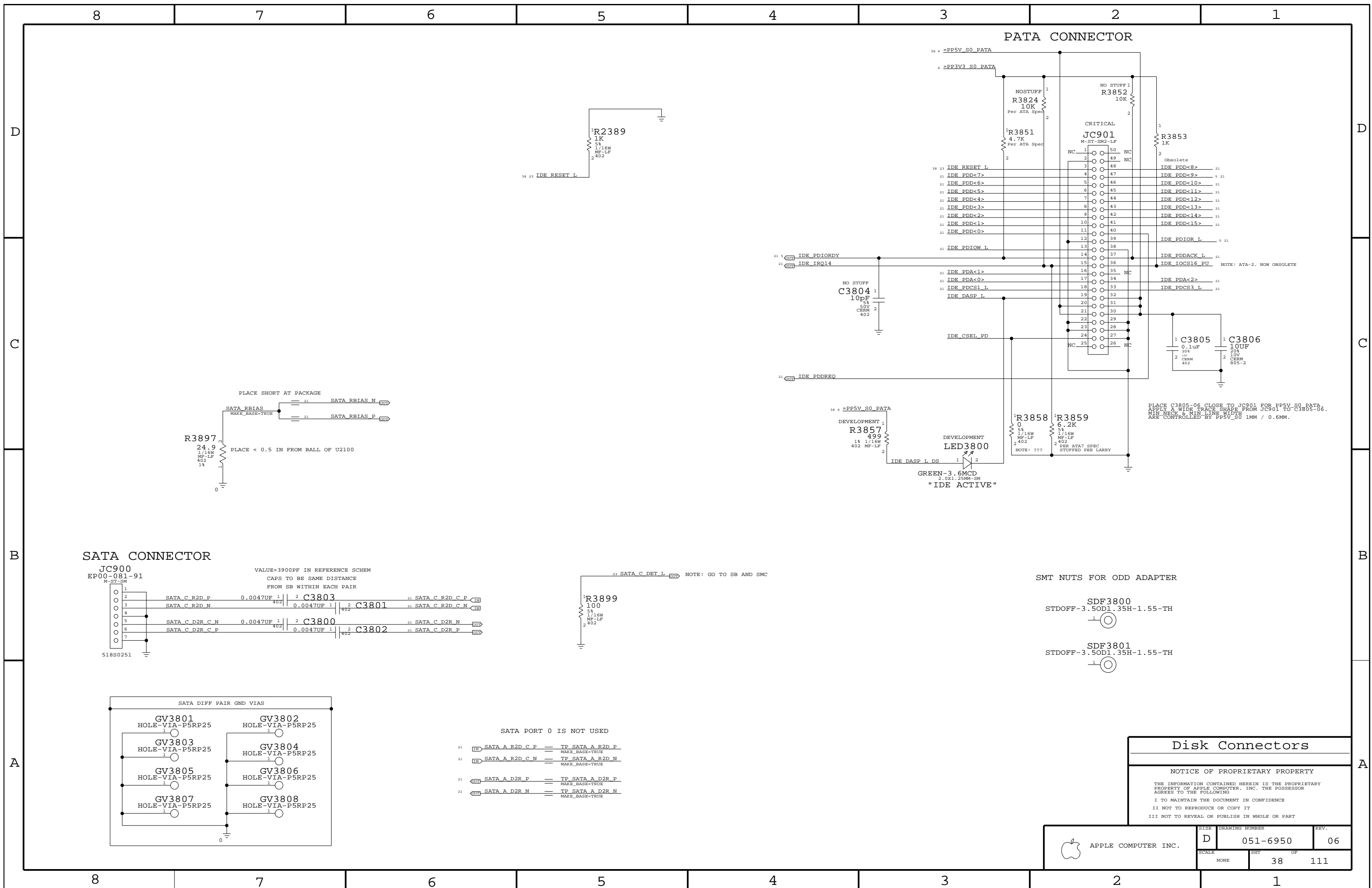
CLOCKS: TERMINATIONS

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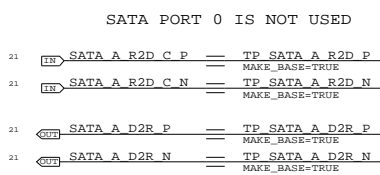
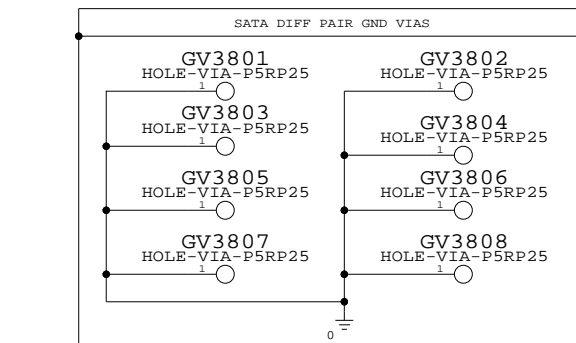
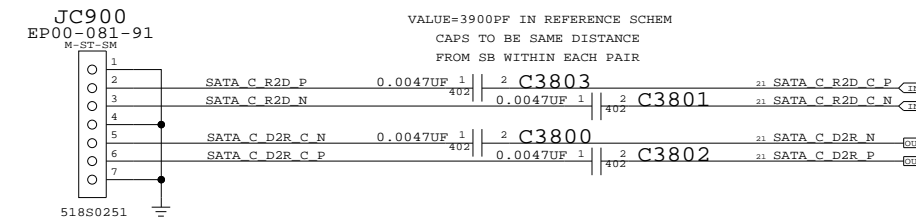
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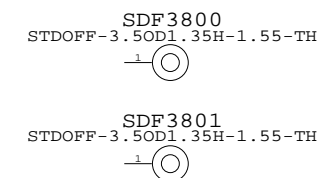
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	111
NONE	34		



SATA CONNECTOR



SMT NUTS FOR ODD ADAPTER



Disk Connectors

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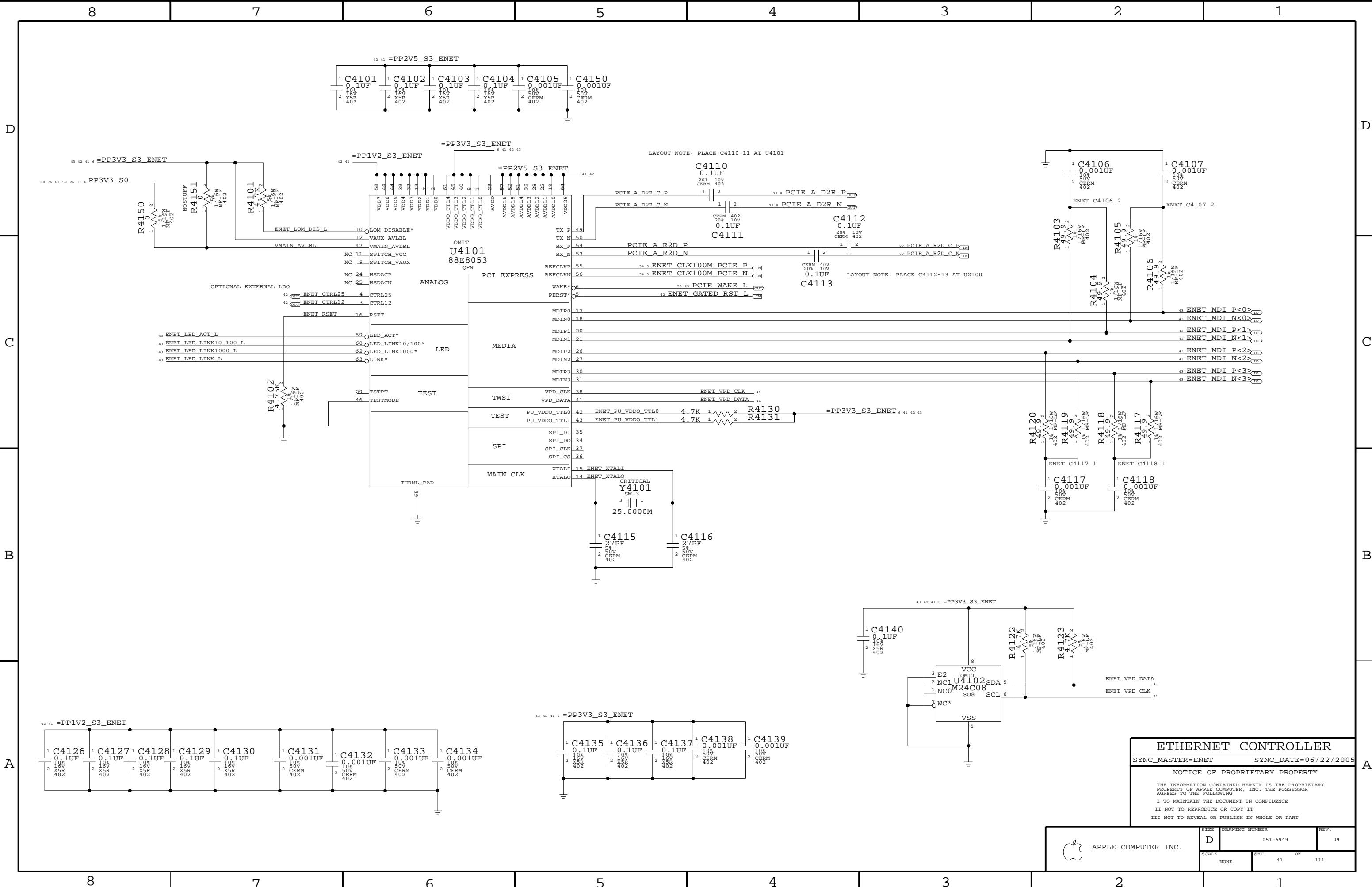
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	D	051-6950	06
SCALE	SHT OF		
NONE	38	111	



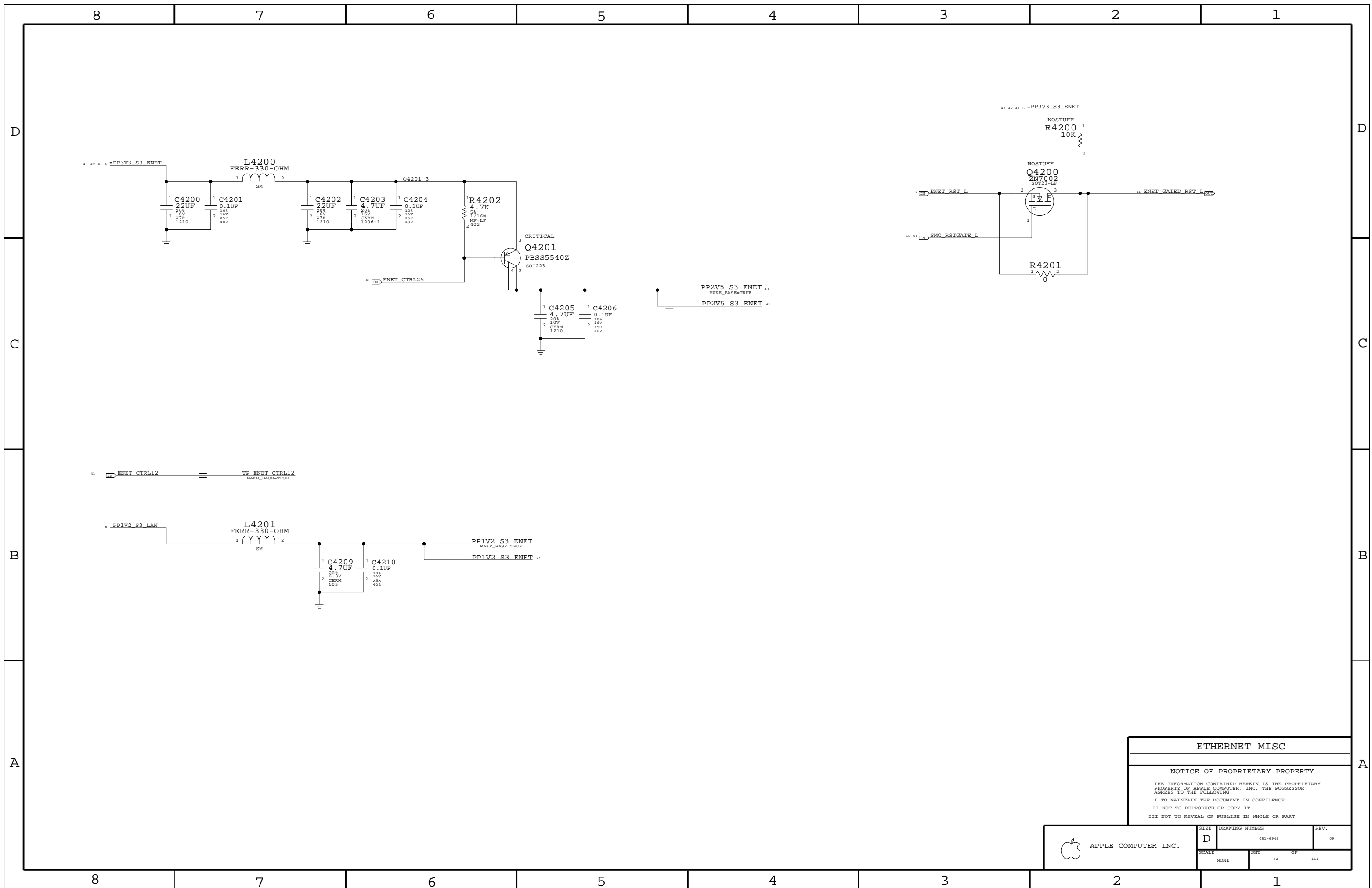
ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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	SCALE NONE	SHEET 41	OF 111



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

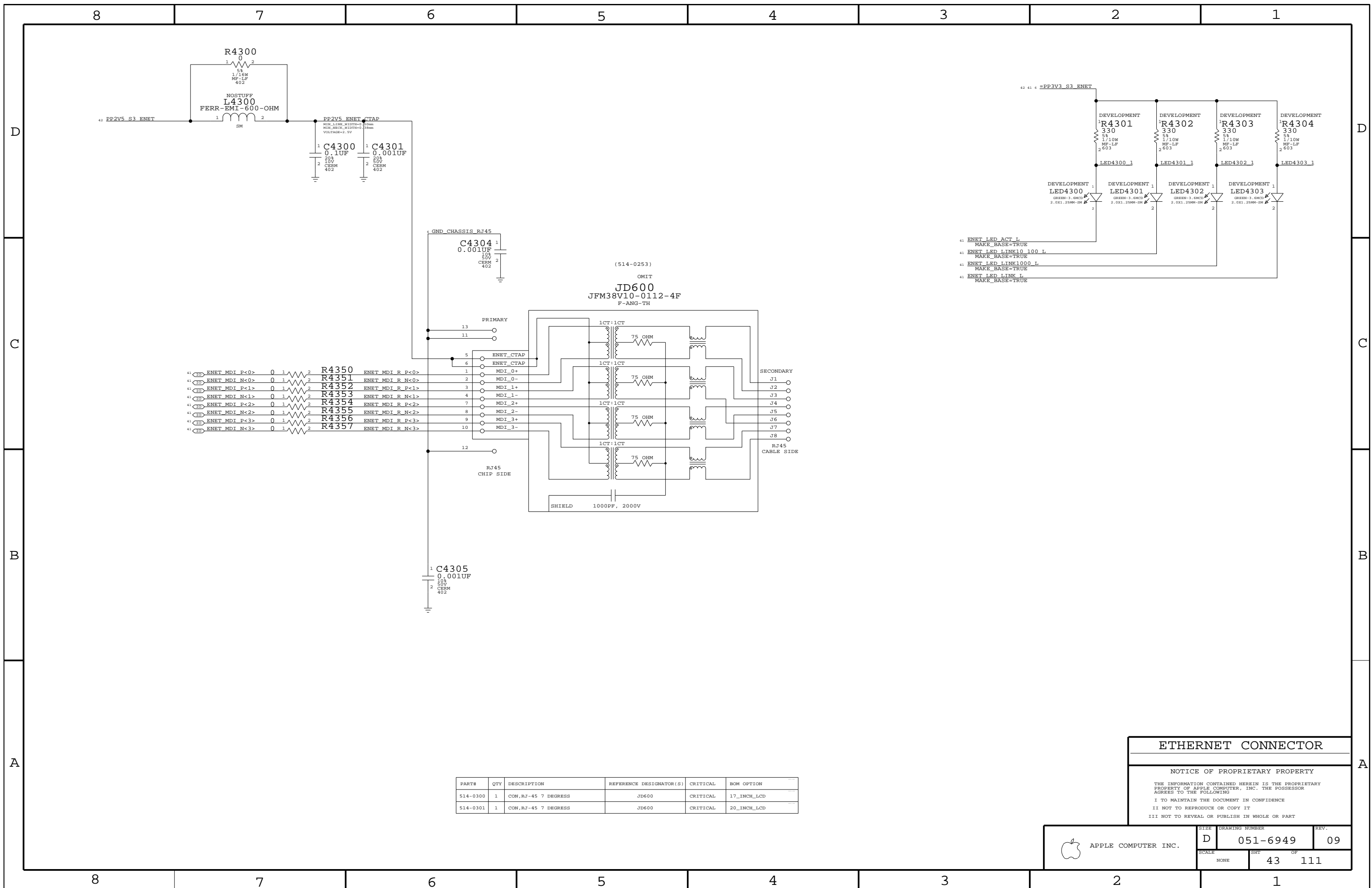
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 42	OF 111



ENET MDI P<0>	0	1	2	R4350	ENET MDI R P<0>
ENET MDI N<0>	0	1	2	R4351	ENET MDI R N<0>
ENET MDI P<1>	0	1	2	R4352	ENET MDI R P<1>
ENET MDI N<1>	0	1	2	R4353	ENET MDI R N<1>
ENET MDI P<2>	0	1	2	R4354	ENET MDI R P<2>
ENET MDI N<2>	0	1	2	R4355	ENET MDI R N<2>
ENET MDI P<3>	0	1	2	R4356	ENET MDI R P<3>
ENET MDI N<3>	0	1	2	R4357	ENET MDI R N<3>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0300	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0301	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

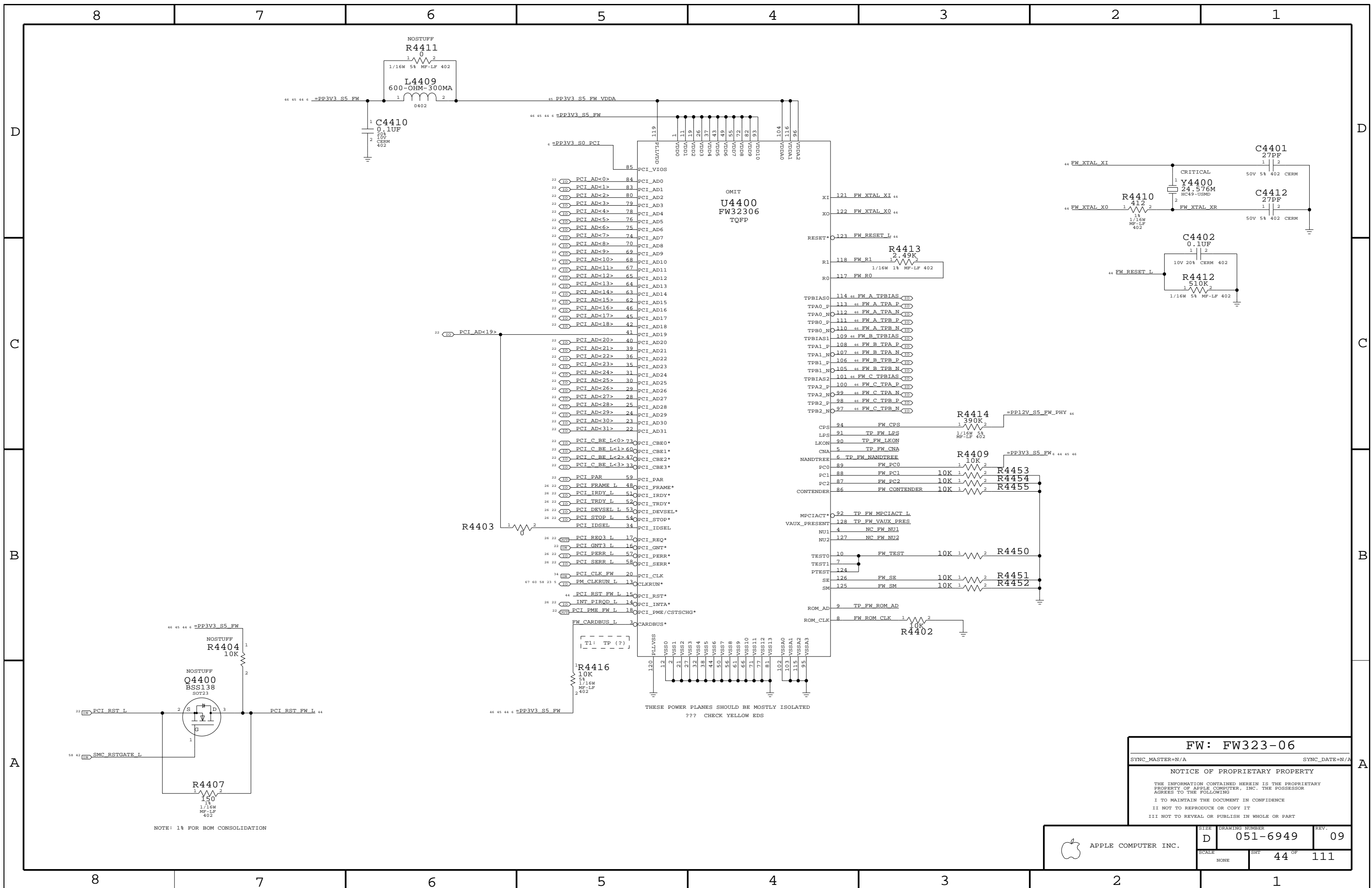
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	NONE	SHT	OF
		43	111



THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
 ??? CHECK YELLOW EDS

NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06

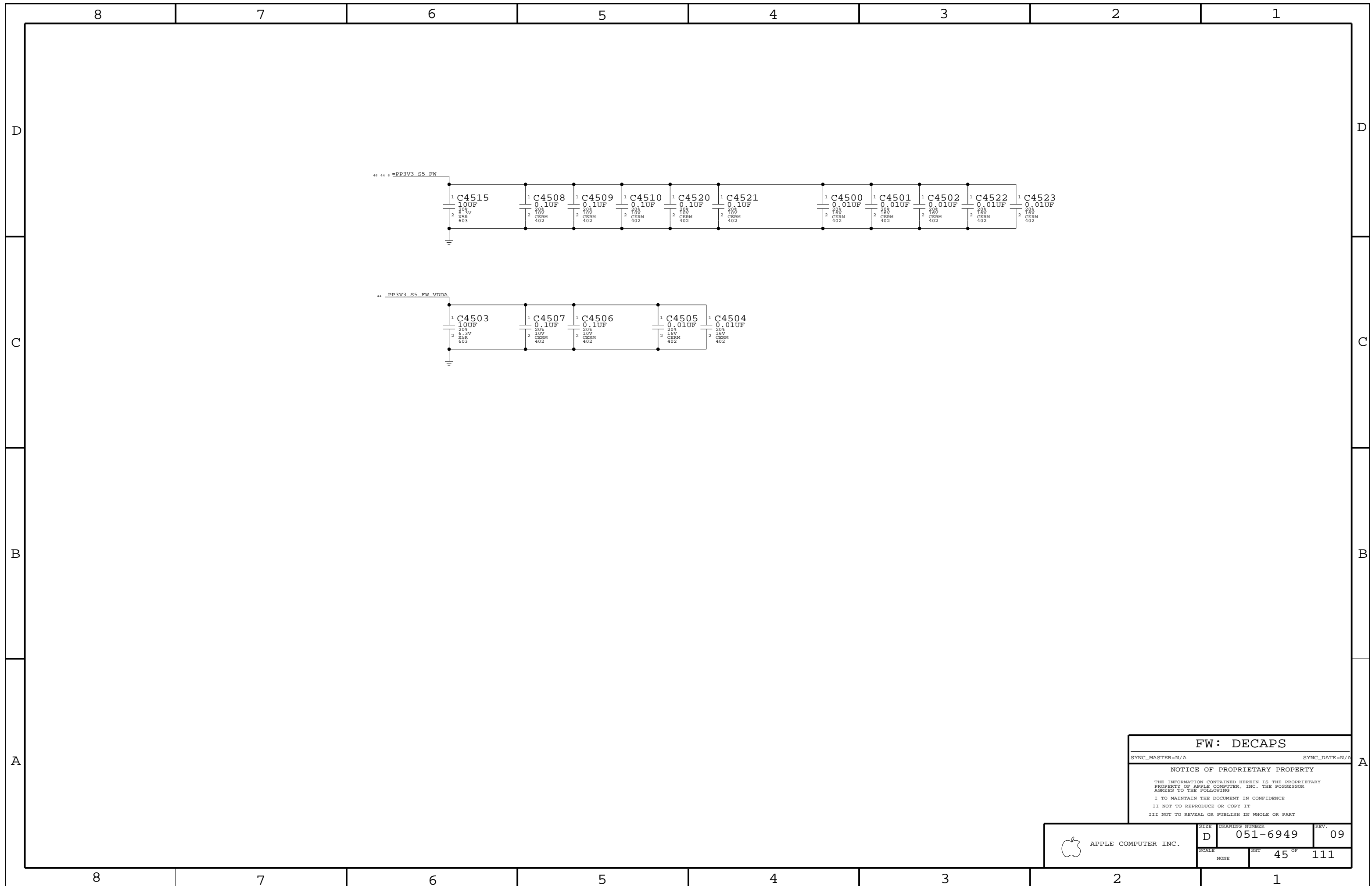
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	SCALE: NONE	SHEET: 44 OF 111	



FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

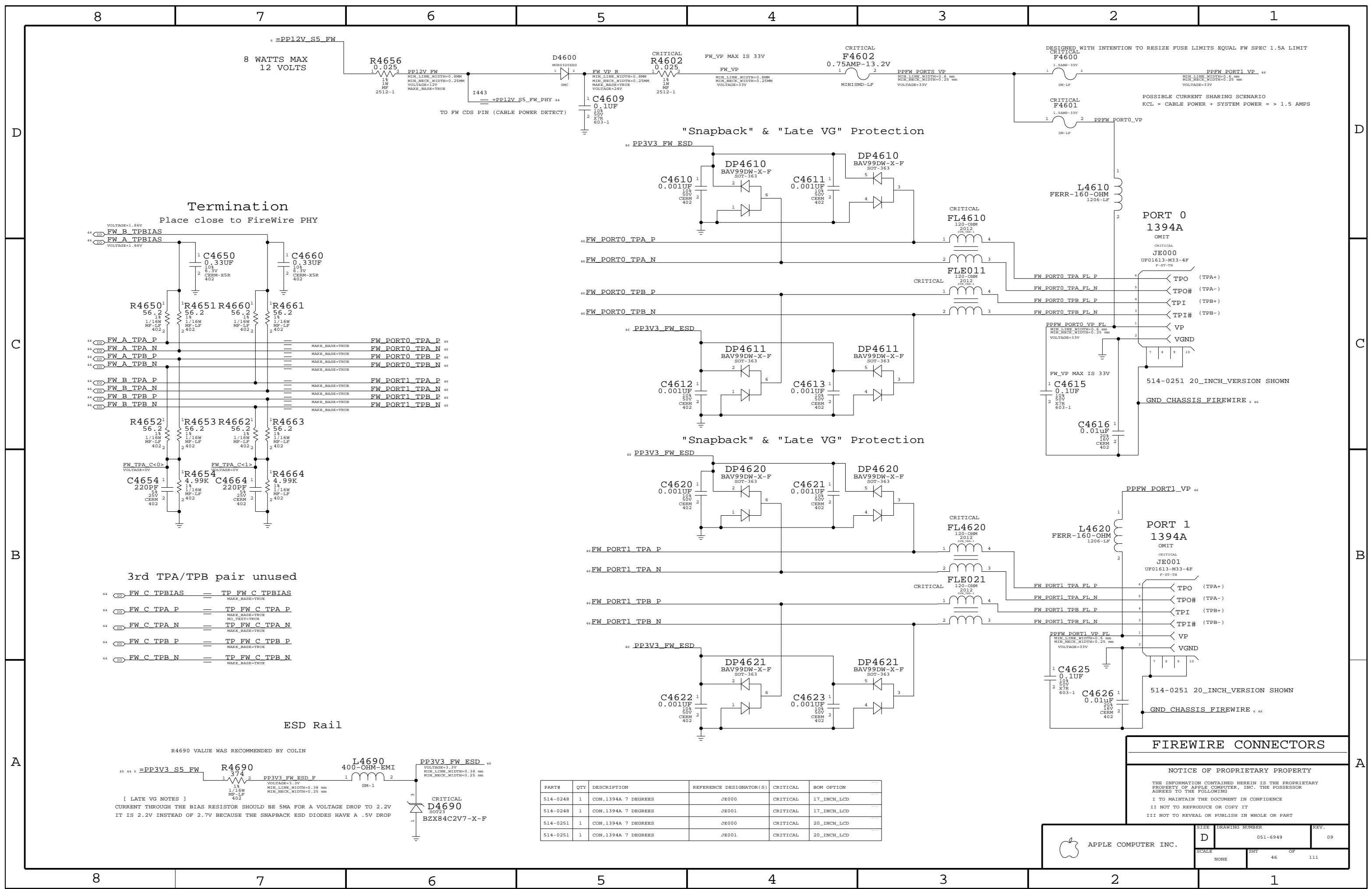
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

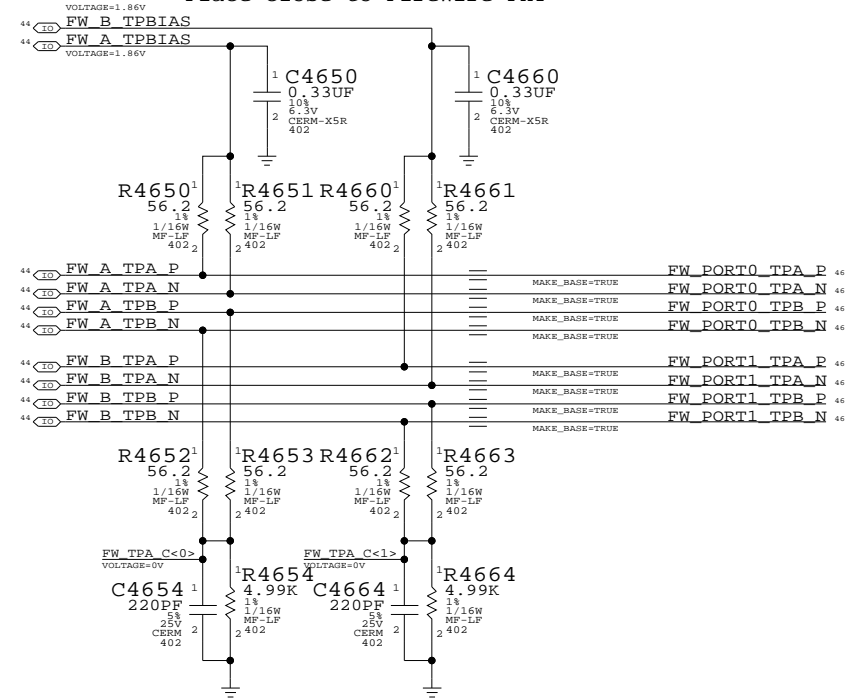
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

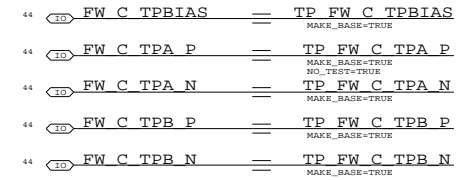
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	D	051-6949	09
	SCALE	SHT	OF
	NONE	45	111



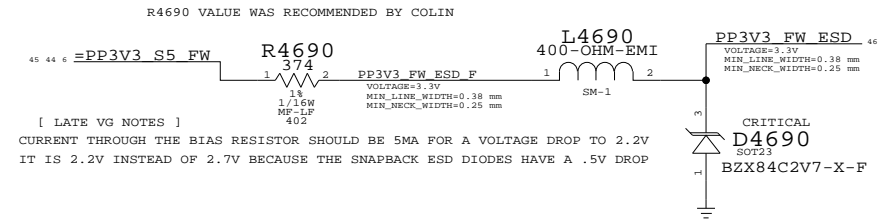
Termination
Place close to FireWire PHY



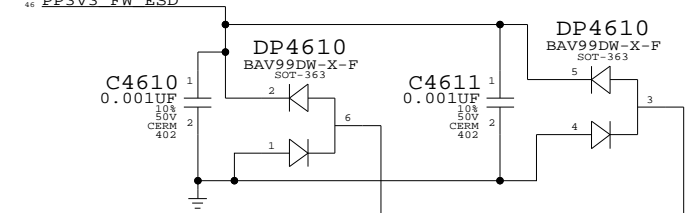
3rd TPA/TPB pair unused



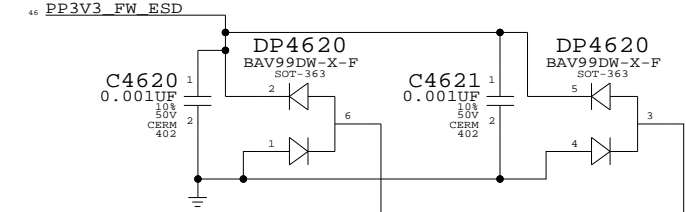
ESD Rail



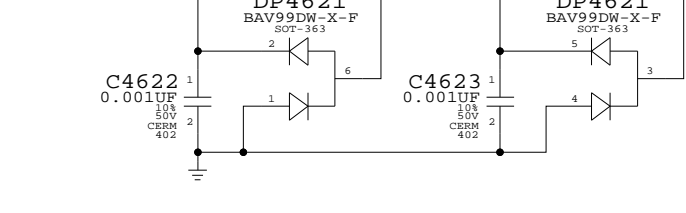
"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

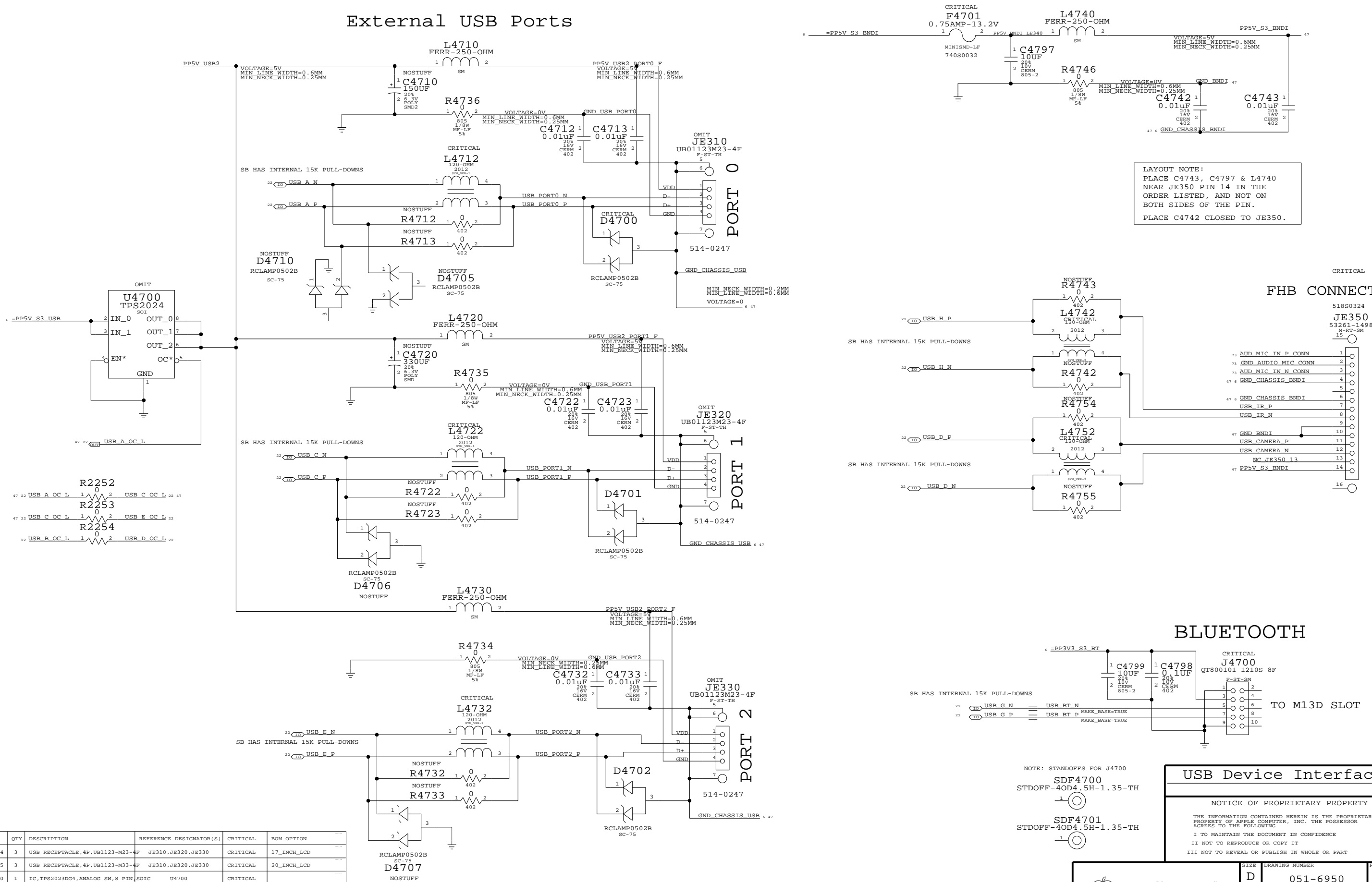
FIREWIRE CONNECTORS

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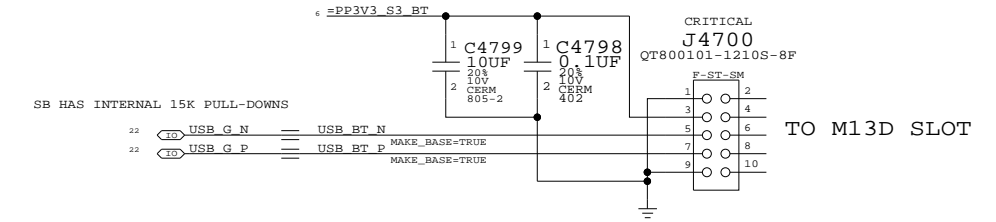
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6949	REV.: 09
	SCALE: NONE	SHEET: 46	OF: 111

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE350 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE350.

BLUETOOTH



NOTE: STANDOFFS FOR J4700

SDF4700
 STDOFF-40D4.5H-1.35-TH

SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	47	111	06

8

7

6

5

4

3

2

1

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BLANK


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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	<small>SIZE</small> D	<small>DRAWING NUMBER</small> 051-6949	<small>REV.</small> 09
	<small>SCALE</small> NONE	<small>SHT</small> 48	<small>OF</small> 111

8

7

6

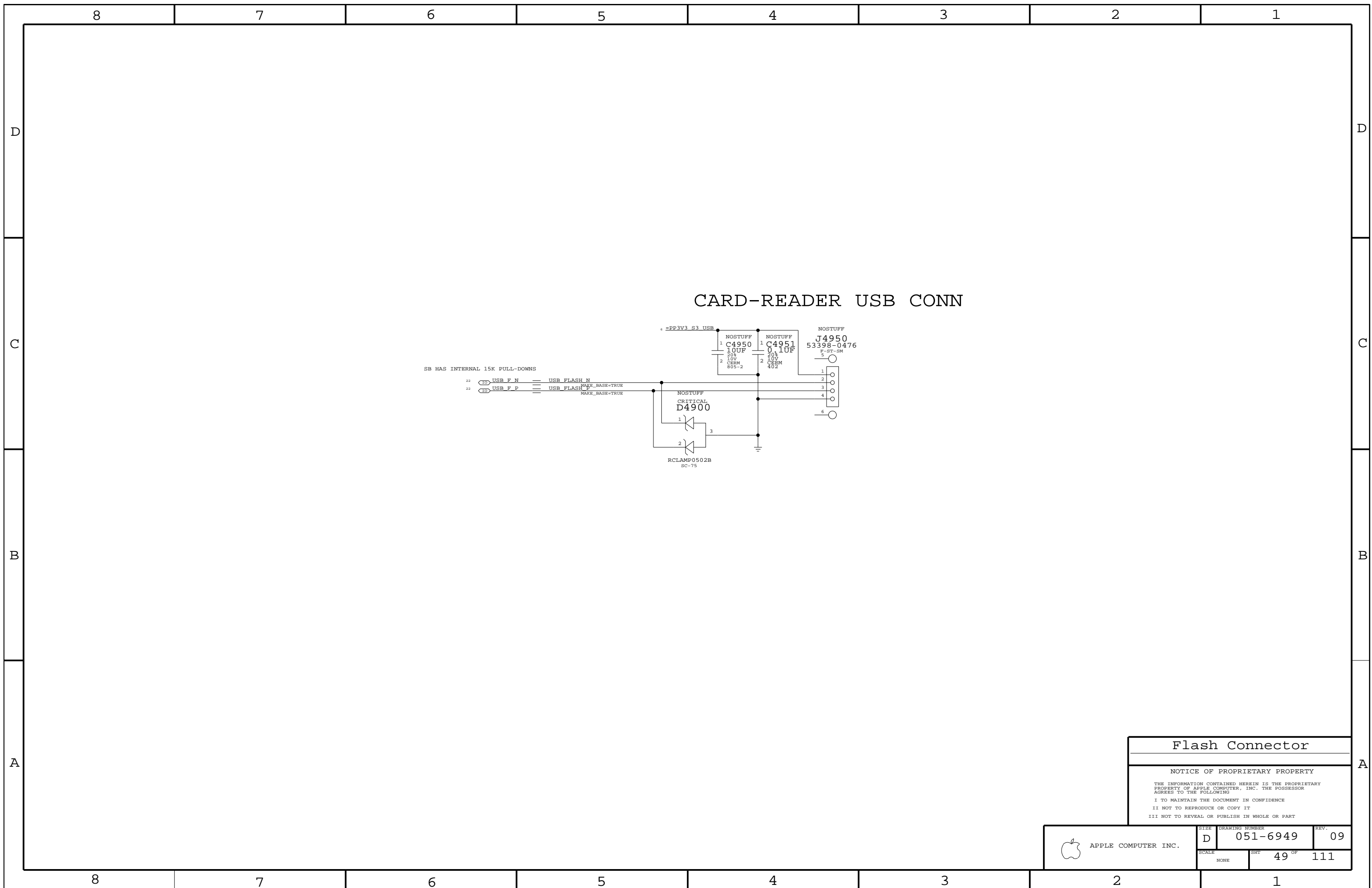
5

4

3

2

1



Flash Connector

NOTICE OF PROPRIETARY PROPERTY

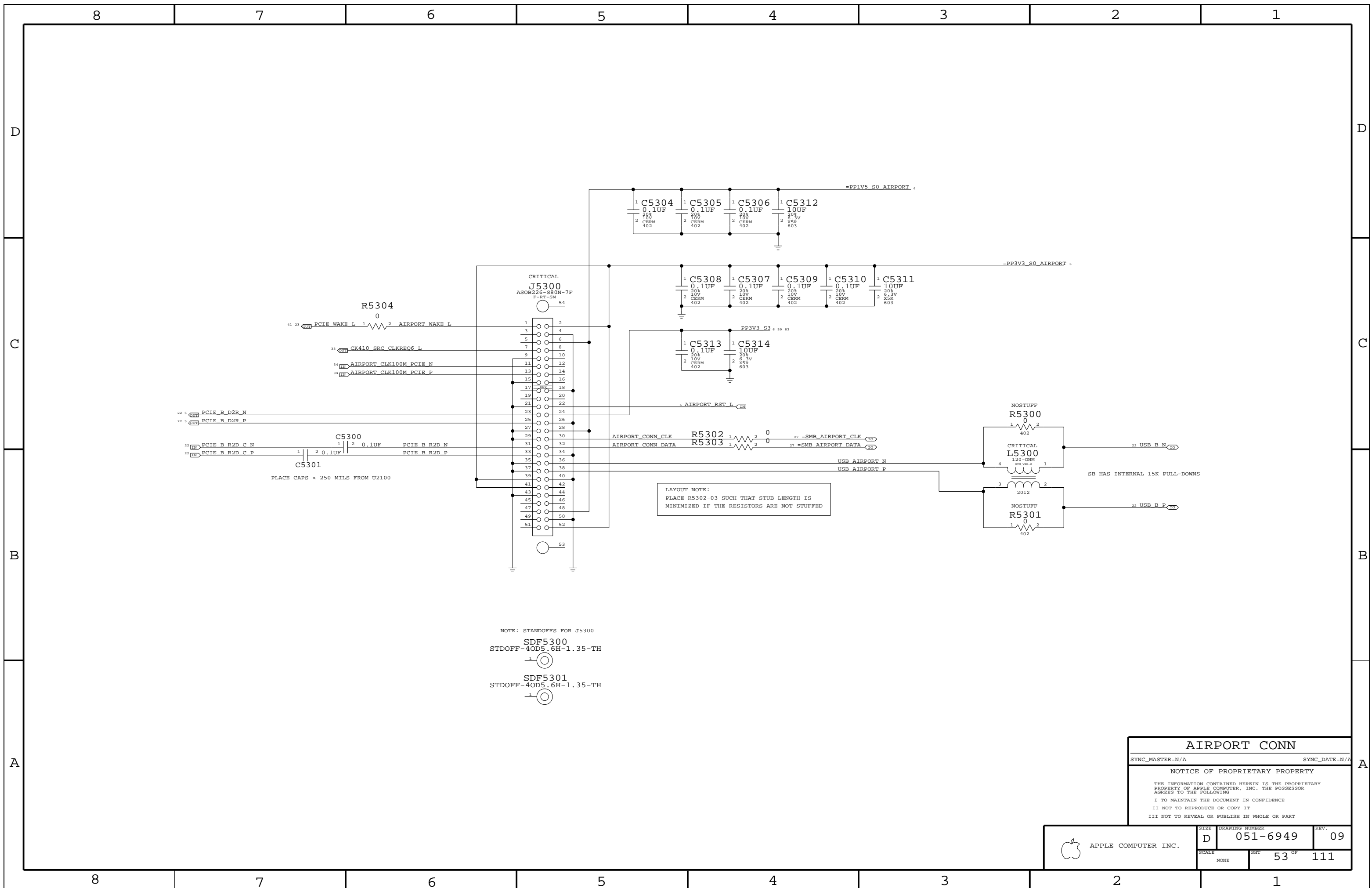
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHIT 49 OF	111



NOTE: STANDOFFS FOR J5300

SDF5300
STDOFF-40D5.6H-1.35-TH

SDF5301
STDOFF-40D5.6H-1.35-TH

LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

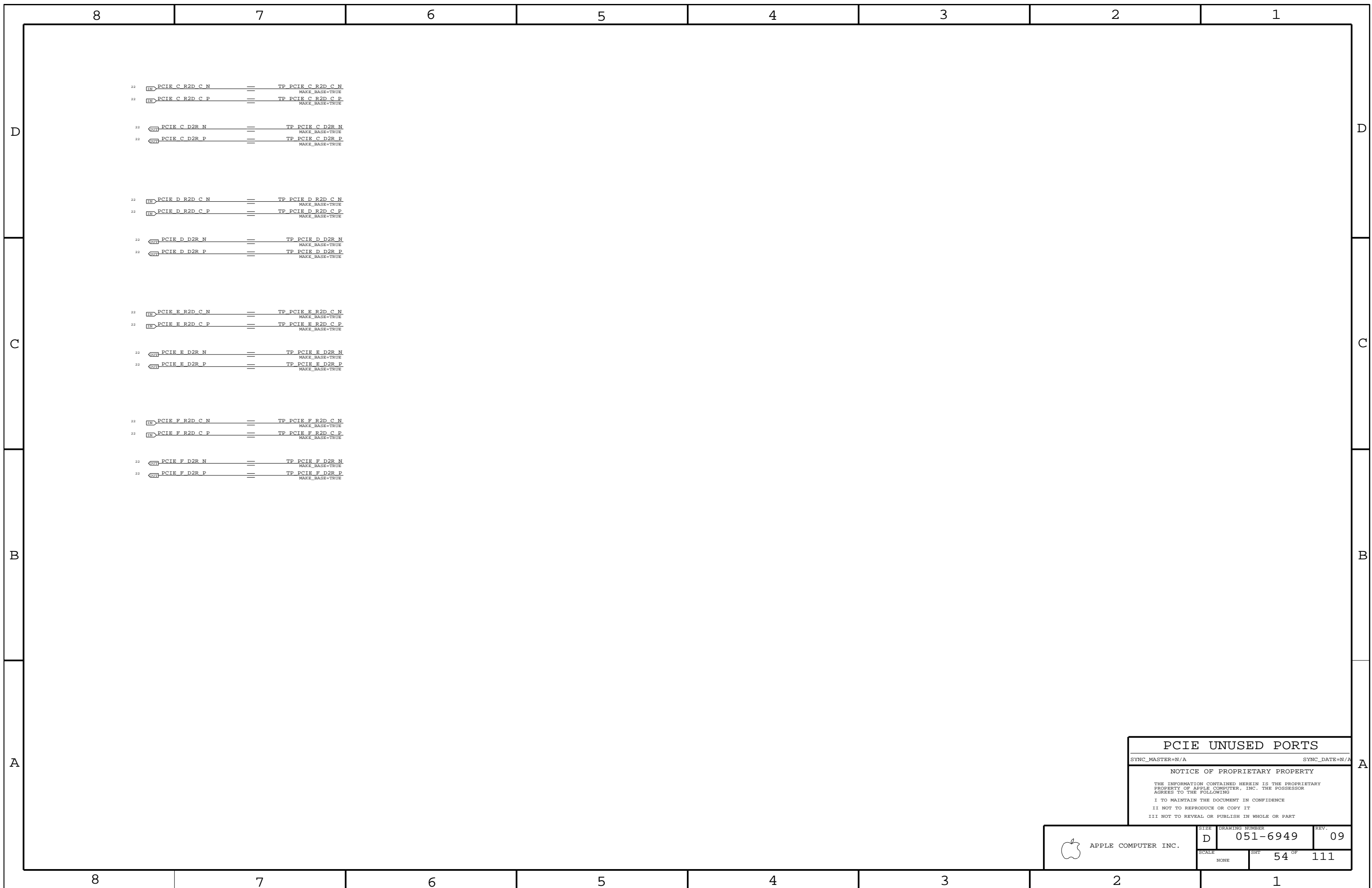
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	
NONE	53	111	



PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

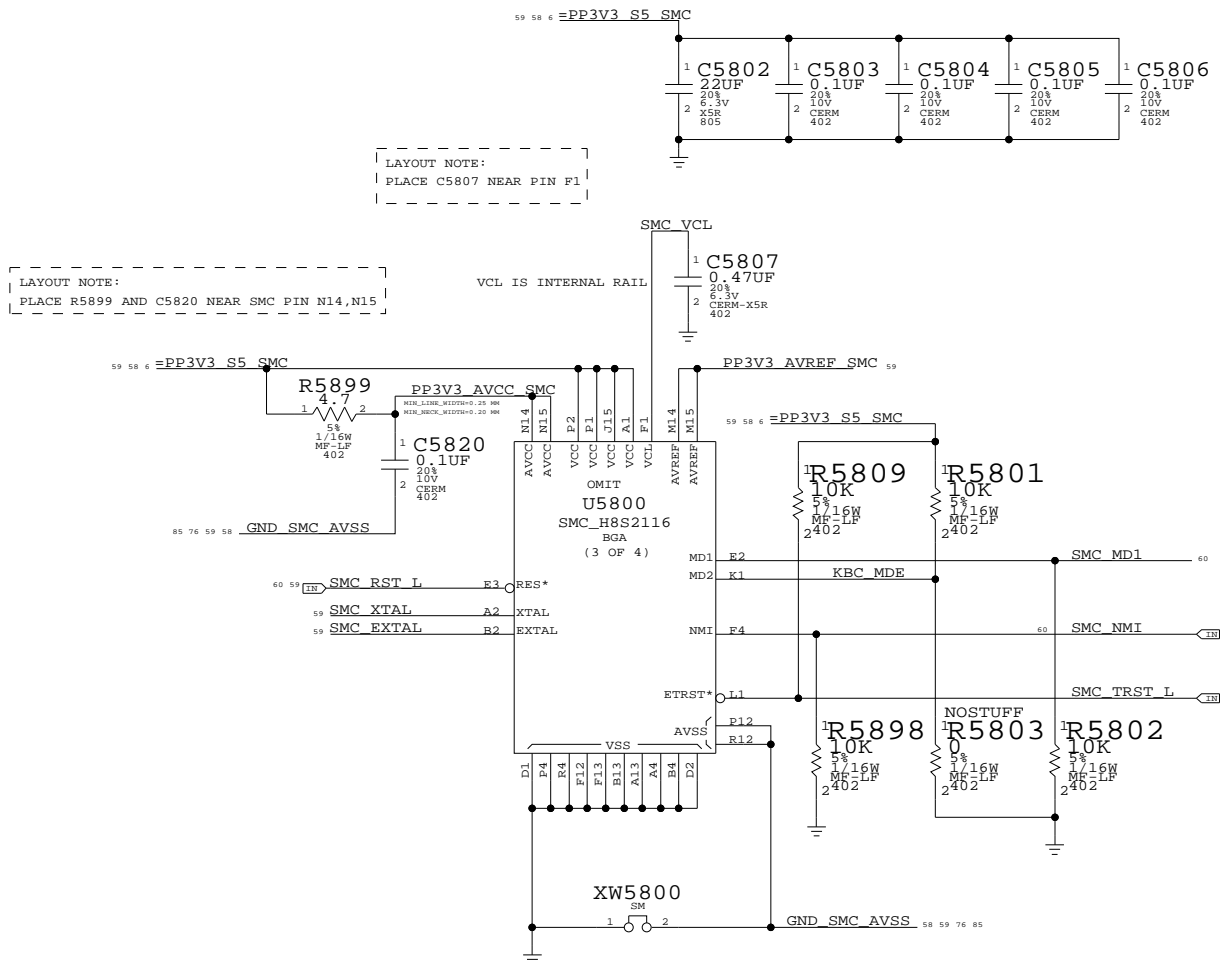
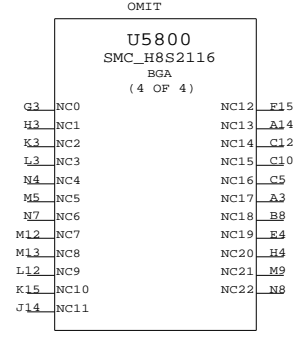
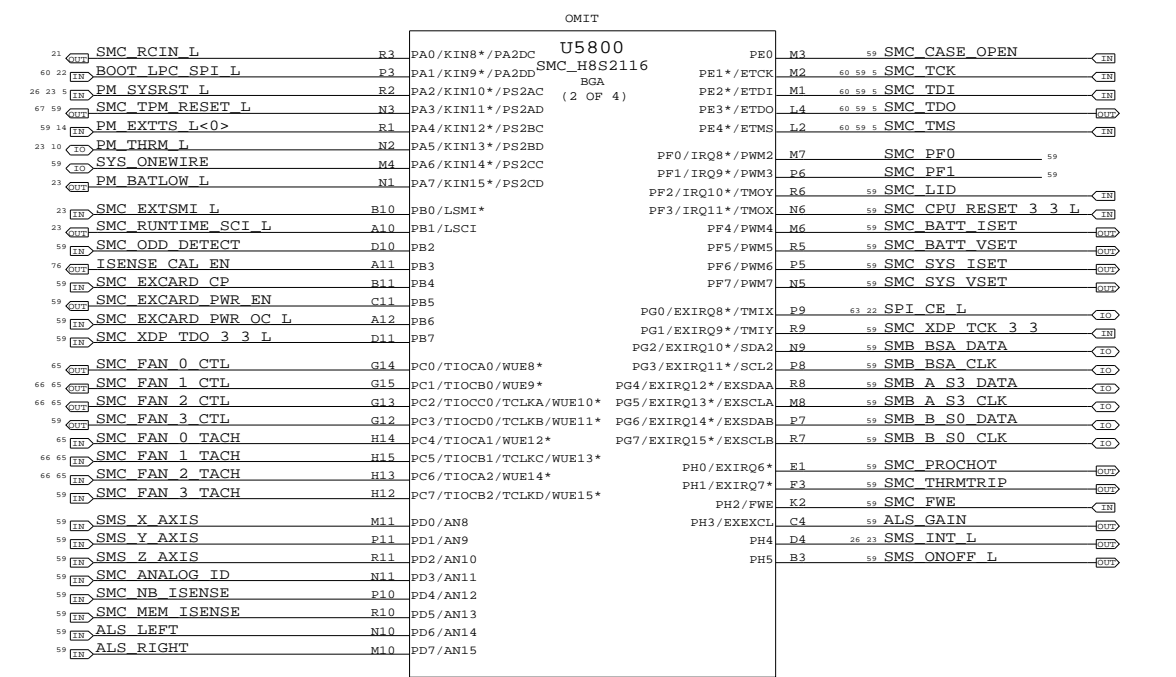
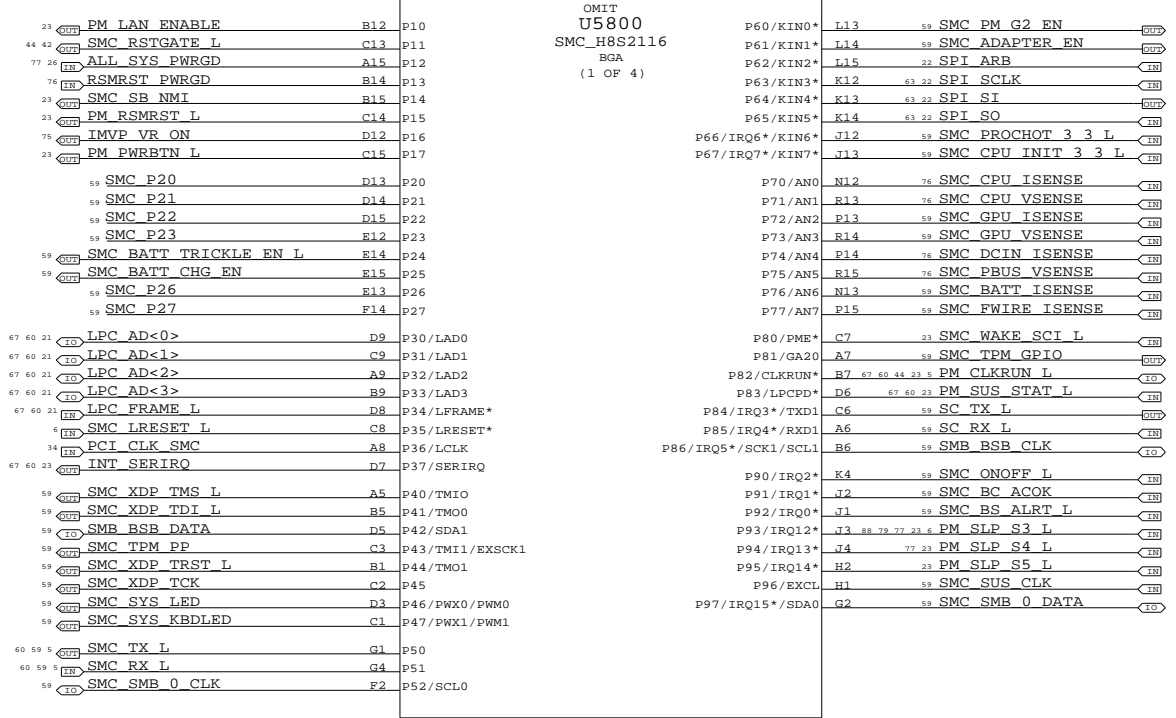
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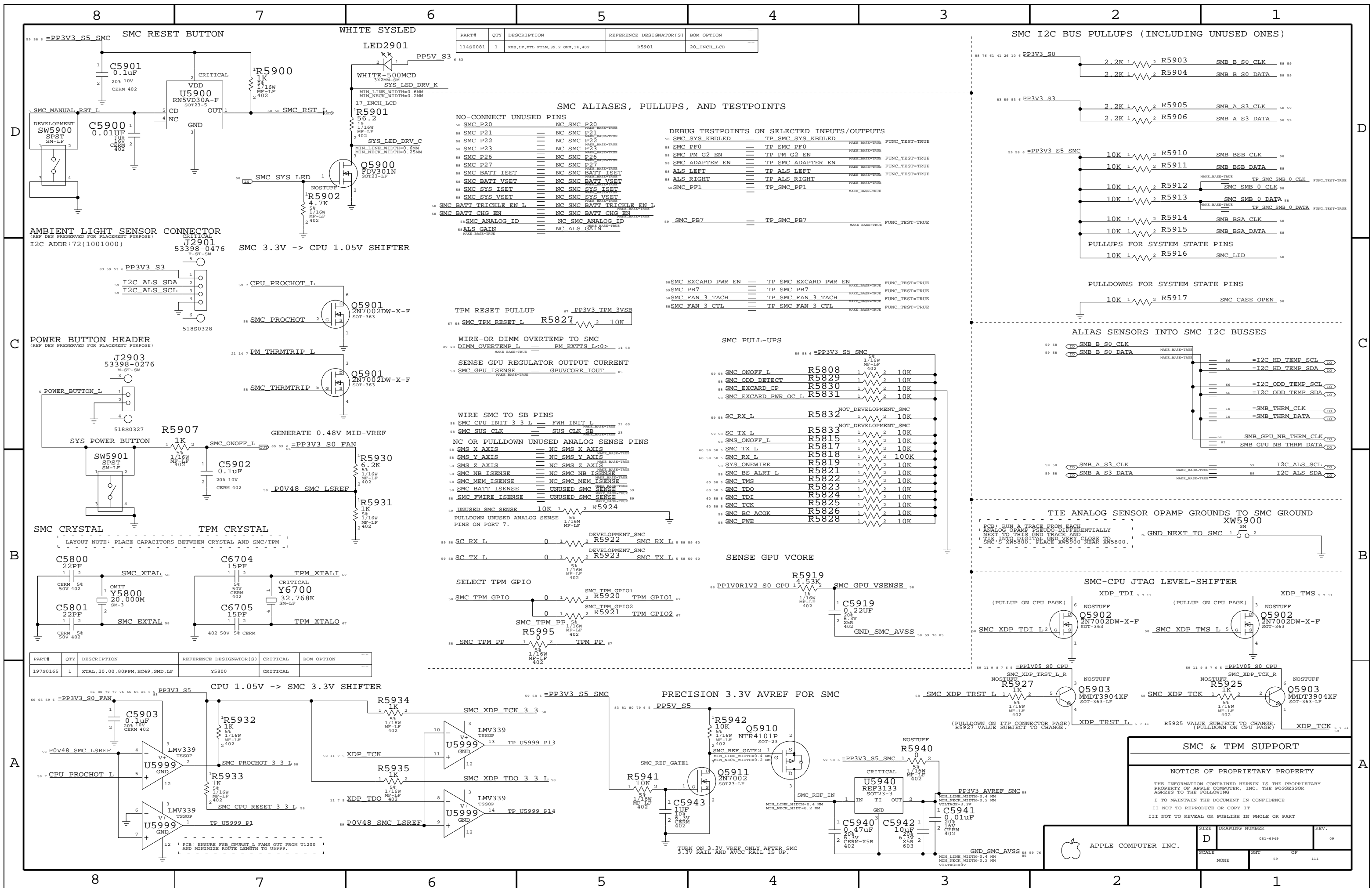
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
	SCALE	SHT	OF
	NONE	54	111

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC
SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC. DRAWING NUMBER 051-6949 REV. 09
SCALE NONE SHEET 58 OF 111



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11450081	1	RES,LP,WTL FILM,39.2 OHM,14,402	R5901	20_INCH_LCD

SMC ALIASES, PULLUPS, AND TESTPOINTS

SMC Alias	SMC Alias	SMC Alias	SMC Alias	SMC Alias	SMC Alias
NO-CONNECT UNUSED PINS	SMC P20	SMC P21	SMC P22	SMC P23	SMC P26
SMC P27	SMC P27	SMC BATT ISET	SMC BATT VSET	SMC SYS ISET	SMC SYS VSET
SMC BATT TRICKLE EN L	SMC BATT TRICKLE EN R	SMC ANALOG ID	SMC ALS GAIN	SMC CPU INIT 3 3 L	SMC SUS CLK
SMC SUS CLK	SMC TX L	SMC TX L	SMC RX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
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SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
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SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
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SMC PULL-UPS

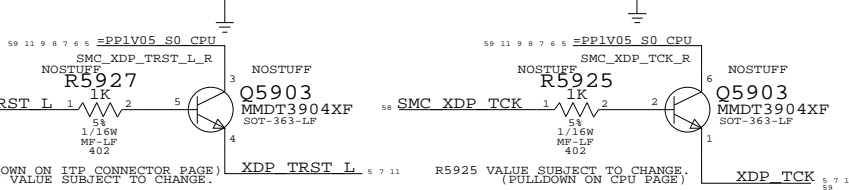
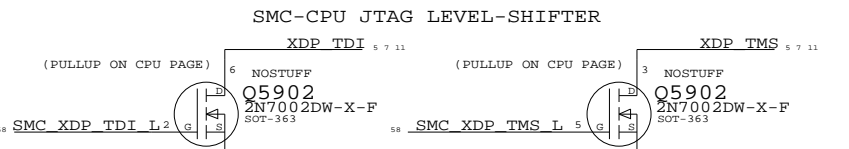
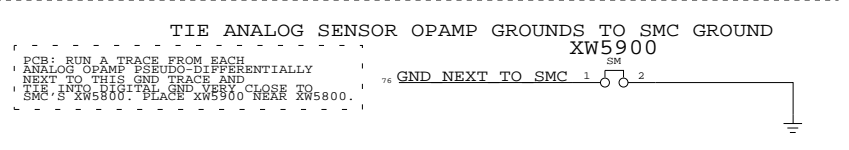
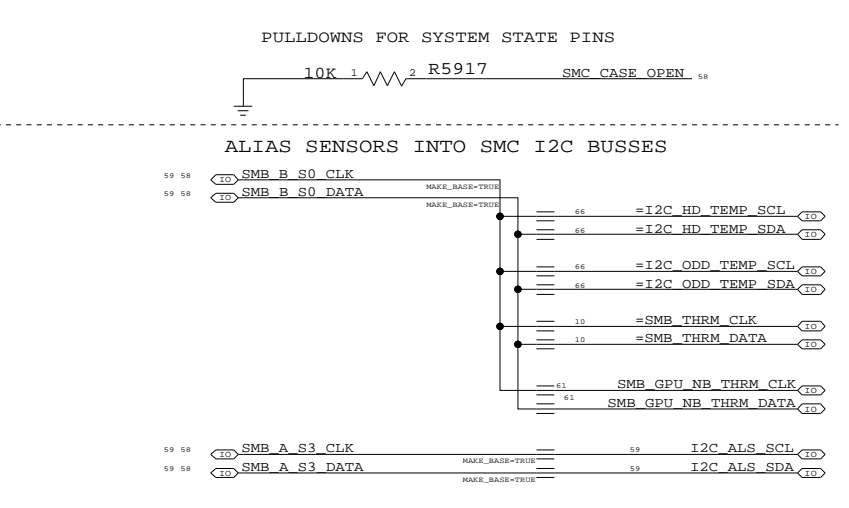
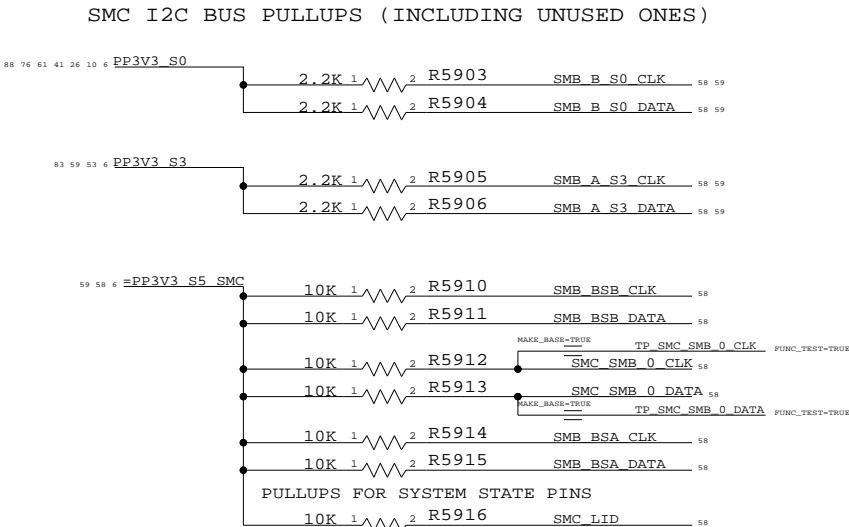
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SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L

SMC PULL-UPS

SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin	SMC Pin
SMC ONOFF L	SMC ODD DETECT	SMC EXCARD CP	SMC EXCARD PWR OC L	SC RX L	SC TX L
SC TX L	SMS ONOFF L	SMC TX L	SMC RX L	SMC ONEWIRE	SMC BS ALRT L
SMC TMS	SMC TDO	SMC TDI	SMC BC ACOK	SMC FWE	SMC CPU INIT 3 3 L
SMC CPU INIT 3 3 L	SMC SUS CLK	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L
SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L	SMC TX L



SMC & TPM SUPPORT

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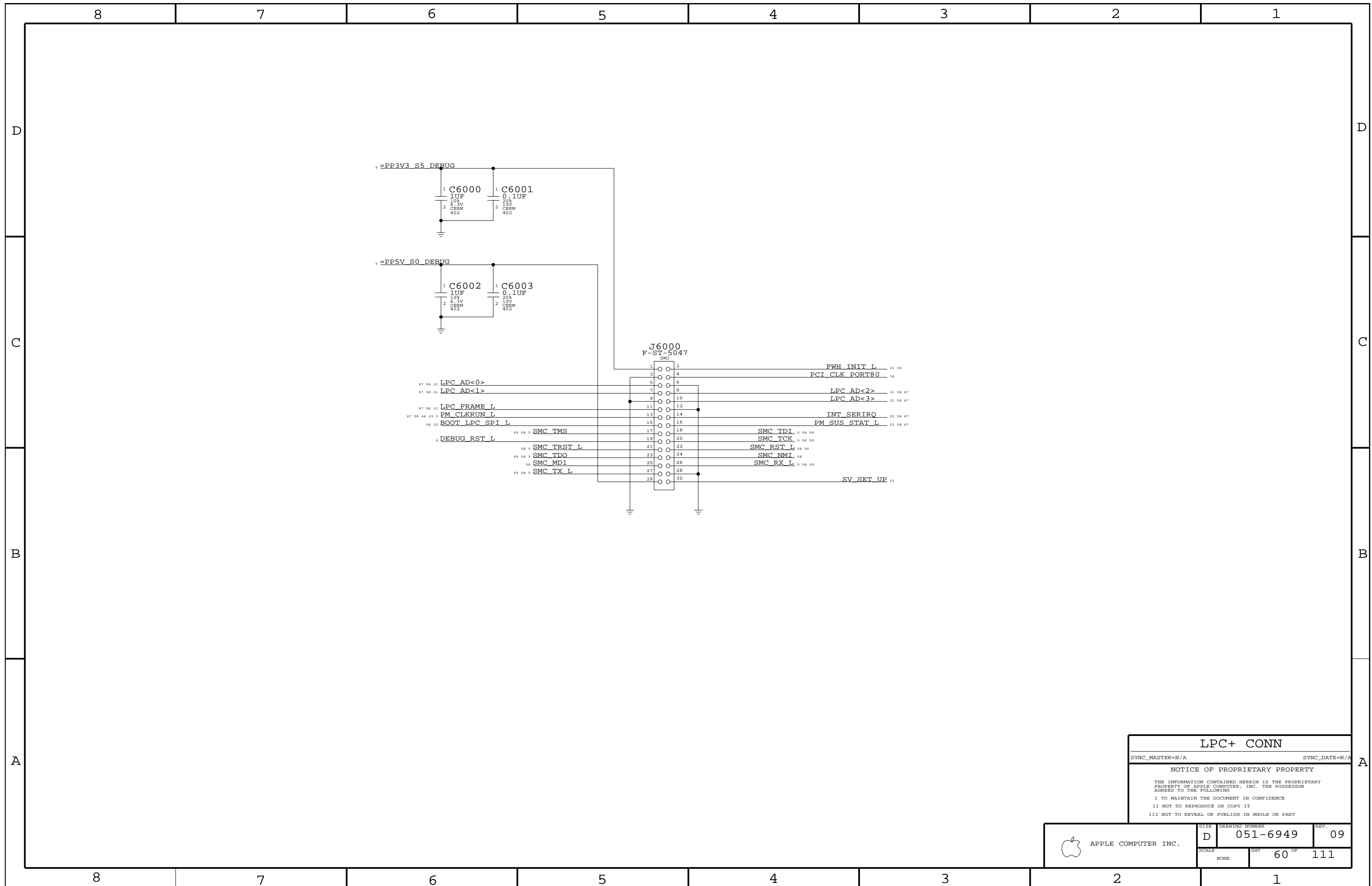
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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHEET	OF
NONE	59	111

APPLE COMPUTER INC.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

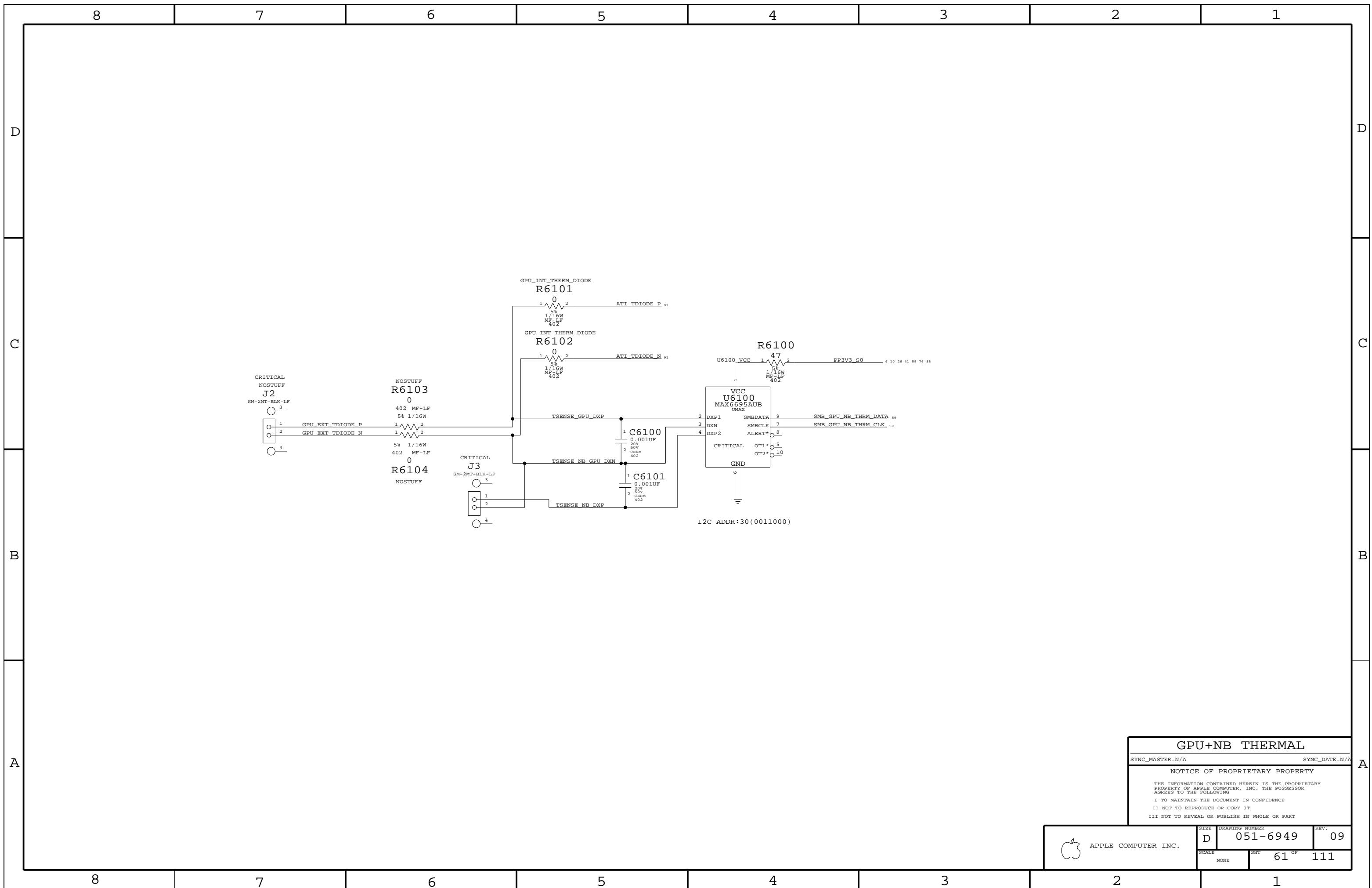
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 60 OF 111	



GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A

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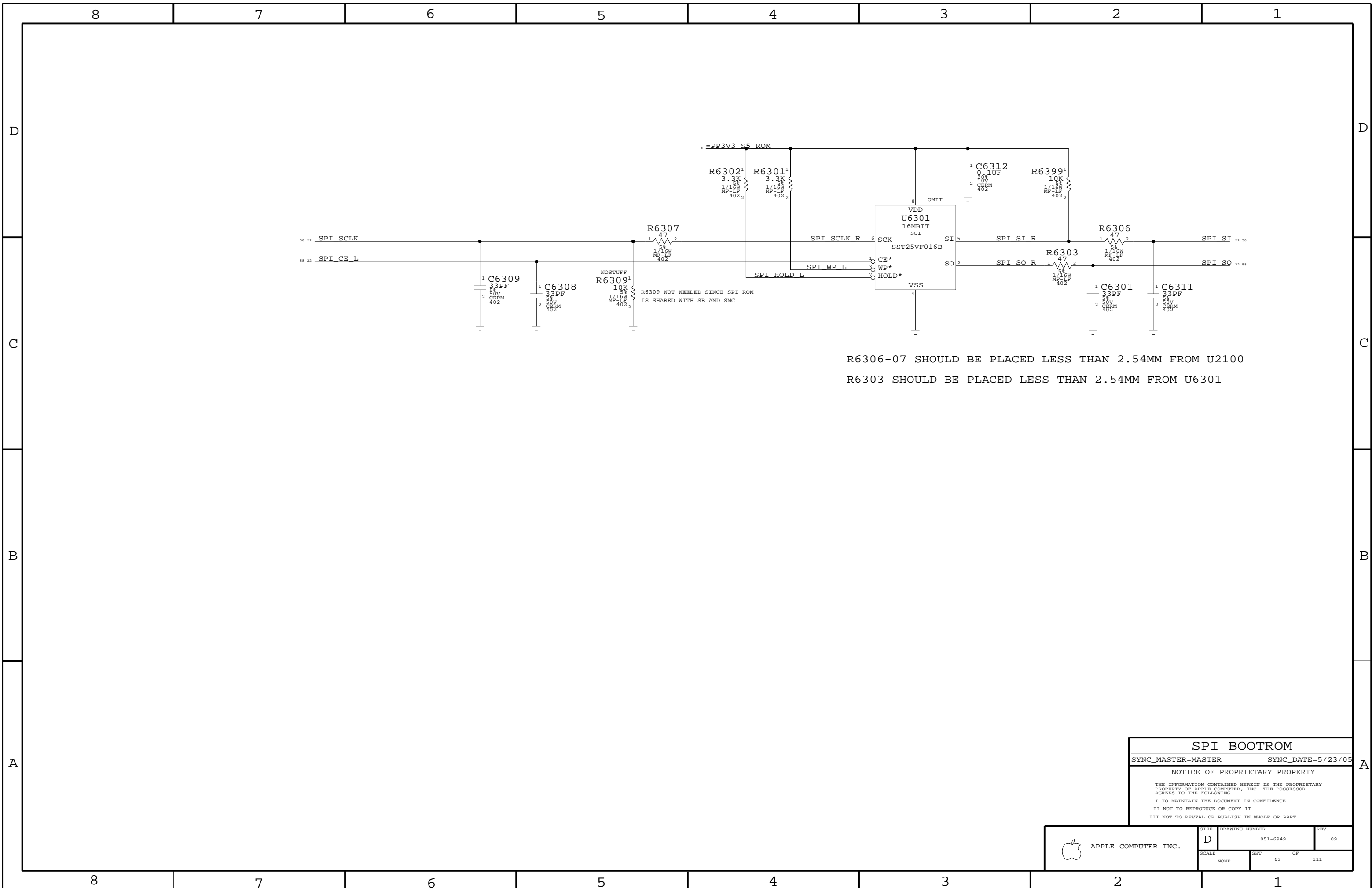
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	D	051-6949	09
SCALE	SHT	61 OF 111	
NONE			



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

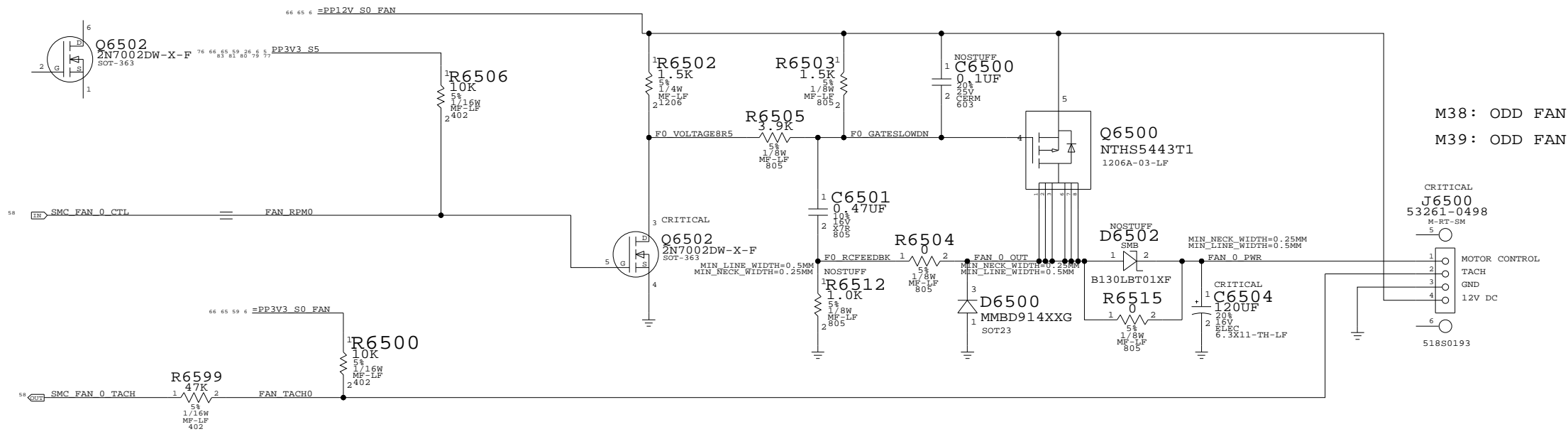
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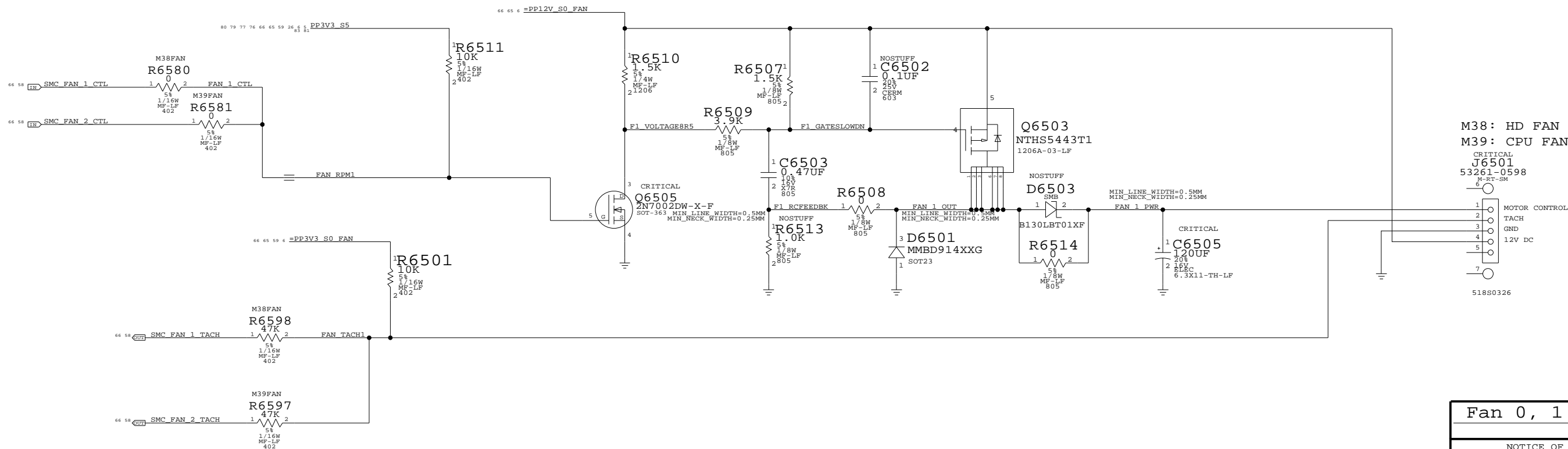
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHEET 63	OF 111

FAN 0



FAN 1



Fan 0, 1 & System Temp

NOTICE OF PROPRIETARY PROPERTY

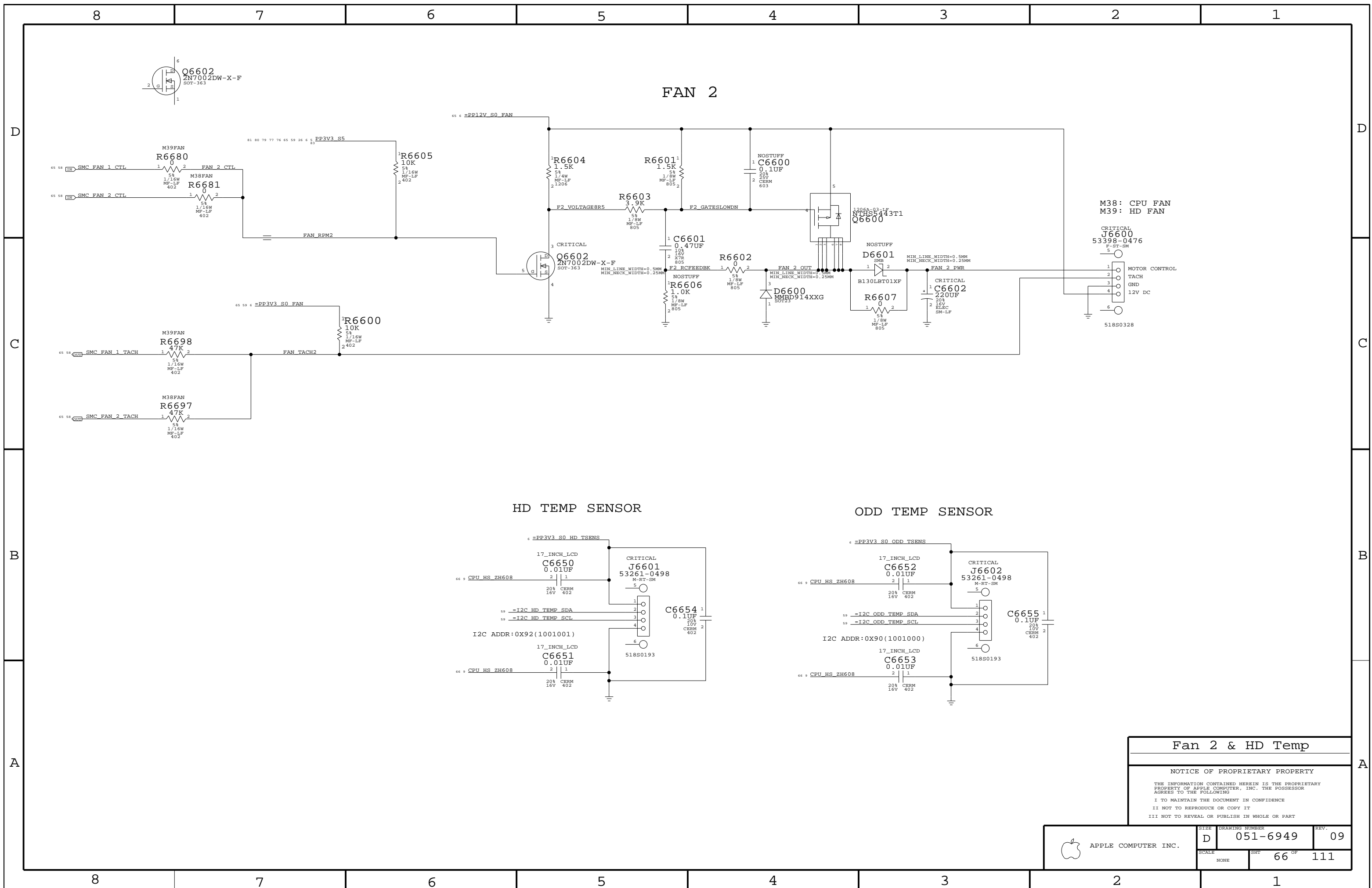
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SCALE		SHT	OF
NONE		65	111



FAN 2

HD TEMP SENSOR

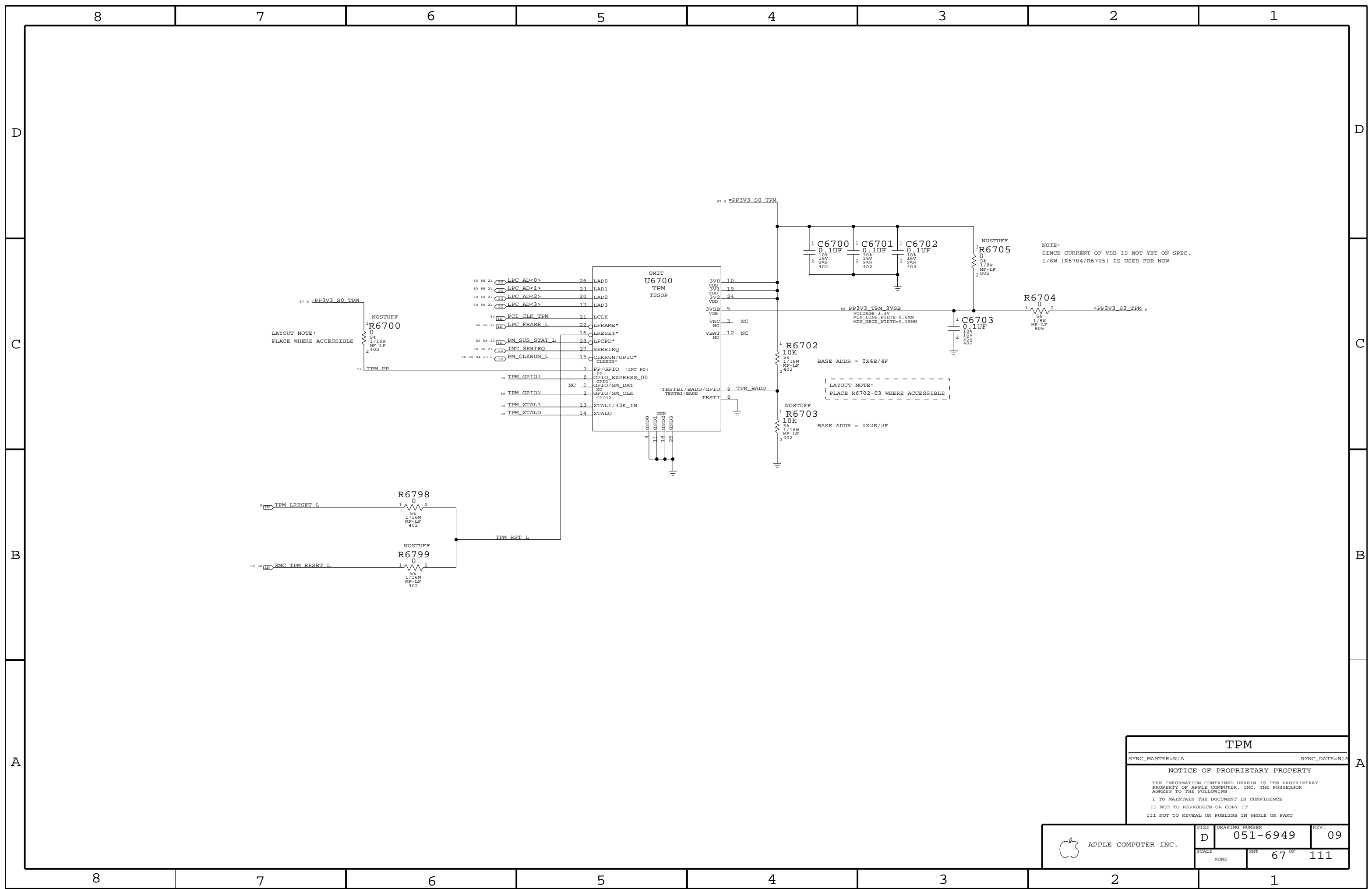
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	REV.
NONE	66	111	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

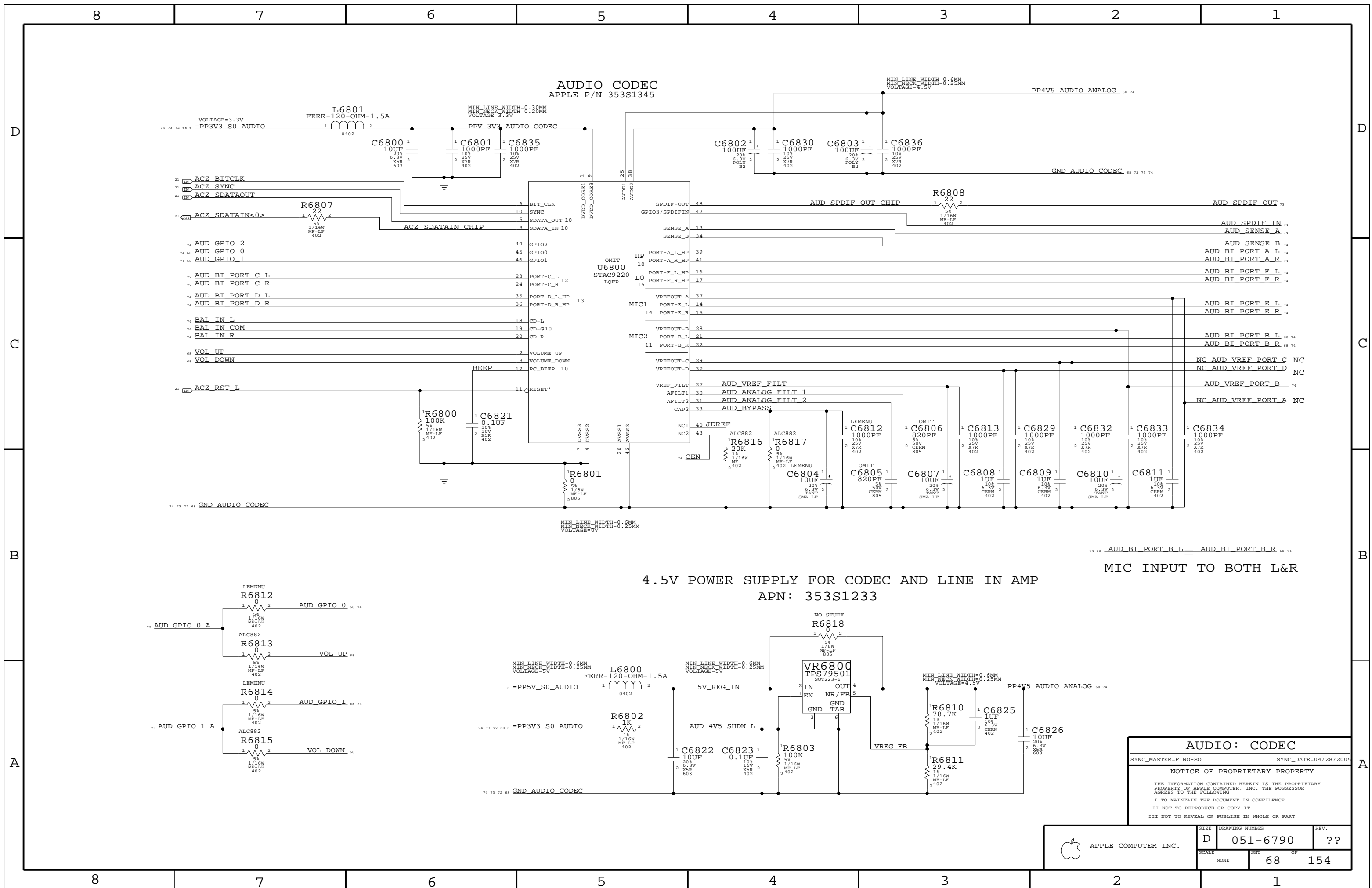
SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6949	09
SCALE	SHT	67 OF	111
NONE			

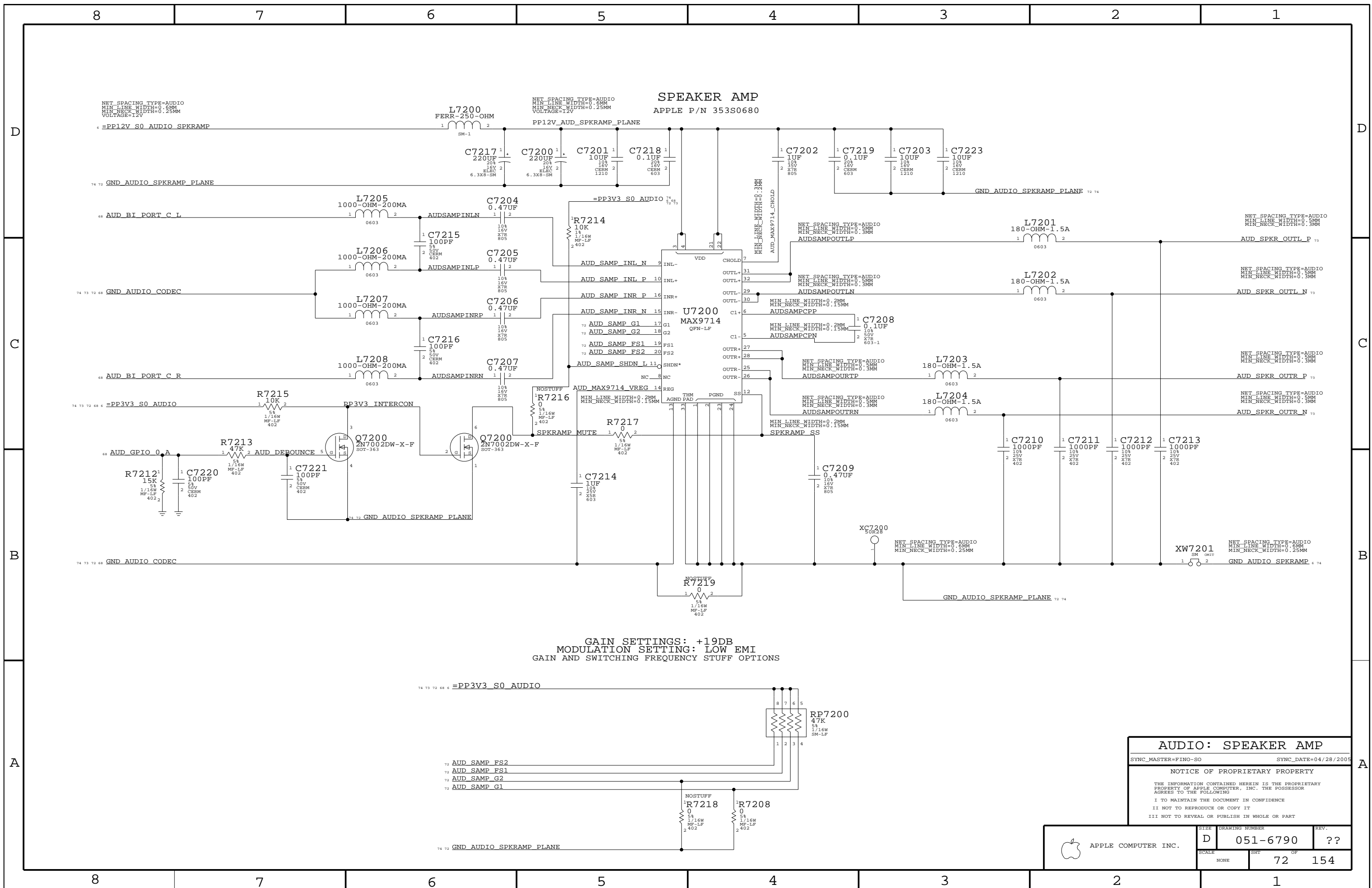


AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC
SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	NONE	SHT	OF
		68	154

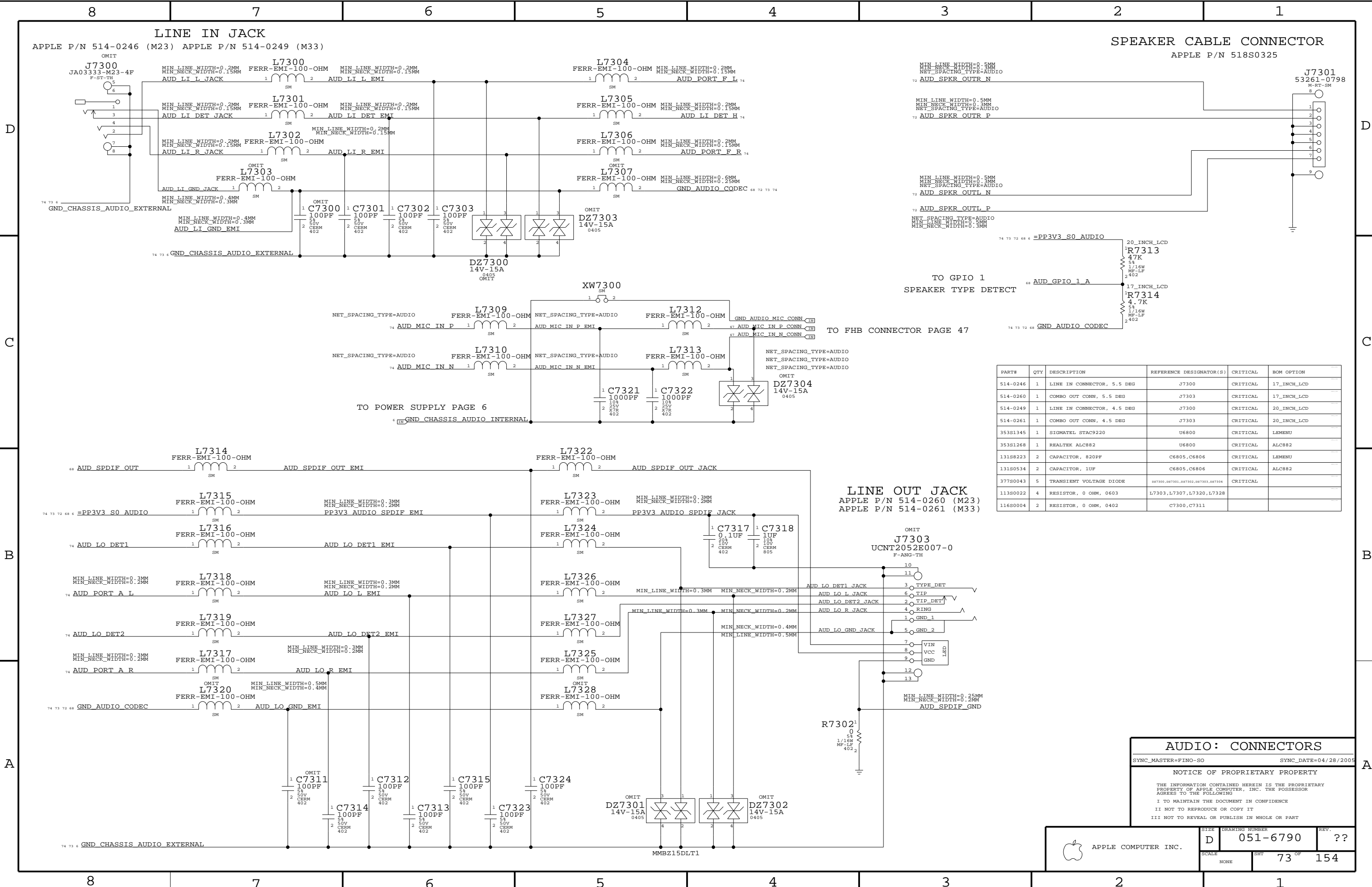


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
SCALE	NONE	SHT	OF
		72	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	J7300	CRITICAL	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 5.5 DEG	J7303	CRITICAL	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 4.5 DEG	J7300	CRITICAL	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	J7303	CRITICAL	20_INCH_LCD
353S1345	1	SIGMATEL STAC9220	U6800	CRITICAL	LEMENU
353S1268	1	REALTEK ALC882	U6800	CRITICAL	ALC882
131S8223	2	CAPACITOR, 820PF	C6805,C6806	CRITICAL	LEMENU
131S0534	2	CAPACITOR, 1UF	C6805,C6806	CRITICAL	ALC882
377S0043	5	TRANSIENT VOLTAGE DIODE	DZ7300,DZ7301,DZ7302,DZ7303,DZ7304	CRITICAL	
113S0022	4	RESISTOR, 0 OHM, 0603	L7303,L7307,L7320,L7328		
116S0004	2	RESISTOR, 0 OHM, 0402	C7300,C7311		

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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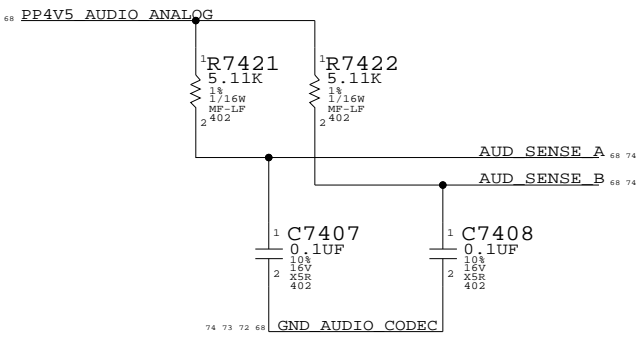
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
SCALE	NONE	SHT	73 OF 154

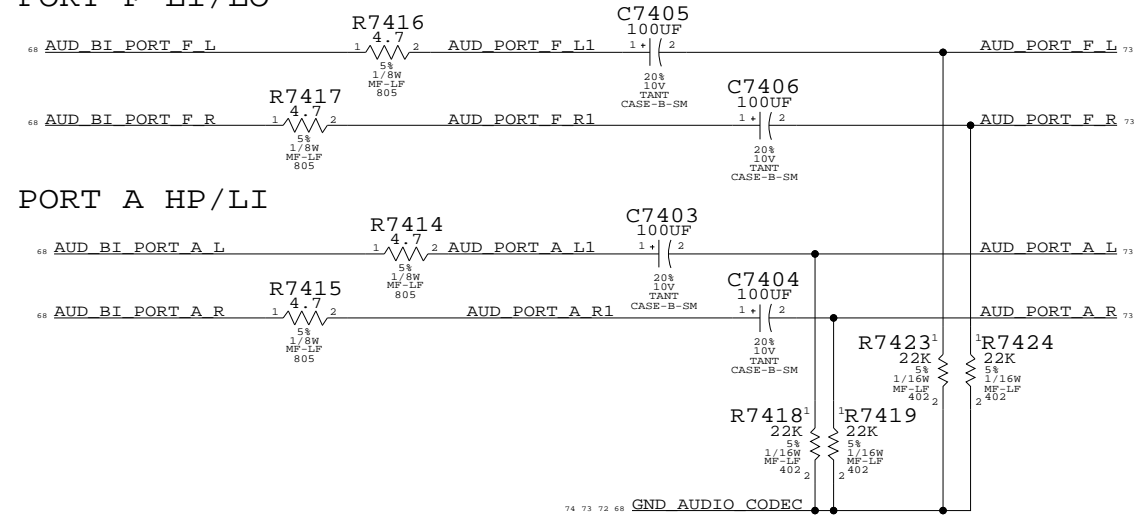
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



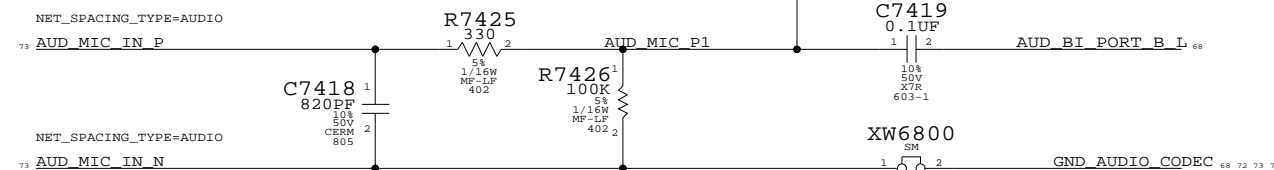
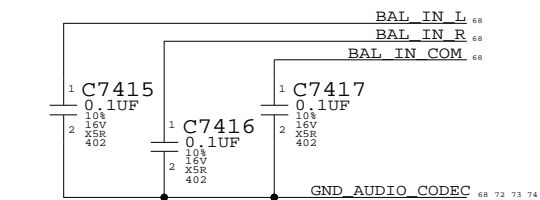
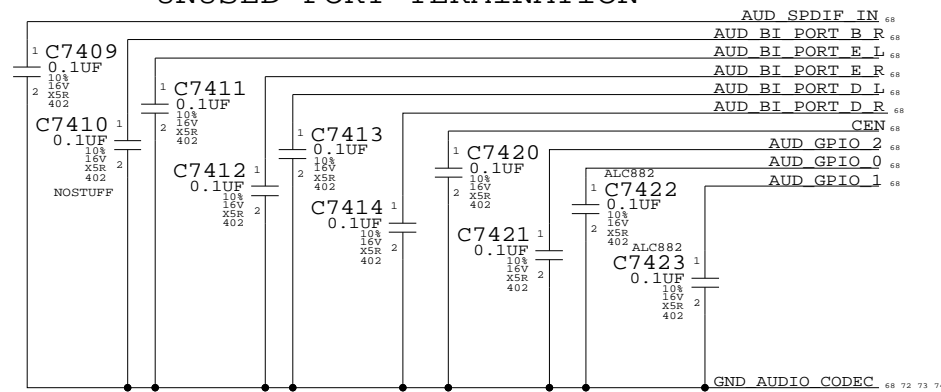
USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

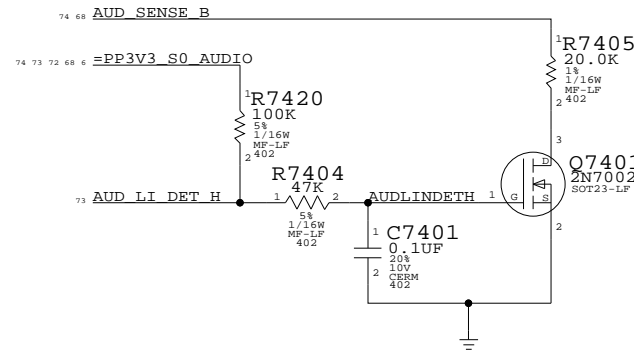
PORT F LI/LO



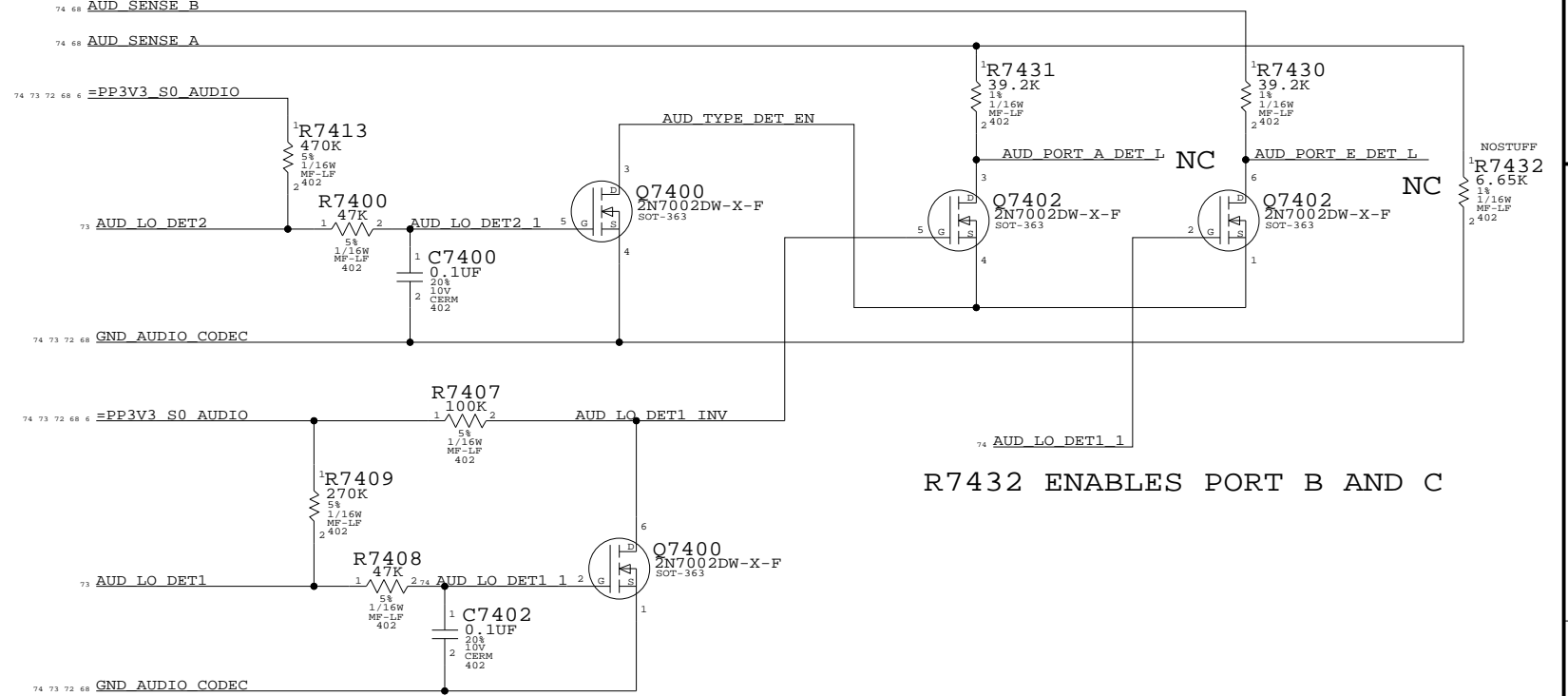
UNUSED PORT TERMINATION



PORT F (LI/LO) PLUG DETECT

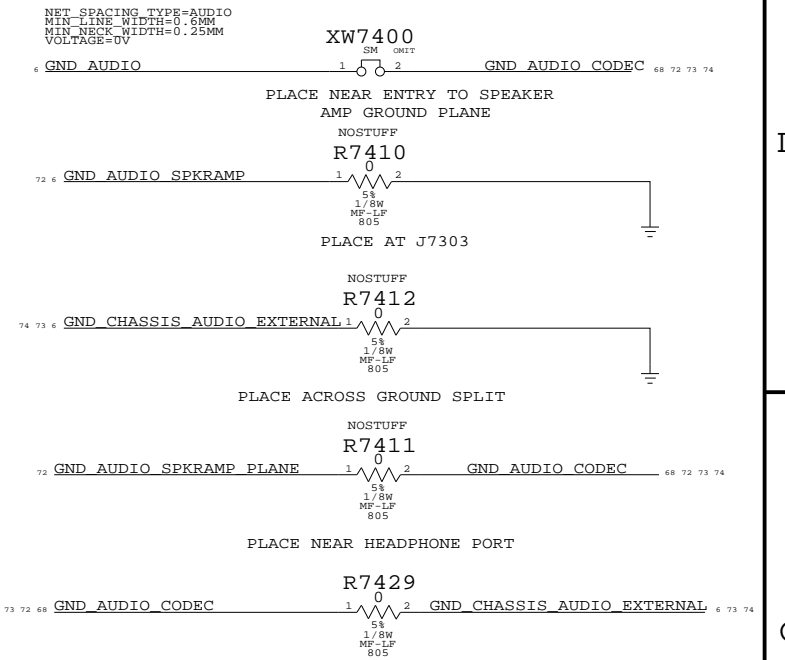


PORT A/H (HP/LI/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



R7432 ENABLES PORT B AND C

AUDIO GROUND RETURNS



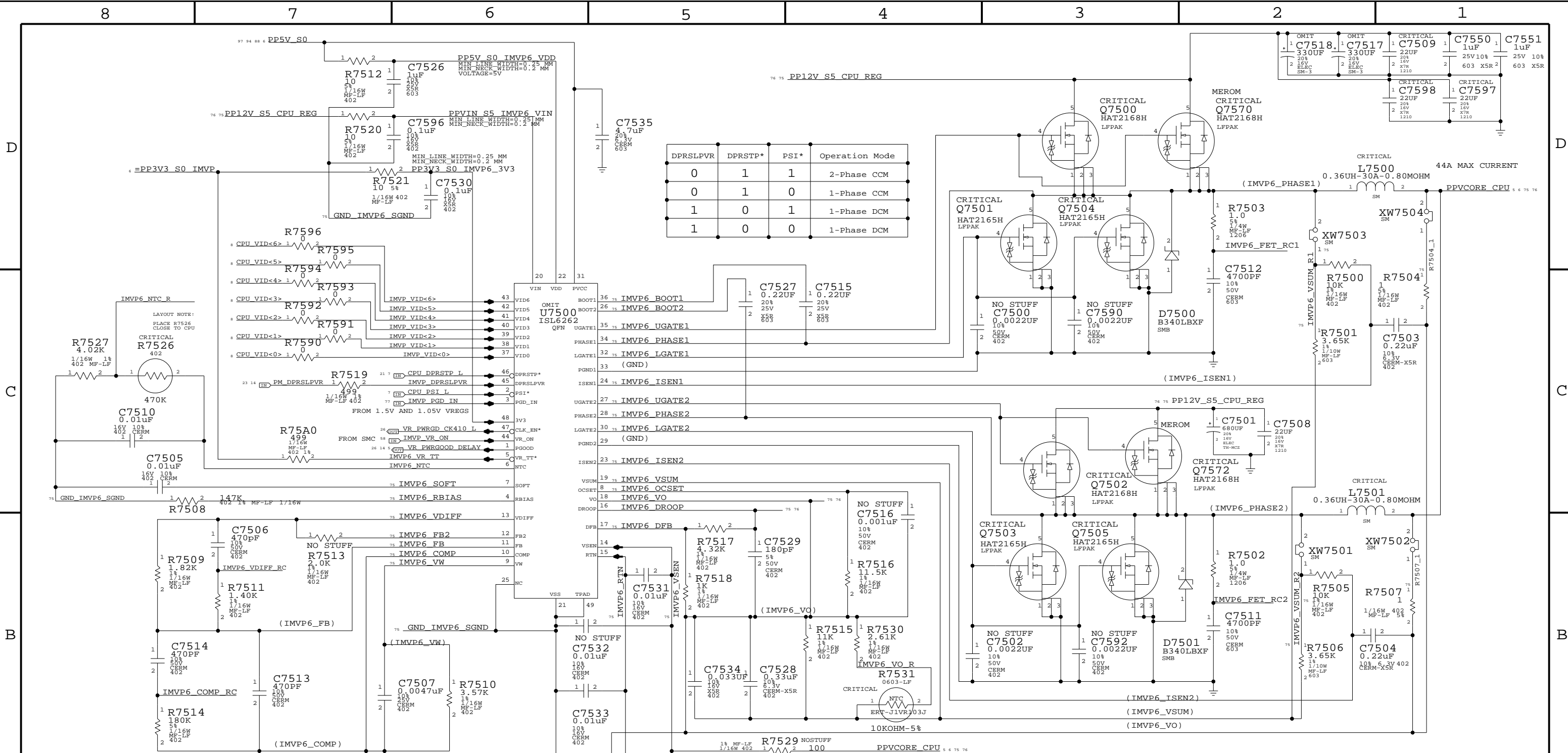
AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
SCALE	NONE	SHT	OF
		74	154



Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_VBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/08/2005

NOTICE OF PROPRIETARY PROPERTY

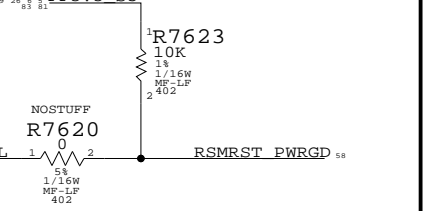
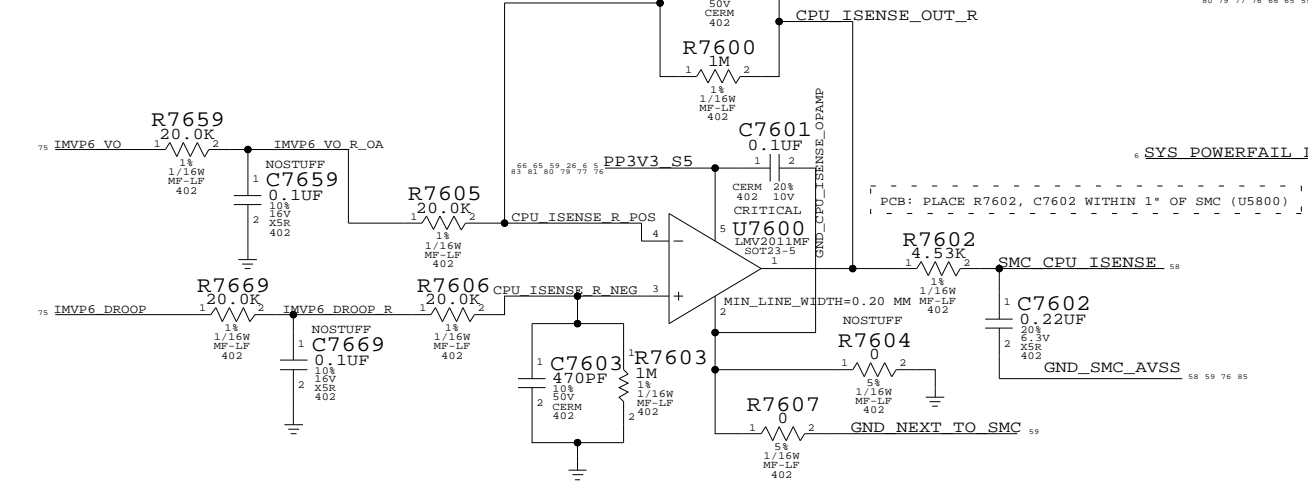
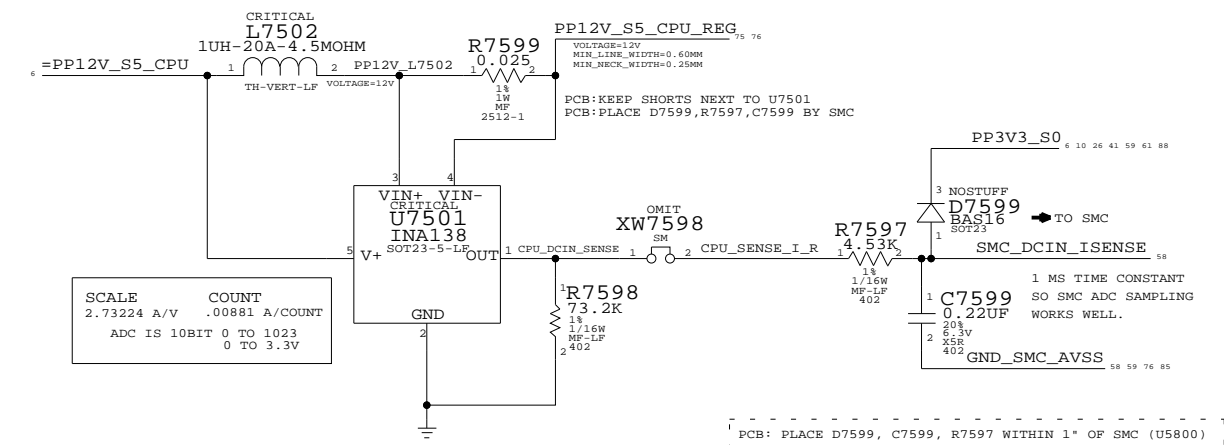
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	SHEET	OF	
	75	111	

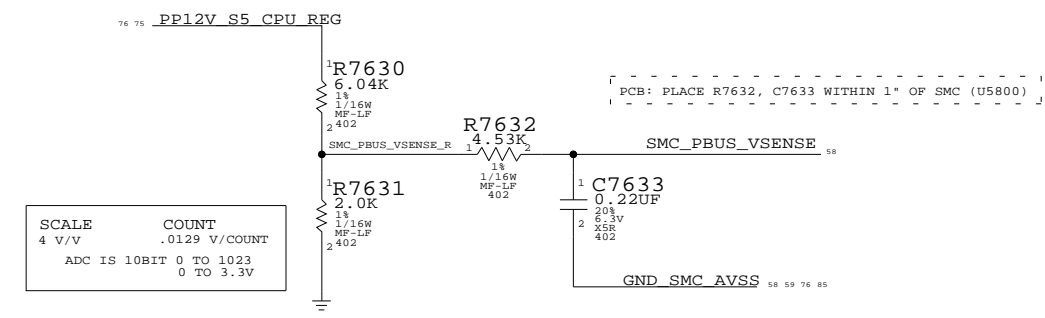
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

SMC PWRGD PULLUP



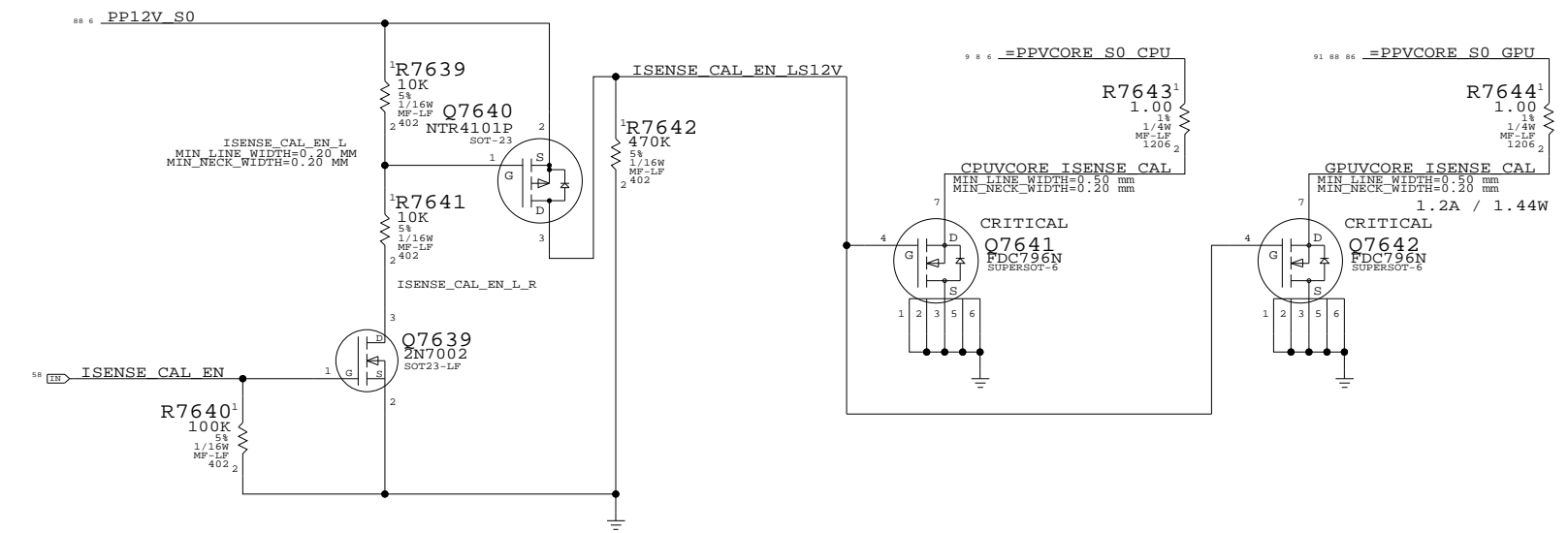
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



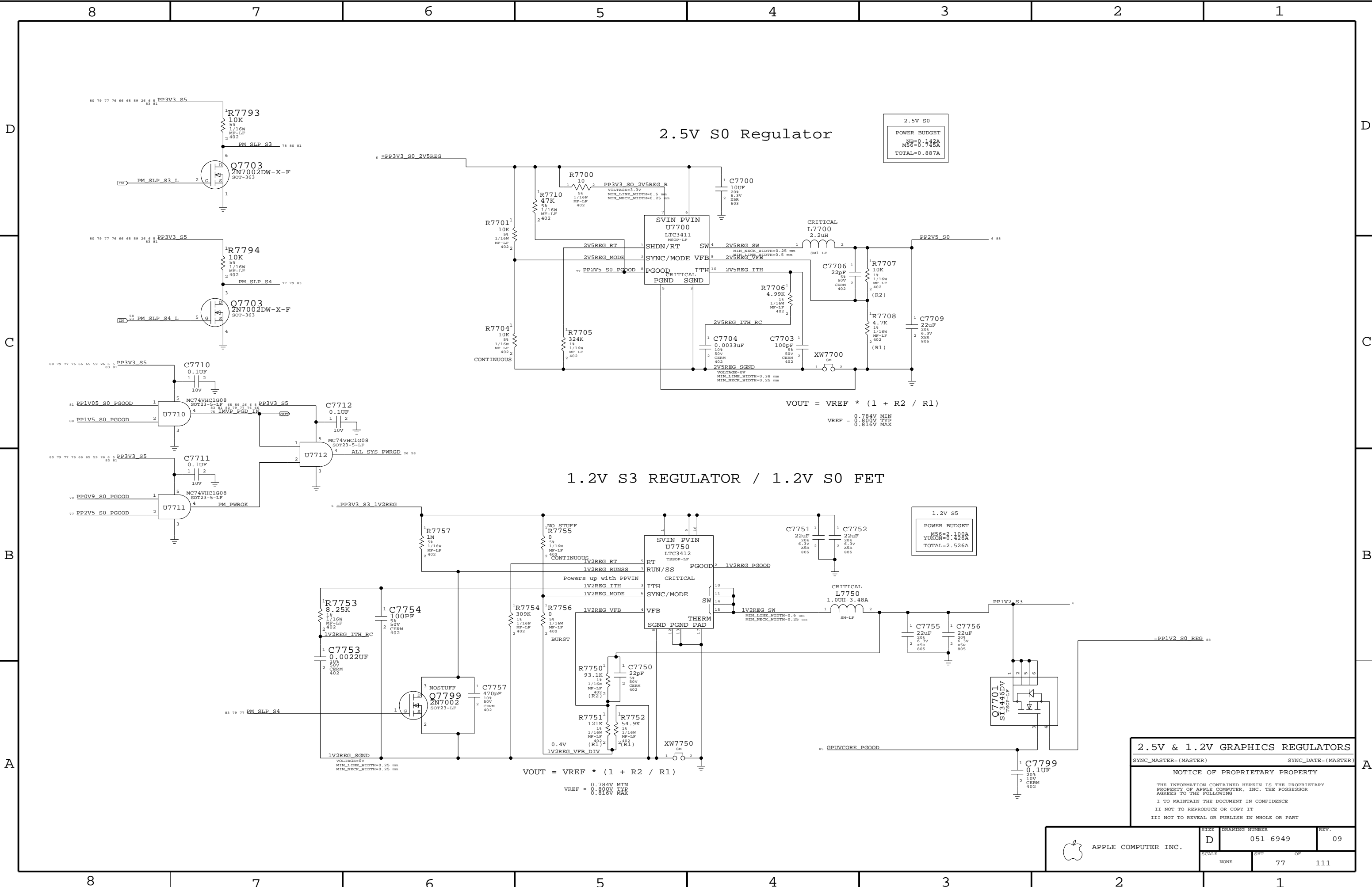
PROCESSOR VCORE SENSE



Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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2.5V S0 Regulator

2.5V S0
POWER BUDGET
MSE=1.42A
MBS=0.745A
TOTAL=0.887A

$V_{OUT} = V_{REF} * (1 + R2 / R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S5
POWER BUDGET
MSE=1.42A
YUSEN=0.108A
TOTAL=2.526A

$V_{OUT} = V_{REF} * (1 + R2 / R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

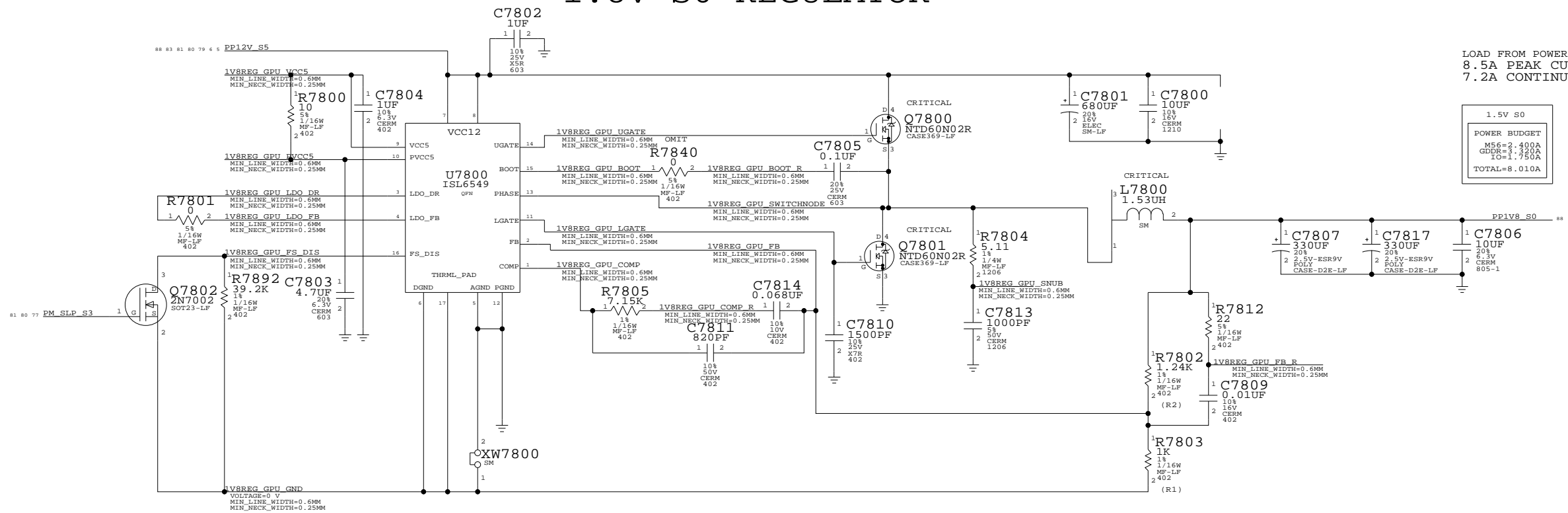
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	D	051-6949	09
SCALE	SHT	OF	
NONE	77	111	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480514	1	5.11 OHM 0402 1% 1/16W LF	R7840		

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0	
POWER BUDGET	
M56=	2.400A
GDDR=	3.200A
IO=	1.750A
TOTAL=	8.010A

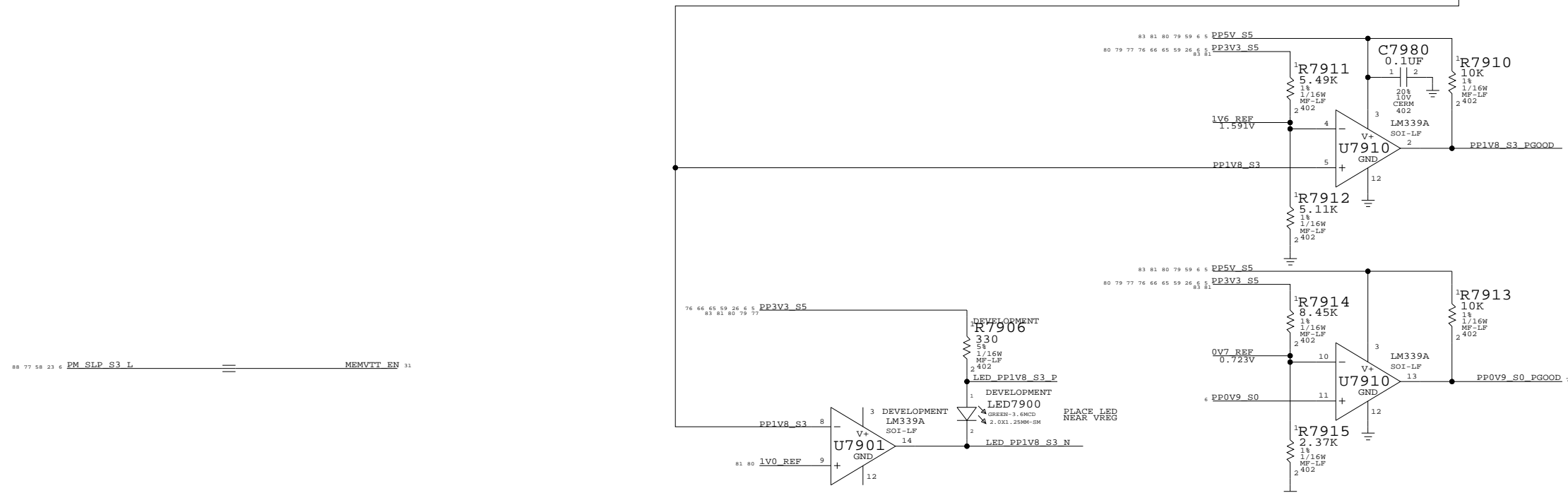
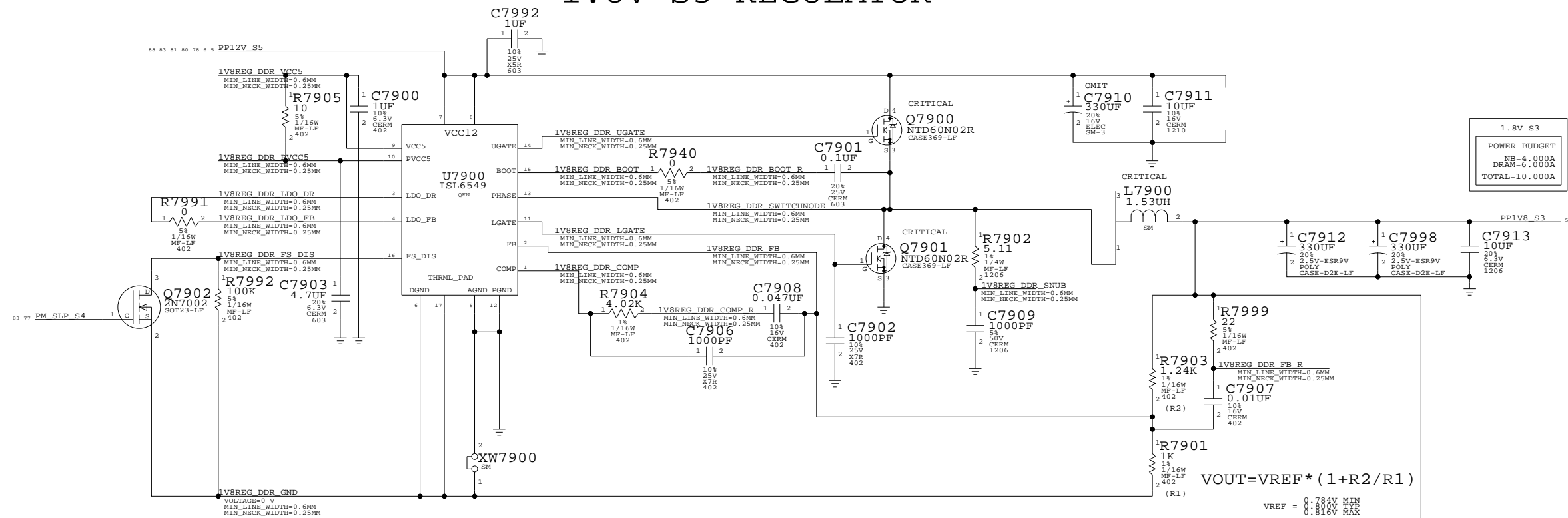
$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.8V GDDR REGULATOR
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-6949	09
SCALE	SHT		
NONE	78 OF 111		

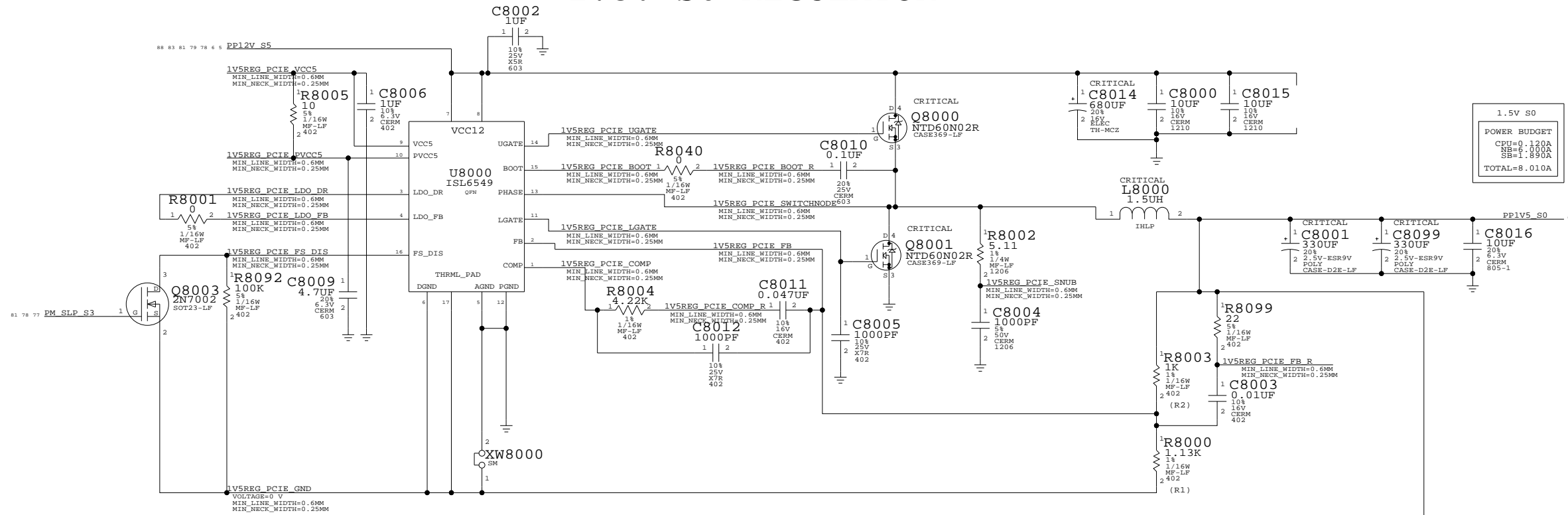
1.8V S3 REGULATOR



1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	79 OF	111
NONE			

1.5V S0 REGULATOR

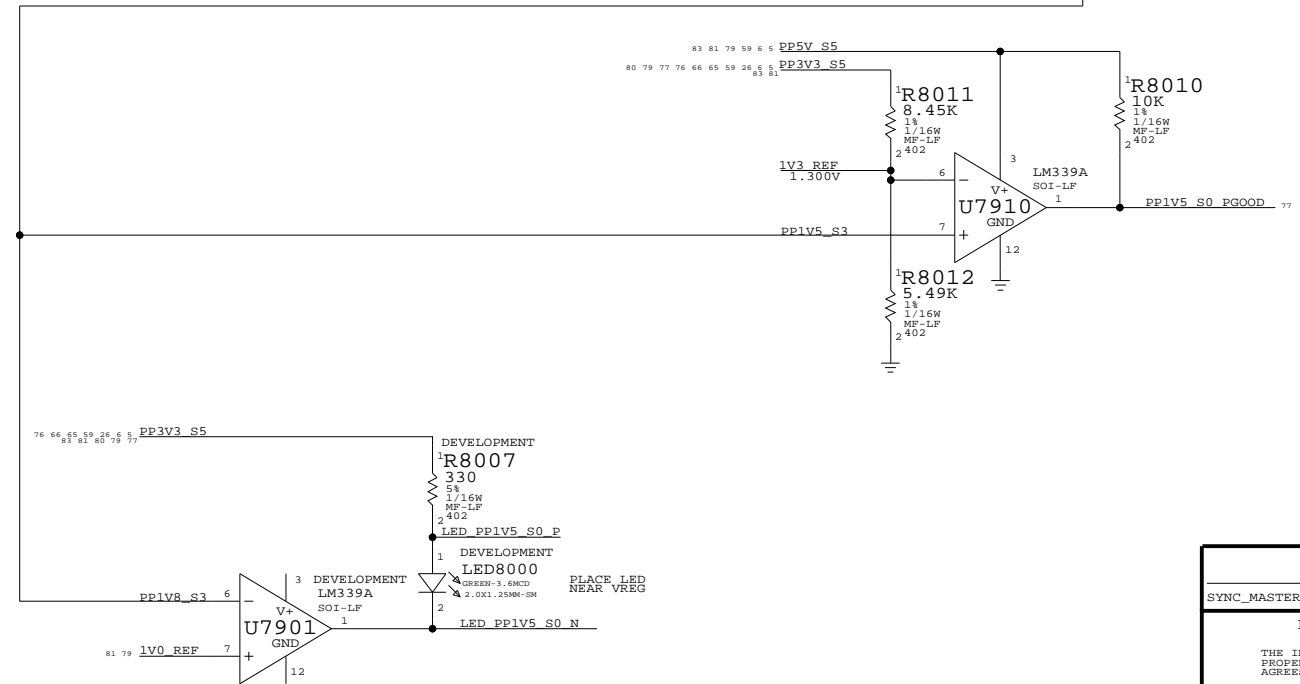


$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$0.800V \text{ TYP}$$

$$0.816V \text{ MAX}$$



1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

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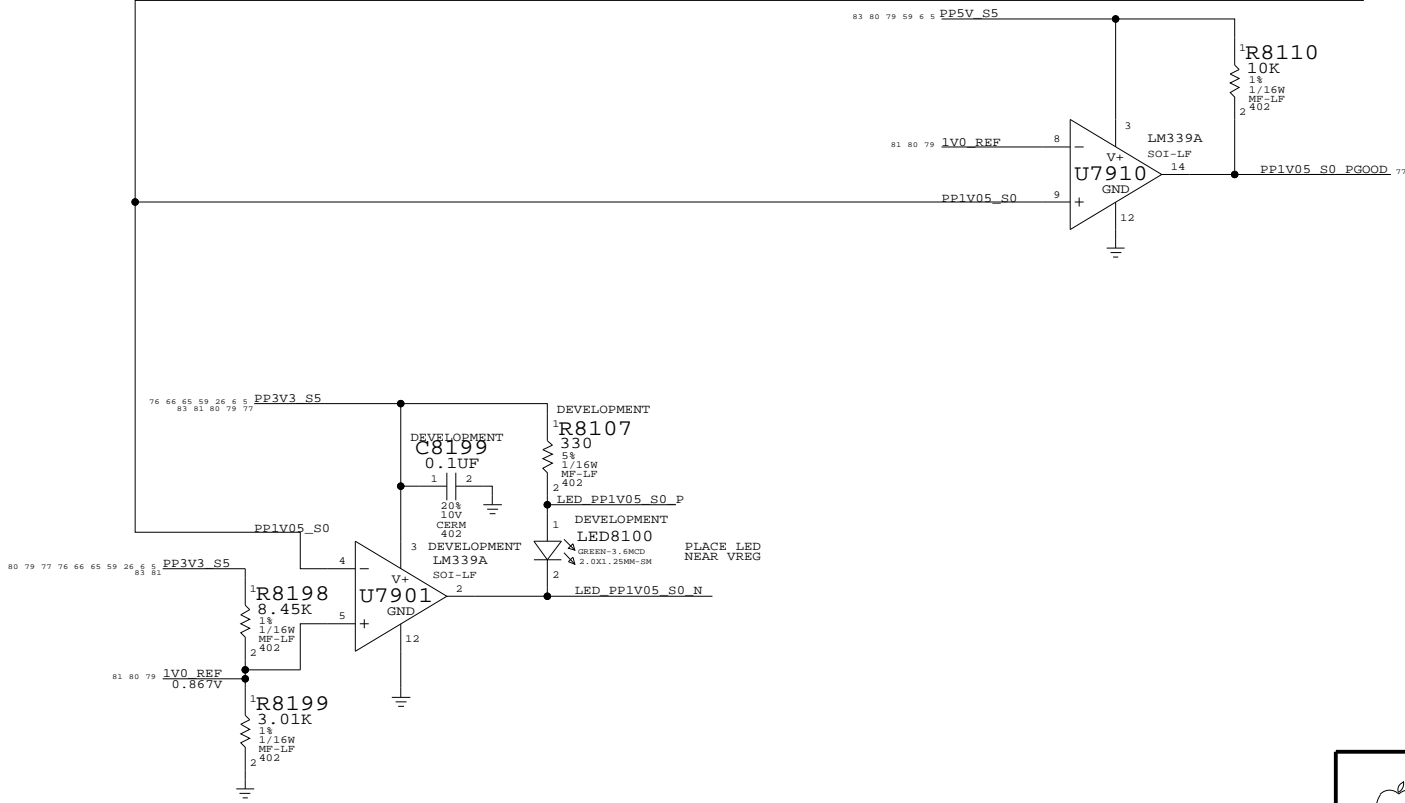
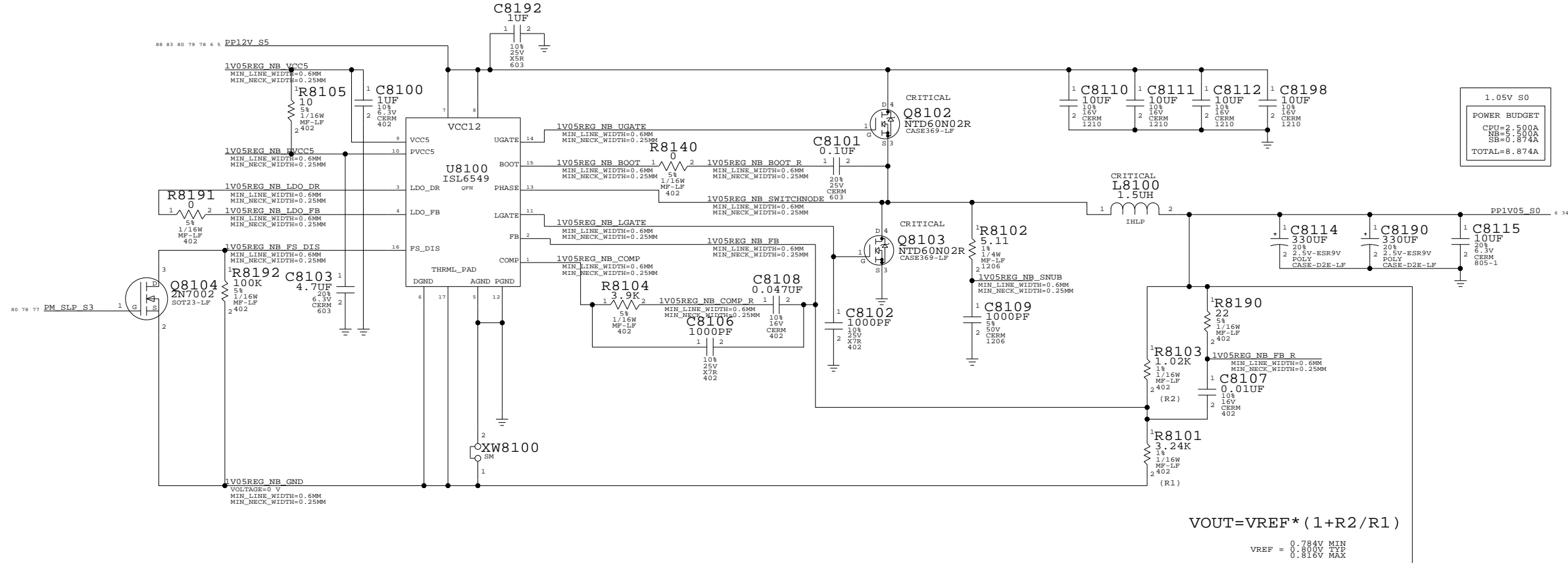
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

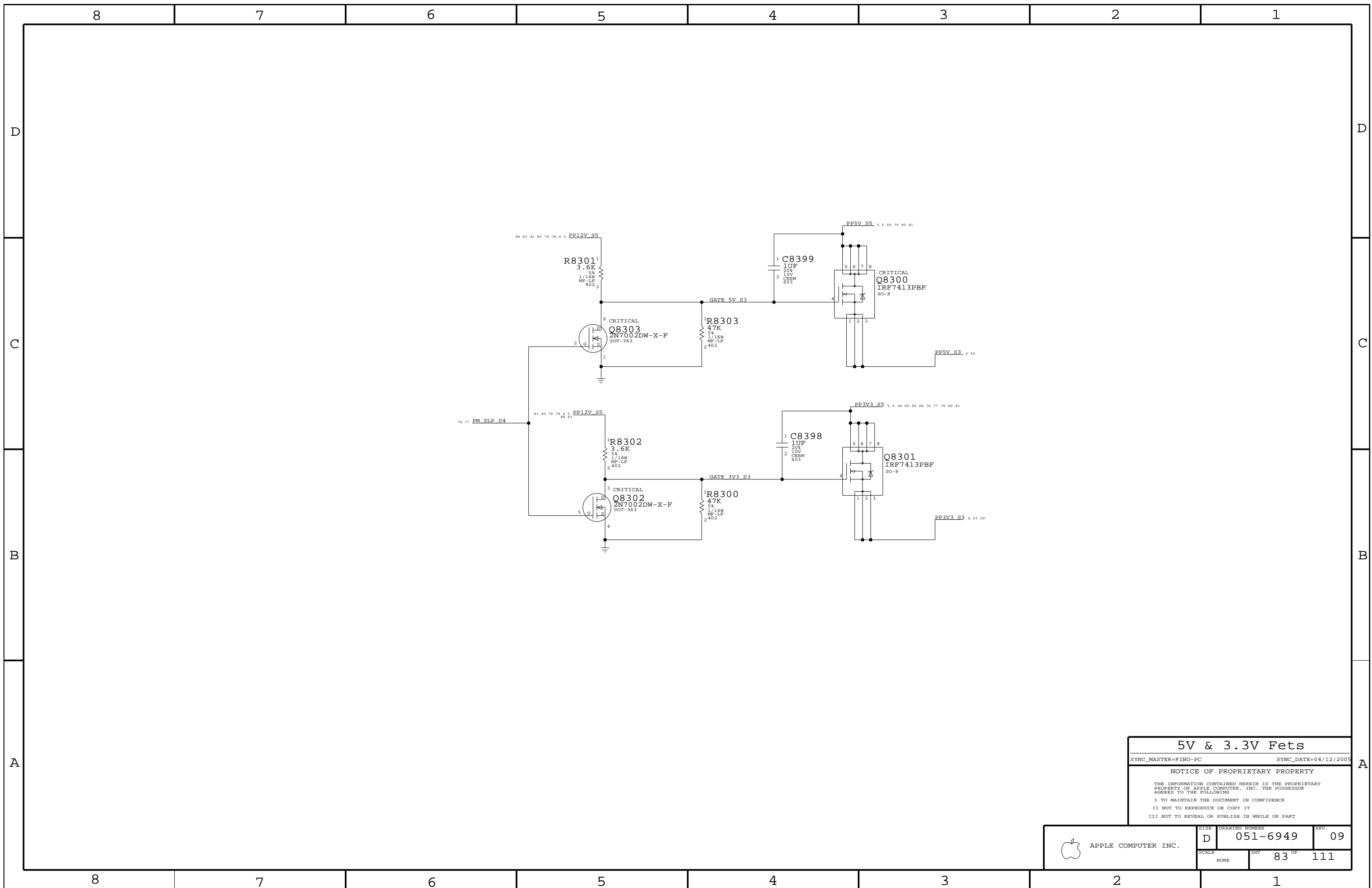
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6950	REV.: 06
	SCALE: NONE	SHEETS: 80 OF 111	

1.05V S0 REGULATOR



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	81 OF	111
NONE			



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

NOTICE OF PROPRIETARY PROPERTY

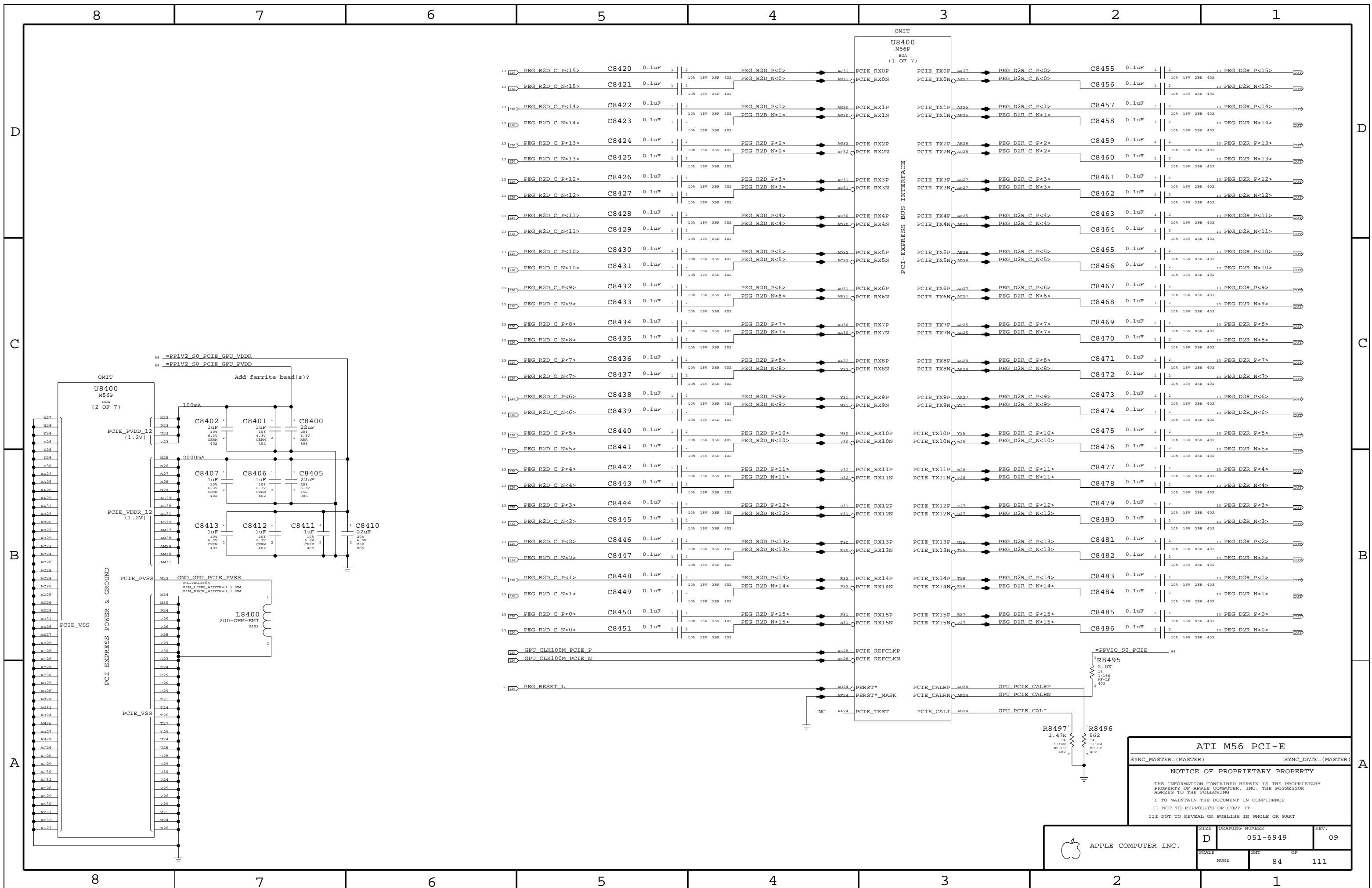
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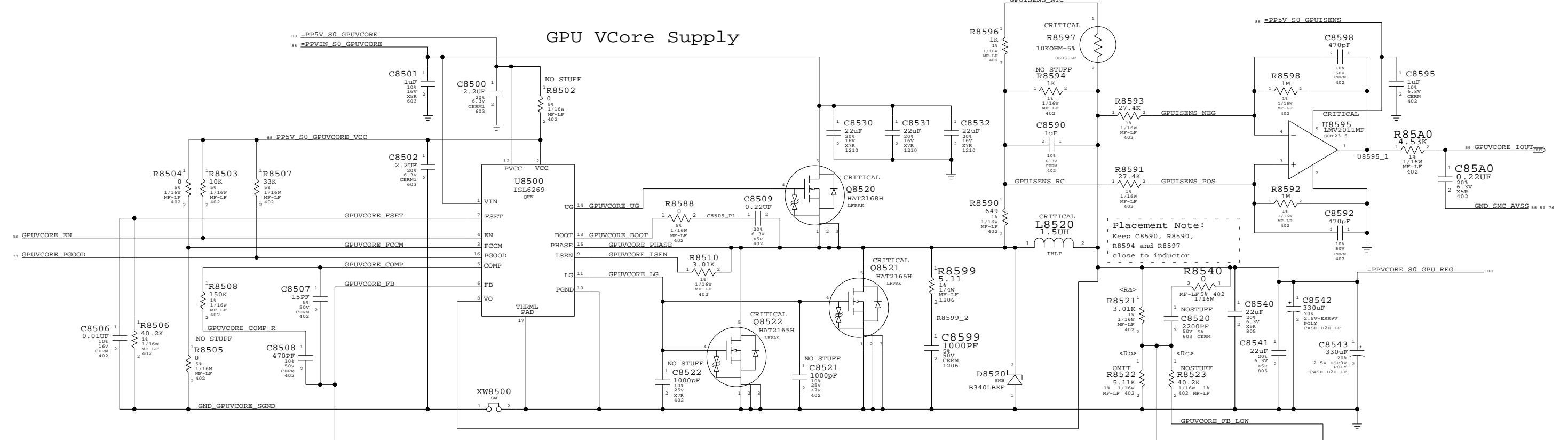
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE		SHT	OF
NONE		83	111

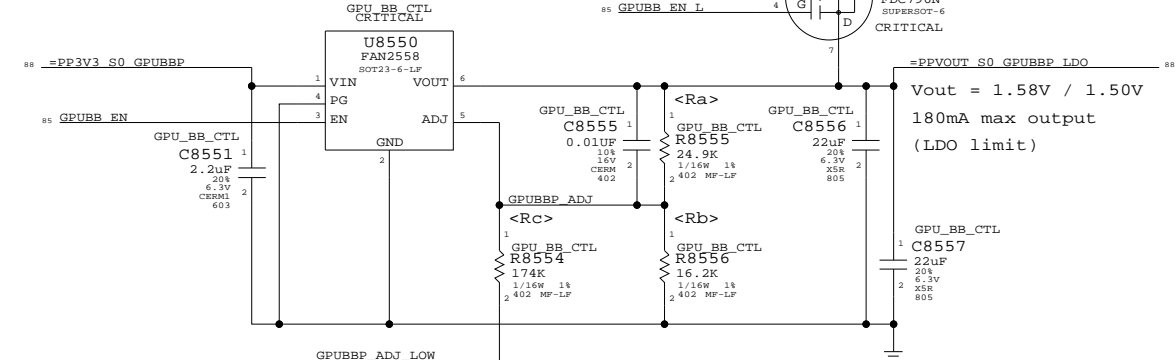


GPU VCore Current Sense



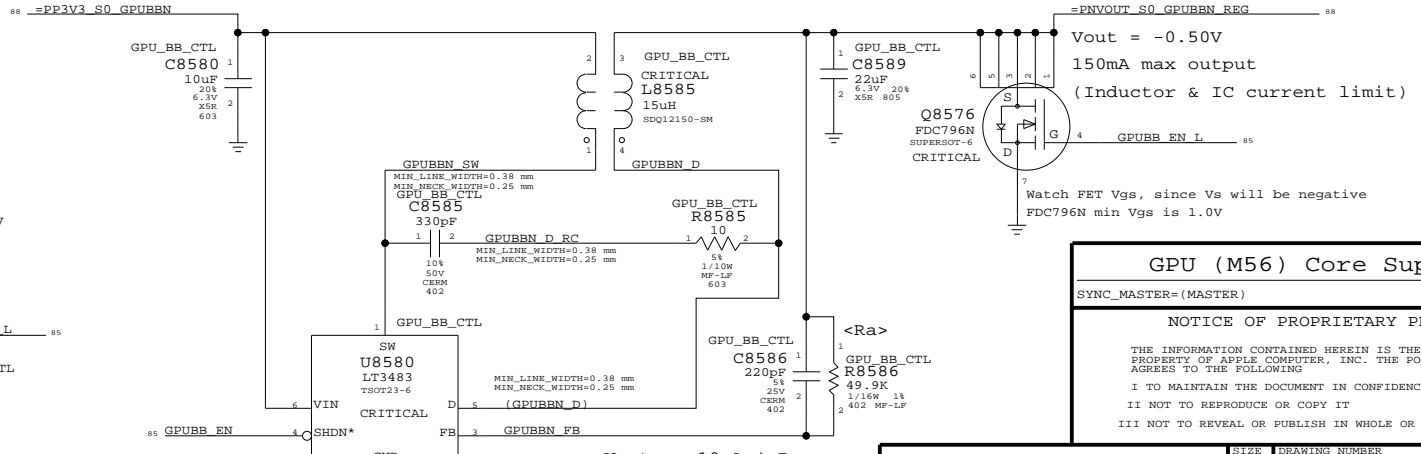
Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active. When inactive, provides VSS to BBN pins.



Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
FDC796N max Vgs is 3.0V
Vin must be > 4.2V

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	
NONE	85	111	

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

8 7 6 5 4 3 2 1

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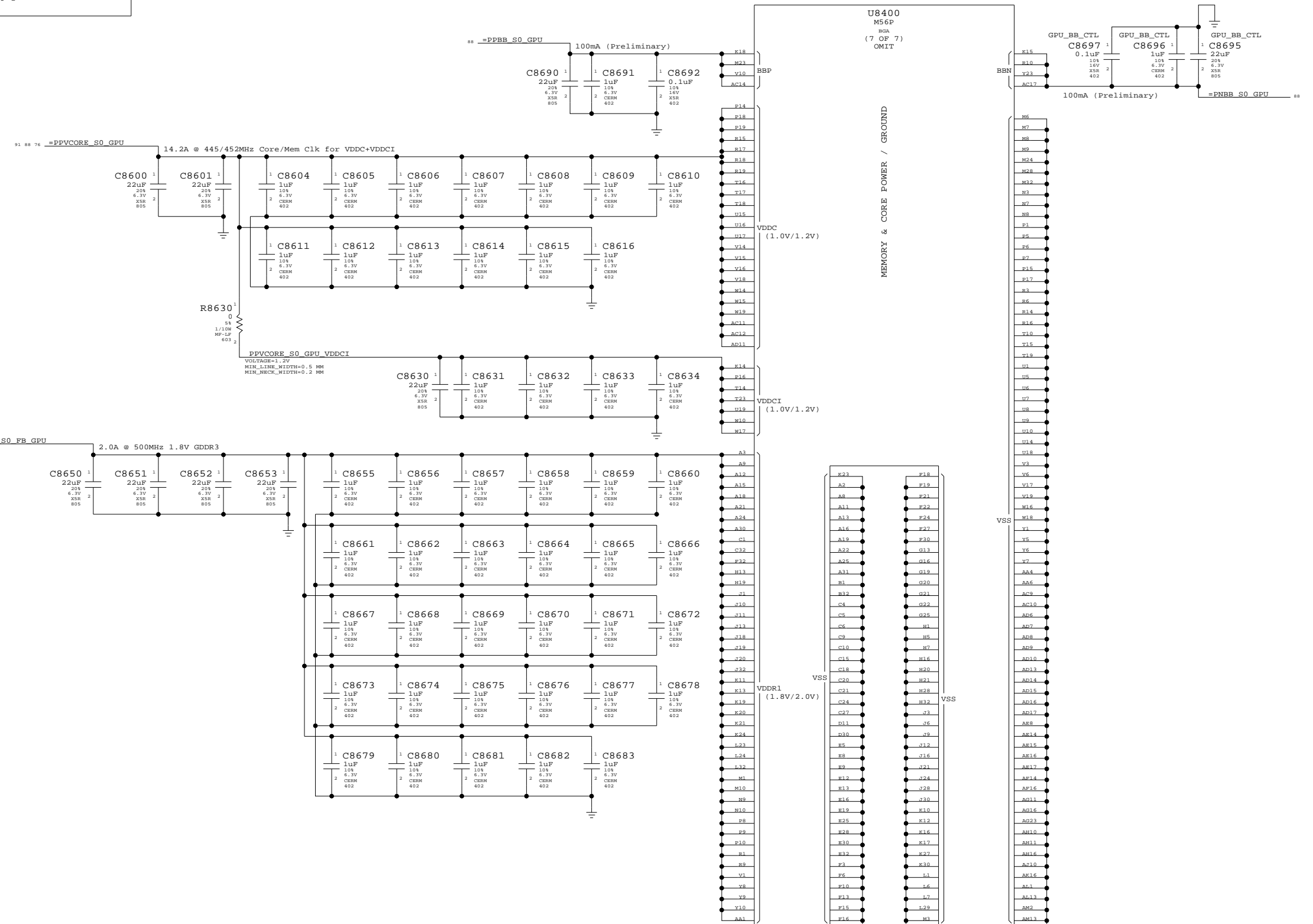
B

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8 7 6 5 4 3 2 1



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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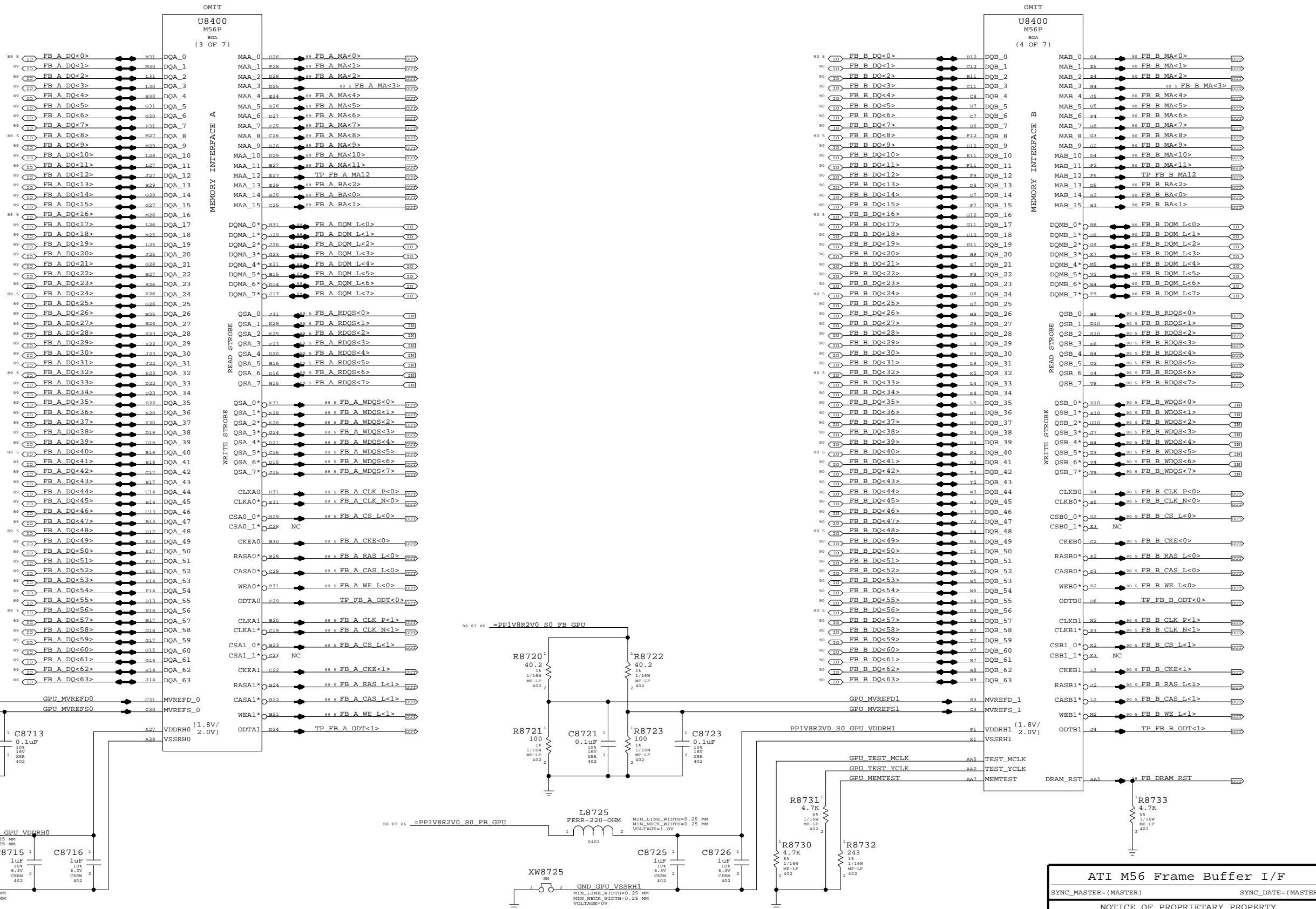
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	NONE	SHT	OF
		86	111

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Table with columns for DRAWING NUMBER (D 051-6949), REV. (09), SCALE (NONE), SHEET (87 OF 111), and APPLE COMPUTER INC. logo.

8

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"S0" GPU RAILS

ONLY ON IN RUN

M56 GPIOs

=PP3V3_S0_GPU_VDDR3 #8 #1

59 EP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

85 PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PPNB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=0V

76 61 59 41 26 10 6 PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

77 6 PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V

83 81 80 79 78 6 5 PP12V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

76 6 PP12V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

97 94 76 6 PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

85 GPUVCORE_EN
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

87 FB_DRAM_RST
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

94 91 GPU_GPIO_0
GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
GPIO 2 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_3
GPIO 3 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_4
GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
GPIO 5 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_6
GPIO 6 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

TP_GPU_GPIO_7
MAKE_BASE=TRUE

91 GPU_GPIO_8
GPIO 8 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

NC_GPU_GPIO_10
MAKE_BASE=TRUE

91 GPU_GPIO_9
GPIO 9 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_13
GPIO 13 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_12
GPIO 12 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_11
GPIO 11 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

GPIO 9,13,12,11 = ROM ID CFG
INTERNAL PULL DOWN
0010 = 256 M APERATURE SIZE

91 GPU_GPIO_24
GPIO 24 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_27
GPIO 27 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_28
GPIO 28 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_29
GPIO 29 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

85 GPU_VCORE_LOW
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

85 GPUVCORE_EN
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

GPU MISC

TP_GPU_GPIO_14
MAKE_BASE=TRUE

TP_GPU_GPIO_17
MAKE_BASE=TRUE

TP_GPU_VGA_R
MAKE_BASE=TRUE

TP_GPU_VGA_G
MAKE_BASE=TRUE

TP_GPU_VGA_B
MAKE_BASE=TRUE

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE

TP_GPU_TV_Y
MAKE_BASE=TRUE

TP_GPU_TV_COMP
MAKE_BASE=TRUE

TP_GPU_TV_C
MAKE_BASE=TRUE

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE

D

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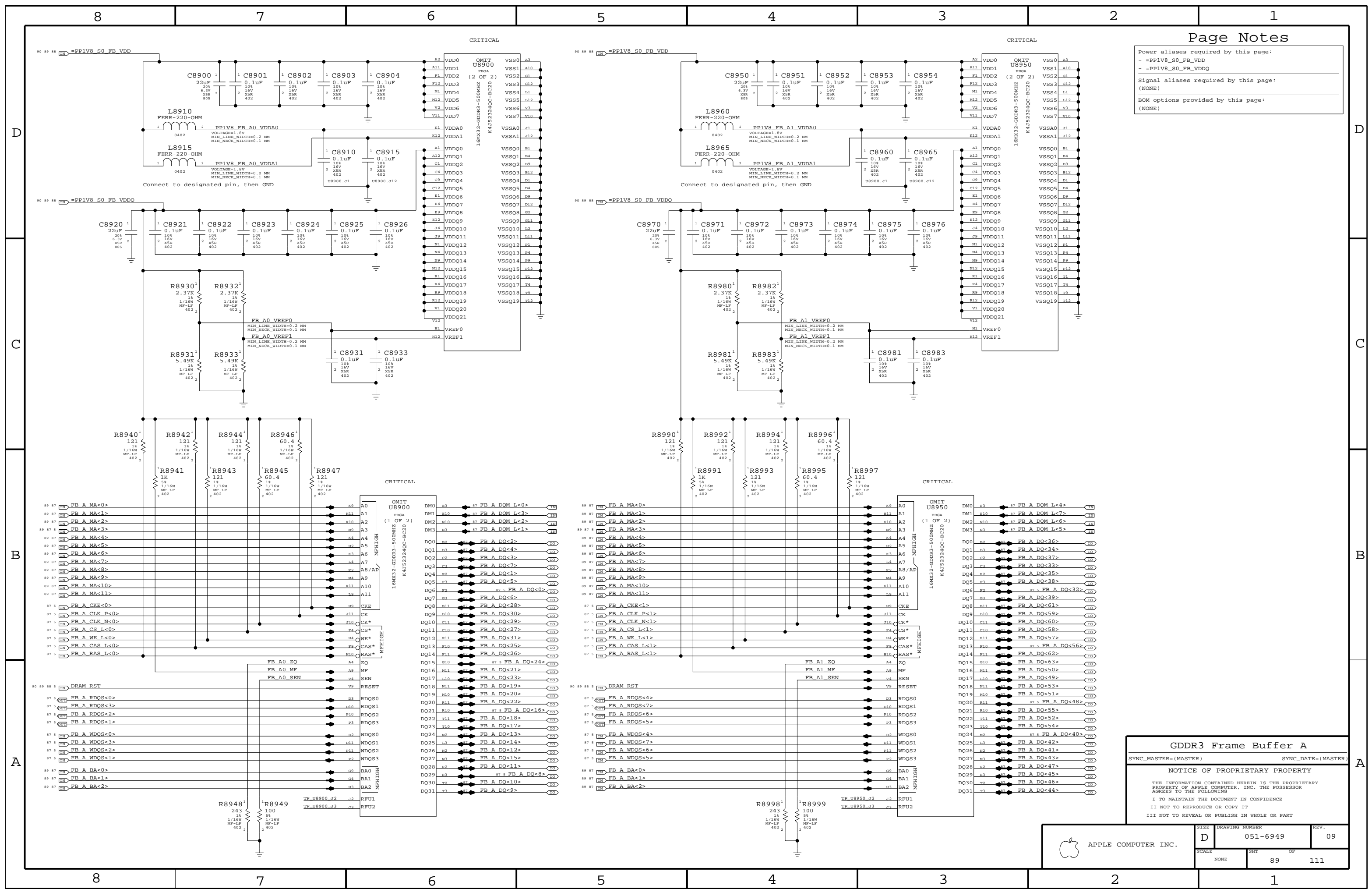
2

1

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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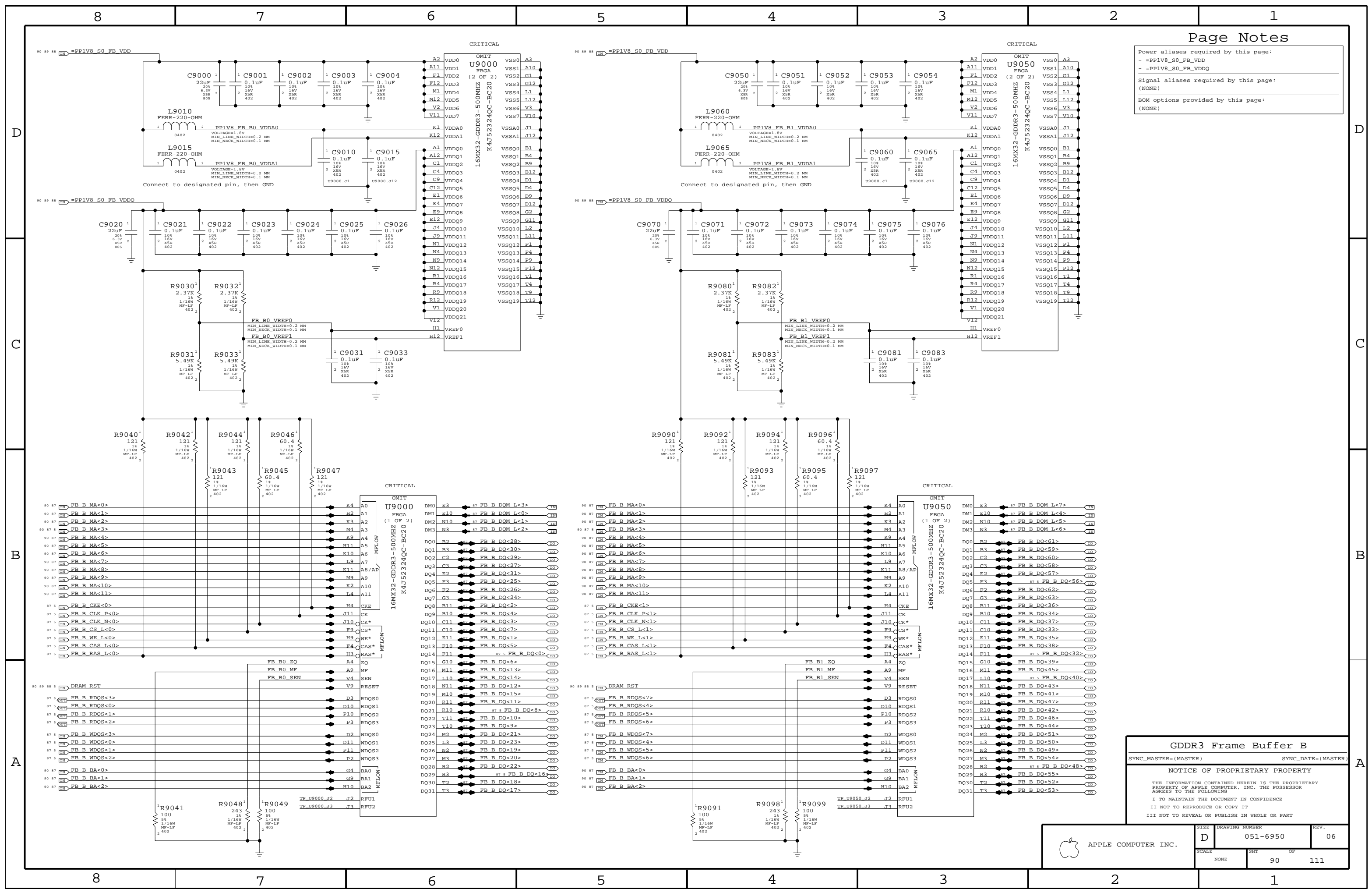
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Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SCALE	SHEET	OF	REV.
	NONE	90	111	06

Page Notes

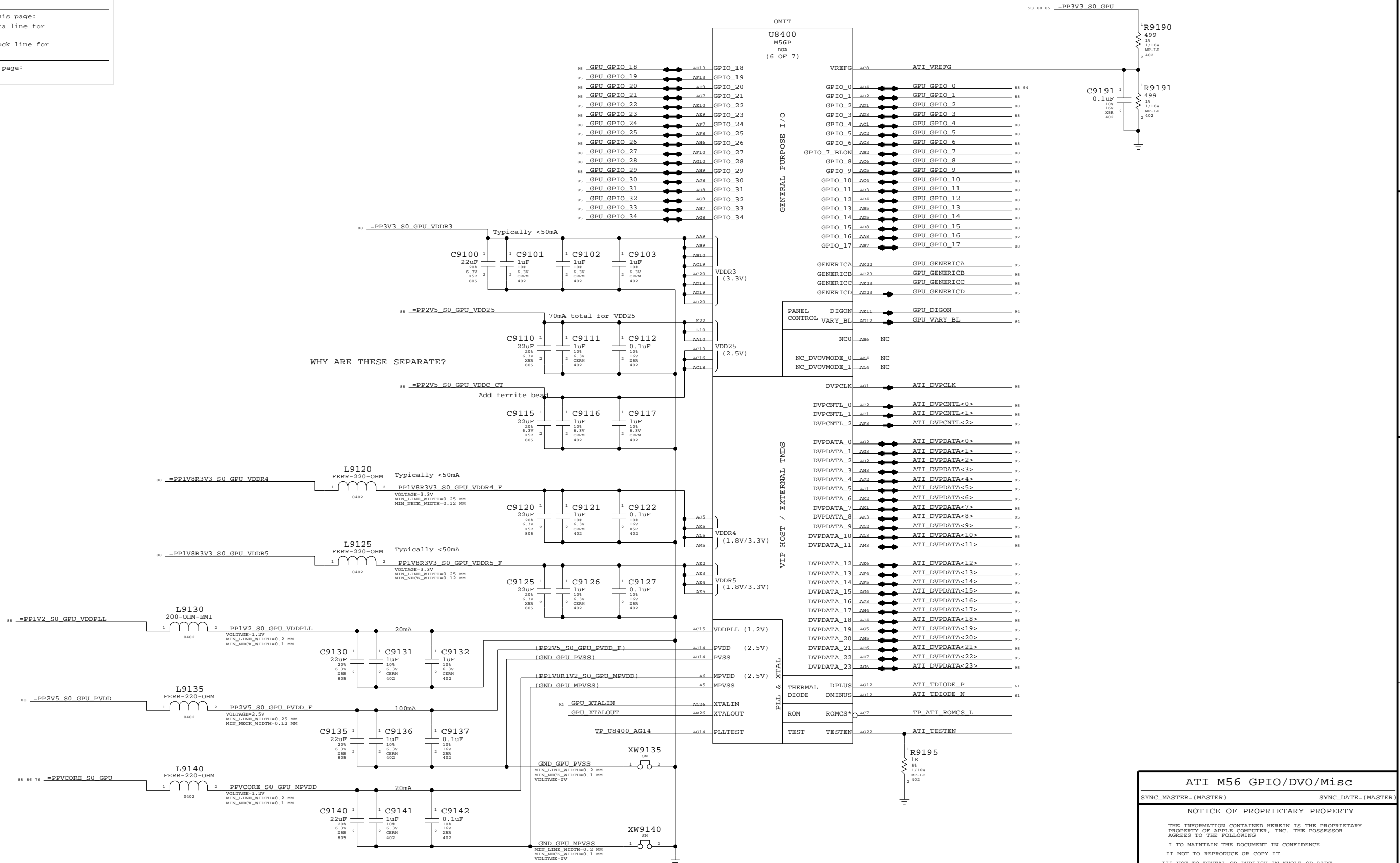
Power aliases required by this page:

- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE	SHT	OF	
NONE	91	111	

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Page Notes

Power aliases required by this page:

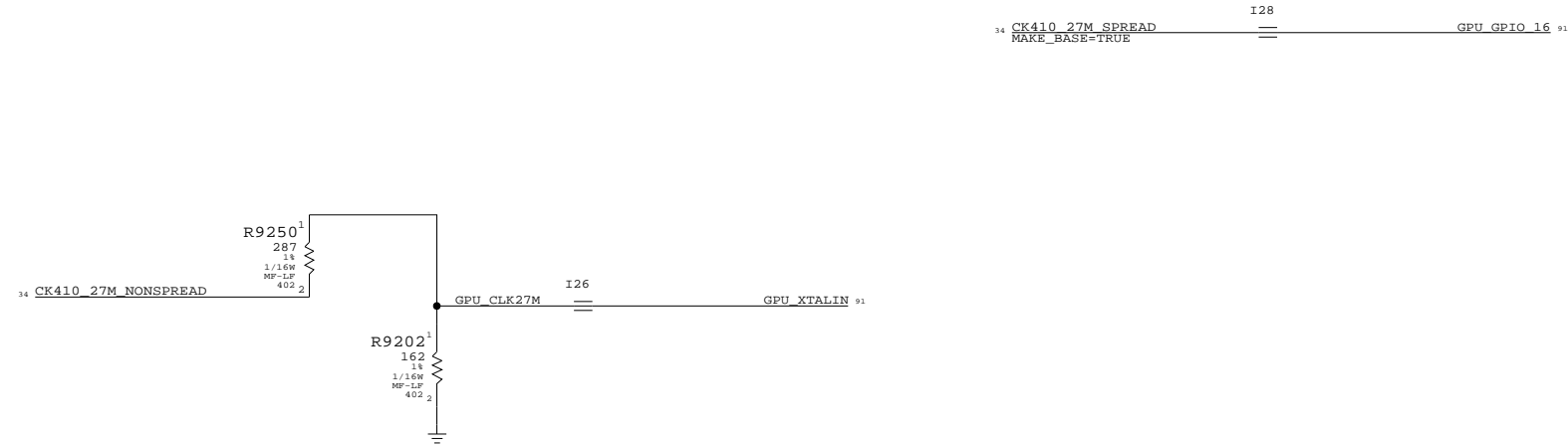
- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8



GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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	SCALE	SHT	OF	REV.
	NONE	92	111	09

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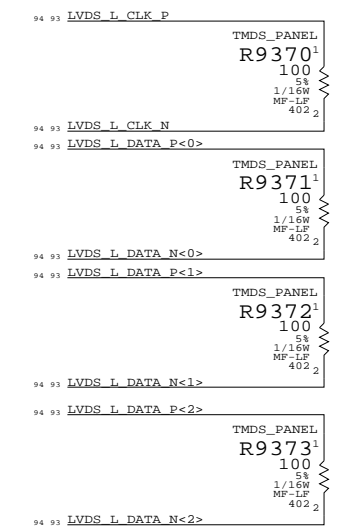
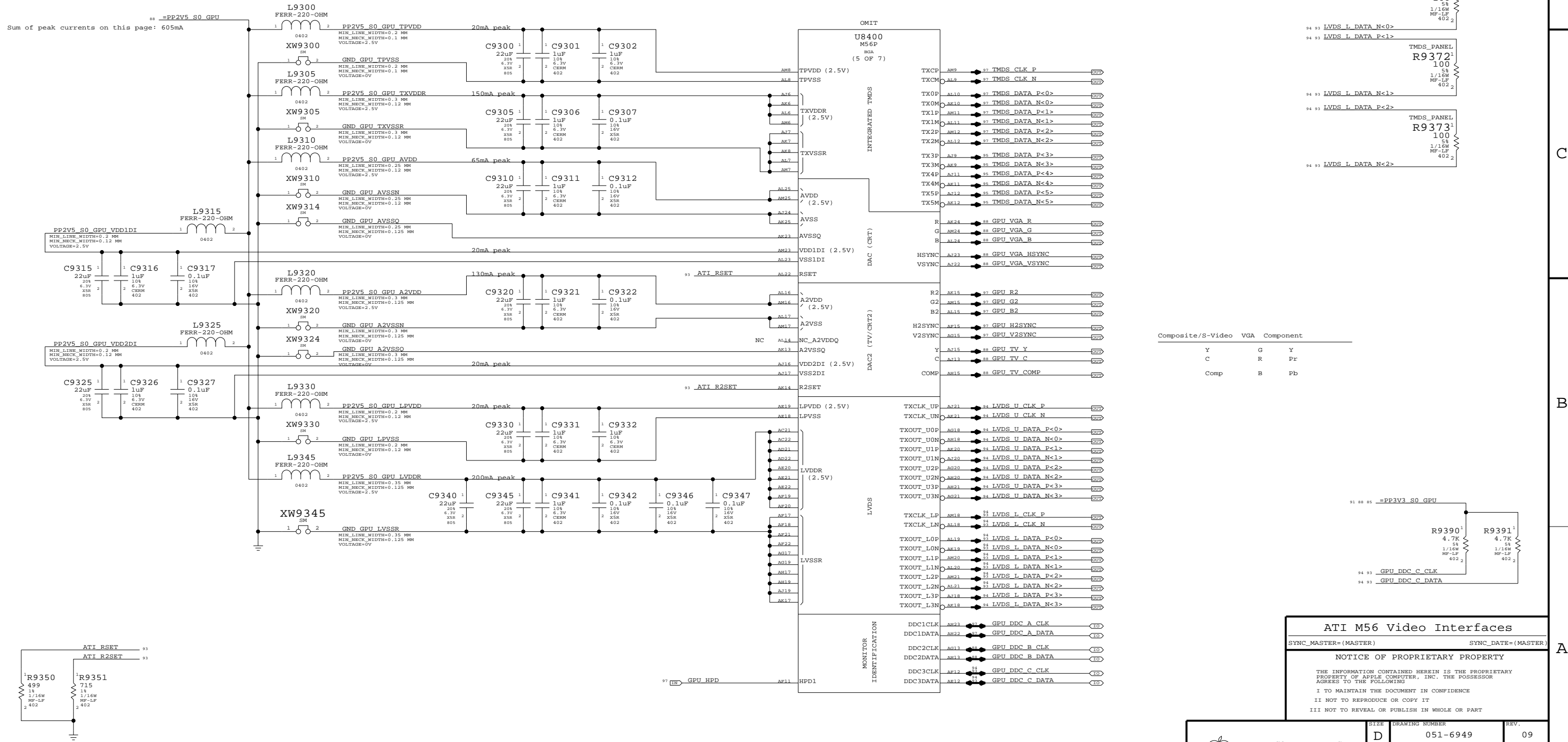
Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

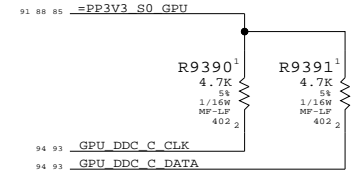
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATA=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

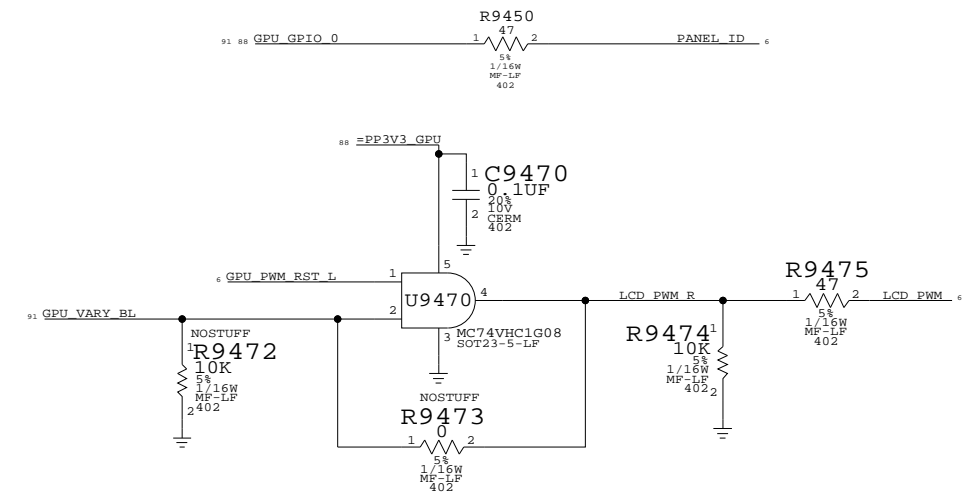
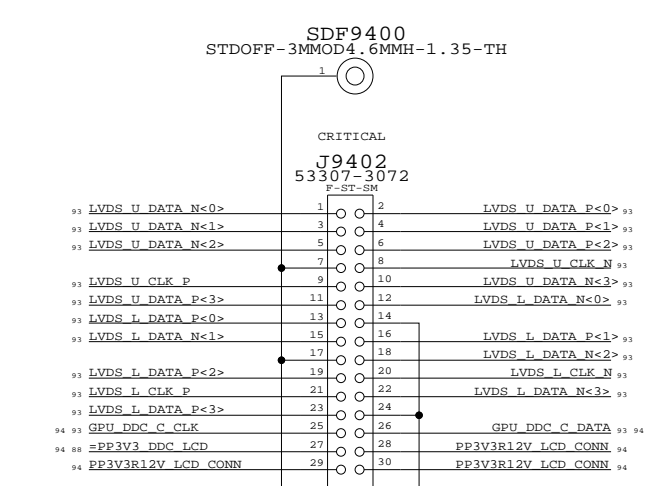
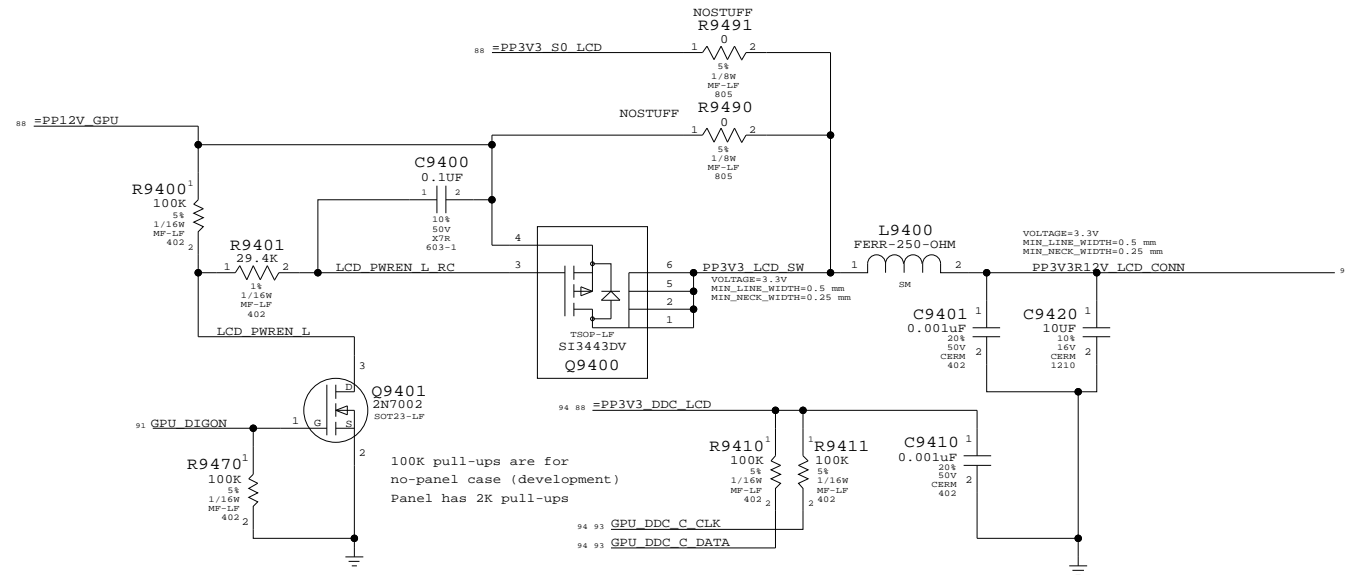
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	93	111	09

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0302	338S0266		U8400	IC,ATI,M560,GRAFIX CTLR,88P8GA,LF

INVERTER INTERFACE

LCD (LVDS) INTERFACE



Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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	D	051-6950	06
SCALE	SHT	OF	
NONE	94	111	

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D

D

TP TMSD DATA P<3> == TMSD DATA P<3> 93
 MAKE_BASE=TRUE

TP TMSD DATA N<3> == TMSD DATA N<3> 93
 MAKE_BASE=TRUE

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 MAKE_BASE=TRUE

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7

6

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3

2

1

M56 TPS

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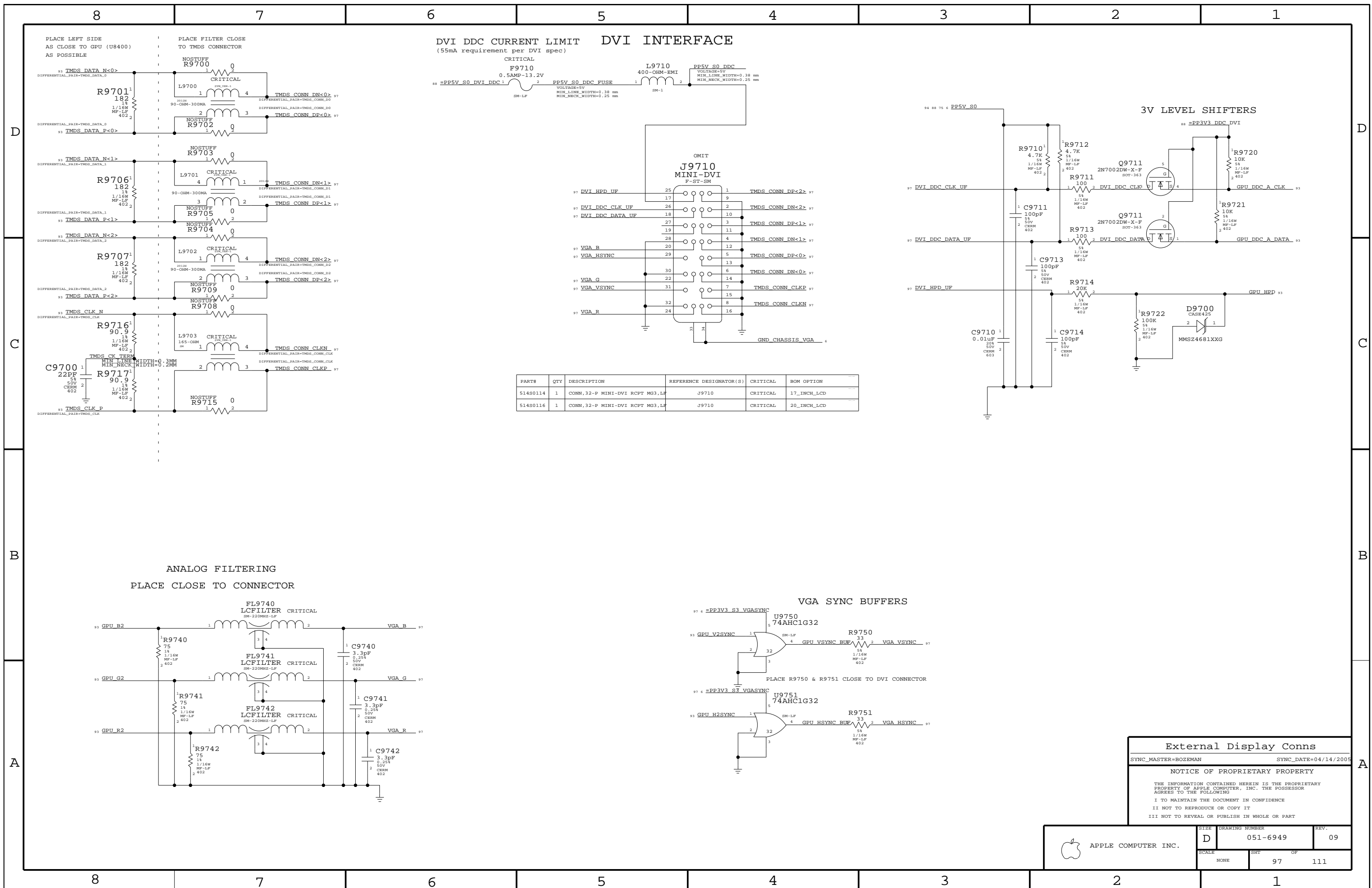
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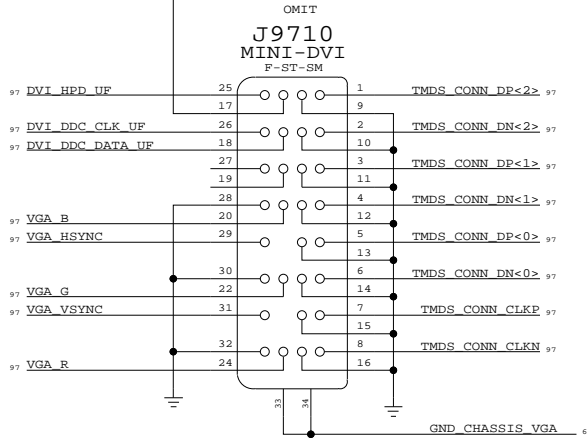
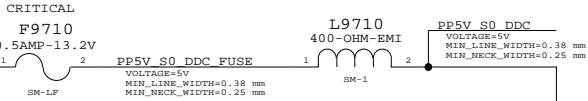
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT 95 OF 111	
NONE		



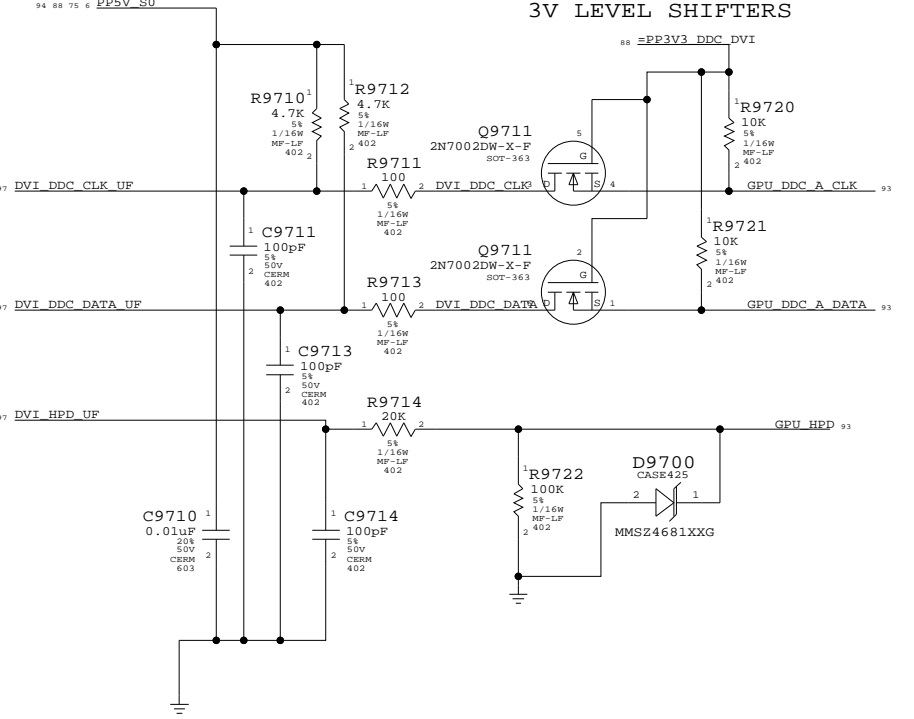
DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

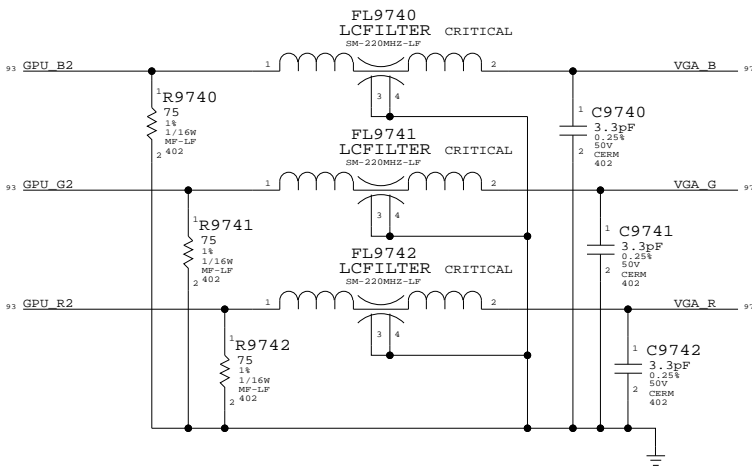


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51480114	1	CONN, 32-P MINI-DVI RCPT MG3, LF	J9710	CRITICAL	17_INCH_LCD
51480116	1	CONN, 32-P MINI-DVI RCPT MG3, LF	J9710	CRITICAL	20_INCH_LCD

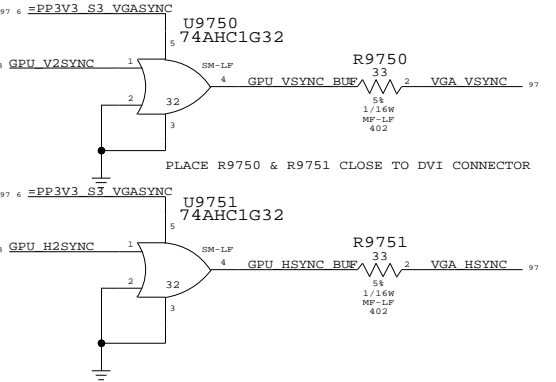
3V LEVEL SHIFTERS



ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS



External Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005
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Table with 8 columns (labeled 1-8) and 1000 rows. The table contains various part numbers, descriptions, and quantities. The columns are numbered 1 through 8 from right to left. The rows are numbered 1 through 1000. The table is divided into sections A, B, C, and D. Section A is at the bottom, B on the right, C on the left, and D at the top. The table contains various part numbers, descriptions, and quantities.

	8			7			6			5			4			3			2			1		
D	R7217	RES_402	m39[72B5]	R7903	RES_402	m39[79C3]	R8948	RES_402	m39[89A7]	U601	SM74VLC1G04_SOT23-5	m39[6C7]	D											
	R7218	RES_402	m39[72A5]	R7904	RES_402	m39[79C5]	R8949	RES_402	m39[89A7]	U1000	AD77461_MSOP	m39[10D5]												
	R7219	RES_402	m39[72B4]	R7905	RES_402	m39[79D7]	R8980	RES_402	m39[89C4]	U1200	NB_945GM_BGA	m39[12D5]												
	R7302	RES_402	m39[73A3]	R7906	RES_402	m39[79A4]	R8981	RES_402	m39[89C4]	U1200	NB_945GM_BGA	m39[13D4]												
	R7313	RES_402	m39[73C2]	R7910	RES_402	m39[79B2]	R8982	RES_402	m39[89C4]	U1200	NB_945GM_BGA	m39[14D5]												
C	R7314	RES_402	m39[73C2]	R7911	RES_402	m39[79B3]	R8983	RES_402	m39[89C4]	U1200	NB_945GM_BGA	m39[15D3 15D7]	C											
	R7400	RES_402	m39[74B4]	R7912	RES_402	m39[79B3]	R8990	RES_402	m39[89B5]	U1200	NB_945GM_BGA	m39[16D2 16C8]												
	R7404	RES_402	m39[74C4]	R7913	RES_402	m39[79A2]	R8991	RES_402	m39[89B4]	U1200	NB_945GM_BGA	m39[17D5]												
	R7405	RES_402	m39[74D3]	R7914	RES_402	m39[79A3]	R8992	RES_402	m39[89B4]	U1200	NB_945GM_BGA	m39[18D7 18D4]												
	R7407	RES_402	m39[74B4]	R7915	RES_402	m39[79A3]	R8993	RES_402	m39[89B4]	U2100	SB_1CH7M_BGA	m39[21D6]												
	R7408	RES_402	m39[74A4]	R7940	RES_402	m39[79D5]	R8994	RES_402	m39[89B4]	U2100	SB_1CH7M_BGA	m39[22D3 22B7]												
	R7409	RES_402	m39[74B4]	R7991	RES_402	m39[79C7]	R8995	RES_402	m39[89B4]	U2100	SB_1CH7M_BGA	m39[23D4]												
	R7410	RES_805	m39[74D2]	R7992	RES_402	m39[79C7]	R8996	RES_402	m39[89B4]	U2100	SB_1CH7M_BGA	m39[24D7 24D4]												
	R7411	RES_805	m39[74C2]	R7999	RES_402	m39[79C3]	R8997	RES_402	m39[89B4]	U2601	MC74VHC1G08_SOT23-5	m39[26D5]												
	R7412	RES_805	m39[74D2]	R8000	RES_402	m39[80C3]	R8998	RES_402	m39[89A4]															
B	R7413	RES_402	m39[74B4]	R8001	RES_402	m39[80C7]	R8999	RES_402	m39[89A4]	U2603	SM74VLC1G04_SOT23-5	m39[26A7]	B											
	R7414	RES_805	m39[74B7]	R8002	RES_1206	m39[80C4]	R9030	RES_402	m39[90C7]	U2698	MC74VHC1G08_SOT23-5	m39[26C4]												
	R7415	RES_805	m39[74B8]	R8003	RES_402	m39[80C3]	R9031	RES_402	m39[90C7]															
	R7416	RES_805	m39[74C7]	R8004	RES_402	m39[80C5]	R9032	RES_402	m39[90C7]	U2699	MAX6816_SOT143	m39[26C5]												
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	R7418	RES_402	m39[74B6]	R8007	RES_402	m39[80A4]	R9040	RES_402	m39[90B8]	8														
	R7419	RES_402	m39[74B6]	R8010	RES_402	m39[80B2]	R9041	RES_402	m39[90A8]	U3301	CLK_GEN_CY284455_QFN	m39[33C5]												
	R7420	RES_402	m39[74D4]	R8011	RES_402	m39[80B3]	R9042	RES_402	m39[90B7]	U4101	88E8053_QFN	m39[41D5]												
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	R7422	RES_402	m39[74D7]	R8040	RES_402	m39[80C5]	R9044	RES_402	m39[90B7]	U4400	FW32306_TQFP	m39[44D5]												
	R7423	RES_402	m39[74B6]	R8092	RES_402	m39[80C7]	R9045	RES_402	m39[90B7]	U4700	SWI_TPS2024_SOI	m39[47C8]												
	R7424	RES_402	m39[74B6]	R8099	RES_402	m39[80C3]	R9046	RES_402	m39[90B7]	U5800	SMC_H8S2116_BGA	m39[58D6 58C6 58C3 58A8]												
	R7425	RES_402	m39[74A5]	R8101	RES_402	m39[81C3]	R9047	RES_402	m39[90B7]	U5900	VFET_RM5VD_SOT23-5	m39[59D8]												
	R7426	RES_402	m39[74A4]	R8102	RES_1206	m39[81C4]	R9048	RES_402	m39[90A7]	U5940	VREF_REF3133_SOT23-3	m39[59A4]												
	R7427	RES_402	m39[74A4]	R8103	RES_402	m39[81C3]	R9049	RES_402	m39[90A7]	U5999	COMPARATOR_LMV339_TS	m39[59A6 59A8 59A8 59A6]												
	R7429	RES_805	m39[74C2]	R8104	RES_402	m39[81C5]	R9080	RES_402	m39[90C4]	SOP														
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	R7502	RES_1206	m39[75B2]	R8191	RES_402	m39[81C7]	R9092	RES_402	m39[90B4]	U7200	MAX3171_4_QFN-LF	m39[72C5]												
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	R7504	RES_402	m39[75C1]	R8198	RES_402	m39[81A5]	R9094	RES_402	m39[90B4]	U7501	INA138_SOT23-5-LF	m39[76D7]												
	R7505	RES_402	m39[75B2]	R8199	RES_402	m39[81A5]	R9095	RES_402	m39[90B4]	U7600	OPAMP_LMV2011_SOT23-	m39[76D3]												
	R7506	RES_603	m39[75B2]	R8300	RES_402	m39[83B4]	R9096	RES_402	m39[90B4]	5														
	R7507	RES_402	m39[75B1]	R8301	RES_402	m39[83C5]	R9097	RES_402	m39[90B4]	U7700	LTC3411_MSOP-LF	m39[77D5]												
	R7508	RES_402	m39[75B8]	R8302	RES_402	m39[83B5]	R9098	RES_402	m39[90A4]	U7710	MC74VHC1G08_SOT23-5-	m39[77C7]												
	R7509	RES_402	m39[75B8]	R8303	RES_402	m39[83C4]	R9099	RES_402	m39[90A4]	LF														
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	R7511	RES_402	m39[75B7]	R8496	RES_402	m39[84A2]	R9191	RES_402	m39[91D2]	LF														
	R7512	RES_402	m39[75B7]	R8497	RES_402	m39[84A2]	R9195	RES_402	m39[91A1]	U7712	MC74VHC1G08_SOT23-5-	m39[77B7]												
	R7513	RES_402	m39[75B7]	R8502	RES_402	m39[85D6]	R9202	RES_402	m39[92C6]	LF														
	R7514	RES_402	m39[75B8]	R8503	RES_402	m39[85D7]	R9250	RES_402	m39[92C6]	U7750	LTC3412_TSSOP-LF	m39[77B5]												
	R7515	RES_402	m39[75B4]	R8504	RES_402	m39[85D7]	R9350	RES_402	m39[93A8]	U7800	ISL6549_QFN	m39[78C6]												
R7516	RES_402	m39[75B4]	R8505	RES_402	m39[85C7]	R9351	RES_402	m39[93A8]	U7900	ISL6549_QFN	m39[79D6]													
R7517	RES_402	m39[75B5]	R8506	RES_402	m39[85C8]	R9370	RES_402	m39[93D1]	U7901	COMPARATOR_LM339A_SO	m39[79A5]													
R7518	RES_402	m39[75B5]	R8507	RES_402	m39[85D7]	R9371	RES_402	m39[93D1]	I-LF															
R7519	RES_402	m39[75C7]	R8508	RES_402	m39[85C7]	R9372	RES_402	m39[93C1]	U7901	COMPARATOR_LM339A_SO	m39[80A4]													
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R7522	RES_402	m39[75A5]	R8522	RES_402	m39[85C3]	R9391	RES_402	m39[93A1]	I-LF															
R7523	RES_402	m39[75A5]	R8523	RES_402	m39[85C3]	R9400	RES_402	m39[94C8]	U7910	COMPARATOR_LM339A_SO	m39[79B3 79A3]													
R7526	THERMISTER_402	m39[75C8]	R8524	RES_402	m39[85B3]	R9401	RES_402	m39[94C7]	I-LF															
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R7531	THERMISTER_0603-LF	m39[75B4]	R8555	RES_402	m39[85B6]	R9472	RES_402	m39[94B3]	U8000	ISL6549_QFN	m39[80D6]													
R7590	RES_402	m39[75C7]	R8556	RES_402	m39[85B6]	R9473	RES_402	m39[94B2]	U8100	ISL6549_QFN	m39[81D6]													
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R7592	RES_402	m39[75C7]	R8561	RES_402	m39[85A7]	R9475	RES_402	m39[94B1]	U8400	ATI_M56P_BGA	m39[85D7]													
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R7594	RES_402	m39[75C7]	R8585	RES_603	m39[85A3]	R9491	RES_805	m39[94D6]	U8400	ATI_M56P_BGA	m39[91D4]													
R7595	RES_402	m39[75C7]	R8586	RES_402	m39[85A3]	R9700	RES_402	m39[97D7]	U8400	ATI_M56P_BGA	m39[93C4]													
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R7597	RES_402	m39[76D6]	R8590	RES_402	m39[85C3]	R9702	RES_402	m39[97D7]	U8550	FAN2558_SOT23-6-LF	m39[85B7]													
R7598	RES_402	m39[76C7]	R8591	RES_402	m39[85D3]	R9703	RES_402	m39[97D7]	U8560	74LVC1G125LF_SOT23-5	m39[85A6]													
R7599	RES_2512-1	m39[76D7]	R8592	RES_402	m39[85D2]	R9704	RES_402	m39[97C7]	U8580	LT3483_TSOT23-6	m39[85A4]													
R7600	RES_402	m39[76D3]	R8593	RES_402	m39[85D3]	R9705	RES_402	m39[97C7]	U8595	OPAMP_LMV2011_SOT23-	m39[85D2]													
R7602	RES_402	m39[76D3]	R8594	RES_402	m39[85D3]	R9706	RES_402	m39[97D8]	5															
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R7604	RES_402	m39[76C3]	R8597	THERMISTER_0603-LF	m39[85D3]	R9708	RES_402	m39[97C7]	36H_FBGA															
R7605	RES_402	m39[76D4]	R8598	RES_402	m39[85D2]	R9709	RES_402	m39[97C7]	U8950	SGRAM_16MX32_GDDR3_1	m39[89B3 89D3]													
R7606	RES_402	m39[76D4]	R8599	RES_1206	m39[85C4]	R9710	RES_402	m39[97D2]	36H_FBGA															
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R7630	RES_402	m39[76C8]	R8713	RES_402	m39[87A7]	R9715	RES_402	m39[97C7]	U9470	MC74VHC1G08_SOT23-5-	m39[94B2]													
R7631	RES_402	m39[76C8]	R8731	RES_402	m39[87A8]	R9716	RES_402	m39[97C8]	LF															
R7632	RES_402	m39[76C7]	R8721	RES_402	m39[87A4]	R9717	RES_402	m39[97C8]	U9750	74AHC1G32_SM-LF	m39[97A4]													
R7639	RES_402	m39[76B7]	R8722	RES_402	m39[87B4]	R9720	RES_402	m39[97D1]	U9751	74AHC1G32_SM-LF	m39[97A4]													
R7640	RES_402	m39[76A7]	R8723	RES_402	m39[87A4]	R9721	RES_402	m39[97D1]	VR6800	LREG_TPS79501_SOT2														

