1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

FINO M33
5/19/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
07		381758	ENGINEERING RELEASED	05/19/05	?

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10	12	1.5V Vreg		FINO-PC	05/19/2005
11	13	1.2V Vreg		FINO-PC	05/19/2005
12	15	2.5V Vreg		FINO-PC	05/19/2005
13	16	5V & 3.3V Fets		FINO-PC	05/19/2005
14	17	Vesta Core / Misc		FINO-HC	05/19/2005
15	19	KODIAK CORE & BYPASS		Q63	05/19/2005
16	20	KODIAK & SHASTA MISC		FINO-ME	05/19/2005
17	23	Shasta Core Power		Q63	05/19/2005
18	24	Shasta Serial / Misc		FINO-ME	05/19/2005
19	25	PULSAR2 POWER		Q63	05/19/2005
20	26	PULSAR2 CLOCKS		FINO-ME	05/19/2005
21	27	Pulsar Aliases		FINO-ME	05/19/2005
22	28	System Management Unit		Q63	05/19/2005
23	29	SMU SUPPLEMENTAL (2)		FINO-MS	05/19/2005
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26	32	Fan 0, 1 & System Temp		FINO-PC	05/19/2005
27	33	Fan 2 & HD Temp		FINO-PC	05/19/2005
28	39	I2C Connections		FINO-ME	05/19/2005
29	41	KODIAK EI PWR & CAPS		Q63	05/19/2005
30	42	KODIAK EI A		Q63	05/19/2005
31	43	CPU EI AND IO		FINO-MS	05/19/2005
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33	47	CPU STRAPS		FINO-MS	05/19/2005
34	48	CPU POWER AND BYPASS		FINO-MS	05/19/2005
35	49	PROC DECOUPLING		FINO-MS	05/19/2005
36	50	CPU VCORE VREG		M33-MS	05/19/2005
37	52	CPU VCORE MORE BYPASS		FINO-MS	05/19/2005
38	54	CPU AVDD VREG		FINO-MS	05/19/2005
39	55	T,V,I SENSORS		FINO-MS	05/19/2005
40	56	CPU ALIASES & MISC		FINO-MS	05/19/2005
41	58	KODIAC NBMEM PWR & CAPS		Q63	05/19/2005
42	59	Kodiak Memory Dq/Ctl		FINO-RT	05/19/2005
43	61	Parallel Term		FINO-RT	05/19/2005
44	62	Main Memory Clock Buffer		FINO-RT	05/19/2005
45	63	MEMORY ADDR BRANCHING		FINO-EG	05/19/2005
46	67	Memory Dimm A		FINO-RT	05/19/2005
47	68	MLB Mem Series Term		FINO-RT	05/19/2005
48	69	On-Board DDR SDRAM		FINO-RT	05/19/2005
49	70	On-Board DDR SDRAM		FINO-RT	05/19/2005
50	82	KODIAK PCI-E X16		Q63	05/19/2005
51	84	GPU PCIe		FINO-DD	05/19/2005
52	85	Graphics Vregs		M33-DD	MASTER
53	86	GPU Core Power		FINO-DD	05/19/2005
54	87	GPU Frame Buffer		FINO-DD	05/19/2005
55	88	FB Series Termination		FINO-DD	05/19/2005
56	89	GPU GDDR SDRAM A		FINO-DD	05/19/2005
57	90	GPU GDDR SDRAM B		FINO-DD	05/19/2005
58	91	FB Parallel Termination		M33-DD	MASTER
59	92	GPU Straps		FINO-DD	05/19/2005
60	93	GPU DVI & DACs		FINO-DD	05/19/2005
61	96	TMDS / ExtVGA		M33-DD	MASTER
62	97	KODIAK PCI-E CONST		FINO-DD	05/19/2005
63	98	KODIAK HT16		Q63	05/19/2005
64	101	HT ALIASES		FINO-EG	05/19/2005
65	103	Shasta HyperTransport		Q63	05/19/2005
66	119	Shasta PCI Interface		Q63	05/19/2005
67	120	PCI SERIES TERMINATION		FINO-EG	05/19/2005
68	121	AIRPORT & BLUETOOTH		FINO-EG	05/19/2005
69	122	USB 2.0 PCI Interface		Q63	05/19/2005
70	125	BootROM		Q63	05/19/2005
71	127	Shasta Disk		M33-MB	05/19/2005
72	129	Disk Connectors		M33-MB	05/19/2005
73	130	ENET SERIES TERM		FINO-HC	05/19/2005
74	131	Shasta Ethernet		Q63	05/19/2005
75	132	Vesta Ethernet PHY		Q63	05/19/2005
76	136	ETHERNET CONNECTOR		FINO-HC	05/19/2005
77	138	Shasta FireWire		Q63	05/19/2005
78	139	Vesta FireWire PHY		Q63	05/19/2005
79	140	FIREWIRE CONNECTORS		FINO-HC	05/19/2005
80	142	USB Host Interfaces		Q63	05/19/2005
81	143	USB Device Interfaces		FINO-MB	05/19/2005
82	144	Flash Media Ctrl		FINO-PC	05/19/2005
83	145	Flash Connector		FINO-PC	05/19/2005
84	147	AUDIO: CODEC		FINO-SO	05/19/2005
85	148	AUDIO: LINE INPUT AMP		FINO-SO	05/19/2005
86	150	AUDIO: LINE OUT AMP		FINO-SO	05/19/2005
87	152	AUDIO: SPEAKER AMP		FINO-SO	05/19/2005
88	153	AUDIO: CONNECTORS		FINO-SO	05/19/2005
89	154	AUDIO: POWER SUPPLIES		FINO-SO	05/19/2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,FINO,M33

DRAWING NUMBER 051-6863 REV. 07

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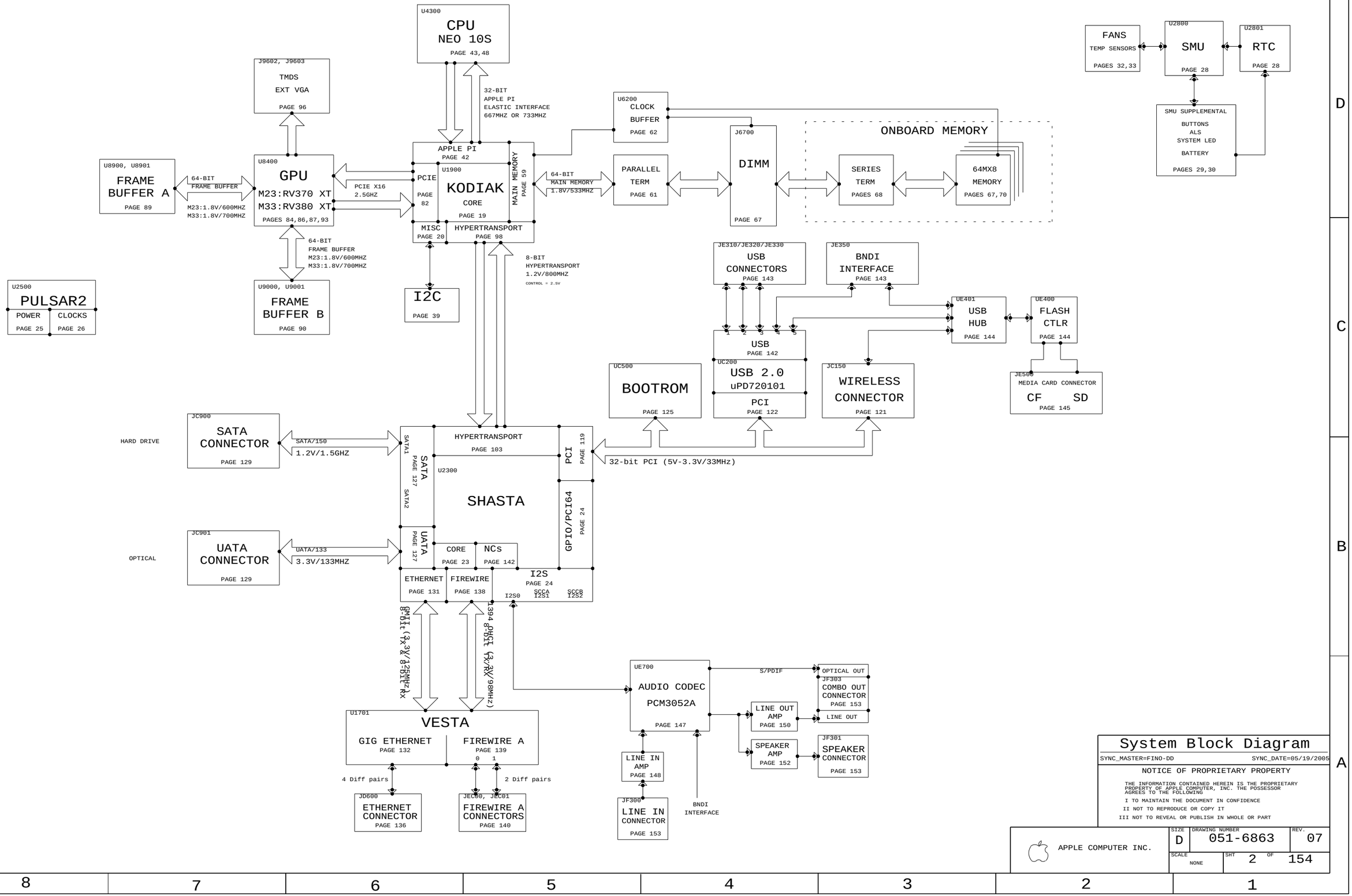

System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

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POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP12V_ALL — FW CONN

PP12V_RUN — 20" PANEL POWER, 17" LCD INVERTER

PP5V_RUN — OPTICAL

PP5V_ALL

PP3V3_ALL

PP3V3_RUN — PCI BUS, AUDIO CODEC

SMU

SYS_POWERUP_L
POWER SEQUENCE PIN

- NC_SMU_PWRSEQ_P1_0 — SMU_PWRSEQ_P1_0
- NC_SMU_PWRSEQ_P1_4 — SMU_PWRSEQ_P1_4
- TURN_ON_PP1V2_L — SMU_PWRSEQ_P1_1
- PP3V3_PWRON
- PWR_GOOD_PP1V2 — SMU_PWRSEQ_P9_5
- PWR_GOOD_PP1V8 — SMU_PWRSEQ_P9_6
- TURN_ON_PP3V3_PWRON_L — SMU_PWRSEQ_P1_2
- SMU_PWRSEQ_P1_3

PP1V5_PWRON SWITCHER
PAGE 12
PULSAR
KODIAK CORE

PP1V5_RUN FET SWITCH
PAGE 12
EI

CPU CORE SWITCHER
PAGE 50

GPU CORE SWITCHER
PAGE 85

PP1V8_PWRON SWITCHER
PAGE 11
MAIN MEMORY

PP1V8_RUN
IN
PP1V8_RUN POWER SW
PAGE 11
GPU MEMORY

PP0V9_GPU_VTT LINEAR
PAGE 91

PP4V5_RUN_AUDIO LINEAR
PAGE 154
AUDIO CODEC

PP5V_PWRON FET SWITCH
PAGE 16
USB CONN

PP3V3_PWRON FET SWITCH
PAGE 16
MODEM & BT
USB2 HOST

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 54

PP2V5_GPU_A2VDD LINEAR
PAGE 85

PP1V8_TPVDD LINEAR
PAGE 85

PP1V5_VDDC_CT LINEAR
PAGE 85

PP2V5_ALL LINEAR
PAGE 15
VESTA

PP2V5_PWRON FET SWITCH
PAGE 15

PP2V5_RUN FET SWITCH
PAGE 15

PP1V8_GPU LINEAR
PAGE 85

PP1V2_ALL SWITCHER
PAGE 13
VESTA CORE

PP1V2_TPVDD LINEAR
PAGE 85

PP1V2_PWRON FET SWITCH
PAGE 13
SHASTA CORE

PP1V2_RUN FET SWITCH
PAGE 13
HT BUS

PP1V2_PWRON

PP2V5_ALL
R431 10K 5% 1/16W MF-LF 402

R430 100K 5% 1/10W MF-LF 402
COMPARE_PP1V2
C430 0.01UF 20% 16V CERM 402
PS_1V_REF
LM339A SOI-LF
U400 V+ GND

PP2V5_ALL
R442 150K 5% 1/16W MF-LF 402
PS_1V_REF
PP5V_ALL
LM339A SOI-LF
U400 V+ GND
PP2V5_ALL
R441 10K 5% 1/16W MF-LF 402

R440 100K 5% 1/16W MF-LF 402
COMPARE_PP1V8
C440 0.01UF 20% 16V CERM 402
R443 100K 1% 1/16W MF-LF 402
C441 0.1UF 20% 16V CERM 402

PP2V5_ALL
U400P2
LM339A SOI-LF
U400 V+ GND

Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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PROCESSORS

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3158	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,CQA	2.0GHZ	1.15V	46W	50MV	U4300	CPU_2_0GHZ
337S3157	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.2G,85C,FQA	2.2GHZ	1.15V	51W	50MV	U4300	CPU_2_2GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3165	337S3158	CPU_2_0GHZ	U4300	IC,DD3.1,2.0G,CJA	1.20V
337S3164	337S3157	CPU_2_2GHZ	U4300	IC,DD3.1,2.0G,FJA	1.20V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0371	1	IC,KODIAK,V1.1,PBGA,200MM	U1900	
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	
343S0324	1	IC,ASIC,VESTA,V1.3	U1701	
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
825-6447	1	BARCODE LABEL, MLB	LBL1	
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500	
341T1752	1	PURCH ASSY, SMU BIG	U2800	
603-7318	1	M23 CPU HEATSINK	MECH1	17_INCH_LCD
603-7321	1	M33 CPU HEATSINK	MECH1	20_INCH_LCD
603-7322	1	M33 GPU HEATSINK	MECH2	20_INCH_LCD
875-1614	1	CPU GAP FILLER	GAP1	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702	KINGBRIGHT LED
376S0204	376S0130		Q5010,Q5020	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q5011,Q5021	MOSFET,N-CH,VISHAY

Table Items

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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NO TEST XW NETS

1017	NO_TEST=YES	GND_U1100	11
1018	NO_TEST=YES	GND_U1200	12
1048	NO_TEST=YES	GND_U1300	13
1050	NO_TEST=YES	PP_2V5PWRONNBMISC	20
1051	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
1052	NO_TEST=YES	PP_3V3PWRONSBPCIG4	23
1053	NO_TEST=YES	PP_2V5PWRONSB	23
1054	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
1055	NO_TEST=YES	PP_OVDD_PULSAR1	25
1056	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
1057	NO_TEST=YES	PP_1V5PULSAR2	25
1058	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
1059	NO_TEST=YES	GND_SMU_AVSS	28 55
1060	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
1061	NO_TEST=YES	PP_3V3ALLSMU	28
1062	NO_TEST=YES	PP_VEINB	41
1063	NO_TEST=YES	GND_CPU_AVDD	48
1064	NO_TEST=YES	VC_AGND	50
1065	NO_TEST=YES	VC_OUTSEN_R	50
1066	NO_TEST=YES	KPVDD2_FMAX	55
1066	NO_TEST=YES	GND_GPU_PVSS	86
1077	NO_TEST=YES	GND_GPU_MPVSS	87
1146	NO_TEST=YES	GND_AUDIO_MIC	153 154

1078	NO_TEST=YES	GND_GPU_TPVSS	93
1140	NO_TEST=YES	GND_GPU_TXVSSR	93
1092	NO_TEST=YES	GND_GPU_VSSDI	93
1160	NO_TEST=YES	GND_GPU_AVSSN	93
1160	NO_TEST=YES	GND_GPU_AVSSQ	93
1112	NO_TEST=YES	GND_GPU_A2VSSN	93
1112	NO_TEST=YES	GND_GPU_A2VSSQ	93
1140	NO_TEST=YES	KOD_L15_GND	98 101
1160	NO_TEST=YES	PP_3V3SBPCI_B9	119
1160	NO_TEST=YES	PP_2V5PWRONSB_B9	119
1160	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
1161	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
1160	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
1161	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
1162	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
1160	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
1160	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
1162	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
1163	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
1160	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
1163	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
1140	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
1140	NO_TEST=YES	GND_AUD_LOAMP	150 154

1101	NO_TEST=YES	GND_NEC_AVSS_R	142
1140	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
1161	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
1161	NO_TEST=YES	KPGND2_FMAX	55
1161	NO_TEST=YES	TDIODE_POS_FMAX	55
1161	NO_TEST=YES	TDIODE_NEG_FMAX	55
1161	NO_TEST=YES	DAGND	55
1161	NO_TEST=YES	INA138_OUT	55
1162	NO_TEST=YES	RAMCLK_AVSS	62
1160	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
1160	NO_TEST=YES	GND_AUDIO	7 154
1160	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
1160	NO_TEST=YES	KOD_H05_GND	82 97
1160	NO_TEST=YES	KOD_K07_GND	82 97
1160	NO_TEST=YES	KOD_G10_GND	82 97
1160	NO_TEST=YES	KOD_J13_GND	82 97
1160	NO_TEST=YES	KOD_L13_GND	82 97
1160	NO_TEST=YES	KOD_H08_GND	82 97
1160	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
1160	NO_TEST=YES	U8500_GND	85
1160	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

1055	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
1057	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
1058	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
1059	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
1060	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
1061	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
1062	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
1063	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
1064	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
1065	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56

1069	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
1072	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
1072	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
1073	NO_TEST=YES	NC_CPU_A1_QACK_L	56
1076	NO_TEST=YES	NC_CPU_B0_QACK_L	56
1074	NO_TEST=YES	NC_CPU_B1_QACK_L	56
1076	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
1076	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
1077	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
1082	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
1104	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
1104	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
1104	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
1104	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
1104	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
1105	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
1105	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
1105	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
1105	NO_TEST=YES	NC_A_AVREG_0	82
1105	NO_TEST=YES	NC_A_AVREG_1	82
1105	NO_TEST=YES	NC_A_AVREG_2	82
1105	NO_TEST=YES	NC_CPU_B_APSYNC	27
1105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
1105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
1105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
1105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
1100	NO_TEST=YES	NC_J2904_11	29
1100	NO_TEST=YES	NC_J2904_12	29
1100	NO_TEST=YES	NC_NCV1009_1	55
1100	NO_TEST=YES	NC_NCV1009_2	55
1100	NO_TEST=YES	NC_NCV1009_3	55
1100	NO_TEST=YES	NC_NCV1009_4	55
1100	NO_TEST=YES	NC_NCV1009_5	55
1100	NO_TEST=YES	NC_NCV1009_ADJ	55
1100	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
1107	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
1107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
1107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4

1110	NO_TEST=YES	RFBD<38>	88 89
1110	NO_TEST=YES	RFBD<37>	88 89
1110	NO_TEST=YES	RFBD<36>	88 89
1110	NO_TEST=YES	RFBD<34>	88 89
1110	NO_TEST=YES	RFBD<33>	88 89
1110	NO_TEST=YES	RFBD<32>	88 89
1110	NO_TEST=YES	RFBD<31>	88 89
1110	NO_TEST=YES	RFBD<30>	88 89
1117	NO_TEST=YES	RFBD<28>	88 89
1117	NO_TEST=YES	RFBD<27>	88 89
1117	NO_TEST=YES	RFBD<26>	88 89
1117	NO_TEST=YES	RFBD<25>	88 89
1117	NO_TEST=YES	RFBD<23>	88 89
1117	NO_TEST=YES	RFBD<22>	88 89
1117	NO_TEST=YES	RFBD<21>	88 89

1160	NO_TEST=YES	KPVDD2	48 50 55
1160	NO_TEST=YES	KPGND2	48 50 55
1160	NO_TEST=YES	CPU_DIODE_POS	48 55
1160	NO_TEST=YES	CPU_DIODE_NEG	48 55
1110	NO_TEST=YES	FMAXT_P	55
1110	NO_TEST=YES	FMAXT_M	55
1110	NO_TEST=YES	CORE_ISNS_P	55
1110	NO_TEST=YES	CORE_ISNS_M	55
1110	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
1110	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
1110	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
1110	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
1110	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
1110	NO_TEST=YES	NC_I2S2_MCLK	154
1111	NO_TEST=YES	NC_SATA_RXD_N2_C	129
1111	NO_TEST=YES	NC_SATA_RXD_P2_C	129
1111	NO_TEST=YES	NC_SATA_TXD_N2	129
1111	NO_TEST=YES	NC_SATA_TXD_P2	129
1111	NO_TEST=YES	TP_SB<29>	142
1111	NO_TEST=YES	TP_SB<28>	142
1111	NO_TEST=YES	TP_SB<27>	142
1111	NO_TEST=YES	TP_SB<26>	142
1111	NO_TEST=YES	TP_SB<25>	142
1112	NO_TEST=YES	TP_SB<24>	142
1112	NO_TEST=YES	TP_SB<23>	142
1112	NO_TEST=YES	TP_SB<22>	142
1112	NO_TEST=YES	TP_SB<21>	142
1112	NO_TEST=YES	TP_SB<20>	142
1112	NO_TEST=YES	TP_SB<19>	142
1112	NO_TEST=YES	TP_SB<18>	142
1112	NO_TEST=YES	TP_SB<17>	142
1112	NO_TEST=YES	TP_SB<16>	142
1112	NO_TEST=YES	TP_SB<15>	142
1112	NO_TEST=YES	TP_SB<14>	142
1113	NO_TEST=YES	TP_SB<13>	142
1113	NO_TEST=YES	TP_SB<12>	142
1113	NO_TEST=YES	TP_SB<11>	142
1113	NO_TEST=YES	TP_SB<10>	142
1113	NO_TEST=YES	TP_SB<9>	142
1113	NO_TEST=YES	TP_SB<8>	142
1113	NO_TEST=YES	TP_SB<7>	142
1113	NO_TEST=YES	TP_SB<6>	142
1113	NO_TEST=YES	TP_SB<5>	142
1114	NO_TEST=YES	TP_SB<4>	142
1114	NO_TEST=YES	TP_SB<3>	142
1114	NO_TEST=YES	TP_SB<2>	142
1114	NO_TEST=YES	TP_SB<1>	142
1114	NO_TEST=YES	TP_SB<0>	142
1115	NO_TEST=YES	RFBD<61>	88 89
1115	NO_TEST=YES	RFBD<60>	88 89
1115	NO_TEST=YES	RFBD<59>	88 89
1117	NO_TEST=YES	RFBD<57>	88 89
1118	NO_TEST=YES	RFBD<56>	88 89
1118	NO_TEST=YES	RFBD<54>	88 89
1118	NO_TEST=YES	RFBD<53>	88 89
1118	NO_TEST=YES	RFBD<52>	88 89
1118	NO_TEST=YES	RFBD<50>	88 89
1118	NO_TEST=YES	RFBD<49>	88 89
1118	NO_TEST=YES	RFBD<48>	88 89
1118	NO_TEST=YES	RFBD<47>	88 89
1119	NO_TEST=YES	RFBD<45>	88 89
1119	NO_TEST=YES	RFBD<44>	88 89
1119	NO_TEST=YES	RFBD<42>	88 89
1119	NO_TEST=YES	RFBD<41>	88 89
1119	NO_TEST=YES	RFBD<40>	88 89

1119	NO_TEST=YES	RFBD<126>	88 90
1120	NO_TEST=YES	RFBD<125>	88 90
1119	NO_TEST=YES	RFBD<124>	88 90
1120	NO_TEST=YES	RFBD<122>	88 90
1120	NO_TEST=YES	RFBD<121>	88 90
1120	NO_TEST=YES	RFBD<120>	88 90
1120	NO_TEST=YES	RFBD<118>	88 90
1120	NO_TEST=YES	RFBD<117>	88 90
1120	NO_TEST=YES	RFBD<116>	88 90
1121	NO_TEST=YES	RFBD<114>	88 90
1122	NO_TEST=YES	RFBD<113>	88 90
1121	NO_TEST=YES	RFBD<112>	88 90
1122	NO_TEST=YES	RFBD<110>	88 90
1123	NO_TEST=YES	RFBD<109>	88 90
1121	NO_TEST=YES	RFBD<108>	88 90
1122	NO_TEST=YES	RFBD<106>	88 90
1122	NO_TEST=YES	RFBD<105>	88 90
1122	NO_TEST=YES	RFBD<104>	88 90
1122	NO_TEST=YES	RFBD<102>	88 90
1122	NO_TEST=YES	RFBD<101>	88 90
1122	NO_TEST=YES	RFBD<100>	88 90
1122	NO_TEST=YES	RFBD<98>	88 90
1122	NO_TEST=YES	RFBD<97>	88 90
1122	NO_TEST=YES	RFBD<96>	88 90
1122	NO_TEST=YES	RFBD<95>	88 90
1122	NO_TEST=YES	RFBD<94>	88 90
1123	NO_TEST=YES	RFBD<92>	88 90
1123	NO_TEST=YES	RFBD<91>	88 90
1123	NO_TEST=YES	RFBD<90>	88 90
1123	NO_TEST=YES	RFBD<88>	88 90
1123	NO_TEST=YES	RFBD<87>	88 90
1123	NO_TEST=YES	RFBD<86>	88 90
1123	NO_TEST=YES	RFBD<85>	88 90
1124	NO_TEST=YES	RFBD<83>	88 90
1124	NO_TEST=YES	RFBD<82>	88 90
1124	NO_TEST=YES	RFBD<81>	88 90
1124	NO_TEST=YES	RFBD<79>	88 90
1124	NO_TEST=YES	RFBD<78>	88 90
1124	NO_TEST=YES	RFBD<76>	88 90
1124	NO_TEST=YES	RFBD<75>	88 90
1124	NO_TEST=YES	RFBD<74>	88 90
1125	NO_TEST=YES	RFBD<72>	88 90
1125	NO_TEST=YES	RFBD<71>	88 90
1125	NO_TEST=YES	RFBD<70>	88 90
1125	NO_TEST=YES	RFBD<69>	88 90
1125	NO_TEST=YES	RFBD<67>	88 90
1125	NO_TEST=YES	RFBD<66>	88 90
1125	NO_TEST=YES	RFBD<65>	88 90
1126	NO_TEST=YES	RFBD<62>	88 89

1800	NO_TEST=YES	TP_FBBCS1_L	87
1824	NO_TEST=YES	AUD_4V5_FB	154
1837	NO_TEST=YES	ITS_RUNNING	7
1838	NO_TEST=YES	LED801_1	8
1839	NO_TEST=YES	LED802_1	8
1841	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
1844	NO_TEST=YES	Q800_D	8
1844	NO_TEST=YES	Q800_G	8
1848	NO_TEST=YES	Q801_B	8
1849	NO_TEST=YES	Q802_B	8
1850	NO_TEST=YES	Q802_E	8
1851	NO_TEST=YES	Q803_B	8
1842	NO_TEST=YES	TP_USB2_PWREN<0>	143
1842	NO_TEST=YES	TP_USB2_PWREN<1>	143
1827	NO_TEST=YES	TP_SB_FSTEST	24
1827	NO_TEST=YES	TP_SB_PLLTEST	24
1834	NO_TEST=YES	TP_USB2_PWREN<2>	143
1835	NO_TEST=YES	TP_USB2_PWREN<3>	143
1834	NO_TEST=YES	TP_USB2_PWREN<4>	143
1835	NO_TEST=YES	TP_NEC_NTEST1	122
1835	NO_TEST=YES	TP_NEC_SMC	122
1835	NO_TEST=YES	TP_NEC_SMI_L	122
1835	NO_TEST=YES	TP_NEC_SRCLK	122
1835	NO_TEST=YES	TP_NEC_SRMOD	122
1835	NO_TEST=YES	TP_NEC_TEST	122
1808	NO_TEST=YES	UATA_DASP_L_DS	129
1126	NO_TEST=YES	RFBD<19>	88 89
1126	NO_TEST=YES	RFBD<18>	88 89
1126	NO_TEST=YES	RFBD<16>	88 89
1126	NO_TEST=YES	RFBD<15>	88 89
1126	NO_TEST=YES	RFBD<14>	88 89
1126	NO_TEST=YES	RFBD<13>	88 89
1127	NO_TEST=YES	RFBD<11>	88 89
1127	NO_TEST=YES	RFBD<10>	88 89
1127	NO_TEST=YES	RFBD<8>	88 89
1127	NO_TEST=YES	RFBD<7>	88 89
1127	NO_TEST=YES	RFBD<6>	88 89
1127	NO_TEST=YES	RFBD<5>	88 89
1127	NO_TEST=YES	RFBD<3>	88 89
1128	NO_TEST=YES	RFBD<2>	88 89
1128	NO_TEST=YES	RFBD<1>	88 89
1128	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
1128	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<39>	61 68 70
1130	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
1131	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
1131	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
1131	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
1131	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
1133	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<26>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
1132	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
1132	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
1132	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
1132	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
1132	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
1132	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
1133	NO_TEST=YES	RAM_DQ_R<11>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<10>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
1134	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST NETS

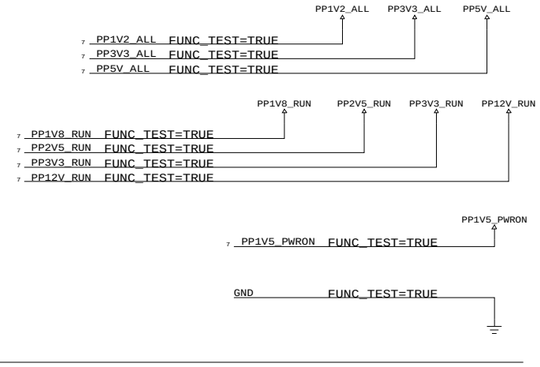
NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

1108	FUNC_TEST=TRUE	PPVCORE_CPU	50
1108	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
1108	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
1109	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
1109	FUNC_TEST=TRUE	POWER_BUTTON_L	29
1109	FUNC_TEST=TRUE	RESET_BUTTON_L	29
1109	FUNC_TEST=TRUE	SMU_RESET_L	28 29
1109	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

1838	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
1838	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
1838	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
1838	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
1838	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
1838	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
1109	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29



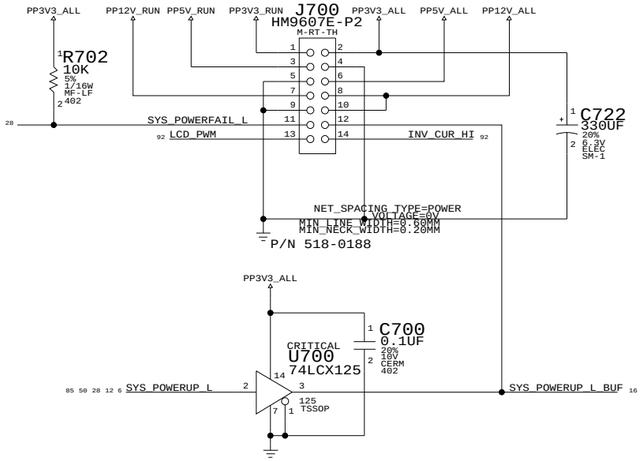
FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

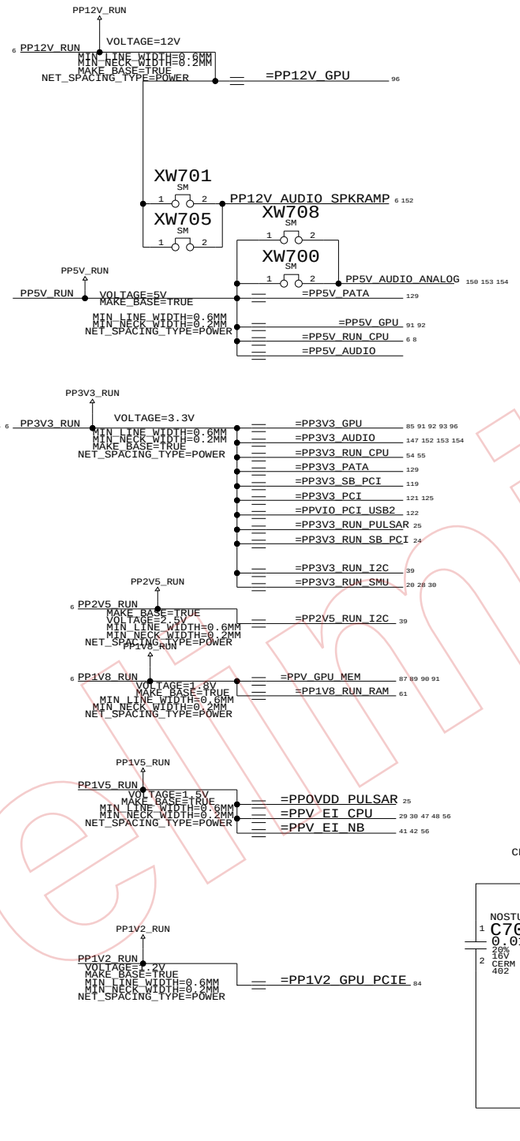
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE NONE SHT 6 OF 154



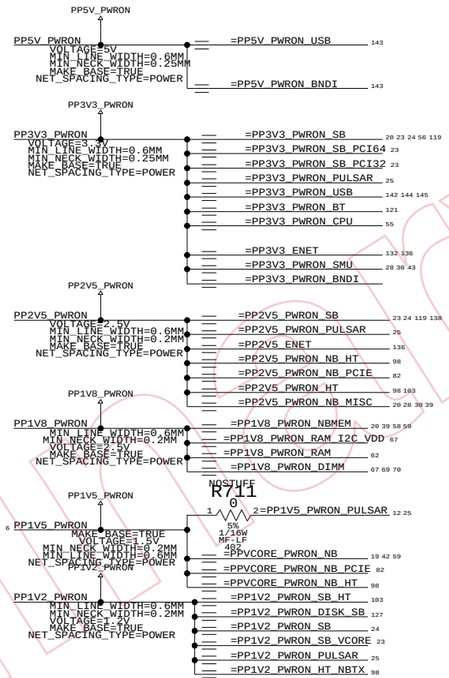
RUN RAILS

ONLY ON IN RUN



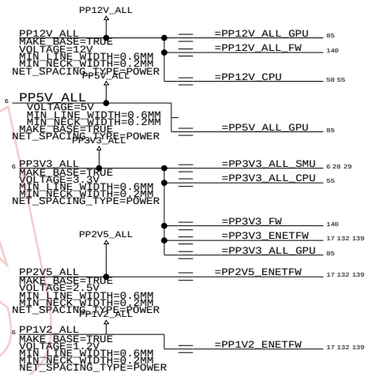
PWRON RAILS

ON IN RUN AND SLEEP

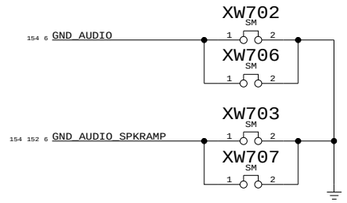


ALL RAILS

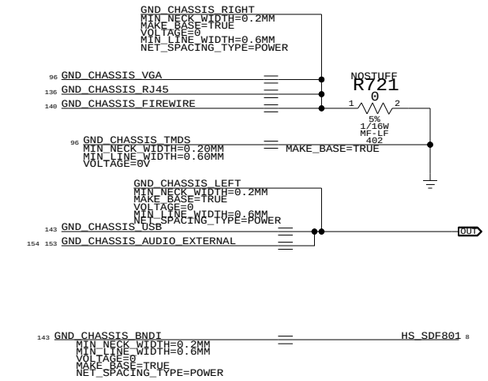
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



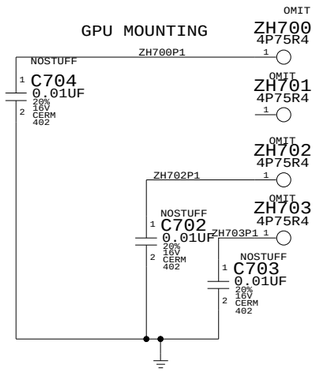
GND RAILS



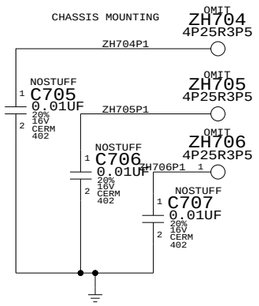
CHASSIS GND



GPU MOUNTING



CHASSIS MOUNTING



POWER CONN / ALIAS

SYNC_MASTER=M33-PC SYNC_DATE=05/19/2005

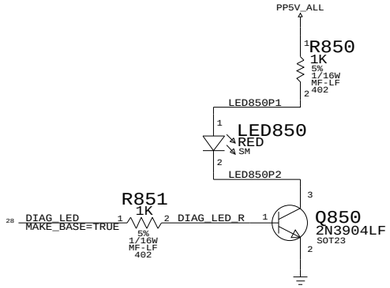
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

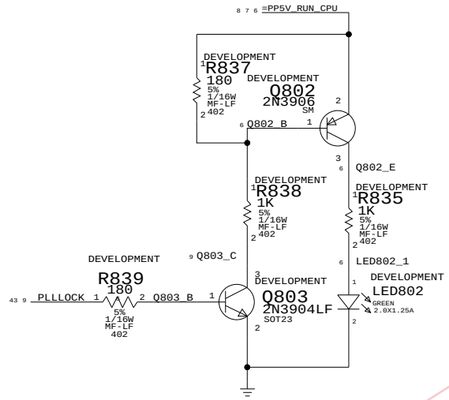
SCALE: NONE SHT 7 OF 154

DIAG LED

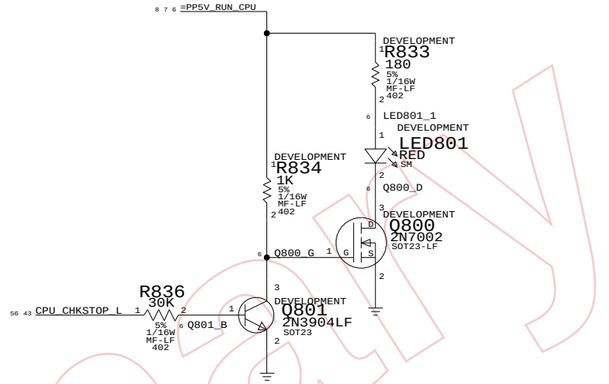
(OVERTEMP LED)



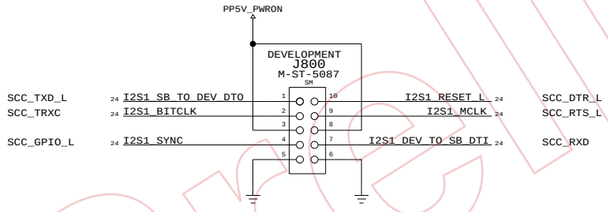
PLL LOCK LED



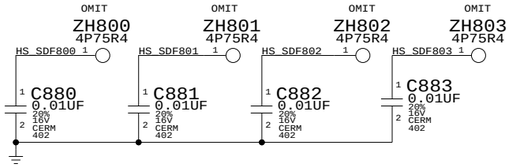
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE

SHT 8 OF 154

I1	NO_TEST=YES	ENET_TXD_R<7>	130 131
I2	NO_TEST=YES	ENET_TXD_R<6>	130 131
I3	NO_TEST=YES	ENET_TXD_R<5>	130 131
I4	NO_TEST=YES	ENET_TXD_R<4>	130 131
I5	NO_TEST=YES	ENET_TXD_R<3>	130 131
I6	NO_TEST=YES	ENET_TXD_R<2>	130 131
I7	NO_TEST=YES	ENET_TXD_R<1>	130 131
I8	NO_TEST=YES	ENET_TXD_R<0>	130 131
I9	NO_TEST=YES	ENET_TXD<7>	130 131 132
I10	NO_TEST=YES	ENET_TXD<6>	130 131 132
I12	NO_TEST=YES	ENET_TXD<5>	130 131 132
I11	NO_TEST=YES	ENET_TXD<4>	130 131 132
I13	NO_TEST=YES	ENET_TXD<3>	130 131 132
I14	NO_TEST=YES	ENET_TXD<2>	130 131 132
I15	NO_TEST=YES	ENET_TXD<1>	130 131 132
I16	NO_TEST=YES	ENET_TXD<0>	130 131 132
I18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
I17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
I19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
I20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
I21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
I22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
I24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
I23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
I25	NO_TEST=YES	ENET_RXD<7>	130 131
I26	NO_TEST=YES	ENET_RXD<6>	130 131
I27	NO_TEST=YES	ENET_RXD<5>	130 131
I28	NO_TEST=YES	ENET_RXD<4>	130 131
I30	NO_TEST=YES	ENET_RXD<3>	130 131
I29	NO_TEST=YES	ENET_RXD<2>	130 131
I31	NO_TEST=YES	ENET_RXD<1>	130 131
I32	NO_TEST=YES	ENET_RXD<0>	130 131
I33	NO_TEST=YES	ENET_TX_EN_R	130 131
I34	NO_TEST=YES	ENET_TX_ER_R	130 131
I36	NO_TEST=YES	ENET_TX_EN	130 131 132
I35	NO_TEST=YES	ENET_TX_ER	130 131 132
I37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
I38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
I39	NO_TEST=YES	NC_CPU_AFN	56
I40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
I42	NO_TEST=YES	NC_PSRO	56
I41	NO_TEST=YES	NC_PSRO_ENABLE	56
I43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
I44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
I45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
I46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
I48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
I47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
I49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
I50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
I51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
I52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
I54	NO_TEST=YES	NC_SMU_SER_SEL	31
I53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
I55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
I56	NO_TEST=YES	TP_VESTA_AN_EN	132
I57	NO_TEST=YES	TP_VESTA_DNC_C9	17
I58	NO_TEST=YES	TP_VESTA_DNC_E9	17
I60	NO_TEST=YES	TP_VESTA_EN_10B	132
I59	NO_TEST=YES	TP_VESTA_ER	132
I61	NO_TEST=YES	TP_VESTA_F1000	132
I62	NO_TEST=YES	TP_VESTA_FDX	132
I63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
I64	NO_TEST=YES	TP_VESTA_HUB	132
I66	NO_TEST=YES	TP_VESTA_LINK1_L	132
I65	NO_TEST=YES	TP_VESTA_LINK2_L	132
I67	NO_TEST=YES	TP_VESTA_MANMS	132
I68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
I69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
I70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
I72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
I71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
I73	NO_TEST=YES	TP_VESTA_RBC0	132
I74	NO_TEST=YES	TP_VESTA_RBC1	132
I75	NO_TEST=YES	TP_VESTA_REGCTL1	17
I76	NO_TEST=YES	TP_VESTA_REGCTL2	17
I78	NO_TEST=YES	TP_VESTA_REGSEN1	17
I77	NO_TEST=YES	TP_VESTA_REGSEN2	17
I79	NO_TEST=YES	TP_VESTA_REGSUP1	17
I80	NO_TEST=YES	TP_VESTA_REGSUP2	17
I81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
I82	NO_TEST=YES	TP_VESTA_SPD0	132
I84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
I83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
I85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
I86	NO_TEST=YES	TP_VESTA_TEST<0>	132
I87	NO_TEST=YES	TP_VESTA_TEST<1>	132
I88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
I90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
I89	NO_TEST=YES	TP_VESTA_TVCO	132
I222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
I223	NO_TEST=YES	TP_VESTA_FAVDDL	139
I224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
I225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

I91	NO_TEST=YES	TP_VESTA_TVCO_24	139
I92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
I93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
I94	NO_TEST=YES	TP_NB_APSYNC	44
I95	NO_TEST=YES	TP_SB_WATCHDOG	24
I96	NO_TEST=YES	NC_CPU_TBEN_CLK	27
I97	NO_TEST=YES	NC_J3108_10	31
I98	NO_TEST=YES	NC_J3108_11	31
I99	NO_TEST=YES	NC_J3108_12	31
I100	NO_TEST=YES	NC_J3108_8	31
I101	NO_TEST=YES	NC_J3108_9	31
I102	NO_TEST=YES	NC_JTAGMUX_3	30
I103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

I109	NO_TEST=YES	Q803_C	8
I108	NO_TEST=YES	PLLLOCK	8 43

I114	NO_TEST=YES	LED_PP1V8_RUN_P	11
I117	NO_TEST=YES	LED_PP1V8_RUN_N	11
I118	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
I115	NO_TEST=YES	LED_PP1V5_RUN_N	12
I116	NO_TEST=YES	LED_PP1V5_RUN_P	12
I119	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
I120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
I123	NO_TEST=YES	LED_PP1V2_RUN_N	13
I124	NO_TEST=YES	LED_PP1V2_RUN_P	13
I122	NO_TEST=YES	KP_V<1>	55
I121	NO_TEST=YES	KP_V<2>	55
I125	NO_TEST=YES	CPU_SENSE_KP_V	55
I126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
I127	NO_TEST=YES	NB_PLL_OUT_TRG	59
I128	NO_TEST=YES	PP5V_T555	92
I133	NO_TEST=YES	T555_DISC	92
I130	NO_TEST=YES	T555_THRES	92
I129	NO_TEST=YES	T555_OUT	92
I132	NO_TEST=YES	T555_PWM	92
I131	NO_TEST=YES	PP3V3_GPU_TSENSE	
I134	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
I135	NO_TEST=YES	TSENSE_GPU_ADD0	93
I136	NO_TEST=YES	TSENSE_GPU_ADD1	93
I137	NO_TEST=YES	GPU_DIODE_PLUS	93
I138	NO_TEST=YES	GPU_DIODE_MINUS	93
I139	NO_TEST=YES	LED8700_P	136
I140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET.

I143	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
I144	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
I145	NO_TEST=YES	CPU_A_APSYNC_R	26
I146	NO_TEST=YES	CPU_B_APSYNC_R	26
I149	NO_TEST=YES	NB_APSYNC_R	26
I150	NO_TEST=YES	HT_SB_REFCLK_R	26
I147	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
I148	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
I140	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
I139	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
I151	NO_TEST=YES	NB_PMR_CLK_P_R	26
I155	NO_TEST=YES	NB_PMR_CLK_N_R	26
I153	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
I154	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
I156	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
I158	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
I157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
I159	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
I152	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
I160	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
I162	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
I161	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
I163	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
I164	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
I165	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
I166	NO_TEST=YES	QUA0_REF_25MHZ_R	26
I167	NO_TEST=YES	SB_CLK25M_SATA_R	26
I168	NO_TEST=YES	QUA1_REF_25MHZ_R	26
I169	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
I170	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
I171	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
I172	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

I170	NO_TEST=YES	100M_N<0>	82 97
I171	NO_TEST=YES	100M_P<0>	82 97
I173	NO_TEST=YES	CKA_N<0>	84 97
I172	NO_TEST=YES	CKA_P<0>	84 97
I177	NO_TEST=YES	HT_NB_N<0>	98 101
I176	NO_TEST=YES	HT_NB_P<0>	98 101
I179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
I178	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
I185	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
I187	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
I186	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
I188	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
I181	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
I180	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
I182	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
I183	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
I189	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	82 84 97
I191	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	82 84 97
I192	NO_TEST=YES	UATA_DA<0>	127 129
I193	NO_TEST=YES	UATA_DD<1>	127 129
I194	NO_TEST=YES	UATA_DD<14>	127 129
I195	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	82 84 97
I196	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	82 84 97
I197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	82 97
I198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	82 97
I199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	82 84 97
I200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	82 84 97
I201	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	82 97
I202	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	82 97
I203	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	82 97
I204	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	82 97
I205	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	82 97
I206	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
I208	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
I207	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
I210	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
I209	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
I211	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
I213	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
I212	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
I214	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
I216	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
I215	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	43 56
I218	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	43 56
I217	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
I219	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
I221	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	43 56
I220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

I220	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
I222	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
I226	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
I224	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
I230	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24

I232	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
I234	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
I233	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
I236	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
I235	FUNC_TEST=TRUE	JTAG_NB_TRST_L	

I238	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	
I240	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	
I239	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	
I242	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	
I241	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	

I244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
I246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
I245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
I248	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
I247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

FUNC TEST 2 OF 2

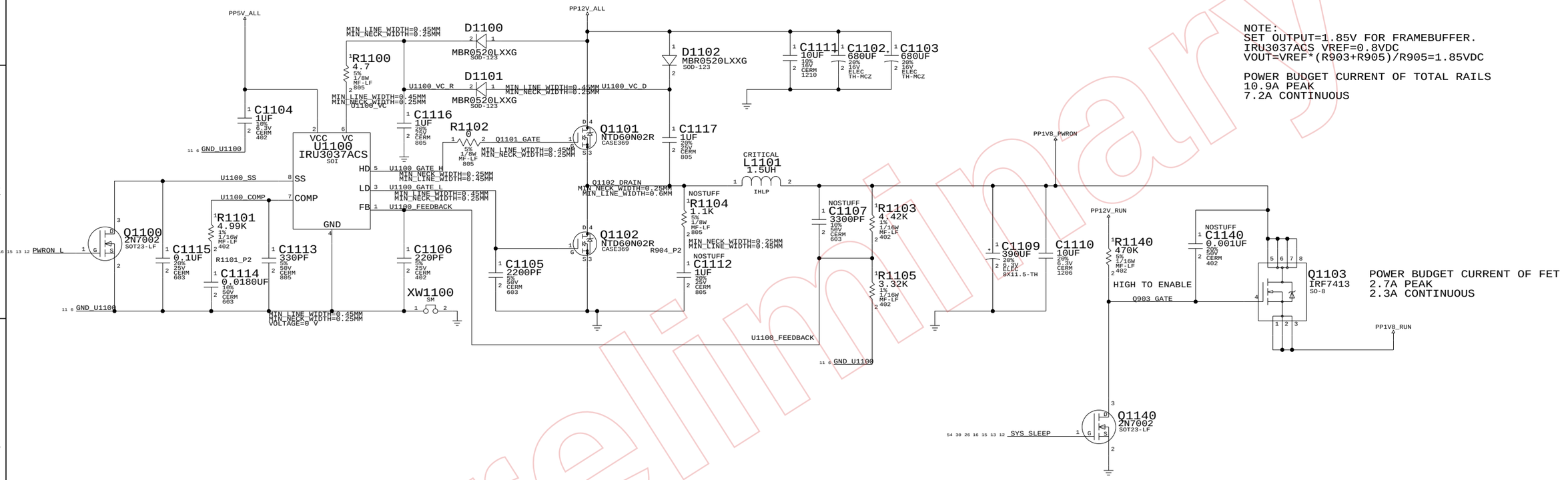
SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT 9 OF 154

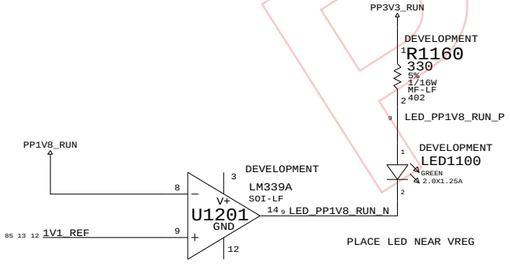
1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
10.9A PEAK
7.2A CONTINUOUS

POWER BUDGET CURRENT OF FET
2.7A PEAK
2.3A CONTINUOUS



1.8V VREG

SYNC_MASTER=M33-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 11 OF 154	

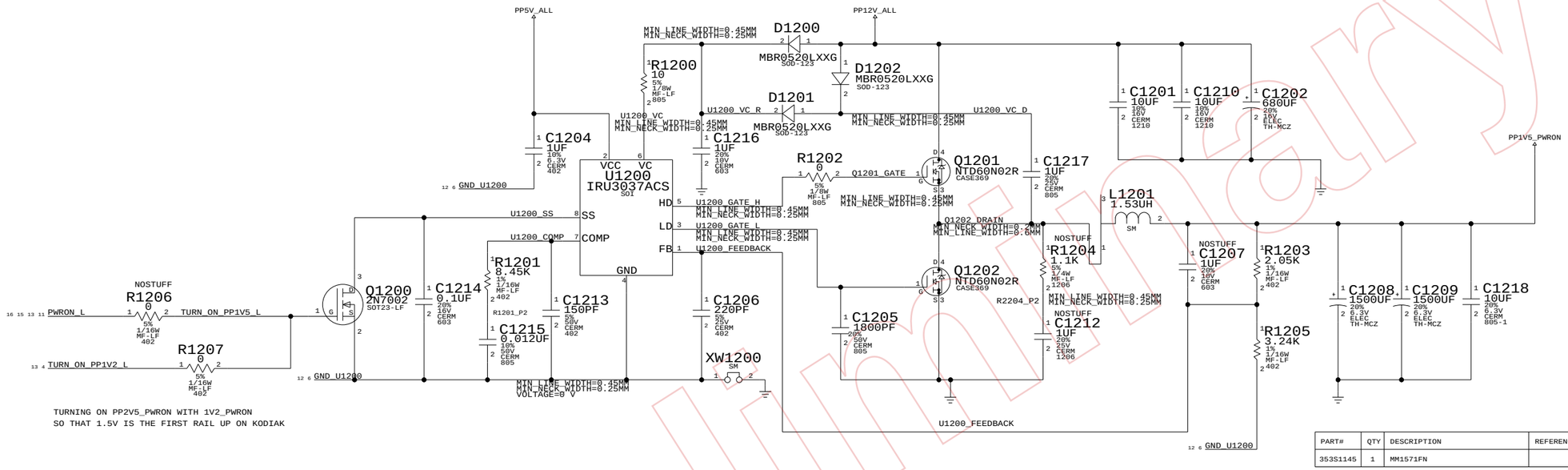
KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.30VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

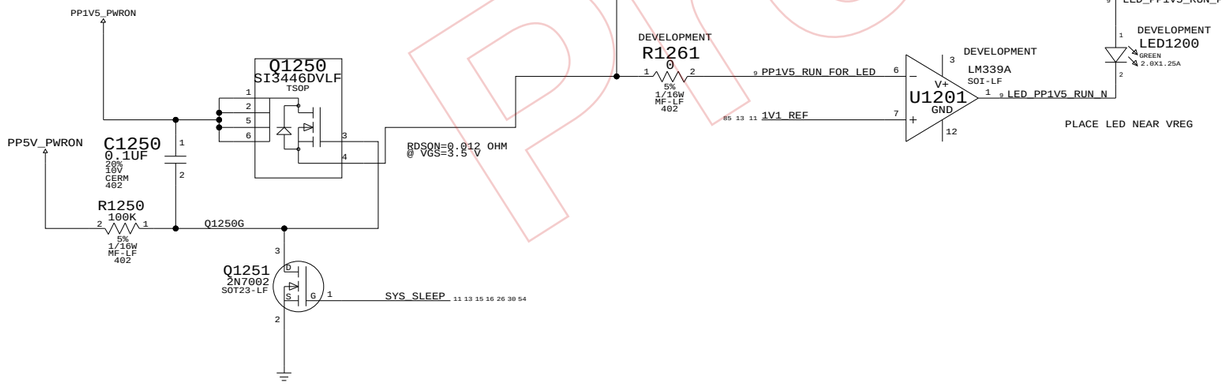
1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=4.02K



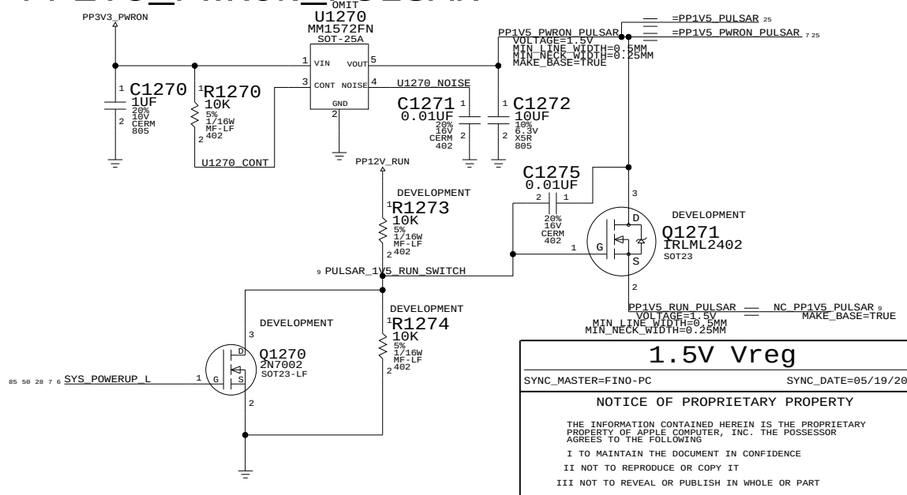
TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1145	1	MM1571FN	U1270	CRITICAL	

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW



PP1V5_PWRON_PULSAR



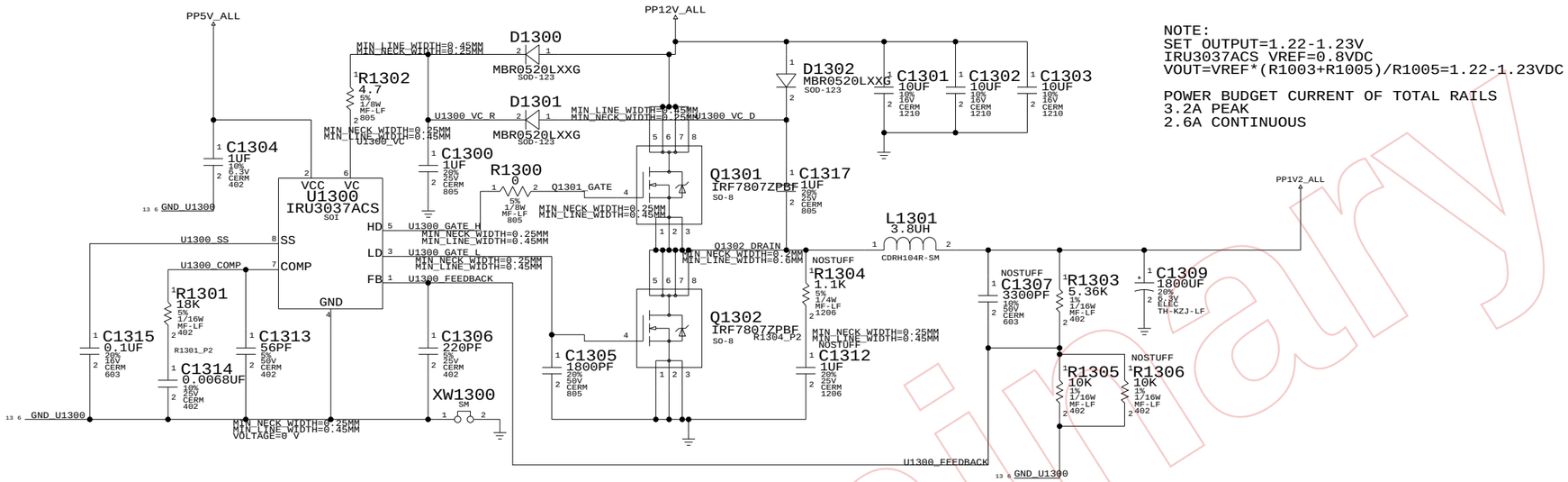
1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 12 OF 154	

PP1V2_ALL VOLTAGE REGULATOR

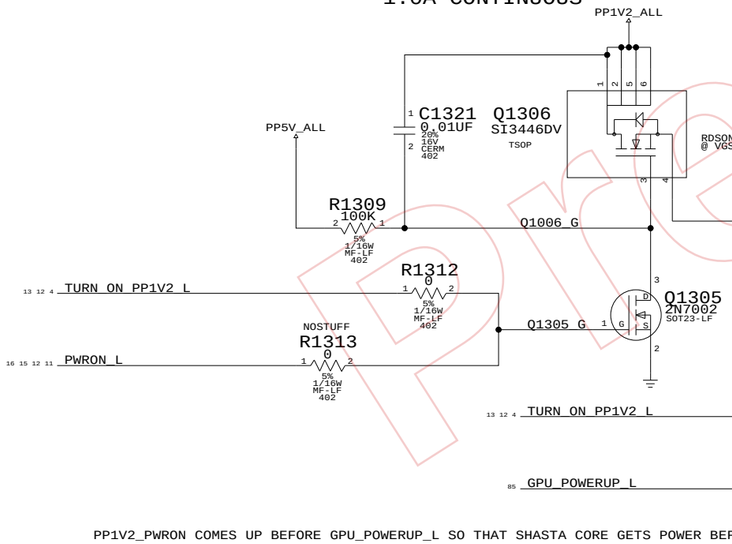


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

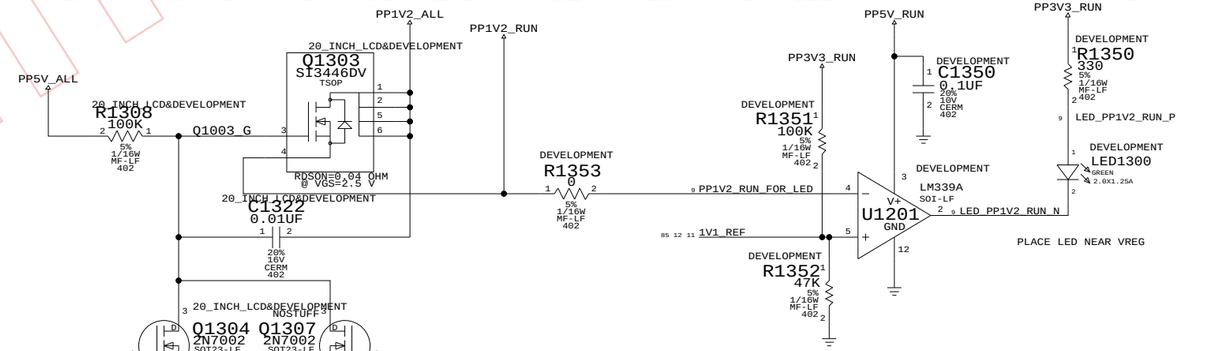
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

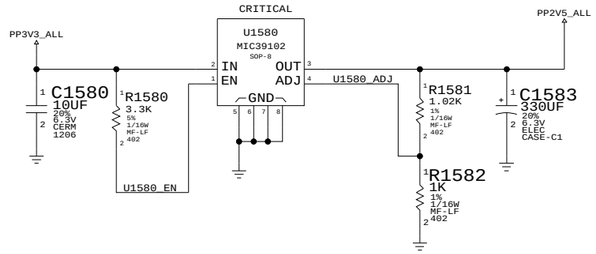
PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg	
SYNC_MASTER=FINO-PC	SYNC_DATE=05/19/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
	SCALE: NONE	SHT 13 OF 154	

PP2V5_ALL VOLTAGE REGULATOR

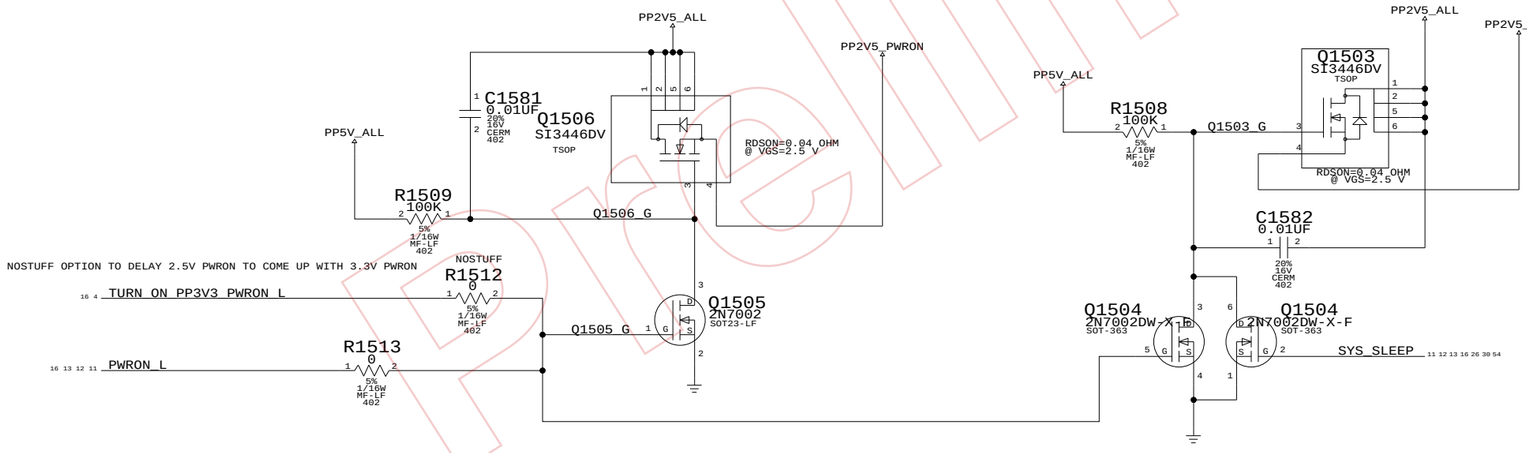


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A

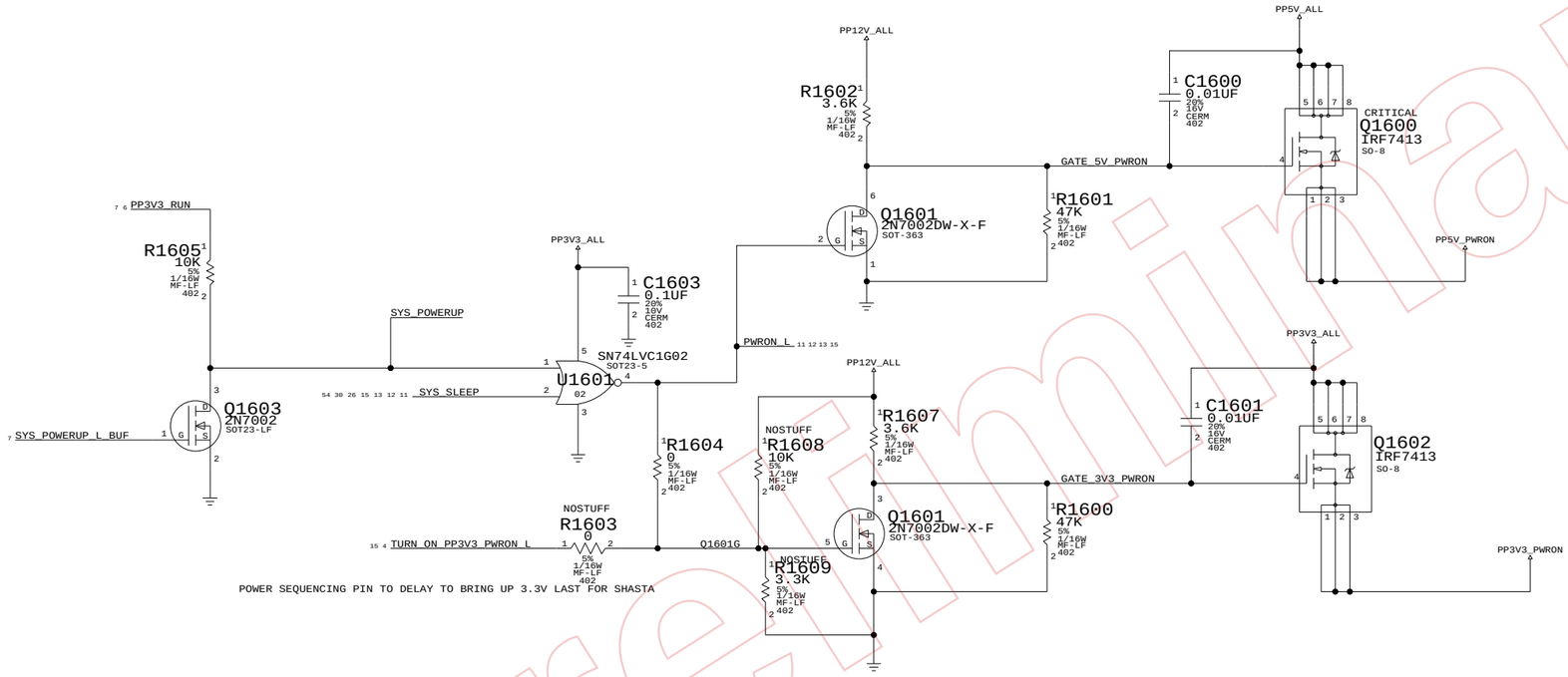


PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A

2.5V Vreg	
SYNC_MASTER=FINO-PC	SYNC_DATE=05/19/2005

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6863	REV: 07
	SCALE: NONE	SHT: 15 OF 154	



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 16 OF 154	

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

139 132 17 7 =PP3V3_ENETFW

VESTA HAS INTERNAL PULLUPS. MLB PULLUPS MAY BE NOSTUFFED IN EVT.

R1741 1K 5% 1/16W MF-LF 402
R1742 1K 5% 1/16W MF-LF 402
R1743 1K 5% 1/16W MF-LF 402

TP_JTAG_VESTA_TCK	MAKE_BASE=TRUE	=JTAG_VESTA_TCK	17
TP_JTAG_VESTA_TDI	MAKE_BASE=TRUE	=JTAG_VESTA_TDI	17
TP_JTAG_VESTA_TDO	MAKE_BASE=TRUE	=JTAG_VESTA_TDO	17
TP_JTAG_VESTA_TMS	MAKE_BASE=TRUE	=JTAG_VESTA_TMS	17
TP_JTAG_VESTA_TRST_L	MAKE_BASE=TRUE	=JTAG_VESTA_TRST_L	

R1740 1K 5% 1/16W MF-LF 402

139 132 7 =PP1V2_ENETFW

L1700 FERR-EMI-600-OHM SM
PP1V2_VESTA_AVDDL
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.2V

C1708 10UF 10% 6.3V X5R 805
C1700 0.1uF 20% 10V CERM 402 (L6/M6)
C1701 0.1uF 20% 10V CERM 402 (L9/M9)
C1702 0.1uF 20% 10V CERM 402 (N5/N6)
C1703 0.1uF 20% 10V CERM 402 (N9/N10)

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1750 10K 5% 1/16W MF-LF 402

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1751 47K 5% 1/16W MF-LF 402

VESTA_RESET_RC

Q1750 2N7002DW-X-F SOT-363

C1750 1UF 10% 6.3V CERM 402

C1714 10UF 10% 6.3V X5R 805
C1710 0.1uF 20% 10V CERM 402
C1711 0.1uF 20% 10V CERM 402
C1712 0.1uF 20% 10V CERM 402
C1713 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

R1752 10K 5% 1/16W MF-LF 402

VESTA_RESET_L
SCHMITT TRIGGER W/ INTERNAL PULLUP

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

NOSTUFF
R1720 0 5% 1/16W MF-LF 402

24 ENETFW_RESET

Q1750 2N7002DW-X-F SOT-363

132 VESTA_RESET_H

To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

VESTA MISC

U1701
VESTA-V1.3
FBGA-200-LF
1 OF 3
OMIT

RESET* IPU	H4	VESTA_RESET_L	
TDI IPU	D7	17 =JTAG_VESTA_TDI	
TDO	E10	17 =JTAG_VESTA_TDO	
TCK IPU	E7	17 =JTAG_VESTA_TCK	
TMS IPU	E8	17 =JTAG_VESTA_TMS	
TRST* IPU	D8	17 =JTAG_VESTA_TRST_L	
DNC	C9	9 TP_VESTA_DNC_C9	
DNC	E9	9 TP_VESTA_DNC_E9	
NC	C3	NC	
NC	M13	NC	

DVDD B1 B15 C15 J1
AVDDL L6 L9 M6 M9 M5 N6 N9 N10
AVDD P4 P5 P10 P11 R3 R12
PVDD A15 N4
OVDD A1 A7 F15 K1
AGND H11 H12 J11 J12 L7 L8 M7 M8 N7 N8 P6 P7 P8 P9
GND A2 B2 B7 C14 F14 J2 K2

IPD 2.5V_EN M3 TP_VESTA_2_5V_EN 9

REGSUP1	E1	TP_VESTA_REGSUP1	9
REGSEN1	F1	TP_VESTA_REGSEN1	9
REGCTL1	G5	TP_VESTA_REGCTL1	9
REGSUP2	E2	TP_VESTA_REGSUP2	9
REGSEN2	F2	TP_VESTA_REGSEN2	9
REGCTL2	G4	TP_VESTA_REGCTL2	9

M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS

=PP2V5_ENETFW 7 132 139

C1720 0.1uF 20% 10V CERM 402
C1721 0.1uF 20% 10V CERM 402
C1722 0.1uF 20% 10V CERM 402
C1723 0.1uF 20% 10V CERM 402
C1724 0.1uF 20% 10V CERM 402
C1725 0.1uF 20% 10V CERM 402
C1726 10UF 10% 6.3V X5R 805

C1730 0.1uF 20% 10V CERM 402
C1731 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

C1740 0.1uF 20% 10V CERM 402
C1741 0.1uF 20% 10V CERM 402
C1742 0.1uF 20% 10V CERM 402
C1743 0.1uF 20% 10V CERM 402
C1744 10UF 10% 6.3V X5R 805

2.5V_EN
0 - OVDD=3.3V
1 - OVDD=2.5V
WHEN OVDD=2.5V GMII PINS ARE NOT 3.3V TOLERANT

Vesta Core / Misc

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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59A6 42A4 20A8 3A4 =PPVCORE_PWRON_NB

KODIAK CORE
PP1900
P4MM
1.6V (PP) 3M 1
Q63 = PP1V6

SEE_TABLE

U1900
KODIAK-ASIC-040812
CORE & PCI-E POWER
BGA
(9 OF 10)
(1.6V-1.2V)

N15	VDD_CORE	CORE_GND	N14
P17	VDD_CORE	CORE_GND	P16
P21	VDD_CORE	CORE_GND	P20
R14	VDD_CORE	CORE_GND	R15
R18	VDD_CORE	CORE_GND	R19
R22	VDD_CORE	CORE_GND	R23
T16	VDD_CORE	CORE_GND	T17
T20	VDD_CORE	CORE_GND	T21
U15	VDD_CORE	CORE_GND	U14
U19	VDD_CORE	CORE_GND	U18
V17	VDD_CORE	CORE_GND	V16
V21	VDD_CORE	CORE_GND	V20
W14	VDD_CORE	CORE_GND	W15
W18	VDD_CORE	CORE_GND	W19
W22	VDD_CORE	CORE_GND	W23
Y16	VDD_CORE	CORE_GND	Y17
Y20	VDD_CORE	CORE_GND	Y21
AA15	VDD_CORE	CORE_GND	AA14
AA19	VDD_CORE	CORE_GND	AA18
AA23	VDD_CORE	CORE_GND	AA22
AB17	VDD_CORE	CORE_GND	AB16
AB21	VDD_CORE	CORE_GND	AB20
AC14	VDD_CORE	CORE_GND	AC15
AC18	VDD_CORE	CORE_GND	AC19
AC22	VDD_CORE	CORE_GND	AC23

C1900 C1901 C1902 C1903 C1904
C1905 C1906 C1907 C1908 C1909
C1910 C1911 C1912 C1913 C1914
C1915 C1916 C1917 C1918 C1919
C1920 C1921 C1922 C1923 C1924

1UF 10% 6.3V CERM 402

KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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DRAWING

SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

119 92 PCI_RESET_L — MAKE_BASE=TRUE
- =PCI_AIRPORT_RESET_L 121
- =PCI_ROM_RESET_L 125
- =PCI_USB2_RESET_L 122

24 NB_SLOT_RESET_L — MAKE_BASE=TRUE — =GPU_RESET_L 84

SHASTA JTAG

24 9 JTAG_SB_TRST_L

THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS

9 TP_JTAG_SB_TCK — MAKE_BASE=TRUE — JTAG_SB_TCK 24
9 TP_JTAG_SB_TDI — MAKE_BASE=TRUE — JTAG_SB_TDI 24
9 TP_JTAG_SB_TDO — MAKE_BASE=TRUE — JTAG_SB_TDO 24
9 TP_JTAG_SB_TMS — MAKE_BASE=TRUE — JTAG_SB_TMS 24

R2053 4.7K 5% 1/16W MF-LF 402

SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)

119 56 24 23 7 =PP3V3_PWRON_SB

24 RAI_EXP_INTR_L<3> — R2061 10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<2> — R2062 10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<1> — R2063 10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<0> — R2064 10K 5% 1/16W MF-LF 402

NB_OVERTEMP

30 28 7 =PP3V3_RUN_SMU

R2082 200 5% 1/16W MF-LF 402
C2080 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.38MM
TSENSE_NB_VCC

U2080 MAX6690MEE
STBY, VCC, ALERT, SMBDATA, SMBCLK, ADD0, ADD1, DXP (SYM_VER2), DXN, QSOP, NC_1, NC_5, NC_9, NC_13, NC_16, GND

39 I2C_NB_TEMP_SDA
39 I2C_NB_TEMP_SCL

20 NB_THERM_A
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB
NET_PHYSICAL_TYPE=10MIL_WIDTH
NET_SPACING_TYPE=TSENSE_DIFPAIR

C2081 0.0022UF 10% 50V CERM 402 PLACE BY IC

20 NB_THERM_K
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB

NET_SPACING_TYPE=TSENSE_DIFPAIR
NET_PHYSICAL_TYPE=10MIL_WIDTH

TSENSE_NB_OVERTEMP_L
TSENSE_NB_ADD0
TSENSE_NB_ADD1

R2083 1K 5% 1/16W MF-LF 402
NOSTUFF R2084 1K 5% 1/16W MF-LF 402
NOSTUFF R2086 1K 5% 1/16W MF-LF 402
R2085 1K 5% 1/16W MF-LF 402

NOSTUFF R2087 0 5% 1/16W MF-LF 402
SYS_OVERTEMP_L 24 28 93

NEED TO CHECK ALL I2C ADDRESSES

A0	A1	ADDR
0	0	30/31
0	hiZ	32/33
0	1	34/35
hiZ	0	52/53
hiZ	hiZ	54/55
hiZ	1	56/57
1	0	9A/9B
1	hiZ	9A/9B
1	1	9C/9D

=PP1V8_PWRON_NBMEM 7 39 58 59

C2055 1UF 10% 6.3V CERM 402

C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP

KODIAK ALIASES

6 NC_PMR_CLK_DIS_L — MAKE_BASE=TRUE — PMR_CLK_DIS_L 20

KODIAK JTAG_TRST PULLED HIGH TO ALLOW SMU DEBUG ACCESS

=PP2V5_PWRON_NB_MISC 7 20 28 30 39

R2073 4.7K 5% 1/16W MF-LF 402
NOSTUFF R2074 0 5% 1/16W MF-LF 402
NOSTUFF R2054 4.7K 5% 1/16W MF-LF 402

20 9 JTAG_NB_TRST_L — NB_PU_RST_L 20 30

U1900 KODIAK-ASIC-040812 BGA (10 OF 10) — POWER/TEST/MISC

30 9 JTAG_NB_TCK	AJ04	CE1_LT_TCK	
30 9 JTAG_NB_TDI	AG07	CE1_MC_TDI	
30 9 JTAG_NB_TDO	AG05	CE1_B_TDO	
30 9 JTAG_NB_TMS	AL02	CE1_DI1_TMS	
20 9 JTAG_NB_TRST_L	AK06	CE1_DI2_TRST	
	AG08	CE0_TEST	
20 NB_THERM_A	F15	SYS_THDIO_D	
20 NB_THERM_K	G15	SYS_THDIO_G	
39 30 28 20 7 =PP2V5_PWRON_NB_MISC	AF02	VD5_0	
	AF05	VD5_1	
	AH01	VD5_2	
	AL01	NORTH_BRIDGE_RESET_L	NB_PU_RST_L 20 30
	AG01	HRESET_L	NB_HRST_L
	AJ03	SUSPENDACK_L	NB_SUSPEND_ACK_L 30 62
	AJ01	SUSPENDREQ_L	NB_SUSPEND_REQ_L 30
	AG04	SYS_ISCA0	I2C_NB_B_SDA 39
	AK03	SYS_ISCL0	I2C_NB_B_SCL 39
	AH06	SYS_ISCA1	I2C_NB_C_SDA 39
	AJ05	SYS_ISCL1	I2C_NB_C_SCL 39
	AG03	API_ISCA	I2C_NB_A_SDA 39
	AH03	API_ISCL	I2C_NB_A_SCL 39
	AE09	PMR_CLK_P	NB_PMR_CLK_P 26 27
	AE10	PMR_CLK_N	NB_PMR_CLK_N 26 27
	AG02	PMR_CLK_STOP_L	

39 30 28 20 7 =PP2V5_PWRON_NB_MISC

P4MM SM TP2002

R2003 1K 1% 1/16W MF-LF 402

C2050 1UF 10% 6.3V CERM 402
C2051 1UF 10% 6.3V CERM 402
C2052 1UF 10% 6.3V CERM 402

R2000 0 5% 1/16W MF-LF 402

NOSTUFF R2001 60.4 1% 1/16W MF-LF 402
NOSTUFF R2002 60.4 1% 1/16W MF-LF 402
TERM_RC

NOSTUFF C2053 1.5PF +/-0.25PF 50V CERM 402

PLACE TERM R/C CLOSE TO KODIAK

P4MM SM TP2000
1 6 PP_2V5PWRONNBMISC
XW2000

R2013 10K 5% 1/16W MF-LF 402

NOSTUFF R2012 0 5% 1/16W MF-LF 402
20 PMR_CLK_DIS_L
NB_PMR_CLK_STOP_L

NOTE: LOW = DISABLE PMR_CLK

NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07

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<XR_PAGE_TITLE>

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

3B2 =PP1V2_PWRON_SB_VCORE

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314
0.1uF 20% 10V CERM 402

149A3 120C4 119A3 29C7 29B4 24D2 24C3 24B7 24A6 20D2 3A3 =PP3V3_PWRON_SB 154D2

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339
0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.1
BGA-LP
(1 OF 8)

POWER
SEE_TABLE

VDDC
VDDO33
VDDO25
VIO1
VIO2
VDDP_KL
GND

Shasta max (est 06/30/03) current:

DIGITAL	1.2V	950 mA (1175 mW)
ANALOG12	1.2V	600 mA (760 mW)
VDDPs	2.5V	100 mA (250 mW)
I/O 2.5	2.5V	20 mA (60 mW)
I/O 3.3	3.3V	220 mA (770 mW)
Total:		3015 mW

XW2300 PP_1V2PWRONSBVCORE PP2300
XW2303 PP_3V3PWRONSBPCI64 PP2303
XW2304 NO_TEST=YES PP_2V5PWRONSB PP2304
P4MM SM

=PP2V5_PWRON_SB 3C1 23B2 24D5 119C3 138C6
C2350 C2351 0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB_PCI64 3A2
C2355 C2356 C2357 0.1uF 20% 10V CERM 402
For PCI_AD<63..32>

=PP3V3_PWRON_SB_PCI32 3A2
C2360 C2361 C2362 0.1uF 20% 10V CERM 402
For PCI_AD<31..0>

=PP2V5_PWRON_SB 3C1 23C2 24D5 119C3 138C6
C2365 0.1uF 20% 10V CERM 402

Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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LAST_MODIFIED=Thu May 19 14:26:40 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI 24 147
I2S0_SB_TO_DEV_DTO 24 147
I2S0_MCLK 24 154
I2S0_BITCLK 24 147
I2S0_SYNC 24 147

I2S1_DEV_TO_SB_DTI 8 24
I2S1_SB_TO_DEV_DTO 8 24
I2S1_MCLK 8 24
I2S1_BITCLK 8 24
I2S1_SYNC 8 24

I2S2_DEV_TO_SB_DTI 24 154
I2S2_SB_TO_DEV_DTO 24 154
I2S2_MCLK 24 154
I2S2_BITCLK 24 154
I2S2_SYNC 24 154

SB_CLK18M_XTALI 24
SB_CLK18M_XTALO 24
SB_CLK18M_XTALO_R 24
SB_CLK25M_SATA 24 26
NB_TO_SB_INT 24
SB_CPU_A0_INT_L 24
SB_CPU_A1_INT_L 24
SB_CPU_B0_INT_L 24
SB_CPU_B1_INT_L 24
PCI_AIRPORT_INT_L 24 121
PCI_USB2_INT_L 24 122
I2S0_RESET_L 24 147
I2S1_RESET_L 8 24
I2S2_RESET_L 24 154
MB_SLOT_RESET_L 24
NB_SLOT_RESET_L 20 24
SB_CPU_A0_SRESET_L 24 56
SB_CPU_A1_SRESET_L 24 56
SB_CPU_B0_SRESET_L 24 56
SB_CPU_B1_SRESET_L 24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

=PP3V3_RUN_SB_PCI 7 24

R2476 10K 5% 1/16W MF-LF 402 — To SouthBridge -> NB_TO_SB_INT 24

MPIC_SB
NB_CPU_A0_INT_L (42) FROM NORTHBRIDGE — R2475 10K 5% 1/16W MF-LF 402 — NB_INT_L_R
R2479 MPIC_NB 0 5% 1/16W MF-LF 402 2
CPU_A0_INT_R_L (56) TO CPU — R2478 0 5% 1/16W MF-LF 402 — MPIC_SB SB_CPU_A0_INT_L 24 — FROM SOUTHBRIDGE
Q2476 2N3904LF SOT23

NorthBridge / SouthBridge MPIC Routing

=PP2V5_PWRON_SB 7 23 119 138

R2405 3.3 5% 1/8W MF-LF 805 — PP2V5_PWRON_SB_XTAL18VDD (VOLTAGE=2.5V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — C2400 10UF 10% 6.3V X5R 805; C2401 1uF 10% 6.3V CERM 402

R2410 3.3 5% 1/8W MF-LF 805 — PP2V5_PWRON_SB_XTALVDD (VOLTAGE=2.5V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — C2410 10UF 10% 6.3V X5R 805; C2411 1uF 10% 6.3V CERM 402

Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

I2S0_DEV_TO_SB_DTI	RP2410 3	6	33	I2S0_SB_TO_DEV_DTO_R	W7	I2S0DTI_H
I2S0_SB_TO_DEV_DTO	RP2410 4	5	33	I2S0_MCLK_R	Y9	I2S0DTO_H
I2S0_MCLK	RP2420 1	8	33	I2S0_BITCLK_R	U8	I2S0MCLK_H
I2S0_BITCLK	RP2410 2	7	33	I2S0_SYNC_R	AA4	I2S0BITCLK_H
I2S0_SYNC					Y6	I2S0SYNC_H
I2S1_DEV_TO_SB_DTI					V10	I2S1DTI_H
I2S1_SB_TO_DEV_DTO	RP2420 3	6	33	I2S1_SB_TO_DEV_DTO_R	AB5	I2S1DTO_H
I2S1_MCLK	RP2430 2	7	33	I2S1_MCLK_R	V9	I2S1MCLK_H
I2S1_BITCLK	RP2430 3	6	33	I2S1_BITCLK_R	AA8	I2S1BITCLK_H
I2S1_SYNC	RP2410 1	8	33	I2S1_SYNC_R	AA7	I2S1SYNC_H
I2S1_RESET_L					V5	GPIO_H_0
I2S2_DEV_TO_SB_DTI					AA5	I2S2DTI_H
I2S2_SB_TO_DEV_DTO	RP2430 4	5	33	I2S2_SB_TO_DEV_DTO_R	Y8	I2S2DTO_H
I2S2_MCLK	RP2420 4	5	33	I2S2_MCLK_R	Y7	I2S2MCLK_H
I2S2_BITCLK	RP2420 2	7	33	I2S2_BITCLK_R	AB4	I2S2BITCLK_H
I2S2_SYNC	RP2430 1	8	33	I2S2_SYNC_R	W9	I2S2SYNC_H
I2S2_RESET_L					Y2	GPIO_H_1

AUDIO GPIO - see note on right

119 56 24 23 20 7 =PP3V3_PWRON_SB

R2400 10K 5% 1/16W MF-LF 402 2

SB_PCI_SEL32BIT — GPIO_H_2 (147 24 I2S0_RESET_L, AB3); GPIO_H_3 (24 SB_GPIO_H_3, W8); PCI_SEL32BIT_H (W6)

I2C_SB_SCL (39) — I2CCLK_H (Y9)
I2C_SB_SDA (39) — I2CDATA_H (AB7)

R2402 0 5% 1/16W MF-LF 402 — SYS_TO_RESET_L (122 119 30 28) — SHASTA_SYS_IO_RESET_L (E9) — RESET_L

PLACE R2402 CLOSE TO SHASTA

SB_STOPXTALS_L (28)	W10	STOPXTALS_L
SMU_SUSPENDREQ_L (43 30 28)	U11	SUSPENDREQ_L
SB_SUSPENDACK_L (28)	V11	SUSPENDACK_L
SYS_PME_L (122 28)	W18	PCI1PME_L
TP_SB_WATCHDOG (9)	V12	INTRWD_H
JTAG_SB_TDI (20)	AA11	TDI
JTAG_SB_TDO (20)	W11	TDO
JTAG_SB_TCK (20)	AB11	TCK
JTAG_SB_TMS (20)	Y11	TMS
JTAG_SB_TRST_L (20 9)	W12	TRST_L
SB_TEST_MODE_PD	A3	TEST_MODE_H
TP_SB_PLLTEST (6)	U14	PLLTEST
TP_SB_FSTEST (6)	V14	FSTEST
SB_CLK18M_XTALI (24)	W13	XTAL_18_I
SB_CLK18M_XTALO_R (24)	V13	XTAL_18_O
SB_CLK25M_SATA (26 24)	U15	XTALI
	V15 (NC)	XTALO

XTAL VDD (W14) · XTAL_18 VDD (Y13) · PLL_45 VDD (AA13) · PLL_49 VDD (Y12) · VIO PME (W17)

U2300 SHASTA V1.1 BGA-LF (2 OF 8)

I2S0 · I2S1 (GGCA) · I2S2 (GGCB) · GPIO · I2C · PCI · PWR_MGT · TEST · XTALS · XGI

PCI1REQ_3_L	U17	NB_CHP_FLT_N_B	24
PCI1GNT_3_L	AA19	SB_SFC_RESET_L	24
PCI1REQ_4_L	AB21	SB_CPU_VDNAP1	24 28
PCI1GNT_4_L	AA20	SB_CPU_VDNAP2	24 28
PCI1REQ_5_L	U16	SB_TO_SMU_INT_L	24 28
PCI1GNT_5_L	Y20	LOGIC_BRD_GOOD	24
PCI1AD_32_H	D18	SB_VDNAP0	24 31
PCI1AD_33_H	A20	SYS_OVERTEMP_L	20 24 28 93
PCI1AD_34_H	F18	SB_GPIO14	24 143
PCI1AD_35_H	F17	MB_SLOT_RESET_L	24
PCI1AD_36_H	G16	NB_SLOT_RESET_L_R	24
PCI1AD_37_H	F16	PCI_AIRPORT_INT_L	24 121
PCI1AD_38_H	A21	PCIX_INT_L	24
PCI1AD_39_H	B21	RAI_EXP_INTR_L<3>	20
PCI1AD_40_H	C20	RAI_EXP_INTR_L<2>	20
PCI1AD_41_H	G17	RAI_EXP_INTR_L<1>	20
PCI1AD_42_H	G18	RAI_EXP_INTR_L<0>	20
PCI1AD_43_H	E19	GIGE_P1_INTA_L	24
PCI1AD_44_H	F19	GIGE_P2_INTB_L	24
PCI1AD_45_H	D20	RAI_ALERT_L	24
PCI1AD_46_H	E20	RAI_FATAL_L	24
PCI1AD_47_H	C21	PCI_USB2_INT_L	24 122
PCI1AD_48_H	F20	FW_LOWPWR_R	24
PCI1AD_49_H	G19	ENETFW_RESET	17 24
PCI1AD_50_H	C22	MAKE_TBEN_SYNC_L	24
PCI1AD_51_H	D21	ENET_ENERGYDET	24 132
PCI1AD_52_H	G20	AUDIO_LO_DET_L	153
PCI1AD_53_H	D22	AUDIO_LO_OPTICAL_PLUG_L	153
PCI1AD_54_H	K18	AUDIO_LI_DET_L	153
PCI1AD_55_H	H19	AUDIO_LI_OPTICAL_PLUG_L	154
PCI1AD_56_H	J17	AUDIO_HP_DET_L	154
PCI1AD_57_H	F21	AUDIO_MIC_ID	154
PCI1AD_58_H	G21	AUDIO_LO_MUTE_L	150
PCI1AD_59_H	H20	AUDIO_HP_MUTE_L	154
PCI1AD_60_H	J19	AUDIO_SPKR_MUTE_L	152
PCI1AD_61_H	F22	AUDIO_EXT_MCLK_SEL	154
PCI1AD_62_H	G22	AUDIO_SPDIFIN_INT_L	154
PCI1AD_63_H	H21	AUDIO_SPKR_ID	153
PCI1C_BE_4_L	J20	SB_CPU_A0_INT_L	24
PCI1C_BE_5_L	H22	SB_CPU_A1_INT_L	24
PCI1C_BE_6_L	K22	SB_CPU_B0_INT_L	24
PCI1C_BE_7_L	K20	SB_CPU_B1_INT_L	24
PCI1REQ64_L	K17	SYS_SLEWING_L	24 26 28 50
PCI1ACK64_L	L17	SB_CPU_A0_SRESET_L	24 56
PCI1PAR64_H	E18	SB_CPU_A1_SRESET_L	24 56
XGI_CLK_H	Y4	SB_CPU_B0_SRESET_L	24 56
XGI_DTO0_H	U7	SB_CPU_B1_SRESET_L	24 56
XGI_DTO1_H	T9	NB_TO_SB_INT	24
XGI_DTI_H	W2	SMU_TO_SB_INT_L	24

XTAL_18 GND (AB12) · PLL_45 GND (AB13) · PLL_49 GND (AA12)

AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

XW2400 — PP_1V2PWRONSBPLL45VDD — P4MM SM — PP2400

PP1V2_PWRON_SB_PLL45VDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
C2421 1uF 10% 6.3V CERM 402; C2420 10UF 10% 6.3V X5R 805
R2420 3.3 5% 1/8W MF-LF 805 — =PP1V2_PWRON_SB 7

PP1V2_PWRON_SB_PLL49VDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
C2431 1uF 10% 6.3V CERM 402; C2430 10UF 10% 6.3V X5R 805
R2430 3.3 5% 1/8W MF-LF 805

=PP3V3_PWRON_SB 7 20 23 24 56 119
C2440 0.1uF 20% 6.3V CERM 402

NET_SPACING_TYPE=P3MM SPACING — P4MM SM — PP2405

R2432 0 5% 1/16W MF-LF 402 — NB_SLOT_RESET_L 20 24

PLACE R2432 CLOSE TO SHASTA

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

119 56 24 23 20 7 =PP3V3_PWRON_SB

SB_CPU_A0_INT_L (24)	R2408	10K	MPIC_NB
SB_CPU_A1_INT_L (24)	R2409	10K	MPIC_NB
SB_CPU_B0_INT_L (24)	R2412	10K	MPIC_NB
SB_CPU_B1_INT_L (24)	R2418	10K	MPIC_NB

5% 1/16W MF-LF 402

R2480 4.7K 1% 1/16W MF-LF 402 2

R2490 200 1% 1/16W MF-LF 402 2 — PP2406 — P4MM SM 1

CRITICAL Y2490 18.432M SM — SB_CLK18M_XTALO 24

C2490 22pF 5% 50V CERM 402; C2491 22pF 5% 50V CERM 402

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

24 7 =PP3V3_RUN_SB_PCI

R2456	10K	PCI_AIRPORT_INT_L	24 121
R2459	10K	PCI_USB2_INT_L	24 122
	SAT_RUN		
R2416	1K	SYS_OVERTEMP_L	20 24 28 93
NOSTUFF R2417	10K	MAKE_TBEN_SYNC_L	24

5% 1/16W MF-LF 402 (1% 1/16W MF-LF 402 for R2416)

119 56 24 23 20 7 =PP3V3_PWRON_SB

SB_GPIO_H_3	R2463	10K	
NB_CHP_FLT_N_B	R2450	10K	
SB_SFC_RESET_L	R2451	10K	
SB_CPU_VDNAP1	R2452	10K	
SB_CPU_VDNAP2	R2453	10K	
SB_TO_SMU_INT_L	R2454	10K	
LOGIC_BRD_GOOD	R2455	10K	
SB_VDNAP0	R2404	10K	
SAT_PWRON SYS_OVERTEMP_L (93 28 24 20)	R2460	1K	
SB_GPIO14 (143 24)	R2422	10K	
MB_SLOT_RESET_L (24)	R2461	4.7K	
NB_SLOT_RESET_L (24 20)	NOSTUFF R2406	4.7K	
PCIX_INT_L (24)	R2419	10K	
GIGE_P1_INTA_L (24)	R2457	10K	
GIGE_P2_INTB_L (24)	R2413	10K	
RAI_ALERT_L (24)	R2414	10K	
RAI_FATAL_L (24)	R2465	10K	
SYS_SLEWING_L (50 28 26 24)	NOSTUFF R2462	1K	
SMU_TO_SB_INT_L (24)	R2421	10K	
MAKE_TBEN_SYNC_L (24)	R2415	10K	

5% 1/16W MF-LF 402 (1% 1/16W MF-LF 402 for R2462)

R2407 0 NO STUFF 5% 1/16W MF-LF 402 — FW_LOWPWR 139

FW_LOWPWR_R (24)	R2466	10K	
ENETFW_RESET (24 17)	R2467	10K	
ENET_ENERGYDET (132 24)	R2468	10K	

5% 1/16W MF-LF 402

Shasta Serial / Misc

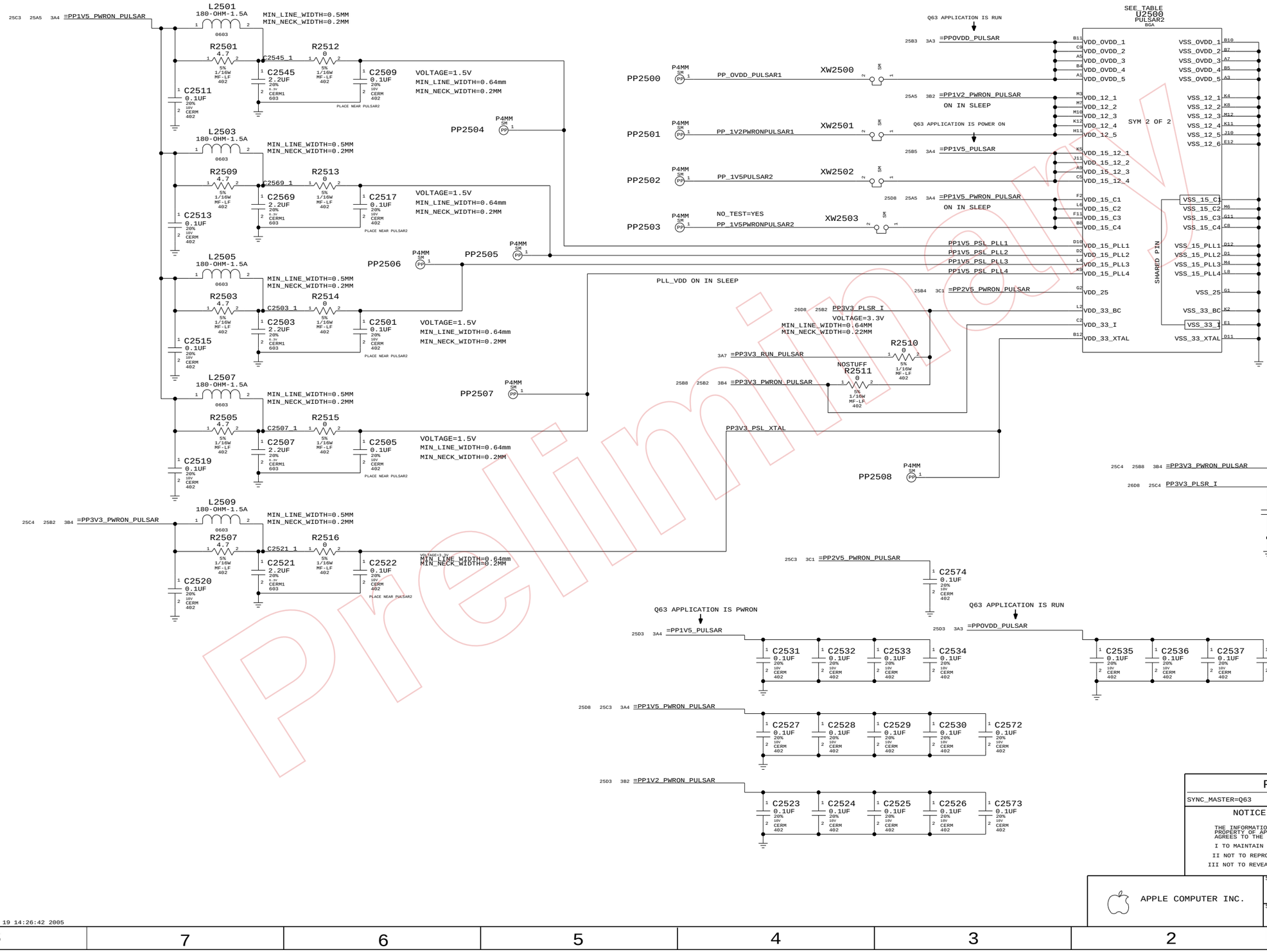
SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT: 24 OF: 154	

LAST_MODIFIED=Thu May 19 14:26:41 2005

DRAWING



PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	25	154

LAST_MODIFIED=Thu May 19 14:26:42 2005

DRAWING

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR

P4MM SM PP2602

R2612 0 5% 402 — 28 CLOCK_RESET_L — PLS2_RESET_L

U2500 PULSAR2 BGA SYM 1 OF 2

PLS2_RESET_L → C3 RESET*
PLSR2_ASEL_INT_L → D3 ASEL_INT*
39 I2C_CLOCK_B_SCL → B4 SCLK
39 I2C_CLOCK_B_SDA → B2 SDATA
PLSR2_PD → C4 PD
PLSR2_TM → E3 TEST_MODE
PLSR2_OEMODE → E2 OEMODE

25 PP3V3_PLSR_I

R2613 10K 5% 1/16W MF-LF 402
NOSTUFF R2614 10K 5% 1/16W MF-LF 402
R2616 10K 5% 1/16W MF-LF 402
R2623 0 5% 1/16W MF-LF 402
NOSTUFF R2618 1K 1% 1/16W MF-LF 402
NOSTUFF R2621 1K 1% 1/16W MF-LF 402

P4MM SM PP2601
P4MM SM PP2600

PLS2_X_IN → C12 XIN
PLS2_X_OUT → C11 XOUT
PLS2_REF15 → H10 REF_15
PLS2_REF25 → F1 REF_25
PLS2_REF33 → L1 REF_33

R2625 1K 1% 1/16W MF-LF 402
R2626 1K 1% 1/16W MF-LF 402
R2627 1K 1% 1/16W MF-LF 402

R2600 0 5% 402 — 54 30 16 15 13 12 11 SYS_SLEEP

NOSTUFF J2600 U.FL-R_SMT F-ST-SM

PLS2_EXTCLK → NOSTUFF R2662 24 5% 1/16W MF-LF 402 → PLS2_INTERM
NOSTUFF R2664 24 5% 1/16W MF-LF 402

NO STUFF R2652 0 5% 1/16W MF-LF 402
R2654 0 5% 1/16W MF-LF 402
NO STUFF R2658 330K 5% 1/16W MF-LF 402
R2656 0 5% 1/16W MF-LF 402

CRITICAL Y2601 25.0000M SM-2

PLS2_X_IN_B
PLS2_X_OUT_B

C2607 33PF 5% 50V CERM 402
C2605 33PF 5% 50V CERM 402

R2628 0 5% 1/16W MF-LF 402 — PULLED UP TO PP3V3_RUN ON P.28 — SYS_SLEWING_L_R → SYS_SLEWING_L — 24 28 50

SLEWING* A12

HCLKP_0	A6	200MHZ, 1.5VDVDD	
HCLKN_0	B6	200MHZ, 1.5VDVDD	
HCLKP_1	C4	200MHZ, 1.5VDVDD	
HCLKN_1	A4	200MHZ, 1.5VDVDD	
HCLKP_2	B3	200MHZ, 1.5VDVDD	
HCLKN_2	A2	200MHZ, 1.5VDVDD	
HTBEN_0	A11	66MHZ, 1.5VDVDD	9 CPU_A_TBEN_CLK_R
HTBEN_1	A10	66MHZ, 1.5VDVDD	9 CPU_B_TBEN_CLK_R
HSYNC_0	A8	1.5VDVDD	9 CPU_A_APSYNC_R
HSYNC_1	B9	1.5VDVDD	9 CPU_B_APSYNC_R
HSYNC_2	C10	1.5VDVDD	9 NB_APSYNC_R
GPCLK12_C0	H12	66MHZ, 1.2V (100MHZ FOR ASPEN)	9 HT_SB_REFCLK_R
GPCLK12P_A0	K3	200MHZ, 1.2V	9 HT_NB_REFCLK_H0_R
GPCLK12N_A0	L3	200MHZ, 1.2V	9 HT_NB_REFCLK_L0_R
GPCLK12P_A1	M5	200MHZ, 1.2V	9 CLK_RAIREF_200M_P_R
GPCLK12N_A1	L5	200MHZ, 1.2V	9 CLK_RAIREF_200M_N_R
GPCLK12P_B0	L7	300MHZ, 1.2V	9 NB_PMR_CLK_P_R
GPCLK12N_B0	M8	300MHZ, 1.2V	9 NB_PMR_CLK_N_R
GPCLK12P_C0	M9	100MHZ, 1.2V	9 NB_PCIE_REFCLK_P_C
GPCLK12N_C0	L9	100MHZ, 1.2V	9 NB_PCIE_REFCLK_N_C
GPCLK12P_C1	L10	100MHZ, 1.2V	9 GFX_SLOT_PCIE_REFCLK_P_C
GPCLK12N_C1	M11	100MHZ, 1.2V	9 GFX_SLOT_PCIE_REFCLK_N_C
GPCLK12P_C2	L11	100MHZ, 1.2V	9 PCIE_A_REFCLKIN_P_C
GPCLK12N_C2	L12	100MHZ, 1.2V	9 PCIE_A_REFCLKIN_N_C
GPCLK12P_C3	K10	100MHZ, 1.2V	9 PCIE_B_REFCLKIN_P_C
GPCLK12N_C3	J12	100MHZ, 1.2V	9 PCIE_B_REFCLKIN_N_C
GPCLK12P_C4	G12	100MHZ, 1.2V	9 PCIE_C_REFCLKIN_P_C
GPCLK12N_C4	F12	100MHZ, 1.2V	9 PCIE_C_REFCLKIN_N_C
GPCLK12P_D0	E10	66MHZ, 1.2V	9 NB_DDR_REFCLK_P_R
GPCLK12N_D0	E11	66MHZ, 1.2V	9 NB_DDR_REFCLK_N_R
GPCLK25_E0	H1	25MHZ, 2.5V	9 CLK_RAI_GIGE_25MHZ_R
GPCLK25_E1	H3	25MHZ, 2.5V	9 QUA0_REF_25MHZ_R
GPCLK25_F0	H2	25MHZ, 2.5V	9 SB_CLK25M_SATA_R
GPCLK25_F1	J3	25MHZ, 2.5V	9 QUA1_REF_25MHZ_R
GPCLK33_E0	J1	66MHZ, 3.3V	6 PCI_CLK66M_SB_INT_R
GPCLK33_E1	J2	33MHZ, 3.3V	9 PCI_CLK33M_SB_EXT_R
GPCLK33_F0	K1	33MHZ, 3.3V	9 SB_AIRPRT_CLK_33MHZ_R
GPCLK33_F1	M1	66MHZ, 3.3V	9 CLK_RAI_REFCLK_66M_R
GPCLK33_F2	M2	33MHZ, 3.3V	9 SB_USB2_CLK_33MHZ_R

EI_CPU_A_SYSCLK_P 56
EI_CPU_A_SYSCLK_N 56
EI_CPU_B_SYSCLK_P 27
EI_CPU_B_SYSCLK_N 27
EI_NB_SYSCLK_P 42 56
EI_NB_SYSCLK_N 42 56

R2629 0 5% 1/16W MF-LF 402 — CPU_A_TBEN_CLK_US 56
R2630 0 5% 1/16W MF-LF 402 — NOSTUFF — NC_CPU_B_TBEN_CLK_US 6
R2631 0 5% 1/16W MF-LF 402 — CPU_A_APSYNC 56
R2632 0 5% 1/16W MF-LF 402 — CPU_B_APSYNC 27
R2633 0 5% 1/16W MF-LF 402 — NB_APSYNC 42 56
R2634 0 5% 1/16W MF-LF 402 — HT_CLK66M_SB 103
R2635 0 5% 1/16W MF-LF 402 — HT_NB_REFCLK_P<0> 98 101
R2636 0 5% 1/16W MF-LF 402 — HT_NB_REFCLK_N<0> 98 101
R2637 0 5% 1/16W MF-LF 402 — CLK_RAI_200M_P<0> 27
R2639 0 5% 1/16W MF-LF 402 — CLK_RAI_200M_N<0> 27
R2641 0 5% 1/16W MF-LF 402 — NB_PMR_CLK_P 20 27
R2643 0 5% 1/16W MF-LF 402 — NB_PMR_CLK_N 20 27
R2666 0 5% 1/16W MF-LF 402 — CLK_KOD_100M_P<0> 82 97
R2667 0 5% 1/16W MF-LF 402 — CLK_KOD_100M_N<0> 82 97
R2674 0 5% 1/16W MF-LF 402 — CLK_PCIE_SLOTA_P<0> 84 97
R2675 0 5% 1/16W MF-LF 402 — CLK_PCIE_SLOTA_N<0> 84 97
R2668 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEA_P<0> 27
R2669 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEA_N<0> 27
R2670 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEB_P<0> 27
R2671 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEB_N<0> 27
R2672 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEC_P<0> 27
R2673 0 5% 1/16W MF-LF 402 — CLK_RAI_PCIEC_N<0> 27
R2645 0 5% 1/16W MF-LF 402 — NB_DDR_REFCLK_P 59
R2647 0 5% 1/16W MF-LF 402 — NB_DDR_REFCLK_N 59
R2649 0 5% 1/16W MF-LF 402 — CLK_RAI_GIGE_25MHZ 27
R2651 0 5% 1/16W MF-LF 402 — RAM_ARB0_REF25MHZ 27
R2653 0 5% 1/16W MF-LF 402 — SB_CLK25M_SATA 24
R2655 0 5% 1/16W MF-LF 402 — RAM_ARB1_REF25MHZ 27
R2657 0 5% 1/16W MF-LF 402 — PCI_CLK66M_SB_INT 27 119
PCI_CLK33M_SB_EXT_RR 27 119
R2659 0 5% 402 MF-LF 1/16W — NOSTUFF R2601 49.9 1% 1/16W MF-LF 402 — PLACE R2602 BESIDE R2659 — CPU_TBEN_CLK 27
R2660 0 5% 1/16W MF-LF 402 — PCI_CLK33M_AIRPORT 121
R2663 0 5% 1/16W MF-LF 402 — CLK_RAI_REFCLK_66M 27
MB_PCIX_REFCLK
R2665 0 5% 1/16W MF-LF 402 — PCI_CLK33M_USB2 27

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 26 OF 154	

LAST_MODIFIED=Thu May 19 14:26:43 2005

DRAWING
TITLE=K2LOWMA
ABORDU=SHAWING

N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M — CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_GIGE_25MHZ — CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_P<0> — CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_N<0> — CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_P<0> — CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_N<0> — CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_P<0> — CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_N<0> — CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_P<0> — CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_N<0> — CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

9 NC_CPU_TBEN_CLK — CPU_TBEN_CLK 26
MAKE_BASE=TRUE

CPU_TBEN_CLK IS FOR Q63 ONLY
IT IS THE INPUT TO THE AND GATE WHICH
GENERATES CPUA AND CPUB TBEN_CLK

6 NC_EI_CPU_B_SYSCLK_P — EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

6 NC_EI_CPU_B_SYSCLK_N — EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

6 NC_CPU_B_APSYNC — CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ — RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

6 NC_RAM_ARB1_REF25MHZ — RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	167
25 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	168
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	169
26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB	170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

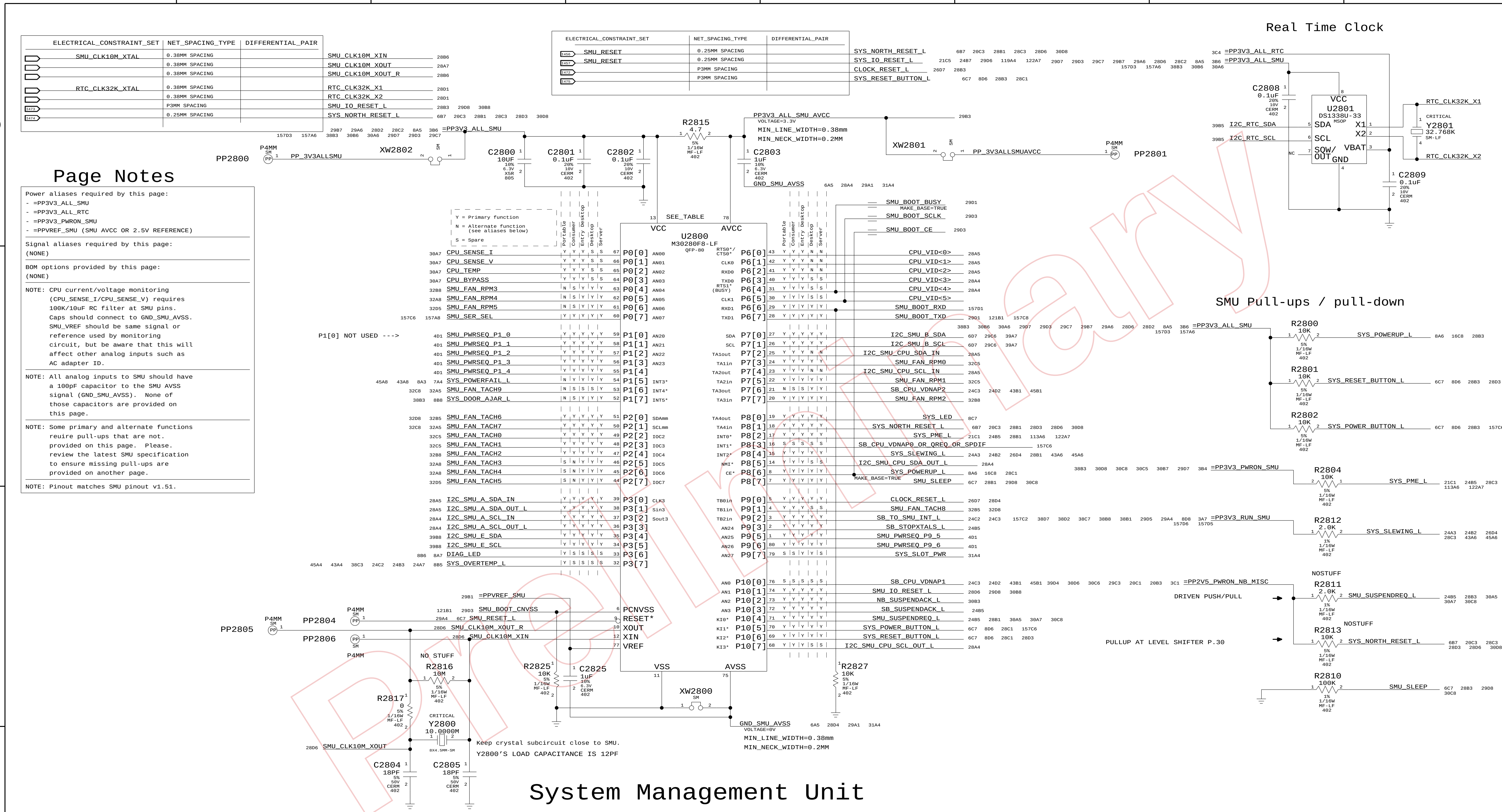
26 PCI_CLK33M_USB2 — =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 27 OF 154	



Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

System Management Unit

Alternate Functions

Tower & Server

		Port		
28C3	CPU_VID<0>	6.0	SAT_MRESET_L	29A5
28C3	CPU_VID<1>	6.1	CPU_A_INSERTED_L	30D4
28C3	CPU_VID<2>	6.2	CPU_B_INSERTED_L	30C3
28C3	I2C_SMU_CPU_SDA_IN	7.2	SMU_FAN_PWM8	32B5
28C3	I2C_SMU_CPU_SCL_IN	7.4	SMU_FAN_PWM9	32D8 32A5
28B6	I2C_SMU_A_SDA_IN	3.0	I2C_SMU_A_SDA	32C8 39D8
28B6	I2C_SMU_A_SDA_OUT_L	3.1	I2C_SMU_A_SCL	39D8

		Port		
28C3	CPU_VID<3>	6.3	SMU_FAN_RPM6	32B5
28C3	CPU_VID<4>	6.4	SMU_FAN_RPM7	32D8 32A5 32C8
28B6	I2C_SMU_A_SCL_IN	3.2	NB_TDI	29C3
28B6	I2C_SMU_A_SCL_OUT_L	3.3	NB_TCK	29C3 29C3
28B3	I2C_SMU_CPU_SDA_OUT_L	8.5	NB_TMS	6C7 20B3
28B3	I2C_SMU_CPU_SCL_OUT_L	10.7	NB_TDO_SMU	29D7

LAST_MODIFIED=Thu May 19 14:26:45 2005

System Management Unit

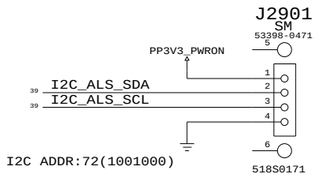
SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

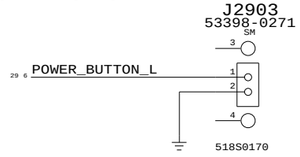
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	28	154

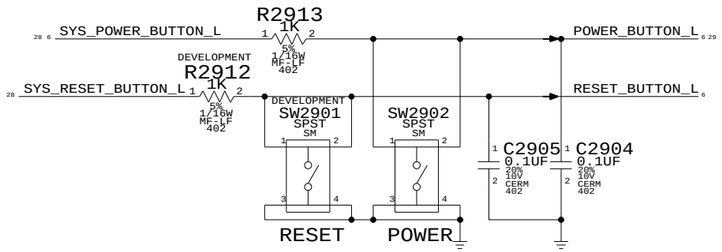
AMBIENT LIGHT SENSOR CONNECTOR



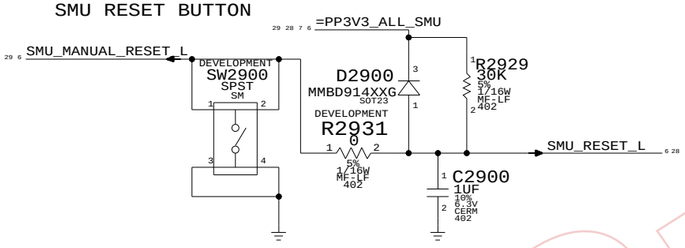
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

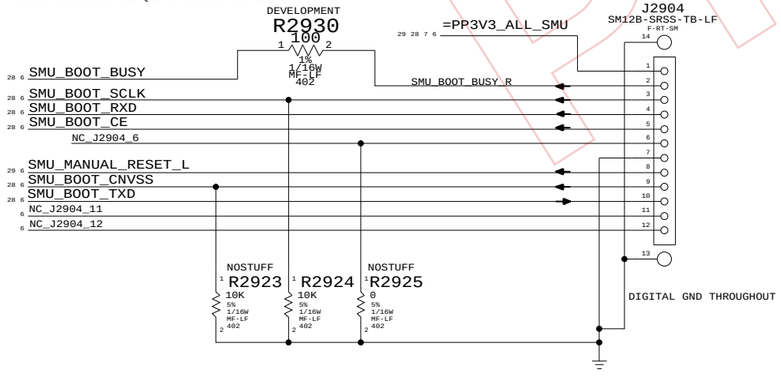


SMU RESET BUTTON

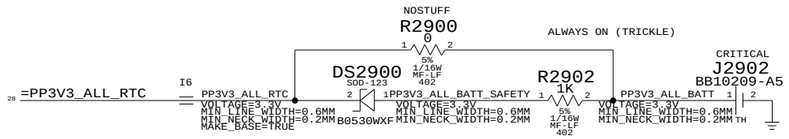


SMU DEBUG/DOWNLOAD CONNECTOR

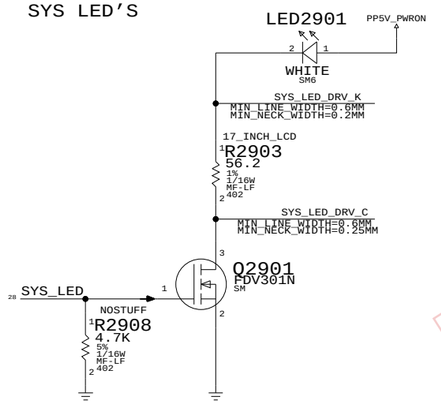
SAME CONNECTOR AS Q63 CPU CARD FOR SAT



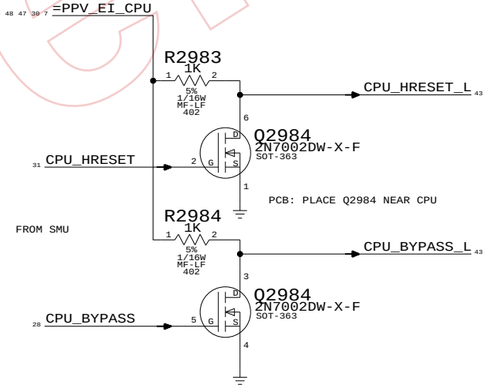
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 29 OF 154	

SMU TO NB SUSPEND_REQ

SAME AS Q63.

=PP3V3_PWRON_SMU

R3000 1K 5% 1/16W MF-LF 402

R3003 4.7K 5% 1/16W MF-LF 402

PMU_SUSPEND_REQ

=PP2V5_PWRON_NB_MISC

R3001 100 5% 1/16W MF-LF 402

NB_SUSPEND_REQ_L

SMU_SUSPENDREQ_L

Q3005 2N7002DW-X-F SOT-363

Q3000 2N7002DW-X-F SOT-363

NOSTUFF R3002 0 5% 1/16W MF-LF 402

SMU_SUSPENDREQ_L_R

NOSTUFF R3099 0 5% 1/16W MF-LF 402

=PP2V5_PWRON_NB_MISC

R3038 10K 5% 1/16W MF-LF 402

JTAG_NB_TDO

SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

=PP3V3_PWRON_SMU

R3006 10K 5% 1/16W MF-LF 402

R3010 4.7K 5% 1/16W MF-LF 402

NB_PU_RESET

SYS_NORTH_RESET_L

Q3005 2N7002DW-X-F SOT-363

=PP2V5_PWRON_NB_MISC

R3007 4.7K 5% 1/16W MF-LF 402

Q3000 2N7002DW-X-F SOT-363

NB_PU_RST_L

NOSTUFF R3008 0 5% 1/16W MF-LF 402

SYS_NORTH_RESET_L_R

NOSTUFF R3098 0 5% 1/16W MF-LF 402

NOSTUFF R3009 0 5% 1/16W MF-LF 402

SYS_SLEEP

SYS_2SLEEP_R

Q3006 2N7002 SOT23-LF

CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART

MISC. SMU BUFFERS

SAME AS (Q63).

=PP3V3_PWRON_SMU

R3021 4.7K 5% 1/16W MF-LF 402

U700 IS POWERED BY PP3V3_ALL

SMU_IO_RESET_L

U700 74LCX125 TSSOP

SYS_IO_RST_L_R

R3022 100 5% 1/16W MF-LF 402

SYS_IO_RESET_L

SMU_SLEEP

U700 74LCX125 TSSOP

SYS_SLEEP_R

R3023 100 5% 1/16W MF-LF 402

SYS_SLEEP

SMU JTAG TCK TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3081 1K 5% 1/16W MF-LF 402

=PP3V3_RUN_SMU

R3080 4.7K 5% 1/16W MF-LF 402

NOSTUFF R3082 33 5% 1/16W MF-LF 402

JTAG_CPU_TCK

Q3081 2N7002DW-X-F SOT-363

SMU_JTAG_TCK

Q3080 2N7002DW-X-F SOT-363

STUFF IF USING REGISTERED DIMM

=PP3V3_PWRON_SMU

R3040 1K 5% 1/16W MF-LF 402

SMU_IO_RESET

NOSTUFF Q3040 2N7002 SOT23-LF

SYS_IO_RST_L_R

SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)

=PPV_EI_CPU

C3030 0.1UF 20% 10V CERM 402

VCC RANGE 0.8V - 2.7V

U3030 SN74AUC2G34 SOT23-6

VIH = 1.0V, 3.3V TOLERANT

SMU_JTAG_TDI

R3030 33 5% 1/16W MF-LF 402

JTAG_CPU_TDI

CRITICAL

SHARE CPU AND NB JTAG TDO WITH SMU

=PP3V3_PWRON_SMU

SMU DRIVES 3.3V PUSH-PULL ON ALL JTAG-RELATED PINS

PCB: PLACE U3070 NEAR SMU

CRITICAL

U3070 SN74LVC2G157 TSSOP

=PP3V3_RUN_SMU

JTAG_CPU_TDO_3V3

JTAG_NB_TDO

SMU_CPU_NB_SEL

VIH=2V

SMU_JTAG_TDO

NC_JTAGMUX_3

C3070 0.1UF 20% 10V CERM 402

SMU JTAG TDI TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3084 1K 5% 1/16W MF-LF 402

NOSTUFF R3085 33 5% 1/16W MF-LF 402

JTAG_CPU_TDI

R3083 4.7K 5% 1/16W MF-LF 402

Q3081 2N7002DW-X-F SOT-363

SMU_JTAG_TDI_L

SMU_JTAG_TDI

Q3080 2N7002DW-X-F SOT-363

NB JTAG IS A DEVELOPMENT ONLY FEATURE

PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.

PCB: PLACE 33 OHM RES NEAR U3030/31 PART.

=PP2V5_PWRON_NB_MISC

DEVELOPMENT C3031 0.1UF 20% 10V CERM 402

VCC RANGE 0.8V - 2.7V

DEVELOPMENT U3031 SN74AUC2G34 SOT23-6

VIH = 2.0V, 3.3V TOLERANT

DEVELOPMENT R3032 33 5% 1/16W MF-LF 402

JTAG_NB_TDI

R3034 10K 5% 1/16W MF-LF 402

VIH = 2.0V, 3.3V TOLERANT

SHARE CPU AND NB JTAG TMS WITH SMU

=PP2V5_PWRON_NB_MISC

C3071 0.1UF 20% 10V CERM 402

PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.

CRITICAL

U3071 74LVC1G SC70-6

TO LEVEL SHIFTER

SMU_CPU_TMS

3.3V TOLERANT

STRAIGHT TO NB

JTAG_NB_TMS

SMU_JTAG_TMS

LEVEL SHIFT TDO FROM CPU TO MUX

=PP3V3_PWRON_SMU

R3051 1K 5% 1/16W MF-LF 402

R3052 100 5% 1/16W MF-LF 402

JTAG_CPU_TDO_L

JTAG_CPU_TDO_3V3

JTAG_CPU_TDO_R

R3050 10K 5% 1/16W MF-LF 402

Q3050 2N3904LF SOT23

Q3021 2N7002DW-X-F SOT-363

JTAG_CPU_TDO

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

PULLDOWNS TO BUFFERS/LOGIC GATES

R3036 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TDI

R3037 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TCK

R3070 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TMS

R3071 100K 5% 1/16W MF-LF 402 — SMU_CPU_NB_SEL

NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER

=PP3V3_PWRON_SMU

R3091 1K 5% 1/16W MF-LF 402

R3093 1K 5% 1/16W MF-LF 402

NB_SUSPEND_ACK_L_R

NB_SUSPENDACK

NB_SUSPENDACK_L

NB_SUSPEND_ACK_L

R3090 10K 5% 1/16W MF-LF 402

Q3090 2N3904LF SOT23

Q3021 2N7002DW-X-F SOT-363

NOSTUFF R3092 0 5% 1/16W MF-LF 402

LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)

=PPV_EI_CPU

=PP3V3_PWRON_SMU

R3026 1K 5% 1/16W MF-LF 402

R3027 1K 5% 1/16W MF-LF 402

JTAG_SMU_TMS_2_R

JTAG_CPU_TMS_2_L

JTAG_CPU_TMS_2_R

NOSTUFF R3028 33 5% 1/16W MF-LF 402

JTAG_CPU_TMS

SMU_CPU_TMS

R3020 10K 5% 1/16W MF-LF 402

Q3030 2N3904LF SOT23

Q3031 2N7002DW-X-F SOT-363

LEVEL SHIFT SMU TMS TO CPU (PRIMARY PLAN)

U5640 IS POWERED BY PPV_EI_CPU

CRITICAL

VIH = 1.0V

U5640 SN74AUC2G34 SOT23-6

SMU_CPU_TMS

R3039 33 5% 1/16W MF-LF 402

JTAG_CPU_TMS

DEMUX DRIVES PUSH-PULL 2.5V

PCB: PLACE U5640 AND R3039 NEAR CPU

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)

VCC RANGE 0.8V - 2.7V

U3030 SN74AUC2G34 SOT23-6

VIH = 1.0V, 3.3V TOLERANT

SMU_JTAG_TCK

R3031 33 5% 1/16W MF-LF 402

JTAG_CPU_TCK

SHARE CPU AND NB JTAG TCK WITH SMU

=PP2V5_PWRON_NB_MISC

PULLUP IF KODIAK JTAG IS NOSTUFFED

VCC RANGE 0.8V - 2.7V

DEVELOPMENT U3031 SN74AUC2G34 SOT23-6

VIH = 2.0V, 3.3V TOLERANT

DEVELOPMENT R3033 33 5% 1/16W MF-LF 402

JTAG_NB_TCK

R3035 10K 5% 1/16W MF-LF 402

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. 07
	SCALE NONE	SHT 30 OF 154	

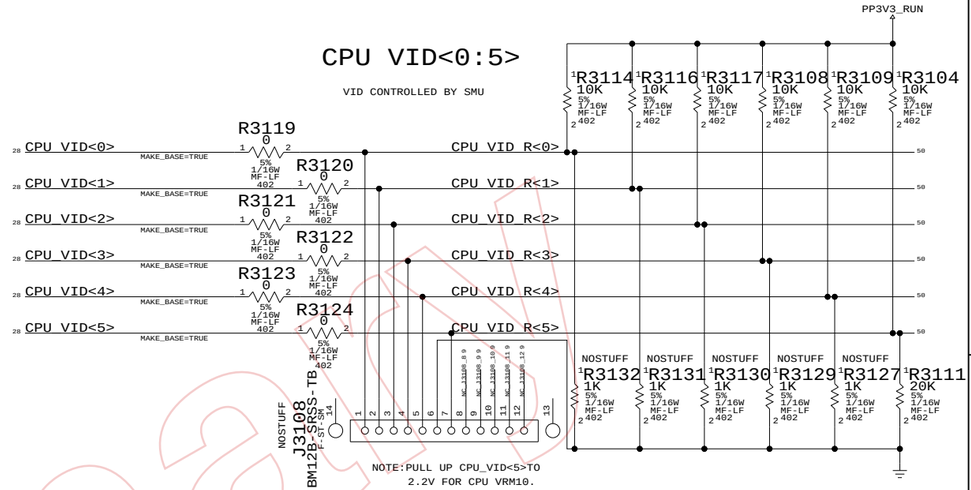
SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
		CPU_TEMP0	P0.2	
Q63 NC'S THESE AS IT USES A SAT.		CPU_BYPASS	P0.3	
	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3 28
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
		CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L 28
	30 SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN 28
	30 SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN — SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	30 SMU_CPU_NB_SEL	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING*	P8.4	
	30 SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
		PS9_5	P9.5	
		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR 28
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	30 SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L 28

CPU VID<0:5>

VID CONTROLLED BY SMU



SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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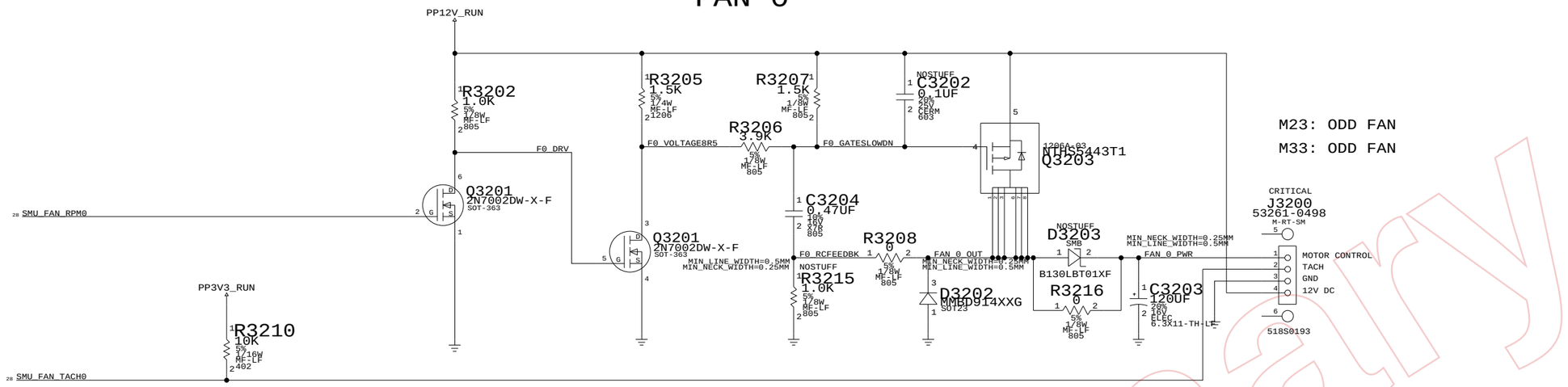
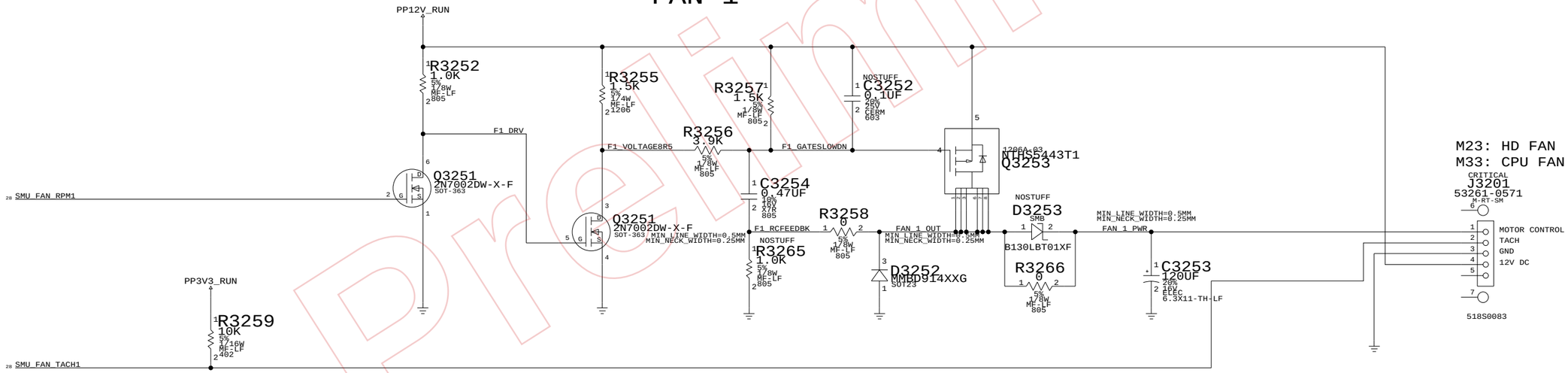
FAN 0



FAN 1



Fan 0, 1 & System Temp

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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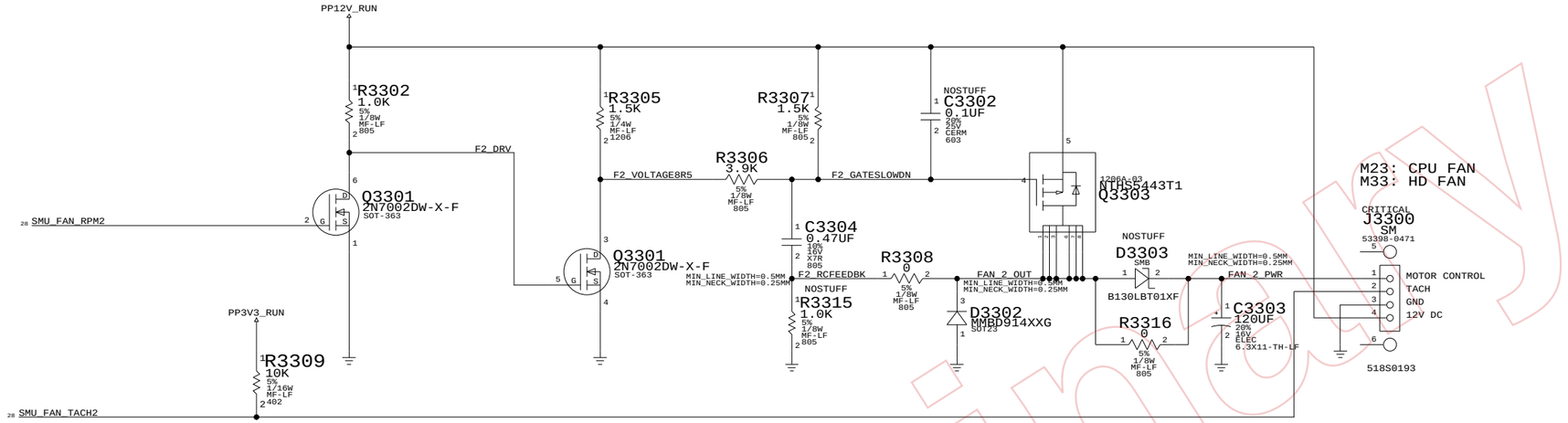
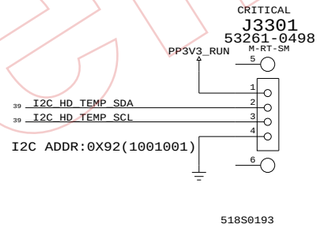
D	051-6863	07
SCALE: NONE	SHT 32 OF 154	

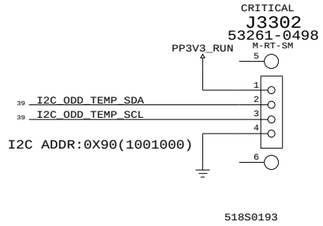
FAN 2



HD TEMP SENSOR



ODD TEMP SENSOR



Fan 2 & HD Temp

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 33 OF 154	

SMU AND NB I2C A BUS

SMU
MASTER
I2C_SMU_A_SDA — NET_SPACING_TYPE=I2C
I2C_SMU_A_SCL — NET_SPACING_TYPE=I2C

R3950 0 — I2C_NB_SMU_SDA — NET_SPACING_TYPE=I2C
R3951 0 — I2C_NB_SMU_SCL — NET_SPACING_TYPE=I2C

=PP3V3_RUN_I2C
R3953 2.0K
R3969 2.0K
VDIV=2.9V
NOSTUFF R3954 15K
NOSTUFF R3955 15K

NOSTUFF R3956 0 — I2C_NB_NB_SDA — NET_SPACING_TYPE=I2C
NOSTUFF R3957 0 — I2C_NB_NB_SCL — NET_SPACING_TYPE=I2C

=PP2V5_RUN_I2C
R3958 2.0K
R3959 2.0K

R3960 0 — I2C_NB_A_SDA — NET_SPACING_TYPE=I2C
R3961 0 — I2C_NB_A_SCL — NET_SPACING_TYPE=I2C

KODIAK
I2C_NB_A_SDA — NET_SPACING_TYPE=I2C
I2C_NB_A_SCL — NET_SPACING_TYPE=I2C

Q3902 SI2302ADSE3 SOT23-3 (D, G, S)
Q3902_1 — R3962 0 — =PP2V5_RUN_I2C

Q3901 SI2302ADSE3 SOT23-3 (D, G, S)
Q3901_1 — R3963 0

SB I2C BUS

SHASTA
MASTER
U2300
I2C_SB_SDA MAKE_BASE=TRUE
I2C_SB_SCL MAKE_BASE=TRUE
PINS Y9, AB7

PP3V3_RUN
R3915 1K
R3914 1K
NET_SPACING_TYPE=AUDIO
NET_SPACING_TYPE=AUDIO

AUDIO
U9500 / AU300
I2C_AUDIO_SDA
I2C_AUDIO_SCL
PINS 18, 19

SMU I2C B BUS

PP3V3_PWRON
R3903 2.0K
R3902 2.0K

SMU
MASTER
U1300
I2C_SMU_B_SDA MAKE_BASE=TRUE
I2C_SMU_B_SCL MAKE_BASE=TRUE
PINS 26, 27
NET_SPACING_TYPE=I2C
NET_SPACING_TYPE=I2C

PULSAR2
U2600
I2C_CLOCK_B_SDA
I2C_CLOCK_B_SCL NET_SPACING_TYPE=I2C
I2C ADDR:0XD5
R3904 33

ALS HEADER
J2901
I2C_ALS_SDA
I2C_ALS_SCL NET_SPACING_TYPE=I2C
I2C ADDR:52
R3908 33

SMU I2C E BUS

PP3V3_ALL
R3907 2.0K
R3906 2.0K
R3965 0
R3964 0

SMU 'E'
MASTER
U2800
I2C_SMU_E_SDA
I2C_SMU_E_SCL
PINS 34,35

RTC
U2801
I2C_RTC_SDA
I2C_RTC_SCL
PINS 5, 6

NB I2C C BUS

=PP2V5_RUN_I2C
R3970 2.0K
R3971 2.0K

KODIAK I2C C
I2C_NB_C_SDA NET_SPACING_TYPE=I2C
I2C_NB_C_SCL NET_SPACING_TYPE=I2C

=PP3V3_RUN_I2C
R3972 2.0K
R3973 2.0K

MAKE_BASE=TRUE I2C_NB_C_3V3_SDA NET_SPACING_TYPE=I2C
MAKE_BASE=TRUE I2C_NB_C_3V3_SCL NET_SPACING_TYPE=I2C

Q3970 SI2302ADSE3 SOT23-3 (D, G, S)
Q3970_G — R3974 0
Q3971 SI2302ADSE3 SOT23-3 (D, G, S)
Q3971_G — R3975 0 — =PP2V5_RUN_I2C

ODD TEMP SENSOR HEADER
J3302
I2C_ODD_TEMP_SDA — R3976 33
I2C_ODD_TEMP_SCL NET_SPACING_TYPE=I2C
I2C ADDR:90

HD TEMP SENSOR HEADER
J3301
I2C_HD_TEMP_SDA — R3977 33
I2C_HD_TEMP_SCL NET_SPACING_TYPE=I2C
I2C ADDR:92

GPU TEMP SENSOR
U9390
I2C_GPU_DIODE_SDA — R3978 33
I2C_GPU_DIODE_SCL NET_SPACING_TYPE=I2C
I2C ADDR:9C

KODIAK TEMP SENSOR
U2080
I2C_NB_TEMP_SDA — R3979 33
I2C_NB_TEMP_SCL NET_SPACING_TYPE=I2C
I2C ADDR:98

NB I2C B BUS

=PP2V5_PWRON_NB_MISC
=PP1V8_PWRON_NBMEM

KODIAK I2C B
MASTER
U1900
I2C_NB_B_SDA NET_SPACING_TYPE=I2C
I2C_NB_B_SCL NET_SPACING_TYPE=I2C
PINS AG04, AK03

R3925 2.0K
R3936 2.0K

Q3903 SI2302ADSE3 SOT23-3 (D, G, S)
Q3903_G — R3924 0
R3931 2.0K
NB_IIC_B_DAT_1V8 — NET_SPACING_TYPE=I2C — R3932 0

Q3904 SI2302ADSE3 SOT23-3 (D, G, S)
Q3904_G — R3937 0
R3938 2.0K
NB_IIC_B_CLK_1V8 — NET_SPACING_TYPE=I2C — R3939 0

DDR2 DIMMS
I2C_NB_RAM_SDA — NET_SPACING_TYPE=I2C
I2C_NB_RAM_SCL — NET_SPACING_TYPE=I2C

I2C Connections

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 39 OF 154	

Q63 APPLICATION IS PP1V5 PWRON

=PPV_EI_NB 3A3 20B8 41D4 42B4

XW4100 SM NO_TEST=YES PP_VEINB P4MM SM PP

PP4100

U1900
BGA
(7 OF 10)
PART 0
PWR/GND
KODIAK-ASIC-040812

AB01	GND_0	VD2_0	AB02
AB04	GND_1	VD2_1	AB05
AB07	GND_2	VD2_2	AB08
AB10	GND_3	VD2_3	AB11
AB12	GND_4	VD2_4	AB13
AD02	GND_5	VD2_5	AD01
AD05	GND_6	VD2_6	AD04
AD08	GND_7	VD2_7	AD07
AD11	GND_8	VD2_8	AD10
AD13	GND_9	VD2_9	AD12
AD17	GND_10	VD2_10	AD16
AD21	GND_11	VD2_11	AD20
AE15	GND_12	VD2_12	AE14
AE19	GND_13	VD2_13	AE18
AF07	GND_14	VD2_14	AF08
AF10	GND_15	VD2_15	AF11
AF13	GND_16	VD2_16	AF15
AF17	GND_17	VD2_17	AF19
AG11	GND_18	VD2_18	AG13
AG15	GND_19	VD2_19	AG17
AG19	GND_20	VD2_20	AG21
AH02	GND_21	VD2_21	AH04
AH05	GND_22	VD2_22	AH07
AH08	GND_23	VD2_23	AH09
AJ13	GND_24	VD2_24	AJ11
AJ17	GND_25	VD2_25	AJ15
AJ21	GND_26	VD2_26	AJ19
AK01	GND_27	VD2_27	AK02
AK04	GND_28	VD2_28	AK05
AK07	GND_29	VD2_29	AK09
AK11	GND_30	VD2_30	AK13
AK15	GND_31	VD2_31	AK17
AK19	GND_32	VD2_32	AK21
AM02	GND_33	VD2_33	AM01
AM05	GND_34	VD2_34	AM04
AM09	GND_35	VD2_35	AM07
AM13	GND_36	VD2_36	AM11
AM17	GND_37	VD2_37	AM15
AM21	GND_38	VD2_38	AM19
AN04	GND_39	VD2_39	AN05
AN07	GND_40	VD2_40	AN09
AN11	GND_41	VD2_41	AN13
AN15	GND_42	VD2_42	AN17
AN19	GND_43	VD2_43	AN21
AP01	GND_44	VD2_44	AP02
AR05	GND_45	VD2_45	AR03
AR09	GND_46	VD2_46	AR07
AR13	GND_47	VD2_47	AR11
AR17	GND_48	VD2_48	AR15
AR21	GND_49	VD2_49	AR19
AT03	GND_50	VD2_50	AT05
AT07	GND_51	VD2_51	AT09
AT11	GND_52	VD2_52	AT13
AT15	GND_53	VD2_53	AT17
AT19	GND_54	VD2_54	AT21
K01	GND_55	VD2_55	K02
K04	GND_56	VD2_56	K05
M02	GND_57	VD2_57	K08
M05	GND_58	VD2_58	M01
M08	GND_59	VD2_59	M04
P01	GND_60	VD2_60	M07
P04	GND_61	VD2_61	M10
P07	GND_62	VD2_62	P02
P10	GND_63	VD2_63	P05
P12	GND_64	VD2_64	P08
T02	GND_65	VD2_65	P11
T05	GND_66	VD2_66	P13
T08	GND_67	VD2_67	T01
T11	GND_68	VD2_68	T04
T13	GND_69	VD2_69	T07
V01	GND_70	VD2_70	T10
V04	GND_71	VD2_71	T12
V07	GND_72	VD2_72	V02
V10	GND_73	VD2_73	V05
V12	GND_74	VD2_74	V08
Y02	GND_75	VD2_75	V11
Y05	GND_76	VD2_76	V13
Y08	GND_77	VD2_77	Y01
Y11	GND_78	VD2_78	Y04
Y13	GND_79	VD2_79	Y07
AF01	GND_80	VD2_80	Y10
AF04	GND_81	VD2_81	Y12
AF21	GND_82		
AJ08	GND_83		
AJ09	GND_84		

Q63 APPLICATION IS PP1V5 PWRON

42B4 41D6 20B8 3A3 =PPV_EI_NB

C4168 0.22UF 20% 6.3V X5R 402
C4146 0.22UF 20% 6.3V X5R 402
C4143 0.22UF 20% 6.3V X5R 402
C4139 0.22UF 20% 6.3V X5R 402
C4137 0.22UF 20% 6.3V X5R 402
C4113 0.22UF 20% 6.3V X5R 402
C4112 0.22UF 20% 6.3V X5R 402
C4106 0.22UF 20% 6.3V X5R 402
C4122 0.22UF 20% 6.3V X5R 402
C4100 0.22UF 20% 6.3V X5R 402

C4169 0.22UF 20% 6.3V X5R 402
C4147 0.22UF 20% 6.3V X5R 402
C4145 0.22UF 20% 6.3V X5R 402
C4140 0.22UF 20% 6.3V X5R 402
C4138 0.22UF 20% 6.3V X5R 402
C4114 0.22UF 20% 6.3V X5R 402
C4110 0.22UF 20% 6.3V X5R 402
C4107 0.22UF 20% 6.3V X5R 402
C4133 0.22UF 20% 6.3V X5R 402
C4111 0.22UF 20% 6.3V X5R 402

C4170 0.22UF 20% 6.3V X5R 402
C4149 0.22UF 20% 6.3V X5R 402
C4148 0.22UF 20% 6.3V X5R 402
C4142 0.22UF 20% 6.3V X5R 402
C4141 0.22UF 20% 6.3V X5R 402
C4115 0.22UF 20% 6.3V X5R 402
C4109 0.22UF 20% 6.3V X5R 402
C4108 0.22UF 20% 6.3V X5R 402
C4155 0.22UF 20% 6.3V X5R 402
C4144 0.22UF 20% 6.3V X5R 402

C4171 0.22UF 20% 6.3V X5R 402
C4161 0.22UF 20% 6.3V X5R 402
C4159 0.22UF 20% 6.3V X5R 402
C4152 0.22UF 20% 6.3V X5R 402
C4150 0.22UF 20% 6.3V X5R 402
C4125 0.22UF 20% 6.3V X5R 402
C4118 0.22UF 20% 6.3V X5R 402
C4116 0.22UF 20% 6.3V X5R 402
C4181 0.22UF 20% 6.3V X5R 402
C4166 0.22UF 20% 6.3V X5R 402

C4172 0.22UF 20% 6.3V X5R 402
C4162 0.22UF 20% 6.3V X5R 402
C4160 0.22UF 20% 6.3V X5R 402
C4153 0.22UF 20% 6.3V X5R 402
C4151 0.22UF 20% 6.3V X5R 402
C4126 0.22UF 20% 6.3V X5R 402
C4124 0.22UF 20% 6.3V X5R 402
C4117 0.22UF 20% 6.3V X5R 402
C4101 0.22UF 20% 6.3V X5R 402
C4177 0.22UF 20% 6.3V X5R 402

C4174 0.22UF 20% 6.3V X5R 402
C4165 0.22UF 20% 6.3V X5R 402
C4163 0.22UF 20% 6.3V X5R 402
C4157 0.22UF 20% 6.3V X5R 402
C4154 0.22UF 20% 6.3V X5R 402
C4127 0.22UF 20% 6.3V X5R 402
C4123 0.22UF 20% 6.3V X5R 402
C4104 0.22UF 20% 6.3V X5R 402
C4102 0.22UF 20% 6.3V X5R 402

C4173 0.22UF 20% 6.3V X5R 402
C4167 0.22UF 20% 6.3V X5R 402
C4164 0.22UF 20% 6.3V X5R 402
C4158 0.22UF 20% 6.3V X5R 402
C4156 0.22UF 20% 6.3V X5R 402
C4128 0.22UF 20% 6.3V X5R 402
C4121 0.22UF 20% 6.3V X5R 402
C4120 0.22UF 20% 6.3V X5R 402
C4105 0.22UF 20% 6.3V X5R 402
C4103 0.22UF 20% 6.3V X5R 402

C4180 0.22UF 20% 6.3V X5R 402
C4179 0.22UF 20% 6.3V X5R 402
C4178 0.22UF 20% 6.3V X5R 402
C4176 0.22UF 20% 6.3V X5R 402
C4175 0.22UF 20% 6.3V X5R 402
C4136 0.22UF 20% 6.3V X5R 402
C4135 0.22UF 20% 6.3V X5R 402
C4134 0.22UF 20% 6.3V X5R 402
C4130 0.22UF 20% 6.3V X5R 402
C4129 0.22UF 20% 6.3V X5R 402

C4132 0.22UF 20% 6.3V X5R 402
C4131 0.22UF 20% 6.3V X5R 402

KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

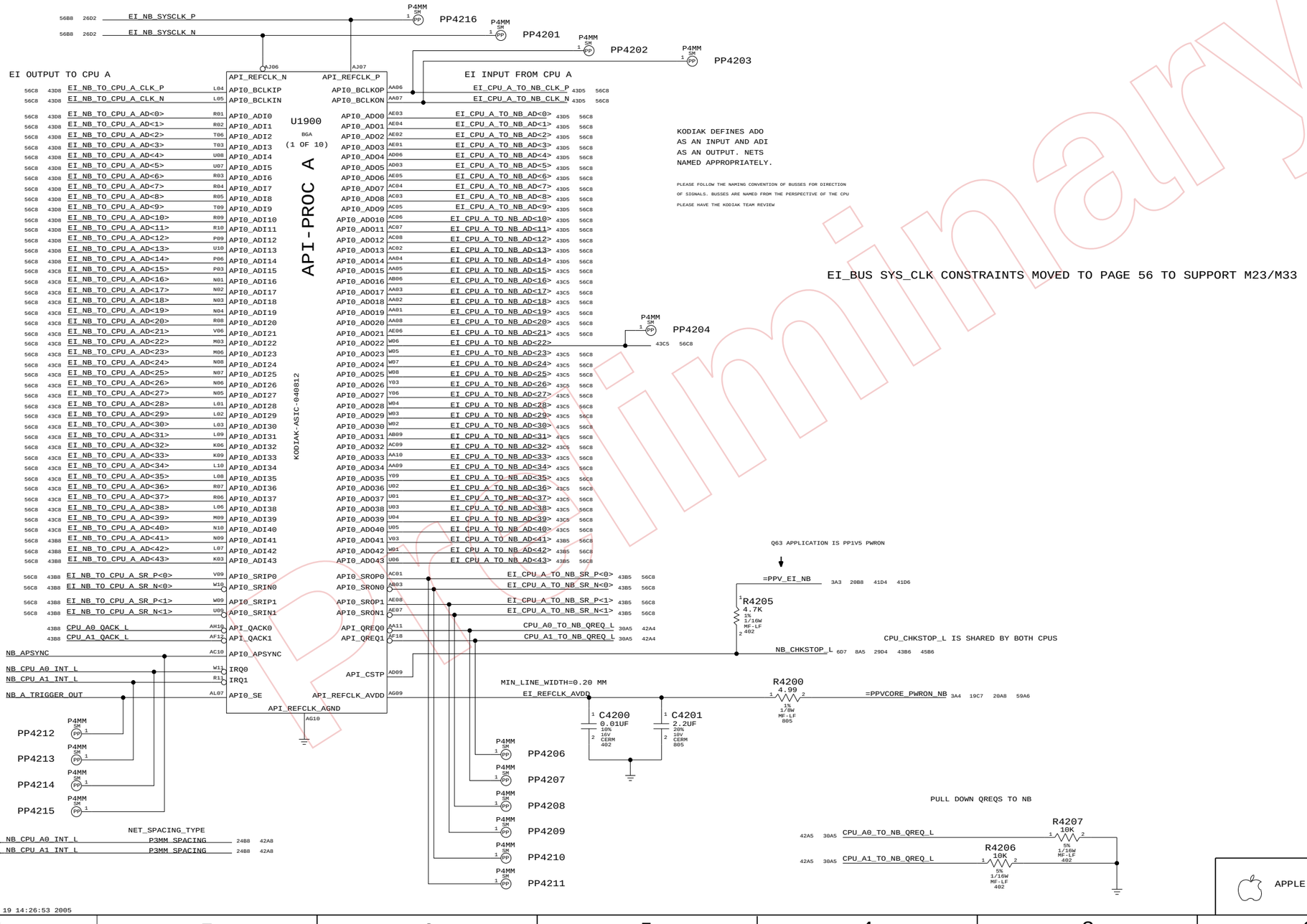
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	41	154

LAST_MODIFIED=Thu May 19 14:26:53 2005

DRAWING



KODIAK EI A

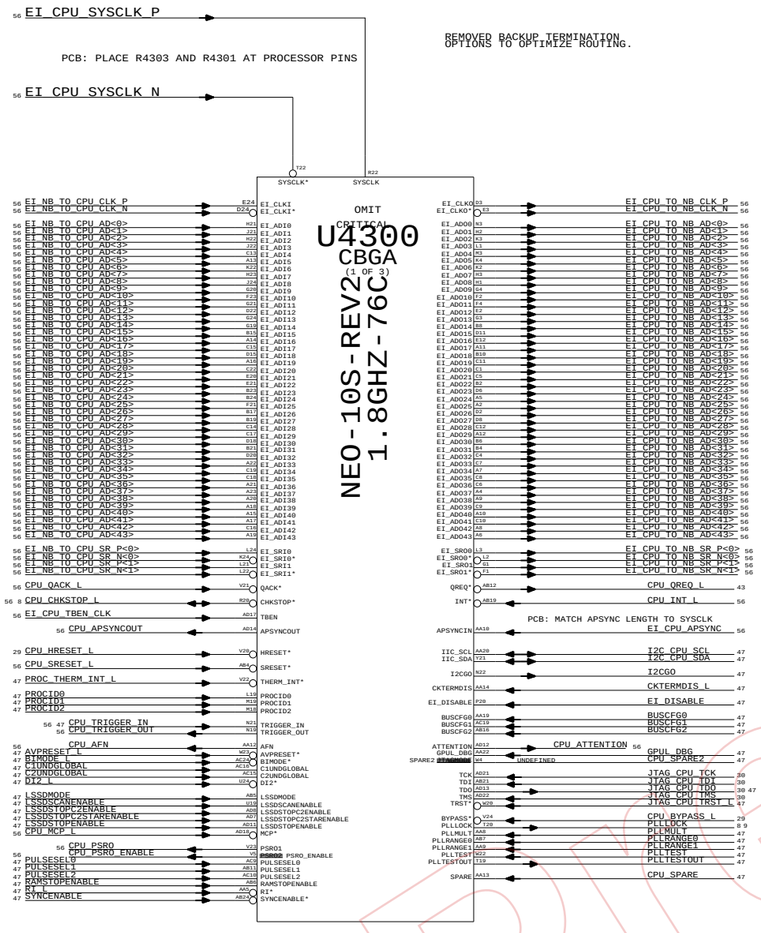
SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 42 OF 154	

LAST_MODIFIED=Thu May 19 14:26:53 2005

DRAWING



PG 49 & 52 HAVE MORE CAPS

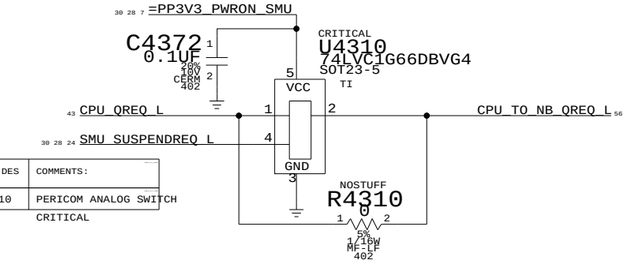
56 55 52 50 49 48 =PPVCORE_CPU

C4353 C4347 C4345 C4339 C4337 C4328 C4324 C4320 C4314 C4312
C4354 C4348 C4346 C4340 C4338 C4329 C4325 C4321 C4315 C4313
C4355 C4351 C4349 C4343 C4341 C4330 C4326 C4322 C4318 C4316
C4356 C4352 C4350 C4344 C4342 C4331 C4327 C4323 C4319 C4317
C4300 C4360 C4359 C4358 C4357 C4336 C4335 C4334 C4333 C4332
C4311 C4310 C4309 C4308 C4307 C4306 C4305 C4304 C4303 C4302

1UF 10% 6.3V 2 CERM 402

QREQ_L AND SUSPENDREQ_L AND HACK

SAME AS Q45



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U4310	PERICOM ANALOG SWITCH CRITICAL

CPU EI AND IO

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 43 OF 154	

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI INPUT FROM CPU B

U1900
BGA
(2 OF 10)
API-PROC B
KODIAK-ASIC-040812

56B8	45D8	EI_NB_TO_CPU_B_CLK_P	AT08	API1_BCLKIP	API1_BCLKOP	AT16	EI_CPU_B_TO_NB_CLK_P	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_CLK_N	AR08	API1_BCLKIN	API1_BCLKON	AR16	EI_CPU_B_TO_NB_CLK_N	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<0>	AM12	API1_ADI0	API1_AD00	AP20	EI_CPU_B_TO_NB_AD<0>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<1>	AN12	API1_ADI1	API1_AD01	AN20	EI_CPU_B_TO_NB_AD<1>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<2>	AL12	API1_ADI2	API1_AD02	AR20	EI_CPU_B_TO_NB_AD<2>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<3>	AK12	API1_ADI3	API1_AD03	AT20	EI_CPU_B_TO_NB_AD<3>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<4>	AP11	API1_ADI4	API1_AD04	AL19	EI_CPU_B_TO_NB_AD<4>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<5>	AL11	API1_ADI5	API1_AD05	AP19	EI_CPU_B_TO_NB_AD<5>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<6>	AP12	API1_ADI6	API1_AD06	AM20	EI_CPU_B_TO_NB_AD<6>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<7>	AR12	API1_ADI7	API1_AD07	AM18	EI_CPU_B_TO_NB_AD<7>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<8>	AT12	API1_ADI8	API1_AD08	AL18	EI_CPU_B_TO_NB_AD<8>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<9>	AH12	API1_ADI9	API1_AD09	AN18	EI_CPU_B_TO_NB_AD<9>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<10>	AG12	API1_ADI10	API1_AD10	AP18	EI_CPU_B_TO_NB_AD<10>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<11>	AH13	API1_ADI11	API1_AD11	AR18	EI_CPU_B_TO_NB_AD<11>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<12>	AJ12	API1_ADI12	API1_AD12	AT18	EI_CPU_B_TO_NB_AD<12>	45D6	56B8
56B8	45D8	EI_NB_TO_CPU_B_AD<13>	AG14	API1_ADI13	API1_AD13	AK18	EI_CPU_B_TO_NB_AD<13>	45D6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<14>	AM10	API1_ADI14	API1_AD14	AP17	EI_CPU_B_TO_NB_AD<14>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<15>	AL10	API1_ADI15	API1_AD15	AL17	EI_CPU_B_TO_NB_AD<15>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<16>	AN10	API1_ADI16	API1_AD16	AH20	EI_CPU_B_TO_NB_AD<16>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<17>	AP10	API1_ADI17	API1_AD17	AJ20	EI_CPU_B_TO_NB_AD<17>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<18>	AR10	API1_ADI18	API1_AD18	AK20	EI_CPU_B_TO_NB_AD<18>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<19>	AT10	API1_ADI19	API1_AD19	AH19	EI_CPU_B_TO_NB_AD<19>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<20>	AK10	API1_ADI20	API1_AD20	AG20	EI_CPU_B_TO_NB_AD<20>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<21>	AJ10	API1_ADI21	API1_AD21	AL20	EI_CPU_B_TO_NB_AD<21>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<22>	AM08	API1_ADI22	API1_AD22	AM16	EI_CPU_B_TO_NB_AD<22>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<23>	AN08	API1_ADI23	API1_AD23	AN16	EI_CPU_B_TO_NB_AD<23>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<24>	AL08	API1_ADI24	API1_AD24	AL16	EI_CPU_B_TO_NB_AD<24>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<25>	AP07	API1_ADI25	API1_AD25	AK16	EI_CPU_B_TO_NB_AD<25>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<26>	AT06	API1_ADI26	API1_AD26	AP15	EI_CPU_B_TO_NB_AD<26>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<27>	AR06	API1_ADI27	API1_AD27	AL15	EI_CPU_B_TO_NB_AD<27>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<28>	AP08	API1_ADI28	API1_AD28	AP16	EI_CPU_B_TO_NB_AD<28>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<29>	AT04	API1_ADI29	API1_AD29	AM14	EI_CPU_B_TO_NB_AD<29>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<30>	AR04	API1_ADI30	API1_AD30	AL14	EI_CPU_B_TO_NB_AD<30>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<31>	AP05	API1_ADI31	API1_AD31	AN14	EI_CPU_B_TO_NB_AD<31>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<32>	AM06	API1_ADI32	API1_AD32	AP14	EI_CPU_B_TO_NB_AD<32>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<33>	AN06	API1_ADI33	API1_AD33	AR14	EI_CPU_B_TO_NB_AD<33>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<34>	AP06	API1_ADI34	API1_AD34	AT14	EI_CPU_B_TO_NB_AD<34>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<35>	AP04	API1_ADI35	API1_AD35	AK14	EI_CPU_B_TO_NB_AD<35>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<36>	AM03	API1_ADI36	API1_AD36	AP13	EI_CPU_B_TO_NB_AD<36>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<37>	AN01	API1_ADI37	API1_AD37	AL13	EI_CPU_B_TO_NB_AD<37>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<38>	AL06	API1_ADI38	API1_AD38	AG16	EI_CPU_B_TO_NB_AD<38>	45C6	56B8
56B8	45C8	EI_NB_TO_CPU_B_AD<39>	AL05	API1_ADI39	API1_AD39	AH15	EI_CPU_B_TO_NB_AD<39>	45C6	56B8
56B8	45B8	EI_NB_TO_CPU_B_AD<40>	AL04	API1_ADI40	API1_AD40	AJ14	EI_CPU_B_TO_NB_AD<40>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_AD<41>	AL03	API1_ADI41	API1_AD41	AH14	EI_CPU_B_TO_NB_AD<41>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_AD<42>	AN02	API1_ADI42	API1_AD42	AH16	EI_CPU_B_TO_NB_AD<42>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_AD<43>	AN03	API1_ADI43	API1_AD43	AH17	EI_CPU_B_TO_NB_AD<43>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_SR_P<0>	AP09	API1_SRIP0	API1_SROP0	AG18	EI_CPU_B_TO_NB_SR_P<0>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_SR_N<0>	AL09	API1_SRIN0	API1_SRON0	AJ16	EI_CPU_B_TO_NB_SR_N<0>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_SR_P<1>	AR02	API1_SRIP1	API1_SROP1	AJ18	EI_CPU_B_TO_NB_SR_P<1>	45B6	56B8
56B8	45B8	EI_NB_TO_CPU_B_SR_N<1>	AP02	API1_SRIN1	API1_SRON1	AH18	EI_CPU_B_TO_NB_SR_N<1>	45B6	56B8
45B8		CPU_B0_QACK_L	AF14	API_QACK2	API_QREQ2	AF16	CPU_B0_TO_NB_QREQ_L	30A3	44A5
45B8		CPU_B1_QACK_L	AC11	API_QACK3	API_QREQ3	AF20	CPU_B1_TO_NB_QREQ_L	30A3	44A5
44A7	24B8	NB_CPU_B0_INT_L	N11	IRQ2					
44A7	24A8	NB_CPU_B1_INT_L	U11	IRQ3					
		TP_NB_APSYNC	AH11	API1_APSYNC					
45A6		NB_B_TRIGGER_OUT	AK08	API1_SE					

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT
ELECTRICAL_CONSTRAINT_SET
FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

WIRE TP_NB_APSYNC TO A TEST POINT

P4MM SM 1 (PP)
PP4410
PP4411
PP4413
PP4400
PP4401
PP4402
PP4403
PP4404
PP4405
PP4406
PP4407
PP4408

NET_SPACING_TYPE

Net	NB_CPU_B0_INT_L	P3MM_SPACING	24B8	44B8
Net	NB_CPU_B1_INT_L	P3MM_SPACING	24A8	44B8

PULL DOWN QREQS TO NB

44B5	30A3	CPU_B0_TO_NB_QREQ_L	R4407	10K	5% 1/10W MF-LF	402
44B5	30A3	CPU_B1_TO_NB_QREQ_L	R4406	10K	5% 1/10W MF-LF	402

KODIAK EI B

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

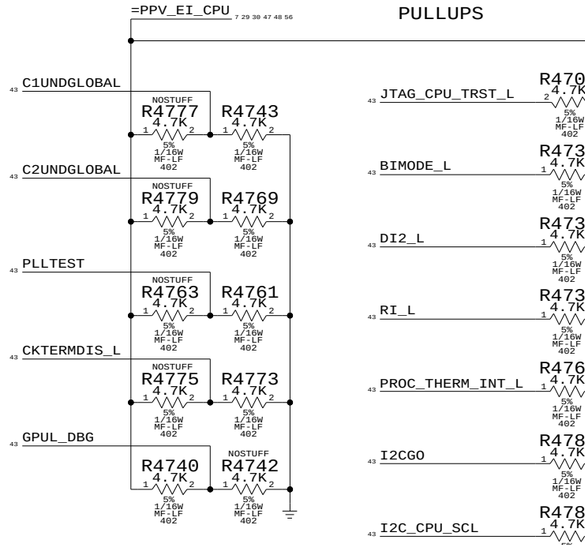
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

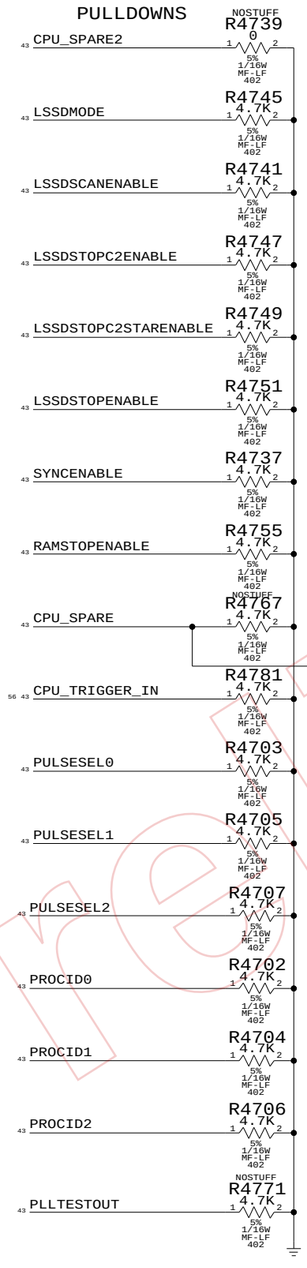
SCALE: NONE SHT 44 OF 154

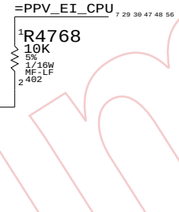
LAST_MODIFIED=Thu May 19 14:26:55 2005

DRAWING



M23/M33 IS JTAG ONLY, NO I2C





NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

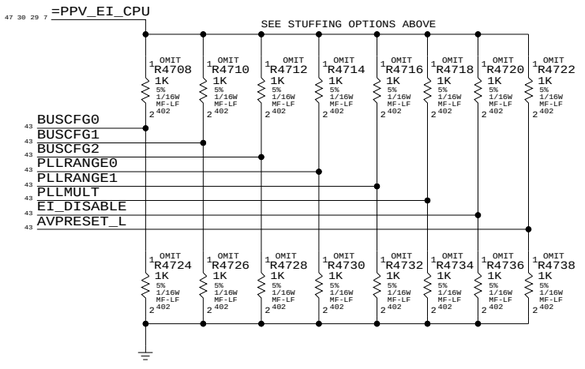
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	>= 1.8 GHZ *
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



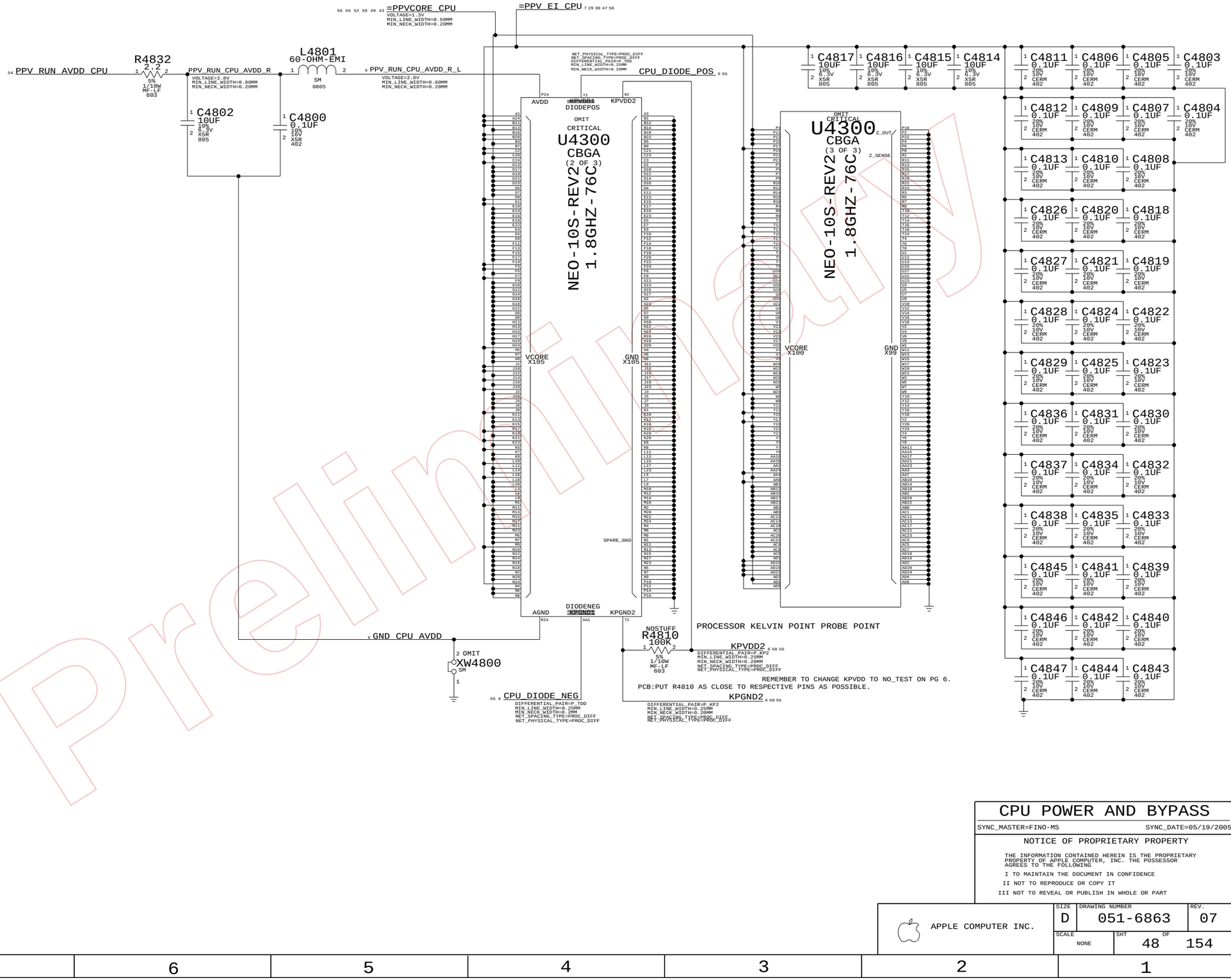
CPU STRAPS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	47	154



CPU POWER AND BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	48	154

56 55 52 50 48 43 =PPVCORE_CPU

C4922 1UF 10% 6.3V CERM 402	C4921 1UF 10% 6.3V CERM 402	C4920 1UF 10% 6.3V CERM 402	C4919 1UF 10% 6.3V CERM 402	C4918 1UF 10% 6.3V CERM 402	C4917 1UF 10% 6.3V CERM 402	C4916 1UF 10% 6.3V CERM 402	C4915 1UF 10% 6.3V CERM 402	C4912 1UF 10% 6.3V CERM 402	C4900 1UF 10% 6.3V CERM 402
C4993 1UF 10% 6.3V CERM 402	C4968 1UF 10% 6.3V CERM 402	C4961 1UF 10% 6.3V CERM 402	C4959 1UF 10% 6.3V CERM 402	C4935 1UF 10% 6.3V CERM 402	C4932 1UF 10% 6.3V CERM 402	C4926 1UF 10% 6.3V CERM 402	C4924 1UF 10% 6.3V CERM 402	C4945 1UF 10% 6.3V CERM 402	C4923 1UF 10% 6.3V CERM 402
C4994 1UF 10% 6.3V CERM 402	C4969 1UF 10% 6.3V CERM 402	C4964 1UF 10% 6.3V CERM 402	C4960 1UF 10% 6.3V CERM 402	C4936 1UF 10% 6.3V CERM 402	C4933 1UF 10% 6.3V CERM 402	C4927 1UF 10% 6.3V CERM 402	C4925 1UF 10% 6.3V CERM 402	C4956 1UF 10% 6.3V CERM 402	C4934 1UF 10% 6.3V CERM 402
C4995 1UF 10% 6.3V CERM 402	C4971 1UF 10% 6.3V CERM 402	C4965 1UF 10% 6.3V CERM 402	C4962 1UF 10% 6.3V CERM 402	C4939 1UF 10% 6.3V CERM 402	C4937 1UF 10% 6.3V CERM 402	C4930 1UF 10% 6.3V CERM 402	C4928 1UF 10% 6.3V CERM 402	C4989 1UF 10% 6.3V CERM 402	C4967 1UF 10% 6.3V CERM 402
C4996 1UF 10% 6.3V CERM 402	C4970 1UF 10% 6.3V CERM 402	C4966 1UF 10% 6.3V CERM 402	C4963 1UF 10% 6.3V CERM 402	C4940 1UF 10% 6.3V CERM 402	C4938 1UF 10% 6.3V CERM 402	C4931 1UF 10% 6.3V CERM 402	C4929 1UF 10% 6.3V CERM 402	C4901 1UF 10% 6.3V CERM 402	C4978 1UF 10% 6.3V CERM 402
C4997 1UF 10% 6.3V CERM 402	C4982 1UF 10% 6.3V CERM 402	C4976 1UF 10% 6.3V CERM 402	C4972 1UF 10% 6.3V CERM 402	C4952 1UF 10% 6.3V CERM 402	C4950 1UF 10% 6.3V CERM 402	C4943 1UF 10% 6.3V CERM 402	C4941 1UF 10% 6.3V CERM 402	C4906 1UF 10% 6.3V CERM 402	C4904 1UF 10% 6.3V CERM 402
C4998 1UF 10% 6.3V CERM 402	C4981 1UF 10% 6.3V CERM 402	C4977 1UF 10% 6.3V CERM 402	C4973 1UF 10% 6.3V CERM 402	C4953 1UF 10% 6.3V CERM 402	C4951 1UF 10% 6.3V CERM 402	C4944 1UF 10% 6.3V CERM 402	C4942 1UF 10% 6.3V CERM 402	C4907 1UF 10% 6.3V CERM 402	C4905 1UF 10% 6.3V CERM 402
C4999 1UF 10% 6.3V CERM 402	C4984 1UF 10% 6.3V CERM 402	C4979 1UF 10% 6.3V CERM 402	C4974 1UF 10% 6.3V CERM 402	C4957 1UF 10% 6.3V CERM 402	C4954 1UF 10% 6.3V CERM 402	C4948 1UF 10% 6.3V CERM 402	C4946 1UF 10% 6.3V CERM 402	C4910 1UF 10% 6.3V CERM 402	C4908 1UF 10% 6.3V CERM 402
C4902 1UF 10% 6.3V CERM 402	C4983 1UF 10% 6.3V CERM 402	C4980 1UF 10% 6.3V CERM 402	C4975 1UF 10% 6.3V CERM 402	C4958 1UF 10% 6.3V CERM 402	C4955 1UF 10% 6.3V CERM 402	C4949 1UF 10% 6.3V CERM 402	C4947 1UF 10% 6.3V CERM 402	C4911 1UF 10% 6.3V CERM 402	C4909 1UF 10% 6.3V CERM 402
C4903 1UF 10% 6.3V CERM 402	C4992 1UF 10% 6.3V CERM 402	C4991 1UF 10% 6.3V CERM 402	C4990 1UF 10% 6.3V CERM 402	C4988 1UF 10% 6.3V CERM 402	C4987 1UF 10% 6.3V CERM 402	C4986 1UF 10% 6.3V CERM 402	C4985 1UF 10% 6.3V CERM 402	C4914 1UF 10% 6.3V CERM 402	C4913 1UF 10% 6.3V CERM 402

PROC DECOUPLING

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE NONE	SHT 49 OF 154	

VCORE VOLTAGE CONTROLLER (VC)

M23/M33: PP12V_CPU IS AN ALL RAIL

=PP12V_CPU
R5029 10 5% 1/16W MF-LF 402
C5019 1UF 20% 16V CERM 1206
VC_VCC
SYS_POWERUP_L
R5000 1.5K 5% 1/16W MF-LF 402
VRM_EN
Q5012 2N7002 SOT23-LF
C5001 1UF 10% 6.3V CERM 402
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
CPU_VID_R<3>
CPU_VID_R<4>
CPU_VID_R<5>
VC_AGND
VC_BGOUT
VC_OSCREF
VC_DACSTEP
U5000 SC2642 TSSOP
BGOUT
OSCREF
VID0
VID1
VID2
VID3
VID4
VID5
DACSTEP
FB
GSENSE
OS1
OS2
AGND
VCC
OUTSEN
OUT1
OUT2
PGOOD
EROUT
VC_OUTSEN
VC_OUT1
VC_OUT2
VC_PGOOD
PGOOD IS OC
R5030 0 5% 1/10W MF-LF 402
SYS_SLEWING_L
NOSTUFF R5003 2.7M 5% 1/10W MF-LF 603
VC_EROUT
R5001 20K 5% 1/16W MF-LF 402
NOSTUFF R5002 0 5% 1/16W MF-LF 402
VC_EROUT_RC
C5002 470PF 10% 50V CERM 402
OMIT XW5000 SM
C5000 0.1UF 20% 10V CERM 402
R5028 221K 1% 1/16W MF-LF 402
VC_OS1
VC_OS2
VC_AUX1
VC_AUX2
R5013 20.5K 1% 1/16W MF-LF 402
R5016 20.5K 1% 1/16W MF-LF 402
C5004 0.0082UF 10% 25V X7R 402
NOSTUFF R5014 20.5K 1% 1/16W MF-LF 402
C5005 0.0082UF 10% 25V X7R 402
NOSTUFF R5015 20.5K 1% 1/16W MF-LF 402
VCORE_SENSE_GND
DIFFERENTIAL PAIR FOR REMOTE SENSE
VCORE_SENSE_VOUT
VC_OUTSEN
R5005 4.99K 1% 1/16W MF-LF 402
VC_VCC
VC_OS_HUB
R5004 261 1% 1/16W MF-LF 402
C5008 0.068UF 10% 10V CERM 402
R5026 301 1% 1/16W MF-LF 402
AVP ADJUSTMENT
NOSTUFF R5024 330 5% 1/10W MF-LF 402
NOSTUFF R5025 1K 5% 1/16W MF-LF 402
VC_OS_HUB_RC
PCB:PLACE R5025 CLOSE TO INDUCTOR OUTPUT LEAD.
NOSTUFF C5009 0.015UF 10% 16V X7R 402
R5027 1.5K 1% 1/16W MF-LF 402
VC_OUTSEN_R
OMIT XW5002 SM
=PPVCORE_CPU
PCB:CONNECT BETWEEN THE INDUCTOR & BULK CAPS.

VC PROCESSOR VOLTAGE SENSING

CHOICE OF:
1) VCORE PLANE SENSING
2) KELVIN POINT SENSING

PPVCORE_CPU
R5035 0 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
UNDER PROCESSOR
R5036 0 5% 1/16W MF-LF 402
VCORE_SENSE_VOUT
VCORE_SENSE_GND
NOSTUFF R5041 0 5% 1/16W MF-LF 402
KPVDD2
CPU SENSE SIDE
NOSTUFF R5042 0 5% 1/16W MF-LF 402
KPGND2

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD1_DRN	0.25 MM	0.25 MM
GD1_BST	0.25 MM	0.25 MM
GD1_VREG	0.25 MM	0.25 MM
GD1_VPN	0.25 MM	0.25 MM
GD1_TG	0.25 MM	0.25 MM
GD1_BG	0.25 MM	0.25 MM
GD1_FET_RC	0.25 MM	0.25 MM
GD1_PN	0.60 MM	0.25 MM
GD1_BST_R	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD2_DRN	0.25 MM	0.25 MM
GD2_BST	0.25 MM	0.25 MM
GD2_VREG	0.25 MM	0.25 MM
GD2_VPN	0.25 MM	0.25 MM
GD2_TG	0.25 MM	0.25 MM
GD2_BG	0.25 MM	0.25 MM
GD2_FET_RC	0.25 MM	0.25 MM
GD2_PN	0.60 MM	0.25 MM
GD2_BST_R	0.25 MM	0.25 MM

VCORE SUPPLY PHASE 1 (GD1)

PP12V_CPU_R_L
C5010 1UF 20% 16V CERM 1206
GD1_BST_R
GD1_DRN
U5010 SC1211 SOIC THMPAD
VIN
CO
DRN
BST
BG
VREG
TG
VPN
C5029 1UF 20% 16V CERM 1206
R5007 2.2 5% 1/10W MF-LF 603
GD1_BST
D5010 BAS16 SOT23
GD1_VREG
C5013 1UF 20% 16V CERM 1206
GD1_VPN
R5012 200 5% 1/16W MF-LF 402
VC_AUX1
C5014 470PF 10% 50V CERM 402
GD1_PN
C5011 330UF 20% 16V ELEC SM-3
C5035 330UF 20% 16V ELEC SM-3
CRITICAL C5012 10UF 10% 16V CERM 1210
CRITICAL Q5010 NTD60N02R CASE369
GD1_TG
R5050 10K 5% 1/16W MF-LF 402
R5010 1 5% 1/10W MF-LF 402
GD1_BG
CRITICAL Q5011 NTD70N03R CASE369
NOSTUFF C5015 0.0022UF 10% 50V CERM 402
CRITICAL Q5013 NTD70N03R CASE369
C5016 0.0047UF 10% 25V CERM 402
GD1_FET_RC
R5011 1 5% 1/8W MF-LF 805
L5010 0.36UH-30A-0.80MOHM SM
=PPVCORE_CPU
PPVCORE_CPU
C5018 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5017 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5032 1500UF 20% 0.3V ELEC TH-MCZ
C5038 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
NEED TO CHANGE TO 10MOHM CAPS - 8 PCS

VCORE SUPPLY PHASE 2 (GD2)

PP12V_CPU_R_L
C5020 1UF 20% 16V CERM 1206
GD2_BST_R
GD2_DRN
U5020 SC1211 SOIC THMPAD
VIN
CO
DRN
BST
BG
VREG
TG
VPN
VC_OUT2
C5030 1UF 20% 16V CERM 1206
R5006 2.2 5% 1/10W MF-LF 603
GD2_BST
D5020 BAS16 SOT23
GD2_VREG
C5023 1UF 20% 16V CERM 1206
GD2_VPN
R5022 200 5% 1/16W MF-LF 402
VC_AUX2
C5024 470PF 10% 50V CERM 402
GD2_PN
C5021 1000UF 20% 16V ELEC TH-KZJ-LF
C5022 10UF 10% 16V CERM 1210
CRITICAL Q5020 NTD60N02R CASE369
GD2_TG
R5051 10K 5% 1/16W MF-LF 402
R5020 1 5% 1/10W MF-LF 402
GD2_BG
CRITICAL Q5021 NTD70N03R CASE369
NOSTUFF C5025 0.0022UF 10% 50V CERM 402
CRITICAL Q5023 NTD70N03R CASE369
C5026 0.0047UF 10% 25V CERM 402
GD2_FET_RC
R5021 1 5% 1/8W MF-LF 805
L5020 0.36UH-30A-0.80MOHM SM
PPVCORE_CPU
C5028 1800UF 20% 2.5V ELEC TH-KZJ-LF
C5033 1800UF 20% 2.5V ELEC TH-KZJ-LF
C5040 1500UF 20% 0.3V ELEC TH-MCZ
C5041 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C5042 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
NEED TO CHANGE TO 10MOHM CAPS - 8 PCS

PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
VC_OSCREF	0.25 MM	0.20 MM	A76
CPU_VID_R<0..5>	0.25 MM	0.20 MM	A77
VC_DACSTEP	0.25 MM	0.20 MM	A76
VC_AGND	0.50 MM	0.20 MM	A78
VC_BGOUT	0.25 MM	0.20 MM	A80
VC_OS1	0.25 MM	0.20 MM	A76
VC_OS2	0.25 MM	0.20 MM	A82
VC_VCC	0.25 MM	0.25 MM	A81
VC_OS_HUB	0.25 MM	0.20 MM	A83
VC_OUTSEN	0.25 MM	0.20 MM	A84
VC_OUTSEN_R	0.25 MM	0.20 MM	A85
VCORE_SENSE_GND	0.25 MM	0.20 MM	A86
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	A87
VC_AUX1	0.25 MM	0.25 MM	A88
VC_AUX2	0.25 MM	0.25 MM	A89
VC_OUT1	0.45 MM	0.25 MM	A90
VC_OUT2	0.45 MM	0.25 MM	A91
VC_EROUT	0.25 MM	0.20 MM	A92
VC_EROUT_RC	0.25 MM	0.20 MM	A93
VC_OS_HUB_RC	0.25 MM	0.20 MM	A94
EI_REFCLK_AVDD	0.20 MM	0.08 MM	A95

CPU VCORE VREG

SYNC_MASTER=M33-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6863 | REV. 07

SCALE NONE | SHT 50 OF 154

56 55 50 49 48 43 =PPVCORE_CPU

CRITICAL

C5200 10UF 10% 6.3V X5R 805	C5212 10UF 10% 6.3V X5R 805	C5223 10UF 10% 6.3V X5R 805	C5234 10UF 10% 6.3V X5R 805	C5245 10UF 10% 6.3V X5R 805	C5201 10UF 10% 6.3V X5R 805	C5289 10UF 10% 6.3V X5R 805	C5278 10UF 10% 6.3V X5R 805	C5267 10UF 10% 6.3V X5R 805	C5256 10UF 10% 6.3V X5R 805
C5213 10UF 10% 6.3V X5R 805	C5211 10UF 10% 6.3V X5R 805	C5210 10UF 10% 6.3V X5R 805	C5209 10UF 10% 6.3V X5R 805	C5208 10UF 10% 6.3V X5R 805	C5207 10UF 10% 6.3V X5R 805	C5206 10UF 10% 6.3V X5R 805	C5205 10UF 10% 6.3V X5R 805	C5204 10UF 10% 6.3V X5R 805	C5203 10UF 10% 6.3V X5R 805
C5224 10UF 10% 6.3V X5R 805	C5222 10UF 10% 6.3V X5R 805	C5221 10UF 10% 6.3V X5R 805	C5220 10UF 10% 6.3V X5R 805	C5219 10UF 10% 6.3V X5R 805	C5218 10UF 10% 6.3V X5R 805	C5217 10UF 10% 6.3V X5R 805	C5216 10UF 10% 6.3V X5R 805	C5215 10UF 10% 6.3V X5R 805	C5214 10UF 10% 6.3V X5R 805
C5235 10UF 10% 6.3V X5R 805	C5233 10UF 10% 6.3V X5R 805	C5232 10UF 10% 6.3V X5R 805	C5231 10UF 10% 6.3V X5R 805	C5230 10UF 10% 6.3V X5R 805	C5229 10UF 10% 6.3V X5R 805	C5228 10UF 10% 6.3V X5R 805	C5227 10UF 10% 6.3V X5R 805	C5226 10UF 10% 6.3V X5R 805	C5225 10UF 10% 6.3V X5R 805
C5246 10UF 10% 6.3V X5R 805	C5244 10UF 10% 6.3V X5R 805	C5243 10UF 10% 6.3V X5R 805	C5242 10UF 10% 6.3V X5R 805	C5241 10UF 10% 6.3V X5R 805	C5240 10UF 10% 6.3V X5R 805	C5239 10UF 10% 6.3V X5R 805	C5238 10UF 10% 6.3V X5R 805	C5237 10UF 10% 6.3V X5R 805	C5236 10UF 10% 6.3V X5R 805
C5257 10UF 10% 6.3V X5R 805	C5255 10UF 10% 6.3V X5R 805	C5254 10UF 10% 6.3V X5R 805	C5253 10UF 10% 6.3V X5R 805	C5252 10UF 10% 6.3V X5R 805	C5251 10UF 10% 6.3V X5R 805	C5250 10UF 10% 6.3V X5R 805	C5249 10UF 10% 6.3V X5R 805	C5248 10UF 10% 6.3V X5R 805	C5247 10UF 10% 6.3V X5R 805
C5268 10UF 10% 6.3V X5R 805	C5266 10UF 10% 6.3V X5R 805	C5265 10UF 10% 6.3V X5R 805	C5264 10UF 10% 6.3V X5R 805	C5263 10UF 10% 6.3V X5R 805	C5262 10UF 10% 6.3V X5R 805	C5261 10UF 10% 6.3V X5R 805	C5260 10UF 10% 6.3V X5R 805	C5259 10UF 10% 6.3V X5R 805	C5258 10UF 10% 6.3V X5R 805
C5279 10UF 10% 6.3V X5R 805	C5277 10UF 10% 6.3V X5R 805	C5276 10UF 10% 6.3V X5R 805	C5275 10UF 10% 6.3V X5R 805	C5274 10UF 10% 6.3V X5R 805	C5273 10UF 10% 6.3V X5R 805	C5272 10UF 10% 6.3V X5R 805	C5271 10UF 10% 6.3V X5R 805	C5270 10UF 10% 6.3V X5R 805	C5269 10UF 10% 6.3V X5R 805
C5290 10UF 10% 6.3V X5R 805	C5288 10UF 10% 6.3V X5R 805	C5287 10UF 10% 6.3V X5R 805	C5286 10UF 10% 6.3V X5R 805	C5285 10UF 10% 6.3V X5R 805	C5284 10UF 10% 6.3V X5R 805	C5283 10UF 10% 6.3V X5R 805	C5282 10UF 10% 6.3V X5R 805	C5281 10UF 10% 6.3V X5R 805	C5280 10UF 10% 6.3V X5R 805
C5202 10UF 10% 6.3V X5R 805	C5299 10UF 10% 6.3V X5R 805	C5298 10UF 10% 6.3V X5R 805	C5297 10UF 10% 6.3V X5R 805	C5296 10UF 10% 6.3V X5R 805	C5295 10UF 10% 6.3V X5R 805	C5294 10UF 10% 6.3V X5R 805	C5293 10UF 10% 6.3V X5R 805	C5292 10UF 10% 6.3V X5R 805	C5291 10UF 10% 6.3V X5R 805

CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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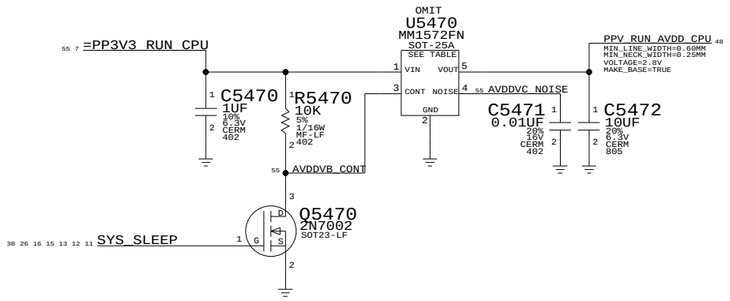
D	051-6863	07
SCALE NONE	SHT 52 OF 154	

PROCESSOR AVDD VREG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0671	1	IIC,MM1572FN,2.5V,150MA,REG,5P SOT-25A	U5470	AVDD_2V5
353S0807	1	IIC,MM1572,2.8V,150MA,REG,5P SOT-25A	U5470	AVDD_2V8

ZH5400 HOLE-VIA
ZH5401 HOLE-VIA
ZH5402 HOLE-VIA
ZH5403 HOLE-VIA
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ZH5470 HOLE-VIA
ZH5471 HOLE-VIA

CPU AVDD VREG

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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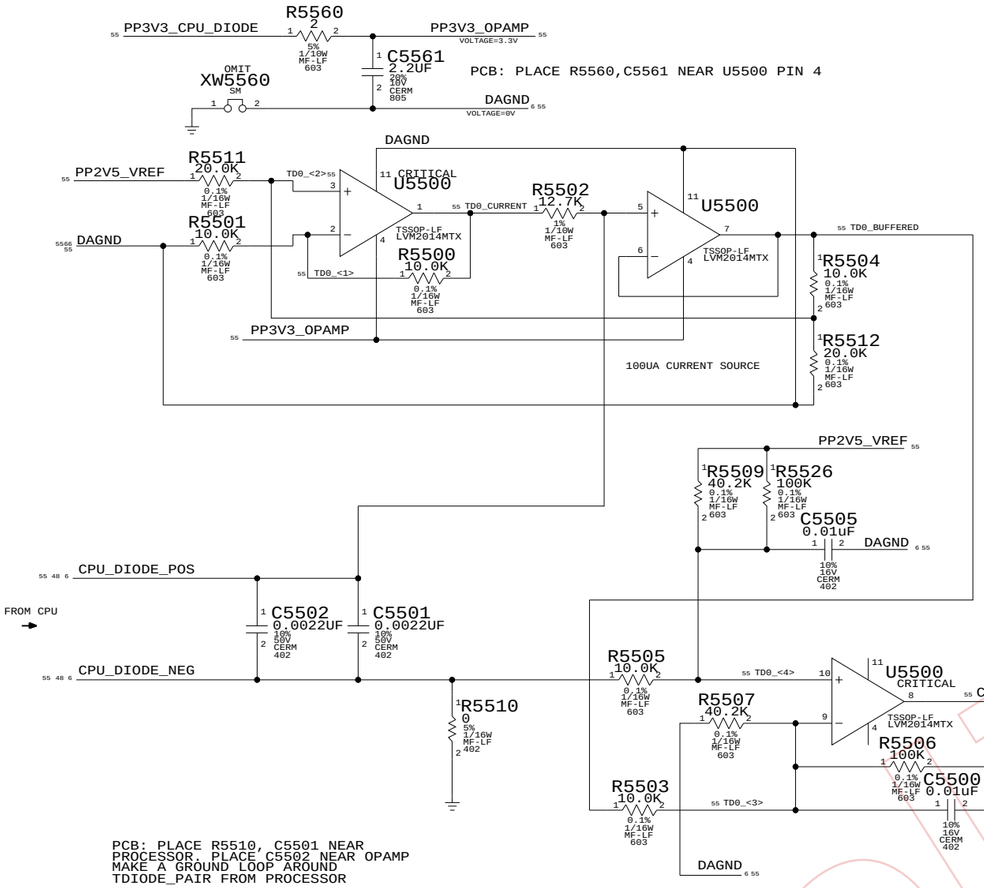
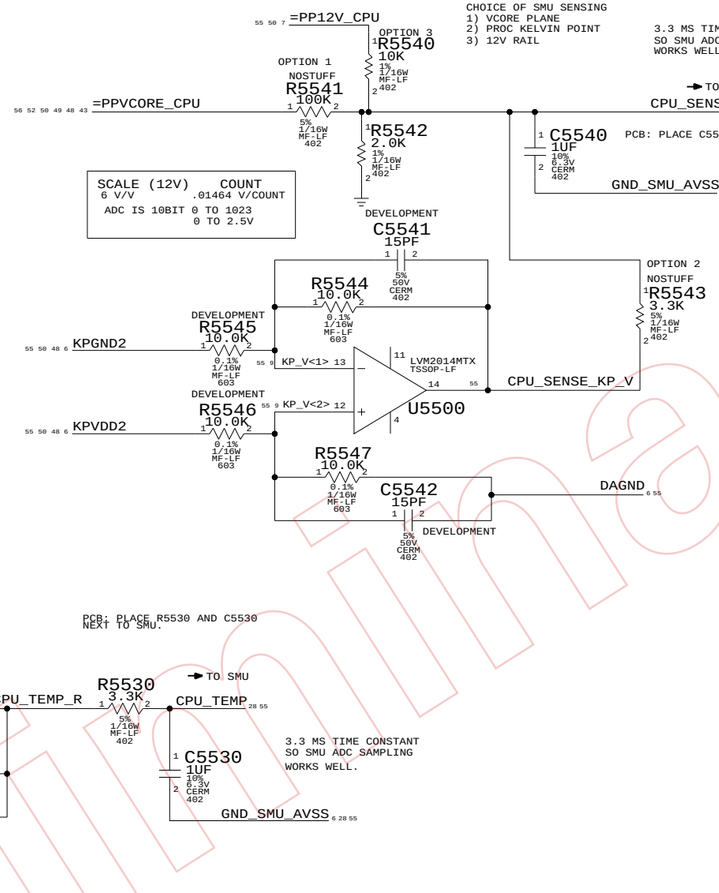
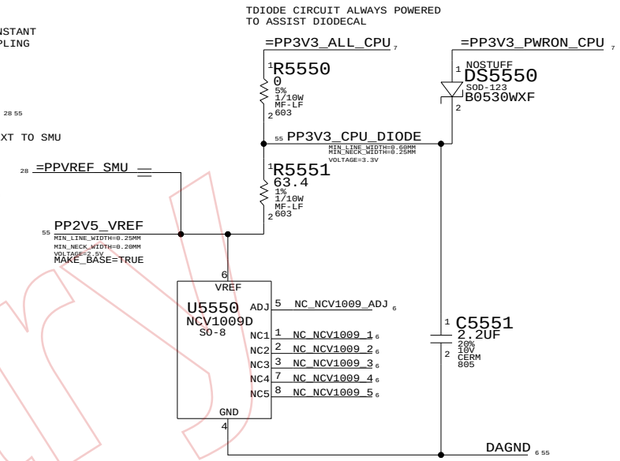
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



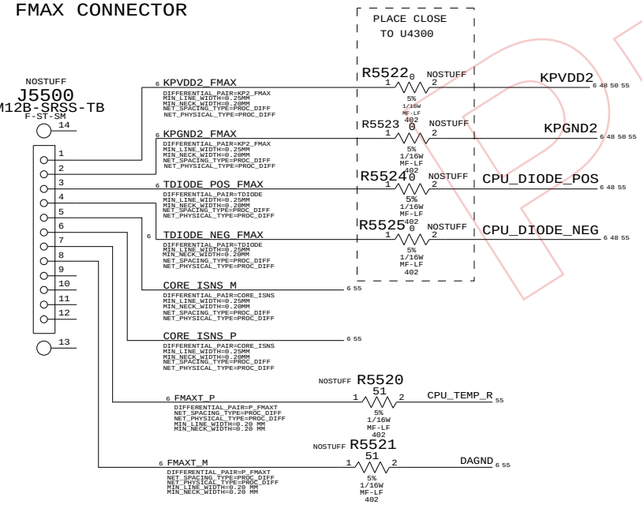
2.5V PRECISION VOLTAGE REFERENCE SOURCE



PHYSICAL CONSTRAINTS

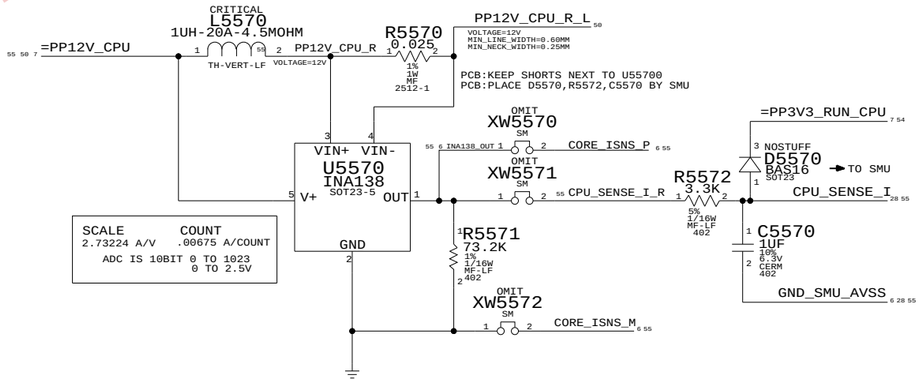
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE

(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T,V,I SENSORS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 55 OF 154	

CONNECT PULSAR CLKS TO CPU/NB

56 43	EI_CPU_SYSCLK_P	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_P 26
56 43	EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N 26
56 43	EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC 26
43	EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US 26
56	EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC 26 42
		MAKE_BASE=TRUE	

CONNECT KODIAK EI A TO/FROM CPU

56 43	EI_NB_TO_CPU_CLK_P		EI_NB_TO_CPU_A_CLK_P 42
56 43	EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N 42
56 43	EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43> 42
56 43	EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1> 42
56 43	EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1> 42
		MAKE_BASE=TRUE	
56 43	EI_CPU_TO_NB_CLK_P		EI_CPU_A_TO_NB_CLK_P 42
56 43	EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N 42
56 43	EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43> 42
56 43	EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1> 42
56 43	EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1> 42
		MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK QREQ A0

43	CPU_TO_NB_QREQ_L		CPU_A0_TO_NB_QREQ_L 42
		MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

43	CPU_QACK_L		CPU_A0_QACK_L 42
6	NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L 42
6	NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L 44
6	NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L 44
		MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

43	CPU_INT_L		CPU_A0_INT_R_L 24 56
6	NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L 42
6	NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L 44
6	NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L 44
		MAKE_BASE=TRUE	

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

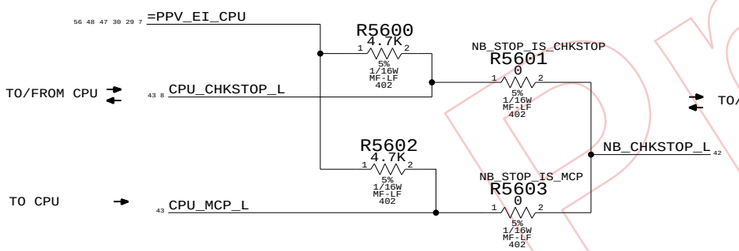
	CPU_SRESET_L_R		SB_CPU_A0_SRESET_L 24 56
	NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L 24 56
	NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L 24 56
	NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L 24 56
		MAKE_BASE=TRUE	

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

	TP_NB_B_TRIGGER_OUT		NB_B_TRIGGER_OUT 44
	TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT 42
	TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT 43
	TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN 43 47
	TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT 43
9	NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO 43
9	NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE 43
9	TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION 43
9	NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN 43
		MAKE_BASE=TRUE	

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

		ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43	EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
56 43	EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
56 43	EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
56 43	EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
56 43	EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
56 43	EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	
56 43	EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
56 43	EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		130
56 43	EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
56 43	EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		140
						137
56	EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		
56 43	EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
56 43	EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	
56 43	EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	140
42 26	EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	141
42 26	EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	139
56 43	EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		142
56 43	EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496
						1496

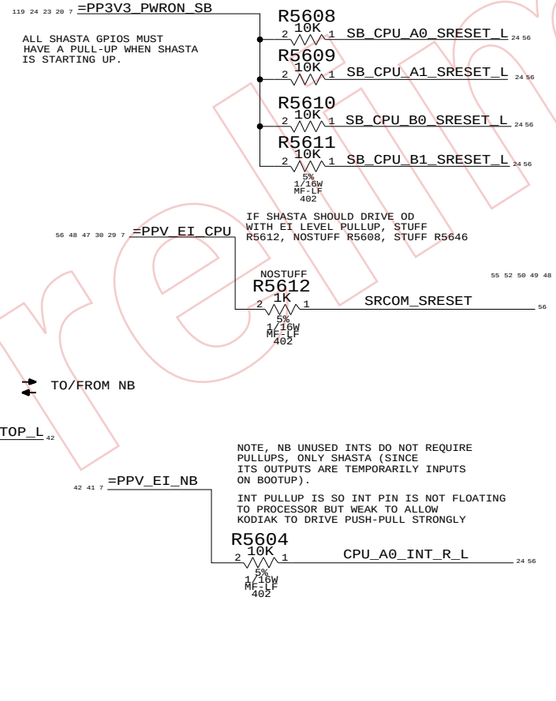
NC KODIAK EI B OUTPUT PORT

6	NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P
6	NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N 44
6	NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43> 44
6	NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1> 44
6	NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1> 44
		MAKE_BASE=TRUE	

NC KODIAK EI B INPUT PORT

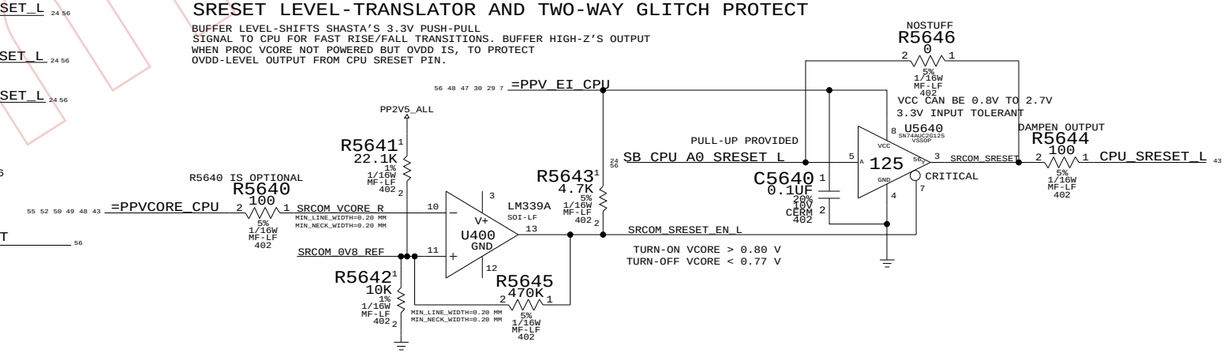
6	NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P 44
6	NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N 44
6	NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43> 44
6	NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1> 44
6	NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1> 44
		MAKE_BASE=TRUE	

PULLUPS FOR SRESET'S FROM SHASTA



SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.



CPU ALIASES & MISC

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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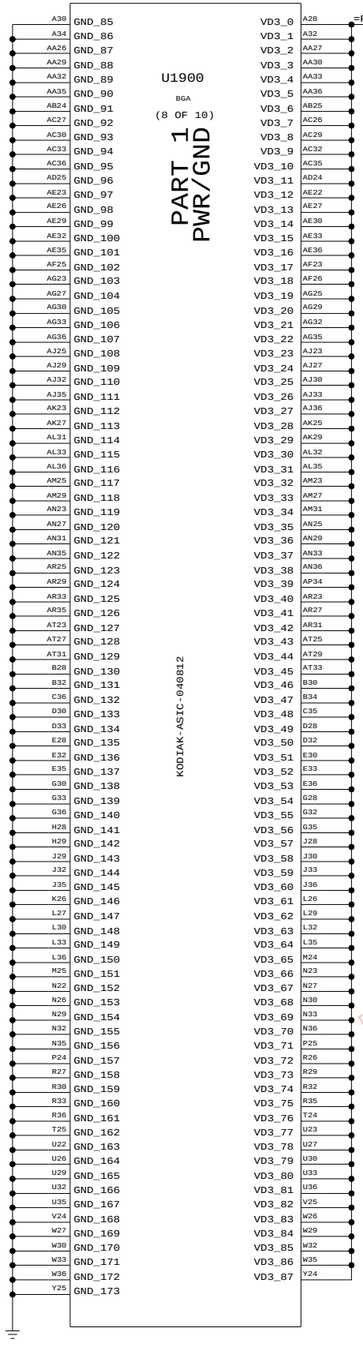

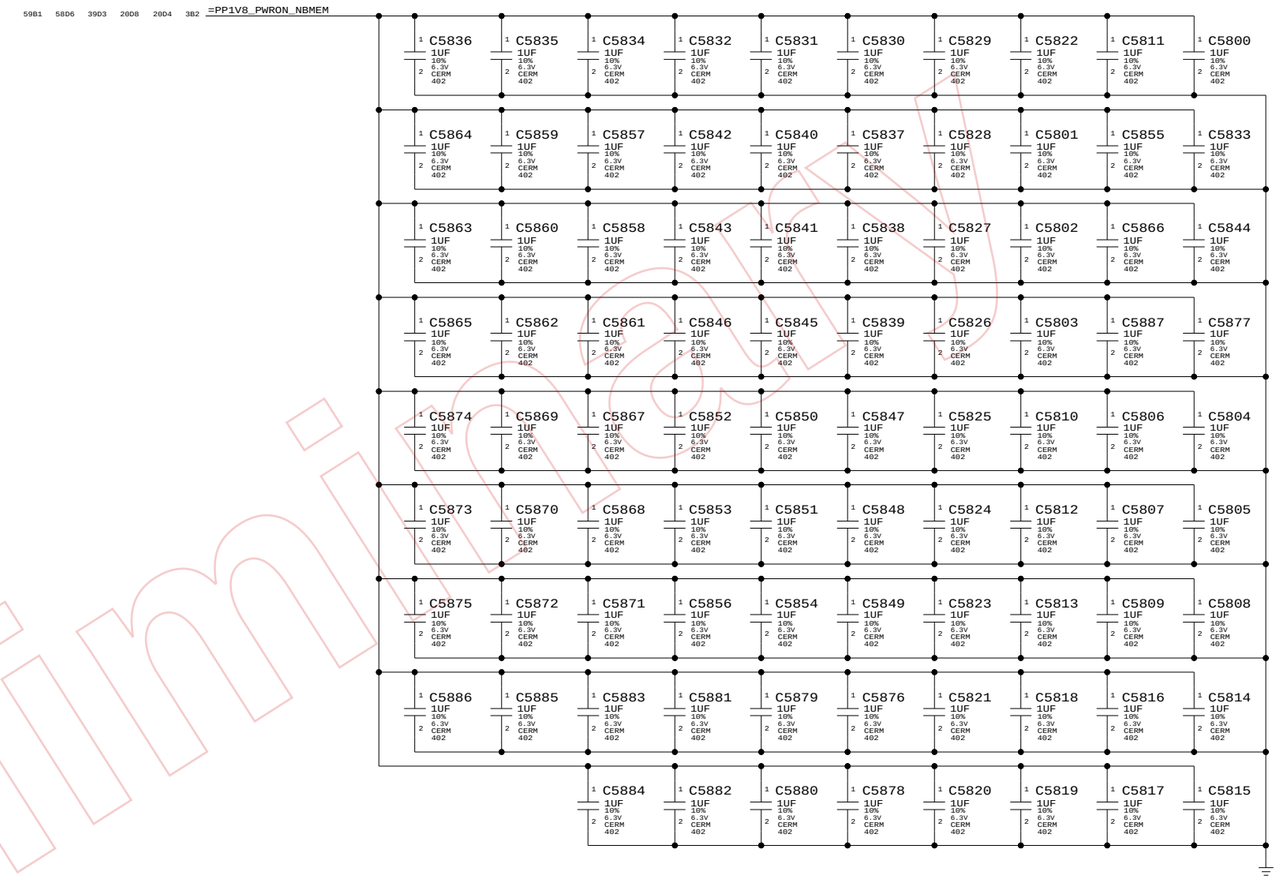

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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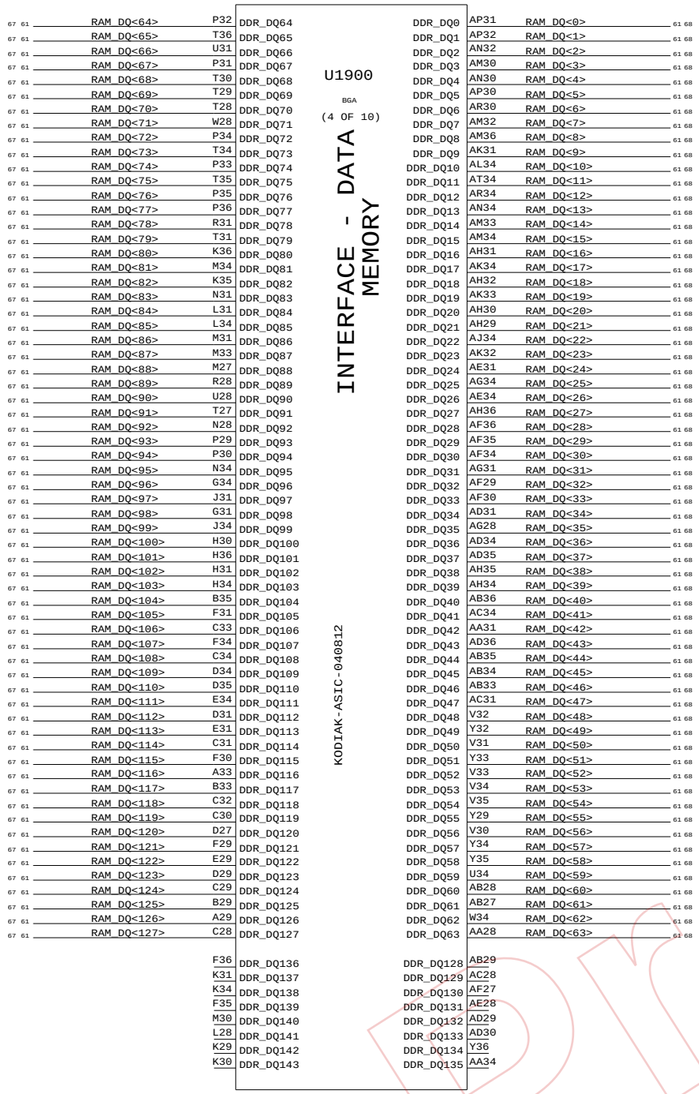
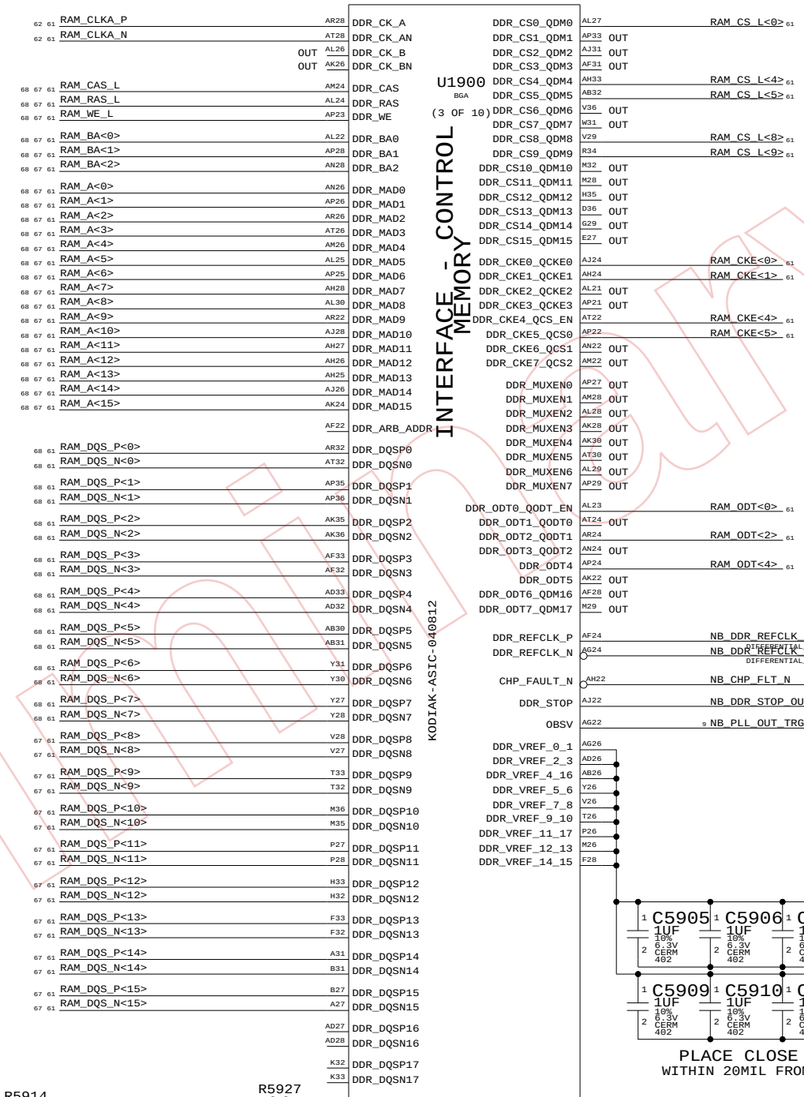
D	051-6863	07
SCALE: NONE	SHT 58 OF 154	

LAST_MODIFIED=Thu May 19 14:27:05 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS



Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	0	0	4	J6700 rank 1	64:127
B3	1	1	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	10	4	5	*unused*	64:127
D7	11	5	-	*unused*	64:127
E8	4	2	2	*unused*	0:63
E9	5	3	-	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	-	*unused*	64:127
G12	6	3	3	*unused*	0:63
G13	7	3	-	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	-	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	-	*unused*	64:127

Kodiak Memory Dq/Ctl

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

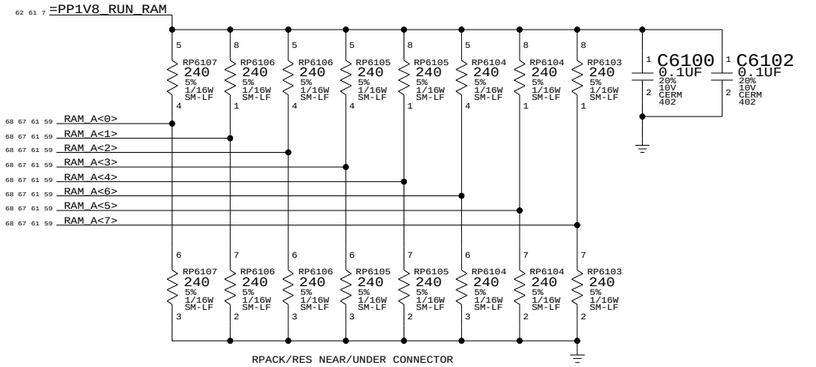
APPLE COMPUTER INC.

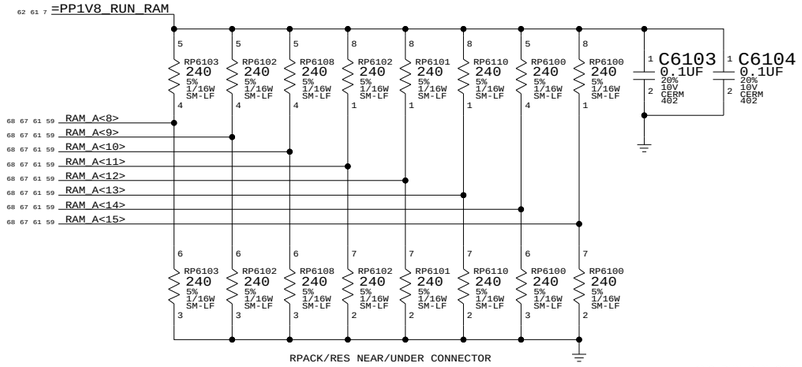
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

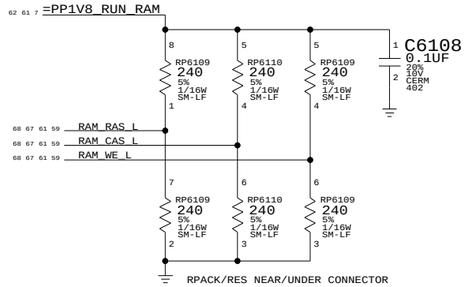
SCALE	SHT	OF
NONE	59	154

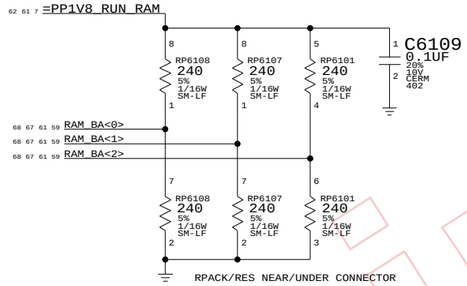
KODIAK MEMORY INTERFACE

ALL R PACKS ARE 1/16W 5%









RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		1245
RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		1487
RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		1242
RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT		1246
RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT		1244
RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		1238
RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		1241
RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT		1675
RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		1234
RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		1236
RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT		1235
RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT		1237
RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		1239
RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT		1592
RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		1232
RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		1674
RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		1676
RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT		1677
RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		1593
RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		1594

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	1206
RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	1207
RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	1210
RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	1211
RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	1212
RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	1213
RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	1214
RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	1215
RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	1216
RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	1217
RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	1218
RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	1219
RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	1220
RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	1221
RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	1222
RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	1223
RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	1224
RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	1225
RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	1226
RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	1227
RAM_DQ<7..0>		RAM_CAD	RAM_CAD		1628
RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	1229
RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	1470
RAM_DQ<15..8>		RAM_CAD	RAM_CAD		1629
RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	1251
RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	1471
RAM_DQ<23..16>		RAM_CAD	RAM_CAD		1654
RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	1253
RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	1472
RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD		1256
RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	1255
RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	1473
RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD		1258
RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	1257
RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	1474
RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD		1260
RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	1259
RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	1475
RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD		1262
RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	1261
RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	1476
RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD		1264
RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	1263
RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	1477
RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD		1267
RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	1266
RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	1478
RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD		1608
RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	1269
RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	1479
RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD		1609
RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	1270
RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	1480
RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD		1611
RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	1272
RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	1481
RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD		1274
RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	1273
RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	1482
RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD		1277
RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	1276
RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	1483
RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD		1278
RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	1279
RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	1484
RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD		1281
RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	1280
RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	1485
RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		1554
RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS		1556
RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS		1486
RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1572
RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1256
RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1258
RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		1574
RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1257
RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1568
RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1569
RAM_A_R<15..0>		RAM_CAD	RAM_CAD		1606
RAM_BA_R<2..0>		RAM_CAD	RAM_CAD		1604
RAM_RAS_L_R		RAM_CAD	RAM_CAD		1603
RAM_CAS_L_R		RAM_CAD	RAM_CAD		1605
RAM_WE_L_R		RAM_CAD	RAM_CAD		1601

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

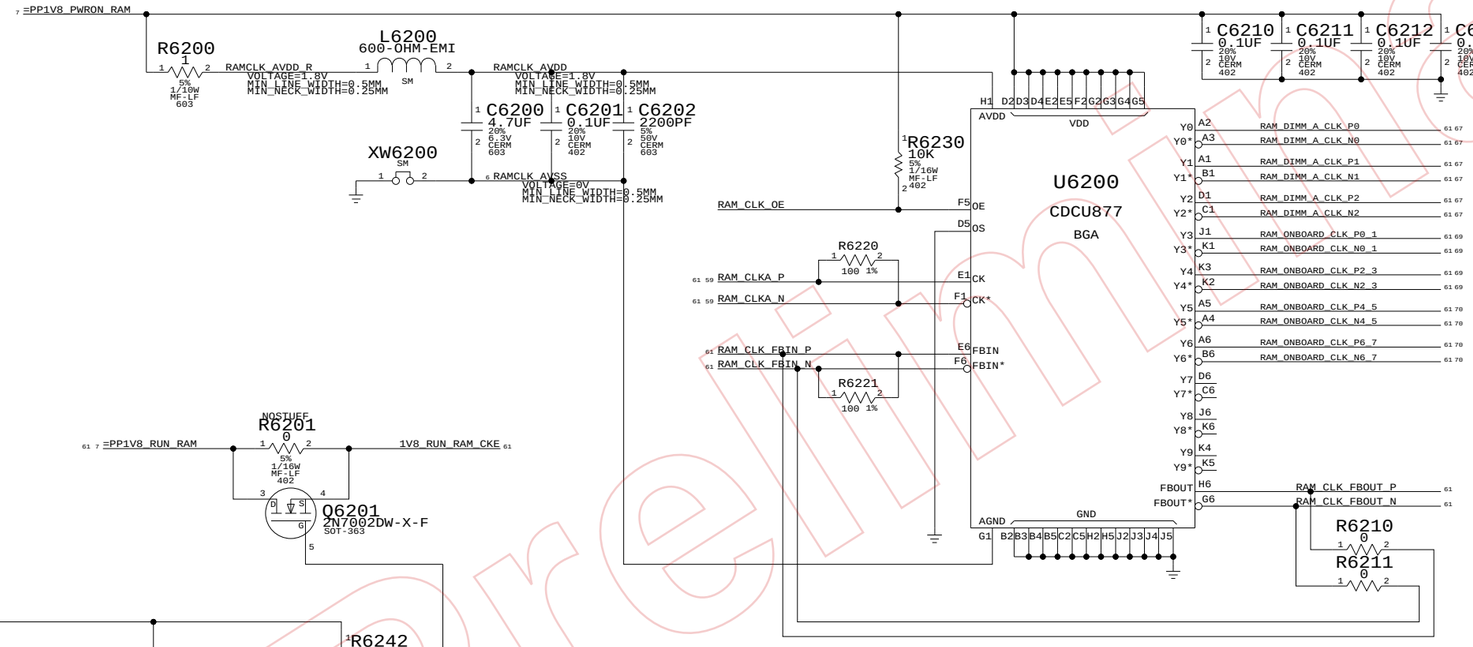
RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 61 OF 154	



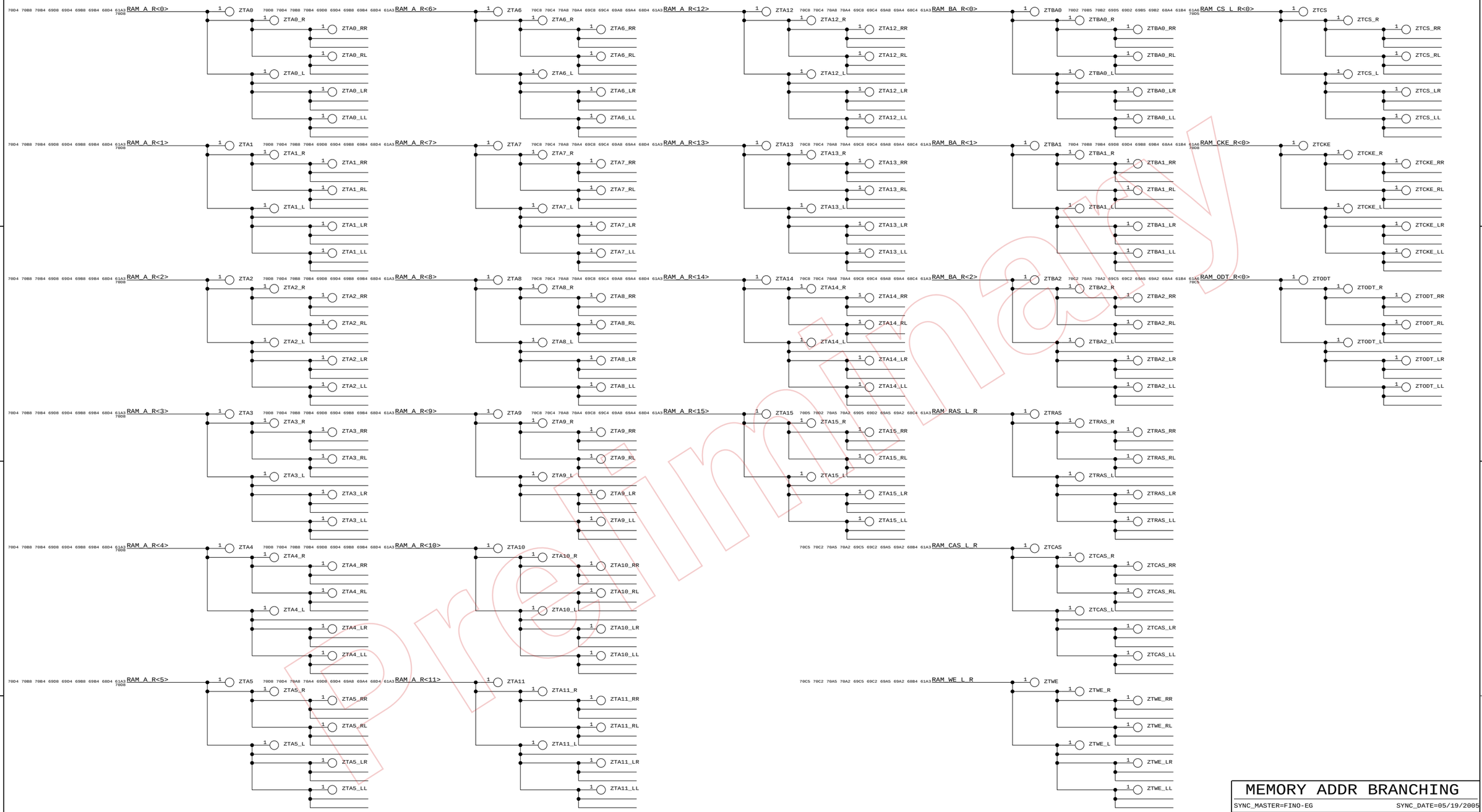
Main Memory Clock Buffer

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT
NONE	62 OF 154



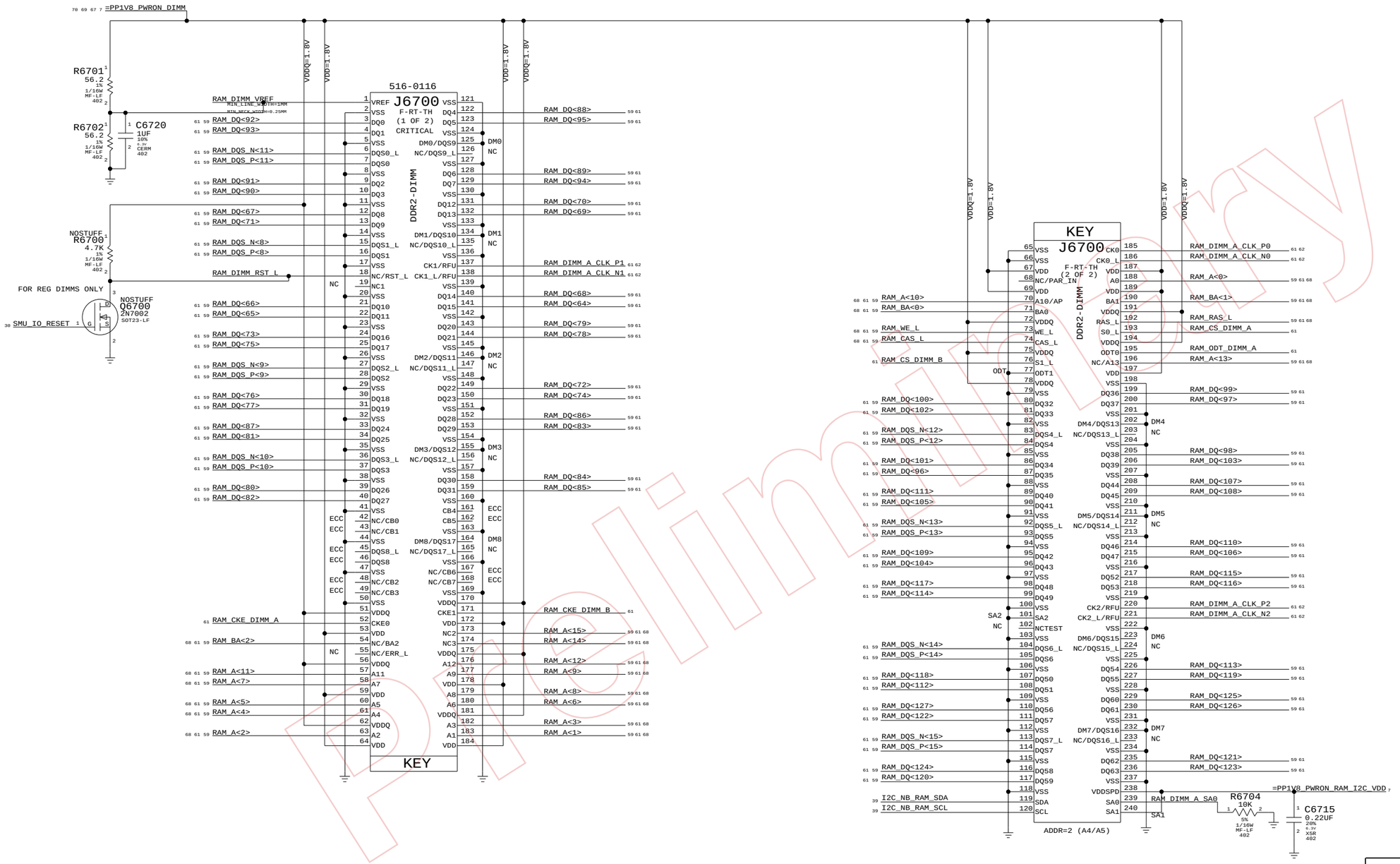
MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE NONE SHT 63 OF 154



Memory Dimm A

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 67 OF 154	

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

61 59	RAM_DQ<0>	22	4	5	RP6800	RAM_DQ_R<0>	61 69
61 59	RAM_DQ<1>	22	3	6	RP6800	RAM_DQ_R<1>	6 61 69
61 59	RAM_DQ<2>	22	1	8	RP6801	RAM_DQ_R<2>	6 61 69
61 59	RAM_DQ<3>	22	3	6	RP6801	RAM_DQ_R<3>	6 61 69
61 59	RAM_DQ<4>	22	4	5	RP6801	RAM_DQ_R<4>	61 69
61 59	RAM_DQ<5>	22	2	7	RP6800	RAM_DQ_R<5>	6 61 69
61 59	RAM_DQ<6>	22	2	7	RP6801	RAM_DQ_R<6>	6 61 69
61 59	RAM_DQ<7>	22	1	8	RP6800	RAM_DQ_R<7>	6 61 69
61 59	RAM_DQ<8>	22	3	6	RP6802	RAM_DQ_R<8>	6 61 69
61 59	RAM_DQ<9>	22	4	5	RP6803	RAM_DQ_R<9>	61 69
61 59	RAM_DQ<10>	22	1	8	RP6803	RAM_DQ_R<10>	6 61 69
61 59	RAM_DQ<11>	22	4	5	RP6802	RAM_DQ_R<11>	6 61 69
61 59	RAM_DQ<12>	22	3	6	RP6803	RAM_DQ_R<12>	6 61 69
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61 59	RAM_DQ<14>	22	2	7	RP6803	RAM_DQ_R<14>	6 61 69
61 59	RAM_DQ<15>	22	1	8	RP6802	RAM_DQ_R<15>	61 69
61 59	RAM_DQ<16>	22	3	6	RP6805	RAM_DQ_R<16>	6 61 69
61 59	RAM_DQ<17>	22	4	5	RP6805	RAM_DQ_R<17>	6 61 69
61 59	RAM_DQ<18>	22	1	8	RP6804	RAM_DQ_R<18>	61 69
61 59	RAM_DQ<19>	22	2	7	RP6805	RAM_DQ_R<19>	6 61 69
61 59	RAM_DQ<20>	22	2	7	RP6804	RAM_DQ_R<20>	6 61 69
61 59	RAM_DQ<21>	22	4	5	RP6804	RAM_DQ_R<21>	6 61 69
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61 59	RAM_DQ<23>	22	1	8	RP6805	RAM_DQ_R<23>	61 69
61 59	RAM_DQ<24>	22	4	5	RP6807	RAM_DQ_R<24>	6 61 69
61 59	RAM_DQ<25>	22	2	7	RP6806	RAM_DQ_R<25>	6 61 69
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61 59	RAM_DQ<28>	22	3	6	RP6807	RAM_DQ_R<28>	6 61 69
61 59	RAM_DQ<29>	22	3	6	RP6806	RAM_DQ_R<29>	6 61 69
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61 59	RAM_DQ<32>	22	4	5	RP6809	RAM_DQ_R<32>	6 61 70
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61 59	RAM_DQ<62>	22	1	8	RP6815	RAM_DQ_R<62>	61 70
61 59	RAM_DQ<63>	22	4	5	RP6814	RAM_DQ_R<63>	6 61 70

61 59	RAM_DQS_P<0>	22	1	2	R6800	RAM_DQS_P_R<0>	61 69
61 59	RAM_DQS_N<0>	22	1	2	R6810	RAM_DQS_N_R<0>	61 69
61 59	RAM_DQS_P<1>	22	1	2	R6801	RAM_DQS_P_R<1>	61 69
61 59	RAM_DQS_N<1>	22	1	2	R6811	RAM_DQS_N_R<1>	61 69
61 59	RAM_DQS_P<2>	22	1	2	R6802	RAM_DQS_P_R<2>	61 69
61 59	RAM_DQS_N<2>	22	1	2	R6812	RAM_DQS_N_R<2>	61 69
61 59	RAM_DQS_P<3>	22	1	2	R6803	RAM_DQS_P_R<3>	61 69
61 59	RAM_DQS_N<3>	22	1	2	R6813	RAM_DQS_N_R<3>	61 69
61 59	RAM_DQS_P<4>	22	1	2	R6804	RAM_DQS_P_R<4>	61 70
61 59	RAM_DQS_N<4>	22	1	2	R6814	RAM_DQS_N_R<4>	61 70
61 59	RAM_DQS_P<5>	22	1	2	R6805	RAM_DQS_P_R<5>	61 70
61 59	RAM_DQS_N<5>	22	1	2	R6815	RAM_DQS_N_R<5>	61 70
61 59	RAM_DQS_P<6>	22	1	2	R6806	RAM_DQS_P_R<6>	61 70
61 59	RAM_DQS_N<6>	22	1	2	R6816	RAM_DQS_N_R<6>	61 70
61 59	RAM_DQS_P<7>	22	1	2	R6807	RAM_DQS_P_R<7>	61 70
61 59	RAM_DQS_N<7>	22	1	2	R6817	RAM_DQS_N_R<7>	61 70

67 61 59	RAM_A<0>	5.1	1	8	RP6824	RAM_A_R<0>	61 63 69 70
67 61 59	RAM_A<1>	5.1	1	8	RP6823	RAM_A_R<1>	61 63 69 70
67 61 59	RAM_A<2>	5.1	2	7	RP6823	RAM_A_R<2>	61 63 69 70
67 61 59	RAM_A<3>	5.1	4	5	RP6822	RAM_A_R<3>	61 63 69 70
67 61 59	RAM_A<4>	5.1	3	6	RP6822	RAM_A_R<4>	61 63 69 70
67 61 59	RAM_A<5>	5.1	2	7	RP6822	RAM_A_R<5>	61 63 69 70
67 61 59	RAM_A<6>	5.1	1	8	RP6822	RAM_A_R<6>	61 63 69 70
67 61 59	RAM_A<7>	5.1	3	6	RP6821	RAM_A_R<7>	61 63 69 70
67 61 59	RAM_A<8>	5.1	4	5	RP6821	RAM_A_R<8>	61 63 69 70
67 61 59	RAM_A<9>	5.1	1	8	RP6821	RAM_A_R<9>	61 63 69 70
67 61 59	RAM_A<10>	5.1	3	6	RP6824	RAM_A_R<10>	61 63 69 70
67 61 59	RAM_A<11>	5.1	2	7	RP6821	RAM_A_R<11>	61 63 69 70
67 61 59	RAM_A<12>	5.1	4	5	RP6820	RAM_A_R<12>	61 63 69 70
67 61 59	RAM_A<13>	5.1	4	5	RP6825	RAM_A_R<13>	61 63 69 70
67 61 59	RAM_A<14>	5.1	2	7	RP6820	RAM_A_R<14>	61 63 69 70
67 61 59	RAM_A<15>	5.1	1	8	RP6820	RAM_A_R<15>	61 63 69 70

ZT6800 ZT6801 ZT6802 ZT6803 ZT6804 ZT6805 ZT6806 ZT6807 ZT6808 ZT6809 ZT6810 ZT6811 ZT6812 ZT6813 ZT6814 ZT6815

VIAS FOR ECC STUB

67 61 59	RAM_BA<0>	5.1	4	5	RP6824	RAM_BA_R<0>	61 63 69 70
67 61 59	RAM_BA<1>	5.1	2	7	RP6824	RAM_BA_R<1>	61 63 69 70
67 61 59	RAM_BA<2>	5.1	3	6	RP6820	RAM_BA_R<2>	61 63 69 70
67 61 59	RAM_RAS_L	5.1	1	8	RP6825	RAM_RAS_L_R	61 63 69 70
67 61 59	RAM_CAS_L	5.1	3	6	RP6825	RAM_CAS_L_R	61 63 69 70
67 61 59	RAM_WE_L	5.1	2	7	RP6825	RAM_WE_L_R	61 63 69 70

ZT6820 ZT6821 ZT6822 ZT6825 ZT6826 ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870 24PF 5% 50V C0G 402

C6871 2PF +/-0.25PF 50V C0G 402-1 — RAM_CS_L_R<0> 61 63 69 70

C6880 24PF 5% 50V C0G 402

C6881 2PF +/-0.25PF 50V C0G 402-1 — RAM_CKE_R<0> 61 63 69 70

C6890 24PF 5% 50V C0G 402

C6891 2PF +/-0.25PF 50V C0G 402-1 — RAM_ODT_R<0> 61 63 69 70

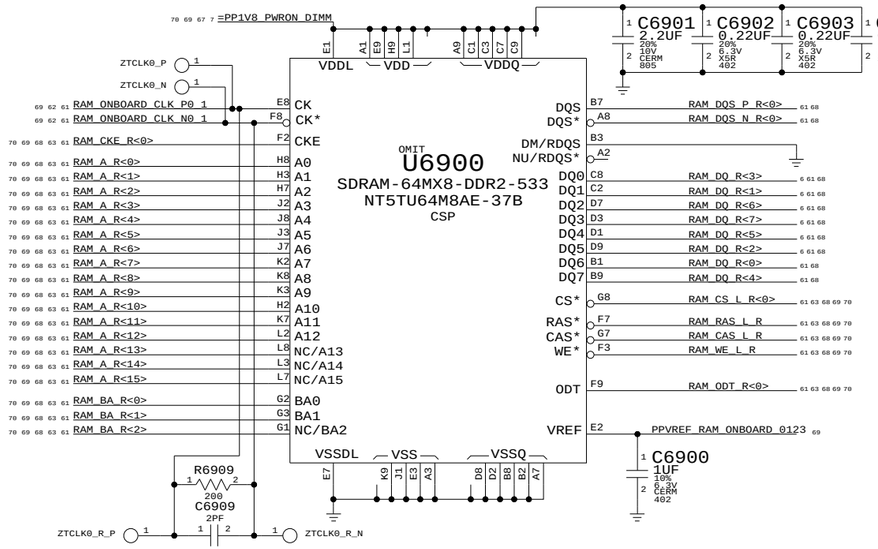
MLB Mem Series Term

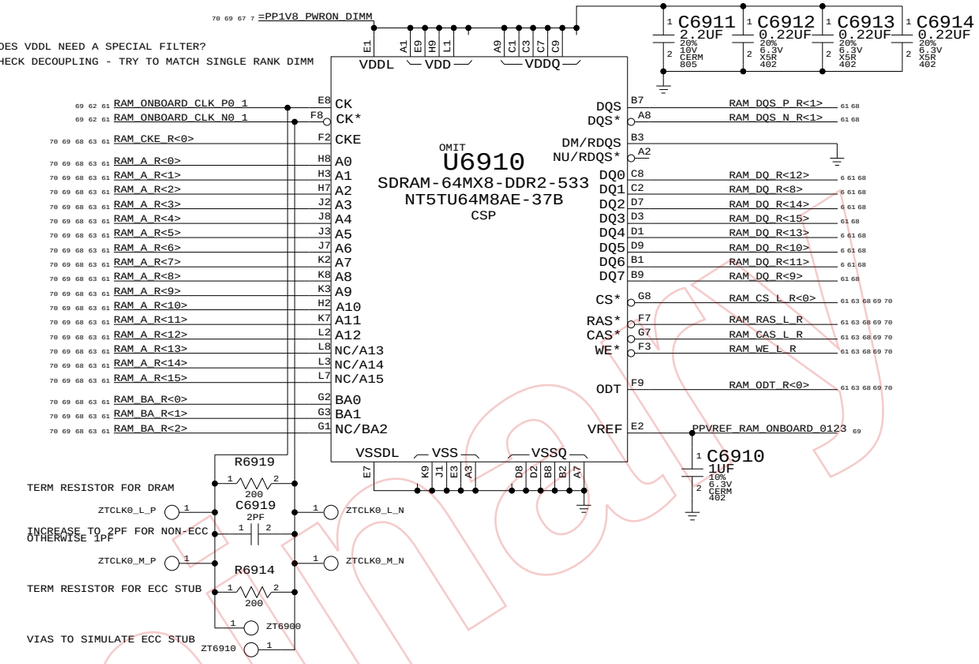
SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

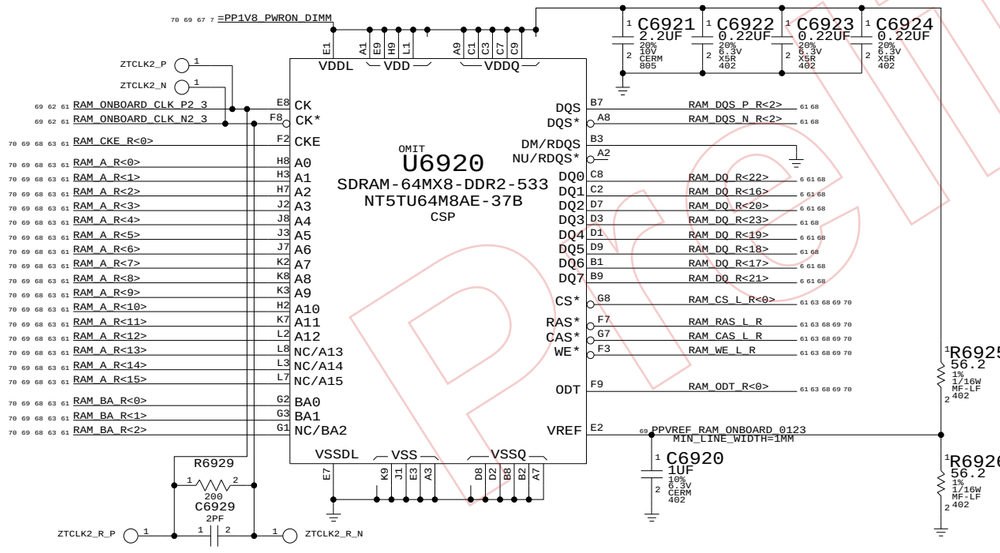
APPLE COMPUTER INC.

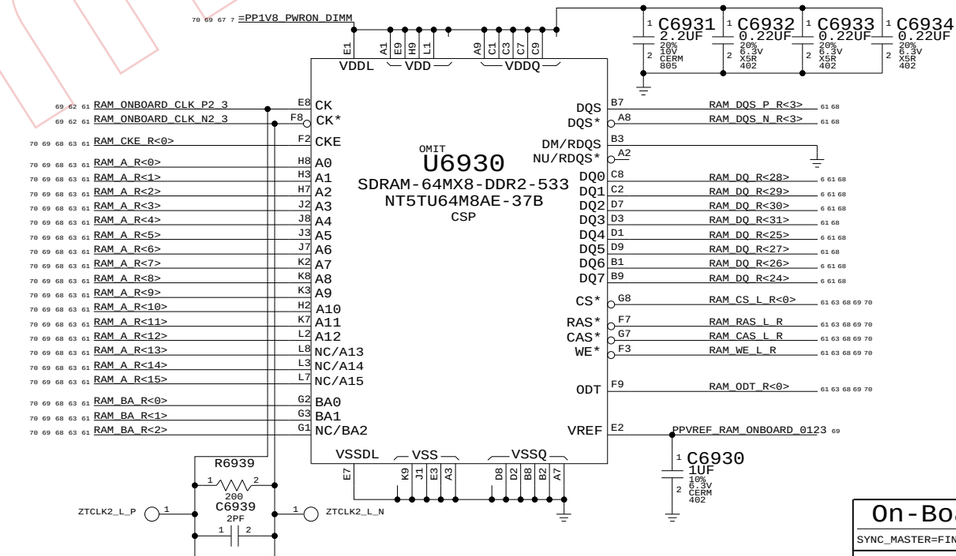
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	68	154









PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	

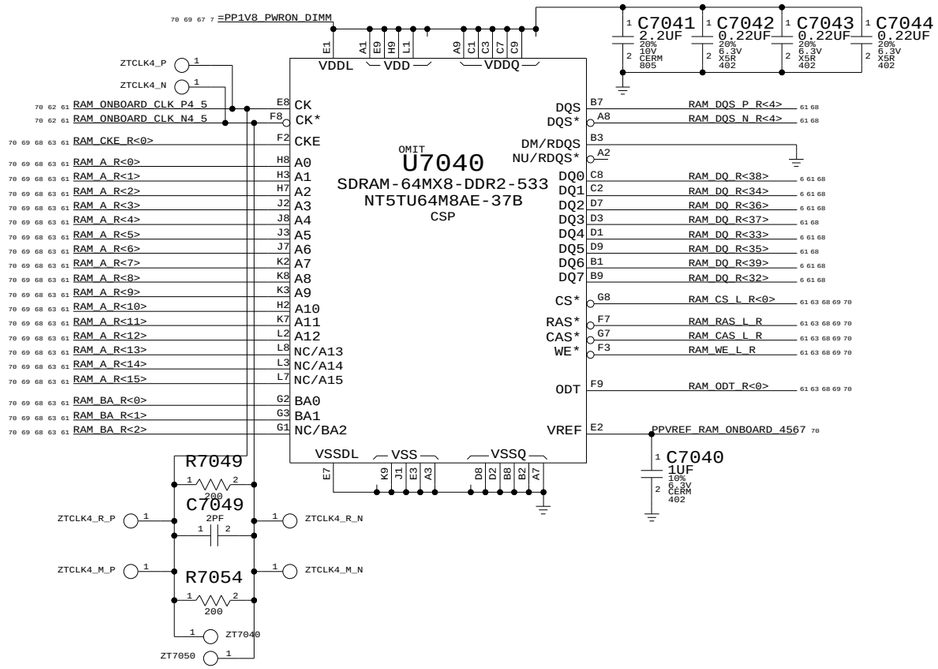
On-Board DDR SDRAM

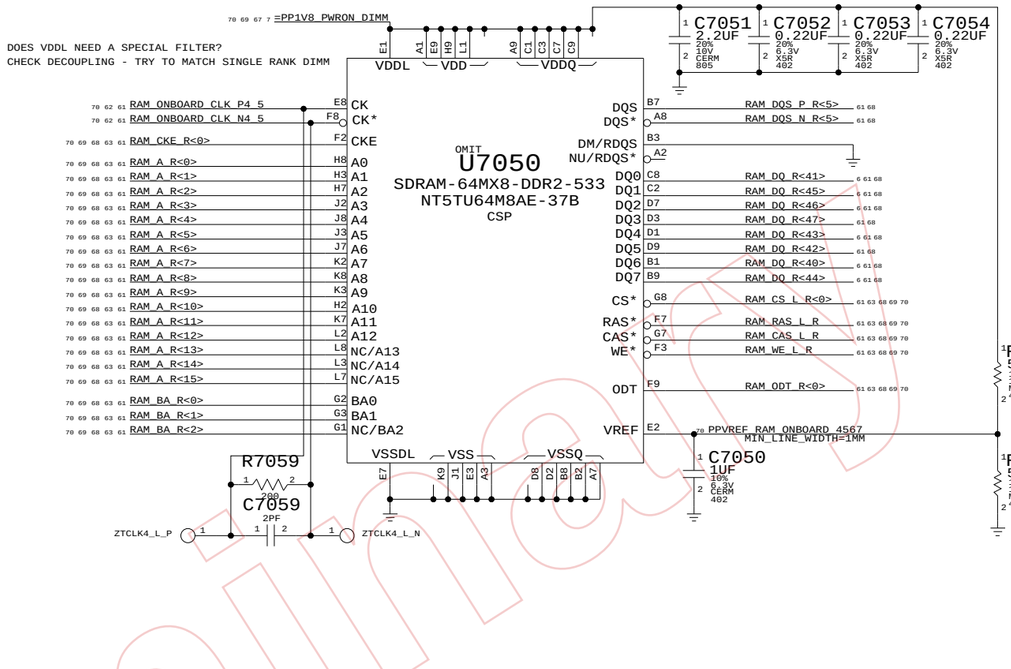
SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

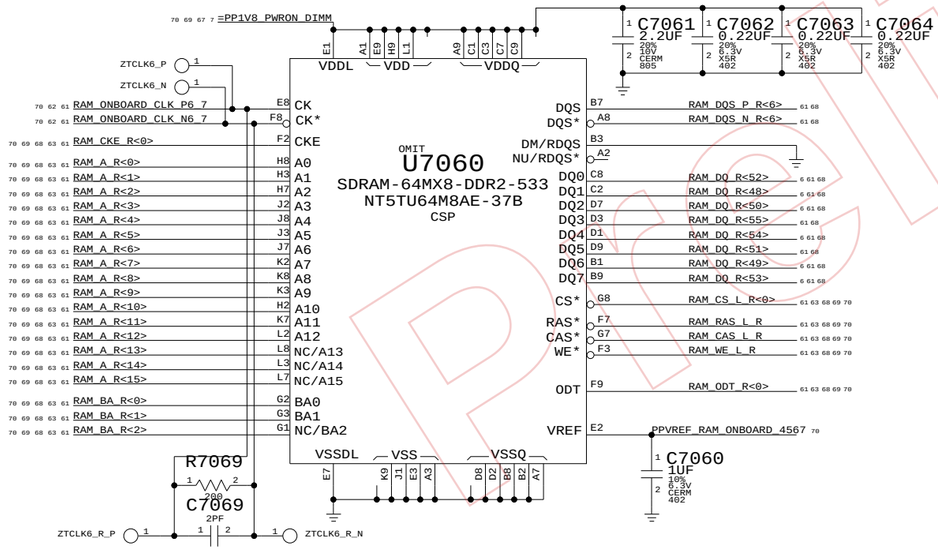
APPLE COMPUTER INC.

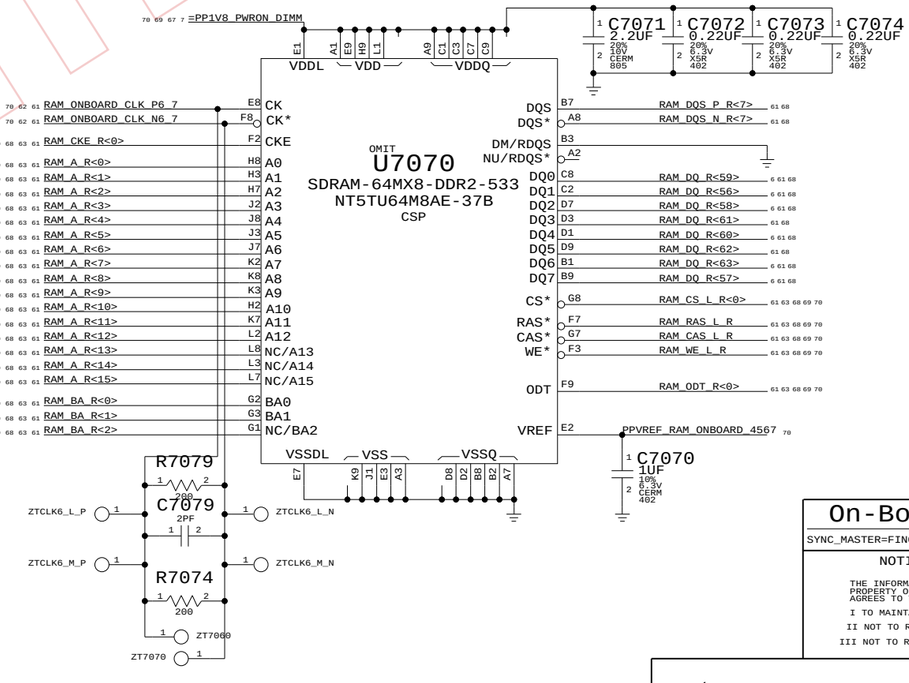
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	69	154









On-Board DDR SDRAM

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 70 OF 154	

KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

82D8 82B7 3C1 82D1 82C8 =PP2V5_PWRON_NB_PCIE

L8200 0.22UH 0805-1

C8200 0.01UF 10% 16V CERM 402 — C8201 10UF 10% 6.3V XSR 805 — C8202 1UF 10% 6.3V CERM 402

PWR_PCIE_A_AVDD_2 82D6 97C4 97D4

97D4 82A6 6A3 KOD_G10_GND (THIS PAGE)

L8201 0.22UH 0805-1

C8203 0.01UF 10% 16V CERM 402 — C8204 10UF 10% 6.3V XSR 805 — C8205 1UF 10% 6.3V CERM 402

PWR_PCIE_A_AVDD_1 82D6 97D4

97D4 82A6 6A3 KOD_K07_GND (THIS PAGE)

L8202 0.22UH 0805-1

C8206 0.01UF 10% 16V CERM 402 — C8207 10UF 10% 6.3V XSR 805 — C8208 1UF 10% 6.3V CERM 402

PWR_PCIE_A_AVDD_0 82D6 97C4 97D4

97D4 82A6 6A3 KOD_H05_GND (THIS PAGE)

97D4 97C4 82D6 PWR_PCIE_A_AVDD_2
97D4 82D6 PWR_PCIE_A_AVDD_1
97D4 97C4 82C6 PWR_PCIE_A_AVDD_0

97D4 PWR_PCIE_A_AVDD_A
97D4 PWR_PCIE_A_AVDD_B
97C4 PWR_PCIE_A_AVDD_C

97D4 PWR_PCIE_A_AVDD

L8203 0.22UH 0805-1

82D8 82C8 3C1 82B7 82D1 =PP2V5_PWRON_NB_PCIE

C8222 1UF 10% 6.3V CERM 402 — C8225 1UF 10% 6.3V CERM 402 — C8223 10UF 10% 6.3V XSR 805 — C8224 0.01UF 10% 16V CERM 402

KOD_L13_GND 6A3 82A3 97D4 (THIS PAGE)

KOD_J13_GND 6A3 82A3 97D4 (THIS PAGE)

L8205 0.22UH 0805-1

82D8 82C8 3C1 82B7 82C8 82D1 82D8 =PP2V5_PWRON_NB_PCIE

C8228 1UF 10% 6.3V CERM 402 — C8229 10UF 10% 6.3V XSR 805 — C8230 0.01UF 10% 16V CERM 402

KOD_H08_GND 6A3 82A3 97D4 (THIS PAGE)

PCIE_AVDD_0 (1.65V-2.75V) SERDES	PCIE_AVDD_1 (1.65V-2.75V) SERDES	PCIE_AVDD_2 (1.65V-2.75V) SERDES	PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL	PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL	PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL
J06	J07	H11	J12	K13	J09

U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE

(1.6V-1.2V)

PCIE_VDD	A04	PCIE_VDD	F02
PCIE_VDD	A08	PCIE_VDD	F05
PCIE_VDD	A12	PCIE_VDD	G08
PCIE_VDD	B06	PCIE_VDD	G12
PCIE_VDD	B10	PCIE_VDD	H01
PCIE_VDD	C03	PCIE_VDD	H04
PCIE_VDD	D01	PCIE_VDD	H07
PCIE_VDD	D04	PCIE_VDD	H10
PCIE_VDD	D08	PCIE_VDD	H14
PCIE_VDD	D12	PCIE_VDD	K12
PCIE_VDD	E06	PCIE_VDD	L11
PCIE_VDD	E10	PCIE_VDD	L14
PCIE_VDD	E14	PCIE_VDD	M12

82B2 82A8 82B2 82C6 82C8 3A4 =PPVCORE_PWRON_NB_PCIE

PCIE_REFCLK_P
PCIE_REFCLK_N (100MHZ)

PCIE_HSIN0	J11	PCIE_HSOP0	E03
PCIE_HSIP0	J10	PCIE_HSON1	J01
PCIE_HSIN1	G05	PCIE_HSOP1	J02
PCIE_HSIP1	G04	PCIE_HSON2	C01
PCIE_HSIN2	G01	PCIE_HSOP2	C02
PCIE_HSIP2	G02	PCIE_HSON3	A07
PCIE_HSIN3	C04	PCIE_HSOP3	B07
PCIE_HSIP3	C05	PCIE_HSON4	F03
PCIE_HSIN4	C07	PCIE_HSOP4	G03
PCIE_HSIP4	C06	PCIE_HSON5	H03
PCIE_HSIN5	E01	PCIE_HSOP5	J03
PCIE_HSIP5	E02	PCIE_HSON6	A03
PCIE_HSIN6	J05	PCIE_HSOP6	B03
PCIE_HSIP6	J04	PCIE_HSON7	A05
PCIE_HSIN7	H06	PCIE_HSOP7	B05
PCIE_HSIP7	G06	PCIE_HSON8	C11
PCIE_HSIN8	E05	PCIE_HSOP8	C10
PCIE_HSIP8	D05	PCIE_HSON9	B11
PCIE_HSIN9	D11	PCIE_HSOP9	A11
PCIE_HSIP9	E11	PCIE_HSON10	F11
PCIE_HSIN10	F12	PCIE_HSOP10	F10
PCIE_HSIP10	F13	PCIE_HSON11	B09
PCIE_HSIN11	H09	PCIE_HSOP11	A09
PCIE_HSIP11	G09	PCIE_HSON12	D13
PCIE_HSIN12	F09	PCIE_HSOP12	E13
PCIE_HSIP12	F08	PCIE_HSON13	B13
PCIE_HSIN13	G13	PCIE_HSOP13	A13
PCIE_HSIP13	H13	PCIE_HSON14	D09
PCIE_HSIN14	C13	PCIE_HSOP14	E09
PCIE_HSIP14	C12	PCIE_HSON15	C08
PCIE_HSIN15	D07	PCIE_HSOP15	C09
PCIE_HSIP15	E07		
PCIE_PRESENTN	G07		
PCIE_UCAL_RES0	F07		
PCIE_UCAL_RES1	AJ02		
	F14		
	J14		

(DNU)

PCIE_AVREG_2	G11	NC_A_AVREG_2	
PCIE_AVREG_1	J08	NC_A_AVREG_1	
PCIE_AVREG_0	E04	NC_A_AVREG_0	

PCIE_GND	A06	PCIE_GND	F04
PCIE_GND	A10	PCIE_GND	F06
PCIE_GND	B02	PCIE_GND	G14
PCIE_GND	B04	PCIE_GND	H02
PCIE_GND	B08	PCIE_GND	H12
PCIE_GND	B12	PCIE_GND	K10
PCIE_GND	D02	PCIE_GND	K14
PCIE_GND	D06	PCIE_GND	L12
PCIE_GND	D10	PCIE_GND	M11
PCIE_GND	D14	PCIE_GND	M13
PCIE_GND	E08		
PCIE_GND	E12		
PCIE_GND	F01		

AVDD_0_GND AVDD_1_GND AVDD_2_GND REFCLK_AGNDA REFCLK_AGNDB REFCLK_AGND2

97D4 82C7 6A3 KOD_H05_GND
97D4 82D7 6A3 KOD_K07_GND
97D4 82D7 6A3 KOD_G10_GND
(THIS PAGE, X3)

XW8200 XW8201 XW8202 XW8203 XW8204 XW8205

KOD_H08_GND 6A3 82C2 97D4
KOD_L13_GND 6A3 82D2 97D4
KOD_J13_GND 6A3 82D2 97D4
(THIS PAGE, X3)

KODIAK PCI-E 100MHZ REFCLK

PP8201 P4MM SM
100+ 97D8 CLK_KOD_100M_PF<0>
100- 97D8 CLK_KOD_100M_NF<0>

PP8200 P4MM SM 82B2 82D2 82A8 3A4 82C6 =PPVCORE_PWRON_NB_PCIE

NOSTUFF R8206 8.2K 5% 1/16W MF-LF 402
R8202 20.5 1% 1/10W MF-LF 402 26C2 97D8 CLK_KOD_100M_P<0> — 97D8 100M_P<0>
C8245 0.01UF 10% 16V CERM 402

NOSTUFF C8244 0.01UF 10% 16V CERM 402 — 100M_G
R8204 29.4 1% 1/16W MF-LF 402
R8205 20.5 1% 1/10W MF-LF 402 26B2 97D8 CLK_KOD_100M_N<0> — 97D8 100M_N<0>
C8246 0.01UF 10% 16V CERM 402
NOSTUFF R8207 8.2K 5% 1/16W MF-LF 402

KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

82D8 82D1 82C8 3C1 =PP2V5_PWRON_NB_PCIE

R8200 8.2K 5% 1/16W MF-LF 402

113C7 84C7 PCIE_SLOTA_PRSNT_L

6A5 PCIE_VCAL_RES0
PCIE_VCAL_RES1

R8201 200 1% 1/16W MF-LF 402

84C3 83C8 97C4	PCIE_SLOTA_TO_NB_N<0>	G05	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_P<0>	G04	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_N<1>	G01	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_P<1>	G02	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_N<2>	C04	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_P<2>	C05	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_N<3>	C07	
84C3 83C8 97C4	PCIE_SLOTA_TO_NB_P<3>	C06	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_N<4>	E01	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_P<4>	E02	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_N<5>	J05	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_P<5>	J04	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_N<6>	H06	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_P<6>	G06	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_N<7>	E05	
84B3 83C8 97B4	PCIE_SLOTA_TO_NB_P<7>	D05	
84A3 83C8 97B4	PCIE_SLOTA_TO_NB_N<8>	D11	
84A3 83C8 97B4	PCIE_SLOTA_TO_NB_P<8>	E11	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<9>	F12	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<9>	F13	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<10>	H09	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<10>	G09	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<11>	F09	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<11>	F08	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<12>	G13	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<12>	H13	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<13>	C13	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<13>	C12	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<14>	D07	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<14>	E07	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_N<15>	G07	
84A3 83B8 97B4	PCIE_SLOTA_TO_NB_P<15>	F07	

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

PCIE_HSON0	D03 97D8	PCIE_NB_TO_SLOTA_NF<0>	0.1UF	C8247	PCIE_NB_TO_SLOTA_N<0>	84C6	97B8
PCIE_HSOP0	E03 97D8	PCIE_NB_TO_SLOTA_PF<0>	0.1UF	C8248	PCIE_NB_TO_SLOTA_P<0>	84C6	97B8
PCIE_HSON1	J01 97D8	PCIE_NB_TO_SLOTA_NF<1>	0.1UF	C8249	PCIE_NB_TO_SLOTA_N<1>	84C6	97B8
PCIE_HSOP1	J02 97D8	PCIE_NB_TO_SLOTA_PF<1>	0.1UF	C8250	PCIE_NB_TO_SLOTA_P<1>	84C6	97B8
PCIE_HSON2	C01 97C8	PCIE_NB_TO_SLOTA_NF<2>	0.1UF	C8251	PCIE_NB_TO_SLOTA_N<2>	84C6	97B8
PCIE_HSOP2	C02 97C8	PCIE_NB_TO_SLOTA_PF<2>	0.1UF	C8252	PCIE_NB_TO_SLOTA_P<2>	84C6	97B8
PCIE_HSON3	A07 97C8	PCIE_NB_TO_SLOTA_NF<3>	0.1UF	C8253	PCIE_NB_TO_SLOTA_N<3>	84C6	97B8
PCIE_HSOP3	B07 97C8	PCIE_NB_TO_SLOTA_PF<3>	0.1UF	C8254	PCIE_NB_TO_SLOTA_P<3>	84C6	97B8
PCIE_HSON4	F03 97C8	PCIE_NB_TO_SLOTA_NF<4>	0.1UF	C8255	PCIE_NB_TO_SLOTA_N<4>	84B6	97B8
PCIE_HSOP4	G03 97C8	PCIE_NB_TO_SLOTA_PF<4>	0.1UF	C8256	PCIE_NB_TO_SLOTA_P<4>	84C6	97B8
PCIE_HSON5	H03 97C8	PCIE_NB_TO_SLOTA_NF<5>	0.1UF	C8257	PCIE_NB_TO_SLOTA_N<5>	84B6	97B8
PCIE_HSOP5	J03 97C8	PCIE_NB_TO_SLOTA_PF<5>	0.1UF	C8258	PCIE_NB_TO_SLOTA_P<5>	84B6	97B8
PCIE_HSON6	A03 97C8	PCIE_NB_TO_SLOTA_NF<6>	0.1UF	C8259	PCIE_NB_TO_SLOTA_N<6>	84B6	97B8
PCIE_HSOP6	B03 97C8	PCIE_NB_TO_SLOTA_PF<6>	0.1UF	C8260	PCIE_NB_TO_SLOTA_P<6>	84B6	97B8
PCIE_HSON7	A05 97C8	PCIE_NB_TO_SLOTA_NF<7>	0.1UF	C8261	PCIE_NB_TO_SLOTA_N<7>	84B6	97B8
PCIE_HSOP7	B05 97C8	PCIE_NB_TO_SLOTA_PF<7>	0.1UF	C8262	PCIE_NB_TO_SLOTA_P<7>	84B6	97B8
PCIE_HSON8	C11 97C8	PCIE_NB_TO_SLOTA_NF<8>	0.1UF	C8263	PCIE_NB_TO_SLOTA_N<8>	84A6	97B8
PCIE_HSOP8	C10 97C8	PCIE_NB_TO_SLOTA_PF<8>	0.1UF	C8264	PCIE_NB_TO_SLOTA_P<8>	84B6	97B8
PCIE_HSON9	B11 97C8	PCIE_NB_TO_SLOTA_NF<9>	0.1UF	C8265	PCIE_NB_TO_SLOTA_N<9>	84B6	97B8
PCIE_HSOP9	A11 97C8	PCIE_NB_TO_SLOTA_PF<9>	0.1UF	C8266	PCIE_NB_TO_SLOTA_P<9>	84B6	97B8
PCIE_HSON10	F11 97C8	PCIE_NB_TO_SLOTA_NF<10>	0.1UF	C8267	PCIE_NB_TO_SLOTA_N<10>	84B6	97B8
PCIE_HSOP10	F10 97C8	PCIE_NB_TO_SLOTA_PF<10>	0.1UF	C8268	PCIE_NB_TO_SLOTA_P<10>	84B6	97B8
PCIE_HSON11	B09 97C8	PCIE_NB_TO_SLOTA_NF<11>	0.1UF	C8269	PCIE_NB_TO_SLOTA_N<11>	84A6	97B8
PCIE_HSOP11	A09 97C8	PCIE_NB_TO_SLOTA_PF<11>	0.1UF	C8270	PCIE_NB_TO_SLOTA_P<11>	84A6	97A8
PCIE_HSON12	D13 97C8	PCIE_NB_TO_SLOTA_NF<12>	0.1UF	C8271	PCIE_NB_TO_SLOTA_N<12>	84A6	97A8
PCIE_HSOP12	E13 97C8	PCIE_NB_TO_SLOTA_PF<12>	0.1UF	C8272	PCIE_NB_TO_SLOTA_P<12>	84A6	97A8
PCIE_HSON13	B13 97C8	PCIE_NB_TO_SLOTA_NF<13>	0.1UF	C8273	PCIE_NB_TO_SLOTA_N<13>	84A6	97A8
PCIE_HSOP13	A13 97C8	PCIE_NB_TO_SLOTA_PF<13>	0.1UF	C8274	PCIE_NB_TO_SLOTA_P<13>	84A6	97A8
PCIE_HSON14	D09 97C8	PCIE_NB_TO_SLOTA_NF<14>	0.1UF	C8275	PCIE_NB_TO_SLOTA_N<14>	84A6	97A8
PCIE_HSOP14	E09 97C8	PCIE_NB_TO_SLOTA_PF<14>	0.1UF	C8276	PCIE_NB_TO_SLOTA_P<14>	84A6	97A8
PCIE_HSON15	C08 97B8	PCIE_NB_TO_SLOTA_NF<15>	0.1UF	C8277	PCIE_NB_TO_SLOTA_N<15>	84A6	97A8
PCIE_HSOP15	C09 97B8	PCIE_NB_TO_SLOTA_PF<15>	0.1UF	C8278	PCIE_NB_TO_SLOTA_P<15>	84A6	97A8

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

=PPVCORE_PWRON_NB_PCIE 3A4 82B2 82C2 82C6 82C8

C8209 C8210 C8211 C8212
C8213 C8214 C8215 C8216
C8217 C8218 C8219 C8220 C8221
1UF 10% 6.3V CERM 402

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

=PPVCORE_PWRON_NB_PCIE 3A4 82A8 82C2 82C6 82C8

C8231 C8232 C8233 C8234 C8235 C8236
C8241 C8242 C8243 C8237 C8238 C8239 C8240
1UF 10% 6.3V CERM 402

KODIAK PCI-E X16

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 82 OF 154	

DRAWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT
338S0244	1	IC,RV380 XT, GRAPHICS CTLR	U8400	RV380XT

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

=PP1V2_GPU_PCIE
THIS SHOULD BE ALIASED TO PPVCORE_GPU WITH RV370 AND PP1V2_RUN WITH RV380

L8460 1.8UH 0805
L8461 1.8UH 0805

PP1V2_GPU_PCIE_VDDR
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8460 C8461 C8462 C8463 C8464 C8465 C8466 1UF 10% 6.3V CERM 402 / 0.1UF 20% 10V CERM 402

PP1V2_GPU_PCIE_PVDD

C8450 C8451 1UF 10% 6.3V CERM 402
C8452 C8453 C8454 C8455 0.1UF 20% 10V CERM 402

SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN

=PP1V8_GPU

L8440 1.8UH 0805

PP1V8_GPU_PCIE_PVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8440 C8441 1UF 10% 6.3V CERM 402
C8442 C8443 C8444 C8445 0.1UF 20% 10V CERM 402

PLACE R8470 CLOSE TO U9670

=GPU_RESET_L
U9670 74LCX125 TSSOP
ATI_RESET_L
R8470 33 5% 1/10W MF-LF 402
R8469 8.2K 5% 1/16W MF-LF 402

PERST* AD25 ATI_RESET_L_R

PP1V2_GPU_PCIE_PVDD

R8471 301 1% 1/16W MF-LF 402
R8472 21 1% 1/16W MF-LF 402
R8473 21 1% 1/16W MF-LF 402
R8474 60.4 1% 1/16W MF-LF 402
R8475 21 1% 1/16W MF-LF 402
R8476 60.4 1% 1/16W MF-LF 402
R8477 21 1% 1/16W MF-LF 402
R8478 301 1% 1/16W MF-LF 402

CKA_PCIE_P<0>
CKA_PCIE_N<0>
C8472 5PF +/-0.25PF 50V CERM 402
C8473 5PF +/-0.25PF 50V CERM 402

CLK_PCIE_SLOTA_P<0>
CLK_PCIE_SLOTA_N<0>

PP1V2_GPU_PCIE_PVDD

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

U8400
RV370XT
BGA
(1 OF 5)
OMIT
PCI-E

CLK_PCIE_SLOTA_PF<0>	AF27	PCIE_REFCLKP
CLK_PCIE_SLOTA_NF<0>	AE27	PCIE_REFCLKN
PCIE_NB_TO_SLOTA_P<0>	AH30	PCIE_RX0P
PCIE_NB_TO_SLOTA_N<0>	AG30	PCIE_RX0N
PCIE_NB_TO_SLOTA_P<1>	AG29	PCIE_RX1P
PCIE_NB_TO_SLOTA_N<1>	AF29	PCIE_RX1N
PCIE_NB_TO_SLOTA_P<2>	AE29	PCIE_RX2P
PCIE_NB_TO_SLOTA_N<2>	AE30	PCIE_RX2N
PCIE_NB_TO_SLOTA_P<3>	AD30	PCIE_RX3P
PCIE_NB_TO_SLOTA_N<3>	AD29	PCIE_RX3N
PCIE_NB_TO_SLOTA_P<4>	AC29	PCIE_RX4P
PCIE_NB_TO_SLOTA_N<4>	AB29	PCIE_RX4N
PCIE_NB_TO_SLOTA_P<5>	AB30	PCIE_RX5P
PCIE_NB_TO_SLOTA_N<5>	AA30	PCIE_RX5N
PCIE_NB_TO_SLOTA_P<6>	AA29	PCIE_RX6P
PCIE_NB_TO_SLOTA_N<6>	Y29	PCIE_RX6N
PCIE_NB_TO_SLOTA_P<7>	W29	PCIE_RX7P
PCIE_NB_TO_SLOTA_N<7>	W30	PCIE_RX7N
PCIE_NB_TO_SLOTA_P<8>	V30	PCIE_RX8P
PCIE_NB_TO_SLOTA_N<8>	V29	PCIE_RX8N
PCIE_NB_TO_SLOTA_P<9>	U29	PCIE_RX9P
PCIE_NB_TO_SLOTA_N<9>	T29	PCIE_RX9N
PCIE_NB_TO_SLOTA_P<10>	T30	PCIE_RX10P
PCIE_NB_TO_SLOTA_N<10>	R30	PCIE_RX10N
PCIE_NB_TO_SLOTA_P<11>	R29	PCIE_RX11P
PCIE_NB_TO_SLOTA_N<11>	P29	PCIE_RX11N
PCIE_NB_TO_SLOTA_P<12>	N29	PCIE_RX12P
PCIE_NB_TO_SLOTA_N<12>	N30	PCIE_RX12N
PCIE_NB_TO_SLOTA_P<13>	M30	PCIE_RX13P
PCIE_NB_TO_SLOTA_N<13>	M29	PCIE_RX13N
PCIE_NB_TO_SLOTA_P<14>	L29	PCIE_RX14P
PCIE_NB_TO_SLOTA_N<14>	K29	PCIE_RX14N
PCIE_NB_TO_SLOTA_P<15>	K30	PCIE_RX15P
PCIE_NB_TO_SLOTA_N<15>	J30	PCIE_RX15N

PCIE_PVDD_18: T23 U23 V23 W23
PCIE_PVDD_12: N23 N24 P23
PCIE_VDDR_12: AG26 AG27 AG28 AJ30 AK29

R8400 100 1% 1/16W MF-LF 402
PP1V2_GPU_PCIE_VDDR

GPU_PCIE_CALRN	AB24	PCIE_CALRN
GPU_PCIE_CALRP	AC23	PCIE_CALRP

R8401 150 1% 1/16W MF-LF 402

PCIE_VSS: K28 L28 M24 M25 M26 M27 M28 N28 P28 R23
PCIE_VSS: R24 R25 R26 R27 R28 T24 T28 U28 V24 V25 V26 V27 V28 W24 W28 Y28 AA23 AA24 AA25 AA26 AA27
PCIE_VSS: AH29 AF28 AE28 AD28 AD27 AD26 AD24 AC28 AB28 AA28

PCIE_CALI	AB23	GPU_PCIE_CALI
PCIE_TEST	AE25	GPU_PCIE_TEST

R8402 10K 1% 1/16W MF-LF 402
R8403 10K 1% 1/16W MF-LF 402

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

PCIE_TX0P	AE26	PCIE_SLOTA_TO_NB_PF<0>	0.1UF	C8400	PCIE_SLOTA_TO_NB_P<0>
PCIE_TX0N	AE26	PCIE_SLOTA_TO_NB_NF<0>	0.1UF	C8401	PCIE_SLOTA_TO_NB_N<0>
PCIE_TX1P	AC25	PCIE_SLOTA_TO_NB_PF<1>	0.1UF	C8402	PCIE_SLOTA_TO_NB_P<1>
PCIE_TX1N	AB25	PCIE_SLOTA_TO_NB_NF<1>	0.1UF	C8403	PCIE_SLOTA_TO_NB_N<1>
PCIE_TX2P	AC27	PCIE_SLOTA_TO_NB_PF<2>	0.1UF	C8404	PCIE_SLOTA_TO_NB_P<2>
PCIE_TX2N	AB27	PCIE_SLOTA_TO_NB_NF<2>	0.1UF	C8405	PCIE_SLOTA_TO_NB_N<2>
PCIE_TX3P	AC26	PCIE_SLOTA_TO_NB_PF<3>	0.1UF	C8406	PCIE_SLOTA_TO_NB_P<3>
PCIE_TX3N	AB26	PCIE_SLOTA_TO_NB_NF<3>	0.1UF	C8407	PCIE_SLOTA_TO_NB_N<3>
PCIE_TX4P	Y25	PCIE_SLOTA_TO_NB_PF<4>	0.1UF	C8408	PCIE_SLOTA_TO_NB_P<4>
PCIE_TX4N	W25	PCIE_SLOTA_TO_NB_NF<4>	0.1UF	C8409	PCIE_SLOTA_TO_NB_N<4>
PCIE_TX5P	Y27	PCIE_SLOTA_TO_NB_PF<5>	0.1UF	C8410	PCIE_SLOTA_TO_NB_P<5>
PCIE_TX5N	W27	PCIE_SLOTA_TO_NB_NF<5>	0.1UF	C8411	PCIE_SLOTA_TO_NB_N<5>
PCIE_TX6P	Y26	PCIE_SLOTA_TO_NB_PF<6>	0.1UF	C8412	PCIE_SLOTA_TO_NB_P<6>
PCIE_TX6N	W26	PCIE_SLOTA_TO_NB_NF<6>	0.1UF	C8413	PCIE_SLOTA_TO_NB_N<6>
PCIE_TX7P	U25	PCIE_SLOTA_TO_NB_PF<7>	0.1UF	C8414	PCIE_SLOTA_TO_NB_P<7>
PCIE_TX7N	T25	PCIE_SLOTA_TO_NB_NF<7>	0.1UF	C8415	PCIE_SLOTA_TO_NB_N<7>
PCIE_TX8P	U27	PCIE_SLOTA_TO_NB_PF<8>	0.1UF	C8416	PCIE_SLOTA_TO_NB_P<8>
PCIE_TX8N	T27	PCIE_SLOTA_TO_NB_NF<8>	0.1UF	C8417	PCIE_SLOTA_TO_NB_N<8>
PCIE_TX9P	U26	PCIE_SLOTA_TO_NB_PF<9>	0.1UF	C8418	PCIE_SLOTA_TO_NB_P<9>
PCIE_TX9N	T26	PCIE_SLOTA_TO_NB_NF<9>	0.1UF	C8419	PCIE_SLOTA_TO_NB_N<9>
PCIE_TX10P	P25	PCIE_SLOTA_TO_NB_PF<10>	0.1UF	C8420	PCIE_SLOTA_TO_NB_P<10>
PCIE_TX10N	N25	PCIE_SLOTA_TO_NB_NF<10>	0.1UF	C8421	PCIE_SLOTA_TO_NB_N<10>
PCIE_TX11P	P27	PCIE_SLOTA_TO_NB_PF<11>	0.1UF	C8422	PCIE_SLOTA_TO_NB_P<11>
PCIE_TX11N	N27	PCIE_SLOTA_TO_NB_NF<11>	0.1UF	C8423	PCIE_SLOTA_TO_NB_N<11>
PCIE_TX12P	P26	PCIE_SLOTA_TO_NB_PF<12>	0.1UF	C8424	PCIE_SLOTA_TO_NB_P<12>
PCIE_TX12N	N26	PCIE_SLOTA_TO_NB_NF<12>	0.1UF	C8425	PCIE_SLOTA_TO_NB_N<12>
PCIE_TX13P	L25	PCIE_SLOTA_TO_NB_PF<13>	0.1UF	C8426	PCIE_SLOTA_TO_NB_P<13>
PCIE_TX13N	K25	PCIE_SLOTA_TO_NB_NF<13>	0.1UF	C8427	PCIE_SLOTA_TO_NB_N<13>
PCIE_TX14P	L27	PCIE_SLOTA_TO_NB_PF<14>	0.1UF	C8428	PCIE_SLOTA_TO_NB_P<14>
PCIE_TX14N	K27	PCIE_SLOTA_TO_NB_NF<14>	0.1UF	C8429	PCIE_SLOTA_TO_NB_N<14>
PCIE_TX15P	L26	PCIE_SLOTA_TO_NB_PF<15>	0.1UF	C8430	PCIE_SLOTA_TO_NB_P<15>
PCIE_TX15N	K26	PCIE_SLOTA_TO_NB_NF<15>	0.1UF	C8431	PCIE_SLOTA_TO_NB_N<15>

GROUND VIAS FOR LAYER TRANSITIONS

ZH8400 HOLE-VIA
ZH8401 HOLE-VIA
ZH8402 HOLE-VIA
ZH8403 HOLE-VIA
ZH8404 HOLE-VIA
ZH8405 HOLE-VIA
ZH8406 HOLE-VIA
ZH8407 HOLE-VIA
ZH8408 HOLE-VIA
ZH8409 HOLE-VIA
ZH8410 HOLE-VIA
ZH8411 HOLE-VIA
ZH8412 HOLE-VIA
ZH8413 HOLE-VIA
ZH8414 HOLE-VIA
ZH8415 HOLE-VIA
ZH8416 HOLE-VIA
ZH8417 HOLE-VIA
ZH8418 HOLE-VIA
ZH8419 HOLE-VIA

XW8405 SM
PCIE_SLOTA_PRSNT_L

GPU PCIe

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 84 OF 154	

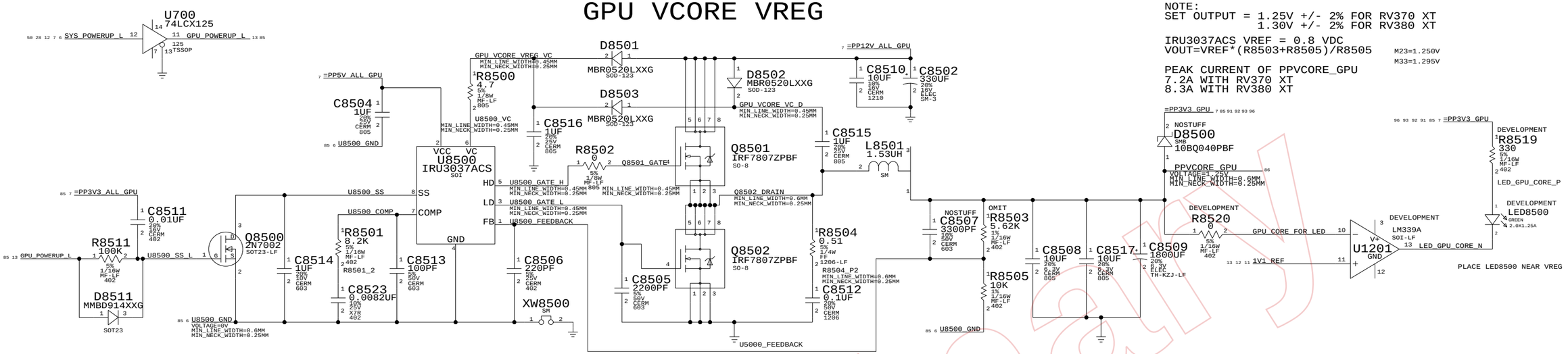
GPU VCORE VREG

NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505

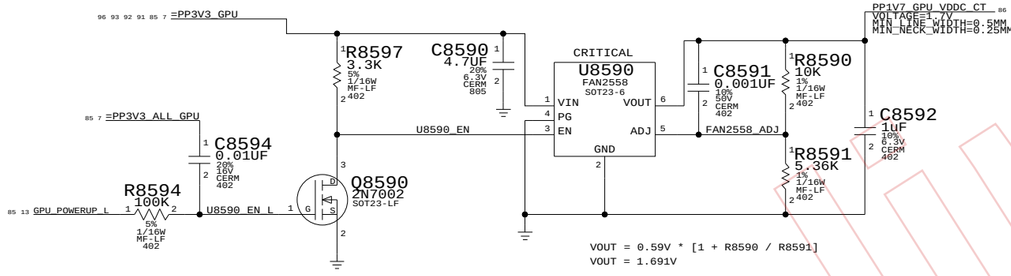
M23=1.250V
M33=1.295V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

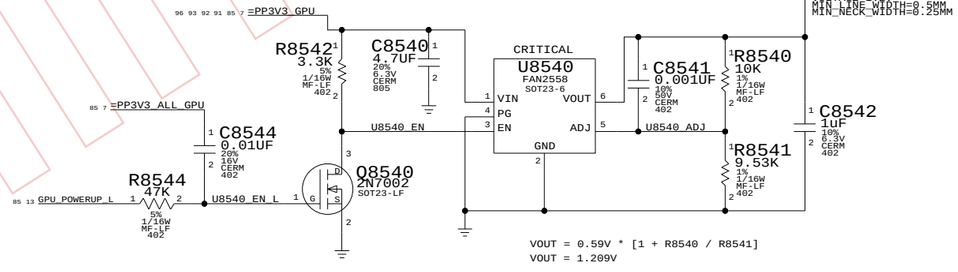


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0291	1	RES,5.62K OHM,1/16W,1%,0402	R8503	RV370XT
114S0295	1	RES,6.19K OHM,1/16W,1%,0402	R8503	RV380XT

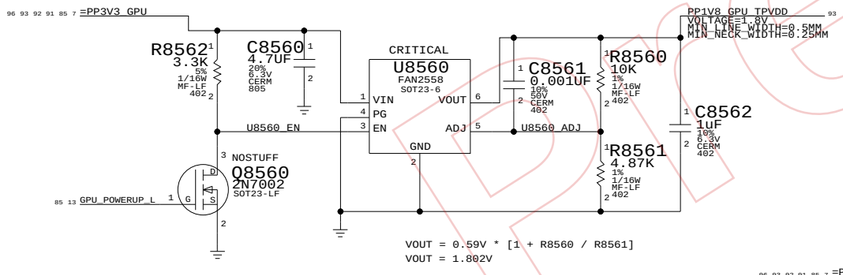
GPU 1.7V VDDC_CT



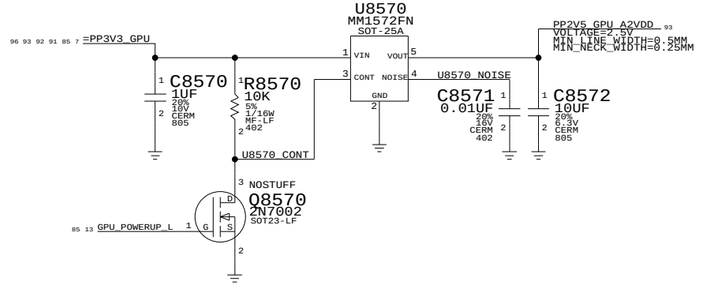
GPU 1.20V PCIE PVDD



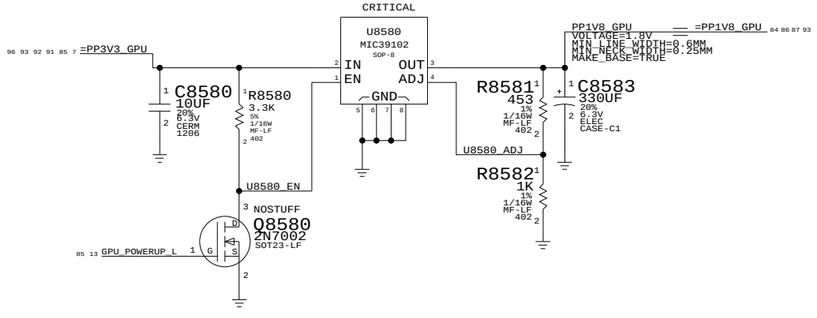
GPU 1.80V TPVDD



GPU 2.5V A2VDD



GPU 1.8V VREG



POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

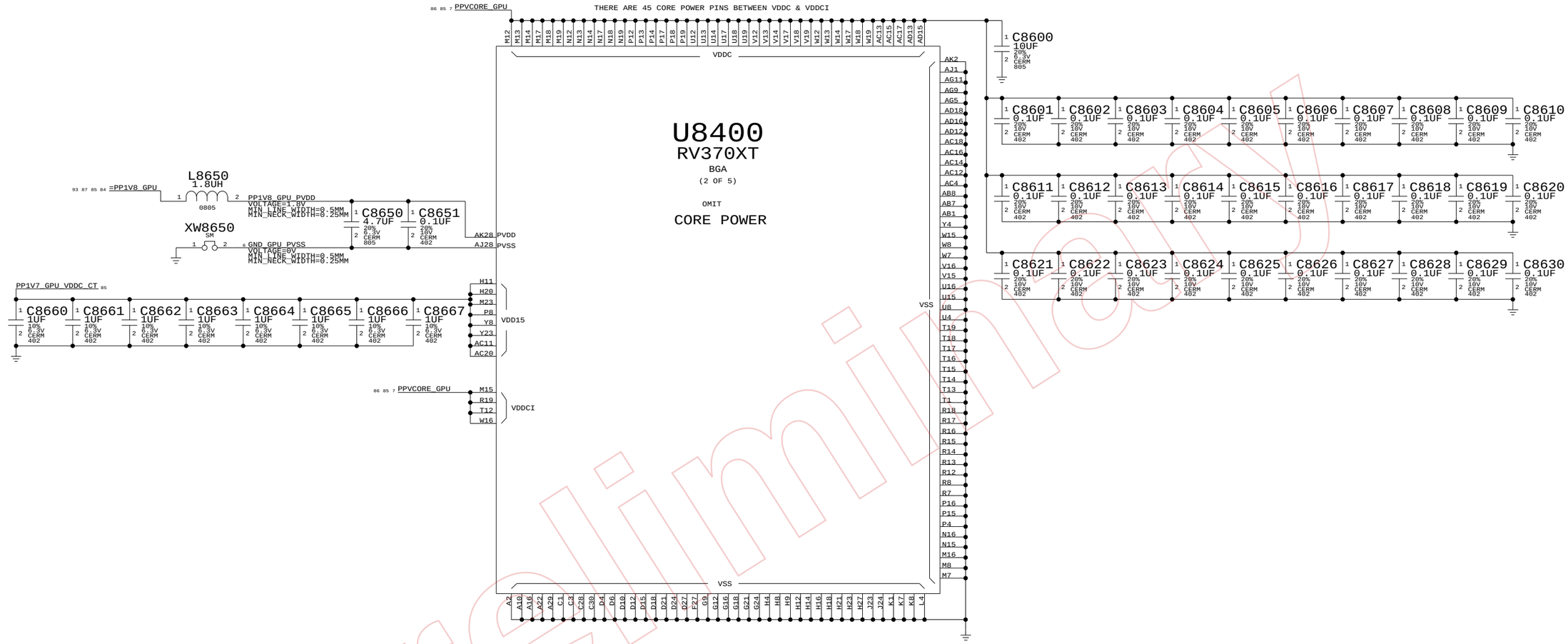
Graphics Vregs

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT 85 OF 154



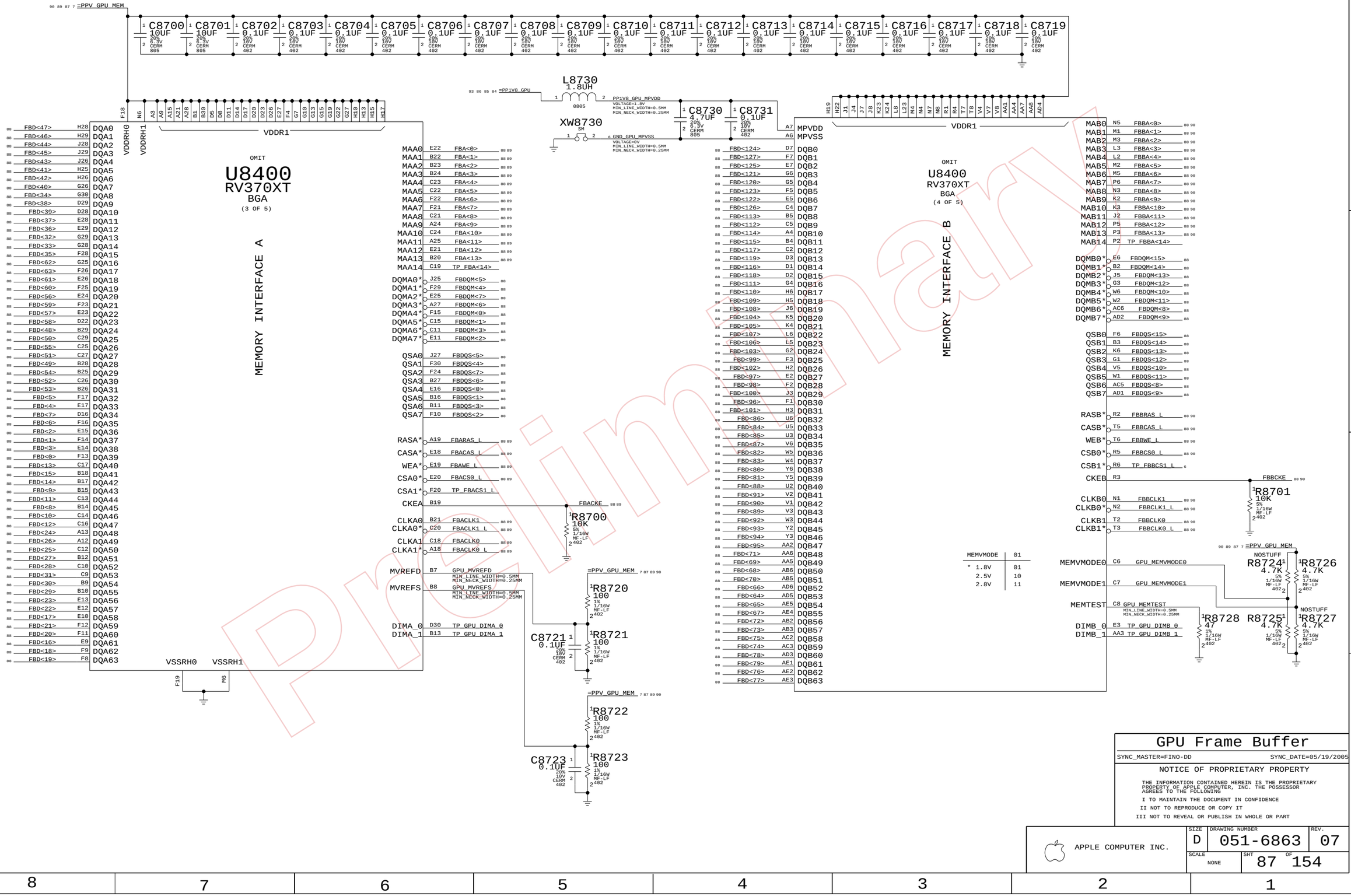
GPU Core Power

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	86	154


=PPV_GPU_MEM
C8700 10UF 20% 6.3V CERM 805
C8701 10UF 20% 6.3V CERM 805
C8702 0.1UF 20% 10V CERM 402
C8703 0.1UF 20% 10V CERM 402
C8704 0.1UF 20% 10V CERM 402
C8705 0.1UF 20% 10V CERM 402
C8706 0.1UF 20% 10V CERM 402
C8707 0.1UF 20% 10V CERM 402
C8708 0.1UF 20% 10V CERM 402
C8709 0.1UF 20% 10V CERM 402
C8710 0.1UF 20% 10V CERM 402
C8711 0.1UF 20% 10V CERM 402
C8712 0.1UF 20% 10V CERM 402
C8713 0.1UF 20% 10V CERM 402
C8714 0.1UF 20% 10V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8716 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8719 0.1UF 20% 10V CERM 402
L8730 1.8UH 0805
=PP1V8_GPU
PP1V8_GPU_MPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C8730 4.7UF 20% 6.3V CERM 805
C8731 0.1UF 20% 10V CERM 402
XW8730 SM
GND_GPU_MPVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
VDDR1
OMIT
U8400
RV370XT
BGA
(3 OF 5)
MEMORY INTERFACE A
DQA0 DQA1 DQA2 DQA3 DQA4 DQA5 DQA6 DQA7 DQA8 DQA9 DQA10 DQA11 DQA12 DQA13 DQA14 DQA15 DQA16 DQA17 DQA18 DQA19 DQA20 DQA21 DQA22 DQA23 DQA24 DQA25 DQA26 DQA27 DQA28 DQA29 DQA30 DQA31 DQA32 DQA33 DQA34 DQA35 DQA36 DQA37 DQA38 DQA39 DQA40 DQA41 DQA42 DQA43 DQA44 DQA45 DQA46 DQA47 DQA48 DQA49 DQA50 DQA51 DQA52 DQA53 DQA54 DQA55 DQA56 DQA57 DQA58 DQA59 DQA60 DQA61 DQA62 DQA63
VDDRH0 VDDRH1
VSSRH0 VSSRH1
MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14
DQMA0* DQMA1* DQMA2* DQMA3* DQMA4* DQMA5* DQMA6* DQMA7*
QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
RASA* CASA* WEA*
CSA0* CSA1*
CKEA
CLKA0 CLKA0* CLKA1 CLKA1*
MVREFD MVREFS
DIMA_0 DIMA_1
R8700 10K 5% 1/16W MF-LF 402
R8720 100 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
R8722 100 1% 1/16W MF-LF 402
R8723 100 1% 1/16W MF-LF 402
C8721 0.1UF 20% 10V CERM 402
C8723 0.1UF 20% 10V CERM 402
OMIT
U8400
RV370XT
BGA
(4 OF 5)
MEMORY INTERFACE B
MPVDD MPVSS
DQB0 DQB1 DQB2 DQB3 DQB4 DQB5 DQB6 DQB7 DQB8 DQB9 DQB10 DQB11 DQB12 DQB13 DQB14 DQB15 DQB16 DQB17 DQB18 DQB19 DQB20 DQB21 DQB22 DQB23 DQB24 DQB25 DQB26 DQB27 DQB28 DQB29 DQB30 DQB31 DQB32 DQB33 DQB34 DQB35 DQB36 DQB37 DQB38 DQB39 DQB40 DQB41 DQB42 DQB43 DQB44 DQB45 DQB46 DQB47 DQB48 DQB49 DQB50 DQB51 DQB52 DQB53 DQB54 DQB55 DQB56 DQB57 DQB58 DQB59 DQB60 DQB61 DQB62 DQB63
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13 MAB14
DQMB0* DQMB1* DQMB2* DQMB3* DQMB4* DQMB5* DQMB6* DQMB7*
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
RASB* CASB* WEB*
CSB0* CSB1*
CKEB
CLKB0 CLKB0* CLKB1 CLKB1*
MEMVMODE0 MEMVMODE1 MEMTEST
DIMB_0 DIMB_1
R8701 10K 5% 1/16W MF-LF 402
R8724 4.7K 5% 1/16W MF-LF 402
R8726 4.7K 5% 1/16W MF-LF 402
R8725 4.7K 5% 1/16W MF-LF 402
R8727 4.7K 5% 1/16W MF-LF 402
R8728 47 1% 1/16W MF-LF 402
NOSTUFF
MEMVMODE | 01
* 1.8V | 01
2.5V | 10
2.8V | 11
GPU Frame Buffer
SYNC_MASTER=FINO-DD
SYNC_DATE=05/19/2005
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FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

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FBD<22>	22	3	6	RP8827	RFBD<22>
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FBDQM<3>	22	1	R8833
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FBDQM<5>	22	1	R8835
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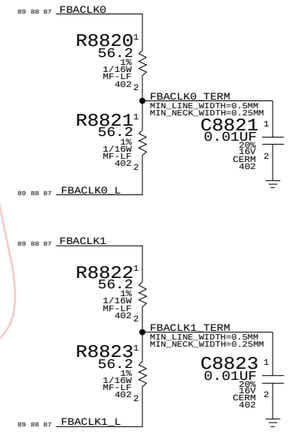
PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION



FRAME BUFFER B TERMINATION

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FBA<13..0>	GPU_FB	GPU_FB	
FBBA<13..0>	GPU_FB	GPU_FB	
FBDQM<15..0>	GPU_FB	GPU_FB	
FBDQS<15..0>	GPU_FB	GPU_FBDQS	
FBARAS_L	GPU_FB	GPU_FB	
FBACAS_L	GPU_FB	GPU_FB	
FBAWE_L	GPU_FB	GPU_FB	
FBACS0_L	GPU_FB	GPU_FB	
FBACKE	GPU_FB	GPU_FB	
FBBRAS_L	GPU_FB	GPU_FB	
FBBCAS_L	GPU_FB	GPU_FB	
FBBWE_L	GPU_FB	GPU_FB	
FBBCS0_L	GPU_FB	GPU_FB	
FBBCKE	GPU_FB	GPU_FB	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBACLK0	GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L	GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1	GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L	GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0	GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L	GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1	GPU_FBCLK	GPU_FBCLK	FBBCLK1
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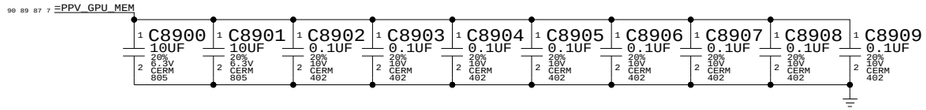
FB Series Termination

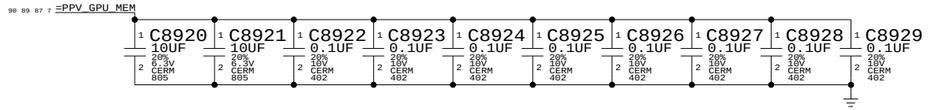
SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

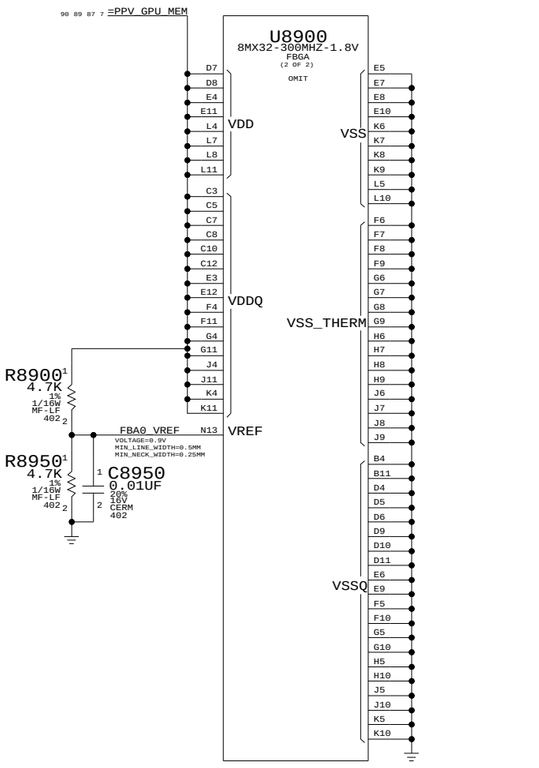
APPLE COMPUTER INC.

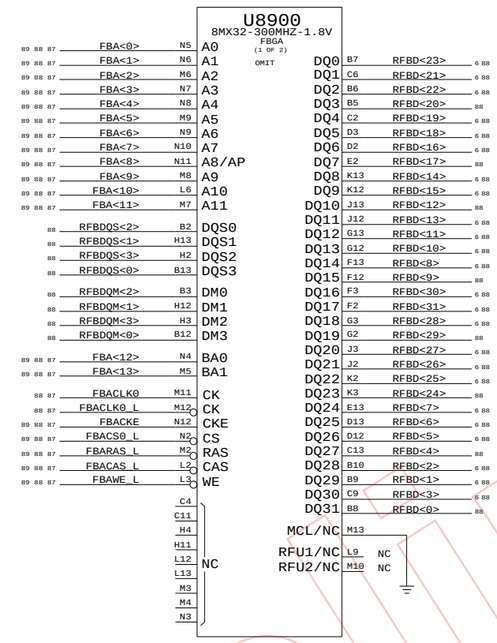
SIZE	DRAWING NUMBER	REV.
D	051-6863	07

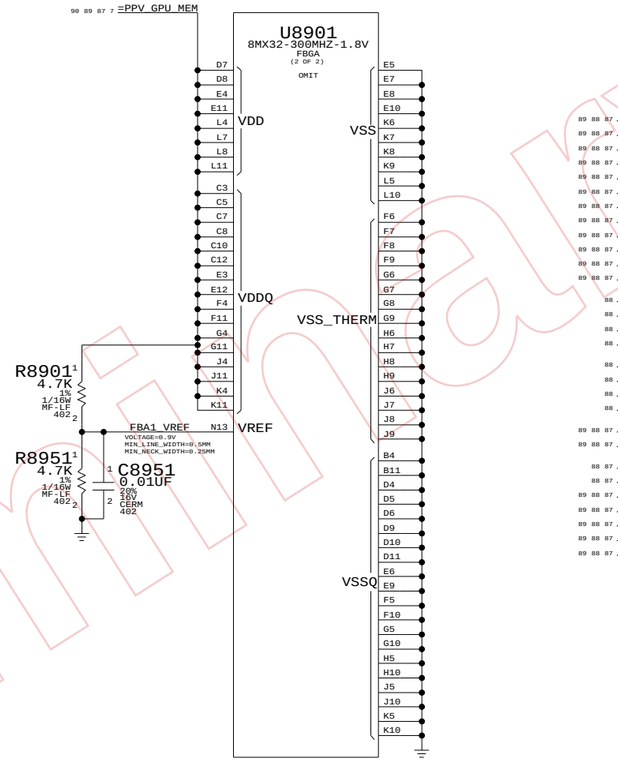
SCALE	SHT	OF
NONE	88	154

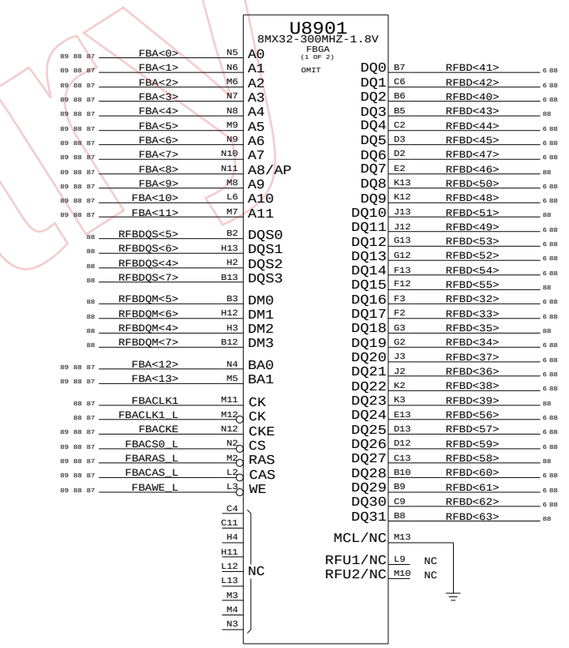


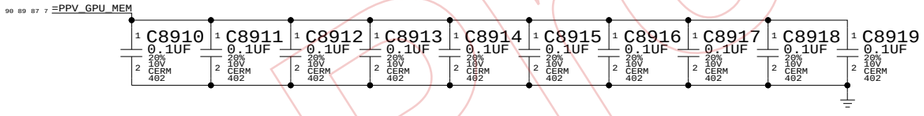


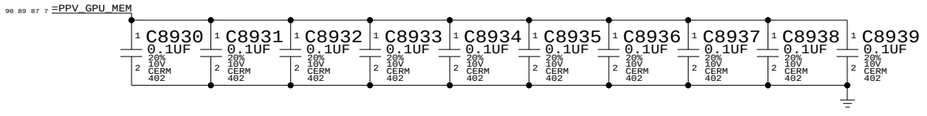


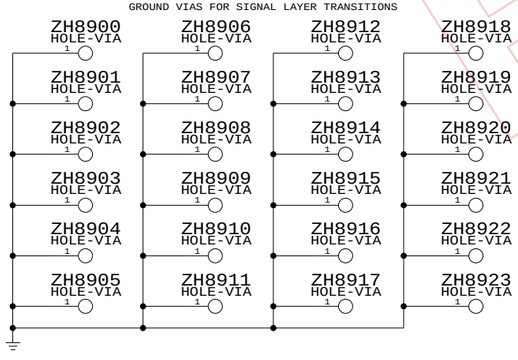












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM A

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

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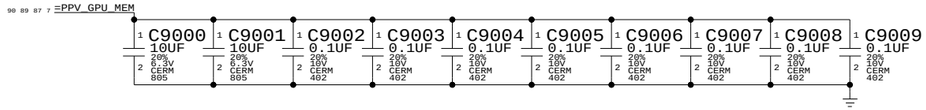
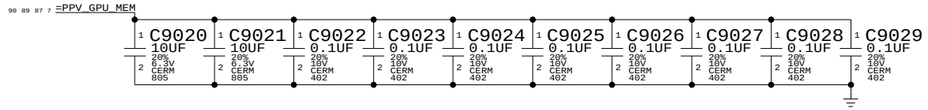
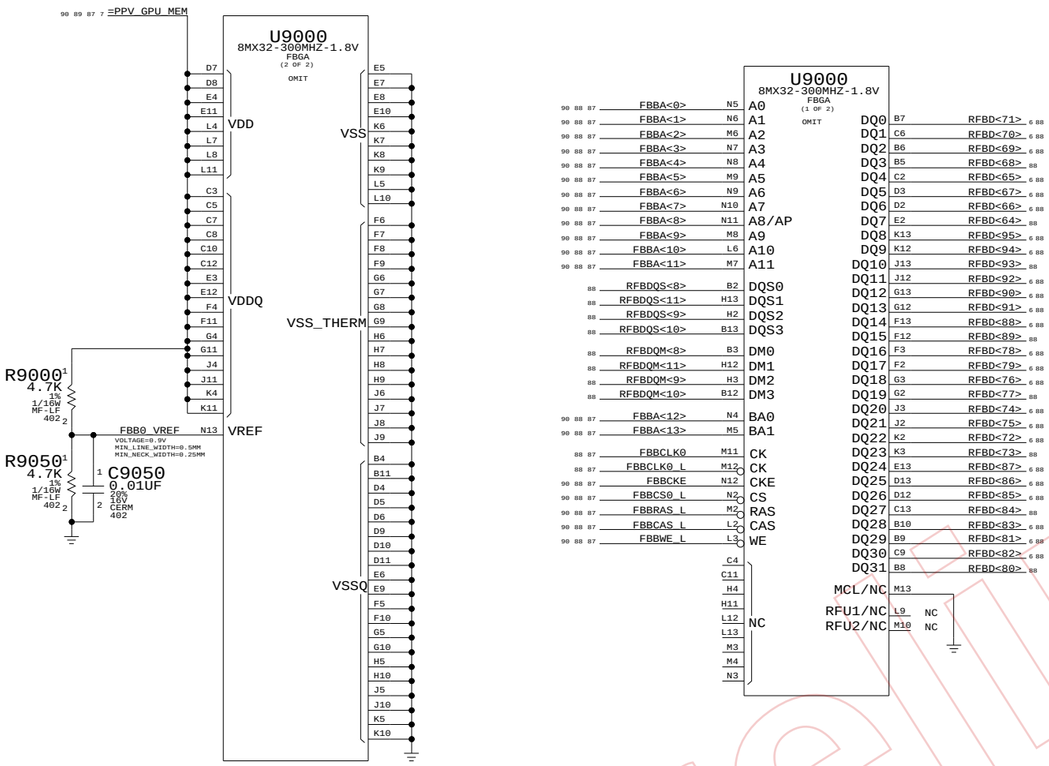
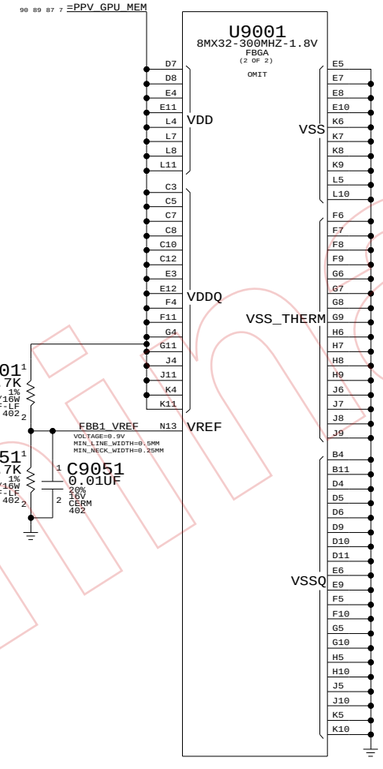
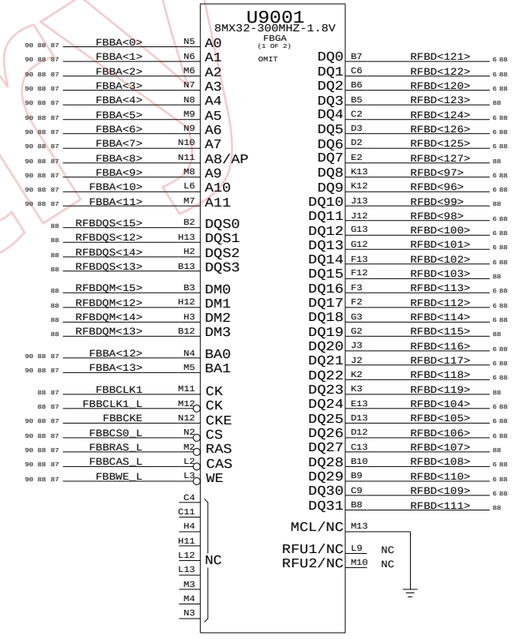
SCALE: NONE	SHT 89 OF 154	

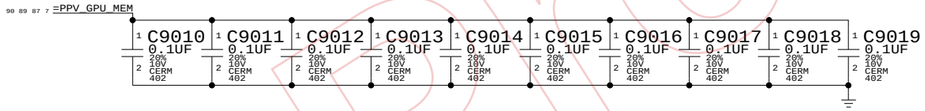


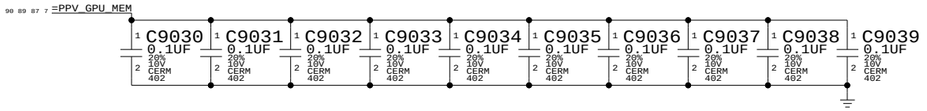


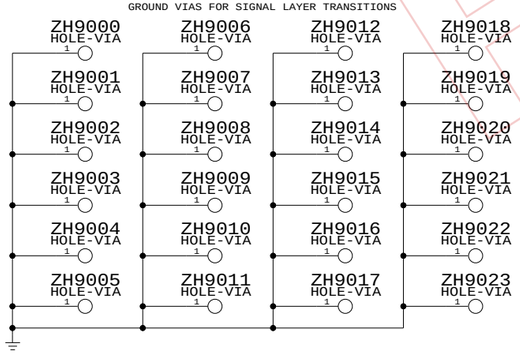












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
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333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

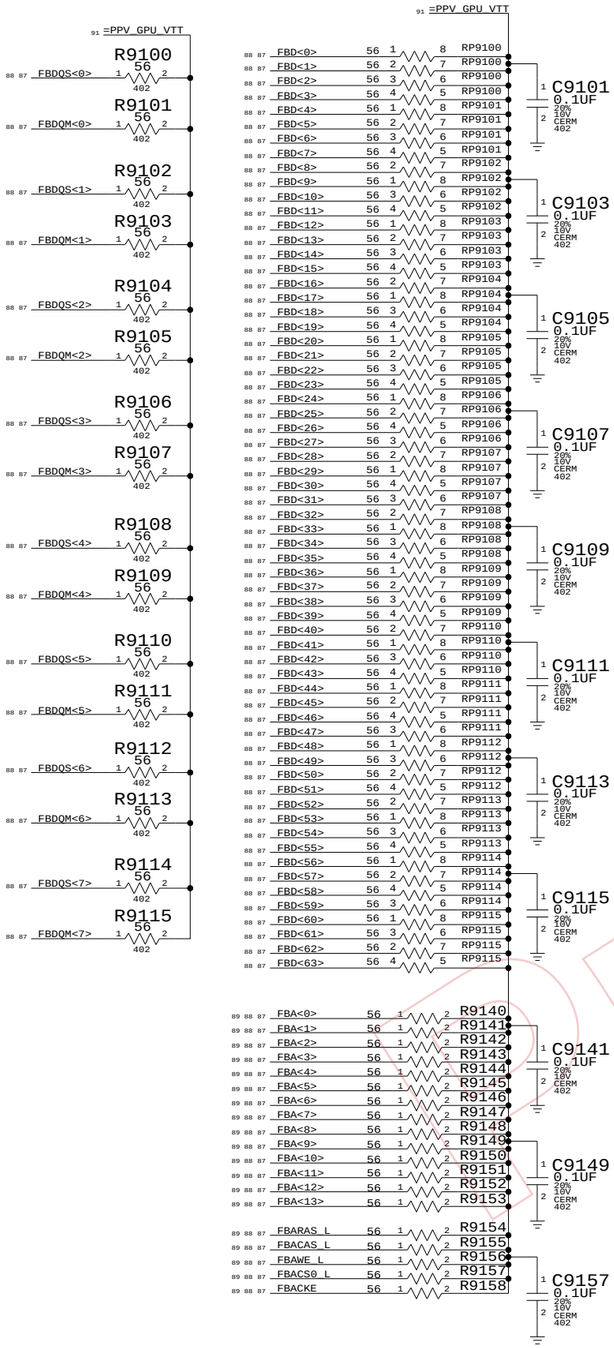
GPU GDDR SDRAM B

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

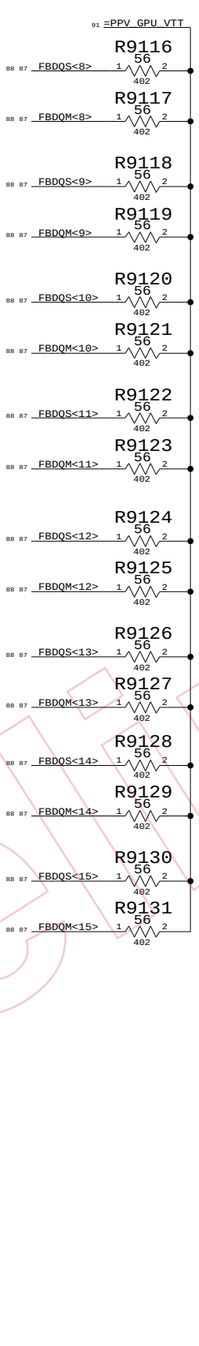
APPLE COMPUTER INC.

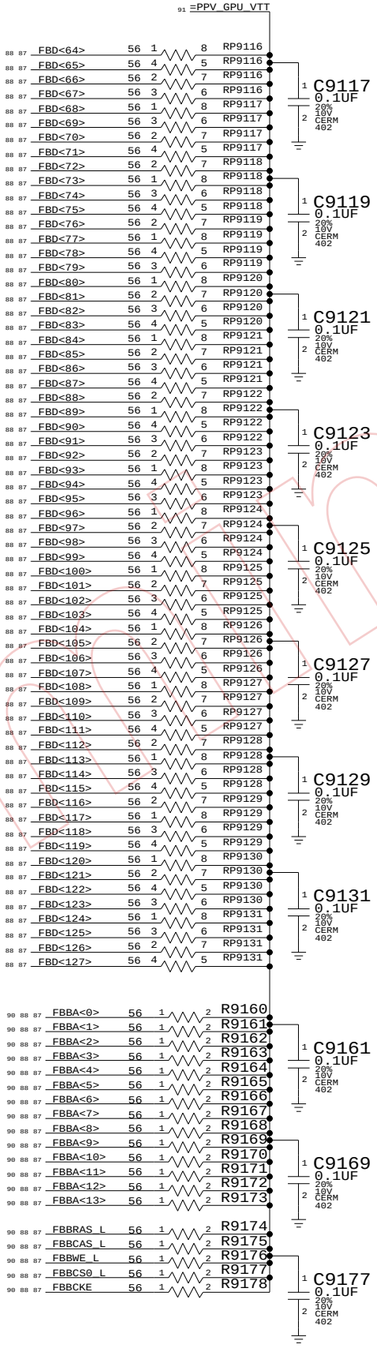
SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 90 OF 154	

FRAME BUFFER A TERMINATION

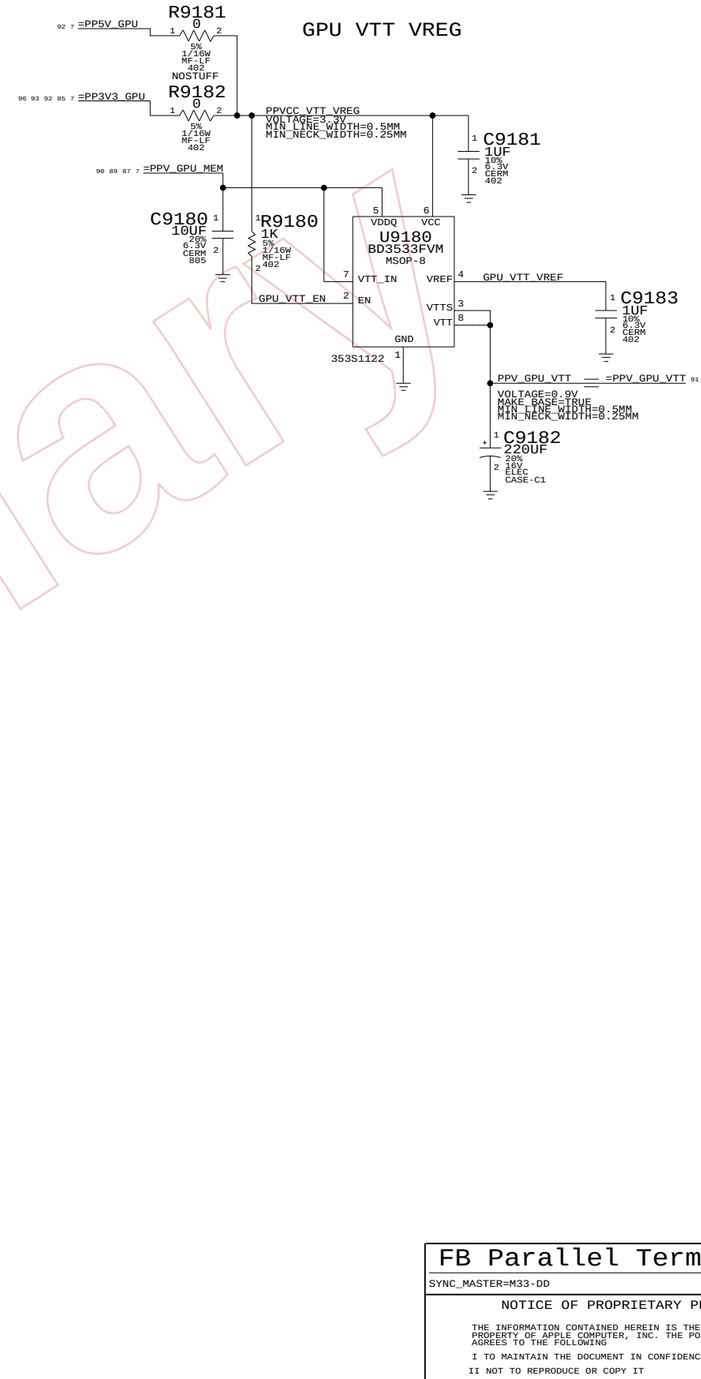


FRAME BUFFER B TERMINATION





GPU VTT VREG



FB Parallel Termination

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

APPLE COMPUTER INC.

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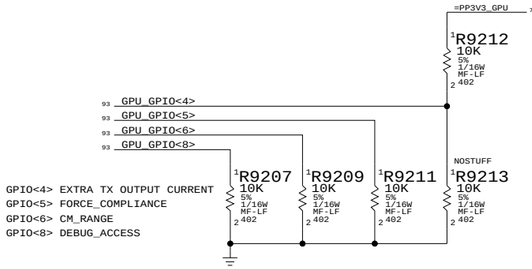
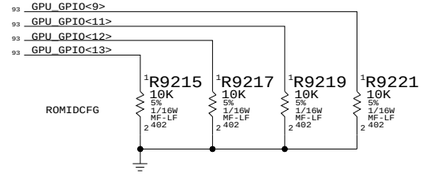
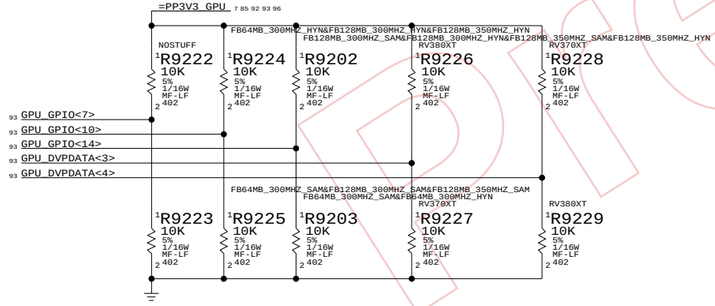
ATI STRAPS



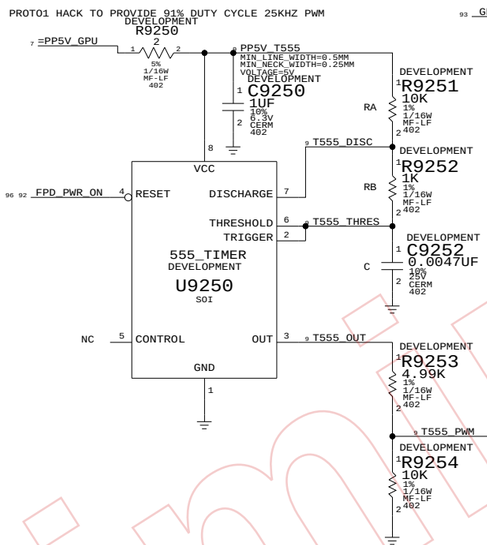


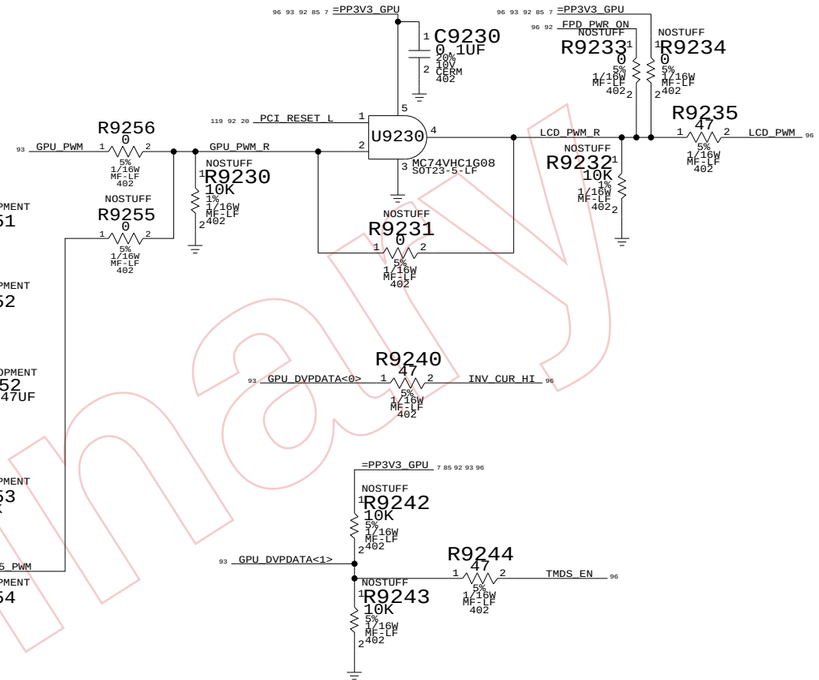
MEMORY STRAPS

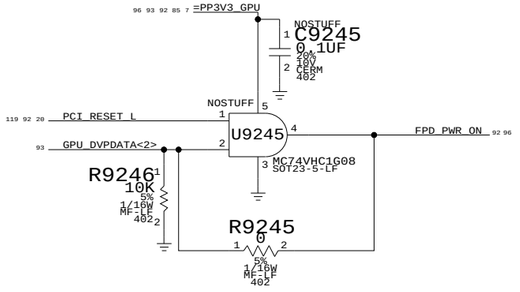


GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS







GPU Straps

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

(PLACE THE OSCILLATOR AND R9372 AND R9373 CLOSE TO ATI PIN AH28)

(PLACE R9371 CLOSE TO OSC)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0131	1	RES,130 OHM,1/16W,1%,0402	R9373	RV370XT
114S0134	1	RES,140 OHM,1/16W,1%,0402	R9373	RV380XT

U8400 RV370XT BGA (5 OF 5)

OMIT

GPIO: GPIO_GPIO<0> … GPIO_GPIO<14>, TP_GPU_GPIO<2>, TP_GPU_GPIO<3>, GPIO_MEMSSIN

GPIO+PWRCNTL

VREFG

CLK: XTALOUT, XTALIN

TEST: PLLTEST, TESTEN, TEST_YCLK, TEST_MCLK

DPLUS, DMINUS, HPD1

NC — NO CONNECTS — NC

EXTERNAL TMDS

DVPDATA: TP_GPU_DVPDATA<0> … TP_GPU_DVPDATA<23>

DVPCNTL, DVOMODE

TMDS: TXCP, TXCM*, TX0P, TX0M*, TX1P, TX1M*, TX2P, TX2M*, DDC3CLK, DDC3DATA

DAC1: R, G, B, HSYNC, VSYNC, RSET, DDC1CLK, DDC1DATA, GPIO_AUXWIN, STEREOSYNC

DAC2: Y_G, C_R, COMP_B, H2SYNC, V2SYNC, R2SET, DDC2CLK, DDC2DATA

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_TCKM	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	I2C	I2C	
	I2C	I2C	
	I2C	I2C	
	I2C	I2C	

GPU THERMAL SENSOR

U9390 MAX6690MEE (QSOP, SYM_VER2)

PLACE C9392 CLOSE TO TEMP SENSOR

GPU DVI & DACs

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

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PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

APPLE COMPUTER INC.

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INTERNAL LCD

NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
GPU_TMDS	GPU_TMDS	TCK
GPU_TMDS	GPU_TMDS	TCK
GPU_TMDS	GPU_TMDS	TD0
GPU_TMDS	GPU_TMDS	TD0
GPU_TMDS	GPU_TMDS	TD1
GPU_TMDS	GPU_TMDS	TD1
GPU_TMDS	GPU_TMDS	TD2
GPU_TMDS	GPU_TMDS	TD2

TCKP, TCKM, TD0P, TD0M, TD1P, TD1M, TD2P, TD2M

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

TMDS_D2M, TMDS_D2P, TMDS_D1M, TMDS_D1P, TMDS_D0M, TMDS_D0P, TMDS_CKM, TMDS_CKP

R9604 332 1% 1/16W MF-LF 402
R9603 332 1% 1/16W MF-LF 402
R9602 332 1% 1/16W MF-LF 402
R9601 165 1% 1/16W MF-LF 402
R9600 165 1% 1/16W MF-LF 402
C9600 22PF 5% 50V CERM 402

NOSTUFF R9626 0
NOSTUFF R9627 0
NOSTUFF R9628 0
NOSTUFF R9629 0
NOSTUFF R9630 0
NOSTUFF R9631 0
NOSTUFF R9632 0
NOSTUFF R9633 0

L9602 90-OHM SM
L9608 90-OHM SM
L9609 90-OHM SM
L9610 90-OHM SM

TMDS_CK_TERM
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM

=PP3V3_GPU

R9605 2.0K 5% 1/16W MF-LF 402
R9607 2.0K 5% 1/16W MF-LF 402
R9682 0 5% 1/8W MF-LF 805
C9601 0.01UF 10% 16V CERM 402
R9608 33 5% 1/16W MF-LF 402
R9606 33 5% 1/16W MF-LF 402

PP3V3_DDC
I2C_GPU_TMDS_SCL, I2C_GPU_TMDS_SDA
I2C_TMDS_SCL, I2C_TMDS_SDA

INTERNAL TMDS CONNECTOR

SDF9600
STDOFF-1180D-181H-TH
(516S0241)
J9602 53307-3072 F-ST-SM

PPVCC_TMDS
PP3V3_DDC VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
TD0M, TD0P, TD2M, TD2P, I2C_TMDS_SDA
TCKM, TCKP, TD1M, TD1P, I2C_TMDS_SCL
GND_CHASSIS_TMDS

C9616 10UF 10% 16V CERM 1210
C9615 0.01UF 10% 16V CERM 402

SDF9601
STDOFF-1180D-181H-TH

PANEL POWER SEQUENCING

=PP12V_GPU
NOSTUFF Q9600 SI4435DY SOI
R9634 0 5% 1/8W MF-LF 805
C9619 0.01UF 20% 16V CERM 402
R9625 100K 5% 1/16W MF-LF 402
C9618 0.022UF 20% 16V CERM 402
FPD_PWR_SW_G
R9613 100K 5% 1/16W MF-LF 402
D9614 MMBD914XXG SOT23
C9617 10UF 10% 16V CERM 1210
R9660 10K 5% 1/16W MF-LF 402
PPVCC_TMDS VOLTAGE=12V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
FPD_PWR_ON_D
Q9601 2N7002 SOT23-LF
FPD_PWR_ON
TMDS_EN_R
R9614 10K 5% 1/16W MF-LF 402
TMDS_EN
DZ9600 MMBZ5227B SOT23

U9670 74LCX125 TSSOP
FPD_PWR_ON
LED5900_PWR
R9612 330 5% 1/10W MF-LF 603
LED5900_P1
LED9600 GREEN 2.0X1.25A

SILKSCREEN: 3

EXTERNAL VGA CONNECTOR

NET_PHYSICAL_TYPE	NET_SPACING_TYPE
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA
GPU_VGA	GPU_VGA

FILT_ANALOG_GRN, FILT_ANALOG_RED, FILT_ANALOG_BLU, VGA_VSYNC, VGA_VSYNC_R, VGA_HSYNC, VGA_HSYNC_R

PP5V_USB2
R9680 0 5% 1/8W MF-LF 805
PP5V_VGA VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
C9602 0.01UF 10% 16V CERM 402
GND_CHASSIS_VGA

=PP3V3_GPU
U9670 74LCX125 TSSOP
ANALOG_VSYNC, VGA_VSYNC, VGA_VSYNC_R
C9670 0.1UF 20% 10V CERM 402
R9671 33 5% 1/16W MF-LF 402
ANALOG_HSYNC, VGA_HSYNC, VGA_HSYNC_R
R9672 33 5% 1/16W MF-LF 402
NOSTUFF C9607 22PF 5% 50V CERM 402
NOSTUFF C9608 22PF 5% 50V CERM 402
GND_CHASSIS_VGA

=PP3V3_GPU
R9673 10K 5% 1/16W MF-LF 402
R9674 10K 5% 1/16W MF-LF 402
Q9675 2N7002DW-X-F SOT-363
I2C_GPU_MON_SCL, I2C_MON_SCL, I2C_MON_SCL_R
R9675 100 5% 1/16W MF-LF 402
I2C_GPU_MON_SDA, I2C_MON_SDA, I2C_MON_SDA_R
R9676 100 5% 1/16W MF-LF 402
PP5V_VGA
R9677 4.7K 5% 1/16W MF-LF 402
R9678 4.7K 5% 1/16W MF-LF 402
C9677 47PF 5% 50V CERM 402
C9678 47PF 5% 50V CERM 402
GND_CHASSIS_VGA

NOSTUFF FL9600 LCFILTER SM-220MHZ
ANALOG_RED
R9640 0 5% 1/16W MF-LF 402
NOSTUFF FL9601 LCFILTER SM-220MHZ
ANALOG_GRN
R9641 0 5% 1/16W MF-LF 402
NOSTUFF FL9602 LCFILTER SM-220MHZ
ANALOG_BLU
R9642 0 5% 1/16W MF-LF 402

PLACE R9321-3 & FL9600-2 CLOSE TO J9603

M33: 514S0097

CRITICAL
J9603 DV01793-M33-4F F-ST-SM
NC 15 PIN 15 NC REQUESTED BY EMC
VGA_HSYNC_R, FILT_ANALOG_RED, FILT_ANALOG_GRN, FILT_ANALOG_BLU, I2C_MON_SCL_R, MON_DETECT
VGA_VSYNC_R, (4 (RED_RTN), 6 (GRN_RTN), 8, PP5V_VGA, 10 I2C_MON_SDA_R, 12 (BLU_RTN), 14, 16)
C9605 0.01UF 10% 16V CERM 402
C9604 0.01UF 10% 16V CERM 402
C9603 0.01UF 10% 16V CERM 402
GND_CHASSIS_VGA

TMDS / ExtVGA

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

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KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

KODIAK PCI-E CONST

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	97	154

PLANE-SPLIT AC RETURN PATHS

LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)

=PPVCORE_PWRON_NB_HT 3A4 98D5 98D7

C9806 1UF 10% 6.3V CERM 402
C9807 1UF 10% 6.3V CERM 402
C9808 1UF 10% 6.3V CERM 402
C9809 1UF 10% 6.3V CERM 402
C9810 1UF 10% 6.3V CERM 402
C9811 1UF 10% 6.3V CERM 402
C9812 1UF 10% 6.3V CERM 402
C9813 1UF 10% 6.3V CERM 402
C9814 1UF 10% 6.3V CERM 402
C9815 1UF 10% 6.3V CERM 402

98D7 98D5 3A4 =PPVCORE_PWRON_NB_HT — C9834 0.1UF 20% 10V CERM 402 — =PP1V2_PWRON_HT_NBTX 3C2 98B1 98C8 98D1 98D3 98D4

KODIAK CORES

PP9806 P4MM SM — 1.6V — Q63 = PP1V6

98D7 3A4 =PPVCORE_PWRON_NB_HT

98D2 3C1 =PP2V5_PWRON_NB_HT — L9800 0.22UH 0805-1 — 104D4 PWR_HT_AVDD

C9800 0.01UF 10% 16V CERM 402
C9801 10UF 10% 6.3V X5R 805
C9802 1UF 10% 6.3V CERM 402

104D4 98C3 98A6 6A3 KOD_L15_GND (THIS PAGE)

PP9808 P4MM SM — HTM2NC0- / HTM2NC0+ — PP9809 P4MM SM

K15

HT_REFCLK_AVDD (1.65V-2.75V) (1.6V-1.2V)

E25	HT_CLK_RXN0	HT_RX_VDD	A24
D25	HT_CLK_RXP0	HT_RX_VDD	B22
J27	HT_CTL_RXN0	HT_RX_VDD	B26
K27	HT_CTL_RXP0	HT_RX_VDD	D24
F26	HT_CAD_RXN0	HT_RX_VDD	E22
F27	HT_CAD_RXP0	HT_RX_VDD	E26
F25	HT_CAD_RXN1	HT_RX_VDD	G24
F24	HT_CAD_RXP1	HT_RX_VDD	H26
A25	HT_CAD_RXN2	HT_RX_VDD	K24
B25	HT_CAD_RXP2	HT_RX_VDD	L22
G25	HT_CAD_RXN3		
H25	HT_CAD_RXP3		
L25	HT_CAD_RXN4		
K25	HT_CAD_RXP4		
G27	HT_CAD_RXN5		
H27	HT_CAD_RXP5		
J25	HT_CAD_RXN6		
J26	HT_CAD_RXP6		
C26	HT_CAD_RXN7		
C27	HT_CAD_RXP7		
F22	HT_CLK_RXN1		
F23	HT_CLK_RXP1		
E21	HT_CTL_RXP1		
D21	HT_CTL_RXN1		
E23	HT_CAD_RXN8		
D23	HT_CAD_RXP8		
A23	HT_CAD_RXN9		
B23	HT_CAD_RXP9		
H23	HT_CAD_RXN10		
G23	HT_CAD_RXP10		
C22	HT_CAD_RXN11		
C23	HT_CAD_RXP11		
K23	HT_CAD_RXN12		
L23	HT_CAD_RXP12		
J23	HT_CAD_RXN13		
J24	HT_CAD_RXP13		
A21	HT_CAD_RXN14		
B21	HT_CAD_RXP14		
C24	HT_CAD_RXN15		
C25	HT_CAD_RXP15		
K19	HT_PVTREF0		
L19	HT_PVTREF1		
L17	HT_PVTREF2_ALT		
K17	HT_PVTREF3_ALT		
J16	HT_REFCLK_N		
J15	HT_REFCLK_P		

(200MHZ)

HT_REFCLK_AGND

L15

104D4 98C3 98C6 6A3 KOD_L15_GND (THIS PAGE) — XW9800 SM

PP9807 P4MM SM — 1.2V — Q63 = PP1V2

=PP1V2_PWRON_HT_NBTX 3C2 98B1 98D3 98D5

104D4 PWR_HT_AVDD2 — L9801 0.22UH 0805-1 — =PP2V5_PWRON_NB_HT 3C1 98D7

C9803 1UF 10% 6.3V CERM 402
C9804 10UF 10% 6.3V X5R 805
C9805 0.01UF 10% 16V CERM 402

KOD_L15_GND 6A3 98A6 98C6 104D4 (THIS PAGE)

H15

HT_REFCLK_AVDD2 (1.65V-2.75V) (1.6V-1.2V)

A16	HT_VD4	HT_CLK_TXN0	J19
A20	HT_VD4	HT_CLK_TXP0	J20
B14	HT_VD4	HT_CTL_TXN0	J22
B18	HT_VD4	HT_CTL_TXP0	J21
D16	HT_VD4	HT_CAD_TXN0	F16
D20	HT_VD4	HT_CAD_TXP0	F17
E18	HT_VD4	HT_CAD_TXN1	G17
G16	HT_VD4	HT_CAD_TXP1	H17
G20	HT_VD4	HT_CAD_TXN2	J18
H18	HT_VD4	HT_CAD_TXP2	J17
H22	HT_VD4	HT_CAD_TXN3	F18
K16	HT_VD4	HT_CAD_TXP3	F19
K20	HT_VD4	HT_CAD_TXN4	G19
L18	HT_VD4	HT_CAD_TXP4	H19
M17	HT_VD4	HT_CAD_TXN5	G21
M21	HT_VD4	HT_CAD_TXP5	H21
N19	HT_VD4	HT_CAD_TXN6	F21
		HT_CAD_TXP6	F20
		HT_CAD_TXN7	K21
		HT_CAD_TXP7	L21
		HT_CLK_TXN1	C16
		HT_CLK_TXP1	C17
		HT_CTL_TXP1	E15
		HT_CTL_TXN1	D15
		HT_CAD_TXN8	D19
		HT_CAD_TXP8	E19
		HT_CAD_TXN9	D17
		HT_CAD_TXP9	E17
		HT_CAD_TXN10	C19
		HT_CAD_TXP10	C18
		HT_CAD_TXN11	A15
		HT_CAD_TXP11	B15
		HT_CAD_TXN12	A17
		HT_CAD_TXP12	B17
		HT_CAD_TXN13	B19
		HT_CAD_TXP13	A19
		HT_CAD_TXN14	C15
		HT_CAD_TXP14	C14
		HT_CAD_TXN15	C20
		HT_CAD_TXP15	C21
		HT_LDTSTOP_L	AF06
		HT_LDTREQ_L	AF09
		HT_PWROK	AF03
		HT_RESET_L	AE11

U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE

A14	HT_VD4_GND	HT_RX_GND	A22
A18	HT_VD4_GND	HT_RX_GND	A26
B16	HT_VD4_GND	HT_RX_GND	B24
B20	HT_VD4_GND	HT_RX_GND	D22
D18	HT_VD4_GND	HT_RX_GND	D26
E16	HT_VD4_GND	HT_RX_GND	E24
E20	HT_VD4_GND	HT_RX_GND	G26
G18	HT_VD4_GND	HT_RX_GND	H24
G22	HT_VD4_GND	HT_RX_GND	K22
H16	HT_VD4_GND	HT_RX_GND	L24
H20	HT_VD4_GND		
K18	HT_VD4_GND		
L16	HT_VD4_GND		
L20	HT_VD4_GND		
M16	HT_VD4_GND		
M20	HT_VD4_GND		
N18	HT_VD4_GND		

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)

98D5 98D4 98D1 98C8 98B1 3C2 =PP1V2_PWRON_HT_NBTX

C9817 1UF 10% 6.3V CERM 402
C9818 1UF 10% 6.3V CERM 402
C9819 1UF 10% 6.3V CERM 402
C9820 1UF 10% 6.3V CERM 402
C9821 1UF 10% 6.3V CERM 402
C9822 1UF 10% 6.3V CERM 402
C9823 1UF 10% 6.3V CERM 402
C9824 1UF 10% 6.3V CERM 402
C9825 1UF 10% 6.3V CERM 402
C9826 1UF 10% 6.3V CERM 402

98D5 98D4 98D3 98C8 98B1 3C2 =PP1V2_PWRON_HT_NBTX

C9827 1UF 10% 6.3V CERM 402
C9828 1UF 10% 6.3V CERM 402
C9829 1UF 10% 6.3V CERM 402
C9830 1UF 10% 6.3V CERM 402
C9831 1UF 10% 6.3V CERM 402
C9832 1UF 10% 6.3V CERM 402
C9833 1UF 10% 6.3V CERM 402
C9839 1UF 10% 6.3V CERM 402
C9840 1UF 10% 6.3V CERM 402
C9841 1UF 10% 6.3V CERM 402
C9847 1UF 10% 6.3V CERM 402
C9842 1UF 10% 6.3V CERM 402
C9843 1UF 10% 6.3V CERM 402
C9844 1UF 10% 6.3V CERM 402
C9845 1UF 10% 6.3V CERM 402
C9846 1UF 10% 6.3V CERM 402

98D5 98D4 98D3 98D1 98B1 3C2 =PP1V2_PWRON_HT_NBTX

104B8 100D3 99C4 HT_MB_TO_NB_CLK_N<0>
104B8 100D3 99C4 HT_MB_TO_NB_CLK_P<0>
104B8 100B3 99D4 HT_MB_TO_NB_CTL_N<0>
104B8 100B3 99D4 HT_MB_TO_NB_CTL_P<0>

PP9800 P4MM SM — MHT0- / MHT0+ — PP9801 P4MM SM

KODIAK HT RECEIVE CLOCKS

PP9802 P4MM SM — MHT1- / MHT1+ — PP9803 P4MM SM

104B8 100C3 99C2 HT_MB_TO_NB_CAD_N<0>
104B8 100D3 99C2 HT_MB_TO_NB_CAD_P<0>
104B8 100C3 99C2 HT_MB_TO_NB_CAD_N<1>
104B8 100C3 99C2 HT_MB_TO_NB_CAD_P<1>
104B8 100C3 99C2 HT_MB_TO_NB_CAD_N<2>
104B8 100C3 99C2 HT_MB_TO_NB_CAD_P<2>
104B8 100C3 99B2 HT_MB_TO_NB_CAD_N<3>
104B8 100C3 99B4 HT_MB_TO_NB_CAD_P<3>
104B8 100C3 99B4 HT_MB_TO_NB_CAD_N<4>
104B8 100C3 99B4 HT_MB_TO_NB_CAD_P<4>
104B8 100C3 99B4 HT_MB_TO_NB_CAD_N<5>
104B8 100C3 99B4 HT_MB_TO_NB_CAD_P<5>
104B8 100C3 99C4 HT_MB_TO_NB_CAD_N<6>
104B8 100C3 99C4 HT_MB_TO_NB_CAD_P<6>
104B8 100C3 99C4 HT_MB_TO_NB_CAD_N<7>
104B8 100C3 99C4 HT_MB_TO_NB_CAD_P<7>

R9806 8.2K 5% 1/16W MF-LF 402

104B8 100C3 99D7 HT_MB_TO_NB_CLK_N<1>
104B8 100C3 99D7 HT_MB_TO_NB_CLK_P<1>

6A5 HT_MB_TO_NB_CTL_N<1>
6A5 HT_MB_TO_NB_CTL_P<1>

R9807 8.2K 5% 1/16W MF-LF 402

104A8 100C3 99D2 HT_MB_TO_NB_CAD_N<8>
104A8 100D3 99D2 HT_MB_TO_NB_CAD_P<8>
104A8 100C3 99D2 HT_MB_TO_NB_CAD_N<9>
104A8 100D3 99D2 HT_MB_TO_NB_CAD_P<9>
104A8 100C3 99D2 HT_MB_TO_NB_CAD_N<10>
104A8 100D3 99D2 HT_MB_TO_NB_CAD_P<10>
104A8 100C3 99D2 HT_MB_TO_NB_CAD_N<11>
104A8 100D3 99C2 HT_MB_TO_NB_CAD_P<11>
104B8 100B3 99C4 HT_MB_TO_NB_CAD_N<12>
104B8 100B3 99C4 HT_MB_TO_NB_CAD_P<12>
104B8 100B3 99D4 HT_MB_TO_NB_CAD_N<13>
104B8 100B3 99D4 HT_MB_TO_NB_CAD_P<13>
104B8 100B3 99D4 HT_MB_TO_NB_CAD_N<14>
104B8 100B3 99D4 HT_MB_TO_NB_CAD_P<14>
104B8 100B3 99D4 HT_MB_TO_NB_CAD_N<15>
104B8 100B3 99D4 HT_MB_TO_NB_CAD_P<15>

R9800 100 1% 1/16W MF-LF 402
R9801 200 1% 1/16W MF-LF 402

104D4 6A5 HT_KOD_PVTREF0
104D4 6A5 HT_KOD_PVTREF1
104D4 6A5 HT_KOD_PVTREF2_ALT
104D4 6A5 HT_KOD_PVTREF3_ALT

KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

104D8 26C2 HT_NB_REFCLK_P<0>

R9802 20.5 1% 1/16W MF-LF 402
C9837 0.01UF 10% 16V CERM 402
104D8 HT_NB_P<0>
R9803 29.4 1% 1/16W MF-LF 402
NOSTUFF C9836 0.01UF 10% 16V CERM 402
HT_NB_G
R9804 29.4 1% 1/16W MF-LF 402
C9838 0.01UF 10% 16V CERM 402
104D8 HT_NB_N<0>
R9805 20.5 1% 1/16W MF-LF 402

104D8 26C2 HT_NB_REFCLK_N<0>

104D8 HT_NB_REFCLK_PF<0>
104D8 HT_NB_REFCLK_NF<0>

PP9804 P4MM SM — HREF0- / HREF0+ — PP9805 P4MM SM

KODIAK HT REFCLK

PAGE 98

KODIAK HT16

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

NOTICE OF PROPRIETARY PROPERTY

LAST_MODIFIED=Thu May 19 14:27:39 2005
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 98 OF 154	

DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT_NB_TO_MB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_MB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE				HT_MB_TO_NB_CAD_P<8..15>
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE				HT_MB_TO_NB_CAD_N<8..15>
TP_HT_MB_TO_NB_CLK_N<1>	TRUE				HT_MB_TO_NB_CLK_N<1>
TP_HT_MB_TO_NB_CLK_P<1>	TRUE				HT_MB_TO_NB_CLK_P<1>
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE				HT_NB_TO_MB_CAD_P<8..15>
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE				HT_NB_TO_MB_CAD_N<8..15>
NC_HT_NB_TO_MB_CLK_N<1>	TRUE				HT_NB_TO_MB_CLK_N<1>
NC_HT_NB_TO_MB_CLK_P<1>	TRUE				HT_NB_TO_MB_CLK_P<1>
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0

HT ALIASES

FINO-EG 05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT 101 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	HT_CLK66M_SB_C
HT_CLK66M_SB	0.38mm SPACING	HT_CLK66M_SB
	P3MM SPACING	HT_LDTRESET_L

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.

=PP1V2_PWRON_SB_HT — RA300 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLDVDDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — CA300 10UF 10% 6.3V X5R 805; CA301 1uF 10% 6.3V CERM 402

RA310 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLAVDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — CA310 10UF 10% 6.3V X5R 805; CA311 1uF 10% 6.3V CERM 402

=PP2V5_PWRON_HT — CA320 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT — CA302 10UF 10% 6.3V X5R 805; CA330 0.1uF 20% 10V CERM 402; CA331 0.1uF 20% 10V CERM 402; CA332 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT — CA309 10UF 10% 6.3V X5R 805; CA340 0.1uF 20% 10V CERM 402; CA341 0.1uF 20% 10V CERM 402; CA342 0.1uF 20% 10V CERM 402

HTS2MC0+ PPA300 P4MM SM
HTS2MC0- PPA301 P4MM SM
HTS2MC0+ PPA303 P4MM SM
HTS2MC0- PPA304 P4MM SM

U2300 SHASTA V1.1 BGA-LF (3 OF 8) HYPERTRANSPORT — SEE_TABLE

AVDD HT_PLL; DVDD; VDDP HT; HT_RXVDD; HT_TXVDD

HT_MB_TO_SB_CLK_P<0>	HT_CLKIN_P	HT_CLKOUT_P
HT_MB_TO_SB_CLK_N<0>	HT_CLKIN_N	HT_CLKOUT_N
HT_MB_TO_SB_CAD_P<0>	HT_CADIN_0_P	HT_CADOUT_0_P
HT_MB_TO_SB_CAD_N<0>	HT_CADIN_0_N	HT_CADOUT_0_N
HT_MB_TO_SB_CAD_P<1>	HT_CADIN_1_P	HT_CADOUT_1_P
HT_MB_TO_SB_CAD_N<1>	HT_CADIN_1_N	HT_CADOUT_1_N
HT_MB_TO_SB_CAD_P<2>	HT_CADIN_2_P	HT_CADOUT_2_P
HT_MB_TO_SB_CAD_N<2>	HT_CADIN_2_N	HT_CADOUT_2_N
HT_MB_TO_SB_CAD_P<3>	HT_CADIN_3_P	HT_CADOUT_3_P
HT_MB_TO_SB_CAD_N<3>	HT_CADIN_3_N	HT_CADOUT_3_N
HT_MB_TO_SB_CAD_P<4>	HT_CADIN_4_P	HT_CADOUT_4_P
HT_MB_TO_SB_CAD_N<4>	HT_CADIN_4_N	HT_CADOUT_4_N
HT_MB_TO_SB_CAD_P<5>	HT_CADIN_5_P	HT_CADOUT_5_P
HT_MB_TO_SB_CAD_N<5>	HT_CADIN_5_N	HT_CADOUT_5_N
HT_MB_TO_SB_CAD_P<6>	HT_CADIN_6_P	HT_CADOUT_6_P
HT_MB_TO_SB_CAD_N<6>	HT_CADIN_6_N	HT_CADOUT_6_N
HT_MB_TO_SB_CAD_P<7>	HT_CADIN_7_P	HT_CADOUT_7_P
HT_MB_TO_SB_CAD_N<7>	HT_CADIN_7_N	HT_CADOUT_7_N
HT_MB_TO_SB_CTL_P<0>	HT_CTLIN_P	HT_CTLOUT_P
HT_MB_TO_SB_CTL_N<0>	HT_CTLIN_N	HT_CTLOUT_N
HT_PWROK	HT_PWROK_H	
HT_LDTRESET_L	HT_RESET_L	
HT_LDTSTOP_L	HT_LDTSTOP_L	HT_LDTREQ_L
HT_CLK66M_SB_C	HT_REFCLK	HT_R100P
SB_HT_S100M66M	HT_S100M66M	HT_R100N
SB_SELHT100	SEL_HT00_H	

HT_SB_TO_MB_CLK_P<0> / HT_SB_TO_MB_CLK_N<0>
HT_SB_TO_MB_CAD_P<0> … HT_SB_TO_MB_CAD_P<7>
HT_SB_TO_MB_CAD_N<0> … HT_SB_TO_MB_CAD_N<7>
HT_SB_TO_MB_CTL_P<0> / HT_SB_TO_MB_CTL_N<0>

HT_LDTREQ_L — RA301 0 5% 1/10W MF-LF 402 — HT_LDTREQ_L

SB_HT_R100_P / SB_HT_R100_N

HT_PLL AGND DGND; HT_RXGND; HT_TXGND

RA350 82.5 1% 1/16W MF-LF 402 — CA350 47pF 5% 50V CERM 402; CA351 47pF 5% 50V CERM 402

PPA302 P4MM SM

RA355 0 5% 1/16W MF-LF 402 — HT_CLK66M_SB — 1.0V pk-pk

=PP1V2_PWRON_SB_HT

RA352 NOSTUFF 4.7K 1% 1/16W MF-LF 402 — 1 = 100MHz
RA354 NOSTUFF 10K 5% 1/16W MF-LF 402 — 1 = 100MHz
RA353 4.7K 1% 1/16W MF-LF 402 — 0 = 66MHz
RA351 1K 1% 1/16W MF-LF 402 — 0 = 200MHz

HT RefClk	HT I/F Speed	
1 = 100MHz	1 = 100MHz	DETERMINES THE OPERATING FREQUENCY OF HT CORE
0 = 66MHz	0 = 200MHz	1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
		0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	103	154

LAST_MODIFIED=Thu May 19 14:26:14 2005

DRAWING
TITLE=ICE1,DRAWING
ASSEMBLY=SYMMETRIC

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	P3MM_SPACING	

PCI_AD<31..28>	120B6	121C3	121C4	122B5	122C5	125C3	
PCI_AD<27>	120B6	121C4	122C6	125C3			
PCI_AD<26..24>	120B6	121C3	121C4	122C5	125C3		
PCI_AD<23>	120B6	121C4	122C5				
PCI_AD<22>	120C6	121C3	122C5				
PCI_AD<21>	120C6	121C4	122C5				
PCI_AD<20>	120C6	121C3	122C5	125B5			
PCI_AD<19..18>	120C6	121C3	121C4	122C5	125B5		
PCI_AD<17>	120C6	121C1	121C4	122C5	125B5		
PCI_AD<16..0>	120C6	120D6	121B3	121B4	121C3	121C4	122C5	122D5	125B5	125C5
PCI_CBE_L<3..0>	120B6	121B3	121C4	122B5						
PCI_PAR	120B6	121C3	122B5							
PCI_DEVSEL_L	119B2	120B6	121C3	122B5						
PCI_FRAME_L	119B2	120B6	121C3	122B5						
PCI_IRDY_L	119B2	120B6	121C4	122B5						
PCI_TRDY_L	119A2	120B6	121C3	122B5						
PCI_STOP_L	119A2	120B6	121C3	122B5						
PCI_CLK66M_SB_INT	26A2	119C5								

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

119B8 119B1 3A7 =PP3V3_SB_PCI

PPB905 P4MM SM PP 1 PP_3V3SBPCI_B9

XWB900 SM 2 1

CB910 10UF 10% 6.3V X5R 805
CB900 0.1uF 20% 16V CERM 402
CB901 0.1uF 20% 16V CERM 402
CB902 0.1uF 20% 16V CERM 402
CB903 0.1uF 20% 16V CERM 402
CB904 0.1uF 20% 16V CERM 402

NO STUFF
CB911 10UF 10% 6.3V X5R 805
CB905 0.1uF 20% 16V CERM 402
CB906 0.1uF 20% 16V CERM 402
CB907 0.1uF 20% 16V CERM 402
CB908 0.1uF 20% 16V CERM 402
CB909 0.1uF 20% 16V CERM 402

XWB901 SM 2 1 PP_2V5PWRONSB_B9

PPB906 P4MM SM PP 1

=PP2V5_PWRON_SB 3C1 23B2 23C2 24D5 138C6

CB920 0.1uF 20% 16V CERM 402
CB921 0.1uF 20% 16V CERM 402
CB922 0.1uF 20% 16V CERM 402
CB923 0.1uF 20% 16V CERM 402

PPB900 P4MM SM PP 1 119D6 26A2 P3MM SPACING PCI_CLK66M_SB_INT

PPB901 P4MM SM PP 1 26A1 PCI_CLK33M_SB_EXT_RR

NOSTUFF
CB912 2PF +/-0.25PF 50V C0G 402-1
STUFF NEAR SHASTA

U2300 SHASTA V1.1 BGA-LF (4 OF 8)

VDDOPC: AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19
PCIVDDP: B20 J18 M20 U20

SEE_TABLE

PCIBR_CLK_H AB9
PCI1CLK_H U19

PCI

PCI1AD_0_H	L18	PCI_SB_AD<0>	6C1 120D7
PCI1AD_1_H	K19	PCI_SB_AD<1>	120D7
PCI1AD_2_H	L22	PCI_SB_AD<2>	6C1 120C7
PCI1AD_3_H	M22	PCI_SB_AD<3>	6C1 120C7
PCI1AD_4_H	M18	PCI_SB_AD<4>	6C1 120C7
PCI1AD_5_H	L20	PCI_SB_AD<5>	120C7
PCI1AD_6_H	M21	PCI_SB_AD<6>	120C7
PCI1AD_7_H	N16	PCI_SB_AD<7>	120C7
PCI1AD_8_H	M20	PCI_SB_AD<8>	120C7
PCI1AD_9_H	P22	PCI_SB_AD<9>	6C1 120C7
PCI1AD_10_H	M17	PCI_SB_AD<10>	6C1 120C7
PCI1AD_11_H	N18	PCI_SB_AD<11>	6C1 120C7
PCI1AD_12_H	M19	PCI_SB_AD<12>	120C7
PCI1AD_13_H	N19	PCI_SB_AD<13>	6C1 120C7
PCI1AD_14_H	P21	PCI_SB_AD<14>	6C1 120C7
PCI1AD_15_H	R22	PCI_SB_AD<15>	120C7
PCI1AD_16_H	P20	PCI_SB_AD<16>	120C7
PCI1AD_17_H	V21	PCI_SB_AD<17>	120C7
PCI1AD_18_H	P18	PCI_SB_AD<18>	6C1 120C7
PCI1AD_19_H	T20	PCI_SB_AD<19>	6C1 120C7
PCI1AD_20_H	R16	PCI_SB_AD<20>	120C7
PCI1AD_21_H	R17	PCI_SB_AD<21>	6C1 120C7
PCI1AD_22_H	W21	PCI_SB_AD<22>	120C7
PCI1AD_23_H	Y22	PCI_SB_AD<23>	6C1 120B7
PCI1AD_24_H	R18	PCI_SB_AD<24>	120B7
PCI1AD_25_H	T19	PCI_SB_AD<25>	6C1 120B7
PCI1AD_26_H	T18	PCI_SB_AD<26>	6C1 120B7
PCI1AD_27_H	Y21	PCI_SB_AD<27>	120B7
PCI1AD_28_H	W20	PCI_SB_AD<28>	6C1 120B7
PCI1AD_29_H	T16	PCI_SB_AD<29>	6C1 120B7
PCI1AD_30_H	AA21	PCI_SB_AD<30>	6C1 120B7
PCI1AD_31_H	T17	PCI_SB_AD<31>	6C1 120B7

PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	6C1 120B7
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	6C1 120B7
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	6C1 120B7
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	6C1 120B7
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	120B7
PCI1FRAME_L	T21	PCI_SB_FRAME_L	6B1 120B7
PCI1IRDY_L	R21	PCI_SB_IRDY_L	6B1 120B7
PCI1TRDY_L	P19	PCI_SB_TRDY_L	6B1 120B7
PCI1STOP_L	P17	PCI_SB_STOP_L	6B1 120B7
PCI1PAR_H	N17	PCI_SB_PAR	6B1 120B7
PCI1RST_L	U18	SB_PCI_RESET_L	

NET_SPACING_TYPE=P3MM SPACING

"Slot A" - AD17
121C4 119B7 PCI_SLOTA_REQ_L AB18 PCI1REQ_0_L
121C3 119B7 PCI_SLOTA_GNT_L AA18 PCI1GNT_0_L

"Slot G" - AD27
122B5 119B7 PCI_SLOTG_REQ_L AB20 PCI1REQ_1_L
122B5 119B7 PCI_SLOTG_GNT_L AB19 PCI1GNT_1_L

"Slot D" - AD20
119B7 PCI_SLOTD_REQ_L V17 PCI1REQ_2_L
119A7 PCI_SLOTD_GNT_L V18 PCI1GNT_2_L

125B7 121B4 ROM_CS_L AB8 ROMCS_L
125B7 121B3 ROM_OE_L AA9 ROMOE_L
125B7 121B4 ROM_WE_L Y10 ROMRW_L

122A7 29D6 28D4 24B7 21C5 SYS_IO_RESET_L

Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

=PP3V3_PWRON_SB 3A3 149A3 20D2 154D2 23B7 24A6 24B7 24C3 24D2 29B4 29C7 120C4

RB955 4.7K 1% 1/16W MF-LF 402
CB950 0.1uF 20% 16V CERM 402
NOSTUFF RB950 4.7K 1% 1/16W MF-LF 402

UB950 MC74VHC1G08 SOT23-5-LF

PCI_RESET_L 120B4 120C2

RB900 0 5% 1/16W MF-LF 402 NOSTUFF

=PP3V3_SB_PCI 119C7 119B8 3A7

RPB902 4.7K 5% 1/16W SM-LF
122B5 121C3 120B6 119D6 PCI_DEVSEL_L
122B5 121C3 120B6 119D6 PCI_FRAME_L
122B5 121C4 120B6 119D6 PCI_IRDY_L
122B5 121C3 120B6 119D6 PCI_TRDY_L
RPB901 4.7K 5% 1/16W SM-LF
122B5 121C3 120B6 119D6 PCI_STOP_L

=PP3V3_SB_PCI 3A7 119B1 119C7

RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTA_REQ_L 119B5 121C4
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTA_GNT_L 119B5 121C3
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTG_REQ_L 119B5 122B5
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTG_GNT_L 119B5 122B5
RPB901 4.7K 5% 1/16W SM-LF
PCI_SLOTD_REQ_L 119B5
RPB901 4.7K 5% 1/16W SM-LF
PCI_SLOTD_GNT_L 119B5

Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 119 OF 154	

LAST_MODIFIED=Thu May 19 14:26:18 2005

DRAWING
TITLE=K1LOHANA
ASSEMVI=SHASTA

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119C3	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119D6	121B5	122D5	125C5							
119B3	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119D6	121B5	122D5	125C5							
119B3	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119D6	121B4	122D5	125C5							
119B3	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119D6	121B5	122D5	125C5							
119B3	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119D6	121B4	122C5	125C5							
119B3	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119D6	121B5	122C5	125C5							
119B3	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119D6	121B5	122C5	125C5							
119B3	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119D6	121B5	122C5	125C5							
119B3	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119D6	121B5	122C5	125C5							
119B3	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119D6	121B5	122C5	125C5							
119B3	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119D6	121B4	122C5	125B5							
119B3	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119D6	121B4	122C5	125B5							
119B3	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119D6	121B5	122C5	125B5							
119B3	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119D6	121B4	122C5	125B5							
119B3	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119D6	121B4	122C5	125B5							
119B3	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119D6	121B4	122C5	125B5							
119B3	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119D6	121B4	122C5	125B5							

RC000

119B3	PCI_SB_AD<17>	47 5% 1/16W MF-LF 402	1	2		PCI_AD<17>	119D6	121C4	121C6	122C5	125B5						

119B3	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119D6	121C5	122C5	125B5							
119B3	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119D6	121C5	122C5	125B5							
119B3	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119D6	121C4	122C5	125B5							
119B3	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119D6	121C5	122C5								
119B3	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119D6	121C5	122C5								
119B3	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119D6	121C4	122C5								
119B3	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119D6	121C4	122C5	125C3							
119B3	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119D6	121C5	122C5	125C3							
119B3	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119D6	121C5	122C5	125C3							

RC001

119A3	PCI_SB_AD<27>	47 5% 1/16W MF-LF 402	1	2		PCI_AD<27>	119D6	121C5	122C6	125C3							

119A3	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119D6	121C4	122C5	125C3							
119A3	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119D6	121C5	122C5	125C3							
119A3	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119D6	121C5	122B5	125C3							
119A3	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119D6	121C4	122B5	125C3							
119A3	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119D6	121B5	122B5								
119A3	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119D6	121B4	122B5								
119A3	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119D6	121B4	122B5								
119A3	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119D6	121C5	122B5								
119A3	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119B2	119D6	121C5	122B5							
119A3	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119B2	119D6	121C4	122B5							
119A3	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119B2	119D6	121C5	122B5							
119A3	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119A2	119D6	121C4	122B5							
119A3	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119A2	119D6	121B5	122B5							
119A3	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119D6	121B5	122B5								

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 120 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR

125 7 =PP3V3_PCI

SDFC100
STDOFF-3MMOD5MMH-TH

NOSTUFF
CC150 10UF 10% 6.3V X6S 805
CC151 1UF 10% 6.3V CERM 402
CC152 1UF 10% 6.3V CERM 402

CRITICAL
JC150
962-001-8028R
F-ST-SM

	1	2	PCI_AD<31>	119 120 122 125
125 122 120 119 PCI_AD<30>	3	4	AIRPORT_CLKRUN_L_PD	
	5	6	TP_AP_PME_L	
125 122 120 119 PCI_AD<27>	7	8	PCI_SLOTA_GNT_L	119
119 PCI_SLOTA_REQ_L	9	10		
125 122 120 119 PCI_AD<25>	11	12		
125 122 120 119 PCI_AD<29>	13	14	PCI_AD<24>	119 120 122 125
	15	16	=PCI_AIRPORT_RESET_L	20
122 120 119 PCI_CBE_L<3>	17	18	PCI_AD<28>	119 120 122 125
125 122 120 119 PCI_AD<26>	19	20		
122 120 119 PCI_AD<22>	21	22	PCI_AD<23>	119 120 122
PCI_SLOTA_IDSEL	23	24		
	25	26	PCI_AD<20>	119 120 122 125
125 122 120 119 PCI_AD<19>	27	28	PCI_FRAME_L	119 120 122
122 120 119 PCI_AD<21>	29	30	PCI_AD<17>	119 120 121 122 125
122 120 119 PCI_IRDY_L	31	32		
125 122 120 119 PCI_AD<18>	33	34	PCI_TRDY_L	119 120 122
122 120 119 PCI_DEVSEL_L	35	36		
	37	38	PCI_CBE_L<2>	119 120 122
121 26 PCI_CLK33M_AIRPORT	39	40	PCI_AD<16>	119 120 122 125
122 120 119 PCI_STOP_L	41	42		
125 122 120 119 PCI_AD<12>	43	44		
122 120 119 PCI_PAR	45	46		
	47	48	PCI_AD<14>	119 120 122 125
125 122 120 119 PCI_AD<8>	49	50	PCI_AD<13>	119 120 122 125
125 122 120 119 PCI_AD<9>	51	52		
122 120 119 PCI_CBE_L<0>	53	54	PCI_AD<10>	119 120 122 125
	55	56	PCI_AD<15>	119 120 122 125
125 122 120 119 PCI_AD<7>	57	58	AP_ALT_ANT	= NC_AP_ALT_ANT
125 122 120 119 PCI_AD<3>	59	60	PCI_CBE_L<1>	= MAKE_BASE=TRUE NO_TEST=YES 119 120 122
125 122 120 119 PCI_AD<6>	61	62	PCI_AD<4>	119 120 122 125
	63	64		
125 122 120 119 PCI_AD<1>	65	66	PCI_AD<11>	119 120 122 125
125 122 120 119 PCI_AD<5>	67	68	ROM_WE_L	119 125
125 122 120 119 PCI_AD<0>	69	70	PCI_AD<2>	119 120 122 125
	71	72		
143 USB_BT_P	73	74	PCI_AIRPORT_INT_L	24
143 USB_BT_N	75	76	ROM_OE_L	119 125
	77	78	ROM_ONBOARD_CS_L	125
7 =PP3V3_PWRON_BT	79	80	ROM_CS_L	119 125

516S0347

RC150 10K 5% 1/16W MF-LF 402

RC151 22 5% 1/16W MF-LF 402
125 122 121 120 119 PCI_AD<17>

CC160 1UF 10% 6.3V CERM 402

SDFC101
STDOFF-3MMOD5MMH-TH

AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 120A3 122B5

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122B7 3A7 =PPVIO_PCI_USB2

CC201 0.1uF 20% 10V CERM 402
CC202 0.1uF 20% 10V CERM 402
CC203 0.1uF 20% 10V CERM 402

XWC200 3M 2 1 PP_VIOPCIUSB2_C2 P4MM 3M PP PPC203

H3 H4 C8 VDD_PCI

UC200
NEC_UPD720101_USB2
FBGA-LF

125C5	121B3	120D6	119D6	PCI_AD<0>	M5	AD0
125C5	121B4	120D6	119D6	PCI_AD<1>	P5	AD1
125C5	121B3	120C6	119D6	PCI_AD<2>	N5	AD2
125C5	121B4	120C6	119D6	PCI_AD<3>	P4	AD3
125C5	121B3	120C6	119D6	PCI_AD<4>	N4	AD4
125C5	121B4	120C6	119D6	PCI_AD<5>	M3	AD5
125C5	121B3	120C6	119D6	PCI_AD<6>	N3	AD6
125C5	121B4	120C6	119D6	PCI_AD<7>	M4	AD7
125C5	121B4	120C6	119D6	PCI_AD<8>	L2	AD8
125C5	121B3	120C6	119D6	PCI_AD<9>	L1	AD9
125B5	121C4	120C6	119D6	PCI_AD<10>	K2	AD10
125B5	121C3	120C6	119D6	PCI_AD<11>	L3	AD11
125B5	121C4	120C6	119D6	PCI_AD<12>	K1	AD12
125B5	121C3	120C6	119D6	PCI_AD<13>	K3	AD13
125B5	121C4	120C6	119D6	PCI_AD<14>	J2	AD14
125B5	121C3	120C6	119D6	PCI_AD<15>	J1	AD15
125B5	121C3	120C6	119D6	PCI_AD<16>	F2	AD16
125B5	121C4	121C1	120C6	119D6 PCI_AD<17>	E1	AD17
125B5	121C3	120C6	119D6	PCI_AD<18>	E3	AD18
125B5	121C4	120C6	119D6	PCI_AD<19>	D2	AD19
125B5	121C3	120C6	119D6	PCI_AD<20>	D1	AD20
	121C4	120C6	119D6	PCI_AD<21>	D3	AD21
	121C3	120C6	119D6	PCI_AD<22>	C2	AD22
	121C4	120B6	119D6	PCI_AD<23>	C1	AD23
125C3	121C3	120B6	119D6	PCI_AD<24>	B2	AD24
125C3	121C4	120B6	119D6	PCI_AD<25>	A2	AD25
125C3	121C3	120B6	119D6	PCI_AD<26>	B1	AD26
125C3	121C4	120B6	119D6	PCI_AD<27> (PCI_AD<27>)	C4	AD27
125C3	121C3	120B6	119D6	PCI_AD<28>	A1	AD28
125C3	121C4	120B6	119D6	PCI_AD<29>	C3	AD29
125C3	121C3	120B6	119D6	PCI_AD<30>	B3	AD30
125C3	121C4	120B6	119D6	PCI_AD<31>	A3	AD31

	121B3	120B6	119D6	PCI_CBE_L<0>	M2	CBE0
	121C4	120B6	119D6	PCI_CBE_L<1>	J3	CBE1
	121C4	120B6	119D6	PCI_CBE_L<2>	F1	CBE2
	121C4	120B6	119D6	PCI_CBE_L<3>	C5	CBE3
	121C3	120B6	119D6	PCI_PAR	J4	PAR
121C3	120B6	119D6	119B2	PCI_FRAME_L	F3	FRAME
121C4	120B6	119D6	119B2	PCI_IRDY_L	F4	IRDY
121C3	120B6	119D6	119A2	PCI_TRDY_L	G1	TRDY
121C3	120B6	119D6	119A2	PCI_STOP_L	G3	STOP
		PCI_SLOTG_IDSEL			B5	IDSEL
121C3	120B6	119D6	119B2	PCI_DEVSEL_L	G2	DEVSEL
		119B7	119B5	PCI_SLOTG_REQ_L	C6	REQ
		119B7	119B5	PCI_SLOTG_GNT_L	D6	GNT
		NEC_PERR_L_PU			H2	PERR
		NEC_SERR_L_PU			H1	SERR (OD)
		NEC_INTA_L			C7	INTA (OD)
		NEC_INTB_L			B7	INTB (OD)
		NEC_INTC_L			A7	INTC (OD)
		122D6 120A3 =PCI_CLK33M_USB2			A8	PCLK
		NEC_VBBRST_L			B8	VBBRST (CHIP RESET)
		NEC_CRUN_L_PD			N6	CRUN
		NEC_PME_L			D5	PME (OD)
					C9	VCCRST (PCI RESET)
		TP_NEC_SMI_L			L6	SMI (OD)
		NEC_LEGC_PD			L7	LEGC

IPD	NTEST1	M8	TP_NEC_NTEST1
IPD	SMC	M7	TP_NEC_SMC
IPD	TEB	N7	TP_NEC_TEB
IPD	AMC	P7	TP_NEC_AMC
IPD	TEST	L8	TP_NEC_TEST
	NANDTEST	M10	TP_NEC_NANDTEST
	SRCLK	M9	TP_NEC_SRCLK
	SRDTA	N9	TP_NEC_SRDATA
IPD	SRMOD	P9	TP_NEC_SRMOD

ALL NETS TO FUNCTIONAL TEST PAGE

RC214 22 5% 1/16W MF-LF 402

122D5 3A7 =PPVIO_PCI_USB2

RC216 10K 5% 1/16W MF-LF 402
RC213 10K 5% 1/16W MF-LF 402

24C6 24B3 24A7 PCI_USB2_INT_L

RPC203 47 5% 1/16W SM-LF (4-5)
RPC203 47 5% 1/16W SM-LF (2-7)
RPC203 47 5% 1/16W SM-LF (3-6)

119A4 29D6 28D4 24B7 21C5 SYS_IO_RESET_L
RC250 47 5% 1/16W MF-LF 402

113A6 28C3 28B1 24B5 21C1 SYS_PME_L
RC251 47 5% 1/16W MF-LF 402

120A3 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

RC215 4.7K 1% 1/16W MF-LF 402
RPC203 47 5% 1/16W SM-LF (8-1)

PPC200 P4MM 3M PP 1
PPC201 P4MM 3M PP 1

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 122 OF 154	

LAST_MODIFIED=Thu May 19 14:26:20 2005

DRAWING

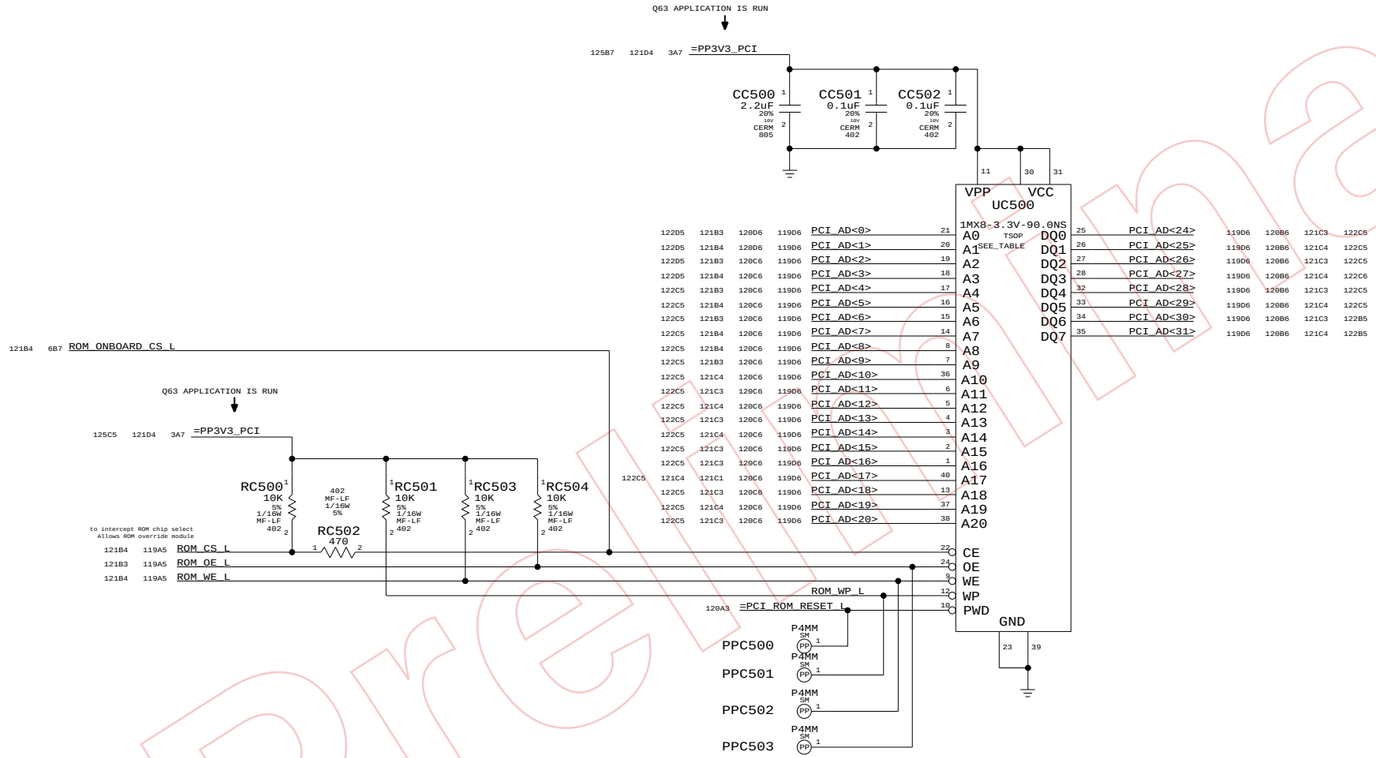
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



LAST_MODIFIED=Thu May 19 14:26:21 2005

DRAWING
TITLE:K11.DWMA
ASSEMSYS:DRAWING

BootROM

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT: 125 OF: 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
	SATA	SATA	SATA_TXD1	SATA_TXD_P1
	SATA	SATA	SATA_TXD1	SATA_TXD_N1
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
	SATA	SATA	SATA_TXD2	SATA_TXD_P2
	SATA	SATA	SATA_TXD2	SATA_TXD_N2
				UATA_DD<15..8>
				UATA_DD<7>
				UATA_DD<6..0>
				UATA_DA<2..0>
				UATA_CS0_L
				UATA_CS1_L
				UATA_HSTROBE
				UATA_STOP
				UATA_DMACK_L
	UATA_NETSPA			UATA_RESET_L
				UATA_DSTROBE
				UATA_DMARQ
				UATA_INTRQ
				UATA_DD_R<15..8>
				UATA_DD_R<7>
				UATA_DD_R<6..0>
				UATA_DA_R<2..0>
				UATA_CS0_L_R
				UATA_CS1_L_R
				UATA_DMACK_L_R
				UATA_HSTROBE_R
				UATA_STOP_R
				UATA_RESET_L_R

Page Notes

Power aliases required by this page:
- _P1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

4-29-05

AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
RPAK PINS WERE REMAPPED FOR BETTER ROUTING AROUND UATA CONNECTOR.

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A (0805)

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
PP1V2_SATA_VDD

CC705 2.2UF 20% 6.3V CERM1 603
CC700 0.1UF 20% 10V CERM 402
CC701 0.1UF 20% 10V CERM 402
CC702 0.1UF 20% 10V CERM 402
CC703 0.1UF 20% 10V CERM 402
CC704 0.1UF 20% 10V CERM 402

XWCC00 (SM) → PP1V2PWRONDISKSB_CC, NO_TEST=YES → P4MM SM (PP) PPCC00

SATA_VDD x 5 (AB14, AB17, T14, M15, Y18)

U2300 SHASTA V1.1 BGA-LF (5 OF 8) SEE_TABLE

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>	
UD_IDEDD_1_H	H7	UATA_DD_R<1>	
UD_IDEDD_2_H	H6	UATA_DD_R<2>	
UD_IDEDD_3_H	E2	UATA_DD_R<3>	
UD_IDEDD_4_H	C1	UATA_DD_R<4>	
UD_IDEDD_5_H	C2	UATA_DD_R<5>	
UD_IDEDD_6_H	E3	UATA_DD_R<6>	
UD_IDEDD_7_H	G6	UATA_DD_R<7>	
UD_IDEDD_8_H	G5	UATA_DD_R<8>	
UD_IDEDD_9_H	D4	UATA_DD_R<9>	
UD_IDEDD_10_H	G7	UATA_DD_R<10>	
UD_IDEDD_11_H	F6	UATA_DD_R<11>	
UD_IDEDD_12_H	C3	UATA_DD_R<12>	
UD_IDEDD_13_H	F5	UATA_DD_R<13>	
UD_IDEDD_14_H	E5	UATA_DD_R<14>	
UD_IDEDD_15_H	D5	UATA_DD_R<15>	
UD_IDEDA0_H	E6	UATA_DA_R<0>	
UD_IDEDA1_H	C4	UATA_DA_R<1>	
UD_IDEDA2_H	D6	UATA_DA_R<2>	
UD_IDECS1FX_L	B3	UATA_CS0_L_R	
UD_IDECS3FX_L	B4	UATA_CS1_L_R	
UD_IDEDMACK_L	E8	UATA_DMACK_L_R	
UD_IDERD_L	E4	UATA_HSTROBE_R	
UD_IDEWR_L	D3	UATA_STOP_R	
UD_IDERST_L	E7	UATA_RESET_L_R	

DSTROBE aka: IORDY/HDMARDY*
HSTROBE aka: DIOR*
STOP aka: DIOW*

UATA_DSTROBE	F9	UD_IDECHRDY_H	
UATA_DMARQ	D7	UD_IDEDMARQ_H	
UATA_INTRQ	C5	UD_IDEINTRQ_H	

SATA 0

SATA_RXD_P1_C	Y17	RXDP1	
SATA_RXD_N1_C	Y16	RXDN1	
		TXDP1	AA16 SATA_TXD_P1
		TXDN1	AB16 SATA_TXD_N1

SATA 1

SATA_RXD_P2_C	AB15	RXDP2	
SATA_RXD_N2_C	AA15	RXDN2	
		TXDP2	Y15 SATA_TXD_P2
		TXDN2	Y14 SATA_TXD_N2

SATA_GND (AA14, AA17, T13, M13)

P4MM SM (PP) PPCC01

PLACE UATA TERMINATION RESISTORS NEAR JC901 CONNECTOR

DIOR- :HDMARDY- :HSTROBE >
DIOW- :STOP >

RC706 33	UATA_RESET_L_R	UATA_RESET_L
RC704 22	UATA_DMACK_L_R	UATA_DMACK_L
RC702 22	UATA_HSTROBE_R	UATA_HSTROBE
RC703 22	UATA_STOP_R	UATA_STOP
RC700 33	UATA_CS0_L_R	UATA_CS0_L
RC701 33	UATA_CS1_L_R	UATA_CS1_L

SPARE
RPC704 33 (3, 6)

RPC704 33 (2, 7)	UATA_DA_R<0>	UATA_DA<0>
RPC704 33 (1, 8)	UATA_DA_R<1>	UATA_DA<1>
RPC704 33 (4, 5)	UATA_DA_R<2>	UATA_DA<2>

RPC700 33 (4, 5)	UATA_DD_R<0>	UATA_DD<0>
RPC700 33 (3, 6)	UATA_DD_R<1>	UATA_DD<1>
RPC700 33 (2, 7)	UATA_DD_R<2>	UATA_DD<2>
RPC700 33 (1, 8)	UATA_DD_R<3>	UATA_DD<3>
RPC701 33 (4, 5)	UATA_DD_R<4>	UATA_DD<4>
RPC701 33 (3, 6)	UATA_DD_R<5>	UATA_DD<5>
RPC701 33 (2, 7)	UATA_DD_R<6>	UATA_DD<6>
RPC701 33 (1, 8)	UATA_DD_R<7>	UATA_DD<7>
RPC702 33 (1, 8)	UATA_DD_R<8>	UATA_DD<8>
RPC702 33 (2, 7)	UATA_DD_R<9>	UATA_DD<9>
RPC702 33 (3, 6)	UATA_DD_R<10>	UATA_DD<10>
RPC702 33 (4, 5)	UATA_DD_R<11>	UATA_DD<11>
RPC703 33 (4, 5)	UATA_DD_R<12>	UATA_DD<12>
RPC703 33 (3, 6)	UATA_DD_R<13>	UATA_DD<13>
RPC703 33 (2, 7)	UATA_DD_R<14>	UATA_DD<14>
RPC703 33 (1, 8)	UATA_DD_R<15>	UATA_DD<15>

RC705 10K 5% 1/16W MF-LF 402

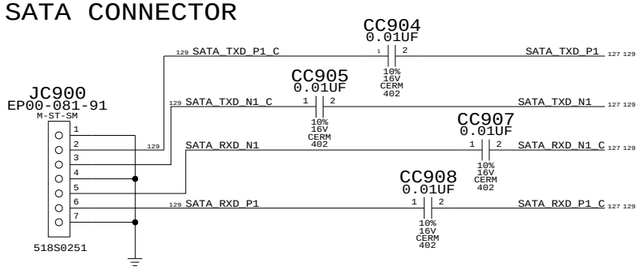
Shasta Disk
SYNC_MASTER=M33-MB SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 127 OF 154	

LAST_MODIFIED=Thu May 19 14:26:22 2005
DRAWING
TITLE=MISCMMAP
ABBREV=SHMISC

SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

SATA_TXD_P2	NC_SATA_TXD_P2	MAKE_BASE=TRUE
SATA_TXD_N2	NC_SATA_TXD_N2	MAKE_BASE=TRUE
SATA_RXD_N2_C	NC_SATA_RXD_N2_C	MAKE_BASE=TRUE
SATA_RXD_P2_C	NC_SATA_RXD_P2_C	MAKE_BASE=TRUE

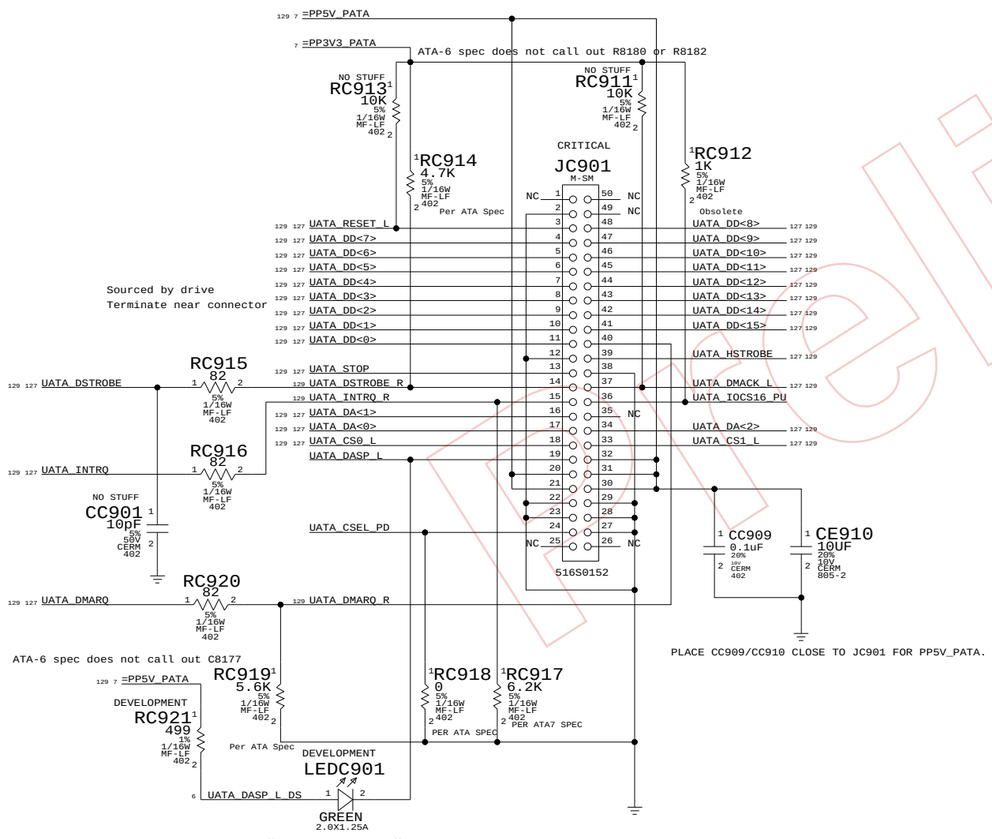
SATA & USB DIFF PAIR GND VIAS

ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA APPROXIMATELY 0.152MM AWAY FROM SIGNAL VIA.

GV901 HOLE-VIA-P5RP25
GV902 HOLE-VIA-P5RP25
GV903 HOLE-VIA-P5RP25
GV904 HOLE-VIA-P5RP25
GV905 HOLE-VIA-P5RP25
GV906 HOLE-VIA-P5RP25
GV907 HOLE-VIA-P5RP25
GV908 HOLE-VIA-P5RP25
GV909 HOLE-VIA-P5RP25
GV910 HOLE-VIA-P5RP25
GV911 HOLE-VIA-P5RP25
GV912 HOLE-VIA-P5RP25
GV913 HOLE-VIA-P5RP25
GV914 HOLE-VIA-P5RP25
GV915 HOLE-VIA-P5RP25
GV916 HOLE-VIA-P5RP25

M33 PATA CONNECTOR

4-12-05



UATA FROM RPAKS TO JC901

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM SHASTA U2300 TO RPAKS

UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA		R392
UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA		R393
UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA		R394
UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA		R395
UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA		R396
UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA		R397
UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA		R398
UATA_STOP_R		UATA_NETPH	UATA_NETSPA		R399
UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA		R400
UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA		R401
UATA_DSTROBE		UATA_NETPH	UATA_NETSPA		R402
UATA_DMARQ		UATA_NETPH	UATA_NETSPA		R403
UATA_INTRQ		UATA_NETPH	UATA_NETSPA		R404
SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M33-MB SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHT 129 OF 154

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	130	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	

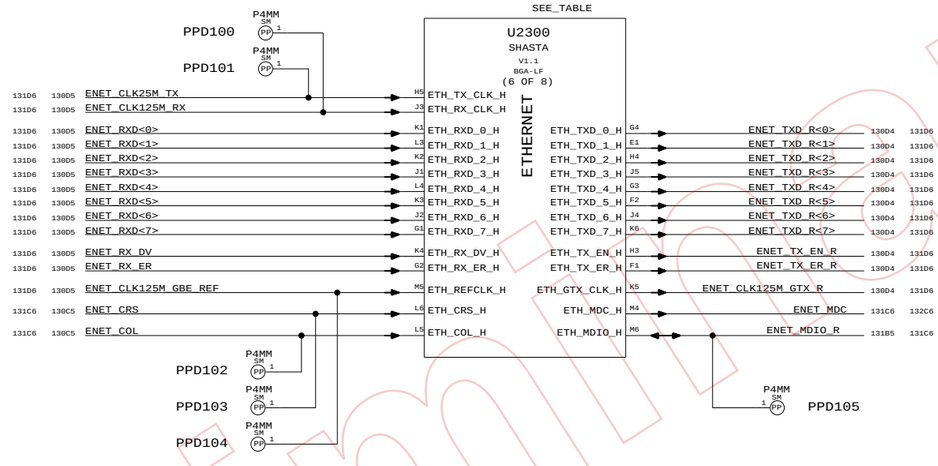
ENET_CLK25M_TX	130D5	131C6		
ENET_CLK125M_RX	130D5	131C6		
ENET_CLK125M_GBE_REF	130D5	131C6		
ENET_CLK125M_GTX	130B6	132C5		
ENET_CLK125M_GTX_R	130D4	131C3		
ENET_RXD_R<7..0>	130B4	130C4	132C3	
ENET_RX_DV_R	130B4	132C3		
ENET_RX_ER_R	130B4	132C3		
ENET_RXD<7..0>	130D5	131C6		
ENET_RX_DV	130D5	131C6		
ENET_RX_ER	130D5	131C6		
ENET_TXD_R<7..0>	130D4	131C3		
ENET_TX_EN_R	130D4	131C3		
ENET_TX_ER_R	130D4	131C3		
ENET_TXD<7..0>	130B6	130C6	132C5	
ENET_TX_EN	130B6	132C5		
ENET_TX_ER	130B6	132C5		
ENET_CRS_R	130B4	132C3		
ENET_COL_R	130B4	132C3		
ENET_CRS	130C5	131C6		
ENET_COL	130C5	131C6		
ENET_MDC	131C3	132C6		
ENET_MDIO	131B3	132C6		
ENET_MDIO_R	131B5	131C3		
R8405_1	131B4			
R8405_2	131B4			
R8407_2	131A4			

Page Notes

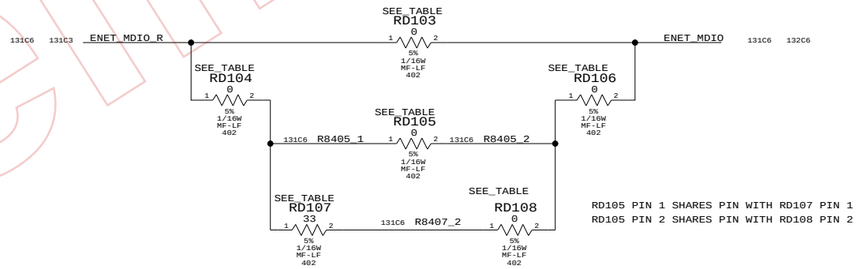
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	131	154

LAST_MODIFIED=Thu May 19 14:01:02 2005

DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TBD	0.38mm SPACING	
TBD	0.38mm SPACING	
TBD	0.38mm SPACING	
TBD	ENET	ENET_MDI0
TBD	ENET	ENET_MDI0
TBD	ENET	ENET_MDI1
TBD	ENET	ENET_MDI1
TBD	ENET	ENET_MDI2
TBD	ENET	ENET_MDI2
TBD	ENET	ENET_MDI3
TBD	ENET	ENET_MDI3
TBD	0.38mm SPACING	
TBD	0.38mm SPACING	
TBD	0.38mm SPACING	

ENET_CLK125M_GBE_REF_R 130C4 132C3
ENET_CLK125M_RX_R 130C4 132C3
ENET_CLK25M_TX_R 130C4 132C3
ENET_MDI_P<0> 130B3 132B1
ENET_MDI_N<0> 130B3 132B1
ENET_MDI_P<1> 130B3 132B1
ENET_MDI_N<1> 130B3 132B1
ENET_MDI_P<2> 130B3 132B1
ENET_MDI_N<2> 130B3 132B1
ENET_MDI_P<3> 130B3 132B1
ENET_MDI_N<3> 130A3 132B1
VESTA_CLK25M_XTALI 132B5
VESTA_CLK25M_XTALO 132A4
VESTA_CLK25M_XTALO_R 132B5

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL
139D5 139D1 3B5 =PP2V5_ENETFW

LD200 FERR-EMI-600-OHM SM
PP2V5_VESTA_BIASVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD201 0.1uF 20% 10V CERM 402

LD201 FERR-EMI-600-OHM SM
PP2V5_VESTA_XTALVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD202 10UF 10% 0.3V X5R 805
CD203 0.001uF 20% 50V CERM 402

XWD200 SM OMIT 6B1 TP_VESTA_BIASVDD1 P4MM SM PPD239
XWD201 SM OMIT 6B1 TP_VESTA_XTALVDD1 P4MM SM PPD201
XWD202 SM OMIT 6B1 TP_VESTA_PLLVDD1 P4MM SM PPD238

PP1V2_VESTA_PLLVDD1 VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD204 0.001uF 20% 50V CERM 402
CD205 10UF 10% 0.3V X5R 805
LD202 FERR-EMI-600-OHM SM
Q63 APPLICATION IS ALL
=PP1V2_ENETFW 3B4 139C1 139D5
VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms

P4MM SM PPD200
131D6 130B6 ENET_CLK125M_GTX

XTALVDD1 BIASVDD1 PLLVDD1

VESTA ENET
U1701
VESTA-V1.3
FBGA-200-LF
2 OF 3

GTXCLK A4 IPD
TXD[0] B6 IPD ← ENET_TXD<0>
TXD[1] C6 IPD ← ENET_TXD<1>
TXD[2] C7 IPD ← ENET_TXD<2>
TXD[3] D6 IPD ← ENET_TXD<3>
TXD[4] E6 IPD ← ENET_TXD<4>
TXD[5] C5 IPD ← ENET_TXD<5>
TXD[6] B5 IPD ← ENET_TXD<6>
TXD[7] A5 IPD ← ENET_TXD<7>
TX_EN B4 IPD ← ENET_TX_EN
TX_ER C4 IPD ← ENET_TX_ER
MDC G1 IPU ← ENET_MDC
MDIO G2 IPU ↔ ENET_MDIO
LOWPWR H5 IPD ← VESTA_ENET_LOWPWR
IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP
PHYA[0] L5 IPD ← TP_VESTA_PHYA<0>
PHYA[1] L4 IPD ← TP_VESTA_PHYA<1>
PHYA[2] L3 IPD ← TP_VESTA_PHYA<2>
PHYA[3] L2 IPD ← TP_VESTA_PHYA<3>
PHYA[4] L1 IPD ← TP_VESTA_PHYA<4>
EN_10B K3 IPD ← TP_VESTA_EN_10B
RGMIIEN B8 IPD ← TP_VESTA_RGMIIEN
FDX C8 IPU ← TP_VESTA_FDX
F1000 K4 IPU ← TP_VESTA_F1000
SPD0 K5 IPD ← TP_VESTA_SPD0
MANMS D9 IPD ← TP_VESTA_MANMS
HUB A9 IPD ← TP_VESTA_HUB
ER H3 IPD ← TP_VESTA_ER
TEST[0] M4 ← TP_VESTA_TEST<0>
TEST[1] M5 ← TP_VESTA_TEST<1>
TVCO N3 ← TP_VESTA_TVCO
XTALI N2 ← VESTA_CLK25M_XTALI
XTALO P2 → VESTA_CLK25M_XTALO_R
XTALGND BIASGND PLLGND1

CLK125 D1 ← ENET_CLK125M_GBE_REF_R 130C4 132D6
TXC A6 ← ENET_CLK25M_TX_R 130C4 132D6
RXC C1 ← ENET_CLK125M_RX_R 130C4 132D6
RXD[0] F4 → ENET_RXD_R<0> 130C4 131D6
RXD[1] F5 → ENET_RXD_R<1> 130B4 131D6
RXD[2] E5 → ENET_RXD_R<2> 130B4 131D6
RXD[3] E4 → ENET_RXD_R<3> 130B4 131D6
RXD[4] E3 → ENET_RXD_R<4> 130B4 131D6
RXD[5] D5 → ENET_RXD_R<5> 130B4 131D6
RXD[6] D4 → ENET_RXD_R<6> 130B4 131D6
RXD[7] D3 → ENET_RXD_R<7> 130B4 131D6
RX_DV D2 → ENET_RX_DV_R 130B4 131D6
RX_ER C2 → ENET_RX_ER_R 130B4 131D6
COL F3 → ENET_COL_R 130B4 131C6
CRS G3 → ENET_CRS_R 130B4 131D6
RBC0 A3 ↔ TP_VESTA_RBC0
RBC1 B3 ↔ TP_VESTA_RBC1
TRD+[0] R4 ↔ ENET_MDI_P<0> 130B3 132D6
TRD-[0] R5 ↔ ENET_MDI_N<0> 130B3 132D6
TRD+[1] R7 ↔ ENET_MDI_P<1> 130B3 132D6
TRD-[1] R6 ↔ ENET_MDI_N<1> 130B3 132D6
TRD+[2] R8 ↔ ENET_MDI_P<2> 130B3 132D6
TRD-[2] R9 ↔ ENET_MDI_N<2> 130B3 132D6
TRD+[3] R11 ↔ ENET_MDI_P<3> 130B3 132D6
TRD-[3] R10 ↔ ENET_MDI_N<3> 130A3 132D6
INTR*/ENERGYDET D10 → ENET_ENERGYDET 24A2 24B3
SLAVE*/AN_EN C10 ← TP_VESTA_AN_EN
QUALITY*/TXC_RXC_DELAY A8 ← TP_VESTA_TXC_RXC_DELAY
LINK1* A10 → TP_VESTA_LINK1_L
LINK2* B11 → TP_VESTA_LINK2_L
FDXLED* B10 → TP_VESTA_FDXLED_L
XMTLED* B12 → TP_VESTA_XMTLED_L
ACTLED* A11 → TP_VESTA_ACTLED_L
RDAC1 R1 VESTA_RDAC1_PD

TERMINATION OFF PAGE

Q63 APPLICATION IS ALL
140B4 139D1 139C6 139A6 139A1 17D7 17B8 17B1 17A6 3B6 =PP3V3_ENETFW
RD204 1K 1% 1/10W MF-LF 402
QD200 2N7002DW-X-F SOT-363
132C6 3A3 =PP3V3_ENET
CD206 1UF 10% 6.3V CERM 402
17A6 VESTA_RESET_H
QD200 2N7002DW-X-F SOT-363

132B7 3A3 =PP3V3_ENET
RD250 1.5K 5% 1/10W MF-LF 402
131C6 131C3 ENET_MDC
131C6 131B3 ENET_MDIO
VESTA_ENET_LOWPWR

Put crystal circuit close to PHY
132D6 VESTA_CLK25M_XTALI
132D6 VESTA_CLK25M_XTALO_R
RD209 0 5% 1/16W MF-LF 402
CRITICAL
YD200 25.0000M SM-2
VESTA_CLK25M_XTALO 132D6
CD218 33pF 5% 50V CERM 402
CD219 33pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 20PF
RD213 1.24K 1% 1/16W MF-LF 402

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07
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LAST_MODIFIED=Thu May 19 14:26:25 2005
DRAWING:

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

U292	ENET	ENET_MDI_P<0>	132 136
U296	ENET	ENET_MDI_N<0>	132 136
U297	ENET	ENET_MDI_P<1>	132 136
U298	ENET	ENET_MDI_N<1>	132 136
U299	ENET	ENET_MDI_P<2>	132 136
U300	ENET	ENET_MDI_N<2>	132 136
U301	ENET	ENET_MDI_P<3>	132 136
U302	ENET	ENET_MDI_N<3>	132 136

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD601 330 5% 1/10W MF-LF 603
LED8700_P
DEVELOPMENT
LEDD600 GREEN 2.0X1.25A

132 TP_VESTA_XMTLED_L — VESTA_XMTLED_L MAKE_BASE=TRUE

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>
RD604 49.9 1% 1/16W MF-LF 402
RD605 49.9 1% 1/16W MF-LF 402
ENET_MDI0
136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>
CD606 0.01UF 20% 16V CERM 402
RD606 49.9 1% 1/16W MF-LF 402
RD607 49.9 1% 1/16W MF-LF 402
ENET_MDI1
136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>
RD608 49.9 1% 1/16W MF-LF 402
RD609 49.9 1% 1/16W MF-LF 402
CD607 0.01UF 20% 16V CERM 402
ENET_MDI2
136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>
CD608 0.01UF 20% 16V CERM 402
RD610 49.9 1% 1/16W MF-LF 402
RD611 49.9 1% 1/16W MF-LF 402
ENET_MDI3
CD609 0.01UF 20% 16V CERM 402

LD600 FERR-EMI-600-OHM SM
7 =PP2V5_ENET
PP2V5_ENET_CTAP MIN_LINE_WIDTH=0.58mm MIN_NECK_WIDTH=0.38mm VOLTAGE=2.5V
CD600 0.1UF 20% 10V CERM 402
CD601 0.1UF 20% 10V CERM 402
7 GND_CHASSIS_RJ45
CD604 0.001UF 10% 50V CERM 402
CD605 0.001UF 10% 50V CERM 402

(514-0253)
OMIT
JD600 JFM38V10-0112-4F F-ANG-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
RJ45 CHIP SIDE

1CT:1CT
75 OHM
SECONDARY
J1 J2 J3 J4 J5 J6 J7 J8
RJ45 CABLE SIDE
SHIELD 1000PF, 2000V

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD603 330 5% 1/10W MF-LF 603
LED8701_P
DEVELOPMENT
LEDD601 GREEN 2.0X1.25A

132 TP_VESTA_ACTLED_L — VESTA_ACTLED_L MAKE_BASE=TRUE

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE-VIA
ZHD691 HOLE-VIA
ZHD692 HOLE-VIA
ZHD693 HOLE-VIA

ETHERNET CONNECTOR

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_2X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	ENET_FW_3X	
	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

FW_DATA<7..0> 138B4 138C4 139B7 139C7
FW_CTL_S<1..0> 138B4 139D6
FW_CTL<1..0> 138B2 139A4 139A6 139B7 139D6
FW_DATA_R<7..0> 139B5 139C5
FW_CTL_R<1..0> 139B5 139D6
FW_LPS 138B4 139B5
FW_LREQ 138B4 139B5
FW_PINT 138B5 139C3
FW_CLK98M_LCLK 138B2 139C5
FW_CLK98M_PCLK 138B5 139C1
FW_CLK98M_LCLK_R 138B4

119C3 24D5 23C2 23B2 3C1 =PP2V5_PWRON_SB

CD800 0.1uF 20% 10V CERM 402
CD801 0.1uF 20% 10V CERM 402
CD802 0.1uF 20% 10V CERM 402

N5 J7 A4 FWVDDP

U2300
SHASTA
V1.1
BGA-LF
SEE_TABLE
(7 OF 8)
FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	138D6	139C7
PHY_DATA_1_H	P5	FW_DATA<1>	138D6	139C7
PHY_DATA_2_H	N1	FW_DATA<2>	138D6	139C7
PHY_DATA_3_H	M7	FW_DATA<3>	138D6	139B7
PHY_DATA_4_H	N6	FW_DATA<4>	138D6	139B7
PHY_DATA_5_H	L1	FW_DATA<5>	138D6	139B7
PHY_DATA_6_H	M3	FW_DATA<6>	138D6	139B7
PHY_DATA_7_H	L2	FW_DATA<7>	138D6	139B7
PHY_CTL_0_H	N2	139D6 138D6 FW_CTL_S<0>		
PHY_CTL_1_H	N3	139D6 138D6 FW_CTL_S<1>		
PHY_LPS_H	P6	FW_LPS	138D6	139B5
PHY_LREQ_H	P1	FW_LREQ	138D6	139B5
PHY_SCLK_H	P2	139C1 138D6 FW_CLK98M_PCLK		
PHY_PINT_L	P3	139C3 138D6 FW_PINT		
PHY_LCLK_H	R1	138D6 FW_CLK98M_LCLK_R		
PHY_LINKON_L	N7	FW_LINKON	139C3	

RD801 0 5% 1/16W MF-LF 402 — PHY_CTL_0_H → FW_CTL<0> 138D6 139A4 139A6 139B7 139D6
RD802 0 5% 1/16W MF-LF 402 — PHY_CTL_1_H → FW_CTL<1> 138D6 139A4 139A6 139B7 139D6
RD800 22 5% 1/16W MF-LF 402 — PHY_LCLK_H → FW_CLK98M_LCLK 138D6 139C5

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

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D	051-6863	07
SCALE: NONE	SHT 138 OF 154	

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DRAWING
TYPE:SCHEMATIC
ASSEMBLY:DEMUTAG

<XR_PAGE_TITLE>

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
(PROVIDED BY LINK PAGE)		0.38mm SPACING	
	FW	FW	FW_TPA0
	FW	FW	FW_TPA0
	FW	FW	FW_TPB0
	FW	FW	FW_TPB0
	FW	FW	FW_TPA1
	FW	FW	FW_TPA1
	FW	FW	FW_TPB1
	FW	FW	FW_TPB1
ETHERNET SPACING TO ROUTE ON LAYER 8			
	FW	FW	FW_TPA2
	FW	FW	FW_TPA2
	FW	FW	FW_TPB2
	FW	FW	FW_TPB2
		0.38mm SPACING	
		0.38mm SPACING	
		0.38mm SPACING	
	FW_CTL		
	FW_CTL		
	FW_CTL		

FW_CLK98M_PCLK_R	139C3	
FW_TPA_P<0>	139B2	140A5 140B8
FW_TPA_N<0>	139B2	140A5 140B8
FW_TPB_P<0>	139B2	140A5 140B8
FW_TPB_N<0>	139B2	140A5 140B8
FW_TPA_P<1>	139B2	140A5 140B8
FW_TPA_N<1>	139B2	140A5 140A8
FW_TPB_P<1>	139B2	140A5 140A8
FW_TPB_N<1>	139B2	140A5 140A8
FW_TPA_P<2>	139B2	140A5 140B8
FW_TPA_N<2>	139B2	140A5 140B8
FW_TPB_P<2>	139B2	140A5 140B8
FW_TPB_N<2>	139B2	140A5 140B8
VESTA_CLK24M_XTALI	139B5	
VESTA_CLK24M_XTALO	139A4	
VESTA_CLK24M_XTALO_R	139B5	
FW_CTL_S<1..0>	138B4	138D6
FW_CTL<1..0>	138B2	138D6 139A4 139A6 139B7
FW_CTL_R<1..0>	138D6	139B5

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

ESDET[0]
1=PORTS 1 AND 2 DS ONLY
0=PARTS 1 AND 2 BI-LINGUAL
ESDET[1]
1=PORT 1 PRESENT
0=PORT 1 NOT PRESENT
ESDET[2]
1=PORT 2 PRESENT
0=PORT 2 NOT PRESENT

CRYSTAL LOAD CAPACITANCE IS 12PF

IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP

LAST_MODIFIED=Thu May 19 14:26:28 2005

SYNC_MASTER=Q63	SYNC_DATE=05/19/2005

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Vesta FireWire PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 139 OF 154	

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
T401	FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL
T400	FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL
T402	FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL
T403	FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL
T493	FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL
T495	FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL
T497	FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL
T496	FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL

=PP12V_ALL_FW

8 WATTS MAX
12 VOLTS

RE056 1.3 20% 1W FF 2512 — PP12V_FW (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V, MAKE_BASE=TRUE)

I443 =PPFW_PHY

TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XXG SMC — FW_VP_R (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, MAKE_BASE=TRUE, VOLTAGE=24V)

CE009 0.1UF 10% 50V X7R 603-1

FW_VP MAX IS 24V

CRITICAL
RE002 1.3 20% 1W FF 2512 — FW_VP (MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=24V)

FE002 0.75AMP-13.2V MINISMD — PPFW_PORT0_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

FE000 1.5AMP-33V SM — PPFW_PORT1_VP (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
FW_TPBIAS<1>
FW_TPBIAS<0>
VOLTAGE=1.86V

CE050 1UF 10% 6.3V CERM 402
CE060 1UF 10% 6.3V CERM 402

RE050 56.2 1% 1/10W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/10W MF-LF 402

FW_TPA_P<0>	MAKE_BASE=TRUE	FW_PORT0_TPA_P	
FW_TPA_N<0>	MAKE_BASE=TRUE	FW_PORT0_TPA_N	
FW_TPB_P<0>	MAKE_BASE=TRUE	FW_PORT0_TPB_P	
FW_TPB_N<0>	MAKE_BASE=TRUE	FW_PORT0_TPB_N	
FW_TPA_P<1>	MAKE_BASE=TRUE	FW_PORT1_TPA_P	
FW_TPA_N<1>	MAKE_BASE=TRUE	FW_PORT1_TPA_N	
FW_TPB_P<1>	MAKE_BASE=TRUE	FW_PORT1_TPB_P	
FW_TPB_N<1>	MAKE_BASE=TRUE	FW_PORT1_TPB_N	

RE052 56.2 1% 1/10W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/10W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V — CE054 270pF 5% 25V CERM 402 — RE054 4.99K 1% 1/16W MF-LF 402
FW_TPA_C<1> VOLTAGE=0V — CE064 270pF 5% 25V CERM 402 — RE064 4.99K 1% 1/16W MF-LF 402

3rd TPA/TPB pair unused

FW_TPBIAS<2>	NC_FW_TPBIAS2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPA_P<2>	NC_FW_TPA_P2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPA_N<2>	NC_FW_TPA_N2	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPB_P<2>	FW_TPB2_PD	MAKE_BASE=TRUE, NO_TEST=YES
FW_TPB_N<2>		

RE070 1K 5% 1/10W MF-LF 402

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

=PP3V3_FW — RE090 215 1% 1/10W MF-LF 402 — PP3V3_FW_ESD_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — LE090 400-OHM-EMI SM-1 — PP3V3_FW_ESD (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD

DPE010 BAV99DW-X-F SOT-363

CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

FLE010 120-OHM 2012
FLE011 120-OHM 2012

FW_PORT0_TPA_P	FW_PORT0_TPA_P_FL
FW_PORT0_TPA_N	FW_PORT0_TPA_N_FL
FW_PORT0_TPB_P	FW_PORT0_TPB_P_FL
FW_PORT0_TPB_N	FW_PORT0_TPB_N_FL

PP3V3_FW_ESD

DPE011 BAV99DW-X-F SOT-363

CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

LE010 FERR-160-OHM 1206-LF

PORT 0
1394A
OMIT

JE000 UF01613-M33-4F F-ST-TH

TPO	(TPA+)
TPO#	(TPA-)
TPI	(TPB+)
TPI#	(TPB-)
VP	
VGND	

PPFW_PORT0_VP_FL (VOLTAGE=24V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm)

FW_VP MAX IS 24V
CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE

"Snapback" & "Late VG" Protection

PP3V3_FW_ESD

DPE020 BAV99DW-X-F SOT-363

CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

FLE020 120-OHM 2012
FLE021 120-OHM 2012

FW_PORT1_TPA_P	FW_PORT1_TPA_P_FL
FW_PORT1_TPA_N	FW_PORT1_TPA_N_FL
FW_PORT1_TPB_P	FW_PORT1_TPB_P_FL
FW_PORT1_TPB_N	FW_PORT1_TPB_N_FL

PP3V3_FW_ESD

DPE021 BAV99DW-X-F SOT-363

CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

GND_CHASSIS_FIREWIRE

PPFW_PORT1_VP

LE020 FERR-160-OHM 1206-LF

PORT 1
1394A
OMIT

JE001 UF01613-M33-4F F-ST-TH

TPO	(TPA+)
TPO#	(TPA-)
TPI	(TPB+)
TPI#	(TPB-)
VP	
VGND	

PPFW_PORT1_VP_FL (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=24V)

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN

GND_CHASSIS_FIREWIRE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 140 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_2
	USB2	USB2	USB2_3
	USB2	USB2	USB2_3
	USB2	USB2	USB2_4
	USB2	USB2	USB2_4
	0.38mm SPACING		
	0.38mm SPACING		
	0.38mm SPACING		

USB2_P<0> 142C2 143D1 143D8
USB2_N<0> 142C2 143D1 143D8
USB2_P<1> 6B7 142C2 143C8 143D1
USB2_N<1> 6B7 142C2 143C8 143D1
USB2_P<2> 142B2 143B8 143D1
USB2_N<2> 142B2 143B8 143D1
USB2_P<3> 142B2 143A8 143D1
USB2_N<3> 142B2 143A8 143D1
USB2_P<4> 142A2 143A4 143D1
USB2_N<4> 142A2 143A4 143D1
NEC_CLK30M_XT1 142A5
NEC_CLK30M_XT2 142A5
NEC_CLK30M_XT2_R 142A5

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

U2300
SHASTA
V1.1
BGA-LF
(8 OF 8)

NC0 P7 TP_SB<0>
NC1 P8 TP_SB<1>
NC2 R3 TP_SB<2>
NC3 R4 TP_SB<3>
NC4 R5 TP_SB<4>
NC5 R6 TP_SB<5>
NC6 R7 TP_SB<6>
NC7 R8 TP_SB<7>
NC8 T1 TP_SB<8>
NC9 T2 TP_SB<9>
NC10 T3 TP_SB<10>
NC11 T4 TP_SB<11>
NC12 T5 TP_SB<12>
NC13 T6 TP_SB<13>
NC14 T7 TP_SB<14>
NC15 T8 TP_SB<15>
NC16 U1 TP_SB<16>
NC17 U2 TP_SB<17>
NC18 U3 TP_SB<18>
NC19 U4 TP_SB<19>
NC20 U5 TP_SB<20>
NC21 U6 TP_SB<21>
NC22 V1 TP_SB<22>
NC23 V2 TP_SB<23>
NC24 V3 TP_SB<24>
NC25 V4 TP_SB<25>
NC26 W1 TP_SB<26>
NC27 W3 TP_SB<27>
NC28 Y1 TP_SB<28>
NC29 Y3 TP_SB<29>

142C6 142B6 3A3 =PP3V3_PWRON_USB
LE235 FERR-EMI-100-OHM SM
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
RE235 4.7 5% 1/16W MF-LF 603
CE235 10UF 10% 6.3V X5R 805
CE236 0.1uF 20% 10V CERM 402
CE237 0.1uF 20% 10V CERM 402
XWE200 OMIT SM
TP_NEC_AVDD
P4MM SM PP
PPE2000
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
GND_NEC_AVSS_R 6B1 142A2
CE220 10UF 10% 6.3V X5R 805
CE221 CE222 CE223 CE224 CE225 0.1uF 20% 10V CERM 402
CE226 CE227 CE228 CE229 CE230 0.1uF 20% 10V CERM 402
P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7
VDD
N10 N12
AVDD

UC200
NEC_UPD720101_USB
FBGA-LF

RSDM1 M14 USB_NEC_N<0>
DM1 M13 (USB2_N<0>)
DP1 L14 (USB2_P<0>)
RSDP1 K13 USB_NEC_P<0>
RE200 36 1% 1/16W MF-LF 402
RE201 36 1% 1/16W MF-LF 402
USB2_N<0> 142D6 143D1 143D8
USB2_P<0> 142D6 143D1 143D8

P4MM SM PP
PPE2002
RSDM2 K14 USB_NEC_N<1>
DM2 K12 (USB2_N<1>)
DP2 J14 (USB2_P<1>)
RSDP2 J12 USB_NEC_P<1>
RE202 36 1% 1/16W MF-LF 402
RE203 36 1% 1/16W MF-LF 402
USB2_N<1> 6B7 142D6 143C8 143D1
USB2_P<1> 6B7 142D6 143C8 143D1

P4MM SM PP
PPE2001
RSDM3 H11 USB_NEC_N<2>
DM3 G11 (USB2_N<2>)
DP3 G13 (USB2_P<2>)
RSDP3 G14 USB_NEC_P<2>
RE204 36 1% 1/16W MF-LF 402
RE205 36 1% 1/16W MF-LF 402
USB2_N<2> 142D6 143B8 143D1
USB2_P<2> 142D6 143B8 143D1
40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

RSDM4 F12 USB_NEC_N<3>
DM4 F14 (USB2_N<3>)
DP4 E12 (USB2_P<3>)
RSDP4 E14 USB_NEC_P<3>
RE206 36 1% 1/16W MF-LF 402
RE207 36 1% 1/16W MF-LF 402
USB2_N<3> 142D6 143A8 143D1
USB2_P<3> 142D6 143A8 143D1

RSDM5 E13 USB_NEC_N<4>
DM5 D14 (USB2_N<4>)
DP5 C13 (USB2_P<4>)
RSDP5 C14 USB_NEC_P<4>
RE208 36 1% 1/16W MF-LF 402
RE209 36 1% 1/16W MF-LF 402
USB2_N<4> 142D6 143A4 143D1
USB2_P<4> 142D6 143A4 143D1
BLUTOOTH CONNECTOR,(PORT #4)

142D5 142B6 3A3 =PP3V3_PWRON_USB
RE210 33K 5% 1/16W MF-LF 402
RPE210 10K 5% 1/16W SM-LF
USB2_OC<0> 143B4 (USB2_OC<0>) B12 OCI1
USB2_OC<1> 143B4 (USB2_OC<1>) B11 OCI2
USB2_OC<2> 143B4 (USB2_OC<2>) B10 OCI3
USB2_OC<3> 143B4 (USB2_OC<3>) A10 OCI4
USB2_OC<4> 121B6 (USB2_OC<4>) B9 OCI5
USB2_PWREN<0> 143B2 C12 PPON1
USB2_PWREN<1> 143B2 A11 PPON2
USB2_PWREN<2> 143B2 C11 PPON3
USB2_PWREN<3> 143B2 C10 PPON4
USB2_PWREN<4> 143B2 A9 PPON5

142D5 142C6 3A3 =PP3V3_PWRON_USB
RE240 1.5K 5% 1/16W MF-LF 402
RE241 1.5K 5% 1/16W MF-LF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

142D6 NEC_CLK30M_XT1 L9 XT1/SCLK
142D6 NEC_CLK30M_XT2_R P8 XT2
RE245 100 1% 1/16W MF-LF 402
CRITICAL
YE245 30.0000M SM-1
NEC_CLK30M_XT2
CE245 22pF 5% 50V CERM 402
CE246 22pF 5% 50V CERM 402
SPEC SHOWS LOAD CAPACITANCE OF 16PF

142D6
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8
VSS
XWE201 SM OMIT
P13 M12 N11
AVSS
AVSS(R)
Tie to GND at ball N11

RREF P11 NEC_RREF_PD
RE238 9.09K 1% 1/16W MF-LF 402
MINIMIZE TRACE LENGTH TO PINS
GND_NEC_AVSS_R VOLTAGE=0V 6B1 142D3
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

USB Host Interfaces

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 142 OF 154	

LAST_MODIFIED=Thu May 19 14:26:30 2005

DRAWING
TITLE=XCLDWWA
ABBREV=DRAWING

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- USB2_PWREN<0> — TP_USB2_PWREN<0> MAKE_BASE=TRUE
- USB2_PWREN<1> — TP_USB2_PWREN<1> MAKE_BASE=TRUE
- USB2_PWREN<2> — TP_USB2_PWREN<2> MAKE_BASE=TRUE
- USB2_PWREN<3> — TP_USB2_PWREN<3> MAKE_BASE=TRUE
- USB2_PWREN<4> — TP_USB2_PWREN<4> MAKE_BASE=TRUE

External USB Ports

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0247	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0250	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F
	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F
	USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2>
	USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2>
	USB2	USB2_BNDI_F	USB2	USB2_P_L<3>
	USB2	USB2_BNDI_F	USB2	USB2_N_L<3>

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT

SENDS USB HUB PORT 3 TO BLUETOOTH MODULE

USB HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEED HERE

USB Device Interfaces

SYNC_MASTER=FINO-MB SYNC_DATE=05/19/2005

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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 143 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
	0.38MM SPACING			XTAL_IN_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER
	0.38MM SPACING			XTAL_OUT_CARD_READER_R
	0.38MM SPACING			XTAL_IN_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB
	0.38MM SPACING			XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

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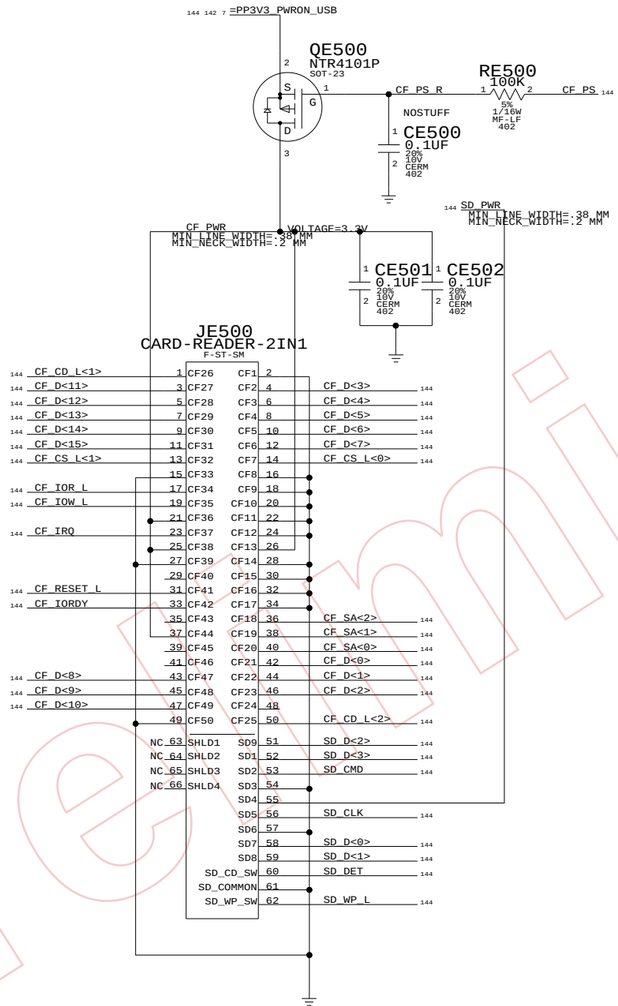
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 144 OF 154	



Flash Connector

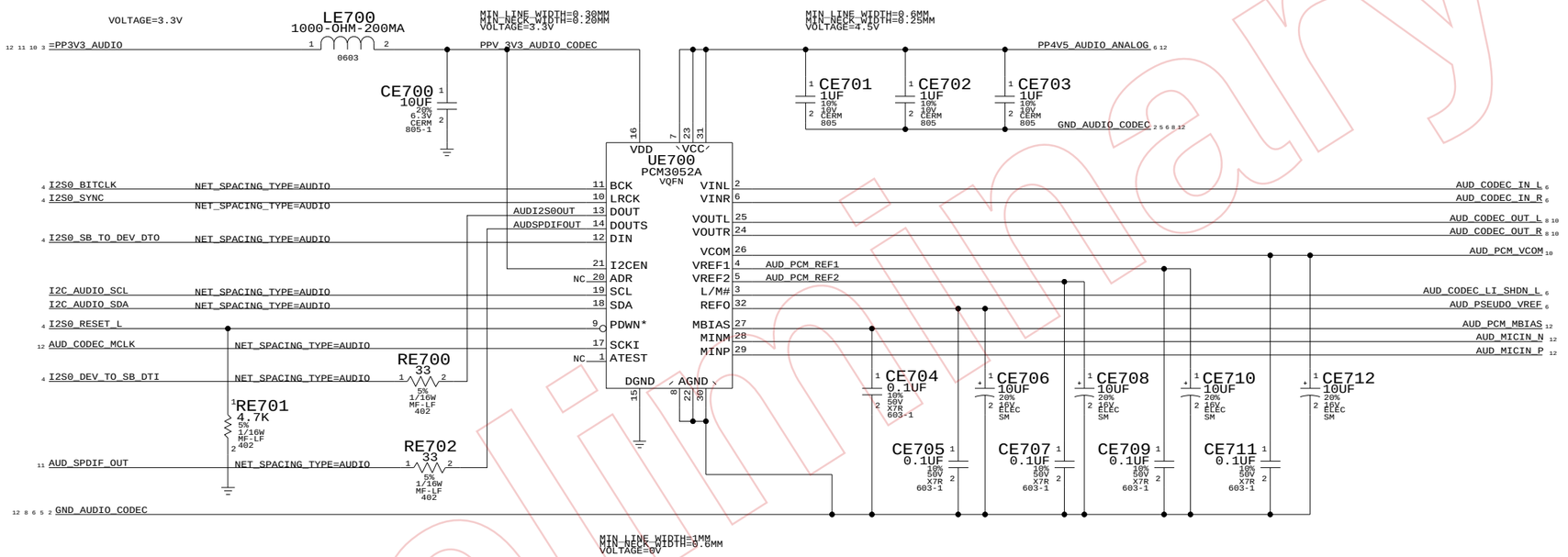
SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	145	154

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

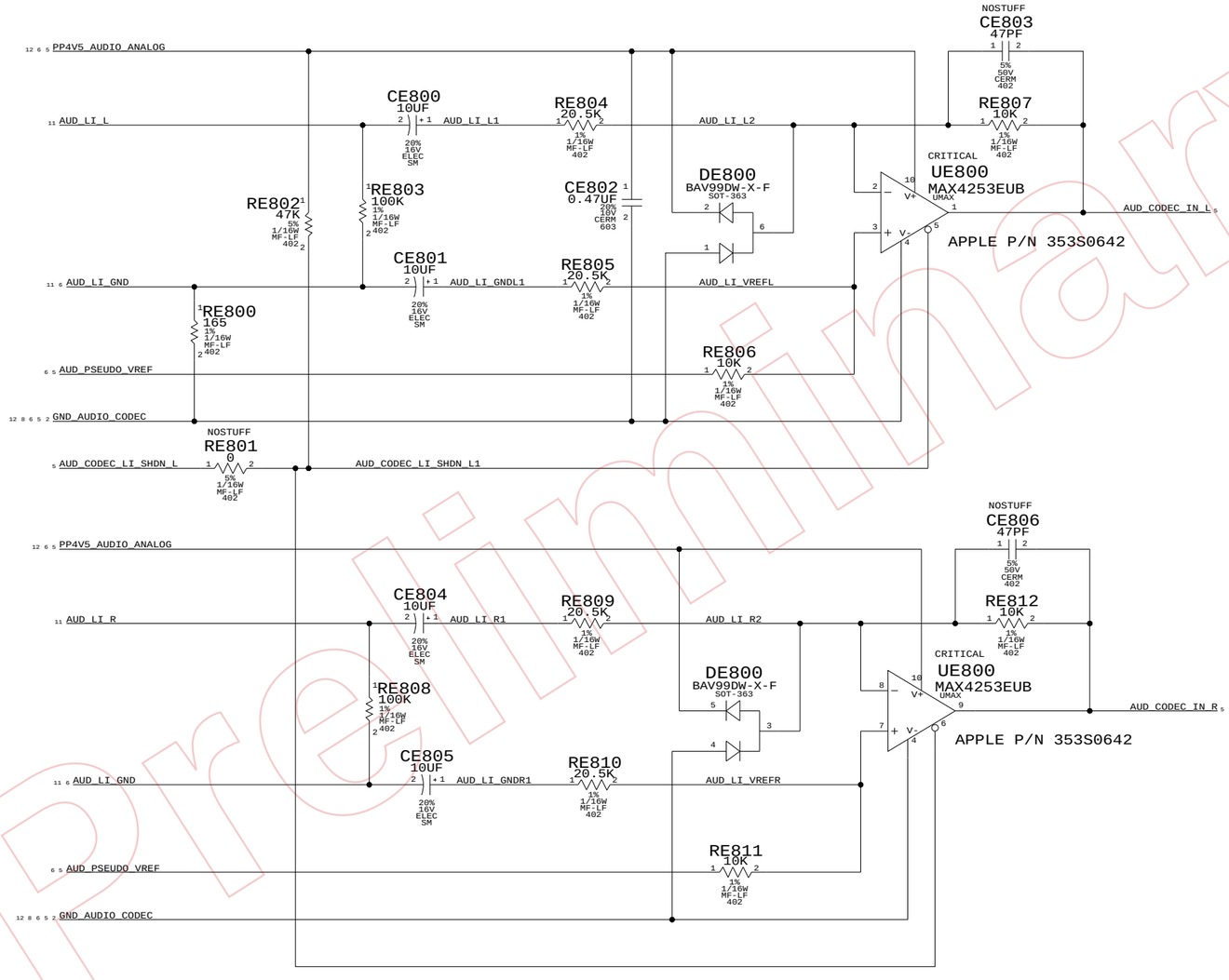
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	147	154

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

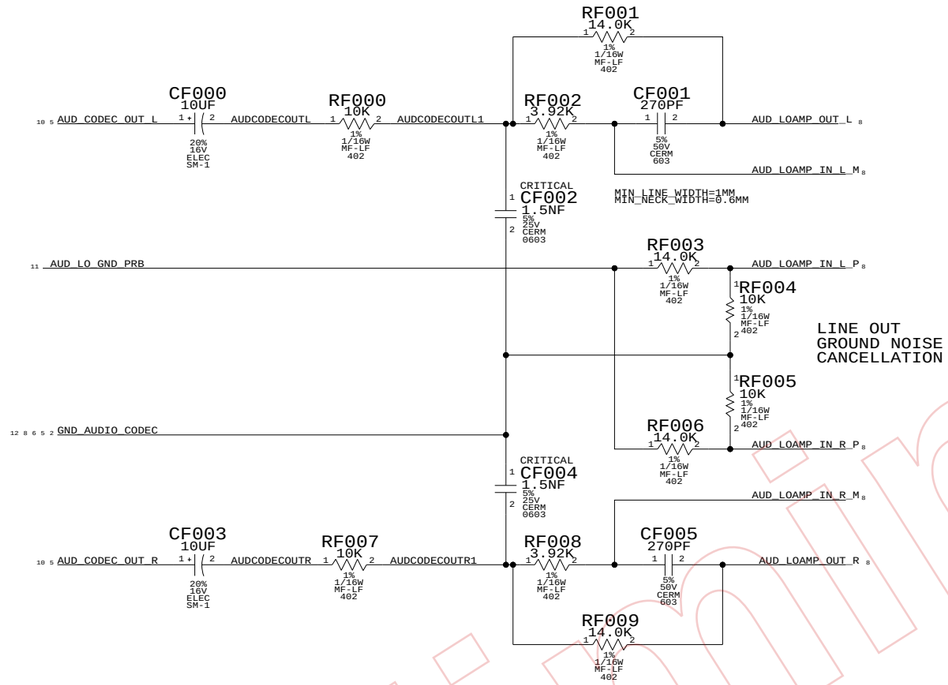
SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 148 OF 154	

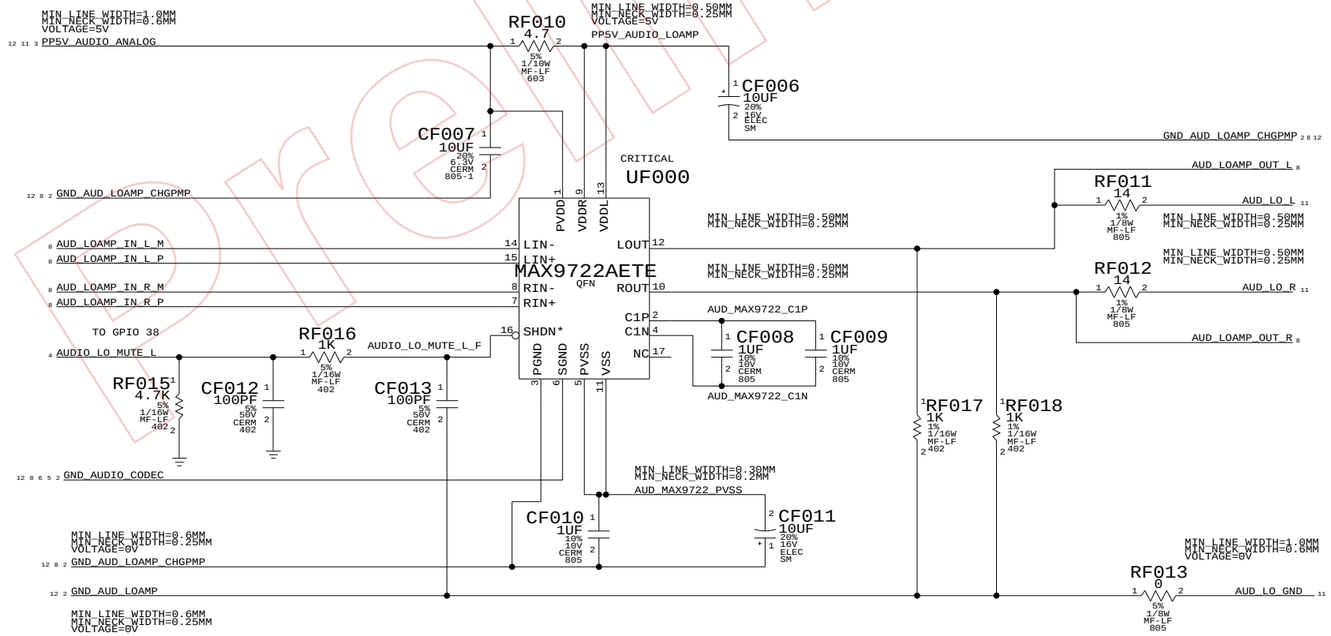
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

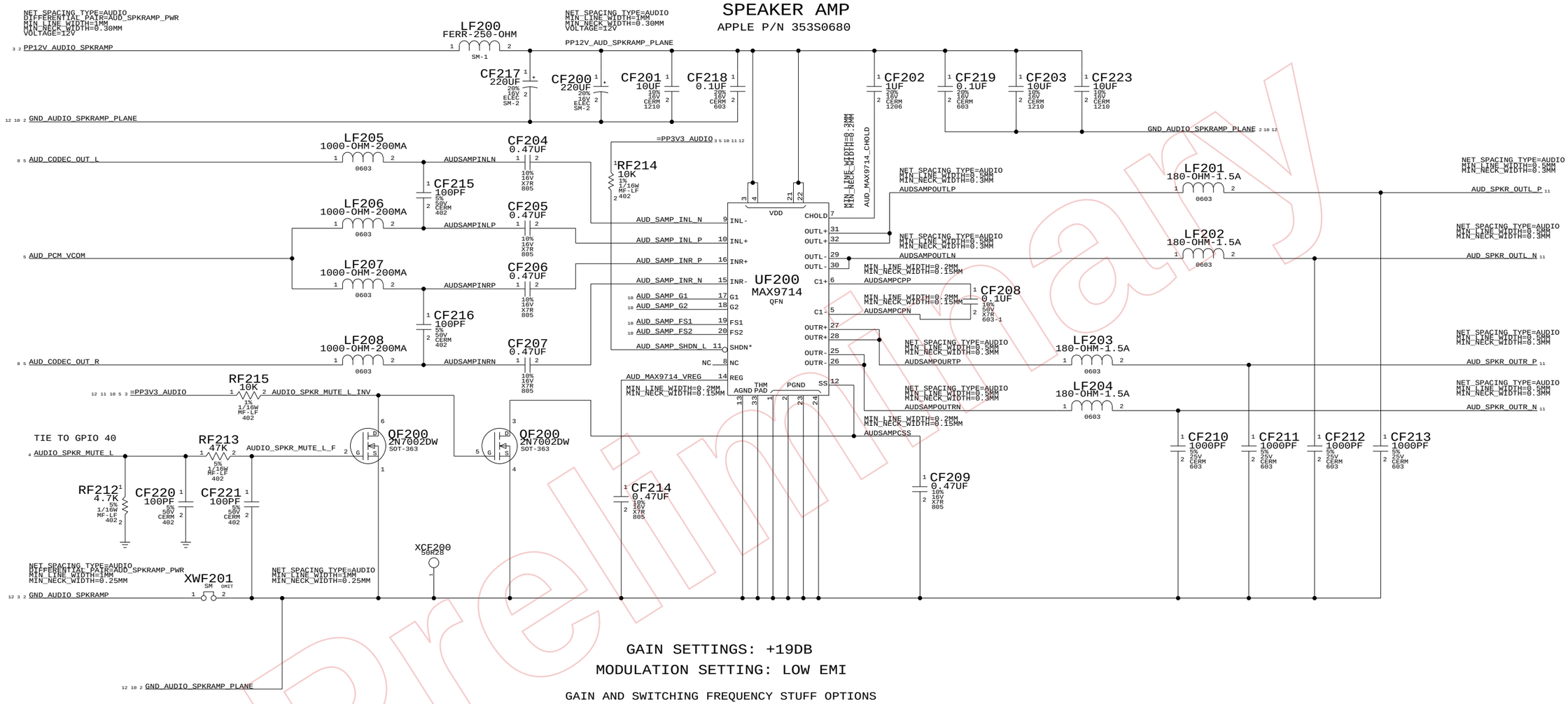
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT OF
NONE	150 154

SPEAKER AMP

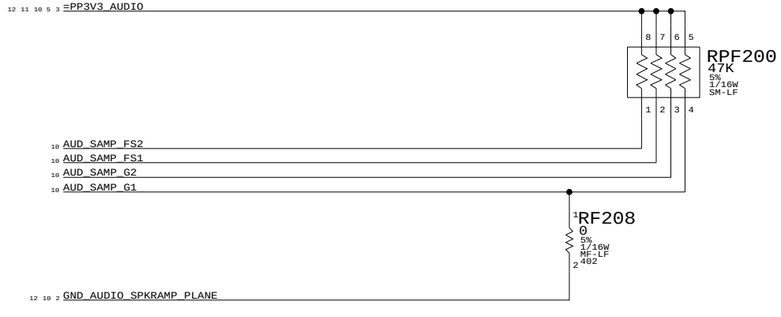
APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

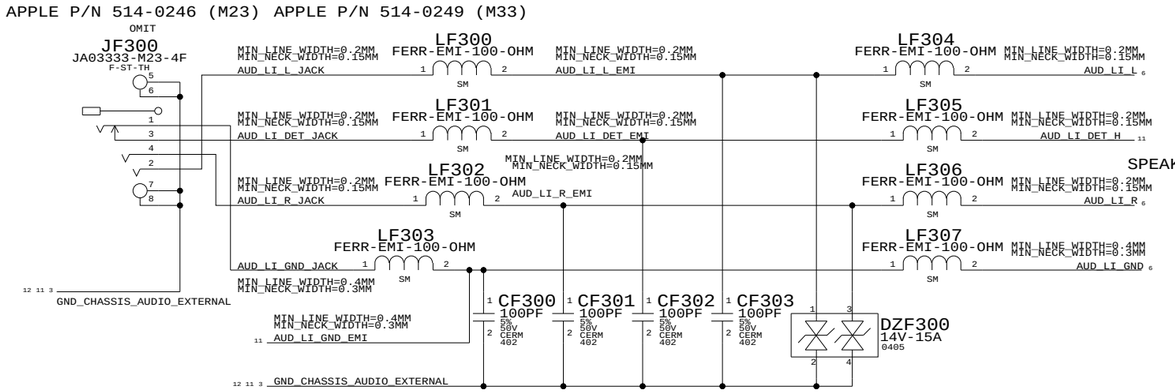
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE	SHT	OF
NONE	152	154

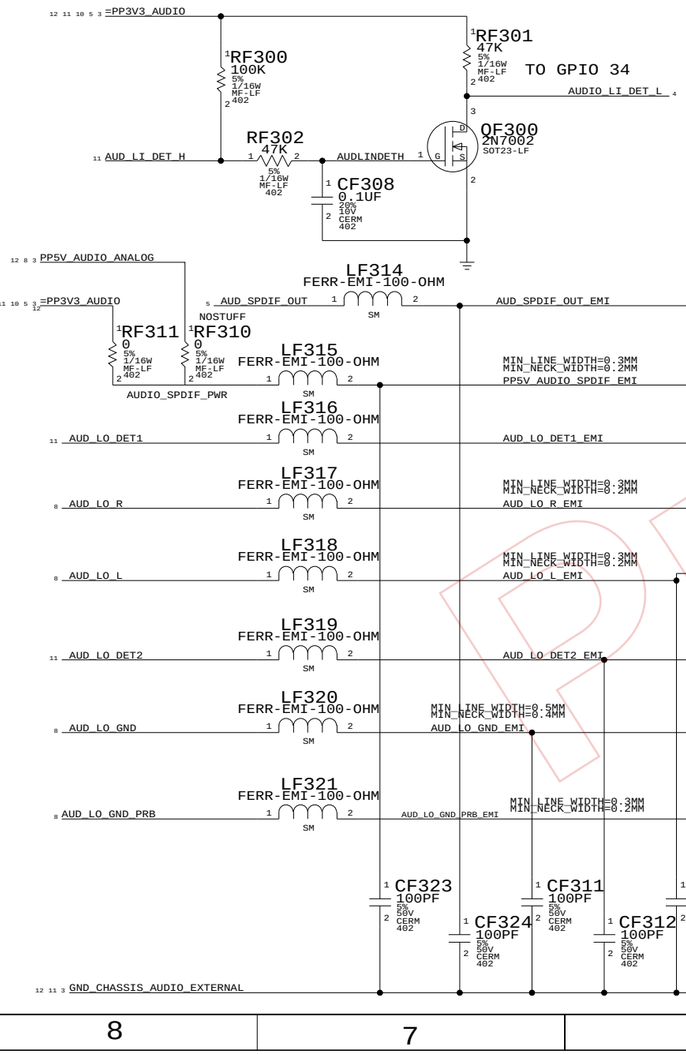
LINE IN JACK

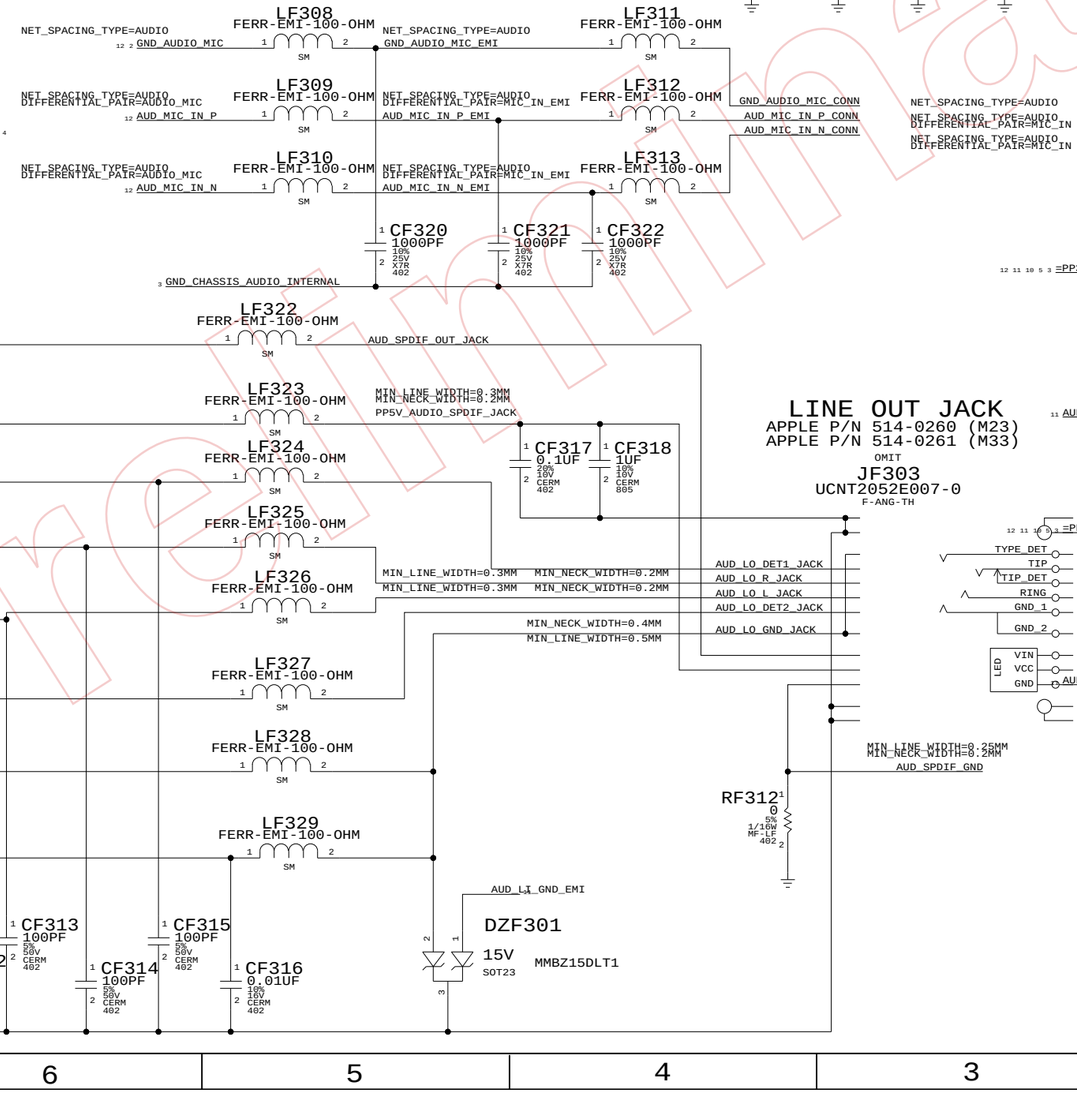
APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)



LINE IN PLUG DETECT

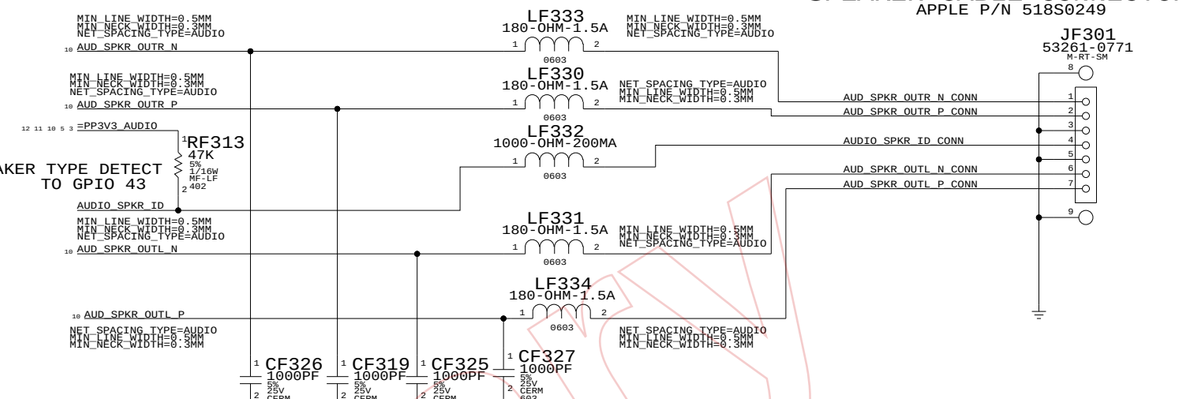
AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED





SPEAKER CABLE CONNECTOR

APPLE P/N 518S0249

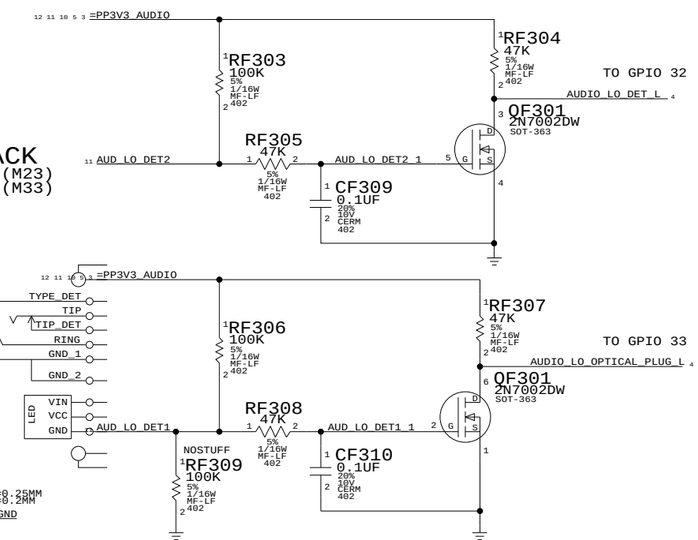


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

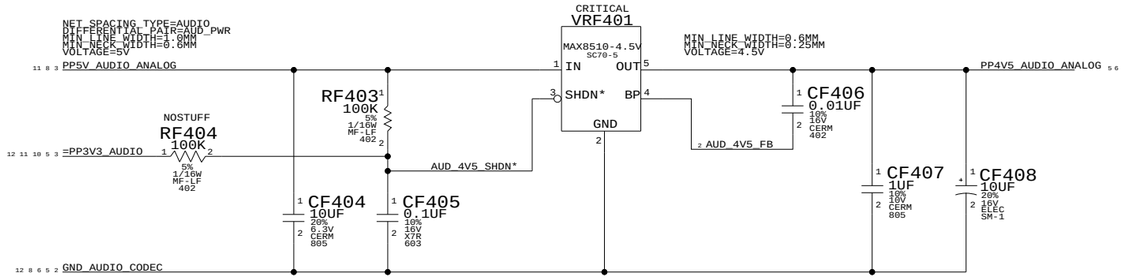
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 153 OF 154	

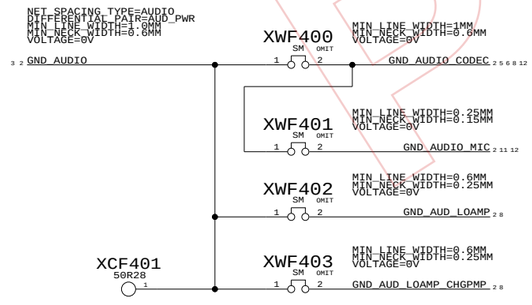
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

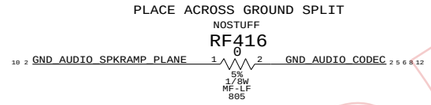
APPLE P/N 353S0733



AUDIO GROUND RETURNS

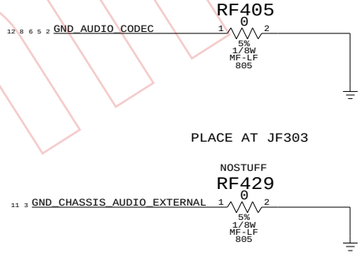


PLACE ACROSS GROUND SPLIT



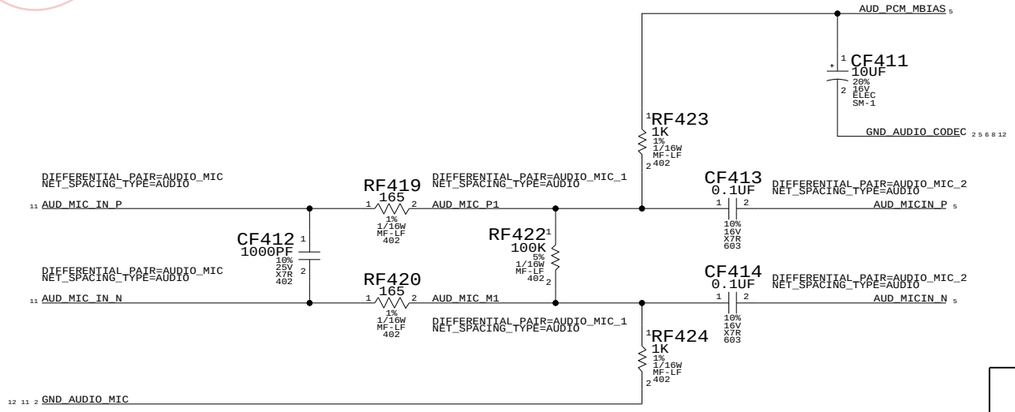
PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE

PLACE ACROSS GROUND SPLIT AT CODEC UE700

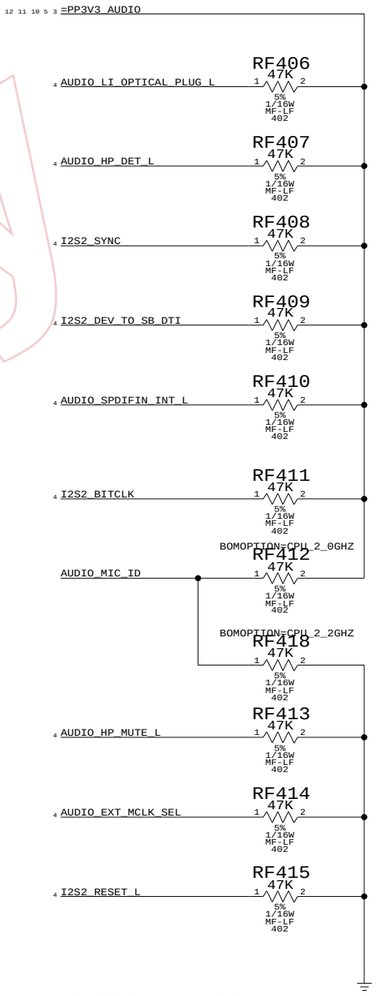


PLACE AT JF303

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE: NONE	SHT 154 OF 154	