1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SEEDY
02/17/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
11		365610	ENGINEERING RELEASED	02/17/05	?

CSA	PDF	CIRCUIT	BLOCK
1	1	TABLE OF CONTENTS	TOP
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16	15	FAN 0, 1 AND SYSTEM TEMP SENSOR	
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18	17	I2C CONNECTIONS	
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22	19	1.5V VREG / U3LITE CORE	
23	20	SHASTA CORE	
24	21	U3LITE MISC	
25	22	SHASTA SERIAL	
26	23	PULSAR POWER	
27	24	PULSAR CLOCKS	
28	25	U3LITE APPLE PI	PROCESSOR
29	26	NEO APPLE PI	
30	27	CPU STRAPS	
31	28	NEO POWER & BYPASS	
32	29	CPU BYPASS	
33	30	CPU VREG	
34	31	CPU VREG	
35	32	CPU VREG OUTPUT CAPS	
36	33	CPU DIODE CONDITIONER	
37	34	U3LITE MEMORY	MEMORY
38	35	SERIES TERMINATION	
40	36	DIMMS	
44	37	PARALLEL TERMINATION	
45	38	PARALLEL TERMINATION	
46	39	VTT VREG	
48	40	U3LITE AGP	GRAPHICS
49	41	GPU AGP	
50	42	GRAPHICS VREGS	

CSA	PDF	CIRCUIT	BLOCK
51	43	GPU CORE POWER	GRAPHICS
52	44	GPU FRAME BUFFER	
53	45	FRAME BUFFER TERMINATION	
54	46	GRAPHICS DDR SDRAM A	
55	47	GRAPHICS DDR SDRAM B	
56	48	GPU STRAPS	
58	49	GPU DVI & DACS	
59	50	EXT VGA & TMDS	
60	51	U3LITE HYPERTRANSPORT	HT
62	52	SHASTA HYPERTRANSPORT	
64	53	HYPERTRANSPORT LA CONNECTORS	
73	54	PCI SERIES TERMINATION	PCI
74	55	SHASTA PCI	
75	56	BOOT ROM	
76	57	AIRPORT EXTREME & BLUETOOTH	
77	58	USB2 PCI	
80	59	SHASTA DISK	DISK
83	60	DISK CONNECTORS	
84	61	SHASTA ETHERNET	ETHERNET
86	62	VESTA ETHERNET PHY	
87	63	ETHERNET CONNECTOR	
88	64	SHASTA FIREWIRE	FIREWIRE
89	65	VESTA FIREWIRE PHY	
90	66	FIREWIRE CONNECTORS	
91	67	USB HOST INTERFACE	USB
92	68	USB DEVICE INTERFACE	
94	69	MODEM CONNECTOR	MODEM
95*	70	PCM3052A AUDIO CODEC	AUDIO
96*	71	LINE IN AMP	
98*	72	LINE OUT AMP	
100*	73	SPEAKER AMP	
101*	74	AUDIO CONNECTORS	
102*	75	AUDIO POWER SUPPLIES	

* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE: SCH,MLB,SEEDY

DRAWING NUMBER 051-6772 REV. 11

SHT 1 OF 102

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE

U2900
CPU
NEO 10S
PAGE 29

32-BIT
APPLE PI
ELASTIC INTERFACE
1.2V/900MHZ

U1300
SMU
PAGE 13

U1301
RTC
PAGE 13

J5900, J5901
J5902, J5903
17",20" INVERTER
TMDS
EXT VGA
PAGE 59

U5400, U5401
FRAME
BUFFER A
PAGE 54

64-BIT
FRAME BUFFER
2.6V/400MHZ

U4900
GPU
RV351LE
PAGE 49

32-BIT
8X AGP
0.8V/533MHZ
4X = 1.5V
I/O = 1.5V

APPLE PI
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AGP
PAGE 48

U3
U3LITE
CORE
PAGE 22

MAIN MEMORY
PAGE 37

64/128-BIT
MAIN MEMORY
2.6V/400MHZ

SERIES
TERM
PAGE 38

J4000
J4001
DIMMS
PAGE 40

PARALLEL
TERM
PAGES 44&45

64-BIT
FRAME BUFFER
2.6V/400MHZ

U5500, U5501
FRAME
BUFFER B
PAGE 55

MISC
PAGE 24

HYPERTRANSPORT
PAGE 60

8-BIT
HYPERTRANSPORT
1.2V/800MHZ
CONTROL = 2.5V

J9210/J9220/J9230
USB
CONNECTORS
PAGE 92

U2600
PULSAR
POWER
PAGE 26
CLOCKS
PAGE 27

I2C
PAGE 18

J6400
J6401
J6402
HT
DEBUG
PAGE 64

J9240
BLUETOOTH
CONNECTOR
PAGE 92

1 2 3 4 5
USB
PAGE 91

U7700
USB 2.0
uPD720101
PCI
PAGE 77

U7500
BOOTROM
PAGE 75

J7600
AIRPORT
EXTREME
CONNECTOR
PAGE 76

HARD DRIVE

JXXXX
SATA
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA1
PAGE 80

HYPERTRANSPORT
PAGE 62

U2300

PCI
PAGE 74

32-bit PCI (5V-3.3V/33MHz)

FOR DEVELOPMENT ONLY

J8302
SATA DEV
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA2
PAGE 80

SHASTA

GPIO/PCI64
PAGE 25

OPTICAL

J8301
UATA
CONNECTOR
PAGE 83

UATA/133
3.3V/133MHZ

UATA
PAGE 80

CORE
PAGE 23

NCS
PAGE 91

J9401
CTL-LESS /
SOFT MODEM
CONNECTOR
PAGE 94

ETHERNET
PAGE 84

FIREWIRE
PAGE 88

I2S
PAGE 25
SCCA
I2S1
SCCB
I2S2
I2S0

GMII (3.3V/125MHz)
8-BIT TX
8-BIT RX

1394 PHY (3.3V/98MHz)

U9500
AUDIO CODEC
PCM3052A
PAGE 95

S/PDIF

OPTICAL OUT
J9803
COMBO OUT
CONNECTOR
PAGE 98
LINE OUT

LINE OUT
AMP
PAGE 97

SPEAKER
AMP
PAGE 97

J9801
SPEAKER
CONNECTOR
PAGE 98

LINE IN
AMP
PAGE 97

U8600
VESTA
GIG ETHERNET
PAGE 86
FIREWIRE A
PAGE 89
0 1

4 Diff pairs
2 Diff pairs

J8700
ETHERNET
CONNECTOR
PAGE 87

J9000, J9001
FIREWIRE A
CONNECTORS
PAGE 90

J9800
LINE IN
CONNECTOR
PAGE 98

J9802
MIC
CONNECTOR
PAGE 98

SYSTEM BLOCK DIAGRAM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 11

SCALE NONE | SHT 2 OF 102

POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP24V_RUN — FW CONN, 20" LCD INVERTER

PP12V_RUN — 20" PANEL POWER, 20" LCD INVERTER

PP5V_RUN — HDD & OPTICAL

PP5V_ALL

PP3V3_RUN — PCI BUS, AUDIO CODEC

SMU

SYS_POWERUP_L
POWER SEQUENCE PIN

PULSAR_POWER_DOWN
MAKE_BASE=TRUE
=PULSAR_POWER_DOWN 27

TP_SMU_PWRSEQ_P1_0
MAKE_BASE=TRUE

TURN_ON_PP1V2_PWRON_L 10

SMU_PWRSEQ_P1_4 13
SMU_PWRSEQ_P1_0 13
SMU_PWRSEQ_P1_1 13
SMU_PWRSEQ_P9_5 13 (PWR_GOOD_SB_CORE)
SMU_PWRSEQ_P9_6 13 (PWR_GOOD_PP2V5)
SMU_PWRSEQ_P1_2 13 (TURN_ON_VTT)

5V

PP5V_RUN_AUDIO LINEAR
PAGE 99
5V — HP/LINEOUT AMP

PP4V5_RUN_AUDIO LINEAR
PAGE 99
4.5V — AUDIO CODEC

CPU CORE SWITCHER
PAGE 33 SC1211 4
SC2643VX*1
0.8~1.2V — GPUL

=PP5V_RUN_CPU 6 7 8 31
ALIAS CPU_AVDD_EN 31

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 31
2.8V — CPU AVDD

PP5V_PWRON FET SWITCH
PAGE 11
5V — USB CONN

PP3V3_ALL LINEAR
PAGE 11
3.3V — FW PHY, SMU

PP3V3_PWRON FET SWITCH
PAGE 11
3.3V — ENET PHY, USB2 HOST, MODEM & BT

GPU CORE SWITCHER
PAGE 50 IRU3037ACS
1.20V — RV351

PP2V5_GPU_A2VDD LINEAR
PAGE 50
GPU

PP1V8_TPVDD LINEAR
PAGE 50 GPU

PP1V5_VDDC_CT LINEAR
PAGE 50 GPU

U3LITE CORE SWITCHER
PAGE 22 IRU3037CS
1.53V — U3LITE CORE

PP2V5_PWRON SWITCHER
PAGE 9 IRU3037CS
2.59V — SHASTA HT, DDR DIMM

PP1V2_ALL SWITCHER
PAGE 10 IRU3037ACS
1.2V — VESTA CORE

PP1V2_PWRON FET SWITCH
PAGE 10
SHASTA CORE
PWRON_SD
PWRON_DISK_SB
23 7 6 =PPVCORE_PWRON_SB

PP1V2_RUN FET SWITCH
PAGE 10
HT BUS

PP2V5_PWRON

PP2V5_RUN FET SWITCH
PAGE 9
RAM TERM, GRAPHIC FB

PP1V8_GPU LINEAR
PAGE 50
GPU

PP1V25_RAM_VTT LINEAR
PAGE 46
1.3V — RAM VTT

PP1V5_PWRON LINEAR
PAGE 50
1.5V — PULSAR CORE

PP1V5_RUN POWER SW
PAGE 50
AGP BUS

46 TURN_ON_VTT

PP3V3_ALL
R331 10K 5% 1/10W MF-LF 402
PWR_GOOD_SB_CORE

11 RAIL_CTL_NEG
R330 100K 5% 1/10W MF-LF 402
COMPARE_SB_CORE
C330 0.01UF 20% 16V CERM 402
U1100 LM339A SOI

PP5V_ALL
R342 150K 5% 1/10W MF-LF 402
PS_2V_REF
R340 100K 5% 1/10W MF-LF 402
COMPARE_PP2V5
C340 0.01UF 20% 16V CERM 402
R343 100K 5% 1/16W MF-LF 402
U1100 LM339A SOI

PP3V3_ALL
R341 10K 5% 1/10W MF-LF 402
PWR_GOOD_PP2V5

POWER BLOCK DIAGRAM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 3 OF 102	

DATE DESCRIPTION

10/20/04
CLONED DESIGN FROM GILA (Q45 A/B) REV G
CHECKIN 00002

10/21/04
ADDED VESTA
ADDED 1.2V REGULATOR FOR VESTA CORE
ADDED 2.5V LDO FOR VESTA
ADDED FW LATE VG PROTECTION
REMOVED BCM5231 ETHERNET PHY
REMOVED FW802A FW PHY
REMOVED FW PORT POWER CIRCUITRY
REMOVED MICRODASH CONNECTOR
CHECKIN 00003

10/22/04
REMOVED NV18/34 GPU
REMOVED AGP VREG (VR5001)
REMOVED GPU VTT VREG
ADDED 2.5V VREG FOR A2VDD
REMOVED EXTERNAL TMDS TRANSMITTER
ADDED RV351LE GPU
CHECKIN 00004

10/26/04
GPU CORE POWER UPDATES
ADDED VESTA ETHERNET LOWPWR CIRCUIT
ADDED DEVELOPMENT LEDS FOR VESTA ENET
CHECKIN 00005

10/28/04
CONNECTED FRAME BUFFER
ADDED 1.8V GPU VREG
CONNECTED GPU TMDS AND VGA
CONNECTED GPU POWER AND POWER FILTERS
CHECKIN 00006

11/01/04
ADDED VOLTAGE, LINE WIDTH, AND NECK WIDTH PROPERTIES FOR GRAPHICS (IN MM)
TIED PPVCORE_NB DIRECTLY TO PP1V5_PWRON (REMOVED R707)
REPLACED EMC FERRITES WITH 0 OHM RESISTORS FOR GRAPHICS AND FANS
REMOVED VESTA CORE REGULATOR
REPURPOSED 1.2V REGULATOR FOR VESTA AND SHASTA
CHANGED FW LATE VG CIRCUITRY TO MATCH Q78 & Q86
CHECKIN 00007

11/03/04
<RADAR 3848831> MOVED SMU RESET BUTTON TO DEVELOPMENT BOM
<RADAR 3849762> MOVED SMU DOWNLOAD CONNECTOR TO DEVELOPMENT BOM
<RADAR 3849798> REDUCED CAPACITANCE OF C1100 & C1102
MASTER PAGE SYNC:
  FRAME BUFFER SWAPS FOR CLEANER ROUTING
  REMOVED VESTA ROM
  AUDIO COST REDUCTIONS <RADAR 3849747 & 3849751>
  AUDIO 3052A CODEC
ADDED 1.55V VREG FOR GPU VDDC_CT
MOVED VTT VREG TO 2.5V PWRON TO REDUCE CURRENT THROUGH Q903
CHANGED FETS IN GPU CORE FOR COST REDUCTION
ADDED SPACING & PHYSICAL CONSTRAINTS TO FRAME BUFFER
CHECKIN 00008

11/04/04
REMOVED 1.6GHZ PROCESSORS
CHANGED VOLTAGE SETTING OF 2.5V VREG TO 2.588V FROM 2.62V
1.2V VREG COST REDUCTIONS - Q1002 TO NTD60N02R; C1002/3 TO 10UF CERM
U2850 - REMOVED MAXIM AS AN ALTERNATE
MOVED GPU ZENER DIODES TO VREG PAGE SINCE THEY SHOULD BE PLACED NEAR THE VREGS
ADDED 8MX32 GRAPHICS MEMORY
ADDED GIGABIT ETHERNET CONNECTOR
CHECKIN 00009

11/06/04
ADDED GPU STRAPS
CONNECTED GPU GPIOS
REMOVED ON BOARD POWER SUPPLY TEMP SENSOR
ADDED AMBIENT LIGHT SENSOR CONNECTOR
CONNECTED GPU TEMP SENSOR
REMOVED CPU VREG 4TH PHASE
ADDED DEVELOPMENT LEDS TO REGULATORS
CHECKIN 00010

11/07/04
ADDED MORE GPU CONSTRAINTS
<RADAR 3616348, 3621390> CHANGED FLS900-2 TO 220 OHM
<RADAR 3848846> 2.5V RUN FET COST REDUCTION
<RADAR 3848859> 1.2V, 1.5V RUN FET COST REDUCTIONS
<RADAR 3848887> 5V & 3.3V PWRON FET COST REDUCTIONS
<RADAR 3849622> STUFFED AROUND TMDS FILTERS
<RADAR 3849656> STUFFED AROUND RGB FILTERS
<RADAR 3849806> CHEAPER SMU CRYSTAL
<RADAR 3849857> CHEAPER USB2 CRYSTAL
BOM RELEASE REV 01

11/08/04
FRAME BUFFER PIN SWAPS
<RADAR 3848846> UPDATE OF 2.5V RUN FET COST REDUCTION
<RADAR 3849743> ADDED RESISTORS TO STUFF AROUND USB FILTERS
CHECKIN 01001

11/09/04
<RADAR 3848850> REGULATOR COST REDUCTIONS
<RADAR 3849767> 2.5V VREG COST REDUCTIONS
<RADAR 3849772> REMOVED OUTPUT CAP ON 1.2V_ALL VREG
<RADAR 3849820> SHASTA FILTER COST REDUCTION
<RADAR 3849854> GPU CORE VREG COST REDUCTION
<RADAR 3865344> SET GPU VDDC_CT VREG TO 1.55V
CHECKIN 01002

11/10/04
CHANGED SOURCE OF Q1003 TO PP1V2_ALL
RGB TERMINATION NOW CONNECTED TO DIGITAL GROUND
WHITE LED - CHANGED INDUCTORS TO 0 OHM RESISTORS
UPDATED POWER BLOCK DIAGRAM
CHECKIN 01003
<RADAR 3848850> 2.5V VREG COST REDUCTION
CHECKIN 01004

11/15/04
ADDED REGULATOR FOR GPU TPVDD
ADDED POWER SEQUENCING FOR GRAPHICS REGULATORS
ADDED TEST POINTS TO GRAPHICS FOR EXOR TESTING
REMOVED EXTERNAL S/PDIF TRANSMITTER
CHECKIN 01005

11/16/04
REMOVED P50 AIRPORT AND Q23 BLUETOOTH CONNECTORS, HOLES, & STANDOFFS
ADDED Q85 AIRPORT & BLUETOOTH CONNECTOR
CHECKIN 01006
(PP 16,17) REPLACED FAN CONTROL WITH NEW CIRCUIT
(P 76) FINISHED CONNECTING Q85 CONNECTOR
(P 7) ADDED PLATED HOLE ZH710 FOR TMDS GROUNDING
(P 7) TIED BOTH EI RAILS TO 1.5V
(P 5) NEW BOOTROM P/N
(P 9) ADDED EXTRA 10UF INPUT CAP
(P 12) VESTA_ENET_LOWPWR UPDATE
(P 18) <RADAR 3878118> MOVED SMU I2C E BUS
(P 22) CHANGED Q2250 TO 376S0143
(P 46) SLEEP SIGNAL TURNS OFF VTT VREG
(P 58) REPLACED THERMAL SENSOR WITH LM63
(P 59) TIED UNUSED BUFFER ENABLE PINS HIGH
(P 90) FIXED FW PORT NAMING
(P 90) CHANGED R9090 TO 665 OHM
(P 91) CHANGED USB2 CHIP GROUNDING
(P 8) ALIASED VESTA JTAG TO TEST POINT NETS
(P 9) <RADAR 3848846> ADDED PAD FOR 1NF CAP TO GATE OF Q903
CHECKIN 01007 / BOM RELEASE REV 02

11/18/04
ADDED PHYSICAL CONSTRAINTS
AUDIO STUFFING CHANGES
CHECKIN 02001

11/20/04
(P 36) CONNECTED NEW CPU DIODE REFERENCE
(P 77) USB2 IDESEL - NOW FROM USB2 SIDE
(P 56) ADDED BOMOPTIONS FOR MEMORY STRAPS
(PP 56, 58) CONNECTED PWM FROM RV351LEP & PUT IN PROTO WORKAROUND
(P 25) <RADAR 3849835> NEW SHASTA XTAL
(P 62) <RADAR 3849855> SHASTA HT_PLL FILTER COST REDUCTION
(P 91) <RADAR 3849858> USB CAP COST REDUCTION
(P 76) ADDED STANDOFFS FOR Q85 CARD
(PP 16,17) NEW FAN CIRCUIT CAPS (C1603, C1653, C1703)
(P 50) <RADAR 3865344> VDDC_CT SET TO 1.50V
(P 50) <RADAR 3877855> TP_VDD SET TO 1.80V
(P 12) VESTA_ENET_LOWPWR UPDATE
(PP 10, 22, 34, 50) USED COMPARATOR FOR LOW VOLTAGE RAIL LEDS
CHECKIN 02002

11/22/04
(P 49) CONNECTED AGPTEST RESISTOR TO VDDP
(P 56) ADDED PADS FOR STRAPPING RESISTORS TO GPU_GPIO<14>
(P 58) ADDED CONSTRAINT SETS
(P 59) STUFFED AROUND Q5900 PANEL PWR SEQUENCING
(P 59) LED 3 NOW DRIVEN FROM FPD_PWR_ON
(P 3) CONNECTED SHASTA CORE POWER FOR POWER SEQUENCING
(P 76) FIXED PCI_CBE_L<1> CONNECTION
MORE PHYSICAL & SPACING UPDATES
(P 83) <RADAR 3890225> OPTICAL DRIVE CONNECTOR CHANGED TO 516S0235
CHECKIN 02003
(P 56) ADDED OPTION OF USING PWM FROM SHASTA
<RADAR 3849718, 3849767, 3849854> MADE ON & VISHAY FETS TRUE ALTERNATES
(P5) ADDED U3L W/ NEW LAMINATE AS ALTERNATE
(P 16) C1653 - REPLACED WITH LOWER HEIGHT CAP
CHECKIN 02004

11/23/04
(P 76) TABLED IN NEW STANDOFFS FOR Q85 CARD
PROTO RELEASE (REV 3)

12/02/04
(P 90) FIXED ALIAS PROBLEM WITH FW_TPB2_PD
(P 90) FIXED FW_CPS SHORT
(P 35) REMOVED DS3500 & DS3501
(P 83) REMOVED SECOND SATA CONNECTOR
CHECKIN 03001
CONVERTED DISCRETES TO LEAD FREE
CHECKIN 03002

12/07/04
CHANGED U7700 BACK TO LEADED PART
(P 5) REMOVED ORIGINAL U3LITE (NEW LAMINATE ONLY FOR C/D)
(P 49) CHANGED GPU TO RV351LEP (338S0231)
(P 76) NOW HAVE CORRECT SYMBOL FOR STANDOFFS
(P 76) J7650 - NEW TO ALLOW 5MM CONNECTED HEIGHT
BOM RELEASE REV 04

12/09/04
CHANGED ALIASES TO SYNONYMS
CHANGED LINE AND NECK WIDTHS TO METRTIC
CHECKIN 04001

12/13/04
ADDED 2.0 GHZ AND ADDITIONAL 1.8 GHZ ALTERNATE PROCESSORS TO PG. 5 TABLE
VESTA XTAL: R5815=249, R8609=332, R8921=332
VESTA ENET: R1262=10K, C1260=10U, R1251=NO STUFF, C1250=2.2U
FANS: NO STUFF DZ1601, DZ1651, DZ1701
  STUFFED R1604, R1654, R1704
CHECKIN 04002

12/14/04
2.5 V REGULATOR - NEW NARROWER OUTPUT CAPS (C908, C909)
(P 46) REMOVED SEMTECH REGULATOR, ADDED RICHTEK AS ALTERNATE VTT
(P 16) CHANGED FAN1 OUTPUT CAP BACK TO THROUGH-HOLE
(P 59) SWAPPED INVERTER CONNECTOR GENDER
CHECKIN 04003
(P 46) RICHTEK VTT UPDATES
BOM RELEASE REV 5

12/15/04
(P 6) ADDED NO_TESET PROPERTIES
(P 12) VESTA ENET LOW POWER FIX
CHECKIN 05001

12/16/04
FIXED I2C_TMDS_SDA/SCL ON P 6
(P 46) NOSTUFF RICHTEK VTT VREG
(P 59) STUFFED TMDS CHOKES
(P 56) USING PWM FROM ATI GPU
(P 38) FIXED MIN_NECK_WIDTH ON TD1 AND TD2
(P 92) ADDED NET_PHYSICAL_TYPE = USB2 TO TABLE
(P 7) ADDED BATTERY SAFETY BYPASS OPTION (NOSTUFF)
CHECKIN 05002
(P 50) ADDED Q5000 TO INPUT OF GPU VCORE VREG
(P 6) REMOVED SOME FUNC_TEST PROPERTIES
(P 50) GPU_VDCC_CT POWER SEQUENCING
CHECKIN 05003

12/17/04
(P 6) ADDED/REMOVED MORE FUNC_TEST PROPERTIES
CHECKIN 05004
(P 50) GPU POWER SEQUENCING
CHECKIN 05005

12/20/04
MINOR TEXT/COMMENT CHANGES
EVT RELEASE (REV 6)

01/11/05
(P 5) REMOVED BRA FROM ALTERNATE PROCESSOR TABLE, REPLACED BPA WITH BNA
(P 5) NEW SMU PART NUMBER

01/18/05
CHANGED SDF7601 TO PART 860-0567
BOM RELEASE REV 7

01/25/05
(P 5) CORRECTED 1.8GHZ CPU APPLE P/N FROM 337S2969 TO 337S2998 ON ALTERNATE PROCESSOR TABLE
(P 12) NOSTUFF Q1250 TO DISCONNECT ENETFW_RESET FROM SHASTA GPIO
(P 5) CORRECTED SMU PART NUMBER TO 341T1703
(P 16, 17) HAROLD'S FAN CIRCUIT CHANGES
CHECKIN 07002

01/27/05
(P 25) REPLACED R2566 WITH 0 OHM TO ELIMINATE FW_LOWPWR GLITCH
  ADDED 0 OHM (R2570, NOSTUFF) TO BREAK FW_LOWPWR FROM SHASTA
(P 56) STUFF R5610 TO PULL DOWN ATI_PWM SIGNAL TO ELIMINATE GLITCH
(P 27,28,29) CONNECTED CPU_APSYNC FROM U3LITE AND DISCONNECTED FROM PULSAR
  NO STUFF: R2768,R2772,R2805,R2910
  STUFF: R2806,R2911
(P 11) CHANGED C1102 TO 16V FOR SUPPLY AND COST ISSUES
(P 5) ADDED KQA (337S3093) TO ALTERNATE PROCESSOR TABLE
CHECKIN 07003
(P 5) MODIFIED PROCESSOR TABLE TO MATCH IBM'S TABLE, AGAIN.
BOM RELEASE REV 8

02/01/05
(P 75) BOOTROM REFLASHING ISSUE FIX: CHANGED R7502 TO 470 OHM
(P 12) ENET_LOWPWR GLITCH FIX:ADDED A CLAMP CIRCUIT FOR ENET_LOWPWR GLITCH
(P 10,22) SHASTA & U3LITE VCORE POWER IMPROVEMENT: STUFF C1005 AND C2205 WITH 2200PF CAPS
(P 13) CHANGED U1301 TO LEADED PART (353S0653) DUE TO SUPPLY
(P 5) ADDED 34S0284 AND 34S0282 AS U3LITE ALTERNATES (OLD LAM)
BOM RELEASE REV 9

02/03/05
(P 28) CHANGED APSYNC SERIES TERMINATION R2806 TO 10 OHM
(P 5) ADDED LEAD FREE PARTS AS ALTERNATE FOR U1301 & VRA201 DUE TO SUPPLY
(P 8) REMOVED SMU DOWNLOAD CONNECTOR FROM DEVELOPMENT BOM
(P 92) STUFFED USB COMMON MODE CHOKES FOR EMC
CHECKIN 09002

02/04/05
(P 50) <RADAR 3919121> NOSTUFF U5090 AND RELATED COMPONENTS, STUFFED R5092 FOR 1.5V GPU VDCC_CT

02/08/05
(P 7) REMOVED ZH701
(P 12) STUFF R1251, CHANGE C1250 TO 10UF, R1262=100K TO LENGTHEN VESTA RESET AND LOWPWR DELAY
(P 59) <RADAR 3849662> STUFFED PANEL POWER SEQUENCING FOR BOTH 17 AND 20 INCH
CHECKIN 09003
(P 92) <RADAR 3742725> CHANGED USB COMMON MODE CHOKES TO 120-OHM 155S0232
(P 59) NOSTUFF R5950, STUFF R5923 FOR 17 INCH PANEL POWER FROM PP3V3_RUN INSTEAD OF PP3V3_ALL

02/09/05
CHECKIN 09004

02/10/05
(P 59) <RADAR 3919083> CHANGED R5971 AND R5972 TO 33 OHMS
(P 56) <RADAR 3960901, 4000359> GPU GPIO GLITCH STUFFED: U5600, U5601, NOSTUFF: R5609, R5621
DVT RELEASE (REV 10)
(P 56) <RADAR 3960901, 4000359> GPU GPIO GLITCH STUFFED: C5600, C5601

02/15/05
(P 12) CHANGED C1250 TO 6.3V PART, TO MATCH A PART ALREADY ON THE BOM
(P 5) ADDED 353S0687 (LEADED) AS ALTERNATE FOR 353S0959 (LEAD FREE) U9800

02/16/05
ADDED PAGE TITLE PROPERTIES FOR SCHEMATIC REUSE WITH M23/M33

02/17/05
(P 12) YET ANOTHER VESTA RESET/LOWPWR STUFFING CHANGE
(P 16,17,36) ADDED SIGNAL ALIASES FOR SCHEMATIC REUSE WITH M23
(P 50) RE-STUFFED GPU 1.5V VDCC_CT BECAUSE OF LEAKAGE WORRIES
BOM RELEASE REV 11

11

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6771 | REV 11
SCALE NONE | SHT 4 OF 102

PROCESSORS

QUALIFIED

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3055	1	PROCESSOR	FCBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,KPA	2.0GHZ	1.20V	42W	?	U2900	CPU_2_0GHZ
337S3060	1	PROCESSOR	FCBGA-576-1MM	IC,GPUL,DD3.1,1.8G,85C,JPA	1.8GHZ	1.20V	42W	?	U2900	CPU_1_8GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3061	337S3060	CPU_1_8GHZ	U2900	IC,DD3.1,1.8G,JRA	1.25V
337S2969	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BPA	1.20V
337S2970	337S3060	CPU_1_8GHZ	U2900	IC,DD3.0,1.8G,BRA	1.25V
337S3093	337S3055	CPU_2_0GHZ	U2900	IC,DD3.1,2.0G,KQA	1.15V
337S3056	337S3055	CPU_2_0GHZ	U2900	IC,DD3.1,2.0G,KRA	1.25V
337S3058	337S3055	CPU_2_0GHZ	U2900	IC,DD3.0,2.0G,CPA	1.20V
337S3059	337S3055	CPU_2_0GHZ	U2900	IC,DD3.0,2.0G,CRA	1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0320	1	IC,U3LITE,NEW LAM,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0321	343S0320		U3	U3L,NEW LAM,200MM
343S0284	343S0320		U3	U3L,OLD LAM,300MM
343S0282	343S0320		U3	U3L,OLD LAM,200MM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0324	1	IC,ASIC,VESTA,V1.3	U8600	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
820-1747	1	PCB,FAB,MLB	MLB1	
825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
051-6772	1	PCB,SCHEM,MLB	SCH1	
341T1667	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
341T1703	1	IC,SMU,Q45C/D	U1300	
CRITICAL 603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL 603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702,LED5900	RINGBRIGHT LED
376S0204	376S0130		Q3310,Q3320,Q3410	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q3311,Q3321,Q3411	MOSFET,N-CH,VISHAY
353S0733	353S0960		VRA201	MAX8510,L-F PART
353S0653	353S0958		U1301	DS1338, L-F PART
353S0959	353S0687		U9800	MAX9722 LEAD

TABLE ITEMS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 11

SCALE NONE | SHT 5 OF 102

1838	NO_TEST=YES	TP_FBBCS1_L	52
1824	NO_TEST=YES	AGP_CLK66M_GPU_R	27
1825	NO_TEST=YES	AGP_CLK66M_NB_R	6 27
1826	NO_TEST=YES	AUD_4V5_FB	102
1828	NO_TEST=YES	CPU_HTBEN_R	27
1829	NO_TEST=YES	EI_CPU_SYNC_R	27
1831	NO_TEST=YES	AGP_CLK66M_NB_R	6 27
1832	NO_TEST=YES	EI_NB_SYNC_R	27
1833	NO_TEST=YES	ERROR_LED	8
1834	NO_TEST=YES	HT_CLK66M_NB_R	27
1835	NO_TEST=YES	HT_CLK66M_SB_R	27
1836	NO_TEST=YES	HT_VREF_DEBUG	64
1837	NO_TEST=YES	ITS_RUNNING	7
1838	NO_TEST=YES	LED801_1	8
1839	NO_TEST=YES	LED802_1	8
1840	NO_TEST=YES	PCI_CLK66M_SB_INT_R	27
1841	NO_TEST=YES	PCI_CLK_P3_R	27
1842	NO_TEST=YES	PCI_CLK_P4_R	27
1843	NO_TEST=YES	PN1	33
1844	NO_TEST=YES	PN2	33
1845	NO_TEST=YES	PN3	34
1846	NO_TEST=YES	Q800_D	8
1847	NO_TEST=YES	Q800_G	8
1848	NO_TEST=YES	Q801_B	8
1849	NO_TEST=YES	Q802_B	8
1850	NO_TEST=YES	Q802_E	8
1851	NO_TEST=YES	Q803_B	8
1852	NO_TEST=YES	Q901_GATE	9
1853	NO_TEST=YES	Q902_DRAIN	9
1854	NO_TEST=YES	Q1002_DRAIN	10
1855	NO_TEST=YES	TP_AGP_MB_AGP8X_DET_L	48
1834	NO_TEST=YES	TP_ATTENTION	29
1834	NO_TEST=YES	TP_AFN	29
1834	NO_TEST=YES	TP_PSRO1	29
1834	NO_TEST=YES	TP_PSRO2	29
1834	NO_TEST=YES	TP_PSYNCOUT	29
1834	NO_TEST=YES	TP_USB2_PWREN<2>	92
1834	NO_TEST=YES	TP_USB2_PWREN<3>	92
1834	NO_TEST=YES	TP_USB2_PWREN<4>	92
1834	NO_TEST=YES	TP_NEC_AMC	77
1834	NO_TEST=YES	TP_NEC_NANDTEST	77
1834	NO_TEST=YES	TP_NEC_NTEST1	77
1834	NO_TEST=YES	TP_NEC_SMC	77
1834	NO_TEST=YES	TP_NEC_SMI_L	77
1834	NO_TEST=YES	TP_NEC_SRCLK	77
1834	NO_TEST=YES	TP_NEC_SRDATA	77
1834	NO_TEST=YES	TP_NEC_SRMOD	77
1834	NO_TEST=YES	TP_NEC_TEB	77
1834	NO_TEST=YES	TP_NEC_TEST	77
1834	NO_TEST=YES	TP_PLS_CLK_66M_0	27
1834	NO_TEST=YES	TP_PLS_CLK_66M_1	27
1834	NO_TEST=YES	TP_PLS_REF_CML	27
1834	NO_TEST=YES	TP_PLS_TEST1	27
1834	NO_TEST=YES	TP_PLS_TEST2	27
1834	NO_TEST=YES	TP_PLS_TEST3	27
1834	NO_TEST=YES	TP_SB_FSTEST	25
1834	NO_TEST=YES	TP_SB_PLLTEST	25
1834	NO_TEST=YES	TP_VREF_CG	48
1834	NO_TEST=YES	TP_SB_NC_P7	91
1834	NO_TEST=YES	TP_SB_NC_P8	91
1834	NO_TEST=YES	TP_SB_NC_R3	91
1834	NO_TEST=YES	TP_SB_NC_R4	91
1834	NO_TEST=YES	TP_SB_NC_R5	91
1834	NO_TEST=YES	TP_SB_NC_R6	91
1834	NO_TEST=YES	TP_SB_NC_R7	91
1834	NO_TEST=YES	TP_SB_NC_R8	91
1834	NO_TEST=YES	TP_SB_NC_T1	91
1834	NO_TEST=YES	TP_SB_NC_T2	91
1834	NO_TEST=YES	TP_SB_NC_T3	91
1834	NO_TEST=YES	TP_SB_NC_T4	91
1834	NO_TEST=YES	TP_SB_NC_T5	91
1834	NO_TEST=YES	TP_SB_NC_T6	91
1834	NO_TEST=YES	TP_SB_NC_T7	91
1834	NO_TEST=YES	TP_SB_NC_T8	91
1834	NO_TEST=YES	TP_SB_NC_U1	91
1834	NO_TEST=YES	TP_SB_NC_U2	91
1834	NO_TEST=YES	TP_SB_NC_U3	91
1834	NO_TEST=YES	TP_SB_NC_U4	91
1834	NO_TEST=YES	TP_SB_NC_U5	91
1834	NO_TEST=YES	TP_SB_NC_U6	91
1834	NO_TEST=YES	TP_SB_NC_V1	91
1834	NO_TEST=YES	TP_SB_NC_V2	91
1834	NO_TEST=YES	TP_SB_NC_V3	91
1834	NO_TEST=YES	TP_SB_NC_V4	91
1834	NO_TEST=YES	TP_SB_NC_W1	91
1834	NO_TEST=YES	TP_SB_NC_W3	91
1834	NO_TEST=YES	TP_SB_NC_Y1	91
1834	NO_TEST=YES	TP_SB_NC_Y3	91
1449	NO_TEST=YES	TP_SATA_CLK25M	27
1442	NO_TEST=YES	TP_USB2_PWREN<0>	92
1442	NO_TEST=YES	TP_USB2_PWREN<1>	92
1442	NO_TEST=YES	TP_DUMMY_A	24
1442	NO_TEST=YES	TP_DUMMY_B	24
1442	NO_TEST=YES	TP_RAM_CKE_R<2>	8
1855	NO_TEST=YES	Q2201_GATE	22
1856	NO_TEST=YES	Q2202_DRAIN	22
1856	NO_TEST=YES	R904_P2	9
1857	NO_TEST=YES	R2204_P2	22
1858	NO_TEST=YES	RAM_CLK66M_NB_R	27

1434	NO_TEST=YES	TP_RAM_CKE_R<3>	8
1435	NO_TEST=YES	TP_RAM_CKE_R<6>	8
1436	NO_TEST=YES	TP_RAM_CKE_R<7>	8
1437	NO_TEST=YES	TP_RAM_CS_L_R<10>	8
1438	NO_TEST=YES	TP_RAM_CS_L_R<11>	8
1439	NO_TEST=YES	TP_RAM_CS_L_R<2>	8
1440	NO_TEST=YES	TP_RAM_CS_L_R<3>	8
1441	NO_TEST=YES	TP_RAM_MUXEN0	8
1442	NO_TEST=YES	TP_RAM_MUXEN4	8
1443	NO_TEST=YES	TP_NB_PM_SLEEP0	24
1444	NO_TEST=YES	TP_J4000_SJRESET_L	40
1445	NO_TEST=YES	TP_J4001_SJRESET_L	40
1446	NO_TEST=YES	U2100_UNUSED	21
1847	NO_TEST=YES	PLS_CLK_66M_0_R	27
1848	NO_TEST=YES	PLS_CLK_66M_1_R	27
1849	NO_TEST=YES	SATA_CLK25M_R	27

1866	NO_TEST=YES	SB_CLK25M_ATA_R	27
1867	NO_TEST=YES	TEK_HT_A7	64
1868	NO_TEST=YES	TEK_HT_A9	64
1869	NO_TEST=YES	TEK_HT_A10	64
1870	NO_TEST=YES	TEK_HT_A12	64
1871	NO_TEST=YES	TEK_HT_B10	64
1872	NO_TEST=YES	TEK_HT_B12	64
1873	NO_TEST=YES	TP_PCI_CLK_P4	8
1874	NO_TEST=YES	U900_COMP	9
1875	NO_TEST=YES	U900_GATE_H	9
1876	NO_TEST=YES	U900_GATE_L	9
1877	NO_TEST=YES	U900_SS	9
1878	NO_TEST=YES	U900_VC	9
1880	NO_TEST=YES	U900_VC_D	9
1881	NO_TEST=YES	U900_VC_R	9
1882	NO_TEST=YES	U1000_FEEDBACK	10
1884	NO_TEST=YES	UATA_DASP_L_DS	83

1885	NO_TEST=YES	RFBD<1>	53 54
1886	NO_TEST=YES	RFBD<2>	53 54
1887	NO_TEST=YES	RFBD<3>	53 54
1888	NO_TEST=YES	RFBD<4>	53 54
1889	NO_TEST=YES	RFBD<6>	53 54
1890	NO_TEST=YES	RFBD<7>	53 54
1891	NO_TEST=YES	RFBD<8>	53 54
1892	NO_TEST=YES	RFBD<9>	53 54
1893	NO_TEST=YES	RFBD<11>	53 54
1894	NO_TEST=YES	RFBD<12>	53 54
1895	NO_TEST=YES	RFBD<13>	53 54
1896	NO_TEST=YES	RFBD<14>	53 54
1897	NO_TEST=YES	RFBD<16>	53 54
1898	NO_TEST=YES	RFBD<18>	53 54
1899	NO_TEST=YES	RFBD<19>	53 54
1900	NO_TEST=YES	RFBD<21>	53 54
1901	NO_TEST=YES	RFBD<22>	53 54
1902	NO_TEST=YES	RFBD<23>	53 54
1903	NO_TEST=YES	RFBD<24>	53 54
1904	NO_TEST=YES	RFBD<25>	53 54
1905	NO_TEST=YES	RFBD<26>	53 54
1906	NO_TEST=YES	RFBD<28>	53 54
1907	NO_TEST=YES	RFBD<29>	53 54
1908	NO_TEST=YES	RFBD<30>	53 54
1909	NO_TEST=YES	RFBD<32>	53 54
1910	NO_TEST=YES	RFBD<33>	53 54
1911	NO_TEST=YES	RFBD<35>	53 54
1912	NO_TEST=YES	RFBD<36>	53 54
1913	NO_TEST=YES	RFBD<37>	53 54
1914	NO_TEST=YES	RFBD<38>	53 54
1915	NO_TEST=YES	RFBD<40>	53 54
1916	NO_TEST=YES	RFBD<42>	53 54
1917	NO_TEST=YES	RFBD<43>	53 54
1918	NO_TEST=YES	RFBD<45>	53 54
1919	NO_TEST=YES	RFBD<46>	53 54
1920	NO_TEST=YES	RFBD<47>	53 54
1921	NO_TEST=YES	RFBD<48>	53 54
1922	NO_TEST=YES	RFBD<49>	53 54

1923	NO_TEST=YES	U2200_COMP	22
1924	NO_TEST=YES	U2200_GATE_H	22
1925	NO_TEST=YES	U2200_GATE_L	22
1926	NO_TEST=YES	U2200_SS	22
1927	NO_TEST=YES	U2200_VC	22
1928	NO_TEST=YES	U2200_VC_D	22
1929	NO_TEST=YES	U2200_VC_R	22
1930	NO_TEST=YES	Q5001_GATE	50
1931	NO_TEST=YES	Q5002_DRAIN	50
1934	NO_TEST=YES	U3310_DRN	33
1935	NO_TEST=YES	U3320_DRN	33
1936	NO_TEST=YES	U3410_DRN	34
1937	NO_TEST=YES	U5000_COMP	50
1938	NO_TEST=YES	U5000_FEEDBACK	50
1939	NO_TEST=YES	U5000_GATE_H	50
1940	NO_TEST=YES	U5000_GATE_L	50
1941	NO_TEST=YES	U5000_SS	50
1942	NO_TEST=YES	U5000_VC	50

GENZ SHOULD USE J1400 FOR THE FOLLOWING NETS:

1743	NO_TEST=TRUE	EI_CPU_TO_NB_AD<0..43>	14 28 29
1744	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	14 28 29
1745	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	14 28 29
1746	NO_TEST=TRUE	EI_CPU_TO_NB_SR_N<0..1>	14 28 29
1747	NO_TEST=TRUE	EI_CPU_TO_NB_SR_P<0..1>	14 28 29
1748	NO_TEST=TRUE	EI_NB_TO_CPU_AD<0..43>	14 28 29
1749	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	14 28 29
1750	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	14 28 29
1751	NO_TEST=TRUE	EI_NB_TO_CPU_SR_N<0..1>	14 28 29
1752	NO_TEST=TRUE	EI_NB_TO_CPU_SR_P<0..1>	14 28 29
1753	NO_TEST=YES	CHKSTOP_L	8 14 29
1754	NO_TEST=YES	CPU_HRESET_L	14 29 30
1755	NO_TEST=YES	CPU_INT_L	14 25 29 30
1756	NO_TEST=YES	CPU1_HTBEN	14
1757	NO_TEST=YES	EI_CPU1_CLK_N	14 27
1758	NO_TEST=YES	EI_CPU1_CLK_P	14 27
1759	NO_TEST=YES	EI_QACK_L	14 28 29
1760	NO_TEST=YES	EI_QREQ_L	14 28 29 30
1761	NO_TEST=YES	EI_SE	14 28 29 30
1762	NO_TEST=YES	I2C_SMU_A_SCL_OUT_L	13 14 18
1763	NO_TEST=YES	I2C_SMU_A_SDA_OUT_L	13 14 18
1764	NO_TEST=YES	MCP_L	14 29
1765	NO_TEST=YES	RI_L	14 29 30
1766	NO_TEST=YES	SYNCENABLE	14 29 30
1767	NO_TEST=YES	TP_PROC_TRIGGER_OUT	14 29
1768	NO_TEST=YES	EI_CPU1_SYNC	14 27
1827	NO_TEST=YES	CPU1_HTBEN_R	14 27
1833	NO_TEST=YES	EI_CPU1_SYNC_R	14 27

101	IN	AUD_MIC_IN_N_CONN		FUNC_TEST=TRUE
101	IN	AUD_MIC_IN_P_CONN		FUNC_TEST=TRUE
90	IN	FW_VP		FUNC_TEST=TRUE
101	IN	GND_AUDIO_MIC_CONN		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SCL		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SDA		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SCL		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SDA		FUNC_TEST=TRUE
36 33 31	IN	KPGND2		FUNC_TEST=TRUE
36 33 31	IN	KPVDD2		FUNC_TEST=TRUE
59 6	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SDA		FUNC_TEST=YES
77 76 75 74 73	IN	PCI_AD<31..0>		FUNC_TEST=TRUE
77 76 74 73	IN	PCI_CBE_L<3..0>		FUNC_TEST=TRUE
8	IN	PCI_CLK33M_AIRPORT		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_REQ_L		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_GNT_L		FUNC_TEST=YES
76 25	IN	PCI_SLOTA_INT_L		FUNC_TEST=YES
74 56 8	IN	PCI_RESET_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_FRAME_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_TRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_IRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_STOP_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_DEVSEL_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_PAR		FUNC_TEST=YES
76	IN	PCI_SLOTA_IDSEL		FUNC_TEST=YES
76 75 74	IN	ROM_CS_L		FUNC_TEST=YES
76 75 74	IN	ROM_OE_L		FUNC_TEST=YES
76 75 74	IN	ROM_WE_L		FUNC_TEST=YES
76 75	IN	ROM_ONBOARD_CS_L		FUNC_TEST=YES
76	IN	AIRPORT_CLKRUN_L_PD		FUNC_TEST=YES
76	IN	USB_BT_N		FUNC_TEST=YES
76	IN	USB_BT_P		FUNC_TEST=YES
92	IN	USB2_PORT1_N_F		FUNC_TEST=YES
92	IN	USB2_PORT1_P_F		FUNC_TEST=YES
92	IN	USB2_PORT2_N_F		FUNC_TEST=YES
92	IN	USB2_PORT2_P_F		FUNC_TEST=YES
92	IN	USB2_PORT3_N_F		FUNC_TEST=YES
92	IN	USB2_PORT3_P_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT1_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT2_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT3_F		FUNC_TEST=YES
94 25	IN	I2S1_DEV_TO_SB_DTI	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SYNC	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_BITCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_MCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SB_TO_DEV_DTO	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_RESET_L	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	MODEM_RING2SYS_L	2 TEST POINTS	FUNC_TEST=YES
59 58	IN	TMDS_CKM		FUNC_TEST=YES
59 58	IN	TMDS_D1M		FUNC_TEST=YES
59	IN	PPVCC_TMDS		FUNC_TEST=YES
59	IN	PP3V3_DDC		FUNC_TEST=YES
59	IN	TD0M		FUNC_TEST=YES
59	IN	TD0P		FUNC_TEST=YES
59	IN	TD1P		FUNC_TEST=YES
59	IN	TD2M		FUNC_TEST=YES
59	IN	TD2P		FUNC_TEST=YES
59	IN	TCKP		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SDA		FUNC_TEST=YES
59 6	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 7	IN	GND_CHASSIS_TMDS		FUNC_TEST=YES
59	IN	FILT_ANALOG_RED		FUNC_TEST=YES
59	IN	FILT_ANALOG_GRN		FUNC_TEST=YES
59	IN	FILT_ANALOG_BLU		FUNC_TEST=YES
59	IN	VGA_HSYNC_R		FUNC_TEST=YES
59	IN	VGA_VSYNC_R		FUNC_TEST=YES
59 58	IN	MON_DETECT		FUNC_TEST=YES
59	IN	PP24V_INV		FUNC_TEST=YES
59	IN	GND_20_INV		FUNC_TEST=YES
59	IN	INV_20_LCD_PWM		FUNC_TEST=YES
59	IN	INV_20_CUR_HI_F		FUNC_TEST=YES
59	IN	GND_17_INV		FUNC_TEST=YES
59	IN	PP5V_AGP_RL		FUNC_TEST=YES
59	IN	INV_17_LCD_PWM_F		FUNC_TEST=YES
59	IN	INV_17_CUR_HI_F		FUNC_TEST=YES
33 8	IN	CPU_VID_R<5..0>		FUNC_TEST=TRUE
36	IN	KPVDD2_FMAX		FUNC_TEST=YES
36	IN	KPGND2_FMAX		FUNC_TEST=YES
36	IN	TDIODE_POS_FMAX		FUNC_TEST=YES
36	IN	TDIODE_NEG_FMAX		FUNC_TEST=YES
36 33	IN	CORE_ISNS_M		FUNC_TEST=YES
36 33	IN	CORE_ISNS_P		FUNC_TEST=YES

PP12V_RUN PP5V_RUN PP24V_RUN PP5V_ALL PP3V3_RUN

	IN	PP12V_RUN	10 TEST POINTS	FUNC_TEST=YES
12 11 7	IN	PP5V_ALL	5 TEST POINTS	FUNC_TEST=YES
18 11 10 7	IN	PP5V_RUN	5 TEST POINTS	FUNC_TEST=YES
50 34 22 18 11 10 7	IN	PP3V3_RUN	5 TEST POINTS	FUNC_TEST=YES
	IN	PP24V_RUN	5 TEST POINTS	FUNC_TEST=YES
83 7	IN	=PP5V_DISK	5 TEST POINTS	FUNC_TEST=YES
83 7	IN	=PP12V_DISK	5 TEST POINTS	FUNC_TEST=YES
	IN	GND	12 TEST POINTS	FUNC_TEST=YES

PP2V5_RUN PP5V_PWRON PP1V2_PWRON PP1V5_RUN PP3V3_PWRON

	IN	PP2V5_RUN		FUNC_TEST=YES
	IN	PP1V5_RUN		FUNC_TEST=YES
18 13	IN	PP5V_PWRON		FUNC_TEST=YES
58 27 18 13	IN	PP3V3_PWRON		FUNC_TEST=YES
	IN	PP1V2_PWRON		FUNC_TEST=YES
23 7 3	IN	=PPVCORE_PWRON_SB		FUNC_TEST=YES
13 8 7	IN	=PP3V3_ALL_SMU		FUNC_TEST=TRUE
31 8 7 3	IN	=PP5V_RUN_CPU		FUNC_TEST=YES
22	IN	PPVCORE_NB		FUNC_TEST=YES
35 34 33 7	IN	PPVCORE_CPU		FUNC_TEST=YES
34 33	IN	PP12V_CPU		FUNC_TEST=YES
33	IN	VCORE_SENSE_GND		FUNC_TEST=YES
33	IN	VCORE_SENSE_VOUT		FUNC_TEST=YES
8 7	IN	SMU_MANUAL_RESET_L	2 TEST POINTS	FUNC_TEST=YES
13 7	IN	SYS_POWER_BUTTON_L	2 TEST POINTS	FUNC_TEST=YES
7	IN	POWER_BUTTON_L		FUNC_TEST=YES
7	IN	RESET_BUTTON_L		FUNC_TEST=YES
13 8	IN	SMU_RESET_L		FUNC_TEST=YES
33 13 11 10 7	IN	SYS_POWERUP_L		FUNC_TEST=YES
50 46 22 11 10 9 8	IN	SYS_SLEEP		FUNC_TEST=YES
13 8	IN	SYS_POWERFAIL_L		FUNC_TEST=YES
9	IN	U900_FEEDBACK		FUNC_TEST=YES
22	IN	U2200_FEEDBACK		FUNC_TEST=YES
59 58	IN	ANALOG_RED		FUNC_TEST=YES
59 58	IN	ANALOG_GRN		FUNC_TEST=YES
59 58	IN	ANALOG_BLU		FUNC_TEST=YES
101 25	IN	AUDIO_LO_DET_L		FUNC_TEST=YES
75	IN	ROM_WP_L		FUNC_TEST=YES
83 80	IN	UATA_DD<15..0>		FUNC_TEST=TRUE
83 80	IN	UATA_DA<2..0>		FUNC_TEST=TRUE
83 80	IN	UATA_CS0_L		FUNC_TEST=YES
83 80	IN	UATA_CS1_L		FUNC_TEST=YES
83 80	IN	UATA_RESET_L		FUNC_TEST=YES
83	IN	UATA_DSTROBE_R		FUNC_TEST=YES
83 80	IN	UATA_HSTROBE		FUNC_TEST=YES
83 80 83 80	IN	UATA_STOP		FUNC_TEST=YES
83	IN	UATA_DMARQ_R		FUNC_TEST=YES
83 80	IN	UATA_DMACK_L		FUNC_TEST=YES
83	IN	UATA_INTRQ_R		FUNC_TEST=YES
83	IN	UATA_IOCS16_PU		FUNC_TEST=YES
83	IN	UATA_CSEL_PD		FUNC_TEST=YES
83	IN	UATA_DASP_L		FUNC_TEST=TRUE
36 31	IN	TDIODE_NEG		FUNC_TEST=YES

FUNC TEST

SYNC_MASTER=N/A SYNC_DATE=N/A

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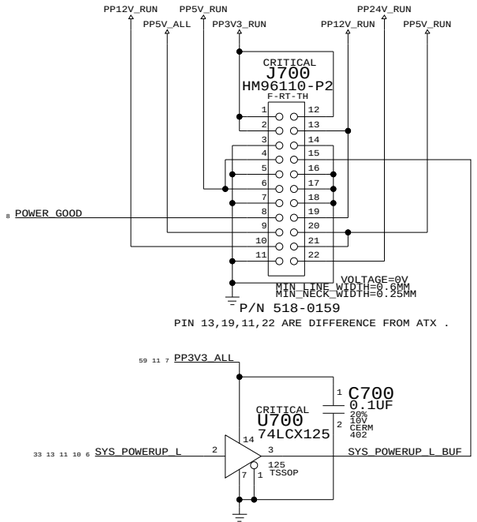
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 6 OF 102	



RUN RAILS

ONLY ON IN RUN

PP24V_RUN
VOLTAGE=24V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
=PP24V_GRAPHICS 59

PP12V_RUN
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
=PP12V_AGP 50 59
=PP12V_RUN_CPU 33
=PP12V_DISK 6 83

XW700 SM
PP12V_AUDIO_CODEC 102
XW704 SM
XW701 SM
PP12V_AUDIO_SPKRAMP 100
XW705 SM

PP5V_RUN
18 11 10 6 PP5V_RUN
VOLTAGE=5V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
=PP5V_PATA 83
=PP5V_DISK 6 83
=PP5V_AGP 50 59
=PP5V_RUN_CPU 3 6 8 31
PP5V_AUDIO 101

PP3V3_RUN
50 34 22 18 11 10 6 PP3V3_RUN
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
=PP3V3_AGP 48 49 50 56 58 59
PP3V3_AUDIO 95 100 101 102
=PP3V3_RUN_CPU 33
=PP3V3_PATA 83
=PP3V3_SB_PCI 74
=PP3V3_PCI 25 74 75 76 77
=PPVIO_PCI_USB2 77
=PP3V3_DISK 83

PP2V5_RUN
VOLTAGE=2.5V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
PP2V5_GPU 52 54 55
=PP2V5_RUN_CPU 31
=PP2V5_RUN_RAM 44 45

PP1V5_RUN
VOLTAGE=1.5V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
=PP1V5_AGP 48 49 50
=PPVCORE_PULSAR 26
=PP1V2_EI_CPU 14 18 29 30 31
=PP1V2_EI_NB 14 18 28

35 34 33 6 PPVCORE_CPU
MAKE_BASE=TRUE
=PPVCORE_CPU 29 31 32 36

PP1V2_RUN
VOLTAGE=1.2V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
=PP1V2_HT 24 60
=PP1V2_PULSAR 26
NOSTUFF
R720
0
5%
1/8W
MF-LF
805
PPVCORE_GPU 22 50 51

PWRON RAILS

ON IN RUN AND SLEEP

PP5V_PWRON
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
PP5V_PWRON_USB 92
=PP5V_PWRON_CPU 36
=PP5V_PWRON_VESTA 12

PP3V3_PWRON
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
=PP3V3_PWRON_SB 23 25 74
=PPPCI64_PWRON_SB 23
=PPPCI32_PWRON_SB 23
PP3V3_PWRON_MODEM 94
=PP3V3_PWRON_USB 91
PP3V3_PWRON_BT 76
=PP3V3_PWRON_CPU 36
=PP3V3_PWRON_EI 28
=PP3V3_PWRON_VESTA 12
=PP3V3_PWRON_RAM 46

PP2V5_PWRON
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
=PP2V5_PWRON_SB 23 25 74 88
=PP2V5_PWRON_RAM 26 37 40 46
=PP2V5_HT 60 64
=PP2V5_PWRON_HT 62
=PP2V5_ENET 87

PP1V5_PWRON
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
=PP1V5_PWRON_NB_AVDD 28 37 48 60
=PPVCORE_PWRON_PULSAR 26
=PPVCORE_NB 22

PP1V2_PWRON
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.2V
=PP1V2_PWRON_HT 62
=PP1V2_PWRON_DISK_SB 80
=PP1V2_PWRON_SB 25
=PPVCORE_PWRON_SB 3 6 23

ALL RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP5V_ALL
12 11 6 PP5V_ALL
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
=PP5V_ALL_CPU 36

59 11 7 PP3V3_ALL
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
=PP3V3_ALL_SMU 6 8 13
=PP3V3_ALL_CPU 36
PP3V3_VESTA 12
=PP3V3_ENET 86 87
=PP3V3_FW 89 90
=PP3V3_ENETFW 89

10 PP1V2_ALL
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
PP1V2_VESTA 12
=PP1V2_ENETFW 86 89

GND RAILS

102 GND_AUDIO
XW702 SM
XW706 SM
102 100 GND_AUDIO_SPKRAMP
XW703 SM
XW707 SM

CHASSIS GND

102 101 GND_CHASSIS_AUDIO_EXTERNAL
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
VOLTAGE=0
MIN_LINE_WIDTH=0.6MM
ZH700
315R138
59 GND_CHASSIS_VGA
92 GND_CHASSIS_USB
90 GND_CHASSIS_FIREWIRE

59 6 GND_CHASSIS_TMDS
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
ZH710
315R138
ZH702
7R4.15
87 GND_CHASSIS_RJ45
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
SH700
101 GND_CHASSIS_AUDIO_INTERNAL
MAKE_BASE=TRUE
21 GND_CHASSIS_LED
SHLD-IO-CONN
Q45-TH1
805-5664
ZH703
6.00MM-PTH
59 GND_CHASSIS_17_INCH_INVERTER
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
NOSTUFF
SDF700
HSK-NUT-6.5MM
TH
59 GND_CHASSIS_20_INCH_INVERTER
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
SDF700 IS USED FOR CPU HEATSINK MOUNTING

RTC BATTERY

ALWAYS ON (TRICKLE)

NOSTUFF
R703
0
5%
1/16W
MF-LF
402
13 =PP3V3_ALL_RTC
PP3V3_ALL_RTC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAKE_BASE=TRUE
DS700
SOD-123
B0530WXF
PP3V3_ALL_BATT_SAFETY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
R702
1K
5%
1/16W
MF-LF
402
CRITICAL
J702
BB10209-A5
PP3V3_ALL_BATT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
TH

POWER CONN / ALIAS

SYNC_MASTER=N/A
SYNC_DATE=N/A

APPLE COMPUTER INC.

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PCI CLOCKS

TP_NB_THMI — MAKE_BASE=TRUE — NB_THMI (24)
TP_THMO — MAKE_BASE=TRUE — NB_THMO (24)
6 TP_RAM_CKE_R<2> — MAKE_BASE=TRUE — RAM_CKE_R<2> (37)
6 TP_RAM_CKE_R<3> — MAKE_BASE=TRUE — RAM_CKE_R<3> (37)
6 TP_RAM_CKE_R<6> — MAKE_BASE=TRUE — RAM_CKE_R<6> (37)
6 TP_RAM_CKE_R<7> — MAKE_BASE=TRUE — RAM_CKE_R<7> (37)
6 TP_RAM_MUXEN0 — MAKE_BASE=TRUE — RAM_MUXEN0 (37)
6 TP_RAM_MUXEN4 — MAKE_BASE=TRUE — RAM_MUXEN4 (37)
6 TP_RAM_CS_L_R<2> — MAKE_BASE=TRUE — RAM_CS_L_R<2> (37)
6 TP_RAM_CS_L_R<3> — MAKE_BASE=TRUE — RAM_CS_L_R<3> (37)
6 TP_RAM_CS_L_R<10> — MAKE_BASE=TRUE — RAM_CS_L_R<10> (37)
6 TP_RAM_CS_L_R<11> — MAKE_BASE=TRUE — RAM_CS_L_R<11> (37)

PCI_CLK33M_USB2 — MAKE_BASE=TRUE — PCI_CLK_GP0 (27)
=PCI_CLK33M_USB2 (77)
TP_PCI_CLK_GP1 — MAKE_BASE=TRUE — PCI_CLK_GP1 (27)
6 PCI_CLK33M_AIRPORT — MAKE_BASE=TRUE — PCI_CLK_P3 (27)
PCI_CLK33M_AIRPORT (76)
6 TP_PCI_CLK_P4 — MAKE_BASE=TRUE — PCI_CLK_P4 (27)
74 27 PCI_CLK33M_SB_EXT — MAKE_BASE=TRUE — PCI_CLK_P1 (27)

SMU

TP_ALS0_OUT — MAKE_BASE=TRUE — ALS0_OUT (13)
TP_ALS1_OUT — MAKE_BASE=TRUE — ALS1_OUT (13)
TP_ALS_GAIN_BOOST — MAKE_BASE=TRUE — ALS_GAIN_BOOST (13)
TP_SMU_ONEWIRE — MAKE_BASE=TRUE — SMU_ONEWIRE (13)
TP_SYS_SLOT_PWR — MAKE_BASE=TRUE — SYS_SLOT_PWR (13)
TP_SMU_PWRSEQ_P1_3 — MAKE_BASE=TRUE — SMU_PWRSEQ_P1_3 (13)
TP_SYS_DOOR_AJAR_L — MAKE_BASE=TRUE — SYS_DOOR_AJAR_L (13)
TP_FAN_PWM8 — MAKE_BASE=TRUE — FAN_PWM8 (13)
TP_SYS_DRIVE_BAY_INT_L — MAKE_BASE=TRUE — SYS_DRIVE_BAY_INT_L (13)
13 8 SMU_WARM_RESET_L — MAKE_BASE=TRUE — NB_WARM_RESET_L (24)
74 56 6 PCI_RESET_L — MAKE_BASE=TRUE — PCI_AIRPORT_RESET_L (76)
GPU_RESET_L (49)
=PCI_ROM_RESET_L (75)
=PCI_USB2_RESET_L (77)

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
16465 SMU_RESET	P25MM		SYS_COLD_RESET_L 13 24
16471 SMU_RESET	P25MM		SYS_WARM_RESET_L 8 25 74 77

DIAG LED

PP5V_ALL
R850 180 5% 1/16W MF-LF 402
LED850P1
LED850 RED SM
LED850P2
13 DIAG_LED — MAKE_BASE=TRUE — R851 1K 5% 1/16W MF-LF 402 — DIAG_LED_R
Q850 2N3904LF SOT23

CPU VID<0:5>

VID CONTROLLED BY SMU

PP3V3_RUN
R814 R816 R817 R808 R809 R804 10K 5% 1/16W MF-LF 402
13 CPU_VID<0> — R819 0 5% 1/16W MF-LF 402 — CPU_VID_R<0> (6 33)
13 CPU_VID<1> — R820 0 — CPU_VID_R<1> (6 33)
13 CPU_VID<2> — R821 0 — CPU_VID_R<2> (6 33)
13 CPU_VID<3> — R822 0 — CPU_VID_R<3> (6 33)
13 CPU_VID<4> — R823 0 — CPU_VID_R<4> (6 33)
13 CPU_VID<5> — R824 0 — CPU_VID_R<5> (6 33)
NOSTUFF J803 BM12B-SRSS-TB 13P
NOSTUFF R832 R831 R830 R829 R827 1K 5% 1/16W MF-LF 402
NOSTUFF R811 20K 5% 1/16W MF-LF 402
NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

DOWNLOAD CONNECTOR

PP3V3_ALL
J802 HC17051 M-ST-TH
13 SMU_BOOT_SCLK
13 SMU_BOOT_CE
13 SMU_BOOT_CNVSS
R826 100 5% 1/16W MF-LF 402
J802_2 — SMU_BOOT_BUSY (13)
SMU_BOOT_RXD (13)
(SMU_BOOT_EPM)
J802_6 — SMU_MANUAL_RESET_L (6 7 8)
SMU_BOOT_TXD (13)
518-0158
NOSTUFF R806 R807 10K 5% 1/16W MF-LF 402
NOSTUFF R805 0 5% 1/16W MF-LF 402
R803 10K 5% 1/16W MF-LF 402
J802 & R826 CAN MOVE TO DEVELOPMENT BOM POST RAMP

DEVELOPMENT J800 U.FL-R-SMT

24 NB_PMR_OBSV
F-ST-SM
518S0104

SMU ANALOG VREF

13 PP3V3_ALL_SMU_AVCC
NOSTUFF R818 200 1% 1/16W MF-LF 402
PPVREF_SMU — MAKE_BASE=TRUE — =PPVREF_SMU (13)
NOSTUFF C801 2.2UF 20% 10V CERM 805
R802 0 — PPVREF_SMU_ADC_REF (36)
NOSTUFF VR801 2.5V SOT-23
NOSTUFF C802 0.47UF 20% 16V CERM 603
GND_SMU_AVSS (13 33 36)
NOSTUFF R828 0 — GND_SMU_AVSS_DAGND (36)

POWER_FAIL_L CONNECTION

7 POWER_GOOD
PP3V3_ALL
NOSTUFF R813 430 5% 1/16W MF-LF 402
NOSTUFF R812 10K 5% 1/16W MF-LF 402
SYS_POWERFAIL_L (6 13)
R860 4.7K 5% 1/16W MF-LF 402
POWER_GOOD IS A 5V DRIVEN SIGNAL FROM POWER SUPPLY
2K PULLUP INSIDE P/S

BACKUP SMU RESET CIRCUIT

13 7 6 =PP3V3_ALL_SMU
NOSTUFF C800 0.1UF 20% 10V CERM 402
NOSTUFF R890 1K 5% 1/16W MF-LF 402
U890 SM
VCC
8 7 6 SMU_MANUAL_RESET_L — DELAY — NOSTUFF RESET — SMU_RESET_L (6 13)
VOLTAGE DETECTOR MC33465N_30ATR
GND
NOSTUFF C890 0.01UF 10% 16V CERM 402
NOSTUFF C891 1UF 10% 6.3V CERM 402
R810 0 5% 1/16W MF-LF 402

PULSAR ERROR_L LED

PP3V3_RUN
DEVELOPMENT R801 4.7K 5% 1/16W MF-LF 402
DEVELOPMENT R800 330 5% 1/16W MF-LF 402
ERROR_LED (6)
DEVELOPMENT D810 RED SM
27 CLOCK_ERROR_L

VESTA JTAG

JTAG_VESTA_TRST_L — MAKE_BASE=TRUE — =JTAG_VESTA_TRST_L (12)
TP_JTAG_VESTA_TCK — MAKE_BASE=TRUE — =JTAG_VESTA_TCK (12)
TP_JTAG_VESTA_TDI — MAKE_BASE=TRUE — =JTAG_VESTA_TDI (12)
TP_JTAG_VESTA_TDO — MAKE_BASE=TRUE — =JTAG_VESTA_TDO (12)
TP_JTAG_VESTA_TMS — MAKE_BASE=TRUE — =JTAG_VESTA_TMS (12)
R840 10K 5% 1/16W MF-LF 402

PLL LOCK LED

31 8 7 6 3 =PP5V_RUN_CPU
DEVELOPMENT R837 180 5% 1/16W MF-LF 402
DEVELOPMENT Q802 2N3906 SM
Q802_B
Q802_E
DEVELOPMENT R838 1K 5% 1/16W MF-LF 402
DEVELOPMENT R835 180 5% 1/16W MF-LF 402
LED802_1
Q803_C
DEVELOPMENT R839 180 5% 1/16W MF-LF 402
29 PLLLOCK — Q803_B
DEVELOPMENT Q803 2N3904LF SOT23
DEVELOPMENT LED802 GREEN 2.0X1.25A

CHKSTOP LED

31 8 7 6 3 =PP5V_RUN_CPU
DEVELOPMENT R833 180 5% 1/16W MF-LF 402
LED801_1
DEVELOPMENT LED801 RED SM
Q800_D
DEVELOPMENT R834 180 5% 1/16W MF-LF 402
Q800_G
DEVELOPMENT Q800 2N7002 SOT23-LF
DEVELOPMENT R836 180 5% 1/16W MF-LF 402
29 14 6 CHKSTOP_L — Q801_B
DEVELOPMENT Q801 2N3904LF SOT23

CPU HEATSINK SMT NUTS

NOSTUFF SDF800 HSK-NUT-6.5MM TH
NOSTUFF SDF801 HSK-NUT-6.5MM TH
NOSTUFF SDF802 HSK-NUT-6.5MM TH
HS_SDF800_1 — C880 0.01UF 20% 16V CERM 402
HS_SDF801_1 — C881 0.01UF 20% 16V CERM 402
HS_SDF802_1 — C882 0.01UF 20% 16V CERM 402
NOSTUFF SDF803 HSK-NUT-6.5MM TH
OMIT ZH804 6P15R5P4
HS_SDF803_1 — C883 0.01UF 20% 16V CERM 402
HS_SDF804_1 — C884 0.01UF 20% 16V CERM 402
SDF700 IS ALSO USED FOR HEATSINK MOUNTING

SHASTA JTAG PULL DOWN

25 JTAG_SB_TRST_L
THESE PINS HAVE INTERNAL PULLUPS
TP_JTAG_SB_TCK — MAKE_BASE=TRUE — JTAG_SB_TCK (25)
TP_JTAG_SB_TDI — MAKE_BASE=TRUE — JTAG_SB_TDI (25)
TP_JTAG_SB_TDO — MAKE_BASE=TRUE — JTAG_SB_TDO (25)
TP_JTAG_SB_TMS — MAKE_BASE=TRUE — JTAG_SB_TMS (25)
R825 10K 5% 1/16W MF-LF 402

SIGNAL ALIAS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6772 | REV. 11
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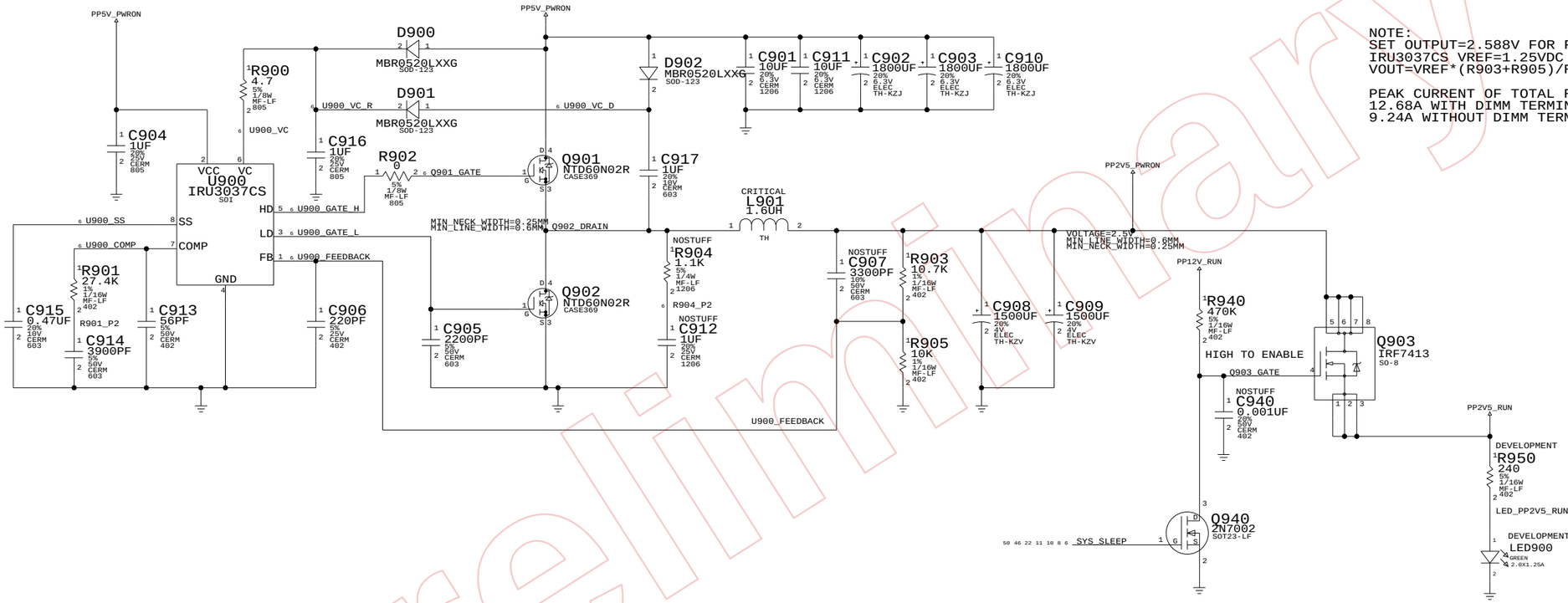
2.5V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=2.588V FOR FRAMEBUFFER.
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R903+R905)/R905=2.588VDC

PEAK CURRENT OF TOTAL RAILS
12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

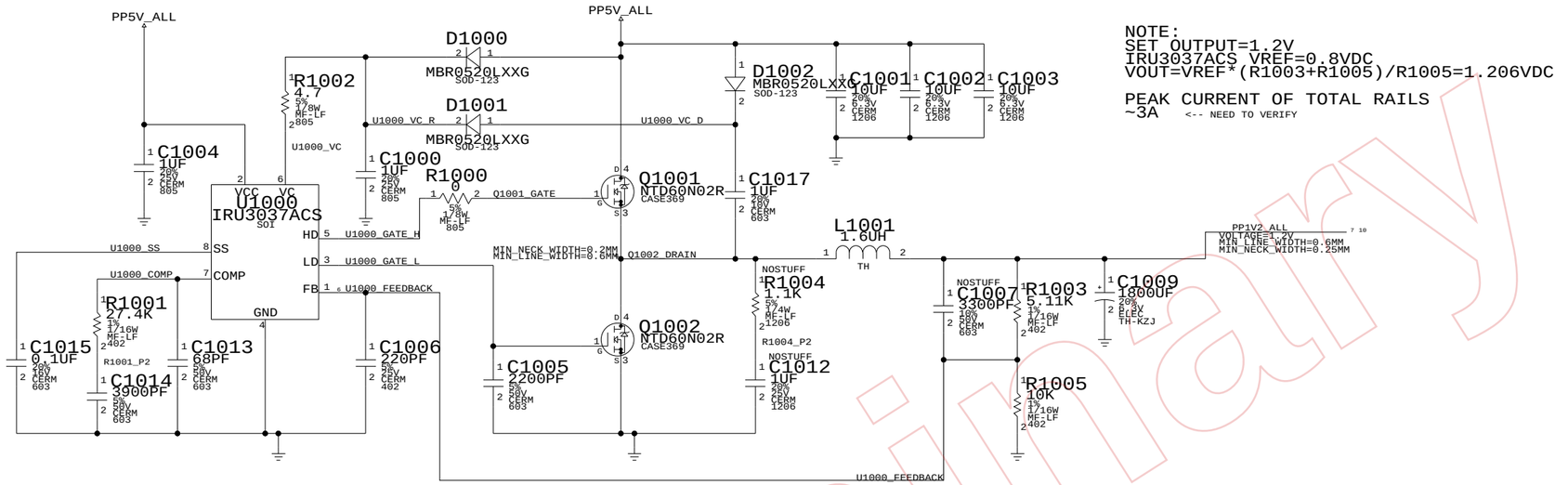
2.5V VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 9 OF 102	

PP1V2_ALL VOLTAGE REGULATOR

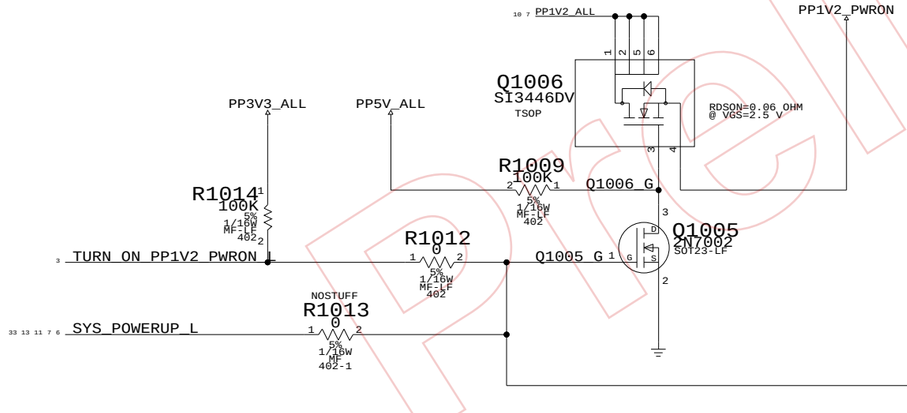


NOTE:
SET OUTPUT=1.2V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.206VDC

PEAK CURRENT OF TOTAL RAILS
~3A <-- NEED TO VERIFY

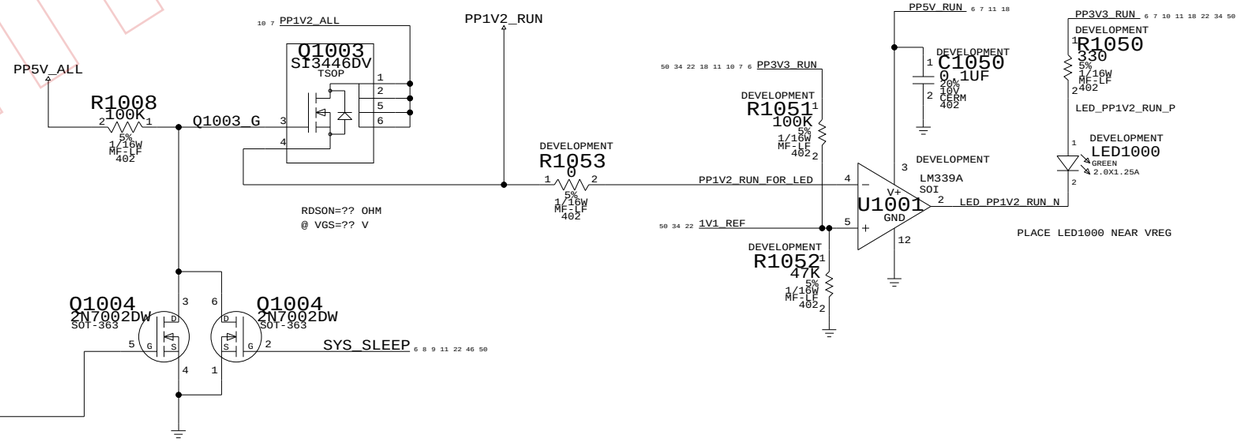
PP1V2_PWRON FET SWITCH

PEAK CURRENT ??A



PP1V2_RUN FET SWITCH

PEAK CURRENT ??A

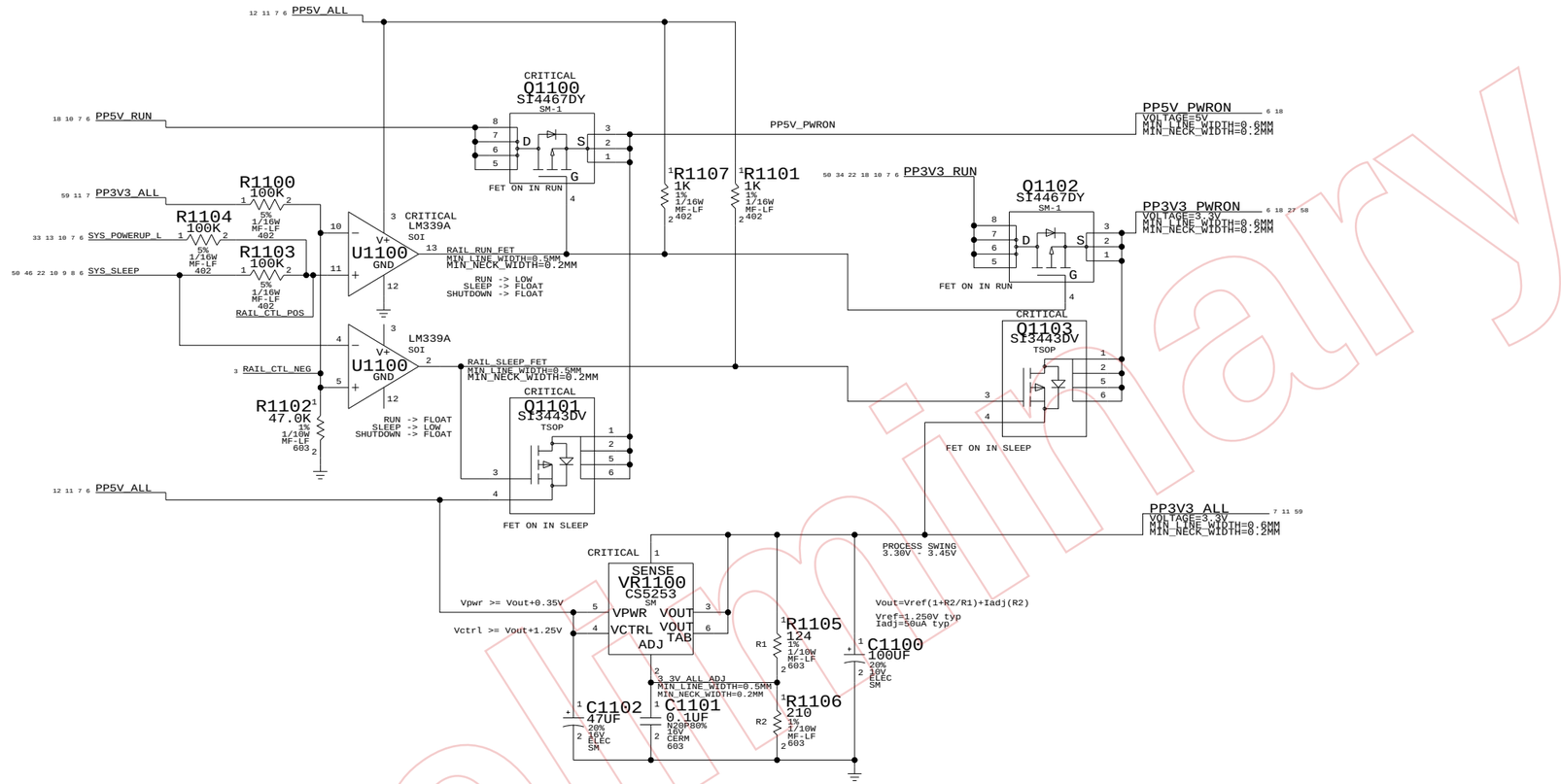


1.2V VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 10 OF 102	



5V & 3.3V VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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D	051-6772	11
SCALE: NONE	SHT 11 OF 102	

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

Ethernet LowPwr

ETHERNET PORTION IN LOW POWER MODE
WHEN NOT IN RUN MODE.

=PP3V3_PWRON_VESTA
=PP5V_PWRON_VESTA
NOSTUFF
R1260 2.0K 5% 1/16W MF-LF 402
R1263 4.7K 5% 1/16W MF-LF 402
PP3V3_VESTA
R1262 10K 5% 1/16W MF-LF 402
VESTA_ENET_LOWPWR
C1260 10UF 20% 6.3V X5R 805
VESTA_ENET_HIGHPWR
Q1260 2N3904LF SOT23
R1261 1K 5% 1/16W MF-LF 402
NOSTUFF
C1261 0.1UF 20% 10V CERM 402

PP5V_ALL
R1265 330 5% 1/10W MF-LF 603
PP3V3_VESTA
R1264 100K 5% 1/16W MF-LF 402
Q1271_B
Q1271 2N3904LF SOT23
Q1270 2N7002 SOT23-LF
Q1270_G
C1270 10UF 20% 6.3V CERM 402

2.5V LDO

CRITICAL
U1280 MM1572FN SOT-25A
PP3V3_VESTA
C1280 1UF 10% 6.3V CERM 402
VESTA2V5_NOISE
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
C1281 0.01UF 10% 16V CERM 402
C1282 10UF 10% 6.3V X5R 805
PP2V5_VESTA
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
MAKE_BASE=TRUE
=PP2V5_ENETFW
Vout = 2.5V @ 150 mA

PP1V2_VESTA
L1200 FERR-EMI-600-OHM SM
PP1V2_VESTA_AVDDL
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
C1208 10UF 20% 6.3V X5R 805
C1200 0.1UF 20% 10V CERM 402 L6/M6
C1201 0.1UF 20% 10V CERM 402 L9/M9
C1202 0.1UF 20% 10V CERM 402 N5/N6
C1203 0.1UF 20% 10V CERM 402 N9/N10
C1210 0.1UF 20% 10V CERM 402
C1211 0.1UF 20% 10V CERM 402
C1212 0.1UF 20% 10V CERM 402
C1213 0.1UF 20% 10V CERM 402

C1220 0.1UF 20% 10V CERM 402
C1221 0.1UF 20% 10V CERM 402
C1222 0.1UF 20% 10V CERM 402
C1223 0.1UF 20% 10V CERM 402
C1224 0.1UF 20% 10V CERM 402
C1225 0.1UF 20% 10V CERM 402
C1230 0.1UF 20% 10V CERM 402
C1231 0.1UF 20% 10V CERM 402
C1240 0.1UF 20% 10V CERM 402
C1241 0.1UF 20% 10V CERM 402
C1242 0.1UF 20% 10V CERM 402
C1243 0.1UF 20% 10V CERM 402

PP3V3_VESTA
R1251 82K 5% 1/10W MF-LFM 402
NO STUFF
R1252 4.7K 5% 1/10W MF-LFM 402
R1252 to enable wirespeed feature
ENETFW_RESET
Q1250 2N3904LF SOT23
NO STUFF
C1250 10UF 20% 6.3V CERM 805

To keep Vesta from being held
in reset when system is off
NOTE: Reset GPIO is active HIGH

VESTA_RESET_L
Schmitt trigger

VESTA MISC

OMIT
U8600 BCM5462 FBGA-200
1 OF 3

RESET*	H4	
TDI	D7	=JTAG_VESTA_TDI
TDO	E10	=JTAG_VESTA_TDO
TCK	E7	=JTAG_VESTA_TCK
TMS	E8	=JTAG_VESTA_TMS
TRST*	D8	=JTAG_VESTA_TRST_L
DNC	B9	TP_VESTA_DNC_B9
DNC	C9	TP_VESTA_DNC_C9
DNC	E9	TP_VESTA_DNC_E9
NC	C3	
NC	M13	
DVDD	B1, B15, C15, J1	
AVDDL	L6, L9, M6, M9, N5, N6, N9, N10	
AVDD	P4, P5, P10, P11, R3, R12	
PVDD	A15, N4	
OVDD	A1, A7, F15, K1	
2.5V_EN	M3	TP_VESTA_2_5V_EN
REGSUP1	E1	TP_VESTA_REGSUP1
REGSEN1	F1	TP_VESTA_REGSEN1
REGCTL1	G5	TP_VESTA_REGCTL1
REGSUP2	E2	TP_VESTA_REGSUP2
REGSEN2	F2	TP_VESTA_REGSEN2
REGCTL2	G4	TP_VESTA_REGCTL2
AGND	H11, H12, J11, J12, L7, L8, M7, M8, N7, N8, P6, P7, P8, P9	
GND	A2, B2, B7, C14, F14, J2, K2	

Vesta Core / Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	P25MM		SMU_CLK10M_XIN 13
	P25MM		SMU_CLK10M_XOUT 13
	P25MM		SMU_CLK10M_XOUT_R 13
RTC_CLK32K_XTAL	P25MM		RTC_CLK32K_X1 13
	P25MM		RTC_CLK32K_X2 13

Page Notes

Power aliases required by this page:
- _P3V3_ALL_SMU
- _P3V3_ALL_RTC
- _P3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

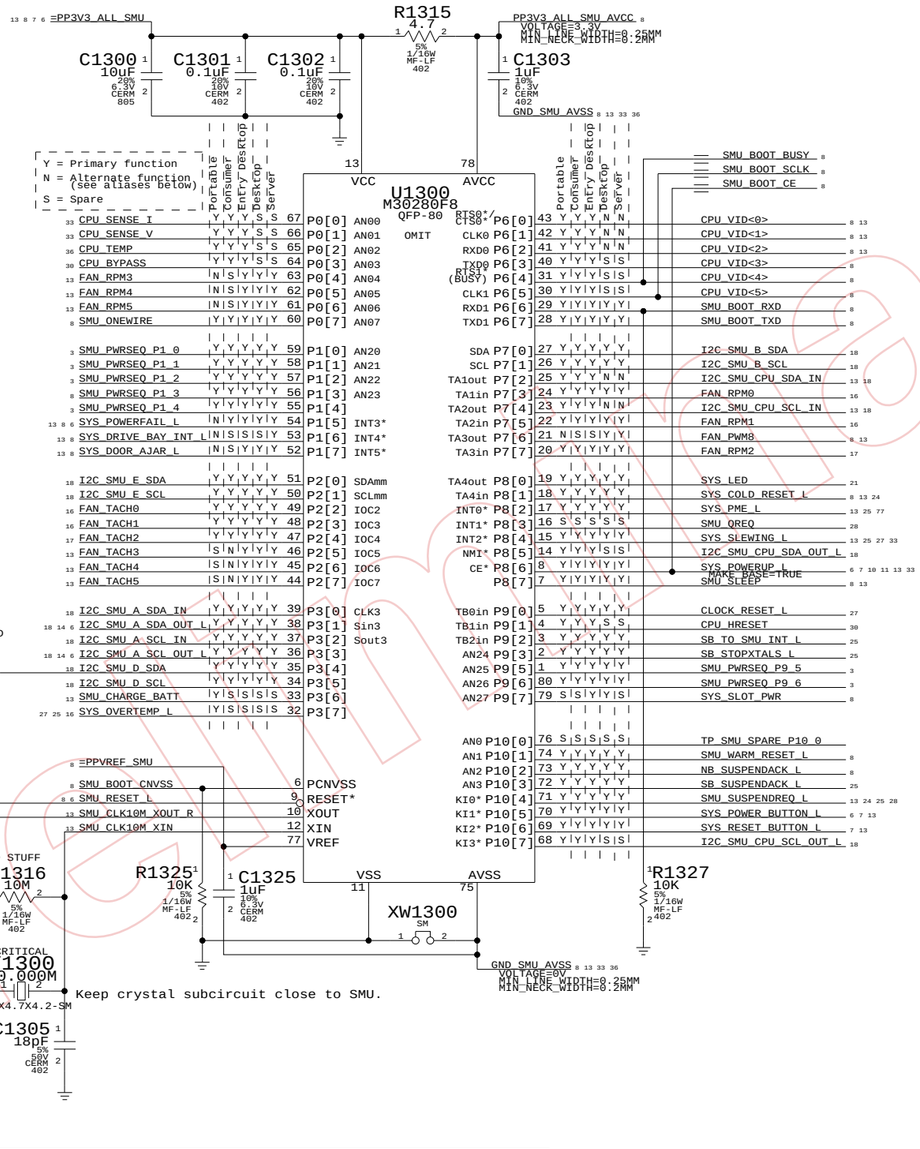
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

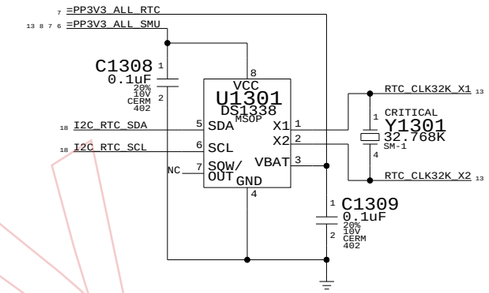
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

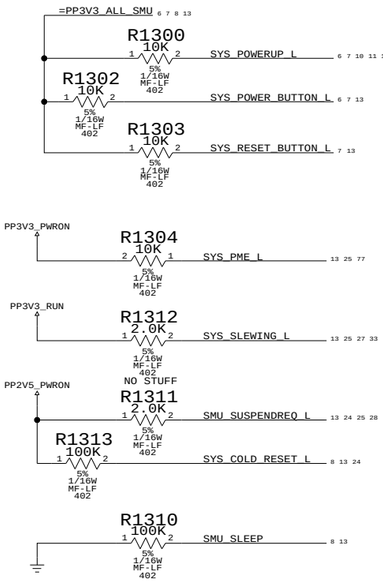
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4	ALS0_OUT	8
FAN_RPM4	0.5	ALS1_OUT	8
FAN_RPM5	0.6	ALS_GAIN_BOOST	8
SYS_POWERFAIL_L	1.5	SMU_ACIN	
SYS_DRIVE_BAY_INT_L	1.6	SMU_BATT_DET_L	
SYS_DOOR_AJAR_L	1.7	SYS_LID_OPEN	
FAN_PWM8	7.6	SYS_KBDLED	

Consumer

	Port		
FAN_TACH3	2.5	SYS_LED_RED	21
FAN_TACH4	2.6	SYS_LED_GREEN	21
FAN_TACH5	2.7	SYS_LED_BLUE	21
SMU_CHARGE_BATT	3.6	DIAG_LED	8

Tower & Server

	Port		
CPU_VID<0>	6.0	FAN_TACH6	
CPU_VID<1>	6.1	FAN_TACH7	
CPU_VID<2>	6.2	FAN_TACH8	
I2C_SMU_CPU_SDA_IN	7.2	FAN_PWM6	
I2C_SMU_CPU_SCL_IN	7.4	FAN_PWM7	

System Management Unit

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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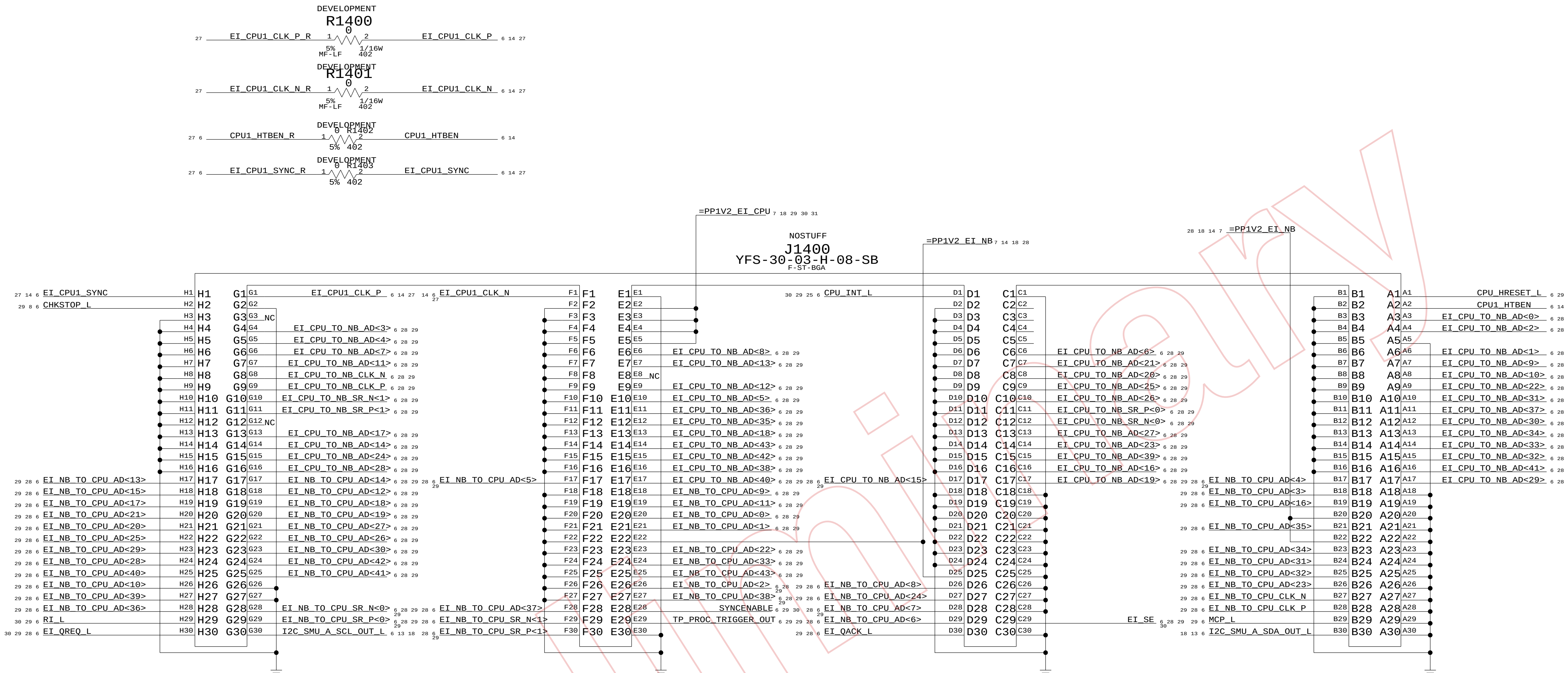

CPU LOGIC ANALYZER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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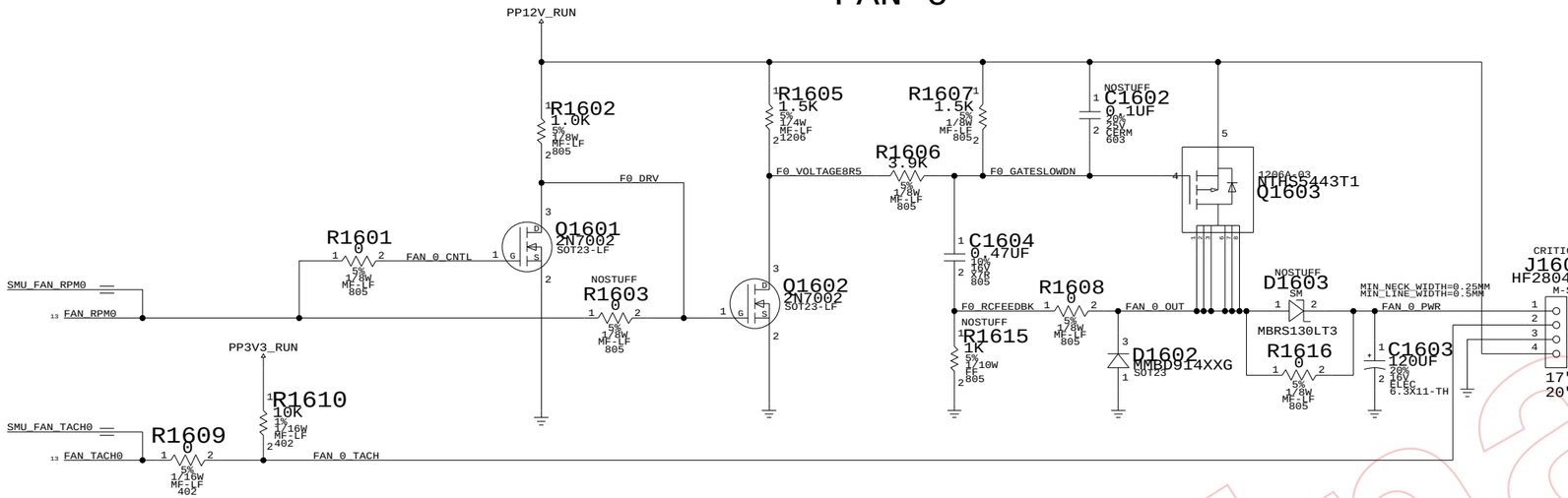
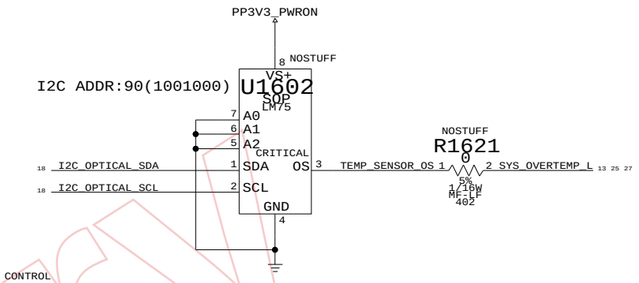
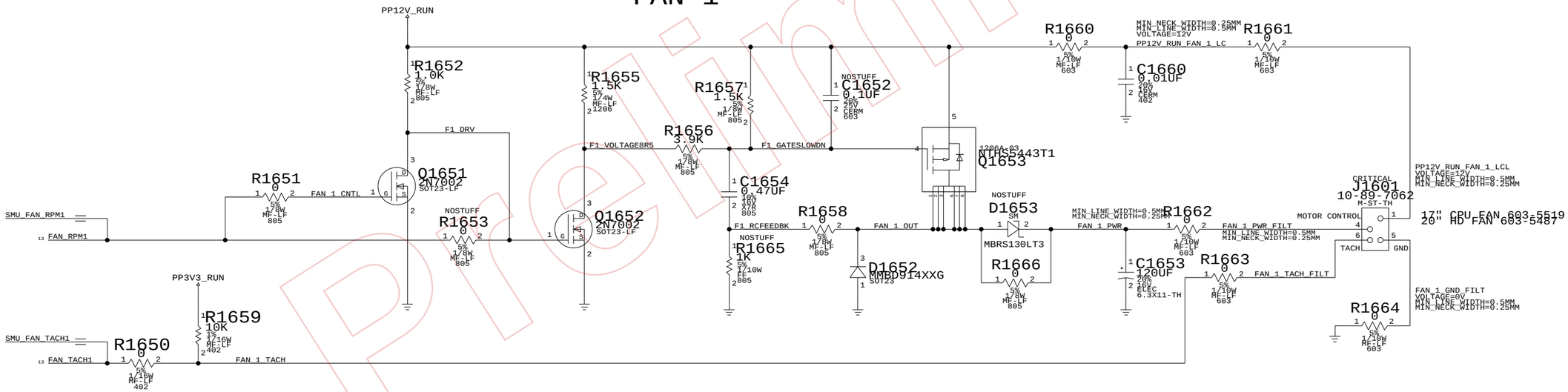
FAN 0



OPTICAL TEMP SENSOR



FAN 1



FAN 0, 1 & SYSTEM TEMP

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

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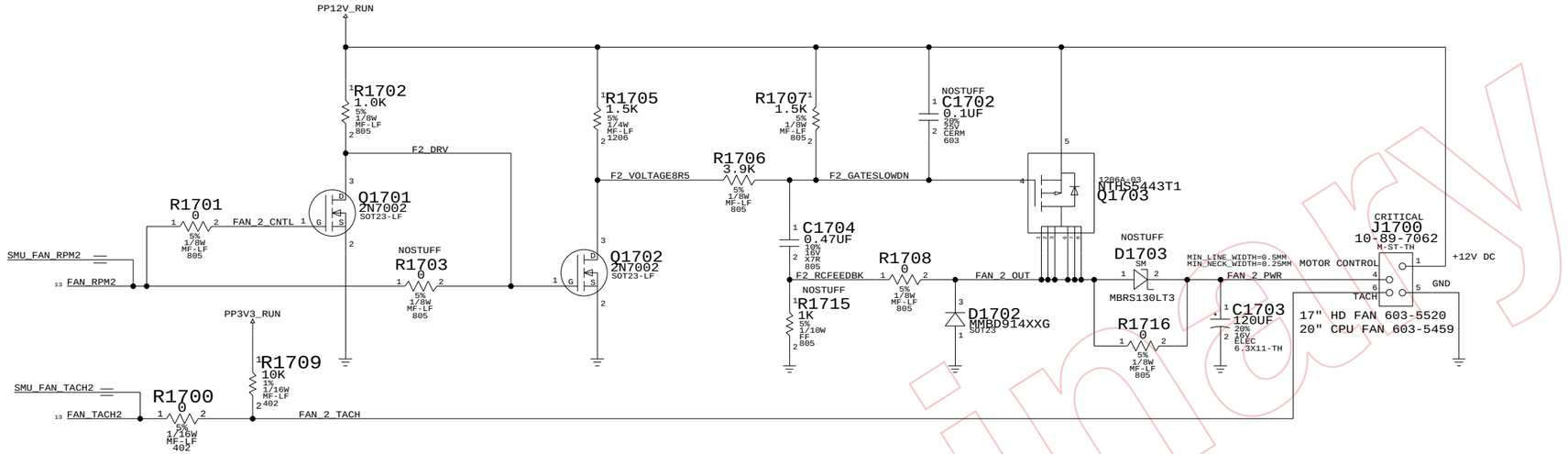
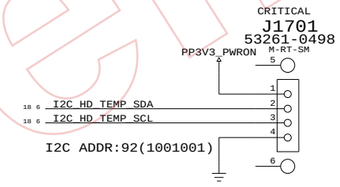
FAN 2



REMOTE HARD DRIVE TEMP SENSOR



518S0193

FAN 2 & HD TEMP	
SYNC_MASTER=N/A	SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 17 OF 102	

I2C A BUS

R1832 0 603 NOSTUFF — 11 6 PP5V_PWRON — PP5V_U1800
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.2MM
R1833 0 603 NOSTUFF — 11 10 7 6 PP5V_RUN

50 34 22 11 10 7 6 PP3V3_RUN — 58 27 18 11 6 PP3V3_PWRON

C1800 0.1UF 20% 10V CERM 402
NOSTUFF R1809 4.7K 5% 1/16W MF-LF 402
R1828 4.7K 5% 1/16W MF-LF 402
C1802 0.1UF 20% 10V CERM 402
R1808 200 5% 1/16W MF-LF 402
R1810 200 5% 1/16W MF-LF 402
=PP1V2_EI_NB 7 14 28

NOSTUFF R1830 2.0K 5% 1/16W MF-LF 402
R1831 2.0K 5% 1/16W MF-LF 402
R1800 2.0K 5% 1/16W MF-LF 402
R1801 2.0K 5% 1/16W MF-LF 402

SMU
MASTER
U1300
13 I2C_SMU_A_SDA_IN MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
14 13 6 I2C_SMU_A_SDA_OUT_L MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
13 I2C_SMU_A_SCL_IN MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
14 13 6 I2C_SMU_A_SCL_OUT_L MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 36-39

LM339A SOI U1800 GND — Q1800 2N7002DW SOT-363

U3LITE
U3
I2C_NB_A_SDA 24
I2C_NB_A_SCL 24
PINS A20, B20

NOSTUFF R1820 0 5% 1/16W MF-LF 402
NOSTUFF R1821 0 5% 1/16W MF-LF 402

58 27 18 11 6 PP3V3_PWRON
R1819 2.0K 5% 1/16W MF-LF 402
R1818 2.0K 5% 1/16W MF-LF 402

=PP1V2_EI_CPU 7 14 29 30 31
R1816 200 5% 1/16W MF-LF 402
R1817 200 5% 1/16W MF-LF 402

SMU
MASTER
U1300
13 I2C_SMU_CPU_SCL_IN MAKE_BASE=TRUE — I2C
13 I2C_SMU_CPU_SCL_OUT_L MAKE_BASE=TRUE — I2C
13 I2C_SMU_CPU_SDA_IN MAKE_BASE=TRUE — I2C
13 I2C_SMU_CPU_SDA_OUT_L MAKE_BASE=TRUE — I2C
PINS 14,25,23,68

RP1800 0 5% 1/16W SM-LF
SMU_CPU_JTAG_OR_I2C
I2C_CPU_A_SCL — NET_SPACING_TYPE=I2C
I2C_CPU_A_SDA_TO_SMU
I2C_CPU_A_SDA_TO_CPU

CPU
U2900
I2C_CPU_A_SCL 29
I2C_CPU_A_SDA 29
PINS AA20, Y21

LM339A SOI U1800 GND — Q1801 2N7002DW SOT-363
I2C_CPU_SCL_LS

NOSTUFF RP1801 0 5% 1/16W SM-LF
CPU JTAG
JTAG_CPU_TDO 29 30
JTAG_CPU_TDI 29 30
JTAG_CPU_TMS 29 30
JTAG_CPU_TCK 29 30

C1801 0.1UF 20% 10V CERM 402
R1811 4.7K 5% 1/16W MF-LF 402
I2C_0V6_REF
USE 576 OHM FOR R1811 IF 5V RAIL IS USED FOR REFERENCE

I2C B BUS

PP3V3_PWRON
R1803 2.0K 5% 1/16W MF-LF 402
R1802 2.0K 5% 1/16W MF-LF 402

SMU
MASTER
U1300
13 I2C_SMU_B_SDA MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
13 I2C_SMU_B_SCL MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 26, 27

PULSAR
U2600
27 I2C_CLOCK_SDA
27 I2C_CLOCK_SCL
PINS C1, B1

OPTICAL TEMP SENSOR
U1602
16 I2C_OPTICAL_SDA
16 I2C_OPTICAL_SCL
PINS 1, 2
I2C ADDR:90

AMBIENT LIGHT SENSOR
J2100
21 I2C_ALS_SDA
21 I2C_ALS_SCL
PINS 2, 3
I2C ADDR:94??
J2100 CAN BE USED AS A SECOND TEMP SENSOR

HD TEMP SENSOR
U1702
17 6 I2C_HD_TEMP_SDA
17 6 I2C_HD_TEMP_SCL
PINS 2, 3
I2C ADDR:92

GPU TEMP SENSOR
U5890
58 I2C_GPU_DIODE_SDA
58 I2C_GPU_DIODE_SCL
PINS 7, 8
I2C ADDR:98

I2C C BUS

PP2V5_PWRON
R1805 2.0K 5% 1/16W MF-LF 402
R1804 2.0K 5% 1/16W MF-LF 402
NET_SPACING_TYPE=I2C
NET_SPACING_TYPE=I2C

U3LITE
MASTER
U3
I2C_NB_C_SDA MAKE_BASE=TRUE 24
I2C_NB_C_SCL MAKE_BASE=TRUE 24
PINS C21, E21

DIMMS
J4000 = A0
J4001 = A2
I2C_DIMM_SDA 40
I2C_DIMM_SCL 40
PINS 91, 92
OF EACH DIMM

I2C D & E BUS

PP2V5_PWRON
R1812 2.0K 5% 1/16W MF-LF 402
R1813 2.0K 5% 1/16W MF-LF 402
PP3V3_ALL
R1807 2.0K 5% 1/16W MF-LF 402
R1806 2.0K 5% 1/16W MF-LF 402

U3LITE 'B'
U3
24 I2C_NB_B_SDA — I2C
24 I2C_NB_B_SCL — I2C
PINS C20, B21

RTC
U1301
I2C — I2C_RTC_SDA 13
I2C — I2C_RTC_SCL 13
PINS 5, 6

NOSTUFF R1822 0 5% 1/16W MF-LF 402
NOSTUFF R1823 0 5% 1/16W MF-LF 402
NOSTUFF R1824 0 5% 1/16W MF-LF 402
R1826 0 5% 1/16W MF-LF 402
NOSTUFF R1825 0 5% 1/16W MF-LF 402
R1827 0 5% 1/16W MF-LF 402

SMU OLD 'E'
MASTER
U1300
13 I2C_SMU_E_SDA — I2C
13 I2C_SMU_E_SCL — I2C
PINS 50, 51

SMU NEW 'E'
MASTER
U1300
I2C — I2C_SMU_D_SDA 13
I2C — I2C_SMU_D_SCL 13
PINS 34, 35

I2C SB BUS

SHASTA
MASTER
U2300
25 6 I2C_SB_SDA MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
25 6 I2C_SB_SCL MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS Y9, AB7

AUDIO
U9500 / AU300
95 I2C_AUDIO_SDA
95 I2C_AUDIO_SCL
PINS 18, 19

PP3V3_RUN
R1815 1K 5% 1/16W MF-LF 402
R1814 1K 5% 1/16W MF-LF 402

I2C CONNECTIONS

SYNC_MASTER=N/A — SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 11

SCALE NONE | SHT 18 OF 102

TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS

PLACE THESE PARTS CLOSE TO SMU IC

PWM INPUT FROM SMU

100% DUTY CYCLE OF 3V-PP PWM = 0.5V

5MV INPUT OFFSET

CHANGE R2100 VALUE TO SET LED CURRENT
MAX LED CURRENT = 0.5 / R

<-- 17 INCH

PLACE THESE PARTS CLOSE TO SMU IC

PWM INPUT FROM SMU

<-- 17 INCH

PLACE THESE PARTS CLOSE TO SMU IC

PWM INPUT FROM SMU

<-- 17 INCH

20 INCH -->

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
114S1821	3	RES, 18.2 OHM, 1%, 402	R2100,R2113,R2126	NOSTUFF

AMBIENT LIGHT SENSOR

J2100 CAN BE USED AS A SECOND TEMP SENSOR

PLACE THESE PARTS CLOSE TO SMU IC

(STUFF WHEN SYS_LED_L = ACTIVE HIGH)
(AND NO STUFF R2132, R2119 & Q2100)

INDICATOR LED

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 21 OF 102	

=PPVCORE_NB

C2222 0.1UF 20% 16V CERM 402 | C2223 0.1UF 20% 16V CERM 402 | C2225 0.1UF 20% 16V CERM 402 | C2227 0.1UF 20% 16V CERM 402 | C2228 0.1UF 20% 16V CERM 402 | C2229 0.1UF 20% 16V CERM 402 | C2230 0.1UF 20% 16V CERM 402 | C2231 0.1UF 20% 16V CERM 402 | C2232 0.1UF 20% 16V CERM 402 | C2233 0.1UF 20% 16V CERM 402 | C2234 0.1UF 20% 16V CERM 402 | C2235 0.1UF 20% 16V CERM 402 | C2236 0.1UF 20% 16V CERM 402 | C2237 0.1UF 20% 16V CERM 402 | C2238 0.1UF 20% 16V CERM 402 | C2239 0.1UF 20% 16V CERM 402 | C2240 0.1UF 20% 16V CERM 402 | C2242 0.1UF 20% 16V CERM 402 | C2243 0.1UF 20% 16V CERM 402 | C2244 0.1UF 20% 16V CERM 402 | C2245 0.1UF 20% 16V CERM 402 | C2246 0.1UF 20% 16V CERM 402 | C2247 0.1UF 20% 16V CERM 402

NOTE:
SET OUTPUT=1.5VDC FOR U3LITE CORE
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R2203+R2205)/R2205=1.53VDC

7.73A OF PEAK CURRENT DRAW ON PCORE_NB

PP5V_PWRON | PP5V_PWRON | PP5V_PWRON

D2200 MBR0520LXXG SOD-123 | D2202 MBR0520LXXG SOD-123 | D2201 MBR0520LXXG SOD-123

R2200 4.7 5% 1/8W MF-LF 2805

U2200_VC_R | U2200_VC_D | U2200_VC

C2204 1UF 20% 25V CERM 805 | C2216 1UF 20% 25V CERM 805

U2200 IRU3037CS SOI

R2202 0 5% 1/8W MF-LF 805 — U2200_GATE_H — Q2201_GATE

Q2201 NTD60N02R CASE369 | C2217 1UF 20% 25V CERM 805

C2201 10UF 20% 6.3V CERM 1206 | C2210 10UF 20% 6.3V CERM 1206 | C2202 1800UF 20% 6.3V FLEX TH-KZJ | C2203 1800UF 20% 6.3V FLEX TH-KZJ

L2201 1.6UH TH

U2200_SS — SS
U2200_COMP — COMP
GND
HD — U2200_GATE_H
LD — U2200_GATE_L
FB — U2200_FEEDBACK

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
Q2202_DRAIN

Q2202 NTD60N02R CASE369

R2201 27.4K 1% 1/16W MF-LF 402 — R2201_P2

C2214 0.1UF 20% 16V CERM 603 | C2213 68PF 5% 50V CERM 603 | C2215 3900PF 5% 50V CERM 603 | C2206 220PF 5% 25V CERM 402 | C2205 2200PF 5% 50V CERM 603

R2204 7.1K 1% 1/16W MF-LF 402 — R2204_P2 — NOSTUFF C2212 1UF 20% 25V CERM 1206

NOSTUFF C2207 1UF 20% 10V CERM 603 | R2203 2.21K 0.1% 1/16W MF-LF 603 | R2205 10K 0.1% 1/16W MF-LF 603

C2208 1800UF 20% 6.3V FLEX TH-KZJ | C2209 1800UF 20% 6.3V FLEX TH-KZJ

U2200_FEEDBACK

CHECK FETS

PPVCORE_NB
VOLTAGE=1.5V
MIN_NECK_WIDTH=0.25MM
MIN_LINE_WIDTH=0.6MM
MAKE_BASE=TRUE

=PPVCORE_NB

OMIT
U3
U3LITE
V1.0-300MM
PBGA
(SYM 6 OF 7)

W14 W17 V12 V15 U10 U13 U18 T11 T16 R14 R17 P12 P15 N13 N18 M11 M16 L14 L17 K12 K15

VDD

AG7 AG13 AG16 AG22 AE4 AE10 AE19 AE25 AC7 AC13 AC16 AC22 AB2 AB6 AB23 AB27 AA10 AA19 Y12 Y15 Y20 W4 W8 W13 W18 W21 W25 V11 V16 V19 U9 U14 U17 T2 T6 T12 T15 T20 T23 T27 R10 R13

GND

R18 P11 P16 P19 N4 N8 N9 N14 N17 N23 N27 M12 M15 M20 L10 L13 L18 K2 K6 K11 K16 K21 K25 J9 J14 H10 H19 G4 G23 G27 F13 F16 F22 D2 D7 D10 D19 D25 B4 B13 B16 B22

1.5V RUN FET

IS D2250 NEEDED?

PPVCORE_GPU | PP1V5_RUN

NOSTUFF D2250 10BQ040PBF SMB

DEVELOPMENT R2261 0 5% 1/10W MF-LF 402

PP1V5_RUN_FOR_LED

DEVELOPMENT U1001 LM339A SOI

1V1_REF

PP3V3_RUN

DEVELOPMENT R2260 330 5% 1/16W MF-LF 402

LED_PP1V5_RUN_P

DEVELOPMENT LED2200 GREEN 2.0X1.25A

LED_PP1V5_RUN_N

PLACE LED2200 NEAR VREG

=PPVCORE_NB

Q2250 IRF7413 SO-8

RDSON=0.012 OHM @ VGS=3.5 V

PP5V_PWRON

R2250 100K 5% 1/16W MF-LF 402 — Q5006G

NOSTUFF C2250 0.1UF 20% 10V CERM 402

Q2251 2N7002 SOT23-LF

SYS_SLEEP

U3LITE CORE POWER

SYNC_MASTER=N/A | SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 22 OF 102	

Page Notes

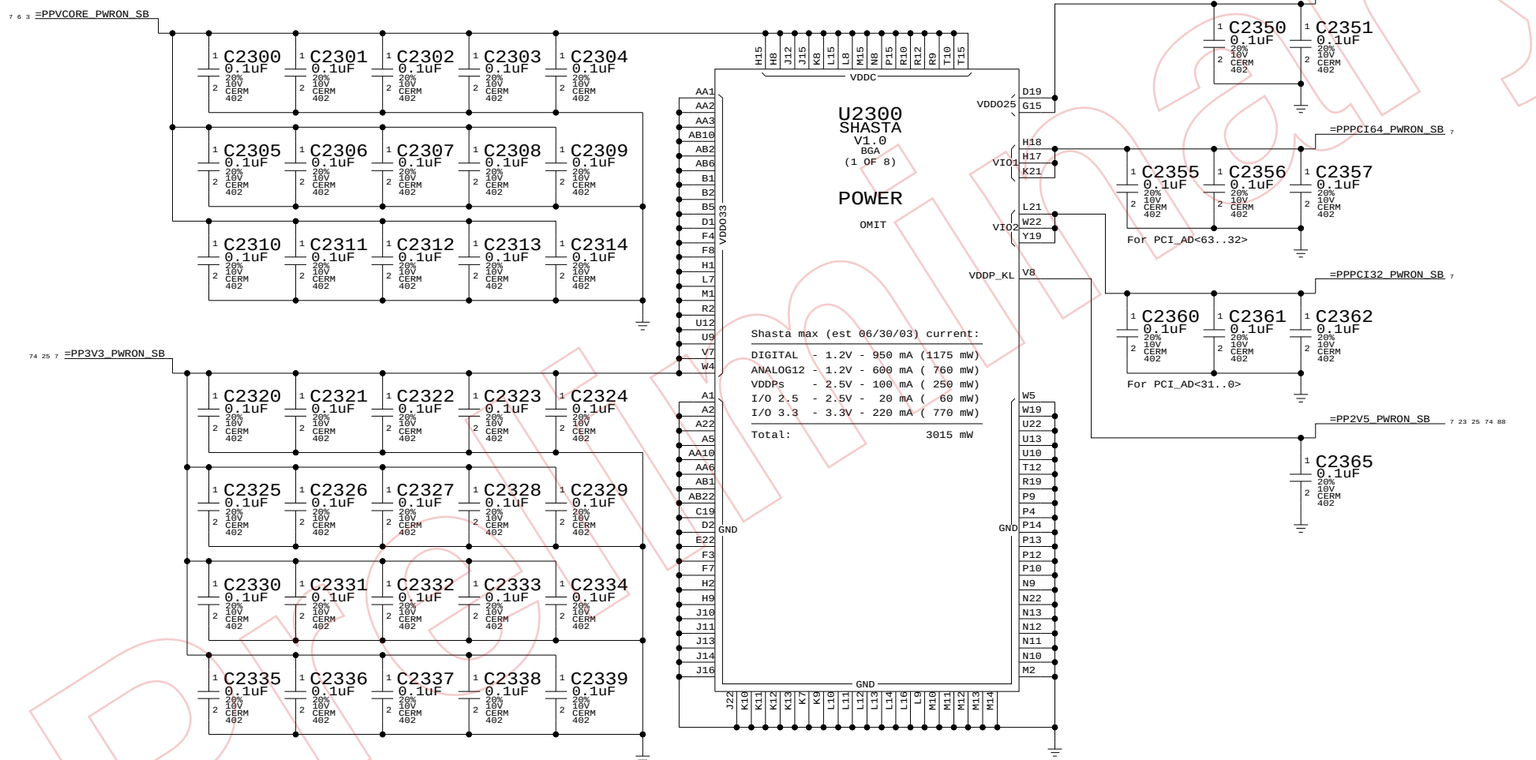
Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



Shasta Core Power

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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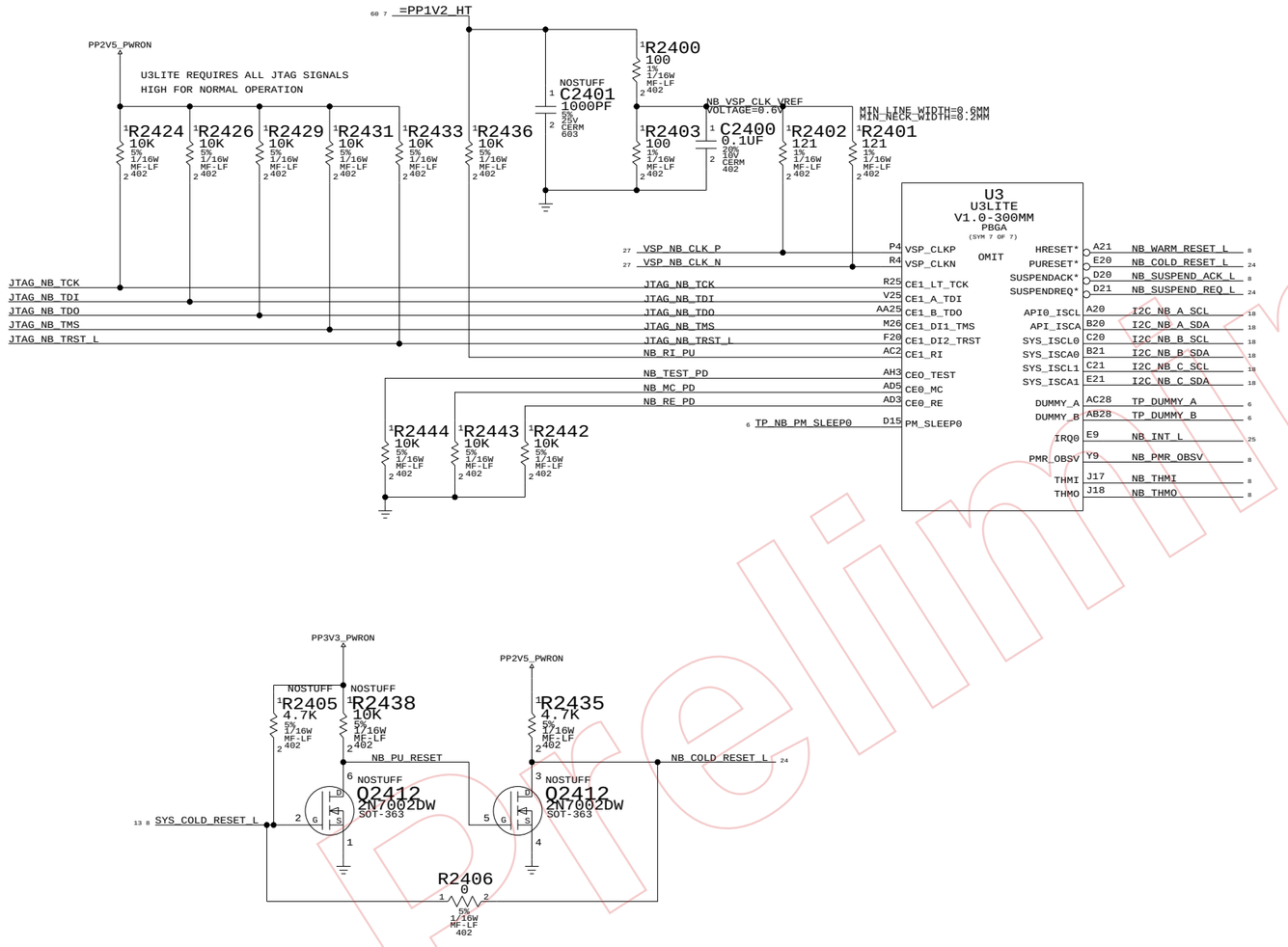

U3LITE MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI	25 95
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO	25 95
I2S0_TO_DEV	AUDIO		I2S0_MCLK	25 102
I2S0_BIDIR			I2S0_BITCLK	25 102
I2S0_BIDIR			I2S0_SYNC	25 95
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI	6 25 94
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO	6 25 94
I2S1_TO_DEV	P25MM		I2S1_MCLK	6 25 94
I2S1_BIDIR			I2S1_BITCLK	6 25 94
I2S1_BIDIR			I2S1_SYNC	6 25 94
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI	25 102
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO	25 102
I2S2_TO_DEV	P25MM		I2S2_MCLK	25 102
I2S2_BIDIR			I2S2_BITCLK	25 102
I2S2_BIDIR			I2S2_SYNC	25 102
SB_CLK18M_XTAL	CLOCKS		SB_CLK18M_XTALI	25
	CLOCKS		SB_CLK18M_XTALO	25
	CLOCKS		SB_CLK18M_XTALO_R	25
SB_CLK25M_ATA	CLOCKS		SB_CLK25M_ATA	25 27

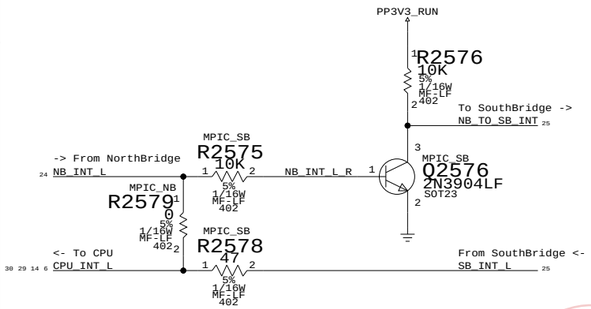
Page Notes

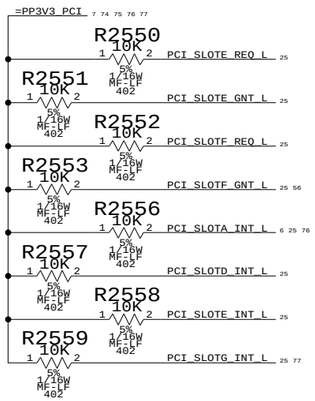
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

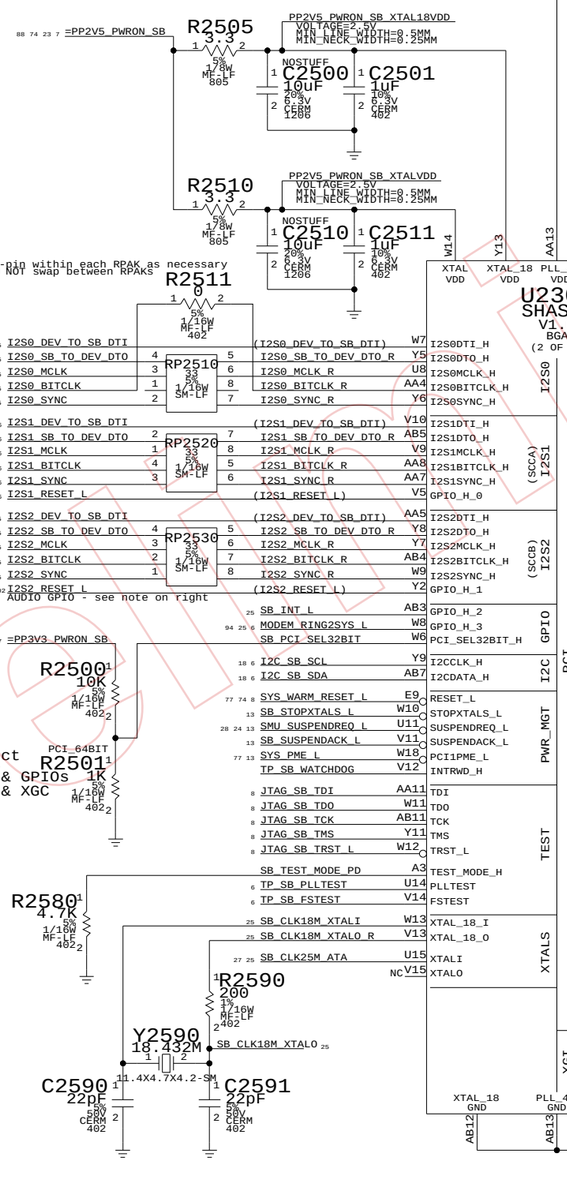
Signal aliases required by this page:
(NONE)

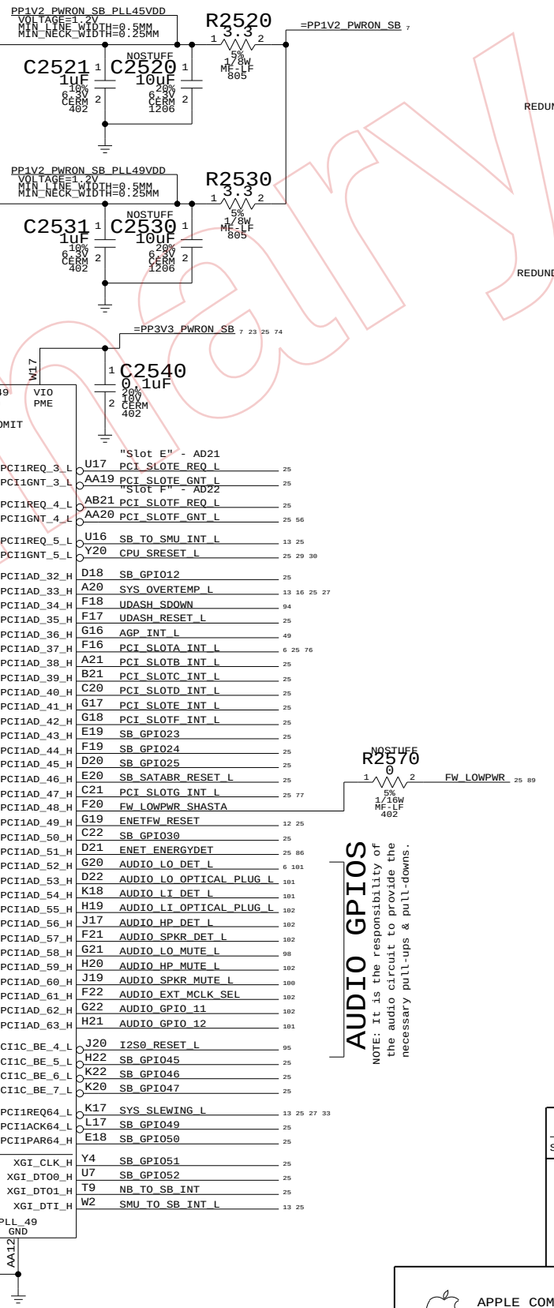
BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

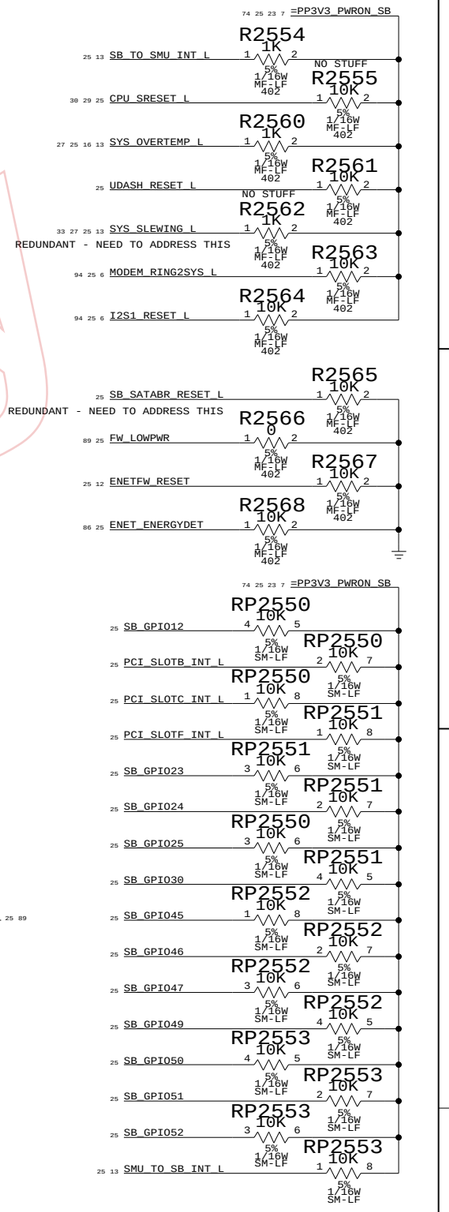
NorthBridge / SouthBridge MPIC Routing











Shasta Serial / Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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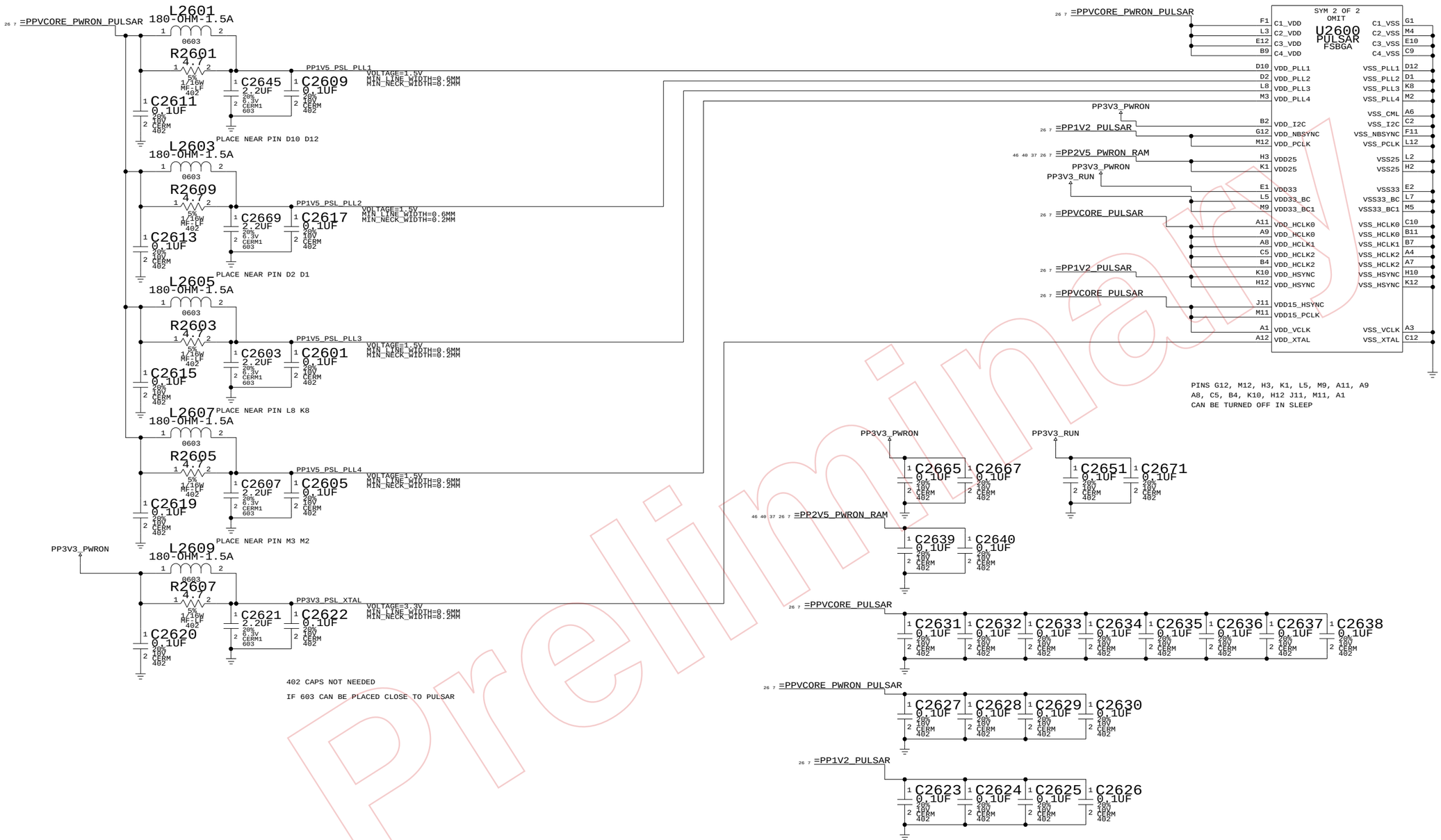

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

PULSAR POWER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	CLOCKS	EI_CPU_CLK	186
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	CLOCKS	EI_CPU_CLK	187
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	CLOCKS	EI_CPU1_CLK	116
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	CLOCKS	EI_CPU1_CLK	117
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	CLOCKS	EI_NB_CLK	190
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	CLOCKS	EI_NB_CLK	191
EI_CPU_SYNC	EI_SYNC	CLOCKS	CLOCKS		188
EI_NB_SYNC		CLOCKS	CLOCKS		189
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	CLOCKS		118
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	CLOCKS	VSP_NB_CLK	194
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	CLOCKS	VSP_NB_CLK	195
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	CLOCKS		186
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	CLOCKS		191
HT_CLK66M_NB	HT_NB_CLK	CLOCKS	CLOCKS		192
HT_CLK66M_SB	HT_SB_CLK	CLOCKS	CLOCKS		193
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	CLOCKS		180
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	CLOCKS		181
PLS_EXTCLK	PLS_XTAL	CLOCKS	CLOCKS		110
CPU_HTBEN		CLOCKS	CLOCKS		126

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

			NET SPACING TYPE
GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS
SLEWING*	K9	SLEWING_L_R	CLOCKS
ERROR*	M8	CLOCK_ERROR_L	
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS

SCLK	C1	I2C_CLOCK_SCL
SDATA	B1	I2C_CLOCK_SDA
RESET*	D3	PLS_RESET_L
XIN	C11	PLS_X_IN
XOUT	B12	PLS_X_OUT
ADDRSEL	E3	PLS_X_ADDRSEL
TEST1	K3	TP_PLS_TEST1
TEST2	E11	TP_PLS_TEST2
TEST3	D11	TP_PLS_TEST3
SCAN_MODE	M1	PLS_SCAN_MODE
REF15	G11	PLS_REF15
REF25	J2	PLS_REF25
REF33	M6	PLS_REF33
REF_CML	A5	TP_PLS_REF_CML
PRES_CML	B6	PLS_PRES_CML
FORCESPO*	F2	PLS_FORCE_P0_L_R
PD	C3	

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

PP3V3_PWRON
SYS_OVERTEMP_L
=PULSAR_POWER_DOWN
CLOCK_RESET_L
PLS_EXTCLK
PLS_INTERM
PLS_X_IN_B
PLS_X_OUT_B

R2722 1K 5% 1/16W MF-LF 402
R2748 0 5% 1/16W MF-LF 402 NOSTUFF
R2738 1K 5% 402 NOSTUFF
R2704 0 5% 402
R2706 249 1% 402
R2744 681 1% 402
R2740 1K 1% 402
R2746 1K 1% 402
R2742 806 1% 402
R2750 47 5% 402
R2724 1K 5% 402 NOSTUFF
R2752 0 5% 1/16W MF-LF 402 NO STUFF
R2754 0 5% 1/16W MF-LF 402
R2758 330K 5% 1/16W MF-LF 402
R2756 0 5% 1/16W MF-LF 402
R2762 24 5% 1/16W MF-LF 402 NOSTUFF
R2764 24 5% 1/16W MF-LF 402 NOSTUFF

J2700 U.FL-R_SMT F-ST-SM
Y2701 25.0000M CRITICAL 8X4.5MM-SM
C2707 33PF 5% 50V CERM 402
C2705 33PF 5% 50V CERM 402

R2701 0 5% 3.3V 33MHZ PCI_CLK_GP0
R2761 0 5% 402 3.3V 33MHZ PCI_CLK_GP1
C2708 0.001UF 10% 50V1 2CERM 402 VSP_NB_CLK_P
C2710 0.001UF 10% 50V 1 2CERM 402 VSP_NB_CLK_N
C2713 0.001UF 10% 50V 1 2CERM 402
C2715 0.001UF 10% 50V1 2CERM 402 EI_CPU_CLK_P EI_CPU_CLK_N
C2700 0.001UF 10% 50V1 2CERM 402 EI_NB_CLK_P
C2702 0.001UF 10% 50V1 2CERM 402 EI_NB_CLK_N

R2775 0 5% 402 NOSTUFF	2.5V	66MHZ	TP_PLS_CLK_66M_0
R2776 0 5% 402	2.5V	66MHZ	TP_PLS_CLK_66M_1
R2703 20 5% 402	2.5V	66MHZ	HT_CLK66M_NB
R2709 20 5% 402	2.5V	66MHZ	RAM_CLK66M_NB
R2705 0 5% 402	3.3V	66MHZ	PCI_CLK66M_SB_INT
R2711 0 5% 402	3.3V	33MHZ	PCI_CLK_P1
R2707 0 5% 402	3.3V	66MHZ	AGP_CLK66M_GPU
R2702 0 5% 402	3.3V	33MHZ	PCI_CLK_P3
R2779 0 5% 402			PCI_CLK_P4
R2715 0 5% 402	1.2V	33MHZ	CPU_HTBEN
R2768 0 5% 402 NOSTUFF	1.2V		EI_NB_SYNC
R2772 0 5% 402	1.2V		EI_CPU_SYNC
R2770 20 5% 402 NOSTUFF	2.5V	25MHZ	SB_CLK25M_ATA
R2700 22 5% 402	2.5V	25MHZ	TP_SATA_CLK25M
R2720 0 5% 402	SYS_SLEWING_L		
R2717 0 5% 402	1.2V	66MHZ	HT_CLK66M_SB
R2719 0 5% 402	1.5V	66MHZ	AGP_CLK66M_NB

PULSAR CLOCKS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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=PP1V2_EI_NB 7 14 18 28

C2800 C2801 C2802 C2803 C2804 C2805 C2806 C2807 C2808 C2809 C2810 C2811 C2812 C2813 C2814 C2815 C2816 C2817
0.1UF 20% 10V CERM 402

60 48 37 7 =PP1V5_PWRON_NB_AVDD

R2800 2.2 5% 1/10W ME-LF 603

PP1V5_PWRON_EI_NB_AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

C2818 1UF 10% 6.3V CERM 402
C2819 0.1UF 20% 10V CERM 402

=PP1V2_EI_NB 7 14 18 28

F21 K4 K8 J13 H13 H16 G2 F7 F10 D4 D13 D16 B7 B10 B19

API APCLK_AVDD VDD_API

U3
U3LITE
V1.0-300MM
PBGA
(SYM 1 OF 7)
OMIT

APPLE PI INTERFACE

29 28 14 6 EI_NB_TO_CPU_CLK_P	F15	APIO_BCLKIP	APIO_BCLKOP	D6	EI_CPU_TO_NB_CLK_P 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_CLK_N	E15	APIO_BCLKIN	APIO_BCLKON	E6	EI_CPU_TO_NB_CLK_N 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<0>	F11	APIO_ADI0	APIO_ADO0	J2	EI_CPU_TO_NB_AD<0> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<1>	F12	APIO_ADI1	APIO_ADO1	H1	EI_CPU_TO_NB_AD<1> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<2>	G11	APIO_ADI2	APIO_ADO2	J1	EI_CPU_TO_NB_AD<2> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<3>	H11	APIO_ADI3	APIO_ADO3	K1	EI_CPU_TO_NB_AD<3> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<4>	G12	APIO_ADI4	APIO_ADO4	E1	EI_CPU_TO_NB_AD<4> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<5>	H12	APIO_ADI5	APIO_ADO5	F2	EI_CPU_TO_NB_AD<5> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<6>	H14	APIO_ADI6	APIO_ADO6	J4	EI_CPU_TO_NB_AD<6> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<7>	G14	APIO_ADI7	APIO_ADO7	H4	EI_CPU_TO_NB_AD<7> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<8>	D9	APIO_ADI8	APIO_ADO8	G1	EI_CPU_TO_NB_AD<8> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<9>	C9	APIO_ADI9	APIO_ADO9	H2	EI_CPU_TO_NB_AD<9> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<10>	D11	APIO_ADI10	APIO_ADO10	F1	EI_CPU_TO_NB_AD<10> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<11>	E11	APIO_ADI11	APIO_ADO11	H5	EI_CPU_TO_NB_AD<11> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<12>	A10	APIO_ADI12	APIO_ADO12	H3	EI_CPU_TO_NB_AD<12> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<13>	A9	APIO_ADI13	APIO_ADO13	J3	EI_CPU_TO_NB_AD<13> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<14>	A8	APIO_ADI14	APIO_ADO14	J5	EI_CPU_TO_NB_AD<14> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<15>	B9	APIO_ADI15	APIO_ADO15	J6	EI_CPU_TO_NB_AD<15> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<16>	C11	APIO_ADI16	APIO_ADO16	E3	EI_CPU_TO_NB_AD<16> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<17>	B11	APIO_ADI17	APIO_ADO17	F4	EI_CPU_TO_NB_AD<17> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<18>	A11	APIO_ADI18	APIO_ADO18	E2	EI_CPU_TO_NB_AD<18> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<19>	A12	APIO_ADI19	APIO_ADO19	F5	EI_CPU_TO_NB_AD<19> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<20>	B12	APIO_ADI20	APIO_ADO20	H6	EI_CPU_TO_NB_AD<20> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<21>	C12	APIO_ADI21	APIO_ADO21	J7	EI_CPU_TO_NB_AD<21> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<22>	D12	APIO_ADI22	APIO_ADO22	F3	EI_CPU_TO_NB_AD<22> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<23>	E12	APIO_ADI23	APIO_ADO23	J8	EI_CPU_TO_NB_AD<23> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<24>	A13	APIO_ADI24	APIO_ADO24	F6	EI_CPU_TO_NB_AD<24> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<25>	A14	APIO_ADI25	APIO_ADO25	E5	EI_CPU_TO_NB_AD<25> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<26>	B14	APIO_ADI26	APIO_ADO26	D5	EI_CPU_TO_NB_AD<26> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<27>	C14	APIO_ADI27	APIO_ADO27	E4	EI_CPU_TO_NB_AD<27> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<28>	A16	APIO_ADI28	APIO_ADO28	D8	EI_CPU_TO_NB_AD<28> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<29>	A15	APIO_ADI29	APIO_ADO29	A5	EI_CPU_TO_NB_AD<29> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<30>	B15	APIO_ADI30	APIO_ADO30	C2	EI_CPU_TO_NB_AD<30> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<31>	C15	APIO_ADI31	APIO_ADO31	C3	EI_CPU_TO_NB_AD<31> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<32>	H15	APIO_ADI32	APIO_ADO32	C5	EI_CPU_TO_NB_AD<32> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<33>	G15	APIO_ADI33	APIO_ADO33	C6	EI_CPU_TO_NB_AD<33> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<34>	F17	APIO_ADI34	APIO_ADO34	B2	EI_CPU_TO_NB_AD<34> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<35>	G17	APIO_ADI35	APIO_ADO35	D1	EI_CPU_TO_NB_AD<35> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<36>	G18	APIO_ADI36	APIO_ADO36	B1	EI_CPU_TO_NB_AD<36> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<37>	H18	APIO_ADI37	APIO_ADO37	C1	EI_CPU_TO_NB_AD<37> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<38>	F18	APIO_ADI38	APIO_ADO38	A6	EI_CPU_TO_NB_AD<38> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<39>	E18	APIO_ADI39	APIO_ADO39	C8	EI_CPU_TO_NB_AD<39> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<40>	A17	APIO_ADI40	APIO_ADO40	A2	EI_CPU_TO_NB_AD<40> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<41>	A18	APIO_ADI41	APIO_ADO41	B3	EI_CPU_TO_NB_AD<41> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<42>	B17	APIO_ADI42	APIO_ADO42	A7	EI_CPU_TO_NB_AD<42> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_AD<43>	C17	APIO_ADI43	APIO_ADO43	B8	EI_CPU_TO_NB_AD<43> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_SR_P<0>	D17	APIO_SRIP0	APIO_SROP0	A3	EI_CPU_TO_NB_SR_P<0> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_SR_N<0>	A19	APIO_SRIN0	APIO_SRON0	A4	EI_CPU_TO_NB_SR_N<0> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_SR_P<1>	E17	APIO_SRIP1	APIO_SROP1	B5	EI_CPU_TO_NB_SR_P<1> 6 14 28 29
29 28 14 6 EI_NB_TO_CPU_SR_N<1>	B18	APIO_SRIN1	APIO_SRON1	B6	EI_CPU_TO_NB_SR_N<1> 6 14 28 29
29 14 6 EI_QACK_L	D14	API_QACK0	API_QREQ0	E14	
	E8	APIO_APSYNC	API_APCLKP	D18	EI_NB_CLK_P
	H17	APIO_SE	API_APCLKN	C18	EI_NB_CLK_N
			API_CSTP	F14	CPU_CHKSTOP_L 29

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
29 28 14 6 EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK 2412
29 28 14 6 EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK 2413
29 28 14 6 EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK 2414
29 28 14 6 EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK 2415
29 28 14 6 EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CAD	EI_CPU_TO_NB_AD	2416
29 28 14 6 EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_CAD	EI_NB_TO_CPU_AD	2417
29 28 14 6 EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR0 2418
29 28 14 6 EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR0 2419
29 28 14 6 EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR1 2420
29 28 14 6 EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_SR	EI_SR	EI_CPU_TO_NB_SR1 2421
29 28 14 6 EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR0 2422
29 28 14 6 EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR0 2423
29 28 14 6 EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR1 2424
29 28 14 6 EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_SR	EI_SR	EI_NB_TO_CPU_SR1 2425

ZT2847 ZT2857 ZT2867 ZT2807 ZT2817 ZT2827 ZT2837
ZT2848 ZT2858 ZT2868 ZT2808 ZT2818 ZT2828 ZT2838
ZT2849 ZT2859 ZT2869 ZT2809 ZT2819 ZT2829 ZT2839
ZT2850 ZT2860 ZT2800 ZT2810 ZT2820 ZT2830 ZT2840
ZT2851 ZT2861 ZT2801 ZT2811 ZT2821 ZT2831 ZT2841
ZT2852 ZT2862 ZT2802 ZT2812 ZT2822 ZT2832 ZT2842
ZT2853 ZT2863 ZT2803 ZT2813 ZT2823 ZT2833 ZT2843
ZT2854 ZT2864 ZT2804 ZT2814 ZT2824 ZT2834 ZT2844
ZT2855 ZT2865 ZT2805 ZT2815 ZT2825 ZT2835 ZT2845
ZT2806 ZT2816 ZT2826 ZT2836
ZT2846 ZT2856 ZT2866
OMIT HOLE-VIA-20R10

=PP1V2_EI_NB 7 14 18 28

NOSTUFF R2802 100 1% 1/16W MF-LF 402

NOSTUFF C2821 0.001UF 10% 50V CERM 402

EI_APCLK_VREF VOLTAGE=0.6V

NOSTUFF R2801 100 1% 1/16W MF-LF 402

NOSTUFF C2820 0.1UF 20% 10V CERM 402

NOSTUFF R2803 121 1% 1/16W MF-LF 402

NOSTUFF R2804 121 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

PLACE R2805 AND R2806 NEAR U3LITE

NOSTUFF R2805 0 5% 1/16W MF-LF 402

27 EI_NB_SYNC — NB_APSYNC

R2806 10 5% 1/16W MF-LF 402

29 EI_SYNC_FROM_NB

30 29 14 6 EI_SE

API_APCLK_AVSS

QREQ_L HACK

28 7 =PP3V3_PWRON_EI

C2850 0.1UF 20% 10V CERM 402

CRITICAL U2850 74LVC1G66DBVG4 SOT23-5 TI

VCC GND

30 29 14 6 EI_QREQ_L

25 24 13 SMU_SUSPENDREQ_L

EI_NB_QREQ_L

NOSTUFF R2850 0 5% 1/16W MF-LF 402

R2851 10K 5% 1/16W MF-LF 402

QREQ TO SMU

28 7 =PP3V3_PWRON_EI

NOSTUFF R2898 10K 5% 1/16W MF-LF 402

SMU_QREQ 13

NOSTUFF R2899 180 5% 1/16W MF-LF 402

EI_NB_QREQ_L_R

NOSTUFF Q2899 2N3904LF SOT23

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U2850	PERICOM ANALOG SWITCH CRITICAL

PLACE QREQ CIRCUITS BETWEEN CPU AND U3LITE

EI_NB_CLK_P — 27
EI_NB_CLK_N — 27

U3LITE APPLE PI

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 28 OF 102	

PLACE AT PROCESSOR PINS.

PLACE NEAR PROCESSOR.

27 EI_CPU_CLK_P — NOSTUFF R2903 46.4 1% 1/10W MF-LF 402 — NOSTUFF C2901 0.22UF 6.3V X5R 402 — SYSCLK_TERM VOLTAGE=0.6V — NOSTUFF R2909 100 1% 1/10W MF-LF 402 — 31 30 29 18 14 7 =PP1V2_EI_CPU

27 EI_CPU_CLK_N — NOSTUFF R2901 46.4 1% 1/10W MF-LF 402 — NOSTUFF R2907 100 1% 1/10W MF-LF 402

SYSCLK* SYSCLK

OMIT ONTOCAD

U2900 CBGA (1 OF 3) NEO-10S-REV2 1.8GHZ-76C

EI_CLKI	E24	EI_CLK	D
EI_CLKI*	D23	EI_CLK*	E
EI_AD0	H23	EI_AD<0>	B3
EI_AD1	J23	EI_AD<1>	B2
EI_AD2	H22	EI_AD<2>	K3
EI_AD3	J22	EI_AD<3>	L1
EI_AD4	C13	EI_AD<4>	K5
EI_AD5	A13	EI_AD<5>	K4
EI_AD6	K23	EI_AD<6>	K2
EI_AD7	H24	EI_AD<7>	K1
EI_AD8	J24	EI_AD<8>	B1
EI_AD9	G26	EI_AD<9>	G4
EI_AD10	F23	EI_AD<10>	F2
EI_AD11	G23	EI_AD<11>	F4
EI_AD12	D22	EI_AD<12>	F3
EI_AD13	E24	EI_AD<13>	E3
EI_AD14	E18	EI_AD<14>	E2
EI_AD15	B15	EI_AD<15>	E1
EI_AD16	A14	EI_AD<16>	D11
EI_AD17	C15	EI_AD<17>	E12
EI_AD18	B15	EI_AD<18>	A11
EI_AD19	A16	EI_AD<19>	B10
EI_AD20	E22	EI_AD<20>	C11
EI_AD21	E26	EI_AD<21>	G1
EI_AD22	F23	EI_AD<22>	E5
EI_AD23	B23	EI_AD<23>	D3
EI_AD24	B24	EI_AD<24>	A5
EI_AD25	F21	EI_AD<25>	A2
EI_AD26	B17	EI_AD<26>	G3
EI_AD27	B18	EI_AD<27>	D8
EI_AD28	C14	EI_AD<28>	C12
EI_AD29	C17	EI_AD<29>	A12
EI_AD30	B16	EI_AD<30>	B5
EI_AD31	B21	EI_AD<31>	B4
EI_AD32	B20	EI_AD<32>	C6
EI_AD33	A22	EI_AD<33>	C7
EI_AD34	C19	EI_AD<34>	A7
EI_AD35	C18	EI_AD<35>	C8
EI_AD36	A21	EI_AD<36>	C9
EI_AD37	A23	EI_AD<37>	A4
EI_AD38	A20	EI_AD<38>	A3
EI_AD39	A18	EI_AD<39>	C3
EI_AD40	A15	EI_AD<40>	A10
EI_AD41	A17	EI_AD<41>	C10
EI_AD42	C16	EI_AD<42>	A8
EI_AD43	A19	EI_AD<43>	A6
EI_SR0	L24	EI_SR0	L3
EI_SR0*	K24	EI_SR0*	L2
EI_SR1	L23	EI_SR1	K1
EI_SR1*	L22	EI_SR1*	F1
EI_QACK_L	V21	QACK*	AB12
CHKSTOP_L	R20	CHKSTOP*	AB19
CPU_HTBEN	AD17	TBEN	
TP_PSYNCOUT	AD14	APSYNCOUT	AA10
CPU_HRESET_L	V20	HRESET*	
CPU_SRESET_L	AB1	SRESET*	
PROC_THERM_INT_L	V22	THERM_INT*	
PROCID0	L19	PROCID0	
PROCID1	K19	PROCID1	
PROCID2	K18	PROCID2	
EI_SE	N21	TRIGGER_IN	
TP_PROC_TRIGGER_OUT	N19	TRIGGER_OUT	
AFN	AA12	AFN	
AVPRESET_L	W23	AVPRESET*	
BIMODE_L	AC19	BIMODE*	
C2UNDGLOBAL	AC15	C1UNDGLOBAL	
C2UNDGLOBAL	AC16	C2UNDGLOBAL	
DI2_L	U23	DI2*	
LSSDMODE	AB5	LSSDMODE	
LSSDSCANENABLE	J18	LSSDSCANENABLE	
LSSDSTOPC2ENABLE	AD3	LSSDSTOPC2ENABLE	
LSSDSTOPC2STARENABLE	AD2	LSSDSTOPC2STARENABLE	
LSSDSTOPENABLE	AD11	LSSDSTOPENABLE	
MCP_L	AD13	MCP*	
TP_PSRO1	V23	PSRO1	
TP_PSRO2	V5	PSRO2	
PULSESEL0	AC3	PULSESEL0	
PULSESEL1	AB11	PULSESEL1	
PULSESEL2	AC18	PULSESEL2	
RAMSTOPENABLE	AB6	RAMSTOPENABLE	
RI_L	AD1	RI*	
SYNCENABLE	AB23	SYNCENABLE*	

EI_CLKO	D3	EI_CLK	D
EI_CLKO*	E3	EI_CLK*	E
EI_AD0	B3	EI_AD<0>	B3
EI_AD1	B2	EI_AD<1>	B2
EI_AD2	K3	EI_AD<2>	K3
EI_AD3	L1	EI_AD<3>	L1
EI_AD4	K5	EI_AD<4>	K5
EI_AD5	K4	EI_AD<5>	K4
EI_AD6	K2	EI_AD<6>	K2
EI_AD7	K1	EI_AD<7>	K1
EI_AD8	B1	EI_AD<8>	B1
EI_AD9	G4	EI_AD<9>	G4
EI_AD10	F2	EI_AD<10>	F2
EI_AD11	F4	EI_AD<11>	F4
EI_AD12	F3	EI_AD<12>	F3
EI_AD13	E3	EI_AD<13>	E3
EI_AD14	E2	EI_AD<14>	E2
EI_AD15	E1	EI_AD<15>	E1
EI_AD16	D11	EI_AD<16>	D11
EI_AD17	E12	EI_AD<17>	E12
EI_AD18	A11	EI_AD<18>	A11
EI_AD19	B10	EI_AD<19>	B10
EI_AD20	C11	EI_AD<20>	C11
EI_AD21	G1	EI_AD<21>	G1
EI_AD22	E5	EI_AD<22>	E5
EI_AD23	D3	EI_AD<23>	D3
EI_AD24	A5	EI_AD<24>	A5
EI_AD25	A2	EI_AD<25>	A2
EI_AD26	G3	EI_AD<26>	G3
EI_AD27	D8	EI_AD<27>	D8
EI_AD28	C12	EI_AD<28>	C12
EI_AD29	A12	EI_AD<29>	A12
EI_AD30	B5	EI_AD<30>	B5
EI_AD31	B4	EI_AD<31>	B4
EI_AD32	C6	EI_AD<32>	C6
EI_AD33	C7	EI_AD<33>	C7
EI_AD34	A7	EI_AD<34>	A7
EI_AD35	C8	EI_AD<35>	C8
EI_AD36	C9	EI_AD<36>	C9
EI_AD37	A4	EI_AD<37>	A4
EI_AD38	A3	EI_AD<38>	A3
EI_AD39	C3	EI_AD<39>	C3
EI_AD40	A10	EI_AD<40>	A10
EI_AD41	C10	EI_AD<41>	C10
EI_AD42	A8	EI_AD<42>	A8
EI_AD43	A6	EI_AD<43>	A6
EI_SR0	L3	EI_SR0	L3
EI_SR0*	L2	EI_SR0*	L2
EI_SR1	K1	EI_SR1	K1
EI_SR1*	F1	EI_SR1*	F1
QREQ*	AB12	EI_QREQ_L	6 14 28 30
INT*	AB19	CPU_INT_L	6 14 25 30
APSYNCIN	AA10	CPU_APSYNC	
IIC_SCL	AA20	I2C_CPU_A_SCL	18
IIC_SDA	Y21	I2C_CPU_A_SDA	18
I2CG0	N22	I2CG0	30
CKTERMDIS	AA14	CKTERMDIS_L	30
EI_DISABLE	F20	EI_DISABLE	30
BUSCFG0	AA19	BUSCFG0	30
BUSCFG1	AC19	BUSCFG1	30
BUSCFG2	AB18	BUSCFG2	30
ATTENTION	AD12	TP_ATTENTION	6
GPUL_DBG	AA22	GPUL_DBG	30
JTAGMODE	N4	JTAGMODE_SPARE2	30
TCK	AB21	JTAG_CPU_TCK	18 30
TDI	AB21	JTAG_CPU_TDI	18 30
TDO	AD13	JTAG_CPU_TDO	18 30
TMS	AD22	JTAG_CPU_TMS	18 30
TRST*	W20	JTAG_CPU_TRST_L	30
BYPASS	V24	CPU_BYPASS_L	30
PLLLOCK	T20	PLLLOCK	8
PLLMULT	AA8	PLLMULT	30
PLLRANGE0	AB7	PLLRANGE0	30
PLLRANGE1	AA9	PLLRANGE1	30
PLLTEST	W22	PLLTEST	30
PLLTESTOUT	T19	PLLTESTOUT	30
SPARE	AA13	CPU_SPARE	30

MATCH TO SYSCLK

NOSTUFF R2910 0 5% 1/16W MF-LF 402 — EI_CPU_SYNC 27

NOSTUFF R2911 0 5% 1/16W MF-LF 402 — EI_SYNC_FROM_NB 28

PROCESSOR IIC ADDRESS: 80,84

MORE PROCESSOR DECOUPLING ON PAGES 31 & 32

36 32 31 7 =PPVCORE_CPU

C2953 C2947 C2945 C2939 C2937 C2928 C2924 C2920 C2914 C2912
C2954 C2948 C2946 C2940 C2938 C2929 C2925 C2921 C2915 C2913
C2955 C2951 C2949 C2943 C2941 C2930 C2926 C2922 C2918 C2916
C2956 C2952 C2950 C2944 C2942 C2931 C2927 C2923 C2919 C2917
C2900 C2960 C2959 C2958 C2957 C2936 C2935 C2934 C2933 C2932
C2911 C2910 C2909 C2908 C2907 C2906 C2905 C2904 C2903 C2902

1UF 10% 6.3V X5R CERM 402

NOSTUFF R2905 49.9 1% 1/16W MF-LF 402 — 30 29 27 CPU_HTBEN

PLACE BY PROCESSOR PIN.

31 30 29 18 14 7 =PP1V2_EI_CPU — R2906 1K 5% 1/16W MF-LF 402 — R2908 1K 5% 1/16W MF-LF 402

R2902 0 5% 1/16W MF-LF 402 — CHKSTOP_L 6 8 14 29

28 CPU_CHKSTOP_L

NOSTUFF R2904 0 5% 1/16W MF-LF 402 — MCP_L 6 14 29

PROCESSOR LOGIC I/O

NEO APPLE PI

SYNC_MASTER=N/A SYNC_DATE=N/A

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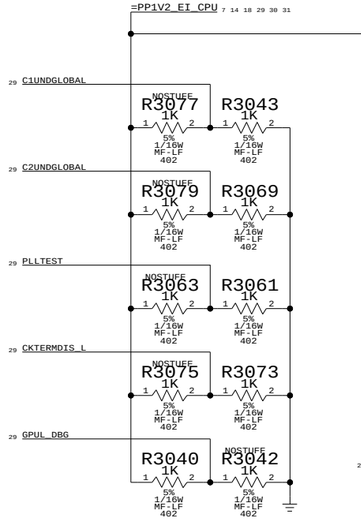
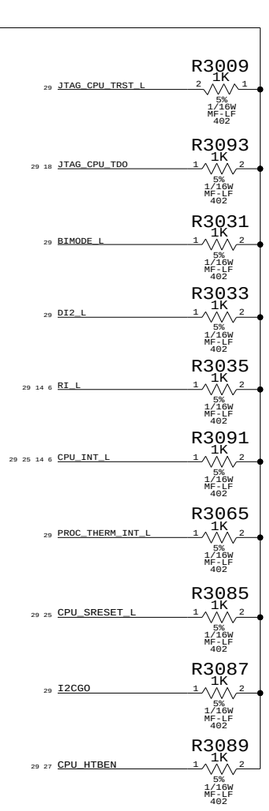
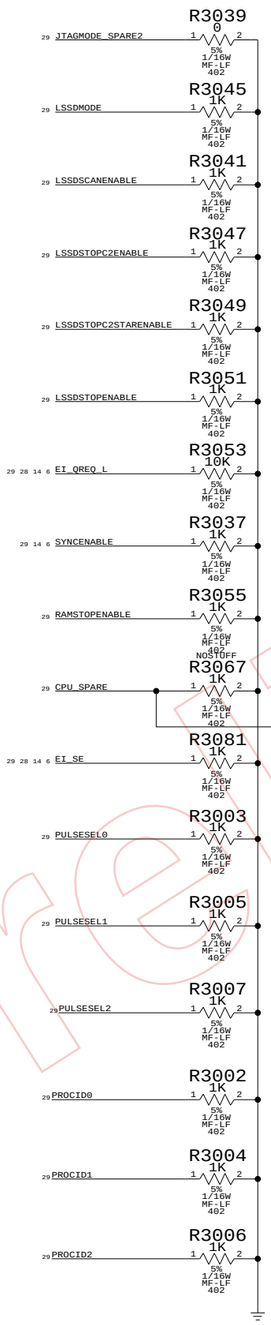
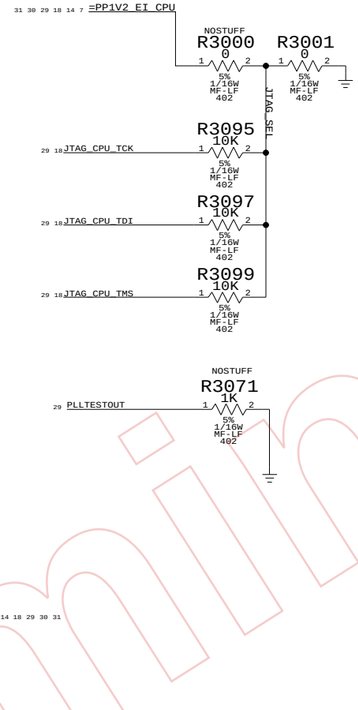
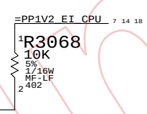
D	051-6772	11
SCALE: NONE	SHT 29 OF 102	

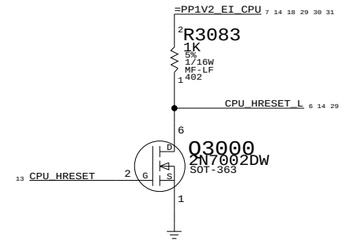


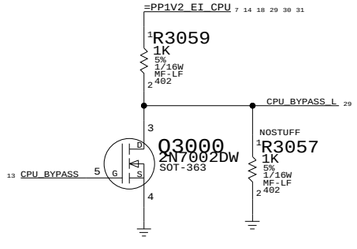












SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

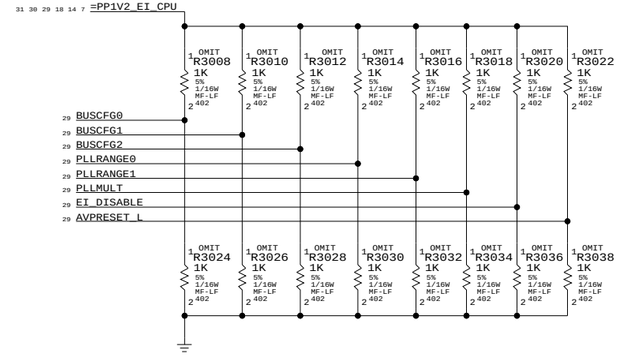
SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	>= 1.8 GHZ *
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	<= 1.6 GHZ *
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



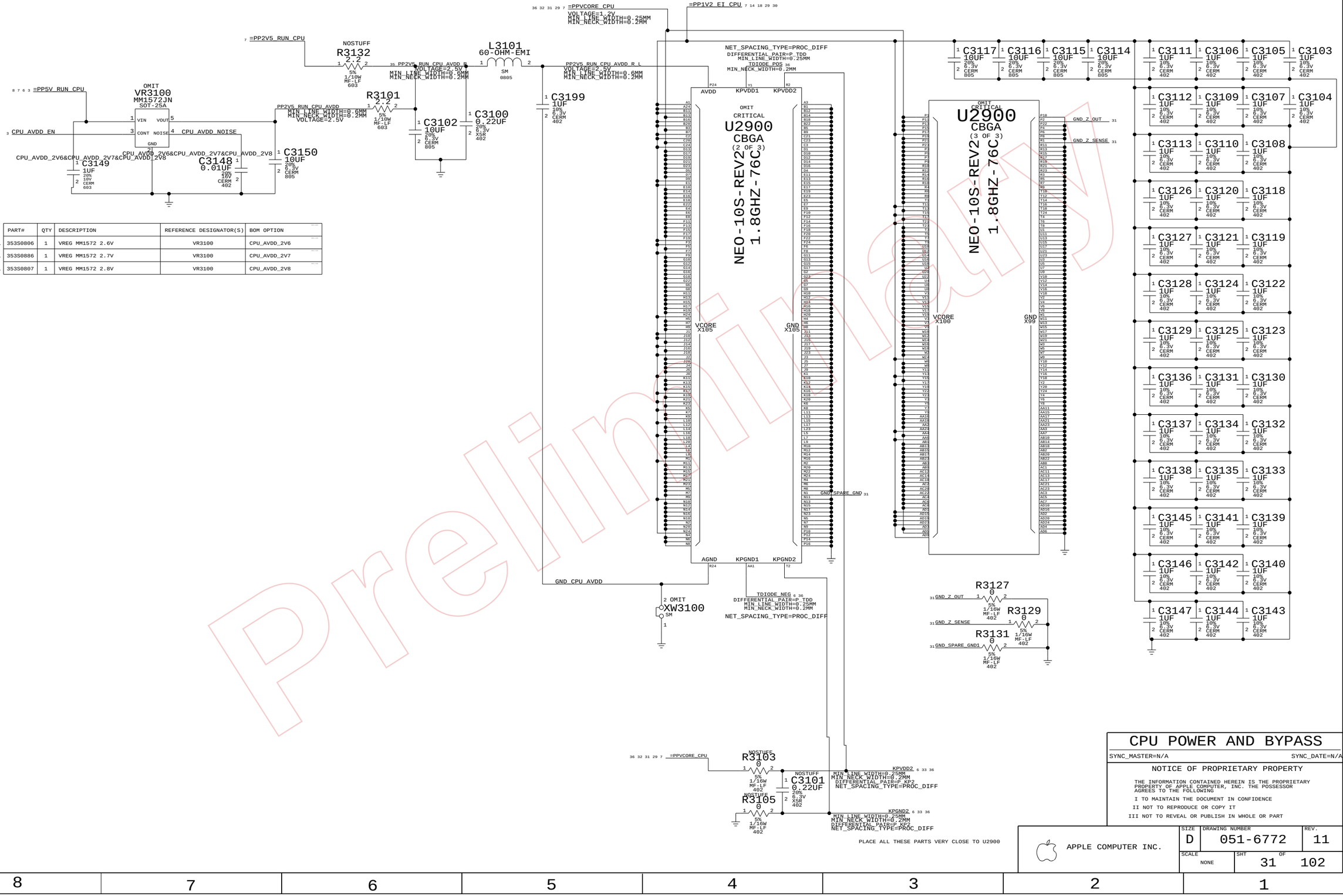
CPU STRAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11

SCALE	SHT	OF
NONE	30	102



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0886	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL	353S0807	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

CPU POWER AND BYPASS

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 31 OF 102	

36 31 29 7 =PPVCORE_CPU

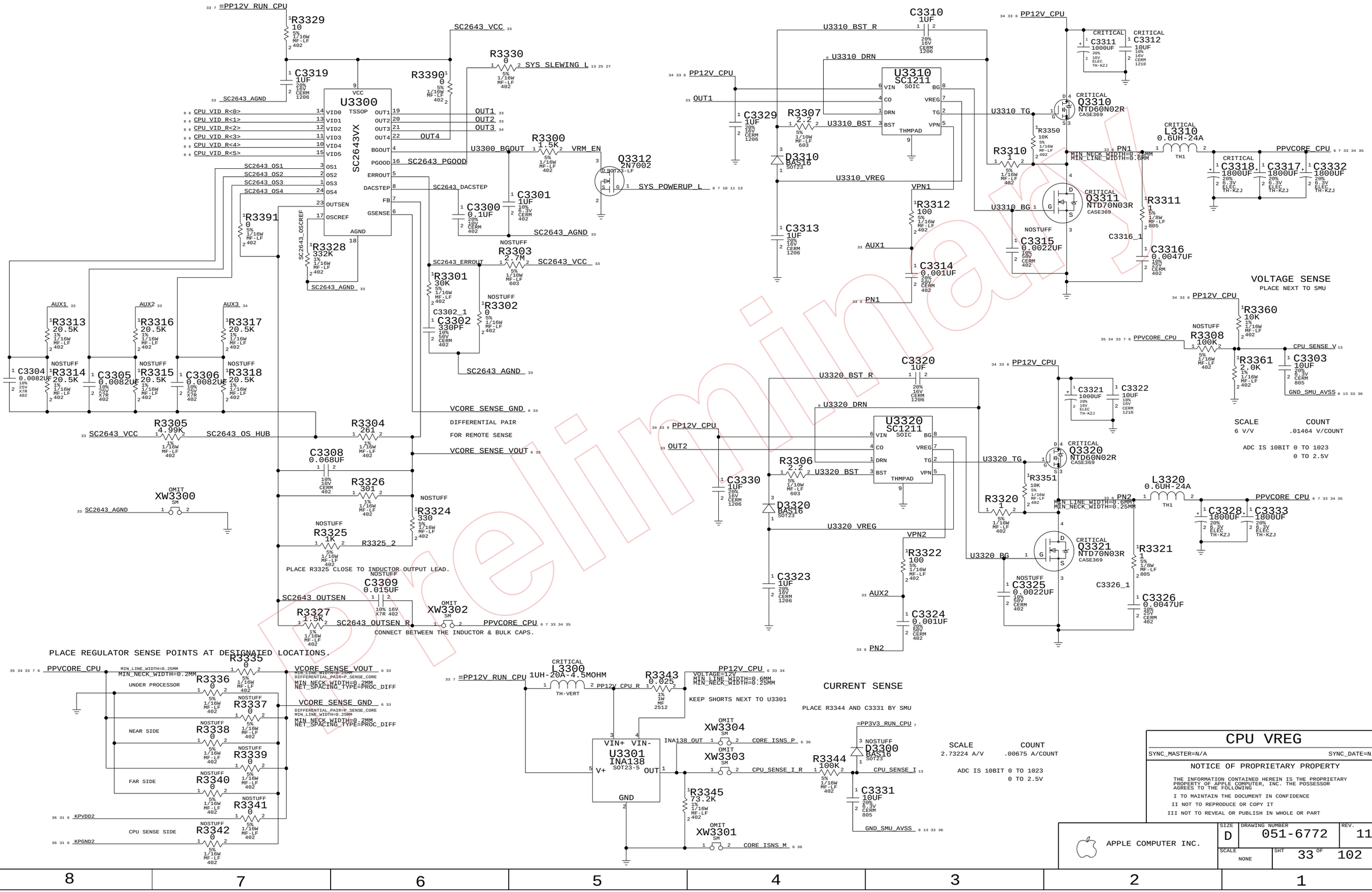
C3222 1UF 10% 6.3V CERM 402	C3221 1UF 10% 6.3V CERM 402	C3220 1UF 10% 6.3V CERM 402	C3219 1UF 10% 6.3V CERM 402	C3218 1UF 10% 6.3V CERM 402	C3217 1UF 10% 6.3V CERM 402	C3216 1UF 10% 6.3V CERM 402	C3215 1UF 10% 6.3V CERM 402	C3212 1UF 10% 6.3V CERM 402	C3200 1UF 10% 6.3V CERM 402
C3293 1UF 10% 6.3V CERM 402	C3268 1UF 10% 6.3V CERM 402	C3261 1UF 10% 6.3V CERM 402	C3259 1UF 10% 6.3V CERM 402	C3235 1UF 10% 6.3V CERM 402	C3232 1UF 10% 6.3V CERM 402	C3226 1UF 10% 6.3V CERM 402	C3224 1UF 10% 6.3V CERM 402	C3245 1UF 10% 6.3V CERM 402	C3223 1UF 10% 6.3V CERM 402
C3294 1UF 10% 6.3V CERM 402	C3269 1UF 10% 6.3V CERM 402	C3264 1UF 10% 6.3V CERM 402	C3260 1UF 10% 6.3V CERM 402	C3236 1UF 10% 6.3V CERM 402	C3233 1UF 10% 6.3V CERM 402	C3227 1UF 10% 6.3V CERM 402	C3225 1UF 10% 6.3V CERM 402	C3256 1UF 10% 6.3V CERM 402	C3234 1UF 10% 6.3V CERM 402
C3295 1UF 10% 6.3V CERM 402	C3271 1UF 10% 6.3V CERM 402	C3265 1UF 10% 6.3V CERM 402	C3262 1UF 10% 6.3V CERM 402	C3239 1UF 10% 6.3V CERM 402	C3237 1UF 10% 6.3V CERM 402	C3230 1UF 10% 6.3V CERM 402	C3228 1UF 10% 6.3V CERM 402	C3289 1UF 10% 6.3V CERM 402	C3267 1UF 10% 6.3V CERM 402
C3296 1UF 10% 6.3V CERM 402	C3270 1UF 10% 6.3V CERM 402	C3266 1UF 10% 6.3V CERM 402	C3263 1UF 10% 6.3V CERM 402	C3240 1UF 10% 6.3V CERM 402	C3238 1UF 10% 6.3V CERM 402	C3231 1UF 10% 6.3V CERM 402	C3229 1UF 10% 6.3V CERM 402	C3201 1UF 10% 6.3V CERM 402	C3278 1UF 10% 6.3V CERM 402
C3297 1UF 10% 6.3V CERM 402	C3282 1UF 10% 6.3V CERM 402	C3276 1UF 10% 6.3V CERM 402	C3272 1UF 10% 6.3V CERM 402	C3252 1UF 10% 6.3V CERM 402	C3250 1UF 10% 6.3V CERM 402	C3243 1UF 10% 6.3V CERM 402	C3241 1UF 10% 6.3V CERM 402	C3206 1UF 10% 6.3V CERM 402	C3204 1UF 10% 6.3V CERM 402
C3298 1UF 10% 6.3V CERM 402	C3281 1UF 10% 6.3V CERM 402	C3277 1UF 10% 6.3V CERM 402	C3273 1UF 10% 6.3V CERM 402	C3253 1UF 10% 6.3V CERM 402	C3251 1UF 10% 6.3V CERM 402	C3244 1UF 10% 6.3V CERM 402	C3242 1UF 10% 6.3V CERM 402	C3207 1UF 10% 6.3V CERM 402	C3205 1UF 10% 6.3V CERM 402
C3299 1UF 10% 6.3V CERM 402	C3284 1UF 10% 6.3V CERM 402	C3279 1UF 10% 6.3V CERM 402	C3274 1UF 10% 6.3V CERM 402	C3257 1UF 10% 6.3V CERM 402	C3254 1UF 10% 6.3V CERM 402	C3248 1UF 10% 6.3V CERM 402	C3246 1UF 10% 6.3V CERM 402	C3210 1UF 10% 6.3V CERM 402	C3208 1UF 10% 6.3V CERM 402
C3202 1UF 10% 6.3V CERM 402	C3283 1UF 10% 6.3V CERM 402	C3280 1UF 10% 6.3V CERM 402	C3275 1UF 10% 6.3V CERM 402	C3258 1UF 10% 6.3V CERM 402	C3255 1UF 10% 6.3V CERM 402	C3249 1UF 10% 6.3V CERM 402	C3247 1UF 10% 6.3V CERM 402	C3211 1UF 10% 6.3V CERM 402	C3209 1UF 10% 6.3V CERM 402
C3203 1UF 10% 6.3V CERM 402	C3292 1UF 10% 6.3V CERM 402	C3291 1UF 10% 6.3V CERM 402	C3290 1UF 10% 6.3V CERM 402	C3288 1UF 10% 6.3V CERM 402	C3287 1UF 10% 6.3V CERM 402	C3286 1UF 10% 6.3V CERM 402	C3285 1UF 10% 6.3V CERM 402	C3214 1UF 10% 6.3V CERM 402	C3213 1UF 10% 6.3V CERM 402

PROC DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE NONE	SHT 32 OF 102	


=PP12V_RUN_CPU
R3329 10
C3319 1UF
SC2643_AGND
SC2643_VCC
R3330 0
SYS_SLEWING_L
R3390 0
U3300
SC2643VX
VCC
TSSOP
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
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CPU_VID_R<4>
CPU_VID_R<5>
VID0
VID1
VID2
VID3
VID4
VID5
OUT1
OUT2
OUT3
OUT4
BGOUT
PGOOD
ERROUT
DACSTEP
FB
GSENSE
OUTSEN
OSCREF
AGND
SC2643_OS1
SC2643_OS2
SC2643_OS3
SC2643_OS4
SC2643_OSCREF
R3328 332K
R3391 0
R3300 1.5K
U3300_BGOUT
VRM_EN
SC2643_PGOOD
Q3312 2N7002
SYS_POWERUP_L
C3300 0.1UF
C3301 1UF
R3303 2.7M
SC2643_ERROUT
R3301 30K
R3302 0
C3302_1
C3302 330PF
AUX1
AUX2
AUX3
R3313 20.5K
R3316 20.5K
R3317 20.5K
R3314 20.5K
R3315 20.5K
R3318 20.5K
C3304 0.0082UF
C3305 0.0082UF
C3306 0.0082UF
R3305 4.99K
R3304 261
C3308 0.068UF
R3326 301
R3324 330
R3325 1K
R3325_2
PLACE R3325 CLOSE TO INDUCTOR OUTPUT LEAD.
C3309 0.015UF
SC2643_OUTSEN
R3327 1.5K
SC2643_OUTSEN_R
XW3300
XW3302
PPVCORE_CPU
CONNECT BETWEEN THE INDUCTOR & BULK CAPS.
VCORE_SENSE_GND
DIFFERENTIAL PAIR
FOR REMOTE SENSE
VCORE_SENSE_VOUT
C3310 1UF
U3310_BST_R
U3310_DRN
U3310
SC1211
SOIC
THMPAD
VIN
CO
DRN
BST
BG
VREG
TG
VPN
U3310_TG
U3310_BG
U3310_VREG
PP12V_CPU
OUT1
C3329 1UF
R3307 2.2
U3310_BST
D3310 BAS16
C3313 1UF
R3350 10K
R3310 1
Q3310 NTD60N02R
CASE369
Q3311 NTD70N03R
PN1
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
L3310 0.6UH-24A
C3311 1000UF
C3312 10UF
C3318 1800UF
C3317 1800UF
C3332 1800UF
PPVCORE_CPU
VPN1
R3312 100
AUX1
C3314 0.001UF
R3311 1
C3315 0.0022UF
C3316 0.0047UF
NOSTUFF
CRITICAL
VOLTAGE SENSE
PLACE NEXT TO SMU
R3360 10K
R3308 100K
R3361 2.0K
C3303 10UF
CPU_SENSE_V
GND_SMU_AVSS
SCALE
6 V/V
COUNT
.01464 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
C3320 1UF
U3320_BST_R
U3320_DRN
U3320
SC1211
U3320_TG
U3320_BG
U3320_VREG
OUT2
C3330 1UF
R3306 2.2
U3320_BST
D3320 BAS16
C3323 1UF
R3351 10K
R3320 1
Q3320 NTD60N02R
Q3321 NTD70N03R
PN2
L3320 0.6UH-24A
C3328 1800UF
C3333 1800UF
VPN2
R3322 100
AUX2
C3324 0.001UF
R3321 1
C3325 0.0022UF
C3326 0.0047UF
C3321 1000UF
C3322 10UF
PLACE REGULATOR SENSE POINTS AT DESIGNATED LOCATIONS.
PPVCORE_CPU
VCORE_SENSE_VOUT
VCORE_SENSE_GND
UNDER PROCESSOR
NEAR SIDE
FAR SIDE
CPU SENSE SIDE
R3335 0
R3336 0
R3337 0
R3338 0
R3339 0
R3340 0
R3341 0
R3342 0
KPVDD2
KPGND2
CURRENT SENSE
PLACE R3344 AND C3331 BY SMU
L3300 1UH-20A-4.5MOHM
R3343 0.025
PP12V_CPU_R
KEEP SHORTS NEXT TO U3301
U3301 INA138
VIN+ VIN-
V+ OUT GND
SOT23-5
INA138_OUT
CORE_ISNS_P
CORE_ISNS_M
CPU_SENSE_I_R
CPU_SENSE_I
XW3304
XW3303
XW3301
R3345 73.2K
R3344 100K
D3300 BAS16
C3331 10UF
=PP3V3_RUN_CPU
SCALE
2.73224 A/V
COUNT
.00675 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
CPU VREG
SYNC_MASTER=N/A
SYNC_DATE=N/A
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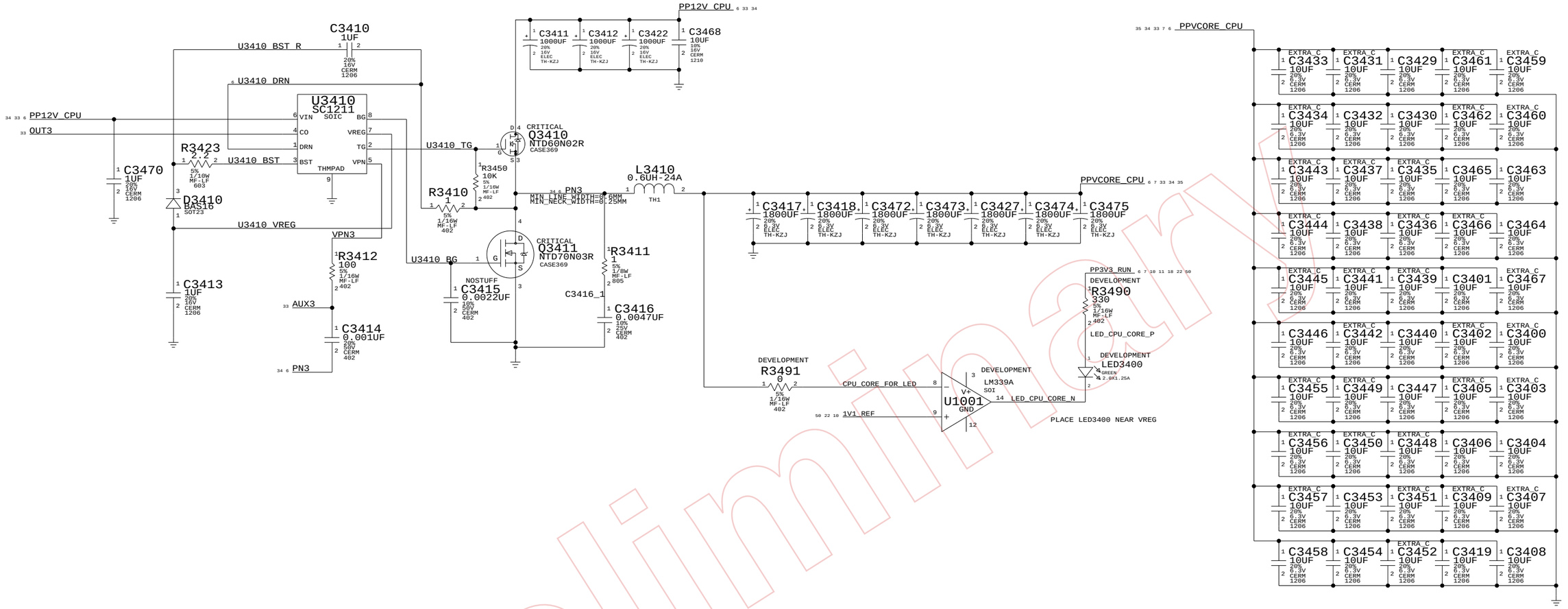
DRAWING NUMBER 051-6772
REV. 11
SCALE NONE
SHT 33 OF 102



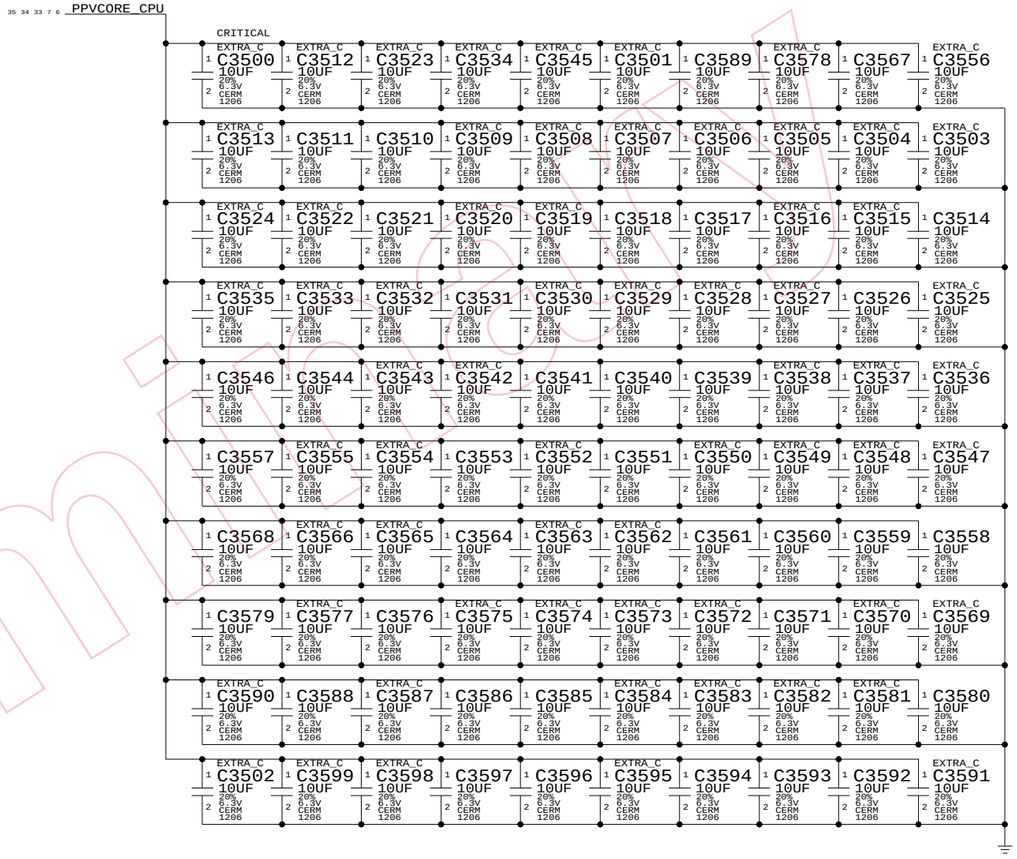
CPU VREG

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11

SCALE NONE SHT 34 OF 102

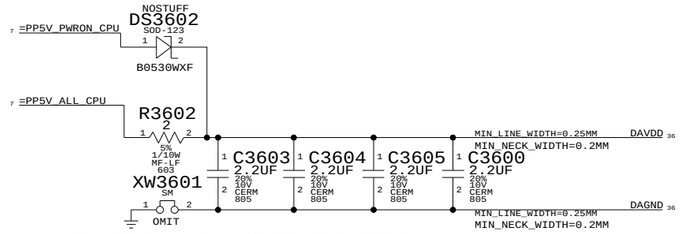


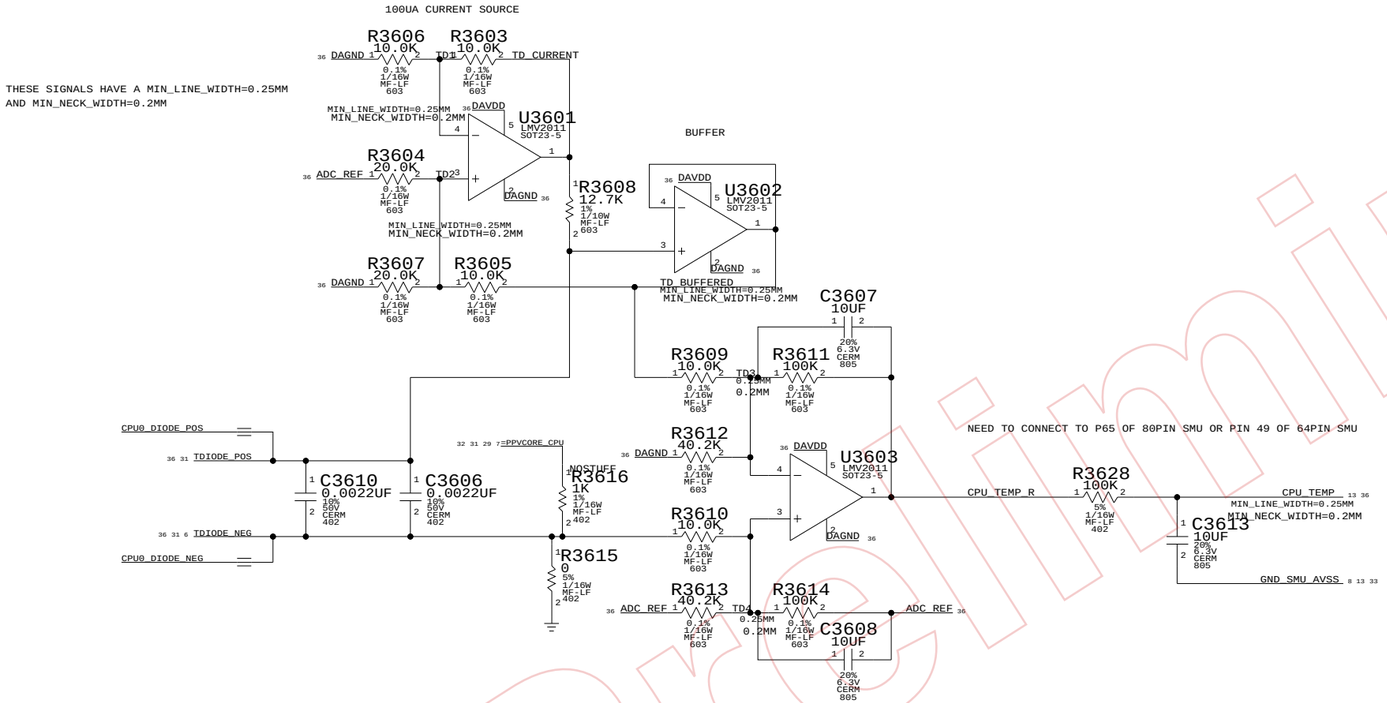
CPU VREG OUTPUT CAPS

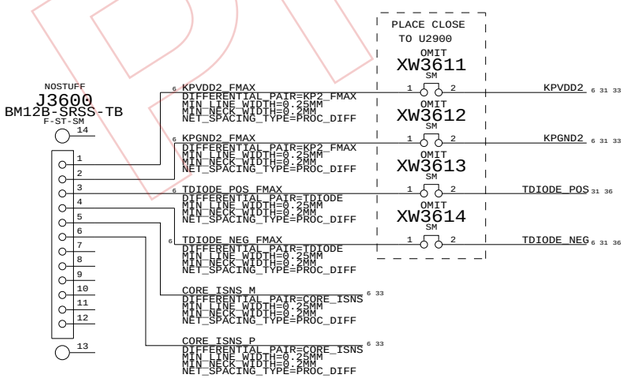
SYNC_MASTER=N/A SYNC_DATE=N/A

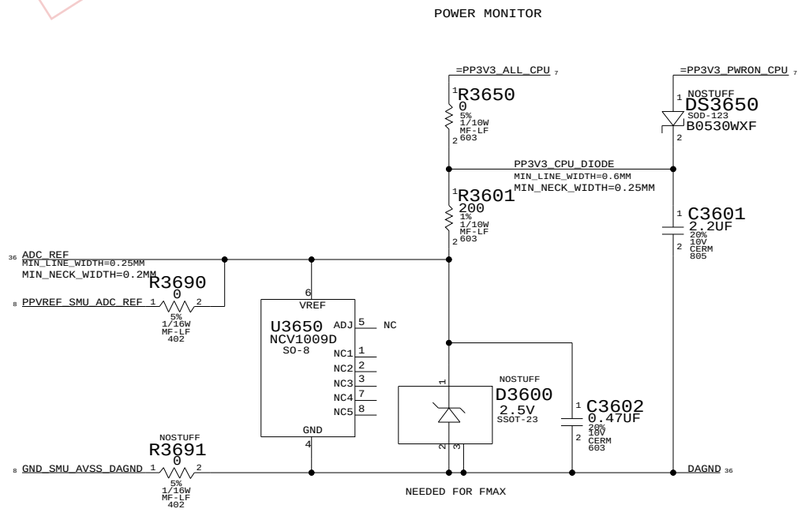
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 35 OF 102	









CPU DIODE CONDITIONER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 36 OF 102	

U3TWINS DO NOT HAVE MASKS

=PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT — MEMORY DATA INTERFACE

RAM_DQ_R<0>	AF20	DDR_DQ0	DDR_DQ64 AG27 RAM_DQ_R<64>
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RAM_DQ_R<2>	AH21	DDR_DQ2	DDR_DQ66 AE24 RAM_DQ_R<66>
RAM_DQ_R<3>	AG21	DDR_DQ3	DDR_DQ67 AG26 RAM_DQ_R<67>
RAM_DQ_R<4>	AB20	DDR_DQ4	DDR_DQ68 AF26 RAM_DQ_R<68>
RAM_DQ_R<5>	AC21	DDR_DQ5	DDR_DQ69 AD24 RAM_DQ_R<69>
RAM_DQ_R<6>	AD23	DDR_DQ6	DDR_DQ70 AD25 RAM_DQ_R<70>
RAM_DQ_R<7>	AD21	DDR_DQ7	DDR_DQ71 AG28 RAM_DQ_R<71>
RAM_DQ_R<8>	AH26	DDR_DQ8	DDR_DQ72 AF28 RAM_DQ_R<72>
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RAM_DQ_R<21>	V23	DDR_DQ21	DDR_DQ85 Y25 RAM_DQ_R<85>
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RAM_DQ_R<26>	R21	DDR_DQ26	DDR_DQ90 V24 RAM_DQ_R<90>
RAM_DQ_R<27>	U23	DDR_DQ27	DDR_DQ91 W28 RAM_DQ_R<91>
RAM_DQ_R<28>	P26	DDR_DQ28	DDR_DQ92 U27 RAM_DQ_R<92>
RAM_DQ_R<29>	R24	DDR_DQ29	DDR_DQ93 V28 RAM_DQ_R<93>
RAM_DQ_R<30>	P24	DDR_DQ30	DDR_DQ94 T28 RAM_DQ_R<94>
RAM_DQ_R<31>	P23	DDR_DQ31	DDR_DQ95 U26 RAM_DQ_R<95>
RAM_DQ_R<32>	M25	DDR_DQ32	DDR_DQ96 R27 RAM_DQ_R<96>
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RAM_DQ_R<35>	P22	DDR_DQ35	DDR_DQ99 P27 RAM_DQ_R<99>
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RAM_DQ_R<43>	C27	DDR_DQ43	DDR_DQ107 K28 RAM_DQ_R<107>
RAM_DQ_R<44>	A22	DDR_DQ44	DDR_DQ108 H27 RAM_DQ_R<108>
RAM_DQ_R<45>	A25	DDR_DQ45	DDR_DQ109 H28 RAM_DQ_R<109>
RAM_DQ_R<46>	C24	DDR_DQ46	DDR_DQ110 J27 RAM_DQ_R<110>
RAM_DQ_R<47>	C23	DDR_DQ47	DDR_DQ111 L24 RAM_DQ_R<111>
RAM_DQ_R<48>	B24	DDR_DQ48	DDR_DQ112 J25 RAM_DQ_R<112>
RAM_DQ_R<49>	B23	DDR_DQ49	DDR_DQ113 J24 RAM_DQ_R<113>
RAM_DQ_R<50>	A23	DDR_DQ50	DDR_DQ114 J26 RAM_DQ_R<114>
RAM_DQ_R<51>	A24	DDR_DQ51	DDR_DQ115 G28 RAM_DQ_R<115>
RAM_DQ_R<52>	A27	DDR_DQ52	DDR_DQ116 H25 RAM_DQ_R<116>
RAM_DQ_R<53>	A28	DDR_DQ53	DDR_DQ117 H24 RAM_DQ_R<117>
RAM_DQ_R<54>	B28	DDR_DQ54	DDR_DQ118 F27 RAM_DQ_R<118>
RAM_DQ_R<55>	A26	DDR_DQ55	DDR_DQ119 H26 RAM_DQ_R<119>
RAM_DQ_R<56>	F24	DDR_DQ56	DDR_DQ120 E28 RAM_DQ_R<120>
RAM_DQ_R<57>	J22	DDR_DQ57	DDR_DQ121 E27 RAM_DQ_R<121>
RAM_DQ_R<58>	E23	DDR_DQ58	DDR_DQ122 F26 RAM_DQ_R<122>
RAM_DQ_R<59>	H23	DDR_DQ59	DDR_DQ123 E26 RAM_DQ_R<123>
RAM_DQ_R<60>	J21	DDR_DQ60	DDR_DQ124 D28 RAM_DQ_R<124>
RAM_DQ_R<61>	H21	DDR_DQ61	DDR_DQ125 C28 RAM_DQ_R<125>
RAM_DQ_R<62>	G21	DDR_DQ62	DDR_DQ126 E25 RAM_DQ_R<126>
RAM_DQ_R<63>	H22	DDR_DQ63	DDR_DQ127 E24 RAM_DQ_R<127>

=PP1V5_PWRON_NB_AVDD — R3702 2.2 5% 1/10W MF-LF 603 — PP1V5_PWRON_RAM_NB_AVDD (VOLTAGE=1.5V)

C3745 1UF 10% 6.3V CERM 402 — C3744 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

=PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT — MEMORY CONTROL INTERFACE

RAM_CLK66M_NB	AC20	DDR_CLKP	DDR_RAS AE21 RAM_RAS_L_R
RAM_CLK_A_P_R	AA12	DDR_CK_A	DDR_CAS AD20 RAM_CAS_L_R
RAM_CLK_A_N_R	AB12	DDR_CK_AN	DDR_WE AC23 RAM_WE_L_R
RAM_CLK_B_P_R	AB14	DDR_CK_B	DDR_BA0 AF21 RAM_BA_R<0>
RAM_CLK_B_N_R	AA14	DDR_CK_BN	DDR_BA1 AE20 RAM_BA_R<1>
RAM_CLK_C_P_R	AE15	DDR_CK_C	DDR_MUXEN0 AH16 RAM_MUXEN0
RAM_CLK_C_N_R	AE14	DDR_CK_CN	DDR_MUXEN4 AH18 RAM_MUXEN4
RAM_CLK_D_P_R	AC14	DDR_CK_D	DDR_MAD0 AG12 RAM_A_R<0>
RAM_CLK_D_N_R	AD14	DDR_CK_DN	DDR_MAD1 AH13 RAM_A_R<1>
RAM_CLK_E_P_R	AD15	DDR_CK_E	DDR_MAD2 AH14 RAM_A_R<2>
RAM_CLK_E_N_R	AC15	DDR_CK_EN	DDR_MAD3 AH15 RAM_A_R<3>
RAM_CLK_F_P_R	AA15	DDR_CK_F	DDR_MAD4 AF12 RAM_A_R<4>
RAM_CLK_F_N_R	AB15	DDR_CK_FN	DDR_MAD5 AE12 RAM_A_R<5>
RAM_CKE_R<0>	AC17	DDR_CKE0	DDR_MAD6 AD12 RAM_A_R<6>
RAM_CKE_R<1>	AD17	DDR_CKE1	DDR_MAD7 AC12 RAM_A_R<7>
RAM_CKE_R<2>	AE17	DDR_CKE2	DDR_MAD8 AG15 RAM_A_R<8>
RAM_CKE_R<3>	AF17	DDR_CKE3	DDR_MAD9 AF15 RAM_A_R<9>
RAM_CKE_R<4>	AB17	DDR_CKE4	DDR_MAD10 AF14 RAM_A_R<10>
RAM_CKE_R<5>	AA17	DDR_CKE5	DDR_MAD11 AG14 RAM_A_R<11>
RAM_CKE_R<6>	AB18	DDR_CKE6	DDR_MAD12 AH17 RAM_A_R<12>
RAM_CKE_R<7>	AA18	DDR_CKE7	DDR_MAD13 AG17 RAM_A_R<13>
	Y21	DDR_VREF0	
	U21	DDR_VREF1	DDR_CS0 AF18 RAM_CS_L_R<0>
	L21	DDR_VREF2	DDR_CS1 AE18 RAM_CS_L_R<1>
	H20	DDR_VREF3	DDR_CS2 AG20 RAM_CS_L_R<2>
	AA21	DDR_VREF4	DDR_CS3 AH20 RAM_CS_L_R<3>
	M21	DDR_VREF5	DDR_CS8 AC18 RAM_CS_L_R<8>
	V21	DDR_VREF6	DDR_CS9 AD18 RAM_CS_L_R<9>
	J20	DDR_VREF7	DDR_CS10 AG18 RAM_CS_L_R<10>
			DDR_CS11 AH19 RAM_CS_L_R<11>
			DDR_DQSP0 AC24 RAM_DQS_R<0>
			DDR_DQSP1 AG23 RAM_DQS_R<1>
			DDR_DQSP2 Y23 RAM_DQS_R<2>
			DDR_DQSP3 R23 RAM_DQS_R<3>
			DDR_DQSP4 M22 RAM_DQS_R<4>
			DDR_DQSP5 B26 RAM_DQS_R<5>
			DDR_DQSP6 B27 RAM_DQS_R<6>
			DDR_DQSP7 F23 RAM_DQS_R<7>
			DDR_DQSP8 AE23 RAM_DQS_R<8>
			DDR_DQSP9 AD28 RAM_DQS_R<9>
			DDR_DQSP10 Y27 RAM_DQS_R<10>
			DDR_DQSP11 U28 RAM_DQS_R<11>
			DDR_DQSP12 M27 RAM_DQS_R<12>
			DDR_DQSP13 J28 RAM_DQS_R<13>
			DDR_DQSP14 F28 RAM_DQS_R<14>
			DDR_DQSP15 F25 RAM_DQS_R<15>

DDR_CLK_AVSS — AA20

=PP1V25_PWRON_RAM_VREF_NB — R3700 1K 1% 1/10W MF-LF 402 — R3701 1K 1% 1/10W MF-LF 402 — PP1V25_PWRON_RAM_VREF_NB (VOLTAGE=1.25V)

C3730 C3746 C3747 C3748 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

=PP2V5_PWRON_RAM

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 — 0.1UF 20% 10V CERM 402

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 C3740 C3739 C3738 — 0.1UF 20% 10V CERM 402

U3LITE MEMORY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11

SCALE: NONE — SHT 37 OF 102

ALL R PACKS ARE 1/16W 5%

RAM_DQ_R<7>	RP3836	4	5	22	RAM_DQ<7>	38 40 44
RAM_DQ_R<2>	RP3836	1	8	22	RAM_DQ<2>	38 40 44
RAM_DQ_R<0>	RP3836	3	6	22	RAM_DQ<0>	38 40 44
RAM_DQ_R<3>	RP3836	2	7	22	RAM_DQ<3>	38 40 44
RAM_DQ_R<1>	RP3816	1	8	22	RAM_DQ<1>	38 40 44
RAM_DQ_R<4>	RP3816	2	7	22	RAM_DQ<4>	38 40 44
RAM_DQ_R<6>	RP3816	4	5	22	RAM_DQ<6>	38 40 44
RAM_DQ_R<5>	RP3816	3	6	22	RAM_DQ<5>	38 40 44
RAM_DQ_R<9>	RP3835	4	5	22	RAM_DQ<9>	38 40 44
RAM_DQ_R<10>	RP3801	1	8	22	RAM_DQ<10>	38 40 44
RAM_DQ_R<11>	RP3801	3	6	22	RAM_DQ<11>	38 40 44
RAM_DQ_R<14>	RP3801	4	5	22	RAM_DQ<14>	38 40 44
RAM_DQ_R<12>	RP3835	2	7	22	RAM_DQ<12>	38 40 44
RAM_DQ_R<13>	RP3801	2	7	22	RAM_DQ<13>	38 40 44
RAM_DQ_R<15>	RP3835	1	8	22	RAM_DQ<15>	38 40 44
RAM_DQ_R<8>	RP3835	3	6	22	RAM_DQ<8>	38 40 44
RAM_DQ_R<17>	RP3822	1	8	22	RAM_DQ<17>	38 40 44
RAM_DQ_R<22>	RP3822	4	5	22	RAM_DQ<22>	38 40 44
RAM_DQ_R<19>	RP3822	2	7	22	RAM_DQ<19>	38 40 44
RAM_DQ_R<18>	RP3822	3	6	22	RAM_DQ<18>	38 40 44
RAM_DQ_R<20>	RP3823	3	6	22	RAM_DQ<20>	38 40 44
RAM_DQ_R<16>	RP3823	4	5	22	RAM_DQ<16>	38 40 44
RAM_DQ_R<21>	RP3823	2	7	22	RAM_DQ<21>	38 40 44
RAM_DQ_R<23>	RP3823	1	8	22	RAM_DQ<23>	38 40 44
RAM_DQ_R<30>	RP3808	3	6	22	RAM_DQ<30>	38 40 44
RAM_DQ_R<26>	RP3824	2	7	22	RAM_DQ<26>	38 40 44
RAM_DQ_R<24>	RP3808	1	8	22	RAM_DQ<24>	38 40 44
RAM_DQ_R<27>	RP3824	1	8	22	RAM_DQ<27>	38 40 44
RAM_DQ_R<28>	RP3808	4	5	22	RAM_DQ<28>	38 40 44
RAM_DQ_R<31>	RP3808	2	7	22	RAM_DQ<31>	38 40 44
RAM_DQ_R<29>	RP3824	4	5	22	RAM_DQ<29>	38 40 44
RAM_DQ_R<25>	RP3824	3	6	22	RAM_DQ<25>	38 40 44
RAM_DQ_R<32>	RP3826	4	5	22	RAM_DQ<32>	38 40 44
RAM_DQ_R<35>	RP3807	2	7	22	RAM_DQ<35>	38 40 44
RAM_DQ_R<38>	RP3826	2	7	22	RAM_DQ<38>	38 40 44
RAM_DQ_R<37>	RP3807	4	5	22	RAM_DQ<37>	38 40 44
RAM_DQ_R<39>	RP3826	3	6	22	RAM_DQ<39>	38 40 44
RAM_DQ_R<33>	RP3807	3	6	22	RAM_DQ<33>	38 40 44
RAM_DQ_R<34>	RP3807	1	8	22	RAM_DQ<34>	38 40 44
RAM_DQ_R<36>	RP3826	1	8	22	RAM_DQ<36>	38 40 44
RAM_DQ_R<47>	RP3811	2	7	22	RAM_DQ<47>	38 40 44
RAM_DQ_R<46>	RP3811	1	8	22	RAM_DQ<46>	38 40 44
RAM_DQ_R<43>	RP3814	2	7	22	RAM_DQ<43>	38 40 44
RAM_DQ_R<41>	RP3814	1	8	22	RAM_DQ<41>	38 40 44
RAM_DQ_R<45>	RP3811	4	5	22	RAM_DQ<45>	38 40 44
RAM_DQ_R<42>	RP3814	3	6	22	RAM_DQ<42>	38 40 44
RAM_DQ_R<40>	RP3814	4	5	22	RAM_DQ<40>	38 40 44
RAM_DQ_R<44>	RP3811	3	6	22	RAM_DQ<44>	38 40 44
RAM_DQ_R<51>	RP3830	4	5	22	RAM_DQ<51>	38 40 44
RAM_DQ_R<50>	RP3830	2	7	22	RAM_DQ<50>	38 40 44
RAM_DQ_R<49>	RP3830	1	8	22	RAM_DQ<49>	38 40 44
RAM_DQ_R<48>	RP3830	3	6	22	RAM_DQ<48>	38 40 44
RAM_DQ_R<52>	RP3812	2	7	22	RAM_DQ<52>	38 40 44
RAM_DQ_R<53>	RP3812	3	6	22	RAM_DQ<53>	38 40 44
RAM_DQ_R<54>	RP3812	4	5	22	RAM_DQ<54>	38 40 44
RAM_DQ_R<55>	RP3812	1	8	22	RAM_DQ<55>	38 40 44
RAM_DQ_R<56>	RP3813	1	8	22	RAM_DQ<56>	38 40 44
RAM_DQ_R<63>	RP3831	4	5	22	RAM_DQ<63>	38 40 44
RAM_DQ_R<59>	RP3813	2	7	22	RAM_DQ<59>	38 40 44
RAM_DQ_R<61>	RP3831	2	7	22	RAM_DQ<61>	38 40 44
RAM_DQ_R<57>	RP3831	3	6	22	RAM_DQ<57>	38 40 44
RAM_DQ_R<60>	RP3831	1	8	22	RAM_DQ<60>	38 40 44
RAM_DQ_R<58>	RP3813	3	6	22	RAM_DQ<58>	38 40 44
RAM_DQ_R<62>	RP3813	4	5	22	RAM_DQ<62>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>	38 40 45
RAM_CKE_R<5>	RP3841	4	5	15	RAM_CKE<5>	38 40 45
RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>	38 40 44
RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>	38 40 44
RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>	38 40 45
RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>	38 40 45
RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>	38 40 44
RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>	38 40 44
RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>	38 40 44
RAM_A_R<10>	RP3832	2	7	15	RAM_A<10>	38 40 45
RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L	38 40 45
RAM_A_R<4>	RP3833	3	6	15	RAM_A<4>	38 40 44
RAM_A_R<6>	RP3833	2	7	15	RAM_A<6>	38 40 44
RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>	38 40 44
	RP3834	1	8	15		
RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>	38 40 44
RAM_A_R<2>	RP3834	2	7	15	RAM_A<2>	38 40 44
RAM_A_R<0>	RP3833	4	5	15	RAM_A<0>	38 40 44
RAM_A_R<5>	RP3832	1	8	15	RAM_A<5>	38 40 44
RAM_A_R<13>	RP3800	2	7	15	RAM_A<13>	38 40 44
RAM_A_R<3>	RP3800	1	8	15	RAM_A<3>	38 40 44
RAM_CAS_L_R	RP3804	1	8	15	RAM_CAS_L	38 40 45
RAM_BA_R<0>	RP3804	4	5	15	RAM_BA<0>	38 40 45
RAM_BA_R<1>	RP3804	2	7	15	RAM_BA<1>	38 40 45
RAM_RAS_L_R	RP3804	3	6	15	RAM_RAS_L	38 40 45
RAM_A_R<9>	RP3834	3	6	15	RAM_A<9>	38 40 44
RAM_A_R<8>	RP3834	4	5	15	RAM_A<8>	38 40 44

RAM_DQ_R<68>	RP3818	2	7	22	RAM_DQ<68>	38 40 45
RAM_DQ_R<65>	RP3805	2	7	22	RAM_DQ<65>	38 40 45
RAM_DQ_R<70>	RP3818	4	5	22	RAM_DQ<70>	38 40 45
RAM_DQ_R<66>	RP3805	1	8	22	RAM_DQ<66>	38 40 45
RAM_DQ_R<71>	RP3818	3	6	22	RAM_DQ<71>	38 40 45
RAM_DQ_R<64>	RP3805	4	5	22	RAM_DQ<64>	38 40 45
RAM_DQ_R<67>	RP3805	3	6	22	RAM_DQ<67>	38 40 45
RAM_DQ_R<69>	RP3818	1	8	22	RAM_DQ<69>	38 40 45
RAM_DQ_R<74>	RP3817	3	6	22	RAM_DQ<74>	38 40 45
RAM_DQ_R<73>	RP3802	4	5	22	RAM_DQ<73>	38 40 45
RAM_DQ_R<72>	RP3817	2	7	22	RAM_DQ<72>	38 40 45
RAM_DQ_R<75>	RP3817	4	5	22	RAM_DQ<75>	38 40 45
RAM_DQ_R<78>	RP3802	2	7	22	RAM_DQ<78>	38 40 45
RAM_DQ_R<79>	RP3817	1	8	22	RAM_DQ<79>	38 40 45
RAM_DQ_R<77>	RP3802	1	8	22	RAM_DQ<77>	38 40 45
RAM_DQ_R<76>	RP3802	3	6	22	RAM_DQ<76>	38 40 45
RAM_DQ_R<87>	RP3806	2	7	22	RAM_DQ<87>	38 40 45
RAM_DQ_R<86>	RP3821	1	8	22	RAM_DQ<86>	38 40 45
RAM_DQ_R<81>	RP3821	4	5	22	RAM_DQ<81>	38 40 45
RAM_DQ_R<80>	RP3821	2	7	22	RAM_DQ<80>	38 40 45
RAM_DQ_R<84>	RP3806	1	8	22	RAM_DQ<84>	38 40 45
RAM_DQ_R<85>	RP3806	3	6	22	RAM_DQ<85>	38 40 45
RAM_DQ_R<83>	RP3821	3	6	22	RAM_DQ<83>	38 40 45
RAM_DQ_R<82>	RP3806	4	5	22	RAM_DQ<82>	38 40 45
RAM_DQ_R<91>	RP3819	3	6	22	RAM_DQ<91>	38 40 45
RAM_DQ_R<93>	RP3819	1	8	22	RAM_DQ<93>	38 40 45
RAM_DQ_R<94>	RP3803	2	7	22	RAM_DQ<94>	38 40 45
RAM_DQ_R<90>	RP3819	4	5	22	RAM_DQ<90>	38 40 45
RAM_DQ_R<88>	RP3803	4	5	22	RAM_DQ<88>	38 40 45
RAM_DQ_R<89>	RP3819	2	7	22	RAM_DQ<89>	38 40 45
RAM_DQ_R<92>	RP3803	3	6	22	RAM_DQ<92>	38 40 45
RAM_DQ_R<95>	RP3803	1	8	22	RAM_DQ<95>	38 40 45
RAM_DQ_R<98>	RP3820	4	5	22	RAM_DQ<98>	38 40 45
RAM_DQ_R<96>	RP3820	3	6	22	RAM_DQ<96>	38 40 45
RAM_DQ_R<103>	RP3820	2	7	22	RAM_DQ<103>	38 40 45
RAM_DQ_R<97>	RP3820	1	8	22	RAM_DQ<97>	38 40 45
RAM_DQ_R<100>	RP3825	2	7	22	RAM_DQ<100>	38 40 45
RAM_DQ_R<99>	RP3825	3	6	22	RAM_DQ<99>	38 40 45
RAM_DQ_R<102>	RP3825	1	8	22	RAM_DQ<102>	38 40 45
RAM_DQ_R<101>	RP3825	4	5	22	RAM_DQ<101>	38 40 45
RAM_DQ_R<111>	RP3809	1	8	22	RAM_DQ<111>	38 40 45
RAM_DQ_R<106>	RP3809	3	6	22	RAM_DQ<106>	38 40 45
RAM_DQ_R<105>	RP3809	2	7	22	RAM_DQ<105>	38 40 45
RAM_DQ_R<108>	RP3829	2	7	22	RAM_DQ<108>	38 40 45
RAM_DQ_R<107>	RP3829	4	5	22	RAM_DQ<107>	38 40 45
RAM_DQ_R<110>	RP3829	3	6	22	RAM_DQ<110>	38 40 45
RAM_DQ_R<104>	RP3809	4	5	22	RAM_DQ<104>	38 40 45
RAM_DQ_R<109>	RP3829	1	8	22	RAM_DQ<109>	38 40 45
RAM_DQ_R<119>	RP3828	4	5	22	RAM_DQ<119>	38 40 45
RAM_DQ_R<112>	RP3815	2	7	22	RAM_DQ<112>	38 40 45
RAM_DQ_R<117>	RP3815	1	8	22	RAM_DQ<117>	38 40 45
RAM_DQ_R<118>	RP3828	1	8	22	RAM_DQ<118>	38 40 45
RAM_DQ_R<113>	RP3815	3	6	22	RAM_DQ<113>	38 40 45
RAM_DQ_R<115>	RP3828	3	6	22	RAM_DQ<115>	38 40 45
RAM_DQ_R<116>	RP3828	2	7	22	RAM_DQ<116>	38 40 45
RAM_DQ_R<114>	RP3815	4	5	22	RAM_DQ<114>	38 40 45
RAM_DQ_R<121>	RP3827	3	6	22	RAM_DQ<121>	38 40 45
RAM_DQ_R<124>	RP3827	2	7	22	RAM_DQ<124>	38 40 45
RAM_DQ_R<120>	RP3827	4	5	22	RAM_DQ<120>	38 40 45
RAM_DQ_R<123>	RP3810	2	7	22	RAM_DQ<123>	38 40 45
RAM_DQ_R<125>	RP3827	1	8	22	RAM_DQ<125>	38 40 45
RAM_DQ_R<122>	RP3810	4	5	22	RAM_DQ<122>	38 40 45
RAM_DQ_R<126>	RP3810	1	8	22	RAM_DQ<126>	38 40 45
RAM_DQ_R<127>	RP3810	3	6	22	RAM_DQ<127>	38 40 45

THE FOLLOWING ARE 0402 5% RESISTORS

RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P	38 40
RAM_CLK_A_N_R	R3817	1	2	15	RAM_CLK_A_N	38 40
RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P	38 40
RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N	38 40
RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P	38 40
RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N	38 40
RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P	38 40
RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N	38 40
RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P	38 40
RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N	38 40
RAM_CLK_F_P_R	R3826	1	2	15	RAM_CLK_F_P	38 40
RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N	38 40

RAM_DQS_R<0>	R3800	1	2	15	RAM_DQS<0>	38 40 44
RAM_DQS_R<1>	R3801	1	2	15	RAM_DQS<1>	38 40 44
RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>	38 40 44
RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>	38 40 44
RAM_DQS_R<4>	R3804	1	2	15	RAM_DQS<4>	38 40 44
RAM_DQS_R<5>	R3805	1	2	15	RAM_DQS<5>	38 40 44
RAM_DQS_R<6>	R3806	1	2	15	RAM_DQS<6>	38 40 44
RAM_DQS_R<7>	R3807	1	2	15	RAM_DQS<7>	38 40 44
RAM_DQS_R<8>	R3808	1	2	15	RAM_DQS<8>	38 40 45
RAM_DQS_R<9>	R3809	1	2	15	RAM_DQS<9>	38 40 45
RAM_DQS_R<10>	R3810	1	2	15	RAM_DQS<10>	38 40 45
RAM_DQS_R<11>	R3811	1	2	15	RAM_DQS<11>	38 40 45
RAM_DQS_R<12>	R3812	1	2	15	RAM_DQS<12>	38 40 45
RAM_DQS_R<13>	R3813	1	2	15	RAM_DQS<13>	38 40 45
RAM_DQS_R<14>	R3814	1	2	15	RAM_DQS<14>	38 40 45
RAM_DQS_R<15>	R3815	1	2	15	RAM_DQS<15>	38 40 45

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLK_A_P_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	2006
RAM_CLK_A_N_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	2007
RAM_CLK_B_P_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	2008
RAM_CLK_B_N_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	2009
RAM_CLK_C_P_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	2010
RAM_CLK_C_N_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	2011
RAM_CLK_D_P_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	2012
RAM_CLK_D_N_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	2013
RAM_CLK_E_P_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	2014
RAM_CLK_E_N_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	2015
RAM_CLK_F_P_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	2016
RAM_CLK_F_N_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	2017
RAM_CLK_A_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	2018
RAM_CLK_A_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	2019
RAM_CLK_B_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	2020
RAM_CLK_B_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	2021
RAM_CLK_C_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	2022
RAM_CLK_C_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	2023
RAM_CLK_D_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	2024
RAM_CLK_D_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	2025
RAM_CLK_E_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	2026
RAM_CLK_E_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	2027
RAM_CLK_F_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	2028
RAM_CLK_F_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	2029
RAM_CKE_R<1..0>		RAM_CAD	RAM_CAD		2340
RAM_CKE_R<5..4>		RAM_CAD	RAM_CAD		2357
RAM_CKE<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		2354
RAM_CKE<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		2355
RAM_CKE<4>	RAM_CKECS1	RAM_CAD	RAM_CAD		2356
RAM_CKE<5>	RAM_CKECS1	RAM_CAD	RAM_CAD		2358
RAM_CS_L_R<1..0>		RAM_CAD	RAM_CAD		2359
RAM_CS_L_R<9..8>		RAM_CAD	RAM_CAD		2341
RAM_CS_L<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		2343
RAM_CS_L<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		2342
RAM_CS_L<8>	RAM_CKECS1	RAM_CAD	RAM_CAD		2345
RAM_CS_L<9>	RAM_CKECS1	RAM_CAD	RAM_CAD		2344
RAM_DQS_R<15..0>		RAM_CAD	RAM_CAD		2305
RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		2704
RAM_DQ<127..0>		RAM_CAD	RAM_CAD		2690
RAM_DQS<0>	RAM_DQS0	RAM_CAD	RAM_CAD		2346
RAM_DQ<7..0>	RAM_DQS0	RAM_CAD	RAM_CAD		2348
RAM_DQS<1>	RAM_DQS1	RAM_CAD	RAM_CAD		2351
RAM_DQ<15..8>	RAM_DQS1	RAM_CAD	RAM_CAD		2352
RAM_DQS<2>	RAM_DQS2	RAM_CAD	RAM_CAD		2353
RAM_DQ<23..16>	RAM_DQS2	RAM_CAD	RAM_CAD		2354
RAM_DQS<3>	RAM_DQS3	RAM_CAD	RAM_CAD		2355
RAM_DQ<31..24>	RAM_DQS3	RAM_CAD	RAM_CAD		2356
RAM_DQS<4>	RAM_DQS4	RAM_CAD	RAM_CAD		2357
RAM_DQ<39..32>	RAM_DQS4	RAM_CAD	RAM_CAD		2358
RAM_DQS<5>	RAM_DQS5	RAM_CAD	RAM_CAD		2359
RAM_DQ<47..40>	RAM_DQS5	RAM_CAD	RAM_CAD		2360
RAM_DQS<6>	RAM_DQS6	RAM_CAD	RAM_CAD		2361
RAM_DQ<55..48>	RAM_DQS6	RAM_CAD	RAM_CAD		2362
RAM_DQS<7>	RAM_DQS7	RAM_CAD	RAM_CAD		2363
RAM_DQ<63..56>	RAM_DQS7	RAM_CAD	RAM_CAD		2364
RAM_DQS<8>	RAM_DQS8	RAM_CAD	RAM_CAD		2365
RAM_DQ<71..64>	RAM_DQS8	RAM_CAD	RAM_CAD		2367
RAM_DQS<9>	RAM_DQS9	RAM_CAD	RAM_CAD		2366
RAM_DQ<79..72>	RAM_DQS9	RAM_CAD	RAM_CAD		2368
RAM_DQS<10>	RAM_DQS10	RAM_CAD	RAM_CAD		2370
RAM_DQ<87..80>	RAM_DQS10	RAM_CAD	RAM_CAD		2369
RAM_DQS<11>	RAM_DQS11	RAM_CAD	RAM_CAD		2372
RAM_DQ<95..88>	RAM_DQS11	RAM_CAD	RAM_CAD		2371
RAM_DQS<12>	RAM_DQS12	RAM_CAD	RAM_CAD		2373
RAM_DQ<103..96>	RAM_DQS12	RAM_CAD	RAM_CAD		2375
RAM_DQS<13>	RAM_DQS13	RAM_CAD	RAM_CAD		2374
RAM_DQ<111..104>	RAM_DQS13	RAM_CAD	RAM_CAD		2377
RAM_DQS<14>	RAM_DQS14	RAM_CAD	RAM_CAD		2376
RAM_DQ<119..112>	RAM_DQS14	RAM_CAD	RAM_CAD		2378
RAM_DQS<15>	RAM_DQS15	RAM_CAD	RAM_CAD		2380
RAM_DQ<127..120>	RAM_DQS15	RAM_CAD	RAM_CAD		2379
RAM_A_R<13..0>		RAM_CAD	RAM_CAD		2350
RAM_BA_R<1..0>		RAM_CAD	RAM_CAD		2360
RAM_RAS_L_R		RAM_CAD	RAM_CAD		2361
RAM_CAS_L_R		RAM_CAD	RAM_CAD		2400
RAM_WE_L_R		RAM_CAD	RAM_CAD		2362
RAM_A<13..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		2380
RAM_BA<1..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		2381
RAM_RAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		2382
RAM_CAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		2382
RAM_WE_L	RAM_A_CTL	RAM_CAD	RAM_CAD		2381

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

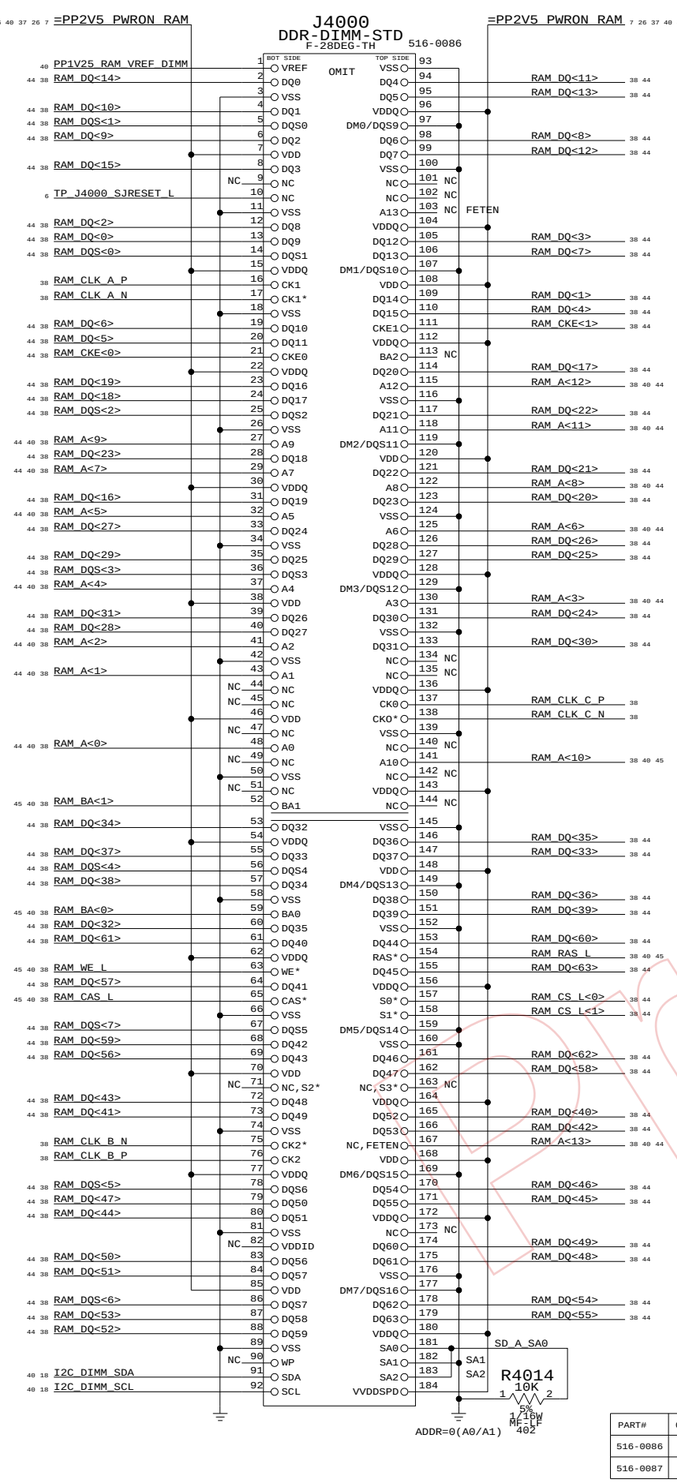
RAM_CAD SPACING IS 10MIL

SERIES TERM

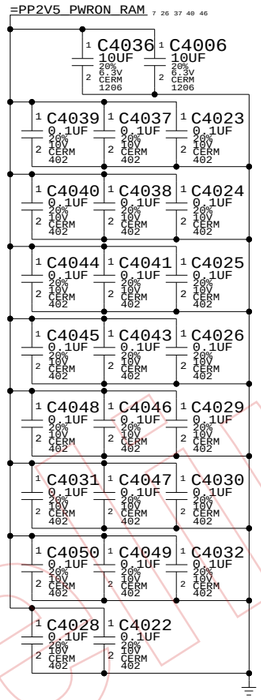
SYNC_MASTER=N/A SYNC_DATE=N/A

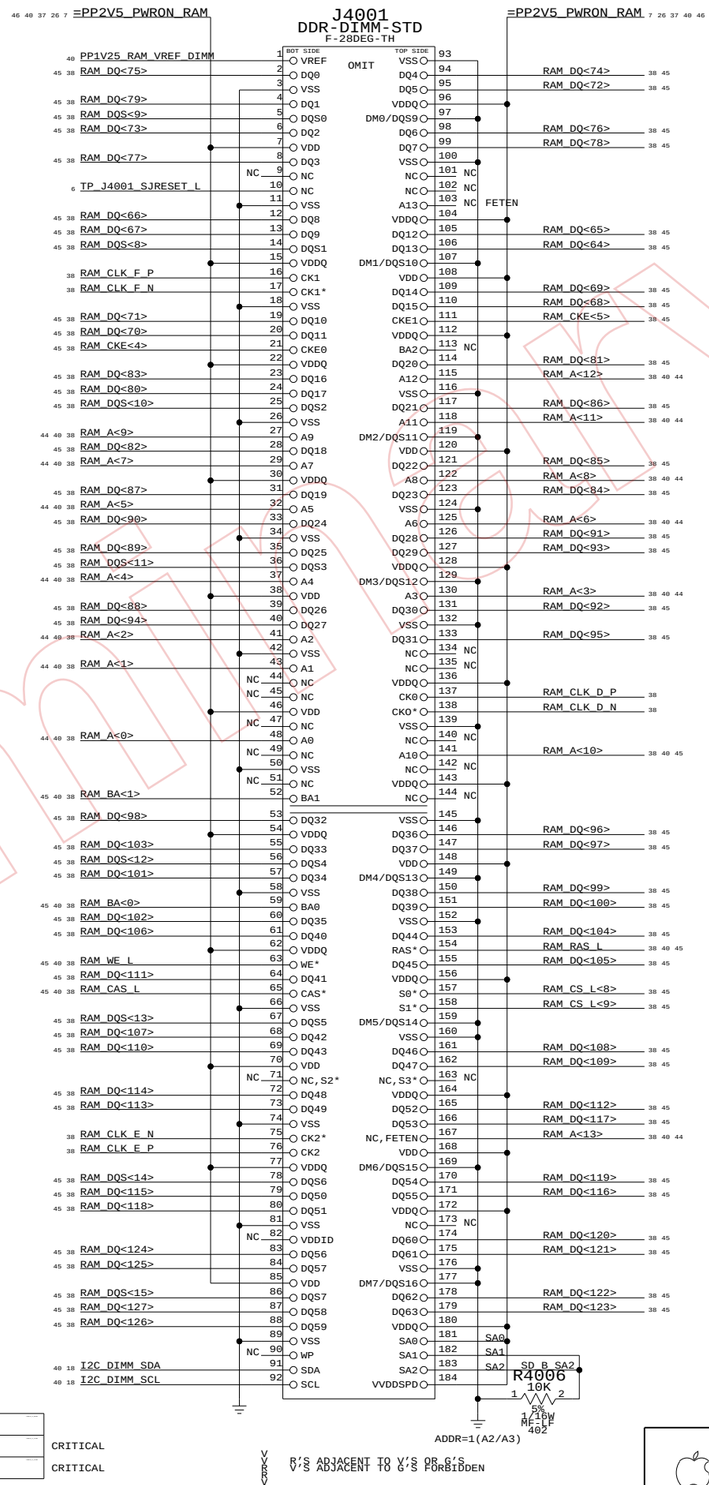
APPLE COMPUTER INC.

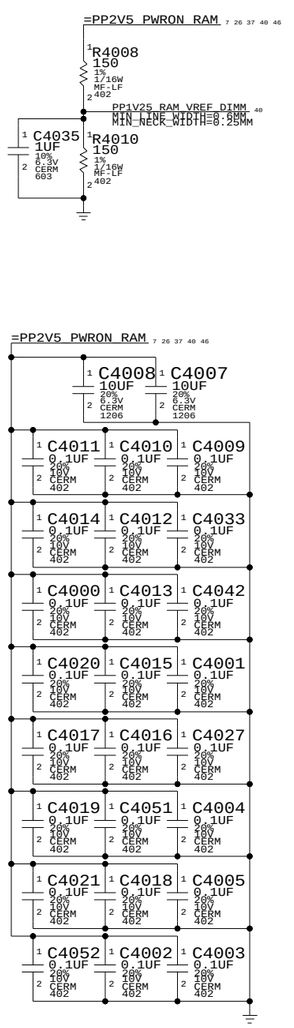
SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 38 OF 102	



PIN 82:
NC: VDD & VDDQ ARE THE SAME
GND: VDD & VDDQ ARE DIFFERENT







PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
516-0086	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD
516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD

CRITICAL
CRITICAL

D'S ADJACENT TO V'S OR G'S
V'S ADJACENT TO G'S FORBIDDEN

DIMMS

SYNC_MASTER=N/A SYNC_DATE=N/A

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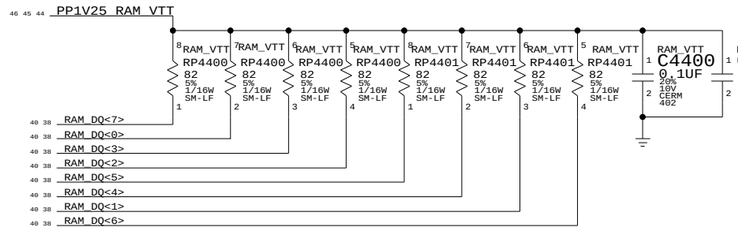
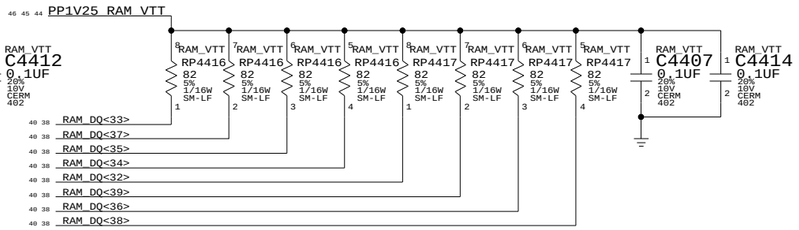
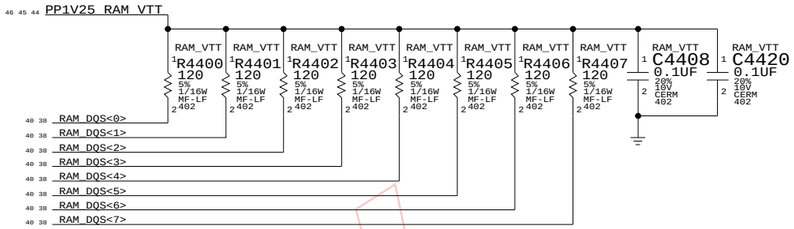
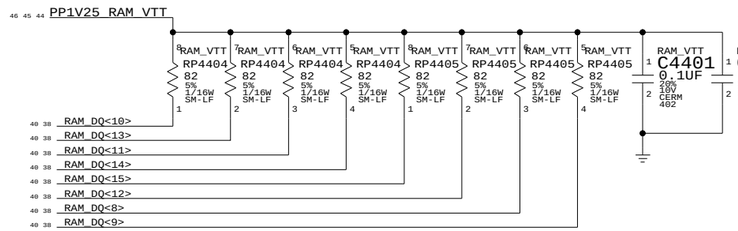
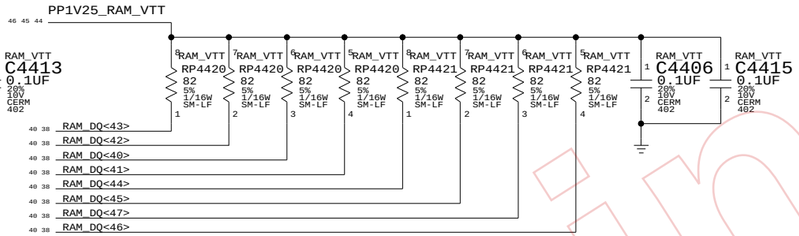
SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 40 OF 102	

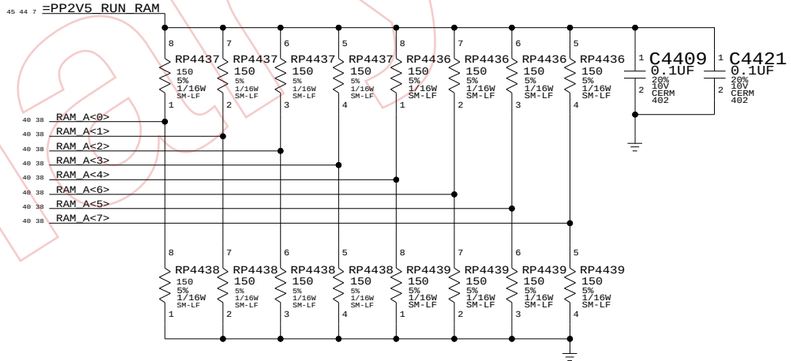


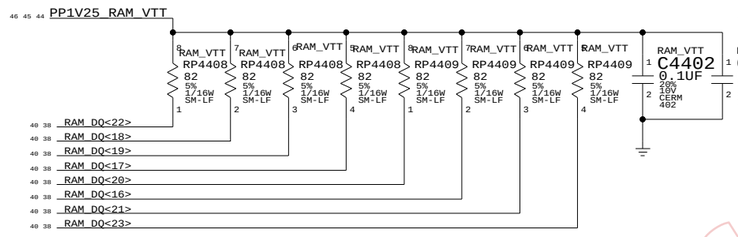


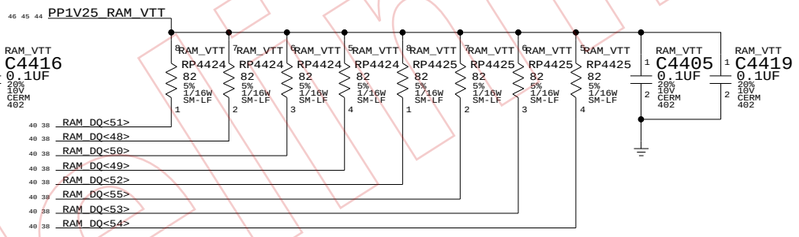


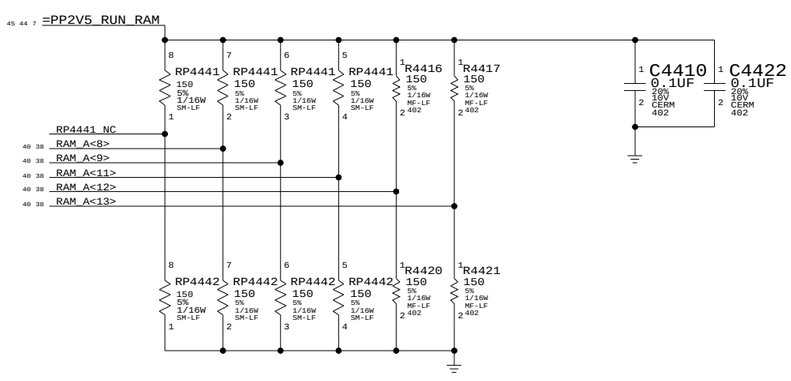


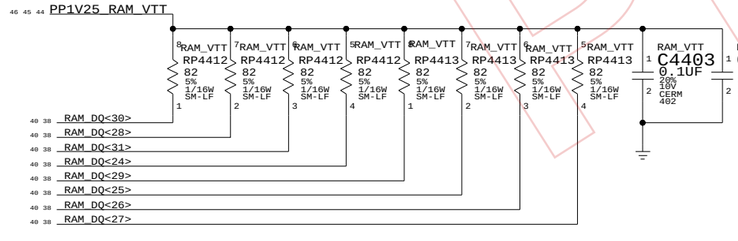


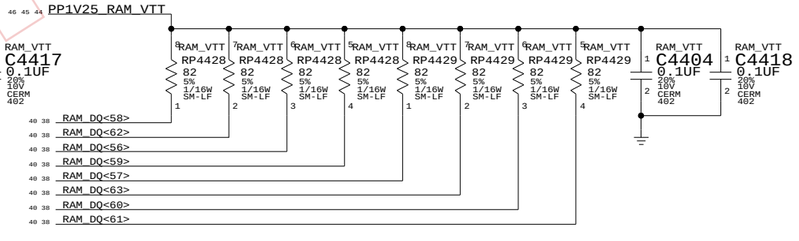


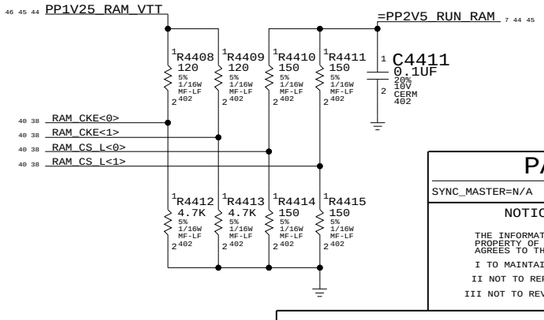










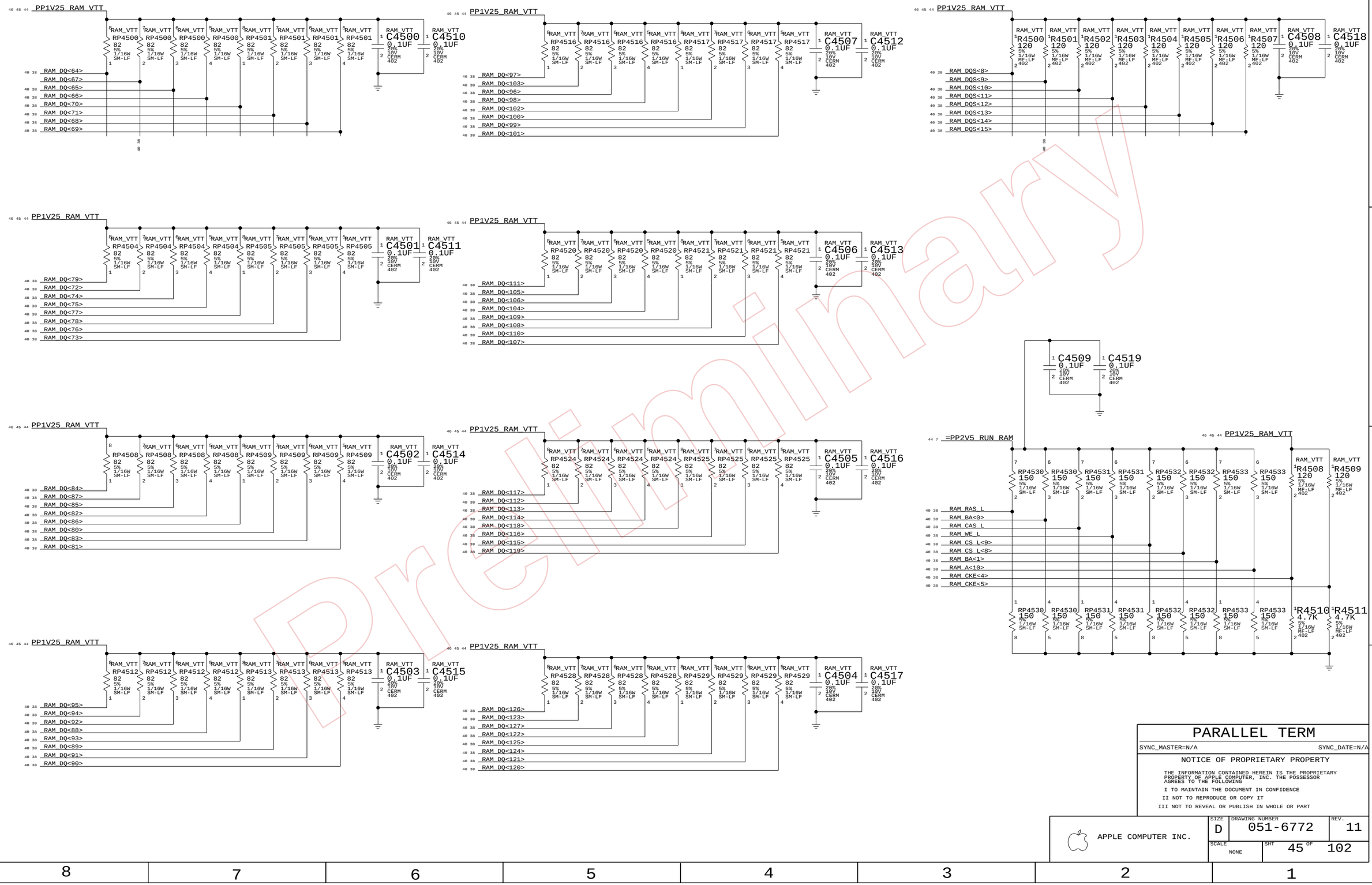


PARALLEL TERM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 44 OF 102	



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APPLE COMPUTER INC.

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D	051-6772	11
SCALE: NONE	SHT 45 OF 102	

ONLY STUFF ONE VTT VREG

=PP2V5_PWRON_RAM

C4610 10UF 20% 6.3V CERM 1206

NOSTUFF R4660 20.5K 1% 1/16W MF-LF 402

NOSTUFF R4661 20.5K 1% 1/16W MF-LF 402

NOSTUFF

RT9173A U4660 TO-252

VIN 1 | VOUT 5 | REFEN 4 | GND (TAB) 2 3 6 | VCNTRL

NOSTUFF C4611 10UF 20% 6.3V CERM 1206

NOSTUFF C4660 1UF 10% 6.3V CERM 402

=PP3V3_PWRON_RAM

NOSTUFF C4661 10UF 20% 6.3V CERM 1206

NOSTUFF C4601 0.1UF 10% 16V X7R 603

NOSTUFF R4603 10K 5% 1/16W MF-LF 402

PHILIPS 353S0603

VDD | REFOUT | VTT | SHTDWN | VSS VSS

U4600_REFOUT

RAM_VTT C4606 0.1UF 10% 16V X7R 603

U4600 NE57811 SPAK-5

RAM_VTT

VR4600_SHTDWN

PP1V25_RAM_VTT
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.25V

C4609 220UF 20% 2V TANT 7343

C4608 10UF 20% 6.3V CERM 1206

C4600 10UF 20% 6.3V CERM 1206

C4602 10UF 20% 6.3V CERM 1206

PLACE 10UF CAPS NEAR DIMMS

NOTE: U4700 PIN 4 IS LOW ACTIVE.

NOSTUFF R4610 0 5% 1/16W MF-LF 402

TURN_ON_VTT

Q4600 2N7002 SOT23-LF

D | G | S

SYS_SLEEP

MEM TERM VREGS

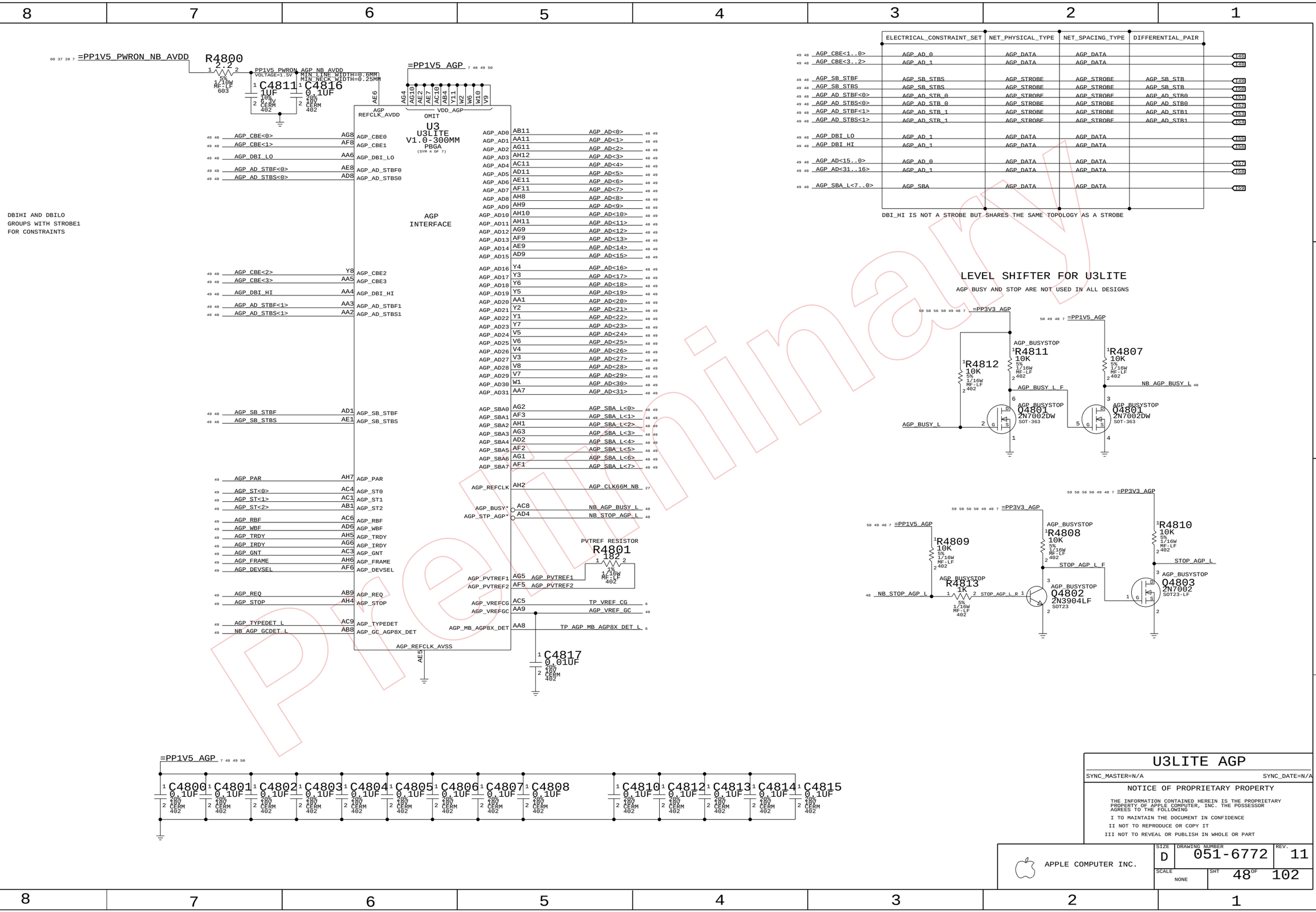
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11

SCALE: NONE

SHT 46 OF 102



ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
AGP_CBE<1..0>	AGP_AD_0	AGP_DATA	AGP_DATA	
AGP_CBE<3..2>	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	AGP_STROBE	AGP_SB_STB
AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	AGP_STROBE	AGP_SB_STB
AGP_AD_STBF<0>	AGP_AD_STB_0	AGP_STROBE	AGP_STROBE	AGP_AD_STB0
AGP_AD_STBS<0>	AGP_AD_STB_0	AGP_STROBE	AGP_STROBE	AGP_AD_STB0
AGP_AD_STBF<1>	AGP_AD_STB_1	AGP_STROBE	AGP_STROBE	AGP_AD_STB1
AGP_AD_STBS<1>	AGP_AD_STB_1	AGP_STROBE	AGP_STROBE	AGP_AD_STB1
AGP_DBI_LO	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_DBI_HI	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_AD<15..0>	AGP_AD_0	AGP_DATA	AGP_DATA	
AGP_AD<31..16>	AGP_AD_1	AGP_DATA	AGP_DATA	
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA	AGP_DATA	

SYNC_MASTER=N/A	SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 48 OF 102	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0231	1	IC,RV351LE, GRAPHICS CTLR	U4900	

U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)

50 49 48 7 =PP1V5_AGP

R4914 3.32K 1% 1/16W MF-LF 402

AGP_VREF_GC 48

R4940 1.02K 1% 1/16W MF-LF 402

C4940 0.01UF 20% 16V CERM 402

VOLTAGE=0.35V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

GPU AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALLS)

50 49 48 7 =PP1V5_AGP

R4906 3.32K 1% 1/16W MF-LF 402

AGP 3.0
0.233 * VDDP
0.35V

GPU_AGP_VREF 49

VOLTAGE=0.35V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

R4907 1.02K 1% 1/16W MF-LF 402

C4957 0.01UF 20% 16V CERM 402

U3LITE SIGNALS

48 NB_AGP_GCDET_L

48 AGP_TYPEDET_L

R4913 0 5% 1/16W MF-LF 402

R4909 10K 5% 1/16W MF-LF 402

50 49 48 7 =PP1V5_AGP

C4900 1UF 10% 6.3V CERM 402

C4901 1UF 10% 6.3V CERM 402

C4902 0.01UF 20% 16V CERM 402

C4903 0.01UF 20% 16V CERM 402

C4904 0.01UF 20% 16V CERM 402

C4905 0.01UF 20% 16V CERM 402

AA23 AA24 P27 T24 T30 U27 V23 V24 W30 Y27 AB30 AC23 AC27 AE30 AF27 J30 M23 M24 N30 P23 T23

VDDP

OMIT

U4900
RV351
BGA
(1 OF 5)

AGP

GPU_AGP_VREF 49

C4910 0.01UF 20% 16V CERM 402

PLACE C4910 CLOSE TO BALL M26

27 AGP_CLK66M_GPU	AG30	PCICLK	
48 AGP_AD<0>	H29	AD0	
48 AGP_AD<1>	H28	AD1	
48 AGP_AD<2>	J29	AD2	
48 AGP_AD<3>	J28	AD3	
48 AGP_AD<4>	K29	AD4	
48 AGP_AD<5>	K28	AD5	
48 AGP_AD<6>	L29	AD6	
48 AGP_AD<7>	L28	AD7	
48 AGP_AD<8>	N28	AD8	
48 AGP_AD<9>	P29	AD9	
48 AGP_AD<10>	P28	AD10	
48 AGP_AD<11>	R29	AD11	
48 AGP_AD<12>	R28	AD12	
48 AGP_AD<13>	T29	AD13	
48 AGP_AD<14>	T28	AD14	
48 AGP_AD<15>	U29	AD15	
48 AGP_AD<16>	N25	AD16	
48 AGP_AD<17>	R26	AD17	
48 AGP_AD<18>	P25	AD18	
48 AGP_AD<19>	R27	AD19	
48 AGP_AD<20>	R25	AD20	
48 AGP_AD<21>	T25	AD21	
48 AGP_AD<22>	T26	AD22	
48 AGP_AD<23>	U25	AD23	
48 AGP_AD<24>	V27	AD24	
48 AGP_AD<25>	W26	AD25	
48 AGP_AD<26>	W25	AD26	
48 AGP_AD<27>	Y26	AD27	
48 AGP_AD<28>	Y25	AD28	
48 AGP_AD<29>	AA26	AD29	
48 AGP_AD<30>	AA25	AD30	
48 AGP_AD<31>	AA27	AD31	
48 AGP_SBA_L<0>	AD28	SBA0	
48 AGP_SBA_L<1>	AD29	SBA1	
48 AGP_SBA_L<2>	AC28	SBA2	
48 AGP_SBA_L<3>	AC29	SBA3	
48 AGP_SBA_L<4>	AA28	SBA4	
48 AGP_SBA_L<5>	AA29	SBA5	
48 AGP_SBA_L<6>	Y28	SBA6	
48 AGP_SBA_L<7>	Y29	SBA7	
8 GPU_RESET_L	AG28	RST*	
48 AGP_ST<0>	AF29	ST0	
48 AGP_ST<1>	AD27	ST1	
48 AGP_ST<2>	AE28	ST2	
48 AGP_REQ	AF28	REQ*	
48 AGP_GNT	AD26	GNT*	
48 AGP_STOP	N26	STOP*	
48 AGP_DEVSEL	V29	DEVSEL*	
48 AGP_TRDY	V28	TRDY*	
48 AGP_IRDY	W29	IRDY*	
48 AGP_FRAME	W28	FRAME*	
48 AGP_WBF	AC26	WBF*	
48 AGP_RBF	AE29	RBF*	

DO WE NEED THE SERIES R?

R4912 0 5% 1/16W MF-LF 402

AGPREF	M26		
CBE0*	N29	AGP_CBE<0>	48
CBE1*	U28	AGP_CBE<1>	48
DBI_LO	AB26	AGP_DBI_LO	48
AD_STBF_0	M28	AGP_AD_STBF<0>	48
AD_STBS_0*	M29	AGP_AD_STBS<0>	48
CBE2*	P26	AGP_CBE<2>	48
CBE3*	U26	AGP_CBE<3>	48
DBI_HI	AB25	AGP_DBI_HI	48
AD_STBF_1	V25	AGP_AD_STBF<1>	48
AD_STBS_1*	V26	AGP_AD_STBS<1>	48
SB_STBF	AB29	AGP_SB_STBF	48
SB_STBS*	AB28	AGP_SB_STBS	48
PAR	M25	AGP_PAR	48
INTA*	AE26		
AGPTEST*	M27	GPU_AGPTEST_L	
AGP8X_DET*	AC25		

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

=PP3V3_AGP 7 48 50 56 58 59

R4908 10K 5% 1/16W MF-LF 402

AGP_INT_L 25

R4910 47 1% 1/16W MF-LF 402

=PP1V5_AGP 7 48 49 50

GPU AGP

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

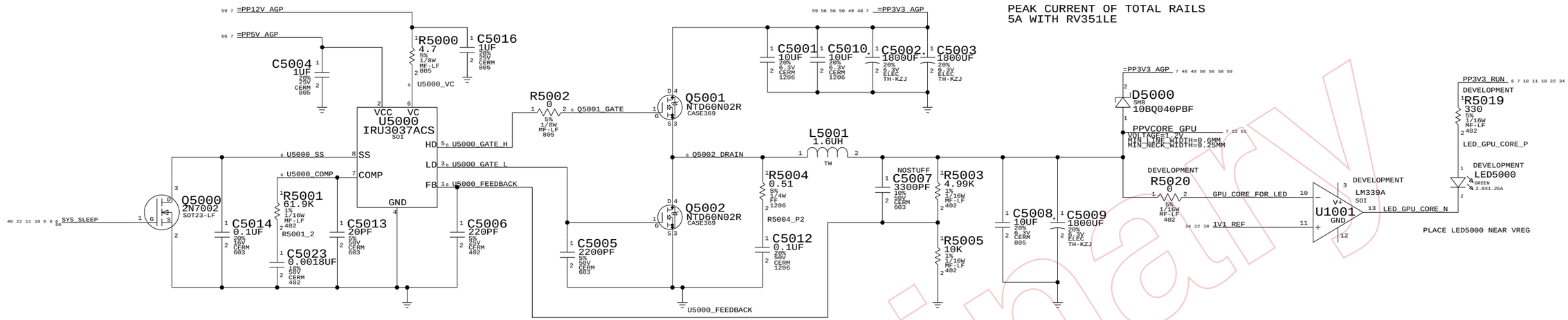
SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 49 OF 102	

GPU VCORE VREG

NOTE:
SET OUTPUT = 1.20V +/- 5% FOR RV351LE

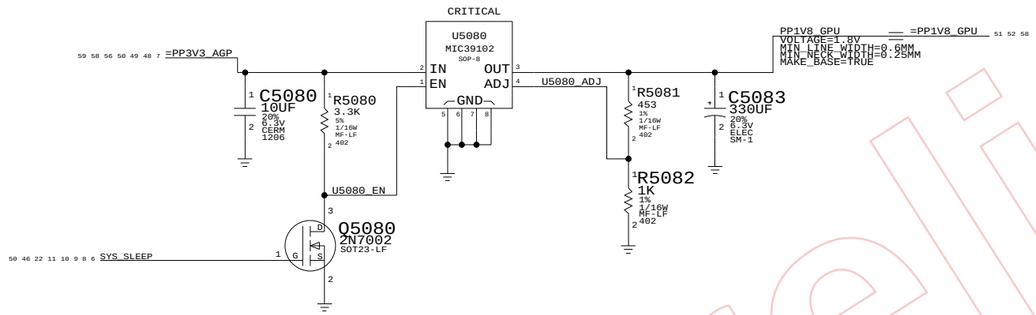
IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R5003+R5005)/R5005 = 1.199 VDC

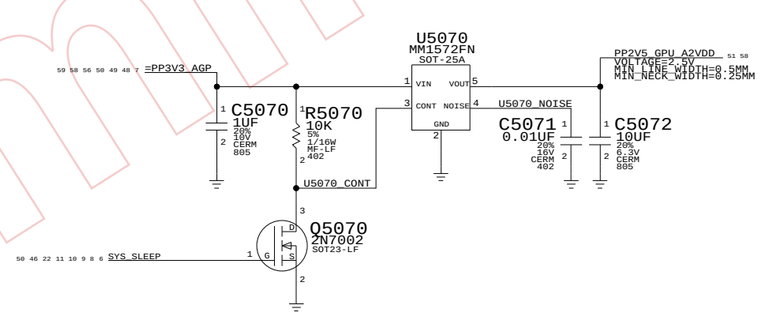
PEAK CURRENT OF TOTAL RAILS
5A WITH RV351LE



GPU 1.8V VREG

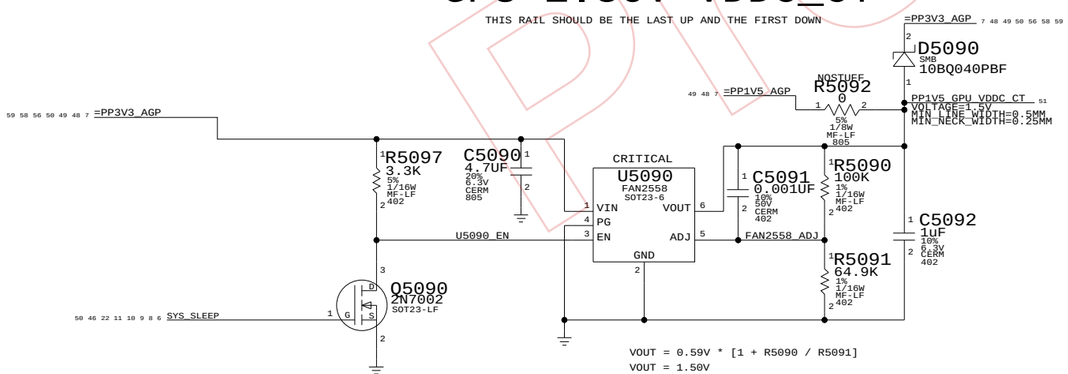
GPU 2.5V A2VDD





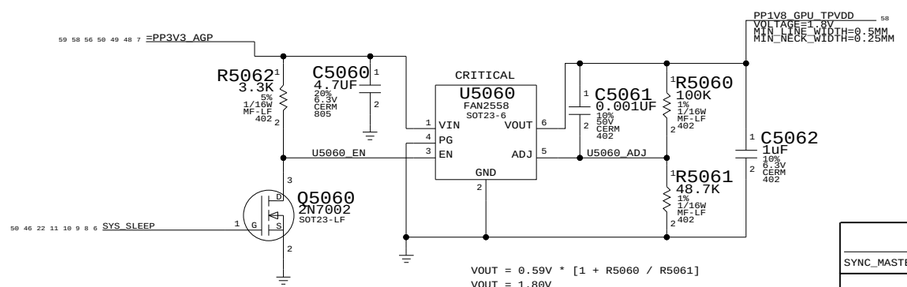
GPU 1.50V VDDC_CT

THIS RAIL SHOULD BE THE LAST UP AND THE FIRST DOWN



VOUT = 0.59V * [1 + R5090 / R5091]
VOUT = 1.50V

GPU 1.80V TPVDD



VOUT = 0.59V * [1 + R5060 / R5061]
VOUT = 1.80V

POWER SEQUENCING FOR RV351: =PP3V3_AGP > PP2V5_GPU > PPVCORE_GPU > VDDC_CT
PP2V5_GPU_A2VDD > PP1V8_GPU
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER

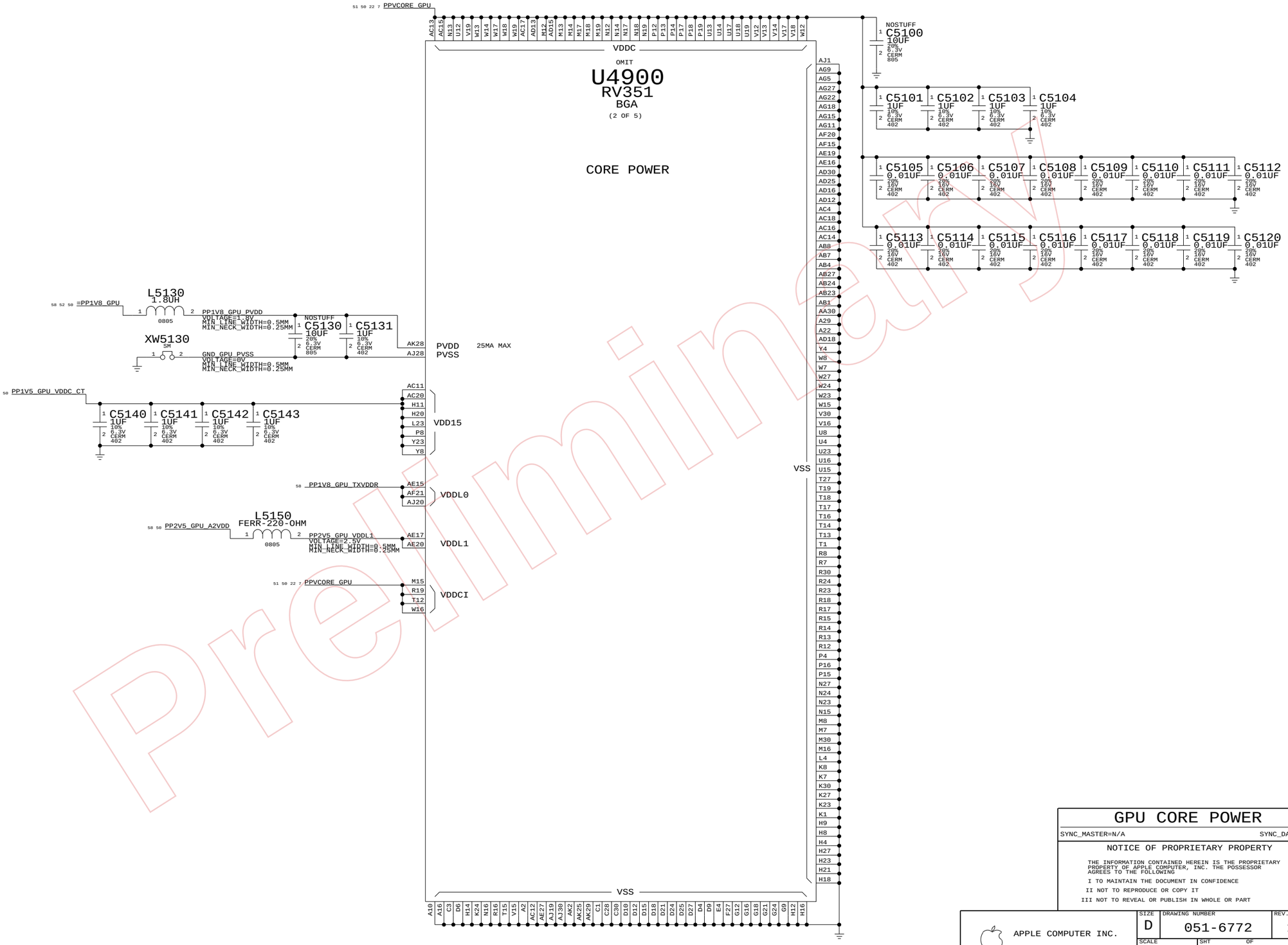
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

GRAPHICS VREGS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 50	OF 102


51 50 22 7 PPVCORE_GPU
VDDC
OMIT
U4900
RV351
BGA
(2 OF 5)
CORE POWER
NOSTUFF C5100 10UF 20% 6.3V CERM 805
C5101 1UF 10% 6.3V CERM 402
C5102 1UF 10% 6.3V CERM 402
C5103 1UF 10% 6.3V CERM 402
C5104 1UF 10% 6.3V CERM 402
C5105 0.01UF 20% 16V CERM 402
C5106 0.01UF 20% 16V CERM 402
C5107 0.01UF 20% 16V CERM 402
C5108 0.01UF 20% 16V CERM 402
C5109 0.01UF 20% 16V CERM 402
C5110 0.01UF 20% 16V CERM 402
C5111 0.01UF 20% 16V CERM 402
C5112 0.01UF 20% 16V CERM 402
C5113 0.01UF 20% 16V CERM 402
C5114 0.01UF 20% 16V CERM 402
C5115 0.01UF 20% 16V CERM 402
C5116 0.01UF 20% 16V CERM 402
C5117 0.01UF 20% 16V CERM 402
C5118 0.01UF 20% 16V CERM 402
C5119 0.01UF 20% 16V CERM 402
C5120 0.01UF 20% 16V CERM 402
58 52 50 =PP1V8_GPU
L5130 1.8UH 0805
PP1V8_GPU_PVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
XW5130 SM
GND_GPU_PVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
NOSTUFF C5130 10UF 20% 6.3V CERM 805
C5131 1UF 10% 6.3V CERM 402
AK28 PVDD 25MA MAX
AJ28 PVSS
50 PP1V5_GPU_VDDC_CT
C5140 1UF 10% 6.3V CERM 402
C5141 1UF 10% 6.3V CERM 402
C5142 1UF 10% 6.3V CERM 402
C5143 1UF 10% 6.3V CERM 402
AC11 AC20 H11 H20 L23 P8 Y23 Y8 VDD15
58 PP1V8_GPU_TXVDDR
AE15 AF21 AJ20 VDDL0
L5150 FERR-220-OHM 0805
58 50 PP2V5_GPU_A2VDD
PP2V5_GPU_VDDL1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
AE17 AE20 VDDL1
51 50 22 7 PPVCORE_GPU
M15 R19 T12 W16 VDDCI
AJ1 AG9 AG5 AG27 AG22 AG18 AG15 AG11 AF20 AF15 AE19 AE16 AD30 AD25 AD16 AD12 AC4 AC18 AC16 AC14 AB8 AB7 AB4 AB27 AB24 AB23 AB1 AA30 A29 A22 AD18 Y4 W8 W7 W27 W24 W23 W15 V30 V16 U8 U4 U23 U16 U15 T27 T19 T18 T17 T16 T14 T13 T1 R8 R7 R30 R24 R23 R18 R17 R15 R14 R13 R12 P4 P16 P15 N27 N24 N23 N15 M8 M7 M30 M16 L4 K8 K7 K30 K27 K23 K1 H9 H8 H4 H27 H23 H21 H18 VSS
A10 A16 C3 D6 H14 K24 N16 R16 T15 V15 A2 AC12 AE27 AJ19 AJ30 AK2 AK25 AK29 C1 C28 C30 D10 D12 D15 D18 D21 D24 D25 D27 D4 D9 E4 F27 G12 G16 G18 G21 G24 G9 H12 H16 VSS
Preliminary
GPU CORE POWER
SYNC_MASTER=N/A
SYNC_DATE=N/A
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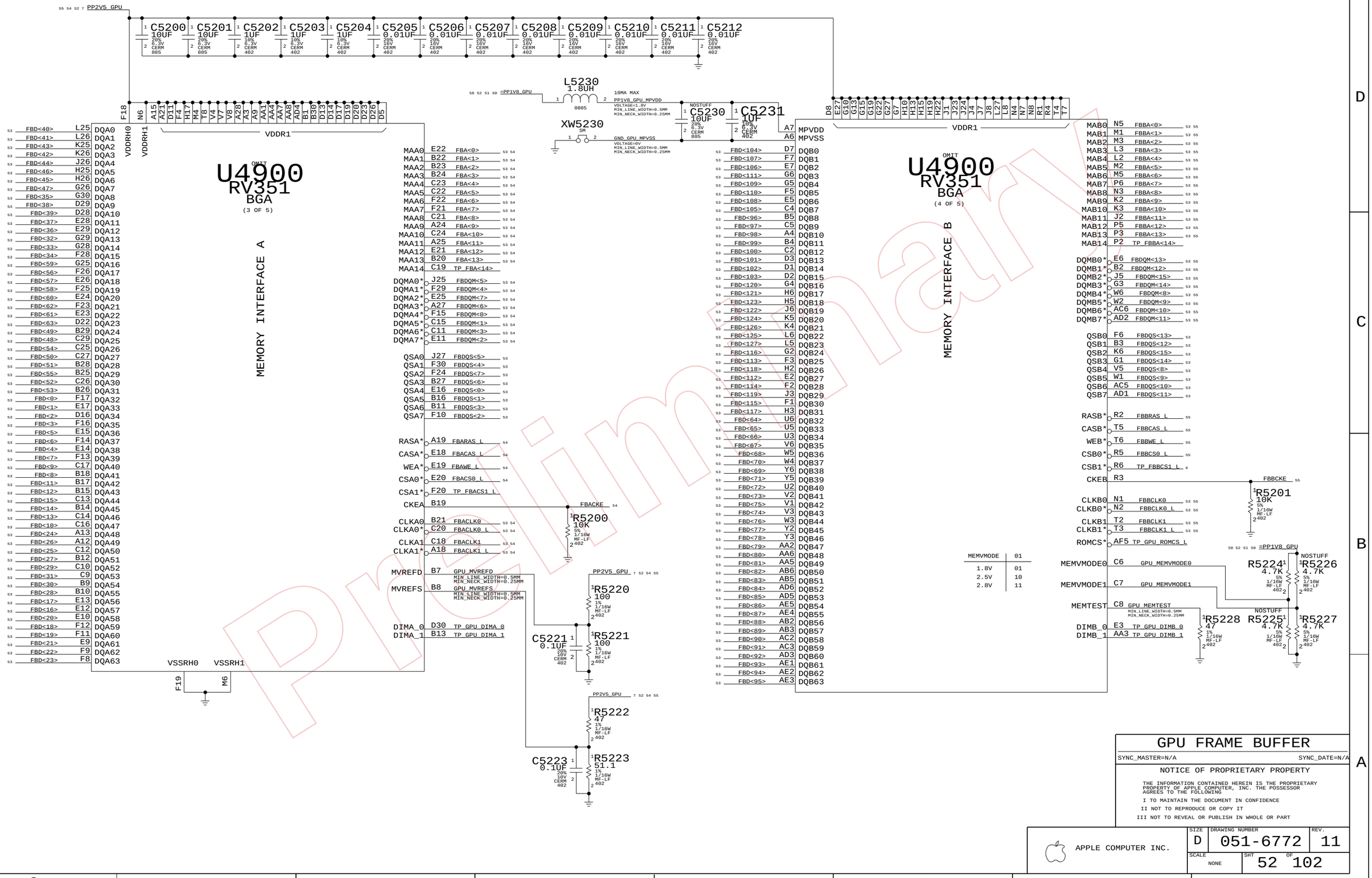
SHT 51 OF 102


PP2V5_GPU
C5200 10UF 20% 6.3V CERM 805
C5201 10UF 20% 6.3V CERM 805
C5202 1UF 10% 6.3V CERM 402
C5203 1UF 10% 6.3V CERM 402
C5204 1UF 10% 6.3V CERM 402
C5205 0.01UF 20% 16V CERM 402
C5206 0.01UF 20% 16V CERM 402
C5207 0.01UF 20% 16V CERM 402
C5208 0.01UF 20% 16V CERM 402
C5209 0.01UF 20% 16V CERM 402
C5210 0.01UF 20% 16V CERM 402
C5211 0.01UF 20% 16V CERM 402
C5212 0.01UF 20% 16V CERM 402
L5230 1.8UH 10MA MAX 0805
=PP1V8_GPU
PP1V8_GPU_MPVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
XW5230 SM
GND_GPU_MPVSS
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
NOSTUFF C5230 10UF 20% 6.3V CERM 805
C5231 1UF 10% 6.3V CERM 402
VDDR1
U4900 RV351 BGA (3 OF 5) OMIT
MEMORY INTERFACE A
DQA0 DQA1 DQA2 DQA3 DQA4 DQA5 DQA6 DQA7 DQA8 DQA9 DQA10 DQA11 DQA12 DQA13 DQA14 DQA15 DQA16 DQA17 DQA18 DQA19 DQA20 DQA21 DQA22 DQA23 DQA24 DQA25 DQA26 DQA27 DQA28 DQA29 DQA30 DQA31 DQA32 DQA33 DQA34 DQA35 DQA36 DQA37 DQA38 DQA39 DQA40 DQA41 DQA42 DQA43 DQA44 DQA45 DQA46 DQA47 DQA48 DQA49 DQA50 DQA51 DQA52 DQA53 DQA54 DQA55 DQA56 DQA57 DQA58 DQA59 DQA60 DQA61 DQA62 DQA63
VDDRH0 VDDRH1
VSSRH0 VSSRH1
MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14
DQMA0* DQMA1* DQMA2* DQMA3* DQMA4* DQMA5* DQMA6* DQMA7*
QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
RASA* CASA* WEA* CSA0* CSA1*
CKEA
CLKA0 CLKA0* CLKA1 CLKA1*
MVREFD MVREFS
DIMA_0 DIMA_1
R5200 10K 5% 1/16W MF-LF 402
R5220 100 1% 1/16W MF-LF 402
R5221 100 1% 1/16W MF-LF 402
C5221 0.1UF 20% 10V CERM 402
R5222 47 1% 1/16W MF-LF 402
R5223 51.1 1% 1/16W MF-LF 402
C5223 0.1UF 20% 10V CERM 402
U4900 RV351 BGA (4 OF 5) OMIT
MEMORY INTERFACE B
MPVDD MPVSS
DQB0 DQB1 DQB2 DQB3 DQB4 DQB5 DQB6 DQB7 DQB8 DQB9 DQB10 DQB11 DQB12 DQB13 DQB14 DQB15 DQB16 DQB17 DQB18 DQB19 DQB20 DQB21 DQB22 DQB23 DQB24 DQB25 DQB26 DQB27 DQB28 DQB29 DQB30 DQB31 DQB32 DQB33 DQB34 DQB35 DQB36 DQB37 DQB38 DQB39 DQB40 DQB41 DQB42 DQB43 DQB44 DQB45 DQB46 DQB47 DQB48 DQB49 DQB50 DQB51 DQB52 DQB53 DQB54 DQB55 DQB56 DQB57 DQB58 DQB59 DQB60 DQB61 DQB62 DQB63
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13 MAB14
DQMB0* DQMB1* DQMB2* DQMB3* DQMB4* DQMB5* DQMB6* DQMB7*
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
RASB* CASB* WEB* CSB0* CSB1* CKEB
CLKB0 CLKB0* CLKB1 CLKB1*
ROMCS*
MEMVMODE0 MEMVMODE1
MEMTEST
DIMB_0 DIMB_1
MEMVMODE 01
1.8V 01
2.5V 10
2.8V 11
R5201 10K 5% 1/16W MF-LF 402
NOSTUFF R5224 4.7K 5% 1/16W MF-LF 402
R5226 4.7K 5% 1/16W MF-LF 402
R5228 47 1% 1/16W MF-LF 402
NOSTUFF R5225 4.7K 5% 1/16W MF-LF 402
R5227 4.7K 5% 1/16W MF-LF 402
GPU FRAME BUFFER
SYNC_MASTER=N/A
SYNC_DATE=N/A
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REV. 11
SCALE NONE
SHT 52 OF 102

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

FBD<31>	22	1	8	RP5320	RFBD<31>	53 52	53 54
FBD<30>	22	2	7	RP5320	RFBD<30>	53 52	6 53 54
FBD<29>	22	3	6	RP5320	RFBD<29>	53 52	6 53 54
FBD<28>	22	4	5	RP5320	RFBD<28>	53 52	6 53 54
FBD<27>	22	1	8	RP5321	RFBD<27>	53 52	53 54
FBD<26>	22	2	7	RP5321	RFBD<26>	53 52	6 53 54
FBD<25>	22	3	6	RP5321	RFBD<25>	53 52	6 53 54
FBD<24>	22	4	5	RP5321	RFBD<24>	53 52	6 53 54
FBD<0>	22	1	8	RP5322	RFBD<0>	53 52	53 54
FBD<1>	22	2	7	RP5322	RFBD<1>	53 52	6 53 54
FBD<2>	22	3	6	RP5322	RFBD<2>	53 52	6 53 54
FBD<3>	22	4	5	RP5322	RFBD<3>	53 52	6 53 54
FBD<17>	22	1	8	RP5323	RFBD<17>	53 52	53 54
FBD<16>	22	2	7	RP5323	RFBD<16>	53 52	6 53 54
FBD<18>	22	3	6	RP5323	RFBD<18>	53 52	6 53 54
FBD<19>	22	4	5	RP5323	RFBD<19>	53 52	6 53 54
FBD<15>	22	1	8	RP5324	RFBD<15>	53 52	53 54
FBD<14>	22	2	7	RP5324	RFBD<14>	53 52	6 53 54
FBD<13>	22	3	6	RP5324	RFBD<13>	53 52	6 53 54
FBD<12>	22	4	5	RP5324	RFBD<12>	53 52	6 53 54
FBD<10>	22	1	8	RP5325	RFBD<10>	53 52	53 54
FBD<11>	22	2	7	RP5325	RFBD<11>	53 52	6 53 54
FBD<9>	22	3	6	RP5325	RFBD<9>	53 52	6 53 54
FBD<8>	22	4	5	RP5325	RFBD<8>	53 52	6 53 54
FBD<5>	22	1	8	RP5326	RFBD<5>	53 52	53 54
FBD<6>	22	2	7	RP5326	RFBD<6>	53 52	6 53 54
FBD<4>	22	3	6	RP5326	RFBD<4>	53 52	6 53 54
FBD<7>	22	4	5	RP5326	RFBD<7>	53 52	6 53 54
FBD<20>	22	1	8	RP5327	RFBD<20>	53 52	53 54
FBD<21>	22	2	7	RP5327	RFBD<21>	53 52	6 53 54
FBD<22>	22	3	6	RP5327	RFBD<22>	53 52	6 53 54
FBD<23>	22	4	5	RP5327	RFBD<23>	53 52	6 53 54

FBD<32>	22	3	6	RP5328	RFBD<32>	53 52	6 53 54
FBD<33>	22	4	5	RP5328	RFBD<33>	53 52	6 53 54
FBD<34>	22	1	8	RP5328	RFBD<34>	53 52	53 54
FBD<35>	22	2	7	RP5328	RFBD<35>	53 52	6 53 54
FBD<36>	22	4	5	RP5316	RFBD<36>	53 52	6 53 54
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FBD<39>	22	1	8	RP5316	RFBD<39>	53 52	53 54
FBD<40>	22	2	7	RP5329	RFBD<40>	53 52	6 53 54
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FBD<48>	22	4	5	RP5331	RFBD<48>	53 52	6 53 54
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FBD<56>	22	1	8	RP5301	RFBD<56>	53 52	53 54
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FBD<58>	22	4	5	RP5301	RFBD<58>	53 52	53 54
FBD<59>	22	3	6	RP5301	RFBD<59>	53 52	53 54
FBD<60>	22	1	8	RP5302	RFBD<60>	53 52	53 54
FBD<61>	22	3	6	RP5302	RFBD<61>	53 52	53 54
FBD<62>	22	2	7	RP5302	RFBD<62>	53 52	53 54
FBD<63>	22	4	5	RP5302	RFBD<63>	53 52	53 54

FBDQS<0>	MAKE_BASE=TRUE	RFBDQS<0>	53 52 54
FBDQS<1>	MAKE_BASE=TRUE	RFBDQS<1>	53 52 54
FBDQS<2>	MAKE_BASE=TRUE	RFBDQS<2>	53 52 54
FBDQS<3>	MAKE_BASE=TRUE	RFBDQS<3>	53 52 54
FBDQS<4>	MAKE_BASE=TRUE	RFBDQS<4>	53 52 54
FBDQS<5>	MAKE_BASE=TRUE	RFBDQS<5>	53 52 54
FBDQS<6>	MAKE_BASE=TRUE	RFBDQS<6>	53 52 54
FBDQS<7>	MAKE_BASE=TRUE	RFBDQS<7>	53 52 54

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

54 53 52 FBACLK0
R5320 56.2 1% 1/10W MF-LF 402
FBACLK0_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R5321 56.2 1% 1/10W MF-LF 402
C5321 0.01UF 20% 16V CERM 402
54 53 52 FBACLK0_L

54 53 52 FBACLK1
R5322 56.2 1% 1/10W MF-LF 402
FBACLK1_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R5323 56.2 1% 1/10W MF-LF 402
C5323 0.01UF 20% 16V CERM 402
54 53 52 FBACLK1_L

FRAME BUFFER B TERMINATION

FBD<64>	GPU128BIT	22	1	8	RP5310	RFBD<64>	53 52	53 55
FBD<65>	GPU128BIT	22	2	7	RP5310	RFBD<65>	53 52	53 55
FBD<66>	GPU128BIT	22	3	6	RP5310	RFBD<66>	53 52	53 55
FBD<67>	GPU128BIT	22	4	5	RP5310	RFBD<67>	53 52	53 55
FBD<84>	GPU128BIT	22	1	8	RP5309	RFBD<84>	53 52	53 55
FBD<85>	GPU128BIT	22	2	7	RP5309	RFBD<85>	53 52	53 55
FBD<86>	GPU128BIT	22	3	6	RP5309	RFBD<86>	53 52	53 55
FBD<87>	GPU128BIT	22	4	5	RP5309	RFBD<87>	53 52	53 55
FBD<72>	GPU128BIT	22	4	5	RP5319	RFBD<72>	53 52	53 55
FBD<73>	GPU128BIT	22	3	6	RP5319	RFBD<73>	53 52	53 55
FBD<75>	GPU128BIT	22	2	7	RP5319	RFBD<75>	53 52	53 55
FBD<74>	GPU128BIT	22	1	8	RP5319	RFBD<74>	53 52	53 55
FBD<68>	GPU128BIT	22	1	8	RP5308	RFBD<68>	53 52	53 55
FBD<70>	GPU128BIT	22	2	7	RP5308	RFBD<70>	53 52	53 55
FBD<69>	GPU128BIT	22	3	6	RP5308	RFBD<69>	53 52	53 55
FBD<71>	GPU128BIT	22	4	5	RP5308	RFBD<71>	53 52	53 55
FBD<80>	GPU128BIT	22	1	8	RP5307	RFBD<80>	53 52	53 55
FBD<81>	GPU128BIT	22	2	7	RP5307	RFBD<81>	53 52	53 55
FBD<82>	GPU128BIT	22	3	6	RP5307	RFBD<82>	53 52	53 55
FBD<83>	GPU128BIT	22	4	5	RP5307	RFBD<83>	53 52	53 55
FBD<76>	GPU128BIT	22	4	5	RP5317	RFBD<76>	53 52	53 55
FBD<77>	GPU128BIT	22	3	6	RP5317	RFBD<77>	53 52	53 55
FBD<78>	GPU128BIT	22	2	7	RP5317	RFBD<78>	53 52	53 55
FBD<79>	GPU128BIT	22	1	8	RP5317	RFBD<79>	53 52	53 55
FBD<91>	GPU128BIT	22	1	8	RP5318	RFBD<91>	53 52	53 55
FBD<90>	GPU128BIT	22	2	7	RP5318	RFBD<90>	53 52	53 55
FBD<89>	GPU128BIT	22	3	6	RP5318	RFBD<89>	53 52	53 55
FBD<88>	GPU128BIT	22	4	5	RP5318	RFBD<88>	53 52	53 55
FBD<95>	GPU128BIT	22	1	8	RP5303	RFBD<95>	53 52	53 55
FBD<94>	GPU128BIT	22	2	7	RP5303	RFBD<94>	53 52	53 55
FBD<93>	GPU128BIT	22	3	6	RP5303	RFBD<93>	53 52	53 55
FBD<92>	GPU128BIT	22	4	5	RP5303	RFBD<92>	53 52	53 55

FBD<96>	GPU128BIT	22	4	5	RP5315	RFBD<96>	53 52	53 55
FBD<97>	GPU128BIT	22	3	6	RP5315	RFBD<97>	53 52	53 55
FBD<98>	GPU128BIT	22	2	7	RP5315	RFBD<98>	53 52	53 55
FBD<99>	GPU128BIT	22	1	8	RP5315	RFBD<99>	53 52	53 55
FBD<100>	GPU128BIT	22	4	5	RP5314	RFBD<100>	53 52	53 55
FBD<101>	GPU128BIT	22	3	6	RP5314	RFBD<101>	53 52	53 55
FBD<102>	GPU128BIT	22	2	7	RP5314	RFBD<102>	53 52	53 55
FBD<103>	GPU128BIT	22	1	8	RP5314	RFBD<103>	53 52	53 55
FBD<104>	GPU128BIT	22	1	8	RP5312	RFBD<104>	53 52	53 55
FBD<105>	GPU128BIT	22	2	7	RP5312	RFBD<105>	53 52	53 55
FBD<106>	GPU128BIT	22	3	6	RP5312	RFBD<106>	53 52	53 55
FBD<107>	GPU128BIT	22	4	5	RP5312	RFBD<107>	53 52	53 55
FBD<108>	GPU128BIT	22	1	8	RP5313	RFBD<108>	53 52	53 55
FBD<109>	GPU128BIT	22	2	7	RP5313	RFBD<109>	53 52	53 55
FBD<110>	GPU128BIT	22	3	6	RP5313	RFBD<110>	53 52	53 55
FBD<111>	GPU128BIT	22	4	5	RP5313	RFBD<111>	53 52	53 55
FBD<112>	GPU128BIT	22	4	5	RP5311	RFBD<112>	53 52	53 55
FBD<113>	GPU128BIT	22	3	6	RP5311	RFBD<113>	53 52	53 55
FBD<114>	GPU128BIT	22	2	7	RP5311	RFBD<114>	53 52	53 55
FBD<115>	GPU128BIT	22	1	8	RP5311	RFBD<115>	53 52	53 55
FBD<116>	GPU128BIT	22	4	5	RP5306	RFBD<116>	53 52	53 55
FBD<117>	GPU128BIT	22	3	6	RP5306	RFBD<117>	53 52	53 55
FBD<118>	GPU128BIT	22	2	7	RP5306	RFBD<118>	53 52	53 55
FBD<119>	GPU128BIT	22	1	8	RP5306	RFBD<119>	53 52	53 55
FBD<120>	GPU128BIT	22	1	8	RP5304	RFBD<120>	53 52	53 55
FBD<121>	GPU128BIT	22	2	7	RP5304	RFBD<121>	53 52	53 55
FBD<122>	GPU128BIT	22	4	5	RP5304	RFBD<122>	53 52	53 55
FBD<123>	GPU128BIT	22	3	6	RP5304	RFBD<123>	53 52	53 55
FBD<124>	GPU128BIT	22	1	8	RP5305	RFBD<124>	53 52	53 55
FBD<125>	GPU128BIT	22	3	6	RP5305	RFBD<125>	53 52	53 55
FBD<126>	GPU128BIT	22	2	7	RP5305	RFBD<126>	53 52	53 55
FBD<127>	GPU128BIT	22	4	5	RP5305	RFBD<127>	53 52	53 55

FBDQS<8>	MAKE_BASE=TRUE	RFBDQS<8>	53 52 55
FBDQS<9>	MAKE_BASE=TRUE	RFBDQS<9>	53 52 55
FBDQS<10>	MAKE_BASE=TRUE	RFBDQS<10>	53 52 55
FBDQS<11>	MAKE_BASE=TRUE	RFBDQS<11>	53 52 55
FBDQS<12>	MAKE_BASE=TRUE	RFBDQS<12>	53 52 55
FBDQS<13>	MAKE_BASE=TRUE	RFBDQS<13>	53 52 55
FBDQS<14>	MAKE_BASE=TRUE	RFBDQS<14>	53 52 55
FBDQS<15>	MAKE_BASE=TRUE	RFBDQS<15>	53 52 55

55 53 52 FBBCLK0
R5324 56.2 1% 1/10W MF-LF 402
FBBCLK0_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R5325 56.2 1% 1/10W MF-LF 402
C5325 0.01UF 20% 16V CERM 402
55 53 52 FBBCLK0_L

55 53 52 FBBCLK1
R5326 56.2 1% 1/10W MF-LF 402
FBBCLK1_TERM MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
R5327 56.2 1% 1/10W MF-LF 402
C5327 0.01UF 20% 16V CERM 402
55 53 52 FBBCLK1_L

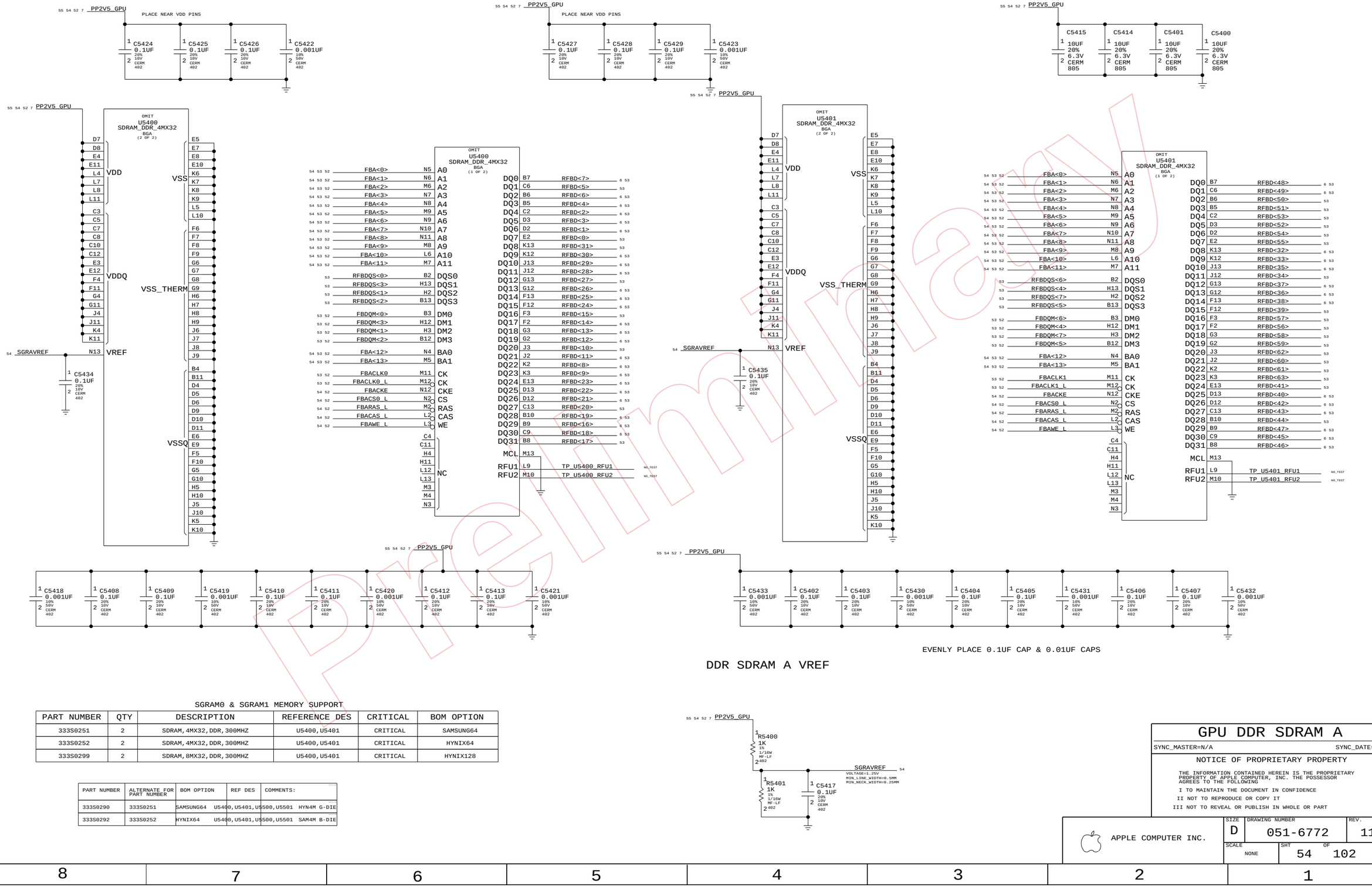
	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
53 52 FBD<127..0>		GPU_FB	GPU_FB		4434
55 54 53 6 RFBD<127..0>		GPU_FB	GPU_FB		4435
54 52 FBA<13..0>		GPU_FB	GPU_FB		4436
55 52 FBBA<13..0>		GPU_FB	GPU_FB		4437
55 54 52 FBDQM<15..0>		GPU_FB	GPU_FB		4438
53 52 FBDQS<15..0>		GPU_FB	GPU_FB		4439
54 53 52 FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0	4440
54 53 52 FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0	4441
54 53 52 FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1	4442
54 53 52 FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1	4443
55 53 52 FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0	4444
55 53 52 FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0	4445
55 53 52 FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1	4446
55 53 52 FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1	4447

FB TERMINATION

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 53 OF 102	



EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

DDR SDRAM A VREF

SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX64
333S0299	2	SDRAM,8MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX128

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0290	333S0251	SAMSUNG64	U5400,U5401,U5500,U5501	HYN4M G-DIE
333S0292	333S0252	HYNIX64	U5400,U5401,U5500,U5501	SAM4M B-DIE

GPU DDR SDRAM A

SYNC_MASTER=N/A SYNC_DATE=N/A

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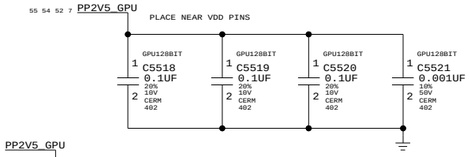
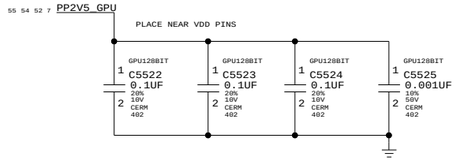
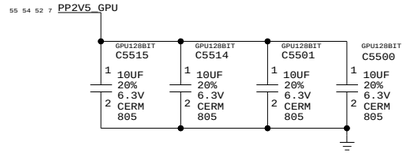
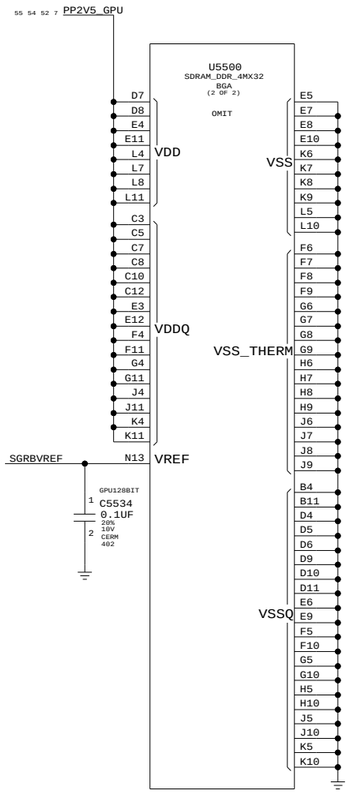
SIZE	DRAWING NUMBER	REV.
D	051-6772	11

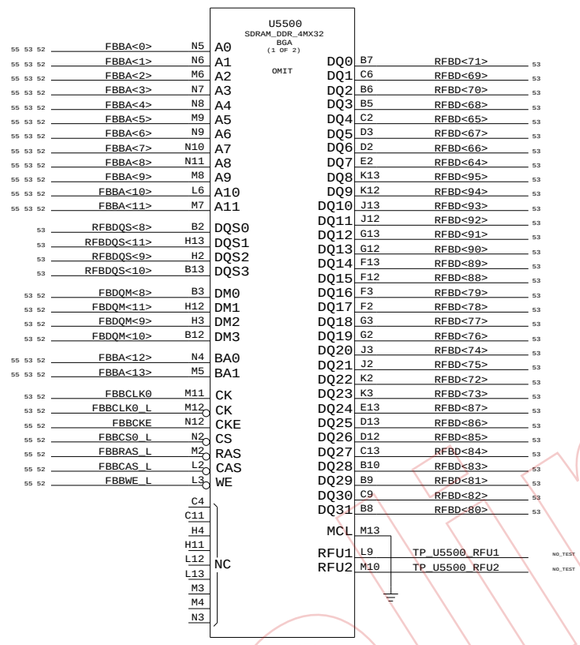
SCALE: NONE SHT 54 OF 102

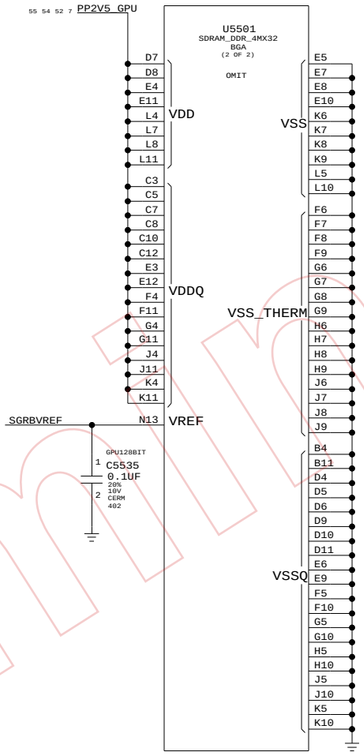


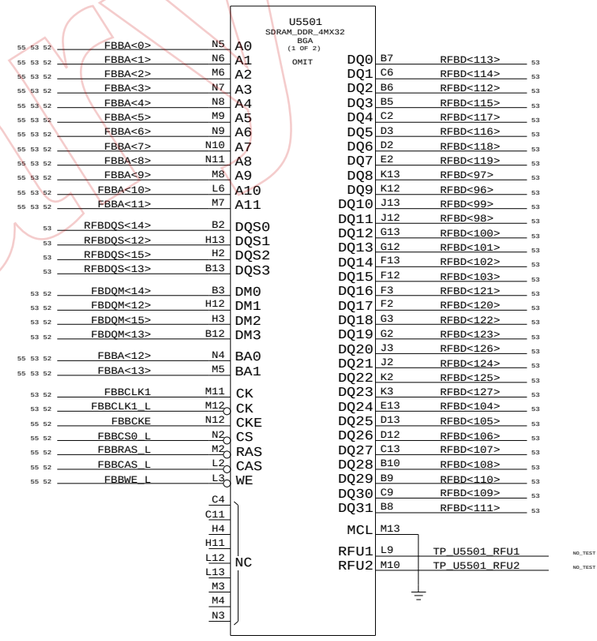


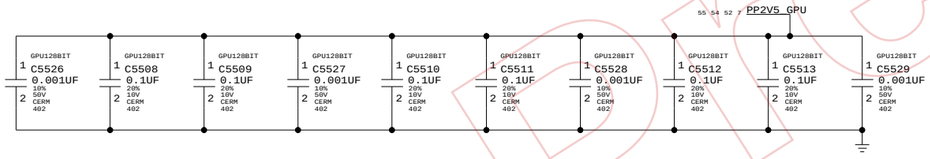




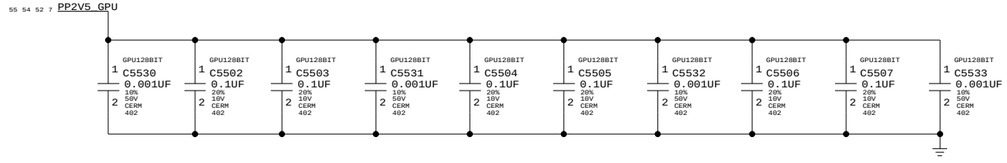




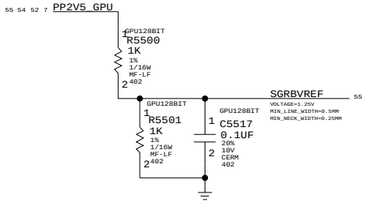




DDR SDRAM B VREF



EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX64
333S0299	2	SDRAM,8MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX128

GPU DDR SDRAM B

SYNC_MASTER=N/A SYNC_DATE=N/A

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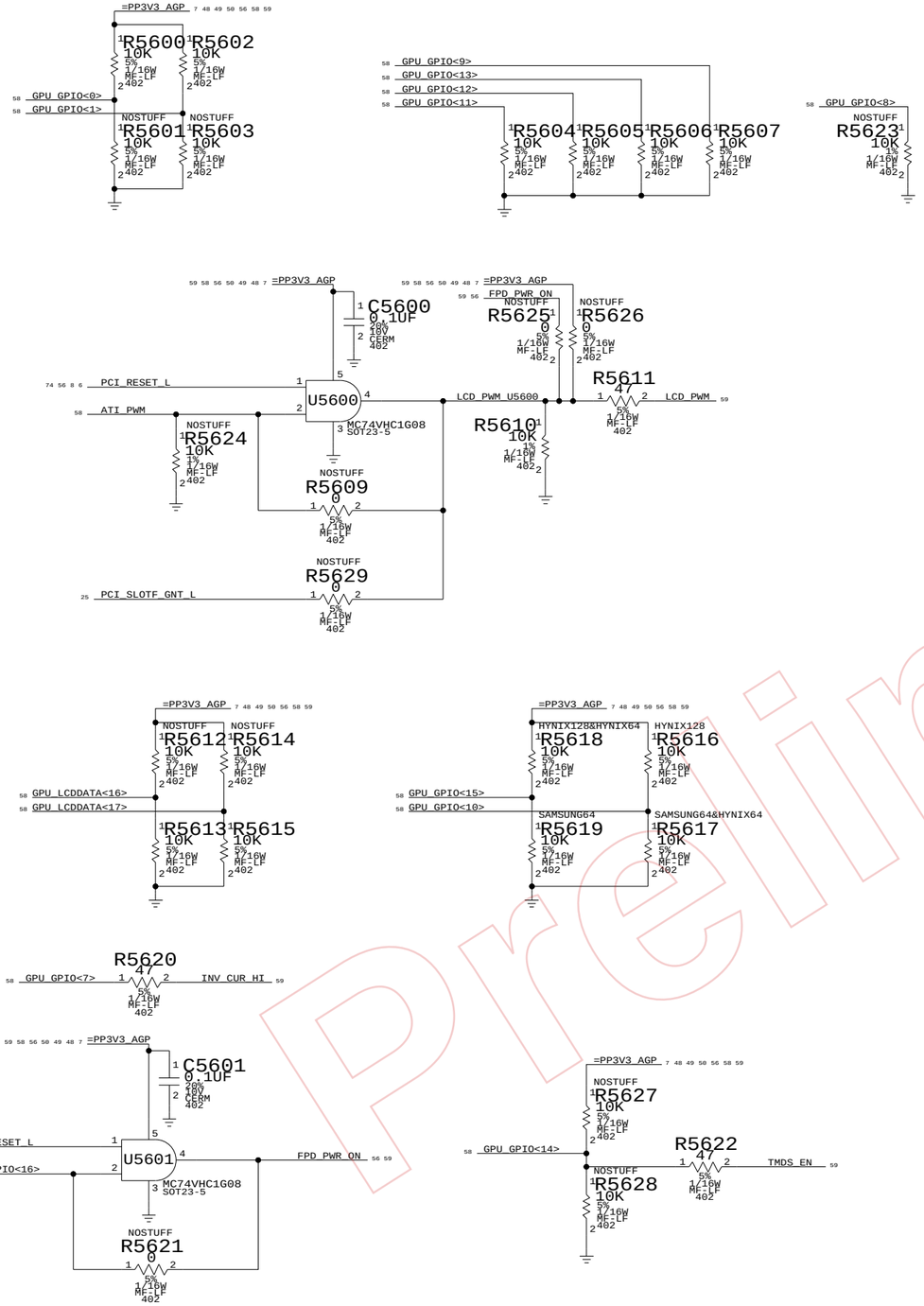
SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 55 OF 102	



APPLE GPIO	ATI STRAP	PIN	DESCRIPTION	DEFAULT
	AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK) 00 - REFCLK SLIGHTLY EARLIER THEN FEEDBACK 01 - REFCLK 1 TAP EARLIER THEN FEEDBACK 10 - REFCLK 1 TAP LATER THEN FEEDBACK 11 - REFCLK 2 TAPS EARLIER THEN FEEDBACK CLOCK (ATI RECOMMENDED)	00 INTERNAL PULL-DOWN
	X1CLK_SKWE(1:0)	GPIO(3:2)	CLOCK PHASE ADJUSTMENT BETWEEN X1 CLK AND X2CLK 00 - 0 TAP DELAY	00 INTERNAL PULL-DOWN
	ROMIDCFG(3:0)	GPIO(9,13:11)	IF NO ROM ATTACHED, CONTROLS CHIP IDS. IF ROM- IDENTIFIES TYPE 0X0X - NO ROM, CHG_ID=0	
	ID_DISABLE	GPIO(8)	STRAP 0 - NORMAL OPERATION 1 - SHUTS THE CHIP DOWN BY NOT RESPONDING TO ANY CONFIG CYCLES	0 INTERNAL PULL-DOWN
	BUSCFG(2:0)	GPIO(6:4)	AGP8X_DETB BUSCFG[2:0] AGPMODE SIGNALING IDSEL 0 000 AGP8X 0.8V AD16	000 INTERNAL PULL-DOWN
	MULTIFUNC(1:0)	LCDDATA(17:16)	MULTI-FUNCTION DEVICE SELECT 00 - SINGLE FUNCTION DEVICE. 01 - TWO FUNCTION DEVICE. NO AGP IN EITHER FUNCTION 10 - TWO FUNCTION DEVICE. AGP ONLY IN FUNCTION 0 11 - TWO FUNCTION DEVICE. AGP IN BOTH FUNCTIONS IF BUSCFG PIN BASED STRAPS ARE SET TO PCI, THEN AGP WILL NOT BE ENABLED IN ANY FUNCTION.	00
	MEMSTRAP(1:0)	GPU_GPIO<15,10>	00 - SAMSUNG 4MX32 01 - UNDEFINED 10 - HYNIX 4MX32 11 - HYNIX 8MX32	
INV_CUR_HI		GPIO<7>	OUTPUT: GPU READS PANEL ID AND SETS THIS BIT ACCORDINGLY FOR REFERENCE ONLY, ACTIONS COME FROM BOOTROM SYSTEM / PANEL ID / INV_CUR_HI Q45 A / 0X9C27 / 1 0X9C38 / 0 Q45 B / 0X9C3A / 1 0X9C39 / 0 Q45 C / TBD / 1 TBD / 0 Q45 D / 0X9C3A / 1 Q45 A/B SUPPORT IS FOR DEVELOPMENT	
FPD_PWR_ON		GPIO<16>	OUTPUT: PANEL POWER SEQUENCING	
TMDS_EN		GPIO<14>	INPUT: PANEL POWER SEQUENCING	

GPU STRAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 56 OF 102	

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA_37P5	GPU_VGA_37P5	
	GPU_VGA_37P5	GPU_VGA_37P5	
	GPU_VGA_37P5	GPU_VGA_37P5	

TMDS_CKP, TMDS_CKM, TMDS_D0P, TMDS_D0M, TMDS_D1P, TMDS_D1M, TMDS_D2P, TMDS_D2M, ANALOG_GRN, ANALOG_RED, ANALOG_BLU

=PP3V3_AGP

U4900 RV351 BGA (5 OF 5)

VDDR3 OMIT: AC19 AC21 AC22 AC8 AD19 AD21 AD22 AD7

VDDR4: AC10 AC9 AD10 AD9 AG7

GPIO: GPU_GPIO<0> AJ5, GPU_GPIO<1> AH5, TP_GPU_GPIO<2> AJ4, TP_GPU_GPIO<3> AK4, TP_GPU_GPIO<4> AH4, TP_GPU_GPIO<5> AF4, TP_GPU_GPIO<6> AJ3, GPU_GPIO<7> AK3, GPU_GPIO<8> AH3, GPU_GPIO<9> AJ2, GPU_GPIO<10> AH2, GPU_GPIO<11> AH1, GPU_GPIO<12> AG3, GPU_GPIO<13> AG1, GPU_GPIO<14> AG2, GPU_GPIO<15> AF3, GPU_GPIO<16> AF2

EXTERNAL TMDS / LCDDATA: AH6 TP_GPU_LCDDATA<0>, AJ6 TP_GPU_LCDDATA<1>, AK6 TP_GPU_LCDDATA<2>, AH7 TP_GPU_LCDDATA<3>, AK7 TP_GPU_LCDDATA<4>, AJ7 TP_GPU_LCDDATA<5>, AH8 TP_GPU_LCDDATA<6>, AJ8 TP_GPU_LCDDATA<7>, AH9 TP_GPU_LCDDATA<8>, AJ9 TP_GPU_LCDDATA<9>, AK9 TP_GPU_LCDDATA<10>, AH10 TP_GPU_LCDDATA<11>, AE6 TP_GPU_LCDDATA<12>, AG6 TP_GPU_LCDDATA<13>, AF6 TP_GPU_LCDDATA<14>, AE7 TP_GPU_LCDDATA<15>, AF7 GPU_LCDDATA<16>, AE8 GPU_LCDDATA<17>, AG8 TP_GPU_LCDDATA<18>, AF8 TP_GPU_LCDDATA<19>, AE9 TP_GPU_LCDDATA<20>, AF9 TP_GPU_LCDDATA<21>, AG10 TP_GPU_LCDDATA<22>, AF10 TP_GPU_LCDDATA<23>

LCDCNTL: AJ10 GPU_LCDCNTL<0>, AK10 GPU_LCDCNTL<1>, AJ11 GPU_LCDCNTL<2>, AH11 GPU_LCDCNTL<3>

DVOMODE AE10

HPD1 AF12 MON_DETECT_R

C5800 10UF 20% 6.3V CERM 805; C5801 1UF 10% 6.3V CERM 402; C5802 1UF 10% 6.3V CERM 402; C5803 1UF 10% 6.3V CERM 402 (NOSTUFF)

Y5800 SM-3 27.000M; C5814 22PF 5% 50V CERM 603; C5815 22PF 5% 50V CERM 603; GPU_CLK27M_XOUT_R

R5814 1M 5% 1/16W MF-LF 402; R5815 249 1% 1/16W MF-LF 402

GPU_CLK27M_XIN AH28, GPU_CLK27M_XOUT AJ29

XTALIN XTALOUT CLK

TEST_MCLK B6, TEST_YCLK E8, PLLTEST NC AE25, TESTEN AH27

TEST

=PP3V3_AGP

R5816 1K 1% 1/16W MF-LF 402; R5817 1K 1% 1/16W MF-LF 402; C5817 0.1UF 20% 10V CERM 402

GPU_DIODE_PLUS AF11, GPU_DIODE_MINUS AE11

DPLUS DMINUS

RSTB_MSK AG29

GPU_VREFG AG4 MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

VREFG

ATI_PWM AF17

NC NO CONNECTS: AF18 AG12 AG16 AG17 AG19 AG20 AH16 AH17 AH19 AH20 AH29

NC: AE12 AE18 AH18 AH30 AJ16 AJ17 AJ18 AJ25 AK16 AK19 AF16

THE FREQUENCY OF THE 20" PIXEL CLOCK IS 119 MHZ

TXVDDR AF13 AF14; TXVSSR AG13 AG14 AH12

TMDS

TXCP AK13 TMDS_CKP, TXCM* AH13 TMDS_CKM, TX0P AH14 TMDS_D0P, TX0M* AJ13 TMDS_D0M, TX1P AH15 TMDS_D1P, TX1M* AJ14 TMDS_D1M, TX2P AK15 TMDS_D2P, TX2M* AJ15 TMDS_D2M

TPVDD AK12 75MA MAX; TPVSS AJ12

DDC2CLK AE13 I2C_GPU_TMDS_SCL, DDC2DATA AE14 I2C_GPU_TMDS_SDA

VDD1DI AE24, VDD2DI AE22, VSS1DI AE23, VSS2DI AE21

DAC1

R AK27 NC, G AJ27 NC, B AJ26 NC, HSYNC AG25 NC, VSYNC AH25

GPU_DAC1_VSYNC NO_TEST=TRUE; DEVELOPMENT R5826 75 1% 1/16W MF-LF 402

RSET AH26

DDC1CLK AF24 NC, DDC1DATA AF25 NC

AUXWIN AF26 NC

STEREOSYNC AG26

GPU_RSET; GPU_STEREOSYNC; MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

R5825 10K 1% 1/16W MF-LF 402; XW5847 SM; R5820 499 1% 1/16W MF-LF 402; GND_GPU_AVSSQ

AVDD AH24, AVSSQ AD24, AVSSN AH23

GND_GPU_AVSSQ AD24

A2VDD AG21 AH21, A2VSSN AH22 AJ21

DAC2

Y_G AJ22 ANALOG_GRN, C_R AJ23 ANALOG_RED, COMP_B AK22 ANALOG_BLU, H2SYNC AJ24 ANALOG_HSYNC, V2SYNC AK24 ANALOG_VSYNC

ROUTE SIGNALS AT 37.5 OHMS

R2SET AK21

R5821 75 1% 1/16W MF-LF 402; R5822 75 1% 1/16W MF-LF 402; R5823 75 1% 1/16W MF-LF 402

DDC3CLK AG23 I2C_GPU_MON_SCL, DDC3DATA AG24 I2C_GPU_MON_SDA

A2VDDQ AF22, A2VSSQ AF23

GPU_R2SET MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

R5824 715 1% 1/16W MF-LF 402

PLACE R5821-3 & FL5900-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

=PP3V3_AGP

RP5810 4.7K 5% 1/16W SM-LF; RP5810 4.7K 5% 1/16W SM-LF; RP5810 4.7K 5% 1/16W SM-LF; RP5810 4.7K 5% 1/16W SM-LF; R5818 10K 5% 1/16W MF-LF 402

R5819 0 5% 1/16W MF-LF 402

MON_DETECT

GPU THERMAL SENSOR

PP3V3_PWRON

DEVELOPMENT C5890 0.1UF 20% 10V CERM 402; DEVELOPMENT C5891 100PF 5% 50V CERM 402; DEVELOPMENT R5891 10K 5% 1/16W MF-LF 402; DEVELOPMENT R5892 10K 5% 1/16W MF-LF 402

U5890 DEVELOPMENT ALERT*/TACH LM63CIMA SOI: VDD, D+, D-, PWM, SMBCLK, SMBDA, GND

U5890_ALERT_L; U5890_PWM; I2C_GPU_DIODE_SCL; I2C_GPU_DIODE_SDA

GPU_DIODE_PLUS; GPU_DIODE_MINUS

DEVELOPMENT C5892 2200PF 5% 50V CERM 603

L5835 FERR-220-OHM 0805 =PP1V8_GPU PP1V8_GPU_TXVDDR VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5835 10UF 20% 6.3V CERM 805; C5836 1UF 10% 6.3V CERM 402; C5837 0.1UF 20% 10V CERM 402

XW5835 SM GND_GPU_TXVSSR VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF L5830 1.8UH 0805 PP1V8_GPU_TPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5830 10UF 20% 6.3V CERM 805; C5831 1UF 10% 6.3V CERM 402; C5832 0.1UF 10% 10V CERM 402; C5833 0.1UF 20% 10V CERM 402

XW5830 SM GND_GPU_TPVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5840 FERR-220-OHM 0805 PP1V8_GPU_VDDDI VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5840 10UF 20% 6.3V CERM 805; C5841 1UF 10% 6.3V CERM 402

XW5840 SM GND_GPU_VSSDI VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5845 FERR-220-OHM 0805 PP1V8_GPU_AVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5845 10UF 20% 6.3V CERM 805; C5846 1UF 10% 6.3V CERM 402

XW5845 SM GND_GPU_AVSSN VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

=PP1V8_GPU; PP2V5_GPU_A2VDD

NOSTUFF C5855 10UF 20% 6.3V CERM 805; C5856 1UF 10% 6.3V CERM 402

XW5855 SM GND_GPU_A2VSSN VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5865 FERR-220-OHM 0805 PP1V8_GPU_A2VDDQ VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5865 10UF 20% 6.3V CERM 805; C5866 1UF 10% 6.3V CERM 402

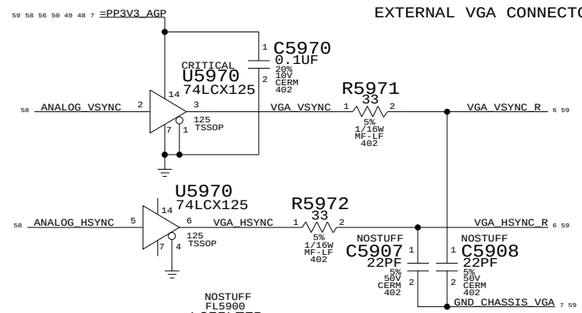
XW5865 SM GND_GPU_A2VSSQ VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

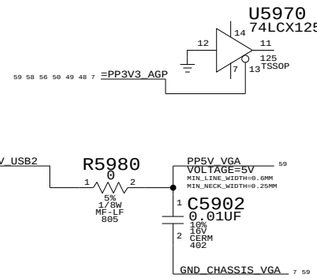
GPU DVI & DACS

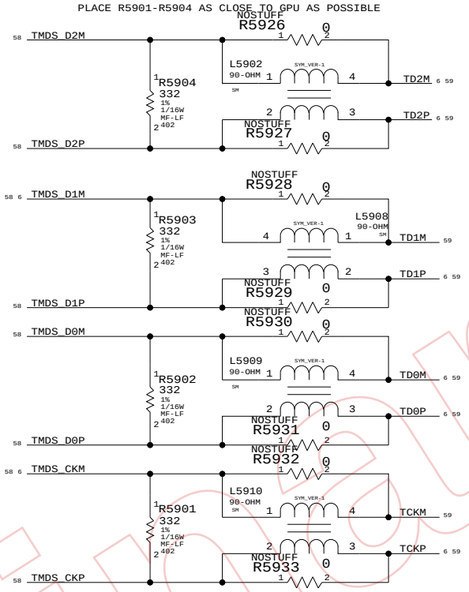
SYNC_MASTER=N/A SYNC_DATE=N/A

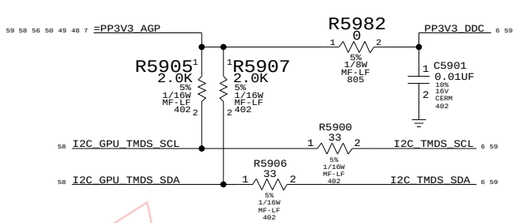
APPLE COMPUTER INC.

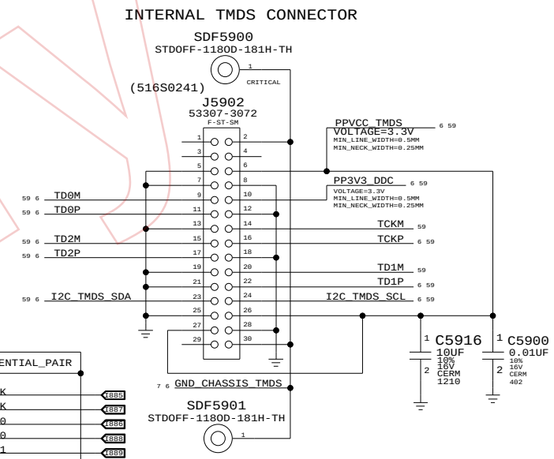
SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 58 OF 102	







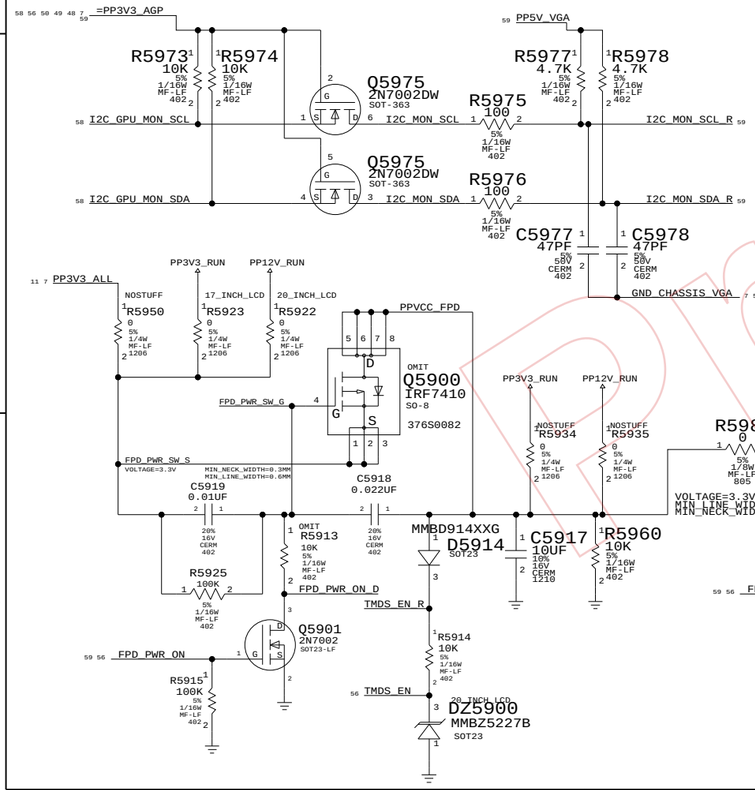


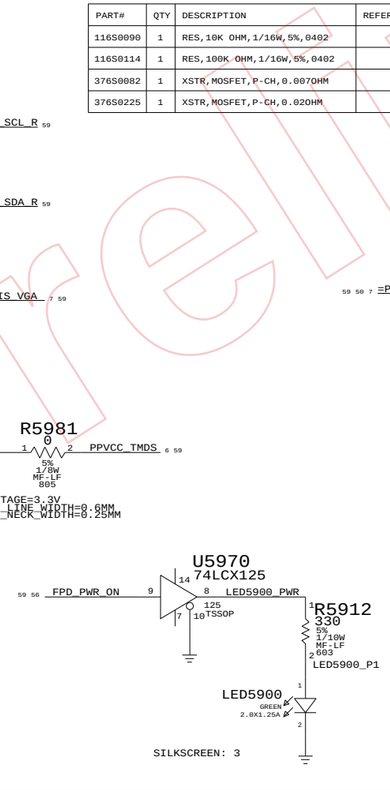


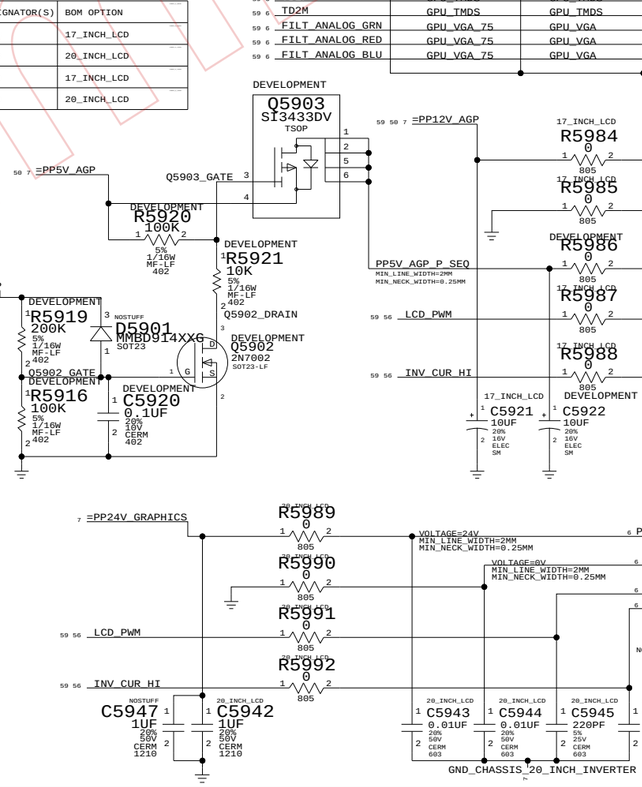
NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
GPU_TMDS	GPU_TMDS	TCK	
GPU_TMDS	GPU_TMDS	TCK	
GPU_TMDS	GPU_TMDS	TD0	
GPU_TMDS	GPU_TMDS	TD0	
GPU_TMDS	GPU_TMDS	TD1	
GPU_TMDS	GPU_TMDS	TD1	
GPU_TMDS	GPU_TMDS	TD2	
GPU_TMDS	GPU_TMDS	TD2	
GPU_VGA_75	GPU_VGA		
GPU_VGA_75	GPU_VGA		
GPU_VGA_75	GPU_VGA		

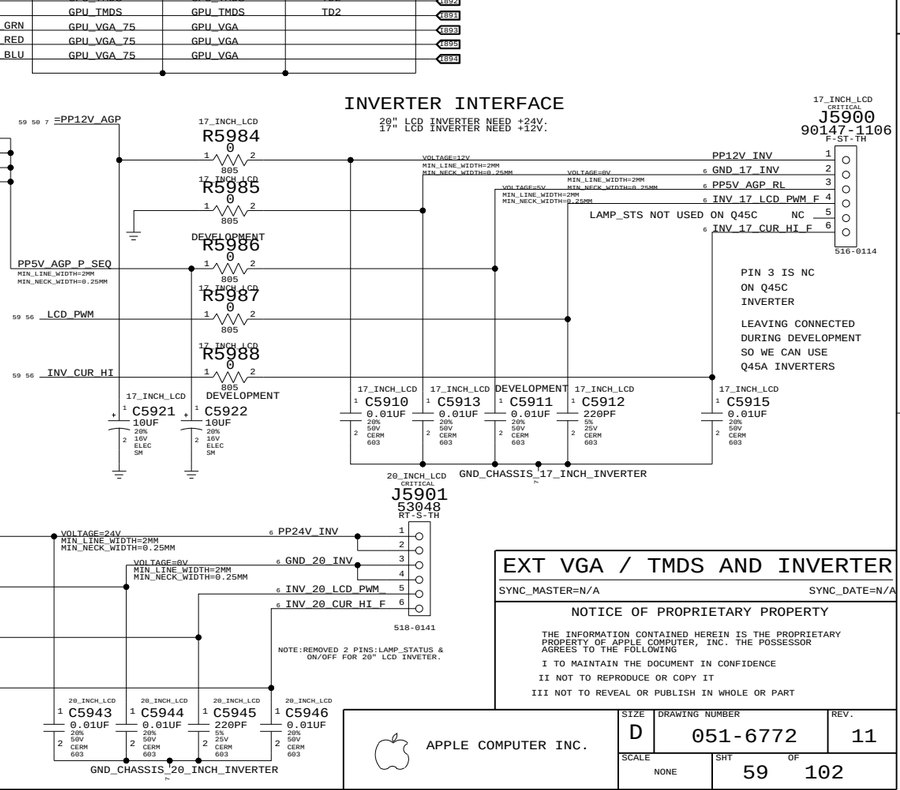
TABLE FOR PANEL POWER SEQUENCING (LOWER LEFT)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S0114	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
376S0082	1	XSTR,MOSFET,P-CH,0.007OHM	Q5900	17_INCH_LCD
376S0225	1	XSTR,MOSFET,P-CH,0.020HM	Q5900	20_INCH_LCD







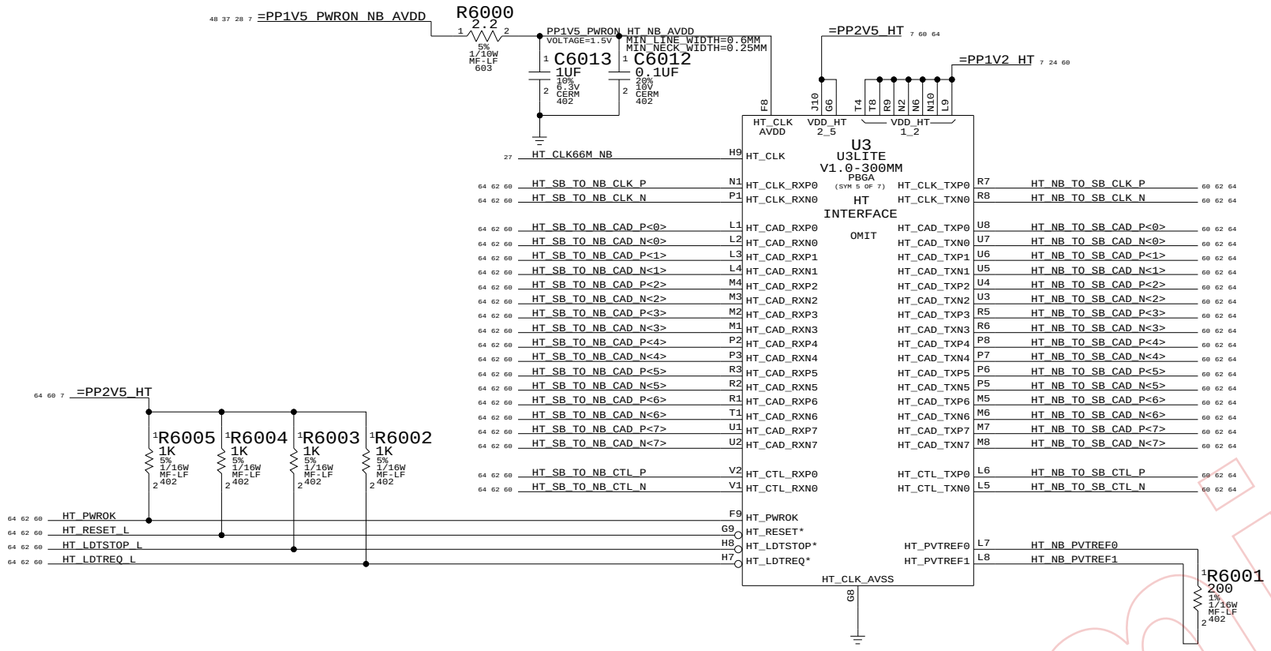


EXT VGA / TMDS AND INVERTER

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 59 OF 102	

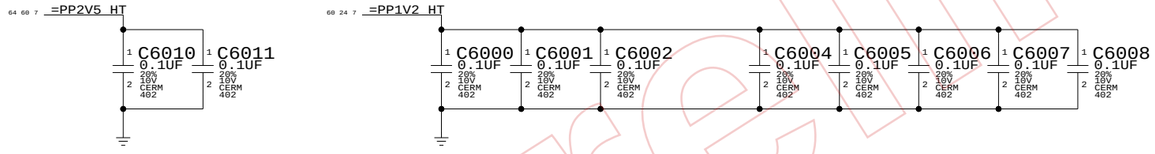


	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5	HT_2V5		189

HT_NB_TO_SB HT_SB_TO_NB
5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5
4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE CAN BE LOOSE
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH



U3LITE HT

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 60 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	P25MM	

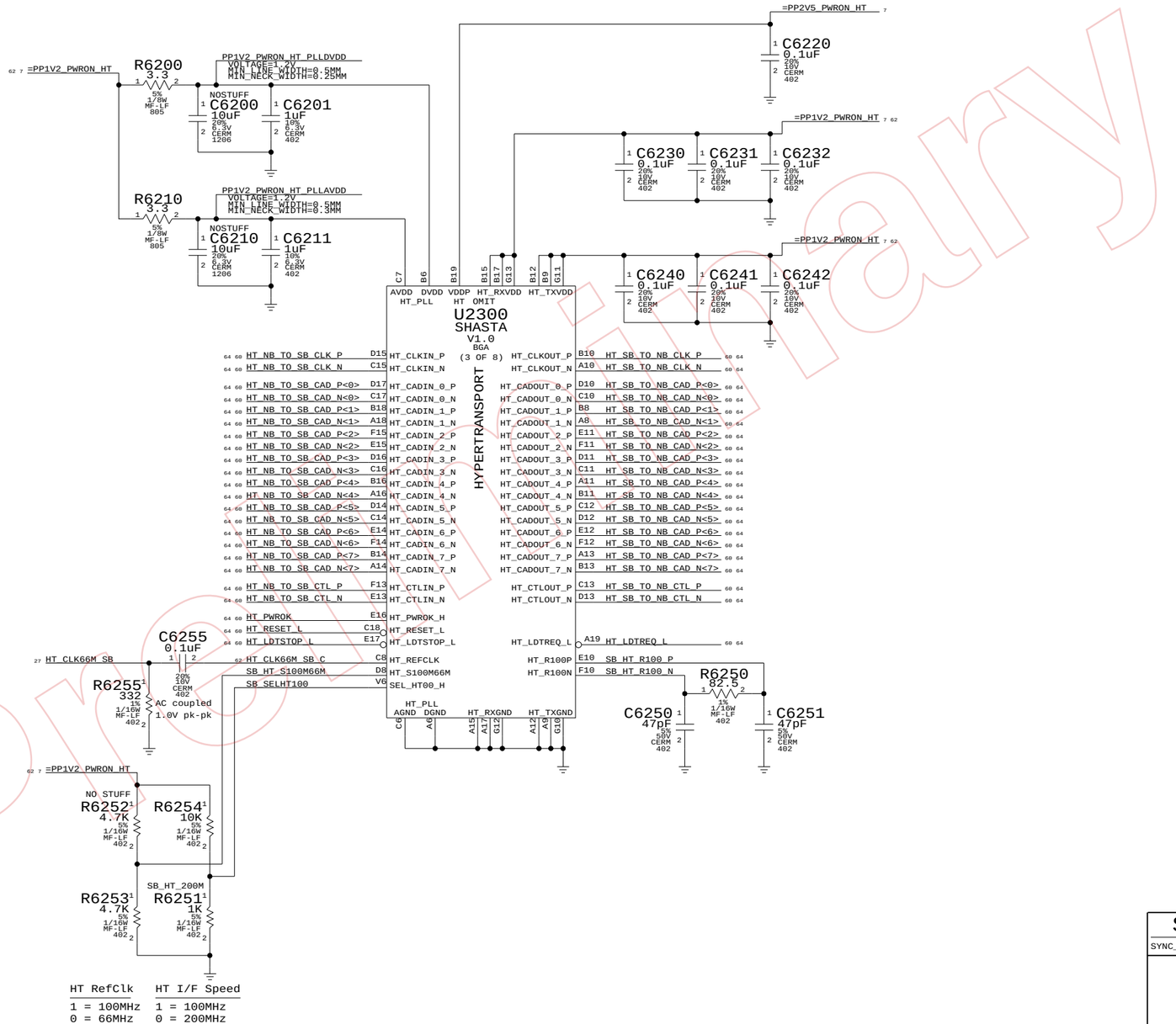
HT_CLK66M_SB_C 62

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



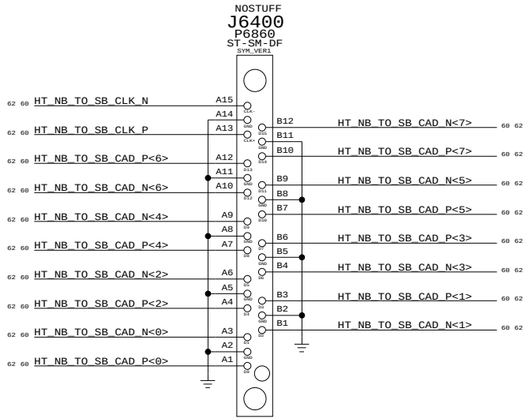
Shasta HyperTransport

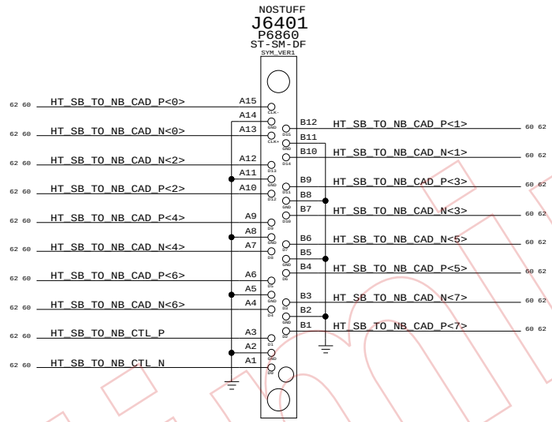
SYNC_MASTER=N/A SYNC_DATE=N/A

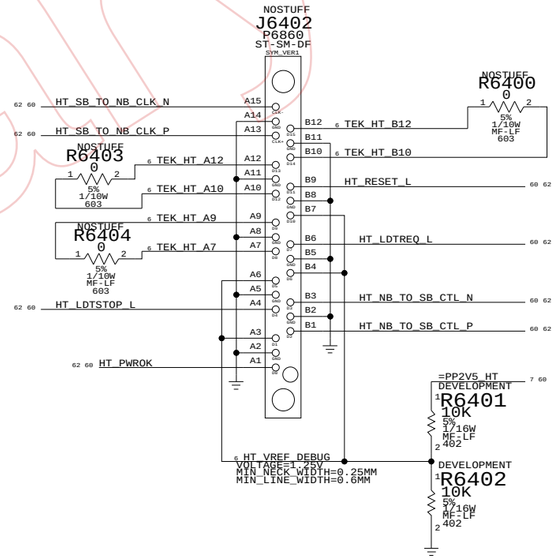
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6772	11
	SCALE	SHT	OF
	NONE	62	102

SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2







HT DEBUG CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11

SCALE	SHT
NONE	64 OF 102

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

74	PCI_SB_AD<0>	RP7300	2	7	47	PCI_AD<0>	6 74 75 76 77
74	PCI_SB_AD<1>	RP7303	1	8	47	PCI_AD<1>	6 74 75 76 77
74	PCI_SB_AD<2>	RP7303	2	7	47	PCI_AD<2>	6 74 75 76 77
74	PCI_SB_AD<3>	RP7303	4	5	47	PCI_AD<3>	6 74 75 76 77
74	PCI_SB_AD<4>	RP7309	2	7	47	PCI_AD<4>	6 74 75 76 77
74	PCI_SB_AD<5>	RP7300	1	8	47	PCI_AD<5>	6 74 75 76 77
74	PCI_SB_AD<6>	RP7300	3	6	47	PCI_AD<6>	6 74 75 76 77
74	PCI_SB_AD<7>	RP7309	4	5	47	PCI_AD<7>	6 74 75 76 77
74	PCI_SB_AD<8>	RP7300	4	5	47	PCI_AD<8>	6 74 75 76 77
74	PCI_SB_AD<9>	RP7301	2	7	47	PCI_AD<9>	6 74 75 76 77
74	PCI_SB_AD<10>	RP7301	1	8	47	PCI_AD<10>	6 74 75 76 77
74	PCI_SB_AD<11>	RP7301	4	5	47	PCI_AD<11>	6 74 75 76 77
74	PCI_SB_AD<12>	RP7309	1	8	47	PCI_AD<12>	6 74 75 76 77
74	PCI_SB_AD<13>	RP7309	3	6	47	PCI_AD<13>	6 74 75 76 77
74	PCI_SB_AD<14>	RP7301	3	6	47	PCI_AD<14>	6 74 75 76 77
74	PCI_SB_AD<15>	RP7307	1	8	47	PCI_AD<15>	6 74 75 76 77
74	PCI_SB_AD<16>	RP7308	1	8	47	PCI_AD<16>	6 74 75 76 77

R7300
47
5%
1/16W
MF-LF
402

74	PCI_SB_AD<17>		1	2		PCI_AD<17>	6 74 75 76 77

74	PCI_SB_AD<18>	RP7307	2	7	47	PCI_AD<18>	6 74 75 76 77
74	PCI_SB_AD<19>	RP7306	3	6	47	PCI_AD<19>	6 74 75 76 77
74	PCI_SB_AD<20>	RP7305	1	8	47	PCI_AD<20>	6 74 75 76 77
74	PCI_SB_AD<21>	RP7305	2	7	47	PCI_AD<21>	6 74 76 77
74	PCI_SB_AD<22>	RP7302	1	8	47	PCI_AD<22>	6 74 76 77
74	PCI_SB_AD<23>	RP7302	3	6	47	PCI_AD<23>	6 74 76 77
74	PCI_SB_AD<24>	RP7304	1	8	47	PCI_AD<24>	6 74 75 76 77
74	PCI_SB_AD<25>	RP7306	4	5	47	PCI_AD<25>	6 74 75 76 77
74	PCI_SB_AD<26>	RP7305	3	6	47	PCI_AD<26>	6 74 75 76 77

R7301
47
5%
1/16W
MF-LF
402

74	PCI_SB_AD<27>		1	2		PCI_AD<27>	6 74 75 76 77

74	PCI_SB_AD<28>	RP7302	2	7	47	PCI_AD<28>	6 74 75 76 77
74	PCI_SB_AD<29>	RP7304	4	5	47	PCI_AD<29>	6 74 75 76 77
74	PCI_SB_AD<30>	RP7302	4	5	47	PCI_AD<30>	6 74 75 76 77
74	PCI_SB_AD<31>	RP7304	2	7	47	PCI_AD<31>	6 74 75 76 77
74	PCI_SB_CBE_L<0>	RP7303	3	6	47	PCI_CBE_L<0>	6 74 76 77
74	PCI_SB_CBE_L<1>	RP7306	2	7	47	PCI_CBE_L<1>	6 74 76 77
74	PCI_SB_CBE_L<2>	RP7305	4	5	47	PCI_CBE_L<2>	6 74 76 77
74	PCI_SB_CBE_L<3>	RP7304	3	6	47	PCI_CBE_L<3>	6 74 76 77
74	PCI_SB_DEVSEL_L	RP7306	1	8	47	PCI_DEVSEL_L	6 74 76 77
74	PCI_SB_FRAME_L	RP7307	4	5	47	PCI_FRAME_L	6 74 76 77
74	PCI_SB_IRDY_L	RP7307	3	6	47	PCI_IRDY_L	6 74 76 77
74	PCI_SB_TRDY_L	RP7308	3	6	47	PCI_TRDY_L	6 74 76 77
74	PCI_SB_STOP_L	RP7308	4	5	47	PCI_STOP_L	6 74 76 77
74	PCI_SB_PAR	RP7308	2	7	47	PCI_PAR	6 74 76 77

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 73 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PCI_AD	PCI		PCI_AD<31..28> 6 73 75 76 77
PCI_AD27	PCI		PCI_AD<27> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<26..24> 6 73 75 76 77
PCI_AD23	PCI		PCI_AD<23> 6 73 76 77
PCI_AD22	PCI		PCI_AD<22> 6 73 76 77
PCI_AD21	PCI		PCI_AD<21> 6 73 76 77
PCI_AD20	PCI		PCI_AD<20> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<19..18> 6 73 75 76 77
PCI_AD17	PCI		PCI_AD<17> 6 73 75 76 77
PCI_AD	PCI		PCI_AD<16..0> 6 73 75 76 77
PCI	PCI		PCI_CBE_L<3..0> 6 73 76 77
PCI	PCI		PCI_PAR 6 73 76 77
PCI_CTL	PCI		PCI_DEVSEL_L 6 73 74 76 77
PCI_CTL	PCI		PCI_FRAME_L 6 73 74 76 77
PCI_CTL	PCI		PCI_IRDY_L 6 73 74 76 77
PCI_CTL	PCI		PCI_TRDY_L 6 73 74 76 77
PCI_CTL	PCI		PCI_STOP_L 6 73 74 76 77

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

7 =PP3V3_SB_PCI

NO_STUFF C7410 10uF 20% 6.3V CERM 805
C7400 0.1uF 20% 10V CERM 402
C7401 0.1uF 20% 10V CERM 402
C7402 0.1uF 20% 10V CERM 402
C7403 0.1uF 20% 10V CERM 402
C7404 0.1uF 20% 10V CERM 402

NO_STUFF C7411 10uF 20% 6.3V CERM 805
C7405 0.1uF 20% 10V CERM 402
C7406 0.1uF 20% 10V CERM 402
C7407 0.1uF 20% 10V CERM 402
C7408 0.1uF 20% 10V CERM 402
C7409 0.1uF 20% 10V CERM 402

=PP2V5_PWRON_SB 7 23 25 88

C7420 0.1uF 20% 10V CERM 402
C7421 0.1uF 20% 10V CERM 402
C7422 0.1uF 20% 10V CERM 402
C7423 0.1uF 20% 10V CERM 402

AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19 — VDDOPC
B20 J18 N20 U20 — PCIVDDP

U2300 SHASTA V1.0 BGA (4 OF 8) OMIT

PCI

27 PCI_CLK66M_SB_INT AB9 PCIBR_CLK_H
27 8 PCI_CLK33M_SB_EXT U19 PCI1CLK_H

"Slot A" - AD17
76 74 6 PCI_SLOTA_REQ_L AB18 PCI1REQ_0_L
76 74 6 PCI_SLOTA_GNT_L AA18 PCI1GNT_0_L

"Slot G" - AD27
77 74 PCI_SLOTG_REQ_L AB20 PCI1REQ_1_L
77 74 PCI_SLOTG_GNT_L AB19 PCI1GNT_1_L

"Slot D" - AD20
74 PCI_SLOTD_REQ_L V17 PCI1REQ_2_L
74 PCI_SLOTD_GNT_L V18 PCI1GNT_2_L

76 75 6 ROM_CS_L AB8 ROMCS_L
76 75 6 ROM_OE_L AA9 ROMOE_L
76 75 6 ROM_WE_L Y10 ROMRW_L

PCI1AD_0_H	L18	PCI_SB_AD<0>	73
PCI1AD_1_H	K19	PCI_SB_AD<1>	73
PCI1AD_2_H	L22	PCI_SB_AD<2>	73
PCI1AD_3_H	M22	PCI_SB_AD<3>	73
PCI1AD_4_H	M18	PCI_SB_AD<4>	73
PCI1AD_5_H	L20	PCI_SB_AD<5>	73
PCI1AD_6_H	M21	PCI_SB_AD<6>	73
PCI1AD_7_H	N16	PCI_SB_AD<7>	73
PCI1AD_8_H	M20	PCI_SB_AD<8>	73
PCI1AD_9_H	P22	PCI_SB_AD<9>	73
PCI1AD_10_H	M17	PCI_SB_AD<10>	73
PCI1AD_11_H	N18	PCI_SB_AD<11>	73
PCI1AD_12_H	M19	PCI_SB_AD<12>	73
PCI1AD_13_H	N19	PCI_SB_AD<13>	73
PCI1AD_14_H	P21	PCI_SB_AD<14>	73
PCI1AD_15_H	R22	PCI_SB_AD<15>	73
PCI1AD_16_H	P20	PCI_SB_AD<16>	73
PCI1AD_17_H	V21	PCI_SB_AD<17>	73
PCI1AD_18_H	P18	PCI_SB_AD<18>	73
PCI1AD_19_H	T20	PCI_SB_AD<19>	73
PCI1AD_20_H	R16	PCI_SB_AD<20>	73
PCI1AD_21_H	R17	PCI_SB_AD<21>	73
PCI1AD_22_H	W21	PCI_SB_AD<22>	73
PCI1AD_23_H	Y22	PCI_SB_AD<23>	73
PCI1AD_24_H	R18	PCI_SB_AD<24>	73
PCI1AD_25_H	T19	PCI_SB_AD<25>	73
PCI1AD_26_H	T18	PCI_SB_AD<26>	73
PCI1AD_27_H	Y21	PCI_SB_AD<27>	73
PCI1AD_28_H	W20	PCI_SB_AD<28>	73
PCI1AD_29_H	T16	PCI_SB_AD<29>	73
PCI1AD_30_H	AA21	PCI_SB_AD<30>	73
PCI1AD_31_H	T17	PCI_SB_AD<31>	73
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	73
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	73
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	73
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	73
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	73
PCI1FRAME_L	T21	PCI_SB_FRAME_L	73
PCI1IRDY_L	R21	PCI_SB_IRDY_L	73
PCI1TRDY_L	P19	PCI_SB_TRDY_L	73
PCI1STOP_L	P17	PCI_SB_STOP_L	73
PCI1PAR_H	N17	PCI_SB_PAR	73
PCI1RST_L	U18	SB_PCI_RESET_L	

=PP3V3_PWRON_SB 7 23 25

R7455 4.7K 5% 1/16W MF-LF 402
C7450 0.1uF 20% 10V CERM 402
R7450 4.7K 5% 1/16W MF-LF 402

U7450 NC74VHC1G08 SOT23-5

77 25 8 SYS_WARM_RESET_L
PCI_RESET_L 6 8 56

Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

=PP3V3_PCI 7 25 74 75 76 77

RP7400 4.7K 5% 1/16W SM-LF — PCI_SLOTA_REQ_L 6 74 76
RP7400 4.7K 5% 1/16W SM-LF — PCI_SLOTA_GNT_L 6 74 76
RP7400 4.7K 5% 1/16W SM-LF — PCI_SLOTG_REQ_L 74 77
RP7400 4.7K 5% 1/16W SM-LF — PCI_SLOTG_GNT_L 74 77
RP7401 4.7K 5% 1/16W SM-LF — PCI_SLOTD_REQ_L 74
RP7401 4.7K 5% 1/16W SM-LF — PCI_SLOTD_GNT_L 74

77 76 75 74 25 7 =PP3V3_PCI

RP7402 4.7K 5% 1/16W SM-LF — PCI_DEVSEL_L 77 76 74 73 6
RP7402 4.7K 5% 1/16W SM-LF — PCI_FRAME_L 77 76 74 73 6
RP7402 4.7K 5% 1/16W SM-LF — PCI_IRDY_L 77 76 74 73 6
RP7402 4.7K 5% 1/16W SM-LF — PCI_TRDY_L 77 76 74 73 6
RP7401 4.7K 5% 1/16W SM-LF — PCI_STOP_L 77 76 74 73 6

Shasta PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 74 OF 102	

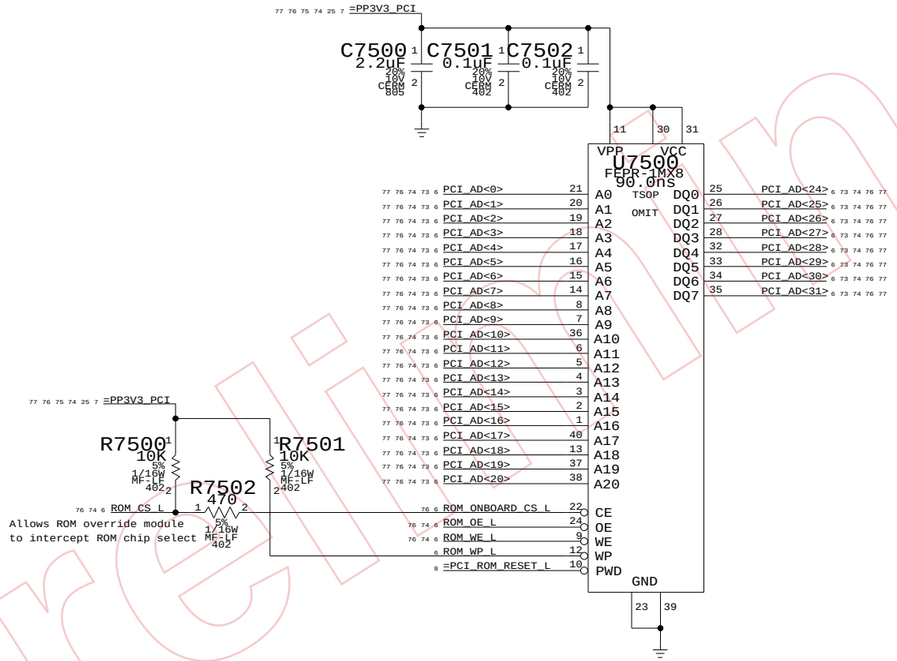
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11

SCALE: NONE

SHT 75 OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

_PCI_CLK33M_AIRPORT 8 76

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR

77 75 74 25 7 =PP3V3_PCI

SDF7600
STDOFF-3MMOD5MMH-TH

NOSTUFF C7650 10UF 20% 6.3V CERM 1206
C7651 1UF 10% 6.3V CERM 402
C7652 1UF 10% 6.3V CERM 402

CRITICAL
J7650
20-5602-080-041-829
F-ST-SM

	1	2	PCI_AD<31> 6 73 74 75 77
77 75 74 73 6 PCI_AD<30>	3	4	AIRPORT_CLKRUN_L_PD 6
	5	6	TP_AP_PME_L
77 75 74 73 6 PCI_AD<27>	7	8	PCI_SLOTA_GNT_L 6 74
74 6 PCI_SLOTA_REQ_L	9	10	
77 75 74 73 6 PCI_AD<25>	11	12	
77 75 74 73 6 PCI_AD<29>	13	14	PCI_AD<24> 6 73 74 75 77
	15	16	PCI_AIRPORT_RESET_L 8
77 74 73 6 PCI_CBE_L<3>	17	18	PCI_AD<28> 6 73 74 75 77
77 75 74 73 6 PCI_AD<26>	19	20	
77 74 73 6 PCI_AD<22>	21	22	PCI_AD<23> 6 73 74 77
6 PCI_SLOTA_IDSEL	23	24	
	25	26	PCI_AD<20> 6 73 74 75 77
77 75 74 73 6 PCI_AD<19>	27	28	PCI_FRAME_L 6 73 74 77
77 74 73 6 PCI_AD<21>	29	30	PCI_AD<17> 6 73 74 75 76 77
77 74 73 6 PCI_IRDY_L	31	32	
77 75 74 73 6 PCI_AD<18>	33	34	PCI_TRDY_L 6 73 74 77
77 74 73 6 PCI_DEVSEL_L	35	36	
	37	38	PCI_CBE_L<2> 6 73 74 77
76 8 _PCI_CLK33M_AIRPORT	39	40	PCI_AD<16> 6 73 74 75 77
77 74 73 6 PCI_STOP_L	41	42	
77 75 74 73 6 PCI_AD<12>	43	44	
77 74 73 6 PCI_PAR	45	46	
	47	48	PCI_AD<14> 6 73 74 75 77
77 75 74 73 6 PCI_AD<8>	49	50	PCI_AD<13> 6 73 74 75 77
77 75 74 73 6 PCI_AD<9>	51	52	
77 74 73 6 PCI_CBE_L<0>	53	54	PCI_AD<10> 6 73 74 75 77
	55	56	PCI_AD<15> 6 73 74 75 77
77 75 74 73 6 PCI_AD<7>	57	58	AP_ALT_ANT
77 75 74 73 6 PCI_AD<3>	59	60	PCI_CBE_L<1> 6 73 74 77
77 75 74 73 6 PCI_AD<6>	61	62	PCI_AD<4> 6 73 74 75 77
	63	64	
77 75 74 73 6 PCI_AD<1>	65	66	PCI_AD<11> 6 73 74 75 77
77 75 74 73 6 PCI_AD<5>	67	68	ROM_WE_L 6 74 75
77 75 74 73 6 PCI_AD<0>	69	70	PCI_AD<2> 6 73 74 75 77
	71	72	
	73	74	PCI_SLOTA_INT_L 6 25
	75	76	ROM_OE_L 6 74 75
	77	78	ROM_ONBOARD_CS_L 6 75
7 _PP3V3_PWRON_BT	79	80	ROM_CS_L 6 74 75
91 USB2_OC<4>			

516S0285

R7650 10K 5% 1/16W MF-LF 402

R7651 22 5% 1/16W MF-LF 402
77 76 75 74 73 6 PCI_AD<17>

91 USB2_P<4> 6 USB_BT_P
91 USB2_N<4> 6 USB_BT_N

R7660 15K 5% 1/16W MF-LF 402
R7661 15K 5% 1/16W MF-LF 402
MAKE_BASE=TRUE
MAKE_BASE=TRUE

C7660 1UF 10% 6.3V CERM 402

SDF7601
STDOFF-3MMOD5MMH-TH1

AIRPORT & BLUETOOTH

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 76 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

=PCI_CLK33M_USB2 8 77

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

7 =PPVIO_PCI_USB2

C7703 0.1uF 20% 10V CERM 402 — 1 / 2 — H1

VDD_PCI: H3, M4, C8

CRITICAL
U7700
NEC_UPD720101_USB2
FBGA

76 75 74 73 6 PCI_AD<0>	M5	AD0			
76 75 74 73 6 PCI_AD<1>	P5	AD1			
76 75 74 73 6 PCI_AD<2>	N5	AD2			
76 75 74 73 6 PCI_AD<3>	P4	AD3			
76 75 74 73 6 PCI_AD<4>	N4	AD4			
76 75 74 73 6 PCI_AD<5>	M3	AD5			
76 75 74 73 6 PCI_AD<6>	N3	AD6			
76 75 74 73 6 PCI_AD<7>	M1	AD7			
76 75 74 73 6 PCI_AD<8>	L2	AD8			
76 75 74 73 6 PCI_AD<9>	L1	AD9			
76 75 74 73 6 PCI_AD<10>	K2	AD10			
76 75 74 73 6 PCI_AD<11>	L3	AD11			
76 75 74 73 6 PCI_AD<12>	K1	AD12			
76 75 74 73 6 PCI_AD<13>	K3	AD13			
76 75 74 73 6 PCI_AD<14>	J2	AD14			
76 75 74 73 6 PCI_AD<15>	J1	AD15			
76 75 74 73 6 PCI_AD<16>	F2	AD16			
76 75 74 73 6 PCI_AD<17>	E3	AD17			
76 75 74 73 6 PCI_AD<18>	E1	AD18			
76 75 74 73 6 PCI_AD<19>	D3	AD19			
76 75 74 73 6 PCI_AD<20>	D1	AD20			
76 74 73 6 PCI_AD<21>	D2	AD21			
76 74 73 6 PCI_AD<22>	C2	AD22			
76 74 73 6 PCI_AD<23>	C1	AD23			
76 75 74 73 6 PCI_AD<24>	B4	AD24			
76 75 74 73 6 PCI_AD<25>	A4	AD25			
76 75 74 73 6 PCI_AD<26>	B5	AD26			
(PCI_AD<27>)	C4	AD27			
76 75 74 73 6 PCI_AD<28>	A5	AD28			
76 75 74 73 6 PCI_AD<29>	C5	AD29			
76 75 74 73 6 PCI_AD<30>	B6	AD30			
76 75 74 73 6 PCI_AD<31>	A6	AD31			
76 74 73 6 PCI_CBE_L<0>	M2	CBE0			
76 74 73 6 PCI_CBE_L<1>	J3	CBE1			
76 74 73 6 PCI_CBE_L<2>	F1	CBE2			
76 74 73 6 PCI_CBE_L<3>	C3	CBE3			
76 74 73 6 PCI_PAR	J4	PAR			
76 74 73 6 PCI_FRAME_L	F3	FRAME			
76 74 73 6 PCI_IRDY_L	F4	IRDY			
76 74 73 6 PCI_TRDY_L	G1	TRDY			
76 74 73 6 PCI_STOP_L	G3	STOP			
PCI_SLOTG_IDSEL	B3	IDSEL			
76 74 73 6 PCI_DEVSEL_L	G2	DEVSEL			
74 PCI_SLOTG_REQ_L	C6	REQ			
74 PCI_SLOTG_GNT_L	D6	GNT			
NEC_PERR_L_PU	H2	PERR			
NEC_SERR_L_PU	H1	SERR OD			
NEC_INTA_L	C7	INTA OD			
NEC_INTB_L	B7	INTB OD			
NEC_INTC_L	A7	INTC OD			
77 8 =PCI_CLK33M_USB2	A8	PCLK			
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)			
NEC_CRUN_L_PD	N6	CRUN			
NEC_PME_L	D9	PME OD			
NEC_VCCRST_L	C9	VCCRST(PCI RESET)			
6 TP_NEC_SMI_L	L6	SMI OD			
NEC_LEGC_PD	L7	LEGC			
			IPD NTEST1	M8	TP_NEC_NTEST1 6
			IPD SMC	M7	TP_NEC_SMC 6
			IPD TEB	N7	TP_NEC_TEB 6
			IPD AMC	P7	TP_NEC_AMC 6
			IPD TEST	L8	TP_NEC_TEST 6
			NANDTEST	M10	TP_NEC_NANDTEST 6
			SRCLK	M9	TP_NEC_SRCLK 6
			SRDTA	N9	TP_NEC_SRDATA 6
			IPD SRMOD	P9	TP_NEC_SRMOD 6

76 75 74 73 6 PCI_AD<27> → R7714 22 5% 1/16W MF-LF 402 — 1 / 2 — (PCI_AD<27>)

76 75 74 25 7 =PP3V3_PCI

R7716 10K 5% 1/16W MF-LF 402 — 1 / 2
R7713 10K 5% 1/16W MF-LF 402 — 1 / 2

RP7703 47 5% 1/16W SM-LF — 4 / 5
RP7703 47 5% 1/10W SM-LF — 2 / 7
RP7703 47 5% 1/10W SM-LF — 3 / 6
RP7702 47 5% 1/10W SM-LF — 3 / 6
RP7702 47 5% 1/10W SM-LF — 4 / 5
RP7702 47 5% 1/10W SM-LF — 2 / 7

25 PCI_SLOTG_INT_L
74 25 8 SYS_WARM_RESET_L
25 13 SYS_PME_L
8 =PCI_USB2_RESET_L

RP7702 & RP7703 required to facilitate NAND-tree testing

R7715 4.7K 5% 1/16W MF-LF 402 — 1 / 2
RP7703 47 5% 1/16W SM-LF — 8 / 1

USB 2.0 PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 77 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C 80 83
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C 80 83
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_P1 80 83
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_N1 80 83
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C 80 83
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C 80 83
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_P2 80 83
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_N2 80 83
UATA_DD				UATA_DD<15..8> 6 80 83
UATA_DD7				UATA_DD<7> 6 80 83
UATA_DD				UATA_DD<6..0> 6 80 83
UATA_HOST				UATA_DA<2..0> 6 80 83
UATA_HOST				UATA_CS0_L 6 80 83
UATA_HOST				UATA_CS1_L 6 80 83
UATA_HOST				UATA_HSTROBE 6 80 83
UATA_HOST				UATA_STOP 6 80 83
UATA_HOST_R				UATA_DMACK_L 6 80 83
UATA_HOST_R				UATA_RESET_L 6 80 83
UATA_DEV_R_C				UATA_DSTROBE 80 83
UATA_DEV_R				UATA_DMARQ 80 83
UATA_DEV_R				UATA_INTRQ 80 83

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

7 =PP1V2_PWRON_DISK_SB

SATA_VDD x 5

C8000 0.1uF 20% 10V CERM 402
C8001 0.1uF 20% 10V CERM 402
C8002 0.1uF 20% 10V CERM 402
C8003 0.1uF 20% 10V CERM 402
C8004 0.1uF 20% 10V CERM 402

AB14 AB17 T14 W15 Y18 SATA_VDD

U2300 OMIT
SHASTA
V1.0
BGA
(5 OF 8)

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0> 80
UD_IDEDD_1_H	H7	UATA_DD_R<1> 80
UD_IDEDD_2_H	H6	UATA_DD_R<2> 80
UD_IDEDD_3_H	E2	UATA_DD_R<3> 80
UD_IDEDD_4_H	C1	UATA_DD_R<4> 80
UD_IDEDD_5_H	C2	UATA_DD_R<5> 80
UD_IDEDD_6_H	E3	UATA_DD_R<6> 80
UD_IDEDD_7_H	G6	UATA_DD_R<7> 80
UD_IDEDD_8_H	G5	UATA_DD_R<8> 80
UD_IDEDD_9_H	D4	UATA_DD_R<9> 80
UD_IDEDD_10_H	G7	UATA_DD_R<10> 80
UD_IDEDD_11_H	F6	UATA_DD_R<11> 80
UD_IDEDD_12_H	C3	UATA_DD_R<12> 80
UD_IDEDD_13_H	F5	UATA_DD_R<13> 80
UD_IDEDD_14_H	E5	UATA_DD_R<14> 80
UD_IDEDD_15_H	D5	UATA_DD_R<15> 80
UD_IDEDA0_H	E6	UATA_DA_R<0> 80
UD_IDEDA1_H	C4	UATA_DA_R<1> 80
UD_IDEDA2_H	D6	UATA_DA_R<2> 80
UD_IDECS1FX_L	B3	UATA_CS0_L_R 80
UD_IDECS3FX_L	B4	UATA_CS1_L_R 80
UD_IDEDMACK_L	E8	UATA_DMACK_L_R 80
UD_IDERD_L	E4	UATA_HSTROBE_R 80
UD_IDEWR_L	D3	UATA_STOP_R 80
UD_IDERST_L	E7	UATA_RESET_L_R 80

DSTROBE aka: IORDY/HDMARDY*
HSTROBE aka: DIOR*
STOP aka: DIOW*

83 80 UATA_DSTROBE	F9	UD_IDECHRDY_H
83 80 UATA_DMARQ	D7	UD_IDEDMARQ_H
83 80 UATA_INTRQ	C5	UD_IDEINTRQ_H

83 80 SATA_RXD_P1_C	Y17	RXDP1	TXDP1 AA16 SATA_TXD_P1 80 83
83 80 SATA_RXD_N1_C	Y16	RXDN1	TXDN1 AB16 SATA_TXD_N1 80 83
83 80 SATA_RXD_P2_C	AB15	RXDP2	TXDP2 Y15 SATA_TXD_P2 80 83
83 80 SATA_RXD_N2_C	AA15	RXDN2	TXDN2 Y14 SATA_TXD_N2 80 83

SATA 0
SATA 1
SATA_GND

AA14 AA17 T13 W16

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

UATA Termination

R8005 10K 5% 1/16W MF-LF 402

80 UATA_DD_R<0>	RP8000 33 5% 1/16W SM-LF		UATA_DD<0> 6 80 83
80 UATA_DD_R<1>	RP8000 33 5% 1/16W SM-LF		UATA_DD<1> 6 80 83
80 UATA_DD_R<2>	RP8000 33 5% 1/16W SM-LF		UATA_DD<2> 6 80 83
80 UATA_DD_R<3>	RP8003 33 5% 1/16W SM-LF		UATA_DD<3> 6 80 83
80 UATA_DD_R<4>	RP8001 33 5% 1/16W SM-LF		UATA_DD<4> 6 80 83
80 UATA_DD_R<5>	RP8001 33 5% 1/16W SM-LF		UATA_DD<5> 6 80 83
80 UATA_DD_R<6>	RP8003 33 5% 1/16W SM-LF		UATA_DD<6> 6 80 83
80 UATA_DD_R<7>	RP8002 33 5% 1/16W SM-LF		UATA_DD<7> 6 80 83
80 UATA_DD_R<8>	RP8002 33 5% 1/16W SM-LF		UATA_DD<8> 6 80 83
80 UATA_DD_R<9>	RP8003 33 5% 1/16W SM-LF		UATA_DD<9> 6 80 83
80 UATA_DD_R<10>	RP8000 33 5% 1/16W SM-LF		UATA_DD<10> 6 80 83
80 UATA_DD_R<11>	RP8002 33 5% 1/16W SM-LF		UATA_DD<11> 6 80 83
80 UATA_DD_R<12>	RP8001 33 5% 1/16W SM-LF		UATA_DD<12> 6 80 83
80 UATA_DD_R<13>	RP8002 33 5% 1/16W SM-LF		UATA_DD<13> 6 80 83
80 UATA_DD_R<14>	RP8004 33 5% 1/16W SM-LF		UATA_DD<14> 6 80 83
80 UATA_DD_R<15>	RP8003 33 5% 1/16W SM-LF		UATA_DD<15> 6 80 83
80 UATA_DA_R<0>	RP8004 33 5% 1/16W SM-LF		UATA_DA<0> 6 80 83
80 UATA_DA_R<1>	RP8001 33 5% 1/16W SM-LF		UATA_DA<1> 6 80 83
80 UATA_DA_R<2>	RP8004 33 5% 1/16W SM-LF		UATA_DA<2> 6 80 83
80 UATA_RESET_L_R	RP8004 33 5% 1/16W SM-LF		UATA_RESET_L 6 80 83
80 UATA_CS0_L_R	R8000 33 5% 1/16W MF-LF 402		UATA_CS0_L 6 80 83
80 UATA_CS1_L_R	R8001 33 5% 1/16W MF-LF 402		UATA_CS1_L 6 80 83
80 UATA_HSTROBE_R	R8002 22 5% 1/16W MF-LF 402		UATA_HSTROBE 6 80 83
80 UATA_STOP_R	R8003 22 5% 1/16W MF-LF 402		UATA_STOP 6 80 83
80 UATA_DMACK_L_R	R8004 22 5% 1/16W MF-LF 402		UATA_DMACK_L 6 80 83

Shasta Disk

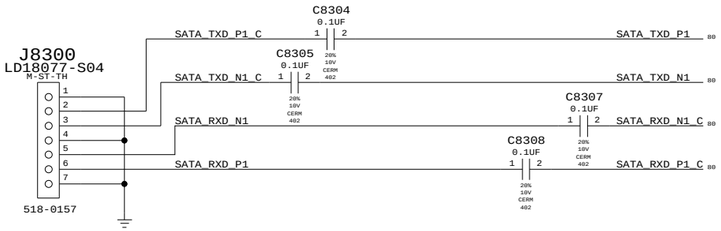
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 80 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
83 80 6 UATA_DD<15..8>	UATA_DD		
83 80 6 UATA_DD<7>	UATA_DD7		
83 80 6 UATA_DD<6..0>	UATA_DD		
83 80 6 UATA_DA<2..0>	UATA_HOST		
83 80 6 UATA_CS0_L	UATA_HOST		
83 80 6 UATA_CS1_L	UATA_HOST		
83 80 6 UATA_HSTROBE	UATA_HOST		
83 80 6 UATA_STOP	UATA_HOST		
83 80 6 UATA_DMACK_L	UATA_HOST_R		
83 80 6 UATA_RESET_L	UATA_HOST_R		
83 80 UATA_DSTROBE	UATA_DEV_R_C		
83 80 UATA_DMARQ	UATA_DEV_R		
83 80 UATA_INTRQ	UATA_DEV_R		

SATA CONNECTORS



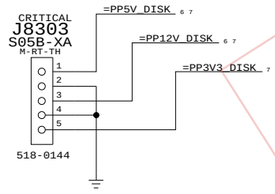
80 SATA_TXD_P2 — TP_SATA_TXD_P2 MAKE_BASE=TRUE

80 SATA_TXD_N2 — TP_SATA_TXD_N2 MAKE_BASE=TRUE

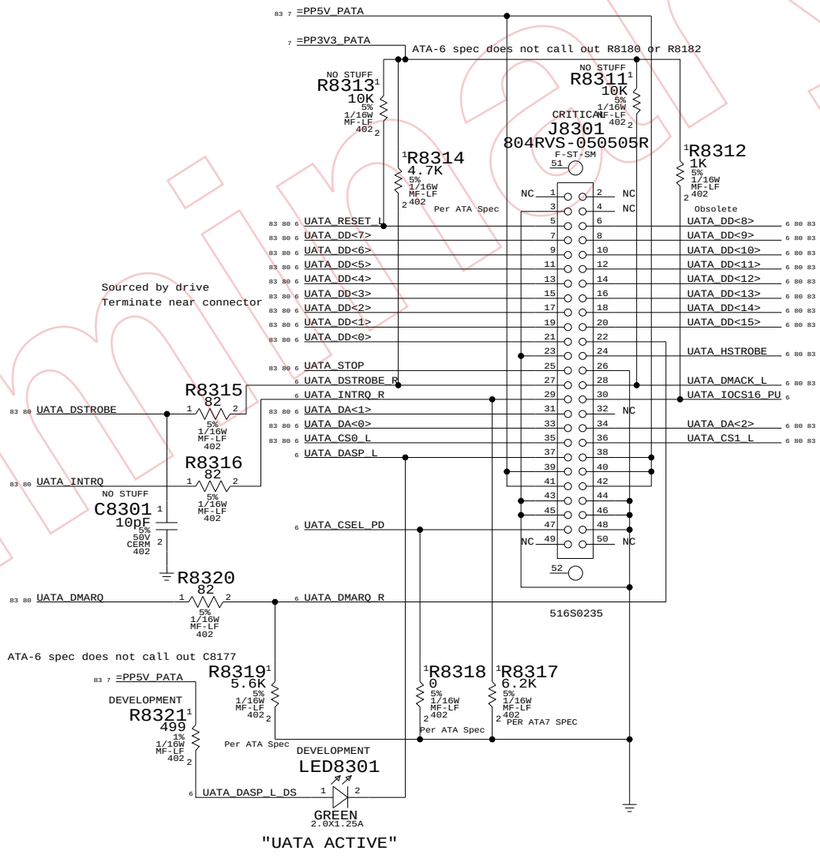
80 SATA_RXD_N2_C — TP_SATA_RXD_N2_C MAKE_BASE=TRUE

80 SATA_RXD_P2_C — TP_SATA_RXD_P2_C MAKE_BASE=TRUE

HD POWER



PATA CONNECTOR



DISK CONNECTORS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 83 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK		P25MM	
ENET_RX_CLK		P25MM	
ENET_GBE_REF		P25MM	
ENET_TX_CLK		P25MM	
ENET_RX			
ENET_RX_CTL			
ENET_RX_CTL			
ENET_TX			
ENET_TX_CTL			
ENET_TX_CTL			
ENET_RX_CTL			
ENET_RX_CTL			
ENET_MDC			
ENET_MDIO			

ENET_CLK25M_TX 84 86
ENET_CLK125M_RX 84 86
ENET_CLK125M_GBE_REF 84 86
ENET_CLK125M_GTX 84 86
ENET_CLK125M_GTX_R 84
ENET_RXD<7..0> 84 86
ENET_RX_DV 84 86
ENET_RX_ER 84 86
ENET_TXD<7..0> 84 86
ENET_TX_EN 84 86
ENET_TX_ER 84 86
ENET_CRS 84 86
ENET_COL 84 86
ENET_MDC 84 86
ENET_MDIO 84 86

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U2300
SHASTA
V1.0
BGA
(6 OF 8)

ETHERNET

86 84 ENET_CLK25M_TX	H5	ETH_TX_CLK_H		
86 84 ENET_CLK125M_RX	J3	ETH_RX_CLK_H		
86 84 ENET_RXD<0>	K1	ETH_RXD_0_H	ETH_TXD_0_H	G4 ENET_TXD_R<0>
86 84 ENET_RXD<1>	L3	ETH_RXD_1_H	ETH_TXD_1_H	E1 ENET_TXD_R<1>
86 84 ENET_RXD<2>	K2	ETH_RXD_2_H	ETH_TXD_2_H	H4 ENET_TXD_R<2>
86 84 ENET_RXD<3>	J1	ETH_RXD_3_H	ETH_TXD_3_H	J5 ENET_TXD_R<3>
86 84 ENET_RXD<4>	L4	ETH_RXD_4_H	ETH_TXD_4_H	G3 ENET_TXD_R<4>
86 84 ENET_RXD<5>	K3	ETH_RXD_5_H	ETH_TXD_5_H	F2 ENET_TXD_R<5>
86 84 ENET_RXD<6>	J2	ETH_RXD_6_H	ETH_TXD_6_H	J4 ENET_TXD_R<6>
86 84 ENET_RXD<7>	G1	ETH_RXD_7_H	ETH_TXD_7_H	K6 ENET_TXD_R<7>
86 84 ENET_RX_DV	K4	ETH_RX_DV_H	ETH_TX_EN_H	H3 ENET_TX_EN_R
86 84 ENET_RX_ER	G2	ETH_RX_ER_H	ETH_TX_ER_H	F1 ENET_TX_ER_R
86 84 ENET_CLK125M_GBE_REF	M5	ETH_REFCLK_H	ETH_GTX_CLK_H	K5 84 ENET_CLK125M_GTX_R
86 84 ENET_CRS	L6	ETH_CRS_H	ETH_MDC_H	M4 ENET_MDC 84 86
86 84 ENET_COL	L5	ETH_COL_H	ETH_MDIO_H	M6 ENET_MDIO 84 86

RP8400 0 2 7 5% 1/16W SM-LF ENET_TXD<0> 84 86
RP8400 0 4 5 5% 1/16W SM-LF ENET_TXD<1> 84 86
RP8400 0 1 8 5% 1/16W SM-LF ENET_TXD<2> 84 86
RP8400 0 3 6 5% 1/16W SM-LF ENET_TXD<3> 84 86
RP8401 0 2 7 5% 1/16W SM-LF ENET_TXD<4> 84 86
RP8401 0 4 5 5% 1/16W SM-LF ENET_TXD<5> 84 86
RP8401 0 1 8 5% 1/16W SM-LF ENET_TXD<6> 84 86
RP8401 0 3 6 5% 1/16W SM-LF ENET_TXD<7> 84 86
R8400 0 1 2 5% 1/16W MF-LF 402 ENET_TX_EN 84 86
R8401 0 1 2 5% 1/16W MF-LF 402 ENET_TX_ER 84 86
R8402 0 1 2 5% 1/16W MF-LF 402 ENET_CLK125M_GTX 84 86

Shasta Ethernet

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 84 OF 102	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	P25MM			ENET_CLK125M_GBE_REF_R
	P25MM			ENET_CLK125M_RX_R
	P25MM			ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_P<0>
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_N<0>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_P<1>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_N<1>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_P<2>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_N<2>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_P<3>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_N<3>
VESTA_CLK25M_XTALI	P25MM			VESTA_CLK25M_XTALI
	P25MM			VESTA_CLK25M_XTALO
	P25MM			VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- _PP3V3_ENET
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38 mms
Length Tolerance: 50 mils
Primary Max Sep: 5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

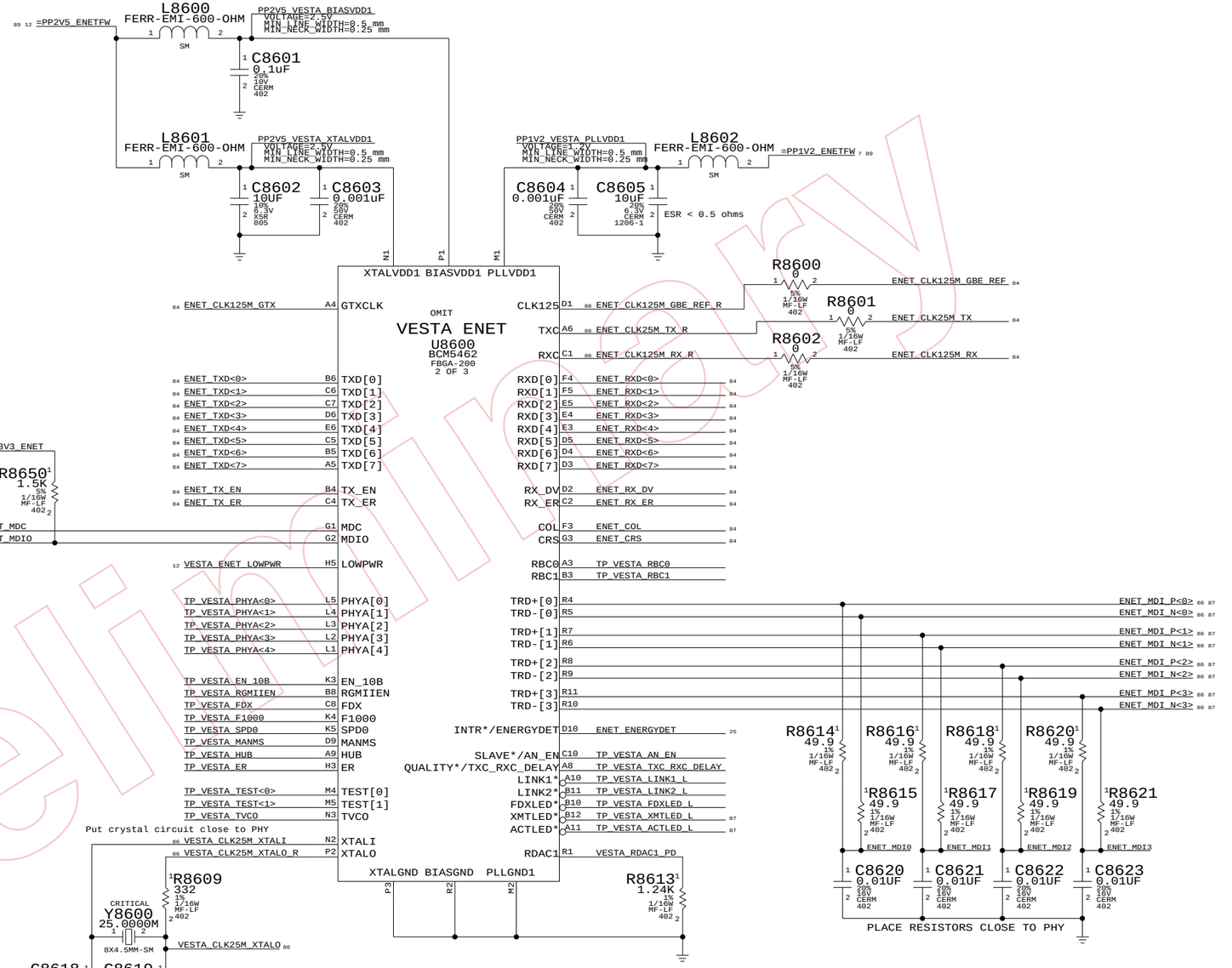
HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

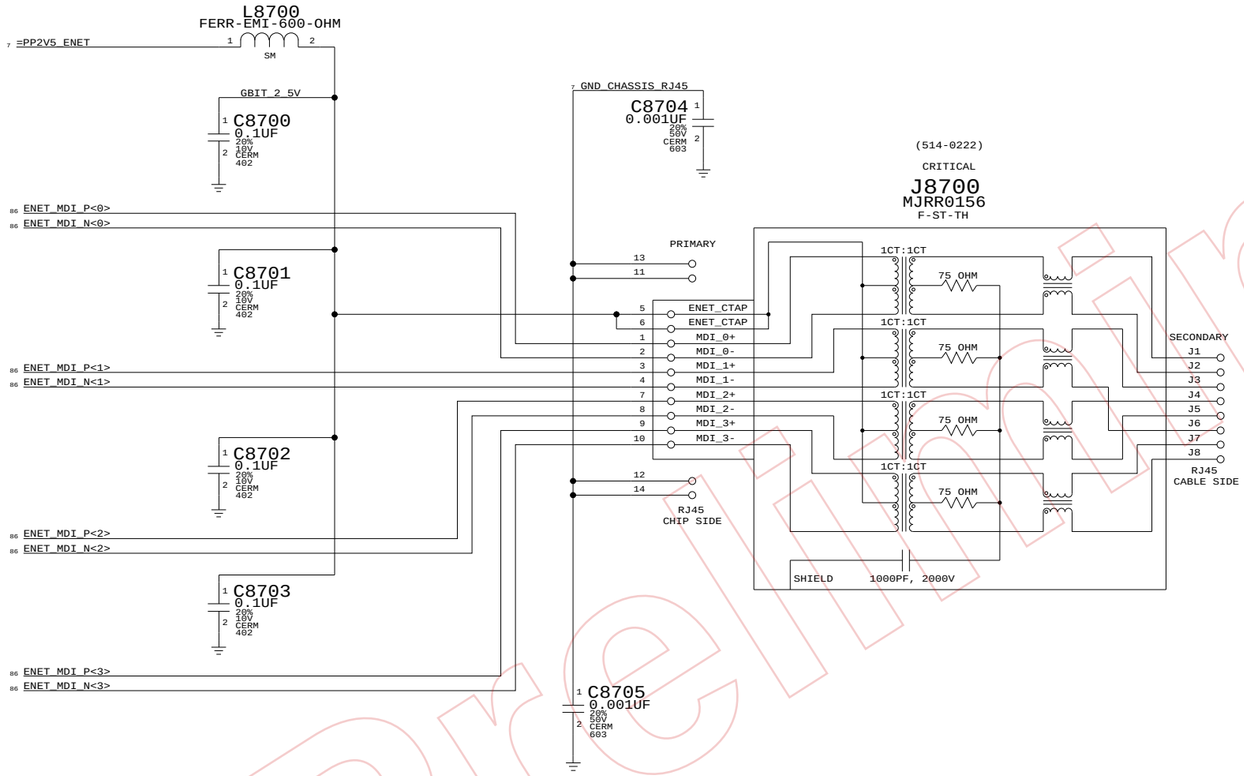


Vesta Ethernet PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 86 OF 102	



ETHERNET CONNECTOR

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 87 OF 102	

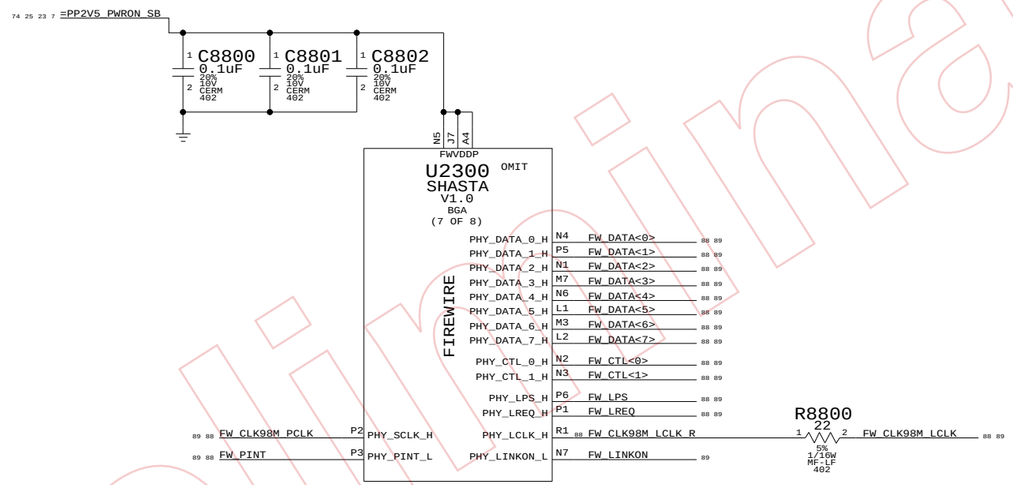
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW			
FW			
FW_LPS			
FW_LREQ			
FW_PINT			
FW_LCLK		P25MM	
FW_PCLK		P25MM	
		P25MM	

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Shasta FireWire

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 88 OF 102	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	P38MM	CLOCKS		FW_CLK98M_PCLK_R
FW_TPA1	FW	FW	FW_TPA0	FW_TPA_P<0>
FW_TPA1	FW	FW	FW_TPA0	FW_TPA_N<0>
FW_TPB1	FW	FW	FW_TPB0	FW_TPB_P<0>
FW_TPB1	FW	FW	FW_TPB0	FW_TPB_N<0>
FW_TPA2	FW	FW	FW_TPA1	FW_TPA_P<1>
FW_TPA2	FW	FW	FW_TPA1	FW_TPA_N<1>
FW_TPB2	FW	FW	FW_TPB1	FW_TPB_P<1>
FW_TPB2	FW	FW	FW_TPB1	FW_TPB_N<1>
FW_TPA3	FW	FW	FW_TPA2	FW_TPA_P<2>
FW_TPA3	FW	FW	FW_TPA2	FW_TPA_N<2>
FW_TPB3	FW	FW	FW_TPB2	FW_TPB_P<2>
FW_TPB3	FW	FW	FW_TPB2	FW_TPB_N<2>
VESTA_CLK24M_XTALI	P38MM			VESTA_CLK24M_XTALI
	P38MM			VESTA_CLK24M_XTALO
	P38MM			VESTA_CLK24M_XTALO_R

Page Notes

Power aliases required by this page:
- _PPFW_PHY
- _PP3V3_FW
- _PP3V3_ENETFW
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

L8900 FERR-EMI-600-OHM SM — PP1V2_VESTA_PLLVDD2 VOLTAGE=1.2V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP1V2_ENETFW
C8900 10uF 20% 6.3V CERM 1206-1 (ESR < 0.5 ohms)
C8901 0.001uF 20% 50V CERM 402

L8901 FERR-EMI-600-OHM SM — PP2V5_VESTA_BIASVDD2 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP2V5_ENETFW
C8903 0.1uF 20% 10V CERM 402

L8902 FERR-EMI-600-OHM SM — PP2V5_VESTA_XTALVDD2 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
C8904 10UF 10% 6.3V X5R 805
C8905 0.001uF 20% 50V CERM 402

L8906 FERR-EMI-600-OHM SM — PP3V3_VESTA_FAVDDH VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP3V3_ENETFW
C8906 0.1uF 20% 10V CERM 402
C8907 0.1uF 20% 10V CERM 402
C8908 0.1uF 20% 10V CERM 402
C8917 10UF 10% 6.3V X5R 805

L8909 FERR-EMI-600-OHM SM — PP2V5_VESTA_FAVDDM VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP2V5_ENETFW
C8909 0.1uF 20% 10V CERM 402
C8911 0.1uF 20% 10V CERM 402
C8918 10UF 10% 6.3V X5R 805

L8913 FERR-EMI-600-OHM SM — PP1V2_VESTA_FAVDDL VOLTAGE=1.2V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm — =PP1V2_ENETFW
C8913 0.1uF 20% 10V CERM 402
C8914 0.1uF 20% 10V CERM 402
C8915 0.1uF 20% 10V CERM 402
C8919 10UF 10% 6.3V X5R 805

=PPFW_PHY
R8914 390K 5% 1/10W MF-LF 402

=PP3V3_FW
VESTA_DS_ONLY_EN0
R8911 10K 5% 1/10W MF-LF 402

VESTA_PWR_CLASS_0
R8912 10K 5% 1/10W MF-LF 402

Put crystal circuit close to PHY

CRITICAL
Y8920 24.576M 8X4.5MM-SM
C8920 22pF 5% 50V CERM 402
C8921 22pF 5% 50V CERM 402
R8921 332 1% 1/10W MF-LF 402
R8903 1K 1% 1/10W MF-LF 402
R8904 10K 1% 1/10W MF-LF 402

CRYSTAL LOAD CAPACITANCE IS 12PF

RP8900 22 5% 1/10W SM-LF — FW_DATA<0>
RP8900 22 5% 1/10W SM-LF — FW_DATA<1>
RP8900 22 5% 1/10W SM-LF — FW_DATA<2>
RP8901 22 5% 1/10W SM-LF — FW_DATA<3>
RP8901 22 5% 1/10W SM-LF — FW_DATA<4>
RP8901 22 5% 1/10W SM-LF — FW_DATA<5>
RP8901 22 5% 1/10W SM-LF — FW_DATA<6>
RP8900 22 5% 1/10W SM-LF — FW_DATA<7>
R8900 22 5% 1/16W MF-LF 402 — FW_CTL<0>
R8901 22 5% 1/16W MF-LF 402 — FW_CTL<1>

VESTA_BILINGUAL_EN12
R8931 10K 5% 1/10W MF-LF 402
R8933 10K 5% 1/10W MF-LF 402
R8935 10K 5% 1/10W MF-LF 402
VESTA_PORT1_DISABLE
VESTA_PORT2_DISABLE
VESTA_BILINGUAL_EN12_L
VESTA_PORT1_DISABLE_L
VESTA_PORT2_DISABLE_L

VESTA FW U8600 BCM5462 FBGA-209 3 OF 3 (OMIT)

FW_CPS	R13	CPS
(Int PU) VESTA_BILINGUAL_EN12_L	C11	ESDET0
(Int PU) VESTA_PORT1_DISABLE_L	C12	ESDET1
(Int PU) VESTA_PORT2_DISABLE_L	C13	ESDET2
FW_CLK98M_LCLK	D15	PLI_LCLK
FW_DATA_R<0>	E12	PLI_DATA[0]
FW_DATA_R<1>	E11	PLI_DATA[1]
FW_DATA_R<2>	F11	PLI_DATA[2]
FW_DATA_R<3>	F12	PLI_DATA[3]
FW_DATA_R<4>	F13	PLI_DATA[4]
FW_DATA_R<5>	G13	PLI_DATA[5]
FW_DATA_R<6>	G12	PLI_DATA[6]
FW_DATA_R<7>	G11	PLI_DATA[7]
FW_CTL_R<0>	E14	PLI_CTL[0]
FW_CTL_R<1>	E13	PLI_CTL[1]
FW_LPS	D11	PLI_LPS
FW_LREQ	D12	PLI_LREQ
FW_LOWPWR	J3	LPWR_1394
VESTA_DS_ONLY_EN0	A13	DS_ONLY_EN0 Internal Pull-Down
VESTA_PWR_CLASS	A12	PWR_CLASS Internal Pull-Up
TP_VESTA_TEST_1394<0>	J5	TEST_1394[0]
TP_VESTA_TEST_1394<1>	J4	TEST_1394[1]
TP_VESTA_TVCO_24	N13	TVCO_24
VESTA_CLK24M_XTALI	P14	XTALI_24
VESTA_CLK24M_XTALO_R	P13	XTALO_24
BIASGND	P12	
PLLGND2	N14	
FAVDDH	K11 K12 K13	
FAVDDM	L11 L12 M11 M12	
FAVDDL	L10 M10 N11 N12	
XTALVDD2	N15	
BIASVDD2	R14	
PLLVDD2	P15	

TDBL[0]	A14	TP_VESTA_TDBL<0>
TDBL[1]	B13	TP_VESTA_TDBL<1>
TDBL[2]	B14	TP_VESTA_TDBL<2>
PLI_PCLK	E15	FW_CLK98M_PCLK_R
PLI_INT	D13	FW_PINT
PLI_LINK	D14	FW_LINKON
TPBIAS[0]	L13	FW_TPBIAS<0> (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm)
TPAP[0]	L15	FW_TPA_P<0>
TPAN[0]	L14	FW_TPA_N<0>
TPBP[0]	M15	FW_TPB_P<0>
TPBN[0]	M14	FW_TPB_N<0>
TPBIAS[1]	J13	FW_TPBIAS<1> (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm)
TPAP[1]	J15	FW_TPA_P<1>
TPAN[1]	J14	FW_TPA_N<1>
TPBP[1]	K15	FW_TPB_P<1>
TPBN[1]	K14	FW_TPB_N<1>
TPBIAS[2]	H13	FW_TPBIAS<2> (MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm)
TPAP[2]	G15	FW_TPA_P<2>
TPAN[2]	G14	FW_TPA_N<2>
TPBP[2]	H15	FW_TPB_P<2>
TPBN[2]	H14	FW_TPB_N<2>
SDC	H1	I2C_VESTA_SCL
SDA	H2	I2C_VESTA_SDA
RDAC2	R15	VESTA_RDAC2_PD

R8902 22 5% 1/10W MF-LF 402 — FW_CLK98M_PCLK
R8909 2.0K 1% 1/10W MF-LF 402
R8915 10K 5% 1/10W MF-LF 402 — =PP3V3_FW
R8916 10K 5% 1/10W MF-LF 402 — (I2C_VESTA_SDA) (I2C_VESTA_SCL)

Vesta FireWire PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 89 OF 102	

NET_TYPE				
SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	90
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	90
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	90
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	90
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	90
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	90
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	90
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	90

8 WATTS MAX

24 VOLTS

PP24V_RUN

R9056 1 3 20% 1W FF 2512

PP24V_FW MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V MAKE_BASE=TRUE

=PPFW_PHY 89

D9000 MURS320XXG SMC

C9009 0.1UF 10% 50V CERM 805

CRITICAL

R9002 1 3 20% 1W FF 2512

PP24V_FW_D MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

PP24V_FW_R MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

L9001 FERR-160-OHM 1206

FW_VP VOLTAGE=24V MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM

F9002 0.5AMP SM

PPFW_PORT0_VP VOLTAGE=33V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

F9000 1.5AMP-33V SM

PPFW_PORT1_VP 90 VOLTAGE=33V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

Termination

Place close to FireWire PHY

89 FW_TPBIAS<1>
89 FW_TPBIAS<0>

C9050 1uF 10% 6.3V CERM 402

C9060 1uF 10% 6.3V CERM 402

R9050 56.2 1% 1/10W MF-LF 402
R9051 56.2 1% 1/10W MF-LF 402
R9060 56.2 1% 1/10W MF-LF 402
R9061 56.2 1% 1/10W MF-LF 402

89 FW_TPA_P<0> — FW_PORT0_TPA_P 90 MAKE_BASE=TRUE
89 FW_TPA_N<0> — FW_PORT0_TPA_N 90 MAKE_BASE=TRUE
89 FW_TPB_P<0> — FW_PORT0_TPB_P 90 MAKE_BASE=TRUE
89 FW_TPB_N<0> — FW_PORT0_TPB_N 90 MAKE_BASE=TRUE
89 FW_TPA_P<1> — FW_PORT1_TPA_P 90 MAKE_BASE=TRUE
89 FW_TPA_N<1> — FW_PORT1_TPA_N 90 MAKE_BASE=TRUE
89 FW_TPB_P<1> — FW_PORT1_TPB_P 90 MAKE_BASE=TRUE
89 FW_TPB_N<1> — FW_PORT1_TPB_N 90 MAKE_BASE=TRUE

R9052 56.2 1% 1/10W MF-LF 402
R9053 56.2 1% 1/10W MF-LF 402
R9062 56.2 1% 1/10W MF-LF 402
R9063 56.2 1% 1/10W MF-LF 402

FW_TPA_C<0>

C9054 270pF 5% 50V CERM 402

R9054 4.99K 1% 1/10W MF-LF 402

FW_TPA_C<1>

C9064 270pF 5% 50V CERM 402

R9064 4.99K 1% 1/10W MF-LF 402

3rd TPA/TPB pair unused

89 FW_TPBIAS<2> — NC_FW_TPBIAS2 MAKE_BASE=TRUE NO_TEST=YES
89 FW_TPA_P<2> — NC_FW_TPA_P2 MAKE_BASE=TRUE NO_TEST=YES
89 FW_TPA_N<2> — NC_FW_TPA_N2 MAKE_BASE=TRUE NO_TEST=YES
89 FW_TPB_P<2> — FW_TPB2_PD MAKE_BASE=TRUE NO_TEST=YES
89 FW_TPB_N<2>

R9070 1K 5% 1/10W MF-LF 402

ESD Rail

89 7 =PP3V3_FW — R9090 665 1% 1/10W MF-LF 402 — PP3V3_FW_ESD_F VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm — L9090 400-OHM-EMI SM-1 — PP3V3_FW_ESD 90 VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

D9090 SOT23 BZX84C2V7-X-F

"Snapback" & "Late VG" Protection

90 PP3V3_FW_ESD

DP9010 BAV99DW-X-F SOT-363

C9010 0.001uF 20% 50V CERM 402

C9011 0.001uF 20% 50V CERM 402

DP9011 BAV99DW-X-F SOT-363

C9012 0.001uF 20% 50V CERM 402

C9013 0.001uF 20% 50V CERM 402

90 FW_PORT0_TPA_P
90 FW_PORT0_TPA_N
90 FW_PORT0_TPB_P
90 FW_PORT0_TPB_N

FL9010 165-OHM SM SYM_VER-1

FL9011 165-OHM SM SYM_VER-1

R9010 0 5% 1/8W MF-LF 805

(PPFW_PORT0_VP)

GND_FW_PORT0_VG VOLTAGE=0V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

C9015 0.01uF 20% 16V CERM 402

C9016 0.01uF 20% 16V CERM 402

PORT 0 1394A

CRITICAL J9000 FWS22 F-ST-TH

90 FW_PORT0_TPA_P_FL — TPO (TPA+)
90 FW_PORT0_TPA_N_FL — TPO# (TPA-)
90 FW_PORT0_TPB_P_FL — TPI (TPB+)
90 FW_PORT0_TPB_N_FL — TPI# (TPB-)
(PPFW_PORT0_VP) — VP
GND_FW_PORT0_VG — VGND

514-0202

GND_CHASSIS_FIREWIRE 7 90

"Snapback" & "Late VG" Protection

90 PP3V3_FW_ESD

DP9020 BAV99DW-X-F SOT-363

C9020 0.001uF 20% 50V CERM 402

C9021 0.001uF 20% 50V CERM 402

DP9021 BAV99DW-X-F SOT-363

C9022 0.001uF 20% 50V CERM 402

C9023 0.001uF 20% 50V CERM 402

90 FW_PORT1_TPA_P
90 FW_PORT1_TPA_N
90 FW_PORT1_TPB_P
90 FW_PORT1_TPB_N

FL9020 165-OHM SM SYM_VER-1

FL9021 165-OHM SM SYM_VER-1

R9020 0 5% 1/8W MF-LF 805

(PPFW_PORT1_VP)

GND_FW_PORT1_VG VOLTAGE=0V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

C9025 0.01uF 20% 16V CERM 402

C9026 0.01uF 20% 16V CERM 402

PPFW_PORT1_VP 90

PORT 1 1394A

CRITICAL J9001 FWS22 F-ST-TH

90 FW_PORT1_TPA_P_FL — TPO (TPA+)
90 FW_PORT1_TPA_N_FL — TPO# (TPA-)
90 FW_PORT1_TPB_P_FL — TPI (TPB+)
90 FW_PORT1_TPB_N_FL — TPI# (TPB-)
(PPFW_PORT1_VP) — VP
GND_FW_PORT1_VG — VGND

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GND_CHASSIS_FIREWIRE 7 90

FIREWIRE CONNECTORS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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D	051-6772	11

SCALE	SHT	OF
NONE	90	102

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0> 91 92
USB2_0	USB2	USB2	USB2_0	USB2_N<0> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_P<1> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_N<1> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_P<2> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_N<2> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_P<3> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_N<3> 91 92
USB2_4	USB2	USB2	USB2_4	USB2_P<4> 76 91
USB2_4	USB2	USB2	USB2_4	USB2_N<4> 76 91
USB2_NEC_XTAL		P25MM		NEC_CLK30M_XT1 91
		P25MM		NEC_CLK30M_XT2 91
		P25MM		NEC_CLK30M_XT2_R 91

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300
SHASTA
V1.0
BGA
(8 OF 8)
OMIT

NC0	P7	TP_SB_NC_P7	6
NC1	P8	TP_SB_NC_P8	6
NC2	R3	TP_SB_NC_R3	6
NC3	R4	TP_SB_NC_R4	6
NC4	R5	TP_SB_NC_R5	6
NC5	R6	TP_SB_NC_R6	6
NC6	R7	TP_SB_NC_R7	6
NC7	R8	TP_SB_NC_R8	6
NC8	T1	TP_SB_NC_T1	6
NC9	T2	TP_SB_NC_T2	6
NC10	T3	TP_SB_NC_T3	6
NC11	T4	TP_SB_NC_T4	6
NC12	T5	TP_SB_NC_T5	6
NC13	T6	TP_SB_NC_T6	6
NC14	T7	TP_SB_NC_T7	6
NC15	T8	TP_SB_NC_T8	6
NC16	U1	TP_SB_NC_U1	6
NC17	U2	TP_SB_NC_U2	6
NC18	U3	TP_SB_NC_U3	6
NC19	U4	TP_SB_NC_U4	6
NC20	U5	TP_SB_NC_U5	6
NC21	U6	TP_SB_NC_U6	6
NC22	V1	TP_SB_NC_V1	6
NC23	V2	TP_SB_NC_V2	6
NC24	V3	TP_SB_NC_V3	6
NC25	V4	TP_SB_NC_V4	6
NC26	W1	TP_SB_NC_W1	6
NC27	W3	TP_SB_NC_W3	6
NC28	Y1	TP_SB_NC_Y1	6
NC29	Y3	TP_SB_NC_Y3	6

91 7 =PP3V3_PWRON_USB
L9135 FERR-EMI-100-OHM SM
R9135 4.7 5% 1/10W MF-LF 603
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
NOSTUFF C9135 10uF 20% 6.3V CERM 805
C9136 0.1uF 20% 10V CERM 402
C9137 0.1uF 20% 10V CERM 402
GND_NEC_AVSS_R 91
NOSTUFF C9120 10uF 20% 6.3V CERM 805
C9121 0.1uF 20% 10V CERM 402
C9122 0.1uF 20% 10V CERM 402
C9123 0.1uF 20% 10V CERM 402
C9124 0.1uF 20% 10V CERM 402
C9125 0.1uF 20% 10V CERM 402
C9126 0.1uF 20% 10V CERM 402
C9127 0.1uF 20% 10V CERM 402
C9128 0.1uF 20% 10V CERM 402
C9129 0.1uF 20% 10V CERM 402
C9130 0.1uF 20% 10V CERM 402
P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 VDD
N10 N12 AVDD
CRITICAL
U7700
NEC_UPD720101_USB2
FBGA
R9100 36 1% 1/16W MF-LF 402
R9101 36 1% 1/16W MF-LF 402
R9102 36 1% 1/16W MF-LF 402
R9103 36 1% 1/16W MF-LF 402
R9104 36 1% 1/16W MF-LF 402
R9105 36 1% 1/16W MF-LF 402
R9106 36 1% 1/16W MF-LF 402
R9107 36 1% 1/16W MF-LF 402
R9108 36 1% 1/16W MF-LF 402
R9109 36 1% 1/16W MF-LF 402

RSDM1	M14	USB_NEC_N<0>	USB2_N<0> 91 92
DM1	M13	(USB2_N<0>)	
DP1	L14	(USB2_P<0>)	USB2_P<0> 91 92
RSDP1	K13	USB_NEC_P<0>	
RSDM2	K14	USB_NEC_N<1>	USB2_N<1> 91 92
DM2	K12	(USB2_N<1>)	
DP2	J14	(USB2_P<1>)	USB2_P<1> 91 92
RSDP2	J12	USB_NEC_P<1>	
RSDM3	H11	USB_NEC_N<2>	USB2_N<2> 91 92
DM3	G11	(USB2_N<2>)	
DP3	G13	(USB2_P<2>)	USB2_P<2> 91 92
RSDP3	G14	USB_NEC_P<2>	
RSDM4	F12	USB_NEC_N<3>	USB2_N<3> 91 92
DM4	F14	(USB2_N<3>)	
DP4	E12	(USB2_P<3>)	USB2_P<3> 91 92
RSDP4	E14	USB_NEC_P<3>	
RSDM5	E13	USB_NEC_N<4>	USB2_N<4> 76 91
DM5	D14	(USB2_N<4>)	
DP5	C13	(USB2_P<4>)	USB2_P<4> 76 91
RSDP5	C14	USB_NEC_P<4>	

91 7 =PP3V3_PWRON_USB
R9110 10K 5% 1/16W MF-LF 402
RP9110 10K 5% 1/16W SM-LF

92 USB2_OC<0>	(USB2_OC<0>)	B12	OCI1
92 USB2_OC<1>	(USB2_OC<1>)	B11	OCI2
92 USB2_OC<2>	(USB2_OC<2>)	B10	OCI3
92 USB2_OC<3>	(USB2_OC<3>)	A10	OCI4
76 USB2_OC<4>	(USB2_OC<4>)	B9	OCI5
92 USB2_PWREN<0>		C12	PPON1
92 USB2_PWREN<1>		A11	PPON2
92 USB2_PWREN<2>		C11	PPON3
92 USB2_PWREN<3>		C10	PPON4
92 USB2_PWREN<4>		A9	PPON5

91 7 =PP3V3_PWRON_USB
R9140 1.5K 5% 1/16W MF-LF 402
R9141 1.5K 5% 1/16W MF-LF 402

NEC_NC1_PU	P6	NC1
NEC_NC2_PU	M6	NC2
91 NEC_CLK30M_XT1	L9	XT1/SCLK
91 NEC_CLK30M_XT2_R	P8	XT2

R9145 100 5% 1/16W MF-LF 402
CRITICAL
Y9145 30.0000M 11.4X4.7X4.2-SM
NEC_CLK30M_XT2 91
C9145 22pF 5% 50V CERM 402
C9146 22pF 5% 50V CERM 402
Y9145 LOAD CAPACITANCE IS ??PF

VSS
B1 N2 P10 M3 H3 B3 A2 D2 M2 N4 B5 M1 L1 H1 D1 G4 J1 F1 D8
XW9100 SM
AVSS AVSS(R) P1 M4 N1
RREF P11 NEC_RREF_PD
R9138 9.09K 1% 1/16W MF-LF 402
Tie to GND at ball N11
91 GND_NEC_AVSS_R
VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

USB Host Interfaces

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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SCALE: NONE	SHT: 91 OF 102	

External USB Ports

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F
	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

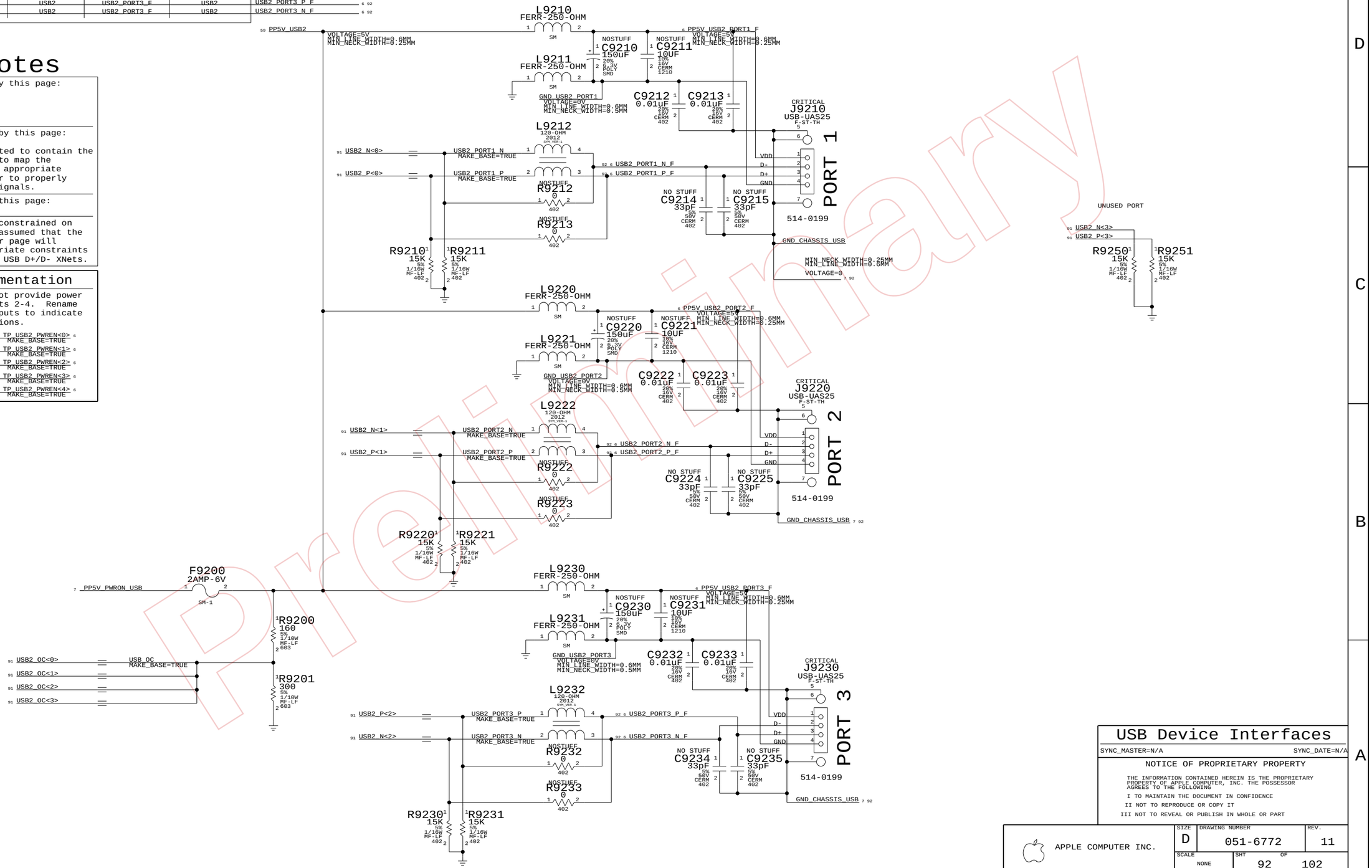
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- USB2_PWREN<0> → TP_USB2_PWREN<0> MAKE_BASE=TRUE
- USB2_PWREN<1> → TP_USB2_PWREN<1> MAKE_BASE=TRUE
- USB2_PWREN<2> → TP_USB2_PWREN<2> MAKE_BASE=TRUE
- USB2_PWREN<3> → TP_USB2_PWREN<3> MAKE_BASE=TRUE
- USB2_PWREN<4> → TP_USB2_PWREN<4> MAKE_BASE=TRUE



USB Device Interfaces

SYNC_MASTER=N/A SYNC_DATE=N/A

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Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

25 UDASH_SDOWN ═══ TP_UDASH_SDOWN
MAKE_BASE=TRUE

Q52 Modem Connector

SDF9400
STDOFF-4MM-9MMH-TH

CRITICAL
J9401
C104A-H9.0
F-ST-SM

94 7 PP3V3_PWRON_MODEM

C9450 10UF 20% 6.3V CERM 805

C9451 0.1UF 20% 10V CERM 402

PP3V3_PWRON_MODEM 7 94

R9451 10K 5% 1/16W MF-LF 402

6 25 MODEM_RING2SYS_L

MODEM_FC_RGDT

6 25 I2S1_SYNC

25 6 I2S1_SB_TO_DEV_DTO

6 25 I2S1_DEV_TO_SB_DTI

25 6 I2S1_RESET_L

25 6 I2S1_MCLK

6 25 I2S1_BITCLK

516S0116

SDF9401
STDOFF-4MM-9MMH-TH

GND_CHASSIS_MODEM

From Intel Mobile Audio/Modem
Daughter Card Specification
Rev 1.0, February 22, 1999

1 - MONO_OUT/PC_BEEP	2 - AUDIO_PWRON
3 - GND	4 - MONO_PHONE
5 - AUXA_RIGHT	6 - RESERVED
7 - AUXA_LEFT	8 - GND
9 - CD_GND	10 - 5Vmain
11 - CD_RIGHT	12 - RESERVED
13 - CD_LEFT	14 - RESERVED
15 - GND	16 - PRIMARY_DN
17 - 3.3Vaux	18 - 5Vd
19 - GND	20 - GND
21 - 3.3Vmain	22 - AC97_SYNC
23 - AC97_SDATA_OUT	24 - AC97_SDATA_INB
25 - AC97_RESET#	26 - AC97_SDATA_INA
27 - GND	28 - GND
29 - AC97_MSTRCLK	30 - AC97_BITCLK

RJ11 CONNECTOR

STUFFED AT FATP
SYMBOL USED FOR PLACEMENT

OMIT
J9402
RJ11-HGT27.5
ST-TH

514-0205

Modem Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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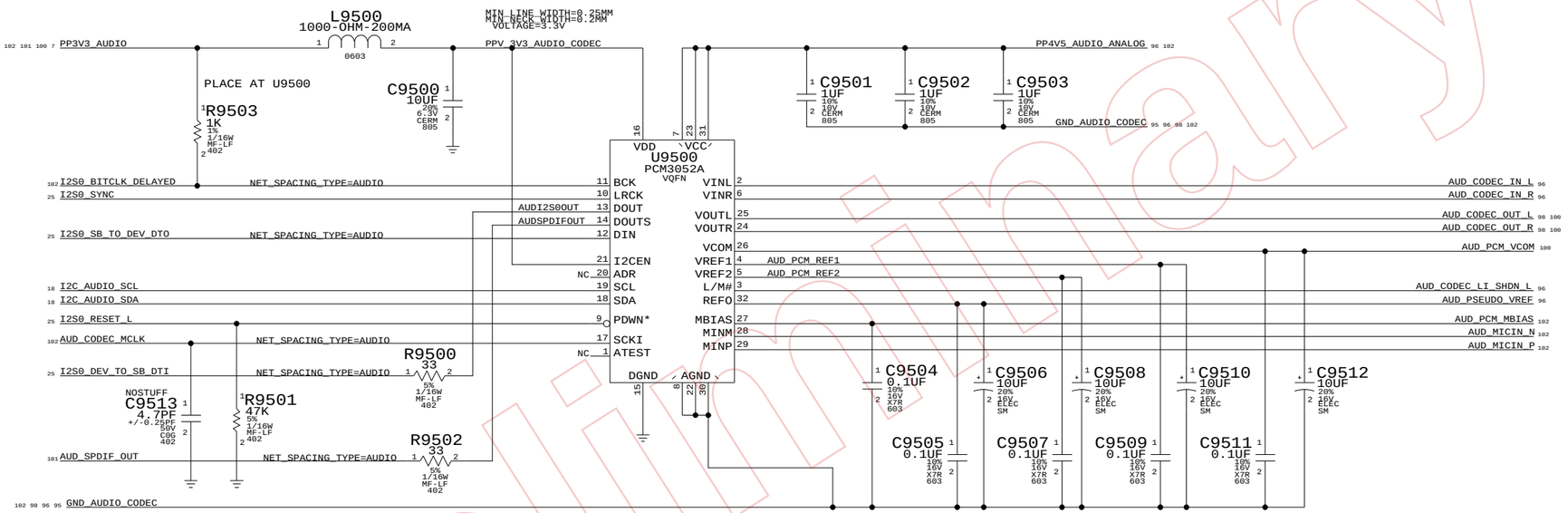
SCALE: NONE	SHT 94 OF 102	

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

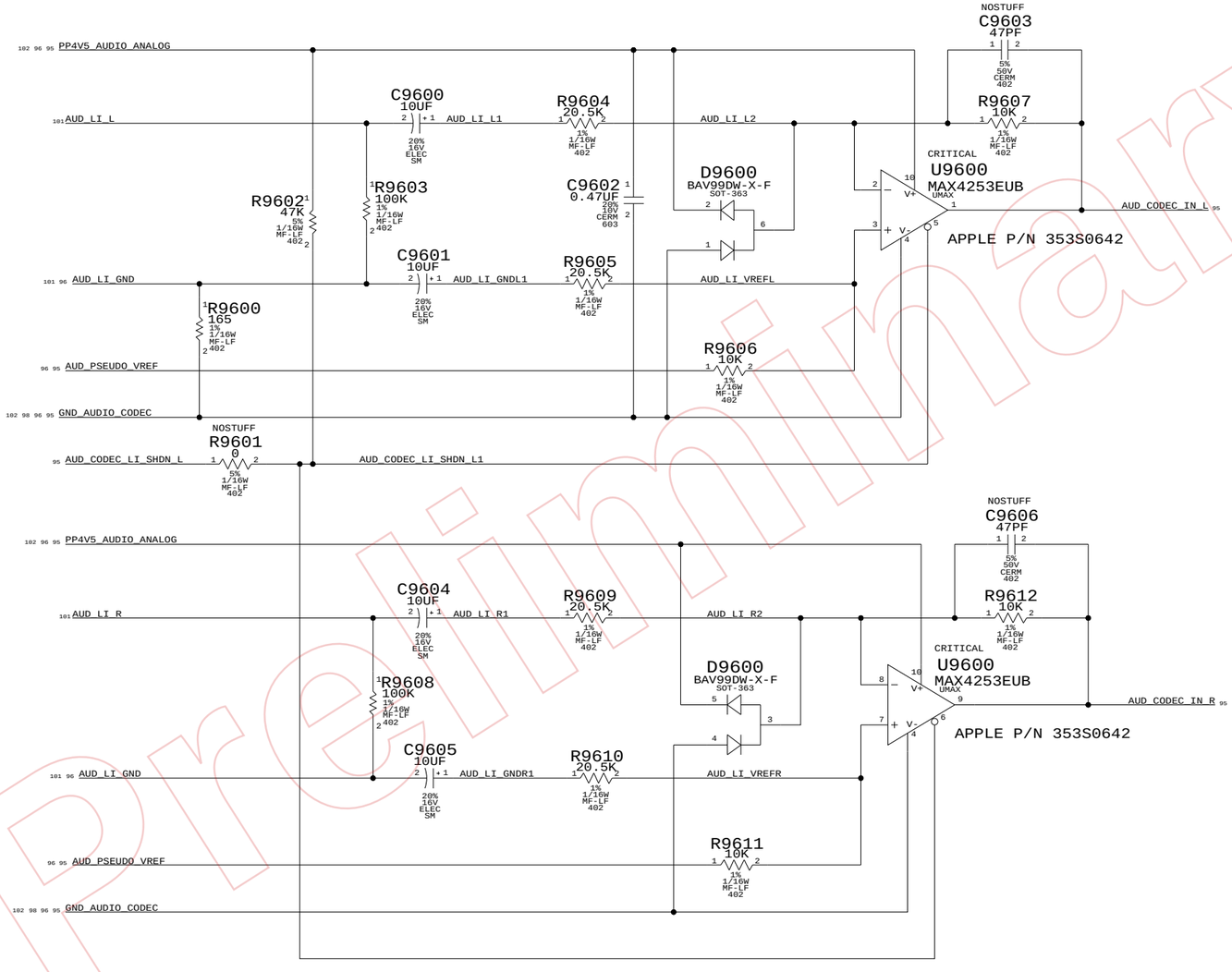
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 95 OF 102	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

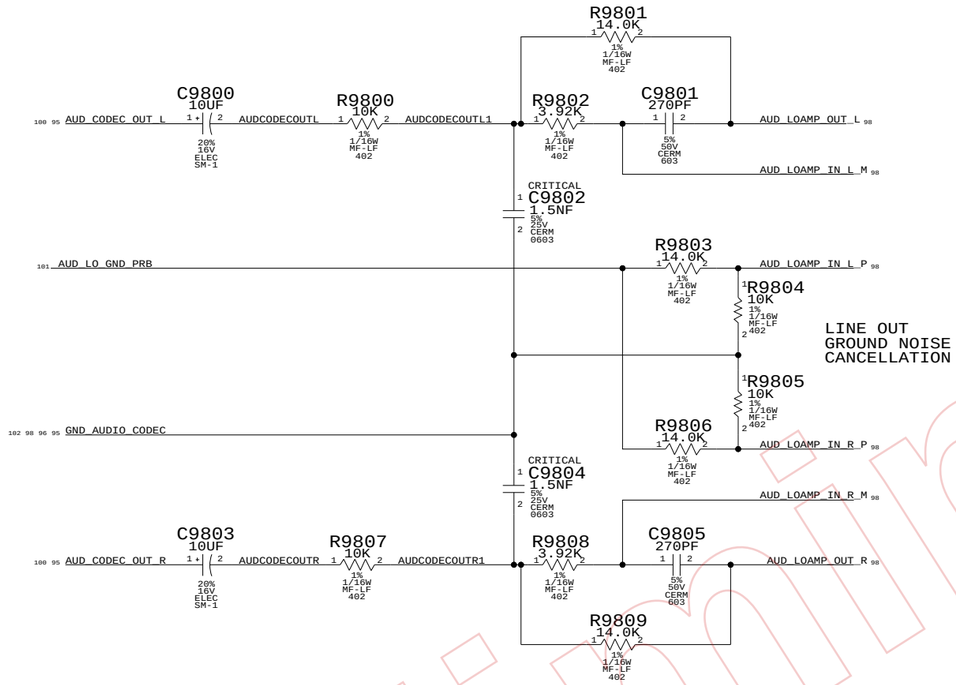
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 96 OF 102	

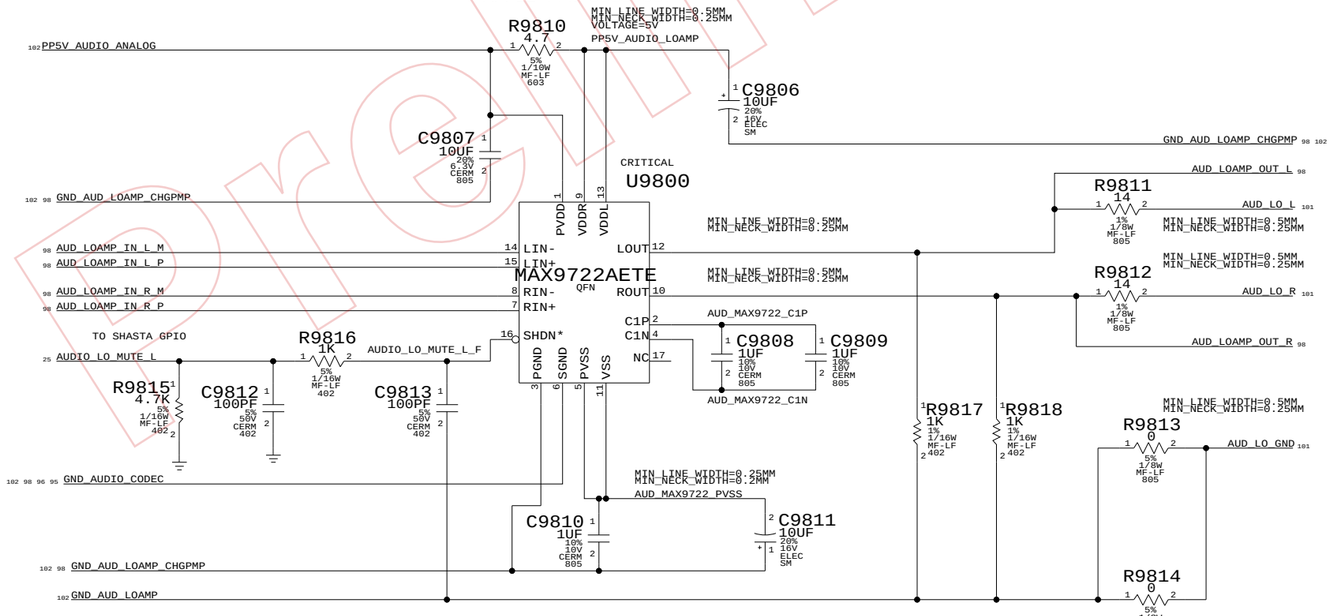
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

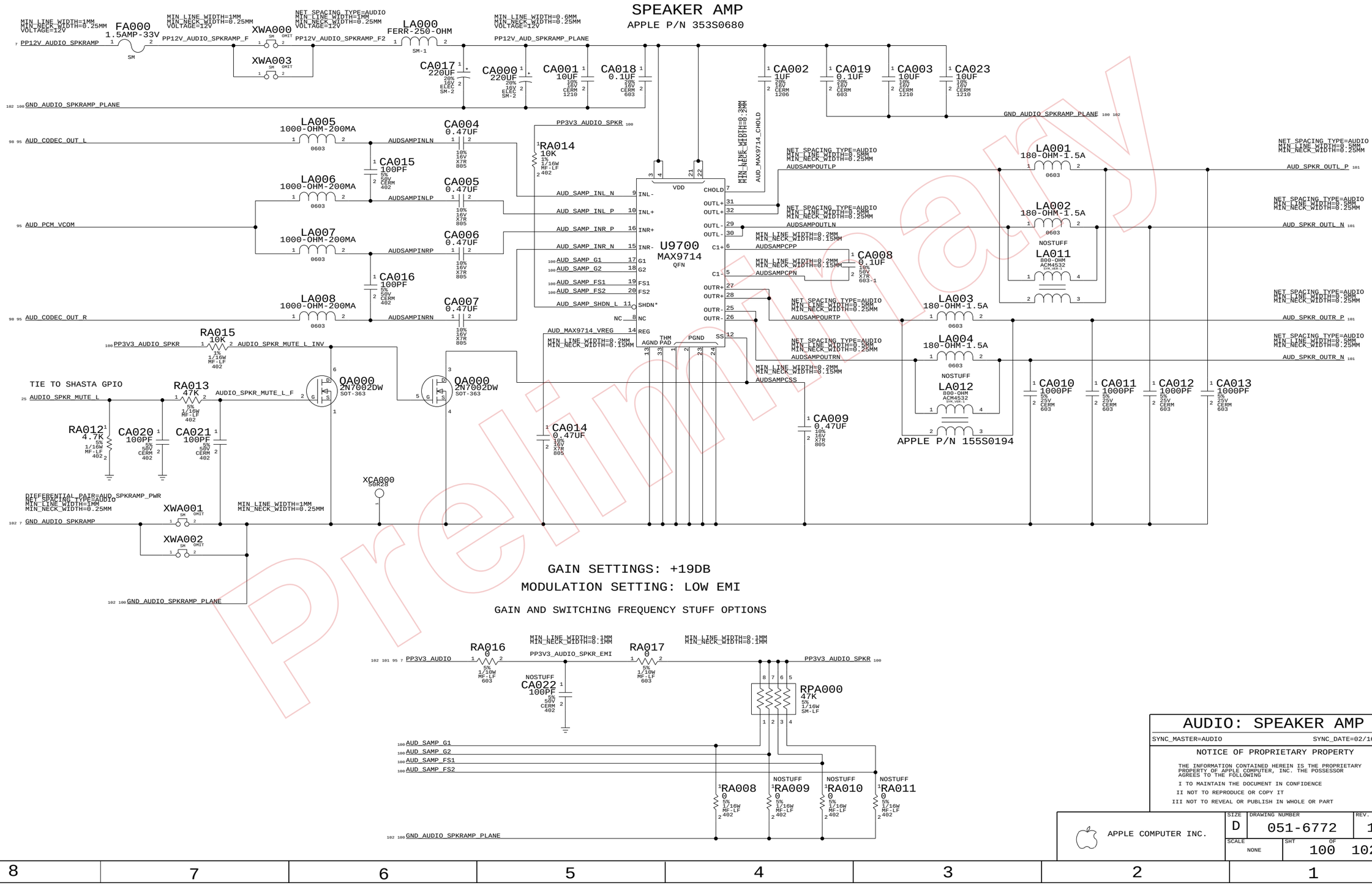
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 98 OF 102	

SPEAKER AMP

APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

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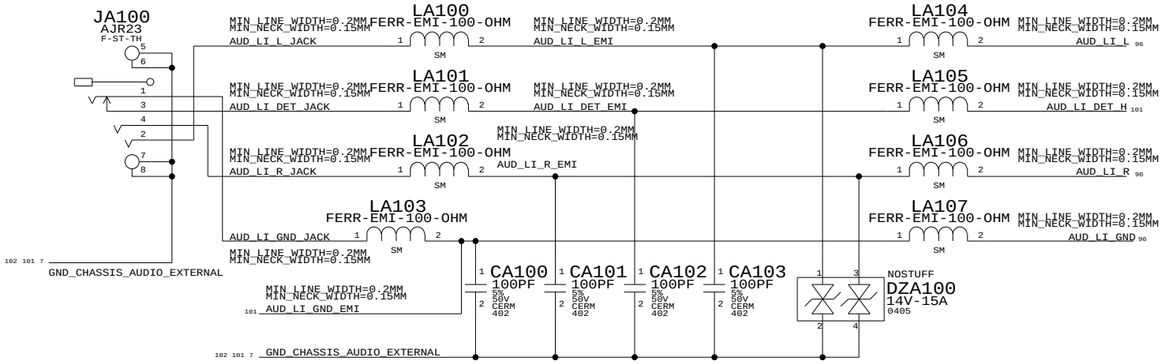
SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 100 OF 102	

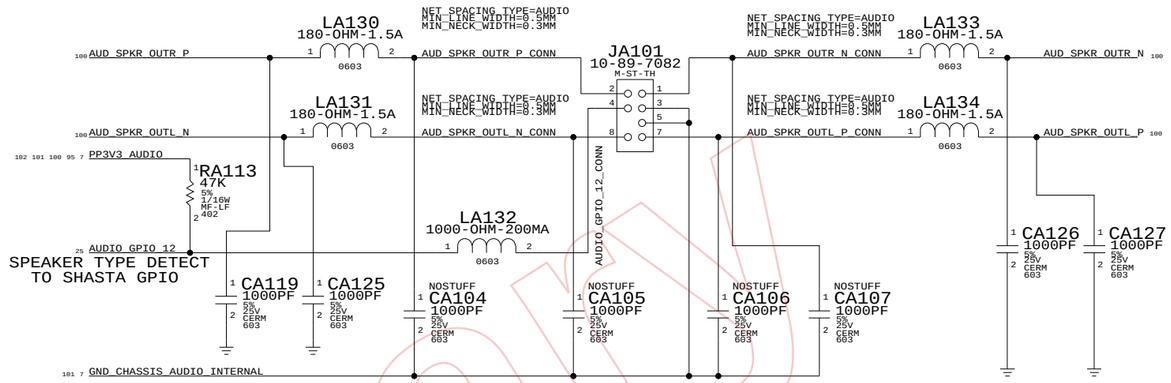
LINE IN JACK

APPLE P/N 514-0203



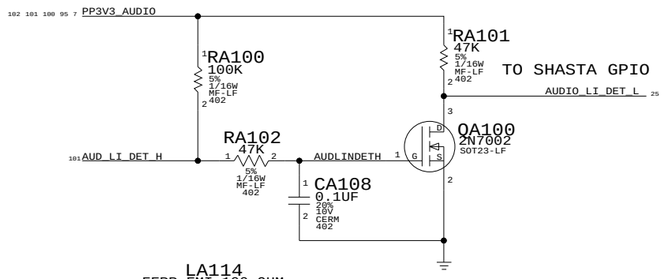
SPEAKER CABLE CONNECTOR

APPLE P/N 518-0138



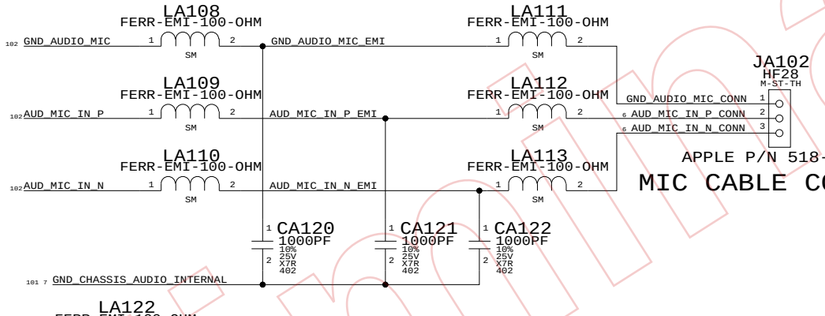
LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED



MIC CABLE CONNECTOR

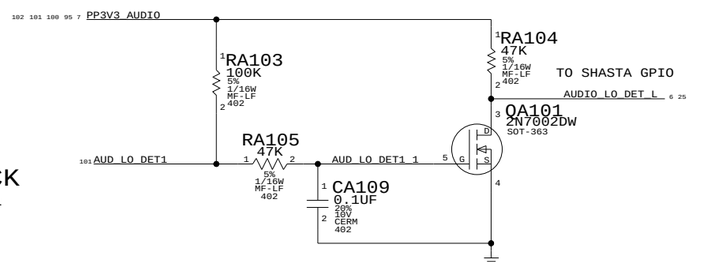
APPLE P/N 518-0034



LINE OUT PLUG DETECTS

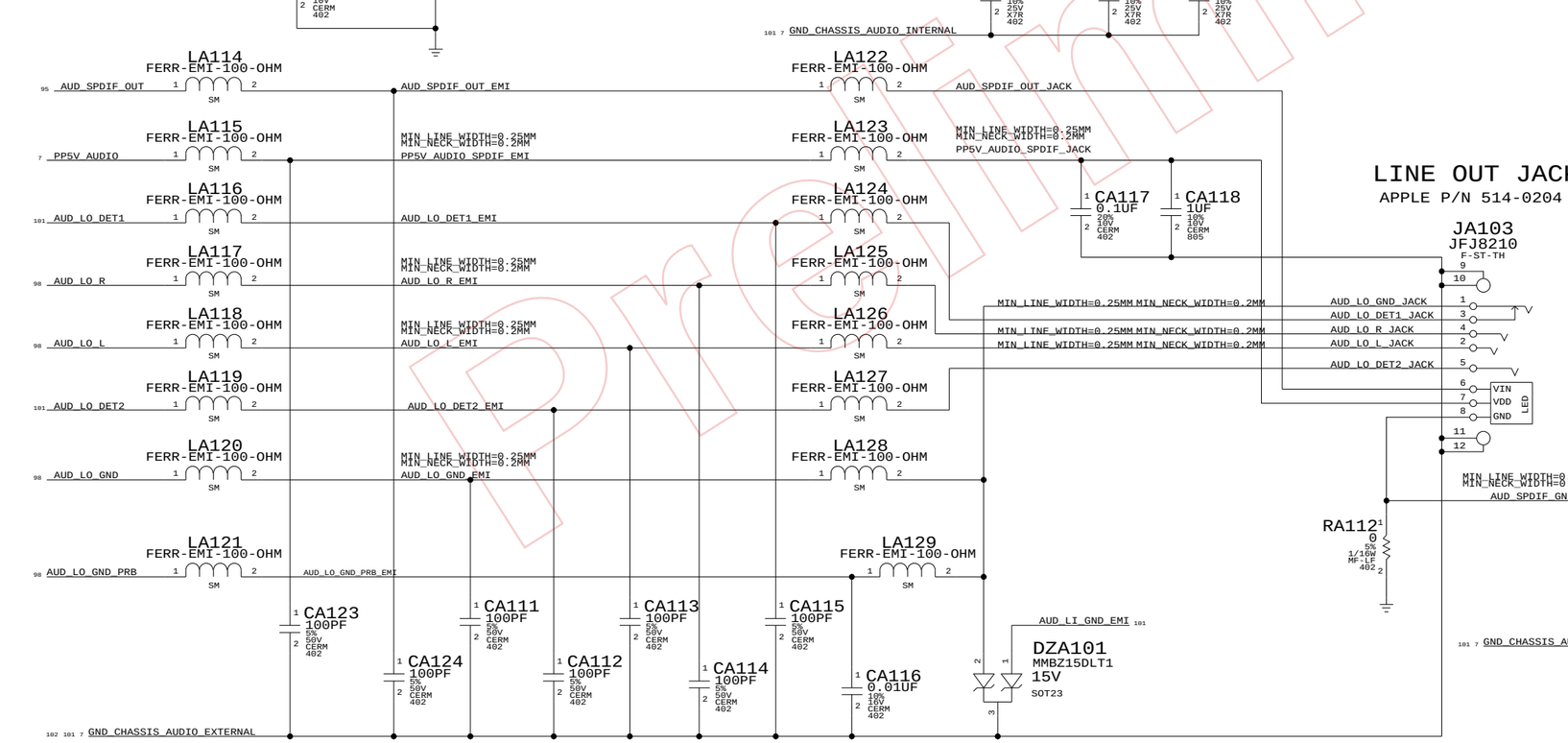
AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK

APPLE P/N 514-0204



AUDIO: Q45 CONNECTORS

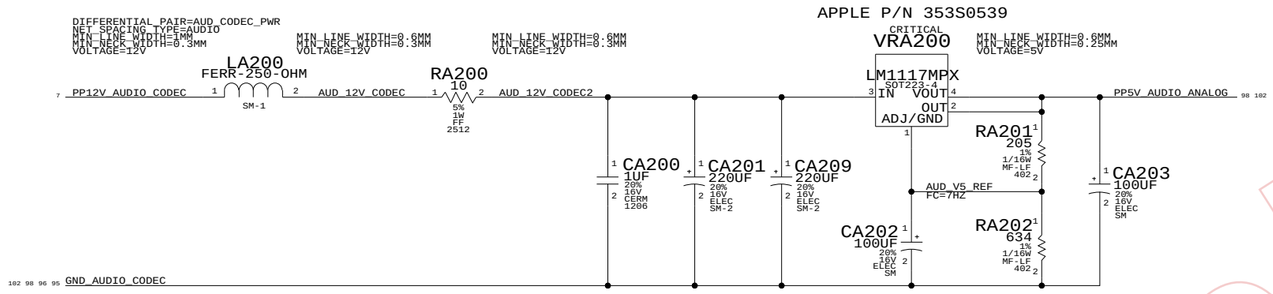
SYNC_MASTER=AUDIO SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 101 OF 102	

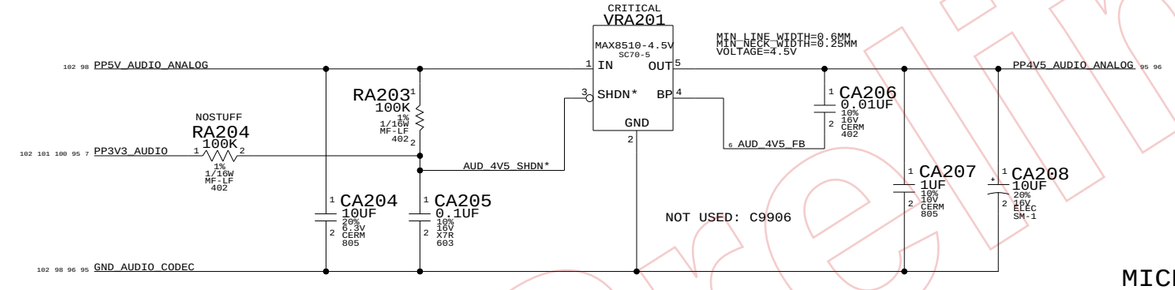
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0655	353S0933		U9500	PCM3052

5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP

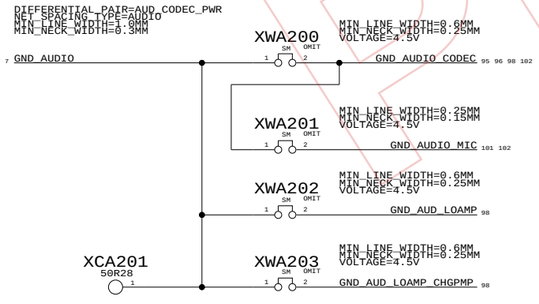


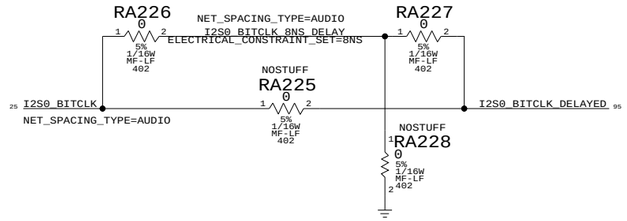
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733



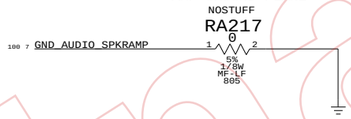
AUDIO GROUND RETURNS



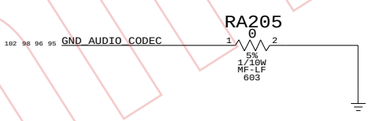


PLACE ACROSS GROUND SPLIT
AT RIGHT SIDE OF CA007

PLACE NEAR ENTRY TO SPEAKER
AMP GROUND PLANE

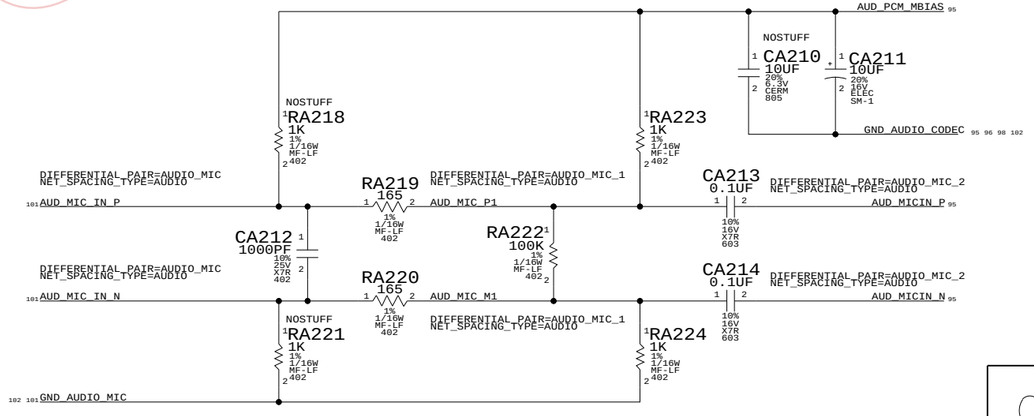


PLACE ACROSS GROUND SPLIT
AT CODEC U9500

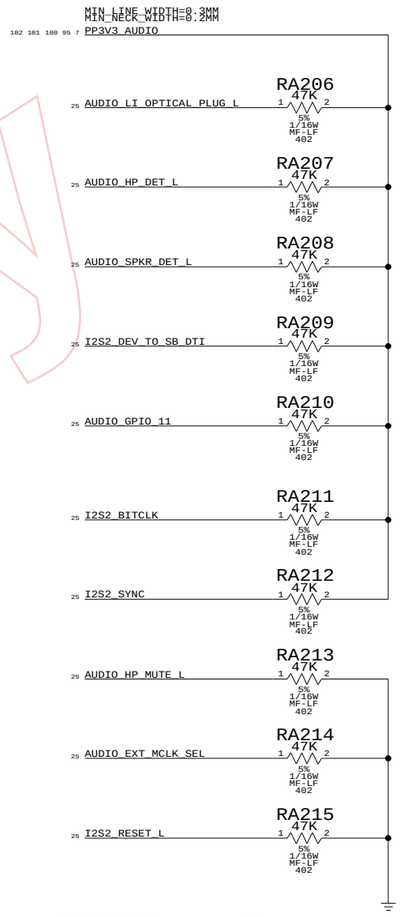


PLACE AT J5903

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



MAKE_BASE=TRUE
TP_I2S2_SB_TO_DEV_DTO — I88 — I2S2_SB_TO_DEV_DTO

MAKE_BASE=TRUE
TP_I2S2_MCLK — I89 — I2S2_MCLK

MAKE_BASE=TRUE
I2S0_MCLK — I116 — AUD_CODEC_MCLK

AUDIO: Q45 POWER SUPPLIES

SYNC_MASTER=AUDIO
SYNC_DATE=02/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	11
SCALE: NONE	SHT 102 OF 102	