1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M78-DVT

05/09/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
33		503047	ENGINEERING RELEASED	05/09/07	?

DRAWING
TITLE=M78
ABBREV=DRAWING
LAST_MODIFIED=Wed May 9 10:26:54 2007

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

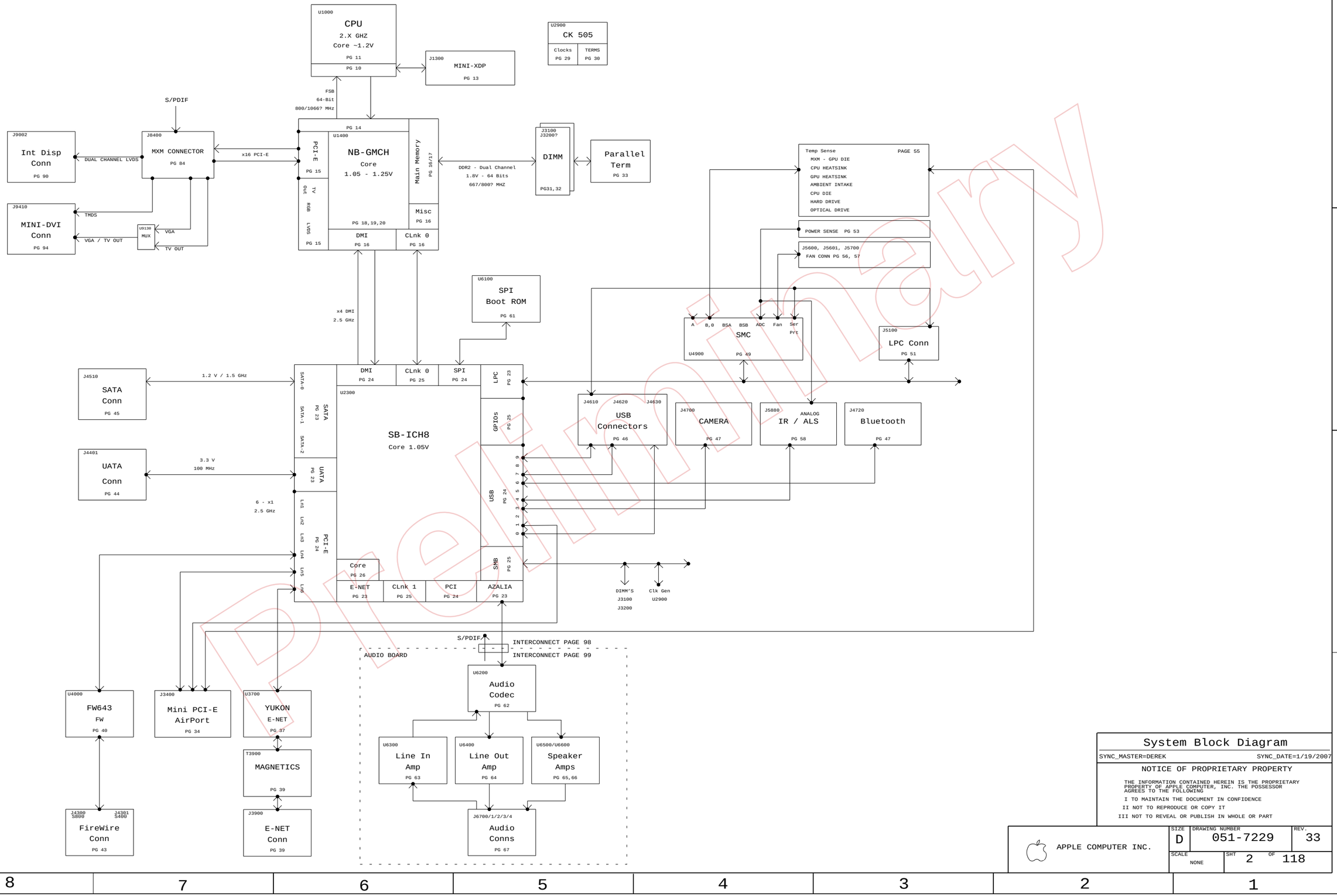
SIZE D

Apple Computer Inc.

TITLE
SCH,M78,MLB

DRAWING NUMBER 051-7229 REV. 33

SHT 1 OF 118



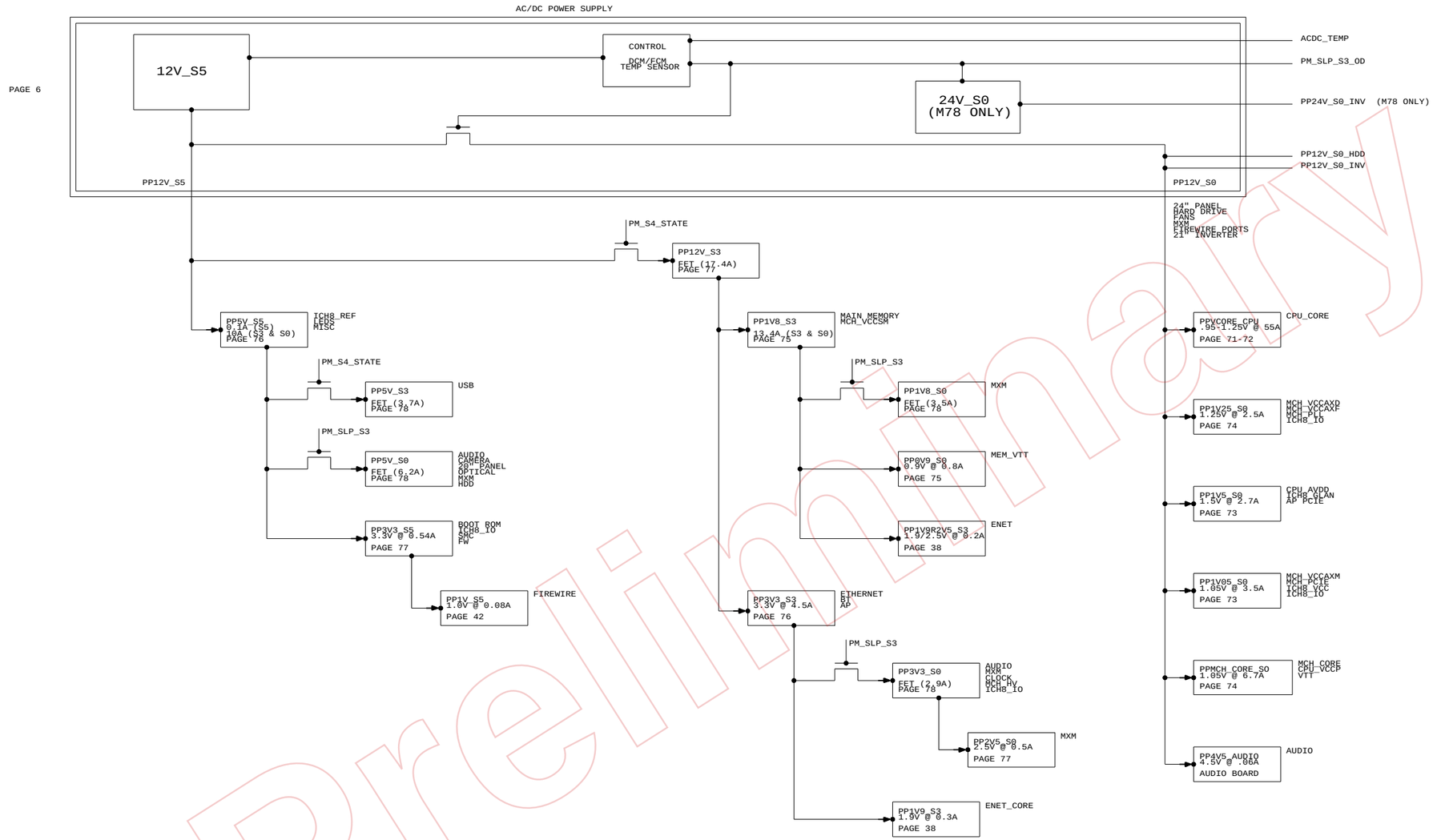
System Block Diagram

SYNC_MASTER=DEREK SYNC_DATE=1/19/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	2	118



Power Block Diagram

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE

SHT 3 OF 118

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7977	PCBA,MLB,M78,CTO,2.8G	24_INCH_LCD,2P8GHZ_CPU,BASIC,CR_E,V8
630-7976	PCBA,MLB,M78,BTR,2.4G	24_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,V6
630-7875	PCBA,MLB,M78,CTO,2.2G	24_INCH_LCD,2P2GHZ_CPU,BASIC,CR_STD,V6
607-0429	M78 DEVELOPMENT	CPU_TDIODE,DEVELOPMENT,XDP_CONN,LIT_IO,LPCPLUS,MXM_PWR_SENSE
630-7979	PCBA,MLB,M72,CTO,2.4G	20_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,V6
630-7978	PCBA,MLB,M72,BTR,2.2G	20_INCH_LCD,2P2GHZ_CPU,BASIC,CR_STD,V6
630-7874	PCBA,MLB,M72,GD,2.0G	20_INCH_LCD,2P0GHZ_CPU,BASIC,CR_STD,V6
607-0462	M72 DEVELOPMENT	CPU_TDIODE,DEVELOPMENT,ITP_CONN,LIT_IO,LPCPLUS,MXM_PWR_SENSE

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	5V1V8REG_SKIP,ALTERNATE,COMMON,ITP/XDP,MXM_ROM,NBCFG_PEG_REVERSE,YUKON_ULTRA
V6	LOW_TDP
V8	HIGH_TDP

Bar Code Labels / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0381 - GM965	338S0430	1	IC,NB,CRESTLINE,PM,C0,QS	U1400	CRITICAL	
	338S0427	1	IC,SB,ICH8M,B1,QS	U2300	CRITICAL	
537 - 359S0127	359S0130	1	CK505 - SILEGO SLG2AP101	U2900	CRITICAL	
DIFFERENT FOR M78?	820-2149	1	PCB,FAB,IO ALIGNMENT,M72	IO1	CRITICAL	
	069-2046	1	M72/M78 22UF CAP INTERCHANGEABILITY	DOC1		
	825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7229	1	PCB,SCHEM,MLB,M78	SCH1		24_INCH_LCD
056-XXXX (MCO) 057-XXXX (PANEL)	820-2110	1	PCB,FAB,MLB,M78,HF	MLB1		24_INCH_LCD
341T0048 = M78 EFI ROM (341S1904 - DEV) (341S1905 - PVT) (335S0384 - BLNK) (341S2066 - PROG) (335S0274 - BLNK)	341T0049	1	IC,SMC,M78	U4900	CRITICAL	24_INCH_LCD
	114S0307	1	RES,8.25K,0402,1%,1/16W,LF	R7117		24_INCH_LCD
	132S0010	1	CAP,CER,390PF,10%,50V,0402	C7113		24_INCH_LCD
	132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		24_INCH_LCD
	132S0082	1	CAP,CER,0.068UF,10%,16V,0402	C7134		24_INCH_LCD
(335S0155 - BLNK)	341S2117	1	IC,2K I2C EEPROM,MXM,M78	U8570	CRITICAL	24_INCH_LCD

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7228	1	PCB,SCHEM,MLB,M72	SCH1		20_INCH_LCD
056-2161 (MCO) 057-0399 (PANEL)	820-2143	1	PCB,FAB,MLB,M72,HF	MLB1		20_INCH_LCD
(341SXXXX - PVT) (335S0384 - BLNK)	341T0056	1	EFI ROM,M72/M78	U6100	CRITICAL	
(341S2069 - PROG) (335S0274 - BLNK)	341T0055	1	IC,SMC,M72	U4900	CRITICAL	20_INCH_LCD
	114S0303	1	RES,7.5K,0402,1%,1/16W,LF	R7117		20_INCH_LCD
	132S0205	1	CAP,CER,270PF,10%,50V,0402	C7113		20_INCH_LCD
	132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		20_INCH_LCD
	132S0082	1	CAP,CER,0.068UF,10%,16V,0402	C7134		20_INCH_LCD
(335S0155 - BLNK)	341S2116	1	IC,2K I2C EEPROM,MXM,M72	U8570	CRITICAL	20_INCH_LCD

337S3438	1	IC,MDC,SR,E1,QS,2.8G,55W,800FSB,4M,PGA	CPU	CRITICAL	2P8GHZ_CPU
337S3436	1	IC,MDC,SR,E1,QS,2.6G,45W,800FSB,4M,PGA	CPU	CRITICAL	2P6GHZ_CPU
337S3435	1	IC,MDC,SR,E1,QS,2.4G,35W,800FSB,4M,PGA	CPU	CRITICAL	2P4GHZ_CPU
337S3461	1	IC,MDC,SR,E1,QS,2.2G,35W,800FSB,4M,PGA	CPU	CRITICAL	2P2GHZ_CPU
337S3460	1	IC,MDC,SR,E1,QS,2.0G,35W,800FSB,4M,PGA	CPU	CRITICAL	2P0GHZ_CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3437	337S3436		CPU	CPU,2.6G,55W
124-0361	124-0339		C7490,C7491	CAP
371S0464	371S0154		D7624,D7664	DIODES

MXM_PWR_SENSE BOMOPTION CHANGE FOR PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0070	1	RES,0-OHM,2512	R5350		PRODUCTION
116S0090	2	RES,10K-OHM,5%,0402	C5358,C5359		PRODUCTION

BOM Configuration

SYNC_MASTER=JAMES SYNC_DATE=10/16/06

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7229 | REV. 33

SCALE NONE | SHT 4 OF 118

PROTO REVIEW - 11/09/06

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

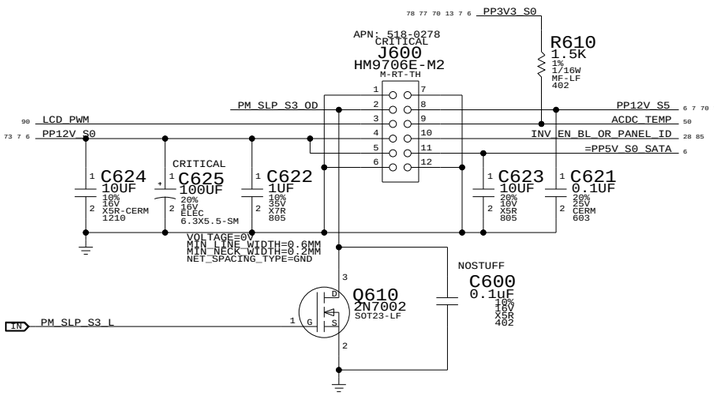
33

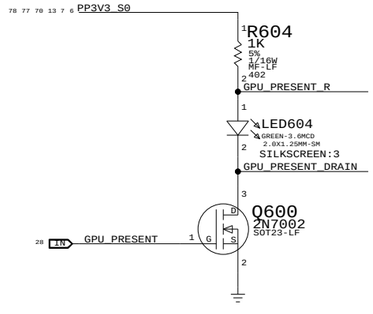
SYNC_MASTER=JAMES SYNC_DATE=10/16/06

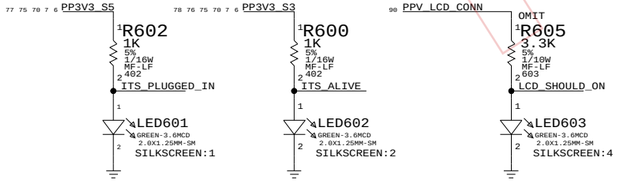
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	5	118







PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0082	1	RES,MF,1/10W,910OHM,5,0603,SMD,LF	R605		20_INCH_LCD
113S0095	1	RES,MF,1/10W,3.3KOHM,5,0603,SMD,LF	R605		24_INCH_LCD

"S0" RAILS

ONLY ON IN RUN

75 70 7 PP0V9_S0 (MAKE_BASE=TRUE, VOLTAGE=0.9V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP0V9_S0M_MEM_TERM 33

72 71 7 PPVCORE_CPU (MAKE_BASE=TRUE, VOLTAGE=1.25V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.3MM, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PPVCORE_S0_CPU 11 12 53

78 70 7 PP1V8_S0 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP1V8_S0_MXM 84

77 7 PP2V5_S0 (MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP2V5_S0_MXM 85

74 73 55 7 PPMCH_CORE_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PPVCORE_S0_NB 18 21
- =PPVCORE_S0_NB_FOLLOW 21
- =PP1V05_S0_CPU 10 11 12 13 50
- =PP1V25R1V05_S0_FSB_NB 14 30
- =PP1V25R1V05_S0_NB_VTT 19 21
- =PP1V05_S0_SB_CPU_IO 23 26 27

73 34 7 PP1V05_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP1V05_S0M_NB_VCCAXM 18 21
- =PP1V05_S0_NB_PCIE 21
- =PP1V05_S0_NB_FOLLOW 21
- =PPVCORE_S0_SB 26 27

73 7 PP1V5_S0 (MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP1V5_S0_CPU 11 12
- =PP1V5_S0_NB_TVDAC 22
- =PP1V5_S0_SB_VCC1_5_A_ARX 26 27
- =PP1V5_S0_SB_VCC1_5_A_ATX 26 27
- =PP1V5_S0_SB_VCCUSBPLL 26 27
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE 26 27
- =PP1V5_S0_SB_VCC1_5_A 26
- =PP1V5_S0_SB 27
- =PP1V5_S0_MINI 34

74 7 PP1V25_S0 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.25V, MAKE_BASE=TRUE, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP1V25_S0_NB_VCCDMI 19 21
- =PP1V25_S0M_NB_VCCA 21
- =PP1V25_S0M_NB_VCC 21
- =PP1V25_S0_NB_PLL 21
- =PP1V25_S0_NB_VCC 21
- =PP1V25_S0M_NB_PLL 21
- =PP1V25_S0_SB_DMI 26 27

78 77 70 13 7 6 PP3V3_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP3V3_S0_NB_VCCHV 16 19 21
- =PP3V3_S0_SB 27
- =PP3V3_S0_SB_GPIO 23 25
- =PP3V3_S0_SB_VCCGLAN3_3 26
- =PP3V3_S0_SB_VCC3_3_PCI 26 27
- =PP3V3_S0_SB_VCC3_3_IDE 26 27
- =PP3V3_S0_SB_PCI 24
- =PP3V3_S0_SB_PM 28
- =PP3V3_S0_PATA 44
- =PP3V3_S0_FAN 56 57
- =PPSPD_S0_MEM 31 32
- =PP3V3_S0_IMVP 71
- =PP3V3_S0_AUDIO 98
- =PP3V3_S0_LPCPLUS 51
- =PP3V3_S0_SMBUS_SB 52
- =PP3V3_S0_SMC_LS 50
- =PP3V3_S0_SMBUS_SMC_0_S0 52
- =PP3V3_S0_SMBUS_SMC_B_S0 52
- =PP3V3_S0_SMBUS_SMC_MGMT 52
- =PP3V3_S0_CK505 29 30
- =PP3V3_S0_MXM 85
- =PP3V3_S0_SATALED 45
- =PP3V3_S0M_CK505 29 30
- =PP3V3_S0MWOL_SB_CLINK0 25
- =PP3V3_S0_SB_VCC3_3_DMI 26 27
- =PP3V3_S0_SB_VCC3_3_SATA 26 27
- =PP3V3_S0_SB_VCC3_3_VCCPCORE 26
- =PP3V3R1V5_S0_SB_VCCHDA 26 27
- =PP3V3_S0MWOL_SB_VCCLAN3_3 26 27
- =PP3V3_S0MWOL_SB_VCCCL3_3 26 27
- =PP3V3_S0_TSENS 55
- =PP3V3_S0_SMC 53
- =PP3V3_S0_NB_VCCA_PEG_BG 19 21
- =PP3V3_S0_NB_FOLLOW 21
- =PP3V3_S0_VIDEO 90 91 94
- =PP3V3_S0_ENET 38

94 78 74 73 72 71 70 7 PP5V_S0 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP5V_S0_SB 27
- =PP5V_S0_PATA 44
- =PP5V_S0_LPCPLUS 7 51
- =PP5V_S0_AUDIO 98
- =PP5V_S0_SATA 6
- =PP5V_S0_MXM 84
- =PPV_S0_LCD_20INCH 90

76 74 73 7 6 PP12V_S0 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP12V_S0_FAN 56 57
- =PP12V_S0_AUDIO_SPKRAMP 98
- =PP12V_S0_CPU 53 71 72
- =PPV_S0_LCD_24INCH 90
- =PPV_S0_MXM_PWRSRC 53

"S3" RAILS

ON IN RUN AND SLEEP

78 75 7 PP1V8_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP1V8_S3M_MEM_NB 16 18 21 22
- =PP1V8_S3M_NB_VCC 21
- =PP1V8_S3_MEM 31 32
- =PP1V8_S3_MEMVTT 75
- =PP1V8_S3_ENET 38

78 76 75 70 7 6 PP3V3_S3 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP3V3_S3_MINI 34
- =PP3V3_S3_ENET 38 39
- =PP3V3_S3_BT 47

78 76 75 70 7 PP5V_S3 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP5V_S3_BNDI 47 58
- =PP5V_S3_MEMVTT 75
- =PP5V_S3_SYSLED 60
- =PP5V_S3_ALS 58

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

77 75 70 7 6 PP3V3_S5 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP3V3_S5_SB 25 27 28
- =PP3V3_S5_SB_USB 24
- =PP3V3_S5_SB_PM 28
- =PP3V3_S5_SB_VCCSUS3_3 26 27
- =PP3V3_S5_SB_VCCSUS3_3_USB 26 27
- =PP3V3_S5_SMBUS_SB_ME 52
- =PP3V3_S5_FW 40 42 43
- =PP3V3_S5_SMC 49 50
- =PP3V3_S5_ROM 61
- =PP3V3_S5_SB_GPIO 25
- =PP3V3_S5_SB_CLINK1 25
- =PP3V3_S5_SB_3V3_VCCSUSHDA 26 27
- =PP3V3_S5_LPCPLUS 7 51
- =PP3V3_S5_SMBUS_SMC_BSA 52
- =PP3V3_S5_FAN 56 57
- =PP3V3_S5_SMCUSBMUX 46
- =PP3V3_S5_SMBUS_SMC_A_S5 52

78 77 76 70 7 PP5V_S5 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP5V_S5_SB 27
- =PPVIN_S5_SMCVREF 50
- =PP5V_S5_USB 46

78 76 70 7 6 PP12V_S5 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=PWR, MAX_NECK_LENGTH=3 MM)
- =PP12V_S5_FET 78
- =PP12V_S5_FW 43

Power Conn / Alias

SYNC_MASTER=MARK SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 6 OF 118	

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

100 14 10 7	FSB_A_L<6>	PP1000	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1001	OMIT P4MM
100 14 10 7	FSB_A_L<27>	PP1002	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1003	OMIT P4MM
100 14 10 7	FSB_D_L<0>	PP1004	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1005	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1006	OMIT P4MM
100 14 10 7	FSB_DINV_L<0>	PP1007	OMIT P4MM
100 14 10 7	FSB_D_L<16>	PP1008	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1009	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1010	OMIT P4MM
100 14 10 7	FSB_DINV_L<1>	PP1011	OMIT P4MM
100 14 10 7	FSB_D_L<41>	PP1012	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1013	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1014	OMIT P4MM
100 14 10 7	FSB_DINV_L<2>	PP1015	OMIT P4MM
100 14 10 7	FSB_D_L<59>	PP1016	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1017	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1018	OMIT P4MM
100 14 10 7	FSB_DINV_L<3>	PP1019	OMIT P4MM
100 14 10 7	FSB_LOCK_L	PP1020	OMIT P4MM
100 14 13 10	FSB_CPURST_L	PP1021	OMIT P4MM
100 51 23 10	CPU_INIT_L	PP1022	OMIT P4MM
100 23 10	CPU_A20M_L	PP1023	OMIT P4MM
100 23 10	CPU_IGNNE_L	PP1024	OMIT P4MM
100 23 10	CPU_STPCLK_L	PP1025	OMIT P4MM
100 23 10	CPU_INTR	PP1026	OMIT P4MM
100 23 10	CPU_NMI	PP1027	OMIT P4MM
100 23 10	CPU_SMI_L	PP1028	OMIT P4MM
100 14 10 7	FSB_REQ_L<0>	PP1029	OMIT P4MM
100 14 10 7	FSB_REQ_L<1>	PP1030	OMIT P4MM
100 14 10 7	FSB_REQ_L<2>	PP1031	OMIT P4MM
100 14 10 7	FSB_REQ_L<3>	PP1032	OMIT P4MM
100 14 10 7	FSB_REQ_L<4>	PP1033	OMIT P4MM
105 30 10	FSB_CLK_CPU_P	PP1034	OMIT P4MM
105 30 10	FSB_CLK_CPU_N	PP1035	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

105 30 23	SB_CLK100M_SATA_P	PP2100	OMIT P4MM
105 30 23	SB_CLK100M_SATA_N	PP2101	OMIT P4MM
103 44 23	IDE_PDIOR_L	PP2102	OMIT P4MM
103 44 23	IDE_PDIORDY	PP2103	OMIT P4MM
103 44 23	IDE_PDD<9>	PP2104	OMIT P4MM
104 34 24	PCIE_MINI_D2R_P	PP2105	OMIT P4MM
104 34 24	PCIE_MINI_D2R_N	PP2106	OMIT P4MM
104 37 24	PCIE_ENET_D2R_P	PP2107	OMIT P4MM
104 37 24	PCIE_ENET_D2R_N	PP2108	OMIT P4MM
104 42 40	PCIE_FW_D2R_P	PP2132	OMIT P4MM
104 42 40	PCIE_FW_D2R_N	PP2133	OMIT P4MM
101 24 16	DMI_N2S_P<0>	PP2109	OMIT P4MM
101 24 16	DMI_N2S_N<0>	PP2110	OMIT P4MM
105 30 24	SB_CLK100M_DMI_P	PP2111	OMIT P4MM
105 30 24 7	SB_CLK100M_DMI_N	PP2112	OMIT P4MM
49 28 25	PM_SYSRST_L	PP2113	OMIT P4MM
51 49 25 7	PM_CLKRUN_L	PP2114	OMIT P4MM
105 30 25	SB_CLK14P3M_TIMER	PP2115	OMIT P4MM
105 30 25	SB_CLK48M_USBCTLR	PP2116	OMIT P4MM
105 30 24	PCI_CLK33M_SB	PP2117	OMIT P4MM
28 23	SB_RTC_RST_L	PP2118	OMIT P4MM
103 45 23	SATA_A_D2R_P	PP2119	OMIT P4MM
103 45 23	SATA_A_D2R_N	PP2120	OMIT P4MM
51 49 23 7	LPC_AD<1>	PP2121	OMIT P4MM
103 47 24	USB_CAMERA_P	PP2122	OMIT P4MM
103 47 24	USB_CAMERA_N	PP2123	OMIT P4MM
103 47 24	USB_IR_P	PP2124	OMIT P4MM
103 47 24	USB_IR_N	PP2125	OMIT P4MM
103 47 24	USB_BT_P	PP2126	OMIT P4MM
103 47 24	USB_BT_N	PP2127	OMIT P4MM
103 61	SPI_SCLK	PP2128	OMIT P4MM
103 61 24	SPI_SO	PP2129	OMIT P4MM
104 25 16 7	CLINK_NB_CLK	PP2130	OMIT P4MM
104 25 16 7	CLINK_NB_DATA	PP2131	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1400

100 14 10 7	FSB_A_L<6>	PP1400	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1401	OMIT P4MM
100 14 10 7	FSB_A_L<27>	PP1402	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1403	OMIT P4MM
100 14 10 7	FSB_D_L<0>	PP1404	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1405	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1406	OMIT P4MM
100 14 10 7	FSB_DINV_L<0>	PP1407	OMIT P4MM
100 14 10 7	FSB_D_L<16>	PP1408	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1409	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1410	OMIT P4MM
100 14 10 7	FSB_DINV_L<1>	PP1411	OMIT P4MM
100 14 10 7	FSB_D_L<41>	PP1412	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1413	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1414	OMIT P4MM
100 14 10 7	FSB_DINV_L<2>	PP1415	OMIT P4MM
100 14 10 7	FSB_D_L<59>	PP1416	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1417	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1418	OMIT P4MM
100 14 10 7	FSB_DINV_L<3>	PP1419	OMIT P4MM
100 14 10 7	FSB_LOCK_L	PP1420	OMIT P4MM
100 14 10	FSB_HIT_L	PP1421	OMIT P4MM
100 14 10	FSB_HITM_L	PP1422	OMIT P4MM
100 14 10	FSB_BNR_L	PP1423	OMIT P4MM
100 14 10	FSB_BREQ0_L	PP1424	OMIT P4MM
100 14 10	FSB_DBSY_L	PP1425	OMIT P4MM
100 14 10	FSB_DPWR_L	PP1426	OMIT P4MM
100 14 10 7	FSB_REQ_L<0>	PP1427	OMIT P4MM
100 14 10 7	FSB_REQ_L<1>	PP1428	OMIT P4MM
100 14 10 7	FSB_REQ_L<2>	PP1429	OMIT P4MM
100 14 10 7	FSB_REQ_L<3>	PP1430	OMIT P4MM
100 14 10 7	FSB_REQ_L<4>	PP1431	OMIT P4MM
105 30 14	FSB_CLK_NB_P	PP1432	OMIT P4MM
105 30 14 7	FSB_CLK_NB_N	PP1433	OMIT P4MM
71 70 22 16 7	VR_PWRGOOD_DELAY	PP1434	OMIT P4MM
28 16	NB_RESET_L	PP1435	OMIT P4MM
105 30 16	NB_CLK100M_PCIE_P	PP1436	OMIT P4MM
105 30 16 7	NB_CLK100M_PCIE_N	PP1437	OMIT P4MM
101 24 16	DMI_S2N_N<0>	PP1438	OMIT P4MM
101 24 16	DMI_S2N_P<0>	PP1439	OMIT P4MM
22 16	=PP0V9_S3M_MEM_NBVREFA	PP1440	OMIT P4MM
22 16	=PP0V9_S3M_MEM_NBVREFB	PP1441	OMIT P4MM
102 31 17	MEM_A_DQ<7>	PP1442	OMIT P4MM
102 31 17	MEM_A_DQ<14>	PP1443	OMIT P4MM
102 31 17	MEM_A_DQ<16>	PP1444	OMIT P4MM
102 31 17	MEM_A_DQ<25>	PP1445	OMIT P4MM
102 31 17	MEM_A_DQ<39>	PP1446	OMIT P4MM
102 31 17	MEM_A_DQ<47>	PP1447	OMIT P4MM
102 31 17	MEM_A_DQ<54>	PP1448	OMIT P4MM
102 31 17	MEM_A_DQ<59>	PP1449	OMIT P4MM
102 31 17	MEM_A_DQS_P<0>	PP1450	OMIT P4MM
102 31 17	MEM_A_DQS_N<0>	PP1451	OMIT P4MM
102 31 17	MEM_A_DQS_P<1>	PP1452	OMIT P4MM
102 31 17	MEM_A_DQS_N<1>	PP1453	OMIT P4MM
102 31 17	MEM_A_DQS_P<2>	PP1454	OMIT P4MM
102 31 17	MEM_A_DQS_N<2>	PP1455	OMIT P4MM
102 31 17	MEM_A_DQS_P<3>	PP1456	OMIT P4MM
102 31 17	MEM_A_DQS_N<3>	PP1457	OMIT P4MM
102 31 17	MEM_A_DQS_P<4>	PP1458	OMIT P4MM
102 31 17	MEM_A_DQS_N<4>	PP1459	OMIT P4MM
102 31 17	MEM_A_DQS_P<5>	PP1460	OMIT P4MM
102 31 17	MEM_A_DQS_N<5>	PP1461	OMIT P4MM
102 31 17	MEM_A_DQS_P<6>	PP1462	OMIT P4MM
102 31 17	MEM_A_DQS_N<6>	PP1463	OMIT P4MM
102 31 17	MEM_A_DQS_P<7>	PP1464	OMIT P4MM
102 31 17	MEM_A_DQS_N<7>	PP1465	OMIT P4MM
102 32 17	MEM_B_DQ<6>	PP1466	OMIT P4MM
102 32 17	MEM_B_DQ<8>	PP1467	OMIT P4MM
102 32 17	MEM_B_DQ<23>	PP1468	OMIT P4MM
102 32 17	MEM_B_DQ<25>	PP1469	OMIT P4MM
102 32 17	MEM_B_DQ<38>	PP1470	OMIT P4MM
102 32 17	MEM_B_DQ<44>	PP1471	OMIT P4MM
102 32 17	MEM_B_DQ<48>	PP1472	OMIT P4MM
102 32 17	MEM_B_DQ<62>	PP1473	OMIT P4MM
102 32 17	MEM_B_DQS_P<0>	PP1474	OMIT P4MM
102 32 17	MEM_B_DQS_N<0>	PP1475	OMIT P4MM
102 32 17	MEM_B_DQS_P<1>	PP1476	OMIT P4MM
102 32 17	MEM_B_DQS_N<1>	PP1477	OMIT P4MM
102 32 17	MEM_B_DQS_P<2>	PP1478	OMIT P4MM
102 32 17	MEM_B_DQS_N<2>	PP1479	OMIT P4MM
102 32 17	MEM_B_DQS_P<3>	PP1480	OMIT P4MM
102 32 17	MEM_B_DQS_N<3>	PP1481	OMIT P4MM
102 32 17	MEM_B_DQS_P<4>	PP1482	OMIT P4MM
102 32 17	MEM_B_DQS_N<4>	PP1483	OMIT P4MM
102 32 17	MEM_B_DQS_P<5>	PP1484	OMIT P4MM
102 32 17	MEM_B_DQS_N<5>	PP1485	OMIT P4MM
102 32 17	MEM_B_DQS_P<6>	PP1486	OMIT P4MM
102 32 17	MEM_B_DQS_N<6>	PP1487	OMIT P4MM
102 32 17	MEM_B_DQS_P<7>	PP1488	OMIT P4MM
102 32 17	MEM_B_DQS_N<7>	PP1489	OMIT P4MM
101 84 15	PEG_D2R_P<7>	PP1490	OMIT P4MM
101 84 15	PEG_D2R_N<7>	PP1491	OMIT P4MM
104 25 16 7	CLINK_NB_CLK	PP1492	OMIT P4MM
104 25 16 7	CLINK_NB_DATA	PP1493	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U3700

105 37 30	PCIE_CLK100M_ENET_P	PP3700	OMIT P4MM
105 37 30	PCIE_CLK100M_ENET_N	PP3701	OMIT P4MM
108 37	PCIE_ENET_R2D_P	PP3702	OMIT P4MM
108 37	PCIE_ENET_R2D_N	PP3703	OMIT P4MM
37 28	ENET_RESET_L	PP3704	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4000

105 40 30	PCIE_CLK100M_FW_P	PP4000	OMIT P4MM
105 40 30	PCIE_CLK100M_FW_N	PP4001	OMIT P4MM
108 40	PCIE_FW_R2D_P	PP4002	OMIT P4MM
108 40	PCIE_FW_R2D_N	PP4003	OMIT P4MM
40 28	FW_RESET_L	PP4004	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4900

105 49 30	PCI_CLK33M_SMC	PP4900	OMIT P4MM
49 28	SMC_LRESET_L	PP4901	OMIT P4MM
51 50 49 7	SMC_RESET_L	PP4902	OMIT P4MM
51 49 23 7	LPC_AD<1>	PP4903	OMIT P4MM

PP3V3_S3 — C701 0.01UF 10% 50V X7R 402 — C702 0.01UF 10% 50V X7R 402 — C703 0.01UF 10% 50V X7R 402 — C704 0.01UF 10% 50V X7R 402 — PP3V3_S0 (8 76 75 70 7 6 / 6 7 13 70 77 78)

PP12V_S5 — C705 0.01UF 10% 50V X7R 402 — C706 0.01UF 10% 50V X7R 402 — C707 0.01UF 10% 50V X7R 402 — C708 0.01UF 10% 50V X7R 402 — C709 0.01UF 10% 50V X7R 402 — C710 0.01UF 10% 50V X7R 402 — PP12V_S3 (78 76 70 7 6 / 7 50 75 76 78)

BTW DIMMS: SC0700 EMI-SPRING CLIP-SM1; SC0701 EMI-SPRING CLIP-SM1; SC0702 EMI-SPRING SC57

LPC CONNECTOR

51 6	=PP3V3_S5_LPCPLUS	FUNC_TEST=TRUE
51 6	=PP5V_S0_LPCPLUS	FUNC_TEST=TRUE
51	FWH_INIT_L	FUNC_TEST=TRUE
105 51 30	PCI_CLK33M_LPCPLUS	FUNC_TEST=TRUE
51 49 23	LPC_AD<0>	FUNC_TEST=TRUE
51 49 23 7	LPC_AD<1>	FUNC_TEST=TRUE
51 49 23	LPC_AD<2>	FUNC_TEST=TRUE
51 49 23	LPC_AD<3>	FUNC_TEST=TRUE
51 49 23	LPC_FRAME_L	FUNC_TEST=TRUE
51 49 25 7	PM_CLKRUN_L	FUNC_TEST=TRUE
51 24	BOOT_LPC_SPI_L	FUNC_TEST=TRUE
51 50 49	SMC_TMS	FUNC_TEST=TRUE
51 28	DEBUG_RESET_L	FUNC_TEST=TRUE
51 49	SMC_TRST_L	FUNC_TEST=TRUE
51 50 49	SMC_TDO	FUNC_TEST=TRUE
51 49	SMC_MD1	FUNC_TEST=TRUE
51 50 49 46	SMC_TX_L	FUNC_TEST=TRUE
51 49 25	INT_SERIRQ	FUNC_TEST=TRUE
51 50 49 25 7	PM_SUS_STAT_L	FUNC_TEST=TRUE
51 50 49	SMC_TDI	FUNC_TEST=TRUE
51 50 49	SMC_TCK	FUNC_TEST=TRUE
51 50 49 7	SMC_RESET_L	FUNC_TEST=TRUE
51 49	SMC_NMI	FUNC_TEST=TRUE
51 50 49 46	SMC_RX_L	FUNC_TEST=TRUE
51 25	LINDACARD_GPIO	FUNC_TEST=TRUE

16 TP'S

PWROK SEQUENCING

84 70 50 49 7	ALL_SYS_PWRGD	FUNC_TEST=TRUE
70 28 25 7	PM_SB_PWROK	FUNC_TEST=TRUE

STARTUP (BOOT/WAKE) TIMING

71 49	IMVP_VR_ON	FUNC_TEST=TRUE
28 25	VR_PWRGD_CLKEN	FUNC_TEST=TRUE
71 70 22 16 7	VR_PWRGOOD_DELAY	FUNC_TEST=TRUE
70 28 25 7	PM_SB_PWROK	FUNC_TEST=TRUE

SHUTDOWN/SLEEP TIMING

51 50 49 25 7	PM_SUS_STAT_L	FUNC_TEST=TRUE
78 75 70 49 25 6	PM_SLP_S3_L	FUNC_TEST=TRUE
78 75 49 46 25 7	PM_S4_STATE_L	FUNC_TEST=TRUE
84 70 50 49 7	ALL_SYS_PWRGD	FUNC_TEST=TRUE
100 23 13 10	CPU_PWRGD	FUNC_TEST=TRUE

"S0" RAILS

75 70 6	PP0V9_S0	FUNC_TEST=TRUE
72 71 6	PPVCORE_CPU	FUNC_TEST=TRUE
78 70 6	PP1V8_S0	FUNC_TEST=TRUE
77 6	PP2V5_S0	FUNC_TEST=TRUE
74 73 55 6	PPMCH_CORE_S0	FUNC_TEST=TRUE
73 34 6	PP1V05_S0	FUNC_TEST=TRUE
74 6	PP1V25_S0	FUNC_TEST=TRUE
78 77 70 13 7 6	PP3V3_S0	FUNC_TEST=TRUE
94 78 74 73 72 71 70 6	PP5V_S0	FUNC_TEST=TRUE
76 74 73 6	PP12V_S0	FUNC_TEST=TRUE
73 6	PP1V5_S0	FUNC_TEST=TRUE

3 TP'S

"S3" RAILS

78 76 75 50 7	PP12V_S3	FUNC_TEST=TRUE
78 75 6	PP1V8_S3	FUNC_TEST=TRUE
78 76 75 70 7 6	PP3V3_S3	FUNC_TEST=TRUE
78 76 75 70 6	PP5V_S3	FUNC_TEST=TRUE
78 75 49 46 25 7	PM_S4_STATE_L	FUNC_TEST=TRUE

3 TP'S

"S5" RAILS

77 75 70 6	PP3V3_S5	FUNC_TEST=TRUE
78 77 76 70 6	PP5V_S5	FUNC_TEST=TRUE
78 76 70 7 6	PP12V_S5	FUNC_TEST=TRUE

5 TP'S

FOR ICT

105 30 16 7	NB_CLK100M_PCIE_N	FUNC_TEST=TRUE
105 30 14 7	FSB_CLK_NB_N	FUNC_TEST=TRUE
16	TP_NB_CFG<13>	FUNC_TEST=TRUE
16	TP_NB_CFG<12>	FUNC_TEST=TRUE
16	TP_NB_CFG<18>	FUNC_TEST=TRUE
16	NB_CFG<19>	FUNC_TEST=TRUE
104 24	PCI_REQ1_L	FUNC_TEST=TRUE
104 24	PCI_REQ2_L	FUNC_TEST=TRUE
105 30 24 7	SB_CLK100M_DMI_N	FUNC_TEST=TRUE
30	TP_CK505_REF1	FUNC_TEST=TRUE
30	TP_CK505_PCI1_CLK	FUNC_TEST=TRUE
40	TP_FW_TCK	FUNC_TEST=TRUE
40	TP_FW_TMS	FUNC_TEST=TRUE
40	TP_FW_TDI	FUNC_TEST=TRUE
40	TP_FW_TDO	FUNC_TEST=TRUE
40	FW_TRST_L	FUNC_TEST=TRUE
40	TP_FW_SM	FUNC_TEST=TRUE
40	TP_FW_SE	FUNC_TEST=TRUE
40	TP_FW_NAND_TREE	FUNC_TEST=TRUE
40	TP_FW_CE	FUNC_TEST=TRUE
103 61	SPI_CE_L<0>	FUNC_TEST=TRUE
103 61	SPI_A_SO_R	FUNC_TEST=TRUE

998-0845 FOR NB HEATSINK

OMIT ZH0722 3P9R3P15 — OMIT ZH0723 3P9R3P15 — OMIT ZH0724 3P9R3P15 — OMIT ZH0725 3P9R3P15

452-0508 NOSTUFF

SDF0726 HSK-NUT-6.5MM TH — SDF0727 HSK-NUT-6.5MM TH

998-0850 FOR CPU HEATSINK

OMIT ZH0700 4P75R4 — OMIT ZH0701 4P75R4 — OMIT ZH0702 4P75R4 — OMIT ZH0703 4P75R4

860-0895

SDF0717 STDOFF-7P0OD15P0H-TH — SDF0721 STDOFF-7P0OD15P0H-TH — SDF0750 STDOFF-7P0OD15P0H-TH — SDF0751 STDOFF-7P0OD15P0H-TH

998-0847

OMIT ZH0711 4P25R3P5 — OMIT ZH0712 4P25R3P5 — OMIT ZH0714 4P25R3P5 — OMIT ZH0715 4P25R3P5 — OMIT ZH0718 4P25R3P5 — OMIT ZH0720 4P25R3P5 — OMIT ZH0750 4P25R3P5

MISC GROUND VIAS - NEEDED?

ZH500 HOLE-VIA — ZH501 HOLE-VIA — ZH502 HOLE-VIA — ZH503 HOLE-VIA — ZH504 HOLE-VIA — ZH505 HOLE-VIA — ZH506 HOLE-VIA — ZH507 HOLE-VIA — ZH508 HOLE-VIA — ZH509 HOLE-VIA

ZH510 HOLE-VIA — ZH511 HOLE-VIA — ZH512 HOLE-VIA — ZH513 HOLE-VIA — ZH514 HOLE-VIA — ZH515 HOLE-VIA — ZH516 HOLE-VIA — ZH517 HOLE-VIA — ZH518 HOLE-VIA — ZH519 HOLE-VIA

ZH520 HOLE-VIA — ZH521 HOLE-VIA — ZH522 HOLE-VIA — ZH523 HOLE-VIA — ZH524 HOLE-VIA — ZH525 HOLE-VIA — ZH526 HOLE-VIA — ZH527 HOLE-VIA — ZH528 HOLE-VIA — ZH529 HOLE-VIA

Functional / ICT Test

SYNC_MASTER=JAMES SYNC_DATE=10/16/06

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE NONE — SHT 7 OF 118

GND RAILS

98 GND_AUDIO_SPKRAMP
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=GND

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

CHASSIS GND

46 GND_CHASSIS_USB

43 GND_CHASSIS_FIREWIRE
39 GND_CHASSIS_ENET
94 =GND_CHASSIS_DVI

NOTE:
PER EMC REQUIREMENTS, ALL CHASSIS GROUNDS ARE TIED DIRECTLY TO GND

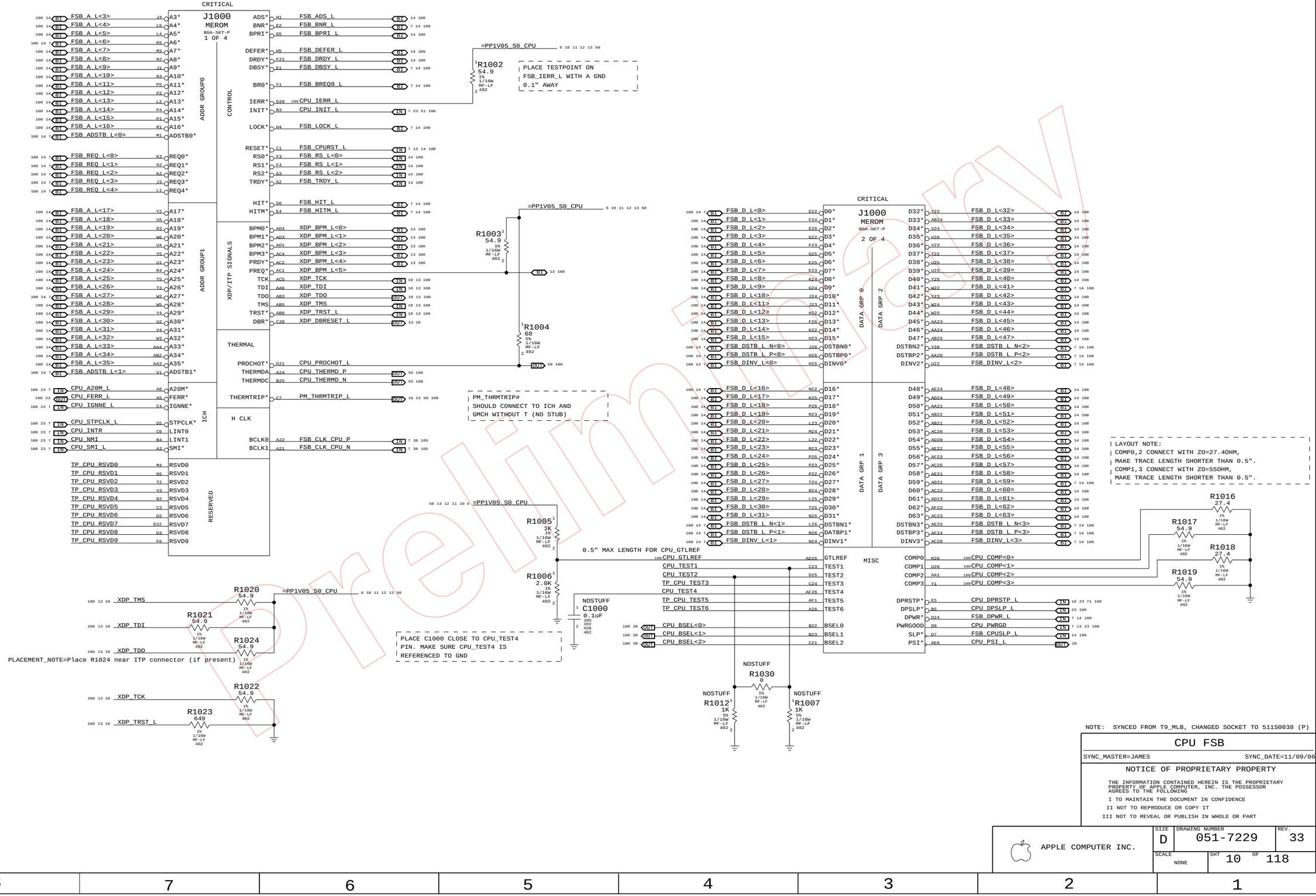
GROUNDING ALIASES

SYNC_MASTER=MARK SYNC_DATE=(10/02/2006)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE NONE SHT 9 OF 118


CRITICAL
J1000
MEROM
BGA-SKT-P
1 OF 4
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
FSB_A_L<10>
FSB_A_L<11>
FSB_A_L<12>
FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
FSB_A_L<20>
FSB_A_L<21>
FSB_A_L<22>
FSB_A_L<23>
FSB_A_L<24>
FSB_A_L<25>
FSB_A_L<26>
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FSB_A_L<28>
FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_A_L<32>
FSB_A_L<33>
FSB_A_L<34>
FSB_A_L<35>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_RSVD0
TP_CPU_RSVD1
TP_CPU_RSVD2
TP_CPU_RSVD3
TP_CPU_RSVD4
TP_CPU_RSVD5
TP_CPU_RSVD6
TP_CPU_RSVD7
TP_CPU_RSVD8
TP_CPU_RSVD9
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
0.5" MAX LENGTH FOR CPU_GTLREF
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND
R1020 54.9
R1021 54.9
R1022 54.9
R1023 649
R1024 54.9
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)
CRITICAL
J1000
MEROM
BGA-SKT-P
2 OF 4
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
FSB_D_L<7>
FSB_D_L<8>
FSB_D_L<9>
FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTB_L_N<0>
FSB_DSTB_L_P<0>
FSB_DINV_L<0>
FSB_D_L<16>
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FSB_D_L<32>
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FSB_DSTB_L_N<2>
FSB_DSTB_L_P<2>
FSB_DINV_L<2>
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FSB_D_L<62>
FSB_D_L<63>
FSB_DSTB_L_N<3>
FSB_DSTB_L_P<3>
FSB_DINV_L<3>
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_CPUSLP_L
CPU_PSI_L
R1016 27.4
R1017 54.9
R1018 27.4
R1019 54.9
LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
NOSTUFF R1030 0
NOSTUFF R1012 1K
NOSTUFF R1007 1K
NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)
CPU FSB
SYNC_MASTER=JAMES
SYNC_DATE=11/09/06
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7229
REV. 33
SCALE NONE
SHT 10 OF 118

(CPU CORE POWER)

=PPVCORE_S0_CPU 6 11 12 53

44 A (SV Design Target)
41 A (SV HFM)
30.4 A (SV LFM)
23 A (LV Design Target)

CRITICAL

J1000
MEROM
BGA-SKT-P
3 OF 4

VCC: A7 A9 A10 A12 A13 A15 A17 A18 A20 B7 B9 B10 B12 B14 B15 B17 B18 B20 C9 C10 C12 C13 C15 C17 C18 D9 D10 D12 D14 D15 D17 D18 E7 E9 E10 E12 E13 E15 E17 E18 E20 F7 F9 F10 F12 F14 F15 F17 F18 F20 AA7 AA9 AA10 AA12 AA13 AA15 AA17 AA18 AA20 AB9 AC10 AB10 AB12 AB14 AB15 AB17 AB18

VCC: AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 6 10 12 13 50

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21 V6 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 6 12

130 mA

VCCA: B26 C26

VID0 AD6 CPU_VID<0> OUT 12 100
VID1 AF5 CPU_VID<1> OUT 12 100
VID2 AE5 CPU_VID<2> OUT 12 100
VID3 AF4 CPU_VID<3> OUT 12 100
VID4 AE3 CPU_VID<4> OUT 12 100
VID5 AF3 CPU_VID<5> OUT 12 100
VID6 AE2 CPU_VID<6> OUT 12 100

VCCSENSE AF7 CPU_VCCSENSE_P OUT 71 100

VSSSENSE AE7 CPU_VCCSENSE_N OUT 71 100

=PPVCORE_S0_CPU 6 11 12 53

R1100
100
1%
1/16W
MF-LF
402

LAYOUT NOTE:
PLACE R1100 AND R1101 WITHIN
1 INCH OF CPU, NO STUBS

R1101
100
1%
1/16W
MF-LF
402

LAYOUT NOTE:
CPU_VCCSENSE_P/CPU_VCCSENSE_N USE
ZO=27.4 OHM DIFFERENTIAL TRACE ROUTING.

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE

CRITICAL

J1000
MEROM
BGA-SKT-P
4 OF 4

VSS: A4 A8 A11 A14 A16 A19 A23 AF2 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C2 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3

VSS: P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 A2 AF6 AF8 AF11 AF13 AF16 AF19 AF21 A25 AF25

NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)

CPU Power & Ground

SYNC_MASTER=JAMES SYNC_DATE=11/09/06

APPLE COMPUTER INC.

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SCALE: NONE SHT 11 OF 118

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU VCORE HF AND BULK DECOUPLING

6X 220UF. 32X 22UF 0805

53 11 6 =PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1200 NOSTUFF, C1201, C1202, C1203, C1204, C1205, C1206, C1207, C1208, C1209
22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1210, C1211, C1212, C1213, C1214, C1215, C1216, C1217, C1218, C1219
22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)

C1220, C1221, C1222 NOSTUFF, C1223 NOSTUFF, C1224 NOSTUFF, C1225 NOSTUFF
22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

C1226, C1227, C1228 NOSTUFF, C1229 NOSTUFF, C1230, C1231 NOSTUFF
22UF 20% 6.3V X5R 805

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

C1250 CRITICAL NOSTUFF, C1251 CRITICAL, C1254 CRITICAL, C1255 CRITICAL, C1252 CRITICAL, C1253 CRITICAL
220UF 20% 2V POLY CASE-D2-SM1

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CPU VCORE VID CONNECTIONS

Resistors to allow for override of CPU VID
Will probably be removed before production

100 11	CPU_VID<0>	R1290 0 5% 1/16W MF-LF 402	IMVP6_VID<0> 71 100
100 11	CPU_VID<1>	R1291 0 5% 1/16W MF-LF 402	IMVP6_VID<1> 71 100
100 11	CPU_VID<2>	R1292 0 5% 1/16W MF-LF 402	IMVP6_VID<2> 71 100
100 11	CPU_VID<3>	R1293 0 5% 1/16W MF-LF 402	IMVP6_VID<3> 71 100
100 11	CPU_VID<4>	R1294 0 5% 1/16W MF-LF 402	IMVP6_VID<4> 71 100
100 11	CPU_VID<5>	R1295 0 5% 1/16W MF-LF 402	IMVP6_VID<5> 71 100
100 11	CPU_VID<6>	R1296 0 5% 1/16W MF-LF 402	IMVP6_VID<6> 71 100

VCCA (CPU AVdd) DECOUPLING

11 6 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

50 13 11 10 6 =PP1V05_S0_CPU

1X 330UF, 6X 0.1UF 0402

C1235 CRITICAL 330UF 20% 6.3V ELEC 6.3X8-SM
C1236, C1237, C1238, C1239, C1240, C1241
0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

SYNC_MASTER=MARK SYNC_DATE=10/10/2006

APPLE COMPUTER INC.

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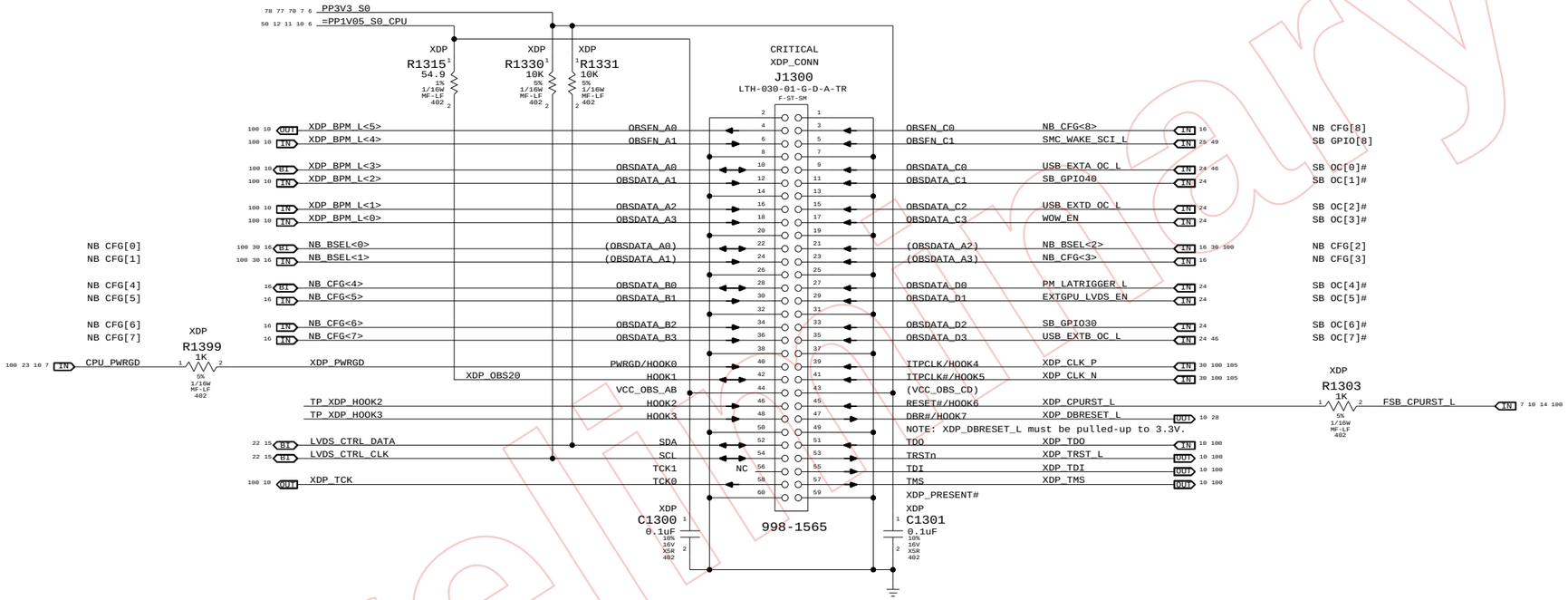
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/06/2006

APPLE COMPUTER INC.

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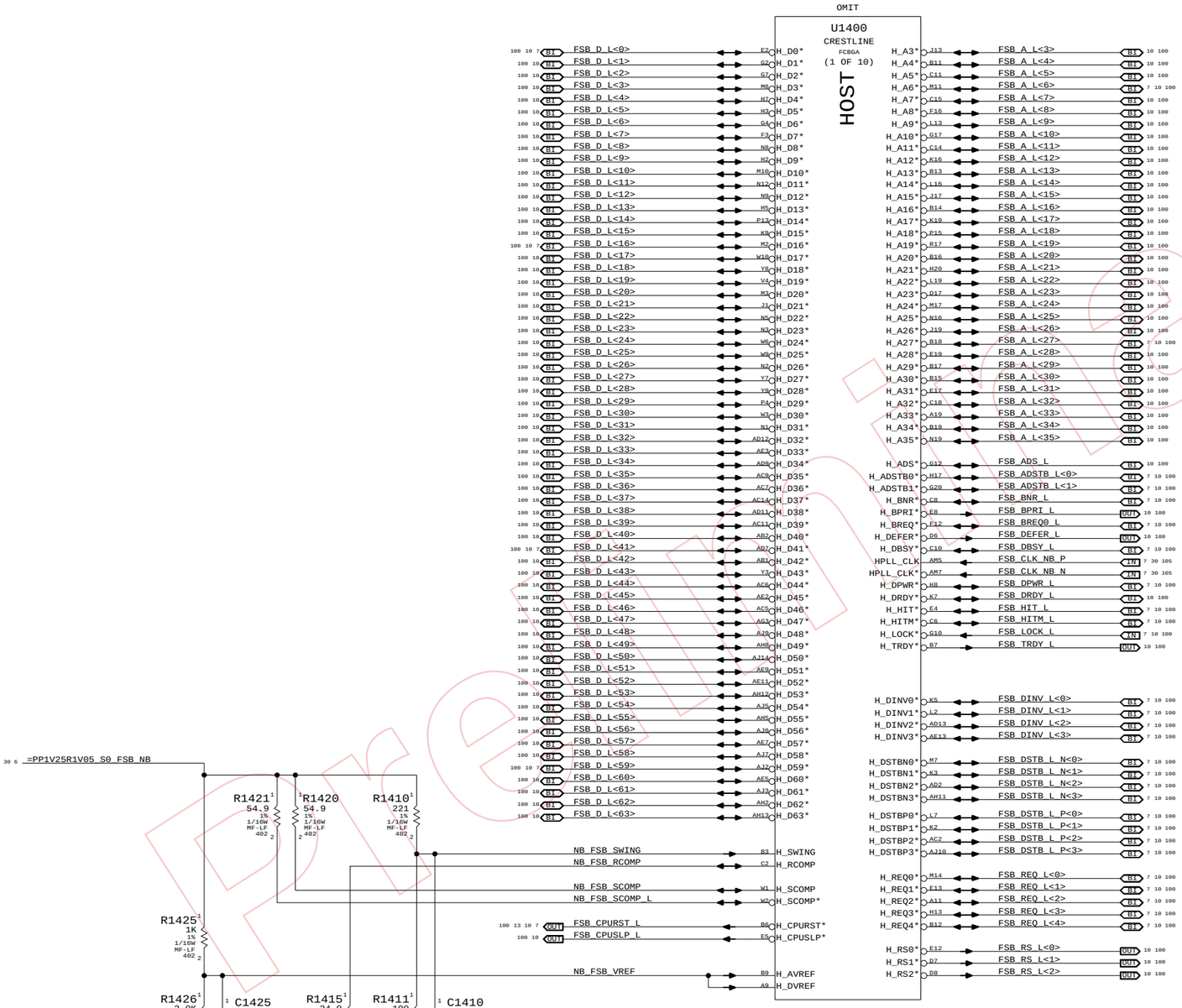

NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
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LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

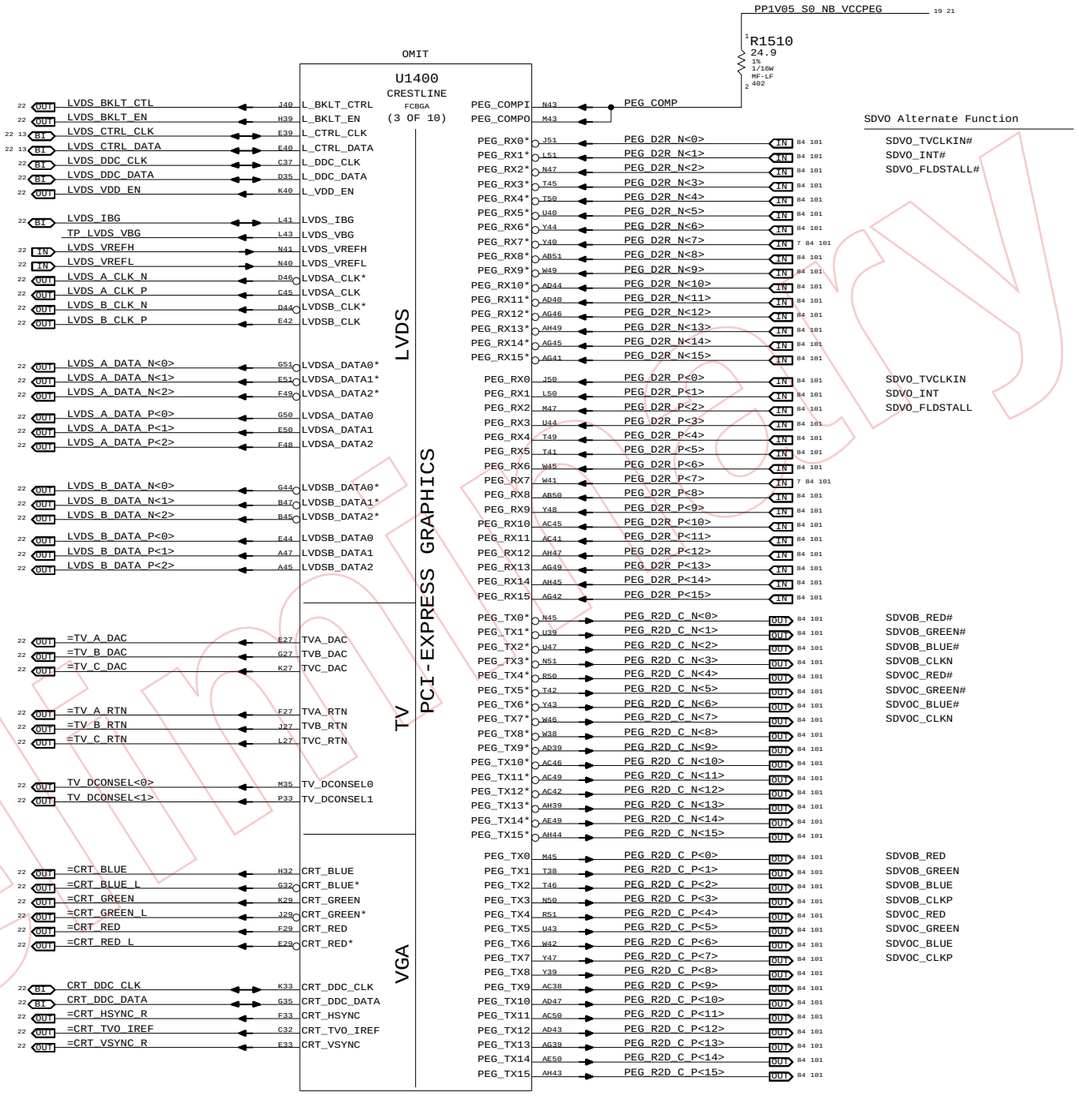
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 15 OF 118	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> — R1655 3.9K 5% 1/16W MF-LF 402 — NBCFG_DMI_X2

NB_CFG<9> — R1659 3.9K 5% 1/16W MF-LF 402 — NBCFG_PEG_REVERSE

NB_CFG<16> — R1666 3.9K 5% 1/16W MF-LF 402 — NBCFG_DYN_ODT_DISABLE

=PP3V3_S0_NB_VCCHV — R1669 3.9K 5% 1/16W MF-LF 402 — NBCFG_DMI_REVERSE — NB_CFG<19>

=PP3V3_S0_NB_VCCHV — R1670 3.9K 5% 1/16W MF-LF 402 — NBCFG_SDVO_AND_PCIE — NB_CFG<20>

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

=PP3V3_S0_NB_VCCHV — R1630 10K 5% 1/16W MF-LF 402 — R1631 10K 5% 1/16W MF-LF 402

PM_EXTTS_L<0>
PM_EXTTS_L<1>

OMIT

U1400 CRESTLINE FCBGA (2 OF 10)

RSVD

TP_NB_RSVD<1>	P36	RSVD1
TP_NB_RSVD<2>	P37	RSVD2
TP_NB_RSVD<3>	R35	RSVD3
TP_NB_RSVD<4>	N35	RSVD4
TP_NB_RSVD<5>	AR12	RSVD5
TP_NB_RSVD<6>	AR13	RSVD6
TP_NB_RSVD<7>	AM12	RSVD7
TP_NB_RSVD<8>	AN13	RSVD8
TP_NB_RSVD<9>	J12	RSVD9
TP_NB_RSVD<10>	AR37	RSVD10
TP_NB_RSVD<11>	AM36	RSVD11
TP_NB_RSVD<12>	AL36	RSVD12
TP_NB_RSVD<13>	AM37	RSVD13
TP_NB_RSVD<14>	D20	RSVD14
TP_NB_RSVD<20>	H10	RSVD20
TP_NB_RSVD<21>	B51	RSVD21
TP_NB_RSVD<22>	BJ20	RSVD22
TP_NB_RSVD<23>	BK22	RSVD23
TP_NB_RSVD<24>	BF19	RSVD24
TP_NB_RSVD<25>	BH20	RSVD25
TP_NB_RSVD<26>	BK18	RSVD26
TP_NB_RSVD<27>	BJ18	RSVD27
TP_MEM_CLKP2	BF23	SM_CK2
TP_MEM_CLKN2	BG23	SM_CK2*
TP_MEM_CLKP5	BC23	SM_CK5
TP_MEM_CLKN5	BD24	SM_CK5*
MEM_A_A<14>	BJ29	SA_MA14
MEM_B_A<14>	BE24	SB_MA14
TP_NB_RSVD<34>	BH39	RSVD34
TP_NB_RSVD<35>	AW20	RSVD35
TP_NB_RSVD<36>	BK20	RSVD36
TP_LVDS_A_DATAN3	C48	RSVD37
TP_LVDS_A_DATAP3	D47	RSVD38
TP_LVDS_B_DATAN3	B44	RSVD39
TP_LVDS_B_DATAP3	C44	RSVD40
TP_NB_RSVD<41>	A35	RSVD41
TP_NB_RSVD<42>	B37	RSVD42
TP_NB_RSVD<43>	B36	RSVD43
TP_NB_RSVD<44>	B34	RSVD44
TP_NB_RSVD<45>	C34	RSVD45

CFG

NB_BSEL<0>	P27	CFG0
NB_BSEL<1>	N27	CFG1
NB_BSEL<2>	N24	CFG2
NB_CFG<3>	C21	CFG3 IPU
NB_CFG<4>	C23	CFG4 IPU
NB_CFG<5>	F23	CFG5 IPU
NB_CFG<6>	N23	CFG6 IPU
NB_CFG<7>	G23	CFG7 IPU
NB_CFG<8>	J20	CFG8 IPU
NB_CFG<9>	C20	CFG9 IPU
TP_NB_CFG<10>	R24	CFG10 IPU
TP_NB_CFG<11>	L23	CFG11 IPU
TP_NB_CFG<12>	J23	CFG12 IPU
TP_NB_CFG<13>	E23	CFG13 IPU
TP_NB_CFG<14>	E20	CFG14 IPU
TP_NB_CFG<15>	G23	CFG15 IPU
NB_CFG<16>	M20	CFG16 IPU
TP_NB_CFG<17>	M24	CFG17 IPU
TP_NB_CFG<18>	L32	CFG18 IPD
NB_CFG<19>	N33	CFG19 IPD
NB_CFG<20>	L35	CFG20 IPD

PM

PM_BMBUSY_L	G41	PM_BM_BUSY*
CPU_DPRSTP_L	L39	PM_DPRSTP*
	L36	PM_EXT_TS0*
	J36	PM_EXT_TS1*
VR_PWRGOOD_DELAY	AW49	PWROK
NB_RESET_L	AV20	RSTIN*
PM_THRMTRIP_L	N20	THERMTRIP*
PM_DPRSLPVR	G36	DPRSLPVR

NC

TP_NB_NC<1>	BJ51	NC1
TP_NB_NC<2>	BK51	NC2
TP_NB_NC<3>	BK50	NC3
TP_NB_NC<4>	BL50	NC4
TP_NB_NC<5>	BL49	NC5
TP_NB_NC<6>	BL3	NC6
TP_NB_NC<7>	BL2	NC7
TP_NB_NC<8>	BK1	NC8
TP_NB_NC<9>	BJ1	NC9
TP_NB_NC<10>	E1	NC10
TP_NB_NC<11>	A5	NC11
TP_NB_NC<12>	C51	NC12
TP_NB_NC<13>	B50	NC13
TP_NB_NC<14>	A50	NC14
TP_NB_NC<15>	A49	NC15
TP_NB_NC<16>	BK2	NC16

DDR MUXING

SM_CK0	AV29	MEM_CLK_P<0>
SM_CK1	BB23	MEM_CLK_P<1>
SM_CK3	BA25	MEM_CLK_P<3>
SM_CK4	AV23	MEM_CLK_P<4>
SM_CK0*	AW30	MEM_CLK_N<0>
SM_CK1*	BA23	MEM_CLK_N<1>
SM_CK3*	AW25	MEM_CLK_N<3>
SM_CK4*	AW23	MEM_CLK_N<4>
SM_CKE0	BE29	MEM_CKE<0>
SM_CKE1	AY32	MEM_CKE<1>
SM_CKE3	BD39	MEM_CKE<3>
SM_CKE4	BG37	MEM_CKE<4>
SM_CS0*	BG20	MEM_CS_L<0>
SM_CS1*	BK16	MEM_CS_L<1>
SM_CS2*	BG16	MEM_CS_L<2>
SM_CS3*	BE13	MEM_CS_L<3>
SM_ODT0	BH18	MEM_ODT<0>
SM_ODT1	BJ15	MEM_ODT<1>
SM_ODT2	BJ14	MEM_ODT<2>
SM_ODT3	BE16	MEM_ODT<3>
SM_RCOMP	BL15	MEM_RCOMP
SM_RCOMP*	BK14	MEM_RCOMP_L
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL
SM_VREF0	AR49	=PP0V9_S3M_MEM_NBVREFA
SM_VREF1	AW4	=PP0V9_S3M_MEM_NBVREFB

=PP1V8_S3M_MEM_NB

R1610 20 1% 1/16W MF-LF 402 — R1620 1K 1% 1/16W MF-LF 402 — R1622 3.01K 1% 1/16W MF-LF 402 — R1611 20 1% 1/16W MF-LF 402 — R1624 1K 1% 1/16W MF-LF 402

C1623 0.01UF 10% 16V CERM 402 — C1622 2.2UF 20% 6.3V CERM1 603 — C1625 0.01UF 10% 16V CERM 402 — C1624 2.2UF 20% 6.3V CERM1 603

C1615 0.1uF 20% 10V CERM 402 — C1616 0.1uF 20% 10V CERM 402

CLK

DPLL_REF_CLK	B42	=NB_CLK96M_DOT_P
DPLL_REF_CLK*	C42	=NB_CLK96M_DOT_N
DPLL_REF_SSCLK	H48	=NB_CLK100M_DPLLSS_P
DPLL_REF_SSCLK*	H47	=NB_CLK100M_DPLLSS_N
PEG_CLK	K44	NB_CLK100M_PCIE_P
PEG_CLK*	K45	NB_CLK100M_PCIE_N

Clk used for PEG and DMI

DMI

DMI_RXN0	AN47	DMI_S2N_N<0>
DMI_RXN1	AJ38	DMI_S2N_N<1>
DMI_RXN2	AN42	DMI_S2N_N<2>
DMI_RXN3	AN46	DMI_S2N_N<3>
DMI_RXP0	AM47	DMI_S2N_P<0>
DMI_RXP1	AJ39	DMI_S2N_P<1>
DMI_RXP2	AN41	DMI_S2N_P<2>
DMI_RXP3	AN45	DMI_S2N_P<3>
DMI_TXN0	AJ46	DMI_N2S_N<0>
DMI_TXN1	AJ41	DMI_N2S_N<1>
DMI_TXN2	AM40	DMI_N2S_N<2>
DMI_TXN3	AM44	DMI_N2S_N<3>
DMI_TXP0	AJ47	DMI_N2S_P<0>
DMI_TXP1	AJ42	DMI_N2S_P<1>
DMI_TXP2	AM39	DMI_N2S_P<2>
DMI_TXP3	AM43	DMI_N2S_P<3>

GRAPHICS VID

GFX_VID0	E35	GFX_VID<0>
GFX_VID1	A39	GFX_VID<1>
GFX_VID2	C38	GFX_VID<2>
GFX_VID3	B39	GFX_VID<3>
GFX_VR_EN	E36	GFX_VR_EN

MISC

SDVO_CTRL_CLK	H35	SDVO_CTRLCLK
SDVO_CTRL_DATA	K36	SDVO_CTRLDATA
CLKREQ*	G39	NB_CLKREQ_L
ICH_SYNC*	G40	NB_SB_SYNC_L
TEST1	A37	NB_TEST1
TEST2	R32	NB_TEST2

CL_CLK	AM49	CLINK_NB_CLK
CL_DATA	AK50	CLINK_NB_DATA
CL_PWROK	AT43	=NB_CLINK_MPWROK
CL_RST*	AN49	CLINK_NB_RESET_L
CL_VREF	AM50	NB_CLINK_VREF

R1691 20K 5% 1/16W MF-LF 402 — R1690 0 5% 1/16W MF-LF 402

PP1V25_S0M_NB_VCCAXD

R1640 1K 1% 1/16W MF-LF 402 — C1640 0.1uF 20% 10V CERM 402 — R1641 392 1% 1/16W MF-LF 402

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=T9_MLB — SYNC_DATE=01/21/2007

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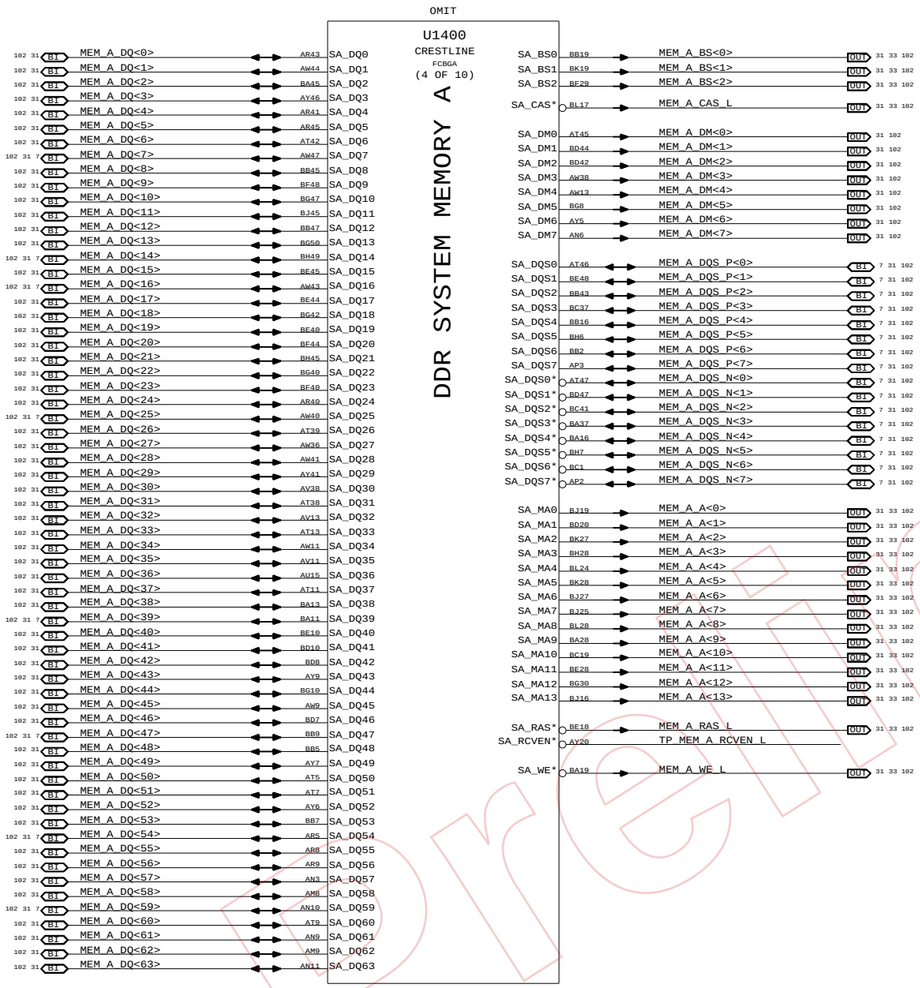
SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 16 OF 118	



NB DDR2 Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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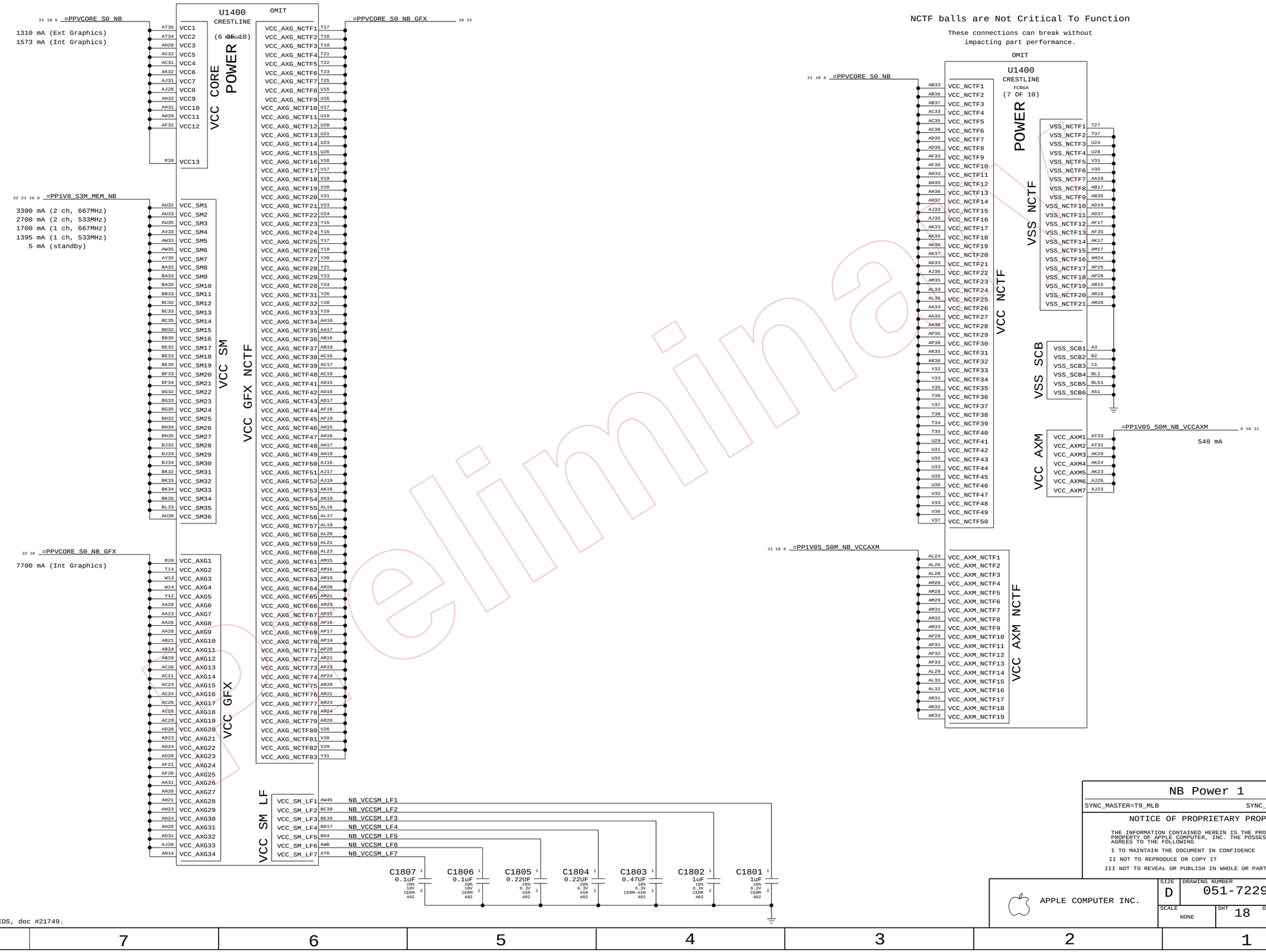
D	051-7229	33

SCALE: NONE

SHT 17 OF 118



NB Power 1

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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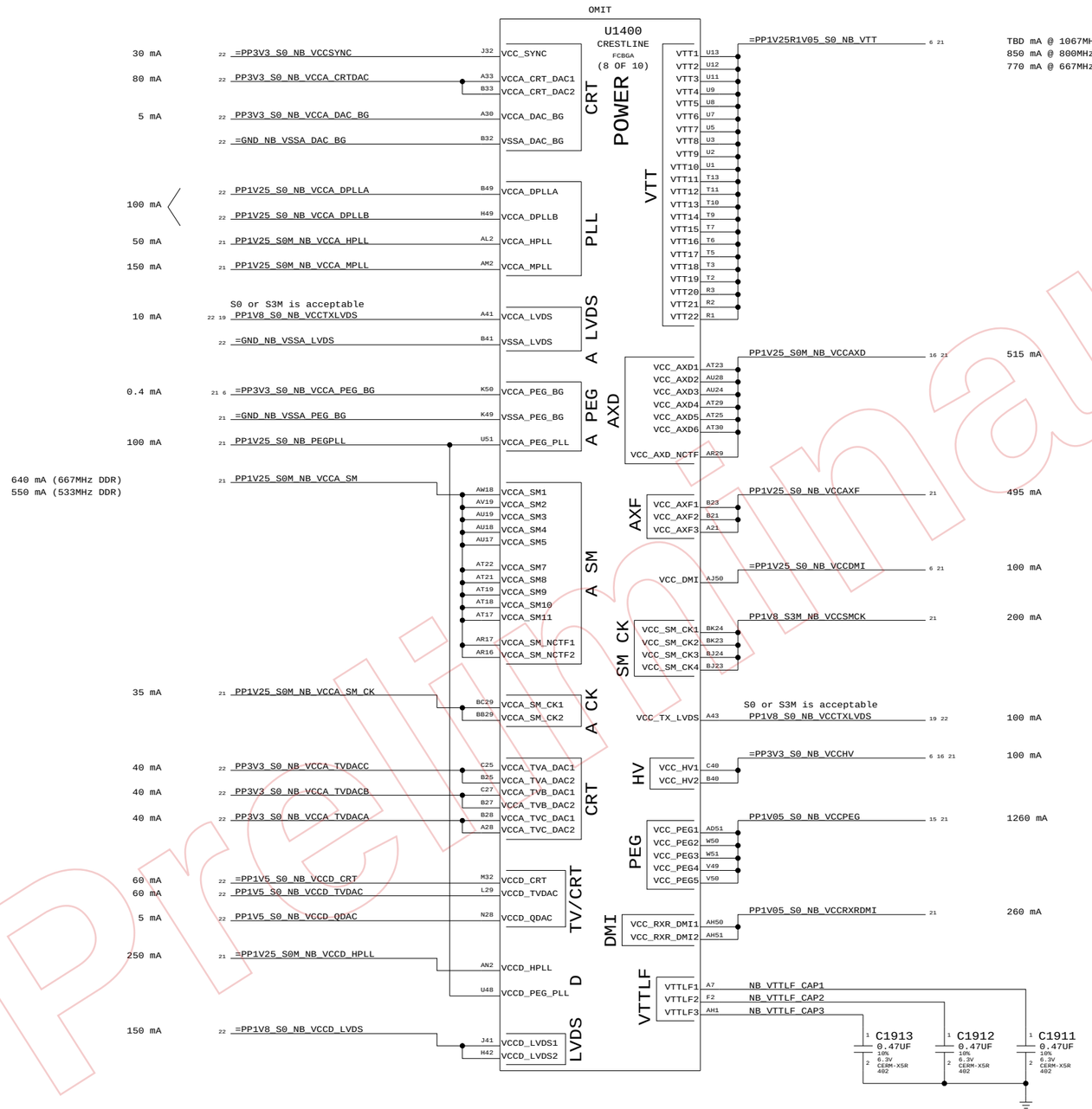

Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE	VSS302 T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE	VSS303 T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE	VSS304 T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE	VSS305 R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 =NB_TDE_SENSE 55

NOTE: TDE = _P

TDE_FORCE T31 =NB_TDE_FORCE 55

TDB_FORCE T33 =NB_TDB_FORCE 55

NOTE: TDB = _N

TDB_SENSE R28 =NB_TDB_SENSE 55

NB Grounds

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE COMPUTER INC.

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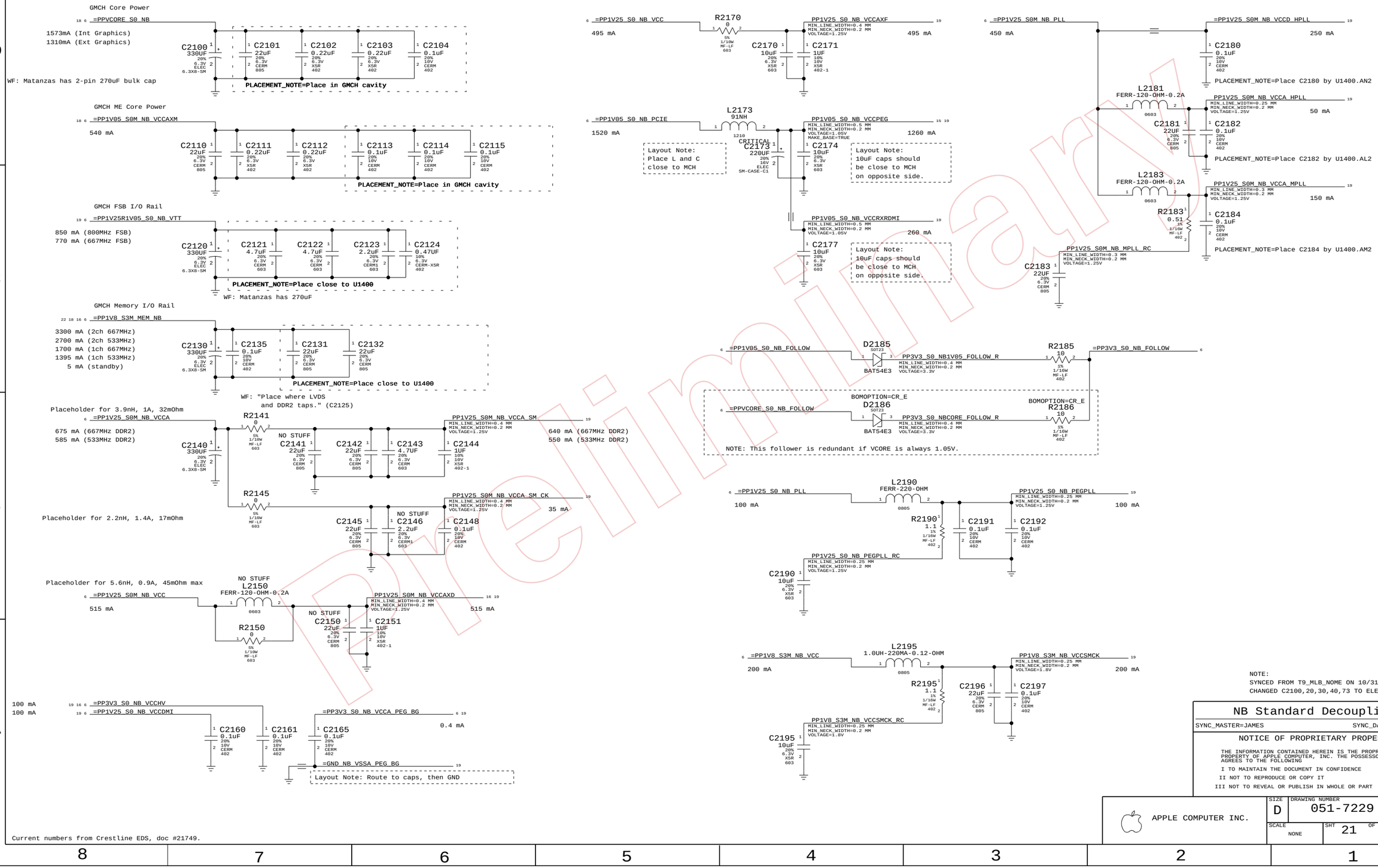
GMCH Core Power
=PPVCORE_S0_NB
1573mA (Int Graphics)
1310mA (Ext Graphics)
C2100 330UF 20% 6.3V ELEC 6.3X8-SM
C2101 22uF 20% 6.3V CERM 805
C2102 0.22uF 20% 6.3V X5R 402
C2103 0.22uF 20% 6.3V X5R 402
C2104 0.1uF 20% 10V CERM 402
WF: Matanzas has 2-pin 270uF bulk cap
PLACEMENT_NOTE=Place in GMCH cavity
GMCH ME Core Power
=PP1V05_S0M_NB_VCCAXM
540 mA
C2110 22uF 20% 6.3V CERM 805
C2111 0.22uF 20% 6.3V X5R 402
C2112 0.22uF 20% 6.3V X5R 402
C2113 0.1uF 20% 10V CERM 402
C2114 0.1uF 20% 10V CERM 402
C2115 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place in GMCH cavity
GMCH FSB I/O Rail
=PP1V25R1V05_S0_NB_VTT
850 mA (800MHz FSB)
770 mA (667MHz FSB)
C2120 330UF 20% 6.3V ELEC 6.3X8-SM
C2121 4.7uF 20% 6.3V CERM 603
C2122 4.7uF 20% 6.3V CERM 603
C2123 2.2uF 20% 6.3V CERM1 603
C2124 0.47UF 10% 6.3V CERM-X5R 402
PLACEMENT_NOTE=Place close to U1400
WF: Matanzas has 270uF
GMCH Memory I/O Rail
=PP1V8_S3M_MEM_NB
3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)
C2130 330UF 20% 6.3V ELEC 6.3X8-SM
C2135 0.1uF 20% 10V CERM 402
C2131 22uF 20% 6.3V CERM 805
C2132 22uF 20% 6.3V CERM 805
PLACEMENT_NOTE=Place close to U1400
WF: "Place where LVDS and DDR2 taps." (C2125)
Placeholder for 3.9nH, 1A, 32mOhm
=PP1V25_S0M_NB_VCCA
675 mA (667MHz DDR2)
585 mA (533MHz DDR2)
R2141 0 5% 1/10W MF-LF 603
NO STUFF
C2140 330UF 20% 6.3V ELEC 6.3X8-SM
C2141 22uF 20% 6.3V CERM 805
C2142 22uF 20% 6.3V CERM 805
C2143 4.7UF 20% 6.3V CERM 603
C2144 1UF 10% 10V X5R 402-1
PP1V25_S0M_NB_VCCA_SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
640 mA (667MHz DDR2)
550 mA (533MHz DDR2)
R2145 0 5% 1/10W MF-LF 603
PP1V25_S0M_NB_VCCA_SM_CK
35 mA
Placeholder for 2.2nH, 1.4A, 17mOhm
NO STUFF
C2145 22uF 20% 6.3V CERM 805
C2146 2.2uF 20% 6.3V CERM1 603
C2148 0.1uF 20% 10V CERM 402
Placeholder for 5.6nH, 0.9A, 45mOhm max
NO STUFF
L2150 FERR-120-OHM-0.2A 0603
=PP1V25_S0M_NB_VCC
515 mA
R2150 0 5% 1/10W MF-LF 603
NO STUFF
C2150 22uF 20% 6.3V CERM 805
C2151 1UF 10% 10V X5R 402-1
PP1V25_S0M_NB_VCCAXD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
515 mA
100 mA
100 mA
=PP3V3_S0_NB_VCCHV
=PP1V25_S0_NB_VCCDMI
C2160 0.1uF 20% 10V CERM 402
C2161 0.1uF 20% 10V CERM 402
=PP3V3_S0_NB_VCCA_PEG_BG
C2165 0.1uF 20% 10V CERM 402
0.4 mA
=GND_NB_VSSA_PEG_BG
Layout Note: Route to caps, then GND
=PP1V25_S0_NB_VCC
495 mA
R2170 0 5% 1/10W MF-LF 603
C2170 10uF 20% 6.3V X5R 603
C2171 1UF 10% 10V X5R 402-1
PP1V25_S0_NB_VCCAXF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
495 mA
=PP1V05_S0_NB_PCIE
1520 mA
L2173 91NH 1210 CRITICAL
C2173 220UF 20% 16V ELEC SM-CASE-C1
Layout Note: Place L and C close to MCH
C2174 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
PP1V05_S0_NB_VCCPEG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
1260 mA
PP1V05_S0_NB_VCCRXRDMI
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
260 mA
C2177 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
=PP1V25_S0M_NB_PLL
450 mA
=PP1V25_S0M_NB_VCCD_HPLL
250 mA
C2180 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2180 by U1400.AN2
L2181 FERR-120-OHM-0.2A 0603
PP1V25_S0M_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
50 mA
C2181 22UF 20% 6.3V CERM 805
C2182 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2182 by U1400.AL2
L2183 FERR-120-OHM-0.2A 0603
PP1V25_S0M_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
150 mA
R2183 0.51 1% 1/10W MF-LF 402
C2184 0.1uF 20% 10V CERM 402
PLACEMENT_NOTE=Place C2184 by U1400.AM2
PP1V25_S0M_NB_MPLL_RC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2183 22UF 20% 6.3V CERM 805
=PP1V05_S0_NB_FOLLOW
D2185 SOT23 BAT54E3
PP3V3_S0_NB1V05_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
R2185 10 1% 1/16W MF-LF 402
=PP3V3_S0_NB_FOLLOW
BOMOPTION=CR_E
=PPVCORE_S0_NB_FOLLOW
D2186 SOT23 BAT54E3
PP3V3_S0_NBCORE_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
BOMOPTION=CR_E
R2186 10 1% 1/16W MF-LF 402
NOTE: This follower is redundant if VCORE is always 1.05V.
=PP1V25_S0_NB_PLL
100 mA
L2190 FERR-220-OHM 0805
R2190 1.1 1% 1/16W MF-LF 402
PP1V25_S0_NB_PEGPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
100 mA
C2191 0.1uF 20% 10V CERM 402
C2192 0.1uF 20% 10V CERM 402
PP1V25_S0_NB_PEGPLL_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V
C2190 10uF 20% 6.3V X5R 603
=PP1V8_S3M_NB_VCC
200 mA
L2195 1.0UH-220MA-0.12-OHM 0805
R2195 1.1 1% 1/16W MF-LF 402
PP1V8_S3M_NB_VCCSMCK
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
200 mA
C2196 22UF 20% 6.3V CERM 805
C2197 0.1uF 20% 10V CERM 402
PP1V8_S3M_NB_VCCSMCK_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
C2195 10uF 20% 6.3V X5R 603
Current numbers from Crestline EDS, doc #21749.
NOTE:
SYNCED FROM T9_MLB_NOME ON 10/31/06
CHANGED C2100,20,30,40,73 TO ELEC
NB Standard Decoupling
SYNC_MASTER=JAMES
SYNC_DATE=11/03/2006
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SIZE D
DRAWING NUMBER 051-7229
REV. 33
SCALE NONE
SHT 21 OF 118

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

15 LVDS_BKLT_CTL — TRUE — TP_LVDS_BKLT_CTL
15 LVDS_BKLT_EN — TRUE — TP_LVDS_BKLT_EN
15 13 LVDS_CTRL_CLK
15 13 LVDS_CTRL_DATA
15 LVDS_DDC_CLK
15 LVDS_DDC_DATA
15 LVDS_VDD_EN — TRUE — TP_LVDS_VDD_EN

15 LVDS_IBG — TRUE — TP_LVDS_IBG
15 LVDS_VREFH — TRUE — TP_LVDS_VREFH
15 LVDS_VREFL — TRUE — TP_LVDS_VREFL
15 LVDS_A_CLK_N — TRUE — TP_LVDS_A_CLK_N
15 LVDS_A_CLK_P — TRUE — TP_LVDS_A_CLK_P
15 LVDS_B_CLK_N — TRUE — TP_LVDS_B_CLK_N
15 LVDS_B_CLK_P — TRUE — TP_LVDS_B_CLK_P

15 LVDS_A_DATA_N<0> — TRUE — TP_LVDS_A_DATA_N<0>
15 LVDS_A_DATA_N<1> — TRUE — TP_LVDS_A_DATA_N<1>
15 LVDS_A_DATA_N<2> — TRUE — TP_LVDS_A_DATA_N<2>

15 LVDS_A_DATA_P<0> — TRUE — TP_LVDS_A_DATA_P<0>
15 LVDS_A_DATA_P<1> — TRUE — TP_LVDS_A_DATA_P<1>
15 LVDS_A_DATA_P<2> — TRUE — TP_LVDS_A_DATA_P<2>

15 LVDS_B_DATA_N<0> — TRUE — TP_LVDS_B_DATA_N<0>
15 LVDS_B_DATA_N<1> — TRUE — TP_LVDS_B_DATA_N<1>
15 LVDS_B_DATA_N<2> — TRUE — TP_LVDS_B_DATA_N<2>

15 LVDS_B_DATA_P<0> — TRUE — TP_LVDS_B_DATA_P<0>
15 LVDS_B_DATA_P<1> — TRUE — TP_LVDS_B_DATA_P<1>
15 LVDS_B_DATA_P<2> — TRUE — TP_LVDS_B_DATA_P<2>

15 =TV_A_DAC
15 =TV_B_DAC
15 =TV_C_DAC

15 =TV_A_RTN
15 =TV_B_RTN
15 =TV_C_RTN

15 TV_DCONSEL<0>
15 TV_DCONSEL<1>

15 =CRT_BLUE
15 =CRT_BLUE_L
15 =CRT_GREEN
15 =CRT_GREEN_L
15 =CRT_RED
15 =CRT_RED_L

15 CRT_DDC_CLK
15 CRT_DDC_DATA
15 =CRT_HSYNC_R
15 =CRT_TVO_IREF
15 =CRT_VSYNC_R

16 =NB_CLK96M_DOT_P
16 =NB_CLK96M_DOT_N

16 =NB_CLK100M_DPLLSS_P
16 =NB_CLK100M_DPLLSS_N

16 SDVO_CTRLCLK
16 SDVO_CTRLDATA

16 GFX_VID<1> — TRUE — TP_GFX_VID<1>
16 GFX_VID<2> — TRUE — TP_GFX_VID<2>
16 GFX_VID<3> — TRUE — TP_GFX_VID<3>
16 GFX_VID<4> — TRUE — TP_GFX_VID<4>
16 =GFX_VR_EN — TRUE — TP_GFX_VR_EN

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

PP1V25_S0_NB_VCCA_DPLLA 19
PP1V25_S0_NB_VCCA_DPLLB 19
=PP1V5_S0_NB_VCCD_CRT 19
PP1V5_S0_NB_VCCD_QDAC 19
=PPVCORE_S0_NB_GFX 18
PP3V3_S0_NB_VCCA_CRTDAC 19
PP3V3_S0_NB_VCCA_TVDACA 19
PP3V3_S0_NB_VCCA_TVDACB 19
PP3V3_S0_NB_VCCA_TVDACC 19
PP3V3_S0_NB_VCCA_DAC_BG 19
=GND_NB_VSSA_DAC_BG 19
PP1V8_S0_NB_VCCTXLVDS 19

NOTE:
SANTA ROSA PLATFORM P180 FIG 119 - NC
ALSO CONFIRMED WITH INTEL

TP_NB_VSSA_LVDS — TRUE — =GND_NB_VSSA_LVDS 19

=PP1V8_S0_NB_VCCD_LVDS 19
=PP3V3_S0_NB_VCCSYNC 19

16 =NB_CLINK_MPWROK — TRUE — VR_PWRGOOD_DELAY 7 16 70 71

VCCD_TVDAC ALSO POWERS INTERNAL THERMAL SENSORS.
CRITICAL
C2201
22000pF-1000mA
16V
NPM1B

6 =PP1V5_S0_NB_TVDAC
65 mA

C2213
10uF
20%
6.3V
X5R
603

C2200
0.1uF
20%
10V
CERM
402

PP1V5_S0_NB_VCCD_TVDAC 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
60 mA

Layout Note:
THESE CAPS SHOULD BE
within 6.35 mm of NB edge

21 18 16 6 =PP1V8_S3M_MEM_NB

R2200
1K
5%
1/16W
MF-LF
402

R2202
1K
5%
1/16W
MF-LF
402

PP0V9_S3M_MEM_NBVREFA — TRUE — =PP0V9_S3M_MEM_NBVREFA 7 16
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM

PP0V9_S3M_MEM_NBVREFB — TRUE — =PP0V9_S3M_MEM_NBVREFB 7 16
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM

R2201
1K
5%
1/16W
MF-LF
402

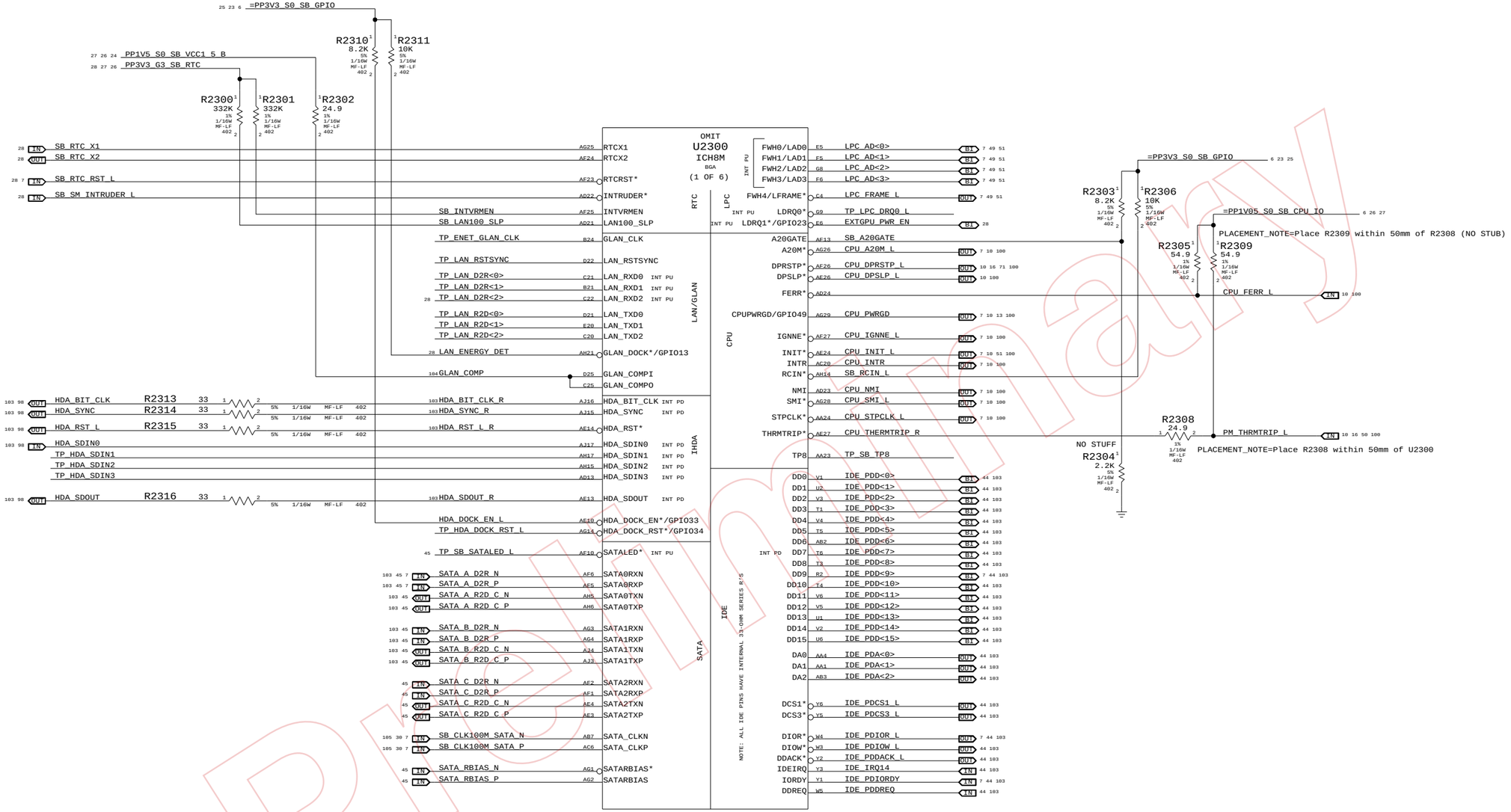
R2203
1K
5%
1/16W
MF-LF
402

NB Graphics Decoupling

SYNC_MASTER=JAMES SYNC_DATE=10/16/06

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 22 OF 118	



	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

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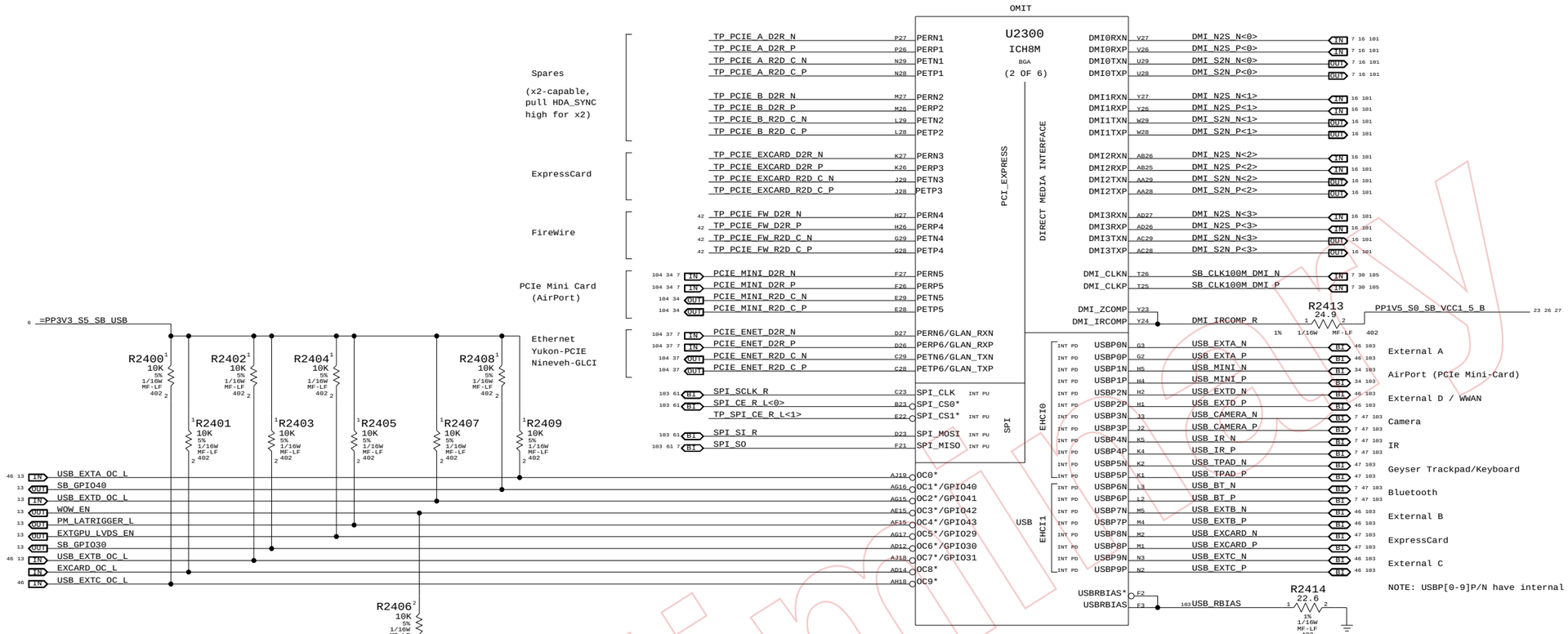
OMIT
U2300
ICH8M
BGA
(2 OF 6)
PCI_EXPRESS
DIRECT MEDIA INTERFACE
SPI
USB
EHCI0
EHCI1
Spares
(x2-capable, pull HDA_SYNC high for x2)
ExpressCard
FireWire
PCIe Mini Card (AirPort)
Ethernet Yukon-PCIE Nineveh-GLCI
TP_PCIE_A_D2R_N
TP_PCIE_A_D2R_P
TP_PCIE_A_R2D_C_N
TP_PCIE_A_R2D_C_P
TP_PCIE_B_D2R_N
TP_PCIE_B_D2R_P
TP_PCIE_B_R2D_C_N
TP_PCIE_B_R2D_C_P
TP_PCIE_EXCARD_D2R_N
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_R2D_C_N
TP_PCIE_EXCARD_R2D_C_P
TP_PCIE_FW_D2R_N
TP_PCIE_FW_D2R_P
TP_PCIE_FW_R2D_C_N
TP_PCIE_FW_R2D_C_P
PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
SPI_SCLK_R
SPI_CE_R_L<0>
TP_SPI_CE_R_L<1>
SPI_SI_R
SPI_SO
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_MOSI
SPI_MISO
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_IRCOMP_R
R2413
24.9
PP1V5_S0_SB_VCC1_5_B
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USB_EXTA_N
USB_EXTA_P
USB_MINI_N
USB_MINI_P
USB_EXTD_N
USB_EXTD_P
USB_CAMERA_N
USB_CAMERA_P
USB_IR_N
USB_IR_P
USB_TPAD_N
USB_TPAD_P
USB_BT_N
USB_BT_P
USB_EXTB_N
USB_EXTB_P
USB_EXCARD_N
USB_EXCARD_P
USB_EXTC_N
USB_EXTC_P
External A
AirPort (PCIe Mini-Card)
External D / WWAN
Camera
IR
Geyser Trackpad/Keyboard
Bluetooth
External B
ExpressCard
External C
NOTE: USBP[0-9]P/N have internal 15K pull-downs.
USBRBIAS*
USBRBIAS
USB_RBIAS
R2414
22.6
=PP3V3_S5_SB_USB
R2400
R2401
R2402
R2403
R2404
R2405
R2407
R2408
R2409
10K
USB_EXTA_OC_L
SB_GPIO40
USB_EXTD_OC_L
WOW_EN
PM_LATRIGGER_L
EXTGPU_LVDS_EN
SB_GPIO30
USB_EXTB_OC_L
EXCARD_OC_L
USB_EXTC_OC_L
OC0*
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
OC8*
OC9*
R2406
10K
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.
PCI
INTERRUPT I/F
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
REQ0*
GNT0*
REQ1*/GPIO50
GNT1*/GPIO51
REQ2*/GPIO52
GNT2*/GPIO53
REQ3*/GPIO54
GNT3*/GPIO55
C/BE0*
C/BE1*
C/BE2*
C/BE3*
IRDY*
PAR
PCIRST*
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
FRAME*
PLTRST*
PCICLK
PME*
PCI_FW_REQ_L
PCI_REQ1_L
PCI_REQ2_L
TP_SB_GPIO51
TP_SB_GPIO53
ODD_RST_5VTOL_L
TP_SB_GPIO55
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_RST_L
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_STOP_L
PCI_SERR_L
PCI_FRAME_L
PLT_RST_L
PCI_CLK33M_SB
TP_PCI_PME_L
PCI_FW_GNT_L
MAKE_BASE=TRUE
BOOT_LPC_SPI_L
R2415
1K
R2415 pull-down on GNT0# selects SPI ROM by default.
INTERRUPT I/F
PIRQA*
PIRQB*
PIRQC*
PIRQD*
PIRQE*/GPIO2
PIRQF*/GPIO3
PIRQG*/GPIO4
PIRQH*/GPIO5
INT_PIRQE_L
INT_PIRQF_L
DVI_HOTPLUG_DET
ODD_PWR_EN_L
FireWire INT*
Provide a pull-down on this GPIO if not used.
SB BOOT BIOS SELECT
I/F
GNT0#
LPC
1
SPI
0
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
=PP3V3_S0_SB_PCI
R2423
R2424
R2425
R2426
R2427
R2428
R2430
R2429
R2432
R2431
R2433
R2437
R2436
R2438
R2439
R2440
R2441
R2442
8.2K
SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_MLB_NOME
SYNC_DATE=05/07/2007
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33
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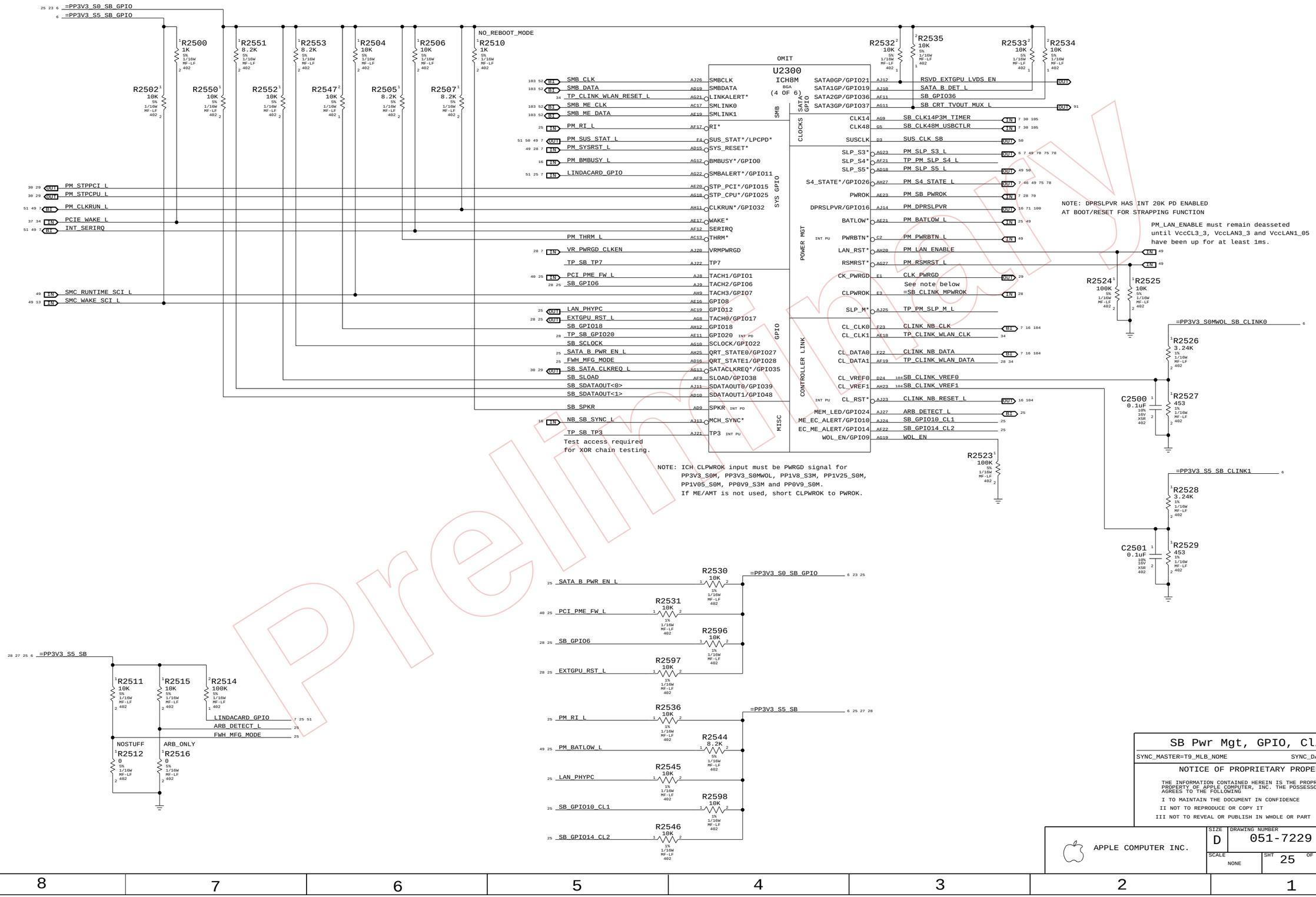
NONE
SHT
24
OF
118



SB Pwr Mgt, GPIO, Clink	
SYNC_MASTER=T9_MLB_NOME	SYNC_DATE=05/07/2007

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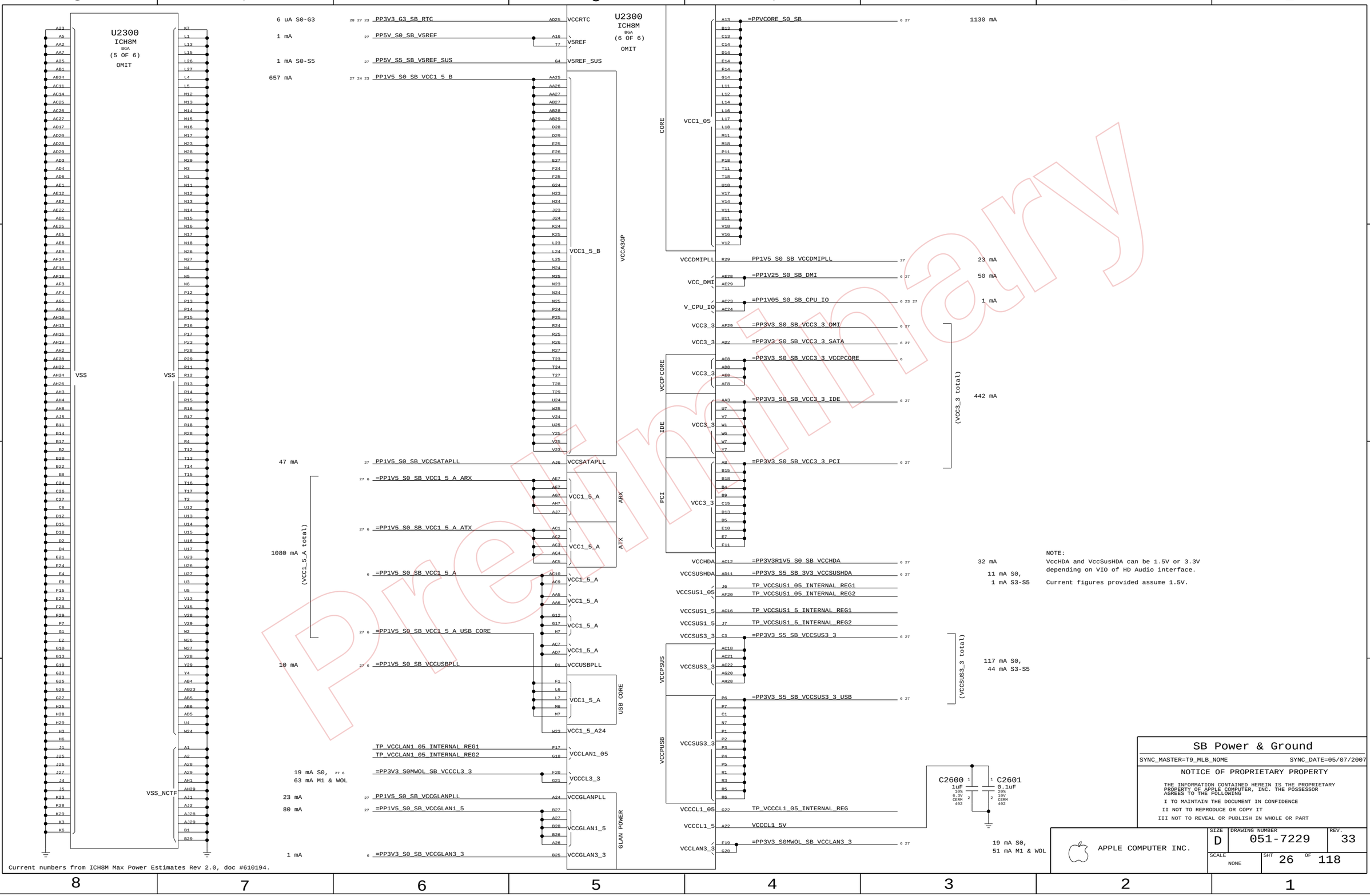
	SCALE: NONE	SHT 25 OF 118	


U2300
ICH8M
BGA
(5 OF 6)
OMIT
VSS
VSS_NCTF
U2300
ICH8M
BGA
(6 OF 6)
OMIT
6 uA S0-G3
1 mA
1 mA S0-S5
657 mA
47 mA
1080 mA (VCC1_5_A total)
10 mA
19 mA S0, 63 mA M1 & WOL
23 mA
80 mA
1 mA
PP3V3_G3_SB_RTC
PP5V_S0_SB_V5REF
PP5V_S5_SB_V5REF_SUS
PP1V5_S0_SB_VCC1_5_B
PP1V5_S0_SB_VCCSATAPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP1V5_S0_SB_VCCUSBPLL
TP_VCCLAN1_05_INTERNAL_REG1
TP_VCCLAN1_05_INTERNAL_REG2
=PP3V3_S0MWOL_SB_VCCCL3_3
PP1V5_S0_SB_VCCGLANPLL
=PP1V5_S0_SB_VCCGLAN1_5
=PP3V3_S0_SB_VCCGLAN3_3
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B
VCCSATAPLL
VCC1_5_A
VCCUSBPLL
VCCLAN1_05
VCCCL3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
VCCA3GP
ARX
ATX
USB CORE
GLAN POWER
=PPVCORE_S0_SB
1130 mA
CORE
VCC1_05
VCCDMIPLL
PP1V5_S0_SB_VCCDMIPLL
23 mA
VCC_DMI
=PP1V25_S0_SB_DMI
50 mA
V_CPU_IO
=PP1V05_S0_SB_CPU_IO
1 mA
VCC3_3
=PP3V3_S0_SB_VCC3_3_DMI
=PP3V3_S0_SB_VCC3_3_SATA
=PP3V3_S0_SB_VCC3_3_VCCPCORE
VCCPCORE
=PP3V3_S0_SB_VCC3_3_IDE
IDE
=PP3V3_S0_SB_VCC3_3_PCI
PCI
(VCC3_3 total)
442 mA
VCCHDA
=PP3V3R1V5_S0_SB_VCCHDA
32 mA
VCCSUSHDA
=PP3V3_S5_SB_3V3_VCCSUSHDA
11 mA S0, 1 mA S3-S5
VCCSUS1_05
TP_VCCSUS1_05_INTERNAL_REG1
TP_VCCSUS1_05_INTERNAL_REG2
VCCSUS1_5
TP_VCCSUS1_5_INTERNAL_REG1
TP_VCCSUS1_5_INTERNAL_REG2
VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3
VCCPSUS
=PP3V3_S5_SB_VCCSUS3_3_USB
VCCPUSB
(VCCSUS3_3 total)
117 mA S0, 44 mA S3-S5
VCCCL1_05
TP_VCCCL1_05_INTERNAL_REG
VCCCL1_5
VCCCL1_5V
VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCLAN3_3
19 mA S0, 51 mA M1 & WOL
C2600 1uF 10% 6.3V CERM 402
C2601 0.1uF 20% 10V CERM 402
NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
SB Power & Ground
SYNC_MASTER=T9_MLB_NOME
SYNC_DATE=05/07/2007
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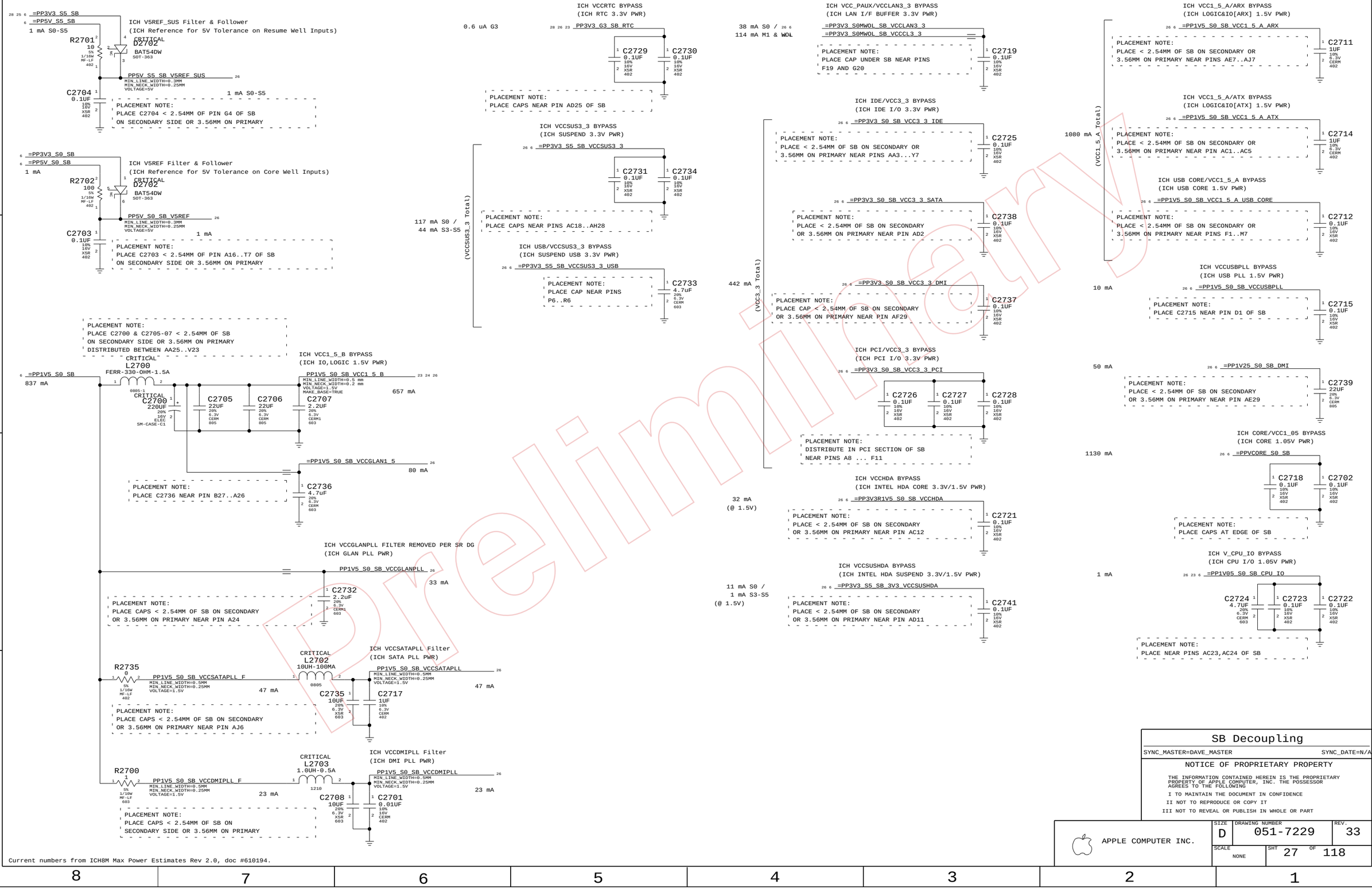
Preliminary


ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)
=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5
R2701
10
D2702
BAT54DW
SOT-363
CRITICAL
PP5V_S5_SB_V5REF_SUS
C2704
0.1UF
1 mA S0-S5
PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)
=PP3V3_S0_SB
=PP5V_S0_SB
1 mA
R2702
100
D2702
BAT54DW
SOT-363
CRITICAL
PP5V_S0_SB_V5REF
C2703
0.1UF
1 mA
PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23
ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
=PP1V5_S0_SB
837 mA
CRITICAL
L2700
FERR-330-OHM-1.5A
PP1V5_S0_SB_VCC1_5_B
657 mA
CRITICAL
C2700
220UF
C2705
22UF
C2706
22UF
C2707
2.2UF
=PP1V5_S0_SB_VCCGLAN1_5
80 mA
C2736
4.7uF
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26
ICH VCCGLANPLL FILTER REMOVED PER SR DG
(ICH GLAN PLL PWR)
PP1V5_S0_SB_VCCGLANPLL
33 mA
C2732
2.2uF
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24
ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
CRITICAL
L2702
10UH-100MA
R2735
0
PP1V5_S0_SB_VCCSATAPLL_F
47 mA
C2735
10UF
PP1V5_S0_SB_VCCSATAPLL
47 mA
C2717
1UF
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6
ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
CRITICAL
L2703
1.0UH-0.5A
R2700
1
PP1V5_S0_SB_VCCDMIPLL_F
23 mA
C2708
10UF
PP1V5_S0_SB_VCCDMIPLL
23 mA
C2701
0.01UF
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729
0.1UF
C2730
0.1UF
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2731
0.1UF
C2734
0.1UF
117 mA S0 /
44 mA S3-S5
(VCCSUS3_3 Total)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
C2733
4.7uF
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCCL3_3
C2719
0.1UF
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
C2725
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7
=PP3V3_S0_SB_VCC3_3_SATA
C2738
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2
442 mA
(VCC3_3 Total)
=PP3V3_S0_SB_VCC3_3_DMI
C2737
0.1UF
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2726
0.1UF
C2727
0.1UF
C2728
0.1UF
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11
ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
=PP3V3R1V5_S0_SB_VCCHDA
C2721
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12
ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
=PP3V3_S5_SB_3V3_VCCSUSHDA
C2741
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2711
1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
1080 mA
(VCC1_5_A Total)
C2714
1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
C2712
0.1UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
=PP1V5_S0_SB_VCCUSBPLL
C2715
0.1UF
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB
50 mA
=PP1V25_S0_SB_DMI
C2739
22UF
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
=PPVCORE_S0_SB
C2718
0.1UF
C2702
0.1UF
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
=PP1V05_S0_SB_CPU_IO
C2724
4.7UF
C2723
0.1UF
C2722
0.1UF
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
SB Decoupling
SYNC_MASTER=DAVE_MASTER
SYNC_DATE=N/A
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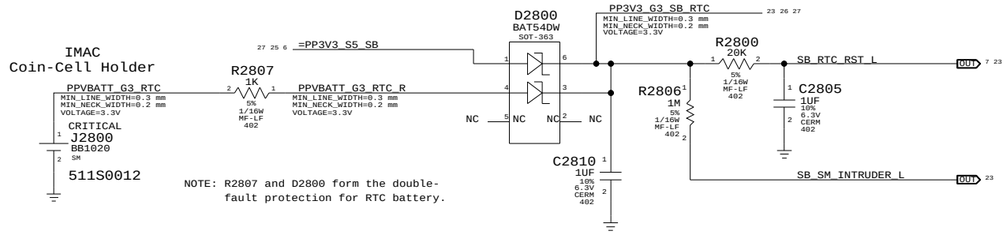
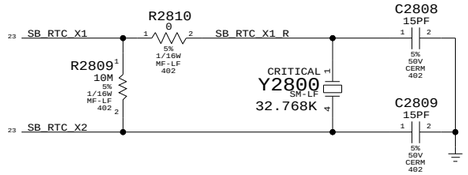
D
DRAWING NUMBER
051-7229
REV.
33
SCALE
NONE
SHT
27
OF
118
Preliminary

RTC Power Sources



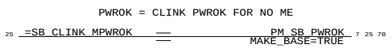
NOTE: R2807 and D2800 form the double-fault protection for RTC battery.

SB RTC Crystal

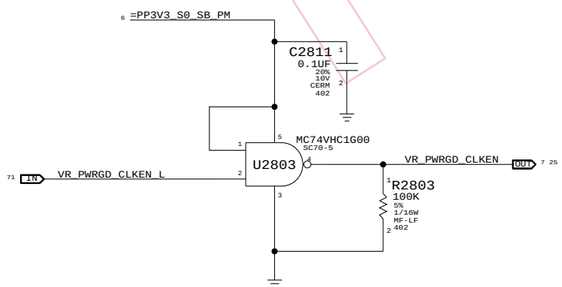


CPU VCORE FORCEPSI UNUSED

PWROK = CLINK PWROK FOR NO ME

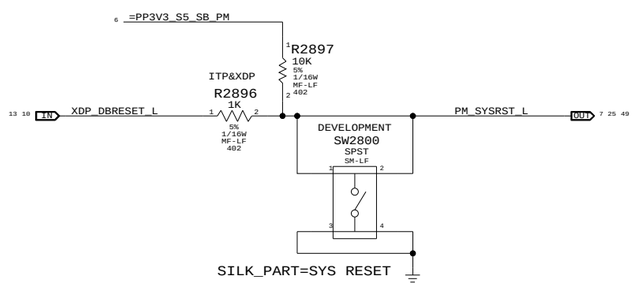


VRMPWRGD INVERTER



UNUSED PCI BUS

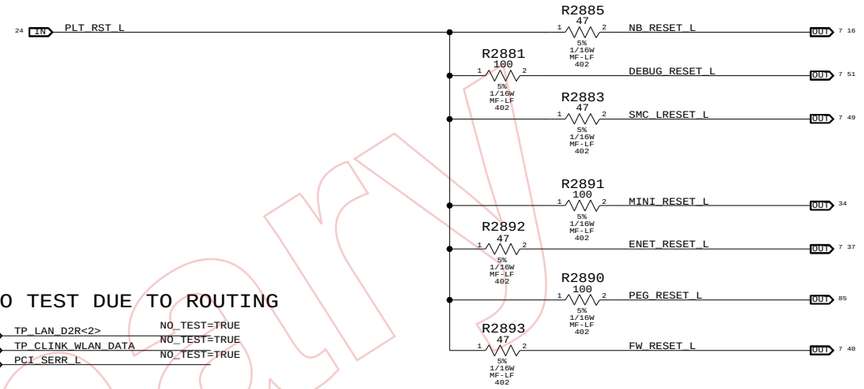
104 24	PCI_AD<0>	MAKE_BASE=TRUE	TP_PCI_AD_0	
104 24	PCI_AD<1>	MAKE_BASE=TRUE	TP_PCI_AD_1	
104 24	PCI_AD<2>	MAKE_BASE=TRUE	TP_PCI_AD_2	
104 24	PCI_AD<3>	MAKE_BASE=TRUE	TP_PCI_AD_3	
104 24	PCI_AD<4>	MAKE_BASE=TRUE	TP_PCI_AD_4	NO_TEST=TRUE
104 24	PCI_AD<5>	MAKE_BASE=TRUE	TP_PCI_AD_5	
104 24	PCI_AD<6>	MAKE_BASE=TRUE	TP_PCI_AD_6	
104 24	PCI_AD<7>	MAKE_BASE=TRUE	TP_PCI_AD_7	
104 24	PCI_AD<8>	MAKE_BASE=TRUE	TP_PCI_AD_8	
104 24	PCI_AD<9>	MAKE_BASE=TRUE	TP_PCI_AD_9	
104 24	PCI_AD<10>	MAKE_BASE=TRUE	TP_PCI_AD_10	
104 24	PCI_AD<11>	MAKE_BASE=TRUE	TP_PCI_AD_11	
104 24	PCI_AD<12>	MAKE_BASE=TRUE	TP_PCI_AD_12	
104 24	PCI_AD<13>	MAKE_BASE=TRUE	TP_PCI_AD_13	
104 24	PCI_AD<14>	MAKE_BASE=TRUE	TP_PCI_AD_14	
104 24	PCI_AD<15>	MAKE_BASE=TRUE	TP_PCI_AD_15	
104 24	PCI_AD<16>	MAKE_BASE=TRUE	TP_PCI_AD_16	
104 24	PCI_AD<17>	MAKE_BASE=TRUE	TP_PCI_AD_17	
104 24	PCI_AD<18>	MAKE_BASE=TRUE	TP_PCI_AD_18	
104 24	PCI_AD<19>	MAKE_BASE=TRUE	TP_PCI_AD_19	
104 24	PCI_AD<20>	MAKE_BASE=TRUE	TP_PCI_AD_20	
104 24	PCI_AD<21>	MAKE_BASE=TRUE	TP_PCI_AD_21	
104 24	PCI_AD<22>	MAKE_BASE=TRUE	TP_PCI_AD_22	
104 24	PCI_AD<23>	MAKE_BASE=TRUE	TP_PCI_AD_23	
104 24	PCI_AD<24>	MAKE_BASE=TRUE	TP_PCI_AD_24	
104 24	PCI_AD<25>	MAKE_BASE=TRUE	TP_PCI_AD_25	
104 24	PCI_AD<26>	MAKE_BASE=TRUE	TP_PCI_AD_26	
104 24	PCI_AD<27>	MAKE_BASE=TRUE	TP_PCI_AD_27	
104 24	PCI_AD<28>	MAKE_BASE=TRUE	TP_PCI_AD_28	
104 24	PCI_AD<29>	MAKE_BASE=TRUE	TP_PCI_AD_29	
104 24	PCI_AD<30>	MAKE_BASE=TRUE	TP_PCI_AD_30	
104 24	PCI_AD<31>	MAKE_BASE=TRUE	TP_PCI_AD_31	
104 24	PCI_C_BE_L<0>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_0	
104 24	PCI_C_BE_L<1>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_1	
104 24	PCI_C_BE_L<2>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_2	
104 24	PCI_C_BE_L<3>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_3	
24	PCI_RST_L	MAKE_BASE=TRUE	TP_PCI_RST_L	
104 24	PCI_PAR	MAKE_BASE=TRUE	TP_PCI_PAR	



SILK_PART=SYS RESET

Platform Reset Connections

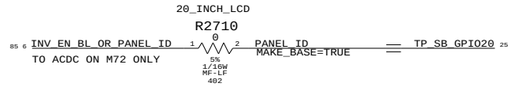
Unbuffered



NO TEST DUE TO ROUTING

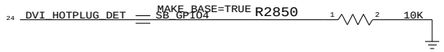
RE-PURPOSED GPIOS

20_INCH_LCD



TO ACDC ON M72 ONLY

UNUSED GPIOS

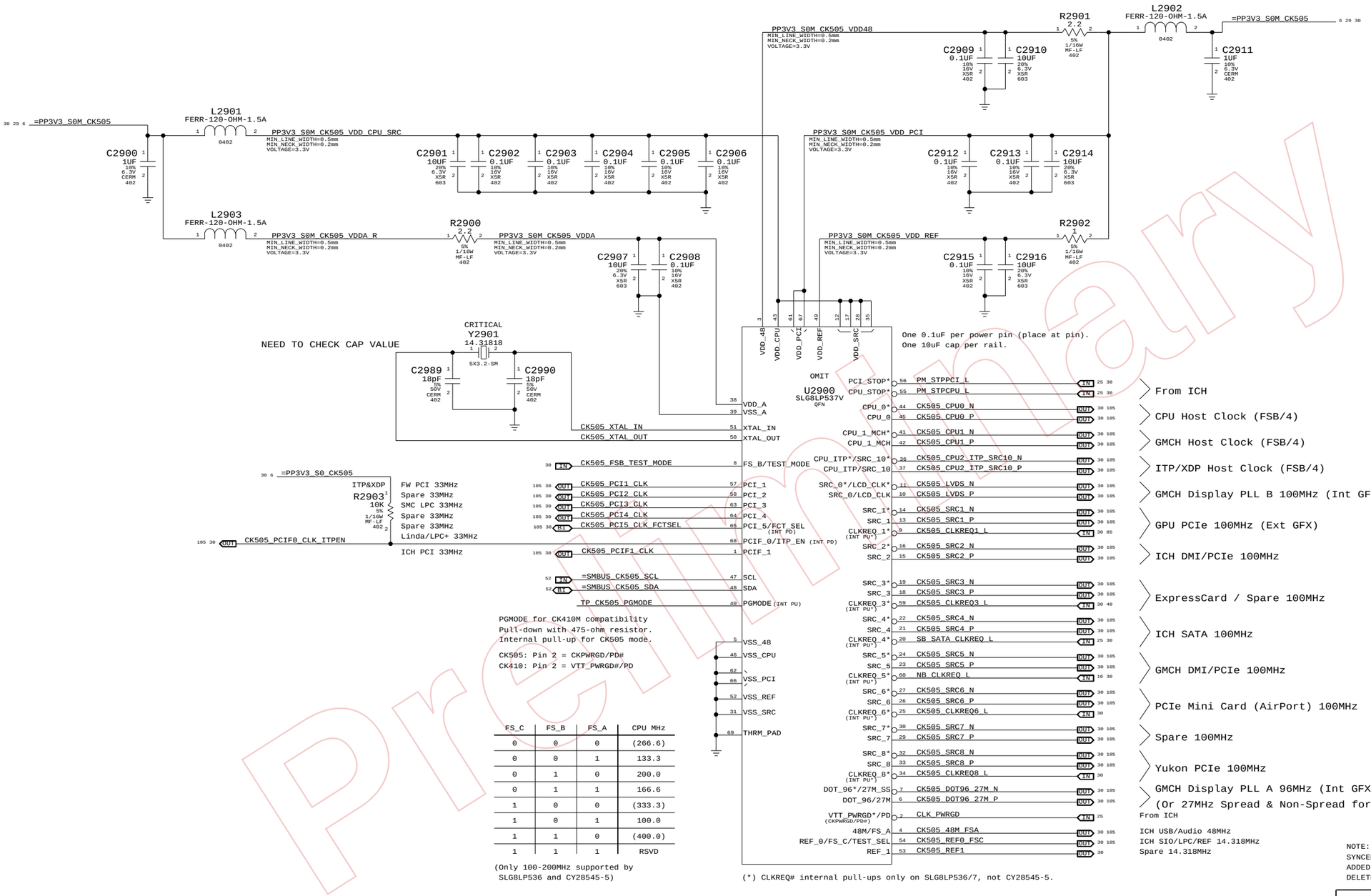


SB Misc

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 28 OF 118	


PP3V3_S0M_CK505_VDD48
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
R2901 2.2 5% 1/16W MF-LF 402
L2902 FERR-120-OHM-1.5A 0402
=PP3V3_S0M_CK505
C2909 0.1UF 10% 16V X5R 402
C2910 10UF 20% 6.3V X5R 603
C2911 1UF 10% 6.3V CERM 402
=PP3V3_S0M_CK505
L2901 FERR-120-OHM-1.5A 0402
PP3V3_S0M_CK505_VDD_CPU_SRC
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
C2900 1UF 10% 6.3V CERM 402
C2901 10UF 20% 6.3V X5R 603
C2902 0.1UF 10% 16V X5R 402
C2903 0.1UF 10% 16V X5R 402
C2904 0.1UF 10% 16V X5R 402
C2905 0.1UF 10% 16V X5R 402
C2906 0.1UF 10% 16V X5R 402
PP3V3_S0M_CK505_VDD_PCI
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
C2912 0.1UF 10% 16V X5R 402
C2913 0.1UF 10% 16V X5R 402
C2914 10UF 20% 6.3V X5R 603
L2903 FERR-120-OHM-1.5A 0402
PP3V3_S0M_CK505_VDDA_R
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
R2900 2.2 5% 1/16W MF-LF 402
PP3V3_S0M_CK505_VDDA
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
C2907 10UF 20% 6.3V X5R 603
C2908 0.1UF 10% 16V X5R 402
PP3V3_S0M_CK505_VDD_REF
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
C2915 0.1UF 10% 16V X5R 402
C2916 10UF 20% 6.3V X5R 603
R2902 1 5% 1/16W MF-LF 402
VDD_48
VDD_CPU
VDD_PCI
VDD_REF
VDD_SRC
One 0.1uF per power pin (place at pin).
One 10uF cap per rail.
NEED TO CHECK CAP VALUE
CRITICAL
Y2901 14.31818 5X3.2-SM
C2989 18pF 5% 50V CERM 402
C2990 18pF 5% 50V CERM 402
CK505_XTAL_IN
CK505_XTAL_OUT
VDD_A
VSS_A
XTAL_IN
XTAL_OUT
OMIT
U2900 SLG8LP537V QFN
PCI_STOP*
CPU_STOP*
PM_STPPCI_L
PM_STPCPU_L
From ICH
CPU_0*
CPU_0
CK505_CPU0_N
CK505_CPU0_P
CPU Host Clock (FSB/4)
CPU_1_MCH*
CPU_1_MCH
CK505_CPU1_N
CK505_CPU1_P
GMCH Host Clock (FSB/4)
CPU_ITP*/SRC_10*
CPU_ITP/SRC_10
CK505_CPU2_ITP_SRC10_N
CK505_CPU2_ITP_SRC10_P
ITP/XDP Host Clock (FSB/4)
SRC_0*/LCD_CLK*
SRC_0/LCD_CLK
CK505_LVDS_N
CK505_LVDS_P
GMCH Display PLL B 100MHz (Int GFX)
SRC_1*
SRC_1
CK505_SRC1_N
CK505_SRC1_P
GPU PCIe 100MHz (Ext GFX)
CLKREQ_1*
CK505_CLKREQ1_L
SRC_2*
SRC_2
CK505_SRC2_N
CK505_SRC2_P
ICH DMI/PCIe 100MHz
SRC_3*
SRC_3
CLKREQ_3*
CK505_SRC3_N
CK505_SRC3_P
CK505_CLKREQ3_L
ExpressCard / Spare 100MHz
SRC_4*
SRC_4
CLKREQ_4*
CK505_SRC4_N
CK505_SRC4_P
SB_SATA_CLKREQ_L
ICH SATA 100MHz
SRC_5*
SRC_5
CLKREQ_5*
CK505_SRC5_N
CK505_SRC5_P
NB_CLKREQ_L
GMCH DMI/PCIe 100MHz
SRC_6*
SRC_6
CLKREQ_6*
CK505_SRC6_N
CK505_SRC6_P
CK505_CLKREQ6_L
PCIe Mini Card (AirPort) 100MHz
SRC_7*
SRC_7
CK505_SRC7_N
CK505_SRC7_P
Spare 100MHz
SRC_8*
SRC_8
CLKREQ_8*
CK505_SRC8_N
CK505_SRC8_P
CK505_CLKREQ8_L
Yukon PCIe 100MHz
DOT_96*/27M_SS
DOT_96/27M
CK505_DOT96_27M_N
CK505_DOT96_27M_P
GMCH Display PLL A 96MHz (Int GFX)
(Or 27MHz Spread & Non-Spread for Ext GFX)
VTT_PWRGD*/PD
CLK_PWRGD
From ICH
48M/FS_A
CK505_48M_FSA
ICH USB/Audio 48MHz
REF_0/FS_C/TEST_SEL
CK505_REF0_FSC
ICH SIO/LPC/REF 14.318MHz
REF_1
CK505_REF1
Spare 14.318MHz
=PP3V3_S0_CK505
ITP&XDP
R2903 10K 5% 1/16W MF-LF 402
CK505_PCIF0_CLK_ITPEN
FW PCI 33MHz
Spare 33MHz
SMC LPC 33MHz
Spare 33MHz
Spare 33MHz
Linda/LPC+ 33MHz
ICH PCI 33MHz
CK505_PCI1_CLK
CK505_PCI2_CLK
CK505_PCI3_CLK
CK505_PCI4_CLK
CK505_PCI5_CLK_FCTSEL
CK505_PCIF1_CLK
PCI_1
PCI_2
PCI_3
PCI_4
PCI_5/FCT_SEL (INT PD)
PCIF_0/ITP_EN (INT PD)
PCIF_1
CK505_FSB_TEST_MODE
FS_B/TEST_MODE
=SMBUS_CK505_SCL
=SMBUS_CK505_SDA
SCL
SDA
TP_CK505_PGMODE
PGMODE (INT PU)
VSS_48
VSS_CPU
VSS_PCI
VSS_REF
VSS_SRC
THRM_PAD
PGMODE for CK410M compatibility
Pull-down with 475-ohm resistor.
Internal pull-up for CK505 mode.
CK505: Pin 2 = CKPWRGD/PD#
CK410: Pin 2 = VTT_PWRGD#/PD
FS_C FS_B FS_A CPU MHz
0 0 0 (266.6)
0 0 1 133.3
0 1 0 200.0
0 1 1 166.6
1 0 0 (333.3)
1 0 1 100.0
1 1 0 (400.0)
1 1 1 RSVD
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)
(*) CLKREQ# internal pull-ups only on SLG8LP536/7, not CY28545-5.
FCT_SEL PIN 6 PIN 7 PIN 10 PIN 11
0 DOT_96+ DOT_96- LCD_CLK+ LCD_CLK- (For Internal Graphics)
1 27M 27M w/SS SRC_0+ SRC_0- (For External Graphics)
NOTE:
SYNCED FROM T9_MLB_NOME
ADDED 475-OHM RESISTOR TO NB_CLKREQ_L PER INTEL
DELETED RES AFTER INTEL SAID IT'S NOT NEEDED!
Clock (CK505)
SYNC_MASTER=JAMES
SYNC_DATE=11/27/2006
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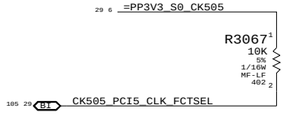
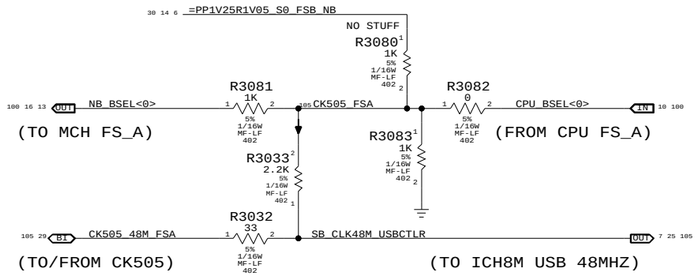
CK505 Configuration Straps

FCT_SEL (GFX clock select)

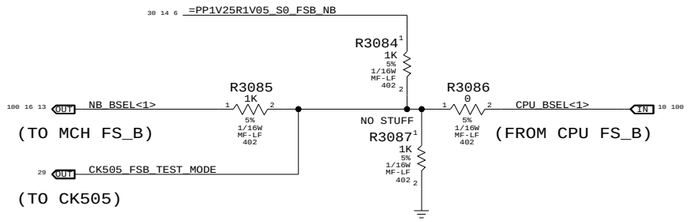


FS_A, FS_B, FS_C (Host clock freq select)



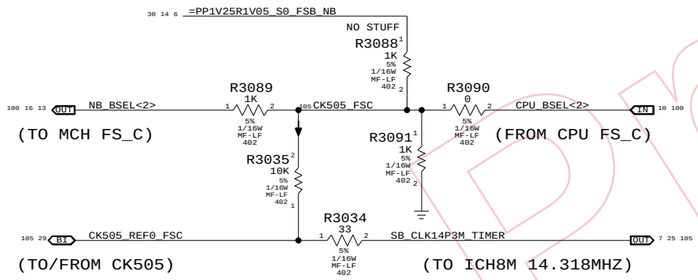
(TO MCH FS_A) (FROM CPU FS_A)

(TO/FROM CK505) (TO ICH8M USB 48MHZ)



(TO MCH FS_B) (FROM CPU FS_B)

(TO CK505)



(TO MCH FS_C) (FROM CPU FS_C)

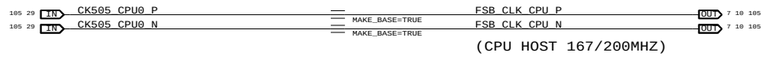
(TO/FROM CK505) (TO ICH8M 14.318MHZ)

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

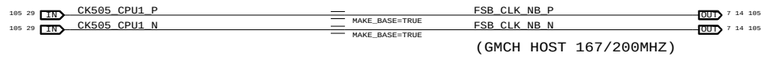
NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

CLK Termination

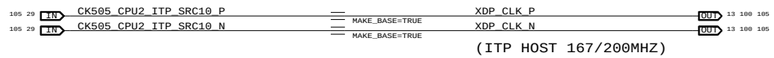
(Note: HOST/SRC/GFX clock termination kept on T9 for Cypress CY28545-5 compatibility)



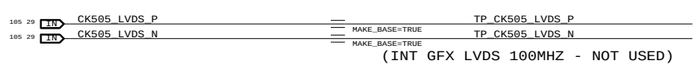
(CPU HOST 167/200MHZ)



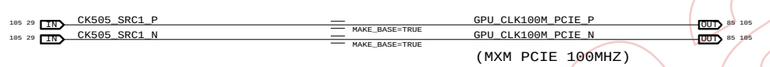
(GMCH HOST 167/200MHZ)



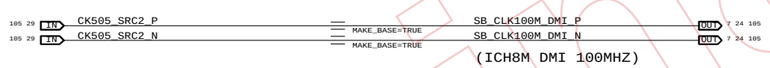
(ITP HOST 167/200MHZ)



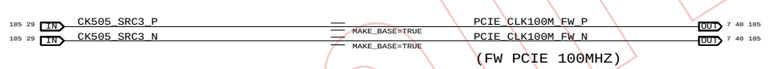
(INT GFX LVDS 100MHZ - NOT USED)



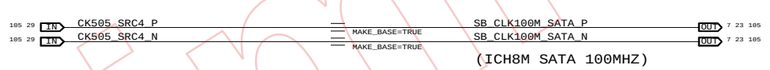
(MXM PCIE 100MHZ)



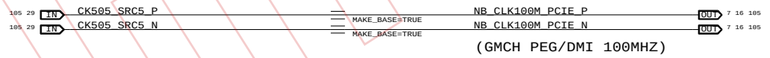
(ICH8M DMI 100MHZ)



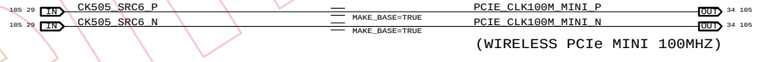
(FW PCIE 100MHZ)



(ICH8M SATA 100MHZ)

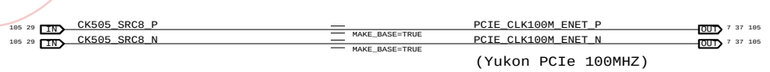


(GMCH PEG/DMI 100MHZ)

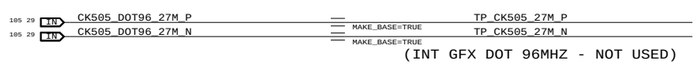


(WIRELESS PCIe MINI 100MHZ)

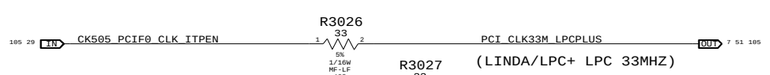
(INT GFX DOT 100MHZ - USED FOR DEBUG)



(Yukon PCIe 100MHZ)

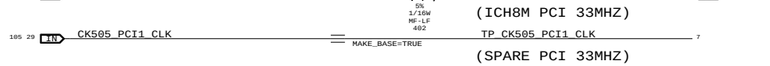


(INT GFX DOT 96MHZ - NOT USED)



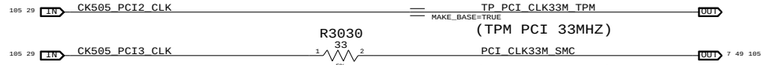
(LINDA/LPC+ LPC 33MHZ)

(ICH8M PCI 33MHZ)



(SPARE PCI 33MHZ)

(TPM PCI 33MHZ)

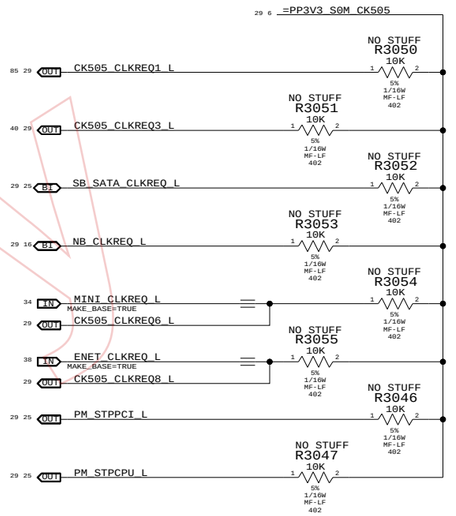


(SMC PCI 33MHZ)

(SPARE PCI 33MHZ)

CLKREQ Controls

Silego SL8GLP537 has internal
PULL-UPS ON ALL CLKREQ# PINS?



Unused Clocks

(Spare 14.318MHZ)

Clock Termination

SYNC_MASTER=JAMES SYNC_DATE=10/18/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 30 OF 118	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

=PP0V9_S3_MEM_A_VREF
C3130 2.2UF 20% 6.3V CERM1 603
C3131 0.1uF 20% 10V CERM 402
=PP1V8_S3_MEM

CRITICAL
J3100
F-RT-SM
DDR2-SODIMM-M72

1	VREF		2	VSS0			
3	VSS1		4	DQ4	MEM_A_DQ<4>	17 102	
5	DQ0	MEM_A_DQ<0>	102 17	6	DQ5	MEM_A_DQ<5>	17 102
7	DQ1	MEM_A_DQ<1>	102 17	8	VSS2		
9	VSS4			10	DM0	MEM_A_DM<0>	17 102
11	DQS0*	MEM_A_DQS_N<0>	102 17 7	12	VSS5		
13	DQS0	MEM_A_DQS_P<0>	102 17 7	14	DQ6	MEM_A_DQ<6>	17 102
15	VSS6			16	DQ7	MEM_A_DQ<7>	7 17 102
17	DQ2	MEM_A_DQ<2>	102 17	18	VSS7		
19	DQ3	MEM_A_DQ<3>	102 17	20	DQ12	MEM_A_DQ<12>	17 102
21	VSS8			22	DQ13	MEM_A_DQ<13>	17 102
23	DQ8	MEM_A_DQ<8>	102 17	24	VSS9		
25	DQ9	MEM_A_DQ<9>	102 17	26	DM1	MEM_A_DM<1>	17 102
27	VSS10			28	VSS11		
29	DQS1*	MEM_A_DQS_N<1>	102 17 7	30	CK0	MEM_CLK_P<0>	16 102
31	DQS1	MEM_A_DQS_P<1>	102 17 7	32	CK0*	MEM_CLK_N<0>	16 102
33	VSS12			34	VSS13		
35	DQ10	MEM_A_DQ<10>	102 17	36	DQ14	MEM_A_DQ<14>	7 17 102
37	DQ11	MEM_A_DQ<11>	102 17	38	DQ15	MEM_A_DQ<15>	17 102
39	VSS14			40	VSS15		
KEY							
41	VSS16			42	VSS17		
43	DQ16	MEM_A_DQ<16>	102 17 7	44	DQ20	MEM_A_DQ<20>	17 102
45	DQ17	MEM_A_DQ<17>	102 17	46	DQ21	MEM_A_DQ<21>	17 102
47	VSS18			48	VSS19		
49	DQS2*	MEM_A_DQS_N<2>	102 17 7	50	NC0	PM_EXTTS_L<0>	16 49
51	DQS2	MEM_A_DQS_P<2>	102 17 7	52	DM2	MEM_A_DM<2>	17 102
53	VSS21			54	VSS22		
55	DQ18	MEM_A_DQ<18>	102 17	56	DQ22	MEM_A_DQ<22>	17 102
57	DQ19	MEM_A_DQ<19>	102 17	58	DQ23	MEM_A_DQ<23>	17 102
59	VSS23			60	VSS24		
61	DQ24	MEM_A_DQ<24>	102 17	62	DQ28	MEM_A_DQ<28>	17 102
63	DQ25	MEM_A_DQ<25>	102 17	64	DQ29	MEM_A_DQ<29>	17 102
65	VSS25			66	VSS26		
67	DM3	MEM_A_DM<3>	102 17	68	DQS3*	MEM_A_DQS_N<3>	7 17 102
69	NC1	NC		70	DQS3	MEM_A_DQS_P<3>	7 17 102
71	VSS27			72	VSS28		
73	DQ26	MEM_A_DQ<26>	102 17	74	DQ30	MEM_A_DQ<30>	17 102
75	DQ27	MEM_A_DQ<27>	102 17	76	DQ31	MEM_A_DQ<31>	17 102
77	VSS29			78	VSS30		
79	CKE0	MEM_CKE<0>	102 33 16	80	NC/CKE1	MEM_CKE<1>	16 33 102
81	VDD0			82	VDD1		
83	NC2	NC		84	NC/A15	TP_MEM_A_A<15>	
85	BA2	MEM_A_BS<2>	102 33 17	86	NC/A14	MEM_A_A<14>	16 33 102
87	VDD2			88	VDD3		
89	A12	MEM_A_A<12>	102 33 17	90	A11	MEM_A_A<11>	17 33 102
91	A9	MEM_A_A<9>	102 33 17	92	A7	MEM_A_A<7>	17 33 102
93	A8	MEM_A_A<8>	102 33 17	94	A6	MEM_A_A<6>	17 33 102
95	VDD4			96	VDD5		
97	A5	MEM_A_A<5>	102 33 17	98	A4	MEM_A_A<4>	17 33 102
99	A3	MEM_A_A<3>	102 33 17	100	A2	MEM_A_A<2>	17 33 102
101	A1	MEM_A_A<1>	102 33 17	102	A0	MEM_A_A<0>	17 33 102
103	VDD6			104	VDD7		
105	A10/AP	MEM_A_A<10>	102 33 17	106	BA1	MEM_A_BS<1>	17 33 102
107	BA0	MEM_A_BS<0>	102 33 17	108	RAS*	MEM_A_RAS_L	17 33 102
109	WE*	MEM_A_WE_L	102 33 17	110	S0*	MEM_CS_L<0>	16 33 102
111	VDD8			112	VDD9		
113	CAS*	MEM_A_CAS_L	102 33 17	114	ODT0	MEM_ODT<0>	16 33 102
115	NC/S1*	MEM_CS_L<1>	102 33 16	116	NC/A13	MEM_A_A<13>	17 33 102
117	VDD10			118	VDD11		
119	NC/ODT1	MEM_ODT<1>	102 33 16	120	NC3	NC	
121	VSS31			122	VSS32		
123	DQ32	MEM_A_DQ<32>	102 17	124	DQ36	MEM_A_DQ<36>	17 102
125	DQ33	MEM_A_DQ<33>	102 17	126	DQ37	MEM_A_DQ<37>	17 102
127	VSS33			128	VSS34		
129	DQS4*	MEM_A_DQS_N<4>	102 17 7	130	DM4	MEM_A_DM<4>	17 102
131	DQS4	MEM_A_DQS_P<4>	102 17 7	132	VSS35		
133	VSS36			134	DQ38	MEM_A_DQ<38>	17 102
135	DQ34	MEM_A_DQ<34>	102 17	136	DQ39	MEM_A_DQ<39>	7 17 102
137	DQ35	MEM_A_DQ<35>	102 17	138	VSS37		
139	VSS38			140	DQ44	MEM_A_DQ<44>	17 102
141	DQ40	MEM_A_DQ<40>	102 17	142	DQ45	MEM_A_DQ<45>	17 102
143	DQ41	MEM_A_DQ<41>	102 17	144	VSS39		
145	VSS40			146	DQS5*	MEM_A_DQS_N<5>	7 17 102
147	DM5	MEM_A_DM<5>	102 17	148	DQS5	MEM_A_DQS_P<5>	7 17 102
149	VSS41			150	VSS42		
151	DQ42	MEM_A_DQ<42>	102 17	152	DQ46	MEM_A_DQ<46>	17 102
153	DQ43	MEM_A_DQ<43>	102 17	154	DQ47	MEM_A_DQ<47>	7 17 102
155	VSS43			156	VSS44		
157	DQ48	MEM_A_DQ<48>	102 17	158	DQ52	MEM_A_DQ<52>	17 102
159	DQ49	MEM_A_DQ<49>	102 17	160	DQ53	MEM_A_DQ<53>	17 102
161	VSS45			162	VSS46		
163	NC_TEST	NC		164	CK1	MEM_CLK_P<1>	16 102
165	VSS47			166	CK1*	MEM_CLK_N<1>	16 102
167	DQS6*	MEM_A_DQS_N<6>	102 17 7	168	VSS48		
169	DQS6	MEM_A_DQS_P<6>	102 17 7	170	DM6	MEM_A_DM<6>	17 102
171	VSS49			172	VSS50		
173	DQ50	MEM_A_DQ<50>	102 17	174	DQ54	MEM_A_DQ<54>	7 17 102
175	DQ51	MEM_A_DQ<51>	102 17	176	DQ55	MEM_A_DQ<55>	17 102
177	VSS51			178	VSS52		
179	DQ56	MEM_A_DQ<56>	102 17	180	DQ60	MEM_A_DQ<60>	17 102
181	DQ57	MEM_A_DQ<57>	102 17	182	DQ61	MEM_A_DQ<61>	17 102
183	VSS53			184	VSS54		
185	DM7	MEM_A_DM<7>	102 17	186	DQS7*	MEM_A_DQS_N<7>	7 17 102
187	VSS55			188	DQS7	MEM_A_DQS_P<7>	7 17 102
189	DQ58	MEM_A_DQ<58>	102 17	190	VSS56		
191	DQ59	MEM_A_DQ<59>	102 17	192	DQ62	MEM_A_DQ<62>	17 102
193	VSS57			194	DQ63	MEM_A_DQ<63>	17 102
195	SDA	=I2C_DIMMA_SDA	52	196	VSS58		
197	SCL	=I2C_DIMMA_SCL	52	198	SA0	MEM_A_SA<0>	
199	VDDSPD			200	SA1	MEM_A_SA<1>	

ADDR=0xA0(WR)/0xA1(RD)
R3140 10K 1/16W 5% MF-LF 402
R3141 10K 1/16W 5% MF-LF 402

GND
201 202 203 204 205
516S0565

=PPSPD_S0_MEM
C3140 2.2UF 20% 6.3V CERM1 603
C3141 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM
R3100 1K 1% 1/16W MF-LF 402
PP0V9_S3_MEM_A_VREF
VOLTAGE=0.9V TRUE
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM
R3101 1K 1% 1/16W MF-LF 402
=PP0V9_S3_MEM_A_VREF

DDR2 Bypass Caps
(For return current)

=PP1V8_S3_MEM
C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 1UF 10% 6.3V CERM 402
C3111 1UF 10% 6.3V CERM 402
C3112 1UF 10% 6.3V CERM 402
C3113 1UF 10% 6.3V CERM 402
C3114 1UF 10% 6.3V CERM 402
C3115 1UF 10% 6.3V CERM 402
C3116 1UF 10% 6.3V CERM 402
C3117 1UF 10% 6.3V CERM 402
C3118 1UF 10% 6.3V CERM 402
C3119 1UF 10% 6.3V CERM 402
C3120 1UF 10% 6.3V CERM 402
C3121 1UF 10% 6.3V CERM 402
C3122 1UF 10% 6.3V CERM 402
C3123 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=JAMES SYNC_DATE=10/17/06

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 31 OF 118	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

=PP0V9_S3_MEM_B_VREF
C3230 2.2UF 20% 6.3V CERM1 603
C3231 0.1uF 20% 10V CERM 402
=PP1V8_S3_MEM

CRITICAL
J3200
F-RT-SM
DDR2-SODIMM-M72

1	VREF		2	VSS0			
3	VSS1		4	DQ4	MEM_B_DQ<4>	17 102	
5	DQ0	MEM_B_DQ<0> 102 17	6	DQ5	MEM_B_DQ<5>	17 102	
7	DQ1	MEM_B_DQ<1> 102 17	8	VSS2			
9	VSS4		10	DM0	MEM_B_DM<0>	17 102	
11	DQS0*	MEM_B_DQS_N<0> 102 17 7	12	VSS5			
13	DQS0	MEM_B_DQS_P<0> 102 17 7	14	DQ6	MEM_B_DQ<6>	7 17 102	
15	VSS6		16	DQ7	MEM_B_DQ<7>	17 102	
17	DQ2	MEM_B_DQ<2> 102 17	18	VSS7			
19	DQ3	MEM_B_DQ<3> 102 17	20	DQ12	MEM_B_DQ<12>	17 102	
21	VSS8		22	DQ13	MEM_B_DQ<13>	17 102	
23	DQ8	MEM_B_DQ<8> 102 17 7	24	VSS9			
25	DQ9	MEM_B_DQ<9> 102 17 7	26	DM1	MEM_B_DM<1>	17 102	
27	VSS10		28	VSS11			
29	DQS1*	MEM_B_DQS_N<1> 102 17 7	30	CK0	MEM_CLK_P<3>	16 102	
31	DQS1	MEM_B_DQS_P<1> 102 17 7	32	CK0*	MEM_CLK_N<3>	16 102	
33	VSS12		34	VSS13			
35	DQ10	MEM_B_DQ<10> 102 17	36	DQ14	MEM_B_DQ<14>	17 102	
37	DQ11	MEM_B_DQ<11> 102 17	38	DQ15	MEM_B_DQ<15>	17 102	
39	VSS14		40	VSS15			
KEY							
41	VSS16		42	VSS17			
43	DQ16	MEM_B_DQ<16> 102 17	44	DQ20	MEM_B_DQ<20>	17 102	
45	DQ17	MEM_B_DQ<17> 102 17	46	DQ21	MEM_B_DQ<21>	17 102	
47	VSS18		48	VSS19			
49	DQS2*	MEM_B_DQS_N<2> 102 17 7	50	NC0	PM_EXTTS_L<1>	16 49	
51	DQS2	MEM_B_DQS_P<2> 102 17 7	52	DM2	MEM_B_DM<2>	17 102	
53	VSS21		54	VSS22			
55	DQ18	MEM_B_DQ<18> 102 17	56	DQ22	MEM_B_DQ<22>	17 102	
57	DQ19	MEM_B_DQ<19> 102 17	58	DQ23	MEM_B_DQ<23>	7 17 102	
59	VSS23		60	VSS24			
61	DQ24	MEM_B_DQ<24> 102 17	62	DQ28	MEM_B_DQ<28>	17 102	
63	DQ25	MEM_B_DQ<25> 102 17 7	64	DQ29	MEM_B_DQ<29>	17 102	
65	VSS25		66	VSS26			
67	DM3	MEM_B_DM<3> 102 17	68	DQS3*	MEM_B_DQS_N<3>	7 17 102	
69	NC1	NC	70	DQS3	MEM_B_DQS_P<3>	7 17 102	
71	VSS27		72	VSS28			
73	DQ26	MEM_B_DQ<26> 102 17	74	DQ30	MEM_B_DQ<30>	17 102	
75	DQ27	MEM_B_DQ<27> 102 17	76	DQ31	MEM_B_DQ<31>	17 102	
77	VSS29		78	VSS30			
79	CKE0	MEM_CKE<3> 102 33 16	80	NC/CKE1	MEM_CKE<4>	16 33 102	
81	VDD0		82	VDD1			
83	NC2	NC	84	NC/A15	TP_MEM_B_A<15>		
85	BA2	MEM_B_BS<2> 102 33 17	86	NC/A14	MEM_B_A<14>	16 33 102	
87	VDD2		88	VDD3			
89	A12	MEM_B_A<12> 102 33 17	90	A11	MEM_B_A<11>	17 33 102	
91	A9	MEM_B_A<9> 102 33 17	92	A7	MEM_B_A<7>	17 33 102	
93	A8	MEM_B_A<8> 102 33 17	94	A6	MEM_B_A<6>	17 33 102	
95	VDD4		96	VDD5			
97	A5	MEM_B_A<5> 102 33 17	98	A4	MEM_B_A<4>	17 33 102	
99	A3	MEM_B_A<3> 102 33 17	100	A2	MEM_B_A<2>	17 33 102	
101	A1	MEM_B_A<1> 102 33 17	102	A0	MEM_B_A<0>	17 33 102	
103	VDD6		104	VDD7			
105	A10/AP	MEM_B_A<10> 102 33 17	106	BA1	MEM_B_BS<1>	17 33 102	
107	BA0	MEM_B_BS<0> 102 33 17	108	RAS*	MEM_B_RAS_L	17 33 102	
109	WE*	MEM_B_WE_L 102 33 17	110	S0*	MEM_CS_L<2>	16 33 102	
111	VDD8		112	VDD9			
113	CAS*	MEM_B_CAS_L 102 33 17	114	ODT0	MEM_ODT<2>	16 33 102	
115	NC/S1*	MEM_CS_L<3> 102 33 16	116	NC/A13	MEM_B_A<13>	17 33 102	
117	VDD10		118	VDD11			
119	NC/ODT1	MEM_ODT<3> 102 33 16	120	NC3	NC		
121	VSS31		122	VSS32			
123	DQ32	MEM_B_DQ<32> 102 17	124	DQ36	MEM_B_DQ<36>	17 102	
125	DQ33	MEM_B_DQ<33> 102 17	126	DQ37	MEM_B_DQ<37>	17 102	
127	VSS33		128	VSS34			
129	DQS4*	MEM_B_DQS_N<4> 102 17 7	130	DM4	MEM_B_DM<4>	17 102	
131	DQS4	MEM_B_DQS_P<4> 102 17 7	132	VSS35			
133	VSS36		134	DQ38	MEM_B_DQ<38>	7 17 102	
135	DQ34	MEM_B_DQ<34> 102 17	136	DQ39	MEM_B_DQ<39>	17 102	
137	DQ35	MEM_B_DQ<35> 102 17	138	VSS37			
139	VSS38		140	DQ44	MEM_B_DQ<44>	7 17 102	
141	DQ40	MEM_B_DQ<40> 102 17	142	DQ45	MEM_B_DQ<45>	17 102	
143	DQ41	MEM_B_DQ<41> 102 17	144	VSS39			
145	VSS40		146	DQS5*	MEM_B_DQS_N<5>	7 17 102	
147	DM5	MEM_B_DM<5> 102 17	148	DQS5	MEM_B_DQS_P<5>	7 17 102	
149	VSS41		150	VSS42			
151	DQ42	MEM_B_DQ<42> 102 17	152	DQ46	MEM_B_DQ<46>	17 102	
153	DQ43	MEM_B_DQ<43> 102 17	154	DQ47	MEM_B_DQ<47>	17 102	
155	VSS43		156	VSS44			
157	DQ48	MEM_B_DQ<48> 102 17 7	158	DQ52	MEM_B_DQ<52>	17 102	
159	DQ49	MEM_B_DQ<49> 102 17	160	DQ53	MEM_B_DQ<53>	17 102	
161	VSS45		162	VSS46			
163	NC_TEST	NC	164	CK1	MEM_CLK_P<4>	16 102	
165	VSS47		166	CK1*	MEM_CLK_N<4>	16 102	
167	DQS6*	MEM_B_DQS_N<6> 102 17 7	168	VSS48			
169	DQS6	MEM_B_DQS_P<6> 102 17 7	170	DM6	MEM_B_DM<6>	17 102	
171	VSS49		172	VSS50			
173	DQ50	MEM_B_DQ<50> 102 17	174	DQ54	MEM_B_DQ<54>	17 102	
175	DQ51	MEM_B_DQ<51> 102 17	176	DQ55	MEM_B_DQ<55>	17 102	
177	VSS51		178	VSS52			
179	DQ56	MEM_B_DQ<56> 102 17	180	DQ60	MEM_B_DQ<60>	17 102	
181	DQ57	MEM_B_DQ<57> 102 17	182	DQ61	MEM_B_DQ<61>	17 102	
183	VSS53		184	VSS54			
185	DM7	MEM_B_DM<7> 102 17	186	DQS7*	MEM_B_DQS_N<7>	7 17 102	
187	VSS55		188	DQS7	MEM_B_DQS_P<7>	7 17 102	
189	DQ58	MEM_B_DQ<58> 102 17	190	VSS56			
191	DQ59	MEM_B_DQ<59> 102 17	192	DQ62	MEM_B_DQ<62>	7 17 102	
193	VSS57		194	DQ63	MEM_B_DQ<63>	17 102	
195	SDA	=I2C_DIMMB_SDA 52	196	VSS58			
197	SCL	=I2C_DIMMB_SCL 52	198	SA0	MEM_B_SA<0>		
199	VDDSPD		200	SA1	MEM_B_SA<1>		
201	GND						
202	GND						
203	GND						
204	GND						
205	GND						

516S0565

R3240 10K 1/16W 5% MF-LF 402
ADDR=0XA4(WR)/0XA5(RD)

=PPSPD_S0_MEM
C3240 2.2UF 20% 6.3V CERM1 603
C3241 0.1uF 20% 10V CERM 402

=PPSPD_S0_MEM
R3241 10K 5% 1/16W MF-LF 402

=PP1V8_S3_MEM
R3200 1K 1% 1/16W MF-LF 402
PP0V9_S3_MEM_B_VREF VOLTAGE=0.9V TRUE MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.25MM =PP0V9_S3_MEM_B_VREF
R3201 1K 1% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM
C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 1UF 10% 6.3V CERM 402
C3211 1UF 10% 6.3V CERM 402
C3212 1UF 10% 6.3V CERM 402
C3213 1UF 10% 6.3V CERM 402
C3214 1UF 10% 6.3V CERM 402
C3215 1UF 10% 6.3V CERM 402
C3216 1UF 10% 6.3V CERM 402
C3217 1UF 10% 6.3V CERM 402
C3218 1UF 10% 6.3V CERM 402
C3219 1UF 10% 6.3V CERM 402
C3220 1UF 10% 6.3V CERM 402
C3221 1UF 10% 6.3V CERM 402
C3222 1UF 10% 6.3V CERM 402
C3223 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=JAMES SYNC_DATE=10/17/06

APPLE COMPUTER INC.

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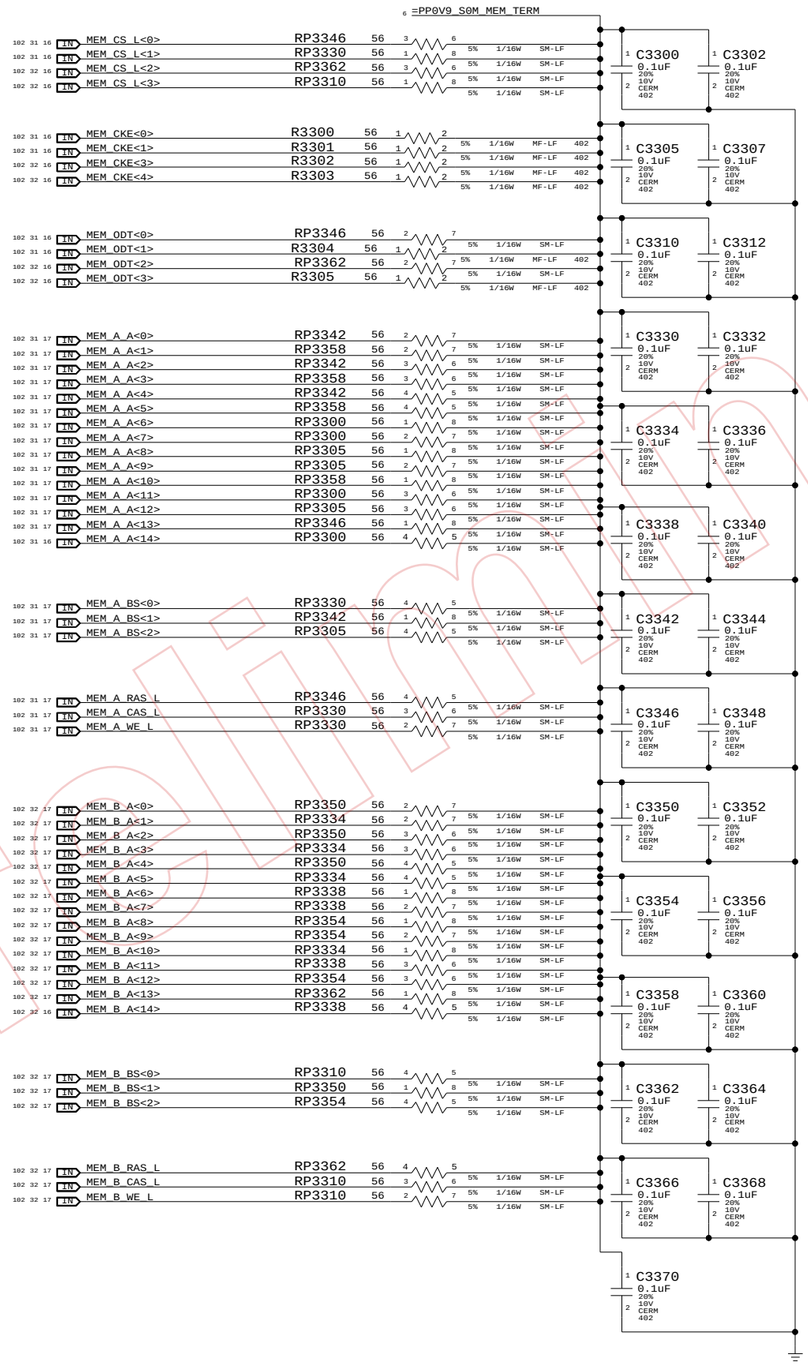
SCALE: NONE	SHT 32 OF 118	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=JAMES SYNC_DATE=12/04/2006

APPLE COMPUTER INC.

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D	051-7229	33

SCALE NONE SHT 33 OF 118

	3.3V_S3_CURRENT	D0-D2_D3HOT	D3COLD
	MAX CONT.	1100MA	250mA
	MAX PEAK	2750MA	2750MA
	1.5V_CURRENT		
	MAX CONT.	375MA	N/A
	MAX PEAK	560MA	N/A

NOTE: CURRENT DATA PER 5/16/2005 PCIE MINI CEM ECN

NO STUFF
R3400
0
5%
1/16W
MF-LF
402

NO STUFF
R3401
0
5%
1/16W
MF-LF
402

CRITICAL
J3400
ASOB226-S80N-7F
F-RT-SM

37 25 OUT PCIE_WAKE_L
RSVD_MINI_WLAN_ACTIVE
RSVD_MINI_BT_ACTIVE
30 OUT MINI_CLKREQ_L
105 30 IN PCIE_CLK100M_MINI_N
105 30 IN PCIE_CLK100M_MINI_P
RESERVED
RESERVED
MINI_RESET_L IN 28
=SMBUS_MINI_SCL IN 52
=SMBUS_MINI_SDA BI 52
USB_MINI_N BI 24 103
USB_MINI_P BI 24 103
PP1V05_S0
=PP3V3_S3_MINI 6
=PP1V5_S0_MINI 6

NC pins: 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603
C3400 0.1uF 20% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

104 24 7 OUT PCIE_MINI_D2R_N
104 24 7 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=Place close to U2300.
C3431
0.1uF
104 24 IN PCIE_MINI_R2D_C_N
10%
16V
X5R
402

PLACEMENT_NOTE=Place close to U2300.
C3430
0.1uF
104 24 IN PCIE_MINI_R2D_C_P
10%
16V
X5R
402

104 PCIE_MINI_R2D_N
104 PCIE_MINI_R2D_P

516S0391

STANDOFF FOR J3400

SDF3400
STDOFF-4OD5.6H-1.35-TH
SDF3400_1
860-0691

R3410
0
5%
1/16W
MF-LF
402

25 CLINK_WLAN_CLK — TP_CLINK_WLAN_CLK MAKE_BASE=TRUE
25 CLINK_WLAN_DATA — TP_CLINK_WLAN_DATA MAKE_BASE=TRUE
25 CLINK_WLAN_RESET_L — TP_CLINK_WLAN_RESET_L MAKE_BASE=TRUE

PCI-E MiniCard Connector

SYNC_MASTER=DOUG SYNC_DATE=10/30/2006

APPLE COMPUTER INC.

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Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V9R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

31 =PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

NOSTUFF C3700 4.7UF 20% 6.3V CERM 603
C3701 0.1UF 10% 16V X5R 402
C3702 0.1UF 10% 16V X5R 402
C3703 0.1UF 10% 16V X5R 402
C3704 0.1UF 10% 16V X5R 402
C3705 0.1UF 10% 16V X5R 402
C3706 0.1UF 10% 16V X5R 402
C3707 0.1UF 10% 16V X5R 402
C3708 0.1UF 10% 16V X5R 402

31 =PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603
C3711 0.1UF 10% 16V X5R 402
C3712 0.1UF 10% 16V X5R 402
C3713 0.1UF 10% 16V X5R 402
C3714 0.1UF 10% 16V X5R 402
C3715 0.1UF 10% 16V X5R 402

31 =PP1V9R2V5_ENET_PHY
R3720 0 5% 1/10W MF-LF 402
32 PP1V9R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603
C3721 0.1UF 10% 16V X5R 402
C3722 0.1UF 10% 16V X5R 402
C3723 0.1UF 10% 16V X5R 402
C3724 0.1UF 10% 16V X5R 402

31 =YUKON_EC_PP2V5_ENET

66 19 3 OUT PCIE_ENET_D2R_P
66 19 3 OUT PCIE_ENET_D2R_N
66 19 IN PCIE_ENET_R2D_C_P
66 19 IN PCIE_ENET_R2D_C_N
67 25 3 IN PCIE_CLK100M_ENET_P
67 25 3 IN PCIE_CLK100M_ENET_N
31 OUT =ENET_CLKREQ_L
29 20 OUT PCIE_WAKE_L
23 3 IN ENET_RESET_L
66 32 BI ENET_MDI_P<0>
66 32 BI ENET_MDI_N<0>
66 32 BI ENET_MDI_P<1>
66 32 BI ENET_MDI_N<1>
66 32 BI ENET_MDI_P<2>
66 32 BI ENET_MDI_N<2>
66 32 BI ENET_MDI_P<3>
66 32 BI ENET_MDI_N<3>

C3735 0.1UF 10% 16V X5R 402
C3736 0.1UF 10% 16V X5R 402
C3730 0.1UF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3730 close to southbridge.
C3731 0.1UF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3731 close to southbridge.

Yukon EC: Pin 42 should be NC (or TP) net.

R3740 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R3741 49.9 1% 1/16W MF-LF 402
R3742 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R3743 49.9 1% 1/16W MF-LF 402
R3744 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R3745 49.9 1% 1/16W MF-LF 402
R3746 49.9 1% 1/16W MF-LF 402 ENET_MDI3
R3747 49.9 1% 1/16W MF-LF 402

C3740 0.001UF 10% 50V CERM 402
C3742 0.001UF 10% 50V CERM 402
C3744 0.001UF 10% 50V CERM 402
C3746 0.001UF 10% 50V CERM 402

CRITICAL Y3750 25.0000M SM-3-LF 197S0167 CL = 20PF
C3750 27PF 5% 50V CERM 402
C3751 27PF 5% 50V CERM 402
ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN CRITICAL OMIT

NC_32	32		
NC_51	51		
NC_52	52		
NC_57	57		
NC_64	64		
AVDD0	19	EC:AVDD 2.5V	
AVDD1	22		
AVDD2	23		
AVDD3	20		
VDDO_TTL0	1		
VDDO_TTL1	40		
VDDO_TTL2	45		
VDDO_TTL3	61		
AVDDH	8		
VDD0	2		
VDD1	7		
VDD2	13		
VDD3	33		
VDD4	39		
VDD5	44		
VDD6	49		
VDD7	59		
TX_P	49	66 PCIE_ENET_D2R_C_P	
TX_N	50	66 PCIE_ENET_D2R_C_N	
RX_P	54	66 3 PCIE_ENET_R2D_P	
RX_N	53	66 3 PCIE_ENET_R2D_N	
REFCLKP	55		
REFCLKN	56		
CLKREQ*	42	EC:NO CONNECT	
WAKE*	6		
PERST*	5		
MDIP0	17		
MDIN0	18		
MDIP1	20		
MDIN1	21		
MDIP2	26		
MDIN2	27		
MDIP3	30		
MDIN3	31		
XTALI	15		
XTALO	14		
THRML_PAD	65		

PCI EXPRESS
MEDIA
MAIN CLK

ANALOG
EC:CTRL25
CTRL18 4 TP_YUKON_CTRL18 OUT 31
CTRL12 3 TP_YUKON_CTRL12 OUT 31
RSET 16 YUKON_RSET
R3760 4.7K 5% 1/16W MF-LF 402
LOM_DISABLE* 10 ENET_LOM_DIS_L
VAUX_AVLBL 12
SWITCH_VAUX 9 NC
VMAIN_AVLBL 47 Must be high in S0 state (can use PP3V3_S0 as input) =ENET_VMAIN_AVLBL IN 31
SWITCH_VCC 11 NC
YUKON_ULTRA R3765 4.99K 1% 1/16W MF-LF 402

LED
LED_ACT* 59 ENET_LED_ACT_L 32
LED_LINK10/100* 60 ENET_LED_LINK10_100_L 32
LED_LINK1000* 62 ENET_LED_LINK1000_L 32
LED_DUPLEX* 63 ENET_LED_LINK_L 32

SPI
(IPU) SPI_DO 34 NC
(IPU) SPI_DI 35 NC
(IPU) SPI_CLK 37 NC
(IPU) SPI_CS 36 NC

TWSI
(IPU) VPD_CLK 38 YUKON_VPD_CLK
(IPU) VPD_DATA 41 YUKON_VPD_DATA

TEST/RSVD
(IPD) TESTMODE 46
RSVD_24 24 NC
RSVD_25 25 NC
RSVD_29 29 NC
RSVD_43 43 NC

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/16W MF-LF 402
R3781 4.7K 5% 1/16W MF-LF 402
E2 NC1 NC0 WC* VCC SDA SCL VSS
U3780 M24C08 SO8 OMIT CRITICAL

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:
- ALIAS =YUKON_EC_PP2V5_ENET TO PP1V9R2V5_ENET_PHY_AVDD, ADD 1X 0.1UF AND 1X 0.001UF CAPS
- USE 0-OHM RESISTORS OR VARIABLE SUPPLY TO PROVIDE 1.8V OR 2.5V TO =PP1V9R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=DOUG SYNC_DATE=11/08/2006

APPLE COMPUTER INC.

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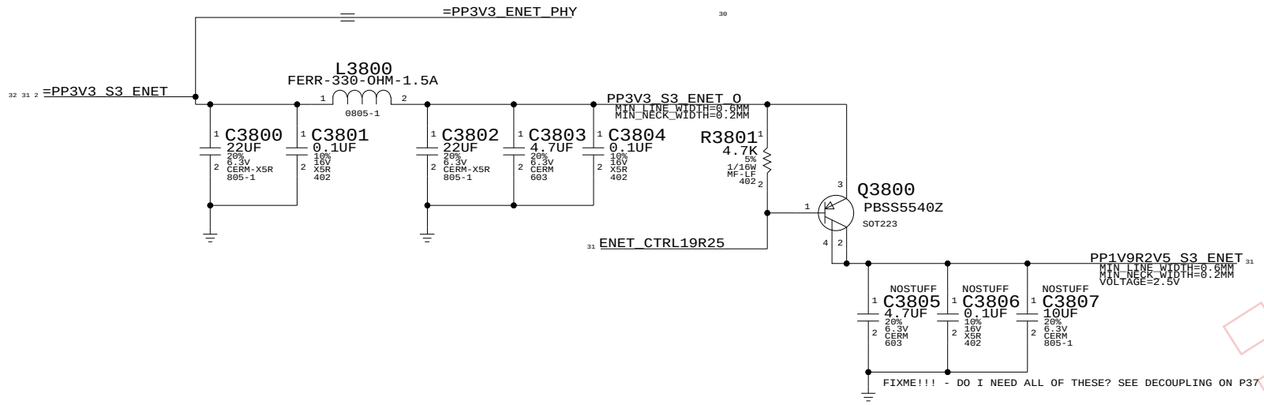
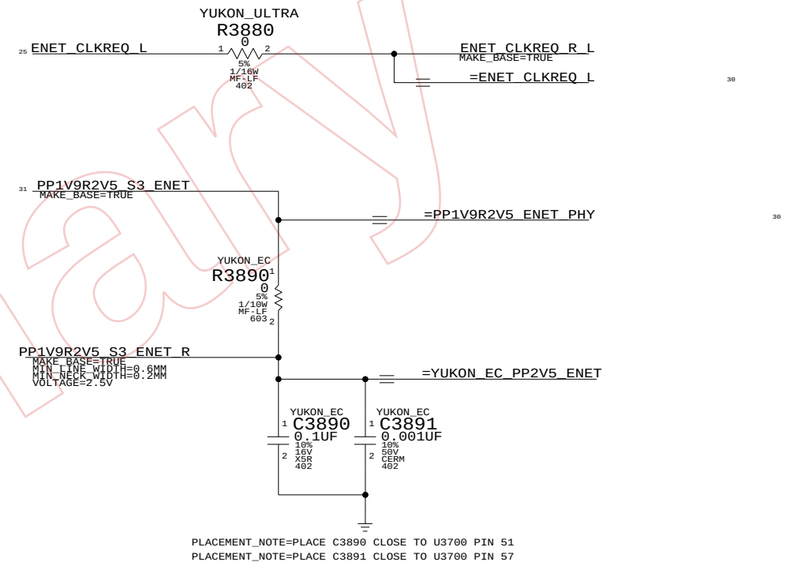
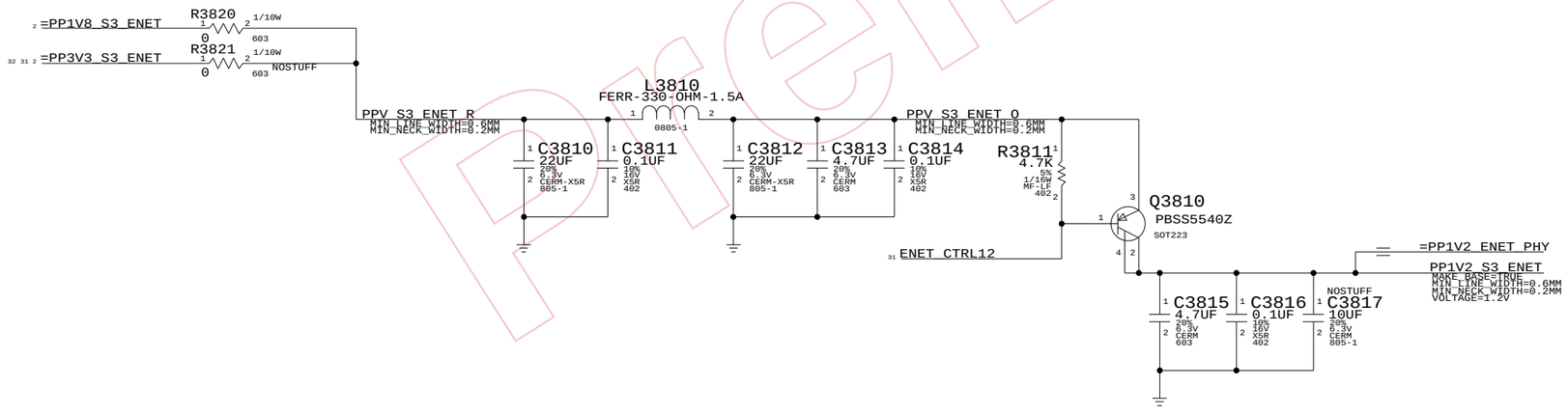
YUKON 1.9/2.5 RAIL SUPPLY



YUKON EC / YUKON ULTRA SUPPORT



YUKON 1.2 RAIL SUPPLY



YUKON T9 ALIASES

TP_YUKON_CTRL18	=	ENET_CTRL19R25 (MAKE_BASE=TRUE)
TP_YUKON_CTRL12	=	ENET_CTRL12 (MAKE_BASE=TRUE)
=ENET_VMAIN_AVLBL	=	=PP3V3_S0_ENET

YUKON/ULTRA SUPPORT

SYNC_MASTER=DOUG SYNC_DATE=(10/02/2006)

APPLE COMPUTER INC.

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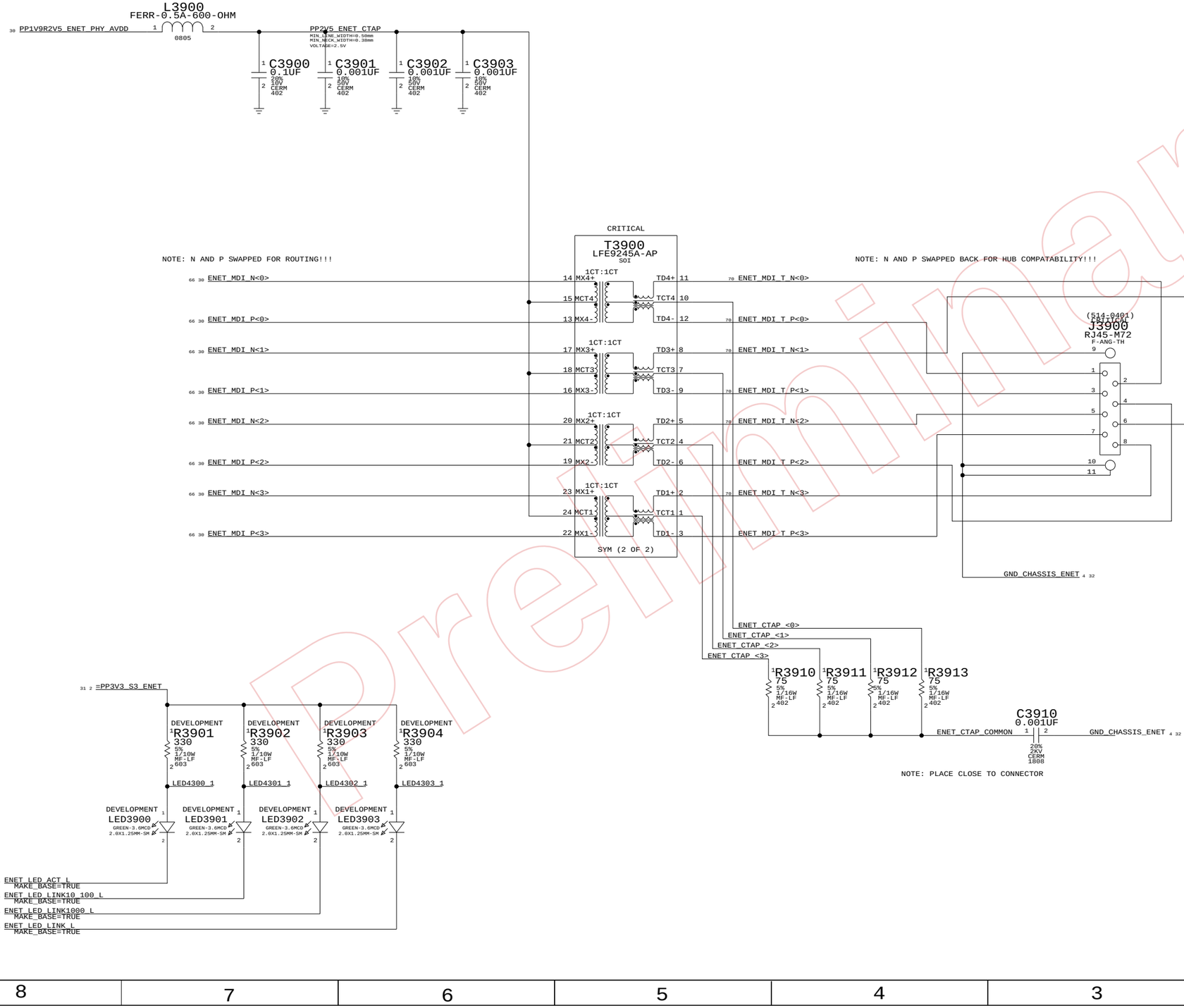
D	051-7229	33

SCALE	SHT	OF
NONE	38	118



ETHERNET CONNECTOR

SYNC_MASTER=DOUG SYNC_DATE=11/06/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE

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FW: 1394B CONTROLLER

SYNC_MASTER=M78_MLB SYNC_DATE=12/15/2006

APPLE COMPUTER INC.

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SCALE: NONE SHT 40 OF 118

FW643 1.0V GENERATION

FIXME!!!: JITTER TOLERANCE WILL DETERMINE NEED FOR FERRITE

L4200
120-OHM-0.3A-EMI
0402-LF

PP1V0_S5_FW_AVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.0V
25MA PCIE SERDES

FIXME!!!: CHOOSE FOR POWER DISSIPATION, DC GAIN, AND LOW VCE SAT

Q4200
BCP69
SOT223-4

=PP3V3_S5_FW

C4200 2.2UF 20% 6.3V CERM 402-LF
C4201 2.2UF 20% 6.3V CERM 402-LF

PP1V0_S5_FW_DVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.0V
110MA DIGITAL CORE

C4210 0.1UF 20% 10V CERM 402
C4211 0.1UF 20% 10V CERM 402
C4212 10UF 20% 6.3V CERM 805-1
C4213 10UF 20% 6.3V CERM 805-1

NOTE: MULTIPLE VIAS TO GND
NOTE: Q4200 COLLECTOR CONNECT TO CAPS WITH 0.4 SQ-IN HEAT SINK

FW_OCR10_CTL — R4200 75 5% 1/10W MF-LF 402 — FW_OCR10_CTL_R

FIXME!!!: WATTAGE AND TOLERANCE NEEDED?

1394 PHY DATA/STROBE OPTIONS

=PP3V3_S5_FW

NOSTUFF
R4250 10K 5% 1/16W MF-LF 402
R4251 10K 5% 1/16W MF-LF 402
R4252 10K 5% 1/16W MF-LF 402

FW_PHY_DS0
FW_PHY_DS1
FW_PHY_DS2

FIXME!!!: MODE FOR UNUSED PORTS?
FIXME!!!: RECOMMENDED PULLME STRENGTHS?

NOSTUFF NOSTUFF
R4260 10K 5% 1/16W MF-LF 402
R4261 10K 5% 1/16W MF-LF 402
R4262 10K 5% 1/16W MF-LF 402

FW643 DECOUPLING

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4000

=PP3V3_S5_FW
7MA I/O

C4250 1UF 10% 6.3V CERM 402
C4251 1UF 10% 6.3V CERM 402
C4252 1UF 10% 6.3V CERM 402
C4253 1UF 10% 6.3V CERM 402
C4254 1UF 10% 6.3V CERM 402

=PP3V3_S5_FW
0MA VREG PWR

C4290 0.1UF 10% 16V X5R-CERM 402
C4291 1UF 10% 6.3V CERM 402

NOTE: PLACE THESE NEAR U4000 PIN K12

PP1V0_S5_FW_DVDD

C4260 1UF 10% 6.3V CERM 402
C4261 1UF 10% 6.3V CERM 402
C4262 1UF 10% 6.3V CERM 402
C4263 1UF 10% 6.3V CERM 402
C4264 1UF 10% 6.3V CERM 402
C4265 1UF 10% 6.3V CERM 402
C4266 1UF 10% 6.3V CERM 402

PP3V3_S5_FW_AVDD1

C4240 1UF 10% 6.3V CERM 402
C4241 1UF 10% 6.3V CERM 402
C4242 1UF 10% 6.3V CERM 402

PP3V3_S5_FW_AVDD2

C4280 1UF 10% 6.3V CERM 402
C4281 1UF 10% 6.3V CERM 402

PP1V0_S5_FW_AVDD

C4230 1UF 10% 6.3V CERM 402
C4231 1UF 10% 6.3V CERM 402

FW 3.3V FILTERING

=PP3V3_S5_FW

L4210
120-OHM-0.3A-EMI
0402-LF

PP3V3_S5_FW_AVDD1
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
114MA FIREWIRE PHY

L4211
120-OHM-0.3A-EMI
0402-LF

PP3V3_S5_FW_AVDD2
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
17MA PCIE SERDES

FW PCIE ALIASES

TP_PCIE_FW_R2D_C_N = PCIE_FW_R2D_C_N (MAKE_BASE=TRUE)
TP_PCIE_FW_R2D_C_P = PCIE_FW_R2D_C_P (MAKE_BASE=TRUE)
PCIE_FW_D2R_N = TP_PCIE_FW_D2R_N (MAKE_BASE=TRUE)
PCIE_FW_D2R_P = TP_PCIE_FW_D2R_P (MAKE_BASE=TRUE)

FW: 1394B MISC

SYNC_MASTER=DOUG
SYNC_DATE=10/10/2006

APPLE COMPUTER INC.

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D	051-7229	33

SCALE: NONE

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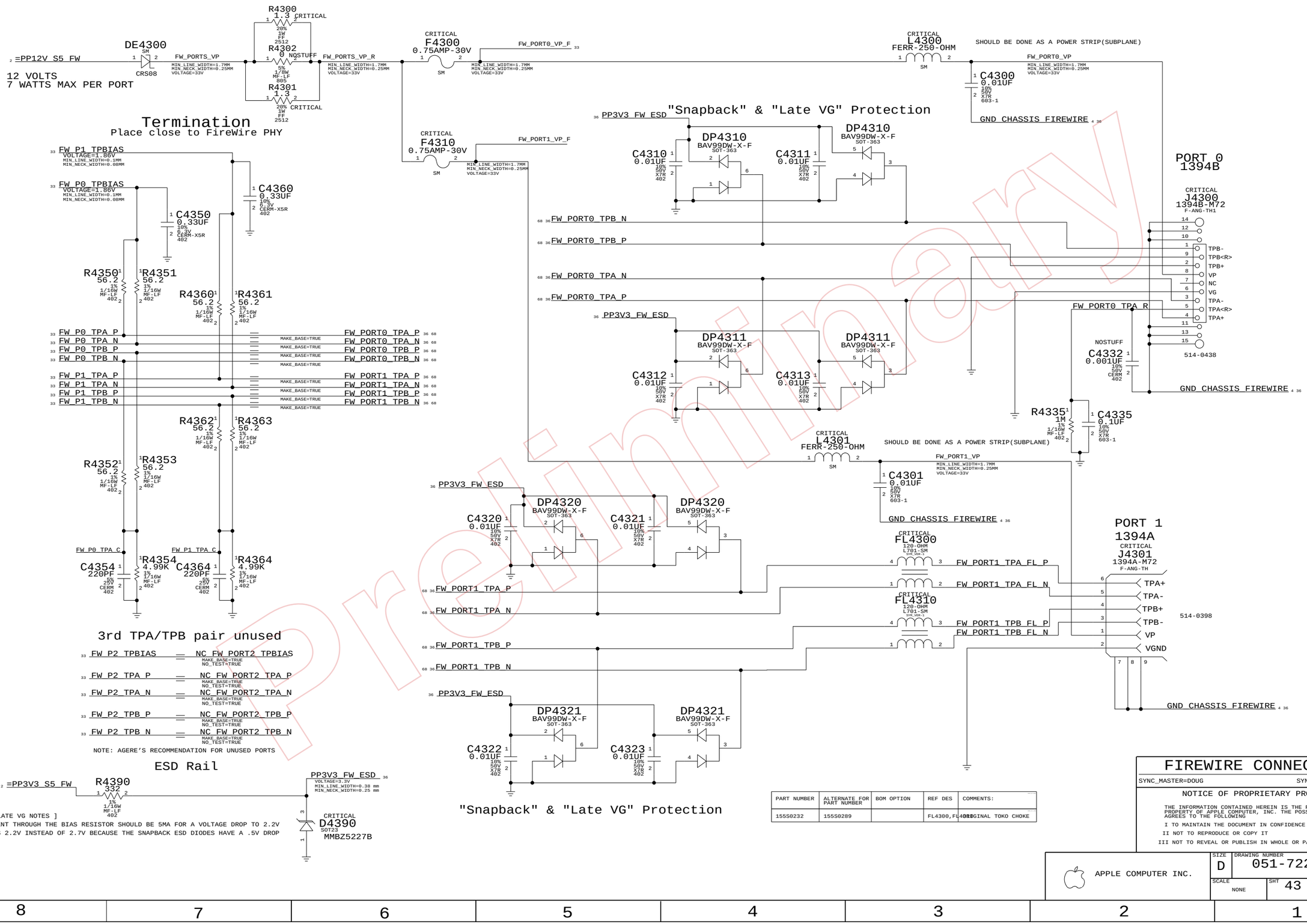

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4300,FL4310	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

SYNC_MASTER=DOUG SYNC_DATE=10/10/2006

APPLE COMPUTER INC.

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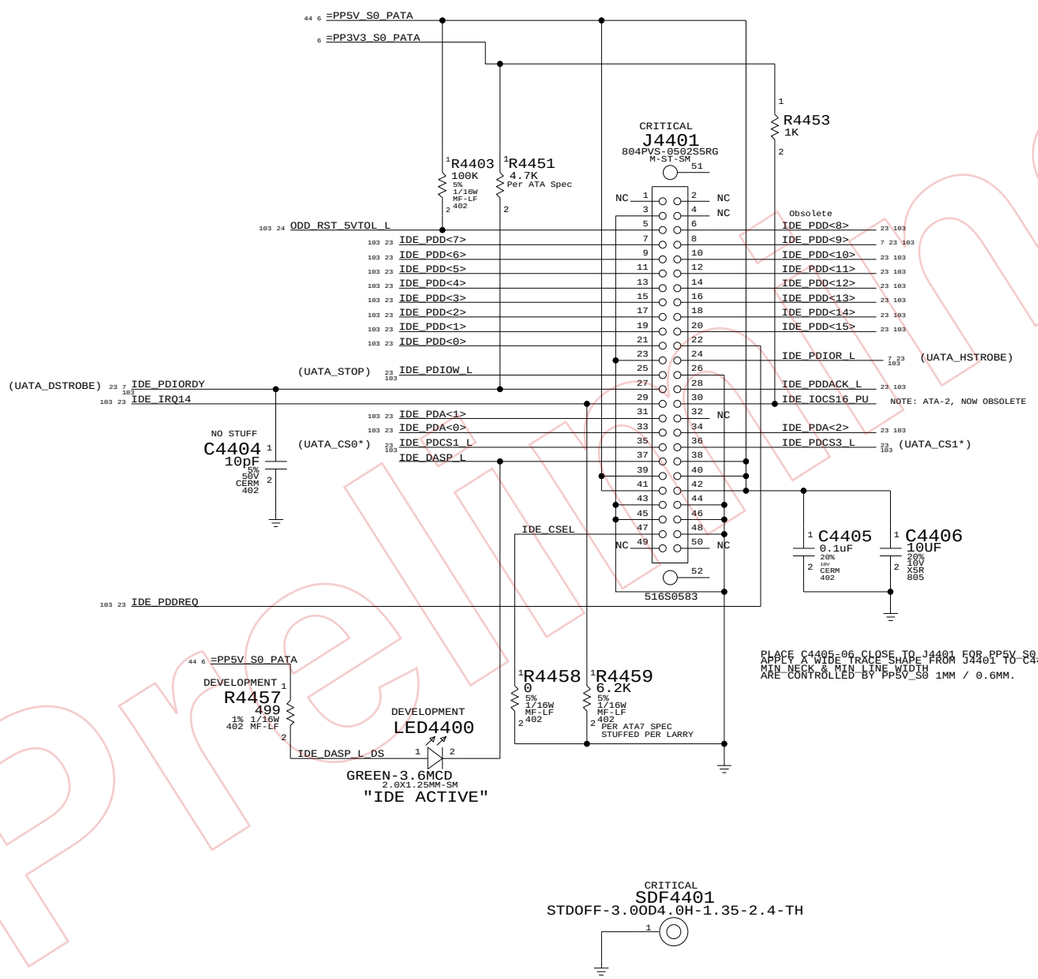
SCALE: NONE	SHT 43 OF 118	

CRITICAL
SDF4400
STDOFF-3.0OD4.0H-1.35-2.4-TH

IDE (ODD) Connector



CRITICAL
SDF4401
STDOFF-3.0OD4.0H-1.35-2.4-TH

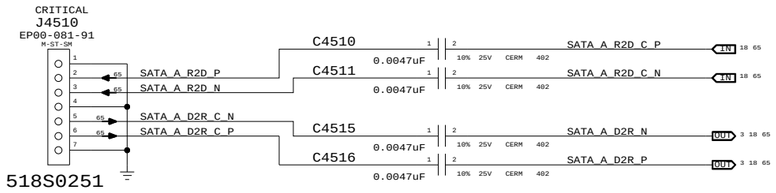
PATA Connector

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

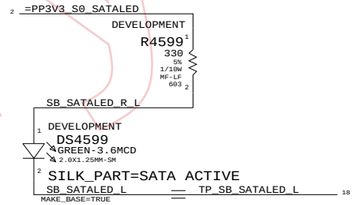
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 44 OF 118	

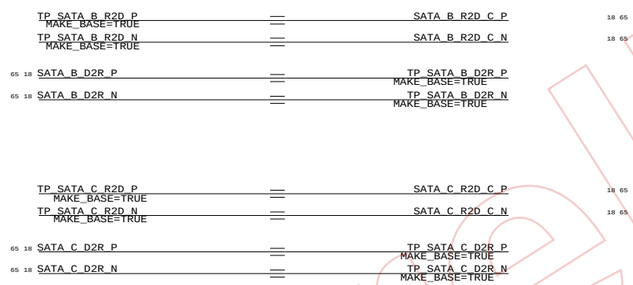
SATA Port A



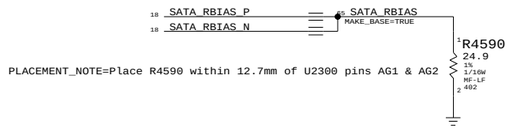
SATA Activity LED



UNUSED SATA PORTS



ICH SATA Support



SATA Connectors

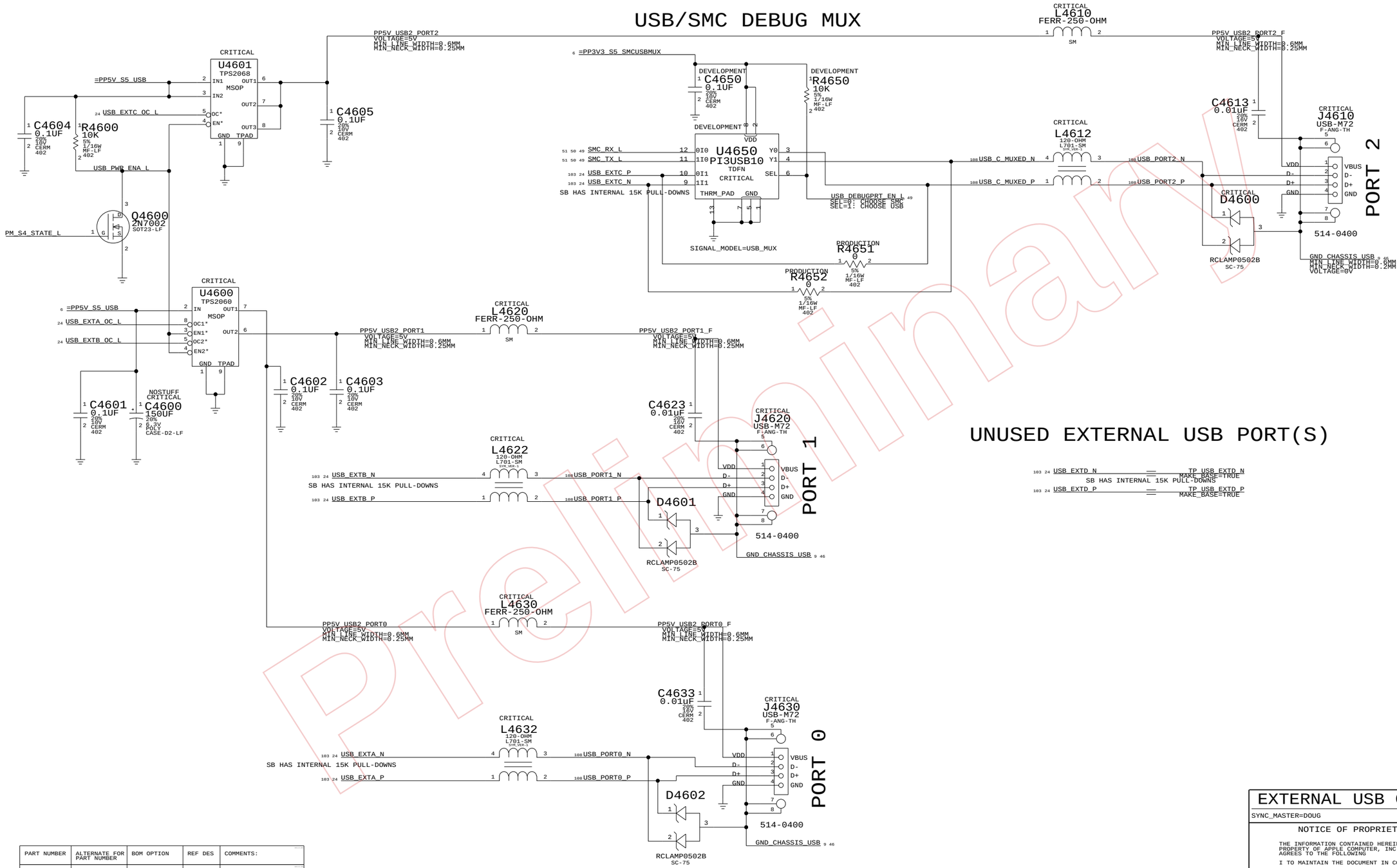
SYNC_MASTER=DOUG SYNC_DATE=10/10/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE SHT 45 OF 118

USB/SMC DEBUG MUX



UNUSED EXTERNAL USB PORT(S)

USB_EXTD_N — TP_USB_EXTD_N (MAKE_BASE=TRUE)
SB HAS INTERNAL 15K PULL-DOWNS
USB_EXTD_P — TP_USB_EXTD_P (MAKE_BASE=TRUE)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		ALL	ORIGINAL TOKO CHOKE

EXTERNAL USB CONNECTORS

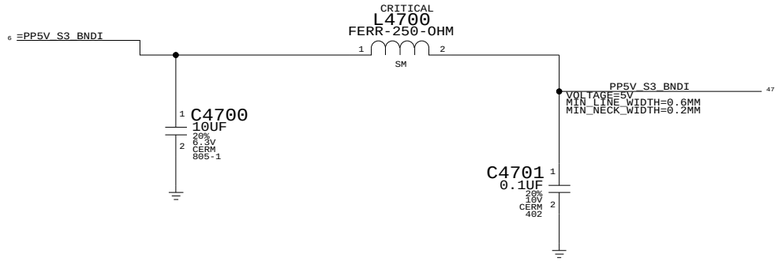
SYNC_MASTER=DOUG SYNC_DATE=12/11/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

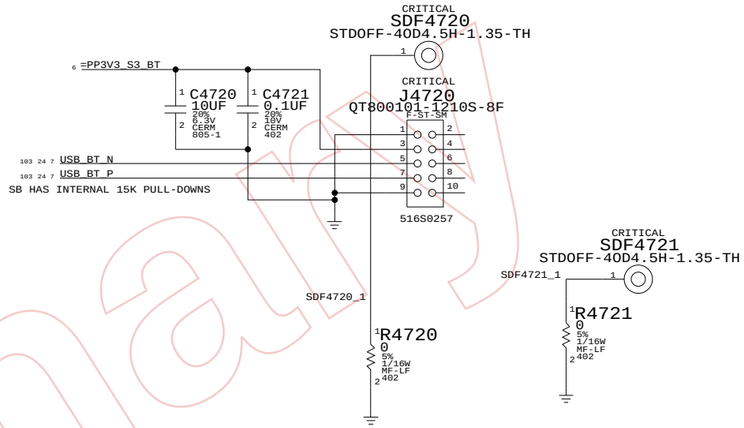
SCALE: NONE SHT 46 OF 118

CAMERA POWER FILTERING

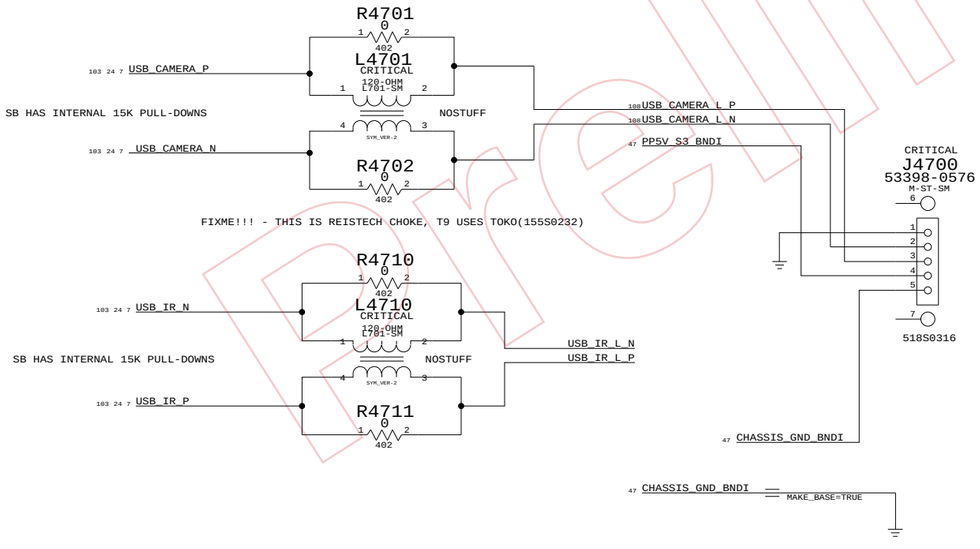


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

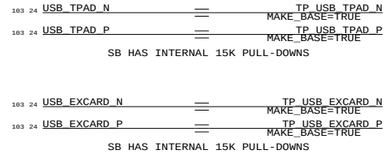
M13D (Bluetooth) Connector



CAMERA CONNECTOR



UNUSED INTERNAL USB PORTS



Internal USB Connections

SYNC_MASTER=M78_MLB SYNC_DATE=12/15/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 47 OF 118	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

OMIT
U4900
SMC_H8S2116
BGA
(1 OF 4)

25	OUT	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN
50	OUT	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN
84 70 50 7	IN	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	SMC_P62
70	IN	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	SMC_P63
50		SMC_P14	B15	P14	P64/KIN4*	K13	SMC_P64
25	OUT	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	PM_LAN_PWRGD
71 7	OUT	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L
25	OUT	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	SMC_P67
		SMC_P20	D13	P20	P70/AN0	N12	SMC_CPU_ISENSE
		SMC_P21	D14	P21	P71/AN1	R13	SMC_CPU_VSENSE
		SMC_P22	D15	P22	P72/AN2	P13	SMC_GPU_ISENSE
		SMC_P23	E12	P23	P73/AN3	R14	SMC_GPU_VSENSE
50	OUT	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE
50	OUT	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE
		SMC_P26	E13	P26	P76/AN6	N13	SMC_BATT_ISENSE
		SMC_P27	E14	P27	P77/AN7	P15	SMC_NB_1V25_ISENSE
51 23 7	BI	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L
51 23 7	BI	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	SMC_P81
51 23 7	BI	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L
51 23 7	BI	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L
51 23 7	IN	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SMC_TX_L
28 7	IN	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SMC_RX_L
105 30 7	IN	PCI_CLK33M_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	(OC) SMB_MGMT_CLK
51 25 7	BI	INT_SERIRQ	D7	P37/SERIRQ			
85	OUT	SMC_GFX_THROTTLE_L	A5	P40/TMIO	P90/IRQ2*	K4	SMC_ONOFF_L
50	OUT	SMC_SYS_LED	B5	P41/TMO0	P91/IRQ1*	J2	SMC_BC_ACOK
52	BI	SMB_MGMT_DATA (OC)	D5	P42/SDA1	P92/IRQ0*	J1	SMC_BS_ALRT_L
50		SMC_P43	C3	P43/TMI1/EXSCK1	P93/IRQ12*	J3	PM_SLP_S3_L_SMC
50		SMC_P44	B1	P44/TMO1	P94/IRQ13*	J4	PM_S4_STATE_L_SMC
50		SMC_P45	C2	P45	P95/IRQ14*	H2	PM_SLP_S5_L
50		SMC_P46	D3	P46/PWX0/PWM0	P96/EXCL	H1	SMC_SUS_CLK
50	OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	P97/IRQ15*/SDA0	G2	(OC) SMB_0_S0_DATA
51 50 49 46 7	OUT	SMC_TX_L	G1	P50			
51 50 49 46 7	IN	SMC_RX_L	G4	P51			
52	BI	SMB_0_S0_CLK (OC)	F2	P52/SCL0			

R4950 100 5% 1/16W MF-LF 402: PM_SLP_S3_L (IN) — 6 7 25 70 75 78
R4951 100 5% 1/16W MF-LF 402: PM_S4_STATE_L (IN) — 7 25 46 75 78

50 PP3V3_S5_AVREF_SMC
50 6 =PP3V3_S5_SMC

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

R4999 4.7 5% 1/16W MF-LF 402
PP3V3_S5_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT_NOTE=Place C4907 close to U4900 pin F1
SMC_VCL
C4907 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U4900
SMC_H8S2116
BGA
(3 OF 4)

AVCC	N14				
AVCC	N15				
VCC	P2				
VCC	P1				
VCC	J15				
VCC	A1				
VCL	F1				
AVREF	M14				
AVREF	M15				
		MD1	E2		SMC_MD1 (IN) 7 51
		MD2	K1		SMC_KBC_MDE
		NMI	F4		SMC_NMI (IN) 7 51
		ETRST*	L1		SMC_TRST_L (IN) 7 51
		AVSS	P12		
		VSS	R12		
51 50 7 IN	SMC_RESET_L	RES*	E3		
50	SMC_XTAL	XTAL	A2		
50	SMC_EXTAL	EXTAL	B2		

VSS: D1 P4 R4 F12 F13 B13 A13 A4 B4 D2

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402 NO STUFF

XW4900 SM

GND_SMC_AVSS 50 53 58

OMIT

(DEBUG_SW_1)		SMC_PA0	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC_CASE_OPEN (IN) 50
(DEBUG_SW_2)		SMC_PA1	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK (IN) 7 50 51
	28 25 7 OUT	PM_SYSRST_L (OC)	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI (IN) 7 50 51
	46 OUT	USB_DEBUGPRT_EN_L (OC)	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO (OUT) 7 50 51
	31 16 BI	PM_EXTTS_L<0> (OC)	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS (IN) 7 50 51
	32 16 BI	PM_EXTTS_L<1> (OC)	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0 50
	50 BI	SYS_ONEWIRE (OC)	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1 50
	25 OUT	PM_BATLOW_L (OC)	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID (IN) 50
(DEBUG_SW_3)		SMC_PB0	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_PF3 50
	25 OUT	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET (OUT) 50
	50 IN	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	SMC_BATT_VSET (OUT) 50
	53 50 OUT	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET (OUT) 50
	50 IN	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	SMC_SYS_VSET (OUT) 50
	50 OUT	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SMC_PG0 50
	50 IN	SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	=SMC_SMS_INT (IN) 50
	85 IN	SMC_GFX_OVERTEMP_L	D11	PB7	PG2/EXIRQ10*/SDA2	N9	(OC) SMB_BSA_DATA (BI) 52
	56 OUT	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	(OC) SMB_BSA_CLK (BI) 52
	56 OUT	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	(OC) SMB_A_S3_DATA (BI) 52
	57 OUT	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	(OC) SMB_A_S3_CLK (BI) 52
	50 OUT	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	(OC) SMB_B_S0_DATA (BI) 52
	56 IN	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	(OC) SMB_B_S0_CLK (BI) 52
	56 IN	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*			
	57 IN	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH0/EXIRQ6*	E1	SMC_PROCHOT (OUT) 50
	50 IN	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH1/EXIRQ7*	F3	SMC_THRMTRIP (OUT) 50
	108 50 IN	SMS_X_AXIS	M11	PD0/AN8	PH2/FWE	K2	SMC_FWE (IN) 50
	108 50 IN	SMS_Y_AXIS	P11	PD1/AN9	PH3/EXEXCL	C4	ALS_GAIN (OUT) 50
	108 50 IN	SMS_Z_AXIS	R11	PD2/AN10	PH4	D4	SMC_PH4 50
	50 IN	SMC_ANALOG_ID	N11	PD3/AN11	PH5	B3	SMS_ONOFF_L (OUT) 50
	50 IN	SMC_NB_CORE_ISENSE	P10	PD4/AN12			
	50 IN	SMC_NB_1V8_ISENSE	R10	PD5/AN13			
	50 IN	ALS_LEFT	N10	PD6/AN14			
	58 IN	ALS_RIGHT	M10	PD7/AN15			

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

OMIT
U4900
SMC_H8S2116
BGA
(4 OF 4)

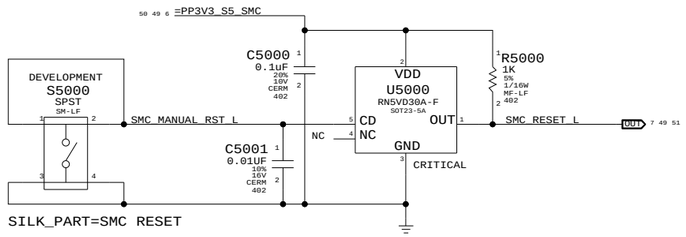
NC	G3	NC0	NC12 F15	NC
NC	H3	NC1	NC13 A14	NC
NC	K3	NC2	NC14 C12	NC
NC	L3	NC3	NC15 C10	NC
NC	N4	NC4	NC16 C5	NC
NC	M5	NC5	NC17 A3	NC
NC	N7	NC6	NC18 B8	NC
NC	M12	NC7	NC19 E4	NC
NC	M13	NC8	NC20 H4	NC
NC	L12	NC9	NC21 M9	NC
NC	K15	NC10	NC22 N8	NC
NC	J14	NC11		

SMC
SYNC_MASTER=T9_MLB_NOME SYNC_DATE=12/15/2006

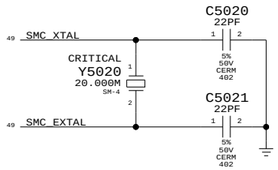
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE NONE	SHT 49 OF 118	

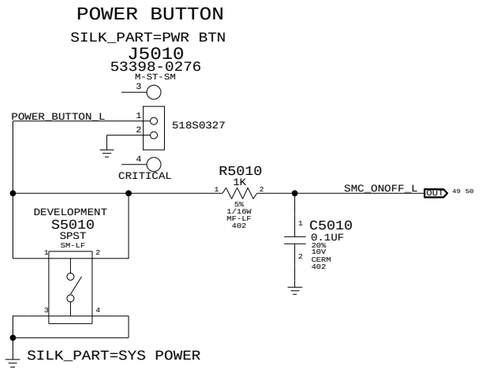
SMC Reset Button / Brownout Detect



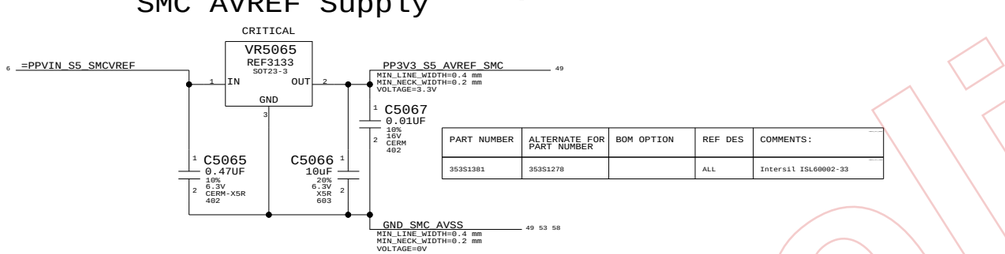
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



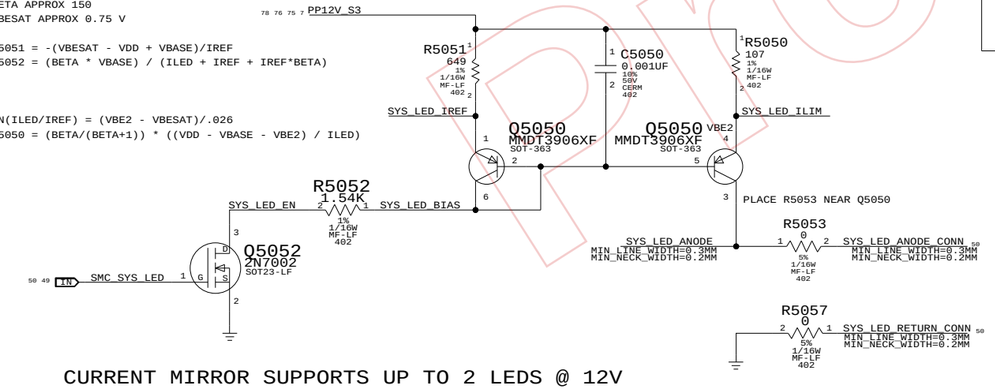
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

SYSTEM (SLEEP) LED CIRCUITS

ILED = 20 MA
IREF = 5 MA @ 12V
VBASE = VFMAX LED = 4V*2 = 8
BETA APPROX 150
VBESAT APPROX 0.75 V

R5051 = -(VBESAT - VDD + VBASE)/IREF
R5052 = (BETA * VBASE) / (ILED + IREF + IREF*BETA)

LN(ILED/IREF) = (VBE2 - VBESAT)/.026
R5050 = (BETA/(BETA+1)) * ((VDD - VBASE - VBE2) / ILED)



CURRENT MIRROR SUPPORTS UP TO 2 LEDS @ 12V
BOOST CIRCUIT UP TO 3 LEDS ON LGP

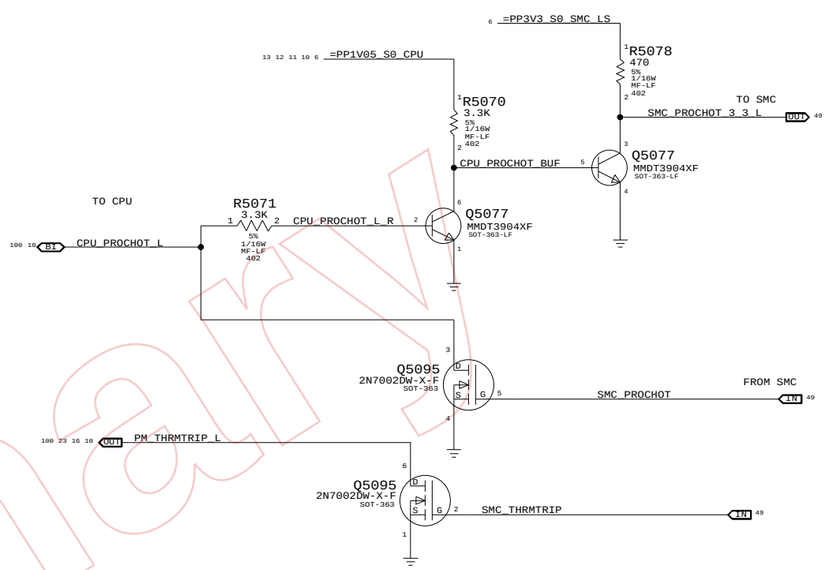
UNUSED TP/NC ALIASES

49 SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE	NO_TEST=TRUE
108 49 SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
108 49 SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
108 49 SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
49 ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	
49 ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE	
49 SMC_P14	TP_SMC_P14	MAKE_BASE=TRUE	
49 SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	
49 SMC_P21	TP_SMC_P21	MAKE_BASE=TRUE	
49 SMC_P22	TP_SMC_P22	MAKE_BASE=TRUE	
49 SMC_P23	TP_SMC_P23	MAKE_BASE=TRUE	
49 SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
49 SMC_P27	TP_SMC_P27	MAKE_BASE=TRUE	
49 SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE	
49 SMC_P44	TP_SMC_P44	MAKE_BASE=TRUE	
49 SMC_P45	TP_SMC_P45	MAKE_BASE=TRUE	
49 SMC_P62	TP_SMC_P62	MAKE_BASE=TRUE	
49 SMC_P63	TP_SMC_P63	MAKE_BASE=TRUE	
49 SMC_P64	TP_SMC_P64	MAKE_BASE=TRUE	
49 SMC_P81	TP_SMC_P81	MAKE_BASE=TRUE	
49 SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE	
49 SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE	
49 SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
49 SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
49 SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
49 SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE	
49 SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	
49 SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
49 SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
49 SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
49 SMC_P46	TP_SMC_P46	MAKE_BASE=TRUE	

UNUSED SENSORS

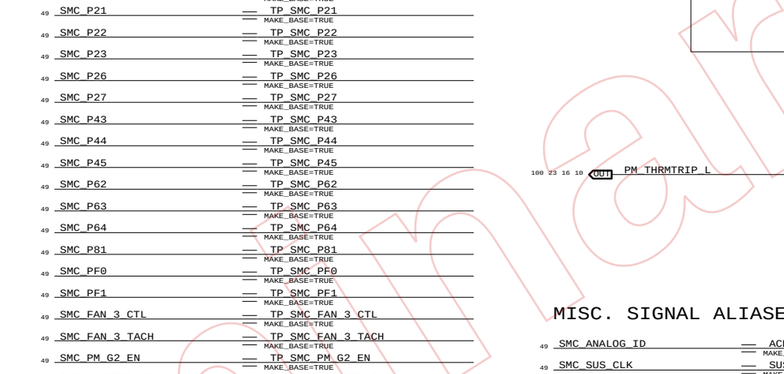
49 SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_NB_CORE_ISENSE	NC_SMC_NB_CORE_ISENSE	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_DCIN_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE	50
49 SMC_PBUS_VSENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE	50
49 SMC_BATT_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE	50
49 SMC_NB_1V25_ISENSE	UNUSED_SMC_SENSE	MAKE_BASE=TRUE	50

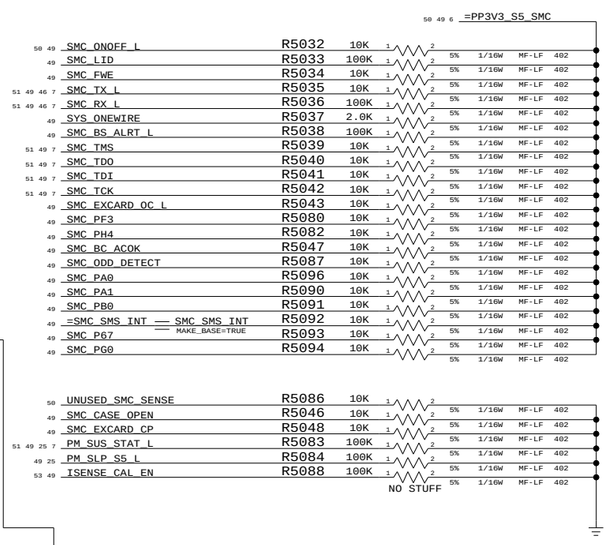
SMC FSB to 3.3V Level Shifting



MISC. SIGNAL ALIASES

49 SMC_ANALOG_ID	ACDC_TEMP	MAKE_BASE=TRUE	6
49 SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE	25
49 PM_LAN_PWRGD	ALL_SYS_PWRGD	MAKE_BASE=TRUE	7 49 70 84





SMC Support

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

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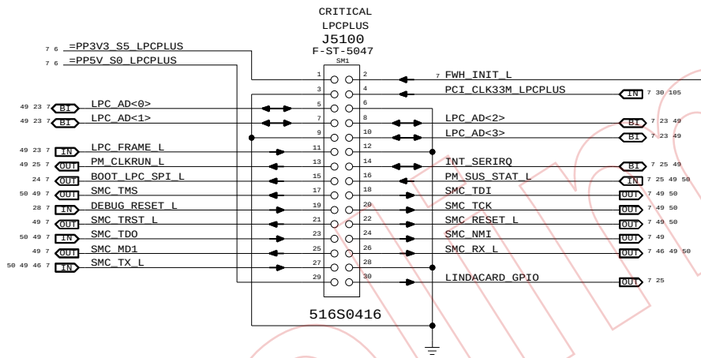
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

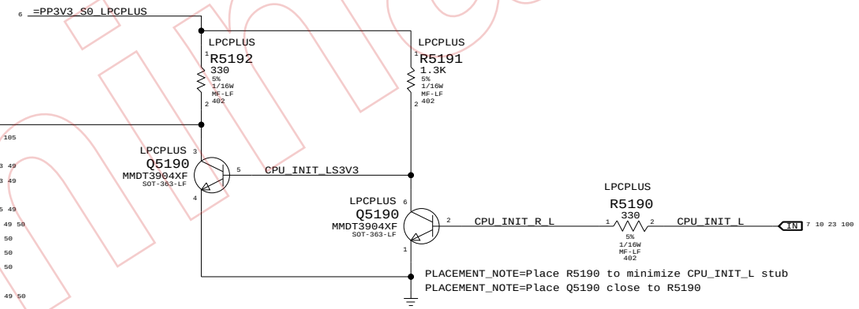
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 50 OF 118	

LPC+ Connector



FWH_INIT_L Generation



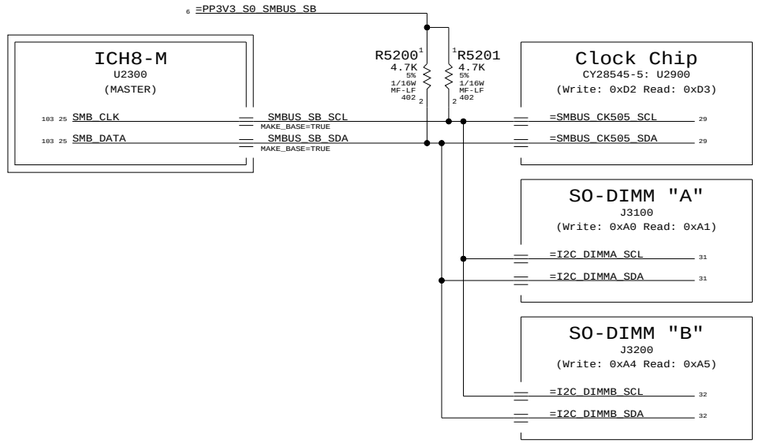
LPC+ Debug Connector

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=05/07/2007

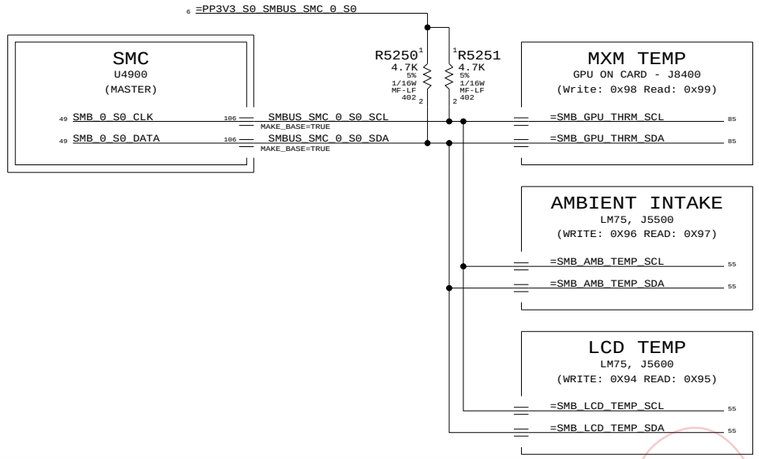
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 51 OF 118	

ICH8-M SMBus Connections

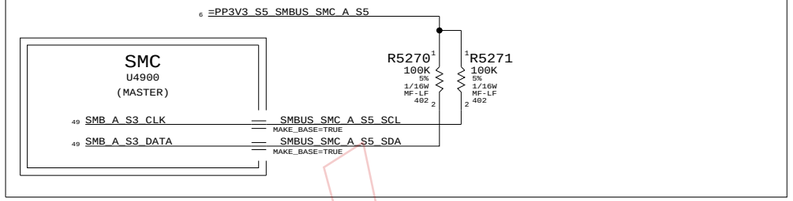


SMC "0" SMBus Connections

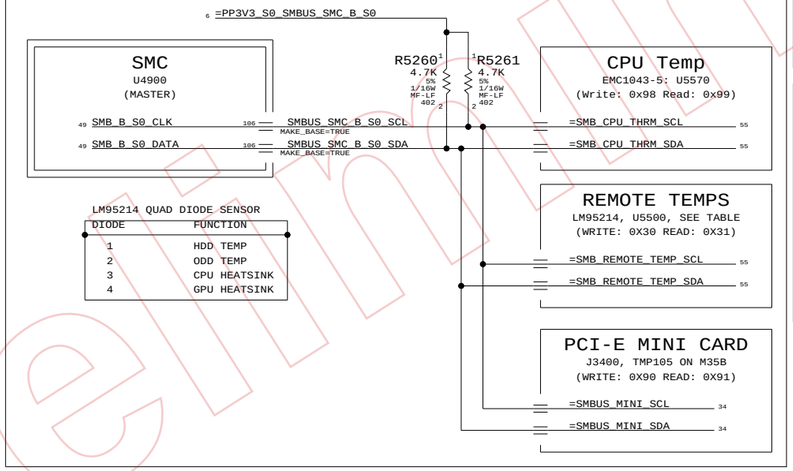


SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S5 STATE



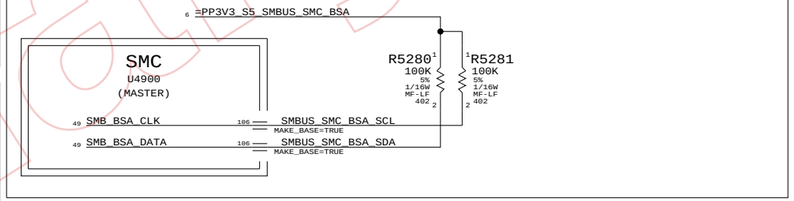
SMC "B" SMBus Connections



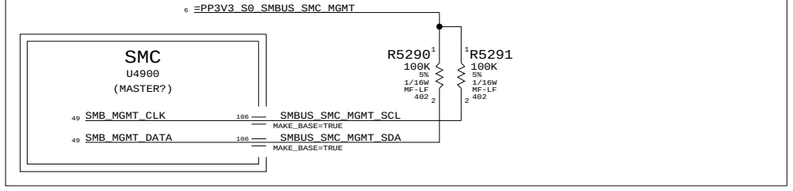
LM95214 QUAD DIODE SENSOR

DIODE	FUNCTION
1	HDD TEMP
2	ODD TEMP
3	CPU HEATSINK
4	GPU HEATSINK

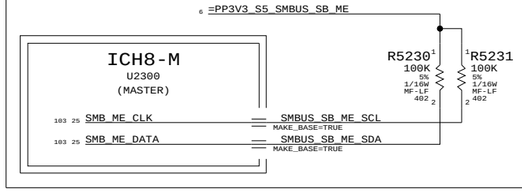
UNUSED SMC "BATTERY A" SMBUS CONNECTIONS



UNUSED SMC "MANAGEMENT" SMBUS CONNECTIONS



UNUSED ICH8-M ME SMBUS CONNECTIONS



SMBUS CONNECTIONS

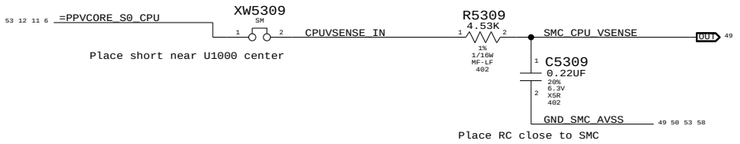
SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

APPLE COMPUTER INC.

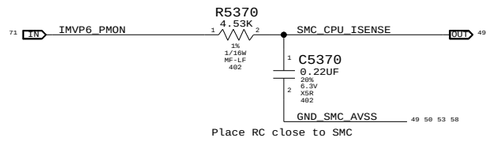
SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	52	118

CPU Voltage Sense / Filter

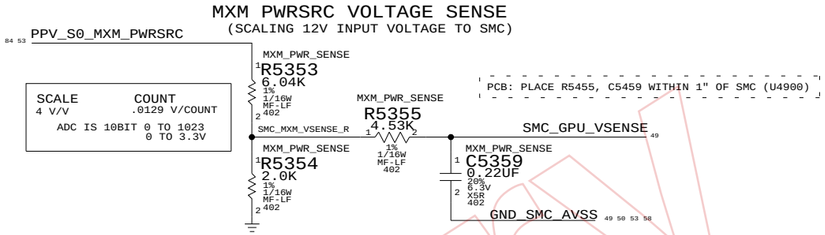


CPU SUPPLY POWER SENSE FILTER

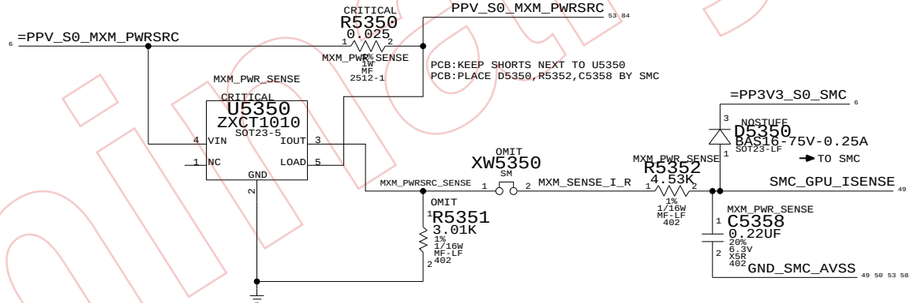


PCPU = VPMON / (17.5 * .0021)

MXM PWRSRC VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



M78 SET FOR APPROX 3V AT 5A ON PWRSRC
MXM-HE CAN GO TO 16A, BUT M78
CARDS TARGET MAX 55W AT 12V

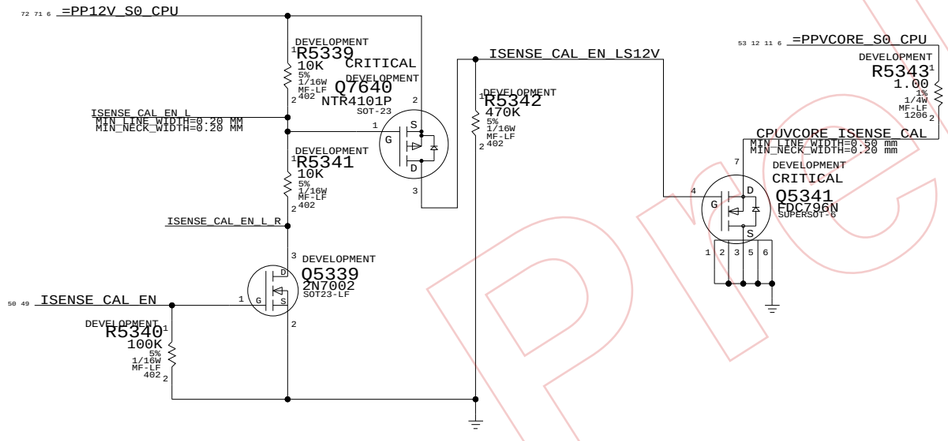
SCALE	COUNT
1.6461 A/V	.005309969 A/COUNT
ADC IS 10BIT 0 TO 1023 0 TO 3.3V	

M72 SET FOR APPROX 3V AT 4A ON PWRSRC

SCALE	COUNT
1.3289 A/V	.004286786 A/COUNT
ADC IS 10BIT 0 TO 1023 0 TO 3.3V	

CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0264	1	RES,3.01K,1%,402	R5351	20_INCH_LCD
114S0254	1	RES,2.43K,1%,402	R5351	24_INCH_LCD

Current & Voltage Sensing

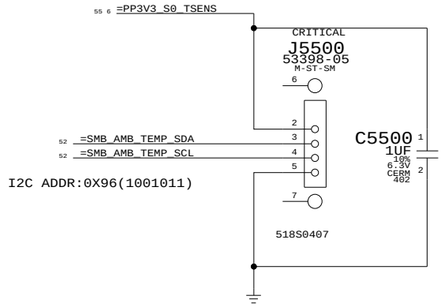
SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

APPLE COMPUTER INC.

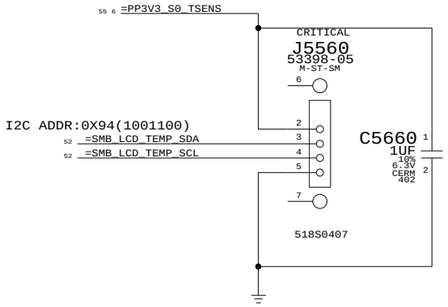
SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE NONE	SHT 53 OF 118	

REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

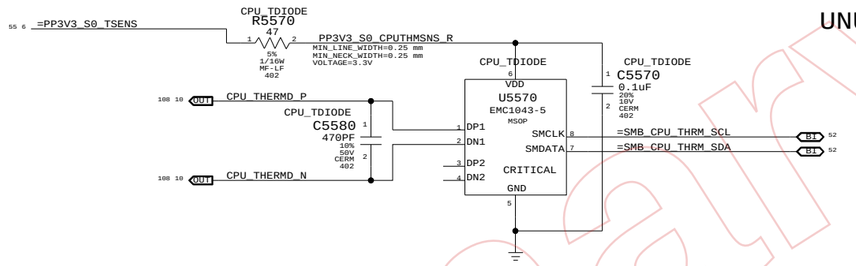
AMBIENT TEMP SENSOR



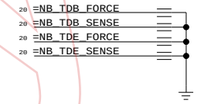
LCD TEMP SENSOR



CPU T-Diode Thermal Sensor

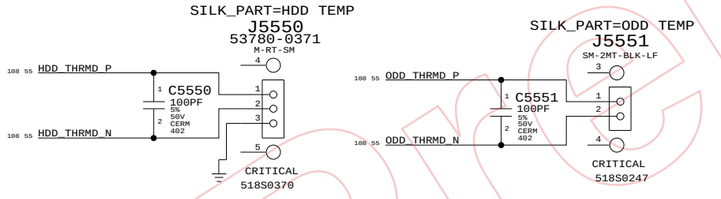


UNUSED NB THERMAL SENSORS

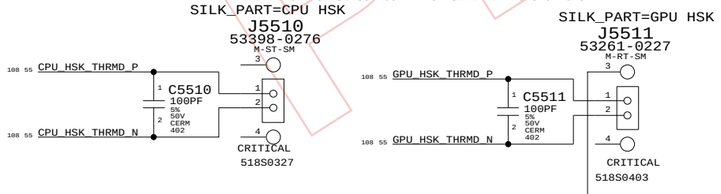


PLACE ALL CAPS NEAR U5500

PLACE DISK SENSOR CONNS BOTTOM SIDE

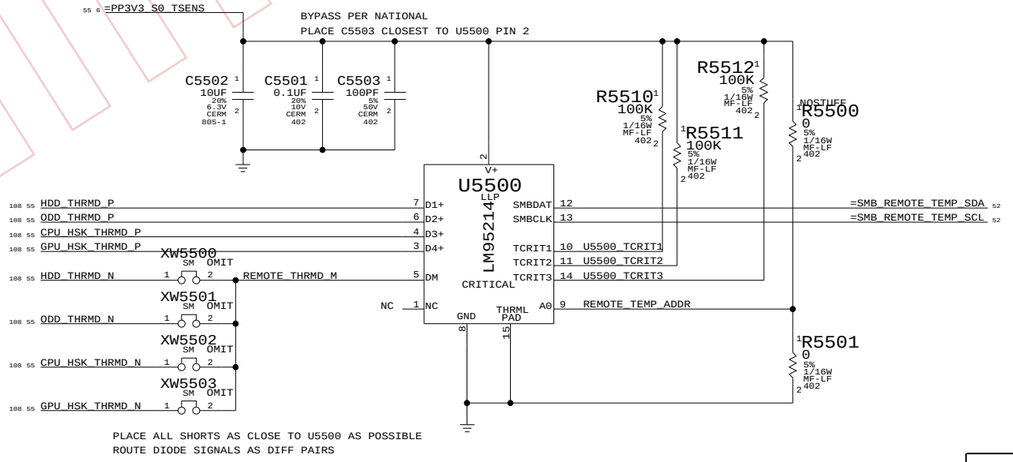


PLACE HSK SENSOR CONN. TOP SIDE NEAR GPU OR CPU



TO HELP POWER DELIVERY

74 73 7 6 PPMCH_CORE_S0



PLACE ALL SHORTS AS CLOSE TO U5500 AS POSSIBLE
ROUTE DIODE SIGNALS AS DIFF PAIRS

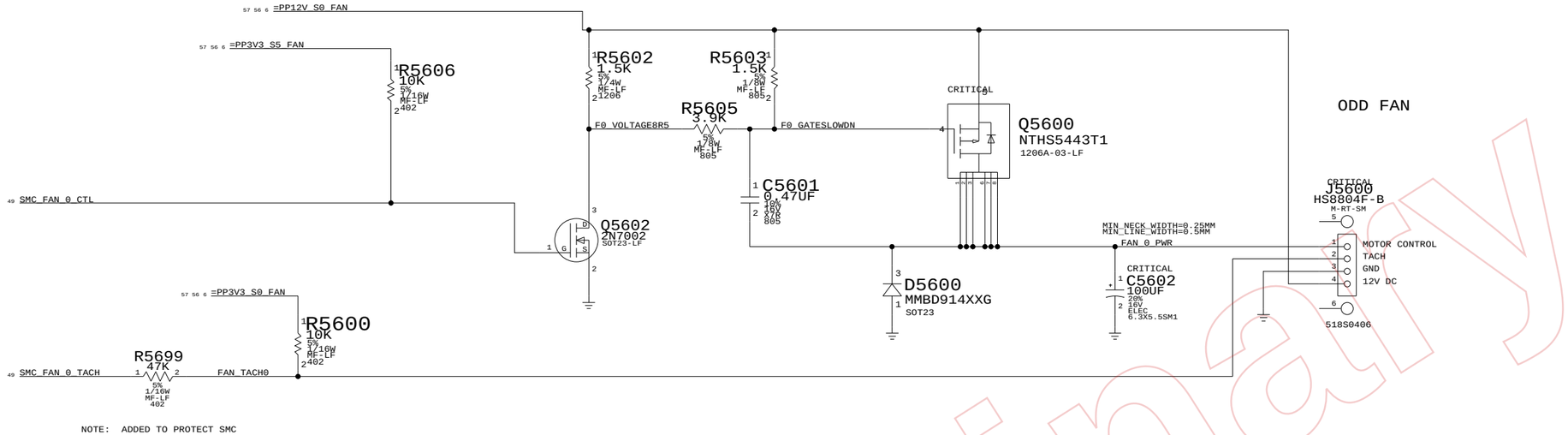
Thermal Sensors

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

APPLE COMPUTER INC.

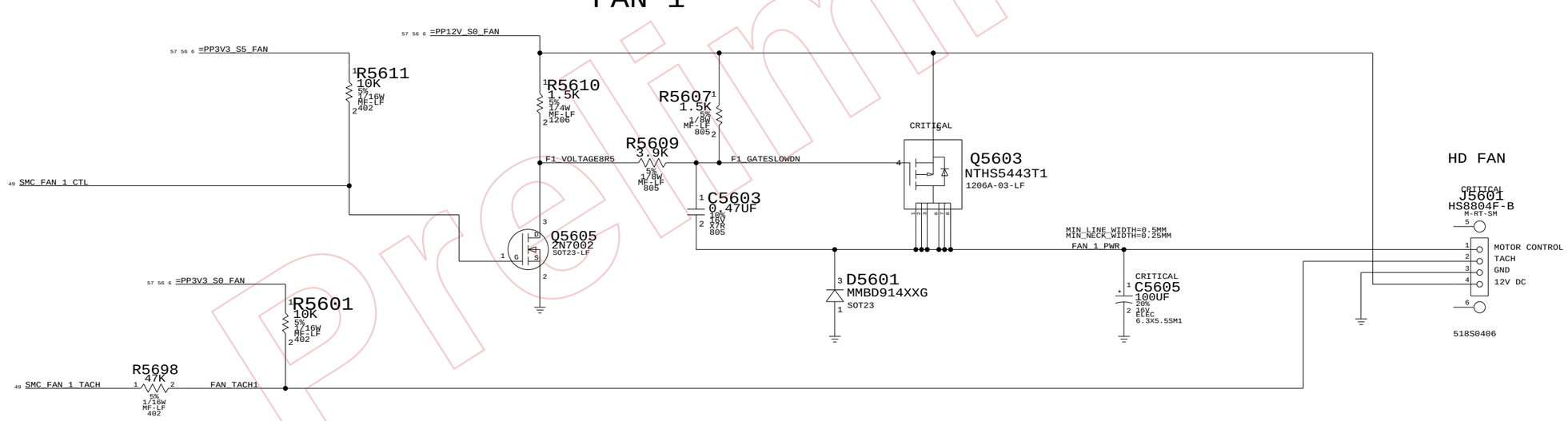
SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 55 OF 118	

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



HD AND OD FAN

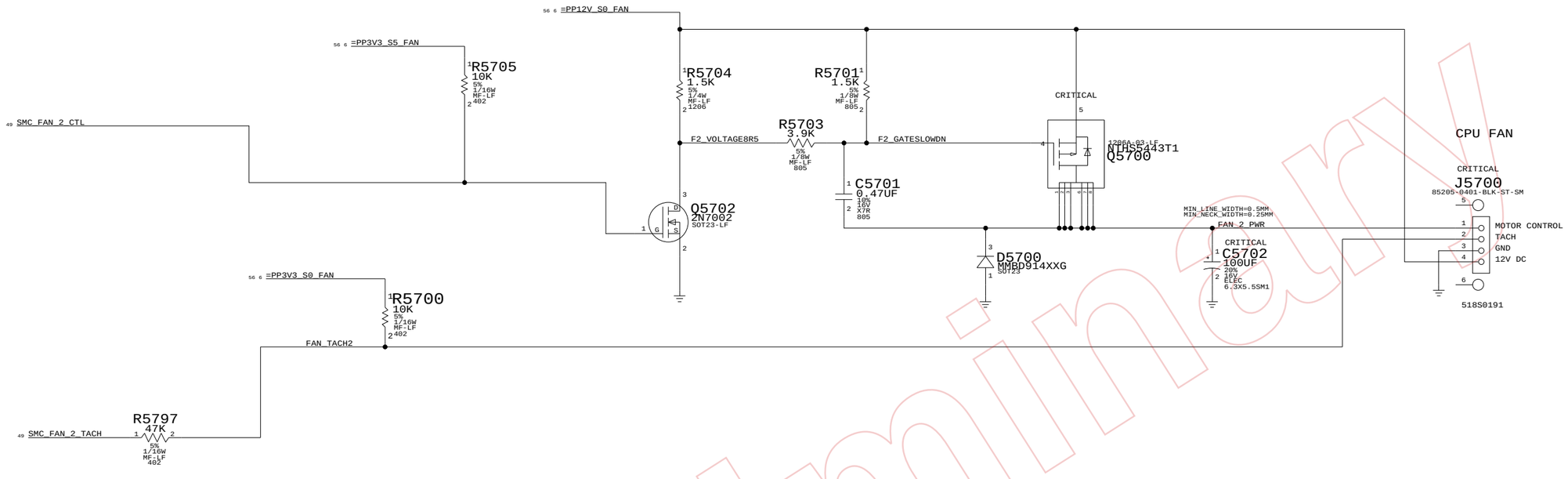
SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	56	118

FAN 2



CPU FAN

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

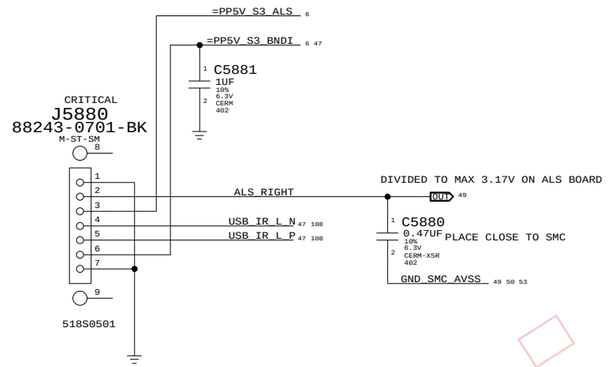
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE NONE

SHT 57 OF 118

ANALOG ALS & IR



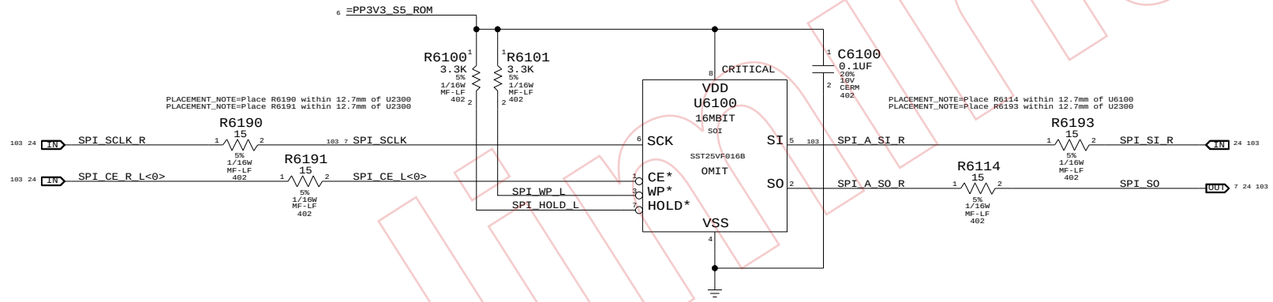
ALS Support

SYNC_MASTER=DAVE_MASTER SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	58	118



SPI BootROM

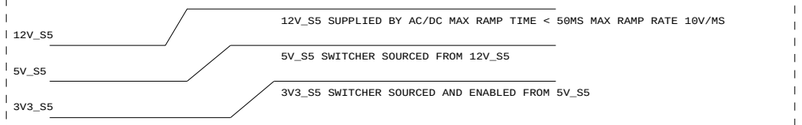
SYNC_MASTER=T9_MLB_NOME SYNC_DATE=05/07/2007

APPLE COMPUTER INC.

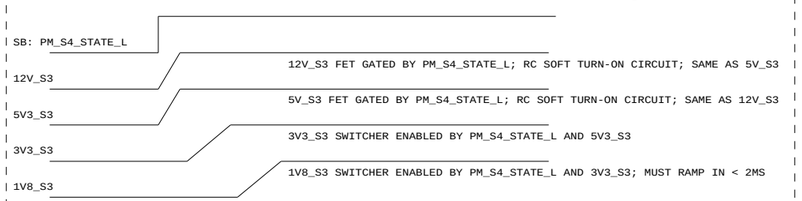
SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	61	118

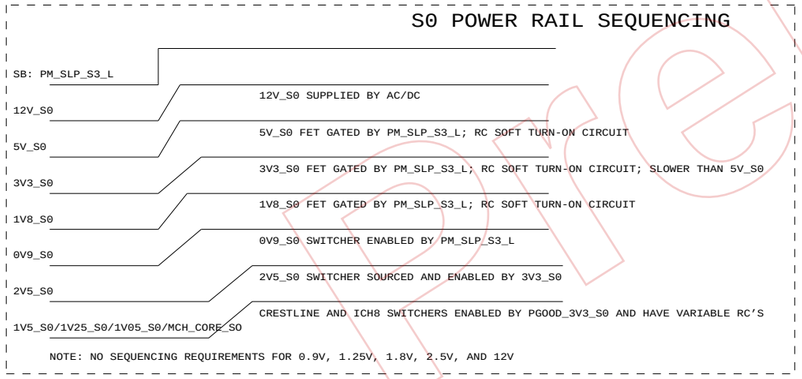
S5 POWER RAIL SEQUENCING



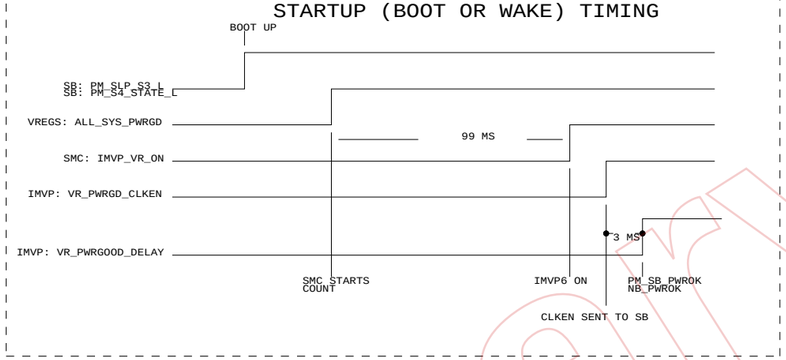
S3 POWER RAIL SEQUENCING



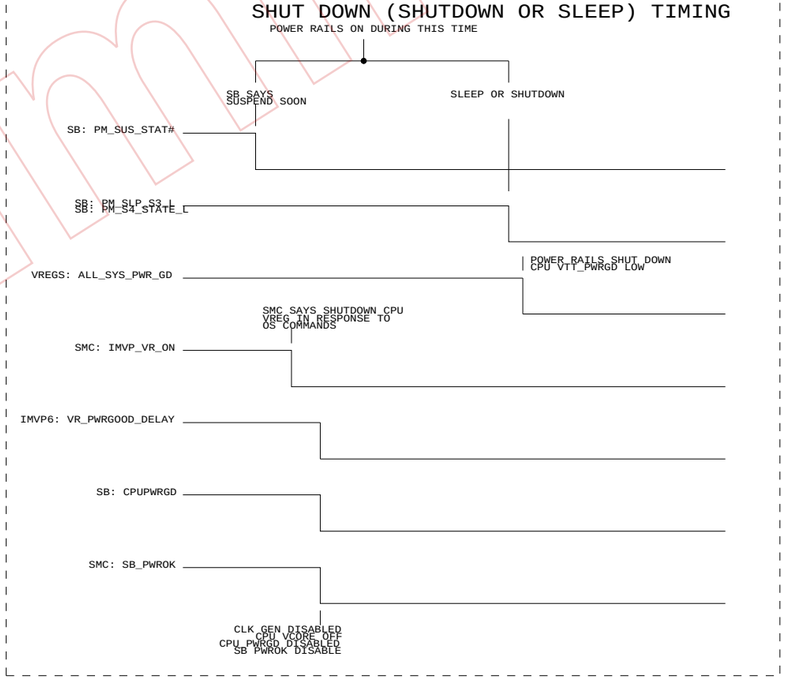
S0 POWER RAIL SEQUENCING



STARTUP (BOOT OR WAKE) TIMING



SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



POWER SEQUENCING BLOCK DIAGRAM

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE NONE SHT 69 OF 118

PGOOD Comparators

78 76 7 6 PP12V_S5
78 77 76 70 7 6 PP5V_S5
78 77 70 13 7 6 PP3V3_S0
78 7 6 PP1V8_S0
94 78 74 73 72 71 7 6 PP5V_S0
75 7 6 PP0V9_S0

C7010 0.1UF 20% 16V CERM 603

R7010[1] 2.21K 1% 1/16W MF-LF 402
R7013[1] 7.5K 1% 1/16W MF-LF 402
R7018[1] 5.62K 1% 1/16W MF-LF 402
R7020[1] 1.62K 1% 1/16W MF-LF 402

R7000 2.74K 1% 1/16W MF-LF 402
R7001 1.43K 1% 1/16W MF-LF 402
R7002 3.92K 1% 1/16W MF-LF 402
R7003 715 1% 1/16W MF-LF 402

R7011[1] 1K 1% 1/16W MF-LF 402
R7014[1] 10K 1% 1/16W MF-LF 402
R7019[1] 1K 1% 1/16W MF-LF 402
R7021[1] 10K 1% 1/16W MF-LF 402

(2.94V/2.61V; 330MV HYSTERESIS)
(1.58V/1.41V; 172MV HYSTERESIS)
(4.47V/4.00V; 470MV HYSTERESIS)
(0.76V/0.67V; 85MV HYSTERESIS)

NOSTUFF C7000 0.1uF 20% 10V CERM 402
NOSTUFF C7001 0.1uF 20% 10V CERM 402
NOSTUFF C7002 0.1uF 20% 10V CERM 402
NOSTUFF C7003 0.1uF 20% 10V CERM 402

CRITICAL
U7010 LM339A SOI-LF

-1	4	5VS5_2V80_REF
+1	5	3V3S0_COMP_REF
-2	6	5VS5_1V53_REF
+2	7	1V8S0_COMP_REF
-3	8	5VS5_4V24_REF1
+3	9	5VS0_COMP_REF
-4	10	5VS5_0V76_REF
+4	11	0V9S0_COMP_REF
V+	3	
GND	12	
OUT1	2	PGOOD_3V3_S0 OUT 70 77
OUT2	1	PGOOD_1V8_S0 OUT 70
OUT3	14	PGOOD_5V_S0 OUT 70
OUT4	13	PGOOD_0V9_S0 OUT 70

R7005 100K 1% 1/16W MF-LF 402
R7006 100K 1% 1/16W MF-LF 402
R7007 100K 1% 1/16W MF-LF 402
R7008 100K 1% 1/16W MF-LF 402

(HYSTERESIS)
(R7000: 10.5K; R7001: 17.4K; R7002: 24.9K; R7003: 8.25K) (200MV; 150MV; 300MV; 100MV HYSTERESIS)
(R7010: 21.5K; R7013: 7.15K; R7018: 52.3K; R7020: 1.97K) (200MV; 150MV; 300MV; 100MV HYSTERESIS)

(PULLUPS ARE NEAR LOADS)

(SUPPLY CHANGED FOR ROUTING)

78 76 75 7 6 PP5V_S3
(REMOVE AFTER DEVELOPMENT, MAKE INTO TP)
75 IN PGOOD_1V8_S3
R7080 100K 5% 1/16W MF-LF 402
76 IN PGOOD_3V3_S3
R7081 100K 5% 1/16W MF-LF 402
78 76 75 7 6 PP3V3_S3

PWROK Sequencing

78 77 70 13 7 6 PP3V3_S0
R7034[1] 5.1K 5% 1/16W MF-LF 402

70 IN PGOOD_0V9_S0
R7030 100 5% 1/16W MF-LF 402
70 IN PGOOD_5V_S0
R7031 100 5% 1/16W MF-LF 402
70 IN PGOOD_1V8_S0
R7032 100 5% 1/16W MF-LF 402
77 IN PGOOD_2V5_S0
R7033 100 5% 1/16W MF-LF 402

(NOT ALL PGOODS ARE NEEDED HERE SINCE
(SOME REGULATORS ARE DAISY CHAIN ENABLED)

PGOOD_S0_OUT1

(MC74VHC1G08 HAS 100NS/V MAX SLEW RATE)
(10PF MAX CIN)

U7052 MC74VHC1G08 SOT23-5-LF

77 75 70 7 6 PP3V3_S5
C7052 0.1uF 20% 10V CERM 402
C7056 0.1uF 20% 10V CERM 402

ALL_SYS_PWRGD OUT 7 49 50 84

U7056 MC74VHC1G08 SOT23-5-LF

71 22 16 7 IN VR_PWRGOOD_DELAY
PM_SB_PWROK OUT 7 25 28

NVIDIA

78 77 70 13 7 6 PP3V3_S0
R7039[1] 5.1K 5% 1/16W MF-LF 402

74 IN PGOOD_MCH_CORE_S0
R7035 100 5% 1/16W MF-LF 402
IMVP_PGD_IN
CRF
73 IN PGOOD_1V05_S0
R7036 100 5% 1/16W MF-LF 402
74 IN PGOOD_1V25_S0
R7037 100 5% 1/16W MF-LF 402
73 IN PGOOD_1V5_S0
R7038 100 5% 1/16W MF-LF 402

77 75 70 7 6 PP3V3_S5
R7092[1] 10K 5% 1/16W MF-LF 402
(3.3V WILL NOT BE UP UNTIL 5V IS IN REGULATION)
(SMC CAN HANDLE SLOW RISE TIME OF RSMRST_PWRGD)
77 IN PGOOD_3V3_S5
RSMRST_PWRGD OUT 49
MAKE_BASE=TRUE
NOSTUFF C7090 220PF 5% 25V CERM 402

1.05V/MCH_CORE S0 RUN/SS CONTROL

77 75 70 7 6 PP3V3_S5
R7070[1] 5.1K 5% 1/16W MF-LF 402

77 76 IN PGOOD_3V3_S0
R7040 0 5% 1/16W MF-LF 402
PGOOD_CR_S0
R7065 100K 5% 1/16W MF-LF 402
1V05S0_RUNSS_BUF
R7066 330 5% 1/16W MF-LF 402
1V05S0_RUNSS OUT 73 74

76 IN PGOOD_12V_S0
R7041 0 5% 1/16W MF-LF 402

Q7007 SSM6N15FE SOT563
70 RUNSS_GATE_D_L

C7062 0.01UF 10% 16V CERM 402

1.25V S0 RUN/SS CONTROL

R7063 51K 5% 1/16W MF-LF 402
1V25S0_RUNSS_BUF
R7064 680 5% 1/16W MF-LF 402
1V25S0_RUNSS OUT 74

Q7006 SSM6N15FE SOT563
70 RUNSS_GATE_D_L

C7061 0.01UF 10% 16V CERM 402

1.5V S0 RUN/SS CONTROL

R7061 10K 5% 1/16W MF-LF 402
1V5S0_RUNSS_BUF
R7062 1K 5% 1/16W MF-LF 402
1V5S0_RUNSS OUT 73

78 77 76 70 7 6 PP5V_S5
R7060 470K 5% 1/16W MF-LF 402

CRITICAL
Q7007 SSM6N15FE SOT563
70 RUNSS_GATE_D_L

C7060 0.01UF 10% 16V CERM 402

CRITICAL
Q7006 SSM6N15FE SOT563
78 75 49 25 7 6 IN PM_SLP_S3_L

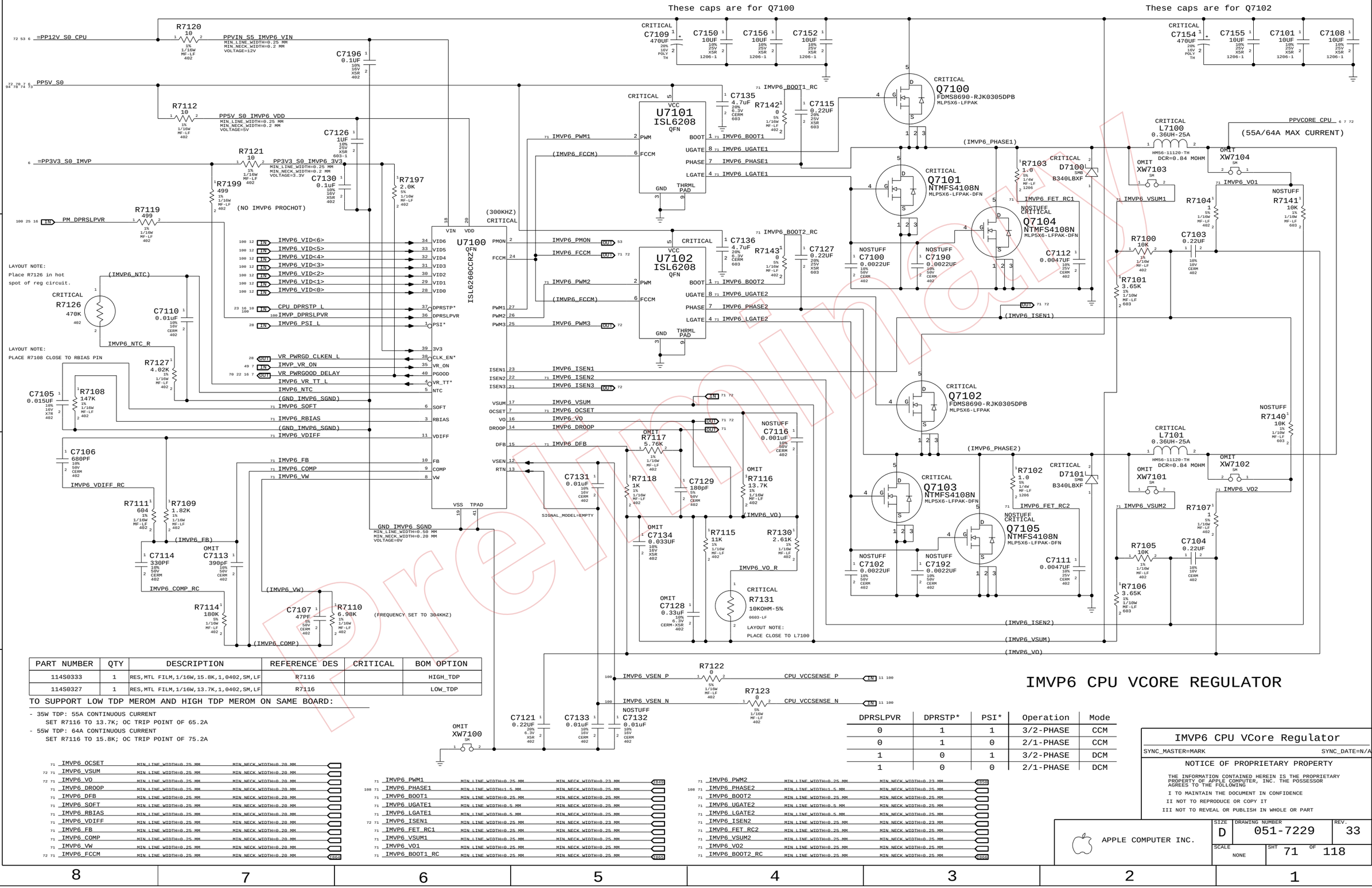
PGOOD and Power Sequencing

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE SHT 70 OF 118



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0333	1	RES,MTL FILM,1/16W,15.8K,1,0402,SM,LF	R7116		HIGH_TDP
114S0327	1	RES,MTL FILM,1/16W,13.7K,1,0402,SM,LF	R7116		LOW_TDP

TO SUPPORT LOW TDP MEROM AND HIGH TDP MEROM ON SAME BOARD:

- 35W TDP: 55A CONTINUOUS CURRENT
  SET R7116 TO 13.7K; OC TRIP POINT OF 65.2A
- 55W TDP: 64A CONTINUOUS CURRENT
  SET R7116 TO 15.8K; OC TRIP POINT OF 75.2A

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

IMVP6_OCSET MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VSUM MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VO MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_DROOP MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_DFB MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_SOFT MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_RBIAS MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VDIFF MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_FB MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_COMP MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_VW MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
IMVP6_FCCM MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM

IMVP6_PWM1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.23 MM
IMVP6_PHASE1 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_UGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_LGATE1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_ISEN1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.23 MM
IMVP6_FET_RC1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VSUM1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VO1 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT1_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM

IMVP6_PWM2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.23 MM
IMVP6_PHASE2 MIN_LINE_WIDTH=1.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_UGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_LGATE2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_ISEN2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.23 MM
IMVP6_FET_RC2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VSUM2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_VO2 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
IMVP6_BOOT2_RC MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM

IMVP6 CPU VCore Regulator	
SYNC_MASTER=MARK	SYNC_DATE=N/A

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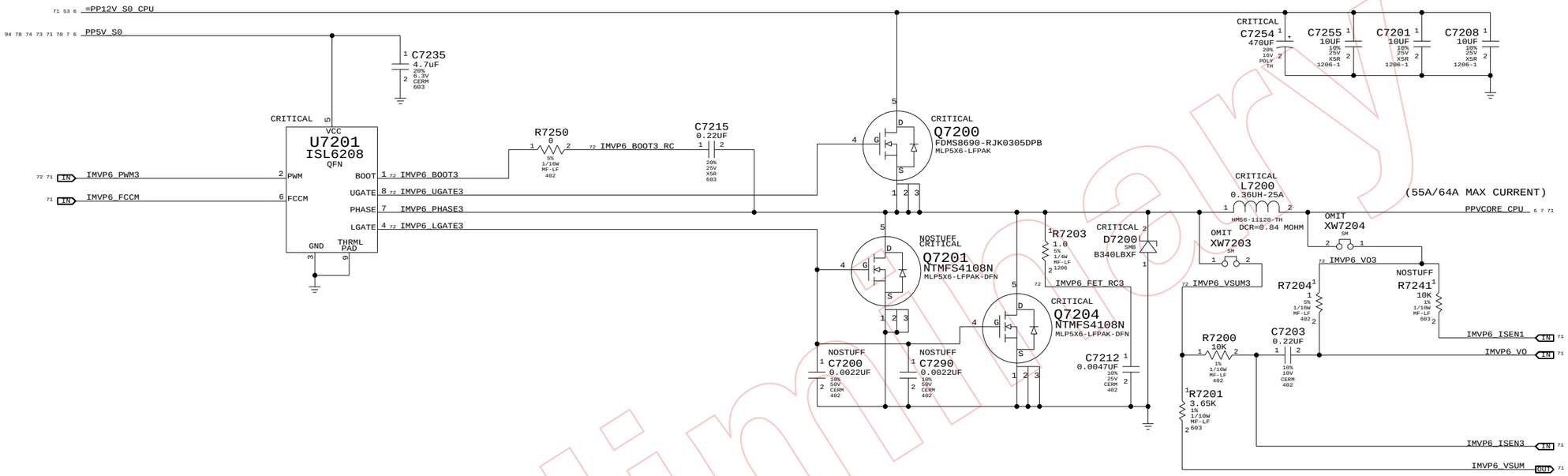
D	051-7229	33
SCALE: NONE	SHT 71 OF 118	

IMVP6 CPU VCORE REGULATOR



72 71	IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	151
108 72	IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	145
72	IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	144
72	IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	145
72	IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	146
72 71	IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	148
72	IMVP6_FET_RC3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	147
72	IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72	IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	150
72	IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	152

IMVP6 3RD PHASE

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE	SHT	OF
NONE	72	118

1.5V S0 & 1.05V SO RAILS

PP12V_S0
C7340 470UF 20% 16V POLY TH (CRITICAL)
C7341 10UF 10% 25V X5R 1206-1
C7342 10UF 10% 25V X5R 1206-1
C7330 1UF 10% 25V X5R 603-1
CR_E C7381 10UF 10% 25V X5R 1206-1
CR_E C7382 10UF 10% 25V X5R 1206-1
CR_E C7360 1UF 10% 25V X5R 603

PP5V_S0
C7310 4.7UF 20% 6.3V CERM 603
D7301 BAT54E3 SOT23 (CRITICAL)
1V5REG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
D7374 CR_E BAT54E3 SOT23 (CRITICAL)
R7361 0 5% 1/16W MF-LF 402 CR_E
1V05REG_BOOT_R MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

C7331 0.1UF 20% 25V CERM 603
R7331 0 5% 1/16W MF-LF 402

U7300 ISL6539 SSOP (300KHZ) CRITICAL
VCC
VIN
SOFT1 — 1V5REG_SOFT
BOOT1 — 1V5REG_BOOT
UGATE1 — 1V5REG_UGATE
PHASE1
ISEN1 — 1V5REG_ISEN
LGATE1 — 1V5REG_LGATE
PGND1
VSEN1 — 1V5REG_SWITCHNODE
EN1 — 1V5S0_RUNSS (200MV HYSTERESIS)
PG1 — PGOOD_1V5_S0 (3MS NOISE FILTER)
OCSET1 — 1V5REG_OCSET
SOFT2 — 1V05REG_SOFT
BOOT2 — 1V05REG_BOOT
UGATE2 — 1V05REG_UGATE
PHASE2
ISEN2 — 1V05REG_ISEN
LGATE2 — 1V05REG_LGATE
PGND2
VSEN2 — 1V05REG_SWITCHNODE
EN2 — 1V05S0_RUNSS (200MV HYSTERESIS)
PG2/REF — PGOOD_1V05_S0 (3MS NOISE FILTER)
OCSET2 — 1V05REG_OCSET
DDR
GND

Q7300 FDMS9620S MLP (CRITICAL) — Q1, Q2
Q7360 CR_E FDMS9620S MLP (CRITICAL) — Q1, Q2

L7300 1.5UH-12A MMD06E2-SM DCR=9 MOHM (CRITICAL)
L7360 CR_E 1.5UH-12A MMD06E2-SM DCR=9 MOHM (CRITICAL)

PP1V5_S0 (1.512V NOMINAL)
C7301 22UF 20% 6.3V CERM 805
C7304 22UF 20% 6.3V CERM 805
C7303 330UF 20% 2V POLY CASE-D2-SM (CRITICAL)
C7300 330UF 20% 2V POLY CASE-D2-SM (CRITICAL)
R7306 5.11 1% 1/4W MF-LF 1206
1V5REG_SNUBBER_R
C7324 1000PF 10% 25V X7R 402
D7300 CTLSH3-30M833 TLM833
NOSTUFF
R7300 10.2K 1% 1/16W MF-LF 402 <RA>
C7302 0.0022UF 10% 50V CERM 402
VOUT = 0.9V * (RA + RB) / RB
1V5REG_VSEN MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7301 15.0K 1% 1/16W MF-LF 402 <RB>
GND_PP1V5REG_SGND MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM VOLTAGE=0V

R7321 1K 1% 1/16W MF-LF 402
NOSTUFF C7335 0.001UF 10% 50V CERM 402
R7323 100K 1% 1/16W MF-LF 402
C7332 0.01UF 10% 50V X7R 402
CR_E R7382 0 1/10W MF-LF 402
OMIT XW7300 SM
CR_STD R7384 10K 1% 1/10W MF-LF 402
CR_E R7383 100K 1% 1/10W MF-LF 402
CR_E C7372 0.01UF 10% 50V X7R 402

R7371 CR_E 1.40K 1% 1/16W MF-LF 402
NOSTUFF C7345 0.001UF 10% 50V CERM 402
D7373 CTLSH3-30M833 TLM833
R7356 CR_E 5.11 1% 1/4W MF-LF 1206
1V05REG_SNUBBER_R
C7364 CR_E 1000PF 10% 25V X7R 402
C7361 CR_E 0.1UF 20% 25V CERM 603
C7390 CR_E 330UF 20% 2V POLY CASE-D2-SM (CRITICAL)
C7391 CR_E 330UF 20% 2V POLY CASE-D2-SM (CRITICAL)
C7392 CR_E 22UF 20% 6.3V CERM 805
C7393 CR_E 22UF 20% 6.3V CERM 805
PP1V05_S0 1.05V NOMINAL
R7390 CR_E 3.32K 1% 1/16W MF-LF 402 <RA>
C7370 CR_E 0.0022UF 10% 50V CERM 402
VOUT = 0.9V * (RA + RB) / RB
1V05REG_VSEN MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
R7391 CR_E 19.6K 1% 1/16W MF-LF 402 <RB>

1.5V S0
M72778
POWER BUDGET
PEAK=2.77A
AVE=2.45A

1.05V S0
M72/M78
POWER BUDGET
PEAK=3.43A
AVE=3.03A

PLANE SHORTING RESISTORS

PP1V05_S0 — CR_STD R7310 0 5% 1/4W MF-LF 1206 — PPMCH_CORE_S0
CR_STD R7311 0 5% 1/4W MF-LF 1206
CR_STD R7312 0 5% 1/4W MF-LF 1206
CR_STD R7313 0 5% 1/4W MF-LF 1206

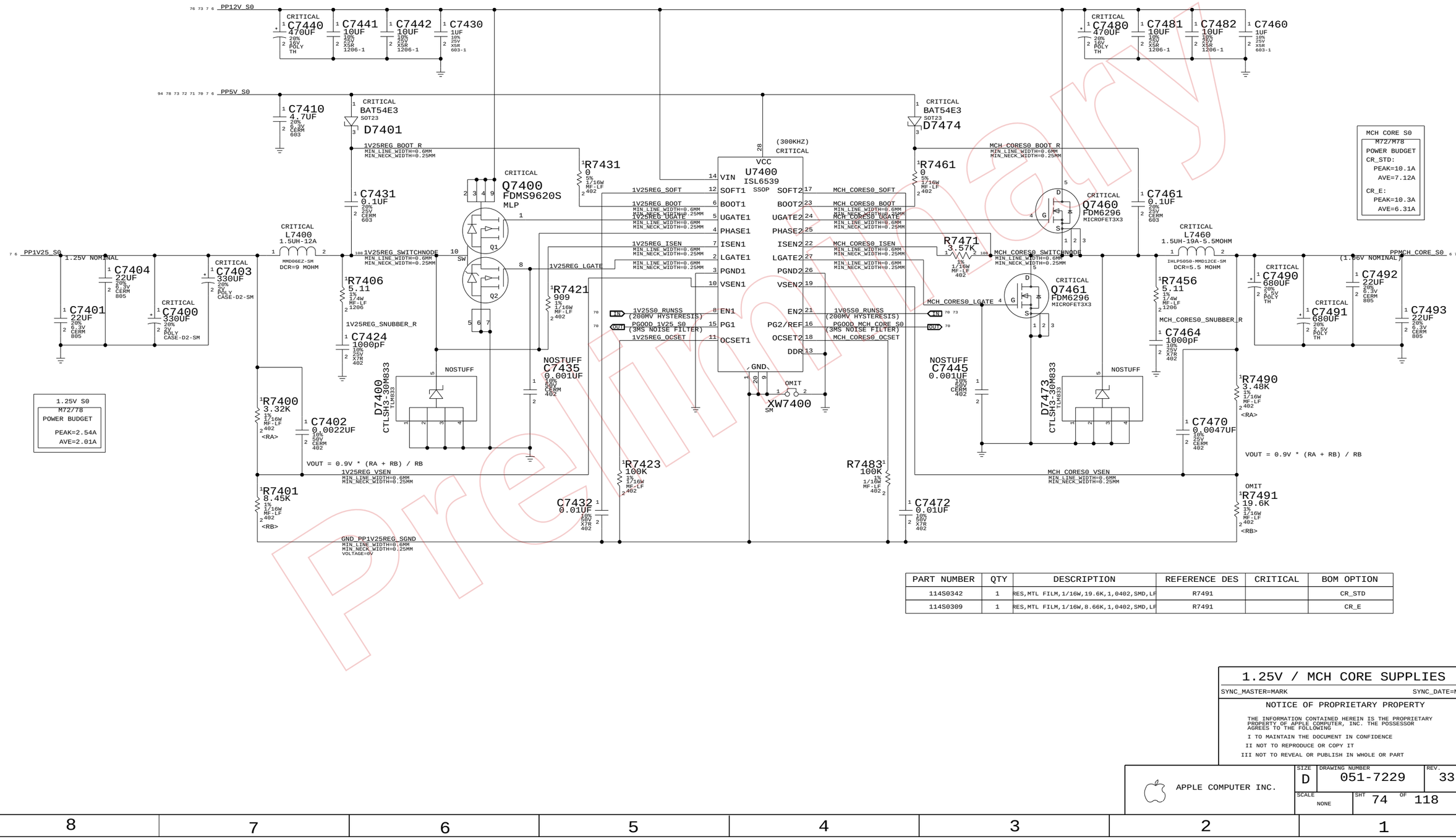
1.5V / 1.05V SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 73 OF 118	

1.25V S0 & MCH CORE RAILS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7491		CR_STD
114S0309	1	RES,MTL FILM,1/16W,8.66K,1,0402,SMD,LF	R7491		CR_E

1.25V / MCH CORE SUPPLIES

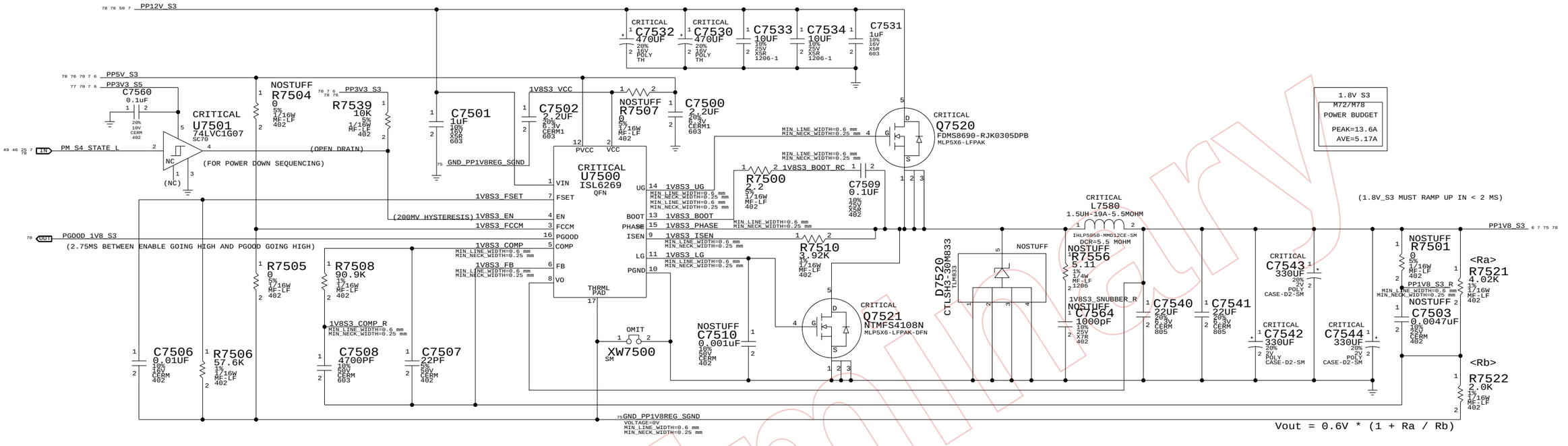
SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

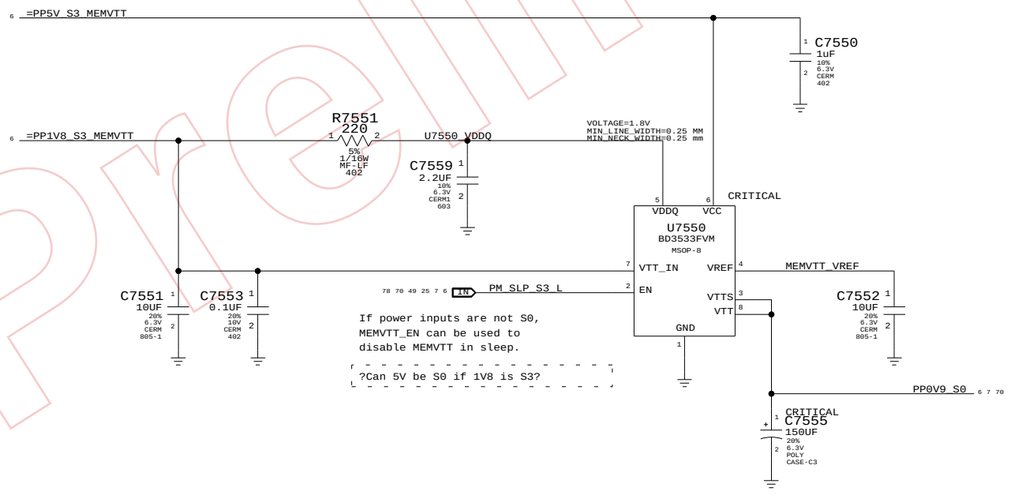
SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE SHT 74 OF 118

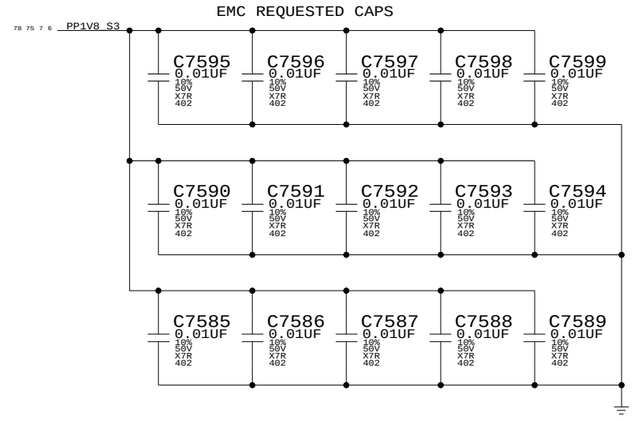
1.8V S3 / MEM VTT RAILS



DDR2 Vtt Regulator



EMC REQUESTED CAPS



1.8V S3 /0.9V S0 SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 75 OF 118	

5V S5 & 3.3V S3 RAILS

PP12V_S0
PP5V_S5
R7615 1.65K 1% 1/16W MF-LF 402
R7616 10K 1% 1/16W MF-LF 402
R7613 10K 1% 1/16W MF-LF 402
R7614 10K 1% 1/16W MF-LF 402
5VS5_4V29_REF
12VS0_6V0_REF
R7617 4.99K 1% 1/16W MF-LF 402
12VS0_COMP_REF
U7601 LM393A SOI-1-LF (CRITICAL)
R7618 100K 1% 1/16W MF-LF 402
PGOOD_12V_S0
(DUAL PACKAGE: SUPPLY PINS CONNECTED ON BOTTOM OF PAGE)

PP12V_S3
C7643 10UF 10% 25V X5R 1206-1
C7640 10UF 10% 25V X5R 1206-1
C7641 10UF 10% 25V X5R 1206-1
C7642 10UF 10% 25V X5R 1206-1
R7621 3.65K 1% 1/16W MF-LF 402
C7609 0.1UF 10% 16V X5R 402
3V3S3_SNS_N
3V3S3_SNS_P
R7629 47.5K 1% 1/16W MF-LF 402
C7631 0.1UF 10% 16V X5R 402
R7626 3.92K 1% 1/16W MF-LF 402
PP5VREG_INTVCC
CRITICAL D7624 CMDSH-3 SOD-323
C7624 0.1uF 10% 16V X5R 402
3V3S3_BOOST_R
R7624 0 5% 1/16W MF-LF 402
C7622 22PF 5% 50V CERM 402
CRITICAL Q7620 FDMS9620S MLP
CRITICAL L7620 1.5UH-12A MMD06E2Z-SM DCR=9 MOHM
D7600 CTLSH3-30M833 TLM833
NOSTUFF
NOSTUFF C7621 0.001UF 10% 50V CERM 402
3V3S3_TG
3V3S3_BOOST
3V3S3_SW
3V3S3_BG
TP_PP5VREG_PLLIN (INTERNAL PULLDOWN)
3V3S3_VOSNS
3V3S3_ITH
3V3S3_RUNSS
P5VREG_FCB
PP5V_S5
U7600 LTC3728LXC QFN
TG1 BOOST1 SW1 BG1 PLLIN SENSE1+ SENSE1- VOSENSE1 ITH1 RUN_SS1 FCB EXTVCC
C7605 1UF 10% 6.3V CERM 402
3V3S3_ITH_R
R7625 10K 1% 1/16W MF-LF 402
C7626 220PF 5% 25V CERM 402
C7625 0.001UF 10% 50V CERM 402
SGND THRML_PAD PGND
OMIT XW7600 SM
(3.34V NOMINAL)
CRITICAL C7652 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
C7650 22UF 20% 6.3V CERM 805
CRITICAL C7651 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
<Rc> R7627 63.4K 1% 1/16W MF-LF 402
C7629 180PF 5% 50V CERM 402
Vout = 0.8V * (1 + Rc / Rd)
<Rd> R7628 20.0K 1% 1/16W MF-LF 402
NOSTUFF C7628 0.001UF 10% 50V CERM 402
GND_PP5VREG_SGND
3.3V S3
M72778
POWER BUDGET
PEAK=6.06A
AVE=3.06A

PP12V_S5
PPVIN_S5_5VS5_R
R7600 10 1% 1/16W MF-LF 402
C7600 1UF 10% 16V X5R 603
R7670 1M 5% 1/16W MF-LF 402
CRITICAL C7682 150UF 20% 16V ELEC SM-1
C7681 10UF 10% 25V X5R 1206-1
C7680 10UF 10% 25V X5R 1206-1
C7662 22PF 5% 50V CERM 402
5VS5_SNS_N
5VS5_SNS_P
PP5VREG_INTVCC
CRITICAL D7664 CMDSH-3 SOD-323
5VS5_BOOST_R
R7664 0 5% 1/16W MF-LF 402
CRITICAL Q7660 FDMS8690-RJK0305DPB MLP5X6-LFPAK
C7664 0.1uF 10% 16V X5R 402
CRITICAL Q7661 NTMFS4108N MLP5X6-LFPAK-DFN
CRITICAL D7601 CTLSH3-30M833 TLM833
NOSTUFF C7661 0.0022UF 10% 50V CERM 402
5VS5_TG
5VS5_BOOST
5VS5_SW
5VS5_BG
P5VREG_FSEL
5VS5_VOSNS
5VS5_ITH
5VS5_RUNSS
(VERIFY WHETHER OK TO PULL THIS UP TO 12V)
PGOOD_3V3_S3
3_3VOUT NC
INTVCC NC1 NC2 NC3 NC4
C7689 220PF 5% 25V CERM 402
C7670 0.1uF 10% 16V X5R 402
C7665 0.001UF 10% 50V CERM 402
5VS5_ITH_R
R7665 20.0K 1% 1/16W MF-LF 402
C7666 100PF 5% 50V CERM 402
C7608 0.1UF 10% 16V X5R 402
R7661 3.65K 1% 1/16W MF-LF 402
R7669 7.68K 1% 1/16W MF-LF 402
C7632 0.1UF 10% 16V X5R 402
R7666 6.98K 1% 1/16W MF-LF 402
CRITICAL L7680 3.0UH-14.0A HM56-11123-TH DCR=8.61 MOHM
C7669 180PF 5% 50V CERM 402
<Ra> R7667 105K 1% 1/16W MF-LF 402
<Rb> R7668 20.0K 1% 1/16W MF-LF 402
NOSTUFF C7668 0.001UF 10% 50V CERM 402
Vout = 0.8V * (1 + Rc / Rd)
(5.0V NOMINAL)
C7690 22UF 20% 6.3V CERM 805
CRITICAL C7691 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
CRITICAL C7692 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
CRITICAL C7693 330UF-0.009OHM 20% 6.3V POLY CASE-D3L
PP5V_S5

5V S5
M72/M78
POWER BUDGET
M72 PEAK=12.0A
M72 AVE=6.83A
M78 PEAK=8.91A
M78 AVE=5.33A

PP12V_S5
PP5V_S5
R7631 11.8K 1% 1/16W MF-LF 402
C7612 0.1UF 20% 16V CERM 603
R7612 47K 5% 1/16W MF-LF 402
R7601 100K 1% 1/16W MF-LF 402
5VS3_COMP_REF
SPARE
R7602 0 5% 1/16W MF-LF 402
PP5V_S3
(4.46V/3.99V; 471MV HYSTERESIS)
5VS5_4V24_REF2
(REPEATED FOR EASE OF ROUTING)
U7601 LM393A SOI-1-LF
PGOOD_5V_S3_L
Q7603 2N7002 SOT23-LF
C7630 0.1UF 10% 16V X5R 402
R7630 86.6K 1% 1/16W MF-LF 402
C7613 0.1UF 20% 16V CERM 402
NOSTUFF
(HYSTERESIS)
(R7631: 71.5K; R7630: 40.2K; 300MV HYSTERESIS)
R7692 100K 5% 1/16W MF-LF 402

(CHANGE FCB IF WE DON'T MEET E*)
C7602 1UF 10% 6.3V CERM 402
C7601 4.7UF 20% 6.3V CERM 603
5V1V8REG_SKIP
R7606 0 5% 1/16W MF-LF 402
5V1V8REG_CONT
R7607 0 5% 1/16W MF-LF 402
C7607 0.01UF 10% 16V CERM 402
R7603 30.1K 1% 1/16W MF-LF 402
R7604 5.62K 1% 1/16W MF-LF 402
C7604 0.01UF 10% 16V CERM 402

5V S5 / 3.3V S3 SUPPLIES

SYNC_MASTER=MARK SYNC_DATE=N/A

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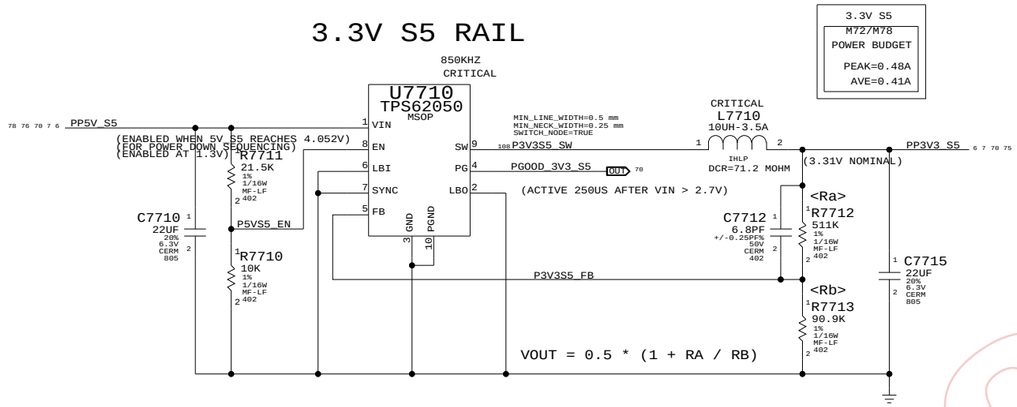
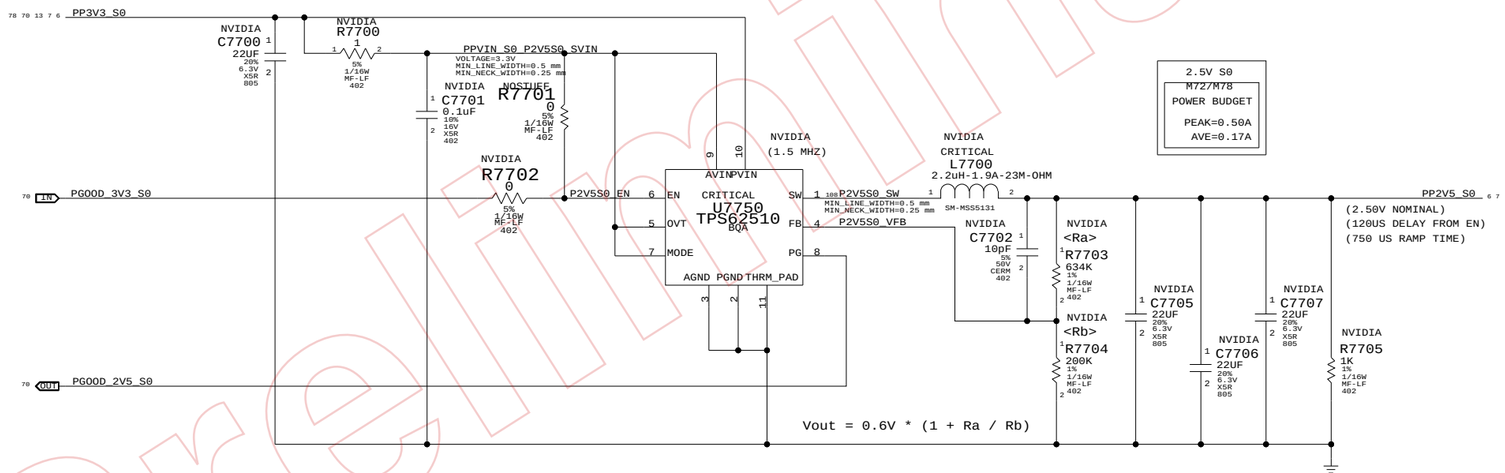
SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 76 OF 118	

3.3V S5 RAIL



2.5V S0 RAIL



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

3.3V / 2.5V POWER SUPPLIES

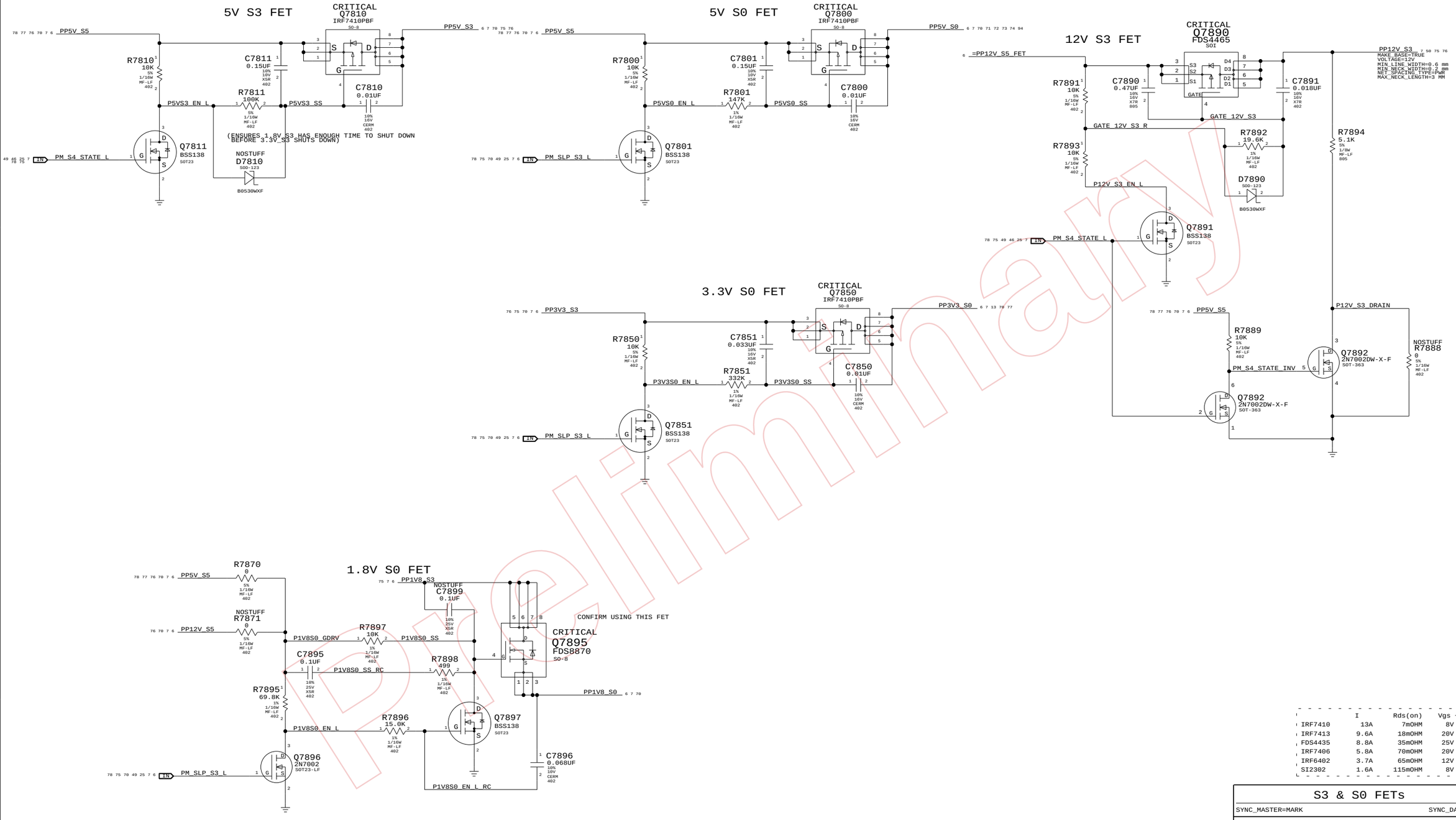
SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE

SHT 77 OF 118



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_MASTER=MARK SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 78 OF 118	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

APPLE P/N: 516S0562

J8400
AS0B52X-S43E-XF
E-RT-SM
(1 OF 2)
CRITICAL

6 =PP1V8_S0_MXM
C8401 22UF 20% 6.3V X5R 805
6 =PP5V_S0_MXM
70 50 49 7 ALL_SYS_PWRGD
PPV_S0_MXM_PWRSRC 53
VOLTAGE=12V MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM
C8400 22UF 20% 35V ELEC SM-LF

(FOR ROUTING EASE ON M72/M78
(POLARITY REVERSED FOR LANES 4,7,14)

PLACE CAPS NEAR NB

PRSNT2_L: RESERVED FOR FUTURE USE

2	1V8RUN0		PWR_SRC0	1					
4	1V8RUN1		PWR_SRC1	3					
6	1V8RUN2		PWR_SRC2	5					
8	1V8RUN3		PWR_SRC3	7					
10	1V8RUN4		PWR_SRC4	9					
12	1V8RUN5		PWR_SRC5	11					
14	1V8RUN6		PWR_SRC6	13					
16	RUNPWROK		PWR_SRC7	15					
18	5VRUN		GND0	17					
20	GND20		GND1	19					
22	GND21		GND2	21					
24	GND22		GND3	23					
		KEY							
38	PRSNT2_L		PEX_RX15_L	37	PEG_R2D_C_P<0>	C8420 0.1uF 16V 10% X5R 402	PEG_R2D_P<15>	PEG_D2R_N<0>	
40	PEX_TX15_L		PEX_RX15	39	PEG_R2D_C_N<0>	C8421 0.1uF	PEG_R2D_N<15>	PEG_D2R_P<0>	
42	PEX_TX15		GND4	41					
44	GND23		PEX_RX14_L	43	PEG_R2D_C_P<1>	C8422 0.1uF	PEG_R2D_P<14>	PEG_D2R_N<1>	
46	PEX_TX14_L		PEX_RX14	45	PEG_R2D_C_N<1>	C8423 0.1uF	PEG_R2D_N<14>	PEG_D2R_P<1>	
48	PEX_TX14		GND5	47					
50	GND24		PEX_RX13_L	49	PEG_R2D_C_P<2>	C8424 0.1uF	PEG_R2D_P<13>	PEG_D2R_N<2>	
52	PEX_TX13_L		PEX_RX13	51	PEG_R2D_C_N<2>	C8425 0.1uF	PEG_R2D_N<13>	PEG_D2R_P<2>	
54	PEX_TX13		GND6	53					
56	GND25		PEX_RX12_L	55	PEG_R2D_C_P<3>	C8426 0.1uF	PEG_R2D_P<12>	PEG_D2R_N<3>	
58	PEX_TX12_L		PEX_RX12	57	PEG_R2D_C_N<3>	C8427 0.1uF	PEG_R2D_N<12>	PEG_D2R_P<3>	
60	PEX_TX12		GND7	59					
62	GND26		PEX_RX11_L	61	PEG_R2D_C_N<4>	C8428 0.1uF	PEG_R2D_N<11>	PEG_D2R_P<4>	
64	PEX_TX11_L		PEX_RX11	63	PEG_R2D_C_P<4>	C8429 0.1uF	PEG_R2D_P<11>	PEG_D2R_N<4>	
66	PEX_TX11		GND8	65					
68	GND27		PEX_RX10_L	67	PEG_R2D_C_P<5>	C8430 0.1uF	PEG_R2D_P<10>	PEG_D2R_N<5>	
70	PEX_TX10_L		PEX_RX10	69	PEG_R2D_C_N<5>	C8431 0.1uF	PEG_R2D_N<10>	PEG_D2R_P<5>	
72	PEX_TX10		GND9	71					
74	GND28		PEX_RX9_L	73	PEG_R2D_C_P<6>	C8432 0.1uF	PEG_R2D_P<9>	PEG_D2R_N<6>	
76	PEX_TX9_L		PEX_RX9	75	PEG_R2D_C_N<6>	C8433 0.1uF	PEG_R2D_N<9>	PEG_D2R_P<6>	
78	PEX_TX9		GND10	77					
80	GND29		PEX_RX8_L	79	PEG_R2D_C_N<7>	C8434 0.1uF	PEG_R2D_N<8>	PEG_D2R_P<7>	7 15 101
82	PEX_TX8_L		PEX_RX8	81	PEG_R2D_C_P<7>	C8435 0.1uF	PEG_R2D_P<8>	PEG_D2R_N<7>	7 15 101
84	PEX_TX8		GND11	83					
86	GND30		PEX_RX7_L	85	PEG_R2D_C_P<8>	C8436 0.1uF	PEG_R2D_P<7>	PEG_D2R_N<8>	
88	PEX_TX7_L		PEX_RX7	87	PEG_R2D_C_N<8>	C8437 0.1uF	PEG_R2D_N<7>	PEG_D2R_P<8>	
90	PEX_TX7		GND12	89					
92	GND31		PEX_RX6_L	91	PEG_R2D_C_P<9>	C8438 0.1uF	PEG_R2D_P<6>	PEG_D2R_N<9>	
94	PEX_TX6_L		PEX_RX6	93	PEG_R2D_C_N<9>	C8439 0.1uF	PEG_R2D_N<6>	PEG_D2R_P<9>	
96	PEX_TX6		GND13	95					
98	GND32		PEX_RX5_L	97	PEG_R2D_C_P<10>	C8440 0.1uF	PEG_R2D_P<5>	PEG_D2R_N<10>	
100	PEX_TX5_L		PEX_RX5	99	PEG_R2D_C_N<10>	C8441 0.1uF	PEG_R2D_N<5>	PEG_D2R_P<10>	
102	PEX_TX5		GND14	101					
104	GND33		PEX_RX4_L	103	PEG_R2D_C_P<11>	C8442 0.1uF	PEG_R2D_P<4>	PEG_D2R_N<11>	
106	PEX_TX4_L		PEX_RX4	105	PEG_R2D_C_N<11>	C8443 0.1uF	PEG_R2D_N<4>	PEG_D2R_P<11>	
108	PEX_TX4		GND15	107					
110	GND34		PEX_RX3_L	109	PEG_R2D_C_P<12>	C8444 0.1uF	PEG_R2D_P<3>	PEG_D2R_N<12>	
112	PEX_TX3_L		PEX_RX3	111	PEG_R2D_C_N<12>	C8445 0.1uF	PEG_R2D_N<3>	PEG_D2R_P<12>	
114	PEX_TX3		GND16	113					
116	GND35		PEX_RX2_L	115	PEG_R2D_C_P<13>	C8446 0.1uF	PEG_R2D_P<2>	PEG_D2R_N<13>	
118	PEX_TX2_L		PEX_RX2	117	PEG_R2D_C_N<13>	C8447 0.1uF	PEG_R2D_N<2>	PEG_D2R_P<13>	
120	PEX_TX2		GND17	119					
122	GND36		PEX_RX1_L	121	PEG_R2D_C_N<14>	C8448 0.1uF	PEG_R2D_N<1>	PEG_D2R_P<14>	
124	PEX_TX1_L		PEX_RX1	123	PEG_R2D_C_P<14>	C8449 0.1uF	PEG_R2D_P<1>	PEG_D2R_N<14>	
126	PEX_TX1		GND18	125					
128	GND37		PEX_RX0_L	127	PEG_R2D_C_P<15>	C8450 0.1uF	PEG_R2D_P<0>	PEG_D2R_N<15>	
130	PEX_TX0_L		PEX_RX0	129	PEG_R2D_C_N<15>	C8451 0.1uF	PEG_R2D_N<0>	PEG_D2R_P<15>	
132	PEX_TX0		GND19	131					

(FOR ROUTING EASE ON M72/M78
(POLARITY REVERSED FOR LANES 0-2)

MXM PCI-E & PWR

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

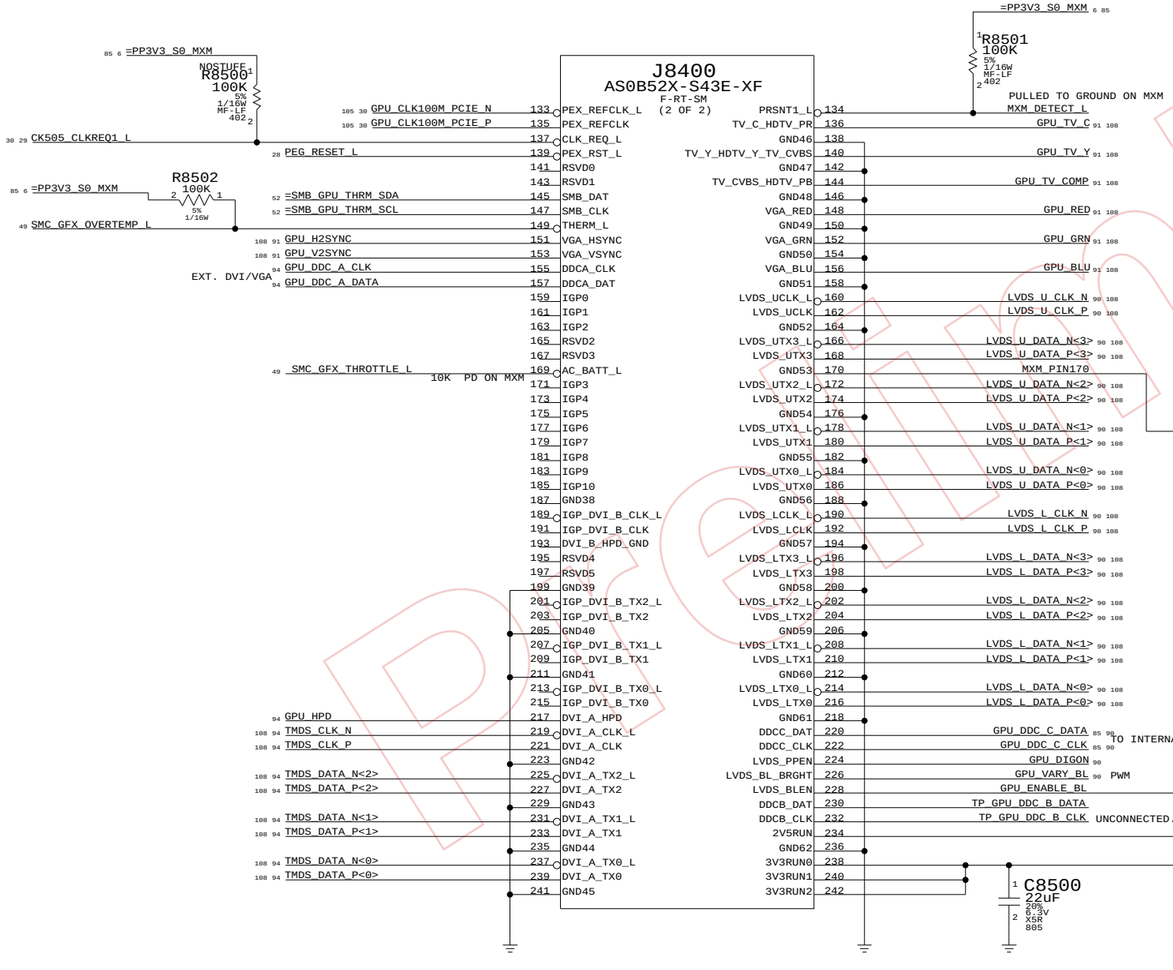
Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
24_INCH_LCD

MXM SPEC POWER REQUIREMENTS

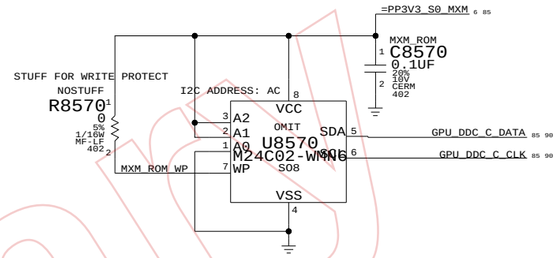
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



MXM I/O

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE: NONE	SHT 85 OF 118	

Page Notes

Power aliases required by this page:
- =PPV_S0_LCD_24INCH
- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
20_INCH_LCD, 24_INCH_LCD

94 91 6 =PP3V3_S0_VIDEO — I20 — =PP3V3_DDC_LCD 90

LCD (LVDS) INTERFACE

24_INCH_LCD
R9002 0 5% 1/8W MF-LF 805
6 =PPV_S0_LCD_24INCH

20_INCH_LCD
R9003 0 5% 1/8W MF-LF 805
6 =PPV_S0_LCD_20INCH

PANEL POWER SEQUENCING

PPV_S0_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

NOSTUFF
R9090 0 5% 1/8W MF-LF 805

C9000 0.1UF 10% 50V X7R 603-1
PLACE NEAR J9002

R9000 100K 5% 1/10W MF-LF 402

R9001 29.4K 1% 1/10W MF-LF 402

LCD_PWREN_L_RC

Q9000 SI3443DV TSOP-LF
PPV_LCD_SW
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9000 FERR-250-OHM SM
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

PPV_LCD_CONN 6 90
5V FOR 20 INCH LCD
12V FOR 24 INCH LCD

C9020 10UF 10% 16V X5R-CERM 1210

C9001 0.001uF 20% 50V CERM 402

LCD_PWREN_DIV

OMIT
R9099 100K 5% 1/10W MF-LF 402

LCD_PWREN_L

Q9001 2N7002 SOT23-LF
85 GPU_DIGON

R9070 100K 5% 1/10W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	RES,100K,5%,0402	R9099		24_INCH_LCD
116S0004	1	RES,0,5%,0402	R9099		20_INCH_LCD

CRITICAL
SDF9000
STDOFF-3MMOD4.6MMH-1.35-TH

516S0241
CRITICAL
J9002
53307-3052
F-ST-SM

108 85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0>	85 108
108 85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1>	85 108
108 85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2>	85 108
	7	8	LVDS_U_CLK_N	85 108
108 85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3>	85 108
108 85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0>	85 108
108 85 LVDS_L_DATA_P<0>	13	14		
108 85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1>	85 108
	17	18	LVDS_L_DATA_N<2>	85 108
108 85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N	85 108
108 85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3>	85 108
108 85 LVDS_L_DATA_P<3>	23	24		
85 GPU_DDC_C_CLK	25	26	GPU_DDC_C_DATA	85
	27	28		
	29	30		

90 =PP3V3_DDC_LCD
90 6 PPV_LCD_CONN
PPV_LCD_CONN 6 90

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9010 0.001uF 20% 50V CERM 402

CRITICAL
SDF9001
STDOFF-3MMOD4.6MMH-1.35-TH

INVERTER INTERFACE

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

85 GPU_VARY_BL
R9075 47 5% 1/10W MF-LF 402
LCD_PWM 6

NOSTUFF
R9074 10K 5% 1/10W MF-LF 402

INTERNAL DISPLAY CONNS

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE
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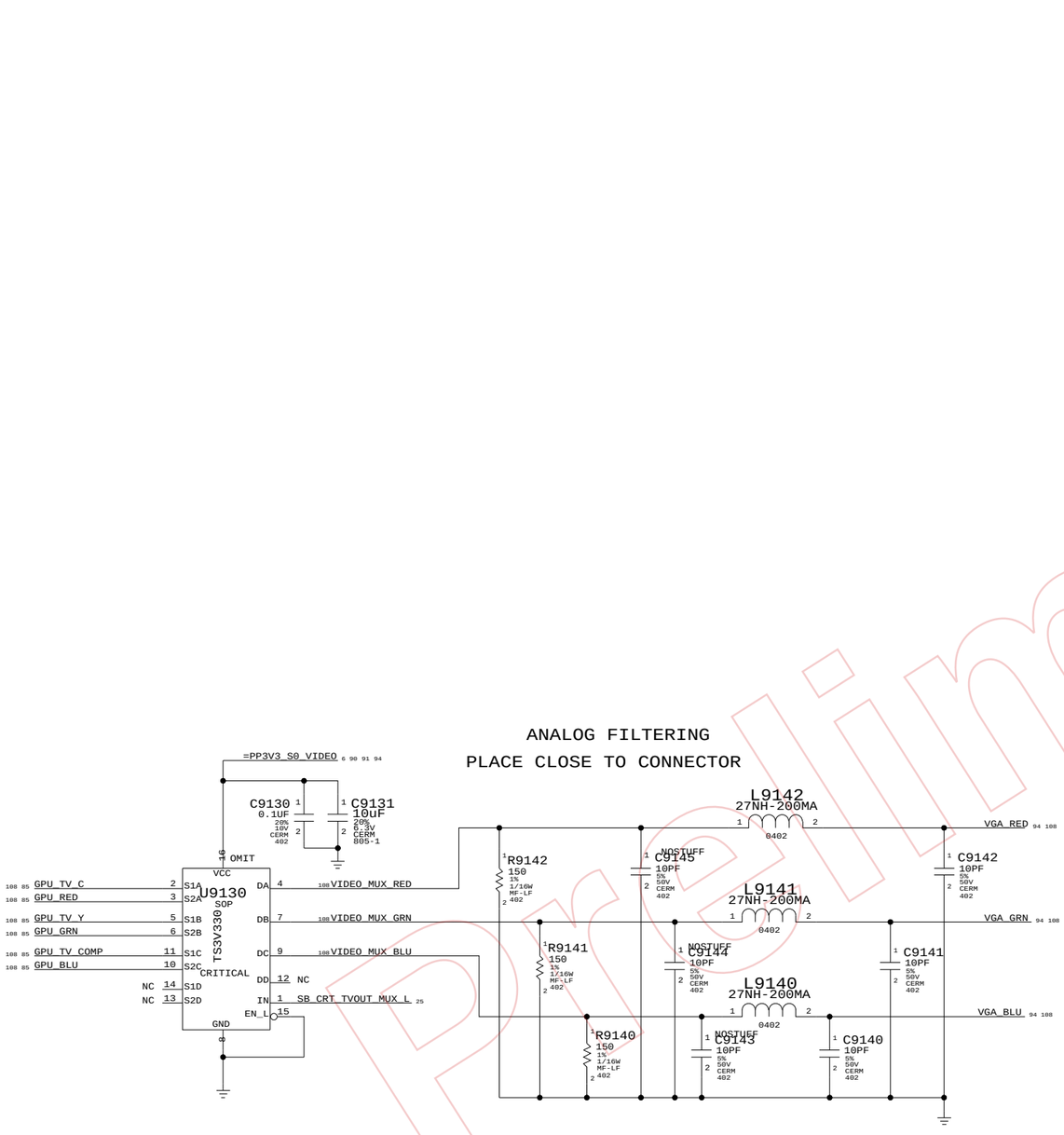
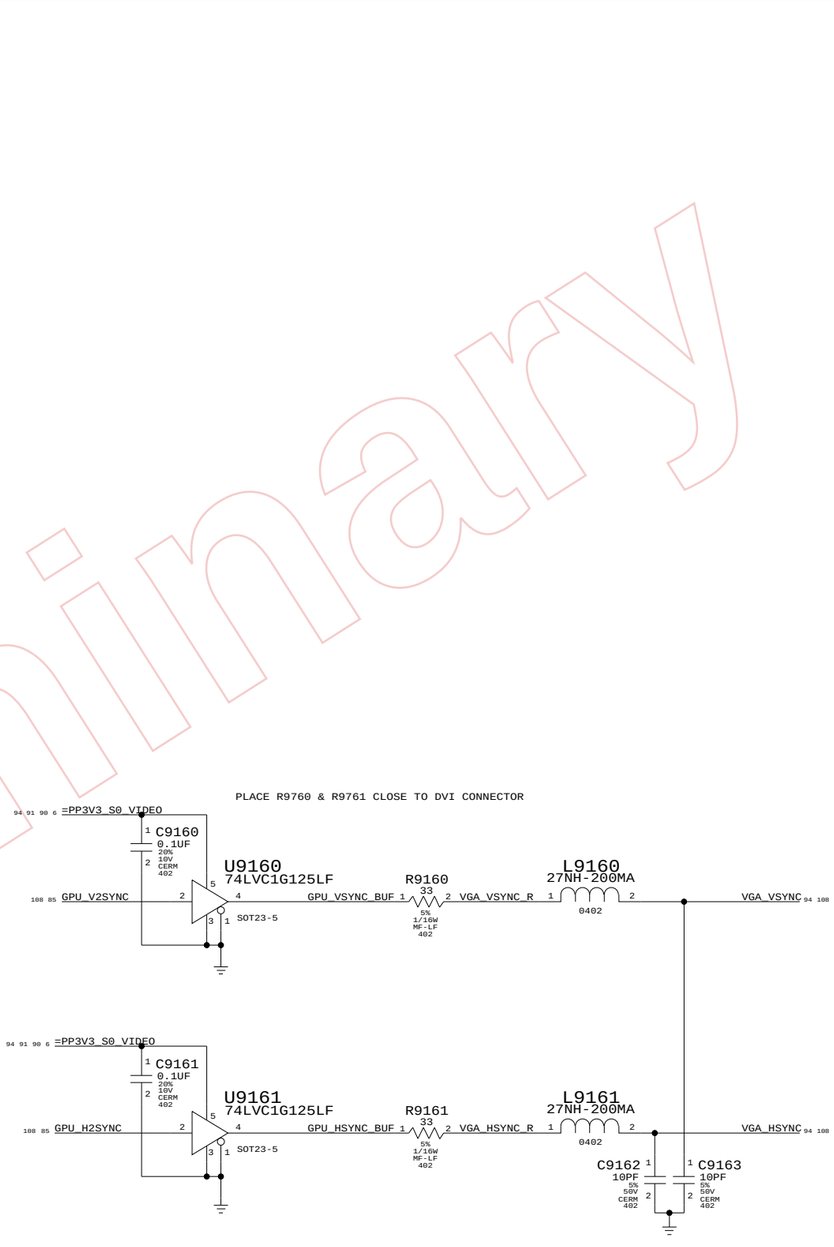
ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



VIDEO_MUX_SEL	OUT
1	CRT
0	TV

PLACE U9120 NEAR GMCH

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1700	1	QUAD SPDT HIGH-BANDWITDH VIDEO SWITCH,LOW ON-RES	U9130	CRITICAL	

Analog Video Support

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

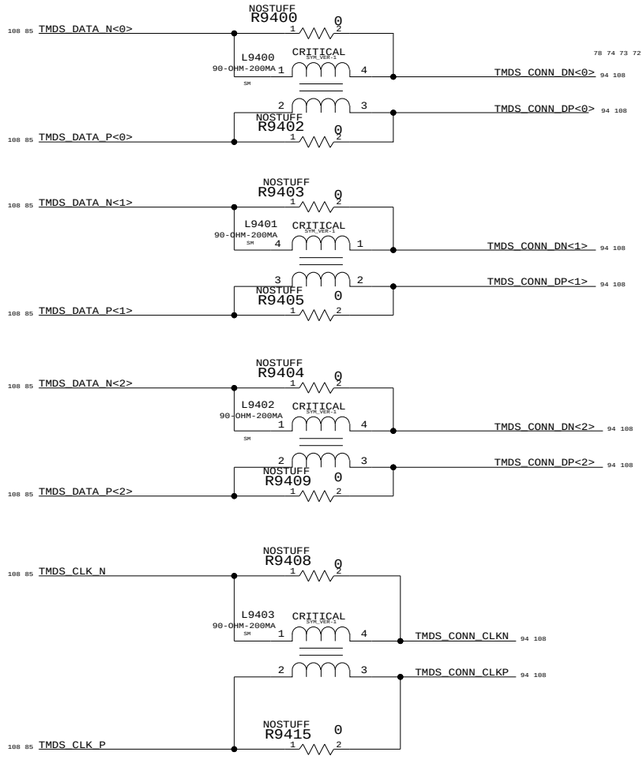
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33
SCALE NONE	SHT 91 OF 118	

DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR



DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

78 74 73 72 71 70 7 6 PP5V_S0 — D9410 SOD-123 B0530WXF — PP5V_S0_DDC_DIODE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — CRITICAL F9410 0.10A-15V 805 — PP5V_S0_DDC_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) — L9410 400-OHM-EMI SM-1 — PP5V_S0_DDC 94 (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

DON'T USE M51 SPECIFIC: 514S0129
APPLE PN: 514S0167

CRITICAL
J9410 MINI-DVI-M72 F-ST-SM

FOR IMAGE PLANE, THE SHELL PINS OF THE CONNECTOR ARE ALIASED DIRECTLY TO DIGITAL GROUND. IF CAPS ARE NECESSARY LATER, THEY SHOULD BE ADDED TO THE PAGE WHERE =GND_CHASSIS_DVI IS CONNECTED

PLACE CLOSE TO MINI-DVI CONNECTOR

3V LEVEL SHIFTERS

External Display Conns

SYNC_MASTER=M78_MLB SYNC_DATE=11/01/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE: NONE SHT 94 OF 118

CRITICAL
SDF9800
STDOFF-4.0OD3.5H-1.35-TH

CRITICAL
SDF9801
STDOFF-4.0OD3.5H-1.35-TH

APN 518S0502

CRITICAL
J9800
52893-2098
F-RT-SM

9 GND_AUDIO_SPKRAMP
C9800 1UF 16V 25% X7R 805
6 =PP12V_S0_AUDIO_SPKRAMP
98 6 =PP5V_S0_AUDIO
103 23 HDA_SDIN0
103 23 HDA_SDOUT
103 23 HDA_BIT_CLK
103 23 HDA_RST_L
103 23 HDA_SYNC
98 6 =PP3V3_S0_AUDIO

=PP5V_S0_AUDIO 6 98
=PP3V3_S0_AUDIO 6 98
NOSTUFF C9801 0.1UF 20% 10V CERM 402
NOSTUFF C9802 0.1UF 20% 10V CERM 402

CRITICAL
SDF9803
STDOFF-4.0OD3.5H-1.35-TH

CRITICAL
SDF9804
STDOFF-4.0OD3.5H-1.35-TH

STANDOFFS ARE 860-0893

MLB: AUDIO CONNECTOR

SYNC_MASTER=DEREK SYNC_DATE=4/23/2007

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

SCALE NONE SHT 98 OF 118

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FSB_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	*	*	SPACING_0.2MM
FSB_ADSTB	*	*	SPACING_0.3MM
FSB_DATA	*	*	SPACING_0.2MM
FSB_DSTB	*	*	SPACING_0.3MM
FSB_COMMON	*	*	SPACING_0.2MM

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_55S	*	55_OHM_SE
CPU_27P4S	*	27P4_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_2TO1	*	*	SPACING_0.2MM
CPU_COMP	*	*	SPACING_0.6MM
CPU_GTLREF	*	*	SPACING_0.6MM
CPU_ITP	*	*	SPACING_0.2MM
CPU_VCCSENSE	*	*	SPACING_0.6MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON_2PP	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..1>	10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_D_L<0>	7 10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..17>	10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_D_L<16>	7 10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..42>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_D_L<41>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<40..32>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..60>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_D_L<59>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<58..48>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..7>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<5..3>	10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_A_L<6>	7 10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..28>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<26..17>	10 14
FSB_ADDR_GROUP1_PP	FSB_55S	FSB_ADDR	FSB_A_L<27>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 50
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB_PP	CPU_55S		CPU_INTR	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_NMI	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_A20M_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	10 23
CPU_FROM_SB_PP	CPU_55S		CPU_IGNNE_L	7 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	7 10 23 51
CPU_FROM_SB_PP	CPU_55S		CPU_SMI_L	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 50
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	16 25 71
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	71
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	10 16 23 71
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 105
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 105
(FSB_CPURST_L)	CPU_55S	CPU_ITP	ITP_CPURST_L	
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	71

CPU/FSB Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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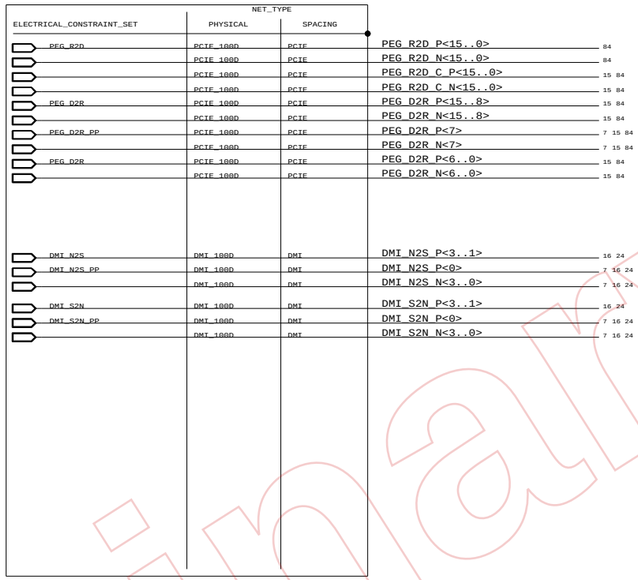
PCI-Express / DMI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_OHM_DIFF
DMI_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	SPACING_0.5MM
DMI	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5



Video Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	100_OHM_DIFF
CRT_55S	*	55_OHM_SE
CRT_50S	*	50_OHM_SE
TMDS_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
LVDS	*	*	SPACING_0.5MM	
CRT	*	*	SPACING_0.6MM	DG Says 40 mil spacing minimum
CRT	CRT	*	SPACING_0.5MM	
TVDAC				DG Says 30 mil spacing minimum
CRT_SYNC	*	*	SPACING_0.6MM	
CRT_SYNC	CRT_SYNC	*	SPACING_0.5MM	DG Says 40 mil spacing minimum
TMDS	*	*	SPACING_0.5MM	

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NB Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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DDR2 Memory Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_45S	*	45_OHM_SE
MEM_55S	*	55_OHM_SE
MEM_70D	*	70_OHM_DIFF
MEM_85D	*	85_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	SPACING_0.6MM
MEM_CMD	*	*	SPACING_0.15MM
MEM_CTRL	*	*	SPACING_0.6MM
MEM_DATA	*	*	SPACING_0.6MM
MEM_DQS	*	*	SPACING_0.6MM
MEM_CLK	MEM_CLK	*	SPACING_0.4MM
MEM_CLK	MEM_CTRL	*	SPACING_0.4MM
MEM_CLK	MEM_CMD	*	SPACING_0.4MM
MEM_CLK	MEM_DATA	*	SPACING_0.4MM
MEM_CLK	MEM_DQS	*	SPACING_0.4MM
MEM_CTRL	MEM_CTRL	*	SPACING_0.2MM
MEM_CTRL	MEM_CMD	*	SPACING_0.3MM
MEM_CTRL	MEM_DATA	*	SPACING_0.3MM
MEM_CTRL	MEM_DQS	*	SPACING_0.3MM
MEM_CMD	MEM_CMD	*	SPACING_0.15MM
MEM_CMD	MEM_DATA	*	SPACING_0.3MM
MEM_CMD	MEM_DQS	*	SPACING_0.3MM
MEM_DATA	MEM_DATA	*	SPACING_0.15MM
MEM_DATA	MEM_DQS	*	SPACING_0.3MM
MEM_DQS	MEM_DQS	*	SPACING_0.3MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<1..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<1..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<6..0>	17 31
MEM_A_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_A_DQ<7>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<13..8>	17 31
MEM_A_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_A_DQ<14>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15>	17 31
MEM_A_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_A_DQ<16>	7 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..17>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<24>	17 31
MEM_A_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_A_DQ<25>	7 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..26>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<38..32>	17 31
MEM_A_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_A_DQ<39>	7 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<46..40>	17 31
MEM_A_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_A_DQ<47>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<53..48>	17 31
MEM_A_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_A_DQ<54>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<58..56>	17 31
MEM_A_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_A_DQ<59>	7 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..60>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	7 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	7 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	7 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	7 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	7 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	7 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	7 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	7 17 31

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<4..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<4..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<5..0>	17 32
MEM_B_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_B_DQ<6>	7 17 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7>	17 32
MEM_B_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_B_DQ<8>	7 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..9>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<22..16>	17 32
MEM_B_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_B_DQ<23>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<24>	17 32
MEM_B_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_B_DQ<25>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..26>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<37..32>	17 32
MEM_B_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_B_DQ<38>	7 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<43..40>	17 32
MEM_B_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_B_DQ<44>	7 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..45>	17 32
MEM_B_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_B_DQ<48>	7 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..49>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<61..56>	17 32
MEM_B_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_B_DQ<62>	7 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	7 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	7 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	7 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	7 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	7 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	7 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	7 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	7 17 32

Memory Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE COMPUTER INC.

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D	051-7229	33

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Disk Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
IDE_55S	*	55_OHM_SE
SATA_55S	*	55_OHM_SE
SATA_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
IDE	*	*	SPACING_0.18MM
SATA	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HDA_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	SPACING_0.18MM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_60S	*	55_OHM_SE
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	SPACING_0.5MM

DG SAYS MINIMUM SPACING 50 MILS FROM USB TO CLOCKS

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_55S	*	55_OHM_SE
SPI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SPACING_0.3MM
SPI	*	*	SPACING_0.18MM

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..10>	23 44
IDE_PDD_PP	IDE_55S	IDE	IDE_PDD<9>	7 23 44
IDE_PDD	IDE_55S	IDE	IDE_PDD<8..0>	23 44
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 44
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	7 23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 44
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	7 23 44
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 44
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	24 44
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 45
	SATA_100D	SATA	SATA_A_R2D_C_N	23 45
	SATA_100D	SATA	SATA_A_R2D_P	45
	SATA_100D	SATA	SATA_A_R2D_N	45
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	7 23 45
	SATA_100D	SATA	SATA_A_D2R_N	7 23 45
	SATA_100D	SATA	SATA_A_D2R_C_P	45
	SATA_100D	SATA	SATA_A_D2R_C_N	45
	SATA_100D	SATA	SATA_B_R2D_C_P	23 45
	SATA_100D	SATA	SATA_B_R2D_C_N	23 45
	SATA_100D	SATA	SATA_B_D2R_P	23 45
	SATA_100D	SATA	SATA_B_D2R_N	23 45
SATA_RBIAS	SATA_55S		SATA_RBIAS	45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 98
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 98
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 98
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 98
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 98
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 46
	USB_90D	USB	USB_EXTA_N	24 46
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
	USB_90D	USB	USB_EXTD_P	24 46
	USB_90D	USB	USB_EXTD_N	24 46
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 47
	USB_90D	USB	USB_CAMERA_N	7 24 47
USB_BT	USB_90D	USB	USB_BT_P	7 24 47
	USB_90D	USB	USB_BT_N	7 24 47
	USB_90D	USB	USB_TPAD_P	24 47
	USB_90D	USB	USB_TPAD_N	24 47
USB_IR	USB_90D	USB	USB_IR_P	7 24 47
	USB_90D	USB	USB_IR_N	7 24 47
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 46
	USB_90D	USB	USB_EXTB_N	24 46
	USB_90D	USB	USB_EXCARD_P	24 47
	USB_90D	USB	USB_EXCARD_N	24 47
USB_EXTC	USB_90D	USB	USB_EXTC_P	24 46
	USB_90D	USB	USB_EXTC_N	24 46
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 52
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 52
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 52
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 52
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	24 61
	SPI_55S	SPI	SPI_SCLK	7 61
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 61
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	61
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	7 24 61
	SPI_55S	SPI	SPI_A_SO_R	7 61
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 61
	SPI_55S	SPI	SPI_CE_L<0>	7 61
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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PCI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	*	*	STANDARD

CHANGED TO 0.1MM SPACING AS THERE ARE NO PCI DEVICES

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLINK_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK	*	*	SPACING_0.18MM
CLINK_VREF	*	*	SPACING_0.3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_12MIL	*	=STANDARD	0.3 MM	0.125 MM	7.5 MM	=STANDARD	=STANDARD

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	*	SPACING_0.5MM
ENET_MDI	ENET_MDI_TERM	*	SPACING_0.2MM

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_AD<18..0>	24 28
	PCI_55S	PCI	PCI_AD<19>	24 28
	PCI_55S	PCI	PCI_AD<20>	24 28
	PCI_55S	PCI	PCI_AD<31..21>	24 28
	PCI_55S	PCI	PCI_PAR	24 28
	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 28
	PCI_55S	PCI	PCI_IRDY_L	24
	PCI_55S	PCI	PCI_DEVSEL_L	24
	PCI_55S	PCI	PCI_PERR_L	24
	PCI_55S	PCI	PCI_LOCK_L	24
	PCI_55S	PCI	PCI_SERR_L	24 28
	PCI_55S	PCI	PCI_STOP_L	24
	PCI_55S	PCI	PCI_TRDY_L	24
	PCI_55S	PCI	PCI_FRAME_L	24
	PCI_55S	PCI	PCI_FW_REQ_L	24
	PCI_55S	PCI	PCI_FW_GNT_L	24
	PCI_55S	PCI	PCI_REQ1_L	7 24
	PCI_55S	PCI	PCI_GNT1_L	
	PCI_55S	PCI	PCI_REQ2_L	7 24
	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	7 24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	7 24 34
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 37
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	7 24 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	7 24 37
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	40 42
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	40 42
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	7 40 42
	PCIE_100D	PCIE	PCIE_FW_D2R_N	7 40 42
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	7 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	7 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
I149		PWR	PP1V9R2V5_ENET_PHY_AVDD	37 39
I150		PWR	PP1V9R2V5_S3_ENET_R	38
I147		ENET_MDI_TERM	ENET_MDI0	37
I148		ENET_MDI_TERM	ENET_MDI1	37
I145		ENET_MDI_TERM	ENET_MDI2	37
I146		ENET_MDI_TERM	ENET_MDI3	37
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	37 39
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	37 39
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	37 39
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	37 39

SB Constraints (2 of 2)

SYNC_MASTER=(MASTER) SYNC_DATE=(10/02/2006)

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_FSB_100D	*	100_OHM_DIFF
CLK_PCIE_100D	*	100_OHM_DIFF
CLK_MED_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	*	*	CLK_SPACING_0.6MM
CLK_PCIE	*	*	CLK_SPACING_0.5MM
CLK_MED	*	*	CLK_SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 100
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 100
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 51
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	7 24 30
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	7 30 49
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	7 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	7 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	30 85
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	30 85
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	7 24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	7 24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	7 30 40
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	7 30 40
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	7 23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	7 23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 30 37
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 30 37

Clock Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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FireWire Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FW_110D	*	110_OHM_DIFF
FW_110D	BGA_P1MM	110_OHM_DIFF_ESCAPE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FW_TP	*	*	SPACING_0.3MM

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	43
	FW_110D	FW_TP	FW_PORT0_TPA_N	43
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	43
	FW_110D	FW_TP	FW_PORT0_TPB_N	43
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_N	43
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_N	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_N	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_N	43

Port 2 Not Used

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	52
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	52
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	52
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	52
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	52
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	52
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	52
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	52

FireWire & SMC Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	900
PWR	*	=STANDARD	900

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PWR	*	PWR_P2MM
MEM_CMD	PWR	*	PWR_P2MM
MEM_CTRL	PWR	*	PWR_P2MM
MEM_DATA	PWR	*	PWR_P2MM
MEM_DQS	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	PWR	*	PWR_P2MM
DMI	PWR	*	PWR_P2MM
SATA	PWR	*	PWR_P2MM
USB	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	PWR	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	SPACING_0.4MM
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
SMS	*	*	SPACING_0.3MM

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<3..0>	85 94
	TMDS_100D	TMDS	TMDS_DATA_N<3..0>	85 94
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	85 94
	TMDS_100D	TMDS	TMDS_CLK_N	85 94
	TMDS_100D	TMDS	TMDS_CONN_DP<3..0>	94
	TMDS_100D	TMDS	TMDS_CONN_DN<3..0>	94
	TMDS_100D	TMDS	TMDS_CONN_CLKP	94
	TMDS_100D	TMDS	TMDS_CONN_CLKN	94
(USB_EXTA)	USB_90D	USB	USB_PORT0_P	46
(USB_EXTA)	USB_90D	USB	USB_PORT0_N	46
(USB_EXTB)	USB_90D	USB	USB_PORT1_P	46
(USB_EXTB)	USB_90D	USB	USB_PORT1_N	46
(USB_EXTC)	USB_90D	USB	USB_PORT2_P	46
(USB_EXTC)	USB_90D	USB	USB_PORT2_N	46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_P	46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_N	46
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_P	47
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_N	47
(USB_IR)	USB_90D	USB	USB_IR_L_P	47 58
(USB_IR)	USB_90D	USB	USB_IR_L_N	47 58
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P	85 90
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_N	85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>	85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>	85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P	85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_N	85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>	85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>	85 90
	PCIE_100D	PCIE	PCIE_FW_R2D_N	7 40
	PCIE_100D	PCIE	PCIE_FW_R2D_P	7 40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_N	40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_P	40
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	7 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	7 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<0>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<0>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<1>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<1>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<2>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<2>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<3>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<3>	39
	ENET_100D	ENET_MDI	ENET_MDI_R_P<0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<1>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<1>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<2>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<2>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3>	
	CRT_50S	CRT	GPU_TV_COMP	85 91
	CRT_50S	CRT	GPU_TV_C	85 91
	CRT_50S	CRT	GPU_TV_Y	85 91
CRT_RED	CRT_50S	CRT	GPU_RED	85 91
CRT_GREEN	CRT_50S	CRT	GPU_GRN	85 91
CRT_BLUE	CRT_50S	CRT	GPU_BLU	85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_H2SYNC	85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_V2SYNC	85 91
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_HSYNC	91 94
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_VSYNC	91 94
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_HSYNC	
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_VSYNC	
	CRT_50S	CRT	VIDEO_MUX_RED	91
	CRT_50S	CRT	VIDEO_MUX_GRN	91
	CRT_50S	CRT	VIDEO_MUX_BLU	91
	CRT_55S	CRT	VGA_RED	91 94
	CRT_55S	CRT	VGA_GRN	91 94
	CRT_55S	CRT	VGA_BLU	91 94
THERM_DIFF	THERM_DIFF	THERMAL	HDD_THRMD_P	55
	THERM_DIFF	THERMAL	HDD_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	ODD_THRMD_P	55
	THERM_DIFF	THERMAL	ODD_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P	10 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	10 55
THERM_DIFF	THERM_DIFF	THERMAL	GPU_HSK_THRMD_P	55
	THERM_DIFF	THERMAL	GPU_HSK_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_HSK_THRMD_P	55
	THERM_DIFF	THERMAL	CPU_HSK_THRMD_N	55

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		SWITCHNODE	IMVP6_PHASE1	71
		SWITCHNODE	IMVP6_PHASE2	71
		SWITCHNODE	IMVP6_PHASE3	72
		SWITCHNODE	1V05REG_SWITCHNODE	73
		SWITCHNODE	1V5REG_SWITCHNODE	73
		SWITCHNODE	MCH_CORES0_SWITCHNODE	74
		SWITCHNODE	1V25REG_SWITCHNODE	74
		SWITCHNODE	1V8S3_PHASE	75
		SWITCHNODE	5VS5_SW	76
		SWITCHNODE	3V3S3_SW	76
		SWITCHNODE	P3V3S5_SW	77
		SWITCHNODE	P2V5S0_SW	77
		SMS	SMS_X_AXIS	49 50
		SMS	SMS_Y_AXIS	49 50
		SMS	SMS_Z_AXIS	49 50

M72/M78 SPECIFIC CONSTRAINTS

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

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M72/M78 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	4 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
DEFAULT	TOP,BOTTOM	Y	=55_OHM_SE	0.100 MM	3 MM	0 MM	0 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
55_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
40_OHM_SE	*	Y	0.185 MM	0.185 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
45_OHM_SE	*	Y	0.150 MM	0.150 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.340 MM	0.340 MM			
27P4_OHM_SE	*	Y	0.265 MM	0.265 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.180 MM	0.180 MM		0.120 MM	0.120 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.215 MM	0.215 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.120 MM	0.120 MM		0.130 MM	0.130 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.175 MM	0.175 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.095 MM	0.095 MM		0.205 MM	0.205 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.280 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF_ESCAPE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF_ESCAPE	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.250 MM	0.250 MM
110_OHM_DIFF_ESCAPE	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.15 MM	0.15 MM			
50_OHM_SE	*	Y	0.120 MM	0.120 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPACING_0.15MM	*	0.15 MM	?
SPACING_0.18MM	*	0.18 MM	?
SPACING_0.2MM	*	0.2 MM	?
SPACING_0.25MM	*	0.25 MM	?
SPACING_0.3MM	*	0.3 MM	?
SPACING_0.4MM	*	0.4 MM	?
SPACING_0.5MM	*	0.5 MM	?
SPACING_0.6MM	*	0.6 MM	?
SWITCHNODE	*	0.6 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_MED	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
CLK_SPACING_0.5MM	TOP,BOTTOM	0.2 MM	?
CLK_SPACING_0.6MM	TOP,BOTTOM	0.2 MM	?

M72/M78 RULE DEFINITIONS

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7229	33

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Title: Basenet Report
Design: m78
Date: May 7 18:11:37 2007

Base nets and synonyms for m78_lib.M78(@m78_lib.m78(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
0V9S0_COMP_REF	0V9S0_COMP_REF - @m78_lib.M78	70C6
1V05REG_BOOT	1V05REG_BOOT - @m78_lib.M78	73C4
1V05REG_BOOT_R	1V05REG_BOOT_R - @m78_lib.M78	73C3
1V05REG_ISEN	1V05REG_ISEN - @m78_lib.M78	73C4
1V05REG_LGATE	1V05REG_LGATE - @m78_lib.M78	73C3
1V05REG_OCSET	1V05REG_OCSET - @m78_lib.M78	73B4
1V05REG_SNUBBER_R	1V05REG_SNUBBER_R - @m78_lib.M78	73C2
1V05REG_SOFT	1V05REG_SOFT - @m78_lib.M78	73C4
1V05REG_SWITCHNODE	1V05REG_SWITCHNODE - @m78_lib.M78	73B3 108D1
1V05REG_UGATE	1V05REG_UGATE - @m78_lib.M78	73C4
1V05REG_VSEN	1V05REG_VSEN - @m78_lib.M78	73B3
1V05S0_EN	1V05S0_EN - @m78_lib.M78	73B4
1V05S0_RUNSS	1V05S0_RUNSS - @m78_lib.M78	70C5 73C3 74C3
1V05S0_RUNSS_BUF	1V05S0_RUNSS_BUF - @m78_lib.M78	70C6
1V5REG_BOOT	1V5REG_BOOT - @m78_lib.M78	73C5
1V5REG_BOOT_R	1V5REG_BOOT_R - @m78_lib.M78	73C6
1V5REG_ISEN	1V5REG_ISEN - @m78_lib.M78	73C5
1V5REG_LGATE	1V5REG_LGATE - @m78_lib.M78	73C5
1V5REG_OCSET	1V5REG_OCSET - @m78_lib.M78	73B5
1V5REG_SNUBBER_R	1V5REG_SNUBBER_R - @m78_lib.M78	73B7
1V5REG_SOFT	1V5REG_SOFT - @m78_lib.M78	73C5
1V5REG_SWITCHNODE	1V5REG_SWITCHNODE - @m78_lib.M78	73C6 108D1
1V5REG_UGATE	1V5REG_UGATE - @m78_lib.M78	73C5
1V5REG_VSEN	1V5REG_VSEN - @m78_lib.M78	73B7
1V5S0_RUNSS	1V5S0_RUNSS - @m78_lib.M78	70A5 73C5
1V5S0_RUNSS_BUF	1V5S0_RUNSS_BUF - @m78_lib.M78	70A6
1V8S0_COMP_REF	1V8S0_COMP_REF - @m78_lib.M78	70D6
1V8S3_BOOT	1V8S3_BOOT - @m78_lib.M78	75C5
1V8S3_BOOT_RC	1V8S3_BOOT_RC - @m78_lib.M78	75D5
1V8S3_COMP	1V8S3_COMP - @m78_lib.M78	75C6
1V8S3_COMP_R	1V8S3_COMP_R - @m78_lib.M78	75C6
1V8S3_EN	1V8S3_EN - @m78_lib.M78	75C6
1V8S3_FB	1V8S3_FB - @m78_lib.M78	75C6
1V8S3_FCCM	1V8S3_FCCM - @m78_lib.M78	75C6
1V8S3_FSET	1V8S3_FSET - @m78_lib.M78	75C6
1V8S3_ISEN	1V8S3_ISEN - @m78_lib.M78	75C5
1V8S3_LG	1V8S3_LG - @m78_lib.M78	75C5
1V8S3_PHASE	1V8S3_PHASE - @m78_lib.M78	75C5 108D1
1V8S3_SNUBBER_R	1V8S3_SNUBBER_R - @m78_lib.M78	75C3
1V8S3_UG	1V8S3_UG - @m78_lib.M78	75C5
1V8S3_VCC	1V8S3_VCC - @m78_lib.M78	75D6
1V25REG_BOOT	1V25REG_BOOT - @m78_lib.M78	74C5
1V25REG_BOOT_R	1V25REG_BOOT_R - @m78_lib.M78	74C6
1V25REG_ISEN	1V25REG_ISEN - @m78_lib.M78	74C5
1V25REG_LGATE	1V25REG_LGATE - @m78_lib.M78	74C5
1V25REG_OCSET	1V25REG_OCSET - @m78_lib.M78	74B5
1V25REG_SNUBBER_R	1V25REG_SNUBBER_R - @m78_lib.M78	74B7
1V25REG_SOFT	1V25REG_SOFT - @m78_lib.M78	74C5
1V25REG_SWITCHNODE	1V25REG_SWITCHNODE - @m78_lib.M78	74C6 108D1
1V25REG_UGATE	1V25REG_UGATE - @m78_lib.M78	74C5
1V25REG_VSEN	1V25REG_VSEN - @m78_lib.M78	74B7
1V25S0_RUNSS	1V25S0_RUNSS - @m78_lib.M78	70B5 74C5
1V25S0_RUNSS_BUF	1V25S0_RUNSS_BUF - @m78_lib.M78	70B6
3V3S0_COMP_REF	3V3S0_COMP_REF - @m78_lib.M78	70D6
3V3S3_BG	3V3S3_BG - @m78_lib.M78	76B5
3V3S3_BOOST	3V3S3_BOOST - @m78_lib.M78	76B5
3V3S3_BOOST_R	3V3S3_BOOST_R - @m78_lib.M78	76C6
3V3S3_ITH	3V3S3_ITH - @m78_lib.M78	76B5
3V3S3_ITH_R	3V3S3_ITH_R - @m78_lib.M78	76B6
3V3S3_RUNSS	3V3S3_RUNSS - @m78_lib.M78	76B5
3V3S3_SNS_N	3V3S3_SNS_N - @m78_lib.M78	76C6
3V3S3_SNS_P	3V3S3_SNS_P - @m78_lib.M78	76C6
3V3S3_SW	3V3S3_SW - @m78_lib.M78	76B5 108D1
3V3S3_TG	3V3S3_TG - @m78_lib.M78	76C5
3V3S3_VOSNS	3V3S3_VOSNS - @m78_lib.M78	76B5
5VS0_COMP_REF	5VS0_COMP_REF - @m78_lib.M78	70C6
5VS3_COMP_REF	5VS3_COMP_REF - @m78_lib.M78	76A7
5VS5_0V76_REF	5VS5_0V76_REF - @m78_lib.M78	70C6
5VS5_1V53_REF	5VS5_1V53_REF - @m78_lib.M78	70D6
5VS5_2V80_REF	5VS5_2V80_REF - @m78_lib.M78	70D6
5VS5_4V24_REF1	5VS5_4V24_REF1 - @m78_lib.M78	70D6
5VS5_4V24_REF2	5VS5_4V24_REF2 - @m78_lib.M78	76A7
5VS5_4V29_REF	5VS5_4V29_REF - @m78_lib.M78	76D7
5VS5_BG	5VS5_BG - @m78_lib.M78	76B4
5VS5_BOOST	5VS5_BOOST - @m78_lib.M78	76B4
5VS5_BOOST_R	5VS5_BOOST_R - @m78_lib.M78	76C3
5VS5_ITH	5VS5_ITH - @m78_lib.M78	76B4
5VS5_ITH_R	5VS5_ITH_R - @m78_lib.M78	76B3
5VS5_RUNSS	5VS5_RUNSS - @m78_lib.M78	76B4
5VS5_SNS_N	5VS5_SNS_N - @m78_lib.M78	76C3
5VS5_SNS_P	5VS5_SNS_P - @m78_lib.M78	76C3
5VS5_SW	5VS5_SW - @m78_lib.M78	76B4 108D1
5VS5_TG	5VS5_TG - @m78_lib.M78	76C4
5VS5_VOSNS	5VS5_VOSNS - @m78_lib.M78	76B4
12VS0_6V0_REF	12VS0_6V0_REF - @m78_lib.M78	76D7
12VS0_COMP_REF	12VS0_COMP_REF - @m78_lib.M78	76D7
=ENET_CLKREQ_L	=ENET_CLKREQ_L - @m78_lib.M78	37B8 38D1
	ENET_CLKREQ_R_L - @m78_lib.M78	38D1
=ENET_VMAIN_AVLBL	=ENET_VMAIN_AVLBL - @m78_lib.M78	37C2 38A3
	PP3V3_S0 - @m78_lib.M78	6B8 6C6 6D7 7C5 7D3 13D6 70C3 70D3 70D8 77C6 78C3
	=PP3V3_DDC_LCD - @m78_lib.M78	90A8 90D5
	=PP3V3_S0_VIDEO - @m78_lib.M78	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_NB_VCCA_PEG_BG - @m78_lib.M78	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @m78_lib.M78	6A4 21C2
	=PP3V3_S0_TSENS - @m78_lib.M78	6A4 55B5 55D5 55D6 55D8
	=PP3V3_S0_SMC - @m78_lib.M78	6A4 53C2
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @m78_lib.M78	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @m78_lib.M78	6A4 26A3 27D4
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @m78_lib.M78	6B4 26C3
	=PP3V3R1V5_S0_SB_VCCHDA - @m78_lib.M78	6B4 26B3 27B4
	=PP3V3_S0_SB_VCC3_3_DMI - @m78_lib.M78	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_SATA - @m78_lib.M78	6B4 26C3 27C4
	=PP3V3_S0MWOL_SB_CLINK0 - @m78_lib.M78	6B4 25C1
	=PP3V3_S0M_CK505 - @m78_lib.M78	6B4 29D2 29D8 30D1
	=PP3V3_S0_SATALED - @m78_lib.M78	6B4 45C2
	=PP3V3_S0_MXM - @m78_lib.M78	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_CK505 - @m78_lib.M78	6B4 29C7 30D7
	=PP3V3_S0_SMBUS_SMC_B_S0 - @m78_lib.M78	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_MGMT - @m78_lib.M78	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_0_S0 - @m78_lib.M78	6B4 52D5
	=PP3V3_S0_SMC_LS - @m78_lib.M78	6B4 50D2
	=PP3V3_S0_LPCPLUS - @m78_lib.M78	6B4 51C4
	=PP3V3_S0_SMBUS_SB - @m78_lib.M78	6B4 52D8
	=PP3V3_S0_IMVP - @m78_lib.M78	6B4 71D8
	=PP3V3_S0_AUDIO - @m78_lib.M78	6B4 98C4 98C6
	=PPSPD_S0_MEM - @m78_lib.M78	6B4 31A7 32A3 32A7
	=PP3V3_S0_FAN - @m78_lib.M78	6B4 56B7 56C7 57C7
	=PP3V3_S0_SB_PM - @m78_lib.M78	6B4 28A7
	=PP3V3_S0_PATA - @m78_lib.M78	6B4 44C6
	=PP3V3_S0_SB_PCI - @m78_lib.M78	6B4 24A3
	=PP3V3_S0_SB_VCC3_3_IDE - @m78_lib.M78	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_PCI - @m78_lib.M78	6B4 26B3 27C4
	=PP3V3_S0_SB_GPIO - @m78_lib.M78	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @m78_lib.M78	6B4 26A6
	=PP3V3_S0_SB - @m78_lib.M78	6C4 27D8
	=PP3V3_S0_NB_VCCHV - @m78_lib.M78	6C4 16B7 16C7 16C7 19B3 21A8
	PP3V3_S0 - @m78_lib.M78	6B8 6C6 6D7 7C5 7D3 13D6 70C3 70D3 70D8 77C6 78C3
	=PPSPD_S0_MEM - @m78_lib.M78	6B4 31A7 32A3 32A7
	=PP3V3_S0_VIDEO - @m78_lib.M78	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_TSENS - @m78_lib.M78	6A4 55B5 55D5 55D6 55D8
	=PP3V3_S0_SMC_LS - @m78_lib.M78	6B4 50D2
	=PP3V3_S0_SMC - @m78_lib.M78	6A4 53C2
	=PP3V3_S0_SMBUS_SMC_MGMT - @m78_lib.M78	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_B_S0 - @m78_lib.M78	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_0_S0 - @m78_lib.M78	6B4 52D5
	=PP3V3_S0_SMBUS_SB - @m78_lib.M78	6B4 52D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @m78_lib.M78	6B4 26A6
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @m78_lib.M78	6B4 26C3
	=PP3V3_S0_SB_VCC3_3_SATA - @m78_lib.M78	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_PCI - @m78_lib.M78	6B4 26B3 27C4
	=PP3V3_S0_SB_VCC3_3_IDE - @m78_lib.M78	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_DMI - @m78_lib.M78	6B4 26C3 27C4
	=PP3V3_S0_SB_PM - @m78_lib.M78	6B4 28A7
	=PP3V3_S0_SB_PCI - @m78_lib.M78	6B4 24A3
	=PP3V3_S0_SB_GPIO - @m78_lib.M78	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB - @m78_lib.M78	6C4 27D8
	=PP3V3_S0_SATALED - @m78_lib.M78	6B4 45C2
	=PP3V3_S0_PATA - @m78_lib.M78	6B4 44C6
	=PP3V3_S0_NB_VCCHV - @m78_lib.M78	6C4 16B7 16C7 16C7 19B3 21A8
	=PP3V3_S0_NB_VCCA_PEG_BG - @m78_lib.M78	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @m78_lib.M78	6A4 21C2
	=PP3V3_S0_MXM - @m78_lib.M78	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_LPCPLUS - @m78_lib.M78	6B4 51C4
	=PP3V3_S0_IMVP - @m78_lib.M78	6B4 71D8
	=PP3V3_S0_FAN - @m78_lib.M78	6B4 56B7 56C7 57C7
	=PP3V3_S0_ENET - @m78_lib.M78	6A4 38A1
	=PP3V3_S0_CK505 - @m78_lib.M78	6B4 29C7 30D7
	=PP3V3_S0_AUDIO - @m78_lib.M78	6B4 98C4 98C6
	=PP3V3_S0M_CK505 - @m78_lib.M78	6B4 29D2 29D8 30D1
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @m78_lib.M78	6A4 26A3 27D4
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @m78_lib.M78	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_CLINK0 - @m78_lib.M78	6B4 25C1
	=PP3V3R1V5_S0_SB_VCCHDA - @m78_lib.M78	6B4 26B3 27B4
=GFX_VR_EN	=GFX_VR_EN - @m78_lib.M78	16B3 22A8
	TP_GFX_VR_EN - @m78_lib.M78	22A7
=GND_NB_VSSA_LVDS	=GND_NB_VSSA_LVDS - @m78_lib.M78	19C6 22C1
	TP_NB_VSSA_LVDS - @m78_lib.M78	22C2
=NB_CLINK_MPWROK	=NB_CLINK_MPWROK - @m78_lib.M78	16A3 22C2
	VR_PWRGOOD_DELAY - @m78_lib.M78	7C4 7C7 16B6 22C1 70C2 71C7
=PP0V9_S0M_MEM_TERM	=PP0V9_S0M_MEM_TERM - @m78_lib.M78	6D4 33D5
	PP0V9_S0 - @m78_lib.M78	6D6 7D3 70C8 75A3
=PP0V9_S3M_MEM_NBVREFA	=PP0V9_S3M_MEM_NBVREFA - @m78_lib.M78	7C7 16C2 22B1
	PP0V9_S3M_MEM_NBVREFA - @m78_lib.M78	22B2
=PP0V9_S3M_MEM_NBVREFB	=PP0V9_S3M_MEM_NBVREFB - @m78_lib.M78	7C7 16C2 22A1
	PP0V9_S3M_MEM_NBVREFB - @m78_lib.M78	22A2
=PP0V9_S3_MEM_A_VREF	=PP0V9_S3_MEM_A_VREF - @m78_lib.M78	31C1 31D6
	PP0V9_S3_MEM_A_VREF - @m78_lib.M78	31C2
=PP0V9_S3_MEM_B_VREF	=PP0V9_S3_MEM_B_VREF - @m78_lib.M78	32C1 32D7
	PP0V9_S3_MEM_B_VREF - @m78_lib.M78	32C2
=PP1V2_ENET_PHY	=PP1V2_ENET_PHY - @m78_lib.M78	37D6 38A3
	PP1V2_S3_ENET - @m78_lib.M78	38A3
=PP1V05_S0M_NB_VCCAXM	=PP1V05_S0M_NB_VCCAXM - @m78_lib.M78	6C4 18B3 18C1 21D8
	=PP1V05_S0_NB_FOLLOW - @m78_lib.M78	6C4 21C4
	=PPVCORE_S0_SB - @m78_lib.M78	6C4 26D3 27B1
	PP1V05_S0 - @m78_lib.M78	6C6 7D3 34C3 73A4 73C1
	=PP1V05_S0_NB_PCIE - @m78_lib.M78	6C4 21D5
	PP1V05_S0 - @m78_lib.M78	6C6 7D3 34C3 73A4 73C1
	=PPVCORE_S0_SB - @m78_lib.M78	6C4 26D3 27B1
	=PP1V05_S0_NB_PCIE - @m78_lib.M78	6C4 21D5
	=PP1V05_S0_NB_FOLLOW - @m78_lib.M78	6C4 21C4
=PP1V05_S0_CPU	=PP1V05_S0_CPU - @m78_lib.M78	6D4 10B5 10B6 10C5 10D5 11C6 12A3 13D6 50D2
	=PP1V05_S0_SB_CPU_IO - @m78_lib.M78	6C4 23D2 26C3 27B2
	=PPVCORE_S0_NB_FOLLOW - @m78_lib.M78	6D4 21B4
	PPMCH_CORE_S0 - @m78_lib.M78	6D6 7D3 55A6 73A2 74C1
	=PP1V25R1V05_S0_NB_VTT - @m78_lib.M78	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @m78_lib.M78	6D4 14B7 30B8 30C8 30C8
	=PPVCORE_S0_NB - @m78_lib.M78	6D4 18D3 18D7 21D8
	PPMCH_CORE_S0 - @m78_lib.M78	6D6 7D3 55A6 73A2 74C1
	=PPVCORE_S0_NB_FOLLOW - @m78_lib.M78	6D4 21B4
	=PPVCORE_S0_NB - @m78_lib.M78	6D4 18D3 18D7 21D8
	=PP1V25R1V05_S0_NB_VTT - @m78_lib.M78	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @m78_lib.M78	6D4 14B7 30B8 30C8 30C8
	=PP1V05_S0_SB_CPU_IO - @m78_lib.M78	6C4 23D2 26C3 27B2
=PP1V5_S0_CPU	=PP1V5_S0_CPU - @m78_lib.M78	6C4 11B6 12B3
	=PP1V5_S0_MINI - @m78_lib.M78	6C4 34C2
	PP1V5_S0 - @m78_lib.M78	6C6 7D3 73C8
	=PP1V5_S0_SB - @m78_lib.M78	6C4 27C8
	PP1V5_S0_SB_VCCGLANPLL - @m78_lib.M78	26A6 27B6
	=PP1V5_S0_SB_VCC1_5_A - @m78_lib.M78	6C4 26B6
	=PP1V5_S0_SB_VCCUSBPLL - @m78_lib.M78	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m78_lib.M78	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m78_lib.M78	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m78_lib.M78	6C4 26B6 27D2
	=PP1V5_S0_NB_TVDAC - @m78_lib.M78	6C4 22B3
	PP1V5_S0 - @m78_lib.M78	6C6 7D3 73C8
	=PP1V5_S0_SB_VCCUSBPLL - @m78_lib.M78	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m78_lib.M78	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m78_lib.M78	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m78_lib.M78	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A - @m78_lib.M78	6C4 26B6
	=PP1V5_S0_SB - @m78_lib.M78	6C4 27C8
	=PP1V5_S0_NB_TVDAC - @m78_lib.M78	6C4 22B3
	=PP1V5_S0_MINI - @m78_lib.M78	6C4 34C2
=PP1V5_S0_SB_VCCGLAN1_5	=PP1V5_S0_SB_VCCGLAN1_5 - @m78_lib.M78	26A6 27B6
	PP1V5_S0_SB_VCC1_5_B - @m78_lib.M78	23D7 24C2 26D6 27C6
=PP1V8_S0_MXM	=PP1V8_S0_MXM - @m78_lib.M78	6D4 84C7
	PP1V8_S0 - @m78_lib.M78	6D6 7D3 70D8 78A5
=PP1V8_S3M_MEM_NB	=PP1V8_S3M_MEM_NB - @m78_lib.M78	6D3 16D2 18D7 21C8 22B3
	=PP1V8_S3M_NB_VCC - @m78_lib.M78	6D3 21A4
	=PP1V8_S3_ENET - @m78_lib.M78	6D3 38B8
	PP1V8_S3 - @m78_lib.M78	6D4 7D3 75B3 75C1 78B6
	=PP1V8_S3_MEMVTT - @m78_lib.M78	6D3 75B6
	=PP1V8_S3_MEM - @m78_lib.M78	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	PP1V8_S3 - @m78_lib.M78	6D4 7D3 75B3 75C1 78B6
	=PP1V8_S3_MEMVTT - @m78_lib.M78	6D3 75B6
	=PP1V8_S3_MEM - @m78_lib.M78	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	=PP1V8_S3_ENET - @m78_lib.M78	6D3 38B8
	=PP1V8_S3M_NB_VCC - @m78_lib.M78	6D3 21A4
=PP1V9R2V5_ENET_PHY	=PP1V9R2V5_ENET_PHY - @m78_lib.M78	37D7 38C1
	PP1V9R2V5_S3_ENET - @m78_lib.M78	38C3 38C4
=PP1V25_S0M_NB_PLL	=PP1V25_S0M_NB_PLL - @m78_lib.M78	6C4 21D3
	=PP1V25_S0M_NB_VCCD_HPLL - @m78_lib.M78	19A6 21D1
	=PP1V25_S0_SB_DMI - @m78_lib.M78	6C4 26C3 27C1
	PP1V25_S0 - @m78_lib.M78	6C6 7D3 74C8
	=PP1V25_S0_NB_VCC - @m78_lib.M78	6C4 21D5
	=PP1V25_S0_NB_PLL - @m78_lib.M78	6C4 21B4
	=PP1V25_S0M_NB_VCC - @m78_lib.M78	6C4 21A8
	=PP1V25_S0M_NB_VCCA - @m78_lib.M78	6C4 21B8
	=PP1V25_S0_NB_VCCDMI - @m78_lib.M78	6C4 19C3 21A8
	PP1V25_S0 - @m78_lib.M78	6C6 7D3 74C8
	=PP1V25_S0_SB_DMI - @m78_lib.M78	6C4 26C3 27C1
	=PP1V25_S0_NB_VCCDMI - @m78_lib.M78	6C4 19C3 21A8
	=PP1V25_S0_NB_VCC - @m78_lib.M78	6C4 21D5
	=PP1V25_S0_NB_PLL - @m78_lib.M78	6C4 21B4
	=PP1V25_S0M_NB_VCCA - @m78_lib.M78	6C4 21B8
	=PP1V25_S0M_NB_VCC - @m78_lib.M78	6C4 21A8
=PP2V5_S0_MXM	=PP2V5_S0_MXM - @m78_lib.M78	6D4 85A3
	PP2V5_S0 - @m78_lib.M78	6D6 7D3 77B2
=PP3V3_ENET_PHY	=PP3V3_ENET_PHY - @m78_lib.M78	37D6 38D6
	=PP3V3_S3_ENET - @m78_lib.M78	6D3 38B8 38D8 39A8
	=PP3V3_S3_BT - @m78_lib.M78	6D3 47D3
	=PP3V3_S3_MINI - @m78_lib.M78	6D3 34D2
	PP3V3_S3 - @m78_lib.M78	6A7 6D4 7C6 7D3 70D2 75D7 76B8 78C6
	=PP3V3_S3_MINI - @m78_lib.M78	6D3 34D2
	=PP3V3_S3_ENET - @m78_lib.M78	6D3 38B8 38D8 39A8
	=PP3V3_S3_BT - @m78_lib.M78	6D3 47D3
=PP3V3_S5_FAN	=PP3V3_S5_FAN - @m78_lib.M78	6D1 56B7 56D7 57D7
	=PP3V3_S5_SMBUS_SMC_A_S5 - @m78_lib.M78	6D1 52D3
	PP3V3_S5 - @m78_lib.M78	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @m78_lib.M78	6D1 46D5
	=PP3V3_S5_SMBUS_SMC_BSA - @m78_lib.M78	6D1 52C3
	=PP3V3_S5_LPCPLUS - @m78_lib.M78	6D1 7D4 51C6
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @m78_lib.M78	6D1 26B3 27B4
	=PP3V3_S5_SB_CLINK1 - @m78_lib.M78	6D1 25B1
	=PP3V3_S5_SB_GPIO - @m78_lib.M78	6D1 25D8
	=PP3V3_S5_ROM - @m78_lib.M78	6D1 61C6
	=PP3V3_S5_SMC - @m78_lib.M78	6D1 49D4 50B1 50D7
	=PP3V3_S5_FW - @m78_lib.M78	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
	=PP3V3_S5_SMBUS_SB_ME - @m78_lib.M78	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m78_lib.M78	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @m78_lib.M78	6D1 26A3 27D5
	=PP3V3_S5_SB_PM - @m78_lib.M78	6D1 28A5
	=PP3V3_S5_SB_USB - @m78_lib.M78	6D1 24C8
	=PP3V3_S5_SB - @m78_lib.M78	6D1 25A3 25A8 27D8 28D7
	PP3V3_S5 - @m78_lib.M78	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @m78_lib.M78	6D1 46D5
	=PP3V3_S5_SMC - @m78_lib.M78	6D1 49D4 50B1 50D7
	=PP3V3_S5_SMBUS_SMC_BSA - @m78_lib.M78	6D1 52C3
	=PP3V3_S5_SMBUS_SMC_A_S5 - @m78_lib.M78	6D1 52D3
	=PP3V3_S5_SMBUS_SB_ME - @m78_lib.M78	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m78_lib.M78	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @m78_lib.M78	6D1 26A3 27D5
	=PP3V3_S5_SB_USB - @m78_lib.M78	6D1 24C8
	=PP3V3_S5_SB_PM - @m78_lib.M78	6D1 28A5
	=PP3V3_S5_SB_GPIO - @m78_lib.M78	6D1 25D8
	=PP3V3_S5_SB_CLINK1 - @m78_lib.M78	6D1 25B1
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @m78_lib.M78	6D1 26B3 27B4
	=PP3V3_S5_SB - @m78_lib.M78	6D1 25A3 25A8 27D8 28D7
	=PP3V3_S5_ROM - @m78_lib.M78	6D1 61C6
	=PP3V3_S5_LPCPLUS - @m78_lib.M78	6D1 7D4 51C6
	=PP3V3_S5_FW - @m78_lib.M78	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO - @m78_lib.M78	6A4 98C4 98C6
	=PP5V_S0_MXM - @m78_lib.M78	6A4 84C7
	=PPV_S0_LCD_20INCH - @m78_lib.M78	6A4 90C8
	PP5V_S0 - @m78_lib.M78	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D3 94D6
	=PP5V_S0_SATA - @m78_lib.M78	6A4 6D6
	=PP5V_S0_LPCPLUS - @m78_lib.M78	6A4 7D4 51C6
	=PP5V_S0_PATA - @m78_lib.M78	6A4 44B6 44D6
	=PP5V_S0_SB - @m78_lib.M78	6A4 27D8
	PP5V_S0 - @m78_lib.M78	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D3 94D6
	=PPV_S0_LCD_20INCH - @m78_lib.M78	6A4 90C8
	=PP5V_S0_SB - @m78_lib.M78	6A4 27D8
	=PP5V_S0_PATA - @m78_lib.M78	6A4 44B6 44D6
	=PP5V_S0_MXM - @m78_lib.M78	6A4 84C7
	=PP5V_S0_LPCPLUS - @m78_lib.M78	6A4 7D4 51C6
=PP5V_S3_ALS	=PP5V_S3_ALS - @m78_lib.M78	6C3 58D5
	PP5V_S3 - @m78_lib.M78	6C4 7D3 70D3 75D8 76A8 78D6
	=PP5V_S3_SYSLED - @m78_lib.M78	6C3 50A5
	=PP5V_S3_MEMVTT - @m78_lib.M78	6C3 75B6
	=PP5V_S3_BNDI - @m78_lib.M78	6C3 47D7 58D5
	PP5V_S3 - @m78_lib.M78	6C4 7D3 70D3 75D8 76A8 78D6
	=PP5V_S3_SYSLED - @m78_lib.M78	6C3 50A5
	=PP5V_S3_MEMVTT - @m78_lib.M78	6C3 75B6
	=PP5V_S3_BNDI - @m78_lib.M78	6C3 47D7 58D5
=PP5V_S5_SB	=PP5V_S5_SB - @m78_lib.M78	6C1 27D8
	=PP5V_S5_USB - @m78_lib.M78	6C1 46C8 46D8
	PP5V_S5 - @m78_lib.M78	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78B7 78C2 78D6 78D8
	=PPVIN_S5_SMCVREF - @m78_lib.M78	6C1 50B8
	PP5V_S5 - @m78_lib.M78	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78B7 78C2 78D6 78D8
	=PPVIN_S5_SMCVREF - @m78_lib.M78	6C1 50B8
	=PP5V_S5_USB - @m78_lib.M78	6C1 46C8 46D8
=PP12V_S0_AUDIO_SPKRAMP	=PP12V_S0_AUDIO_SPKRAMP - @m78_lib.M78	6A4 98C6
	=PP12V_S0_CPU - @m78_lib.M78	6A4 53B8 71D8 72D7
	=PPV_S0_LCD_24INCH - @m78_lib.M78	6A4 90C8
	=PPV_S0_MXM_PWRSRC - @m78_lib.M78	6A4 53C4
	PP12V_S0 - @m78_lib.M78	6A6 6D8 7D3 73D7 74D7 76D8
	=PP12V_S0_FAN - @m78_lib.M78	6A4 56B6 56D7 57D6
	PP12V_S0 - @m78_lib.M78	6A6 6D8 7D3 73D7 74D7 76D8
	=PPV_S0_MXM_PWRSRC - @m78_lib.M78	6A4 53C4
	=PPV_S0_LCD_24INCH - @m78_lib.M78	6A4 90C8
	=PP12V_S0_FAN - @m78_lib.M78	6A4 56B6 56D7 57D6
	=PP12V_S0_CPU - @m78_lib.M78	6A4 53B8 71D8 72D7
=PP12V_S5_FET	=PP12V_S5_FET - @m78_lib.M78	6C1 78D3
	PP12V_S5 - @m78_lib.M78	6C2 6D6 7C3 7C6 70D8 76A8 76D5 78B7
	=PP12V_S5_FW - @m78_lib.M78	6C1 43D8
	PP12V_S5 - @m78_lib.M78	6C2 6D6 7C3 7C6 70D8 76A8 76D5 78B7
	=PP12V_S5_FW - @m78_lib.M78	6C1 43D8
=PPVCORE_S0_CPU	=PPVCORE_S0_CPU - @m78_lib.M78	6D4 11B5 11D6 12D7 53B6 53D8
	PPVCORE_CPU - @m78_lib.M78	6D6 7D3 71D1 72C1
=SB_CLINK_MPWROK	=SB_CLINK_MPWROK - @m78_lib.M78	25C3 28B7
	PM_SB_PWROK - @m78_lib.M78	7C4 7C4 25C3 28B6 70C1
=SMC_SMS_INT	=SMC_SMS_INT - @m78_lib.M78	49B5 50B2
	SMC_SMS_INT - @m78_lib.M78	50B2
ACDC_TEMP	ACDC_TEMP - @m78_lib.M78	6D6 50C2
	SMC_ANALOG_ID - @m78_lib.M78	49A8 50C3
ALL_SYS_PWRGD	ALL_SYS_PWRGD - @m78_lib.M78	7C4 7C4 49D8 50C2 70C1 84C7
	PM_LAN_PWRGD - @m78_lib.M78	49C5 50C3
ALS_GAIN	ALS_GAIN - @m78_lib.M78	49A5 50D5
	NC_ALS_GAIN - @m78_lib.M78	50D3
ALS_LEFT	ALS_LEFT - @m78_lib.M78	49A8 50D5
	TP_ALS_LEFT - @m78_lib.M78	50D3
ALS_RIGHT	ALS_RIGHT - @m78_lib.M78	49A8 58C4
ARB_DETECT_L	ARB_DETECT_L - @m78_lib.M78	25A7 25B3
CK505_48M_FSA	CK505_48M_FSA - @m78_lib.M78	29A3 30C8 105D3
CK505_CLKREQ1_L	CK505_CLKREQ1_L - @m78_lib.M78	29B3 30D2 85C8
CK505_CLKREQ3_L	CK505_CLKREQ3_L - @m78_lib.M78	29B3 30D2 40C3
CK505_CLKREQ6_L	CK505_CLKREQ6_L - @m78_lib.M78	29B3 30C2
	MINI_CLKREQ_L - @m78_lib.M78	30C2 34C6
CK505_CLKREQ8_L	CK505_CLKREQ8_L - @m78_lib.M78	29A3 30C2
	ENET_CLKREQ_L - @m78_lib.M78	30C2 38D3
CK505_CPU0_N	CK505_CPU0_N - @m78_lib.M78	29C3 30D5 105D3
	FSB_CLK_CPU_N - @m78_lib.M78	7C8 10B6 30D3 105C3
CK505_CPU0_P	CK505_CPU0_P - @m78_lib.M78	29C3 30D5 105D3
	FSB_CLK_CPU_P - @m78_lib.M78	7C8 10B6 30D3 105C3
CK505_CPU1_N	CK505_CPU1_N - @m78_lib.M78	29C3 30D5 105D3
	FSB_CLK_NB_N - @m78_lib.M78	7C3 7C7 14B3 30D3 105C3
CK505_CPU1_P	CK505_CPU1_P - @m78_lib.M78	29C3 30D5 105D3
	FSB_CLK_NB_P - @m78_lib.M78	7C7 14B3 30D3 105C3
CK505_CPU2_ITP_SRC10_N	CK505_CPU2_ITP_SRC10_N - @m78_lib.M78	29C3 30D5 105D3
	XDP_CLK_N - @m78_lib.M78	13B3 30D3 100A3 105C3
CK505_CPU2_ITP_SRC10_P	CK505_CPU2_ITP_SRC10_P - @m78_lib.M78	29C3 30D5 105D3
	XDP_CLK_P - @m78_lib.M78	13C3 30D3 100A3 105C3
CK505_DOT96_27M_N	CK505_DOT96_27M_N - @m78_lib.M78	29A3 30A5 105D3
	TP_CK505_27M_N - @m78_lib.M78	30A3
CK505_DOT96_27M_P	CK505_DOT96_27M_P - @m78_lib.M78	29A3 30A5 105D3
	TP_CK505_27M_P - @m78_lib.M78	30A3
CK505_FSA	CK505_FSA - @m78_lib.M78	30C7 105B3
CK505_FSB_TEST_MODE	CK505_FSB_TEST_MODE - @m78_lib.M78	29C5 30B8
CK505_FSC	CK505_FSC - @m78_lib.M78	30B7 105B3
CK505_LVDS_N	CK505_LVDS_N - @m78_lib.M78	29C3 30C5 105C3
	TP_CK505_LVDS_N - @m78_lib.M78	30C3

CK505_LVDS_P	CK505_LVDS_P - @m78_lib.M78	29B3 30C5 105D3
	TP_CK505_LVDS_P - @m78_lib.M78	30C3
CK505_PCI1_CLK	CK505_PCI1_CLK - @m78_lib.M78	29C5 30A5 105D3
	TP_CK505_PCI1_CLK - @m78_lib.M78	7C3 30A3
CK505_PCI2_CLK	CK505_PCI2_CLK - @m78_lib.M78	29B5 30A5 105D3
	TP_PCI_CLK33M_TPM - @m78_lib.M78	30A3
CK505_PCI3_CLK	CK505_PCI3_CLK - @m78_lib.M78	29B5 30A5 105D3
CK505_PCI4_CLK	CK505_PCI4_CLK - @m78_lib.M78	29B5 30A5 105D3
	TP_CK505_PCI4_CLK - @m78_lib.M78	30A3
CK505_PCI5_CLK_FCTSEL	CK505_PCI5_CLK_FCTSEL - @m78_lib.M78	29B5 30D8 105D3
CK505_PCIF0_CLK_ITPEN	CK505_PCIF0_CLK_ITPEN - @m78_lib.M78	29B7 30A5 105D3
CK505_PCIF1_CLK	CK505_PCIF1_CLK - @m78_lib.M78	29B5 30A5 105D3
CK505_REF0_FSC	CK505_REF0_FSC - @m78_lib.M78	29A3 30A8 105D3
CK505_REF1	CK505_REF1 - @m78_lib.M78	29A3 30B2
	TP_CK505_REF1 - @m78_lib.M78	7C3 30B1
CK505_SRC1_N	CK505_SRC1_N - @m78_lib.M78	29B3 30C5 105C3
	GPU_CLK100M_PCIE_N - @m78_lib.M78	30C3 85C7 105B3
CK505_SRC1_P	CK505_SRC1_P - @m78_lib.M78	29B3 30C5 105C3
	GPU_CLK100M_PCIE_P - @m78_lib.M78	30C3 85C7 105B3
CK505_SRC2_N	CK505_SRC2_N - @m78_lib.M78	29B3 30C5 105C3
	SB_CLK100M_DMI_N - @m78_lib.M78	7B8 7C3 24D2 30C3 105B3
CK505_SRC2_P	CK505_SRC2_P - @m78_lib.M78	29B3 30C5 105C3
	SB_CLK100M_DMI_P - @m78_lib.M78	7B8 24C2 30C3 105B3
CK505_SRC3_N	CK505_SRC3_N - @m78_lib.M78	29B3 30C5 105C3
	PCIE_CLK100M_FW_N - @m78_lib.M78	7D6 30C3 40C3 105B3
CK505_SRC3_P	CK505_SRC3_P - @m78_lib.M78	29B3 30C5 105C3
	PCIE_CLK100M_FW_P - @m78_lib.M78	7D6 30C3 40C3 105B3
CK505_SRC4_N	CK505_SRC4_N - @m78_lib.M78	29B3 30B5 105C3
	SB_CLK100M_SATA_N - @m78_lib.M78	7C8 23B6 30B3 105B3
CK505_SRC4_P	CK505_SRC4_P - @m78_lib.M78	29B3 30B5 105C3
	SB_CLK100M_SATA_P - @m78_lib.M78	7C8 23B6 30B3 105B3
CK505_SRC5_N	CK505_SRC5_N - @m78_lib.M78	29B3 30B5 105C3
	NB_CLK100M_PCIE_N - @m78_lib.M78	7C3 7C7 16C3 30B3 105B3
CK505_SRC5_P	CK505_SRC5_P - @m78_lib.M78	29B3 30B5 105C3
	NB_CLK100M_PCIE_P - @m78_lib.M78	7C7 16C3 30B3 105B3
CK505_SRC6_N	CK505_SRC6_N - @m78_lib.M78	29B3 30B5 105C3
	PCIE_CLK100M_MINI_N - @m78_lib.M78	30B3 34C6 105B3
CK505_SRC6_P	CK505_SRC6_P - @m78_lib.M78	29B3 30B5 105C3
	PCIE_CLK100M_MINI_P - @m78_lib.M78	30B3 34C6 105B3
CK505_SRC7_N	CK505_SRC7_N - @m78_lib.M78	29B3 30B5 105C3
CK505_SRC7_P	CK505_SRC7_P - @m78_lib.M78	29B3 30B5 105C3
CK505_SRC8_N	CK505_SRC8_N - @m78_lib.M78	29B3 30B5 105C3
	PCIE_CLK100M_ENET_N - @m78_lib.M78	7D6 30B3 37C8 105B3
CK505_SRC8_P	CK505_SRC8_P - @m78_lib.M78	29A3 30B5 105C3
	PCIE_CLK100M_ENET_P - @m78_lib.M78	7D6 30B3 37C8 105B3
CK505_XTAL_IN	CK505_XTAL_IN - @m78_lib.M78	29C5
CK505_XTAL_OUT	CK505_XTAL_OUT - @m78_lib.M78	29C5
CLINK_NB_CLK	CLINK_NB_CLK - @m78_lib.M78	7A7 7A8 16A3 25C3 104B3
CLINK_NB_DATA	CLINK_NB_DATA - @m78_lib.M78	7A7 7A8 16A3 25C3 104B3
CLINK_NB_RESET_L	CLINK_NB_RESET_L - @m78_lib.M78	16A3 25C3 104B3
CLINK_WLAN_CLK	CLINK_WLAN_CLK - @m78_lib.M78	34A8
	TP_CLINK_WLAN_CLK - @m78_lib.M78	25C3 34A6
CLINK_WLAN_DATA	CLINK_WLAN_DATA - @m78_lib.M78	34A8
	TP_CLINK_WLAN_DATA - @m78_lib.M78	25C3 28C4 34A6
CLINK_WLAN_RESET_L	CLINK_WLAN_RESET_L - @m78_lib.M78	34A8
	TP_CLINK_WLAN_RESET_L - @m78_lib.M78	25D5 34A6
CLK_PWRGD	CLK_PWRGD - @m78_lib.M78	25C3 29A3
CPUVCORE_ISENSE_CAL	CPUVCORE_ISENSE_CAL - @m78_lib.M78	53B6
CPUVSENSE_IN	CPUVSENSE_IN - @m78_lib.M78	53D7
CPU_A20M_L	CPU_A20M_L - @m78_lib.M78	7C8 10C8 23C4 100B3
CPU_BSEL<0>	CPU_BSEL<0> - @m78_lib.M78	10B4 30C6 100B3
CPU_BSEL<1>	CPU_BSEL<1> - @m78_lib.M78	10A4 30B6 100B3
CPU_BSEL<2>	CPU_BSEL<2> - @m78_lib.M78	10A4 30B6 100A3
CPU_COMP<0>	CPU_COMP<0> - @m78_lib.M78	10B3 100A3
CPU_COMP<1>	CPU_COMP<1> - @m78_lib.M78	10B3 100A3
CPU_COMP<2>	CPU_COMP<2> - @m78_lib.M78	10B3 100A3
CPU_COMP<3>	CPU_COMP<3> - @m78_lib.M78	10B3 100A3
CPU_DPRSTP_L	CPU_DPRSTP_L - @m78_lib.M78	10B2 16B6 23C4 71C7 100A3
CPU_DPSLP_L	CPU_DPSLP_L - @m78_lib.M78	10B2 23C4 100B3
CPU_FERR_L	CPU_FERR_L - @m78_lib.M78	10C8 23C2 100B3
CPU_GTLREF	CPU_GTLREF - @m78_lib.M78	10B4 100A3
CPU_HSK_THRMD_N	CPU_HSK_THRMD_N - @m78_lib.M78	55A5 55A7 108A3
CPU_HSK_THRMD_P	CPU_HSK_THRMD_P - @m78_lib.M78	55A7 55B5 108A3
CPU_IERR_L	CPU_IERR_L - @m78_lib.M78	10D6 100B3
CPU_IGNNE_L	CPU_IGNNE_L - @m78_lib.M78	7C8 10C8 23C4 100B3
CPU_INIT_L	CPU_INIT_L - @m78_lib.M78	7C8 10D6 23C4 51B2 100B3
CPU_INIT_LS3V3	CPU_INIT_LS3V3 - @m78_lib.M78	51C4
CPU_INIT_R_L	CPU_INIT_R_L - @m78_lib.M78	51B3
CPU_INTR	CPU_INTR - @m78_lib.M78	7C8 10B8 23C4 100B3
CPU_NMI	CPU_NMI - @m78_lib.M78	7C8 10B8 23C4 100B3
CPU_PROCHOT_BUF	CPU_PROCHOT_BUF - @m78_lib.M78	50D2
CPU_PROCHOT_L	CPU_PROCHOT_L - @m78_lib.M78	10C5 50D3 100B3
CPU_PROCHOT_L_R	CPU_PROCHOT_L_R - @m78_lib.M78	50D2
CPU_PSI_L	CPU_PSI_L - @m78_lib.M78	10A2 28B7
	IMVP6_PSI_L - @m78_lib.M78	28B6 71C7
CPU_PWRGD	CPU_PWRGD - @m78_lib.M78	7C4 10B2 13C7 23C4 100B3
CPU_SMI_L	CPU_SMI_L - @m78_lib.M78	7C8 10B8 23C4 100B3
CPU_STPCLK_L	CPU_STPCLK_L - @m78_lib.M78	7C8 10B8 23C4 100B3
CPU_TEST1	CPU_TEST1 - @m78_lib.M78	10B4
CPU_TEST2	CPU_TEST2 - @m78_lib.M78	10B4
CPU_TEST4	CPU_TEST4 - @m78_lib.M78	10B4
CPU_THERMD_N	CPU_THERMD_N - @m78_lib.M78	10C6 55C4 108A3
CPU_THERMD_P	CPU_THERMD_P - @m78_lib.M78	10C6 55C4 108A3
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @m78_lib.M78	23C4
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @m78_lib.M78	11A5 71A3 100A3
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @m78_lib.M78	11A5 71A3 100A3
CPU_VID<0>	CPU_VID<0> - @m78_lib.M78	11B6 12C2
CPU_VID<6..0>	CPU_VID<6..0> - @m78_lib.M78	100A3
CPU_VID<1>	CPU_VID<1> - @m78_lib.M78	11B6 12C2
CPU_VID<2>	CPU_VID<2> - @m78_lib.M78	11B6 12C2
CPU_VID<3>	CPU_VID<3> - @m78_lib.M78	11B6 12C2
CPU_VID<4>	CPU_VID<4> - @m78_lib.M78	11B6 12C2
CPU_VID<5>	CPU_VID<5> - @m78_lib.M78	11B6 12C2
CPU_VID<6>	CPU_VID<6> - @m78_lib.M78	11B6 12C2
DEBUG_RESET_L	DEBUG_RESET_L - @m78_lib.M78	7D4 28D1 51B6
DMI_IRCOMP_R	DMI_IRCOMP_R - @m78_lib.M78	24C3
DMI_N2S_N<0>	DMI_N2S_N<0> - @m78_lib.M78	7B8 16B3 24D2
DMI_N2S_N<3..0>	DMI_N2S_N<3..0> - @m78_lib.M78	101D3
DMI_N2S_N<1>	DMI_N2S_N<1> - @m78_lib.M78	16B3 24D2
DMI_N2S_N<2>	DMI_N2S_N<2> - @m78_lib.M78	16B3 24D2
DMI_N2S_N<3>	DMI_N2S_N<3> - @m78_lib.M78	16B3 24D2
DMI_N2S_P<0>	DMI_N2S_P<0> - @m78_lib.M78	7B8 16B3 24D2 101D3
DMI_N2S_P<1>	DMI_N2S_P<1> - @m78_lib.M78	16B3 24D2
DMI_N2S_P<3..1>	DMI_N2S_P<3..1> - @m78_lib.M78	101D3
DMI_N2S_P<2>	DMI_N2S_P<2> - @m78_lib.M78	16B3 24D2
DMI_N2S_P<3>	DMI_N2S_P<3> - @m78_lib.M78	16B3 24D2
DMI_S2N_N<0>	DMI_S2N_N<0> - @m78_lib.M78	7C7 16C3 24D2
DMI_S2N_N<3..0>	DMI_S2N_N<3..0> - @m78_lib.M78	101C3
DMI_S2N_N<1>	DMI_S2N_N<1> - @m78_lib.M78	16C3 24D2
DMI_S2N_N<2>	DMI_S2N_N<2> - @m78_lib.M78	16B3 24D2
DMI_S2N_N<3>	DMI_S2N_N<3> - @m78_lib.M78	16B3 24D2
DMI_S2N_P<0>	DMI_S2N_P<0> - @m78_lib.M78	7C7 16B3 24D2 101C3
DMI_S2N_P<1>	DMI_S2N_P<1> - @m78_lib.M78	16B3 24D2
DMI_S2N_P<3..1>	DMI_S2N_P<3..1> - @m78_lib.M78	101D3
DMI_S2N_P<2>	DMI_S2N_P<2> - @m78_lib.M78	16B3 24D2
DMI_S2N_P<3>	DMI_S2N_P<3> - @m78_lib.M78	16B3 24D2
DVI_DDC_CLK	DVI_DDC_CLK - @m78_lib.M78	94D2
DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @m78_lib.M78	94D3 94D5
DVI_DDC_DATA	DVI_DDC_DATA - @m78_lib.M78	94C2
DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @m78_lib.M78	94C3 94D5
DVI_HOTPLUG_DET	DVI_HOTPLUG_DET - @m78_lib.M78	24A6 28B2
	SB_GPIO4 - @m78_lib.M78	28B2
DVI_HPD_UF	DVI_HPD_UF - @m78_lib.M78	94C3 94D5
ENET_CLK25M_XTALI	ENET_CLK25M_XTALI - @m78_lib.M78	37B4
ENET_CLK25M_XTALO	ENET_CLK25M_XTALO - @m78_lib.M78	37B4
ENET_CTAP_<0>	ENET_CTAP_<0> - @m78_lib.M78	39B5
ENET_CTAP_<1>	ENET_CTAP_<1> - @m78_lib.M78	39B5
ENET_CTAP_<2>	ENET_CTAP_<2> - @m78_lib.M78	39B5
ENET_CTAP_<3>	ENET_CTAP_<3> - @m78_lib.M78	39B5
ENET_CTAP_COMMON	ENET_CTAP_COMMON - @m78_lib.M78	39A4
ENET_CTRL12	ENET_CTRL12 - @m78_lib.M78	38A5 38B1
	TP_YUKON_CTRL12 - @m78_lib.M78	37C2 38B3
ENET_CTRL19R25	ENET_CTRL19R25 - @m78_lib.M78	38B1 38C6
	TP_YUKON_CTRL18 - @m78_lib.M78	37C2 38B3
ENET_LED_ACT_L	ENET_LED_ACT_L - @m78_lib.M78	37B2 39A8
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m78_lib.M78	37B2 39A8
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m78_lib.M78	37B2 39A8
ENET_LED_LINK_L	ENET_LED_LINK_L - @m78_lib.M78	37B2 39A8
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m78_lib.M78	37C2
ENET_MDI0	ENET_MDI0 - @m78_lib.M78	37B7 104B3
ENET_MDI1	ENET_MDI1 - @m78_lib.M78	37B6 104B3
ENET_MDI2	ENET_MDI2 - @m78_lib.M78	37B6 104B3
ENET_MDI3	ENET_MDI3 - @m78_lib.M78	37B5 104B3
ENET_MDI_N<0>	ENET_MDI_N<0> - @m78_lib.M78	37B8 39C7 104B3
ENET_MDI_N<1>	ENET_MDI_N<1> - @m78_lib.M78	37B8 39C7 104B3
ENET_MDI_N<2>	ENET_MDI_N<2> - @m78_lib.M78	37B8 39B7 104A3
ENET_MDI_N<3>	ENET_MDI_N<3> - @m78_lib.M78	37B8 39B7 104A3
ENET_MDI_P<0>	ENET_MDI_P<0> - @m78_lib.M78	37B8 39C7 104B3
ENET_MDI_P<1>	ENET_MDI_P<1> - @m78_lib.M78	37B8 39C7 104B3
ENET_MDI_P<2>	ENET_MDI_P<2> - @m78_lib.M78	37B8 39B7 104B3
ENET_MDI_P<3>	ENET_MDI_P<3> - @m78_lib.M78	37B8 39B7 104A3
ENET_MDI_R_N<0>	ENET_MDI_R_N<0> - @m78_lib.M78	108B3
ENET_MDI_R_N<1>	ENET_MDI_R_N<1> - @m78_lib.M78	108B3
ENET_MDI_R_N<2>	ENET_MDI_R_N<2> - @m78_lib.M78	108B3
ENET_MDI_R_N<3>	ENET_MDI_R_N<3> - @m78_lib.M78	108B3
ENET_MDI_R_P<0>	ENET_MDI_R_P<0> - @m78_lib.M78	108B3
ENET_MDI_R_P<1>	ENET_MDI_R_P<1> - @m78_lib.M78	108B3
ENET_MDI_R_P<2>	ENET_MDI_R_P<2> - @m78_lib.M78	108B3
ENET_MDI_R_P<3>	ENET_MDI_R_P<3> - @m78_lib.M78	108B3
ENET_MDI_T_N<0>	ENET_MDI_T_N<0> - @m78_lib.M78	39C5 108B3
ENET_MDI_T_N<1>	ENET_MDI_T_N<1> - @m78_lib.M78	39C5 108B3
ENET_MDI_T_N<2>	ENET_MDI_T_N<2> - @m78_lib.M78	39B5 108B3
ENET_MDI_T_N<3>	ENET_MDI_T_N<3> - @m78_lib.M78	39B5 108B3
ENET_MDI_T_P<0>	ENET_MDI_T_P<0> - @m78_lib.M78	39C5 108B3
ENET_MDI_T_P<1>	ENET_MDI_T_P<1> - @m78_lib.M78	39C5 108B3
ENET_MDI_T_P<2>	ENET_MDI_T_P<2> - @m78_lib.M78	39B5 108B3
ENET_MDI_T_P<3>	ENET_MDI_T_P<3> - @m78_lib.M78	39B5 108B3
ENET_RESET_L	ENET_RESET_L - @m78_lib.M78	7D6 28C1 37B8
EXCARD_OC_L	EXCARD_OC_L - @m78_lib.M78	24C8
EXTGPU_LVDS_EN	EXTGPU_LVDS_EN - @m78_lib.M78	13C3 24C8
EXTGPU_PWR_EN	EXTGPU_PWR_EN - @m78_lib.M78	23C4 28A2
	TP_EXTGPU_PWR_EN - @m78_lib.M78	28A1
EXTGPU_RST_L	EXTGPU_RST_L - @m78_lib.M78	25A5 25C5 28A2
	TP_EXTGPU_RST_L - @m78_lib.M78	28A1
F0_GATESLOWDN	F0_GATESLOWDN - @m78_lib.M78	56D5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @m78_lib.M78	56D6
F1_GATESLOWDN	F1_GATESLOWDN - @m78_lib.M78	56B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @m78_lib.M78	56B6
F2_GATESLOWDN	F2_GATESLOWDN - @m78_lib.M78	57D4
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @m78_lib.M78	57D5
FAN_0_PWR	FAN_0_PWR - @m78_lib.M78	56C4
FAN_1_PWR	FAN_1_PWR - @m78_lib.M78	56B3
FAN_2_PWR	FAN_2_PWR - @m78_lib.M78	57C3
FAN_TACH0	FAN_TACH0 - @m78_lib.M78	56C7
FAN_TACH1	FAN_TACH1 - @m78_lib.M78	56A7
FAN_TACH2	FAN_TACH2 - @m78_lib.M78	57C7
FSB_ADSTB_L<0>	FSB_ADSTB_L<0> - @m78_lib.M78	7D7 7D8 10D8 14C3 100C3
FSB_ADSTB_L<1>	FSB_ADSTB_L<1> - @m78_lib.M78	7D7 7D8 10C8 14C3 100B3
FSB_ADS_L	FSB_ADS_L - @m78_lib.M78	10D6 14C3 100D3
FSB_A_L<3>	FSB_A_L<3> - @m78_lib.M78	10D8 14D3
FSB_A_L<5..3>	FSB_A_L<5..3> - @m78_lib.M78	100C3
FSB_A_L<4>	FSB_A_L<4> - @m78_lib.M78	10D8 14D3
FSB_A_L<5>	FSB_A_L<5> - @m78_lib.M78	10D8 14D3
FSB_A_L<6>	FSB_A_L<6> - @m78_lib.M78	7D7 7D8 10D8 14D3 100C3
FSB_A_L<7>	FSB_A_L<7> - @m78_lib.M78	10D8 14D3
FSB_A_L<16..7>	FSB_A_L<16..7> - @m78_lib.M78	100C3
FSB_A_L<8>	FSB_A_L<8> - @m78_lib.M78	10D8 14D3
FSB_A_L<9>	FSB_A_L<9> - @m78_lib.M78	10D8 14D3
FSB_A_L<10>	FSB_A_L<10> - @m78_lib.M78	10D8 14D3
FSB_A_L<11>	FSB_A_L<11> - @m78_lib.M78	10D8 14D3
FSB_A_L<12>	FSB_A_L<12> - @m78_lib.M78	10D8 14D3
FSB_A_L<13>	FSB_A_L<13> - @m78_lib.M78	10D8 14D3
FSB_A_L<14>	FSB_A_L<14> - @m78_lib.M78	10D8 14D3
FSB_A_L<15>	FSB_A_L<15> - @m78_lib.M78	10D8 14D3
FSB_A_L<16>	FSB_A_L<16> - @m78_lib.M78	10D8 14C3
FSB_A_L<17>	FSB_A_L<17> - @m78_lib.M78	10C8 14C3
FSB_A_L<26..17>	FSB_A_L<26..17> - @m78_lib.M78	100B3
FSB_A_L<18>	FSB_A_L<18> - @m78_lib.M78	10C8 14C3
FSB_A_L<19>	FSB_A_L<19> - @m78_lib.M78	10C8 14C3
FSB_A_L<20>	FSB_A_L<20> - @m78_lib.M78	10C8 14C3
FSB_A_L<21>	FSB_A_L<21> - @m78_lib.M78	10C8 14C3
FSB_A_L<22>	FSB_A_L<22> - @m78_lib.M78	10C8 14C3
FSB_A_L<23>	FSB_A_L<23> - @m78_lib.M78	10C8 14C3
FSB_A_L<24>	FSB_A_L<24> - @m78_lib.M78	10C8 14C3
FSB_A_L<25>	FSB_A_L<25> - @m78_lib.M78	10C8 14C3
FSB_A_L<26>	FSB_A_L<26> - @m78_lib.M78	10C8 14C3
FSB_A_L<27>	FSB_A_L<27> - @m78_lib.M78	7D7 7D8 10C8 14C3 100B3
FSB_A_L<28>	FSB_A_L<28> - @m78_lib.M78	10C8 14C3
FSB_A_L<35..28>	FSB_A_L<35..28> - @m78_lib.M78	100B3
FSB_A_L<29>	FSB_A_L<29> - @m78_lib.M78	10C8 14C3
FSB_A_L<30>	FSB_A_L<30> - @m78_lib.M78	10C8 14C3
FSB_A_L<31>	FSB_A_L<31> - @m78_lib.M78	10C8 14C3
FSB_A_L<32>	FSB_A_L<32> - @m78_lib.M78	10C8 14C3
FSB_A_L<33>	FSB_A_L<33> - @m78_lib.M78	10C8 14C3
FSB_A_L<34>	FSB_A_L<34> - @m78_lib.M78	10C8 14C3
FSB_A_L<35>	FSB_A_L<35> - @m78_lib.M78	10C8 14C3
FSB_BNR_L	FSB_BNR_L - @m78_lib.M78	7C7 10D6 14C3 100D3
FSB_BPRI_L	FSB_BPRI_L - @m78_lib.M78	10D6 14C3 100D3
FSB_BREQ0_L	FSB_BREQ0_L - @m78_lib.M78	7C7 10D6 14B3 100D3
FSB_CPURST_L	FSB_CPURST_L - @m78_lib.M78	7C8 10D6 13B2 14A5 100D3
FSB_CPUSLP_L	FSB_CPUSLP_L - @m78_lib.M78	10A2 14A5 100B3
FSB_DBSY_L	FSB_DBSY_L - @m78_lib.M78	7C7 10D6 14B3 100D3
FSB_DEFER_L	FSB_DEFER_L - @m78_lib.M78	10D6 14B3 100D3
FSB_DINV_L<0>	FSB_DINV_L<0> - @m78_lib.M78	7D7 7D8 10C4 14B3 100D3
FSB_DINV_L<1>	FSB_DINV_L<1> - @m78_lib.M78	7D7 7D8 10B4 14B3 100C3
FSB_DINV_L<2>	FSB_DINV_L<2> - @m78_lib.M78	7D7 7D8 10C2 14B3 100C3
FSB_DINV_L<3>	FSB_DINV_L<3> - @m78_lib.M78	7D7 7D8 10B2 14B3 100C3
FSB_DPWR_L	FSB_DPWR_L - @m78_lib.M78	7C7 10B2 14B3 100D3
FSB_DRDY_L	FSB_DRDY_L - @m78_lib.M78	10D6 14B3 100D3
FSB_DSTB_L_N<0>	FSB_DSTB_L_N<0> - @m78_lib.M78	7D7 7D8 10C4 14B3 100C3
FSB_DSTB_L_N<1>	FSB_DSTB_L_N<1> - @m78_lib.M78	7D7 7D8 10B4 14B3 100C3
FSB_DSTB_L_N<2>	FSB_DSTB_L_N<2> - @m78_lib.M78	7D7 7D8 10C2 14B3 100C3
FSB_DSTB_L_N<3>	FSB_DSTB_L_N<3> - @m78_lib.M78	7D7 7D8 10B2 14B3 100C3
FSB_DSTB_L_P<0>	FSB_DSTB_L_P<0> - @m78_lib.M78	7D7 7D8 10C4 14B3 100D3
FSB_DSTB_L_P<1>	FSB_DSTB_L_P<1> - @m78_lib.M78	7D7 7D8 10B4 14B3 100C3
FSB_DSTB_L_P<2>	FSB_DSTB_L_P<2> - @m78_lib.M78	7D7 7D8 10C2 14A3 100C3
FSB_DSTB_L_P<3>	FSB_DSTB_L_P<3> - @m78_lib.M78	7D7 7D8 10B2 14A3 100C3
FSB_D_L<0>	FSB_D_L<0> - @m78_lib.M78	7D7 7D8 10C4 14D5 100D3
FSB_D_L<1>	FSB_D_L<1> - @m78_lib.M78	10C4 14D5
FSB_D_L<15..1>	FSB_D_L<15..1> - @m78_lib.M78	100D3
FSB_D_L<2>	FSB_D_L<2> - @m78_lib.M78	10C4 14D5
FSB_D_L<3>	FSB_D_L<3> - @m78_lib.M78	10C4 14D5
FSB_D_L<4>	FSB_D_L<4> - @m78_lib.M78	10C4 14D5
FSB_D_L<5>	FSB_D_L<5> - @m78_lib.M78	10C4 14D5
FSB_D_L<6>	FSB_D_L<6> - @m78_lib.M78	10C4 14D5
FSB_D_L<7>	FSB_D_L<7> - @m78_lib.M78	10C4 14D5
FSB_D_L<8>	FSB_D_L<8> - @m78_lib.M78	10C4 14D5
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FSB_D_L<11>	FSB_D_L<11> - @m78_lib.M78	10C4 14D5
FSB_D_L<12>	FSB_D_L<12> - @m78_lib.M78	10C4 14D5
FSB_D_L<13>	FSB_D_L<13> - @m78_lib.M78	10C4 14C5
FSB_D_L<14>	FSB_D_L<14> - @m78_lib.M78	10C4 14C5
FSB_D_L<15>	FSB_D_L<15> - @m78_lib.M78	10C4 14C5
FSB_D_L<16>	FSB_D_L<16> - @m78_lib.M78	7D7 7D8 10C4 14C5 100C3
FSB_D_L<17>	FSB_D_L<17> - @m78_lib.M78	10C4 14C5
FSB_D_L<31..17>	FSB_D_L<31..17> - @m78_lib.M78	100C3
FSB_D_L<18>	FSB_D_L<18> - @m78_lib.M78	10C4 14C5
FSB_D_L<19>	FSB_D_L<19> - @m78_lib.M78	10B4 14C5
FSB_D_L<20>	FSB_D_L<20> - @m78_lib.M78	10B4 14C5
FSB_D_L<21>	FSB_D_L<21> - @m78_lib.M78	10B4 14C5
FSB_D_L<22>	FSB_D_L<22> - @m78_lib.M78	10B4 14C5
FSB_D_L<23>	FSB_D_L<23> - @m78_lib.M78	10B4 14C5
FSB_D_L<24>	FSB_D_L<24> - @m78_lib.M78	10B4 14C5
FSB_D_L<25>	FSB_D_L<25> - @m78_lib.M78	10B4 14C5
FSB_D_L<26>	FSB_D_L<26> - @m78_lib.M78	10B4 14C5
FSB_D_L<27>	FSB_D_L<27> - @m78_lib.M78	10B4 14C5
FSB_D_L<28>	FSB_D_L<28> - @m78_lib.M78	10B4 14C5
FSB_D_L<29>	FSB_D_L<29> - @m78_lib.M78	10B4 14C5
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FSB_D_L<31>	FSB_D_L<31> - @m78_lib.M78	10B4 14C5
FSB_D_L<32>	FSB_D_L<32> - @m78_lib.M78	10C2 14C5
FSB_D_L<40..32>	FSB_D_L<40..32> - @m78_lib.M78	100C3
FSB_D_L<33>	FSB_D_L<33> - @m78_lib.M78	10C2 14C5
FSB_D_L<34>	FSB_D_L<34> - @m78_lib.M78	10C2 14C5
FSB_D_L<35>	FSB_D_L<35> - @m78_lib.M78	10C2 14C5
FSB_D_L<36>	FSB_D_L<36> - @m78_lib.M78	10C2 14C5
FSB_D_L<37>	FSB_D_L<37> - @m78_lib.M78	10C2 14C5
FSB_D_L<38>	FSB_D_L<38> - @m78_lib.M78	10C2 14C5
FSB_D_L<39>	FSB_D_L<39> - @m78_lib.M78	10C2 14B5
FSB_D_L<40>	FSB_D_L<40> - @m78_lib.M78	10C2 14B5
FSB_D_L<41>	FSB_D_L<41> - @m78_lib.M78	7D7 7D8 10C2 14B5 100C3
FSB_D_L<42>	FSB_D_L<42> - @m78_lib.M78	10C2 14B5
FSB_D_L<47..42>	FSB_D_L<47..42> - @m78_lib.M78	100C3
FSB_D_L<43>	FSB_D_L<43> - @m78_lib.M78	10C2 14B5
FSB_D_L<44>	FSB_D_L<44> - @m78_lib.M78	10C2 14B5
FSB_D_L<45>	FSB_D_L<45> - @m78_lib.M78	10C2 14B5
FSB_D_L<46>	FSB_D_L<46> - @m78_lib.M78	10C2 14B5
FSB_D_L<47>	FSB_D_L<47> - @m78_lib.M78	10C2 14B5
FSB_D_L<48>	FSB_D_L<48> - @m78_lib.M78	10C2 14B5
FSB_D_L<58..48>	FSB_D_L<58..48> - @m78_lib.M78	100C3
FSB_D_L<49>	FSB_D_L<49> - @m78_lib.M78	10C2 14B5
FSB_D_L<50>	FSB_D_L<50> - @m78_lib.M78	10C2 14B5
FSB_D_L<51>	FSB_D_L<51> - @m78_lib.M78	10B2 14B5
FSB_D_L<52>	FSB_D_L<52> - @m78_lib.M78	10B2 14B5
FSB_D_L<53>	FSB_D_L<53> - @m78_lib.M78	10B2 14B5
FSB_D_L<54>	FSB_D_L<54> - @m78_lib.M78	10B2 14B5
FSB_D_L<55>	FSB_D_L<55> - @m78_lib.M78	10B2 14B5
FSB_D_L<56>	FSB_D_L<56> - @m78_lib.M78	10B2 14B5
FSB_D_L<57>	FSB_D_L<57> - @m78_lib.M78	10B2 14B5
FSB_D_L<58>	FSB_D_L<58> - @m78_lib.M78	10B2 14B5
FSB_D_L<59>	FSB_D_L<59> - @m78_lib.M78	7D7 7D8 10B2 14B5 100C3
FSB_D_L<60>	FSB_D_L<60> - @m78_lib.M78	10B2 14B5
FSB_D_L<63..60>	FSB_D_L<63..60> - @m78_lib.M78	100C3
FSB_D_L<61>	FSB_D_L<61> - @m78_lib.M78	10B2 14B5
FSB_D_L<62>	FSB_D_L<62> - @m78_lib.M78	10B2 14B5
FSB_D_L<63>	FSB_D_L<63> - @m78_lib.M78	10B2 14B5
FSB_HITM_L	FSB_HITM_L - @m78_lib.M78	7C7 10C6 14B3 100D3
FSB_HIT_L	FSB_HIT_L - @m78_lib.M78	7C7 10C6 14B3 100D3
FSB_LOCK_L	FSB_LOCK_L - @m78_lib.M78	7D7 7D8 10D6 14B3 100D3
FSB_REQ_L<0>	FSB_REQ_L<0> - @m78_lib.M78	7C7 7C8 10D8 14A3
FSB_REQ_L<4..0>	FSB_REQ_L<4..0> - @m78_lib.M78	100C3
FSB_REQ_L<1>	FSB_REQ_L<1> - @m78_lib.M78	7C7 7C8 10D8 14A3
FSB_REQ_L<2>	FSB_REQ_L<2> - @m78_lib.M78	7C7 7C8 10D8 14A3
FSB_REQ_L<3>	FSB_REQ_L<3> - @m78_lib.M78	7C7 7C8 10D8 14A3
FSB_REQ_L<4>	FSB_REQ_L<4> - @m78_lib.M78	7C7 7C8 10C8 14A3
FSB_RS_L<0>	FSB_RS_L<0> - @m78_lib.M78	10D6 14A3
FSB_RS_L<2..0>	FSB_RS_L<2..0> - @m78_lib.M78	100D3
FSB_RS_L<1>	FSB_RS_L<1> - @m78_lib.M78	10D6 14A3
FSB_RS_L<2>	FSB_RS_L<2> - @m78_lib.M78	10D6 14A3
FSB_TRDY_L	FSB_TRDY_L - @m78_lib.M78	10D6 14B3 100D3
FW643_REGCTL	FW643_REGCTL - @m78_lib.M78	40C3
FWH_INIT_L	FWH_INIT_L - @m78_lib.M78	7D4 51C5
FWH_MFG_MODE	FWH_MFG_MODE - @m78_lib.M78	25A7 25C5
FW_OCR10_CTL	FW_OCR10_CTL - @m78_lib.M78	40B6 42C8
FW_OCR10_CTL_R	FW_OCR10_CTL_R - @m78_lib.M78	42C7
FW_P0_TPA_C	FW_P0_TPA_C - @m78_lib.M78	43B8
FW_P0_TPBIAS	FW_P0_TPBIAS - @m78_lib.M78	40C6 43D8
FW_P1_TPA_C	FW_P1_TPA_C - @m78_lib.M78	43B7
FW_P1_TPBIAS	FW_P1_TPBIAS - @m78_lib.M78	40C6 43D8
FW_P2_TPA_N	FW_P2_TPA_N - @m78_lib.M78	40C6 43A8
	NC_FW_PORT2_TPA_N - @m78_lib.M78	43A6
FW_P2_TPA_P	FW_P2_TPA_P - @m78_lib.M78	40C6 43A8
	NC_FW_PORT2_TPA_P - @m78_lib.M78	43A6
FW_P2_TPBIAS	FW_P2_TPBIAS - @m78_lib.M78	40C6 43A8
	NC_FW_PORT2_TPBIAS - @m78_lib.M78	43A6
FW_P2_TPB_N	FW_P2_TPB_N - @m78_lib.M78	40C6 43A8
	NC_FW_PORT2_TPB_N - @m78_lib.M78	43A6
FW_P2_TPB_P	FW_P2_TPB_P - @m78_lib.M78	40C6 43A8
	NC_FW_PORT2_TPB_P - @m78_lib.M78	43A6
FW_PHY_DS0	FW_PHY_DS0 - @m78_lib.M78	40C6 42D3
FW_PHY_DS1	FW_PHY_DS1 - @m78_lib.M78	40C6 42D3
FW_PHY_DS2	FW_PHY_DS2 - @m78_lib.M78	40C6 42D3
FW_PORT0_TPA_N	FW_PORT0_TPA_N - @m78_lib.M78	43C5 43C6 106D3
	FW_P0_TPA_N - @m78_lib.M78	40C6 43C8
FW_PORT0_TPA_P	FW_PORT0_TPA_P - @m78_lib.M78	43C5 43C6 106D3
	FW_P0_TPA_P - @m78_lib.M78	40C6 43C8
FW_PORT0_TPA_R	FW_PORT0_TPA_R - @m78_lib.M78	43C2
FW_PORT0_TPB_N	FW_PORT0_TPB_N - @m78_lib.M78	43C5 43C6 106D3
	FW_P0_TPB_N - @m78_lib.M78	40C6 43C8
FW_PORT0_TPB_P	FW_PORT0_TPB_P - @m78_lib.M78	43C5 43C6 106D3
	FW_P0_TPB_P - @m78_lib.M78	40C6 43C8
FW_PORT0_VP	FW_PORT0_VP - @m78_lib.M78	43D3
FW_PORT0_VP_F	FW_PORT0_VP_F - @m78_lib.M78	43D5
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m78_lib.M78	43B2 106D3
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m78_lib.M78	43B2 106D3
FW_PORT1_TPA_N	FW_PORT1_TPA_N - @m78_lib.M78	43B6 43C6 106D3
	FW_P1_TPA_N - @m78_lib.M78	40C6 43C8
FW_PORT1_TPA_P	FW_PORT1_TPA_P - @m78_lib.M78	43B6 43C6 106D3
	FW_P1_TPA_P - @m78_lib.M78	40C6 43C8
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m78_lib.M78	43B2 106D3
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m78_lib.M78	43B2 106D3
FW_PORT1_TPB_N	FW_PORT1_TPB_N - @m78_lib.M78	43A6 43C6 106D3
	FW_P1_TPB_N - @m78_lib.M78	40C6 43C8
FW_PORT1_TPB_P	FW_PORT1_TPB_P - @m78_lib.M78	43B6 43C6 106D3
	FW_P1_TPB_P - @m78_lib.M78	40C6 43C8
FW_PORT1_VP	FW_PORT1_VP - @m78_lib.M78	43B3
FW_PORT1_VP_F	FW_PORT1_VP_F - @m78_lib.M78	43D5
FW_PORTS_VP	FW_PORTS_VP - @m78_lib.M78	43D7
FW_PORTS_VP_R	FW_PORTS_VP_R - @m78_lib.M78	40C7 43D6
FW_PU_RST_L	FW_PU_RST_L - @m78_lib.M78	40B6
FW_R0	FW_R0 - @m78_lib.M78	40B6
FW_RESET_L	FW_RESET_L - @m78_lib.M78	7D6 28C1 40B3
FW_REXT	FW_REXT - @m78_lib.M78	40B6
FW_SCL	FW_SCL - @m78_lib.M78	40B3
FW_TPCPS	FW_TPCPS - @m78_lib.M78	40B6
FW_TRST_L	FW_TRST_L - @m78_lib.M78	7C3 40C3
FW_VAUX_DETECT	FW_VAUX_DETECT - @m78_lib.M78	40C3
FW_XI	FW_XI - @m78_lib.M78	40B6
FW_XO	FW_XO - @m78_lib.M78	40B6
FW_XO_R	FW_XO_R - @m78_lib.M78	40B7
GATE_12V_S3	GATE_12V_S3 - @m78_lib.M78	78D2
GATE_12V_S3_R	GATE_12V_S3_R - @m78_lib.M78	78D3
GFX_VID<1>	GFX_VID<1> - @m78_lib.M78	16B3 22B8
GFX_VID<2>	GFX_VID<2> - @m78_lib.M78	16B3 22A8
GFX_VID<3>	GFX_VID<3> - @m78_lib.M78	16B3 22A8
GFX_VID<4>	GFX_VID<4> - @m78_lib.M78	16B3 22A8
GLAN_COMP	GLAN_COMP - @m78_lib.M78	23C6 104B3
GND_IMVP6_SGND	GND_IMVP6_SGND - @m78_lib.M78	71B6
GND_PP1V5REG_SGND	GND_PP1V5REG_SGND - @m78_lib.M78	73B7
GND_PP1V8REG_SGND	GND_PP1V8REG_SGND - @m78_lib.M78	75C5 75D6
GND_PP1V25REG_SGND	GND_PP1V25REG_SGND - @m78_lib.M78	74B7
GND_PP5VREG_SGND	GND_PP5VREG_SGND - @m78_lib.M78	76A7
GND_SMC_AVSS	GND_SMC_AVSS - @m78_lib.M78	49B2 50B7 53B2 53C6 53D2 53D6 58C4
GPU_BLU	GPU_BLU - @m78_lib.M78	85C4 91B8 108B3
GPU_BUF_HSYNC	GPU_BUF_HSYNC - @m78_lib.M78	108A3
GPU_BUF_VSYNC	GPU_BUF_VSYNC - @m78_lib.M78	108A3
GPU_DDC_A_CLK	GPU_DDC_A_CLK - @m78_lib.M78	85C7 94D1
GPU_DDC_A_DATA	GPU_DDC_A_DATA - @m78_lib.M78	85C7 94C1
GPU_DDC_C_CLK	GPU_DDC_C_CLK - @m78_lib.M78	85A4 85C1 90A8
GPU_DDC_C_DATA	GPU_DDC_C_DATA - @m78_lib.M78	85A4 85D1 90A6
GPU_DIGON	GPU_DIGON - @m78_lib.M78	85A4 90B8
GPU_ENABLE_BL	GPU_ENABLE_BL - @m78_lib.M78	85A5
GPU_GRN	GPU_GRN - @m78_lib.M78	85C4 91B8 108B3
GPU_H2SYNC	GPU_H2SYNC - @m78_lib.M78	85C7 91A4 108B3
GPU_HPD	GPU_HPD - @m78_lib.M78	85A7 94C1
GPU_HSK_THRMD_N	GPU_HSK_THRMD_N - @m78_lib.M78	55A5 55A6 108A3
GPU_HSK_THRMD_P	GPU_HSK_THRMD_P - @m78_lib.M78	55A6 55B5 108A3
GPU_HSYNC_BUF	GPU_HSYNC_BUF - @m78_lib.M78	91A3
GPU_PRESENT	GPU_PRESENT - @m78_lib.M78	6A8 28C1
	SB_GPIO6 - @m78_lib.M78	25A5 25C5 28C2
GPU_PRESENT_DRAIN	GPU_PRESENT_DRAIN - @m78_lib.M78	6B7
GPU_PRESENT_R	GPU_PRESENT_R - @m78_lib.M78	6B7
GPU_RED	GPU_RED - @m78_lib.M78	85C4 91B8 108B3
GPU_TV_C	GPU_TV_C - @m78_lib.M78	85C4 91B8 108B3
GPU_TV_COMP	GPU_TV_COMP - @m78_lib.M78	85C4 91B8 108B3
GPU_TV_Y	GPU_TV_Y - @m78_lib.M78	85C4 91B8 108B3
GPU_V2SYNC	GPU_V2SYNC - @m78_lib.M78	85C7 91B4 108A3
GPU_VARY_BL	GPU_VARY_BL - @m78_lib.M78	85A4 90B3
GPU_VSYNC_BUF	GPU_VSYNC_BUF - @m78_lib.M78	91B3
HDA_BIT_CLK	HDA_BIT_CLK - @m78_lib.M78	23C8 98C6 103C3
HDA_BIT_CLK_R	HDA_BIT_CLK_R - @m78_lib.M78	23C6 103C3
HDA_DOCK_EN_L	HDA_DOCK_EN_L - @m78_lib.M78	23B6
HDA_RST_L	HDA_RST_L - @m78_lib.M78	23C8 98C6 103C3
HDA_RST_L_R	HDA_RST_L_R - @m78_lib.M78	23C6 103C3
HDA_SDIN0	HDA_SDIN0 - @m78_lib.M78	23C8 98C6 103B3
HDA_SDIN_CODEC	HDA_SDIN_CODEC - @m78_lib.M78	103B3
HDA_SDOUT	HDA_SDOUT - @m78_lib.M78	23B8 98C6 103B3
HDA_SDOUT_R	HDA_SDOUT_R - @m78_lib.M78	23B6 103B3
HDA_SYNC	HDA_SYNC - @m78_lib.M78	23C8 98C6 103C3
HDA_SYNC_R	HDA_SYNC_R - @m78_lib.M78	23C6 103C3
HDD_THRMD_N	HDD_THRMD_N - @m78_lib.M78	55A5 55B7 108A3
HDD_THRMD_P	HDD_THRMD_P - @m78_lib.M78	55B5 55B7 108A3
IDE_CSEL	IDE_CSEL - @m78_lib.M78	44B5
IDE_DASP_L	IDE_DASP_L - @m78_lib.M78	44B5
IDE_DASP_L_DS	IDE_DASP_L_DS - @m78_lib.M78	44B6
IDE_IOCS16_PU	IDE_IOCS16_PU - @m78_lib.M78	44C4
IDE_IRQ14	IDE_IRQ14 - @m78_lib.M78	23B4 44C6 103D3
IDE_PDA<0>	IDE_PDA<0> - @m78_lib.M78	23B4 44B5
IDE_PDA<2..0>	IDE_PDA<2..0> - @m78_lib.M78	103D3
IDE_PDA<1>	IDE_PDA<1> - @m78_lib.M78	23B4 44B5
IDE_PDA<2>	IDE_PDA<2> - @m78_lib.M78	23B4 44B4
IDE_PDCS1_L	IDE_PDCS1_L - @m78_lib.M78	23B4 44B5 103D3
IDE_PDCS3_L	IDE_PDCS3_L - @m78_lib.M78	23B4 44B4 103D3
IDE_PDD<0>	IDE_PDD<0> - @m78_lib.M78	23C4 44C5
IDE_PDD<8..0>	IDE_PDD<8..0> - @m78_lib.M78	103D3
IDE_PDD<1>	IDE_PDD<1> - @m78_lib.M78	23C4 44C5
IDE_PDD<2>	IDE_PDD<2> - @m78_lib.M78	23B4 44C5
IDE_PDD<3>	IDE_PDD<3> - @m78_lib.M78	23B4 44C5
IDE_PDD<4>	IDE_PDD<4> - @m78_lib.M78	23B4 44C5
IDE_PDD<5>	IDE_PDD<5> - @m78_lib.M78	23B4 44C5
IDE_PDD<6>	IDE_PDD<6> - @m78_lib.M78	23B4 44C5
IDE_PDD<7>	IDE_PDD<7> - @m78_lib.M78	23B4 44C5
IDE_PDD<8>	IDE_PDD<8> - @m78_lib.M78	23B4 44C4
IDE_PDD<9>	IDE_PDD<9> - @m78_lib.M78	7B8 23B4 44C4 103D3
IDE_PDD<10>	IDE_PDD<10> - @m78_lib.M78	23B4 44C4
IDE_PDD<15..10>	IDE_PDD<15..10> - @m78_lib.M78	103D3
IDE_PDD<11>	IDE_PDD<11> - @m78_lib.M78	23B4 44C4
IDE_PDD<12>	IDE_PDD<12> - @m78_lib.M78	23B4 44C4
IDE_PDD<13>	IDE_PDD<13> - @m78_lib.M78	23B4 44C4
IDE_PDD<14>	IDE_PDD<14> - @m78_lib.M78	23B4 44C4
IDE_PDD<15>	IDE_PDD<15> - @m78_lib.M78	23B4 44C4
IDE_PDDACK_L	IDE_PDDACK_L - @m78_lib.M78	23B4 44C4 103D3
IDE_PDDREQ	IDE_PDDREQ - @m78_lib.M78	23A4 44B6 103D3
IDE_PDIORDY	IDE_PDIORDY - @m78_lib.M78	7B8 23A4 44C6 103D3
IDE_PDIOR_L	IDE_PDIOR_L - @m78_lib.M78	7C8 23B4 44C4 103D3
IDE_PDIOW_L	IDE_PDIOW_L - @m78_lib.M78	23B4 44C5 103D3
IMVP6_BOOT1	IMVP6_BOOT1 - @m78_lib.M78	71A6 71D4
IMVP6_BOOT1_RC	IMVP6_BOOT1_RC - @m78_lib.M78	71A6 71D4
IMVP6_BOOT2	IMVP6_BOOT2 - @m78_lib.M78	71A4 71C4
IMVP6_BOOT2_RC	IMVP6_BOOT2_RC - @m78_lib.M78	71A4 71C4

IMVP6_BOOT3	IMVP6_BOOT3 - @m78_lib.M78	72A7 72C6
IMVP6_BOOT3_RC	IMVP6_BOOT3_RC - @m78_lib.M78	72A7 72C5
IMVP6_COMP	IMVP6_COMP - @m78_lib.M78	71A8 71B7
IMVP6_COMP_RC	IMVP6_COMP_RC - @m78_lib.M78	71B8
IMVP6_DFB	IMVP6_DFB - @m78_lib.M78	71A8 71B5
IMVP6_DROOP	IMVP6_DROOP - @m78_lib.M78	71A8 71B4
IMVP6_FB	IMVP6_FB - @m78_lib.M78	71A8 71B7
IMVP6_FCCM	IMVP6_FCCM - @m78_lib.M78	71A8 71C5 72C7
IMVP6_FET_RC1	IMVP6_FET_RC1 - @m78_lib.M78	71A6 71C3
IMVP6_FET_RC2	IMVP6_FET_RC2 - @m78_lib.M78	71A4 71B3
IMVP6_FET_RC3	IMVP6_FET_RC3 - @m78_lib.M78	72A7 72C3
IMVP6_ISEN1	IMVP6_ISEN1 - @m78_lib.M78	71A6 71C3 72C1
IMVP6_ISEN2	IMVP6_ISEN2 - @m78_lib.M78	71A4 71C5
IMVP6_ISEN3	IMVP6_ISEN3 - @m78_lib.M78	71C5 72A7 72B1
IMVP6_LGATE1	IMVP6_LGATE1 - @m78_lib.M78	71A6 71D4
IMVP6_LGATE2	IMVP6_LGATE2 - @m78_lib.M78	71A4 71C4
IMVP6_LGATE3	IMVP6_LGATE3 - @m78_lib.M78	72A7 72C6
IMVP6_NTC	IMVP6_NTC - @m78_lib.M78	71C7
IMVP6_NTC_R	IMVP6_NTC_R - @m78_lib.M78	71C8
IMVP6_OCSET	IMVP6_OCSET - @m78_lib.M78	71A8 71B5
IMVP6_PHASE1	IMVP6_PHASE1 - @m78_lib.M78	71A6 71D4 108D1
IMVP6_PHASE2	IMVP6_PHASE2 - @m78_lib.M78	71A4 71C4 108D1
IMVP6_PHASE3	IMVP6_PHASE3 - @m78_lib.M78	72A7 72C6 108D1
IMVP6_PMON	IMVP6_PMON - @m78_lib.M78	53C8 71C5
IMVP6_PWM1	IMVP6_PWM1 - @m78_lib.M78	71A6 71D5
IMVP6_PWM2	IMVP6_PWM2 - @m78_lib.M78	71A4 71C5
IMVP6_PWM3	IMVP6_PWM3 - @m78_lib.M78	71C5 72A7 72C7
IMVP6_RBIAS	IMVP6_RBIAS - @m78_lib.M78	71A8 71B7
IMVP6_SOFT	IMVP6_SOFT - @m78_lib.M78	71A8 71C7
IMVP6_UGATE1	IMVP6_UGATE1 - @m78_lib.M78	71A6 71D4
IMVP6_UGATE2	IMVP6_UGATE2 - @m78_lib.M78	71A4 71C4
IMVP6_UGATE3	IMVP6_UGATE3 - @m78_lib.M78	72A7 72C6
IMVP6_VDIFF	IMVP6_VDIFF - @m78_lib.M78	71A8 71B7
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m78_lib.M78	71B8
IMVP6_VID<0>	IMVP6_VID<0> - @m78_lib.M78	12C1 71C7
IMVP6_VID<6..0>	IMVP6_VID<6..0> - @m78_lib.M78	100A3
IMVP6_VID<1>	IMVP6_VID<1> - @m78_lib.M78	12C1 71C7
IMVP6_VID<2>	IMVP6_VID<2> - @m78_lib.M78	12C1 71C7
IMVP6_VID<3>	IMVP6_VID<3> - @m78_lib.M78	12C1 71C7
IMVP6_VID<4>	IMVP6_VID<4> - @m78_lib.M78	12C1 71C7
IMVP6_VID<5>	IMVP6_VID<5> - @m78_lib.M78	12C1 71C7
IMVP6_VID<6>	IMVP6_VID<6> - @m78_lib.M78	12C1 71C7
IMVP6_VO	IMVP6_VO - @m78_lib.M78	71A8 71B4 72C1
IMVP6_VO1	IMVP6_VO1 - @m78_lib.M78	71A6 71D1
IMVP6_VO2	IMVP6_VO2 - @m78_lib.M78	71A4 71B1
IMVP6_VO3	IMVP6_VO3 - @m78_lib.M78	72A7 72C2
IMVP6_VO_R	IMVP6_VO_R - @m78_lib.M78	71B4
IMVP6_VR_TT_L	IMVP6_VR_TT_L - @m78_lib.M78	71C7
IMVP6_VSEN_N	IMVP6_VSEN_N - @m78_lib.M78	71A5 100A3
IMVP6_VSEN_P	IMVP6_VSEN_P - @m78_lib.M78	71A5 100A3
IMVP6_VSUM	IMVP6_VSUM - @m78_lib.M78	71A8 71C4 72B1
IMVP6_VSUM1	IMVP6_VSUM1 - @m78_lib.M78	71A6 71C2
IMVP6_VSUM2	IMVP6_VSUM2 - @m78_lib.M78	71A4 71B2
IMVP6_VSUM3	IMVP6_VSUM3 - @m78_lib.M78	72A7 72C3
IMVP6_VW	IMVP6_VW - @m78_lib.M78	71A8 71B7
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m78_lib.M78	71C7 100B3
IMVP_PGD_IN	IMVP_PGD_IN - @m78_lib.M78	70B3
IMVP_VR_ON	IMVP_VR_ON - @m78_lib.M78	7C4 49C8 71C7
INT_PIRQA_L	INT_PIRQA_L - @m78_lib.M78	24A4 24A8 104C3
INT_PIRQB_L	INT_PIRQB_L - @m78_lib.M78	24A4 24A8 104C3
INT_PIRQC_L	INT_PIRQC_L - @m78_lib.M78	24A4 24A8 104C3
INT_PIRQD_L	INT_PIRQD_L - @m78_lib.M78	24A4 24A8 104C3
INT_PIRQE_L	INT_PIRQE_L - @m78_lib.M78	24A4 24A6 104C3
INT_PIRQF_L	INT_PIRQF_L - @m78_lib.M78	24A4 24A6 104C3
INT_SERIRQ	INT_SERIRQ - @m78_lib.M78	7D4 25C8 49C8 51B4
INV_EN_BL_OR_PANEL_ID	INV_EN_BL_OR_PANEL_ID - @m78_lib.M78	6D6 28B2 85A3
ISENSE_CAL_EN	ISENSE_CAL_EN - @m78_lib.M78	49B8 50A2 53A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @m78_lib.M78	53B8
ISENSE_CAL_EN_LS12V	ISENSE_CAL_EN_LS12V - @m78_lib.M78	53B7
ISENSE_CAL_EN_L_R	ISENSE_CAL_EN_L_R - @m78_lib.M78	53B8
ITP_CPURST_L	ITP_CPURST_L - @m78_lib.M78	100A3
ITS_ALIVE	ITS_ALIVE - @m78_lib.M78	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @m78_lib.M78	6A8
LAN_ENERGY_DET	LAN_ENERGY_DET - @m78_lib.M78	23C6 28A2
	TP_LAN_ENERGY_DET - @m78_lib.M78	28A1
LAN_PHYPC	LAN_PHYPC - @m78_lib.M78	25A5 25C5
LCD_PWM	LCD_PWM - @m78_lib.M78	6D8 90B1
LCD_PWREN_DIV	LCD_PWREN_DIV - @m78_lib.M78	90C8
LCD_PWREN_L	LCD_PWREN_L - @m78_lib.M78	90B7
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @m78_lib.M78	90C7
LCD_SHOULD_ON	LCD_SHOULD_ON - @m78_lib.M78	6A6
LED4300_1	LED4300_1 - @m78_lib.M78	39A7
LED4301_1	LED4301_1 - @m78_lib.M78	39A7
LED4302_1	LED4302_1 - @m78_lib.M78	39A6
LED4303_1	LED4303_1 - @m78_lib.M78	39A6
LINDACARD_GPIO	LINDACARD_GPIO - @m78_lib.M78	7C4 25A7 25D5 51B4
LPC_AD<0>	LPC_AD<0> - @m78_lib.M78	7D4 23D4 49C8 51C6
LPC_AD<1>	LPC_AD<1> - @m78_lib.M78	7A8 7C6 7D4 23D4 49C8 51C6
LPC_AD<2>	LPC_AD<2> - @m78_lib.M78	7D4 23D4 49C8 51C4
LPC_AD<3>	LPC_AD<3> - @m78_lib.M78	7D4 23D4 49C8 51C4
LPC_FRAME_L	LPC_FRAME_L - @m78_lib.M78	7D4 23D4 49C8 51B6
LVDS_A_CLK_N	LVDS_A_CLK_N - @m78_lib.M78	15C5 22D8
	TP_LVDS_A_CLK_N - @m78_lib.M78	22D7
LVDS_A_CLK_P	LVDS_A_CLK_P - @m78_lib.M78	15C5 22D8
	TP_LVDS_A_CLK_P - @m78_lib.M78	22D7
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m78_lib.M78	15C5 22D8
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m78_lib.M78	15C5 22C8
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m78_lib.M78	15C5 22C8
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m78_lib.M78	15C5 22C8
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m78_lib.M78	15C5 22C8
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m78_lib.M78	15C5 22C8
LVDS_BKLT_CTL	LVDS_BKLT_CTL - @m78_lib.M78	15D5 22D8
	TP_LVDS_BKLT_CTL - @m78_lib.M78	22D7
LVDS_BKLT_EN	LVDS_BKLT_EN - @m78_lib.M78	15D5 22D8
	TP_LVDS_BKLT_EN - @m78_lib.M78	22D7
LVDS_B_CLK_N	LVDS_B_CLK_N - @m78_lib.M78	15C5 22D8
	TP_LVDS_B_CLK_N - @m78_lib.M78	22D7
LVDS_B_CLK_P	LVDS_B_CLK_P - @m78_lib.M78	15C5 22D8
	TP_LVDS_B_CLK_P - @m78_lib.M78	22D7
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m78_lib.M78	15C5 22C8
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m78_lib.M78	15C5 22C8
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m78_lib.M78	15C5 22C8
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m78_lib.M78	15C5 22C8
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m78_lib.M78	15C5 22C8
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m78_lib.M78	15C5 22C8
LVDS_IBG	LVDS_IBG - @m78_lib.M78	15D5 22D8
	TP_LVDS_IBG - @m78_lib.M78	22D7
LVDS_L_CLK_N	LVDS_L_CLK_N - @m78_lib.M78	85B4 90A6 108C3
LVDS_L_CLK_P	LVDS_L_CLK_P - @m78_lib.M78	85B4 90A8 108C3
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @m78_lib.M78	85A4 90A6
LVDS_L_DATA_N<3..0>	LVDS_L_DATA_N<3..0> - @m78_lib.M78	108C3
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @m78_lib.M78	85B4 90A8
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @m78_lib.M78	85B4 90A6
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @m78_lib.M78	85B4 90A6
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @m78_lib.M78	85A4 90A8
LVDS_L_DATA_P<3..0>	LVDS_L_DATA_P<3..0> - @m78_lib.M78	108C3
LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @m78_lib.M78	85B4 90A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @m78_lib.M78	85B4 90A8
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @m78_lib.M78	85B4 90A8
LVDS_U_CLK_N	LVDS_U_CLK_N - @m78_lib.M78	85B4 90A6 108C3
LVDS_U_CLK_P	LVDS_U_CLK_P - @m78_lib.M78	85B4 90A8 108C3
LVDS_U_DATA_N<0>	LVDS_U_DATA_N<0> - @m78_lib.M78	85B4 90A8
LVDS_U_DATA_N<3..0>	LVDS_U_DATA_N<3..0> - @m78_lib.M78	108C3
LVDS_U_DATA_N<1>	LVDS_U_DATA_N<1> - @m78_lib.M78	85B4 90A8
LVDS_U_DATA_N<2>	LVDS_U_DATA_N<2> - @m78_lib.M78	85B4 90A8
LVDS_U_DATA_N<3>	LVDS_U_DATA_N<3> - @m78_lib.M78	85B4 90A6
LVDS_U_DATA_P<0>	LVDS_U_DATA_P<0> - @m78_lib.M78	85B4 90A6
LVDS_U_DATA_P<3..0>	LVDS_U_DATA_P<3..0> - @m78_lib.M78	108C3
LVDS_U_DATA_P<1>	LVDS_U_DATA_P<1> - @m78_lib.M78	85B4 90A6
LVDS_U_DATA_P<2>	LVDS_U_DATA_P<2> - @m78_lib.M78	85B4 90A6
LVDS_U_DATA_P<3>	LVDS_U_DATA_P<3> - @m78_lib.M78	85B4 90A8
LVDS_VDD_EN	LVDS_VDD_EN - @m78_lib.M78	15D5 22D8
	TP_LVDS_VDD_EN - @m78_lib.M78	22D7
LVDS_VREFH	LVDS_VREFH - @m78_lib.M78	15D5 22D8
	TP_LVDS_VREFH - @m78_lib.M78	22D7
LVDS_VREFL	LVDS_VREFL - @m78_lib.M78	15D5 22D8
	TP_LVDS_VREFL - @m78_lib.M78	22D7
MCH_CORES0_BOOT	MCH_CORES0_BOOT - @m78_lib.M78	74C4
MCH_CORES0_BOOT_R	MCH_CORES0_BOOT_R - @m78_lib.M78	74C3
MCH_CORES0_ISEN	MCH_CORES0_ISEN - @m78_lib.M78	74C4
MCH_CORES0_LGATE	MCH_CORES0_LGATE - @m78_lib.M78	74C3
MCH_CORES0_OCSET	MCH_CORES0_OCSET - @m78_lib.M78	74B4
MCH_CORES0_SNUBBER_R	MCH_CORES0_SNUBBER_R - @m78_lib.M78	74C2
MCH_CORES0_SOFT	MCH_CORES0_SOFT - @m78_lib.M78	74C4
MCH_CORES0_SWITCHNODE	MCH_CORES0_SWITCHNODE - @m78_lib.M78	74C3 108D1
MCH_CORES0_UGATE	MCH_CORES0_UGATE - @m78_lib.M78	74C4
MCH_CORES0_VSEN	MCH_CORES0_VSEN - @m78_lib.M78	74B3
MEMVTT_VREF	MEMVTT_VREF - @m78_lib.M78	75A4
MEM_A_A<0>	MEM_A_A<0> - @m78_lib.M78	17C5 31B3 33C6
MEM_A_A<14..0>	MEM_A_A<14..0> - @m78_lib.M78	102D3
MEM_A_A<1>	MEM_A_A<1> - @m78_lib.M78	17C5 31B6 33C6
MEM_A_A<2>	MEM_A_A<2> - @m78_lib.M78	17B5 31B3 33C6
MEM_A_A<3>	MEM_A_A<3> - @m78_lib.M78	17B5 31B6 33C6
MEM_A_A<4>	MEM_A_A<4> - @m78_lib.M78	17B5 31C3 33C6
MEM_A_A<5>	MEM_A_A<5> - @m78_lib.M78	17B5 31C6 33C6
MEM_A_A<6>	MEM_A_A<6> - @m78_lib.M78	17B5 31C3 33C6
MEM_A_A<7>	MEM_A_A<7> - @m78_lib.M78	17B5 31C3 33C6
MEM_A_A<8>	MEM_A_A<8> - @m78_lib.M78	17B5 31C6 33C6
MEM_A_A<9>	MEM_A_A<9> - @m78_lib.M78	17B5 31C6 33C6
MEM_A_A<10>	MEM_A_A<10> - @m78_lib.M78	17B5 31B6 33C6
MEM_A_A<11>	MEM_A_A<11> - @m78_lib.M78	17B5 31C3 33C6
MEM_A_A<12>	MEM_A_A<12> - @m78_lib.M78	17B5 31C6 33C6
MEM_A_A<13>	MEM_A_A<13> - @m78_lib.M78	17B5 31B3 33C6
MEM_A_A<14>	MEM_A_A<14> - @m78_lib.M78	16C6 31C3 33C6
MEM_A_BS<0>	MEM_A_BS<0> - @m78_lib.M78	17D5 31B6 33B6
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @m78_lib.M78	102D3
MEM_A_BS<1>	MEM_A_BS<1> - @m78_lib.M78	17D5 31B3 33B6
MEM_A_BS<2>	MEM_A_BS<2> - @m78_lib.M78	17D5 31C6 33B6
MEM_A_CAS_L	MEM_A_CAS_L - @m78_lib.M78	17D5 31B6 33B6 102D3
MEM_A_DM<0>	MEM_A_DM<0> - @m78_lib.M78	17D5 31D3 102C3
MEM_A_DM<1>	MEM_A_DM<1> - @m78_lib.M78	17D5 31D3 102C3
MEM_A_DM<2>	MEM_A_DM<2> - @m78_lib.M78	17C5 31C3 102C3
MEM_A_DM<3>	MEM_A_DM<3> - @m78_lib.M78	17C5 31C6 102C3
MEM_A_DM<4>	MEM_A_DM<4> - @m78_lib.M78	17C5 31B3 102C3
MEM_A_DM<5>	MEM_A_DM<5> - @m78_lib.M78	17C5 31B6 102C3
MEM_A_DM<6>	MEM_A_DM<6> - @m78_lib.M78	17C5 31A3 102C3
MEM_A_DM<7>	MEM_A_DM<7> - @m78_lib.M78	17C5 31A6 102C3
MEM_A_DQ<0>	MEM_A_DQ<0> - @m78_lib.M78	17D8 31D6
MEM_A_DQ<6..0>	MEM_A_DQ<6..0> - @m78_lib.M78	102D3
MEM_A_DQ<1>	MEM_A_DQ<1> - @m78_lib.M78	17D8 31D6
MEM_A_DQ<2>	MEM_A_DQ<2> - @m78_lib.M78	17D8 31D6
MEM_A_DQ<3>	MEM_A_DQ<3> - @m78_lib.M78	17D8 31D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @m78_lib.M78	17D8 31D3
MEM_A_DQ<5>	MEM_A_DQ<5> - @m78_lib.M78	17D8 31D3
MEM_A_DQ<6>	MEM_A_DQ<6> - @m78_lib.M78	17D8 31D3
MEM_A_DQ<7>	MEM_A_DQ<7> - @m78_lib.M78	7C7 17D8 31D3 102D3
MEM_A_DQ<8>	MEM_A_DQ<8> - @m78_lib.M78	17C8 31D6
MEM_A_DQ<13..8>	MEM_A_DQ<13..8> - @m78_lib.M78	102D3
MEM_A_DQ<9>	MEM_A_DQ<9> - @m78_lib.M78	17C8 31D6
MEM_A_DQ<10>	MEM_A_DQ<10> - @m78_lib.M78	17C8 31D6
MEM_A_DQ<11>	MEM_A_DQ<11> - @m78_lib.M78	17C8 31D6
MEM_A_DQ<12>	MEM_A_DQ<12> - @m78_lib.M78	17C8 31D3
MEM_A_DQ<13>	MEM_A_DQ<13> - @m78_lib.M78	17C8 31D3
MEM_A_DQ<14>	MEM_A_DQ<14> - @m78_lib.M78	7C7 17C8 31D3 102D3
MEM_A_DQ<15>	MEM_A_DQ<15> - @m78_lib.M78	17C8 31D3 102C3
MEM_A_DQ<16>	MEM_A_DQ<16> - @m78_lib.M78	7B7 17C8 31D6 102C3
MEM_A_DQ<17>	MEM_A_DQ<17> - @m78_lib.M78	17C8 31D6
MEM_A_DQ<23..17>	MEM_A_DQ<23..17> - @m78_lib.M78	102C3
MEM_A_DQ<18>	MEM_A_DQ<18> - @m78_lib.M78	17C8 31C6
MEM_A_DQ<19>	MEM_A_DQ<19> - @m78_lib.M78	17C8 31C6
MEM_A_DQ<20>	MEM_A_DQ<20> - @m78_lib.M78	17C8 31D3
MEM_A_DQ<21>	MEM_A_DQ<21> - @m78_lib.M78	17C8 31D3
MEM_A_DQ<22>	MEM_A_DQ<22> - @m78_lib.M78	17C8 31C3
MEM_A_DQ<23>	MEM_A_DQ<23> - @m78_lib.M78	17C8 31C3
MEM_A_DQ<24>	MEM_A_DQ<24> - @m78_lib.M78	17C8 31C6 102C3
MEM_A_DQ<25>	MEM_A_DQ<25> - @m78_lib.M78	7B7 17C8 31C6 102C3
MEM_A_DQ<26>	MEM_A_DQ<26> - @m78_lib.M78	17C8 31C6
MEM_A_DQ<31..26>	MEM_A_DQ<31..26> - @m78_lib.M78	102C3
MEM_A_DQ<27>	MEM_A_DQ<27> - @m78_lib.M78	17C8 31C6
MEM_A_DQ<28>	MEM_A_DQ<28> - @m78_lib.M78	17C8 31C3
MEM_A_DQ<29>	MEM_A_DQ<29> - @m78_lib.M78	17C8 31C3
MEM_A_DQ<30>	MEM_A_DQ<30> - @m78_lib.M78	17C8 31C3
MEM_A_DQ<31>	MEM_A_DQ<31> - @m78_lib.M78	17C8 31C3
MEM_A_DQ<32>	MEM_A_DQ<32> - @m78_lib.M78	17C8 31B6
MEM_A_DQ<38..32>	MEM_A_DQ<38..32> - @m78_lib.M78	102C3
MEM_A_DQ<33>	MEM_A_DQ<33> - @m78_lib.M78	17C8 31B6
MEM_A_DQ<34>	MEM_A_DQ<34> - @m78_lib.M78	17B8 31B6
MEM_A_DQ<35>	MEM_A_DQ<35> - @m78_lib.M78	17B8 31B6
MEM_A_DQ<36>	MEM_A_DQ<36> - @m78_lib.M78	17B8 31B3
MEM_A_DQ<37>	MEM_A_DQ<37> - @m78_lib.M78	17B8 31B3
MEM_A_DQ<38>	MEM_A_DQ<38> - @m78_lib.M78	17B8 31B3
MEM_A_DQ<39>	MEM_A_DQ<39> - @m78_lib.M78	7B7 17B8 31B3 102C3
MEM_A_DQ<40>	MEM_A_DQ<40> - @m78_lib.M78	17B8 31B6
MEM_A_DQ<46..40>	MEM_A_DQ<46..40> - @m78_lib.M78	102C3
MEM_A_DQ<41>	MEM_A_DQ<41> - @m78_lib.M78	17B8 31B6
MEM_A_DQ<42>	MEM_A_DQ<42> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<43>	MEM_A_DQ<43> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<44>	MEM_A_DQ<44> - @m78_lib.M78	17B8 31B3
MEM_A_DQ<45>	MEM_A_DQ<45> - @m78_lib.M78	17B8 31B3
MEM_A_DQ<46>	MEM_A_DQ<46> - @m78_lib.M78	17B8 31A3
MEM_A_DQ<47>	MEM_A_DQ<47> - @m78_lib.M78	7B7 17B8 31A3 102C3
MEM_A_DQ<48>	MEM_A_DQ<48> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<53..48>	MEM_A_DQ<53..48> - @m78_lib.M78	102C3
MEM_A_DQ<49>	MEM_A_DQ<49> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<50>	MEM_A_DQ<50> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<51>	MEM_A_DQ<51> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<52>	MEM_A_DQ<52> - @m78_lib.M78	17B8 31A3
MEM_A_DQ<53>	MEM_A_DQ<53> - @m78_lib.M78	17B8 31A3
MEM_A_DQ<54>	MEM_A_DQ<54> - @m78_lib.M78	7B7 17B8 31A3 102C3
MEM_A_DQ<55>	MEM_A_DQ<55> - @m78_lib.M78	17B8 31A3 102C3
MEM_A_DQ<56>	MEM_A_DQ<56> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<58..56>	MEM_A_DQ<58..56> - @m78_lib.M78	102C3
MEM_A_DQ<57>	MEM_A_DQ<57> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<58>	MEM_A_DQ<58> - @m78_lib.M78	17B8 31A6
MEM_A_DQ<59>	MEM_A_DQ<59> - @m78_lib.M78	7B7 17B8 31A6 102C3
MEM_A_DQ<60>	MEM_A_DQ<60> - @m78_lib.M78	17A8 31A3
MEM_A_DQ<63..60>	MEM_A_DQ<63..60> - @m78_lib.M78	102C3
MEM_A_DQ<61>	MEM_A_DQ<61> - @m78_lib.M78	17A8 31A3
MEM_A_DQ<62>	MEM_A_DQ<62> - @m78_lib.M78	17A8 31A3
MEM_A_DQ<63>	MEM_A_DQ<63> - @m78_lib.M78	17A8 31A3
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @m78_lib.M78	7B7 17C5 31D6 102B3
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @m78_lib.M78	7B7 17C5 31D6 102B3
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @m78_lib.M78	7B7 17C5 31C6 102B3
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @m78_lib.M78	7B7 17C5 31C3 102B3
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @m78_lib.M78	7B7 17C5 31B6 102B3
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @m78_lib.M78	7B7 17C5 31B3 102B3
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @m78_lib.M78	7B7 17C5 31A6 102B3
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @m78_lib.M78	7B7 17C5 31A3 102B3
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @m78_lib.M78	7B7 17C5 31D6 102B3
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @m78_lib.M78	7B7 17C5 31D6 102B3
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @m78_lib.M78	7B7 17C5 31C6 102B3
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @m78_lib.M78	7B7 17C5 31C3 102B3
MEM_A_DQS_P<4>	MEM_A_DQS_P<4> - @m78_lib.M78	7B7 17C5 31B6 102B3
MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @m78_lib.M78	7B7 17C5 31B3 102B3
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @m78_lib.M78	7B7 17C5 31A6 102B3
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @m78_lib.M78	7B7 17C5 31A3 102B3
MEM_A_RAS_L	MEM_A_RAS_L - @m78_lib.M78	17B5 31B3 33B6 102D3
MEM_A_SA<0>	MEM_A_SA<0> - @m78_lib.M78	31A4
MEM_A_SA<1>	MEM_A_SA<1> - @m78_lib.M78	31A4
MEM_A_WE_L	MEM_A_WE_L - @m78_lib.M78	17B5 31B6 33B6 102D3
MEM_B_A<0>	MEM_B_A<0> - @m78_lib.M78	17C1 32B3 33B6
MEM_B_A<14..0>	MEM_B_A<14..0> - @m78_lib.M78	102D1
MEM_B_A<1>	MEM_B_A<1> - @m78_lib.M78	17C1 32B6 33B6
MEM_B_A<2>	MEM_B_A<2> - @m78_lib.M78	17B1 32B3 33B6
MEM_B_A<3>	MEM_B_A<3> - @m78_lib.M78	17B1 32B6 33B6
MEM_B_A<4>	MEM_B_A<4> - @m78_lib.M78	17B1 32C3 33B6
MEM_B_A<5>	MEM_B_A<5> - @m78_lib.M78	17B1 32C6 33B6
MEM_B_A<6>	MEM_B_A<6> - @m78_lib.M78	17B1 32C3 33B6
MEM_B_A<7>	MEM_B_A<7> - @m78_lib.M78	17B1 32C3 33B6
MEM_B_A<8>	MEM_B_A<8> - @m78_lib.M78	17B1 32C6 33B6
MEM_B_A<9>	MEM_B_A<9> - @m78_lib.M78	17B1 32C6 33B6
MEM_B_A<10>	MEM_B_A<10> - @m78_lib.M78	17B1 32B6 33B6
MEM_B_A<11>	MEM_B_A<11> - @m78_lib.M78	17B1 32C3 33A6
MEM_B_A<12>	MEM_B_A<12> - @m78_lib.M78	17B1 32C6 33A6
MEM_B_A<13>	MEM_B_A<13> - @m78_lib.M78	17B1 32B3 33A6
MEM_B_A<14>	MEM_B_A<14> - @m78_lib.M78	16C6 32C3 33A6
MEM_B_BS<0>	MEM_B_BS<0> - @m78_lib.M78	17D1 32B6 33A6
MEM_B_BS<2..0>	MEM_B_BS<2..0> - @m78_lib.M78	102D1
MEM_B_BS<1>	MEM_B_BS<1> - @m78_lib.M78	17D1 32B3 33A6
MEM_B_BS<2>	MEM_B_BS<2> - @m78_lib.M78	17D1 32C6 33A6
MEM_B_CAS_L	MEM_B_CAS_L - @m78_lib.M78	17D1 32B6 33A6 102D1
MEM_B_DM<0>	MEM_B_DM<0> - @m78_lib.M78	17D1 32D3 102C1
MEM_B_DM<1>	MEM_B_DM<1> - @m78_lib.M78	17D1 32D3 102C1
MEM_B_DM<2>	MEM_B_DM<2> - @m78_lib.M78	17C1 32C3 102C1
MEM_B_DM<3>	MEM_B_DM<3> - @m78_lib.M78	17C1 32C6 102C1
MEM_B_DM<4>	MEM_B_DM<4> - @m78_lib.M78	17C1 32B3 102C1
MEM_B_DM<5>	MEM_B_DM<5> - @m78_lib.M78	17C1 32B6 102C1
MEM_B_DM<6>	MEM_B_DM<6> - @m78_lib.M78	17C1 32A3 102C1
MEM_B_DM<7>	MEM_B_DM<7> - @m78_lib.M78	17C1 32A6 102C1
MEM_B_DQ<0>	MEM_B_DQ<0> - @m78_lib.M78	17D4 32D6
MEM_B_DQ<5..0>	MEM_B_DQ<5..0> - @m78_lib.M78	102D1
MEM_B_DQ<1>	MEM_B_DQ<1> - @m78_lib.M78	17D4 32D6
MEM_B_DQ<2>	MEM_B_DQ<2> - @m78_lib.M78	17D4 32D6
MEM_B_DQ<3>	MEM_B_DQ<3> - @m78_lib.M78	17D4 32D6
MEM_B_DQ<4>	MEM_B_DQ<4> - @m78_lib.M78	17D4 32D3
MEM_B_DQ<5>	MEM_B_DQ<5> - @m78_lib.M78	17D4 32D3
MEM_B_DQ<6>	MEM_B_DQ<6> - @m78_lib.M78	7B7 17D4 32D3 102D1
MEM_B_DQ<7>	MEM_B_DQ<7> - @m78_lib.M78	17D4 32D3 102D1
MEM_B_DQ<8>	MEM_B_DQ<8> - @m78_lib.M78	7B7 17C4 32D6 102D1
MEM_B_DQ<9>	MEM_B_DQ<9> - @m78_lib.M78	17C4 32D6
MEM_B_DQ<15..9>	MEM_B_DQ<15..9> - @m78_lib.M78	102D1
MEM_B_DQ<10>	MEM_B_DQ<10> - @m78_lib.M78	17C4 32D6
MEM_B_DQ<11>	MEM_B_DQ<11> - @m78_lib.M78	17C4 32D6
MEM_B_DQ<12>	MEM_B_DQ<12> - @m78_lib.M78	17C4 32D3
MEM_B_DQ<13>	MEM_B_DQ<13> - @m78_lib.M78	17C4 32D3
MEM_B_DQ<14>	MEM_B_DQ<14> - @m78_lib.M78	17C4 32D3
MEM_B_DQ<15>	MEM_B_DQ<15> - @m78_lib.M78	17C4 32D3
MEM_B_DQ<16>	MEM_B_DQ<16> - @m78_lib.M78	17C4 32D6
MEM_B_DQ<22..16>	MEM_B_DQ<22..16> - @m78_lib.M78	102D1
MEM_B_DQ<17>	MEM_B_DQ<17> - @m78_lib.M78	17C4 32D6
MEM_B_DQ<18>	MEM_B_DQ<18> - @m78_lib.M78	17C4 32C6
MEM_B_DQ<19>	MEM_B_DQ<19> - @m78_lib.M78	17C4 32C6
MEM_B_DQ<20>	MEM_B_DQ<20> - @m78_lib.M78	17C4 32D3
MEM_B_DQ<21>	MEM_B_DQ<21> - @m78_lib.M78	17C4 32D3
MEM_B_DQ<22>	MEM_B_DQ<22> - @m78_lib.M78	17C4 32C3
MEM_B_DQ<23>	MEM_B_DQ<23> - @m78_lib.M78	7B7 17C4 32C3 102D1
MEM_B_DQ<24>	MEM_B_DQ<24> - @m78_lib.M78	17C4 32C6 102C1
MEM_B_DQ<25>	MEM_B_DQ<25> - @m78_lib.M78	7B7 17C4 32C6 102C1
MEM_B_DQ<26>	MEM_B_DQ<26> - @m78_lib.M78	17C4 32C6
MEM_B_DQ<31..26>	MEM_B_DQ<31..26> - @m78_lib.M78	102C1
MEM_B_DQ<27>	MEM_B_DQ<27> - @m78_lib.M78	17C4 32C6
MEM_B_DQ<28>	MEM_B_DQ<28> - @m78_lib.M78	17C4 32C3
MEM_B_DQ<29>	MEM_B_DQ<29> - @m78_lib.M78	17C4 32C3
MEM_B_DQ<30>	MEM_B_DQ<30> - @m78_lib.M78	17C4 32C3
MEM_B_DQ<31>	MEM_B_DQ<31> - @m78_lib.M78	17C4 32C3
MEM_B_DQ<32>	MEM_B_DQ<32> - @m78_lib.M78	17C4 32B6
MEM_B_DQ<37..32>	MEM_B_DQ<37..32> - @m78_lib.M78	102C1
MEM_B_DQ<33>	MEM_B_DQ<33> - @m78_lib.M78	17C4 32B6
MEM_B_DQ<34>	MEM_B_DQ<34> - @m78_lib.M78	17B4 32B6
MEM_B_DQ<35>	MEM_B_DQ<35> - @m78_lib.M78	17B4 32B6
MEM_B_DQ<36>	MEM_B_DQ<36> - @m78_lib.M78	17B4 32B3
MEM_B_DQ<37>	MEM_B_DQ<37> - @m78_lib.M78	17B4 32B3
MEM_B_DQ<38>	MEM_B_DQ<38> - @m78_lib.M78	7A7 17B4 32B3 102C1
MEM_B_DQ<39>	MEM_B_DQ<39> - @m78_lib.M78	17B4 32B3 102C1
MEM_B_DQ<40>	MEM_B_DQ<40> - @m78_lib.M78	17B4 32B6
MEM_B_DQ<43..40>	MEM_B_DQ<43..40> - @m78_lib.M78	102C1
MEM_B_DQ<41>	MEM_B_DQ<41> - @m78_lib.M78	17B4 32B6
MEM_B_DQ<42>	MEM_B_DQ<42> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<43>	MEM_B_DQ<43> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<44>	MEM_B_DQ<44> - @m78_lib.M78	7A7 17B4 32B3 102C1
MEM_B_DQ<45>	MEM_B_DQ<45> - @m78_lib.M78	17B4 32B3
MEM_B_DQ<47..45>	MEM_B_DQ<47..45> - @m78_lib.M78	102C1
MEM_B_DQ<46>	MEM_B_DQ<46> - @m78_lib.M78	17B4 32A3
MEM_B_DQ<47>	MEM_B_DQ<47> - @m78_lib.M78	17B4 32A3
MEM_B_DQ<48>	MEM_B_DQ<48> - @m78_lib.M78	7A7 17B4 32A6 102C1
MEM_B_DQ<49>	MEM_B_DQ<49> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<55..49>	MEM_B_DQ<55..49> - @m78_lib.M78	102C1
MEM_B_DQ<50>	MEM_B_DQ<50> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<51>	MEM_B_DQ<51> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<52>	MEM_B_DQ<52> - @m78_lib.M78	17B4 32A3
MEM_B_DQ<53>	MEM_B_DQ<53> - @m78_lib.M78	17B4 32A3
MEM_B_DQ<54>	MEM_B_DQ<54> - @m78_lib.M78	17B4 32A3
MEM_B_DQ<55>	MEM_B_DQ<55> - @m78_lib.M78	17B4 32A3
MEM_B_DQ<56>	MEM_B_DQ<56> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<61..56>	MEM_B_DQ<61..56> - @m78_lib.M78	102C1
MEM_B_DQ<57>	MEM_B_DQ<57> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<58>	MEM_B_DQ<58> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<59>	MEM_B_DQ<59> - @m78_lib.M78	17B4 32A6
MEM_B_DQ<60>	MEM_B_DQ<60> - @m78_lib.M78	17A4 32A3
MEM_B_DQ<61>	MEM_B_DQ<61> - @m78_lib.M78	17A4 32A3
MEM_B_DQ<62>	MEM_B_DQ<62> - @m78_lib.M78	7A7 17A4 32A3 102C1
MEM_B_DQ<63>	MEM_B_DQ<63> - @m78_lib.M78	17A4 32A3 102C1
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @m78_lib.M78	7A7 17C1 32D6 102B1
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @m78_lib.M78	7A7 17C1 32D6 102B1
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @m78_lib.M78	7A7 17C1 32C6 102B1
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @m78_lib.M78	7A7 17C1 32C3 102B1
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @m78_lib.M78	7A7 17C1 32B6 102B1
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @m78_lib.M78	7A7 17C1 32B3 102B1
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @m78_lib.M78	7A7 17C1 32A6 102B1
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @m78_lib.M78	7A7 17C1 32A3 102B1
MEM_B_DQS_P<0>	MEM_B_DQS_P<0> - @m78_lib.M78	7A7 17C1 32D6 102B1
MEM_B_DQS_P<1>	MEM_B_DQS_P<1> - @m78_lib.M78	7A7 17C1 32D6 102B1
MEM_B_DQS_P<2>	MEM_B_DQS_P<2> - @m78_lib.M78	7A7 17C1 32C6 102B1
MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @m78_lib.M78	7A7 17C1 32C3 102B1
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @m78_lib.M78	7A7 17C1 32B6 102B1
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @m78_lib.M78	7A7 17C1 32B3 102B1
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @m78_lib.M78	7A7 17C1 32A6 102B1
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @m78_lib.M78	7A7 17C1 32A3 102B1
MEM_B_RAS_L	MEM_B_RAS_L - @m78_lib.M78	17B1 32B3 33A6 102D1
MEM_B_SA<0>	MEM_B_SA<0> - @m78_lib.M78	32A4
MEM_B_SA<1>	MEM_B_SA<1> - @m78_lib.M78	32A4
MEM_B_WE_L	MEM_B_WE_L - @m78_lib.M78	17B1 32B6 33A6 102D1
MEM_CKE<0>	MEM_CKE<0> - @m78_lib.M78	16D3 31C6 33D6
MEM_CKE<1..0>	MEM_CKE<1..0> - @m78_lib.M78	102D3
MEM_CKE<1>	MEM_CKE<1> - @m78_lib.M78	16D3 31C3 33D6
MEM_CKE<3>	MEM_CKE<3> - @m78_lib.M78	16D3 32C6 33D6
MEM_CKE<4..3>	MEM_CKE<4..3> - @m78_lib.M78	102D1
MEM_CKE<4>	MEM_CKE<4> - @m78_lib.M78	16D3 32C3 33D6
MEM_CLK_N<0>	MEM_CLK_N<0> - @m78_lib.M78	16D3 31D3
MEM_CLK_N<1..0>	MEM_CLK_N<1..0> - @m78_lib.M78	102D3
MEM_CLK_N<1>	MEM_CLK_N<1> - @m78_lib.M78	16D3 31A3
MEM_CLK_N<3>	MEM_CLK_N<3> - @m78_lib.M78	16D3 32D3
MEM_CLK_N<4..3>	MEM_CLK_N<4..3> - @m78_lib.M78	102D1
MEM_CLK_N<4>	MEM_CLK_N<4> - @m78_lib.M78	16D3 32A3
MEM_CLK_P<0>	MEM_CLK_P<0> - @m78_lib.M78	16D3 31D3
MEM_CLK_P<1..0>	MEM_CLK_P<1..0> - @m78_lib.M78	102D3
MEM_CLK_P<1>	MEM_CLK_P<1> - @m78_lib.M78	16D3 31A3
MEM_CLK_P<3>	MEM_CLK_P<3> - @m78_lib.M78	16D3 32D3
MEM_CLK_P<4..3>	MEM_CLK_P<4..3> - @m78_lib.M78	102D1
MEM_CLK_P<4>	MEM_CLK_P<4> - @m78_lib.M78	16D3 32A3
MEM_CS_L<0>	MEM_CS_L<0> - @m78_lib.M78	16D3 31B3 33D6
MEM_CS_L<1..0>	MEM_CS_L<1..0> - @m78_lib.M78	102D3
MEM_CS_L<1>	MEM_CS_L<1> - @m78_lib.M78	16D3 31B6 33D6
MEM_CS_L<2>	MEM_CS_L<2> - @m78_lib.M78	16D3 32B3 33D6
MEM_CS_L<3..2>	MEM_CS_L<3..2> - @m78_lib.M78	102D1
MEM_CS_L<3>	MEM_CS_L<3> - @m78_lib.M78	16C3 32B6 33D6
MEM_ODT<0>	MEM_ODT<0> - @m78_lib.M78	16C3 31B3 33C6
MEM_ODT<1..0>	MEM_ODT<1..0> - @m78_lib.M78	102D3
MEM_ODT<1>	MEM_ODT<1> - @m78_lib.M78	16C3 31B6 33C6
MEM_ODT<2>	MEM_ODT<2> - @m78_lib.M78	16C3 32B3 33C6
MEM_ODT<3..2>	MEM_ODT<3..2> - @m78_lib.M78	102D1
MEM_ODT<3>	MEM_ODT<3> - @m78_lib.M78	16C3 32B6 33C6
MEM_RCOMP	MEM_RCOMP - @m78_lib.M78	16C4
MEM_RCOMP_L	MEM_RCOMP_L - @m78_lib.M78	16C4
MEM_RCOMP_VOH	MEM_RCOMP_VOH - @m78_lib.M78	16C4
MEM_RCOMP_VOL	MEM_RCOMP_VOL - @m78_lib.M78	16C4
MINI_RESET_L	MINI_RESET_L - @m78_lib.M78	28D1 34C3
MXM_DETECT_L	MXM_DETECT_L - @m78_lib.M78	85C4
MXM_PIN170	MXM_PIN170 - @m78_lib.M78	85B5
MXM_PWRSRC_SENSE	MXM_PWRSRC_SENSE - @m78_lib.M78	53C3
MXM_ROM_WP	MXM_ROM_WP - @m78_lib.M78	85C3
MXM_SENSE_I_R	MXM_SENSE_I_R - @m78_lib.M78	53C3
NB_BSEL<0>	NB_BSEL<0> - @m78_lib.M78	13C6 16C6 30C8 100B3
NB_BSEL<1>	NB_BSEL<1> - @m78_lib.M78	13C6 16C6 30B8 100B3
NB_BSEL<2>	NB_BSEL<2> - @m78_lib.M78	13C3 16B6 30B8 100A3
NB_CFG<3>	NB_CFG<3> - @m78_lib.M78	13C3 16B6
NB_CFG<4>	NB_CFG<4> - @m78_lib.M78	13C6 16B6
NB_CFG<5>	NB_CFG<5> - @m78_lib.M78	13C6 16B6 16D7
NB_CFG<6>	NB_CFG<6> - @m78_lib.M78	13C6 16B6
NB_CFG<7>	NB_CFG<7> - @m78_lib.M78	13C6 16B6
NB_CFG<8>	NB_CFG<8> - @m78_lib.M78	13C3 16B6
NB_CFG<9>	NB_CFG<9> - @m78_lib.M78	16B6 16D7
NB_CFG<16>	NB_CFG<16> - @m78_lib.M78	16B6 16D7
NB_CFG<19>	NB_CFG<19> - @m78_lib.M78	7C3 16B6 16C7
NB_CFG<20>	NB_CFG<20> - @m78_lib.M78	16B6 16C7
NB_CLINK_VREF	NB_CLINK_VREF - @m78_lib.M78	16A4 104B3
NB_CLKREQ_L	NB_CLKREQ_L - @m78_lib.M78	16A3 29B3 30C2
NB_FSB_RCOMP	NB_FSB_RCOMP - @m78_lib.M78	14A5
NB_FSB_SCOMP	NB_FSB_SCOMP - @m78_lib.M78	14A5
NB_FSB_SCOMP_L	NB_FSB_SCOMP_L - @m78_lib.M78	14A5
NB_FSB_SWING	NB_FSB_SWING - @m78_lib.M78	14A5
NB_FSB_VREF	NB_FSB_VREF - @m78_lib.M78	14A5
NB_RESET_L	NB_RESET_L - @m78_lib.M78	7C7 16B6 28D1
NB_SB_SYNC_L	NB_SB_SYNC_L - @m78_lib.M78	16A3 25B5
NB_TEST1	NB_TEST1 - @m78_lib.M78	16A4
NB_TEST2	NB_TEST2 - @m78_lib.M78	16A4
NB_VCCSM_LF1	NB_VCCSM_LF1 - @m78_lib.M78	18A6
NB_VCCSM_LF2	NB_VCCSM_LF2 - @m78_lib.M78	18A6
NB_VCCSM_LF3	NB_VCCSM_LF3 - @m78_lib.M78	18A6
NB_VCCSM_LF4	NB_VCCSM_LF4 - @m78_lib.M78	18A6
NB_VCCSM_LF5	NB_VCCSM_LF5 - @m78_lib.M78	18A6
NB_VCCSM_LF6	NB_VCCSM_LF6 - @m78_lib.M78	18A6
NB_VCCSM_LF7	NB_VCCSM_LF7 - @m78_lib.M78	18A6
NB_VTTLF_CAP1	NB_VTTLF_CAP1 - @m78_lib.M78	19A4
NB_VTTLF_CAP2	NB_VTTLF_CAP2 - @m78_lib.M78	19A4
NB_VTTLF_CAP3	NB_VTTLF_CAP3 - @m78_lib.M78	19A4
NC_SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN - @m78_lib.M78	50D3
	SMC_BATT_CHG_EN - @m78_lib.M78	49C8 50D5
NC_SMC_BATT_ISET	NC_SMC_BATT_ISET - @m78_lib.M78	50D3
	SMC_BATT_ISET - @m78_lib.M78	49B5 50D5
NC_SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L - @m78_lib.M78	50D3
	SMC_BATT_TRICKLE_EN_L - @m78_lib.M78	49C8 50D5
NC_SMC_BATT_VSET	NC_SMC_BATT_VSET - @m78_lib.M78	50D3
	SMC_BATT_VSET - @m78_lib.M78	49B5 50D5
NC_SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE - @m78_lib.M78	50B3
	SMC_NB_1V8_ISENSE - @m78_lib.M78	49A8 50B5
NC_SMC_NB_CORE_ISENSE	NC_SMC_NB_CORE_ISENSE - @m78_lib.M78	50B3
	SMC_NB_CORE_ISENSE - @m78_lib.M78	49A8 50B5
NC_SMC_SYS_ISET	NC_SMC_SYS_ISET - @m78_lib.M78	50D3
	SMC_SYS_ISET - @m78_lib.M78	49B5 50D5

NC_SMC_SYS_VSET	NC_SMC_SYS_VSET - @m78_lib.M78	50D3
	SMC_SYS_VSET - @m78_lib.M78	49B5 50D5
ODD_PWR_EN_L	ODD_PWR_EN_L - @m78_lib.M78	24A4 24A6
ODD_RST_5VTOL_L	ODD_RST_5VTOL_L - @m78_lib.M78	24B6 44C6 103D3
ODD_THRMD_N	ODD_THRMD_N - @m78_lib.M78	55A5 55B6 108A3
ODD_THRMD_P	ODD_THRMD_P - @m78_lib.M78	55B5 55B6 108A3
P1V8S0_EN_L	P1V8S0_EN_L - @m78_lib.M78	78A7
P1V8S0_EN_L_RC	P1V8S0_EN_L_RC - @m78_lib.M78	78A6
P1V8S0_GDRV	P1V8S0_GDRV - @m78_lib.M78	78B7
P1V8S0_SS	P1V8S0_SS - @m78_lib.M78	78B6
P1V8S0_SS_RC	P1V8S0_SS_RC - @m78_lib.M78	78B7
P2V5S0_EN	P2V5S0_EN - @m78_lib.M78	77B5
P2V5S0_SW	P2V5S0_SW - @m78_lib.M78	77B4 108D1
P2V5S0_VFB	P2V5S0_VFB - @m78_lib.M78	77B4
P3V3S0_EN_L	P3V3S0_EN_L - @m78_lib.M78	78C5
P3V3S0_SS	P3V3S0_SS - @m78_lib.M78	78C4
P3V3S5_FB	P3V3S5_FB - @m78_lib.M78	77D5
P3V3S5_SW	P3V3S5_SW - @m78_lib.M78	77D5 108D1
P5VREG_FCB	P5VREG_FCB - @m78_lib.M78	76A3 76B5
P5VREG_FSEL	P5VREG_FSEL - @m78_lib.M78	76A2 76B4
P5VS0_EN_L	P5VS0_EN_L - @m78_lib.M78	78D5
P5VS0_SS	P5VS0_SS - @m78_lib.M78	78D4
P5VS3_EN_L	P5VS3_EN_L - @m78_lib.M78	78D8
P5VS3_SS	P5VS3_SS - @m78_lib.M78	78D7
P5VS5_EN	P5VS5_EN - @m78_lib.M78	77D6
P12V_S3_DRAIN	P12V_S3_DRAIN - @m78_lib.M78	78C1
P12V_S3_EN_L	P12V_S3_EN_L - @m78_lib.M78	78D3
PANEL_ID	PANEL_ID - @m78_lib.M78	28B2
	TP_SB_GPIO20 - @m78_lib.M78	25C5 28B1
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N - @m78_lib.M78	37C4 108C3
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P - @m78_lib.M78	37C4 108C3
PCIE_ENET_D2R_N	PCIE_ENET_D2R_N - @m78_lib.M78	7B8 24C5 37C8 104C3
PCIE_ENET_D2R_P	PCIE_ENET_D2R_P - @m78_lib.M78	7B8 24C5 37C8 104C3
PCIE_ENET_R2D_C_N	PCIE_ENET_R2D_C_N - @m78_lib.M78	24C5 37C8 104C3
PCIE_ENET_R2D_C_P	PCIE_ENET_R2D_C_P - @m78_lib.M78	24C5 37C8 104C3
PCIE_ENET_R2D_N	PCIE_ENET_R2D_N - @m78_lib.M78	7D6 37C4 108C3
PCIE_ENET_R2D_P	PCIE_ENET_R2D_P - @m78_lib.M78	7D6 37C4 108C3
PCIE_FW_D2R_C_N	PCIE_FW_D2R_C_N - @m78_lib.M78	40C3 108C3
PCIE_FW_D2R_C_P	PCIE_FW_D2R_C_P - @m78_lib.M78	40C3 108C3
PCIE_FW_D2R_N	PCIE_FW_D2R_N - @m78_lib.M78	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_N - @m78_lib.M78	24D5 42A1
PCIE_FW_D2R_P	PCIE_FW_D2R_P - @m78_lib.M78	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_P - @m78_lib.M78	24D5 42A1
PCIE_FW_R2D_C_N	PCIE_FW_R2D_C_N - @m78_lib.M78	40C1 42A1 104C3
	TP_PCIE_FW_R2D_C_N - @m78_lib.M78	24D5 42A3
PCIE_FW_R2D_C_P	PCIE_FW_R2D_C_P - @m78_lib.M78	40C1 42A1 104C3
	TP_PCIE_FW_R2D_C_P - @m78_lib.M78	24D5 42A3
PCIE_FW_R2D_N	PCIE_FW_R2D_N - @m78_lib.M78	7D6 40C3 108C3
PCIE_FW_R2D_P	PCIE_FW_R2D_P - @m78_lib.M78	7D6 40C3 108C3
PCIE_MINI_D2R_N	PCIE_MINI_D2R_N - @m78_lib.M78	7B8 24D5 34C8 104C3
PCIE_MINI_D2R_P	PCIE_MINI_D2R_P - @m78_lib.M78	7B8 24C5 34C8 104C3
PCIE_MINI_R2D_C_N	PCIE_MINI_R2D_C_N - @m78_lib.M78	24C5 34B8 104C3
PCIE_MINI_R2D_C_P	PCIE_MINI_R2D_C_P - @m78_lib.M78	24C5 34B8 104C3
PCIE_MINI_R2D_N	PCIE_MINI_R2D_N - @m78_lib.M78	34B6 108C3
PCIE_MINI_R2D_P	PCIE_MINI_R2D_P - @m78_lib.M78	34B6 108B3
PCIE_WAKE_L	PCIE_WAKE_L - @m78_lib.M78	25C8 34C6 37B8
PCI_AD<0>	PCI_AD<0> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_0 - @m78_lib.M78	28C4
PCI_AD<18..0>	PCI_AD<18..0> - @m78_lib.M78	104D3
	TP_PCI_AD_18 - @m78_lib.M78	28B4
PCI_AD<1>	PCI_AD<1> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_1 - @m78_lib.M78	28C4
PCI_AD<2>	PCI_AD<2> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_2 - @m78_lib.M78	28C4
PCI_AD<3>	PCI_AD<3> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_3 - @m78_lib.M78	28C4
PCI_AD<4>	PCI_AD<4> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_4 - @m78_lib.M78	28C4
PCI_AD<5>	PCI_AD<5> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_5 - @m78_lib.M78	28C4
PCI_AD<6>	PCI_AD<6> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_6 - @m78_lib.M78	28C4
PCI_AD<7>	PCI_AD<7> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_7 - @m78_lib.M78	28C4
PCI_AD<8>	PCI_AD<8> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_8 - @m78_lib.M78	28C4
PCI_AD<9>	PCI_AD<9> - @m78_lib.M78	24B8 28C5
	TP_PCI_AD_9 - @m78_lib.M78	28C4
PCI_AD<10>	PCI_AD<10> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_10 - @m78_lib.M78	28C4
PCI_AD<11>	PCI_AD<11> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_11 - @m78_lib.M78	28C4
PCI_AD<12>	PCI_AD<12> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_12 - @m78_lib.M78	28C4
PCI_AD<13>	PCI_AD<13> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_13 - @m78_lib.M78	28C4
PCI_AD<14>	PCI_AD<14> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_14 - @m78_lib.M78	28C4
PCI_AD<15>	PCI_AD<15> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_15 - @m78_lib.M78	28C4
PCI_AD<16>	PCI_AD<16> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_16 - @m78_lib.M78	28C4
PCI_AD<17>	PCI_AD<17> - @m78_lib.M78	24A8 28C5
	TP_PCI_AD_17 - @m78_lib.M78	28C4
PCI_AD<18>	PCI_AD<18> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_18 - @m78_lib.M78	28B4
PCI_AD<19>	PCI_AD<19> - @m78_lib.M78	24A8 28B5 104D3
	TP_PCI_AD_19 - @m78_lib.M78	28B4
PCI_AD<20>	PCI_AD<20> - @m78_lib.M78	24A8 28B5 104D3
	TP_PCI_AD_20 - @m78_lib.M78	28B4
PCI_AD<21>	PCI_AD<21> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_21 - @m78_lib.M78	28B4
PCI_AD<31..21>	PCI_AD<31..21> - @m78_lib.M78	104D3
	TP_PCI_AD_31 - @m78_lib.M78	28B4
PCI_AD<22>	PCI_AD<22> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_22 - @m78_lib.M78	28B4
PCI_AD<23>	PCI_AD<23> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_23 - @m78_lib.M78	28B4
PCI_AD<24>	PCI_AD<24> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_24 - @m78_lib.M78	28B4
PCI_AD<25>	PCI_AD<25> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_25 - @m78_lib.M78	28B4
PCI_AD<26>	PCI_AD<26> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_26 - @m78_lib.M78	28B4
PCI_AD<27>	PCI_AD<27> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_27 - @m78_lib.M78	28B4
PCI_AD<28>	PCI_AD<28> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_28 - @m78_lib.M78	28B4
PCI_AD<29>	PCI_AD<29> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_29 - @m78_lib.M78	28B4
PCI_AD<30>	PCI_AD<30> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_30 - @m78_lib.M78	28B4
PCI_AD<31>	PCI_AD<31> - @m78_lib.M78	24A8 28B5
	TP_PCI_AD_31 - @m78_lib.M78	28B4

PCI_CLK33M_LPCPLUS	PCI_CLK33M_LPCPLUS - @m78_lib.M78	7D4 30A3 51C4 105C3
PCI_CLK33M_SB	PCI_CLK33M_SB - @m78_lib.M78	7B8 24A6 30A3 105B3
PCI_CLK33M_SMC	PCI_CLK33M_SMC - @m78_lib.M78	7C6 30A3 49C8 105B3
PCI_CLK33M_TPM	PCI_CLK33M_TPM - @m78_lib.M78	105B3
PCI_C_BE_L<0>	PCI_C_BE_L<0> - @m78_lib.M78	24B6 28B5
	TP_PCI_C_BE_L_0 - @m78_lib.M78	28B4
PCI_C_BE_L<3..0>	PCI_C_BE_L<3..0> - @m78_lib.M78	104D3
	TP_PCI_C_BE_L_3 - @m78_lib.M78	28B4
PCI_C_BE_L<1>	PCI_C_BE_L<1> - @m78_lib.M78	24A6 28B5
	TP_PCI_C_BE_L_1 - @m78_lib.M78	28B4
PCI_C_BE_L<2>	PCI_C_BE_L<2> - @m78_lib.M78	24A6 28B5
	TP_PCI_C_BE_L_2 - @m78_lib.M78	28B4
PCI_C_BE_L<3>	PCI_C_BE_L<3> - @m78_lib.M78	24A6 28B5
	TP_PCI_C_BE_L_3 - @m78_lib.M78	28B4
PCI_DEVSEL_L	PCI_DEVSEL_L - @m78_lib.M78	24A4 24A6 104D3
PCI_FRAME_L	PCI_FRAME_L - @m78_lib.M78	24A4 24A6 104D3
PCI_FW_GNT_L	PCI_FW_GNT_L - @m78_lib.M78	24B5 104D3
	BOOT_LPC_SPI_L - @m78_lib.M78	7D4 24B5 51B6
PCI_FW_REQ_L	PCI_FW_REQ_L - @m78_lib.M78	24A4 24B6 104D3
PCI_GNT1_L	PCI_GNT1_L - @m78_lib.M78	104D3
PCI_GNT2_L	PCI_GNT2_L - @m78_lib.M78	104C3
PCI_IRDY_L	PCI_IRDY_L - @m78_lib.M78	24A4 24A6 104D3
PCI_LOCK_L	PCI_LOCK_L - @m78_lib.M78	24A4 24A6 104D3
PCI_PAR	PCI_PAR - @m78_lib.M78	24A6 28B5 104D3
	TP_PCI_PAR - @m78_lib.M78	28B4
PCI_PERR_L	PCI_PERR_L - @m78_lib.M78	24A4 24A6 104D3
PCI_PME_FW_L	PCI_PME_FW_L - @m78_lib.M78	25B5 25C5 40C3
PCI_REQ1_L	PCI_REQ1_L - @m78_lib.M78	7C3 24A4 24B6 104D3
PCI_REQ2_L	PCI_REQ2_L - @m78_lib.M78	7C3 24A4 24B6 104D3
PCI_RST_L	PCI_RST_L - @m78_lib.M78	24A6 28B5
	TP_PCI_RST_L - @m78_lib.M78	28B4
PCI_SERR_L	PCI_SERR_L - @m78_lib.M78	24A4 24A6 28C4 104D3
PCI_STOP_L	PCI_STOP_L - @m78_lib.M78	24A4 24A6 104D3
PCI_TRDY_L	PCI_TRDY_L - @m78_lib.M78	24A4 24A6 104D3
PEG_COMP	PEG_COMP - @m78_lib.M78	15D3
PEG_D2R_N<0>	PEG_D2R_N<0> - @m78_lib.M78	15D3 84C4
PEG_D2R_N<6..0>	PEG_D2R_N<6..0> - @m78_lib.M78	101D3
PEG_D2R_N<1>	PEG_D2R_N<1> - @m78_lib.M78	15D3 84C4
PEG_D2R_N<2>	PEG_D2R_N<2> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<3>	PEG_D2R_N<3> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<4>	PEG_D2R_N<4> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<5>	PEG_D2R_N<5> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<6>	PEG_D2R_N<6> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<7>	PEG_D2R_N<7> - @m78_lib.M78	7A7 15D3 84B4 101D3
PEG_D2R_N<8>	PEG_D2R_N<8> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<15..8>	PEG_D2R_N<15..8> - @m78_lib.M78	101D3
PEG_D2R_N<9>	PEG_D2R_N<9> - @m78_lib.M78	15D3 84B4
PEG_D2R_N<10>	PEG_D2R_N<10> - @m78_lib.M78	15C3 84B4
PEG_D2R_N<11>	PEG_D2R_N<11> - @m78_lib.M78	15C3 84A4
PEG_D2R_N<12>	PEG_D2R_N<12> - @m78_lib.M78	15C3 84A4
PEG_D2R_N<13>	PEG_D2R_N<13> - @m78_lib.M78	15C3 84A4
PEG_D2R_N<14>	PEG_D2R_N<14> - @m78_lib.M78	15C3 84A4
PEG_D2R_N<15>	PEG_D2R_N<15> - @m78_lib.M78	15C3 84A4
PEG_D2R_P<0>	PEG_D2R_P<0> - @m78_lib.M78	15C3 84C4
PEG_D2R_P<6..0>	PEG_D2R_P<6..0> - @m78_lib.M78	101D3
PEG_D2R_P<1>	PEG_D2R_P<1> - @m78_lib.M78	15C3 84C4
PEG_D2R_P<2>	PEG_D2R_P<2> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<3>	PEG_D2R_P<3> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<4>	PEG_D2R_P<4> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<5>	PEG_D2R_P<5> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<6>	PEG_D2R_P<6> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<7>	PEG_D2R_P<7> - @m78_lib.M78	7A7 15C3 84B4 101D3
PEG_D2R_P<8>	PEG_D2R_P<8> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<15..8>	PEG_D2R_P<15..8> - @m78_lib.M78	101D3
PEG_D2R_P<9>	PEG_D2R_P<9> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<10>	PEG_D2R_P<10> - @m78_lib.M78	15C3 84B4
PEG_D2R_P<11>	PEG_D2R_P<11> - @m78_lib.M78	15C3 84A4
PEG_D2R_P<12>	PEG_D2R_P<12> - @m78_lib.M78	15C3 84A4
PEG_D2R_P<13>	PEG_D2R_P<13> - @m78_lib.M78	15C3 84A4
PEG_D2R_P<14>	PEG_D2R_P<14> - @m78_lib.M78	15C3 84A4
PEG_D2R_P<15>	PEG_D2R_P<15> - @m78_lib.M78	15C3 84A4
PEG_R2D_C_N<0>	PEG_R2D_C_N<0> - @m78_lib.M78	15C3 84C8
PEG_R2D_C_N<15..0>	PEG_R2D_C_N<15..0> - @m78_lib.M78	101D3
PEG_R2D_C_N<1>	PEG_R2D_C_N<1> - @m78_lib.M78	15C3 84C8
PEG_R2D_C_N<2>	PEG_R2D_C_N<2> - @m78_lib.M78	15C3 84B8
PEG_R2D_C_N<3>	PEG_R2D_C_N<3> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<4>	PEG_R2D_C_N<4> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<5>	PEG_R2D_C_N<5> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<6>	PEG_R2D_C_N<6> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<7>	PEG_R2D_C_N<7> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<8>	PEG_R2D_C_N<8> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<9>	PEG_R2D_C_N<9> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_N<10>	PEG_R2D_C_N<10> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_N<11>	PEG_R2D_C_N<11> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_N<12>	PEG_R2D_C_N<12> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_N<13>	PEG_R2D_C_N<13> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_N<14>	PEG_R2D_C_N<14> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_N<15>	PEG_R2D_C_N<15> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_P<0>	PEG_R2D_C_P<0> - @m78_lib.M78	15B3 84C8
PEG_R2D_C_P<15..0>	PEG_R2D_C_P<15..0> - @m78_lib.M78	101D3
PEG_R2D_C_P<1>	PEG_R2D_C_P<1> - @m78_lib.M78	15B3 84C8
PEG_R2D_C_P<2>	PEG_R2D_C_P<2> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<3>	PEG_R2D_C_P<3> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<4>	PEG_R2D_C_P<4> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<5>	PEG_R2D_C_P<5> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<6>	PEG_R2D_C_P<6> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<7>	PEG_R2D_C_P<7> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<8>	PEG_R2D_C_P<8> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<9>	PEG_R2D_C_P<9> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<10>	PEG_R2D_C_P<10> - @m78_lib.M78	15B3 84B8
PEG_R2D_C_P<11>	PEG_R2D_C_P<11> - @m78_lib.M78	15B3 84A8
PEG_R2D_C_P<12>	PEG_R2D_C_P<12> - @m78_lib.M78	15A3 84A8
PEG_R2D_C_P<13>	PEG_R2D_C_P<13> - @m78_lib.M78	15A3 84A8
PEG_R2D_C_P<14>	PEG_R2D_C_P<14> - @m78_lib.M78	15A3 84A8
PEG_R2D_C_P<15>	PEG_R2D_C_P<15> - @m78_lib.M78	15A3 84A8
PEG_R2D_N<0>	PEG_R2D_N<0> - @m78_lib.M78	84A7
PEG_R2D_N<15..0>	PEG_R2D_N<15..0> - @m78_lib.M78	101D3
PEG_R2D_N<1>	PEG_R2D_N<1> - @m78_lib.M78	84A7
PEG_R2D_N<2>	PEG_R2D_N<2> - @m78_lib.M78	84A7
PEG_R2D_N<3>	PEG_R2D_N<3> - @m78_lib.M78	84A7
PEG_R2D_N<4>	PEG_R2D_N<4> - @m78_lib.M78	84A7
PEG_R2D_N<5>	PEG_R2D_N<5> - @m78_lib.M78	84A7
PEG_R2D_N<6>	PEG_R2D_N<6> - @m78_lib.M78	84B7
PEG_R2D_N<7>	PEG_R2D_N<7> - @m78_lib.M78	84B7
PEG_R2D_N<8>	PEG_R2D_N<8> - @m78_lib.M78	84B7
PEG_R2D_N<9>	PEG_R2D_N<9> - @m78_lib.M78	84B7
PEG_R2D_N<10>	PEG_R2D_N<10> - @m78_lib.M78	84B7
PEG_R2D_N<11>	PEG_R2D_N<11> - @m78_lib.M78	84B7
PEG_R2D_N<12>	PEG_R2D_N<12> - @m78_lib.M78	84B7
PEG_R2D_N<13>	PEG_R2D_N<13> - @m78_lib.M78	84B7
PEG_R2D_N<14>	PEG_R2D_N<14> - @m78_lib.M78	84C7
PEG_R2D_N<15>	PEG_R2D_N<15> - @m78_lib.M78	84C7
PEG_R2D_P<0>	PEG_R2D_P<0> - @m78_lib.M78	84A7
PEG_R2D_P<15..0>	PEG_R2D_P<15..0> - @m78_lib.M78	101D3

PEG_R2D_P<1>	PEG_R2D_P<1> - @m78_lib.M78	84A7
PEG_R2D_P<2>	PEG_R2D_P<2> - @m78_lib.M78	84A7
PEG_R2D_P<3>	PEG_R2D_P<3> - @m78_lib.M78	84A7
PEG_R2D_P<4>	PEG_R2D_P<4> - @m78_lib.M78	84A7
PEG_R2D_P<5>	PEG_R2D_P<5> - @m78_lib.M78	84B7
PEG_R2D_P<6>	PEG_R2D_P<6> - @m78_lib.M78	84B7
PEG_R2D_P<7>	PEG_R2D_P<7> - @m78_lib.M78	84B7
PEG_R2D_P<8>	PEG_R2D_P<8> - @m78_lib.M78	84B7
PEG_R2D_P<9>	PEG_R2D_P<9> - @m78_lib.M78	84B7
PEG_R2D_P<10>	PEG_R2D_P<10> - @m78_lib.M78	84B7
PEG_R2D_P<11>	PEG_R2D_P<11> - @m78_lib.M78	84B7
PEG_R2D_P<12>	PEG_R2D_P<12> - @m78_lib.M78	84B7
PEG_R2D_P<13>	PEG_R2D_P<13> - @m78_lib.M78	84B7
PEG_R2D_P<14>	PEG_R2D_P<14> - @m78_lib.M78	84C7
PEG_R2D_P<15>	PEG_R2D_P<15> - @m78_lib.M78	84C7
PEG_RESET_L	PEG_RESET_L - @m78_lib.M78	28C1 85C7
PGOOD_0V9_S0	PGOOD_0V9_S0 - @m78_lib.M78	70C4 70C4
PGOOD_1V05_S0	PGOOD_1V05_S0 - @m78_lib.M78	70B4 73B3
PGOOD_1V5_S0	PGOOD_1V5_S0 - @m78_lib.M78	70B4 73B5
PGOOD_1V8_S0	PGOOD_1V8_S0 - @m78_lib.M78	70C4 70D4
PGOOD_1V8_S3	PGOOD_1V8_S3 - @m78_lib.M78	70D4 75C8
PGOOD_1V25_S0	PGOOD_1V25_S0 - @m78_lib.M78	70B4 74B5
PGOOD_2V5_S0	PGOOD_2V5_S0 - @m78_lib.M78	70C4 77B7
PGOOD_3V3_S0	PGOOD_3V3_S0 - @m78_lib.M78	70C8 70D4 77B7
PGOOD_3V3_S3	PGOOD_3V3_S3 - @m78_lib.M78	70D4 76B4
PGOOD_3V3_S5	PGOOD_3V3_S5 - @m78_lib.M78	70B4 77D4
	RSMRST_PWRGD - @m78_lib.M78	49D8 70B2
PGOOD_5V_S0	PGOOD_5V_S0 - @m78_lib.M78	70C4 70C4
PGOOD_5V_S3_L	PGOOD_5V_S3_L - @m78_lib.M78	76A6
PGOOD_12V_S0	PGOOD_12V_S0 - @m78_lib.M78	70B8 76D5
PGOOD_CR_S0	PGOOD_CR_S0 - @m78_lib.M78	70C7
PGOOD_MCH_CORE_S0	PGOOD_MCH_CORE_S0 - @m78_lib.M78	70B4 74B3
PGOOD_S0_OUT1	PGOOD_S0_OUT1 - @m78_lib.M78	70C3
PLT_RST_L	PLT_RST_L - @m78_lib.M78	24A6 28D4
PM_BATLOW_L	PM_BATLOW_L - @m78_lib.M78	25A5 25C3 49B8
PM_BMBUSY_L	PM_BMBUSY_L - @m78_lib.M78	16B6 25D5
PM_CLKRUN_L	PM_CLKRUN_L - @m78_lib.M78	7B8 7D4 25C8 49C5 51B6
PM_DPRSLPVR	PM_DPRSLPVR - @m78_lib.M78	16A6 25C3 71C8 100B3
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @m78_lib.M78	16B7 31C3 49B8
PM_EXTTS_L<1>	PM_EXTTS_L<1> - @m78_lib.M78	16B7 32C3 49B8
PM_LAN_ENABLE	PM_LAN_ENABLE - @m78_lib.M78	25C2 49D8
PM_LATRIGGER_L	PM_LATRIGGER_L - @m78_lib.M78	13C3 24C8
PM_PWRBTN_L	PM_PWRBTN_L - @m78_lib.M78	25C3 49C8
PM_RI_L	PM_RI_L - @m78_lib.M78	25A5 25D5
PM_RSMRST_L	PM_RSMRST_L - @m78_lib.M78	25C2 49C8
PM_S4_STATE_INV	PM_S4_STATE_INV - @m78_lib.M78	78C2
PM_S4_STATE_L	PM_S4_STATE_L - @m78_lib.M78	7C4 7D3 25D3 46C8 49C4 75D8 78C3 78D8
PM_S4_STATE_L_SMC	PM_S4_STATE_L_SMC - @m78_lib.M78	49C6
PM_SLP_S3_L	PM_SLP_S3_L - @m78_lib.M78	6D8 7C4 25D3 49C4 70A8 75A5 78A8 78C6 78D6
PM_SLP_S3_L_SMC	PM_SLP_S3_L_SMC - @m78_lib.M78	49C6
PM_SLP_S3_OD	PM_SLP_S3_OD - @m78_lib.M78	6D7
PM_SLP_S5_L	PM_SLP_S5_L - @m78_lib.M78	25D3 49C5 50A2
PM_STPCPU_L	PM_STPCPU_L - @m78_lib.M78	25C8 29C3 30C2
PM_STPPCI_L	PM_STPPCI_L - @m78_lib.M78	25C8 29C3 30C2
PM_SUS_STAT_L	PM_SUS_STAT_L - @m78_lib.M78	7C4 7D4 25D5 49C5 50A2 51B4
PM_SYSRST_L	PM_SYSRST_L - @m78_lib.M78	7B8 25D5 28A3 49B8
PM_THRMTRIP_L	PM_THRMTRIP_L - @m78_lib.M78	10C6 16A6 23C2 50C3 100B3
PM_THRM_L	PM_THRM_L - @m78_lib.M78	25C5
POWER_BUTTON_L	POWER_BUTTON_L - @m78_lib.M78	50C7
PP1V0_S5_FW_AVDD	PP1V0_S5_FW_AVDD - @m78_lib.M78	40D3 42A6 42D4
PP1V0_S5_FW_DVDD	PP1V0_S5_FW_DVDD - @m78_lib.M78	40D6 42B8 42C4
PP1V05_S0_NB_VCCPEG	PP1V05_S0_NB_VCCPEG - @m78_lib.M78	15D2 19B3 21D3
	PP1V05_S0_NB_VCCRXRDMI - @m78_lib.M78	19B3 21C3
PP1V5_S0_NB_VCCD_TVDAC	PP1V5_S0_NB_VCCD_TVDAC - @m78_lib.M78	19B6 22B1
PP1V5_S0_SB_VCCDMIPLL	PP1V5_S0_SB_VCCDMIPLL - @m78_lib.M78	26C3 27A6
PP1V5_S0_SB_VCCDMIPLL_F	PP1V5_S0_SB_VCCDMIPLL_F - @m78_lib.M78	27A8
PP1V5_S0_SB_VCCSATAPLL	PP1V5_S0_SB_VCCSATAPLL - @m78_lib.M78	26B6 27A6
PP1V5_S0_SB_VCCSATAPLL_F	PP1V5_S0_SB_VCCSATAPLL_F - @m78_lib.M78	27A8
PP1V8_S3M_NB_VCCSMCK	PP1V8_S3M_NB_VCCSMCK - @m78_lib.M78	19B3 21A2
PP1V8_S3M_NB_VCCSMCK_RC	PP1V8_S3M_NB_VCCSMCK_RC - @m78_lib.M78	21A4
PP1V8_S3_R	PP1V8_S3_R - @m78_lib.M78	75C1
PP1V9R2V5_ENET_PHY_AVDD	PP1V9R2V5_ENET_PHY_AVDD - @m78_lib.M78	37C6 39D8 104B3
PP1V9R2V5_S3_ENET_R	PP1V9R2V5_S3_ENET_R - @m78_lib.M78	38C3 104B2
	=YUKON_EC_PP2V5_ENET - @m78_lib.M78	37C7 38C1
PP1V25_S0M_NB_MPLL_RC	PP1V25_S0M_NB_MPLL_RC - @m78_lib.M78	21C3
PP1V25_S0M_NB_VCCAXD	PP1V25_S0M_NB_VCCAXD - @m78_lib.M78	16A2 19C3 21A6
PP1V25_S0M_NB_VCCA_HPLL	PP1V25_S0M_NB_VCCA_HPLL - @m78_lib.M78	19D6 21D1
PP1V25_S0M_NB_VCCA_MPLL	PP1V25_S0M_NB_VCCA_MPLL - @m78_lib.M78	19D6 21C1
PP1V25_S0M_NB_VCCA_SM	PP1V25_S0M_NB_VCCA_SM - @m78_lib.M78	19C6 21B5
PP1V25_S0M_NB_VCCA_SM_CK	PP1V25_S0M_NB_VCCA_SM_CK - @m78_lib.M78	19B6 21B5
PP1V25_S0_NB_PEGPLL	PP1V25_S0_NB_PEGPLL - @m78_lib.M78	19C6 21B2
PP1V25_S0_NB_PEGPLL_RC	PP1V25_S0_NB_PEGPLL_RC - @m78_lib.M78	21B4
PP1V25_S0_NB_VCCAXF	PP1V25_S0_NB_VCCAXF - @m78_lib.M78	19C3 21D3
PP2V5_ENET_CTAP	PP2V5_ENET_CTAP - @m78_lib.M78	39D7
PP3V3_FW_ESD	PP3V3_FW_ESD - @m78_lib.M78	43A6 43A6 43B6 43C5 43D5
PP3V3_G3_SB_RTC	PP3V3_G3_SB_RTC - @m78_lib.M78	23D7 26D6 27D5 28D5
PP3V3_S0M_CK505_VDD48	PP3V3_S0M_CK505_VDD48 - @m78_lib.M78	29D4
PP3V3_S0M_CK505_VDDA	PP3V3_S0M_CK505_VDDA - @m78_lib.M78	29C6
PP3V3_S0M_CK505_VDDA_R	PP3V3_S0M_CK505_VDDA_R - @m78_lib.M78	29C7
PP3V3_S0M_CK505_VDD_CPU_SRC	PP3V3_S0M_CK505_VDD_CPU_SRC - @m78_lib.M78	29D7
PP3V3_S0M_CK505_VDD_PCI	PP3V3_S0M_CK505_VDD_PCI - @m78_lib.M78	29D4
PP3V3_S0M_CK505_VDD_REF	PP3V3_S0M_CK505_VDD_REF - @m78_lib.M78	29C4
PP3V3_S0_CPUTHMSNS_R	PP3V3_S0_CPUTHMSNS_R - @m78_lib.M78	55D4
PP3V3_S0_IMVP6_3V3	PP3V3_S0_IMVP6_3V3 - @m78_lib.M78	71D7
PP3V3_S0_NB1V05_FOLLOW_R	PP3V3_S0_NB1V05_FOLLOW_R - @m78_lib.M78	21C4
PP3V3_S0_NBCORE_FOLLOW_R	PP3V3_S0_NBCORE_FOLLOW_R - @m78_lib.M78	21B4
PP3V3_S3_ENET_O	PP3V3_S3_ENET_O - @m78_lib.M78	38D6
PP3V3_S5_AVREF_SMC	PP3V3_S5_AVREF_SMC - @m78_lib.M78	49D4 50B7
PP3V3_S5_FW_AVDD1	PP3V3_S5_FW_AVDD1 - @m78_lib.M78	40D4 42A8 42B1
PP3V3_S5_FW_AVDD2	PP3V3_S5_FW_AVDD2 - @m78_lib.M78	40D3 42A7 42B1

PP3V3_S5_SMC_AVCC	PP3V3_S5_SMC_AVCC - @m78_lib.M78	49D3
PP5VREG_INTVCC	PP5VREG_INTVCC - @m78_lib.M78	76A2 76A6 76C3 76C6
PP5V_S0_DDC	PP5V_S0_DDC - @m78_lib.M78	94D3 94D4
PP5V_S0_DDC_DIODE	PP5V_S0_DDC_DIODE - @m78_lib.M78	94D6
PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @m78_lib.M78	94D5
PP5V_S0_IMVP6_VDD	PP5V_S0_IMVP6_VDD - @m78_lib.M78	71D7
PP5V_S0_SB_V5REF	PP5V_S0_SB_V5REF - @m78_lib.M78	26D6 27C7
PP5V_S3_BNDI	PP5V_S3_BNDI - @m78_lib.M78	47B5 47D5
PP5V_S5_SB_V5REF_SUS	PP5V_S5_SB_V5REF_SUS - @m78_lib.M78	26D6 27D7
PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @m78_lib.M78	46B7
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @m78_lib.M78	46B5
PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @m78_lib.M78	46C6
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @m78_lib.M78	46C5
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @m78_lib.M78	46D6
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @m78_lib.M78	46D2
PP12V_S3	PP12V_S3 - @m78_lib.M78	7C5 7D3 50B7 75D8 76D8 78D1
PPVBATT_G3_RTC	PPVBATT_G3_RTC - @m78_lib.M78	28D8
PPVBATT_G3_RTC_R	PPVBATT_G3_RTC_R - @m78_lib.M78	28D7
PPVIN_S0_P2V5S0_SVIN	PPVIN_S0_P2V5S0_SVIN - @m78_lib.M78	77C5
PPVIN_S5_5VS5_R	PPVIN_S5_5VS5_R - @m78_lib.M78	76C5
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @m78_lib.M78	71D7
PPV_LCD_CONN	PPV_LCD_CONN - @m78_lib.M78	6A7 90A6 90A8 90C5
PPV_LCD_SW	PPV_LCD_SW - @m78_lib.M78	90C6
PPV_S0_LCD	PPV_S0_LCD - @m78_lib.M78	90C8
PPV_S0_MXM_PWRSRC	PPV_S0_MXM_PWRSRC - @m78_lib.M78	53C2 53D4 84C4
PPV_S3_ENET_O	PPV_S3_ENET_O - @m78_lib.M78	38B5
PPV_S3_ENET_R	PPV_S3_ENET_R - @m78_lib.M78	38B7
REMOTE_TEMP_ADDR	REMOTE_TEMP_ADDR - @m78_lib.M78	55A3
REMOTE_THRMD_M	REMOTE_THRMD_M - @m78_lib.M78	55A4
RSVD_EXTGPU_LVDS_EN	RSVD_EXTGPU_LVDS_EN - @m78_lib.M78	25D2
RSVD_MINI_BT_ACTIVE	RSVD_MINI_BT_ACTIVE - @m78_lib.M78	34C6
RSVD_MINI_WLAN_ACTIVE	RSVD_MINI_WLAN_ACTIVE - @m78_lib.M78	34C6
RUNSS_GATE_D_L	RUNSS_GATE_D_L - @m78_lib.M78	70A7 70B7 70B7
SATA_A_D2R_C_N	SATA_A_D2R_C_N - @m78_lib.M78	45D7 103C3
SATA_A_D2R_C_P	SATA_A_D2R_C_P - @m78_lib.M78	45C7 103C3
SATA_A_D2R_N	SATA_A_D2R_N - @m78_lib.M78	7B8 23B6 45C5 103C3
SATA_A_D2R_P	SATA_A_D2R_P - @m78_lib.M78	7B8 23B6 45C5 103D3
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @m78_lib.M78	23B6 45D5 103D3
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @m78_lib.M78	23B6 45D5 103D3
SATA_A_R2D_N	SATA_A_R2D_N - @m78_lib.M78	45D7 103D3
SATA_A_R2D_P	SATA_A_R2D_P - @m78_lib.M78	45D7 103D3
SATA_B_D2R_N	SATA_B_D2R_N - @m78_lib.M78	23B6 45B7 103C3
	TP_SATA_B_D2R_N - @m78_lib.M78	45B5
SATA_B_D2R_P	SATA_B_D2R_P - @m78_lib.M78	23B6 45B7 103C3
	TP_SATA_B_D2R_P - @m78_lib.M78	45B5
SATA_B_DET_L	SATA_B_DET_L - @m78_lib.M78	25D3
SATA_B_PWR_EN_L	SATA_B_PWR_EN_L - @m78_lib.M78	25B5 25C5
SATA_B_R2D_C_N	SATA_B_R2D_C_N - @m78_lib.M78	23B6 45B5 103C3
	TP_SATA_B_R2D_N - @m78_lib.M78	45B7
SATA_B_R2D_C_P	SATA_B_R2D_C_P - @m78_lib.M78	23B6 45B5 103C3
	TP_SATA_B_R2D_P - @m78_lib.M78	45B7
SATA_C_D2R_N	SATA_C_D2R_N - @m78_lib.M78	23B6 45B7
	TP_SATA_C_D2R_N - @m78_lib.M78	45B5
SATA_C_D2R_P	SATA_C_D2R_P - @m78_lib.M78	23B6 45B7
	TP_SATA_C_D2R_P - @m78_lib.M78	45B5
SATA_C_R2D_C_N	SATA_C_R2D_C_N - @m78_lib.M78	23B6 45B5
	TP_SATA_C_R2D_N - @m78_lib.M78	45B7
SATA_C_R2D_C_P	SATA_C_R2D_C_P - @m78_lib.M78	23B6 45B5
	TP_SATA_C_R2D_P - @m78_lib.M78	45B7
SATA_RBIAS	SATA_RBIAS - @m78_lib.M78	45B2 103C3
	SATA_RBIAS_N - @m78_lib.M78	23B6 45B2
	SATA_RBIAS_P - @m78_lib.M78	23A6 45B2
	SATA_RBIAS_N - @m78_lib.M78	23B6 45B2
SB_A20GATE	SB_A20GATE - @m78_lib.M78	23C4
SB_CLINK_VREF0	SB_CLINK_VREF0 - @m78_lib.M78	25C3 104B3
SB_CLINK_VREF1	SB_CLINK_VREF1 - @m78_lib.M78	25C3 104B3
SB_CLK14P3M_TIMER	SB_CLK14P3M_TIMER - @m78_lib.M78	7B8 25D3 30A6 105B3
SB_CLK48M_USBCTLR	SB_CLK48M_USBCTLR - @m78_lib.M78	7B8 25D3 30C6 105B3
SB_CRT_TVOUT_MUX_L	SB_CRT_TVOUT_MUX_L - @m78_lib.M78	25D2 91A7
SB_GPIO10_CL1	SB_GPIO10_CL1 - @m78_lib.M78	25A5 25B3
SB_GPIO14_CL2	SB_GPIO14_CL2 - @m78_lib.M78	25A5 25B3
SB_GPIO18	SB_GPIO18 - @m78_lib.M78	25C5
SB_GPIO30	SB_GPIO30 - @m78_lib.M78	13C3 24C8
SB_GPIO36	SB_GPIO36 - @m78_lib.M78	25D3
SB_GPIO40	SB_GPIO40 - @m78_lib.M78	13C3 24C8
SB_INTVRMEN	SB_INTVRMEN - @m78_lib.M78	23D6
SB_LAN100_SLP	SB_LAN100_SLP - @m78_lib.M78	23C6
SB_RCIN_L	SB_RCIN_L - @m78_lib.M78	23C4
SB_RTC_RST_L	SB_RTC_RST_L - @m78_lib.M78	7B8 23D8 28D5
SB_RTC_X1	SB_RTC_X1 - @m78_lib.M78	23D8 28C8
SB_RTC_X1_R	SB_RTC_X1_R - @m78_lib.M78	28C7
SB_RTC_X2	SB_RTC_X2 - @m78_lib.M78	23D8 28C8
SB_SATALED_L	SB_SATALED_L - @m78_lib.M78	45C2
	TP_SB_SATALED_L - @m78_lib.M78	23B6 45C1
SB_SATALED_R_L	SB_SATALED_R_L - @m78_lib.M78	45C2
SB_SATA_CLKREQ_L	SB_SATA_CLKREQ_L - @m78_lib.M78	25C5 29B3 30D2
SB_SCLOCK	SB_SCLOCK - @m78_lib.M78	25C5
SB_SDATAOUT<0>	SB_SDATAOUT<0> - @m78_lib.M78	25C5
SB_SDATAOUT<1>	SB_SDATAOUT<1> - @m78_lib.M78	25C5
SB_SLOAD	SB_SLOAD - @m78_lib.M78	25C5
SB_SM_INTRUDER_L	SB_SM_INTRUDER_L - @m78_lib.M78	23D8 28D5
SB_SPKR	SB_SPKR - @m78_lib.M78	25B5
SDF3400_1	SDF3400_1 - @m78_lib.M78	34A5
SDF4720_1	SDF4720_1 - @m78_lib.M78	47C3
SDF4721_1	SDF4721_1 - @m78_lib.M78	47C2
SMBUS_SMC_0_S0_SCL	SMBUS_SMC_0_S0_SCL - @m78_lib.M78	52D5 106B3
	=SMB_LCD_TEMP_SCL - @m78_lib.M78	52C3 55C6
	=SMB_AMB_TEMP_SCL - @m78_lib.M78	52D3 55C8
	=SMB_GPU_THRM_SCL - @m78_lib.M78	52D3 85C7
	SMB_0_S0_CLK - @m78_lib.M78	49B8 52D6
	=SMB_LCD_TEMP_SCL - @m78_lib.M78	52C3 55C6
	=SMB_GPU_THRM_SCL - @m78_lib.M78	52D3 85C7
	=SMB_AMB_TEMP_SCL - @m78_lib.M78	52D3 55C8
SMBUS_SMC_0_S0_SDA	SMBUS_SMC_0_S0_SDA - @m78_lib.M78	52D5 106B3
	=SMB_LCD_TEMP_SDA - @m78_lib.M78	52C3 55C6
	=SMB_AMB_TEMP_SDA - @m78_lib.M78	52C3 55C8
	=SMB_GPU_THRM_SDA - @m78_lib.M78	52D3 85C7
	SMB_0_S0_DATA - @m78_lib.M78	49B5 52D6
	=SMB_LCD_TEMP_SDA - @m78_lib.M78	52C3 55C6
	=SMB_GPU_THRM_SDA - @m78_lib.M78	52D3 85C7
	=SMB_AMB_TEMP_SDA - @m78_lib.M78	52C3 55C8
SMBUS_SMC_A_S3_SCL	SMBUS_SMC_A_S3_SCL - @m78_lib.M78	106B3
SMBUS_SMC_A_S3_SDA	SMBUS_SMC_A_S3_SDA - @m78_lib.M78	106B3
SMBUS_SMC_A_S5_SCL	SMBUS_SMC_A_S5_SCL - @m78_lib.M78	52D2
	SMB_A_S3_CLK - @m78_lib.M78	49A5 52D3
SMBUS_SMC_A_S5_SDA	SMBUS_SMC_A_S5_SDA - @m78_lib.M78	52D2
	SMB_A_S3_DATA - @m78_lib.M78	49A5 52D3
SMBUS_SMC_BSA_SCL	SMBUS_SMC_BSA_SCL - @m78_lib.M78	52C2 106B3
	SMB_BSA_CLK - @m78_lib.M78	49A5 52C3
SMBUS_SMC_BSA_SDA	SMBUS_SMC_BSA_SDA - @m78_lib.M78	52C2 106B3
	SMB_BSA_DATA - @m78_lib.M78	49A5 52C3
SMBUS_SMC_B_S0_SCL	SMBUS_SMC_B_S0_SCL - @m78_lib.M78	52C5 106B3

	=SMBUS_MINI_SCL - @m78_lib.M78	34B3 52B3
	=SMB_REMOTE_TEMP_SCL - @m78_lib.M78	52B3 55B2
	=SMB_CPU_THRM_SCL - @m78_lib.M78	52C3 55C2
	SMB_B_S0_CLK - @m78_lib.M78	49A5 52C5
	=SMB_REMOTE_TEMP_SCL - @m78_lib.M78	52B3 55B2
	=SMB_CPU_THRM_SCL - @m78_lib.M78	52C3 55C2
	=SMBUS_MINI_SCL - @m78_lib.M78	34B3 52B3
SMBUS_SMC_B_S0_SDA	SMBUS_SMC_B_S0_SDA - @m78_lib.M78	52B5 106B3
	=SMBUS_MINI_SDA - @m78_lib.M78	34B3 52B3
	=SMB_REMOTE_TEMP_SDA - @m78_lib.M78	52B3 55B2
	=SMB_CPU_THRM_SDA - @m78_lib.M78	52B3 55C2
	SMB_B_S0_DATA - @m78_lib.M78	49A5 52B5
	=SMB_REMOTE_TEMP_SDA - @m78_lib.M78	52B3 55B2
	=SMB_CPU_THRM_SDA - @m78_lib.M78	52B3 55C2
	=SMBUS_MINI_SDA - @m78_lib.M78	34B3 52B3
SMBUS_SMC_MGMT_SCL	SMBUS_SMC_MGMT_SCL - @m78_lib.M78	52B2 106B3
	SMB_MGMT_CLK - @m78_lib.M78	49C5 52B3
SMBUS_SMC_MGMT_SDA	SMBUS_SMC_MGMT_SDA - @m78_lib.M78	52B2 106B3
	SMB_MGMT_DATA - @m78_lib.M78	49C8 52B3
SMB_CLK	SMB_CLK - @m78_lib.M78	25D5 52D8 103A3
	=SMBUS_CK505_SCL - @m78_lib.M78	29B5 52D6
	SMBUS_SB_SCL - @m78_lib.M78	52D7
	=I2C_DIMMA_SCL - @m78_lib.M78	31A6 52D6
	=I2C_DIMMB_SCL - @m78_lib.M78	32A6 52C6
	SMBUS_SB_SCL - @m78_lib.M78	52D7
	=SMBUS_CK505_SCL - @m78_lib.M78	29B5 52D6
	=I2C_DIMMB_SCL - @m78_lib.M78	32A6 52C6
	=I2C_DIMMA_SCL - @m78_lib.M78	31A6 52D6
SMB_DATA	SMB_DATA - @m78_lib.M78	25D5 52D8 103A3
	=SMBUS_CK505_SDA - @m78_lib.M78	29B5 52D6
	SMBUS_SB_SDA - @m78_lib.M78	52D7
	=I2C_DIMMA_SDA - @m78_lib.M78	31A6 52D6
	=I2C_DIMMB_SDA - @m78_lib.M78	32A6 52C6
	SMBUS_SB_SDA - @m78_lib.M78	52D7
	=SMBUS_CK505_SDA - @m78_lib.M78	29B5 52D6
	=I2C_DIMMB_SDA - @m78_lib.M78	32A6 52C6
	=I2C_DIMMA_SDA - @m78_lib.M78	31A6 52D6
SMB_ME_CLK	SMB_ME_CLK - @m78_lib.M78	25D5 52A8 103A3
	SMBUS_SB_ME_SCL - @m78_lib.M78	52A7
SMB_ME_DATA	SMB_ME_DATA - @m78_lib.M78	25D5 52A8 103A3
	SMBUS_SB_ME_SDA - @m78_lib.M78	52A7
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @m78_lib.M78	49D5 50C5
	TP_SMC_ADAPTER_EN - @m78_lib.M78	50C3
SMC_BATT_ISENSE	SMC_BATT_ISENSE - @m78_lib.M78	49C5 50B5
	SMC_NB_1V25_ISENSE - @m78_lib.M78	49C5 50B5
	UNUSED_SMC_SENSE - @m78_lib.M78	50A2 50B3 50B3 50B3 50B3
	SMC_PBUS_VSENSE - @m78_lib.M78	49C5 50B5
	SMC_DCIN_ISENSE - @m78_lib.M78	49C5 50B5
	UNUSED_SMC_SENSE - @m78_lib.M78	50A2 50B3 50B3 50B3 50B3
	SMC_PBUS_VSENSE - @m78_lib.M78	49C5 50B5
	SMC_NB_1V25_ISENSE - @m78_lib.M78	49C5 50B5
	SMC_DCIN_ISENSE - @m78_lib.M78	49C5 50B5
SMC_BC_ACOK	SMC_BC_ACOK - @m78_lib.M78	49C5 50B2
SMC_BS_ALRT_L	SMC_BS_ALRT_L - @m78_lib.M78	49C5 50B2
SMC_CASE_OPEN	SMC_CASE_OPEN - @m78_lib.M78	49B5 50A2
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @m78_lib.M78	49C5 53C6
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @m78_lib.M78	49C5 53D6
SMC_EXCARD_CP	SMC_EXCARD_CP - @m78_lib.M78	49B8 50A2
SMC_EXCARD_OC_L	SMC_EXCARD_OC_L - @m78_lib.M78	49B8 50B2
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @m78_lib.M78	49B8 50B5
	TP_SMC_EXCARD_PWR_EN - @m78_lib.M78	50B3
SMC_EXTAL	SMC_EXTAL - @m78_lib.M78	49C3 50C8
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @m78_lib.M78	49A8 56D8
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @m78_lib.M78	49A8 56C8
SMC_FAN_1_CTL	SMC_FAN_1_CTL - @m78_lib.M78	49A8 56B8
SMC_FAN_1_TACH	SMC_FAN_1_TACH - @m78_lib.M78	49A8 56A8
SMC_FAN_2_CTL	SMC_FAN_2_CTL - @m78_lib.M78	49A8 57D8
SMC_FAN_2_TACH	SMC_FAN_2_TACH - @m78_lib.M78	49A8 57C8
SMC_FAN_3_CTL	SMC_FAN_3_CTL - @m78_lib.M78	49A8 50C5
	TP_SMC_FAN_3_CTL - @m78_lib.M78	50C3
SMC_FAN_3_TACH	SMC_FAN_3_TACH - @m78_lib.M78	49A8 50C5
	TP_SMC_FAN_3_TACH - @m78_lib.M78	50C3
SMC_FWE	SMC_FWE - @m78_lib.M78	49A5 50B2
SMC_GFX_OVERTEMP_L	SMC_GFX_OVERTEMP_L - @m78_lib.M78	49A8 85C8
SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L - @m78_lib.M78	49C8 85B7
SMC_GPU_ISENSE	SMC_GPU_ISENSE - @m78_lib.M78	49C5 53C1
SMC_GPU_VSENSE	SMC_GPU_VSENSE - @m78_lib.M78	49C5 53D2
SMC_KBC_MDE	SMC_KBC_MDE - @m78_lib.M78	49C2
SMC_LID	SMC_LID - @m78_lib.M78	49B5 50B2
SMC_LRESET_L	SMC_LRESET_L - @m78_lib.M78	7C6 28D1 49C8
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @m78_lib.M78	50D7
SMC_MD1	SMC_MD1 - @m78_lib.M78	7D4 49C1 51B6
SMC_MXM_VSENSE_R	SMC_MXM_VSENSE_R - @m78_lib.M78	53D3
SMC_NMI	SMC_NMI - @m78_lib.M78	7C4 49C1 51B4
SMC_ODD_DETECT	SMC_ODD_DETECT - @m78_lib.M78	49B8 50B2
SMC_ONOFF_L	SMC_ONOFF_L - @m78_lib.M78	49C5 50B2 50C5
SMC_P14	SMC_P14 - @m78_lib.M78	49D8 50D5
	TP_SMC_P14 - @m78_lib.M78	50D3
SMC_P20	SMC_P20 - @m78_lib.M78	49C8 50D5
	TP_SMC_P20 - @m78_lib.M78	50D3
SMC_P21	SMC_P21 - @m78_lib.M78	49C8 50D5
	TP_SMC_P21 - @m78_lib.M78	50D3
SMC_P22	SMC_P22 - @m78_lib.M78	49C8 50C5
	TP_SMC_P22 - @m78_lib.M78	50C3
SMC_P23	SMC_P23 - @m78_lib.M78	49C8 50C5
	TP_SMC_P23 - @m78_lib.M78	50C3
SMC_P26	SMC_P26 - @m78_lib.M78	49C8 50C5
	TP_SMC_P26 - @m78_lib.M78	50C3
SMC_P27	SMC_P27 - @m78_lib.M78	49C8 50C5
	TP_SMC_P27 - @m78_lib.M78	50C3
SMC_P43	SMC_P43 - @m78_lib.M78	49C8 50C5
	TP_SMC_P43 - @m78_lib.M78	50C3
SMC_P44	SMC_P44 - @m78_lib.M78	49C8 50C5
	TP_SMC_P44 - @m78_lib.M78	50C3
SMC_P45	SMC_P45 - @m78_lib.M78	49C8 50C5
	TP_SMC_P45 - @m78_lib.M78	50C3
SMC_P46	SMC_P46 - @m78_lib.M78	49B8 50B5
	TP_SMC_P46 - @m78_lib.M78	50B3
SMC_P62	SMC_P62 - @m78_lib.M78	49D5 50C5
	TP_SMC_P62 - @m78_lib.M78	50C3
SMC_P63	SMC_P63 - @m78_lib.M78	49D5 50C5
	TP_SMC_P63 - @m78_lib.M78	50C3
SMC_P64	SMC_P64 - @m78_lib.M78	49D5 50C5
	TP_SMC_P64 - @m78_lib.M78	50C3
SMC_P67	SMC_P67 - @m78_lib.M78	49C5 50B2
SMC_P81	SMC_P81 - @m78_lib.M78	49C5 50C5
	TP_SMC_P81 - @m78_lib.M78	50C3
SMC_PA0	SMC_PA0 - @m78_lib.M78	49B8 50B2
SMC_PA1	SMC_PA1 - @m78_lib.M78	49B8 50B2
SMC_PB0	SMC_PB0 - @m78_lib.M78	49B8 50B2
SMC_PF0	SMC_PF0 - @m78_lib.M78	49B5 50C5
	TP_SMC_PF0 - @m78_lib.M78	50C3
SMC_PF1	SMC_PF1 - @m78_lib.M78	49B5 50C5
	TP_SMC_PF1 - @m78_lib.M78	50C3

SMC_PF3	SMC_PF3 - @m78_lib.M78	49B5 50B2
SMC_PG0	SMC_PG0 - @m78_lib.M78	49B5 50B2
SMC_PH4	SMC_PH4 - @m78_lib.M78	49A5 50B2
SMC_PM_G2_EN	SMC_PM_G2_EN - @m78_lib.M78	49D5 50C5
	TP_SMC_PM_G2_EN - @m78_lib.M78	50C3
SMC_PROCHOT	SMC_PROCHOT - @m78_lib.M78	49A5 50C1
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @m78_lib.M78	49C5 50D1
SMC_RESET_L	SMC_RESET_L - @m78_lib.M78	7C4 7C6 49C3 50D6 51B4
SMC_RSTGATE_L	SMC_RSTGATE_L - @m78_lib.M78	49D8 50B5
	TP_SMC_RSTGATE_L - @m78_lib.M78	50B3
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @m78_lib.M78	25C8 49B8
SMC_RX_L	SMC_RX_L - @m78_lib.M78	7C4 46D5 49B8 49C5 50B2 51B4
SMC_SUS_CLK	SMC_SUS_CLK - @m78_lib.M78	49C5 50C3
	SUS_CLK_SB - @m78_lib.M78	25D3 50C2
SMC_SYS_KBDLED	SMC_SYS_KBDLED - @m78_lib.M78	49B8 50B5
	TP_SMC_SYS_KBDLED - @m78_lib.M78	50B3
SMC_SYS_LED	SMC_SYS_LED - @m78_lib.M78	49C8 50A5 50A8
SMC_TCK	SMC_TCK - @m78_lib.M78	7D4 49B5 50B2 51B4
SMC_TDI	SMC_TDI - @m78_lib.M78	7D4 49B5 50B2 51B4
SMC_TDO	SMC_TDO - @m78_lib.M78	7D4 49B5 50B2 51B6
SMC_THRMTRIP	SMC_THRMTRIP - @m78_lib.M78	49A5 50C1
SMC_TMS	SMC_TMS - @m78_lib.M78	7D4 49B5 50B2 51B6
SMC_TRST_L	SMC_TRST_L - @m78_lib.M78	7D4 49C1 51B6
SMC_TX_L	SMC_TX_L - @m78_lib.M78	7D4 46D5 49B8 49C5 50B2 51B6
SMC_VCL	SMC_VCL - @m78_lib.M78	49D2
SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @m78_lib.M78	13C3 25C8 49C5
SMC_XTAL	SMC_XTAL - @m78_lib.M78	49C3 50C8
SMS_ONOFF_L	SMS_ONOFF_L - @m78_lib.M78	49A5 50B5
	TP_SMS_ONOFF_L - @m78_lib.M78	50B3
SMS_X_AXIS	SMS_X_AXIS - @m78_lib.M78	49A8 50D5 108D1
	NC_SMS_X_AXIS - @m78_lib.M78	50D3
SMS_Y_AXIS	SMS_Y_AXIS - @m78_lib.M78	49A8 50D5 108D1
	NC_SMS_Y_AXIS - @m78_lib.M78	50D3
SMS_Z_AXIS	SMS_Z_AXIS - @m78_lib.M78	49A8 50D5 108D1
	NC_SMS_Z_AXIS - @m78_lib.M78	50D3
SPI_A_SCLK_R	SPI_A_SCLK_R - @m78_lib.M78	103A3
SPI_A_SI_R	SPI_A_SI_R - @m78_lib.M78	61B4 103A3
SPI_A_SO_R	SPI_A_SO_R - @m78_lib.M78	7B3 61B4 103A3
SPI_B_SCLK_R	SPI_B_SCLK_R - @m78_lib.M78	103A3
SPI_B_SI_R	SPI_B_SI_R - @m78_lib.M78	103A3
SPI_B_SO	SPI_B_SO - @m78_lib.M78	103A3
SPI_B_SO_R	SPI_B_SO_R - @m78_lib.M78	103A3
SPI_CE_L<0>	SPI_CE_L<0> - @m78_lib.M78	7B3 61B6 103A3
SPI_CE_L<1>	SPI_CE_L<1> - @m78_lib.M78	103A3
SPI_CE_R_L<0>	SPI_CE_R_L<0> - @m78_lib.M78	24C5 61B7 103A3
SPI_CE_R_L<1>	SPI_CE_R_L<1> - @m78_lib.M78	103A3
SPI_HOLD_L	SPI_HOLD_L - @m78_lib.M78	61B5
SPI_SCLK	SPI_SCLK - @m78_lib.M78	7A8 61B6 103A3
SPI_SCLK_R	SPI_SCLK_R - @m78_lib.M78	24C5 61B7 103A3
SPI_SI	SPI_SI - @m78_lib.M78	103A3
SPI_SI_R	SPI_SI_R - @m78_lib.M78	24C5 61B3 103A3
SPI_SO	SPI_SO - @m78_lib.M78	7A8 24C5 61B3 103A3
SPI_WP_L	SPI_WP_L - @m78_lib.M78	61B5
SYSLED_SW	SYSLED_SW - @m78_lib.M78	50A4
SYS_LED_ANODE	SYS_LED_ANODE - @m78_lib.M78	50A6
SYS_LED_ANODE_CONN	SYS_LED_ANODE_CONN - @m78_lib.M78	50A3 50A4 50A5
SYS_LED_BIAS	SYS_LED_BIAS - @m78_lib.M78	50A7
SYS_LED_EN	SYS_LED_EN - @m78_lib.M78	50A8
SYS_LED_ILIM	SYS_LED_ILIM - @m78_lib.M78	50A6
SYS_LED_IREF	SYS_LED_IREF - @m78_lib.M78	50A7
SYS_LED_RETURN_CONN	SYS_LED_RETURN_CONN - @m78_lib.M78	50A3 50A4 50A5
SYS_LGP_ANODE	SYS_LGP_ANODE - @m78_lib.M78	50A4
SYS_LGP_RETURN	SYS_LGP_RETURN - @m78_lib.M78	50A4
SYS_ONEWIRE	SYS_ONEWIRE - @m78_lib.M78	49B8 50B2
TMDS_CLK_N	TMDS_CLK_N - @m78_lib.M78	85A7 94C8 108D3
TMDS_CLK_P	TMDS_CLK_P - @m78_lib.M78	85A7 94B8 108D3
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @m78_lib.M78	94C4 94C7 108D3
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @m78_lib.M78	94B7 94C4 108D3
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @m78_lib.M78	94C4 94D6
TMDS_CONN_DN<3..0>	TMDS_CONN_DN<3..0> - @m78_lib.M78	108D3
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @m78_lib.M78	94C4 94D6
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @m78_lib.M78	94C6 94D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @m78_lib.M78	94C4 94D6
TMDS_CONN_DP<3..0>	TMDS_CONN_DP<3..0> - @m78_lib.M78	108D3
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @m78_lib.M78	94C4 94D6
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @m78_lib.M78	94C6 94D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @m78_lib.M78	85A7 94D8
TMDS_DATA_N<3..0>	TMDS_DATA_N<3..0> - @m78_lib.M78	108D3
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @m78_lib.M78	85A7 94D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @m78_lib.M78	85A7 94C8
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @m78_lib.M78	85A7 94D8
TMDS_DATA_P<3..0>	TMDS_DATA_P<3..0> - @m78_lib.M78	108D3
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @m78_lib.M78	85A7 94C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @m78_lib.M78	85A7 94C8
TP_CK505_PGMODE	TP_CK505_PGMODE - @m78_lib.M78	29B5
TP_CPU_RSVD0	TP_CPU_RSVD0 - @m78_lib.M78	10B8
TP_CPU_RSVD1	TP_CPU_RSVD1 - @m78_lib.M78	10B8
TP_CPU_RSVD2	TP_CPU_RSVD2 - @m78_lib.M78	10B8
TP_CPU_RSVD3	TP_CPU_RSVD3 - @m78_lib.M78	10B8
TP_CPU_RSVD4	TP_CPU_RSVD4 - @m78_lib.M78	10B8
TP_CPU_RSVD5	TP_CPU_RSVD5 - @m78_lib.M78	10B8
TP_CPU_RSVD6	TP_CPU_RSVD6 - @m78_lib.M78	10B8
TP_CPU_RSVD7	TP_CPU_RSVD7 - @m78_lib.M78	10B8
TP_CPU_RSVD8	TP_CPU_RSVD8 - @m78_lib.M78	10B8
TP_CPU_RSVD9	TP_CPU_RSVD9 - @m78_lib.M78	10B8
TP_CPU_TEST3	TP_CPU_TEST3 - @m78_lib.M78	10B4
TP_CPU_TEST5	TP_CPU_TEST5 - @m78_lib.M78	10B4
TP_CPU_TEST6	TP_CPU_TEST6 - @m78_lib.M78	10B4
TP_ENET_GLAN_CLK	TP_ENET_GLAN_CLK - @m78_lib.M78	23C6
TP_FW_AVREG	TP_FW_AVREG - @m78_lib.M78	40B6
TP_FW_CE	TP_FW_CE - @m78_lib.M78	7B3 40B6
TP_FW_FW620_L	TP_FW_FW620_L - @m78_lib.M78	40B6
TP_FW_JASI_EN	TP_FW_JASI_EN - @m78_lib.M78	40B6
TP_FW_MODE_A	TP_FW_MODE_A - @m78_lib.M78	40B6
TP_FW_NAND_TREE	TP_FW_NAND_TREE - @m78_lib.M78	7C3 40B6
TP_FW_SCIFCLK	TP_FW_SCIFCLK - @m78_lib.M78	40B3
TP_FW_SCIFDAIN	TP_FW_SCIFDAIN - @m78_lib.M78	40B3
TP_FW_SCIFDOUT	TP_FW_SCIFDOUT - @m78_lib.M78	40B3
TP_FW_SCIFMC	TP_FW_SCIFMC - @m78_lib.M78	40B3
TP_FW_SDA	TP_FW_SDA - @m78_lib.M78	40B3
TP_FW_SE	TP_FW_SE - @m78_lib.M78	7C3 40B6
TP_FW_SM	TP_FW_SM - @m78_lib.M78	7C3 40B6
TP_FW_TCK	TP_FW_TCK - @m78_lib.M78	7C3 40C3
TP_FW_TDI	TP_FW_TDI - @m78_lib.M78	7C3 40C3
TP_FW_TDO	TP_FW_TDO - @m78_lib.M78	7C3 40C3
TP_FW_TMS	TP_FW_TMS - @m78_lib.M78	7C3 40C3
TP_FW_VAUX_DISABLE	TP_FW_VAUX_DISABLE - @m78_lib.M78	40C3
TP_FW_VBUF	TP_FW_VBUF - @m78_lib.M78	40B6
TP_GPU_DDC_B_CLK	TP_GPU_DDC_B_CLK - @m78_lib.M78	85A4
TP_GPU_DDC_B_DATA	TP_GPU_DDC_B_DATA - @m78_lib.M78	85A4
TP_HDA_DOCK_RST_L	TP_HDA_DOCK_RST_L - @m78_lib.M78	23B6
TP_HDA_SDIN1	TP_HDA_SDIN1 - @m78_lib.M78	23C8

TP_HDA_SDIN2	TP_HDA_SDIN2 - @m78_lib.M78	23C8
TP_HDA_SDIN3	TP_HDA_SDIN3 - @m78_lib.M78	23C8
TP_LAN_D2R<0>	TP_LAN_D2R<0> - @m78_lib.M78	23C6
TP_LAN_D2R<1>	TP_LAN_D2R<1> - @m78_lib.M78	23C6
TP_LAN_D2R<2>	TP_LAN_D2R<2> - @m78_lib.M78	23C6 28C4
TP_LAN_R2D<0>	TP_LAN_R2D<0> - @m78_lib.M78	23C6
TP_LAN_R2D<1>	TP_LAN_R2D<1> - @m78_lib.M78	23C6
TP_LAN_R2D<2>	TP_LAN_R2D<2> - @m78_lib.M78	23C6
TP_LAN_RSTSYNC	TP_LAN_RSTSYNC - @m78_lib.M78	23C6
TP_LPC_DRQ0_L	TP_LPC_DRQ0_L - @m78_lib.M78	23D4
TP_LVDS_A_DATAN3	TP_LVDS_A_DATAN3 - @m78_lib.M78	16C6
TP_LVDS_A_DATAP3	TP_LVDS_A_DATAP3 - @m78_lib.M78	16C6
TP_LVDS_B_DATAN3	TP_LVDS_B_DATAN3 - @m78_lib.M78	16C6
TP_LVDS_B_DATAP3	TP_LVDS_B_DATAP3 - @m78_lib.M78	16C6
TP_LVDS_VBG	TP_LVDS_VBG - @m78_lib.M78	15D5
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @m78_lib.M78	31C3
TP_MEM_A_RCVEN_L	TP_MEM_A_RCVEN_L - @m78_lib.M78	17B5
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @m78_lib.M78	32C3
TP_MEM_B_RCVEN_L	TP_MEM_B_RCVEN_L - @m78_lib.M78	17B2
TP_MEM_CLKN2	TP_MEM_CLKN2 - @m78_lib.M78	16C6
TP_MEM_CLKN5	TP_MEM_CLKN5 - @m78_lib.M78	16C6
TP_MEM_CLKP2	TP_MEM_CLKP2 - @m78_lib.M78	16C6
TP_MEM_CLKP5	TP_MEM_CLKP5 - @m78_lib.M78	16C6
TP_NB_CFG<10>	TP_NB_CFG<10> - @m78_lib.M78	16B6
TP_NB_CFG<11>	TP_NB_CFG<11> - @m78_lib.M78	16B6
TP_NB_CFG<12>	TP_NB_CFG<12> - @m78_lib.M78	7C3 16B6
TP_NB_CFG<13>	TP_NB_CFG<13> - @m78_lib.M78	7C3 16B6
TP_NB_CFG<14>	TP_NB_CFG<14> - @m78_lib.M78	16B6
TP_NB_CFG<15>	TP_NB_CFG<15> - @m78_lib.M78	16B6
TP_NB_CFG<17>	TP_NB_CFG<17> - @m78_lib.M78	16B6
TP_NB_CFG<18>	TP_NB_CFG<18> - @m78_lib.M78	7C3 16B6
TP_NB_NC<1>	TP_NB_NC<1> - @m78_lib.M78	16A6
TP_NB_NC<2>	TP_NB_NC<2> - @m78_lib.M78	16A6
TP_NB_NC<3>	TP_NB_NC<3> - @m78_lib.M78	16A6
TP_NB_NC<4>	TP_NB_NC<4> - @m78_lib.M78	16A6
TP_NB_NC<5>	TP_NB_NC<5> - @m78_lib.M78	16A6
TP_NB_NC<6>	TP_NB_NC<6> - @m78_lib.M78	16A6
TP_NB_NC<7>	TP_NB_NC<7> - @m78_lib.M78	16A6
TP_NB_NC<8>	TP_NB_NC<8> - @m78_lib.M78	16A6
TP_NB_NC<9>	TP_NB_NC<9> - @m78_lib.M78	16A6
TP_NB_NC<10>	TP_NB_NC<10> - @m78_lib.M78	16A6
TP_NB_NC<11>	TP_NB_NC<11> - @m78_lib.M78	16A6
TP_NB_NC<12>	TP_NB_NC<12> - @m78_lib.M78	16A6
TP_NB_NC<13>	TP_NB_NC<13> - @m78_lib.M78	16A6
TP_NB_NC<14>	TP_NB_NC<14> - @m78_lib.M78	16A6
TP_NB_NC<15>	TP_NB_NC<15> - @m78_lib.M78	16A6
TP_NB_NC<16>	TP_NB_NC<16> - @m78_lib.M78	16A6
TP_NB_RSVD<1>	TP_NB_RSVD<1> - @m78_lib.M78	16D6
TP_NB_RSVD<2>	TP_NB_RSVD<2> - @m78_lib.M78	16D6
TP_NB_RSVD<3>	TP_NB_RSVD<3> - @m78_lib.M78	16D6
TP_NB_RSVD<4>	TP_NB_RSVD<4> - @m78_lib.M78	16D6
TP_NB_RSVD<5>	TP_NB_RSVD<5> - @m78_lib.M78	16D6
TP_NB_RSVD<6>	TP_NB_RSVD<6> - @m78_lib.M78	16D6
TP_NB_RSVD<7>	TP_NB_RSVD<7> - @m78_lib.M78	16D6
TP_NB_RSVD<8>	TP_NB_RSVD<8> - @m78_lib.M78	16D6
TP_NB_RSVD<9>	TP_NB_RSVD<9> - @m78_lib.M78	16D6
TP_NB_RSVD<10>	TP_NB_RSVD<10> - @m78_lib.M78	16D6
TP_NB_RSVD<11>	TP_NB_RSVD<11> - @m78_lib.M78	16D6
TP_NB_RSVD<12>	TP_NB_RSVD<12> - @m78_lib.M78	16D6
TP_NB_RSVD<13>	TP_NB_RSVD<13> - @m78_lib.M78	16D6
TP_NB_RSVD<14>	TP_NB_RSVD<14> - @m78_lib.M78	16D6
TP_NB_RSVD<20>	TP_NB_RSVD<20> - @m78_lib.M78	16D6
TP_NB_RSVD<21>	TP_NB_RSVD<21> - @m78_lib.M78	16D6
TP_NB_RSVD<22>	TP_NB_RSVD<22> - @m78_lib.M78	16C6
TP_NB_RSVD<23>	TP_NB_RSVD<23> - @m78_lib.M78	16C6
TP_NB_RSVD<24>	TP_NB_RSVD<24> - @m78_lib.M78	16C6
TP_NB_RSVD<25>	TP_NB_RSVD<25> - @m78_lib.M78	16C6
TP_NB_RSVD<26>	TP_NB_RSVD<26> - @m78_lib.M78	16C6
TP_NB_RSVD<27>	TP_NB_RSVD<27> - @m78_lib.M78	16C6
TP_NB_RSVD<34>	TP_NB_RSVD<34> - @m78_lib.M78	16C6
TP_NB_RSVD<35>	TP_NB_RSVD<35> - @m78_lib.M78	16C6
TP_NB_RSVD<36>	TP_NB_RSVD<36> - @m78_lib.M78	16C6
TP_NB_RSVD<41>	TP_NB_RSVD<41> - @m78_lib.M78	16C6
TP_NB_RSVD<42>	TP_NB_RSVD<42> - @m78_lib.M78	16C6
TP_NB_RSVD<43>	TP_NB_RSVD<43> - @m78_lib.M78	16C6
TP_NB_RSVD<44>	TP_NB_RSVD<44> - @m78_lib.M78	16C6
TP_NB_RSVD<45>	TP_NB_RSVD<45> - @m78_lib.M78	16C6
TP_PCIE_A_D2R_N	TP_PCIE_A_D2R_N - @m78_lib.M78	24D5
TP_PCIE_A_D2R_P	TP_PCIE_A_D2R_P - @m78_lib.M78	24D5
TP_PCIE_A_R2D_C_N	TP_PCIE_A_R2D_C_N - @m78_lib.M78	24D5
TP_PCIE_A_R2D_C_P	TP_PCIE_A_R2D_C_P - @m78_lib.M78	24D5
TP_PCIE_B_D2R_N	TP_PCIE_B_D2R_N - @m78_lib.M78	24D5
TP_PCIE_B_D2R_P	TP_PCIE_B_D2R_P - @m78_lib.M78	24D5
TP_PCIE_B_R2D_C_N	TP_PCIE_B_R2D_C_N - @m78_lib.M78	24D5
TP_PCIE_B_R2D_C_P	TP_PCIE_B_R2D_C_P - @m78_lib.M78	24D5
TP_PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N - @m78_lib.M78	24D5
TP_PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P - @m78_lib.M78	24D5
TP_PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N - @m78_lib.M78	24D5
TP_PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P - @m78_lib.M78	24D5
TP_PCI_PME_L	TP_PCI_PME_L - @m78_lib.M78	24A6
TP_PM_SLP_M_L	TP_PM_SLP_M_L - @m78_lib.M78	25C3
TP_PM_SLP_S4_L	TP_PM_SLP_S4_L - @m78_lib.M78	25D3
TP_PP5VREG_PLLIN	TP_PP5VREG_PLLIN - @m78_lib.M78	76B5
TP_SB_GPIO51	TP_SB_GPIO51 - @m78_lib.M78	24B6
TP_SB_GPIO53	TP_SB_GPIO53 - @m78_lib.M78	24B6
TP_SB_GPIO55	TP_SB_GPIO55 - @m78_lib.M78	24B6
TP_SB_TP3	TP_SB_TP3 - @m78_lib.M78	25B5
TP_SB_TP7	TP_SB_TP7 - @m78_lib.M78	25C5
TP_SB_TP8	TP_SB_TP8 - @m78_lib.M78	23C4
TP_SPI_CE_R_L<1>	TP_SPI_CE_R_L<1> - @m78_lib.M78	24C5
TP_VCCCL1_05_INTERNAL_REG	TP_VCCCL1_05_INTERNAL_REG - @m78_lib.M78	26A3
TP_VCCLAN1_05_INTERNAL_REG1	TP_VCCLAN1_05_INTERNAL_REG1 - @m78_lib.M78	26A6
TP_VCCLAN1_05_INTERNAL_REG2	TP_VCCLAN1_05_INTERNAL_REG2 - @m78_lib.M78	26A6
TP_VCCSUS1_05_INTERNAL_REG1	TP_VCCSUS1_05_INTERNAL_REG1 - @m78_lib.M78	26B3
TP_VCCSUS1_05_INTERNAL_REG2	TP_VCCSUS1_05_INTERNAL_REG2 - @m78_lib.M78	26B3
TP_VCCSUS1_5_INTERNAL_REG1	TP_VCCSUS1_5_INTERNAL_REG1 - @m78_lib.M78	26B3
TP_VCCSUS1_5_INTERNAL_REG2	TP_VCCSUS1_5_INTERNAL_REG2 - @m78_lib.M78	26B3
TP_XDP_HOOK2	TP_XDP_HOOK2 - @m78_lib.M78	13B6
TP_XDP_HOOK3	TP_XDP_HOOK3 - @m78_lib.M78	13B6
U5500_TCRIT1	U5500_TCRIT1 - @m78_lib.M78	55B3
U5500_TCRIT2	U5500_TCRIT2 - @m78_lib.M78	55B3
U5500_TCRIT3	U5500_TCRIT3 - @m78_lib.M78	55A3
U7550_VDDQ	U7550_VDDQ - @m78_lib.M78	75B5
USB_BT_N	USB_BT_N - @m78_lib.M78	7A8 24C2 47D3 103B3
USB_BT_P	USB_BT_P - @m78_lib.M78	7A8 24C2 47C3 103B3

USB_CAMERA_L_N	USB_CAMERA_L_N - @m78_lib.M78	47B5 108C3
USB_CAMERA_L_P	USB_CAMERA_L_P - @m78_lib.M78	47B5 108C3
USB_CAMERA_N	USB_CAMERA_N - @m78_lib.M78	7A8 24C2 47B7 103B3
USB_CAMERA_P	USB_CAMERA_P - @m78_lib.M78	7A8 24C2 47B7 103B3
USB_C_MUXED_N	USB_C_MUXED_N - @m78_lib.M78	46D3 108C3
USB_C_MUXED_P	USB_C_MUXED_P - @m78_lib.M78	46D3 108D3
USB_DEBUGPRT_EN_L	USB_DEBUGPRT_EN_L - @m78_lib.M78	46C4 49B8
USB_EXCARD_N	USB_EXCARD_N - @m78_lib.M78	24C2 47B3 103B3
	TP_USB_EXCARD_N - @m78_lib.M78	47B1
USB_EXCARD_P	USB_EXCARD_P - @m78_lib.M78	24C2 47B3 103B3
	TP_USB_EXCARD_P - @m78_lib.M78	47B1
USB_EXTA_MUXED_N	USB_EXTA_MUXED_N - @m78_lib.M78	103B3
USB_EXTA_MUXED_P	USB_EXTA_MUXED_P - @m78_lib.M78	103B3
USB_EXTA_N	USB_EXTA_N - @m78_lib.M78	24C2 46A7 103B3
USB_EXTA_OC_L	USB_EXTA_OC_L - @m78_lib.M78	13C3 24C8 46C8
USB_EXTA_P	USB_EXTA_P - @m78_lib.M78	24C2 46A7 103B3
USB_EXTB_N	USB_EXTB_N - @m78_lib.M78	24C2 46B7 103B3
USB_EXTB_OC_L	USB_EXTB_OC_L - @m78_lib.M78	13C3 24C8 46C8
USB_EXTB_P	USB_EXTB_P - @m78_lib.M78	24C2 46B7 103B3
USB_EXTC_N	USB_EXTC_N - @m78_lib.M78	24C2 46D5 103A3
USB_EXTC_OC_L	USB_EXTC_OC_L - @m78_lib.M78	24C8 46D8
USB_EXTC_P	USB_EXTC_P - @m78_lib.M78	24C2 46D5 103B3
USB_EXTD_N	USB_EXTD_N - @m78_lib.M78	24C2 46B3 103B3
	TP_USB_EXTD_N - @m78_lib.M78	46B2
USB_EXTD_OC_L	USB_EXTD_OC_L - @m78_lib.M78	13C3 24C8
USB_EXTD_P	USB_EXTD_P - @m78_lib.M78	24C2 46B3 103B3
	TP_USB_EXTD_P - @m78_lib.M78	46B2
USB_IR_L_N	USB_IR_L_N - @m78_lib.M78	47A5 58C5 108C3
USB_IR_L_P	USB_IR_L_P - @m78_lib.M78	47A5 58C5 108C3
USB_IR_N	USB_IR_N - @m78_lib.M78	7A8 24C2 47A7 103B3
USB_IR_P	USB_IR_P - @m78_lib.M78	7A8 24C2 47A7 103B3
USB_MINI_N	USB_MINI_N - @m78_lib.M78	24C2 34B3 103B3
USB_MINI_P	USB_MINI_P - @m78_lib.M78	24C2 34B3 103B3
USB_PORT0_N	USB_PORT0_N - @m78_lib.M78	46A5 108D3
USB_PORT0_P	USB_PORT0_P - @m78_lib.M78	46A5 108D3
USB_PORT1_N	USB_PORT1_N - @m78_lib.M78	46B5 108D3
USB_PORT1_P	USB_PORT1_P - @m78_lib.M78	46B5 108D3
USB_PORT2_N	USB_PORT2_N - @m78_lib.M78	46D2 108D3
USB_PORT2_P	USB_PORT2_P - @m78_lib.M78	46D2 108D3
USB_PWR_ENA_L	USB_PWR_ENA_L - @m78_lib.M78	46D8
USB_RBIAS	USB_RBIAS - @m78_lib.M78	24B3 103A3
USB_TPAD_N	USB_TPAD_N - @m78_lib.M78	24C2 47B3 103B3
	TP_USB_TPAD_N - @m78_lib.M78	47B2
USB_TPAD_P	USB_TPAD_P - @m78_lib.M78	24C2 47B3 103B3
	TP_USB_TPAD_P - @m78_lib.M78	47B2
VCCCL1_5V	VCCCL1_5V - @m78_lib.M78	26A4
VGA_BLU	VGA_BLU - @m78_lib.M78	91A4 94C5 108A3
VGA_GRN	VGA_GRN - @m78_lib.M78	91B4 94C5 108A3
VGA_HSYNC	VGA_HSYNC - @m78_lib.M78	91A2 94C5 108A3
VGA_HSYNC_R	VGA_HSYNC_R - @m78_lib.M78	91A3
VGA_RED	VGA_RED - @m78_lib.M78	91B4 94C5 108A3
VGA_VSYNC	VGA_VSYNC - @m78_lib.M78	91B2 94C5 108A3
VGA_VSYNC_R	VGA_VSYNC_R - @m78_lib.M78	91B3
VIDEO_MUX_BLU	VIDEO_MUX_BLU - @m78_lib.M78	91B7 108A3
VIDEO_MUX_GRN	VIDEO_MUX_GRN - @m78_lib.M78	91B7 108A3
VIDEO_MUX_RED	VIDEO_MUX_RED - @m78_lib.M78	91B7 108A3
VR_PWRGD_CLKEN	VR_PWRGD_CLKEN - @m78_lib.M78	7C4 25C5 28A6
VR_PWRGD_CLKEN_L	VR_PWRGD_CLKEN_L - @m78_lib.M78	28A8 71C7
WOL_EN	WOL_EN - @m78_lib.M78	25B3
WOW_EN	WOW_EN - @m78_lib.M78	13C3 24C8
XDP_BPM_L<0>	XDP_BPM_L<0> - @m78_lib.M78	10C6 13C6
XDP_BPM_L<4..0>	XDP_BPM_L<4..0> - @m78_lib.M78	100A3
XDP_BPM_L<1>	XDP_BPM_L<1> - @m78_lib.M78	10C6 13C6
XDP_BPM_L<2>	XDP_BPM_L<2> - @m78_lib.M78	10C6 13C6
XDP_BPM_L<3>	XDP_BPM_L<3> - @m78_lib.M78	10C6 13C6
XDP_BPM_L<4>	XDP_BPM_L<4> - @m78_lib.M78	10C6 13C6
XDP_BPM_L<5>	XDP_BPM_L<5> - @m78_lib.M78	10C5 13C6 100A3
XDP_CPURST_L	XDP_CPURST_L - @m78_lib.M78	13B4
XDP_DBRESET_L	XDP_DBRESET_L - @m78_lib.M78	10C6 13B3 28A5
XDP_OBS20	XDP_OBS20 - @m78_lib.M78	13B6
XDP_PWRGD	XDP_PWRGD - @m78_lib.M78	13C6
XDP_TCK	XDP_TCK - @m78_lib.M78	10A7 10C6 13B6 100A3
XDP_TDI	XDP_TDI - @m78_lib.M78	10B7 10C6 13B3 100A3
XDP_TDO	XDP_TDO - @m78_lib.M78	10A7 10C6 13B3 100A3
XDP_TMS	XDP_TMS - @m78_lib.M78	10B7 10C6 13B3 100A3
XDP_TRST_L	XDP_TRST_L - @m78_lib.M78	10A7 10C6 13B3 100A3
YUKON_RSET	YUKON_RSET - @m78_lib.M78	37C2
YUKON_VPD_CLK	YUKON_VPD_CLK - @m78_lib.M78	37B2
YUKON_VPD_DATA	YUKON_VPD_DATA - @m78_lib.M78	37B2

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C600	CAP_402	m78[6D7]
C621	CAP_603	m78[6D6]
C622	CAP_805	m78[6D7]
C623	CAP_805	m78[6D7]
C624	CAP_1210	m78[6D8]
C625	CAP_P_6.3X5.5-SM	m78[6D8]
C701	CAP_402	m78[7C6]
C702	CAP_402	m78[7C5]
C703	CAP_402	m78[7C6]
C704	CAP_402	m78[7C5]
C705	CAP_402	m78[7C6]
C706	CAP_402	m78[7B5]
C707	CAP_402	m78[7B6]
C708	CAP_402	m78[7B5]
C709	CAP_402	m78[7B6]
C710	CAP_402	m78[7B5]
C1000	CAP_402	m78[10B5]
C1200	CAP_805	m78[12D7]
C1201	CAP_805	m78[12D6]
C1202	CAP_805	m78[12D6]
C1203	CAP_805	m78[12D6]
C1204	CAP_805	m78[12D6]
C1205	CAP_805	m78[12D5]
C1206	CAP_805	m78[12D5]
C1207	CAP_805	m78[12D5]
C1208	CAP_805	m78[12D4]
C1209	CAP_805	m78[12D4]
C1210	CAP_805	m78[12C7]
C1211	CAP_805	m78[12C6]
C1212	CAP_805	m78[12C6]
C1213	CAP_805	m78[12C6]
C1214	CAP_805	m78[12C6]
C1215	CAP_805	m78[12C5]
C1216	CAP_805	m78[12C5]
C1217	CAP_805	m78[12C5]
C1218	CAP_805	m78[12C4]
C1219	CAP_805	m78[12C4]
C1220	CAP_805	m78[12C7]
C1221	CAP_805	m78[12C6]
C1222	CAP_805	m78[12C6]
C1223	CAP_805	m78[12C6]
C1224	CAP_805	m78[12C6]
C1225	CAP_805	m78[12C5]
C1226	CAP_805	m78[12B7]
C1227	CAP_805	m78[12B6]
C1228	CAP_805	m78[12B6]
C1229	CAP_805	m78[12B6]
C1230	CAP_805	m78[12B6]
C1231	CAP_805	m78[12B5]
C1235	CAP_P_6.3X8-SM	m78[12A3]
C1236	CAP_402	m78[12A2]
C1237	CAP_402	m78[12A2]
C1238	CAP_402	m78[12A2]
C1239	CAP_402	m78[12A2]
C1240	CAP_402	m78[12A1]
C1241	CAP_402	m78[12A1]
C1250	CAP_P_CASE-D2-SM1	m78[12B7]
C1251	CAP_P_CASE-D2-SM1	m78[12B6]
C1252	CAP_P_CASE-D2-SM1	m78[12B5]
C1253	CAP_P_CASE-D2-SM1	m78[12B5]
C1254	CAP_P_CASE-D2-SM1	m78[12B6]
C1255	CAP_P_CASE-D2-SM1	m78[12B5]
C1280	CAP_603	m78[12B3]
C1281	CAP_402	m78[12B2]
C1300	CAP_402	m78[13B5]
C1301	CAP_402	m78[13B4]
C1410	CAP_402	m78[14A6]
C1425	CAP_402	m78[14A7]
C1615	CAP_402	m78[16C3]
C1616	CAP_402	m78[16C3]
C1622	CAP_603	m78[16C1]
C1623	CAP_402	m78[16C1]
C1624	CAP_603	m78[16C1]
C1625	CAP_402	m78[16C1]
C1640	CAP_402	m78[16A3]
C1801	CAP_402	m78[18A4]
C1802	CAP_402	m78[18A4]
C1803	CAP_402	m78[18A4]
C1804	CAP_402	m78[18A4]
C1805	CAP_402	m78[18A5]
C1806	CAP_402	m78[18A5]
C1807	CAP_402	m78[18A5]
C1911	CAP_402	m78[19A3]
C1912	CAP_402	m78[19A3]
C1913	CAP_402	m78[19A3]
C2100	CAP_P_6.3X8-SM	m78[21D7]
C2101	CAP_805	m78[21D7]
C2102	CAP_402	m78[21D7]
C2103	CAP_402	m78[21D6]
C2104	CAP_402	m78[21D6]
C2110	CAP_805	m78[21C7]
C2111	CAP_402	m78[21C7]
C2112	CAP_402	m78[21C7]
C2113	CAP_402	m78[21C6]
C2114	CAP_402	m78[21C6]
C2115	CAP_402	m78[21C6]
C2120	CAP_P_6.3X8-SM	m78[21C7]
C2121	CAP_603	m78[21C7]
C2122	CAP_603	m78[21C7]
C2123	CAP_603	m78[21C6]
C2124	CAP_402	m78[21C6]
C2130	CAP_P_6.3X8-SM	m78[21C7]
C2131	CAP_805	m78[21C7]
C2132	CAP_805	m78[21C7]
C2135	CAP_402	m78[21C7]
C2140	CAP_P_6.3X8-SM	m78[21B7]
C2141	CAP_805	m78[21B7]
C2142	CAP_805	m78[21B6]
C2143	CAP_603	m78[21B6]
C2144	CAP_402-1	m78[21B6]
C2145	CAP_805	m78[21B6]
C2146	CAP_603	m78[21B6]
C2148	CAP_402	m78[21B6]
C2150	CAP_805	m78[21A7]
C2151	CAP_402-1	m78[21A6]
C2160	CAP_402	m78[21A7]
C2161	CAP_402	m78[21A7]
C2165	CAP_402	m78[21A7]
C2170	CAP_603	m78[21D4]
C2171	CAP_402-1	m78[21D4]
C2173	CAP_P_SM-CASE-C1	m78[21C4]
C2174	CAP_603	m78[21C4]
C2177	CAP_603	m78[21C4]
C2180	CAP_402	m78[21D2]
C2181	CAP_805	m78[21D2]
C2182	CAP_402	m78[21D2]
C2183	CAP_805	m78[21C3]
C2184	CAP_402	m78[21C2]
C2190	CAP_603	m78[21B4]
C2191	CAP_402	m78[21B3]
C2192	CAP_402	m78[21B3]
C2195	CAP_603	m78[21A4]
C2196	CAP_805	m78[21A3]
C2197	CAP_402	m78[21A3]
C2200	CAP_402	m78[22B2]
C2201	FILTER_3P_A_NFM18	m78[22B2]
C2213	CAP_603	m78[22B2]
C2500	CAP_402	m78[25C2]
C2501	CAP_402	m78[25B2]
C2600	CAP_402	m78[26A3]
C2601	CAP_402	m78[26A3]
C2700	CAP_P_SM-CASE-C1	m78[27C7]
C2701	CAP_402	m78[27A6]
C2702	CAP_402	m78[27B1]
C2703	CAP_402	m78[27C8]
C2704	CAP_402	m78[27D8]
C2705	CAP_805	m78[27C7]
C2706	CAP_805	m78[27C7]
C2707	CAP_603	m78[27C7]
C2708	CAP_603	m78[27A6]
C2711	CAP_402	m78[27D1]
C2712	CAP_402	m78[27C1]
C2714	CAP_402	m78[27D1]
C2715	CAP_402	m78[27C1]
C2717	CAP_402	m78[27A6]
C2718	CAP_402	m78[27B1]
C2719	CAP_402	m78[27D3]
C2721	CAP_402	m78[27B3]
C2722	CAP_402	m78[27B1]
C2723	CAP_402	m78[27B1]
C2724	CAP_603	m78[27B1]
C2725	CAP_402	m78[27D3]
C2726	CAP_402	m78[27C3]
C2727	CAP_402	m78[27C3]
C2728	CAP_402	m78[27C3]
C2729	CAP_402	m78[27D5]
C2730	CAP_402	m78[27D5]
C2731	CAP_402	m78[27D5]
C2732	CAP_603	m78[27B7]
C2733	CAP_603	m78[27C5]
C2734	CAP_402	m78[27D5]
C2735	CAP_603	m78[27A6]
C2736	CAP_603	m78[27B7]
C2737	CAP_402	m78[27C3]
C2738	CAP_402	m78[27C3]
C2739	CAP_805	m78[27C1]
C2741	CAP_402	m78[27B3]
C2805	CAP_402	m78[28D5]
C2808	CAP_402	m78[28C6]
C2809	CAP_402	m78[28C6]
C2810	CAP_402	m78[28D6]
C2811	CAP_402	m78[28A7]
C2900	CAP_402	m78[29D7]
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C2902	CAP_402	m78[29D6]
C2903	CAP_402	m78[29D6]
C2904	CAP_402	m78[29D5]
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C2906	CAP_402	m78[29D5]
C2907	CAP_603	m78[29C5]
C2908	CAP_402	m78[29C5]
C2909	CAP_402	m78[29D4]
C2910	CAP_603	m78[29D3]
C2911	CAP_402	m78[29D2]
C2912	CAP_402	m78[29D4]
C2913	CAP_402	m78[29D3]
C2914	CAP_603	m78[29D3]
C2915	CAP_402	m78[29C4]
C2916	CAP_603	m78[29C3]
C2989	CAP_402	m78[29C6]
C2990	CAP_402	m78[29C6]
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C3101	CAP_603	m78[31B2]
C3110	CAP_402	m78[31B2]
C3111	CAP_402	m78[31B2]
C3112	CAP_402	m78[31B1]
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C3115	CAP_402	m78[31B2]
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C3121	CAP_402	m78[31B1]
C3122	CAP_402	m78[31A1]
C3123	CAP_402	m78[31A1]
C3130	CAP_603	m78[31D6]
C3131	CAP_402	m78[31D6]
C3140	CAP_603	m78[31A7]
C3141	CAP_402	m78[31A6]
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C3201	CAP_603	m78[32B2]
C3210	CAP_402	m78[32B2]
C3211	CAP_402	m78[32B2]
C3212	CAP_402	m78[32B1]
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C3336	CAP_402	m78[33C4]
C3338	CAP_402	m78[33C4]
C3340	CAP_402	m78[33C4]
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C3370	CAP_402	m78[33A4]
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C3410	CAP_402	m78[34C3]
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C3421	CAP_603	m78[34C3]
C3430	CAP_402	m78[34B7]
C3431	CAP_402	m78[34B7]
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C3710	CAP_603	m78[37D6]
C3711	CAP_402	m78[37D6]
C3712	CAP_402	m78[37D5]
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C3715	CAP_402	m78[37D4]
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C3722	CAP_402	m78[37C5]
C3723	CAP_402	m78[37C4]
C3724	CAP_402	m78[37C4]
C3730	CAP_402	m78[37C7]
C3731	CAP_402	m78[37C7]
C3735	CAP_402	m78[37C5]
C3736	CAP_402	m78[37C5]
C3740	CAP_402	m78[37B7]
C3742	CAP_402	m78[37B6]
C3744	CAP_402	m78[37B6]
C3746	CAP_402	m78[37B5]
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C3751	CAP_402	m78[37B5]
C3780	CAP_402	m78[37B2]
C3800	CAP_805-1	m78[38C8]
C3801	CAP_402	m78[38C7]
C3802	CAP_805-1	m78[38C7]
C3803	CAP_603	m78[38C7]
C3804	CAP_402	m78[38C6]
C3805	CAP_603	m78[38C5]
C3806	CAP_402	m78[38C5]
C3807	CAP_805-1	m78[38C5]
C3810	CAP_805-1	m78[38B6]
C3811	CAP_402	m78[38B6]
C3812	CAP_805-1	m78[38B6]
C3813	CAP_603	m78[38B5]
C3814	CAP_402	m78[38B5]
C3815	CAP_603	m78[38A4]
C3816	CAP_402	m78[38A4]
C3817	CAP_805-1	m78[38A4]
C3890	CAP_402	m78[38C2]
C3891	CAP_402	m78[38C2]
C3900	CAP_402	m78[39D7]
C3901	CAP_402	m78[39D7]
C3902	CAP_402	m78[39D6]
C3903	CAP_402	m78[39D6]
C3910	CAP_1808	m78[39A3]
C4000	CAP_402	m78[40B7]
C4001	CAP_402	m78[40B7]
C4010	CAP_402	m78[40C2]
C4011	CAP_402	m78[40C2]
C4020	CAP_402	m78[40C3]
C4021	CAP_402	m78[40C3]
C4090	CAP_402	m78[40B6]
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C4201	CAP_402-LF	m78[42C7]
C4210	CAP_402	m78[42C6]
C4211	CAP_402	m78[42C5]
C4212	CAP_805-1	m78[42C5]
C4213	CAP_805-1	m78[42C5]
C4230	CAP_402	m78[42A5]
C4231	CAP_402	m78[42A5]
C4240	CAP_402	m78[42A7]
C4241	CAP_402	m78[42A7]
C4242	CAP_402	m78[42A7]
C4250	CAP_402	m78[42B7]
C4251	CAP_402	m78[42B7]
C4252	CAP_402	m78[42B7]
C4253	CAP_402	m78[42B6]
C4254	CAP_402	m78[42B6]
C4260	CAP_402	m78[42B7]
C4261	CAP_402	m78[42B7]
C4262	CAP_402	m78[42B7]
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C4265	CAP_402	m78[42B6]
C4266	CAP_402	m78[42B6]
C4280	CAP_402	m78[42A6]
C4281	CAP_402	m78[42A6]
C4290	CAP_402	m78[42B5]
C4291	CAP_402	m78[42B5]
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C4301	CAP_603-1	m78[43B3]
C4310	CAP_402	m78[43D4]
C4311	CAP_402	m78[43D4]
C4312	CAP_402	m78[43C4]
C4313	CAP_402	m78[43C4]
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C4321	CAP_402	m78[43B5]
C4322	CAP_402	m78[43A5]
C4323	CAP_402	m78[43A5]
C4332	CAP_402	m78[43C2]
C4335	CAP_603-1	m78[43C2]
C4350	CAP_402	m78[43C7]
C4354	CAP_402	m78[43B7]
C4360	CAP_402	m78[43D7]
C4364	CAP_402	m78[43B7]
C4404	CAP_402	m78[44B6]
C4405	CAP_402	m78[44B4]
C4406	CAP_805	m78[44B4]
C4510	CAP_402	m78[45D6]
C4511	CAP_402	m78[45D6]
C4515	CAP_402	m78[45C6]
C4516	CAP_402	m78[45C6]
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C4601	CAP_402	m78[46C8]
C4602	CAP_402	m78[46C7]
C4603	CAP_402	m78[46C7]
C4604	CAP_402	m78[46D8]
C4605	CAP_402	m78[46D7]
C4613	CAP_402	m78[46D2]
C4623	CAP_402	m78[46C5]
C4633	CAP_402	m78[46A5]
C4650	CAP_402	m78[46D5]
C4700	CAP_805-1	m78[47D7]
C4701	CAP_402	m78[47D6]
C4720	CAP_805-1	m78[47D3]
C4721	CAP_402	m78[47D3]
C4902	CAP_805	m78[49D4]
C4903	CAP_402	m78[49D4]
C4904	CAP_402	m78[49D3]
C4905	CAP_402	m78[49D3]
C4906	CAP_402	m78[49D3]
C4907	CAP_402	m78[49D2]
C4920	CAP_402	m78[49C3]
C5000	CAP_402	m78[50D7]
C5001	CAP_402	m78[50D7]
C5010	CAP_402	m78[50C6]
C5020	CAP_402	m78[50C7]
C5021	CAP_402	m78[50C7]
C5050	CAP_402	m78[50B6]
C5051	CAP_402	m78[50A4]
C5052	CAP_603	m78[50A4]
C5065	CAP_402	m78[50B8]
C5066	CAP_603	m78[50B7]
C5067	CAP_402	m78[50B7]
C5309	CAP_402	m78[53D6]
C5358	CAP_402	m78[53C2]
C5359	CAP_402	m78[53D3]
C5370	CAP_402	m78[53C7]
C5500	CAP_402	m78[55C7]
C5501	CAP_402	m78[55B4]
C5502	CAP_805-1	m78[55B4]
C5503	CAP_402	m78[55B4]
C5510	CAP_402	m78[55A7]
C5511	CAP_402	m78[55A6]
C5550	CAP_402	m78[55B7]
C5551	CAP_402	m78[55B6]
C5570	CAP_402	m78[55D3]
C5580	CAP_402	m78[55C4]
C5601	CAP_805	m78[56D5]
C5602	CAP_P_6.3X5.5SM1	m78[56C4]
C5603	CAP_805	m78[56B5]
C5605	CAP_P_6.3X5.5SM1	m78[56B3]
C5660	CAP_402	m78[55C5]
C5701	CAP_805	m78[57C5]
C5702	CAP_P_6.3X5.5SM1	m78[57C3]
C5880	CAP_402	m78[58C5]
C5881	CAP_402	m78[58D5]
C6100	CAP_402	m78[61C4]
C7000	CAP_402	m78[70C6]
C7001	CAP_402	m78[70C6]
C7002	CAP_402	m78[70C6]
C7003	CAP_402	m78[70C6]
C7010	CAP_603	m78[70D6]
C7052	CAP_402	m78[70D2]
C7056	CAP_402	m78[70D1]
C7060	CAP_402	m78[70A5]
C7061	CAP_402	m78[70B5]
C7062	CAP_402	m78[70B5]
C7090	CAP_402	m78[70A3]
C7100	CAP_402	m78[71C4]
C7101	CAP_1206-1	m78[71D1]
C7102	CAP_402	m78[71B4]
C7103	CAP_402	m78[71C2]
C7104	CAP_402	m78[71B2]
C7105	CAP_402	m78[71C8]
C7106	CAP_402	m78[71B8]
C7107	CAP_402	m78[71B7]
C7108	CAP_1206-1	m78[71D1]
C7109	CAP_P_TH	m78[71D5]
C7110	CAP_402	m78[71C7]
C7111	CAP_402	m78[71B2]
C7112	CAP_402	m78[71C2]
C7113	CAP_402	m78[71B7]
C7114	CAP_402	m78[71B8]
C7115	CAP_603	m78[71D4]
C7116	CAP_402	m78[71B4]
C7121	CAP_402	m78[71A5]
C7126	CAP_603-1	m78[71D6]
C7127	CAP_603	m78[71C4]
C7128	CAP_402	m78[71B4]
C7129	CAP_402	m78[71B5]
C7130	CAP_402	m78[71D6]
C7131	CAP_402	m78[71B5]
C7132	CAP_402	m78[71A5]
C7133	CAP_402	m78[71A5]
C7134	CAP_402	m78[71B5]
C7135	CAP_603	m78[71D4]
C7136	CAP_603	m78[71C4]
C7150	CAP_1206-1	m78[71D4]
C7152	CAP_1206-1	m78[71D4]
C7154	CAP_P_TH	m78[71D2]
C7155	CAP_1206-1	m78[71D1]
C7156	CAP_1206-1	m78[71D4]
C7190	CAP_402	m78[71C3]
C7192	CAP_402	m78[71B3]
C7196	CAP_402	m78[71D6]
C7200	CAP_402	m78[72C4]

C7201	CAP_1206-1	m78[72D2]
C7203	CAP_402	m78[72C2]
C7208	CAP_1206-1	m78[72D2]
C7212	CAP_402	m78[72C3]
C7215	CAP_603	m78[72C5]
C7235	CAP_603	m78[72D6]
C7254	CAP_P_TH	m78[72D2]
C7255	CAP_1206-1	m78[72D2]
C7290	CAP_402	m78[72C4]
C7300	CAP_P_CASE-D2-SM	m78[73C8]
C7301	CAP_805	m78[73C8]
C7302	CAP_402	m78[73B7]
C7303	CAP_P_CASE-D2-SM	m78[73C7]
C7304	CAP_805	m78[73C8]
C7310	CAP_603	m78[73C7]
C7324	CAP_402	m78[73B7]
C7330	CAP_603-1	m78[73D6]
C7331	CAP_603	m78[73C6]
C7332	CAP_402	m78[73B5]
C7335	CAP_402	m78[73B6]
C7340	CAP_P_TH	m78[73D7]
C7341	CAP_1206-1	m78[73D7]
C7342	CAP_1206-1	m78[73D6]
C7345	CAP_402	m78[73B3]
C7360	CAP_603	m78[73D2]
C7361	CAP_603	m78[73C2]
C7364	CAP_402	m78[73B2]
C7370	CAP_402	m78[73B2]
C7372	CAP_402	m78[73B4]
C7381	CAP_1206-1	m78[73D2]
C7382	CAP_1206-1	m78[73D2]
C7390	CAP_P_CASE-D2-SM	m78[73C1]
C7391	CAP_P_CASE-D2-SM	m78[73C2]
C7392	CAP_805	m78[73C1]
C7393	CAP_805	m78[73C1]
C7400	CAP_P_CASE-D2-SM	m78[74C8]
C7401	CAP_805	m78[74C8]
C7402	CAP_402	m78[74B7]
C7403	CAP_P_CASE-D2-SM	m78[74C7]
C7404	CAP_805	m78[74C8]
C7410	CAP_603	m78[74C7]
C7424	CAP_402	m78[74B7]
C7430	CAP_603-1	m78[74D6]
C7431	CAP_603	m78[74C6]
C7432	CAP_402	m78[74B5]
C7435	CAP_402	m78[74B6]
C7440	CAP_P_TH	m78[74D7]
C7441	CAP_1206-1	m78[74D7]
C7442	CAP_1206-1	m78[74D6]
C7445	CAP_402	m78[74B3]
C7460	CAP_603-1	m78[74D2]
C7461	CAP_603	m78[74C2]
C7464	CAP_402	m78[74B2]
C7470	CAP_402	m78[74B2]
C7472	CAP_402	m78[74B4]
C7480	CAP_P_TH	m78[74D3]
C7481	CAP_1206-1	m78[74D2]
C7482	CAP_1206-1	m78[74D2]
C7490	CAP_P_TH	m78[74C2]
C7491	CAP_P_TH	m78[74C1]
C7492	CAP_805	m78[74C1]
C7493	CAP_805	m78[74C1]
C7500	CAP_603	m78[75D5]
C7501	CAP_603	m78[75D6]
C7502	CAP_603	m78[75D6]
C7503	CAP_402	m78[75C2]
C7506	CAP_402	m78[75C8]
C7507	CAP_402	m78[75C6]
C7508	CAP_603	m78[75C7]
C7509	CAP_402	m78[75D4]
C7510	CAP_402	m78[75C5]
C7530	CAP_P_TH	m78[75D5]
C7531	CAP_603	m78[75D4]
C7532	CAP_P_TH	m78[75D5]
C7533	CAP_1206-1	m78[75D5]
C7534	CAP_1206-1	m78[75D4]
C7540	CAP_805	m78[75C3]
C7541	CAP_805	m78[75C3]
C7542	CAP_P_CASE-D2-SM	m78[75C2]
C7543	CAP_P_CASE-D2-SM	m78[75C2]
C7544	CAP_P_CASE-D2-SM	m78[75C2]
C7550	CAP_402	m78[75B4]
C7551	CAP_805-1	m78[75A6]
C7552	CAP_805-1	m78[75A4]
C7553	CAP_402	m78[75A6]
C7555	CAP_P_CASE-C3	m78[75A4]
C7559	CAP_603	m78[75B5]
C7560	CAP_402	m78[75D8]
C7564	CAP_402	m78[75C3]
C7585	CAP_402	m78[75A3]
C7586	CAP_402	m78[75A2]
C7587	CAP_402	m78[75A2]
C7588	CAP_402	m78[75A2]
C7589	CAP_402	m78[75A1]
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C7591	CAP_402	m78[75B2]
C7592	CAP_402	m78[75B2]
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C7595	CAP_402	m78[75B3]
C7596	CAP_402	m78[75B2]
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C7599	CAP_402	m78[75B1]
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C7601	CAP_603	m78[76A4]
C7602	CAP_402	m78[76A4]
C7604	CAP_402	m78[76A3]
C7605	CAP_402	m78[76B5]
C7607	CAP_402	m78[76A3]
C7608	CAP_402	m78[76D2]
C7609	CAP_402	m78[76D7]
C7612	CAP_603	m78[76A7]
C7613	CAP_402	m78[76A7]
C7621	CAP_402	m78[76B6]
C7622	CAP_402	m78[76C5]
C7624	CAP_402	m78[76C6]
C7625	CAP_402	m78[76B6]
C7626	CAP_402	m78[76B6]
C7628	CAP_402	m78[76B7]
C7629	CAP_402	m78[76B7]
C7630	CAP_402	m78[76A5]
C7631	CAP_402	m78[76C7]
C7632	CAP_402	m78[76C2]

C7640	CAP_1206-1	m78[76D6]
C7641	CAP_1206-1	m78[76D6]
C7642	CAP_1206-1	m78[76D6]
C7643	CAP_1206-1	m78[76D6]
C7650	CAP_805	m78[76B7]
C7651	CAP_P_CASE-D3L	m78[76B8]
C7652	CAP_P_CASE-D3L	m78[76B8]
C7661	CAP_402	m78[76B3]
C7662	CAP_402	m78[76C4]
C7664	CAP_402	m78[76C3]
C7665	CAP_402	m78[76B4]
C7666	CAP_402	m78[76B3]
C7668	CAP_402	m78[76B2]
C7669	CAP_402	m78[76B2]
C7670	CAP_402	m78[76B4]
C7680	CAP_1206-1	m78[76D3]
C7681	CAP_1206-1	m78[76D4]
C7682	CAP_P_SM-1	m78[76D4]
C7689	CAP_402	m78[76B4]
C7690	CAP_805	m78[76B2]
C7691	CAP_P_CASE-D3L	m78[76B1]
C7692	CAP_P_CASE-D3L	m78[76B1]
C7693	CAP_P_CASE-D3L	m78[76B1]
C7700	CAP_805	m78[77C6]
C7701	CAP_402	m78[77C5]
C7702	CAP_402	m78[77B3]
C7705	CAP_805	m78[77B3]
C7706	CAP_805	m78[77B3]
C7707	CAP_805	m78[77B3]
C7710	CAP_805	m78[77D6]
C7712	CAP_402	m78[77D4]
C7715	CAP_805	m78[77D3]
C7800	CAP_402	m78[78D4]
C7801	CAP_402	m78[78D4]
C7810	CAP_402	m78[78D6]
C7811	CAP_402	m78[78D7]
C7850	CAP_402	m78[78C4]
C7851	CAP_402	m78[78C4]
C7890	CAP_805	m78[78D2]
C7891	CAP_402	m78[78D2]
C7895	CAP_402	m78[78B7]
C7896	CAP_402	m78[78A6]
C7899	CAP_402	m78[78B6]
C8400	CAP_P_SM-LF	m78[84C5]
C8401	CAP_805	m78[84C7]
C8420	CAP_402	m78[84C7]
C8421	CAP_402	m78[84C7]
C8422	CAP_402	m78[84C7]
C8423	CAP_402	m78[84C7]
C8424	CAP_402	m78[84B7]
C8425	CAP_402	m78[84B7]
C8426	CAP_402	m78[84B7]
C8427	CAP_402	m78[84B7]
C8428	CAP_402	m78[84B7]
C8429	CAP_402	m78[84B7]
C8430	CAP_402	m78[84B7]
C8431	CAP_402	m78[84B7]
C8432	CAP_402	m78[84B7]
C8433	CAP_402	m78[84B7]
C8434	CAP_402	m78[84B7]
C8435	CAP_402	m78[84B7]
C8436	CAP_402	m78[84B7]
C8437	CAP_402	m78[84B7]
C8438	CAP_402	m78[84B7]
C8439	CAP_402	m78[84B7]
C8440	CAP_402	m78[84B7]
C8441	CAP_402	m78[84A7]
C8442	CAP_402	m78[84A7]
C8443	CAP_402	m78[84A7]
C8444	CAP_402	m78[84A7]
C8445	CAP_402	m78[84A7]
C8446	CAP_402	m78[84A7]
C8447	CAP_402	m78[84A7]
C8448	CAP_402	m78[84A7]
C8449	CAP_402	m78[84A7]
C8450	CAP_402	m78[84A7]
C8451	CAP_402	m78[84A7]
C8500	CAP_805	m78[85A5]
C8570	CAP_402	m78[85D2]
C9000	CAP_603-1	m78[90C7]
C9001	CAP_402	m78[90C5]
C9010	CAP_402	m78[90A8]
C9020	CAP_1210	m78[90C5]
C9130	CAP_402	m78[91B7]
C9131	CAP_805-1	m78[91B7]
C9140	CAP_402	m78[91A5]
C9141	CAP_402	m78[91B5]
C9142	CAP_402	m78[91B5]
C9143	CAP_402	m78[91A6]
C9144	CAP_402	m78[91B6]
C9145	CAP_402	m78[91B6]
C9160	CAP_402	m78[91B4]
C9161	CAP_402	m78[91B4]
C9162	CAP_402	m78[91A2]
C9163	CAP_402	m78[91A2]
C9410	CAP_603	m78[94C3]
C9411	CAP_402	m78[94D3]
C9413	CAP_402	m78[94C2]
C9414	CAP_402	m78[94C2]
C9900	CAP_805	m78[98C5]
C9901	CAP_402	m78[98C4]
C9902	CAP_402	m78[98C4]
D2185	DIODE_SCHOT_SOT23	m78[21C4]
D2186	DIODE_SCHOT_SOT23	m78[21B4]
D2702	DIODE_SCHOT_6PB_SOT-363	m78[27D8 27D8]
D2800	DIODE_SCHOT_6PB_SOT-363	m78[28D6]
D4390	ZENER_SOT23	m78[43A6]
D4600	DIODE_SCHOT_3P_A_SC-75	m78[46C2]
D4601	DIODE_SCHOT_3P_A_SC-75	m78[46B5]
D4602	DIODE_SCHOT_3P_A_SC-75	m78[46A5]
D5350	DIODE_3P_2NC_SOT23-LF	m78[53C2]
D5600	DIODE_SOT23	m78[56C4]
D5601	DIODE_SOT23	m78[56B4]
D5700	DIODE_SOT23	m78[57C4]
D7100	DIODE_SCHOT_SMB	m78[71D2]
D7101	DIODE_SCHOT_SMB	m78[71B2]
D7200	DIODE_SCHOT_SMB	m78[72C3]
D7300	DIODE_SCHOT_5P_TLM83	m78[73B6]

D7301	DIODE_SCHOT_SOT23	m78[73C6]
D7373	DIODE_SCHOT_5P_TLM83	m78[73B3]
D7374	DIODE_SCHOT_SOT23	m78[73C3]
D7400	DIODE_SCHOT_5P_TLM83	m78[74B6]
D7401	DIODE_SCHOT_SOT23	m78[74C6]
D7473	DIODE_SCHOT_5P_TLM83	m78[74B3]
D7474	DIODE_SCHOT_SOT23	m78[74C4]
D7520	DIODE_SCHOT_5P_TLM83	m78[75C4]
D7600	DIODE_SCHOT_5P_TLM83	m78[76B7]
D7601	DIODE_SCHOT_5P_TLM83	m78[76B2]
D7624	DIODE_SCHOT_SOD-323	m78[76C6]
D7664	DIODE_SCHOT_SOD-323	m78[76C3]
D7810	DIODE_SCHOT_SOD-123	m78[78D7]
D7890	DIODE_SCHOT_SOD-123	m78[78D2]
D9400	ZENER_CASE425	m78[94C1]
D9410	DIODE_SCHOT_SOD-123	m78[94D6]
DE4300	DIODE_SCHOT_SM	m78[43D7]
DP4310	DIODE_DUAL_6P_SOT-363	m78[43D4 43D3]
DP4311	DIODE_DUAL_6P_SOT-363	m78[43C4 43C3]
DP4320	DIODE_DUAL_6P_SOT-363	m78[43B5 43B4]
DP4321	DIODE_DUAL_6P_SOT-363	m78[43A5 43A4]
DS4599	LED_2.0X1.25MM-SM	m78[45C2]
F4300	FUSE_SM	m78[43D6]
F4310	FUSE_SM	m78[43D6]
F9410	FUSE_805	m78[94D5]
FL4300	FILTER_4P_L701-SM	m78[43B3]
FL4310	FILTER_4P_L701-SM	m78[43B3]
J600	CON_M12RT_D_THB_M-RT-TH	m78[6D7]
J1000	MEROM_BGA-SKT-P	m78[10C3 10D7]
J1000	MEROM_BGA-SKT-P	m78[11D3 11D7]
J1300	CON_F60ST_D_SM1_F-SM	m78[13C4]
J2800	BATTERY_2P_SM	m78[28D8]
J3100	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM	m78[31D5]
J3200	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM	m78[32D5]
J3400	CON_F52RT_D2MT_SM_F-RT-SM	m78[34C5]
J3900	CON_RJ45_8ANG_D3MT_TH_F-ANG-TH	m78[39C3]
J4300	CON_F9ANG_1394B_D6MT_TH_F-ANG-TH1	m78[43C2]
J4301	CON_F6ANG_S3MT_1394A_TH_F-ANG-TH	m78[43B2]
J4401	CON_M50ST_D2MT_SM1_M-ST-SM	m78[44C4]
J4510	CON_M7ST_SATA_SM_M-S-T-SM	m78[45D7]
J4610	CON_F4ANG_S4MT_USB_T-H_F-ANG-TH	m78[46D1]
J4620	CON_F4ANG_S4MT_USB_T-H_F-ANG-TH	m78[46B4]
J4630	CON_F4ANG_S4MT_USB_T-H_F-ANG-TH	m78[46A4]
J4700	CON_M5ST_S2MT_SM_M-S-T-SM	m78[47B5]
J4720	CON_F10ST_D_SMA_F-ST-SM	m78[47D2]
J5010	CON_M2ST_S2MT_SM_M-S-T-SM	m78[50C6]
J5050	CON_M2ST_S2MT_SM_M-S-T-SM	m78[50A3]
J5100	CON_F30STSM_5047_SM1	m78[51B5]
J5500	CON_M5ST_S2MT_SM_PN1-VD_M-ST-SM	m78[55D7]
J5510	CON_M2ST_S2MT_SM_M-S-T-SM	m78[55A7]
J5511	CON_M2RT_S2MT_SM_M-R-T-SM	m78[55A5]
J5550	CON_M3RT_S2MT_SM_M-R-T-SM	m78[55B7]
J5551	CON_2RTSM_125_SM-2MT-BLK-LF	m78[55B6]
J5560	CON_M5ST_S2MT_SM_PN1-VD_M-ST-SM	m78[55D6]
J5600	CON_M4RT_S2MT_SM_M-R-T-SM	m78[56D3]
J5601	CON_M4RT_S2MT_SM_M-R-T-SM	m78[56B2]
J5700	CON_4SM_WRIB_85205-0401-BLK-ST-SM	m78[57C2]
J5880	CON_M7ST_S2MT_SM_M-S-T-SM	m78[58C6]
J8400	CON_F232RT_MXM_SM1_F-RT-SM	m78[84C5]
J8400	CON_F232RT_MXM_SM1_F-RT-SM	m78[85C6]
J9002	CON_F30ST_D_SM_F-ST-SM	m78[90B7]
J9410	CON_DVI_F32ST_Q2MT_S-M_F-ST-SM	m78[94D5]
J9800	CON_F20RT_S2MT_SM1_F-RT-SM	m78[98C5]
L2150	IND_0603	m78[21A7]
L2173	IND_1210	m78[21D4]
L2181	IND_0603	m78[21D2]
L2183	IND_0603	m78[21C2]
L2190	IND_0805	m78[21B3]
L2195	IND_0805	m78[21A3]
L2700	IND_0805-1	m78[27C8]
L2702	IND_0805	m78[27A7]
L2703	IND_1210	m78[27A7]
L2901	IND_0402	m78[29D7]
L2902	IND_0402	m78[29D3]
L2903	IND_0402	m78[29C7]
L3800	IND_0805-1	m78[38D7]
L3810	IND_0805-1	m78[38B6]
L3900	IND_0805	m78[39D7]
L4200	IND_0402-LF	m78[42D5]
L4210	IND_0402-LF	m78[42B2]
L4211	IND_0402-LF	m78[42B2]

L4300	IND_SM	m78[43D3]
L4301	IND_SM	m78[43B4]
L4610	IND_SM	m78[46D3]
L4612	FILTER_4P_L701-SM	m78[46D3]
L4620	IND_SM	m78[46C6]
L4622	FILTER_4P_L701-SM	m78[46B6]
L4630	IND_SM	m78[46B6]
L4632	FILTER_4P_L701-SM	m78[46A6]
L4700	IND_SM	m78[47D6]
L4701	FILTER_4P_L701-SM	m78[47B6]
L4710	FILTER_4P_L701-SM	m78[47A6]
L5050	IND_3.8X3.8X1.5MM	m78[50A4]
L7100	IND_HM56-11120-TH	m78[71D2]
L7101	IND_HM56-11120-TH	m78[71B2]
L7200	IND_HM56-11120-TH	m78[72C3]
L7300	IND_MMD06EZ-SM	m78[73C7]
L7360	IND_MMD06EZ-SM	m78[73C2]
L7400	IND_MMD06EZ-SM	m78[74C7]
L7460	IND_IHLP5050-MMD12CE-SM	m78[74C2]
L7580	IND_IHLP5050-MMD12CE-SM	m78[75C3]
L7620	IND_MMD06EZ-SM	m78[76B7]
L7680	IND_HM56-11123-TH	m78[76B2]
L7700	IND_SM-MSS5131	m78[77B4]
L7710	IND_IHLP	m78[77D4]
L9000	IND_SM	m78[90C6]
L9140	IND_0402	m78[91A5]
L9141	IND_0402	m78[91B5]
L9142	IND_0402	m78[91B5]
L9160	IND_0402	m78[91B2]
L9161	IND_0402	m78[91A2]
L9400	FILTER_4P_SM	m78[94D7]
L9401	FILTER_4P_SM	m78[94D7]
L9402	FILTER_4P_SM	m78[94C7]
L9403	FILTER_4P_SM	m78[94B7]
L9410	IND_SM-1	m78[94D4]
LED601	LED_2.0X1.25MM-SM	m78[6A8]
LED602	LED_2.0X1.25MM-SM	m78[6A7]
LED603	LED_2.0X1.25MM-SM	m78[6A6]
LED604	LED_2.0X1.25MM-SM	m78[6B7]
LED3900	LED_2.0X1.25MM-SM	m78[39A7]
LED3901	LED_2.0X1.25MM-SM	m78[39A7]
LED3902	LED_2.0X1.25MM-SM	m78[39A7]
LED3903	LED_2.0X1.25MM-SM	m78[39A6]
LED4400	LED_2.0X1.25MM-SM	m78[44B5]
PP1000	PROBEPOINT_SM	m78[7D7]
PP1001	PROBEPOINT_SM	m78[7D7]
PP1002	PROBEPOINT_SM	m78[7D7]
PP1003	PROBEPOINT_SM	m78[7D7]
PP1004	PROBEPOINT_SM	m78[7D7]
PP1005	PROBEPOINT_SM	m78[7D7]
PP1006	PROBEPOINT_SM	m78[7D7]
PP1007	PROBEPOINT_SM	m78[7D7]
PP1008	PROBEPOINT_SM	m78[7D7]
PP1009	PROBEPOINT_SM	m78[7D7]
PP1010	PROBEPOINT_SM	m78[7D7]
PP1011	PROBEPOINT_SM	m78[7D7]
PP1012	PROBEPOINT_SM	m78[7D7]
PP1013	PROBEPOINT_SM	m78[7D7]
PP1014	PROBEPOINT_SM	m78[7D7]
PP1015	PROBEPOINT_SM	m78[7D7]
PP1016	PROBEPOINT_SM	m78[7D7]
PP1017	PROBEPOINT_SM	m78[7D7]
PP1018	PROBEPOINT_SM	m78[7D7]
PP1019	PROBEPOINT_SM	m78[7D7]
PP1020	PROBEPOINT_SM	m78[7D7]
PP1021	PROBEPOINT_SM	m78[7C7]
PP1022	PROBEPOINT_SM	m78[7C7]
PP1023	PROBEPOINT_SM	m78[7C7]
PP1024	PROBEPOINT_SM	m78[7C7]
PP1025	PROBEPOINT_SM	m78[7C7]
PP1026	PROBEPOINT_SM	m78[7C7]
PP1027	PROBEPOINT_SM	m78[7C7]
PP1028	PROBEPOINT_SM	m78[7C7]
PP1029	PROBEPOINT_SM	m78[7C7]
PP1030	PROBEPOINT_SM	m78[7C7]
PP1031	PROBEPOINT_SM	m78[7C7]
PP1032	PROBEPOINT_SM	m78[7C7]
PP1033	PROBEPOINT_SM	m78[7C7]
PP1034	PROBEPOINT_SM	m78[7C7]
PP1035	PROBEPOINT_SM	m78[7C7]
PP1400	PROBEPOINT_SM	m78[7D6]
PP1401	PROBEPOINT_SM	m78[7D6]
PP1402	PROBEPOINT_SM	m78[7D6]
PP1403	PROBEPOINT_SM	m78[7D6]
PP1404	PROBEPOINT_SM	m78[7D6]
PP1405	PROBEPOINT_SM	m78[7D6]
PP1406	PROBEPOINT_SM	m78[7D6]
PP1407	PROBEPOINT_SM	m78[7D6]
PP1408	PROBEPOINT_SM	m78[7D6]
PP1409	PROBEPOINT_SM	m78[7D6]
PP1410	PROBEPOINT_SM	m78[7D6]
PP1411	PROBEPOINT_SM	m78[7D6]
PP1412	PROBEPOINT_SM	m78[7D6]
PP1413	PROBEPOINT_SM	m78[7D6]
PP1414	PROBEPOINT_SM	m78[7D6]
PP1415	PROBEPOINT_SM	m78[7D6]
PP1416	PROBEPOINT_SM	m78[7D6]
PP1417	PROBEPOINT_SM	m78[7D6]
PP1418	PROBEPOINT_SM	m78[7D6]
PP1419	PROBEPOINT_SM	m78[7D6]
PP1420	PROBEPOINT_SM	m78[7D6]
PP1421	PROBEPOINT_SM	m78[7C6]
PP1422	PROBEPOINT_SM	m78[7C6]
PP1423	PROBEPOINT_SM	m78[7C6]
PP1424	PROBEPOINT_SM	m78[7C6]
PP1425	PROBEPOINT_SM	m78[7C6]
PP1426	PROBEPOINT_SM	m78[7C6]
PP1427	PROBEPOINT_SM	m78[7C6]
PP1428	PROBEPOINT_SM	m78[7C6]
PP1429	PROBEPOINT_SM	m78[7C6]
PP1430	PROBEPOINT_SM	m78[7C6]
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PP1433	PROBEPOINT_SM	m78[7C6]
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PP1435	PROBEPOINT_SM	m78[7C6]
PP1436	PROBEPOINT_SM	m78[7C6]
PP1437	PROBEPOINT_SM	m78[7C6]
PP1438	PROBEPOINT_SM	m78[7C6]
PP1439	PROBEPOINT_SM	m78[7C6]
PP1440	PROBEPOINT_SM	m78[7C6]
PP1441	PROBEPOINT_SM	m78[7C6]

PP1442	PROBEPOINT_SM	m78[7C6]
PP1443	PROBEPOINT_SM	m78[7C6]
PP1444	PROBEPOINT_SM	m78[7B6]
PP1445	PROBEPOINT_SM	m78[7B6]
PP1446	PROBEPOINT_SM	m78[7B6]
PP1447	PROBEPOINT_SM	m78[7B6]
PP1448	PROBEPOINT_SM	m78[7B6]
PP1449	PROBEPOINT_SM	m78[7B6]
PP1450	PROBEPOINT_SM	m78[7B6]
PP1451	PROBEPOINT_SM	m78[7B6]
PP1452	PROBEPOINT_SM	m78[7B6]
PP1453	PROBEPOINT_SM	m78[7B6]
PP1454	PROBEPOINT_SM	m78[7B6]
PP1455	PROBEPOINT_SM	m78[7B6]
PP1456	PROBEPOINT_SM	m78[7B6]
PP1457	PROBEPOINT_SM	m78[7B6]
PP1458	PROBEPOINT_SM	m78[7B6]
PP1459	PROBEPOINT_SM	m78[7B6]
PP1460	PROBEPOINT_SM	m78[7B6]
PP1461	PROBEPOINT_SM	m78[7B6]
PP1462	PROBEPOINT_SM	m78[7B6]
PP1463	PROBEPOINT_SM	m78[7B6]
PP1464	PROBEPOINT_SM	m78[7B6]
PP1465	PROBEPOINT_SM	m78[7B6]
PP1466	PROBEPOINT_SM	m78[7B6]
PP1467	PROBEPOINT_SM	m78[7B6]
PP1468	PROBEPOINT_SM	m78[7B6]
PP1469	PROBEPOINT_SM	m78[7B6]
PP1470	PROBEPOINT_SM	m78[7A6]
PP1471	PROBEPOINT_SM	m78[7A6]
PP1472	PROBEPOINT_SM	m78[7A6]
PP1473	PROBEPOINT_SM	m78[7A6]
PP1474	PROBEPOINT_SM	m78[7A6]
PP1475	PROBEPOINT_SM	m78[7A6]
PP1476	PROBEPOINT_SM	m78[7A6]
PP1477	PROBEPOINT_SM	m78[7A6]
PP1478	PROBEPOINT_SM	m78[7A6]
PP1479	PROBEPOINT_SM	m78[7A6]
PP1480	PROBEPOINT_SM	m78[7A6]
PP1481	PROBEPOINT_SM	m78[7A6]
PP1482	PROBEPOINT_SM	m78[7A6]
PP1483	PROBEPOINT_SM	m78[7A6]
PP1484	PROBEPOINT_SM	m78[7A6]
PP1485	PROBEPOINT_SM	m78[7A6]
PP1486	PROBEPOINT_SM	m78[7A6]
PP1487	PROBEPOINT_SM	m78[7A6]
PP1488	PROBEPOINT_SM	m78[7A6]
PP1489	PROBEPOINT_SM	m78[7A6]
PP1490	PROBEPOINT_SM	m78[7A6]
PP1491	PROBEPOINT_SM	m78[7A6]
PP1492	PROBEPOINT_SM	m78[7A6]
PP1493	PROBEPOINT_SM	m78[7A6]
PP2100	PROBEPOINT_SM	m78[7C7]
PP2101	PROBEPOINT_SM	m78[7C7]
PP2102	PROBEPOINT_SM	m78[7C7]
PP2103	PROBEPOINT_SM	m78[7B7]
PP2104	PROBEPOINT_SM	m78[7B7]
PP2105	PROBEPOINT_SM	m78[7B7]
PP2106	PROBEPOINT_SM	m78[7B7]
PP2107	PROBEPOINT_SM	m78[7B7]
PP2108	PROBEPOINT_SM	m78[7B7]
PP2109	PROBEPOINT_SM	m78[7B7]
PP2110	PROBEPOINT_SM	m78[7B7]
PP2111	PROBEPOINT_SM	m78[7B7]
PP2112	PROBEPOINT_SM	m78[7B7]
PP2113	PROBEPOINT_SM	m78[7B7]
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PP2115	PROBEPOINT_SM	m78[7B7]
PP2116	PROBEPOINT_SM	m78[7B7]
PP2117	PROBEPOINT_SM	m78[7B7]
PP2118	PROBEPOINT_SM	m78[7B7]
PP2119	PROBEPOINT_SM	m78[7B7]
PP2120	PROBEPOINT_SM	m78[7B7]
PP2121	PROBEPOINT_SM	m78[7A7]
PP2122	PROBEPOINT_SM	m78[7A7]
PP2123	PROBEPOINT_SM	m78[7A7]
PP2124	PROBEPOINT_SM	m78[7A7]
PP2125	PROBEPOINT_SM	m78[7A7]
PP2126	PROBEPOINT_SM	m78[7A7]
PP2127	PROBEPOINT_SM	m78[7A7]
PP2128	PROBEPOINT_SM	m78[7A7]
PP2129	PROBEPOINT_SM	m78[7A7]
PP2130	PROBEPOINT_SM	m78[7A7]
PP2131	PROBEPOINT_SM	m78[7A7]
PP2132	PROBEPOINT_SM	m78[7B7]
PP2133	PROBEPOINT_SM	m78[7B7]
PP3700	PROBEPOINT_SM	m78[7D5]
PP3701	PROBEPOINT_SM	m78[7D5]
PP3702	PROBEPOINT_SM	m78[7D5]
PP3703	PROBEPOINT_SM	m78[7D5]
PP3704	PROBEPOINT_SM	m78[7D5]
PP4000	PROBEPOINT_SM	m78[7D5]
PP4001	PROBEPOINT_SM	m78[7D5]
PP4002	PROBEPOINT_SM	m78[7D5]
PP4003	PROBEPOINT_SM	m78[7D5]
PP4004	PROBEPOINT_SM	m78[7D5]
PP4900	PROBEPOINT_SM	m78[7C5]
PP4901	PROBEPOINT_SM	m78[7C5]
PP4902	PROBEPOINT_SM	m78[7C5]
PP4903	PROBEPOINT_SM	m78[7C5]
Q600	TRA_2N7002_SOT23-LF	m78[6A8]
Q610	TRA_2N7002_SOT23-LF	m78[6D7]
Q3800	TRA_PBSS5540Z_SOT223	m78[38C5]
Q3810	TRA_PBSS5540Z_SOT223	m78[38A4]
Q4200	TRA_BCP69_SOT223-4	m78[42D6]
Q4600	TRA_2N7002_SOT23-LF	m78[46C8]
Q5050	TRA_DUAL_MMDT3906_SOT-363	m78[50A6 50A7]
Q5052	TRA_2N7002_SOT23-LF	m78[50A8]
Q5077	TRA_DUAL_MMDT3904_SOT-363-LF	m78[50D1 50D2]
Q5095	TRA_2N7002DW_SOT-363	m78[50C2 50C2]
Q5190	TRA_DUAL_MMDT3904_SOT-363-LF	m78[51B3 51C4]
Q5339	TRA_2N7002_SOT23-LF	m78[53B7]
Q5341	TRA_FDC796N_SUPERSOT-6	m78[53B6]
Q5600	TRA_NTHS5443T1_1206A-03-LF	m78[56D4]
Q5602	TRA_2N7002_SOT23-LF	m78[56D6]
Q5603	TRA_NTHS5443T1_1206A-03-LF	m78[56B4]
Q5605	TRA_2N7002_SOT23-LF	m78[56B6]
Q5700	TRA_NTHS5443T1_1206A	m78[57D4]
Q5702	TRA_2N7002_SOT23-LF	m78[57C5]
Q7006	TRA_DUAL_SSM6N15FE_SOT563	m78[70A7 70B6]
Q7007	TRA_DUAL_SSM6N15FE_SOT563	m78[70A6 70B6]
Q7100	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m78[71D3]
Q7101	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[71D3]
Q7102	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m78[71C3]
Q7103	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[71B3]
Q7104	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[71C3]
Q7105	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[71B3]
Q7200	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m78[72C4]
Q7201	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[72C4]
Q7204	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[72C3]
Q7300	TRA_FDMS9620S_MLP	m78[73C6]
Q7360	TRA_FDMS9620S_MLP	m78[73C3]
Q7400	TRA_FDMS9620S_MLP	m78[74C6]
Q7460	TRA_FDM6296_MICROFET 3X3	m78[74C3]
Q7461	TRA_FDM6296_MICROFET 3X3	m78[74C3]
Q7520	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m78[75D4]
Q7521	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[75C4]
Q7603	TRA_2N7002_SOT23-LF	m78[76A6]
Q7620	TRA_FDMS9620S_MLP	m78[76C7]
Q7640	TRA_SINGLE_MOSFET_PC HN_SOT-23	m78[53B7]
Q7660	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK	m78[76C3]
Q7661	TRA_MOSFET_NCHN_5P1_MLP5X6-LFPAK-DFN	m78[76B3]
Q7800	TRA_IRF7410_SO-8	m78[78D4]
Q7801	TRA_SINGLE_MOSFET_NC HN_SOT23	m78[78D5]
Q7810	TRA_IRF7410_SO-8	m78[78D7]
Q7811	TRA_SINGLE_MOSFET_NC HN_SOT23	m78[78D8]
Q7850	TRA_IRF7410_SO-8	m78[78C4]
Q7851	TRA_SINGLE_MOSFET_NC HN_SOT23	m78[78C5]
Q7890	TRA_MOSFET_PCHN_8P1_SOI	m78[78D2]
Q7891	TRA_SINGLE_MOSFET_NC HN_SOT23	m78[78C2]
Q7892	TRA_2N7002DW_SOT-363	m78[78C2 78C1]
Q7895	TRA_MOSFET_NCHN_8P_S O-8	m78[78B6]
Q7896	TRA_2N7002_SOT23-LF	m78[78A7]
Q7897	TRA_SINGLE_MOSFET_NC HN_SOT23	m78[78A6]
Q9000	TRA_SI3443DV_TSOP-LF	m78[90C7]
Q9001	TRA_2N7002_SOT23-LF	m78[90B7]
Q9411	TRA_2N7002DW_SOT-363	m78[94D2 94C2]
R600	RES_402	m78[6A7]
R602	RES_402	m78[6A8]
R604	RES_402	m78[6B7]
R605	RES_603	m78[6A6]
R610	RES_402	m78[6D6]
R1002	RES_402	m78[10D5]
R1003	RES_402	m78[10C5]
R1004	RES_402	m78[10C5]
R1005	RES_402	m78[10B5]
R1006	RES_402	m78[10B5]
R1007	RES_402	m78[10A4]
R1012	RES_402	m78[10A4]
R1016	RES_402	m78[10B1]
R1017	RES_402	m78[10B1]
R1018	RES_402	m78[10B1]
R1019	RES_402	m78[10B1]
R1020	RES_402	m78[10B7]
R1021	RES_402	m78[10B7]
R1022	RES_402	m78[10A7]
R1023	RES_402	m78[10A7]
R1024	RES_402	m78[10A7]
R1030	RES_402	m78[10A4]
R1100	RES_402	m78[11B5]
R1101	RES_402	m78[11A5]
R1290	RES_402	m78[12C2]
R1291	RES_402	m78[12C2]
R1292	RES_402	m78[12C2]
R1293	RES_402	m78[12C2]
R1294	RES_402	m78[12C2]
R1295	RES_402	m78[12C2]
R1296	RES_402	m78[12C2]
R1303	RES_402	m78[13B2]
R1315	RES_402	m78[13C6]
R1330	RES_402	m78[13C5]
R1331	RES_402	m78[13C5]
R1399	RES_402	m78[13C7]
R1410	RES_402	m78[14B6]
R1411	RES_402	m78[14A6]
R1415	RES_402	m78[14A6]
R1420	RES_402	m78[14B6]
R1421	RES_402	m78[14B6]
R1425	RES_402	m78[14A7]
R1426	RES_402	m78[14A7]
R1510	RES_402	m78[15D3]
R1610	RES_402	m78[16C2]
R1611	RES_402	m78[16C2]
R1620	RES_402	m78[16C1]
R1622	RES_402	m78[16C1]
R1624	RES_402	m78[16C1]
R1630	RES_402	m78[16B7]
R1631	RES_402	m78[16B7]
R1640	RES_402	m78[16A3]
R1641	RES_402	m78[16A3]
R1655	RES_402	m78[16D7]
R1659	RES_402	m78[16D7]
R1666	RES_402	m78[16C7]
R1669	RES_402	m78[16C7]
R1670	RES_402	m78[16C7]
R1690	RES_402	m78[16A3]
R1691	RES_402	m78[16A3]
R2141	RES_603	m78[21B7]
R2145	RES_603	m78[21B7]
R2159	RES_603	m78[21A7]
R2170	RES_603	m78[21D4]
R2183	RES_402	m78[21C2]
R2185	RES_402	m78[21C3]
R2186	RES_402	m78[21B3]
R2190	RES_402	m78[21B3]
R2195	RES_402	m78[21A3]
R2200	RES_402	m78[22B2]
R2201	RES_402	m78[22A2]
R2202	RES_402	m78[22B2]
R2203	RES_402	m78[22A2]
R2300	RES_402	m78[23D7]
R2301	RES_402	m78[23D7]
R2302	RES_402	m78[23D6]
R2303	RES_402	m78[23D3]
R2304	RES_402	m78[23C3]
R2305	RES_402	m78[23C3]
R2306	RES_402	m78[23D3]
R2308	RES_402	m78[23C3]
R2309	RES_402	m78[23C3]
R2310	RES_402	m78[23D6]
R2311	RES_402	m78[23D6]
R2313	RES_402	m78[23C7]
R2314	RES_402	m78[23C7]
R2315	RES_402	m78[23C7]
R2316	RES_402	m78[23B7]
R2400	RES_402	m78[24C7]
R2401	RES_402	m78[24C7]
R2402	RES_402	m78[24C7]
R2403	RES_402	m78[24C7]
R2404	RES_402	m78[24C7]
R2405	RES_402	m78[24C6]
R2406	RES_402	m78[24B6]
R2407	RES_402	m78[24C6]
R2408	RES_402	m78[24C6]
R2409	RES_402	m78[24C6]
R2413	RES_402	m78[24C3]
R2414	RES_402	m78[24B3]
R2415	RES_402	m78[24B5]
R2423	RES_402	m78[24A3]
R2424	RES_402	m78[24A3]
R2425	RES_402	m78[24A3]
R2426	RES_402	m78[24A3]
R2427	RES_402	m78[24A3]
R2428	RES_402	m78[24A3]
R2429	RES_402	m78[24A3]
R2430	RES_402	m78[24A3]
R2431	RES_402	m78[24A3]
R2432	RES_402	m78[24A3]
R2433	RES_402	m78[24A3]
R2436	RES_402	m78[24A3]
R2437	RES_402	m78[24A3]
R2438	RES_402	m78[24A3]
R2439	RES_402	m78[24A3]
R2440	RES_402	m78[24A3]
R2441	RES_402	m78[24A3]
R2442	RES_402	m78[24A3]
R2500	RES_402	m78[25D7]
R2502	RES_402	m78[25D7]
R2504	RES_402	m78[25D6]
R2505	RES_402	m78[25D6]
R2506	RES_402	m78[25D6]
R2507	RES_402	m78[25D6]
R2510	RES_402	m78[25D6]
R2511	RES_402	m78[25A8]
R2512	RES_402	m78[25A8]
R2514	RES_402	m78[25A7]
R2515	RES_402	m78[25A7]
R2516	RES_402	m78[25A7]
R2523	RES_402	m78[25B3]
R2524	RES_402	m78[25C2]
R2525	RES_402	m78[25C2]
R2526	RES_402	m78[25C2]
R2527	RES_402	m78[25B2]
R2528	RES_402	m78[25B2]
R2529	RES_402	m78[25B2]
R2530	RES_402	m78[25B4]
R2531	RES_402	m78[25B4]
R2532	RES_402	m78[25D3]
R2533	RES_402	m78[25D2]
R2534	RES_402	m78[25D2]
R2535	RES_402	m78[25D3]
R2536	RES_402	m78[25A4]
R2544	RES_402	m78[25A4]
R2545	RES_402	m78[25A4]
R2546	RES_402	m78[25A4]
R2547	RES_402	m78[25D6]
R2550	RES_402	m78[25D7]
R2551	RES_402	m78[25D7]
R2552	RES_402	m78[25D7]
R2553	RES_402	m78[25D7]
R2596	RES_402	m78[25A4]
R2597	RES_402	m78[25A4]
R2598	RES_402	m78[25A4]
R2700	RES_603	m78[27A8]
R2701	RES_402	m78[27D8]
R2702	RES_402	m78[27D8]
R2710	RES_402	m78[28B2]
R2735	RES_402	m78[27A8]
R2800	RES_402	m78[28D5]
R2803	RES_402	m78[28A6]
R2806	RES_402	m78[28D6]
R2807	RES_402	m78[28D7]
R2809	RES_402	m78[28C7]
R2810	RES_402	m78[28C7]
R2850	RES_402	m78[28B1]
R2881	RES_402	m78[28D2]
R2883	RES_402	m78[28D2]
R2885	RES_402	m78[28D2]
R2890	RES_402	m78[28C2]
R2891	RES_402	m78[28D2]
R2892	RES_402	m78[28C2]
R2893	RES_402	m78[28C2]
R2896	RES_402	m78[28A4]
R2897	RES_402	m78[28A4]
R2900	RES_402	m78[29C6]
R2901	RES_402	m78[29D3]
R2902	RES_402	m78[29C3]
R2903	RES_402	m78[29B6]
R3026	RES_402	m78[30A4]
R3027	RES_402	m78[30A4]
R3030	RES_402	m78[30A4]
R3032	RES_402	m78[30C7]
R3033	RES_402	m78[30C7]
R3034	RES_402	m78[30A7]
R3035	RES_402	m78[30A7]
R3046	RES_402	m78[30C1]
R3047	RES_402	m78[30C1]
R3050	RES_402	m78[30D1]
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R3052	RES_402	m78[30D1]
R3053	RES_402	m78[30C1]
R3054	RES_402	m78[30C1]
R3055	RES_402	m78[30C1]
R3067	RES_402	m78[30D7]
R3080	RES_402	m78[30C7]
R3081	RES_402	m78[30C7]
R3082	RES_402	m78[30C7]
R3083	RES_402	m78[30C7]
R3084	RES_402	m78[30B7]
R3085	RES_402	m78[30B7]
R3086	RES_402	m78[30B7]
R3087	RES_402	m78[30B7]
R3088	RES_402	m78[30B7]
R3089	RES_402	m78[30B7]
R3090	RES_402	m78[30B7]
R3091	RES_402	m78[30B7]
R3098	RES_402	m78[30B4]
R3100	RES_402	m78[31D2]
R3101	RES_402	m78[31C2]
R3140	RES_402	m78[31A3]
R3141	RES_402	m78[31A3]
R3200	RES_402	m78[32C2]
R3201	RES_402	m78[32C2]
R3240	RES_402	m78[32A3]
R3241	RES_402	m78[32A3]
R3300	RES_402	m78[33D5]
R3301	RES_402	m78[33D5]
R3302	RES_402	m78[33D5]
R3303	RES_402	m78[33D5]
R3304	RES_402	m78[33C5]
R3305	RES_402	m78[33C5]
R3400	RES_402	m78[34C7]
R3401	RES_402	m78[34C7]
R3410	RES_402	m78[34A5]
R3720	RES_402	m78[37C6]
R3740	RES_402	m78[37B7]
R3741	RES_402	m78[37B7]
R3742	RES_402	m78[37B6]
R3743	RES_402	m78[37B6]
R3744	RES_402	m78[37B6]
R3745	RES_402	m78[37B5]
R3746	RES_402	m78[37B5]
R3747	RES_402	m78[37B5]
R3760	RES_402	m78[37C2]
R3765	RES_402	m78[37B2]
R3780	RES_402	m78[37B2]
R3781	RES_402	m78[37B2]
R3801	RES_402	m78[38C6]
R3811	RES_402	m78[38A5]
R3820	RES_603	m78[38B8]
R3821	RES_603	m78[38B8]
R3880	RES_402	m78[38D3]
R3890	RES_603	m78[38C2]
R3901	RES_603	m78[39A7]
R3902	RES_603	m78[39A7]
R3903	RES_603	m78[39A7]
R3904	RES_603	m78[39A6]
R3910	RES_402	m78[39A4]
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R3912	RES_402	m78[39A4]
R3913	RES_402	m78[39A4]
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R4002	RES_402	m78[40C7]
R4010	RES_402	m78[46C2]
R4011	RES_402	m78[40B2]
R4012	RES_402	m78[40B2]
R4013	RES_402	m78[40C2]
R4080	RES_402	m78[40B8]
R4090	RES_402	m78[40B6]
R4200	RES_402	m78[42C7]
R4250	RES_402	m78[42D3]
R4251	RES_402	m78[42D2]
R4252	RES_402	m78[42D2]
R4260	RES_402	m78[42C3]
R4261	RES_402	m78[42C2]
R4262	RES_402	m78[42C2]
R4300	RES_2512	m78[43D7]
R4301	RES_2512	m78[43D7]
R4302	RES_805	m78[43D7]
R4335	RES_402	m78[43B2]
R4350	RES_402	m78[43C7]
R4351	RES_402	m78[43C7]
R4352	RES_402	m78[43B7]
R4353	RES_402	m78[43B7]
R4354	RES_402	m78[43B7]
R4360	RES_402	m78[43C7]
R4361	RES_402	m78[43C7]
R4362	RES_402	m78[43B7]
R4363	RES_402	m78[43B7]
R4364	RES_402	m78[43B7]
R4390	RES_402	m78[43A7]
R4403	RES_402	m78[44C5]
R4451	RES_402	m78[44C5]
R4453	RES_402	m78[44C4]
R4457	RES_402	m78[44B6]
R4458	RES_402	m78[44B5]
R4459	RES_402	m78[44B5]
R4590	RES_402	m78[45B1]
R4599	RES_603	m78[45C2]
R4600	RES_402	m78[46D8]
R4650	RES_402	m78[46D4]
R4651	RES_402	m78[46C4]
R4652	RES_402	m78[46C4]
R4701	RES_402	m78[47B6]
R4702	RES_402	m78[47B6]
R4710	RES_402	m78[47A6]
R4711	RES_402	m78[47A6]
R4720	RES_402	m78[47C2]
R4721	RES_402	m78[47C2]
R4901	RES_402	m78[49C1]
R4902	RES_402	m78[49C2]
R4903	RES_402	m78[49C1]
R4909	RES_402	m78[49C1]

R4950	RES_402	m78[49C4]
R4951	RES_402	m78[49C4]
R4998	RES_402	m78[49C2]
R4999	RES_402	m78[49D4]
R5000	RES_402	m78[50D6]
R5010	RES_402	m78[50C6]
R5032	RES_402	m78[50B1]
R5033	RES_402	m78[50B1]
R5034	RES_402	m78[50B1]
R5035	RES_402	m78[50B1]
R5036	RES_402	m78[50B1]
R5037	RES_402	m78[50B1]
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R5039	RES_402	m78[50B1]
R5040	RES_402	m78[50B1]
R5041	RES_402	m78[50B1]
R5042	RES_402	m78[50B1]
R5043	RES_402	m78[50B1]
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R5047	RES_402	m78[50B1]
R5048	RES_402	m78[50A1]
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R5056	RES_402	m78[50A3]
R5057	RES_402	m78[50A6]
R5058	RES_402	m78[50A5]
R5059	RES_402	m78[50A4]
R5070	RES_402	m78[50D2]
R5071	RES_402	m78[50D3]
R5078	RES_402	m78[50D1]
R5080	RES_402	m78[50B1]
R5082	RES_402	m78[50B1]
R5083	RES_402	m78[50A1]
R5084	RES_402	m78[50A1]
R5086	RES_402	m78[50A1]
R5087	RES_402	m78[50B1]
R5088	RES_402	m78[50A1]
R5090	RES_402	m78[50B1]
R5091	RES_402	m78[50B1]
R5092	RES_402	m78[50B1]
R5093	RES_402	m78[50B1]
R5094	RES_402	m78[50B1]
R5096	RES_402	m78[50B1]
R5190	RES_402	m78[51B2]
R5191	RES_402	m78[51C3]
R5192	RES_402	m78[51C4]
R5200	RES_402	m78[52D7]
R5201	RES_402	m78[52D7]
R5230	RES_402	m78[52A7]
R5231	RES_402	m78[52A7]
R5250	RES_402	m78[52D4]
R5251	RES_402	m78[52D4]
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R5261	RES_402	m78[52C4]
R5270	RES_402	m78[52D2]
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R5342	RES_402	m78[53B7]
R5343	RES_1206	m78[53B5]
R5350	RES_2512-1	m78[53C3]
R5351	RES_402	m78[53C3]
R5352	RES_402	m78[53C2]
R5353	RES_402	m78[53D3]
R5354	RES_402	m78[53D3]
R5355	RES_402	m78[53D3]
R5370	RES_402	m78[53C7]
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R5501	RES_402	m78[55A2]
R5510	RES_402	m78[55B3]
R5511	RES_402	m78[55B3]
R5512	RES_402	m78[55B3]
R5570	RES_402	m78[55D4]
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R5601	RES_402	m78[56A7]
R5602	RES_1206	m78[56D6]
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R5605	RES_805	m78[56D5]
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R5609	RES_805	m78[56B5]
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R5699	RES_402	m78[56C7]
R5700	RES_402	m78[57C7]
R5701	RES_805	m78[57D5]
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R5705	RES_402	m78[57D6]
R5797	RES_402	m78[57C8]
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R6101	RES_402	m78[61C5]
R6114	RES_402	m78[61B4]
R6190	RES_402	m78[61B6]
R6191	RES_402	m78[61B6]
R6193	RES_402	m78[61B3]
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R7001	RES_402	m78[70D8]
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R7008	RES_402	m78[70D5]
R7010	RES_402	m78[70D7]
R7011	RES_402	m78[70C7]
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R7014	RES_402	m78[70C7]
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R7019	RES_402	m78[70C7]
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R7021	RES_402	m78[70C7]
R7030	RES_402	m78[70C3]
R7031	RES_402	m78[70C3]

R7032	RES_402	m78[70C3]
R7033	RES_402	m78[70C3]
R7034	RES_402	m78[70D3]
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R7036	RES_402	m78[70B3]
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R7064	RES_402	m78[70B6]
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R7066	RES_402	m78[70C6]
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R7092	RES_402	m78[70B3]
R7100	RES_402	m78[71C2]
R7101	RES_603	m78[71C2]
R7102	RES_1206	m78[71B3]
R7103	RES_1206	m78[71D3]
R7104	RES_402	m78[71C1]
R7105	RES_402	m78[71B2]
R7106	RES_603	m78[71B2]
R7107	RES_402	m78[71B1]
R7108	RES_402	m78[71C8]
R7109	RES_402	m78[71B7]
R7110	RES_402	m78[71B7]
R7111	RES_402	m78[71B8]
R7112	RES_402	m78[71D7]
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R7118	RES_402	m78[71B5]
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R7123	RES_402	m78[71A4]
R7126	THERMISTER_402	m78[71C8]
R7127	RES_402	m78[71C7]
R7130	RES_402	m78[71B4]
R7131	THERMISTER_0603-LF	m78[71B4]
R7140	RES_603	m78[71B1]
R7141	RES_603	m78[71C1]
R7142	RES_402	m78[71D4]
R7143	RES_402	m78[71C4]
R7197	RES_402	m78[71D6]
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R7200	RES_402	m78[72C3]
R7201	RES_603	m78[72B3]
R7203	RES_1206	m78[72C3]
R7204	RES_402	m78[72C2]
R7241	RES_603	m78[72C2]
R7250	RES_402	m78[72C5]
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R7311	RES_1206	m78[73A3]
R7312	RES_1206	m78[73A3]
R7313	RES_1206	m78[73A3]
R7321	RES_402	m78[73C5]
R7323	RES_402	m78[73B5]
R7331	RES_402	m78[73C5]
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R7384	RES_402	m78[73B4]
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R7391	RES_402	m78[73B2]
R7400	RES_402	m78[74B7]
R7401	RES_402	m78[74B7]
R7406	RES_1206	m78[74C7]
R7421	RES_402	m78[74C5]
R7423	RES_402	m78[74B5]
R7431	RES_402	m78[74C5]
R7456	RES_1206	m78[74C2]
R7461	RES_402	m78[74C4]
R7471	RES_402	m78[74C3]
R7483	RES_402	m78[74B4]
R7490	RES_402	m78[74B2]
R7491	RES_402	m78[74B2]
R7500	RES_402	m78[75D5]
R7501	RES_402	m78[75C2]
R7504	RES_402	m78[75D7]
R7505	RES_402	m78[75C7]
R7506	RES_402	m78[75C7]
R7507	RES_402	m78[75D5]
R7508	RES_402	m78[75C7]
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R7618	RES_402	m78[76D6]
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R7626	RES_402	m78[76C7]
R7627	RES_402	m78[76B7]
R7628	RES_402	m78[76B7]
R7629	RES_402	m78[76C7]

R7630	RES_402	m78[76A7]
R7631	RES_402	m78[76A7]
R7661	RES_402	m78[76C2]
R7664	RES_402	m78[76C3]
R7665	RES_402	m78[76B4]
R7666	RES_402	m78[76C2]
R7667	RES_402	m78[76B2]
R7668	RES_402	m78[76B2]
R7669	RES_402	m78[76C2]
R7670	RES_402	m78[76C4]
R7692	RES_402	m78[76A6]
R7700	RES_402	m78[77C6]
R7701	RES_402	m78[77C5]
R7702	RES_402	m78[77B5]
R7703	RES_402	m78[77B3]
R7704	RES_402	m78[77B3]
R7705	RES_402	m78[77B2]
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R7712	RES_402	m78[77D4]
R7713	RES_402	m78[77C4]
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R7810	RES_402	m78[78D8]
R7811	RES_402	m78[78D7]
R7850	RES_402	m78[78C5]
R7851	RES_402	m78[78C5]
R7870	RES_402	m78[78B7]
R7871	RES_402	m78[78B7]
R7888	RES_402	m78[78C1]
R7889	RES_402	m78[78C2]
R7891	RES_402	m78[78D3]
R7892	RES_402	m78[78D2]
R7893	RES_402	m78[78D3]
R7894	RES_805	m78[78D1]
R7895	RES_402	m78[78A7]
R7896	RES_402	m78[78A6]
R7897	RES_402	m78[78B6]
R7898	RES_402	m78[78B6]
R8500	RES_402	m78[85C7]
R8501	RES_402	m78[85C5]
R8502	RES_402	m78[85C7]
R8503	RES_402	m78[85A4]
R8505	RES_402	m78[85B4]
R8570	RES_402	m78[85D3]
R9000	RES_402	m78[90C8]
R9001	RES_402	m78[90C7]
R9002	RES_805	m78[90C8]
R9003	RES_805	m78[90C8]
R9070	RES_402	m78[90B7]
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R9075	RES_402	m78[90B2]
R9090	RES_805	m78[90C6]
R9099	RES_402	m78[90C8]
R9140	RES_402	m78[91A6]
R9141	RES_402	m78[91B6]
R9142	RES_402	m78[91B6]
R9160	RES_402	m78[91B3]
R9161	RES_402	m78[91A3]
R9400	RES_402	m78[94D7]
R9402	RES_402	m78[94D7]
R9403	RES_402	m78[94D7]
R9404	RES_402	m78[94C7]
R9405	RES_402	m78[94C7]
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R9409	RES_402	m78[94C7]
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R9413	RES_402	m78[94C2]
R9414	RES_402	m78[94C2]
R9415	RES_402	m78[94B7]
R9420	RES_402	m78[94D1]
R9421	RES_402	m78[94D1]
R9422	RES_402	m78[94C2]
RP3300	RPAK4P_SM-LF	m78[33C4 33C4 33C4 33C4]
RP3305	RPAK4P_SM-LF	m78[33B4 33C4 33C4 33C4]
RP3310	RPAK4P_SM-LF	m78[33D4 33A4 33A4 33A4]
RP3330	RPAK4P_SM-LF	m78[33D4 33B4 33B4 33B4]
RP3334	RPAK4P_SM-LF	m78[33B4 33B4 33B4 33B4]
RP3338	RPAK4P_SM-LF	m78[33A4 33B4 33B4 33A4]
RP3342	RPAK4P_SM-LF	m78[33B4 33C4 33C4 33C4]
RP3346	RPAK4P_SM-LF	m78[33D4 33C4 33B4 33C4]
RP3350	RPAK4P_SM-LF	m78[33B4 33A4 33B4 33B4]
RP3354	RPAK4P_SM-LF	m78[33B4 33A4 33A4 33B4]
RP3358	RPAK4P_SM-LF	m78[33C4 33C4 33C4 33C4]
RP3362	RPAK4P_SM-LF	m78[33A4 33C4 33D4 33A4]
S5000	SWI_TACT_4SM_EVQPH_S M-LF	m78[50D8]
S5010	SWI_TACT_4SM_EVQPH_S M-LF	m78[50C7]
SC0700	SPRING_CLIP_1P_EMI_C LIP-SM1	m78[7B6]
SC0701	SPRING_CLIP_1P_EMI_C LIP-SM1	m78[7B5]
SC0702	SPRING_CLIP_1P_EMI_S C57	m78[7B5]
SDF0717	PCB_STANDOFF	m78[7A3]
SDF0721	PCB_STANDOFF	m78[7A3]
SDF0726	HSK_NUT_TH	m78[7A6]
SDF0727	HSK_NUT_TH	m78[7A5]
SDF0750	PCB_STANDOFF	m78[7A3]
SDF0751	PCB_STANDOFF	m78[7A2]
SDF3400	PCB_STANDOFF	m78[34A5]
SDF4400	PCB_STANDOFF	m78[44D4]
SDF4401	PCB_STANDOFF	m78[44A4]
SDF4720	PCB_STANDOFF	m78[47D2]
SDF4721	PCB_STANDOFF	m78[47C1]
SDF9000	PCB_STANDOFF	m78[90B7]
SDF9001	PCB_STANDOFF	m78[90A7]
SDF9800	PCB_STANDOFF	m78[98D5]
SDF9801	PCB_STANDOFF	m78[98D5]
SDF9803	PCB_STANDOFF	m78[98B5]
SDF9804	PCB_STANDOFF	m78[98B5]
SW2800	SWI_TACT_4SM_EVQPH_S M-LF	m78[28A4]
T3900	XFR_LFE9245A_SOI	m78[39C5]
U1400	CRESTLINE_FCBGA	m78[14D4]
U1400	CRESTLINE_FCBGA	m78[15D4]
U1400	CRESTLINE_FCBGA	m78[16D5]
U1400	CRESTLINE_FCBGA	m78[17D3 17D7]
U1400	CRESTLINE_FCBGA	m78[18D3 18D7]
U1400	CRESTLINE_FCBGA	m78[19D5]
U1400	CRESTLINE_FCBGA	m78[20D4 20D7]

U2300	SB_ICH8M_BGA	m78[23D5]
U2300	SB_ICH8M_BGA	m78[24B7 24D4]
U2300	SB_ICH8M_BGA	m78[25D4]
U2300	SB_ICH8M_BGA	m78[26D5 26D8]
U2803	MC74VHC1G00_SC70-5	m78[28A7]
U2900	CLK_SYN_SLG8LP537_QF N	m78[29C5]
U3700	88E8058_QFN	m78[37C4]
U3780	EEPROM_M24C08_SO8	m78[37B2]
U4000	FW643_BGA	m78[40C5]
U4600	SWI_TPS2060_MSOP	m78[46C7]
U4601	SWI_TPS2068_MSOP	m78[46D7]
U4650	PI3USB10_TDFN	m78[46D4]
U4900	SMC_H8S2116_BGA	m78[49A3 49C3 49B7 49D7]
U5000	VDET_RN5VD_SOT23-5A	m78[50D7]
U5050	MM3120_LLP	m78[50A4]
U5350	ZXCT1010_SOT23-5	m78[53C4]
U5500	LM95214_LLP	m78[55B4]
U5570	EMC1043_MSOP	m78[55D4]
U6100	FLASH_SST25VF016B_SO I_SOI	m78[61C5]
U7010	COMPARATOR_LM339A_SO I-LF	m78[70D6]
U7052	MC74VHC1G08_SOT23-5- LF	m78[70C2]
U7056	MC74VHC1G08_SOT23-5- LF	m78[70C2]
U7100	ISL6260C_QFN	m78[71C6]
U7101	ISL6208_QFN	m78[71D5]
U7102	ISL6208_QFN	m78[71C5]
U7201	ISL6208_QFN	m78[72C7]
U7300	ISL6539_SSOP	m78[73C5]
U7400	ISL6539_SSOP	m78[74C5]
U7500	ISL6269_QFN	m78[75D6]
U7501	SN74LVC1G07_SC70	m78[75D8]
U7550	LREG_BD3533FVM_MSOP- 8	m78[75B4]
U7600	LTC3728L_QFN	m78[76C5]
U7601	COMPARATOR_LM393_SOI -1-LF	m78[76D6 76A7]
U7710	TPS62050_MSOP	m78[77D5]
U7750	TPS62510_BQA	m78[77B4]
U8570	EEPROM_M24C02_SO8	m78[85D2]
U9130	VIDEO_TS3V330_SOP	m78[91B7]
U9160	74LVC1G125LF_SOT23-5	m78[91B4]
U9161	74LVC1G125LF_SOT23-5	m78[91A4]
VR5065	VREF_REF3133_SOT23-3	m78[50B8]
XW4900	SHORT_SM	m78[49C2]
XW5300	SHORT_SM	m78[53D7]
XW5350	SHORT_SM	m78[53C3]
XW5500	SHORT_SM	m78[55A4]
XW5501	SHORT_SM	m78[55A4]
XW5502	SHORT_SM	m78[55A4]
XW5503	SHORT_SM	m78[55A4]
XW7100	SHORT_SM	m78[71A6]
XW7101	SHORT_SM	m78[71B2]
XW7102	SHORT_SM	m78[71B1]
XW7103	SHORT_SM	m78[71D2]
XW7104	SHORT_SM	m78[71D1]
XW7203	SHORT_SM	m78[72C3]
XW7204	SHORT_SM	m78[72C2]
XW7300	SHORT_SM	m78[73B4]
XW7400	SHORT_SM	m78[74B4]
XW7500	SHORT_SM	m78[75C5]
XW7600	SHORT_SM	m78[76A5]
Y2800	CRYSTAL_4PIN_SM-LF	m78[28C7]
Y2901	CRYSTAL_5X3.2-SM	m78[29C6]
Y3750	CRYSTAL_SM-3-LF	m78[37B5]
Y4000	CRYSTAL_HC49-USMD	m78[40B7]
Y5020	CRYSTAL_SM-4	m78[50C8]
ZH500	HOLE_VIA	m78[7C1]
ZH501	HOLE_VIA	m78[7C1]
ZH502	HOLE_VIA	m78[7C1]
ZH503	HOLE_VIA	m78[7C1]
ZH504	HOLE_VIA	m78[7B1]
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ZH0701	MTGHOLE	m78[7A5]
ZH0702	MTGHOLE	m78[7A4]
ZH0703	MTGHOLE	m78[7A4]
ZH0711	MTGHOLE	m78[7A6]
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ZH0718	MTGHOLE	m78[7A5]
ZH0720	MTGHOLE	m78[7A4]
ZH0722	MTGHOLE	m78[7B4]
ZH0723	MTGHOLE	m78[7B4]
ZH0724	MTGHOLE	m78[7B3]
ZH0725	MTGHOLE	m78[7B3]
ZH0750	MTGHOLE	m78[7A4]