

M50 - DVT

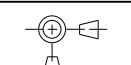
04/05/06

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
13		405954	ENGINEERING RELEASED	10/18/05	06/22/04

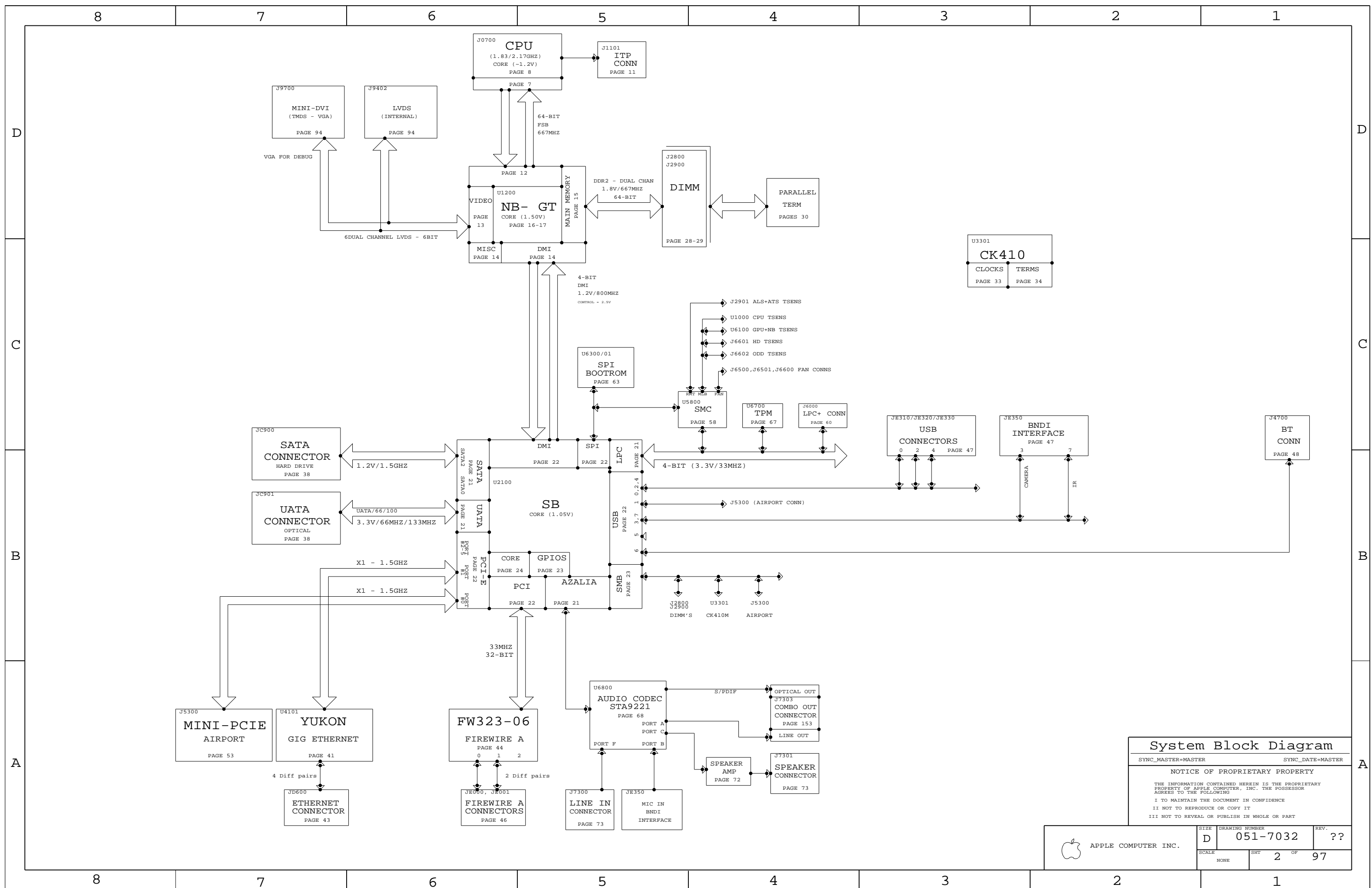
PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
5	5	FUNC TEST 1 OF 2	MASTER	MASTER	
6	6	Power Conn / Alias	MASTER	MASTER	
7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006	
12	12	NB CPU Interface	M1	01/05/2006	
13	13	NB PEG / Video Interfaces	M1	01/05/2006	
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1	01/05/2006	
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40	01/05/2006	
18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER	
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	03/30/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	03/30/2006	
54	73	AUDIO: CONNECTORS	AUDIO	03/30/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	03/30/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUI	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTR	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7032	REV. ??
SHT 1 OF 97					

D
C
B
A

D
C
B
A



System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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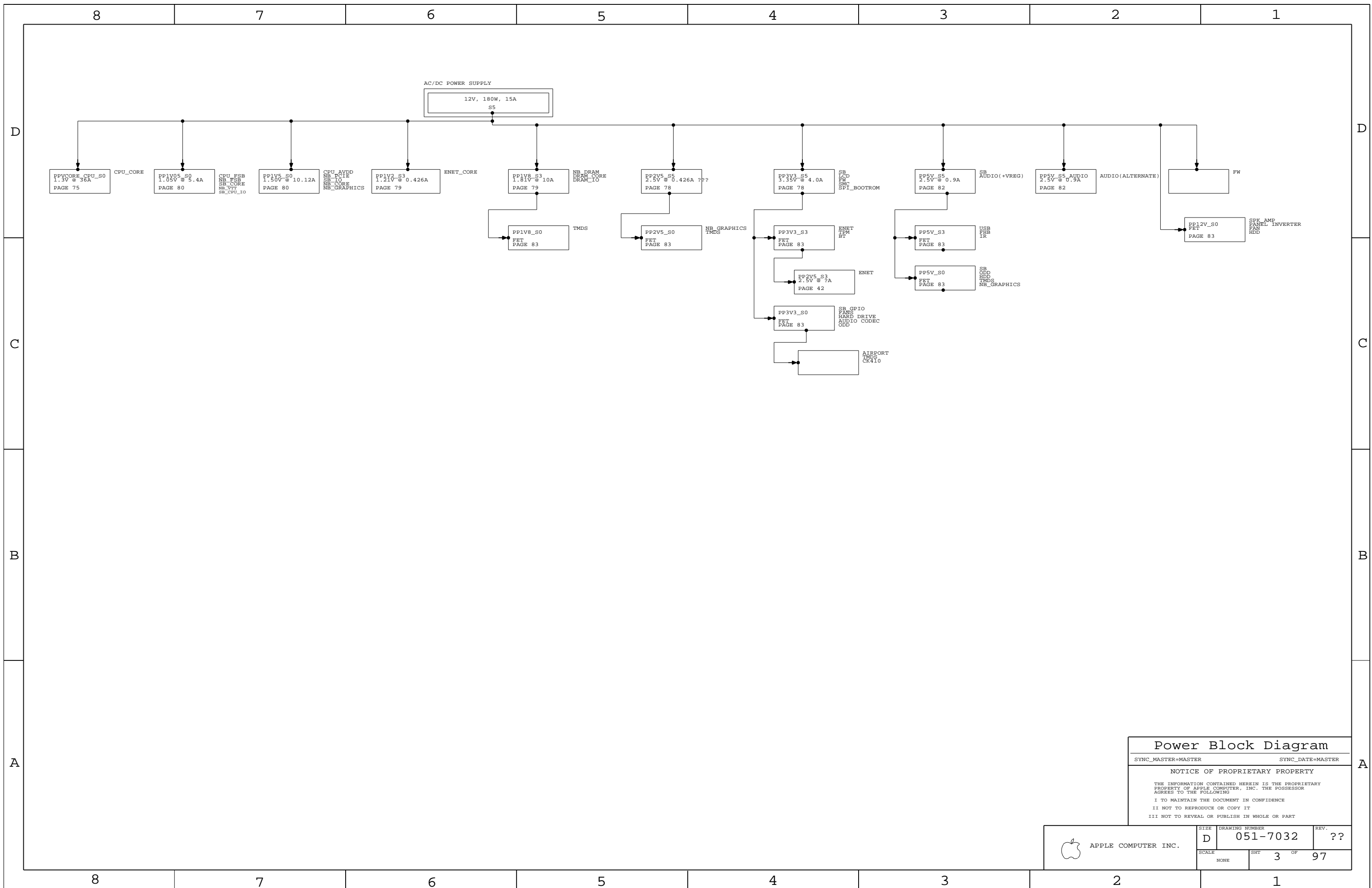
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	OF	REV.
NONE	2	97	



Power Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	OF	REV.
NONE	3	97	

8

7

6

5

4

3

2

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
338S0270	1	IC,888053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382)	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHEM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384)	1	EFI ROM,M50	U6301	CRITICAL	
341T0021	1	M50 1.66G CPU (C0)	CPU	CRITICAL	YONAH
337S3242	1	M38 CPU (C0)	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		0628	FACTORY SHORTAGE
353S1381	353S1278		U5940	SMC VREF
378S0140	378S0141		LXD601,LXD602,LXD603	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:V3M]	CRITICAL	

Table Items

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE	SHT	OF
NONE	4	97

8

7

6

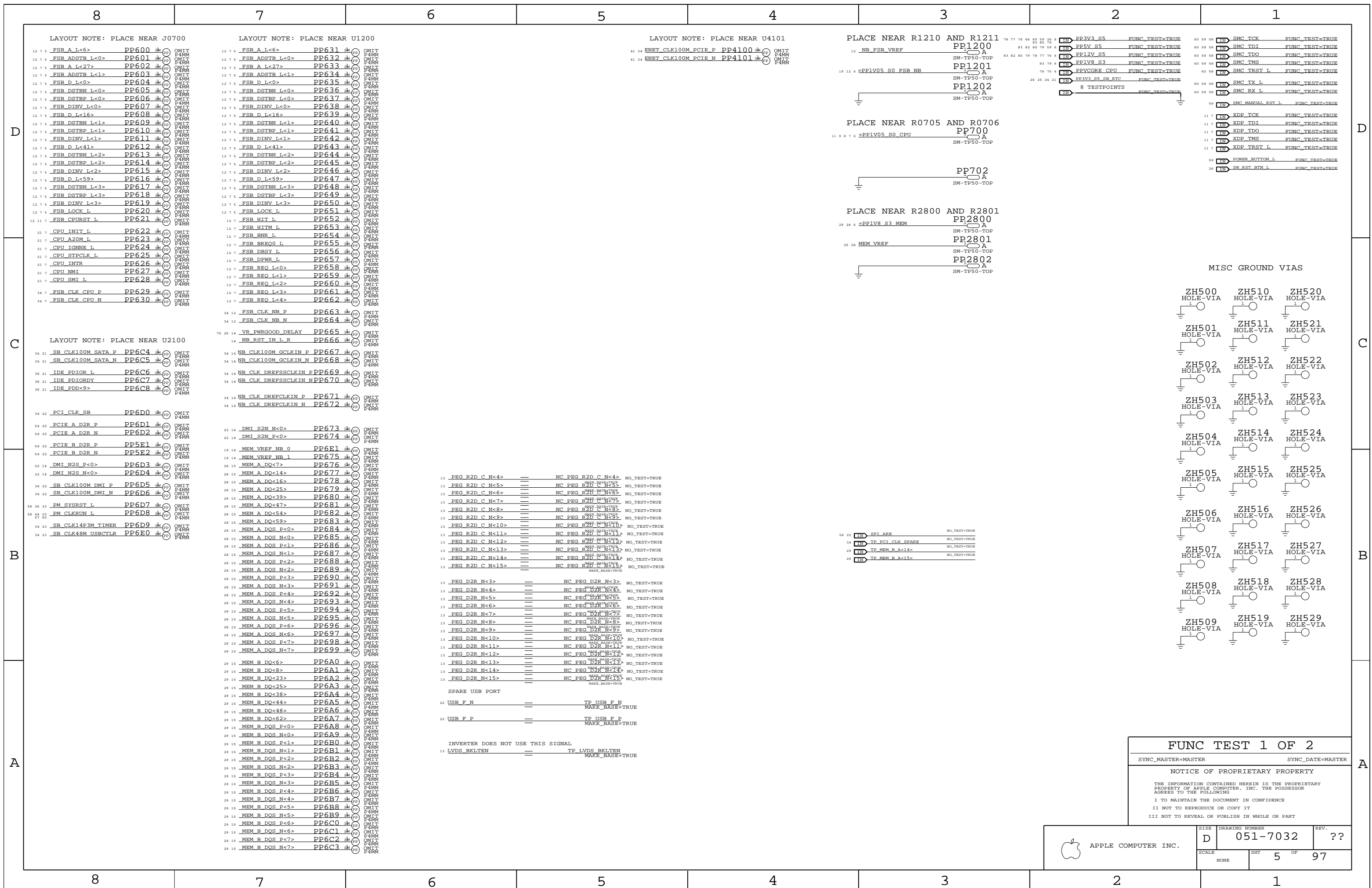
5

4

3

2

1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U4101

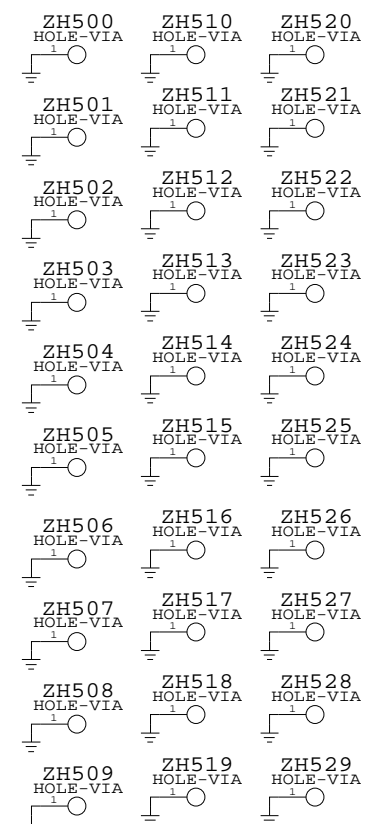
PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

LAYOUT NOTE: PLACE NEAR U2100

MISC GROUND VIAS



- 11 PEG R2D C N<4> NC PEG R2D C N<4> NO_TEST=TRUE
- 11 PEG R2D C N<5> NC PEG R2D C N<5> NO_TEST=TRUE
- 11 PEG R2D C N<6> NC PEG R2D C N<6> NO_TEST=TRUE
- 11 PEG R2D C N<7> NC PEG R2D C N<7> NO_TEST=TRUE
- 11 PEG R2D C N<8> NC PEG R2D C N<8> NO_TEST=TRUE
- 11 PEG R2D C N<9> NC PEG R2D C N<9> NO_TEST=TRUE
- 11 PEG R2D C N<10> NC PEG R2D C N<10> NO_TEST=TRUE
- 11 PEG R2D C N<11> NC PEG R2D C N<11> NO_TEST=TRUE
- 11 PEG R2D C N<12> NC PEG R2D C N<12> NO_TEST=TRUE
- 11 PEG R2D C N<13> NC PEG R2D C N<13> NO_TEST=TRUE
- 11 PEG R2D C N<14> NC PEG R2D C N<14> NO_TEST=TRUE
- 11 PEG R2D C N<15> NC PEG R2D C N<15> NO_TEST=TRUE
- 11 PEG D2R N<3> NC PEG D2R N<3> NO_TEST=TRUE
- 11 PEG D2R N<4> NC PEG D2R N<4> NO_TEST=TRUE
- 11 PEG D2R N<5> NC PEG D2R N<5> NO_TEST=TRUE
- 11 PEG D2R N<6> NC PEG D2R N<6> NO_TEST=TRUE
- 11 PEG D2R N<7> NC PEG D2R N<7> NO_TEST=TRUE
- 11 PEG D2R N<8> NC PEG D2R N<8> NO_TEST=TRUE
- 11 PEG D2R N<9> NC PEG D2R N<9> NO_TEST=TRUE
- 11 PEG D2R N<10> NC PEG D2R N<10> NO_TEST=TRUE
- 11 PEG D2R N<11> NC PEG D2R N<11> NO_TEST=TRUE
- 11 PEG D2R N<12> NC PEG D2R N<12> NO_TEST=TRUE
- 11 PEG D2R N<13> NC PEG D2R N<13> NO_TEST=TRUE
- 11 PEG D2R N<14> NC PEG D2R N<14> NO_TEST=TRUE
- 11 PEG D2R N<15> NC PEG D2R N<15> NO_TEST=TRUE

SPARE USB PORT

22 USB_F_N TP USB_F_N
MAKE_BASE=TRUE

22 USB_F_P TP USB_F_P
MAKE_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL

13 LVDS_BKLTEN TP LVDS_BKLTEN
MAKE_BASE=TRUE

FUNC TEST 1 OF 2

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SCALE NONE	SHEET 5 OF 97	SIZE D	DRAWING NUMBER 051-7032	REV. ??
		APPLE COMPUTER INC.		

"S0" RAILS

ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

82 78 76 SYS POWERFAIL L I632 POWER_GOOD

PP0V9_S0 =PP0V9_S0_MEMVTT_LDO =PP0V9_S0_MEM_TERM

PP1V2_S3 =PP1V2_S3_LAN

PP3V3_S5 =PP3V3_S5_SB =PP3V3_S5_SB_USB =PP3V3_S5_SB_PM =PP3V3_S5_SB_VCCSUS3_3 =PP3V3_S5_SB_VCCSUS3_3_USB =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA =PP3V3_S5_SB_IO =PP3V3_S5_SB_FW =PP3V3_S5_SMC =PP3V3_S5_2V5_LDO =PP3V3_S5_DEBUG =PP3V3_S5_ROM =PP3V3_S5_LCD

PPVCORE_CPU =PPVCORE_S0_CPU

PP1V8_S3 =PP1V8_S3_MEM_NB =PP1V8_S3_MEM =PP1V8_S3_1V2_LDO

PP5V_S5 =PP5V_S5_SB =PP5V_S5_AUDIO_LDO XW604 SM OMIT PP5V_S5_AUDIO =PP5V_S5_AUDIO

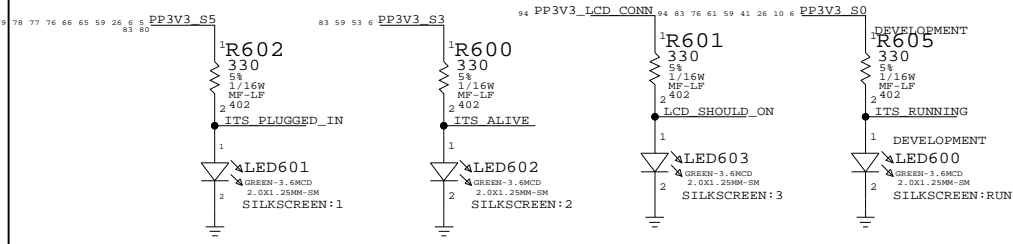
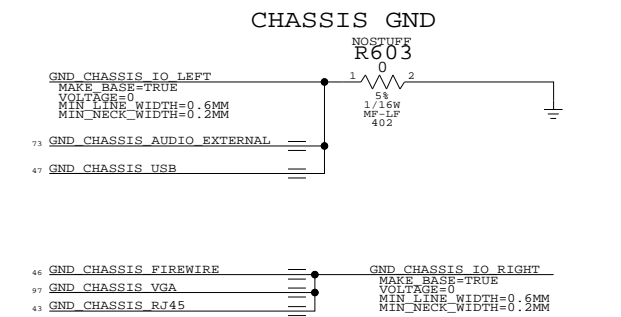
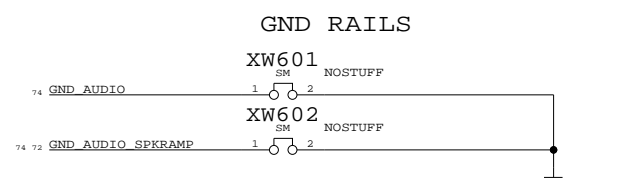
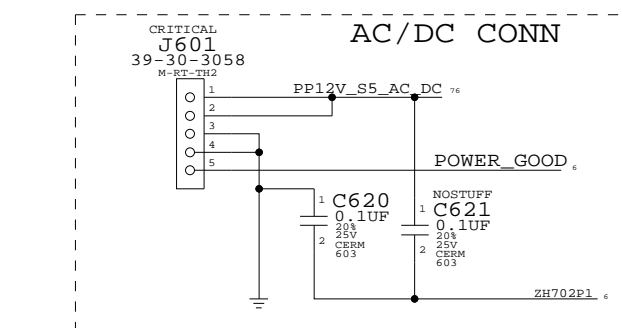
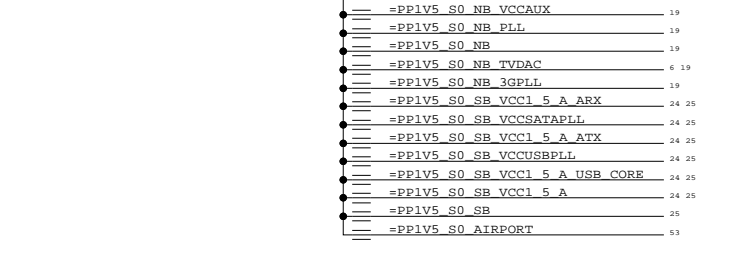
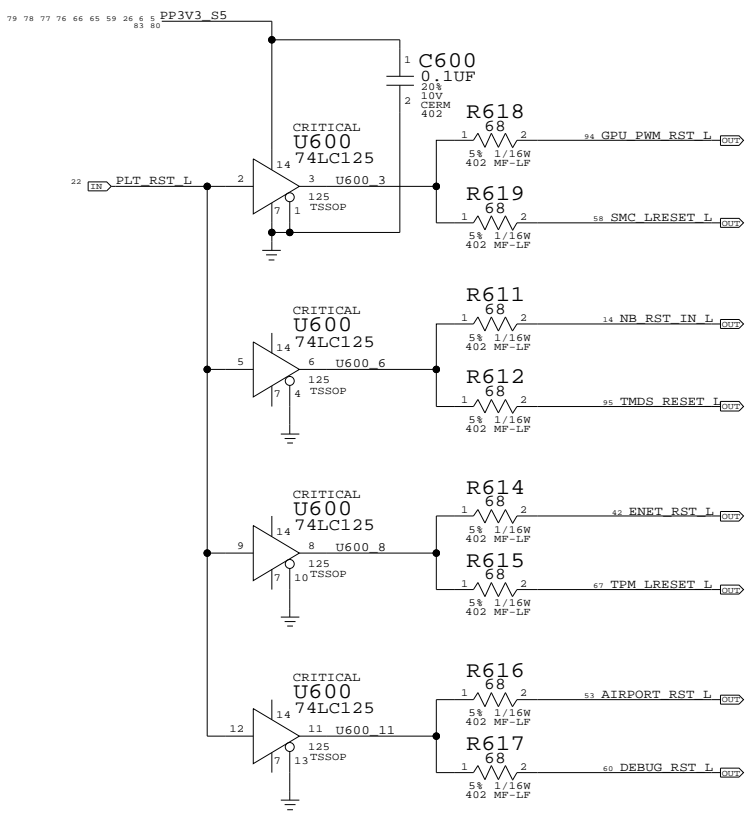
PP1V05_S0 =PP1V05_S0_CPU =PP1V05_S0_FSB_NB =PP1V05_S0_NB_VTT =PP1V05_S0_SB_CPU_IO =PPVCORE_S0_SB

PP3V3_S3 =PP3V3_S3_ENET =PP3V3_S3_TPM =PP3V3_S3_BT

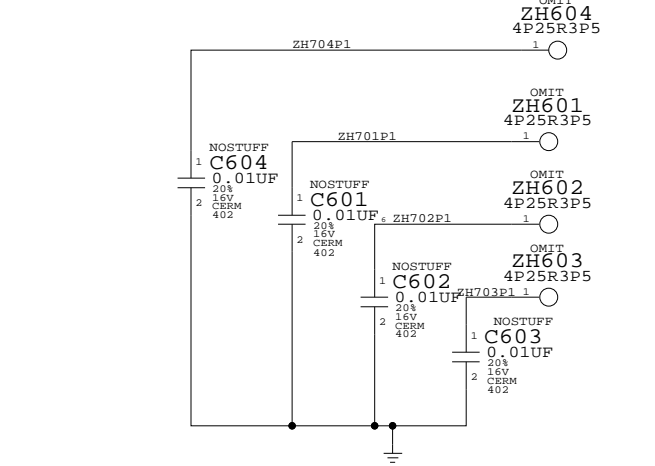
PP1V5_S0 =PPVCORE_S0_NB =PP1V5_S0_CPU =PP1V5_S0_NB_PCIE =PP1V5_S0_NB_TVDAC =PP1V5_S0_NB_VCCD_HMPLL =PP1V5_S0_NB_VCCD_LVDS =PP1V5_S0_NB_VCCD_LVDS =PP1V5_S0_NB_VCCAUX =PP1V5_S0_NB_PLL =PP1V5_S0_NB =PP1V5_S0_NB_TVDAC =PP1V5_S0_NB_3GPLL =PP1V5_S0_SB_VCC1_5_A_ARX =PP1V5_S0_SB_VCCSATAPLL =PP1V5_S0_SB_VCC1_5_A_ATX =PP1V5_S0_SB_VCCSUSBLL =PP1V5_S0_SB_VCC1_5_A_USB_CORE =PP1V5_S0_SB_VCC1_5_A =PP1V5_S0_SB =PP1V5_S0_AIRPORT

PP5V_S3 =PP5V_S3_USB =PP5V_S3_BNDI =PP5V_S0_MEMVTT USING S3 TO DRIVE S0 OK IN THIS CASE

PP12V_S5 =PP12V_S5_FW =PP12V_S5_CPU



PP4V5_S0_AUDIO_ANALOG =PP4V5_S0_AUDIO_ANALOG



PP5V_S0 =PP5V_S0_SB =PP5V_S0_PATA =PP5V_S0_NBISENSE =PP5V_S0_DEBUG =PP5V_S0_SATA =PP5V_S0_TMSD =PP5V_S0_NB_TVDAC

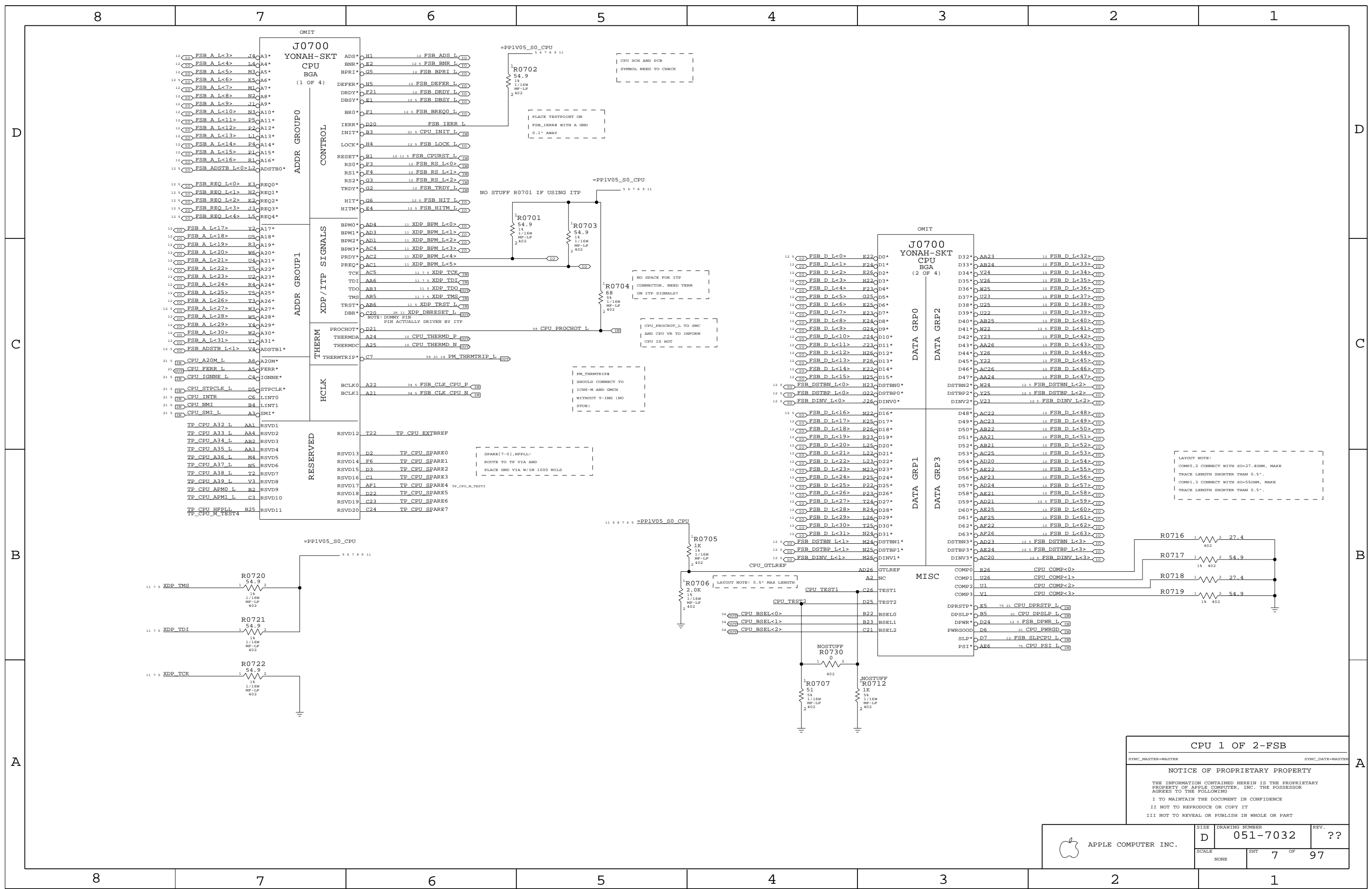
Power Conn / Alias

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Table with columns: SCALE, SHEET, OF, REV. Row 1: NONE, 6, OF, 97. Row 2: APPLE COMPUTER INC., D, 051-7032, ??



CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATE-MASTER

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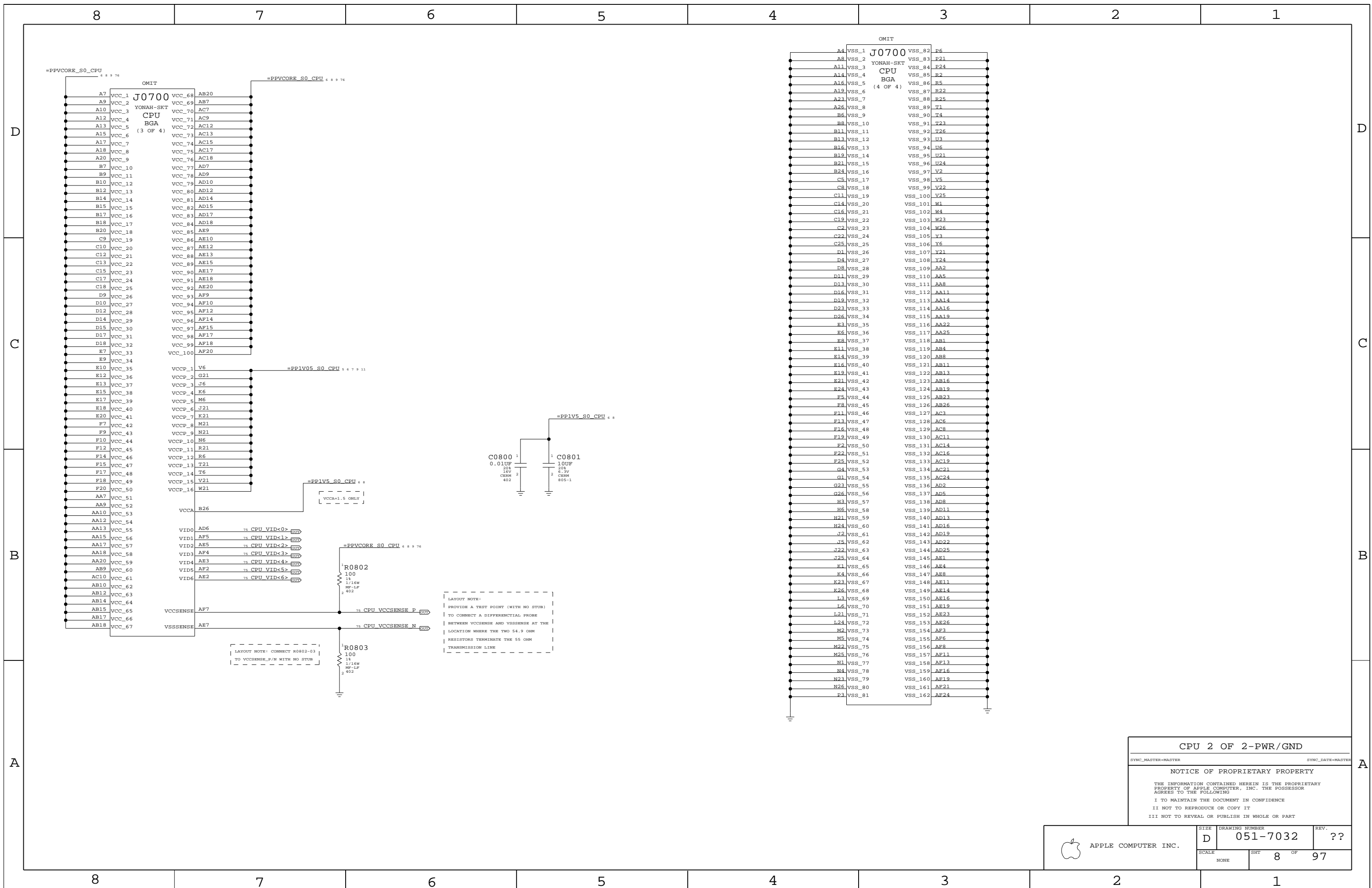
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	SCALE NONE	SHEET 7 OF 97	



CPU 2 OF 2-PWR/GND

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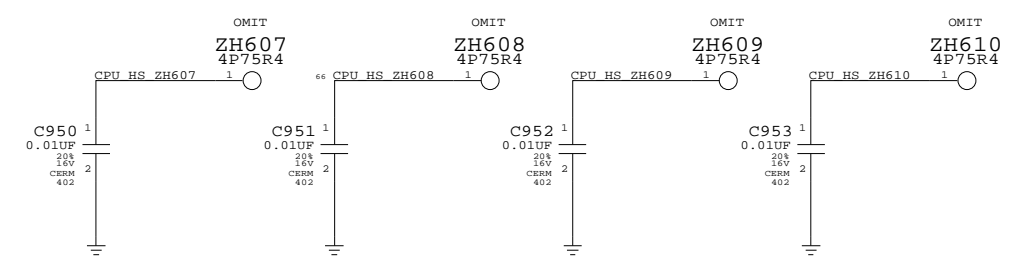
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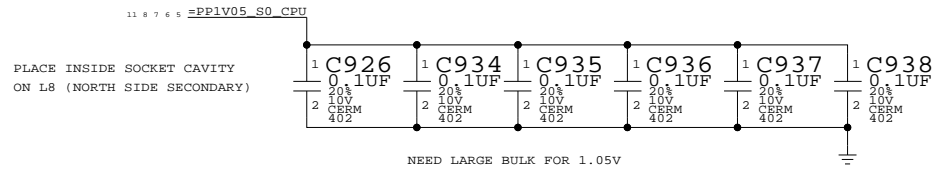
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 8 OF 97	

CPU HEATSINK MOUNTING HOLES



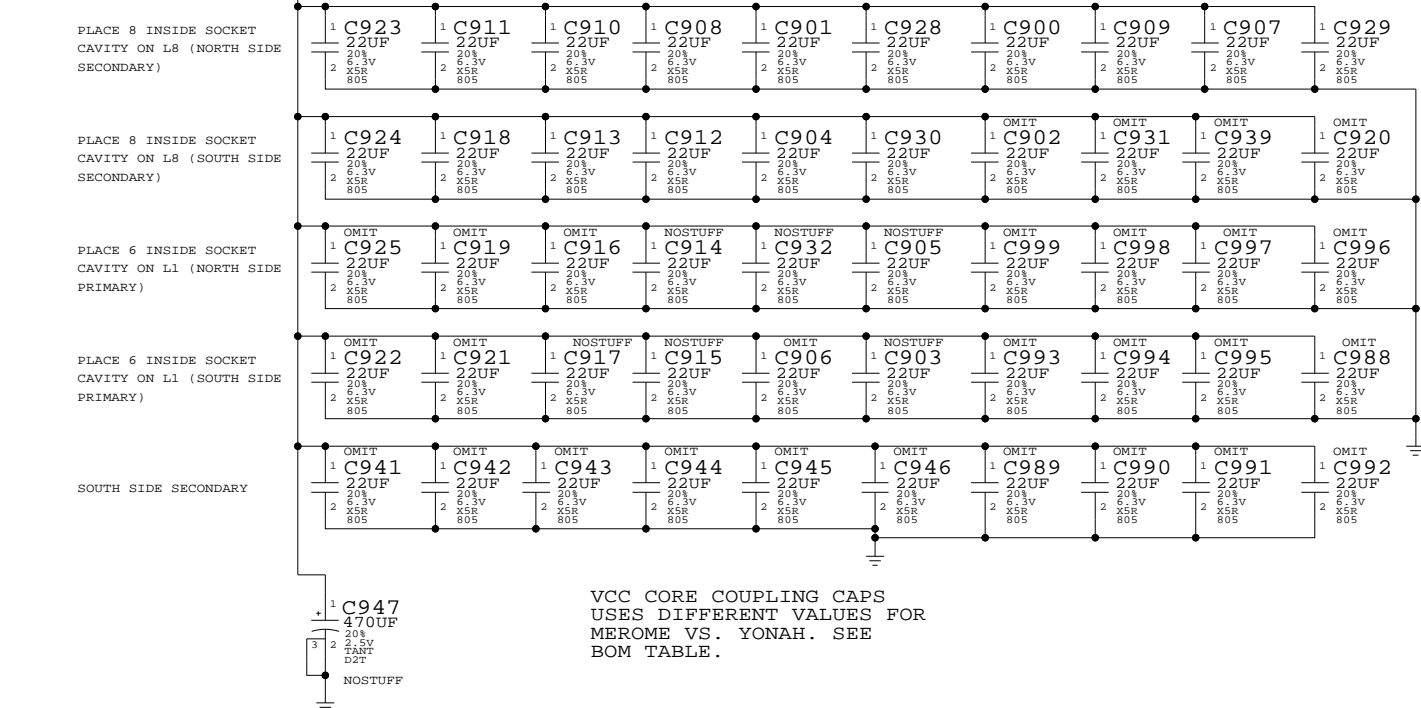
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

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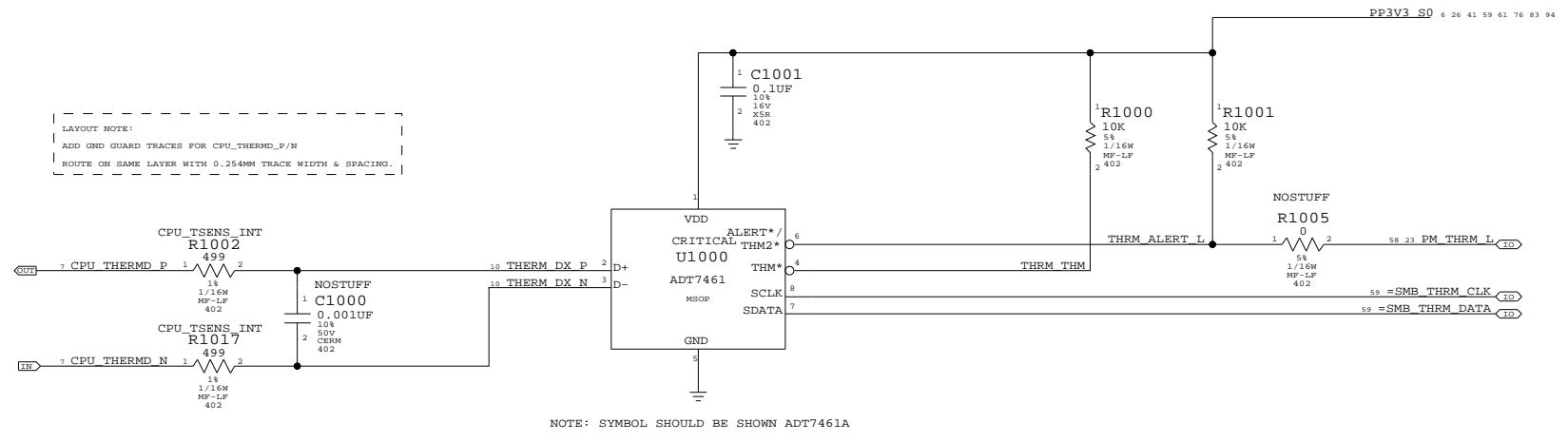
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	9 OF	97
NONE			

CPU THERMAL SENSOR

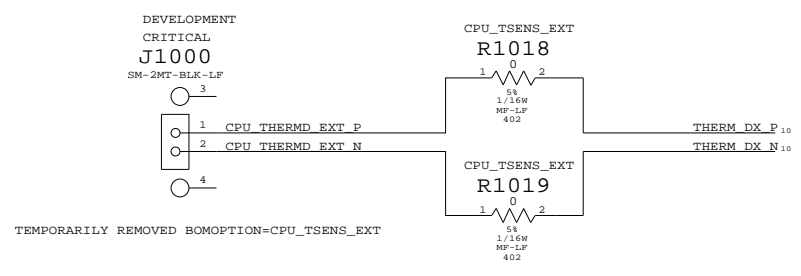
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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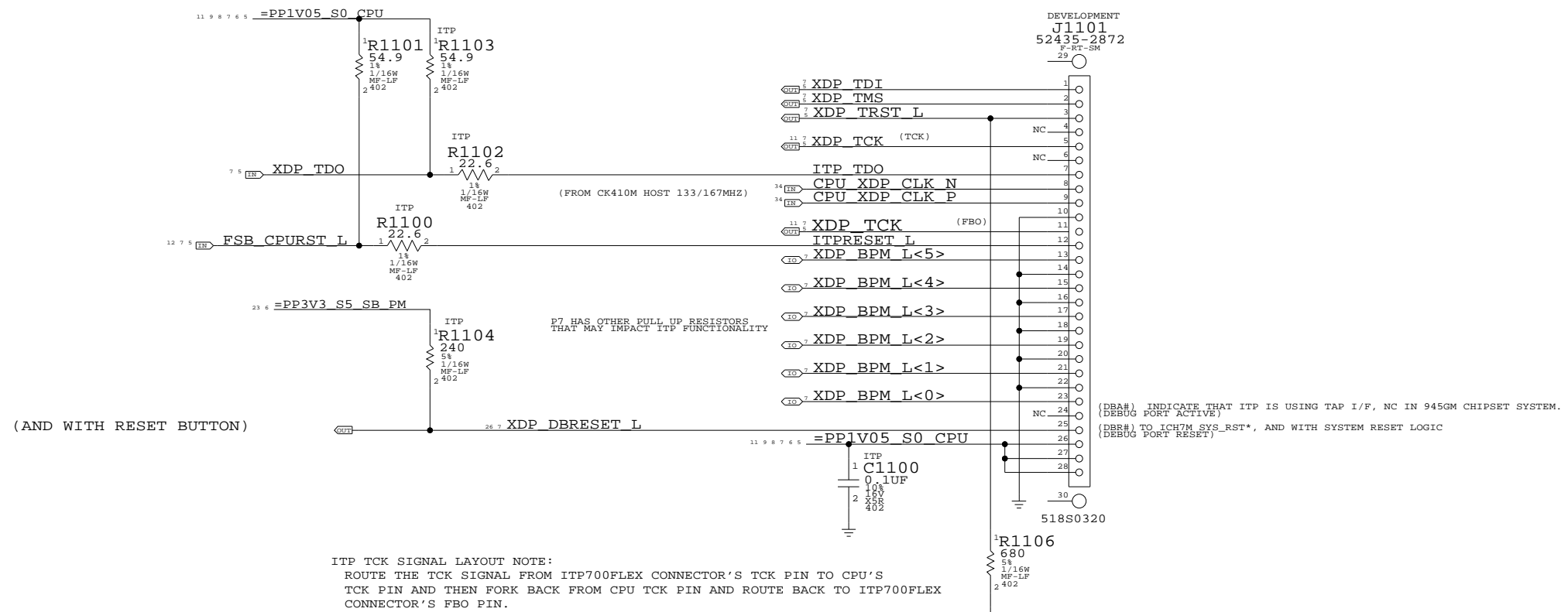
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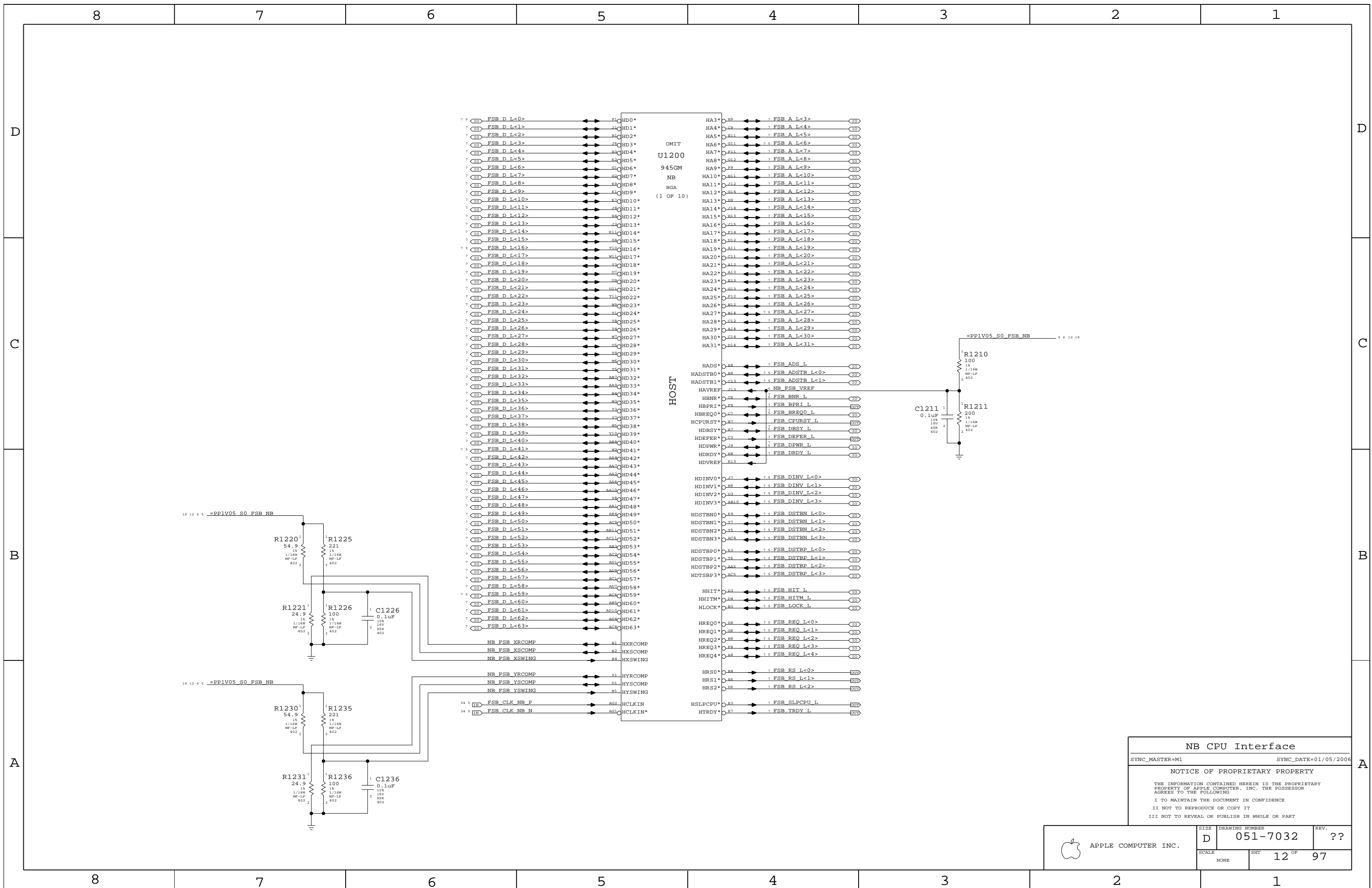
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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	D	051-7032	??
SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

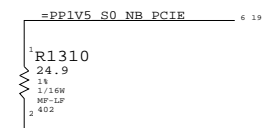
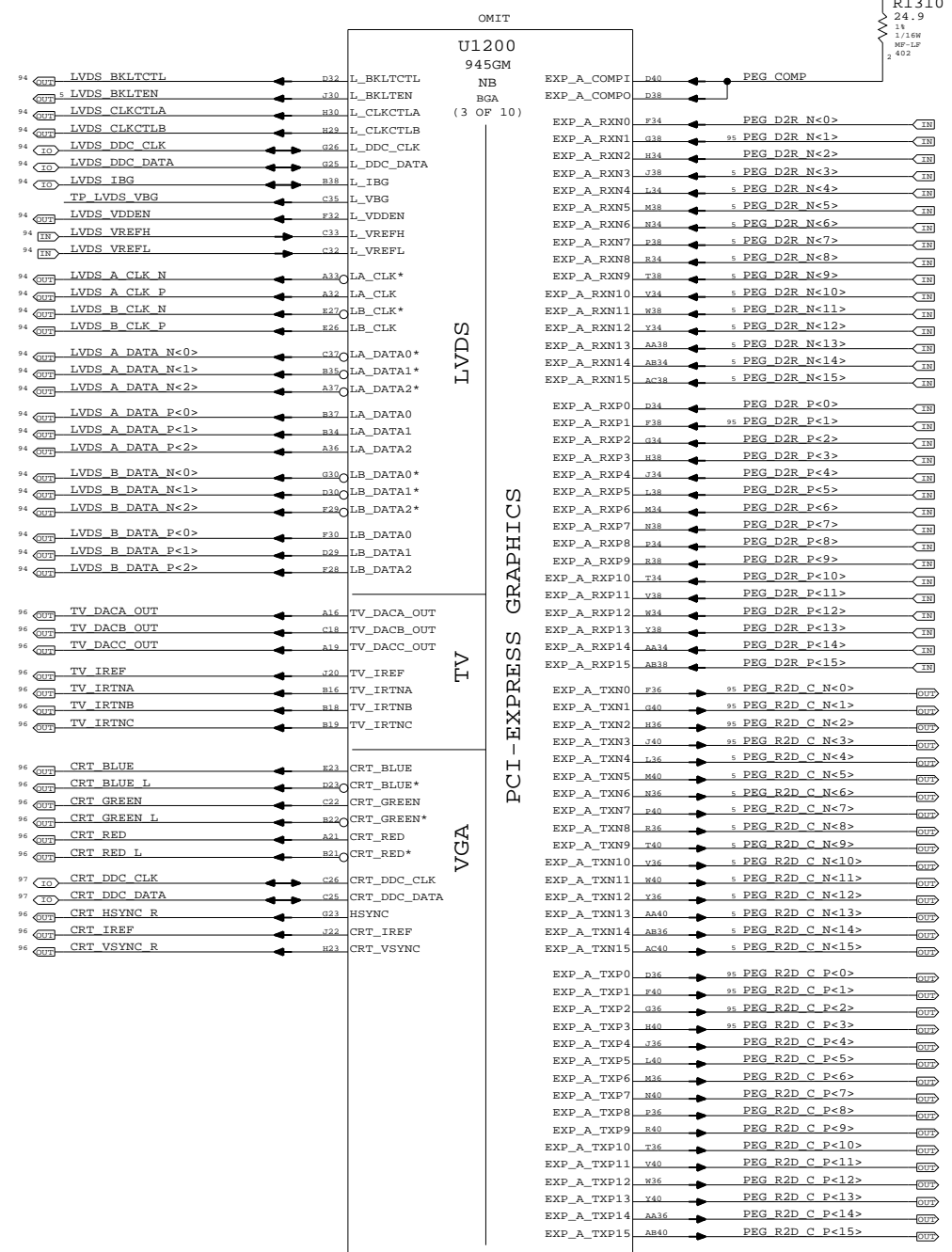
LVDS Disable
Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable
Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

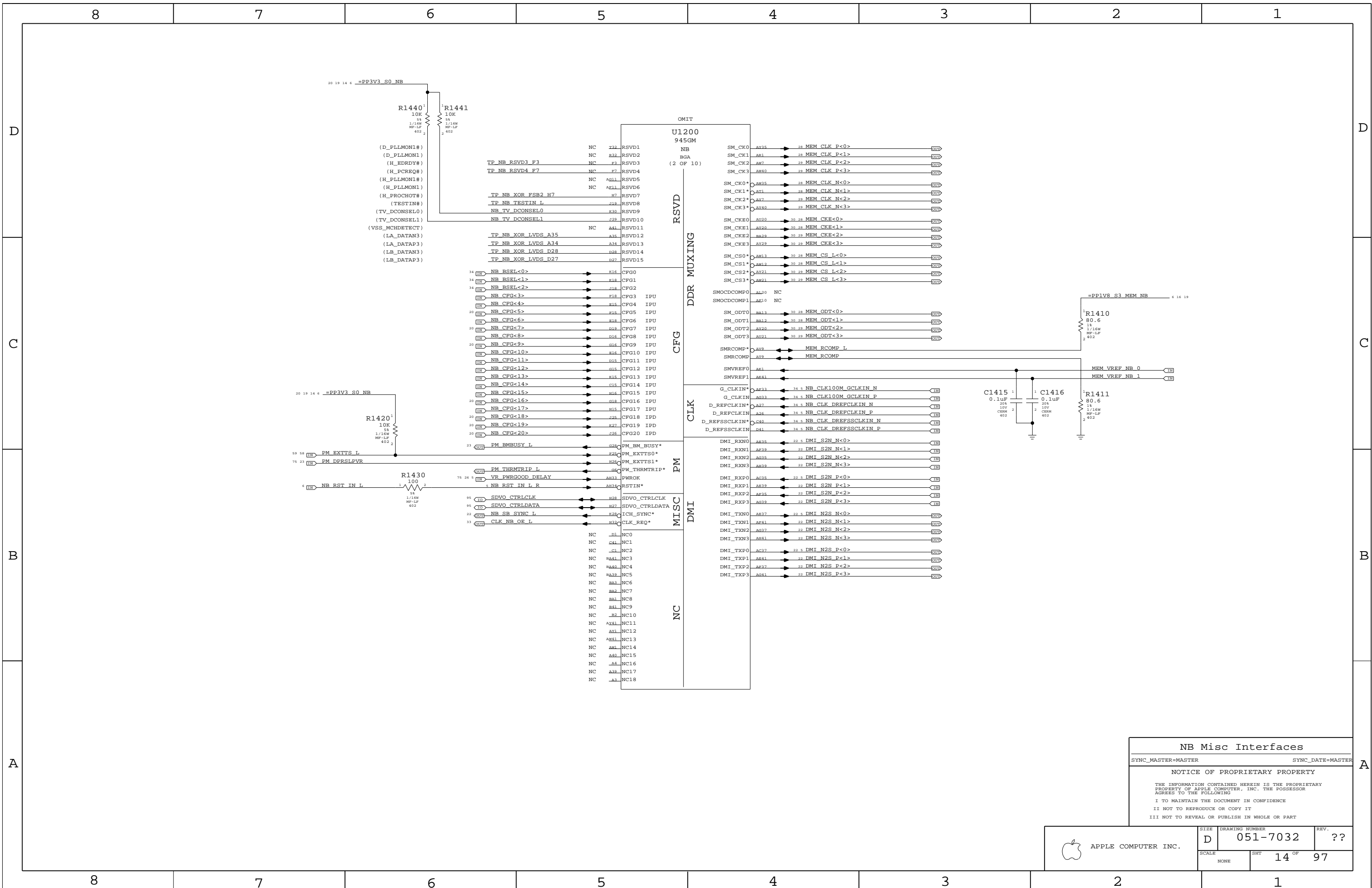
NB PEG / Video Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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SCALE	SHT	13 OF	97
NONE			



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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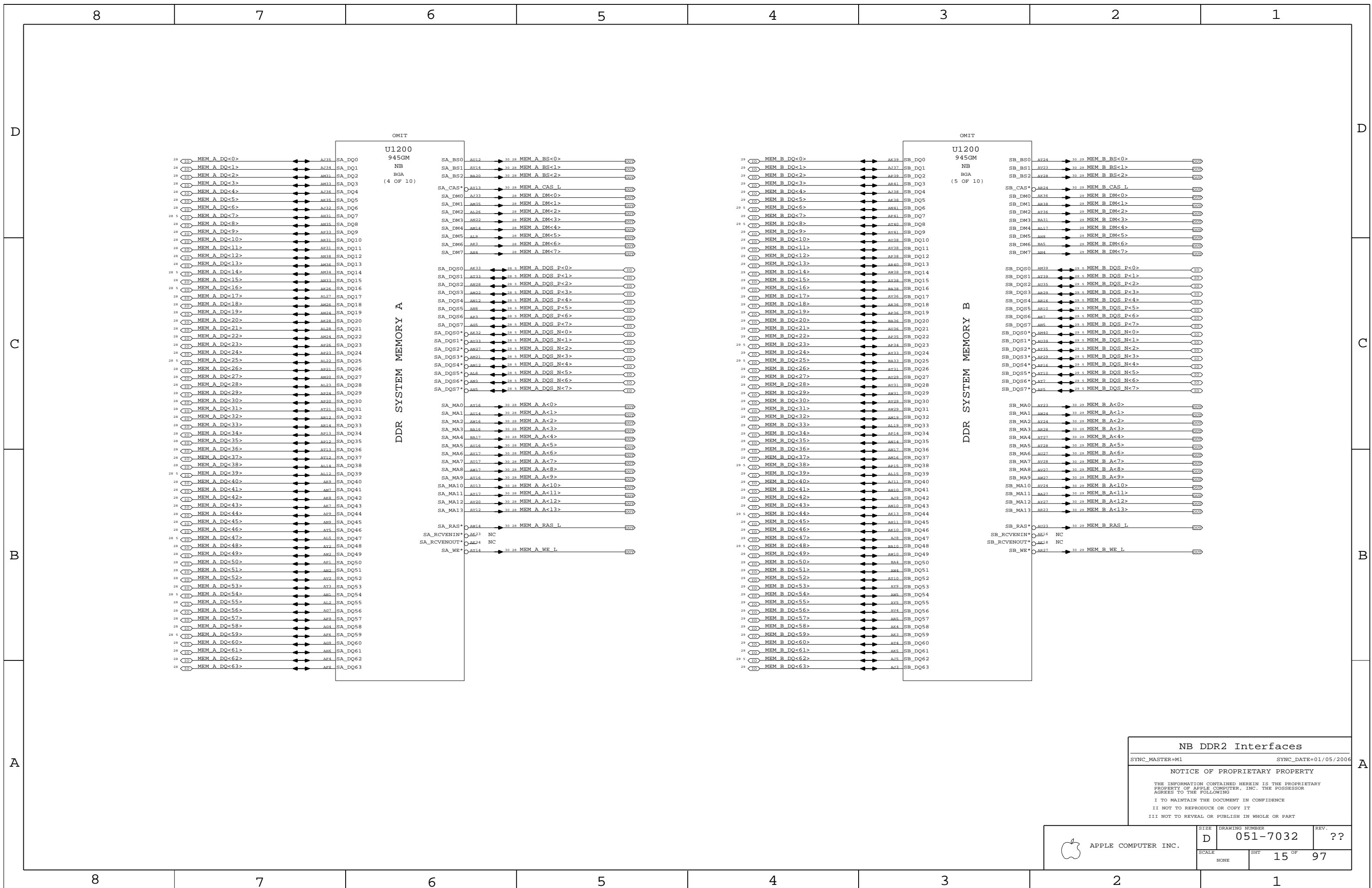
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SCALE	SHT	14 OF 97	
NONE			



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 15 OF 97	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT

D

D

C

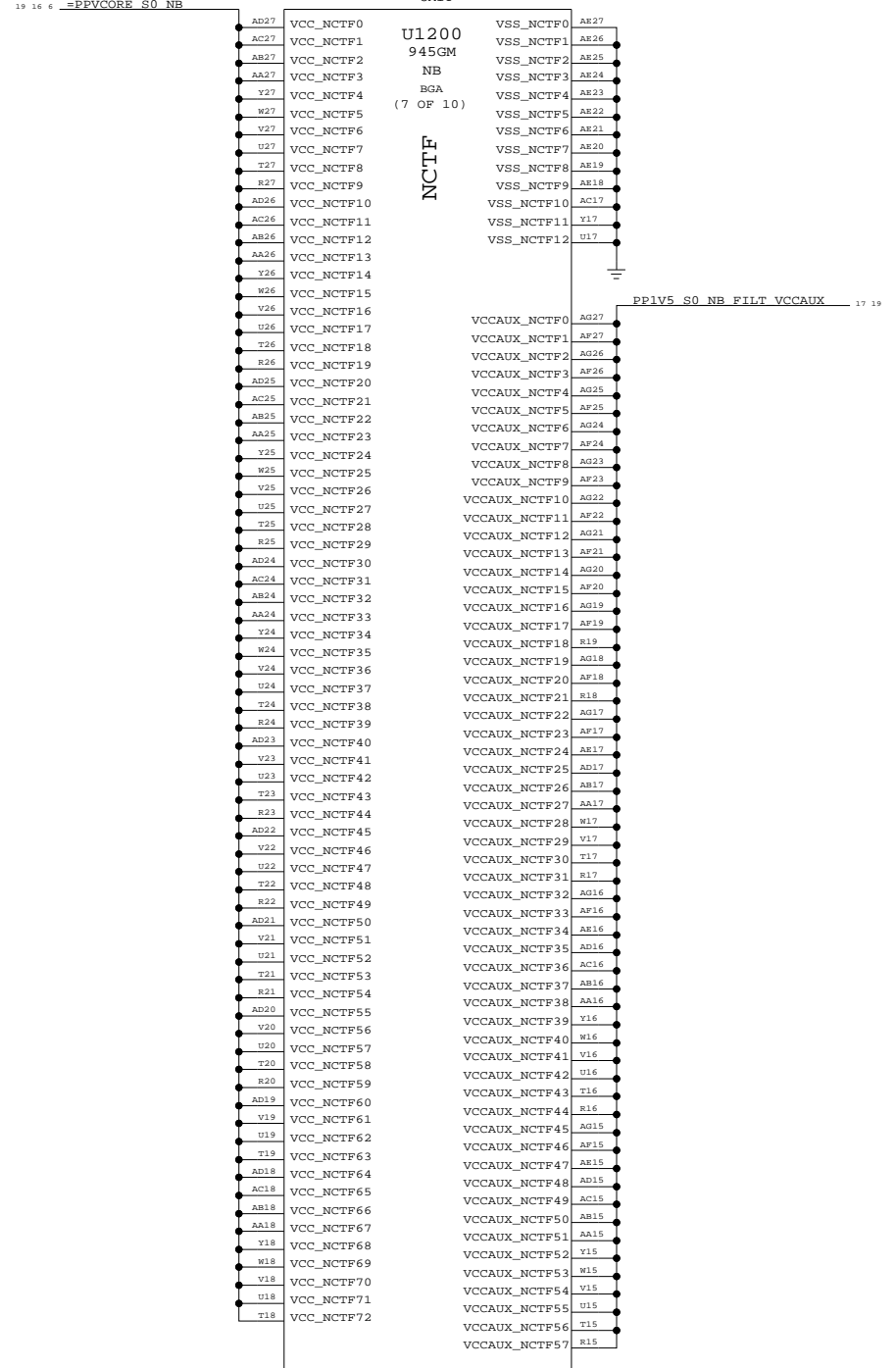
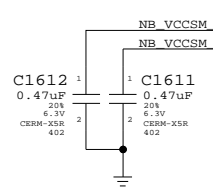
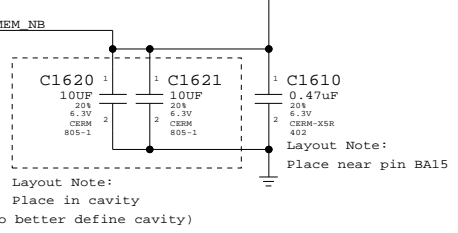
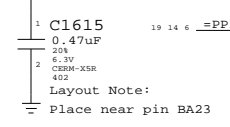
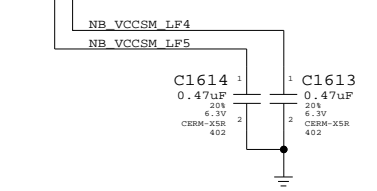
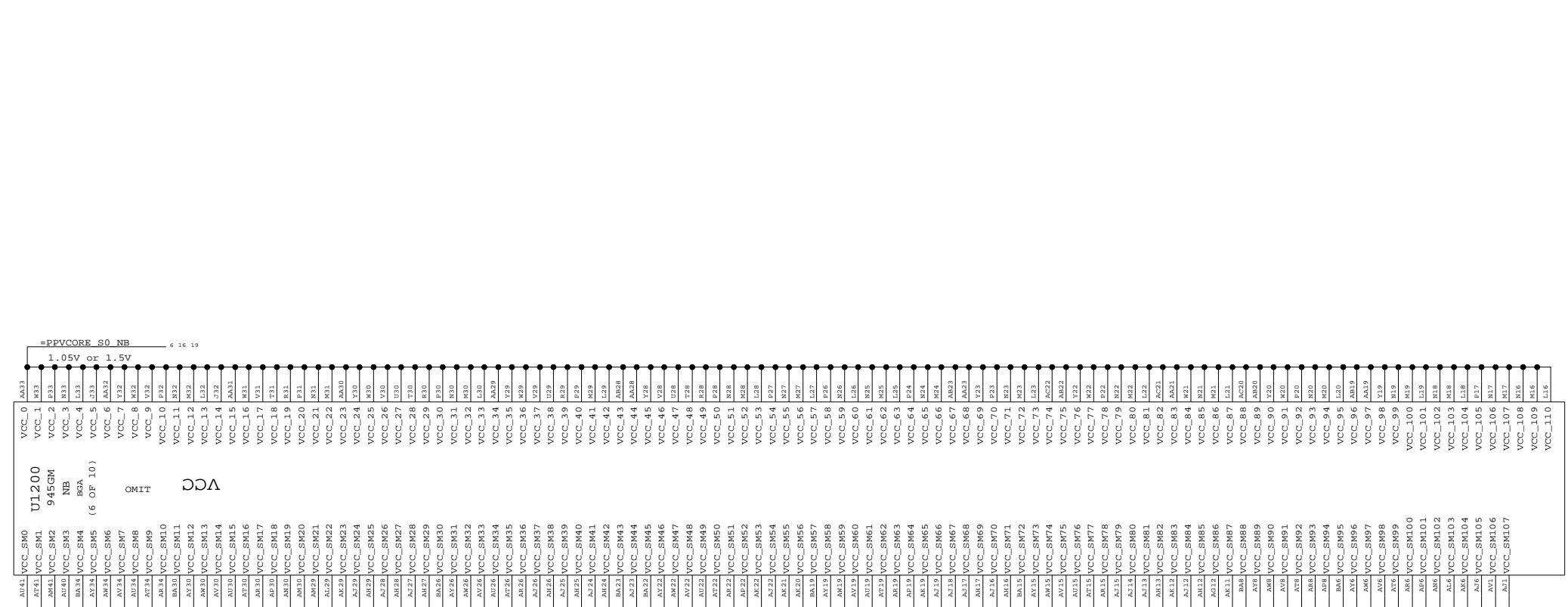
C

B

B

A

A



NB Power 1

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

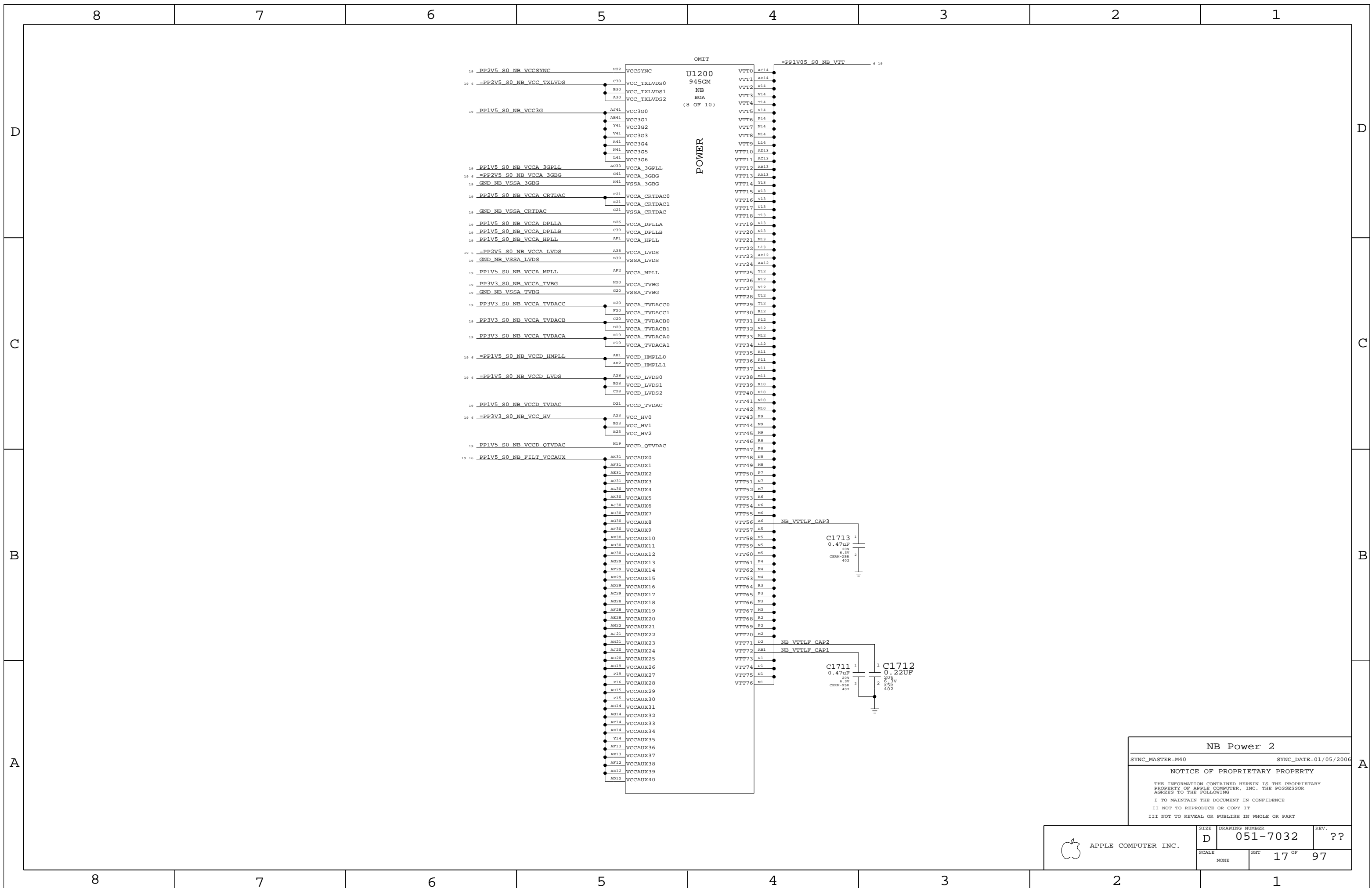
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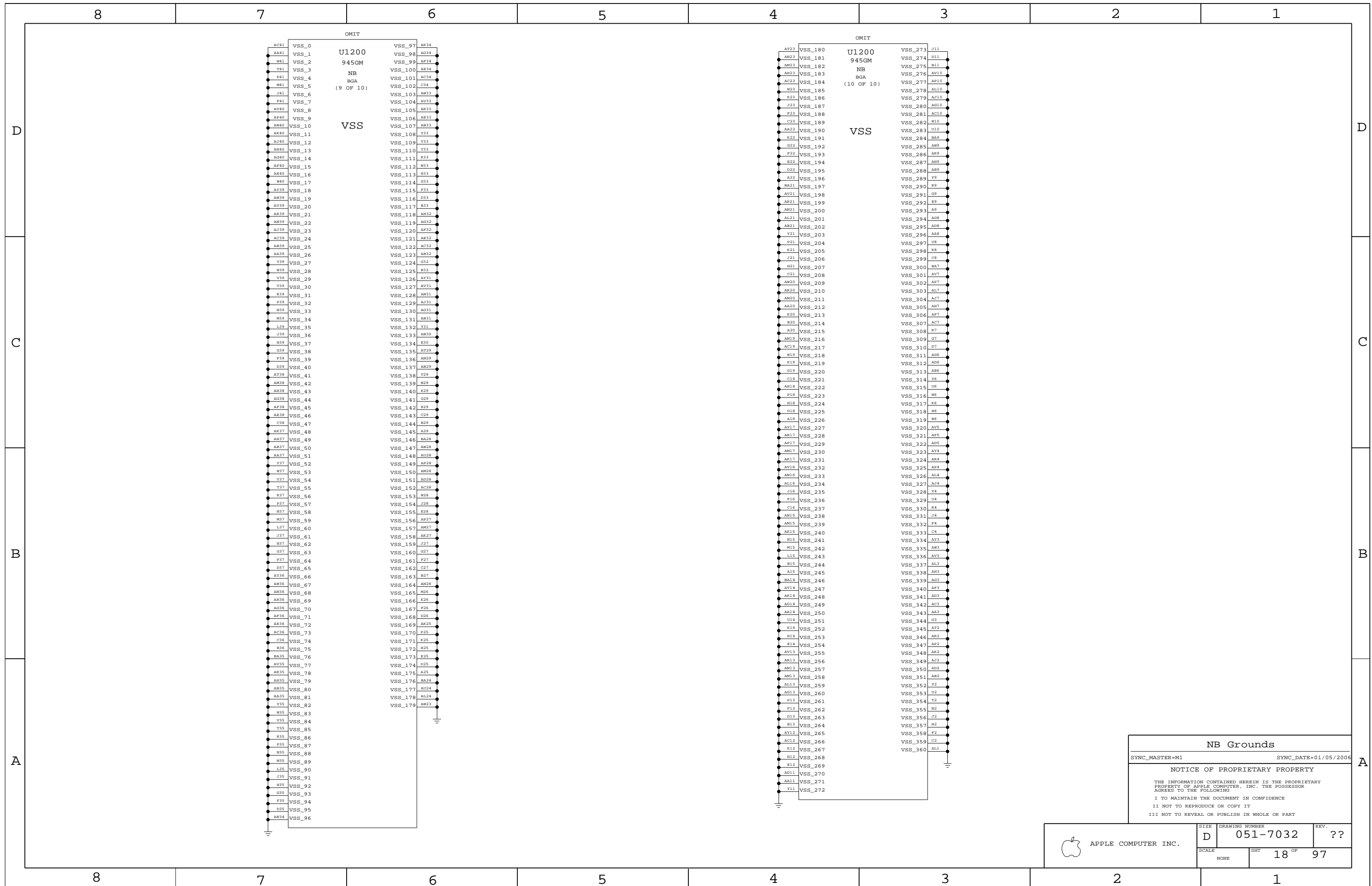
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	16 OF	97
NONE			



NB Power 2
 SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	17 OF 97	
NONE			



NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 18 OF 97	

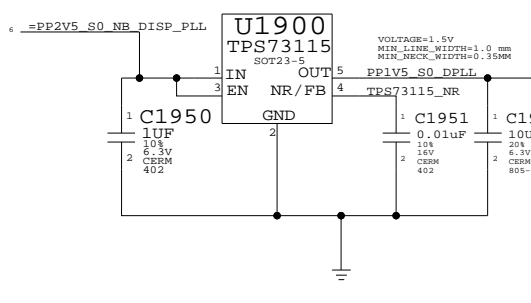
Power Interface

These are the power signals that leave the NB "block"

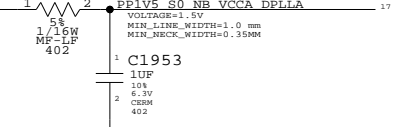
- =PP1V05_S0_FSB_NB 5 6 12
- =PPVCORE_S0_NB 6 16 19
- =PP1V05_S0_NB_VTT 6 17 19
- =PP1V5_S0_NB 6 19
- =PP1V5_S0_NB_PCIE 6 13
- =PP1V5_S0_NB_PLL 6 19
- =PP1V5_S0_NB_TVDAC 6 19
- =PP1V5_S0_NB_VCCD_HMPLL 6 17
- =PP1V5_S0_NB_VCCD_LVDS 6 17 19
- =PP1V5_S0_NB_VCCAUX 6 19
- =PP1V8_S3_MEM_NB 6 14 16 19

- I276
- =PP2V5_S0_NB_VCCSYNC 19 6
- =PP2V5_S0_NB_VCC_TXLVDS 6 17 19
- =PP2V5_S0_NB_VCCA_3GBG 6 17 19
- =PP2V5_S0_NB_VCCA_LVDS 6 17 19
- =PP3V3_S0_NB 6 14 20
- =PP3V3_S0_NB_VCC_HV 6 17 19
- =PP5V_S0_NB_TVDAC 6 19

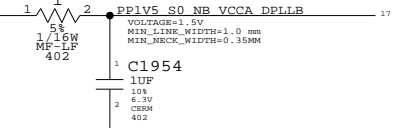
MCH DISPLAY PLL POWER LDO



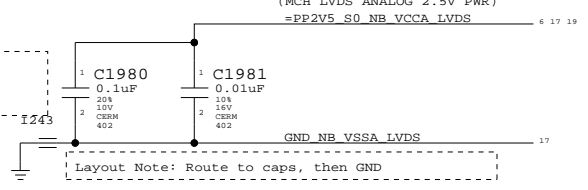
MCH VCCA_DPLL_A FILTER



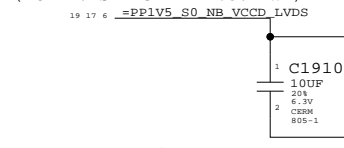
GMCH VCCA_DPLL_B FILTER



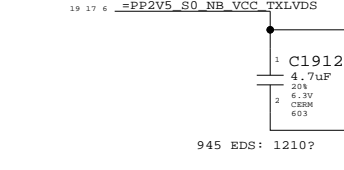
MCH VCCA_LVDS FILTER



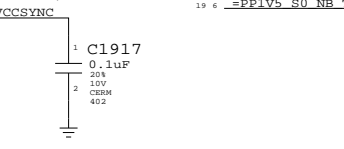
GMCH VCCD_LVDS BYPASS



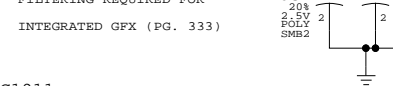
GMCH VCCD_LVDS BYPASS



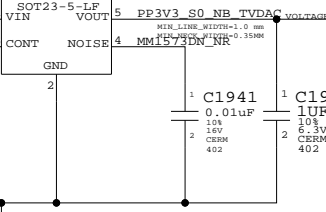
MCH VCCSYNC BYPASS



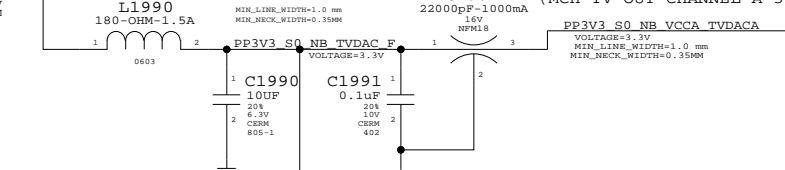
FILTERING REQUIRED FOR INTEGRATED GFX



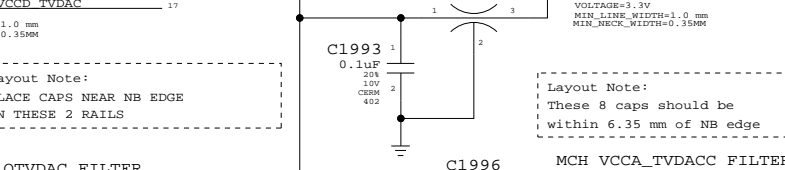
PP3V3_S0_NB_TVDAC



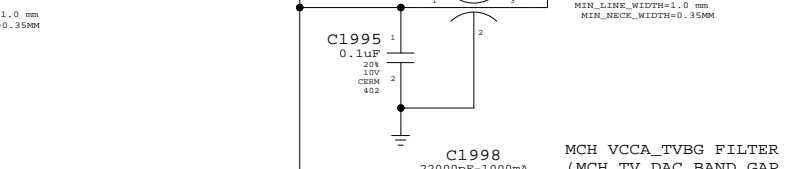
MCH VCCA_TVDACC FILTER



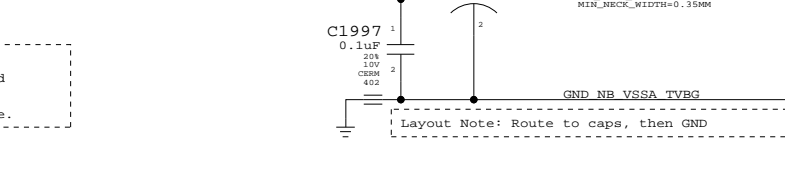
MCH VCCA_TVDACC FILTER



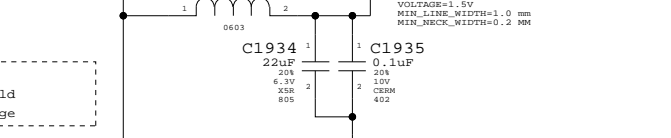
MCH VCCA_TVDACC FILTER



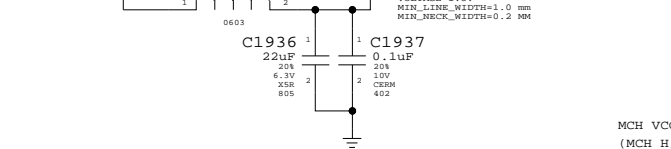
MCH VCCA_TVBG FILTER



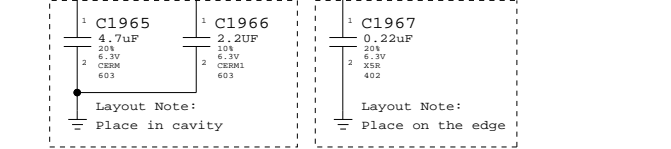
PP1V5_S0_NB_VTT



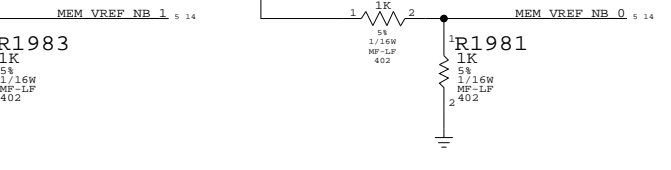
PP1V5_S0_NB_VCCA_HPLL



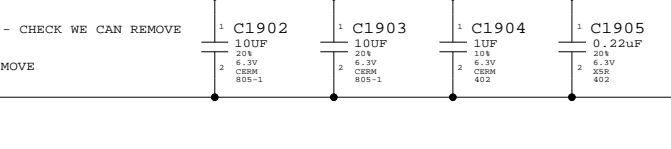
PP1V5_S0_NB_VTT



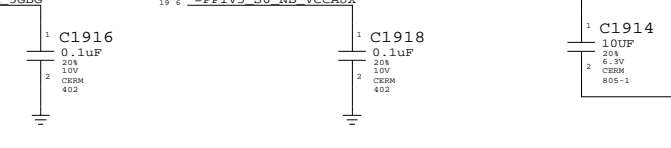
PP1V8_S3_MEM_NB



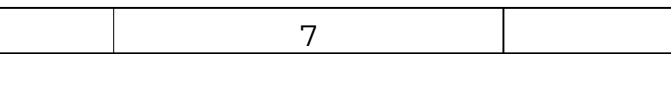
PPVCORE_S0_NB



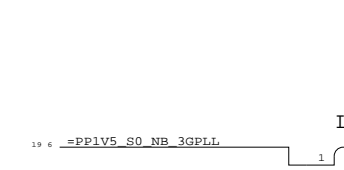
PP2V5_S0_NB_VCCA_3GBG



PP1V5_S0_NB_VCCAUX



PP1V5_S0_NB_VTT



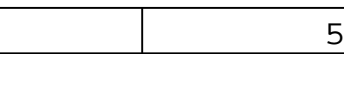
PP1V5_S0_NB_VTT



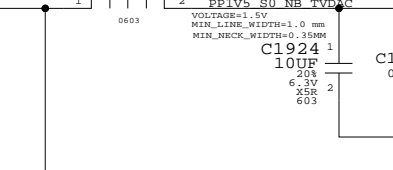
PP1V5_S0_NB_VTT



PP1V5_S0_NB_VTT



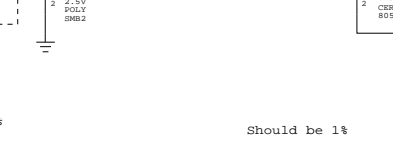
PP1V5_S0_NB_TVDAC



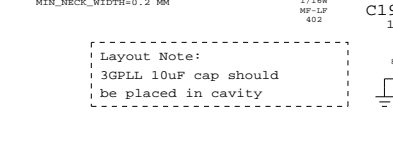
PP1V5_S0_NB_TVDAC



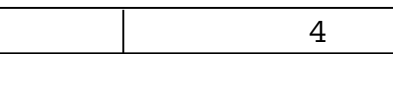
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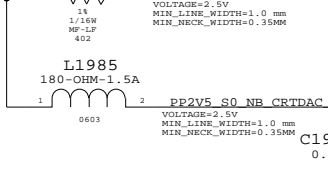
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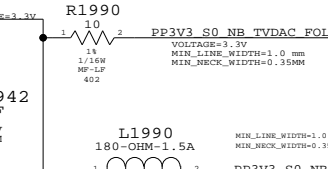
PP1V5_S0_NB_VTT



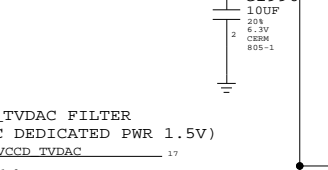
PP2V5_S0_NB_CRTDAC



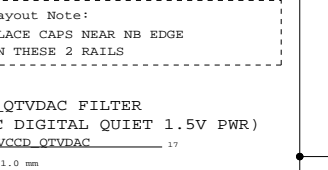
PP2V5_S0_NB_CRTDAC



PP2V5_S0_NB_CRTDAC



PP2V5_S0_NB_CRTDAC



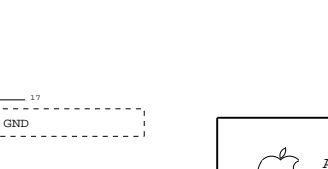
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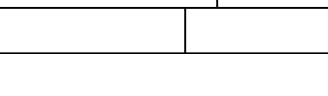
PP2V5_S0_NB_CRTDAC



PP2V5_S0_NB_CRTDAC



PP2V5_S0_NB_CRTDAC



NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

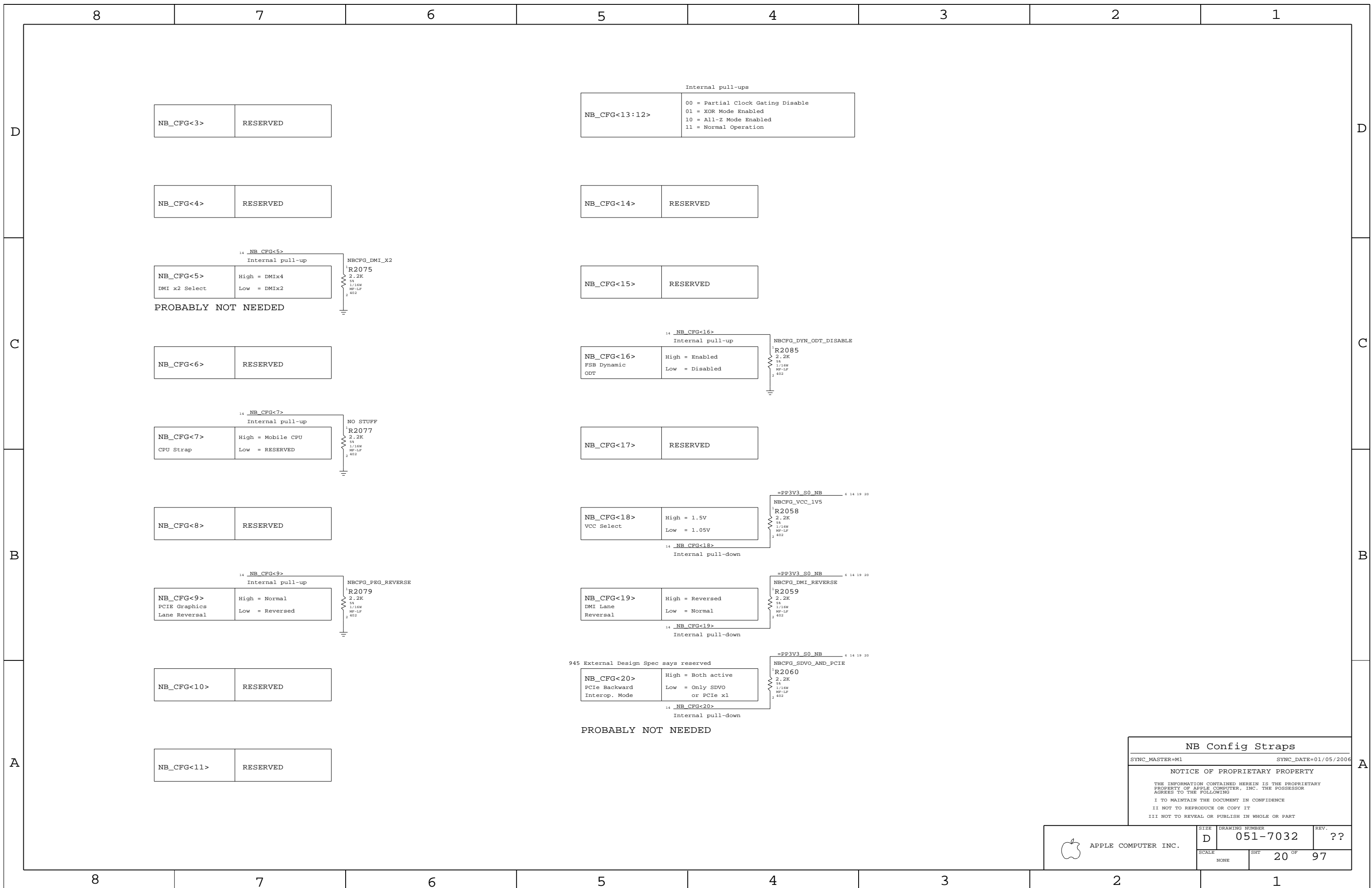
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D	051-7032	??
SCALE	SHT	
NONE	19 OF 97	



APPLE COMPUTER INC.



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB_CFG<5>
Internal pull-up

NB_CFG<5>	High = DMIx4 DMI x2 Select Low = DMIx2
-----------	--

PROBABLY NOT NEEDED

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LP
402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16>
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LP
402

14 NB_CFG<7>
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NO STUFF
R2077
2.2K
5%
1/16W
MF-LP
402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

=PP3V3_S0_NB 6 14 19 20
NBCFG_VCC_LV5
R2058
2.2K
5%
1/16W
MF-LP
402

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

14 NB_CFG<18>
Internal pull-down

14 NB_CFG<9>
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LP
402

=PP3V3_S0_NB 6 14 19 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LP
402

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

14 NB_CFG<19>
Internal pull-down

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved
=PP3V3_S0_NB 6 14 19 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LP
402

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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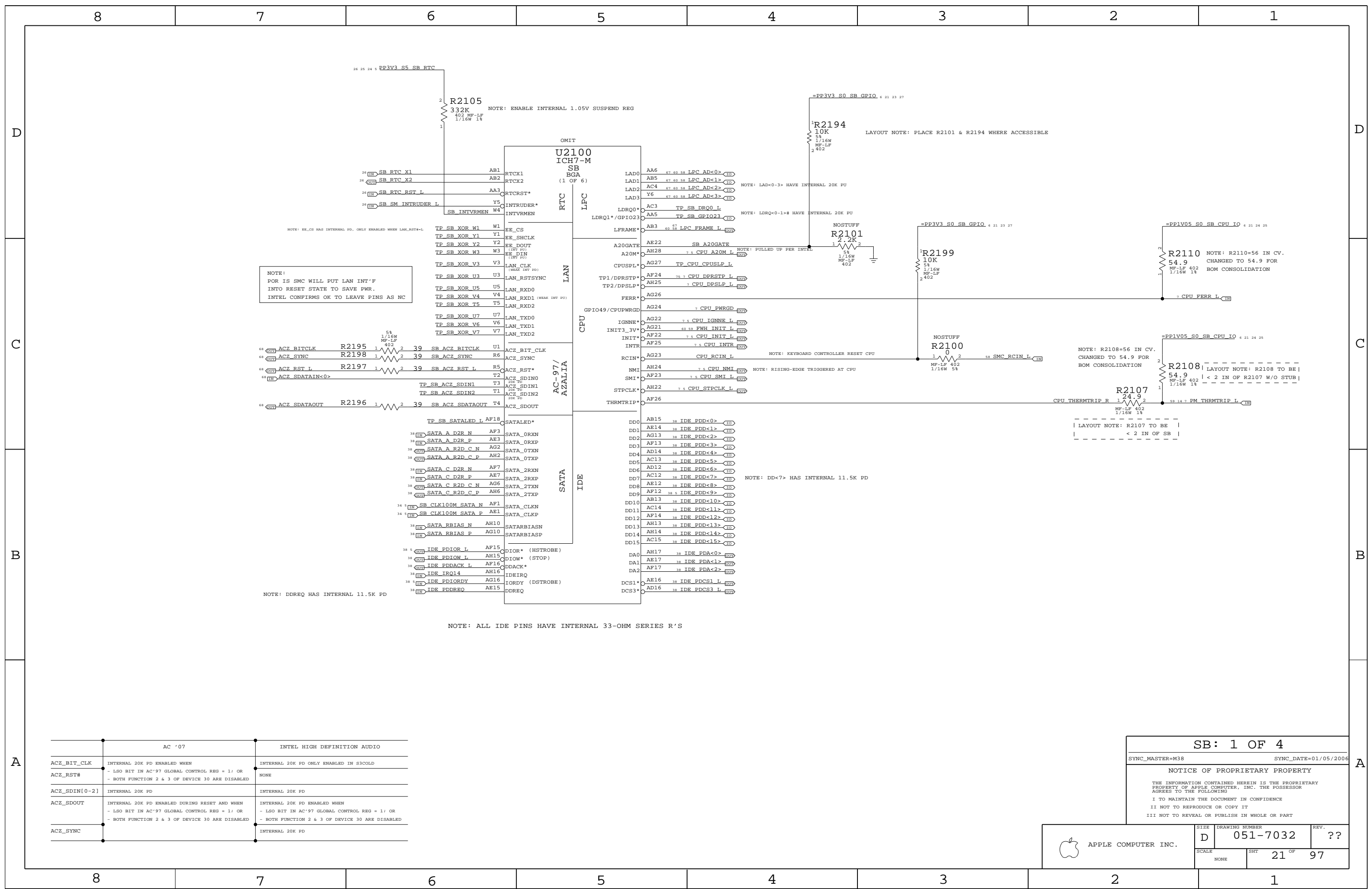
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	D	051-7032	??
SCALE	SHT	20 OF 97	
NONE			



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

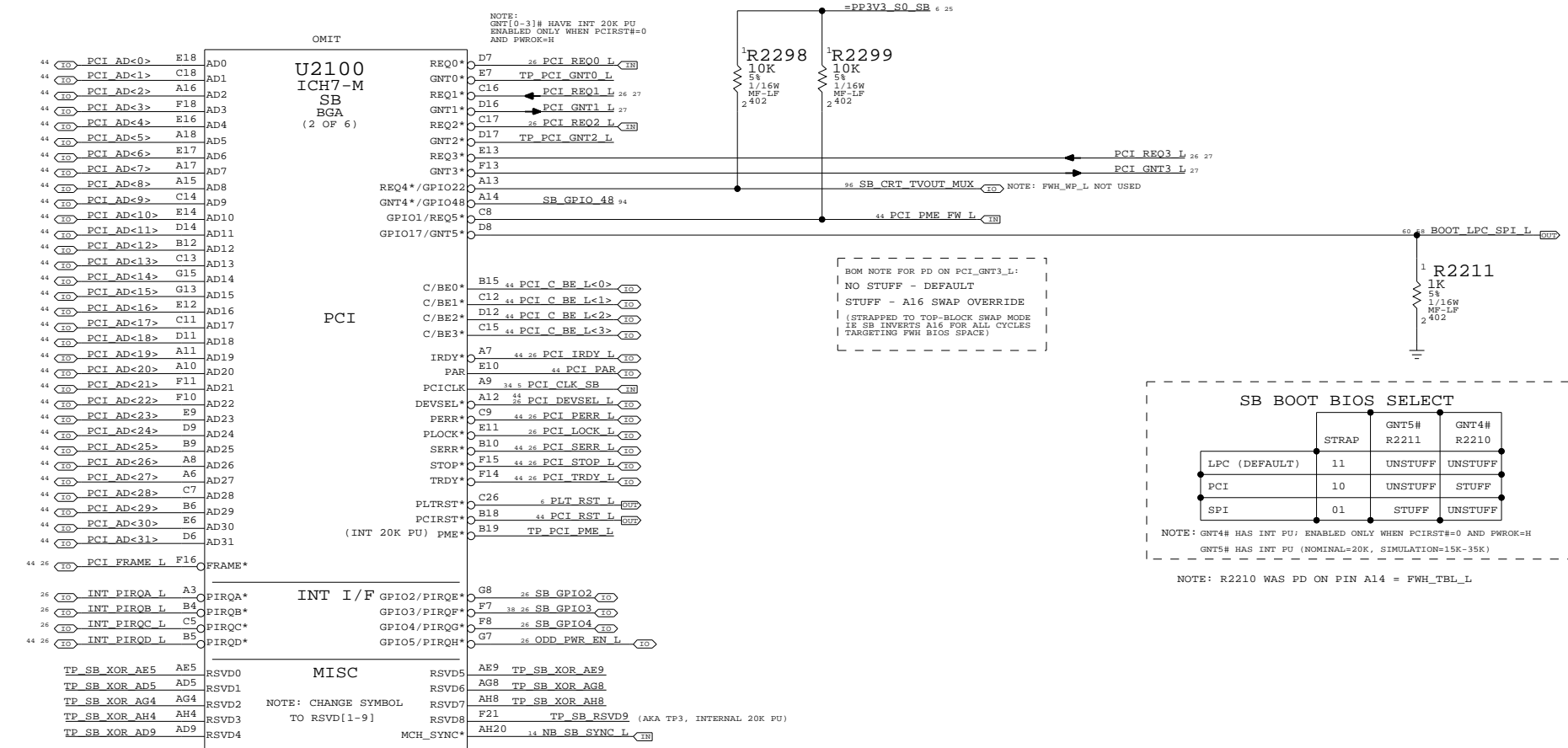
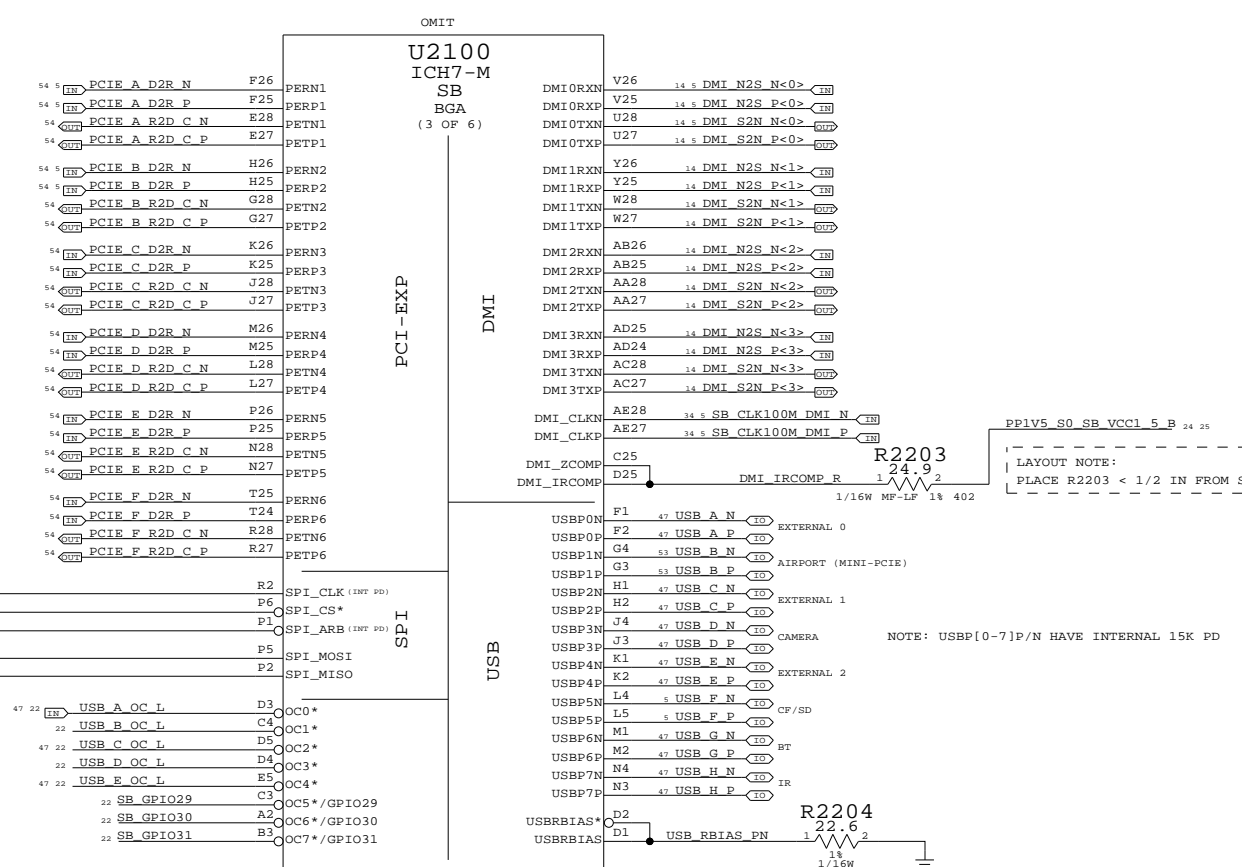
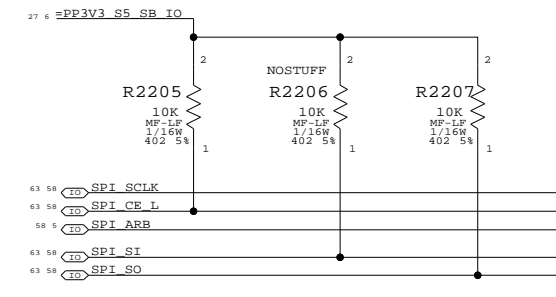
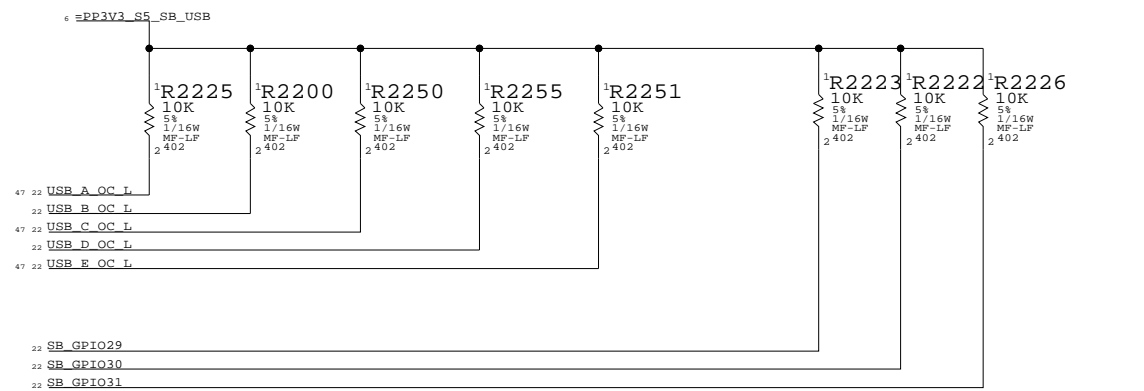
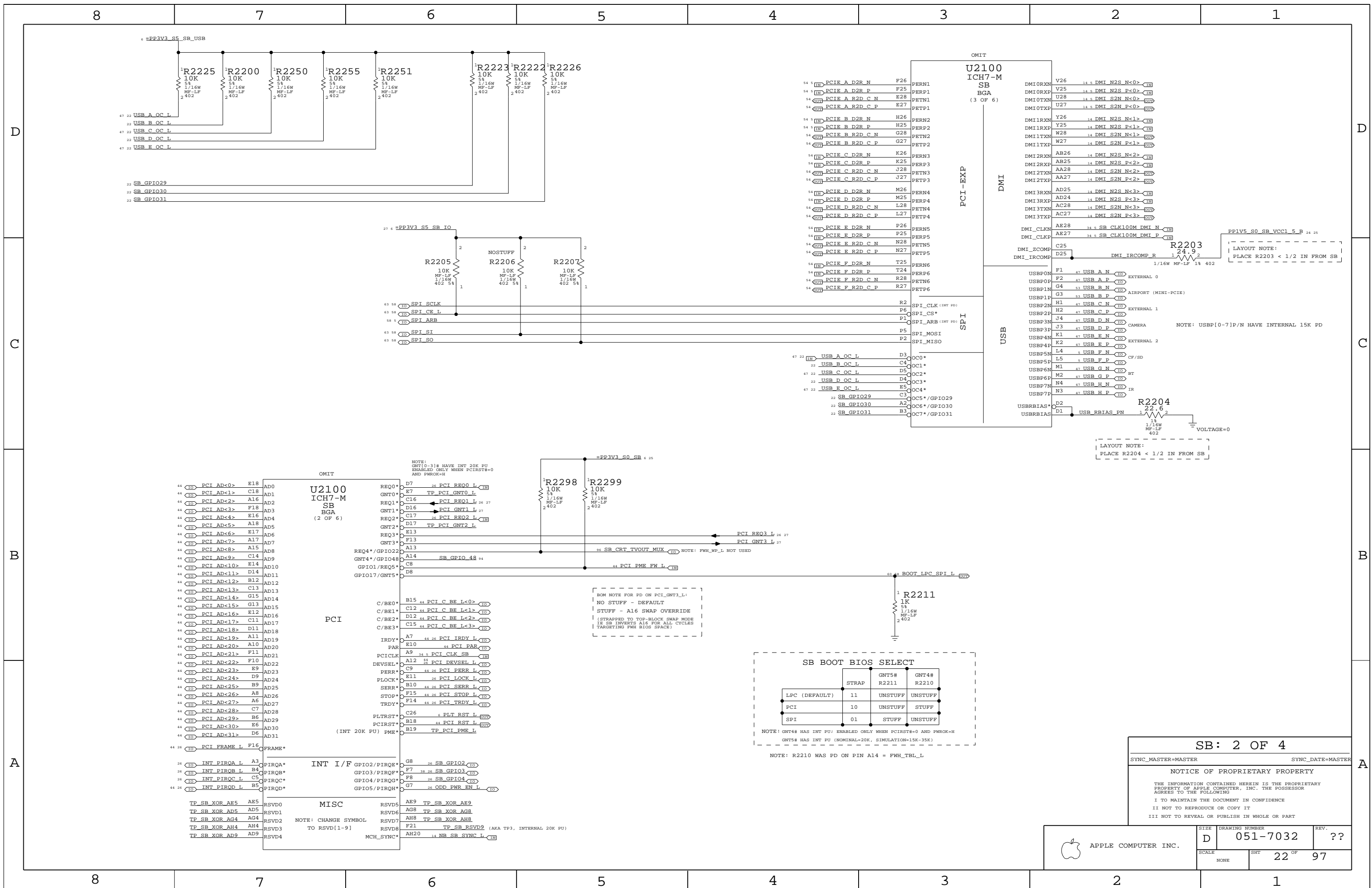
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7032	??
SCALE	SHT	21 OF 97	
NONE			



SB: 2 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

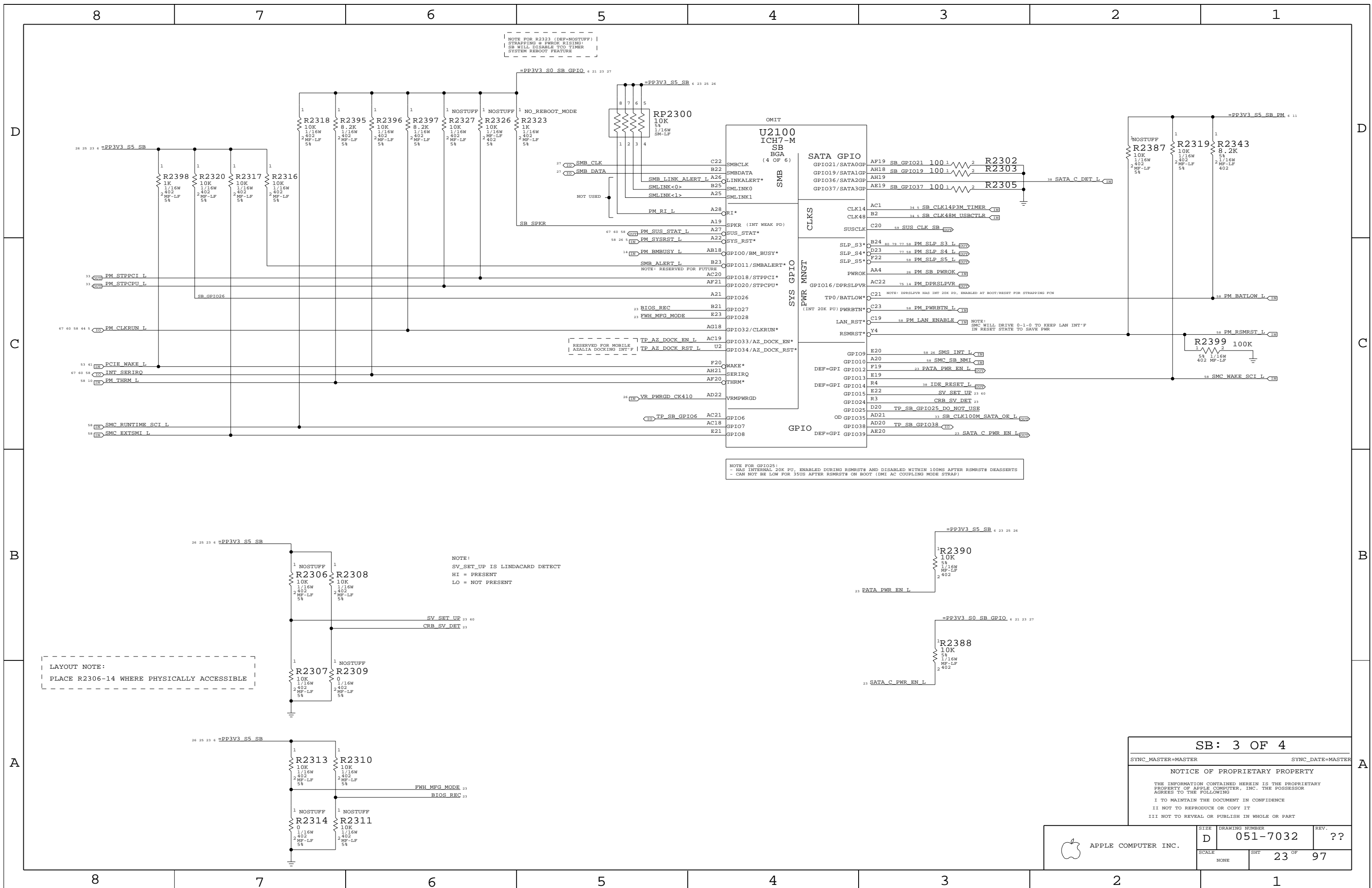
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NOTE FOR R2333 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TCO TIMER SYSTEM REBOOT FEATURE

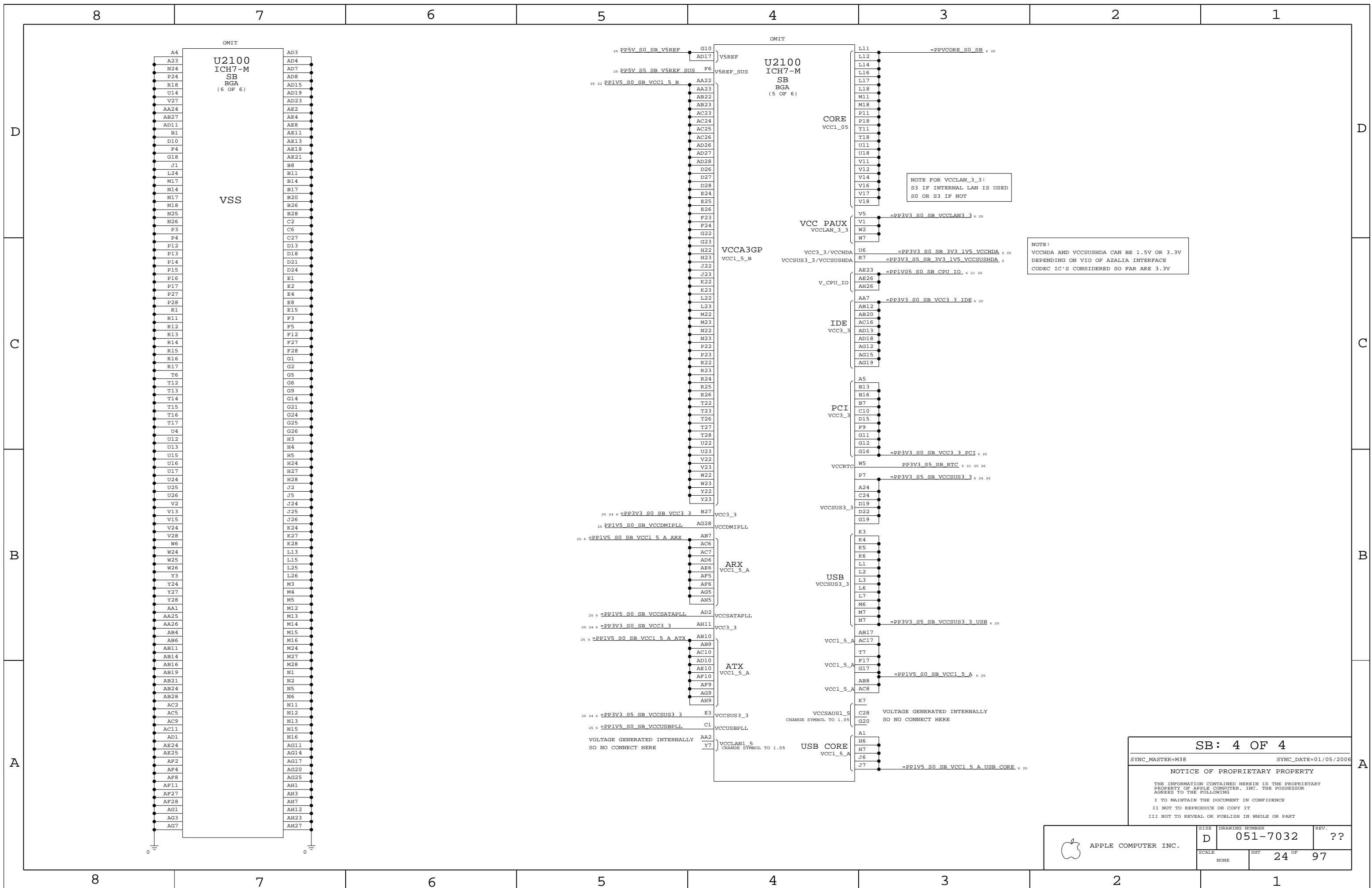
NOTE FOR GPIO25:
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

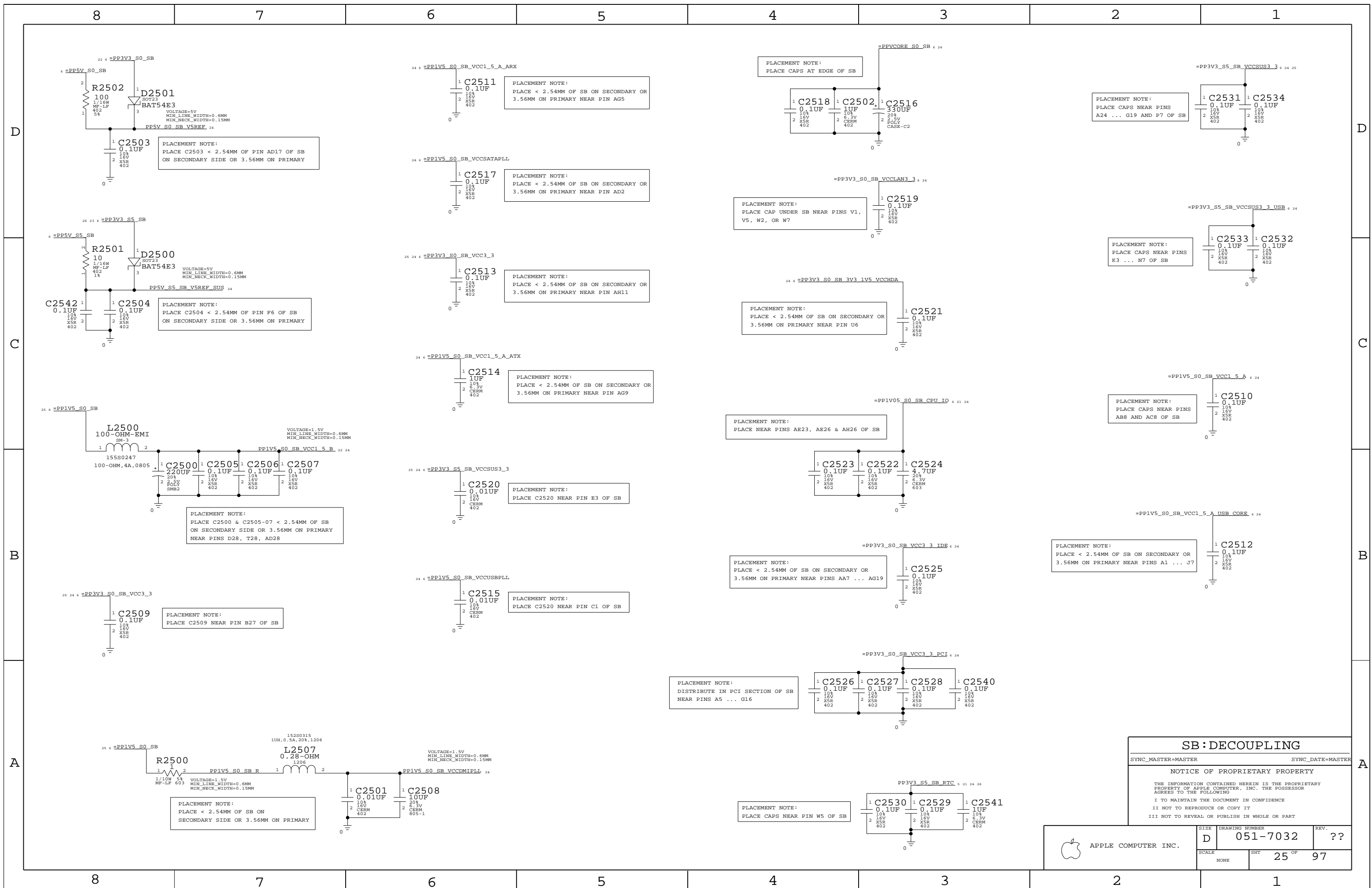
SB: 3 OF 4
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	??
SCALE	NONE	SHT	23 OF 97



SB: 4 OF 4
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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	D	051-7032	??
	SCALE NONE	SHT 24 OF 97	



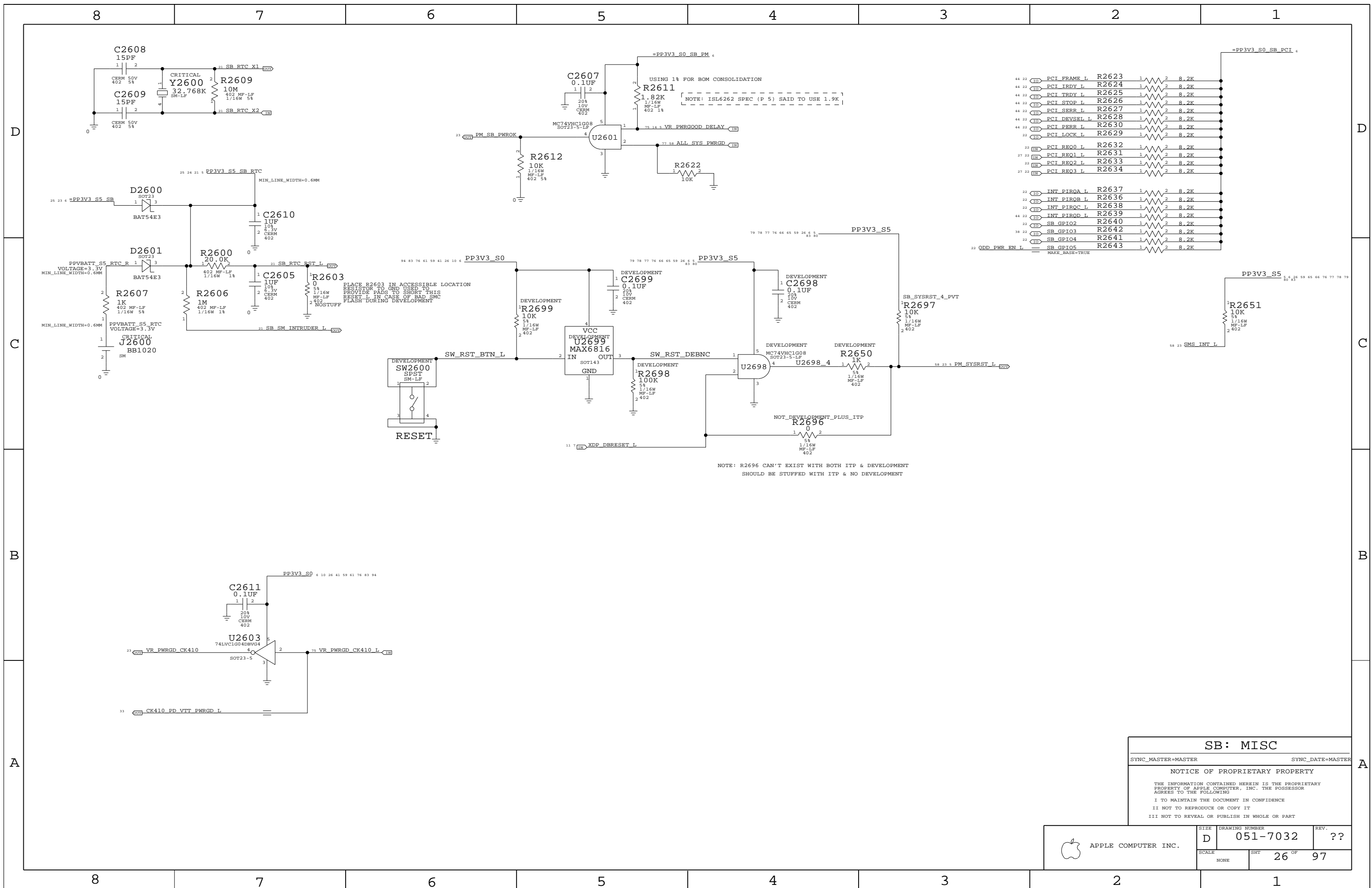
SB : DECOUPLING

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	25 OF	97
NONE			



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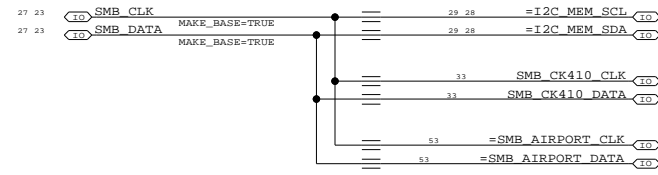
2

1

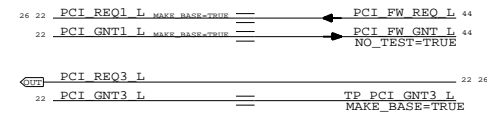
D

D

SB I2C BUSSES

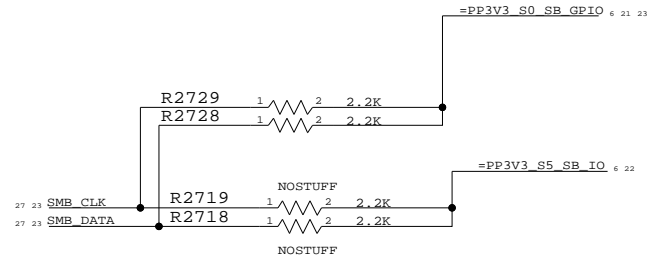


PCI CONTROL



C

C



B

B

A

A

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	??
SCALE	SHT	27 OF 97	
NONE			

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Page Notes

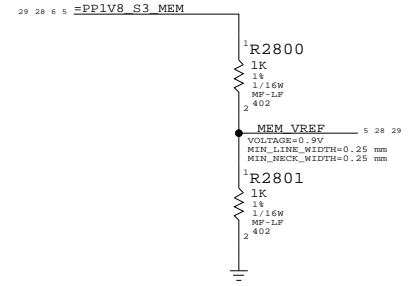
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

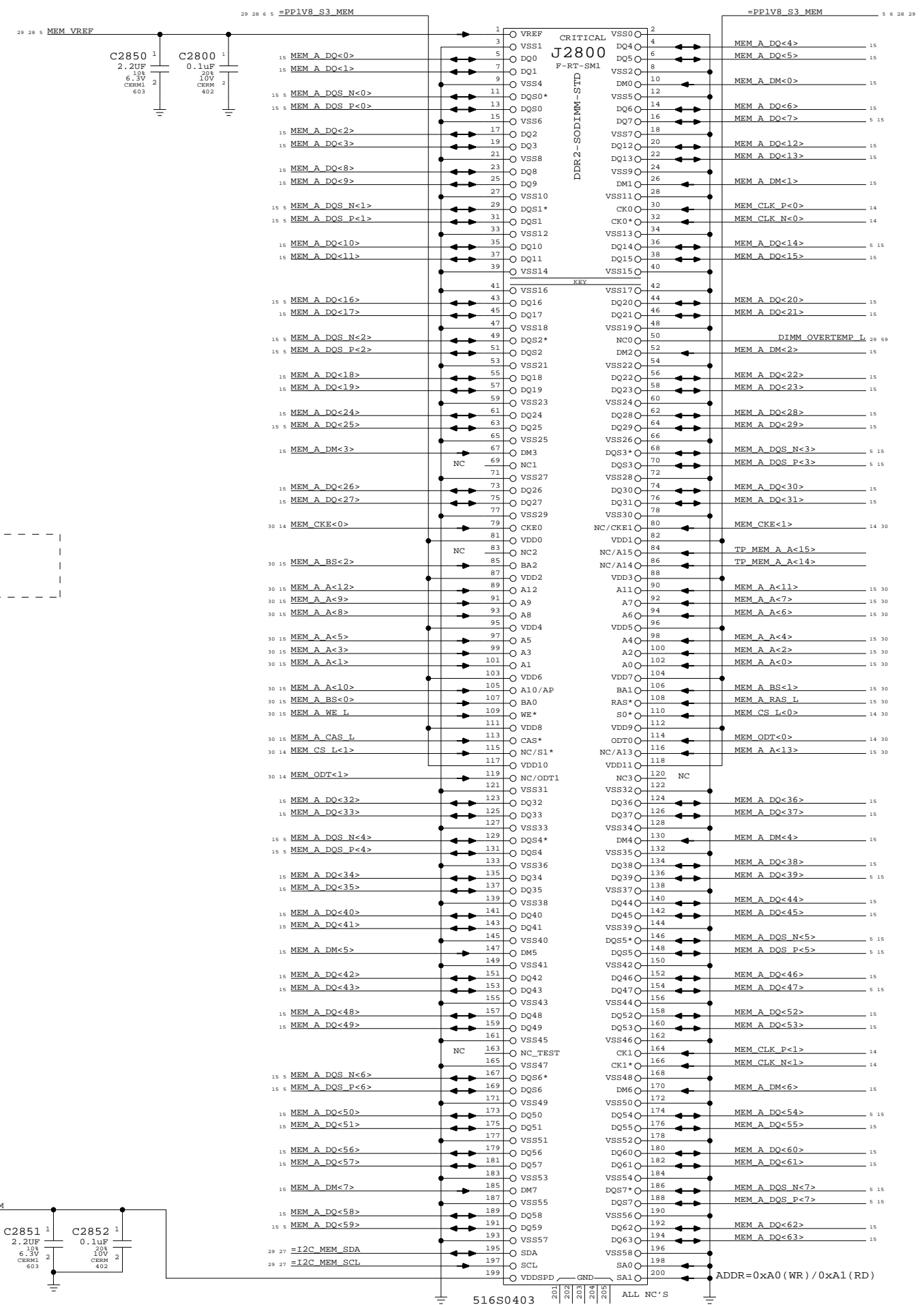
BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector

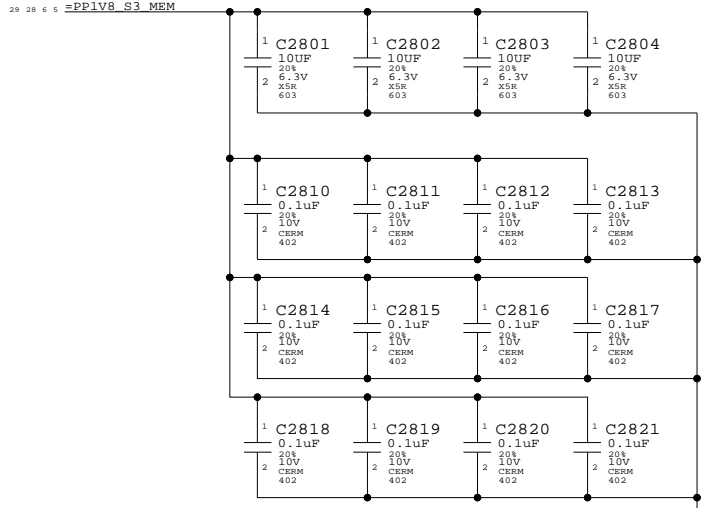


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
 (See Capell Valley pg 47)



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	??
SCALE	SHT	28 OF 97	
NONE			

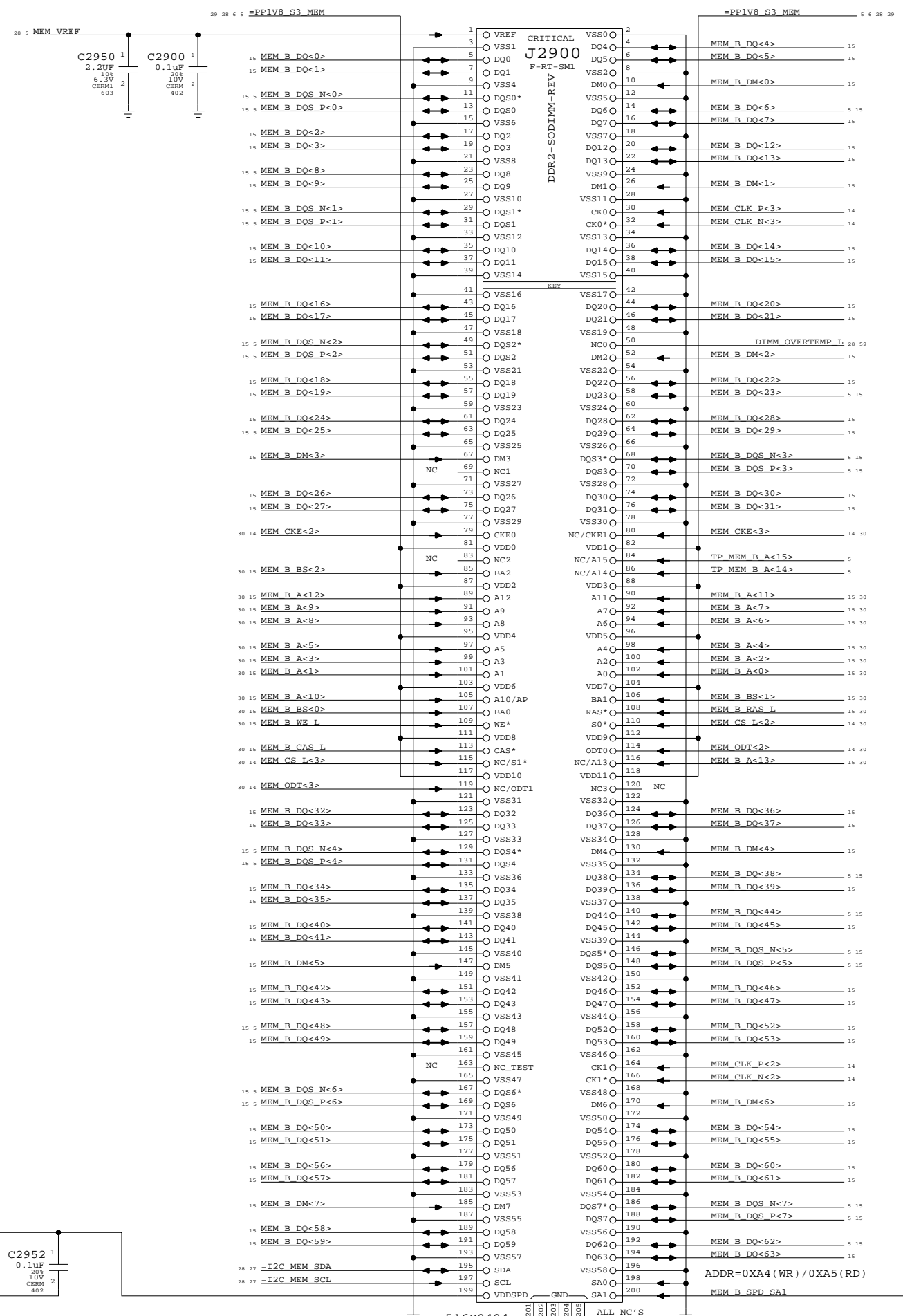
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

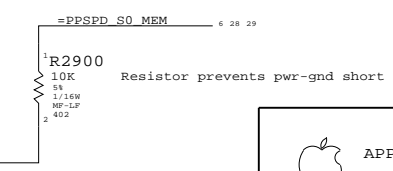
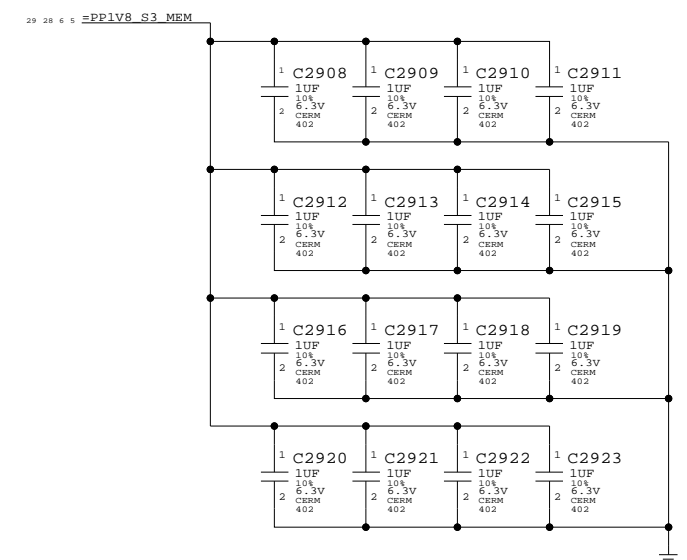
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	29 OF 97	
NONE			

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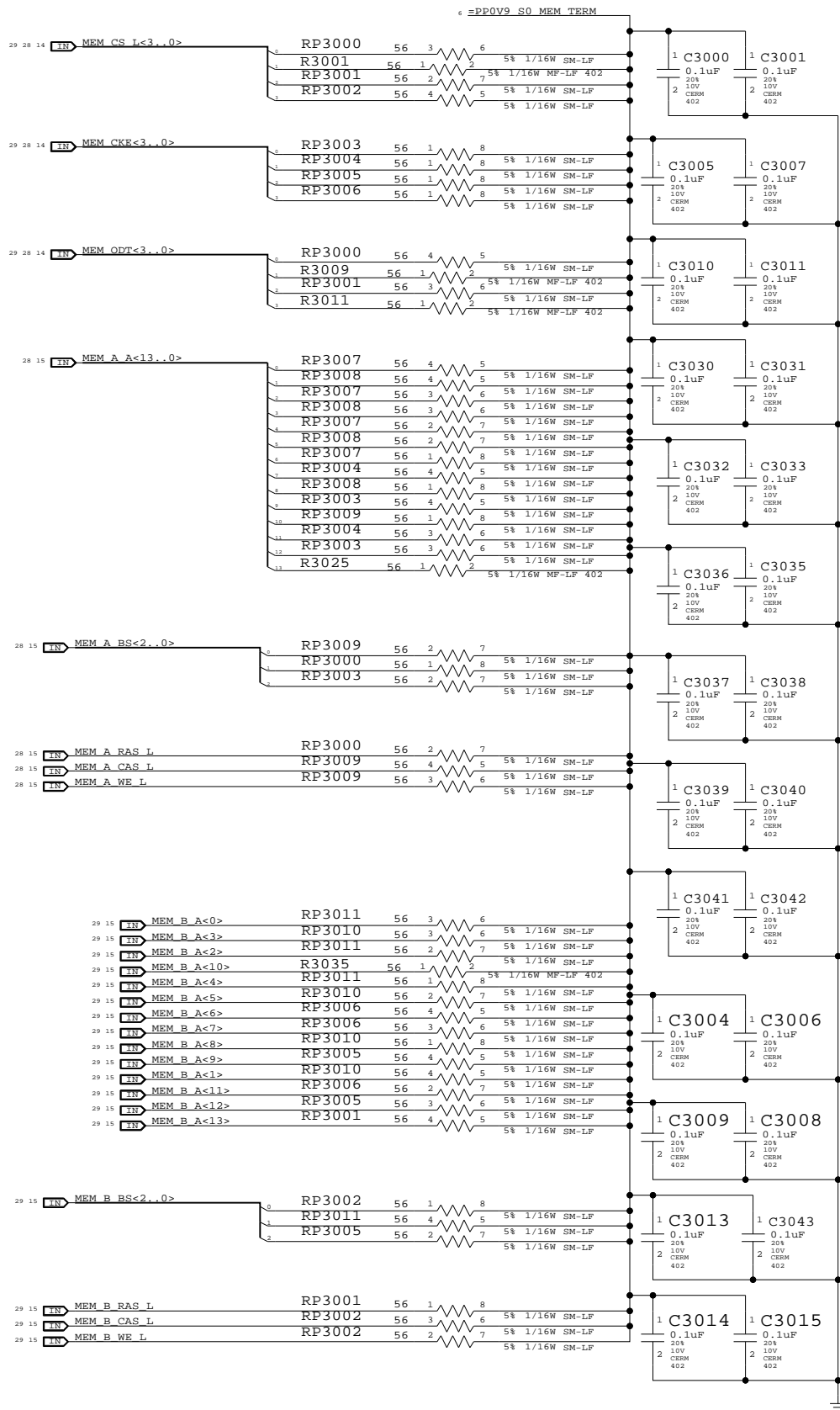
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One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



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Memory Active Termination

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	D	051-7032	??
SCALE	SHT	OF	
NONE	30	97	

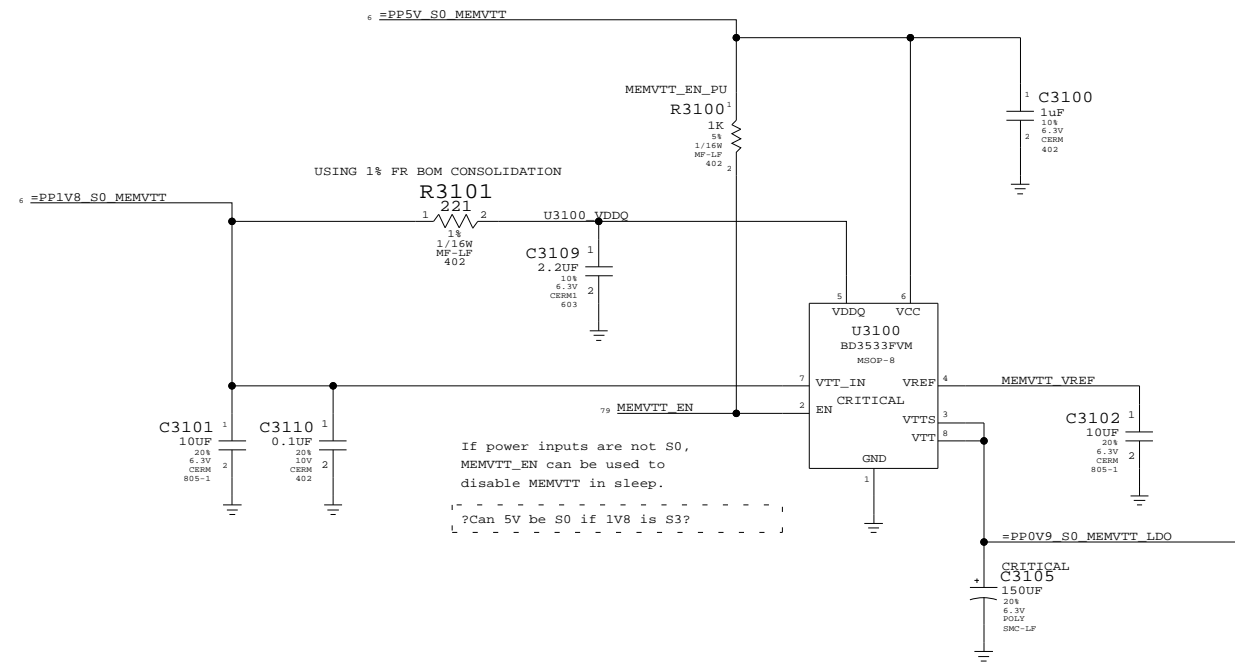
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

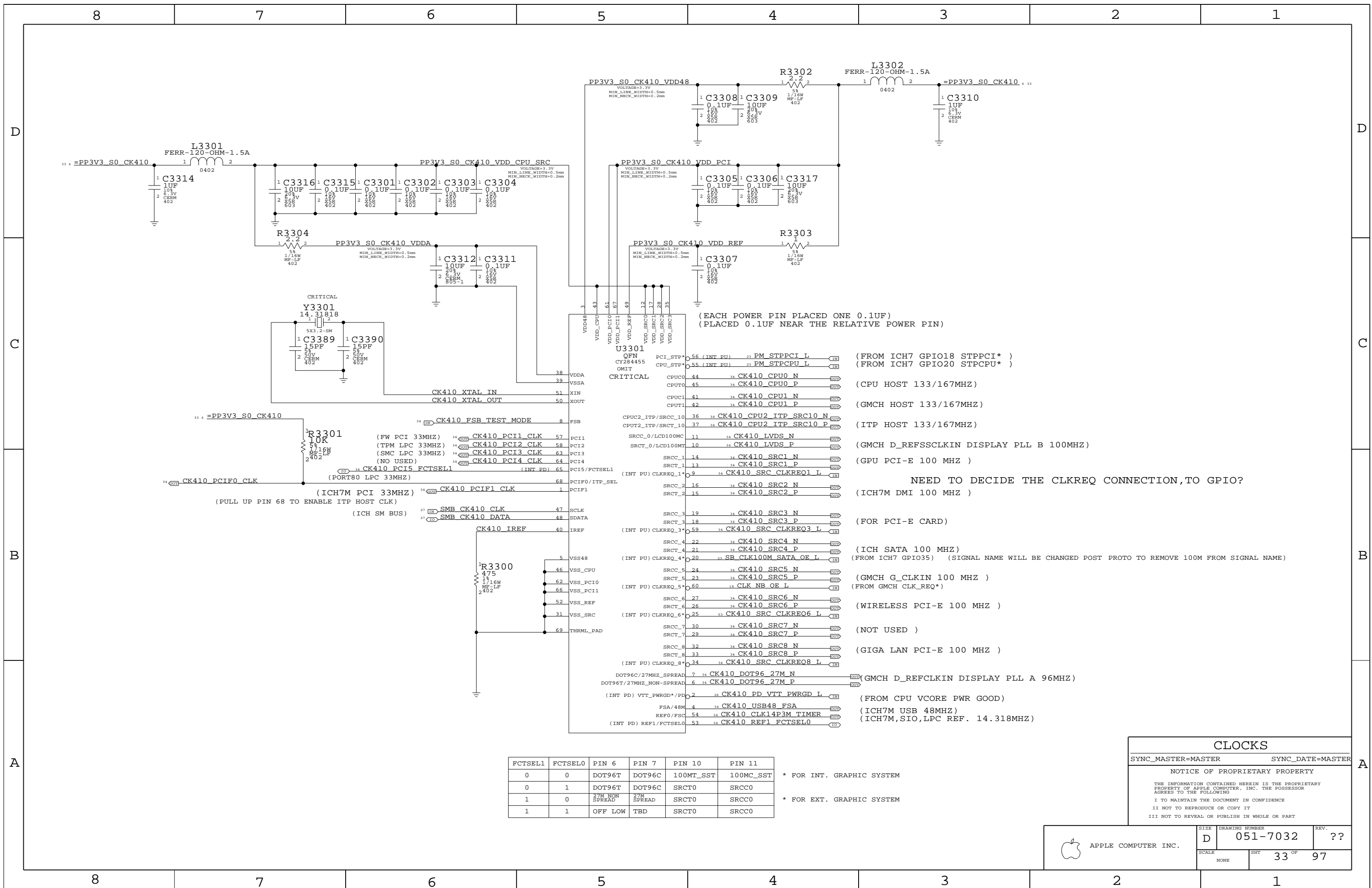
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	??
SCALE	SHT	31 OF 97	
NONE			



- (EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)
- U3301 QFN CY284455
 - PCI_STP* 56 (INT PU) 23 PM_STPPCI L (FROM ICH7 GPIO18 STPPCI*)
 - CPU_STP* 55 (INT PU) 23 PM_STPCPU L (FROM ICH7 GPIO20 STPCPU*)
 - CRITICAL
 - CPU0 44 34 CK410 CPU0 N (CPU HOST 133/167MHZ)
 - CPU0 45 34 CK410 CPU0 P
 - CPU1 41 34 CK410 CPU1 N (GMCH HOST 133/167MHZ)
 - CPU1 42 34 CK410 CPU1 P
 - CPUC2_ITP/SRCC_10 36 34 CK410 CPU2 ITP_SRC10_N (ITP HOST 133/167MHZ)
 - CPUT2_ITP/SRCC_10 37 34 CK410 CPU2 ITP_SRC10_P
 - SRCC_0/LCD100MC 11 34 CK410 LVDS N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
 - SRCT_0/LCD100MT 10 34 CK410 LVDS P
 - SRCC_1 14 34 CK410 SRC1 N (GPU PCI-E 100 MHZ)
 - SRCT_1 13 34 CK410 SRC1 P
 - (INT PU) CLKREQ_1* 9 34 CK410 SRC CLKREQ1 L NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?
 - SRCC_2 16 34 CK410 SRC2 N (ICH7M DMI 100 MHZ)
 - SRCT_2 15 34 CK410 SRC2 P
 - SRCC_3 19 34 CK410 SRC3 N (FOR PCI-E CARD)
 - SRCT_3 18 34 CK410 SRC3 P
 - (INT PU) CLKREQ_3* 59 34 CK410 SRC CLKREQ3 L
 - SRCC_4 22 34 CK410 SRC4 N (ICH SATA 100 MHZ)
 - SRCT_4 21 34 CK410 SRC4 P (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
 - (INT PU) CLKREQ_4* 20 34 SB_CLK100M_SATA_OE L
 - SRCC_5 24 34 CK410 SRC5 N (GMCH G_CLKIN 100 MHZ)
 - SRCT_5 23 34 CK410 SRC5 P (FROM GMCH CLK_REQ*)
 - (INT PU) CLKREQ_5* 60 34 CLK_NB_OE L
 - SRCC_6 27 34 CK410 SRC6 N (WIRELESS PCI-E 100 MHZ)
 - SRCT_6 26 34 CK410 SRC6 P
 - (INT PU) CLKREQ_6* 25 34 CK410 SRC CLKREQ6 L
 - SRCC_7 30 34 CK410 SRC7 N (NOT USED)
 - SRCT_7 29 34 CK410 SRC7 P
 - SRCC_8 32 34 CK410 SRC8 N (GIGA LAN PCI-E 100 MHZ)
 - SRCT_8 33 34 CK410 SRC8 P
 - (INT PU) CLKREQ_8* 34 34 CK410 SRC CLKREQ8 L
 - DOT96C/27MHZ_SPREAD 7 34 CK410 DOT96 27M N (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
 - DOT96T/27MHZ_NON-SPREAD 6 34 CK410 DOT96 27M P
 - (INT PD) VTT_PWRGD*/PD 2 34 CK410 PD VTT_PWRGD L (FROM CPU VCORE PWR GOOD)
 - FSA/48M 4 34 CK410 USB48 FSA (ICH7M USB 48MHZ)
 - REF0/FSC 54 34 CK410 CLK14P3M_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
 - (INT PD) REF1/FCTSEL0 53 34 CK410 REF1_FCTSEL0

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

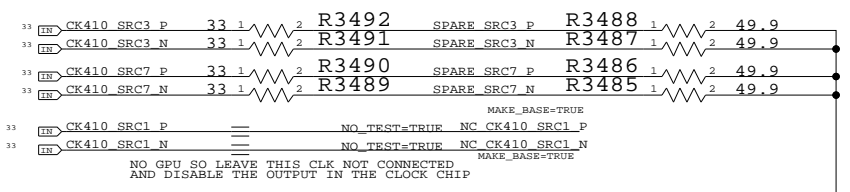
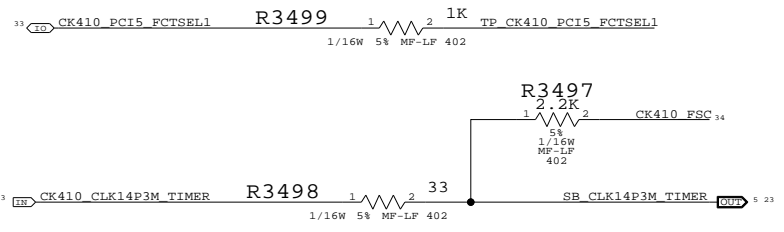
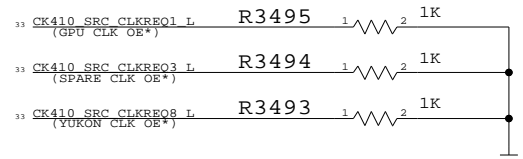
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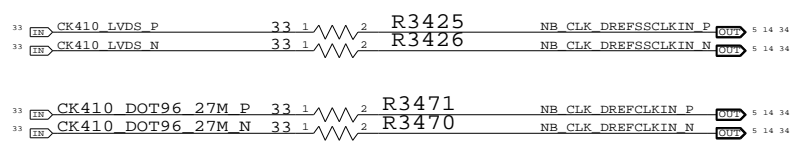
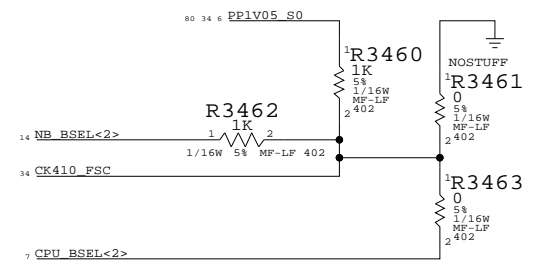
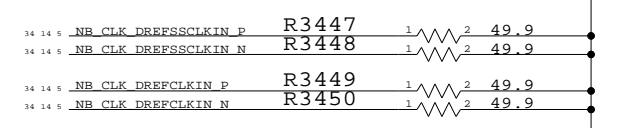
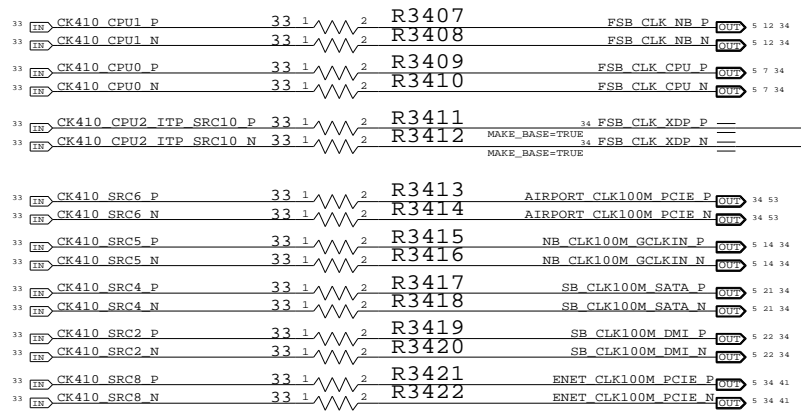
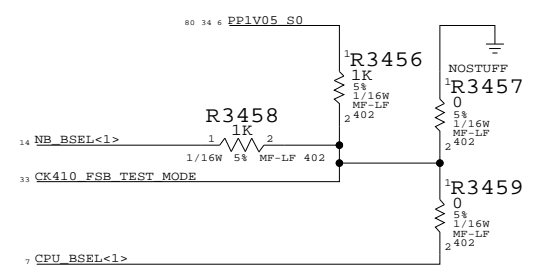
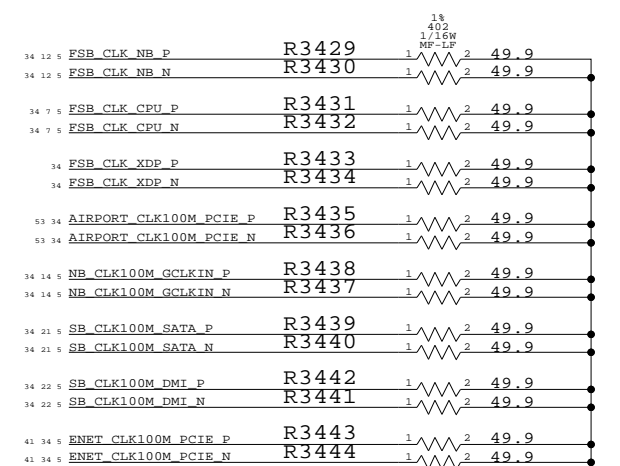
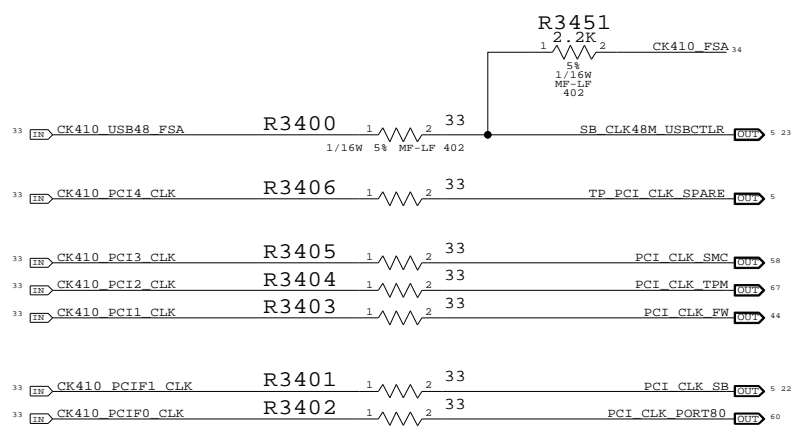
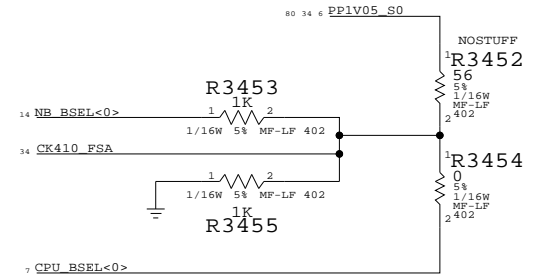
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	33 OF 97	
NONE			

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457 R3458
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458



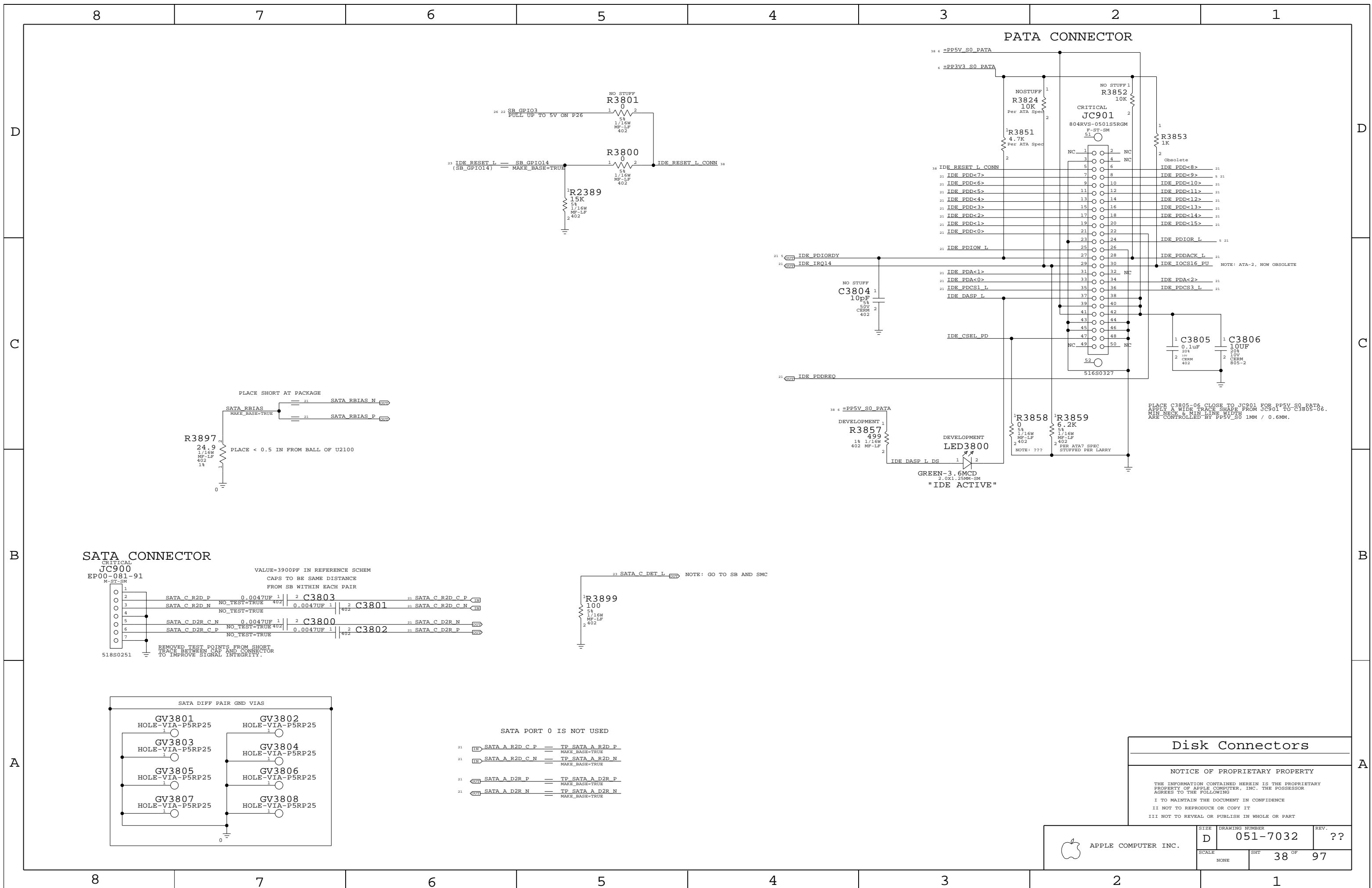
CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

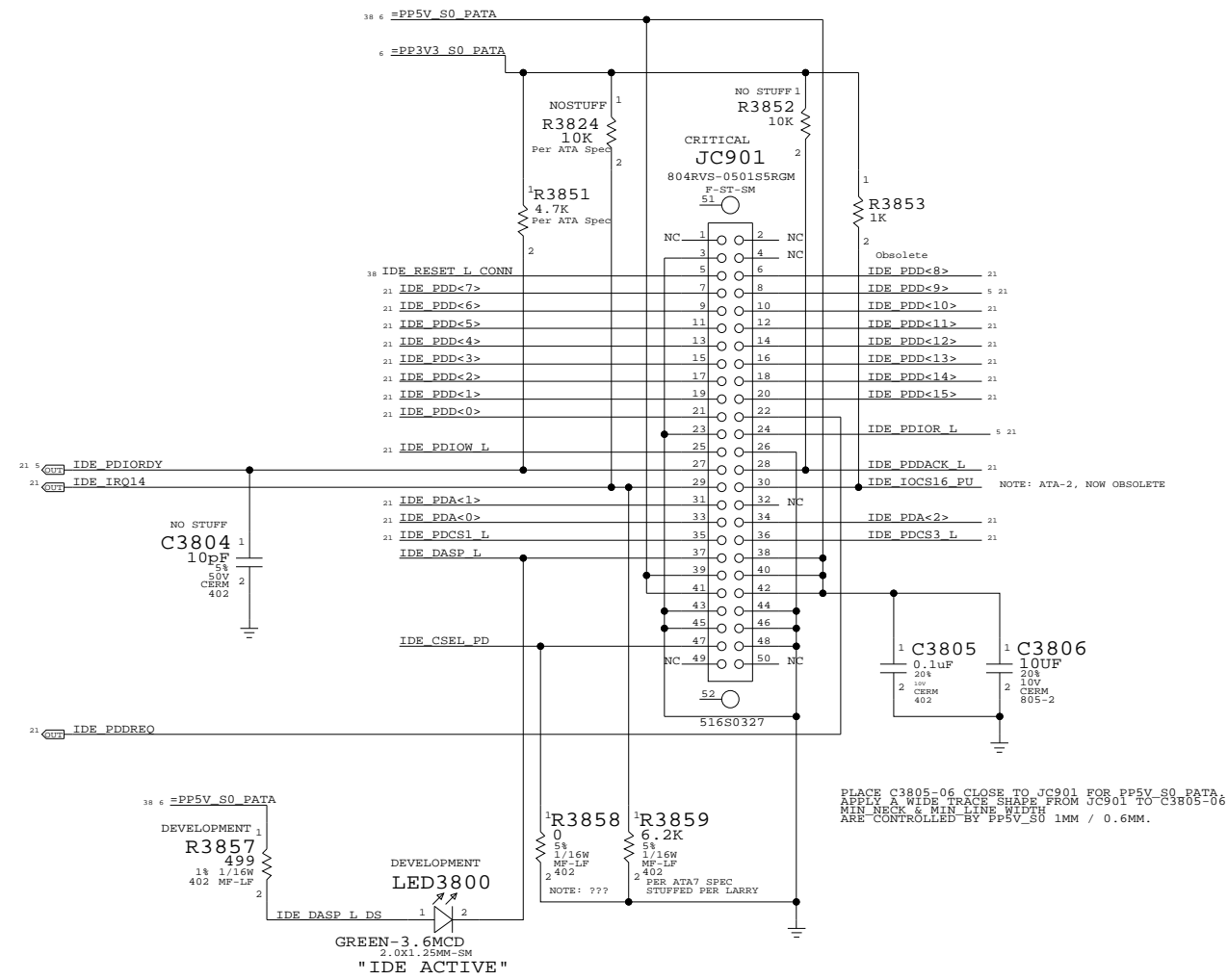
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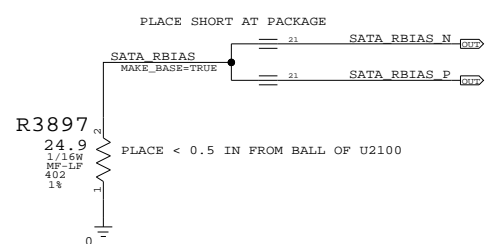
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	34 OF	97
NONE			



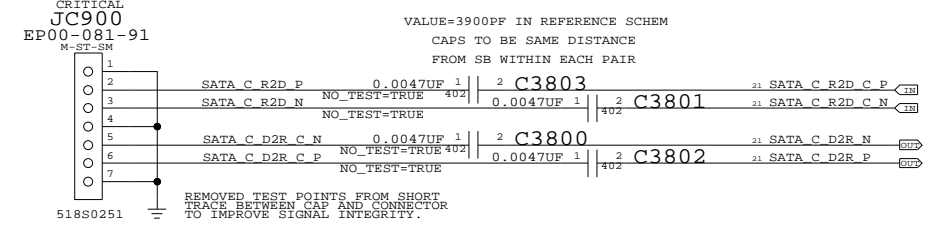
PATA CONNECTOR



PLACE C3805-06 CLOSE TO JC901 FOR PP5V_S0_PATA. APPLY A WIDE TRACE SHADE FROM JC901 TO C3805-06. MIN NECK & MIN LINE WIDTHS ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.

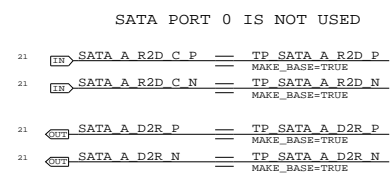
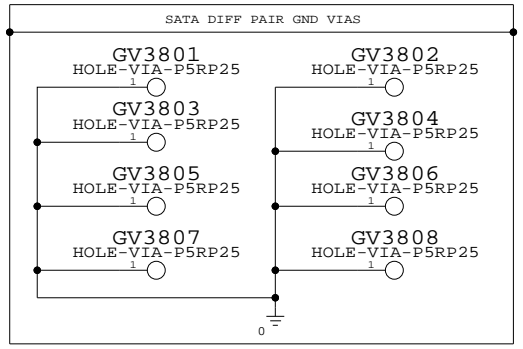
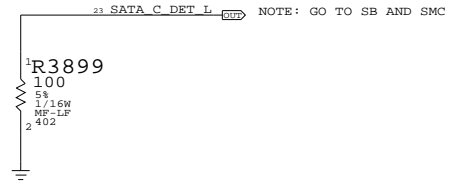


SATA CONNECTOR



VALUE=3900PF IN REFERENCE SCHEM CAPS TO BE SAME DISTANCE FROM SB WITHIN EACH PAIR

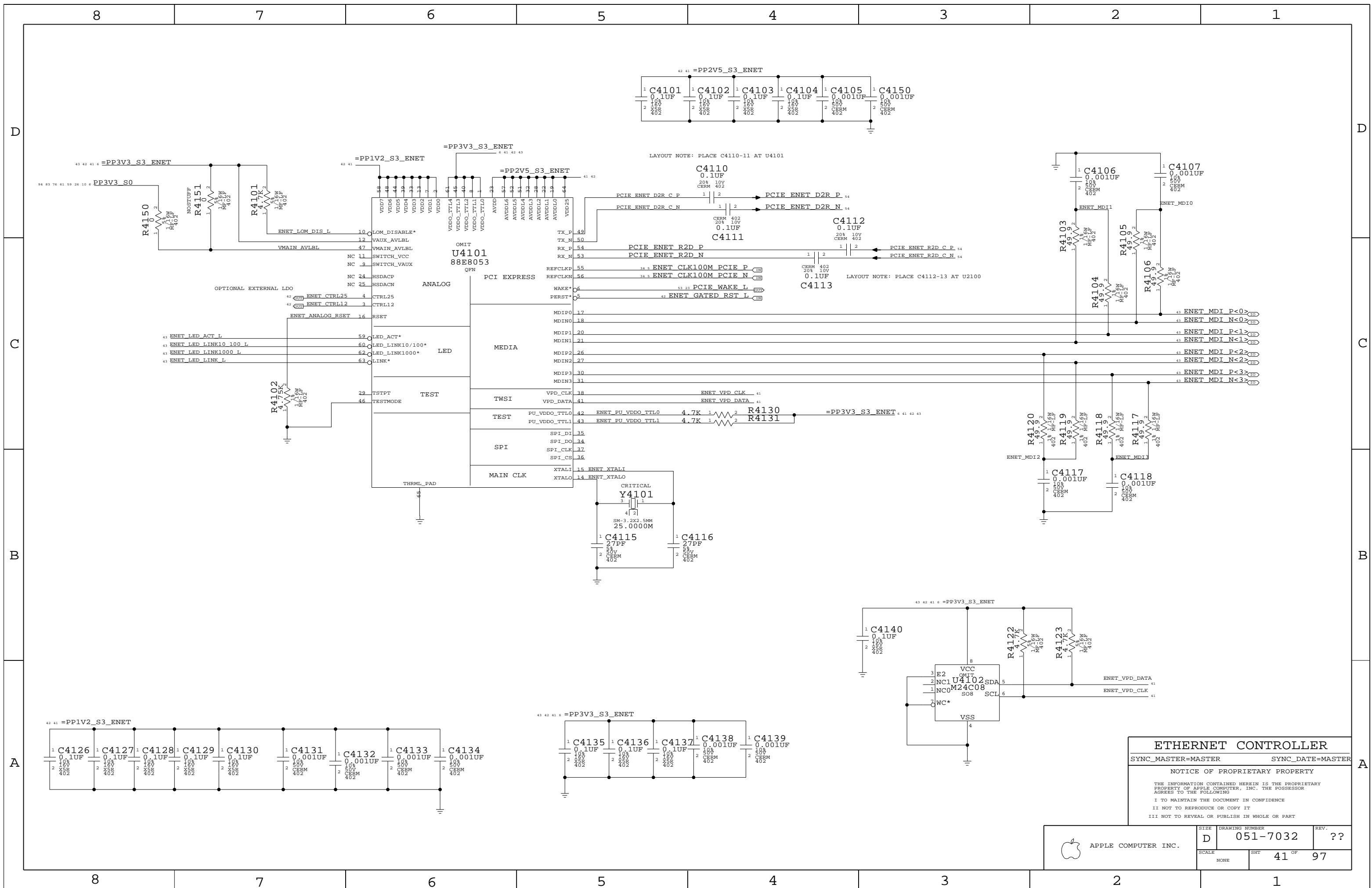
REMOVED TEST POINTS FROM SHORT TRACE BETWEEN CAP AND CONNECTOR TO IMPROVE SIGNAL INTEGRITY.



Disk Connectors

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	38 OF 97	
NONE			



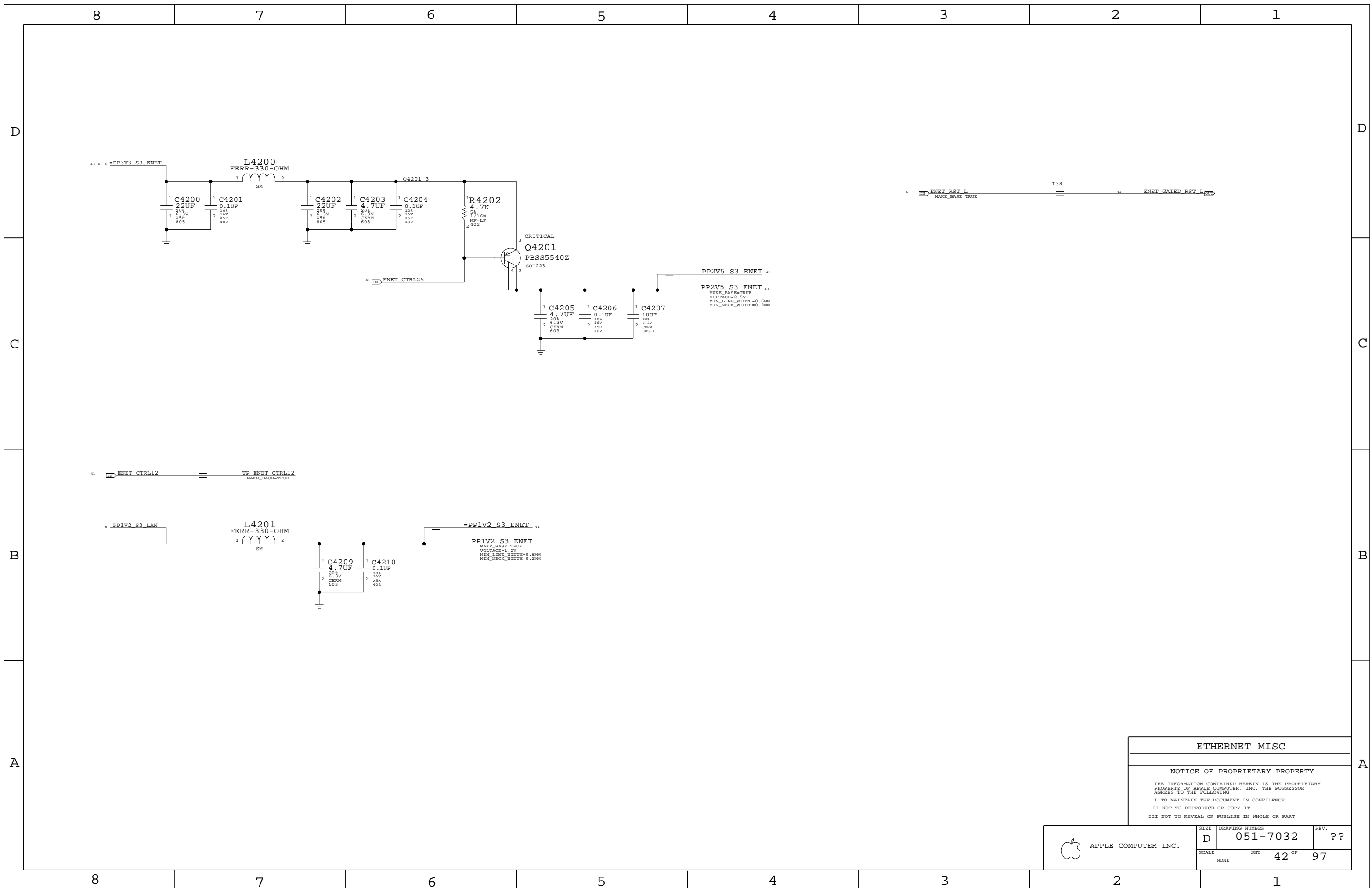
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

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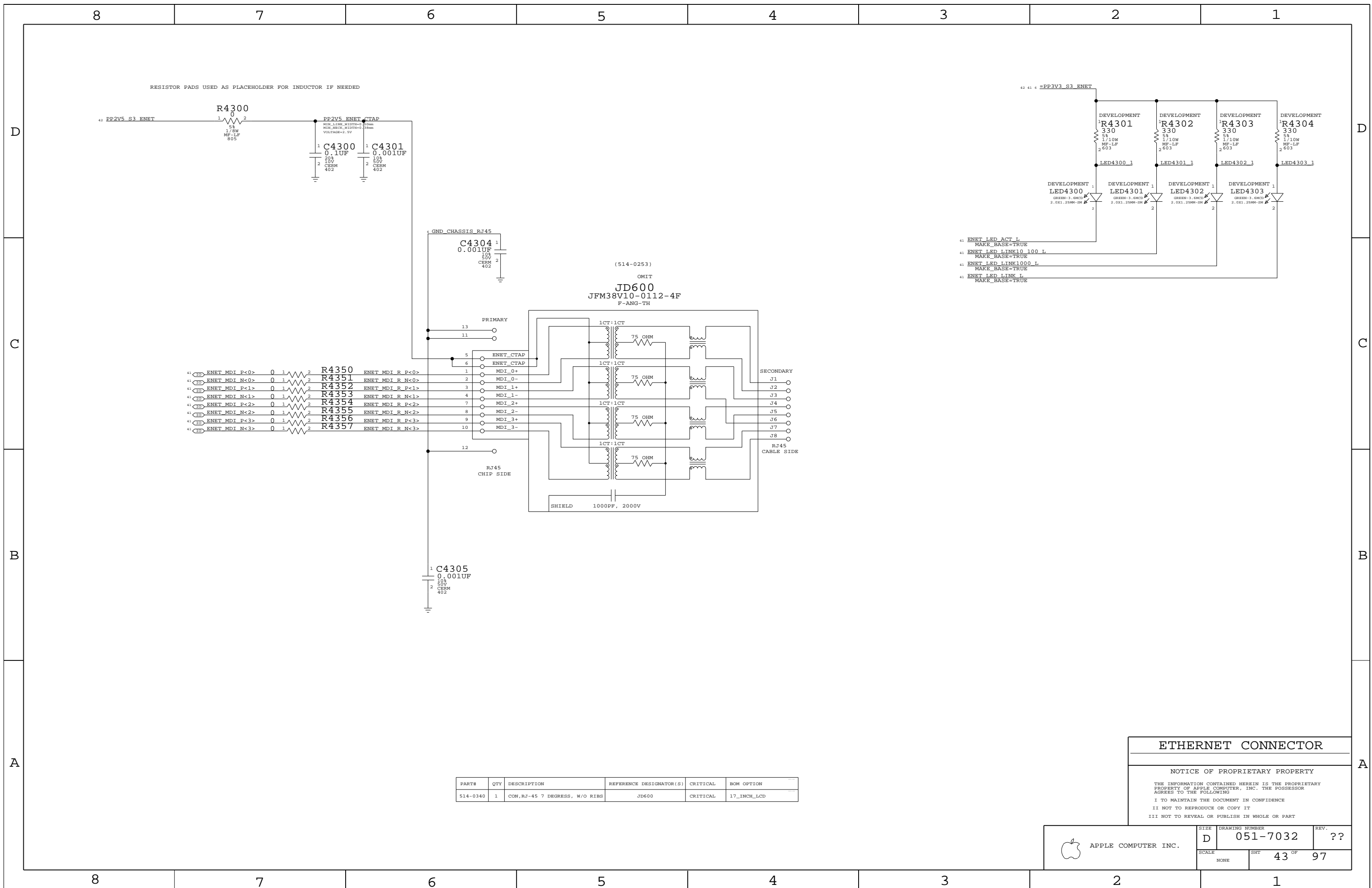
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 42 OF 97	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED

42 41 6 =PP3V3_S3_ENET

ENET MDI P<0>	0	1	2	R4350	ENET MDI R P<0>
ENET MDI N<0>	0	1	2	R4351	ENET MDI R N<0>
ENET MDI P<1>	0	1	2	R4352	ENET MDI R P<1>
ENET MDI N<1>	0	1	2	R4353	ENET MDI R N<1>
ENET MDI P<2>	0	1	2	R4354	ENET MDI R P<2>
ENET MDI N<2>	0	1	2	R4355	ENET MDI R N<2>
ENET MDI P<3>	0	1	2	R4356	ENET MDI R P<3>
ENET MDI N<3>	0	1	2	R4357	ENET MDI R N<3>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0340	1	CON,RJ-45 7 DEGRESS, W/O RIBS	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

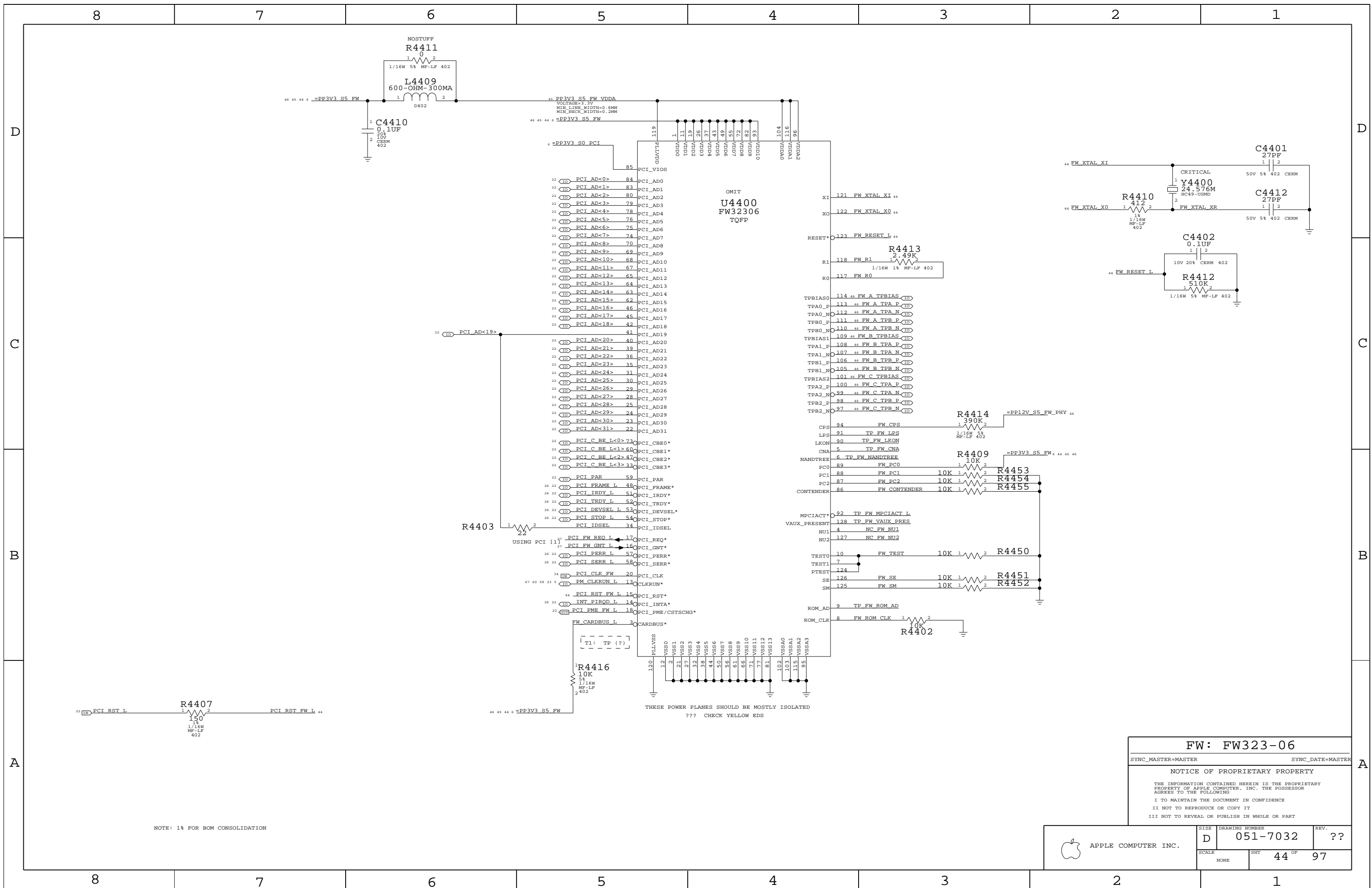
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	43 OF 97	
NONE			



NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

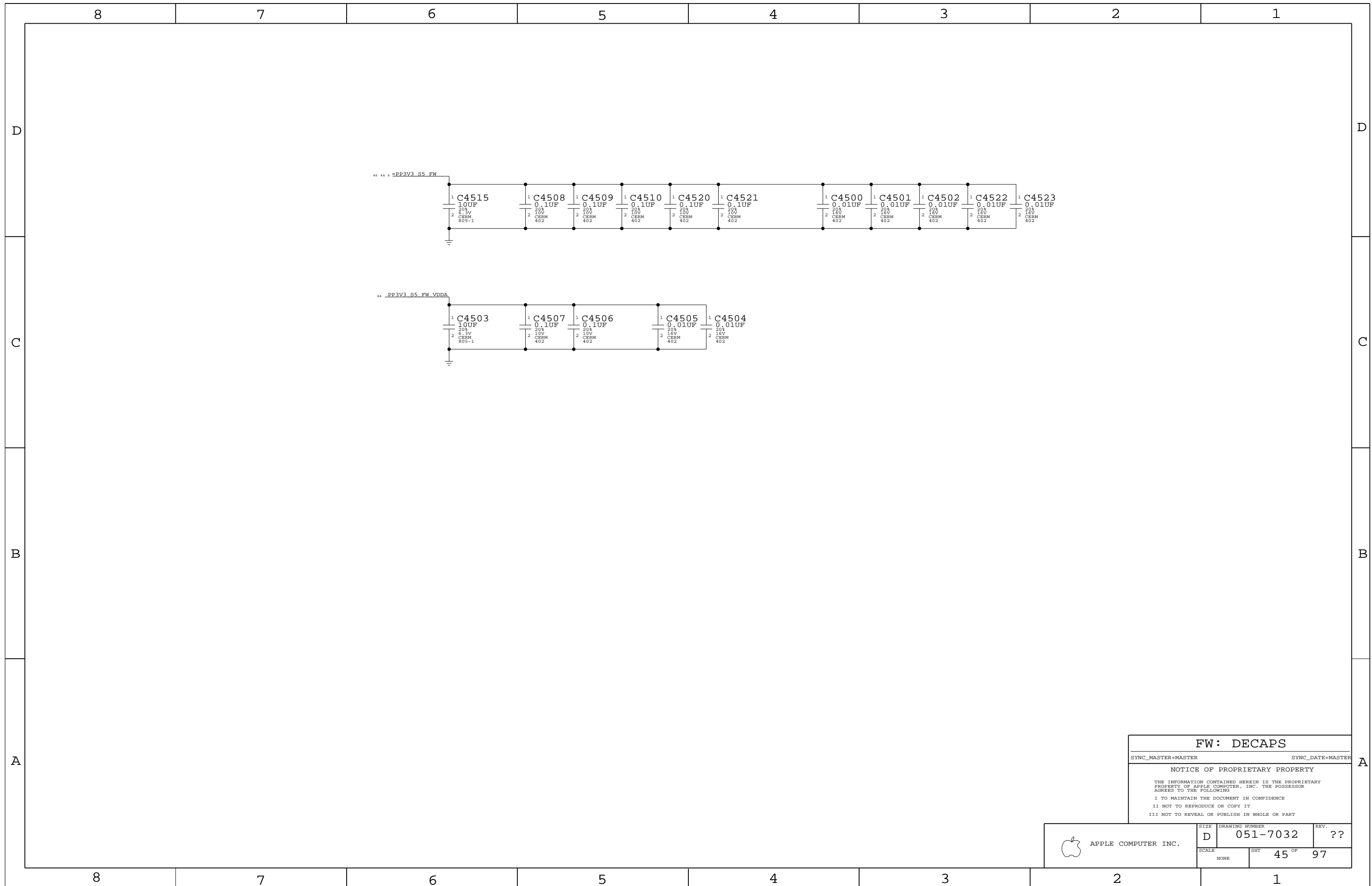
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	44 OF 97	
NONE			



FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER


NOTICE OF PROPRIETARY PROPERTY

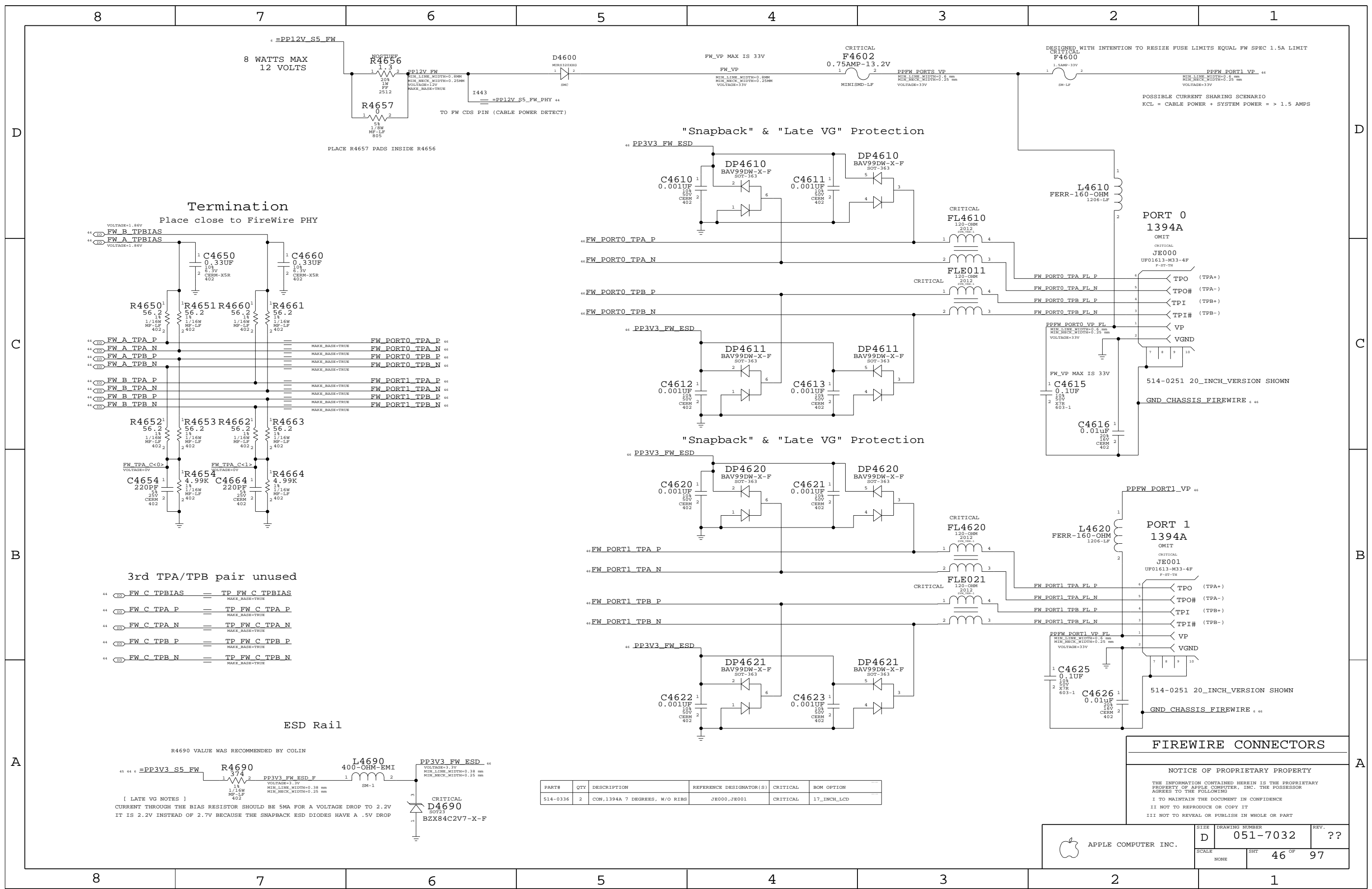
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	45 OF 97	
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

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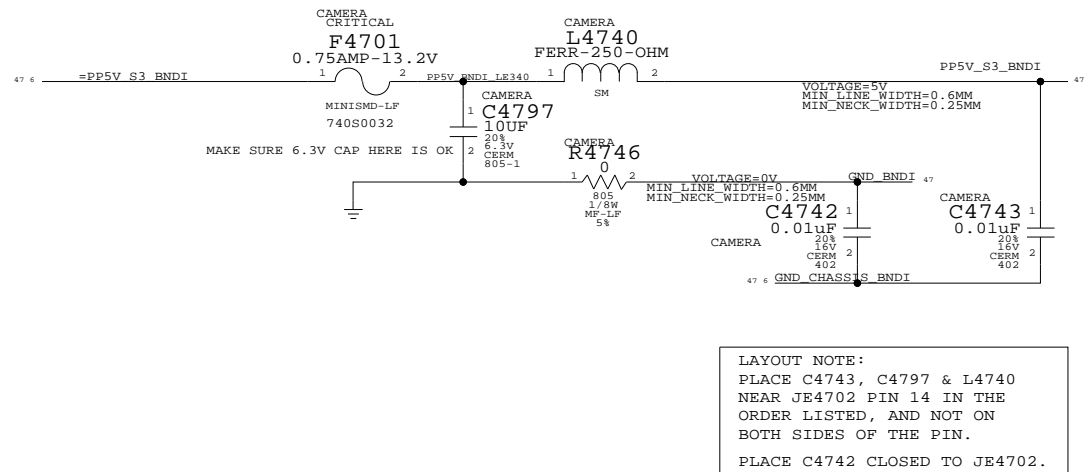
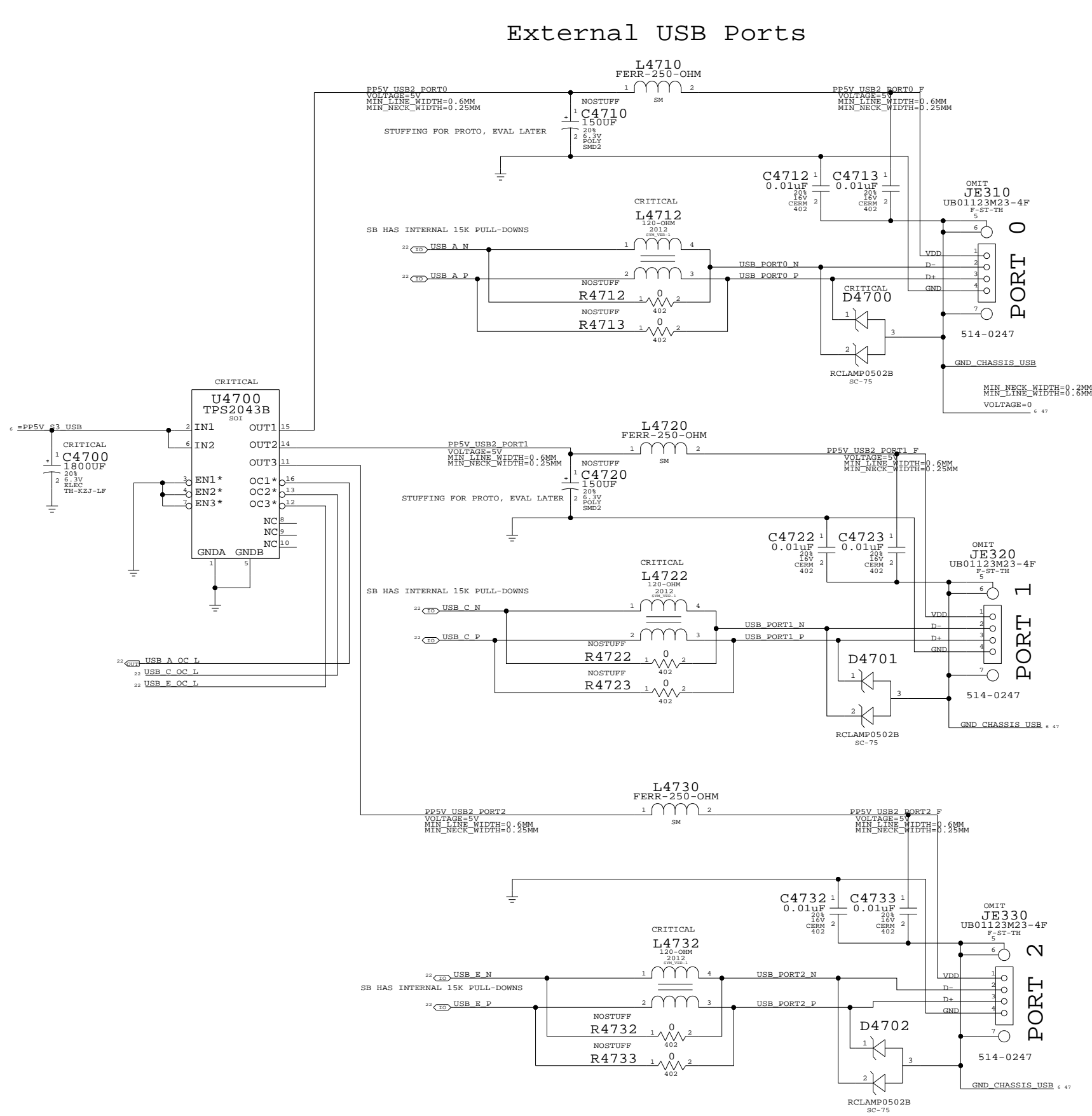
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II NOT TO REPRODUCE OR COPY IT

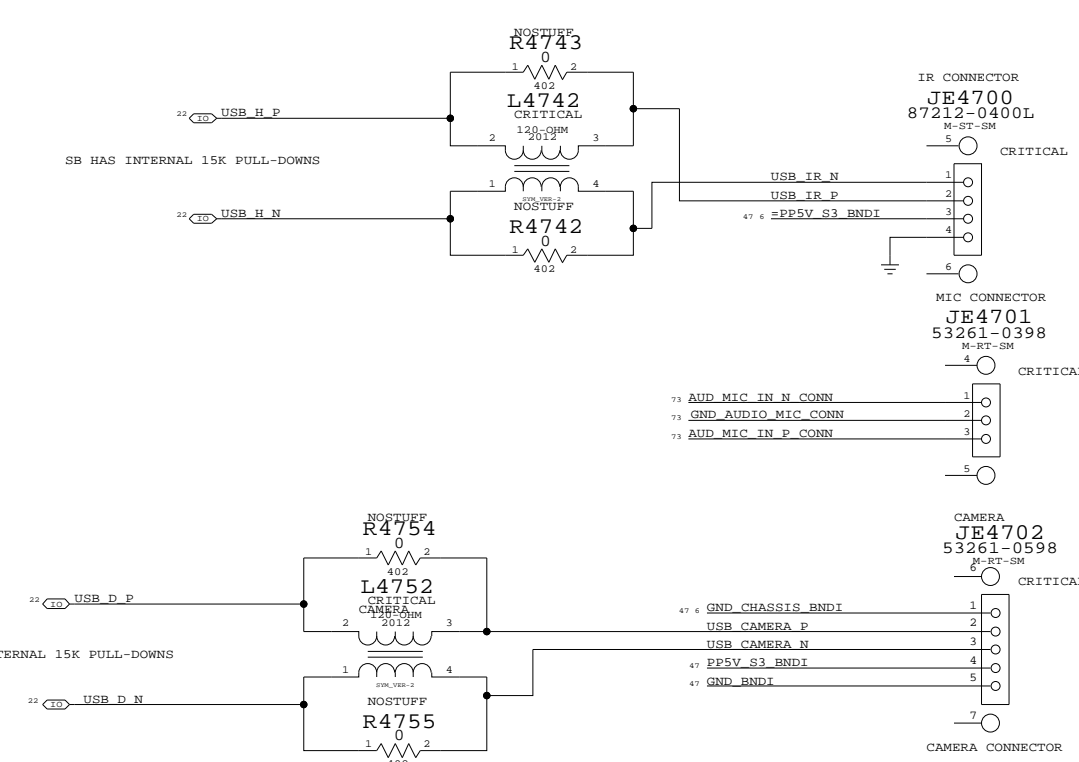
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 46	OF 97

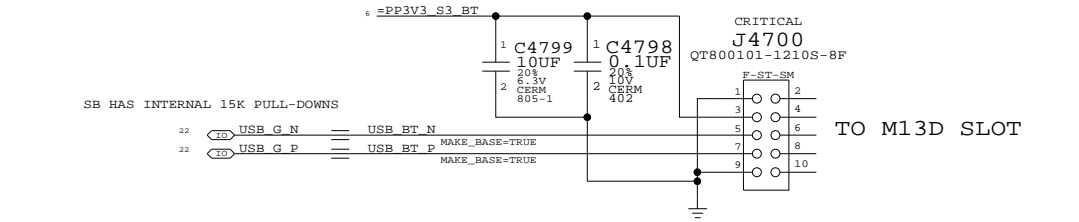
External USB Ports



LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE4702 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE4702.



BLUETOOTH



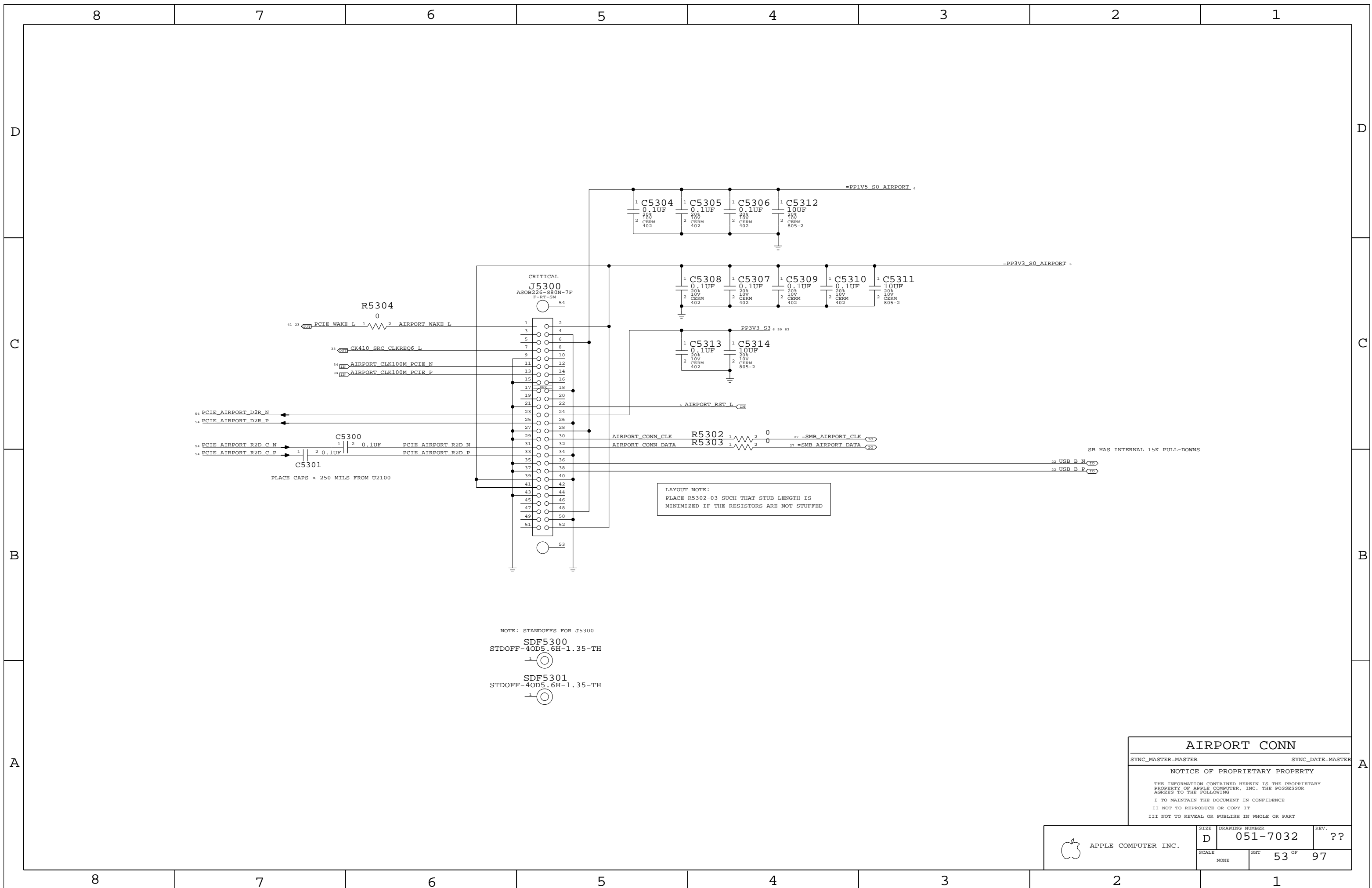
NOTE: STANDOFFS FOR J4700
SDF4700
STDOFF-40D4.5H-1.35-TH
SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7032	REV.	??
	SCALE	NONE	SHT	47 OF 97		



LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH

 SDF5301
 STDOFF-40D5.6H-1.35-TH


SB HAS INTERNAL 15K PULL-DOWNS


AIRPORT CONN

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	53 OF 97	
NONE			

8

7

6

5

4

3

2

1

D

D

C


C


B


B


A


A


22  PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE


22  PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE


22  PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE


22  PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE


22  PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE


22  PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE


22  PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE


22  PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE


22  PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE


22  PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE


22  PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22  PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE


22  PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE


22  PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE


22  PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE


22  PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE


USED PCIE PORTS


22  PCIE A R2D C N == PCIE AIRPORT R2D C N ⁵³
MAKE_BASE=TRUE


22  PCIE A R2D C P == PCIE AIRPORT R2D C P ⁵³
MAKE_BASE=TRUE


22 ⁵  PCIE A D2R N == PCIE AIRPORT D2R N ⁵³
MAKE_BASE=TRUE

22 ⁵  PCIE A D2R P == PCIE AIRPORT D2R P ⁵³
MAKE_BASE=TRUE

22  PCIE B R2D C N == PCIE ENET R2D C N ⁴¹
MAKE_BASE=TRUE

22  PCIE B R2D C P == PCIE ENET R2D C P ⁴¹
MAKE_BASE=TRUE

22 ⁵  PCIE B D2R N == PCIE ENET D2R N ⁴¹
MAKE_BASE=TRUE

22 ⁵  PCIE B D2R P == PCIE ENET D2R P ⁴¹
MAKE_BASE=TRUE

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE	SHT	
NONE	54 OF 97	

8

7

6

5

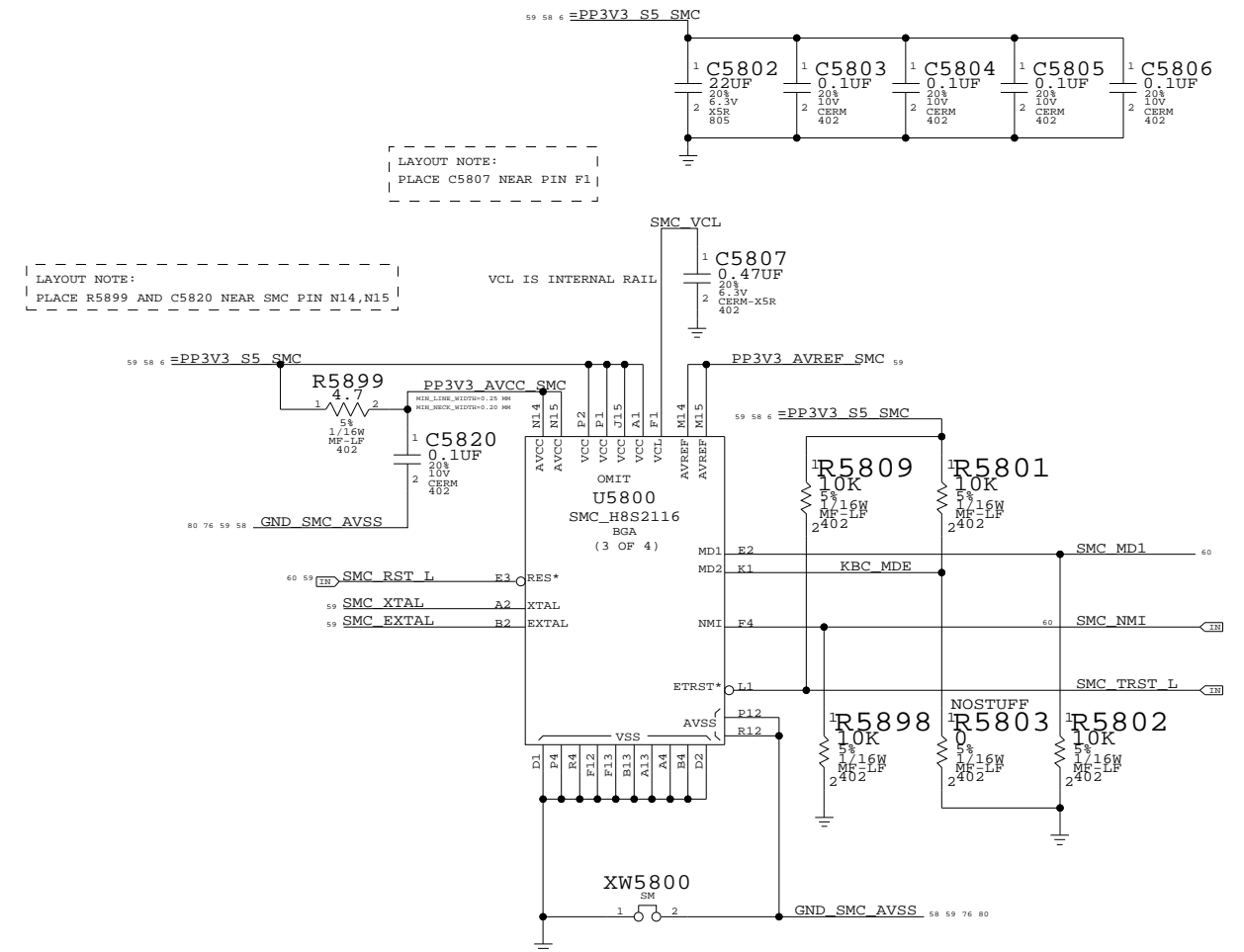
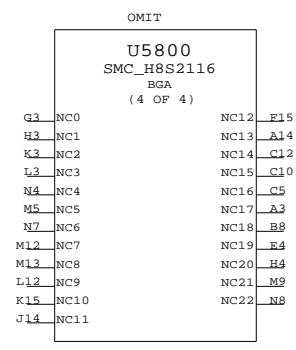
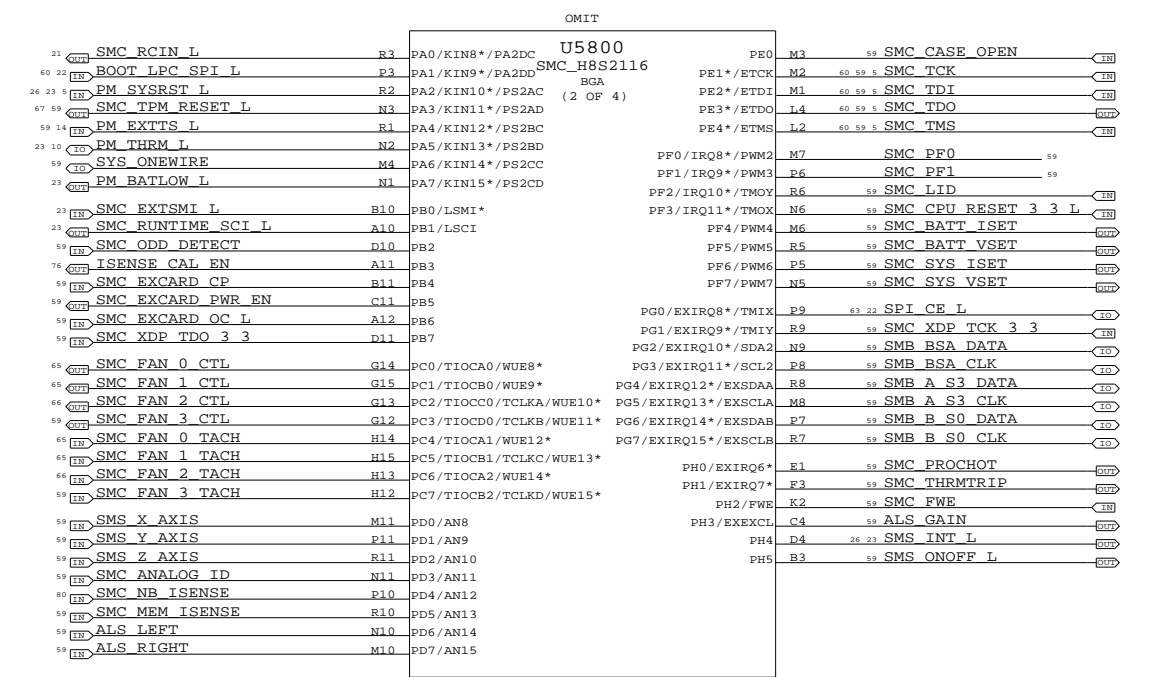
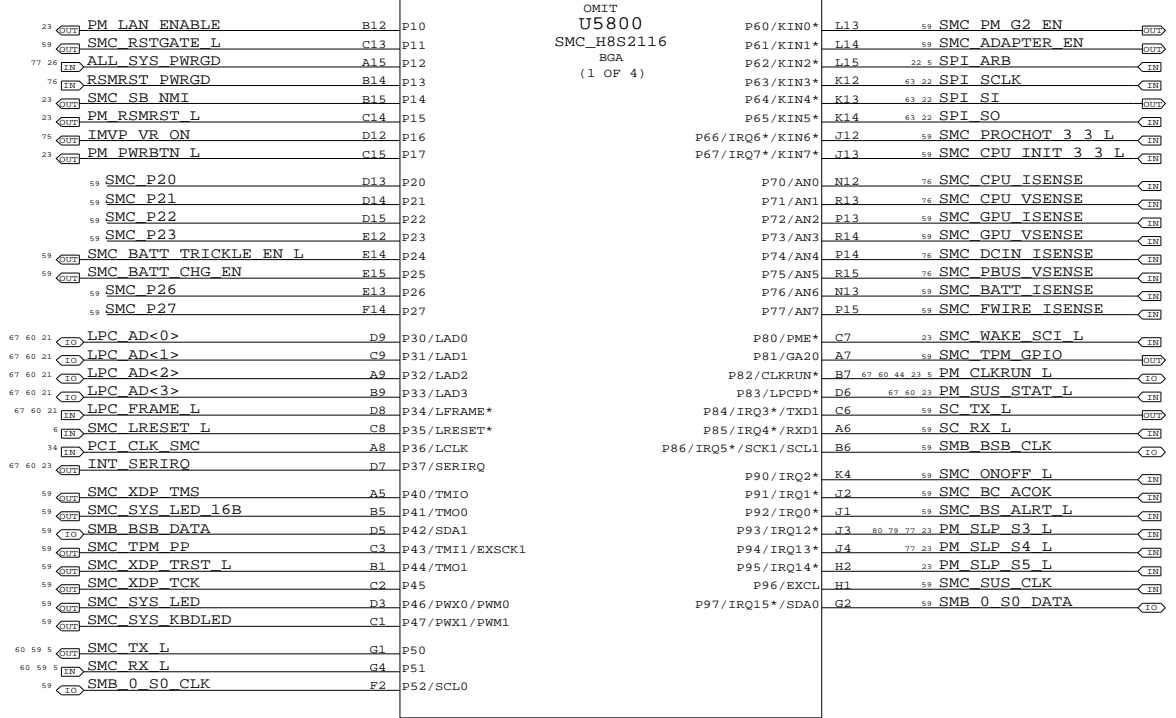
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

NOTICE OF PROPRIETARY PROPERTY

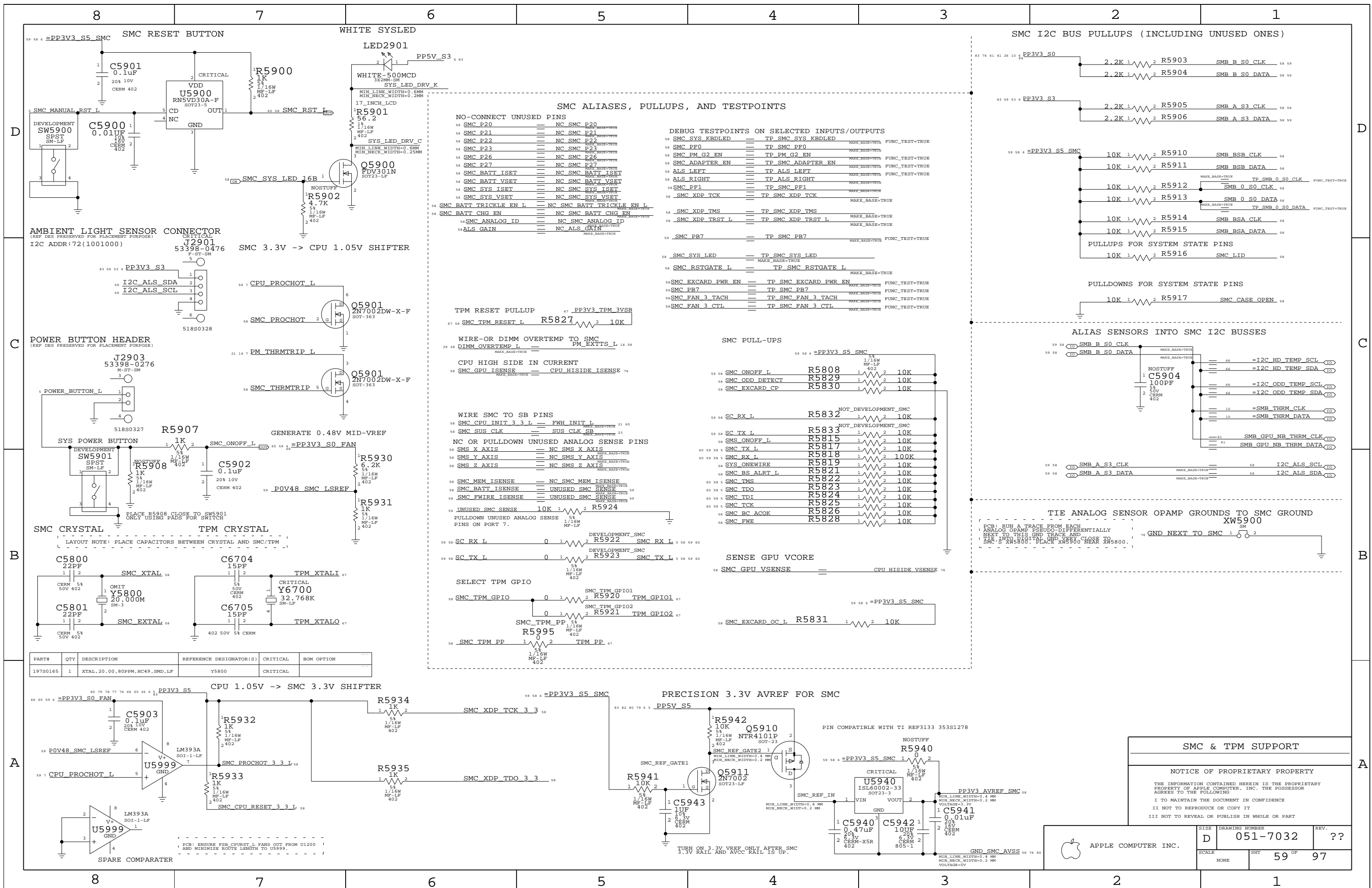
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	<p>SCALE</p> <p>NONE</p>	<p>SHT</p> <p>58 OF 97</p>	

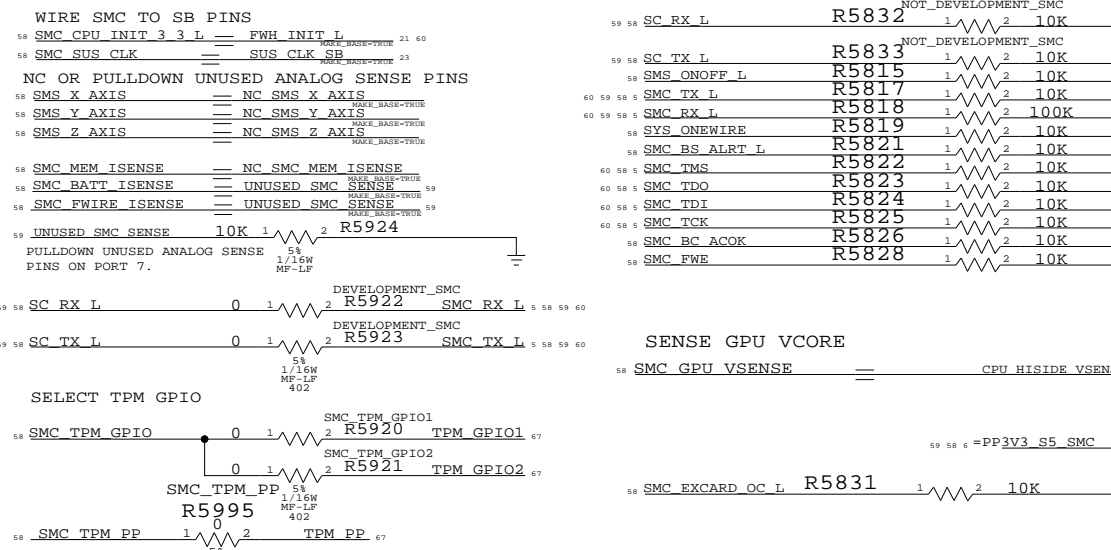


SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC PM_G2_EN == TP_PM_G2_EN MAKE_BASE=TRUE
58 SMC P23 == NC SMC P23	58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P26 == NC SMC P26	58 ALS_LEFT == TP_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P27 == NC SMC P27	58 ALS_RIGHT == TP_ALS_RIGHT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_ISET == NC SMC_BATT_ISET	58 SMC_PFI == TP_SMC_PFI MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC SMC_BATT_VSET	58 SMC_XDP_TCK == TP_SMC_XDP_TCK MAKE_BASE=TRUE
58 SMC_SYS_ISET == NC SMC_SYS_ISET	58 SMC_XDP_TMS == TP_SMC_XDP_TMS MAKE_BASE=TRUE
58 SMC_SYS_VSET == NC SMC_SYS_VSET	58 SMC_XDP_TRST_L == TP_SMC_XDP_TRST_L MAKE_BASE=TRUE
58 SMC_BATT_TRICKLE_EN_L == NC SMC_BATT_TRICKLE_EN_L	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_CHG_EN == NC SMC_BATT_CHG_EN	58 SMC_SYS_LED == TP_SMC_SYS_LED MAKE_BASE=TRUE
58 SMC_ANALOG_ID == NC SMC_ANALOG_ID	58 SMC_RSTGATE_L == TP_SMC_RSTGATE_L MAKE_BASE=TRUE
58 ALS_GAIN == NC ALS_GAIN MAKE_BASE=TRUE	58 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL MAKE_BASE=TRUE FUNC_TEST=TRUE

SMC PULL-UPS

58 SMC_ONOFF_L	R5808	10K
58 SMC_ODD_DETECT	R5829	10K
58 SMC_EXCARD_CP	R5830	10K
58 SC_RX_L	R5832	10K
58 SC_TX_L	R5833	10K
58 SMS_ONOFF_L	R5815	10K
58 SMC_TX_L	R5817	10K
58 SMC_RX_L	R5818	100K
58 SYS_ONEWIRE	R5819	10K
58 SMC_BS_ALRT_L	R5821	10K
58 SMC_TMS	R5822	10K
58 SMC_TDO	R5823	10K
58 SMC_TDI	R5824	10K
58 SMC_TCK	R5825	10K
58 SMC_BC_ACOK	R5826	10K
58 SMC_FWE	R5828	10K



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

SMC & TPM SUPPORT

NOTICE OF PROPRIETARY PROPERTY

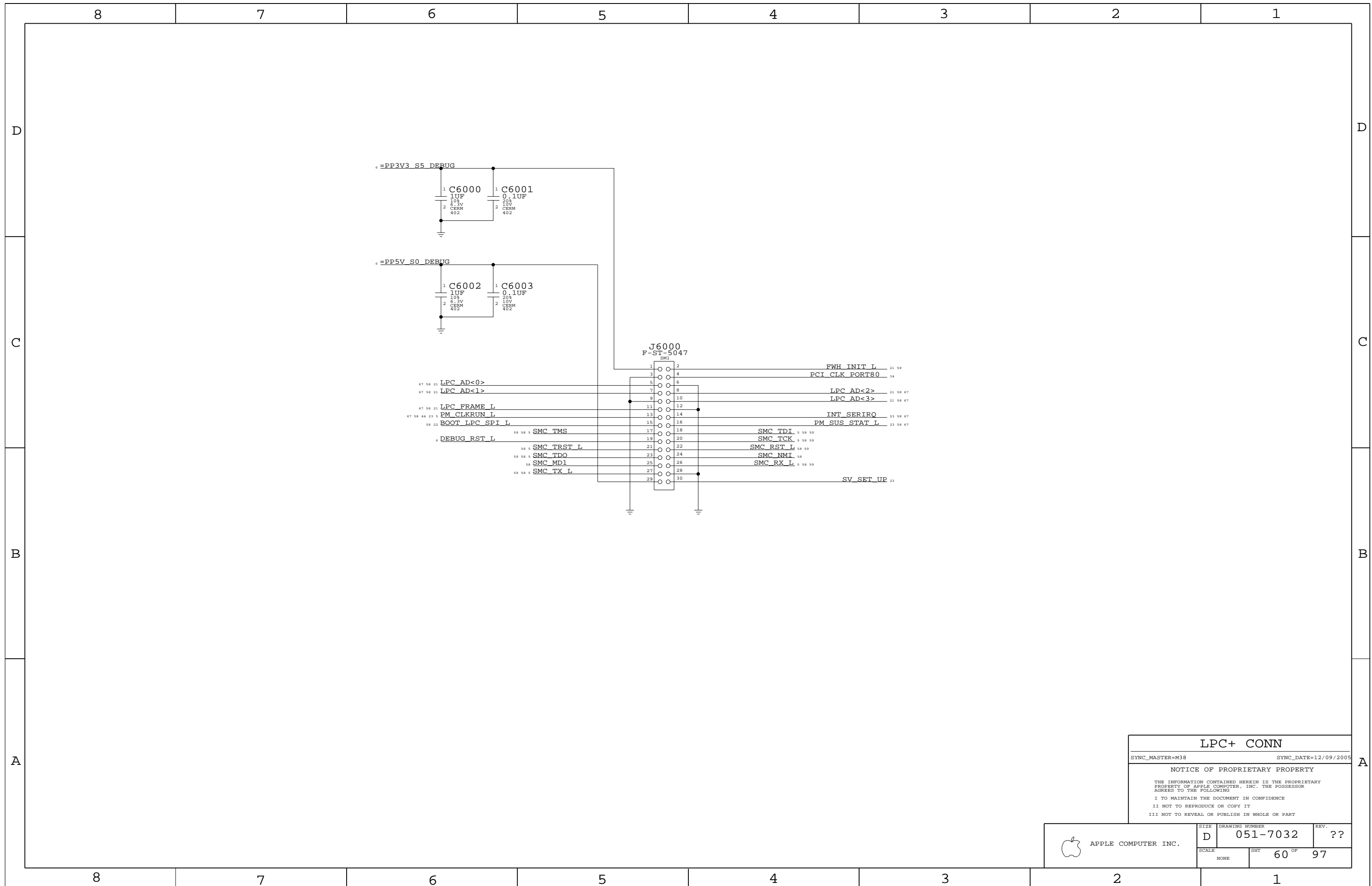
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SCALE NONE	SHEET 59 OF 97	SIZE D	DRAWING NUMBER 051-7032	REV. ??
		APPLE COMPUTER INC.		



LPC+ CONN

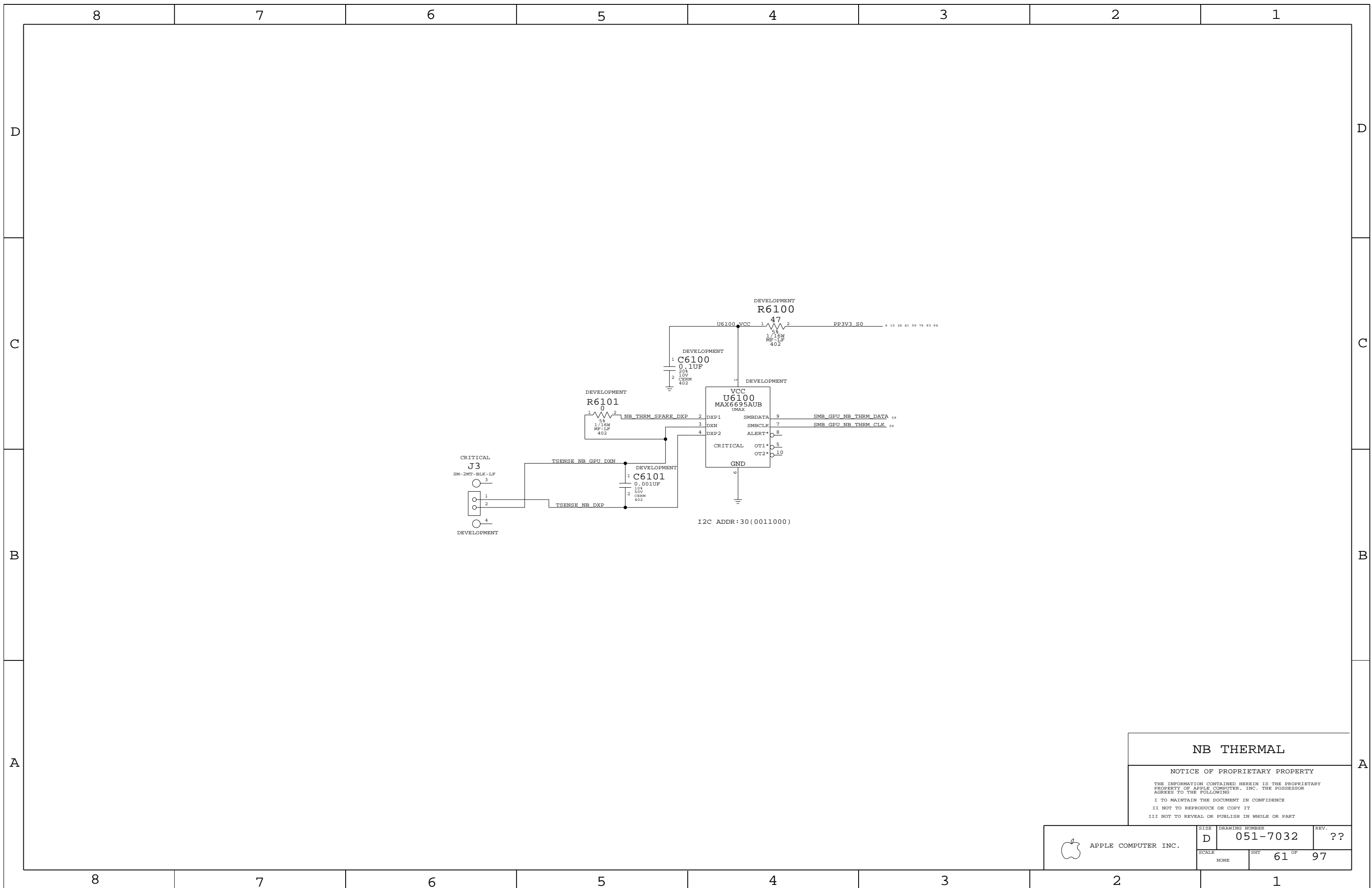
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHT 60 OF 97	



NB THERMAL


NOTICE OF PROPRIETARY PROPERTY

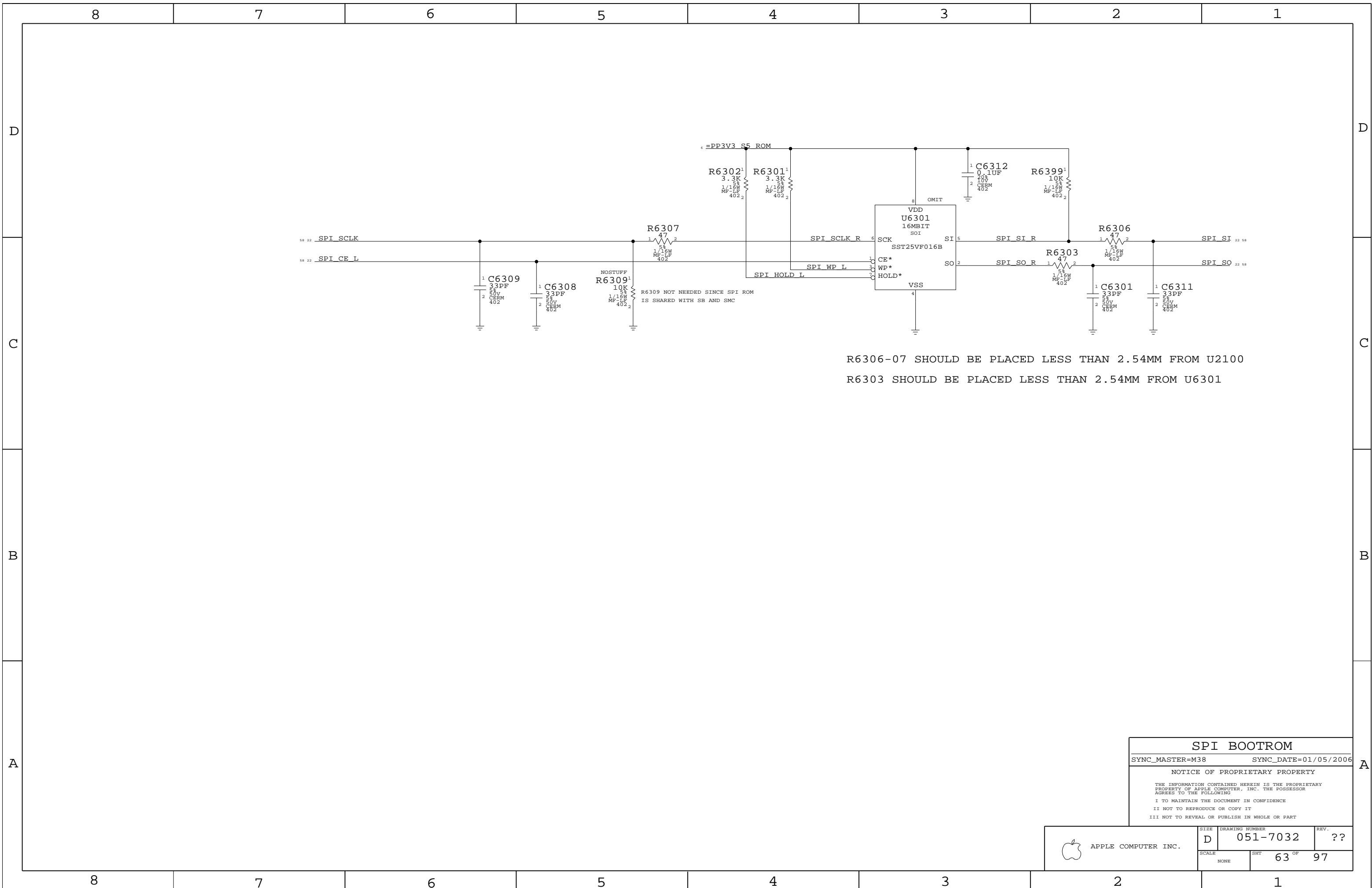
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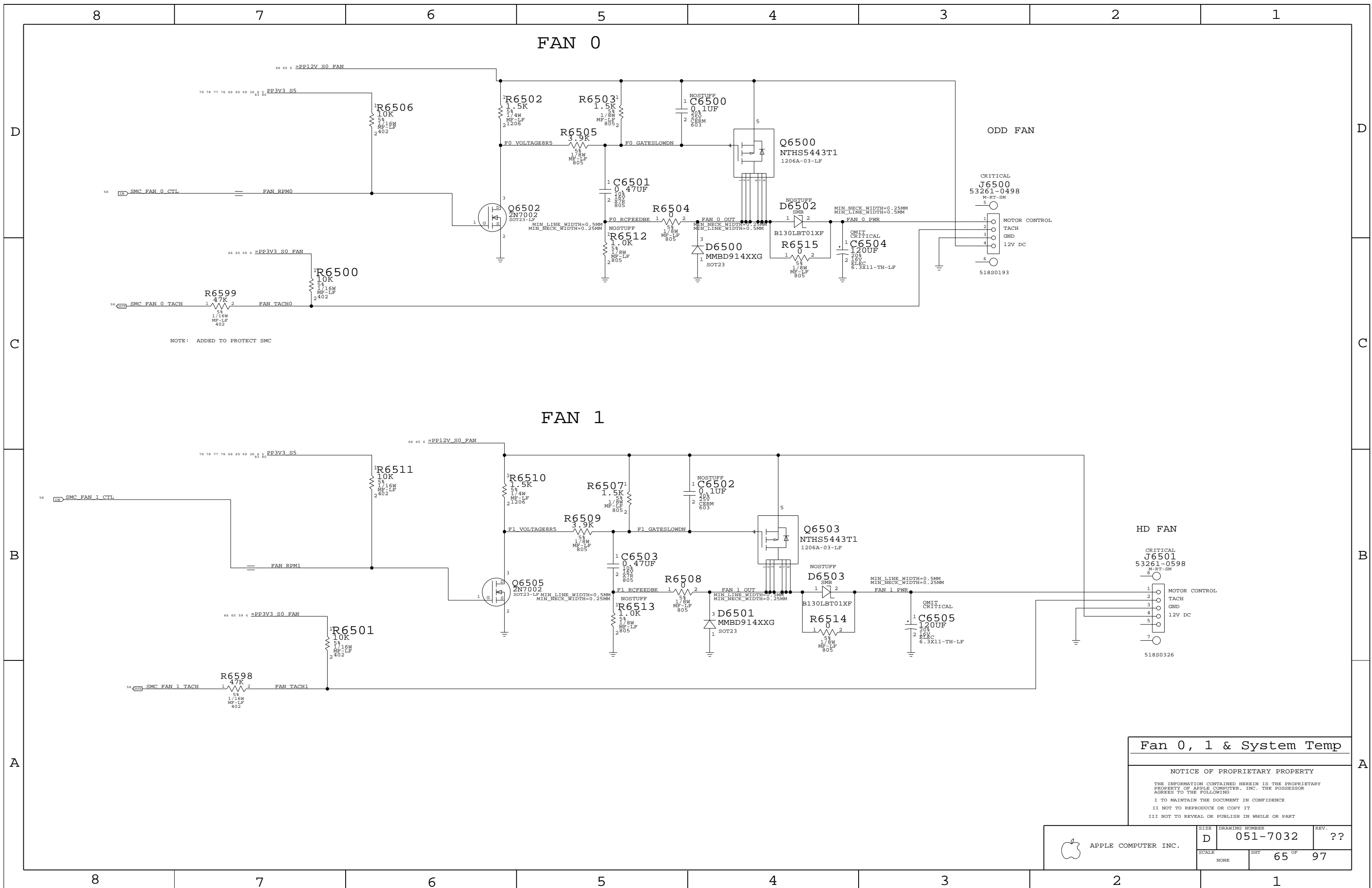
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	OF	
NONE	61	97	



SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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	SCALE NONE	SHEET 63 OF 97	

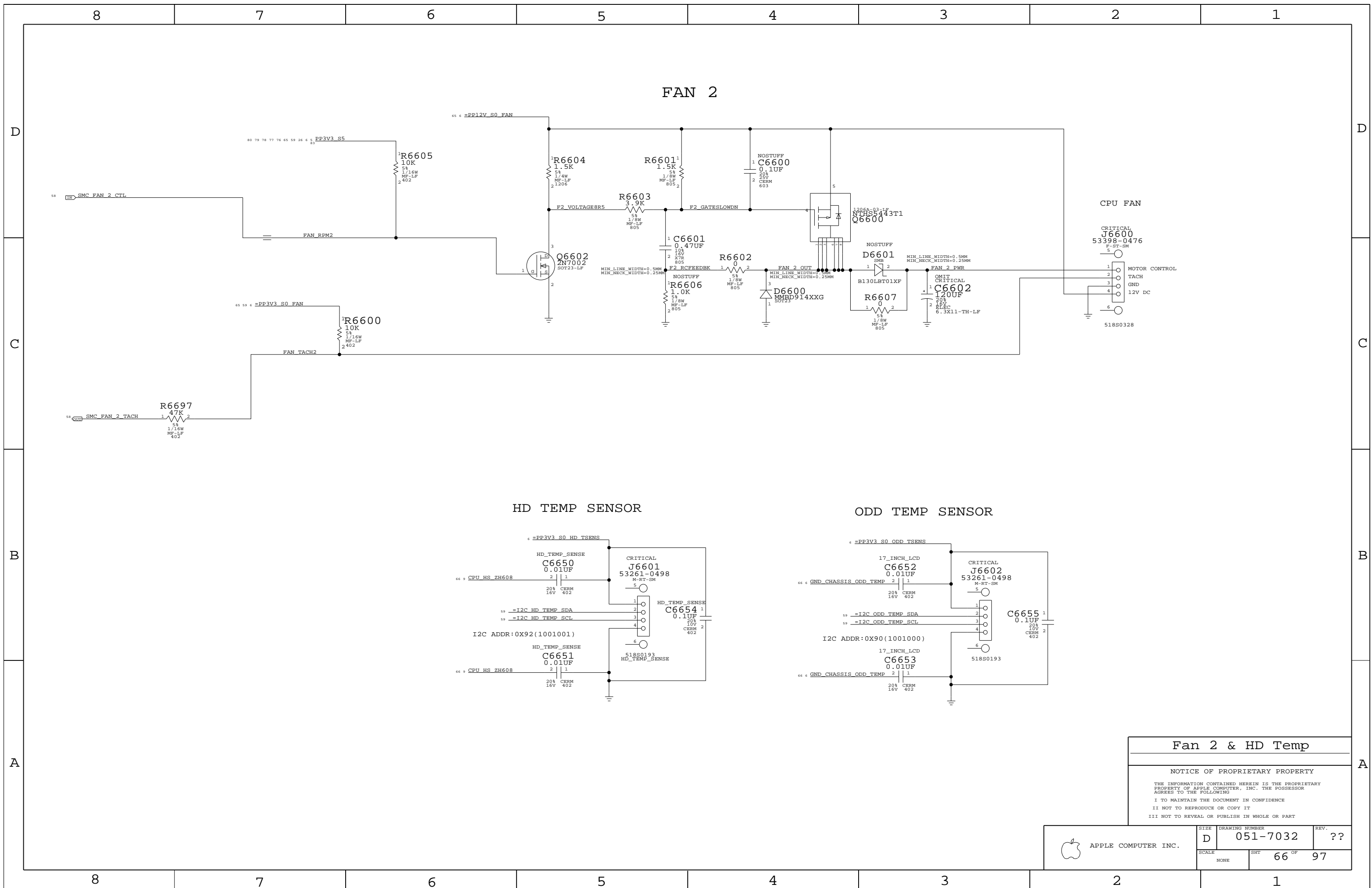


Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	65 OF 97	
NONE			



HD TEMP SENSOR

ODD TEMP SENSOR

Fan 2 & HD Temp

NOTICE OF PROPRIETARY PROPERTY

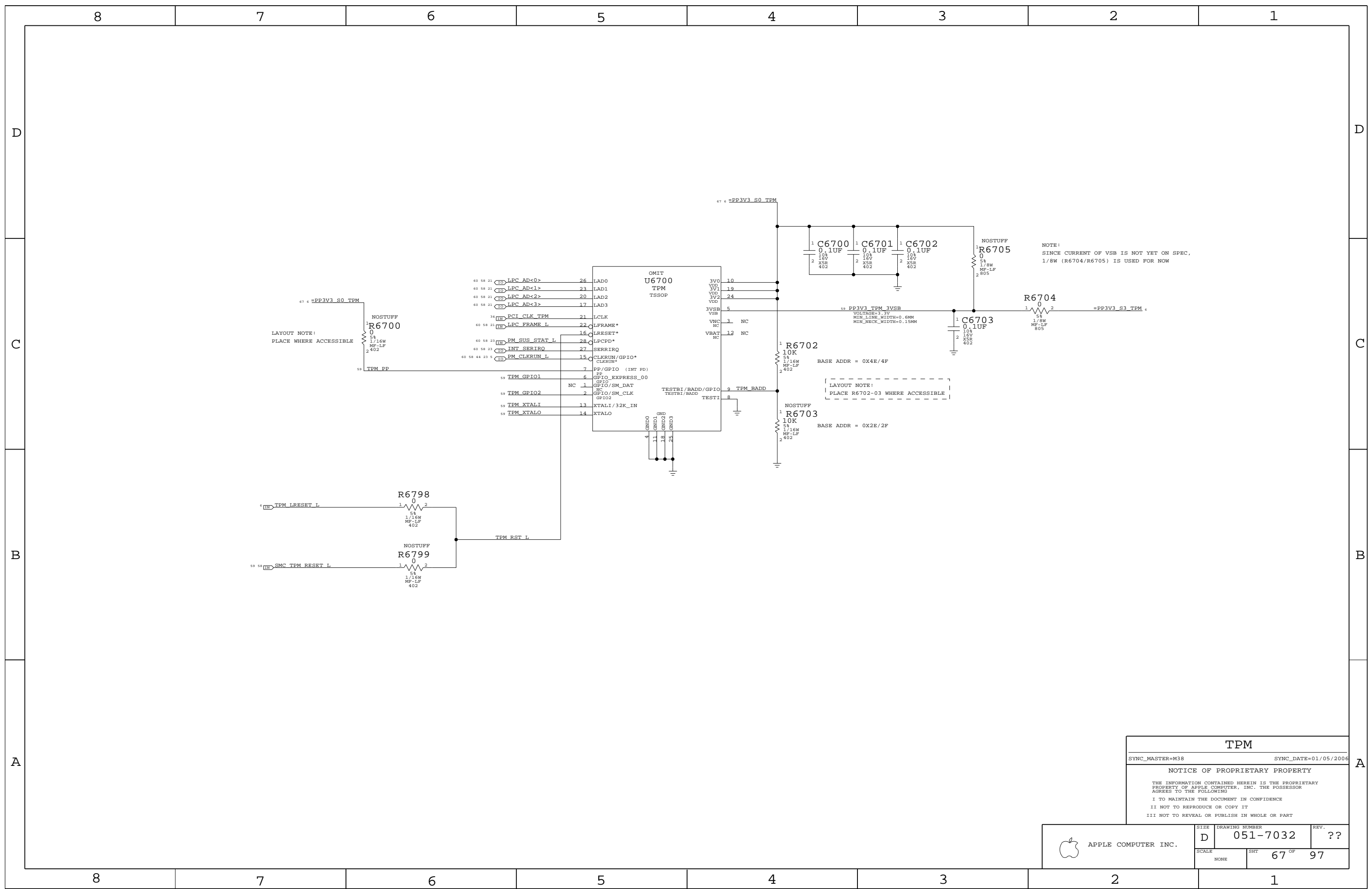
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 66 OF 97	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

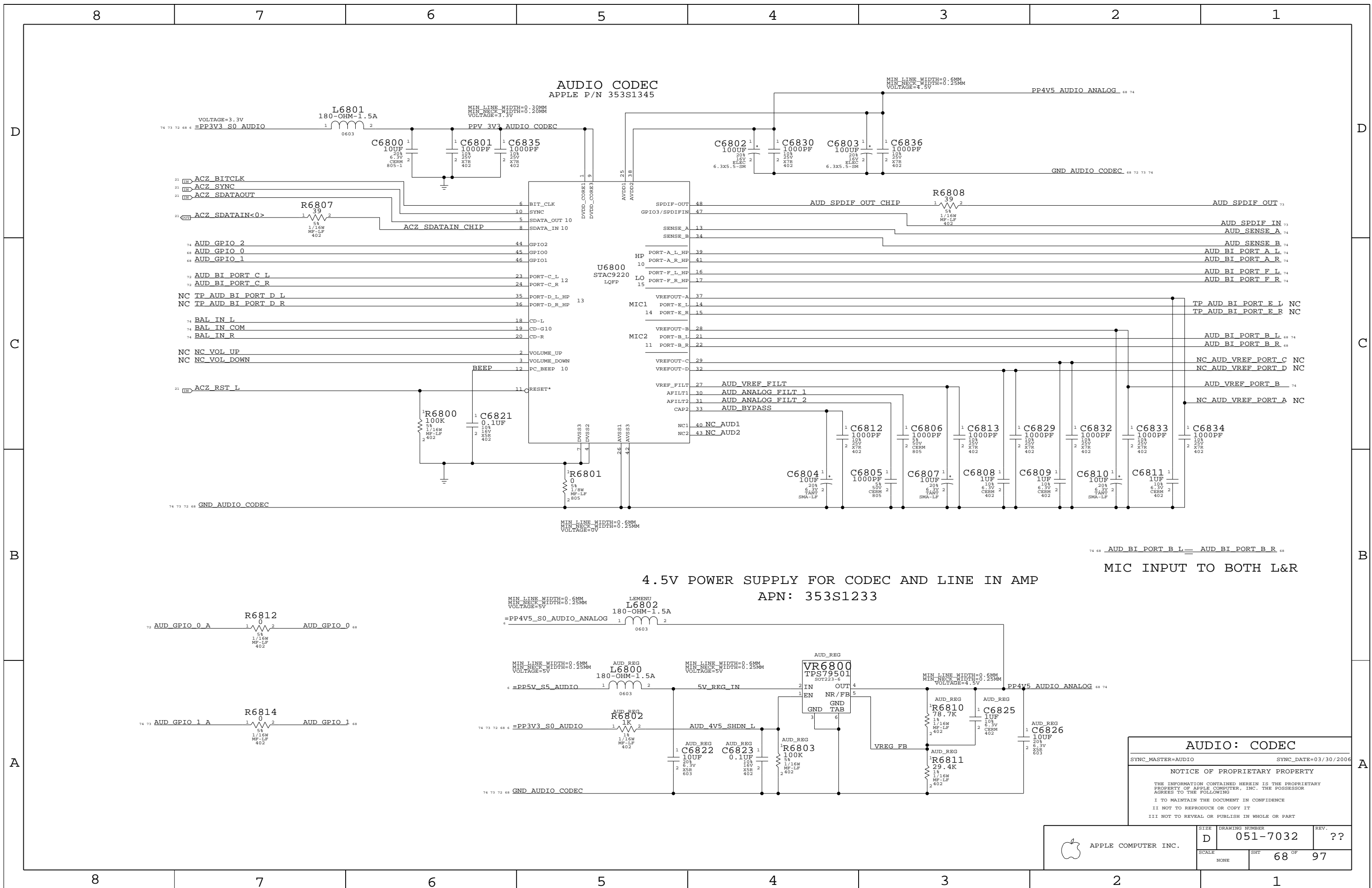
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	67 OF 97	
NONE			

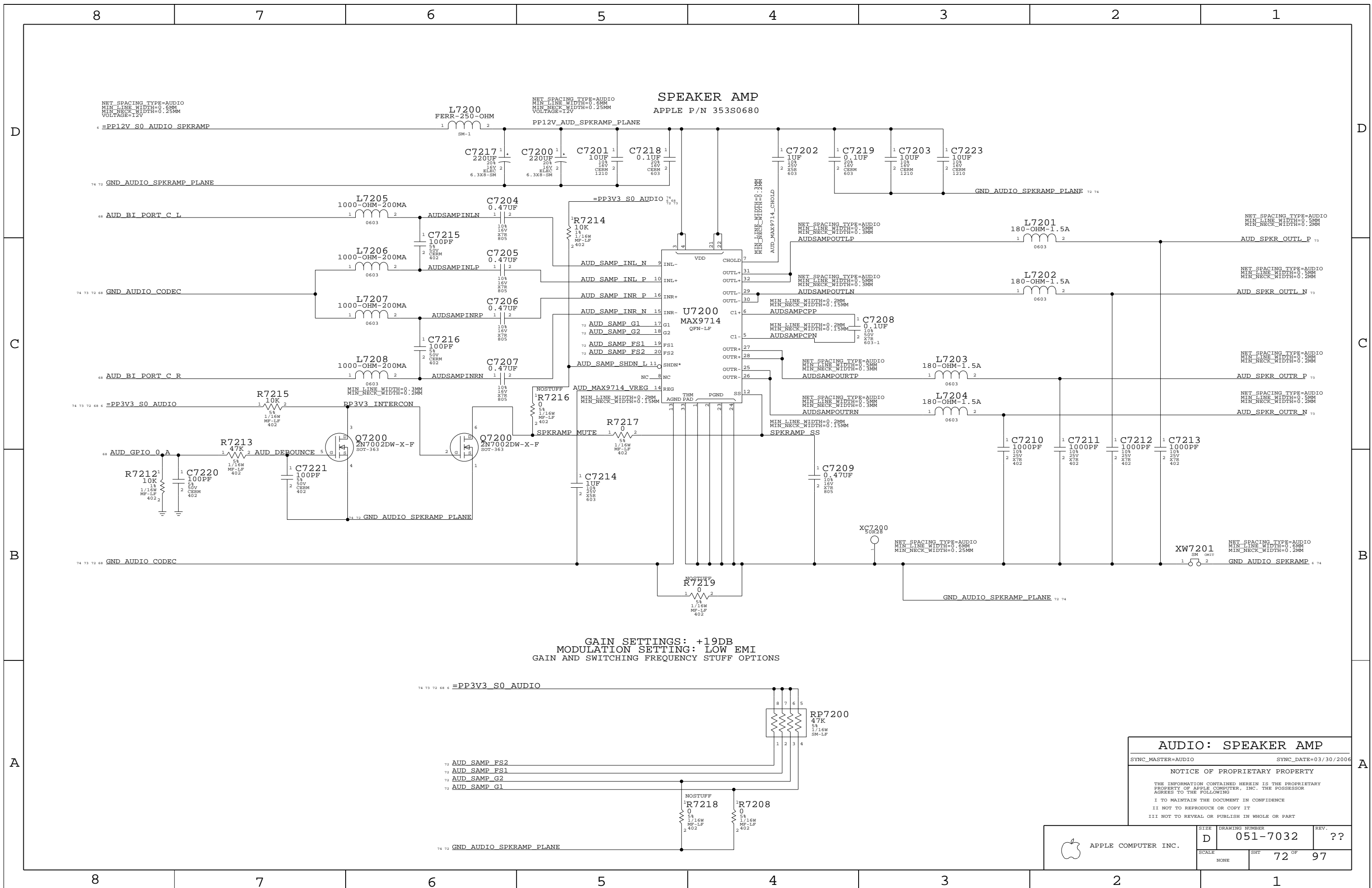


AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 68 OF 97	



SPEAKER AMP
APPLE P/N 353S0680

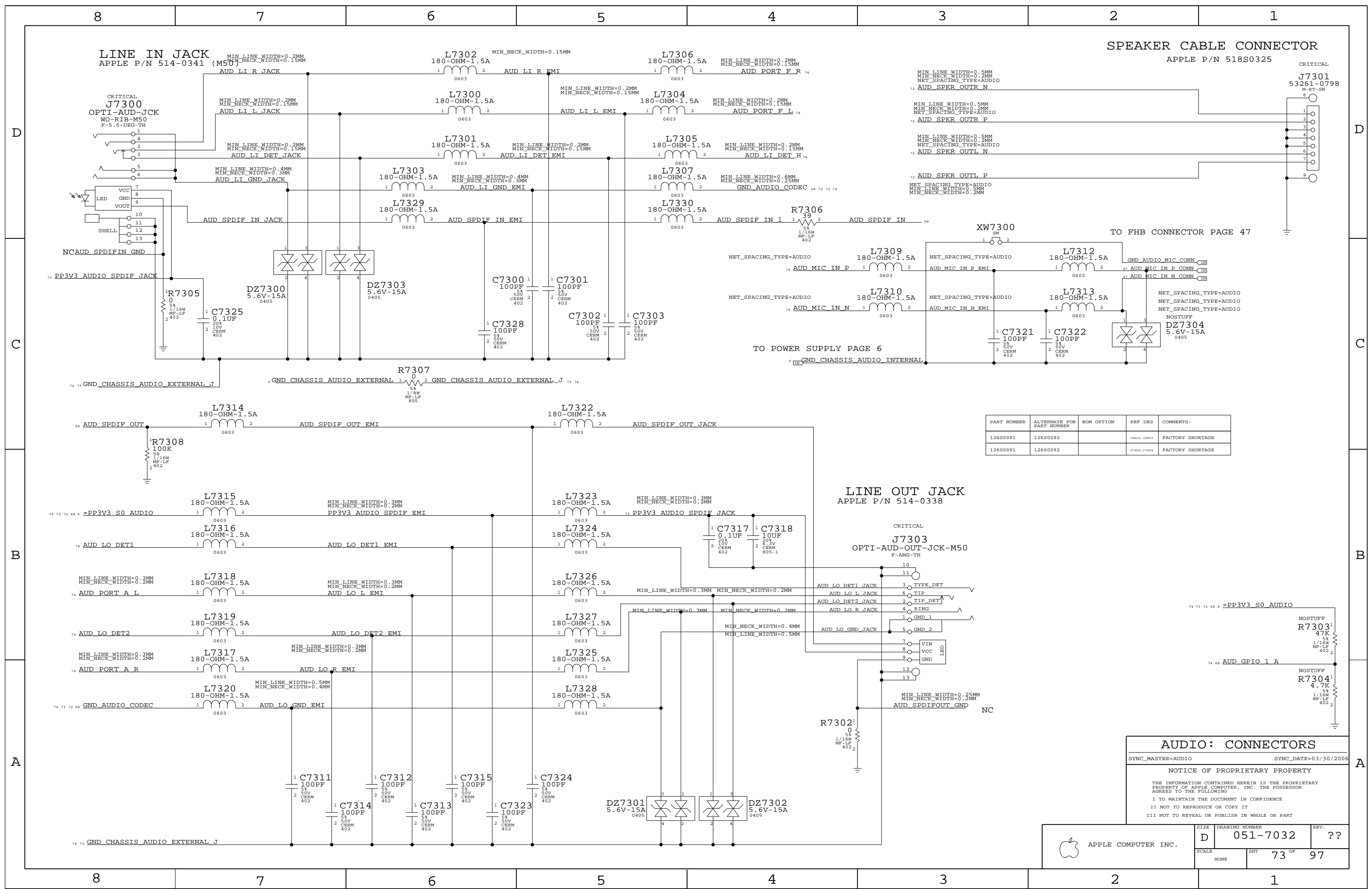
GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	72 OF	97
NONE			

LINE IN JACK
APPLE P/N 514-0341 (M50)

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

LINE OUT JACK
APPLE P/N 514-0338

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

NOTICE OF PROPRIETARY PROPERTY

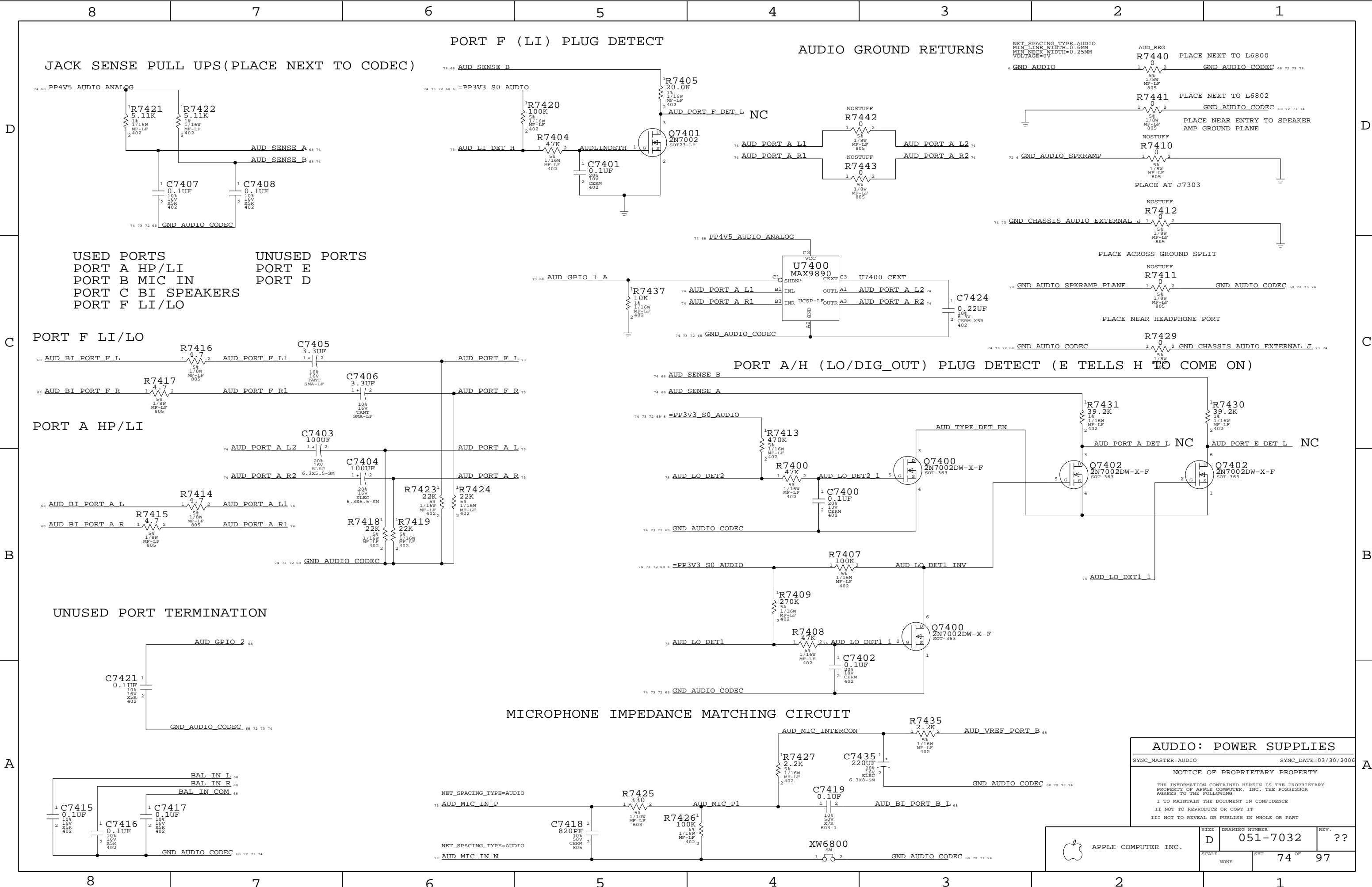
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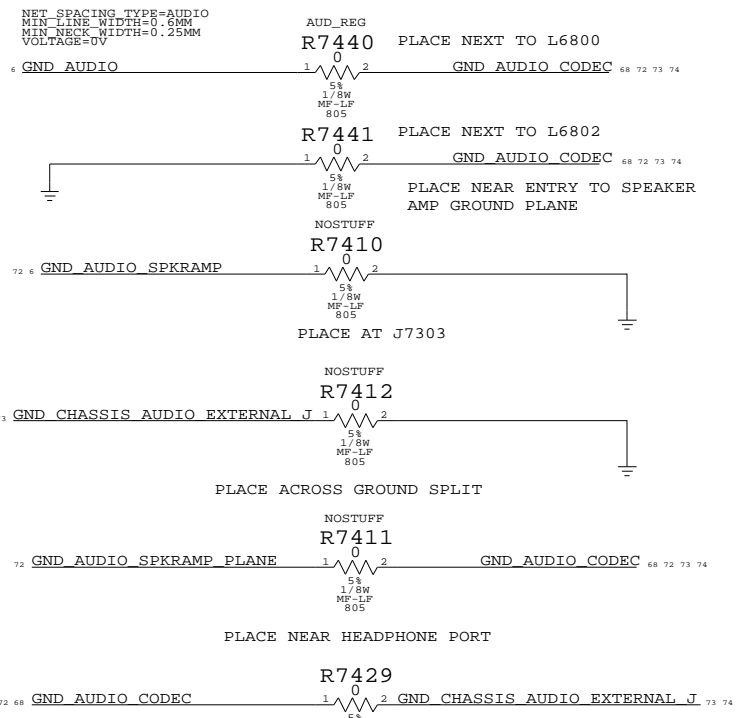
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	73 OF	97
NONE			



JACK SENSE PULL UPS (PLACE NEXT TO CODEC)

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS



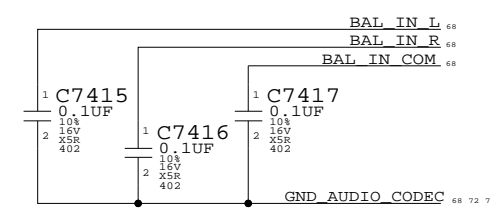
USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E
PORT D

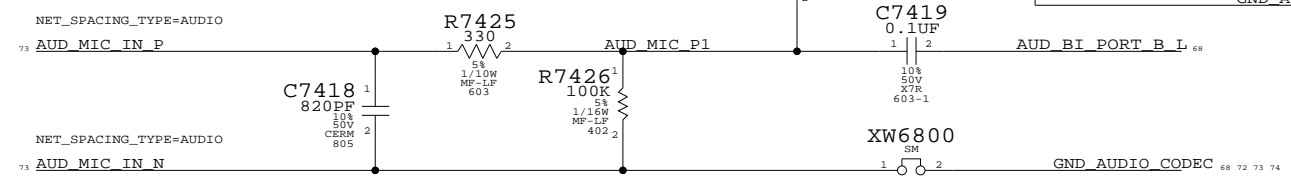
PORT F LI/LO

PORT A HP/LI

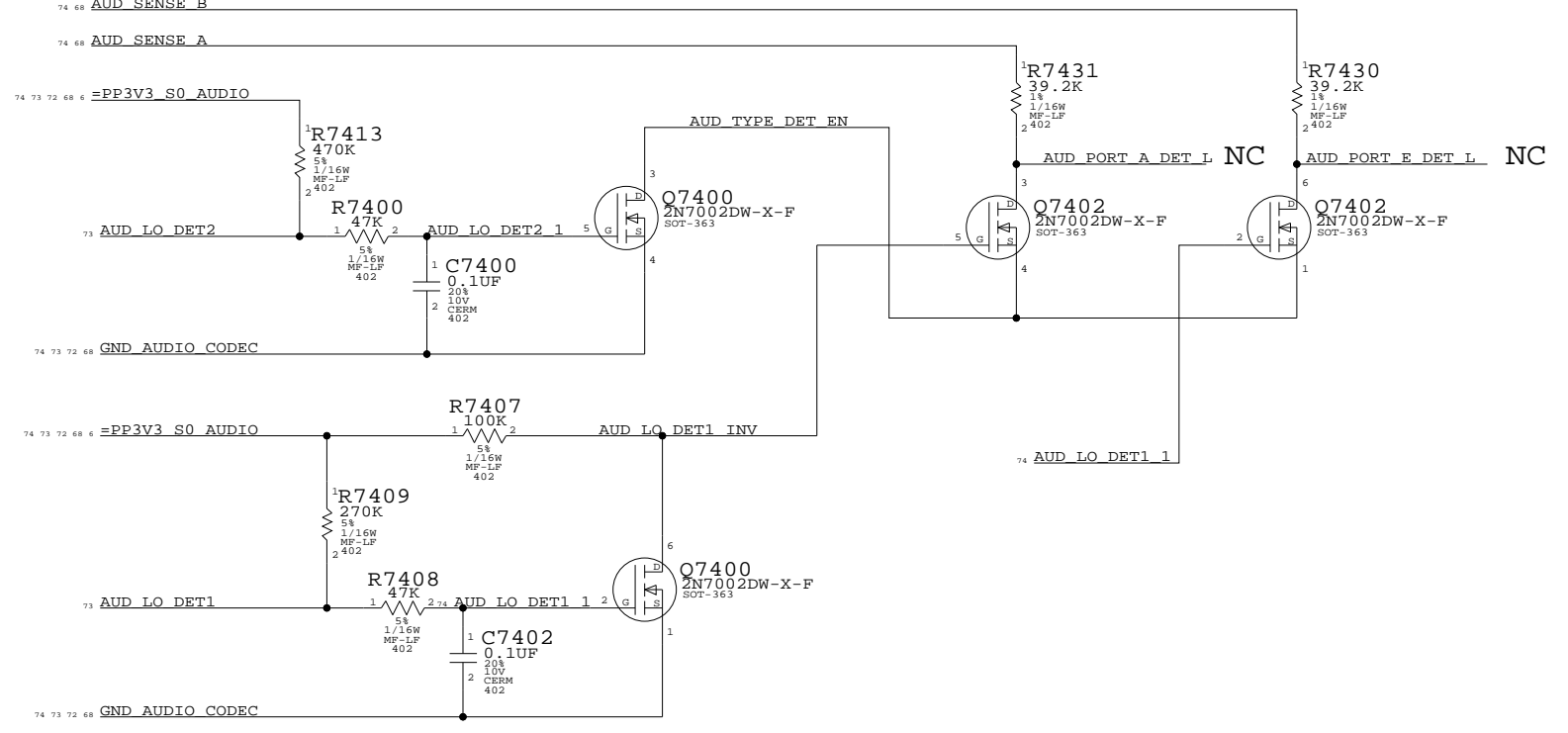
UNUSED PORT TERMINATION



MICROPHONE IMPEDANCE MATCHING CIRCUIT



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



AUDIO: POWER SUPPLIES

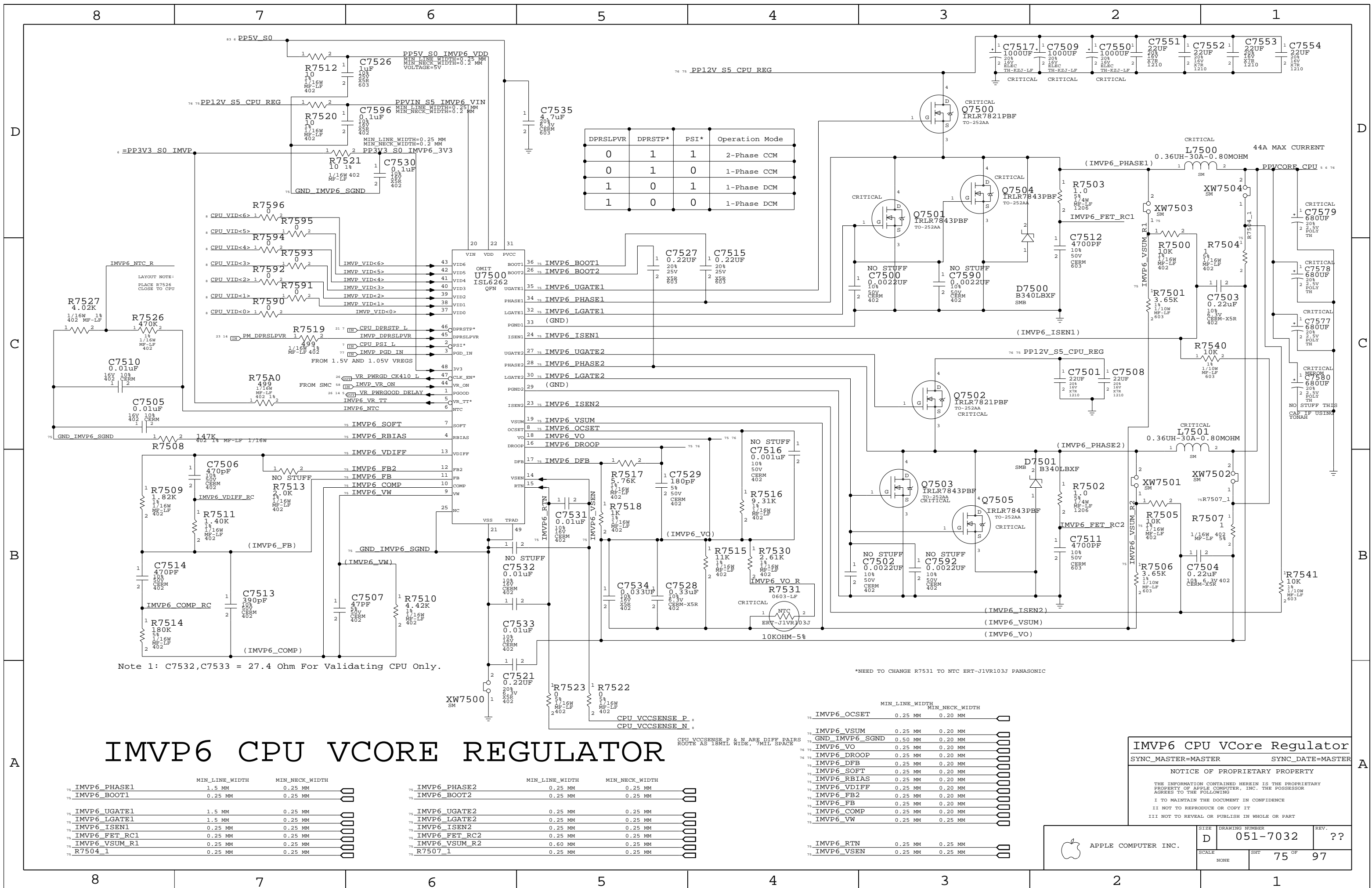
SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

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	D	051-7032	??
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

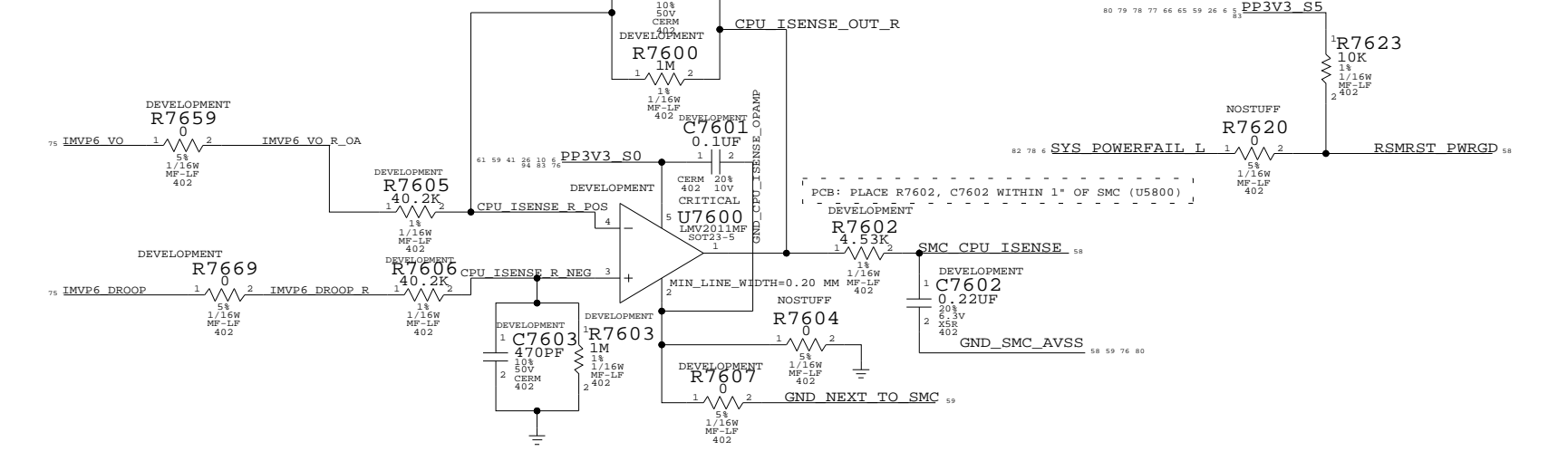
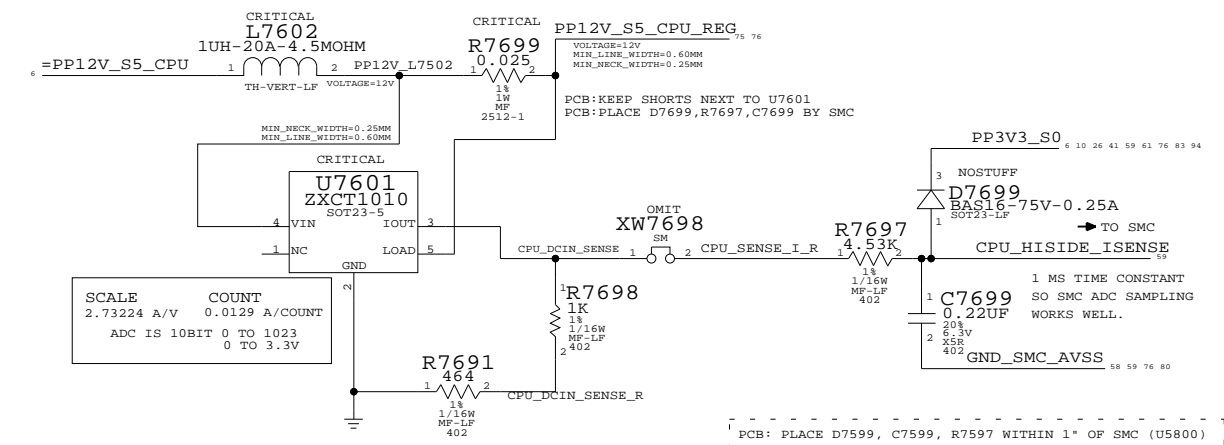
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	NONE	D 051-7032	??
	SHEET	75 OF 97	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

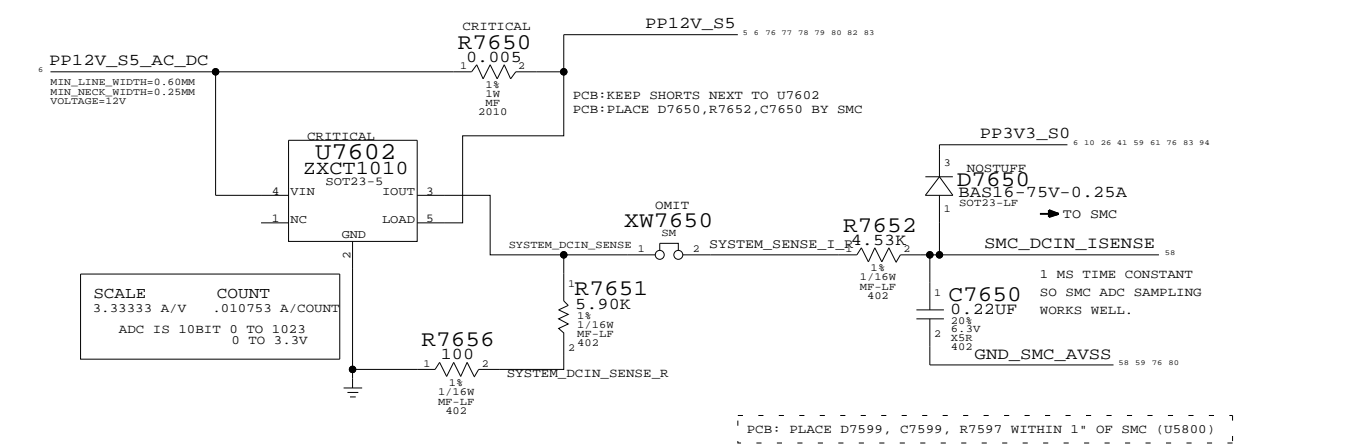
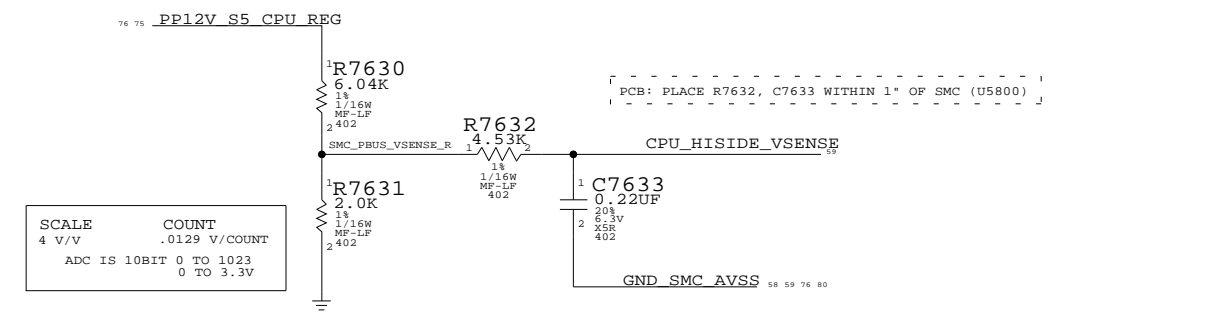
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

SMC PWRGD PULLUP



PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

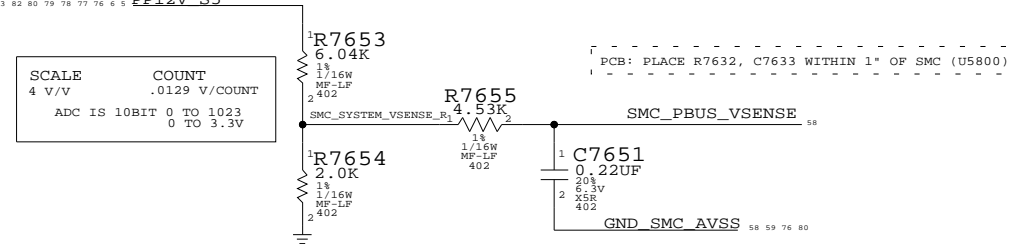
SYSTEM CURRENT SENSE



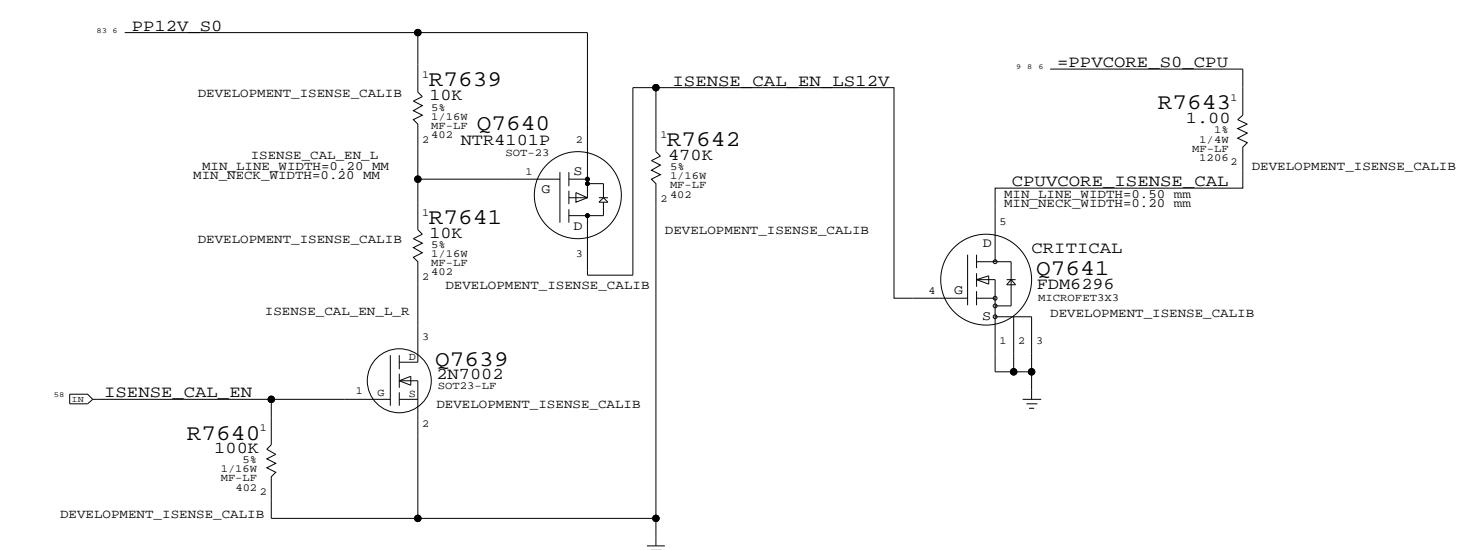
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



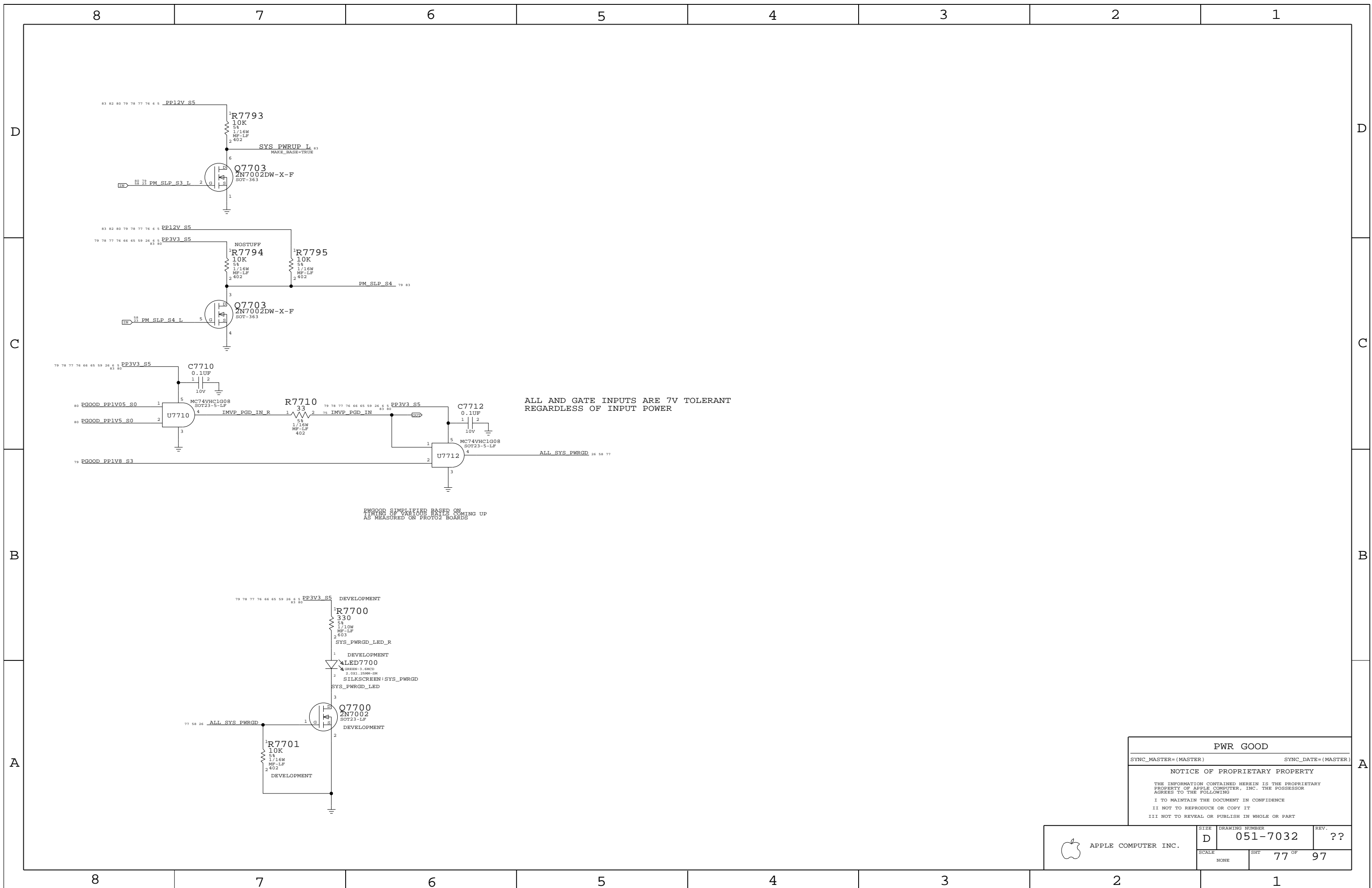
PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	76 OF	97
NONE			



ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWRGOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS


PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

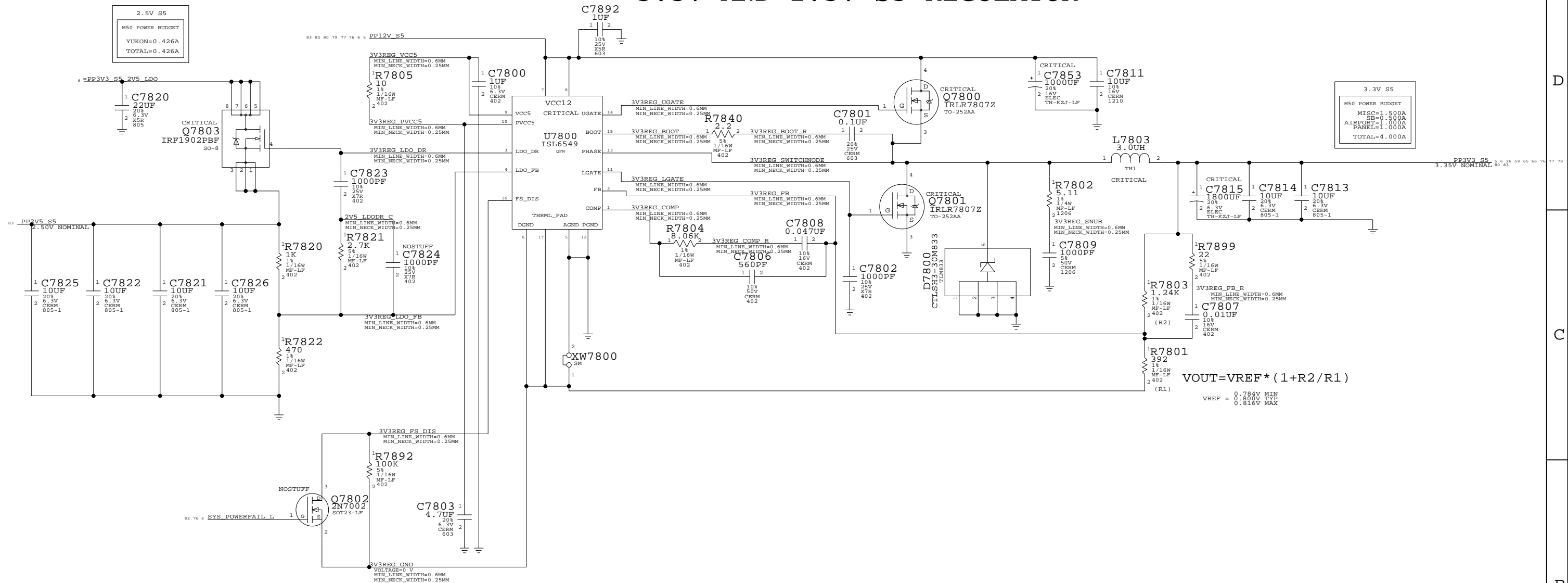
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	D	051-7032	??
SCALE	SHT	77 OF	97
NONE			

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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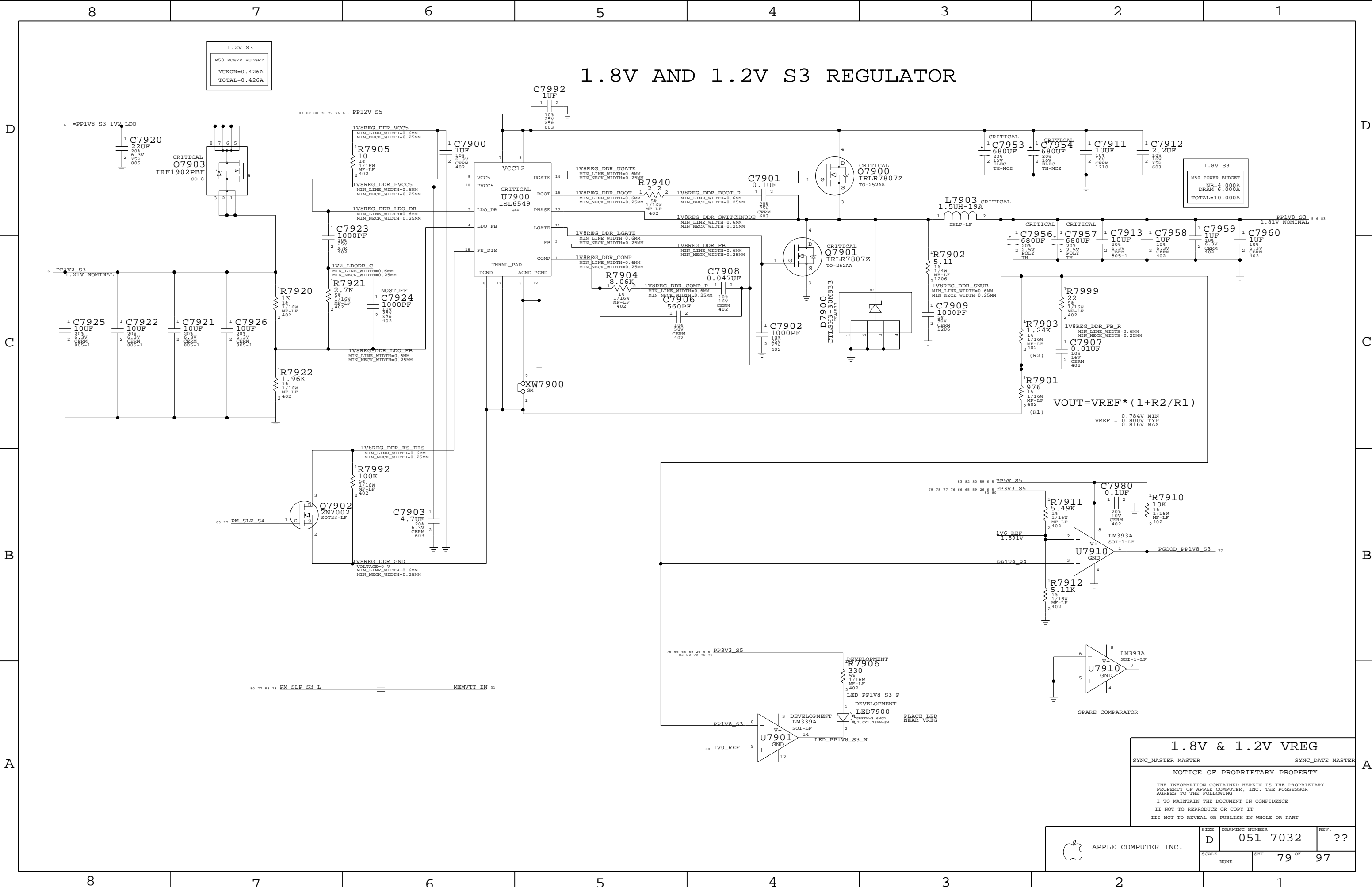
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	78 OF 97	
NONE			

TRUE

1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A

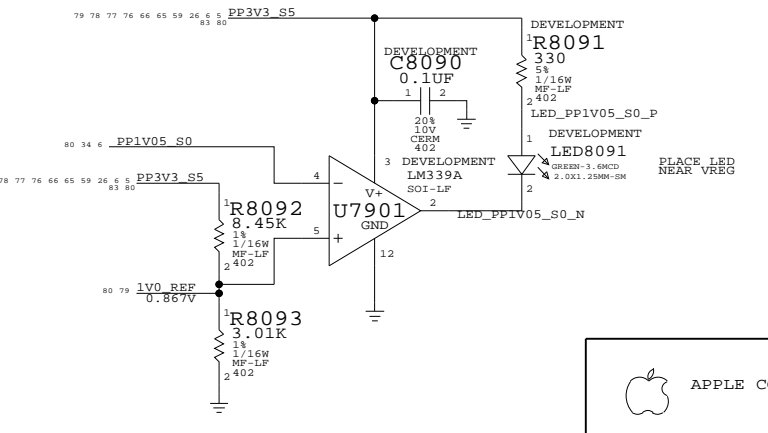
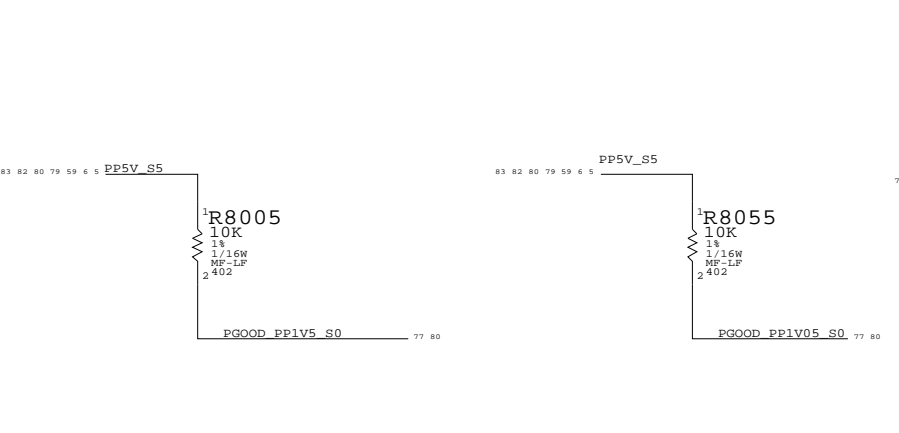
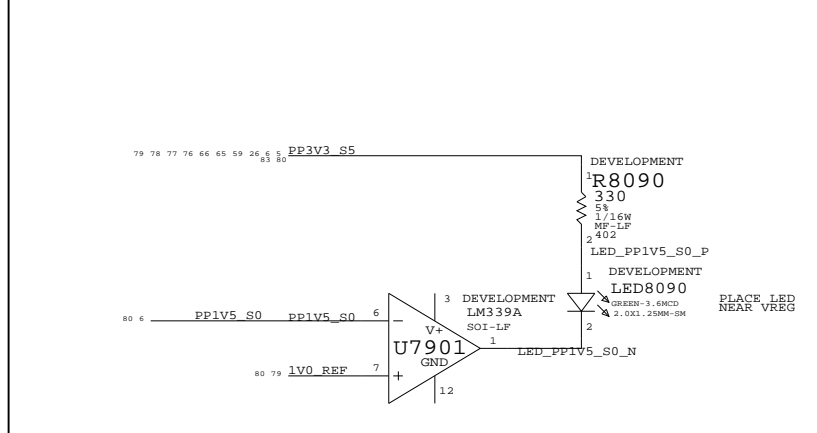
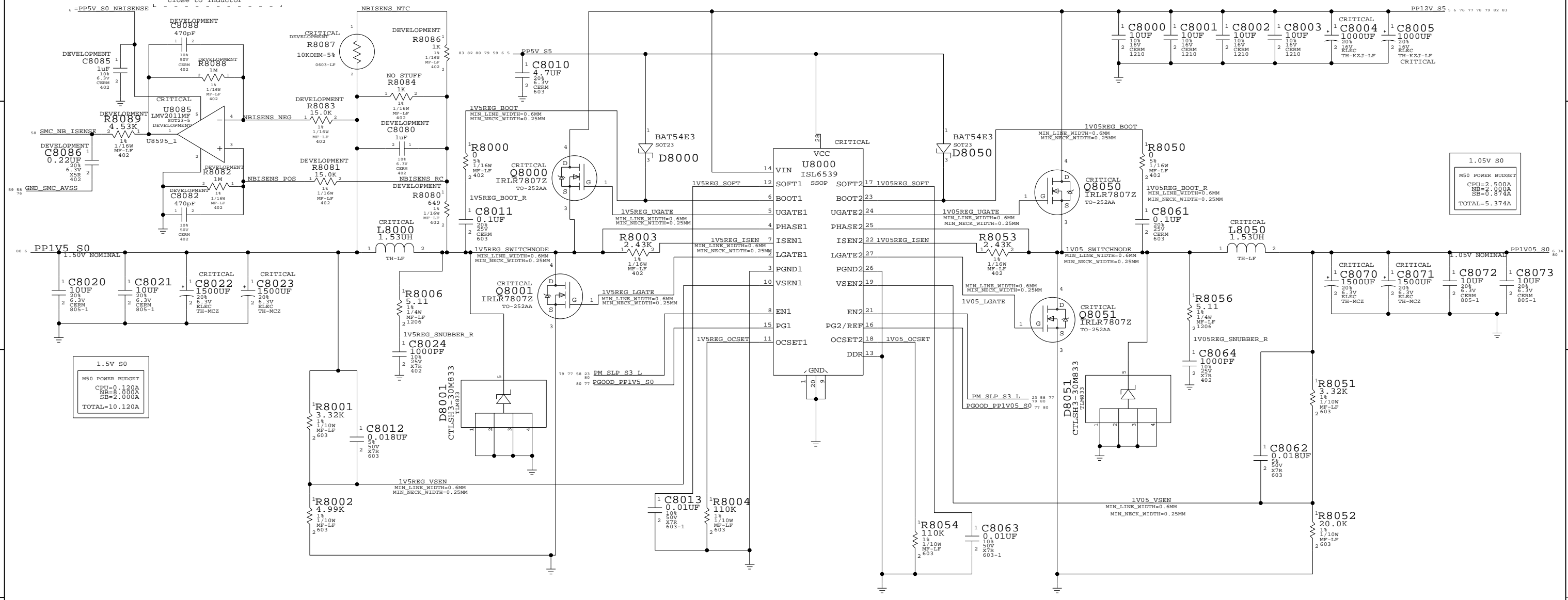


1.8V & 1.2V VREG
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	??
SCALE	SHT	79 OF 97	
NONE			

1.5V S0 AND 1.05V S0 RAILS

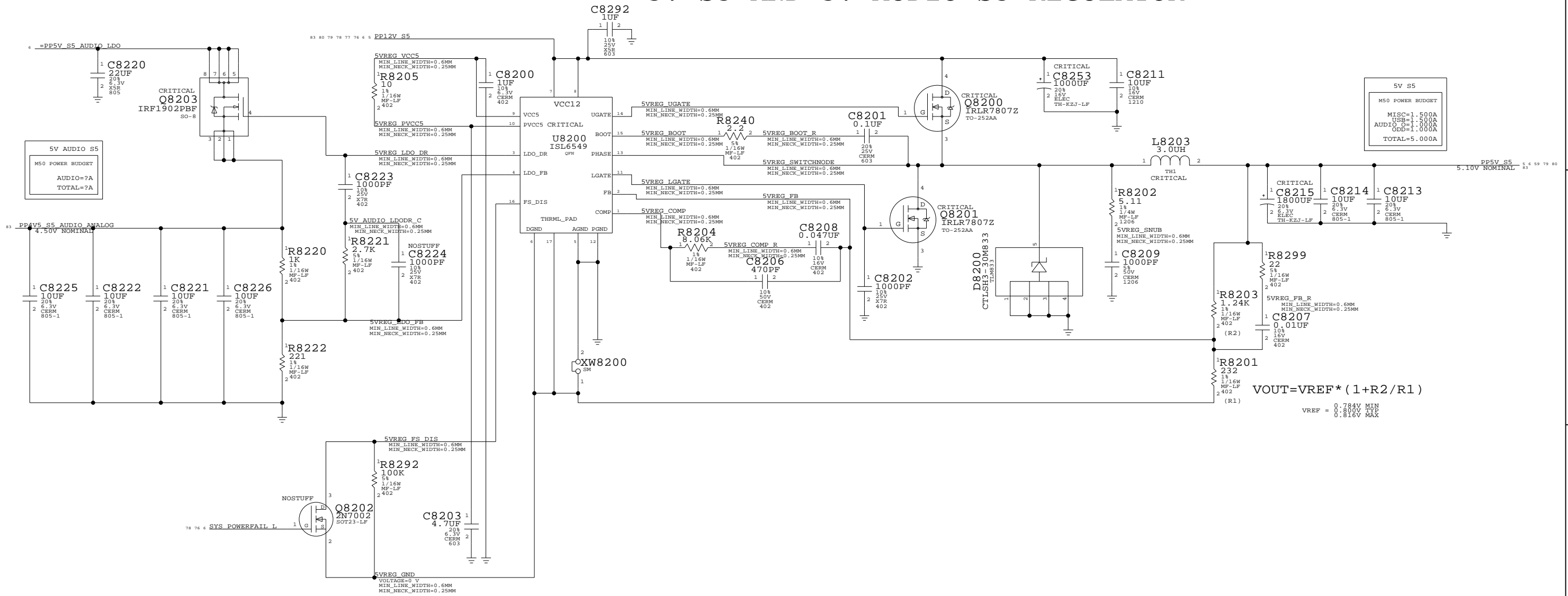
Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	??
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

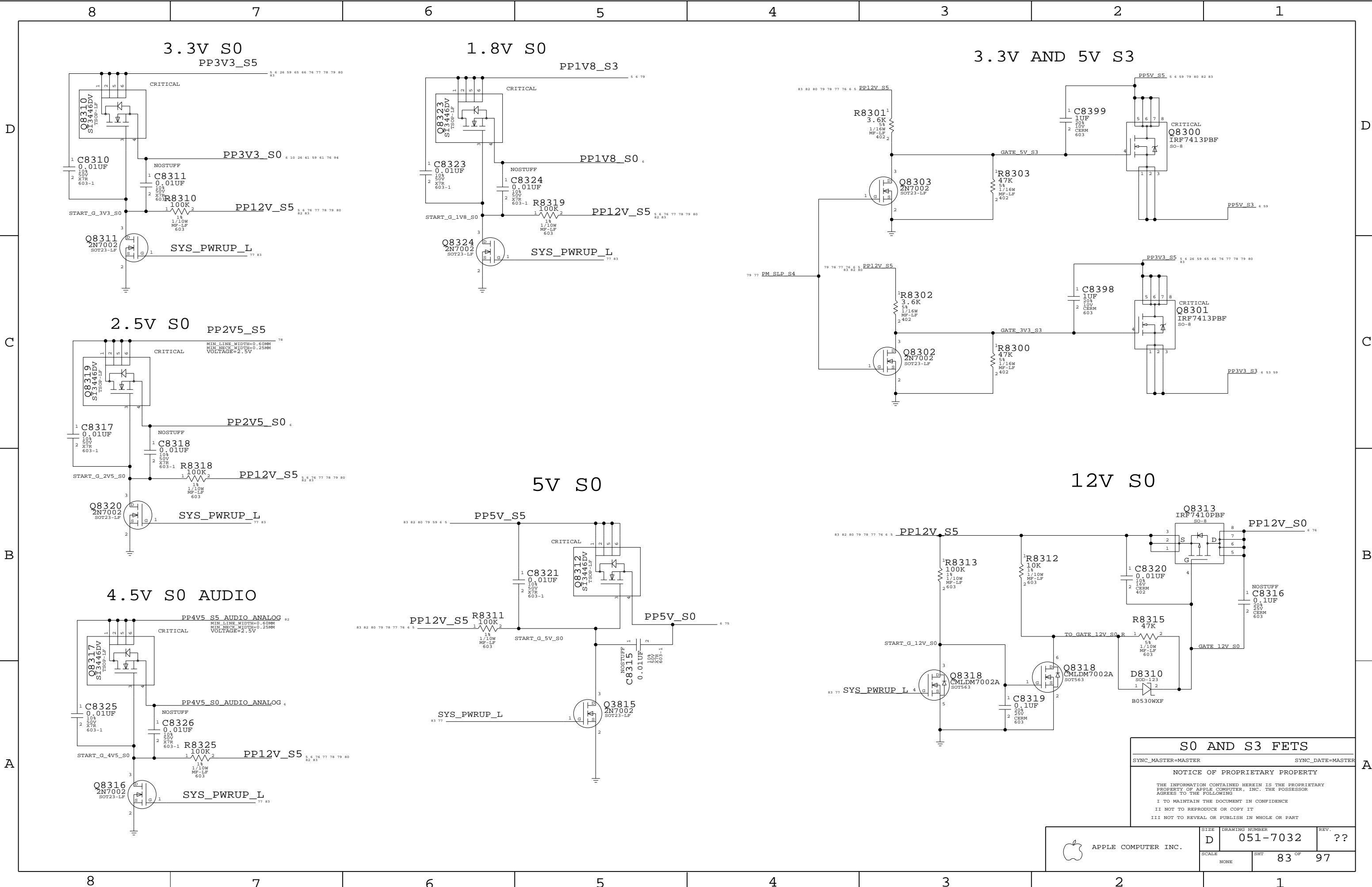
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	D	051-7032	??
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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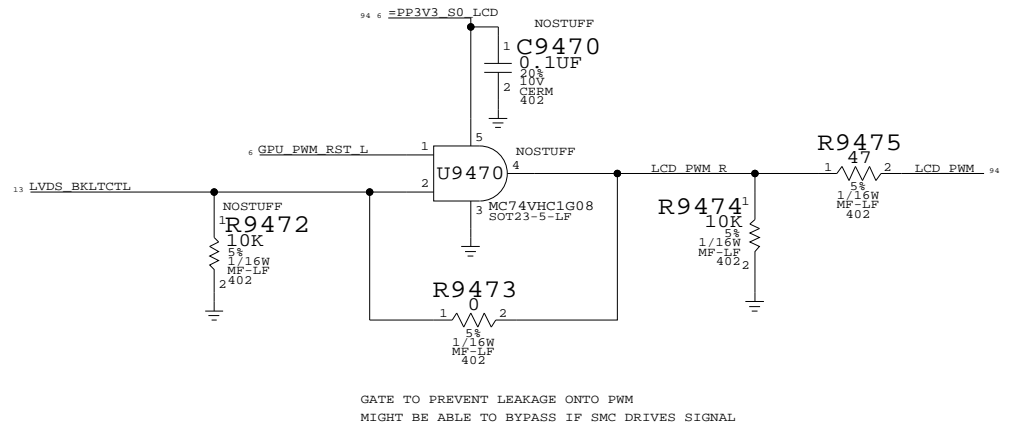
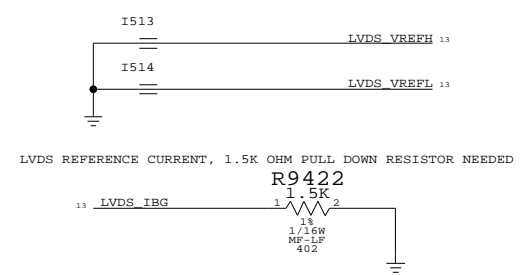
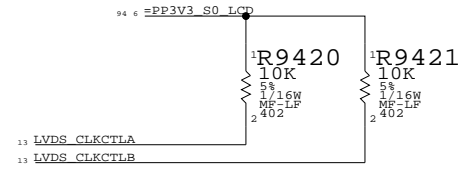
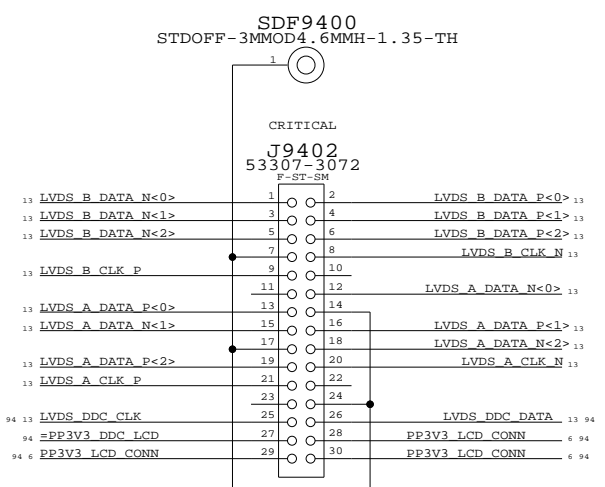
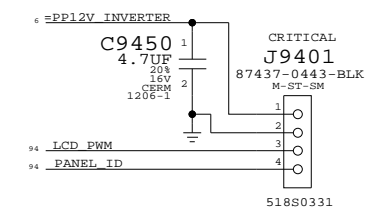
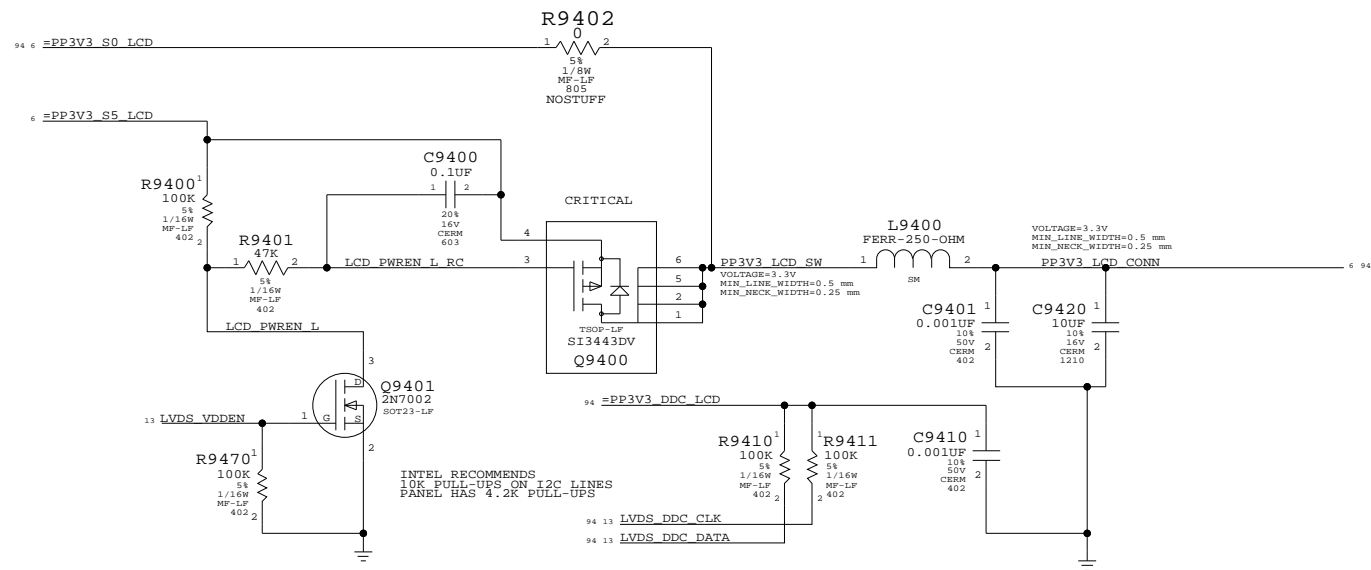
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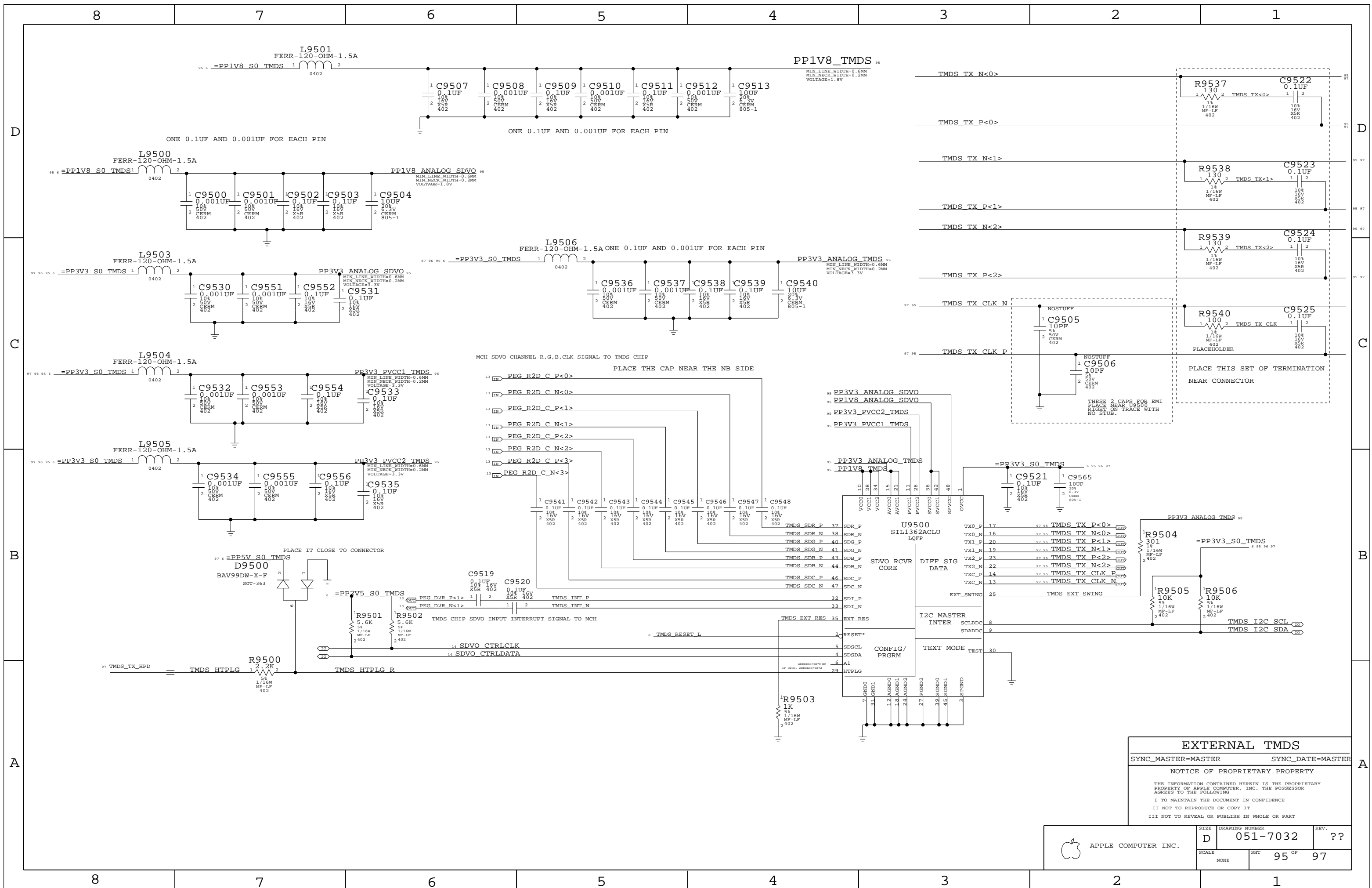
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
SCALE NONE	SHEET 83	OF 97	

LCD (LVDS) INTERFACE

INVERTER INTERFACE



Internal Display Conns
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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EXTERNAL TMSD

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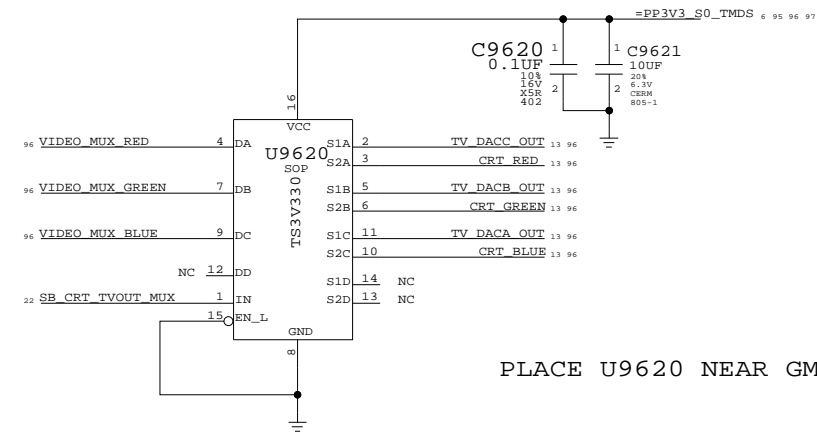
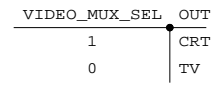
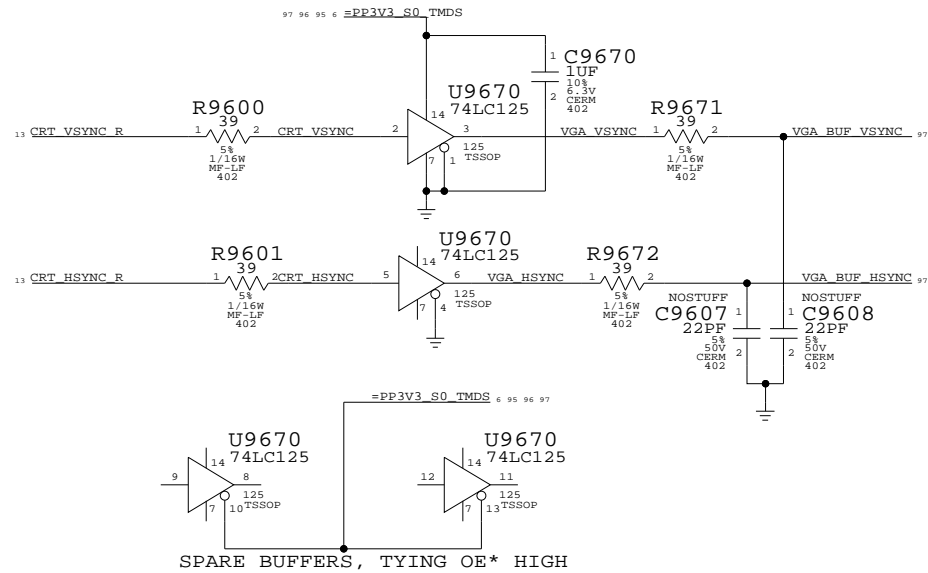
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 95 OF 97	

U9500
SIL1362ACLU

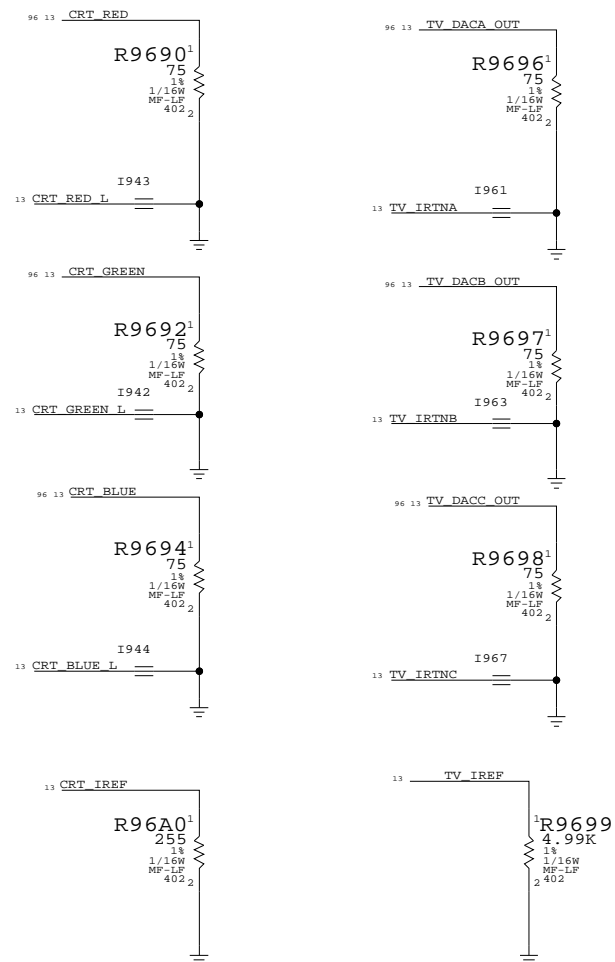
10	VCC0	17	TX0_P	97, 95	TMDS TX P<0>
11	VCC1	16	TX0_N	97, 95	TMDS TX N<0>
12	VCC2	19	TX1_P	97, 95	TMDS TX P<1>
13	VCC3	20	TX1_N	97, 95	TMDS TX N<1>
14	AVCC0	23	TX2_P	97, 95	TMDS TX P<2>
15	AVCC1	22	TX2_N	97, 95	TMDS TX N<2>
16	AVCC2	14	TXC_P	97, 95	TMDS TX CLK P
17	AVCC3	13	TXC_N	97, 95	TMDS TX CLK N
18	PVCC1	25	EXT_SWING		TMDS EXT SWING
19	PVCC2				
20	PVCC3				
21	SVCC1				
22	SVCC2				
23	SVCC3				
24	SPVCC				
25	OVC0				
26					
27					
28					
29					
30					
31	GND1				
32	GND2				
33	AGND0				
34	AGND1				
35	AGND2				
36	AGND3				
37	AGND4				
38	AGND5				
39	AGND6				
40	AGND7				
41	AGND8				
42	AGND9				
43	AGND10				
44	AGND11				
45	AGND12				
46	AGND13				
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96	AGND63				
97	AGND64				

VGA SYNC BUFFERS

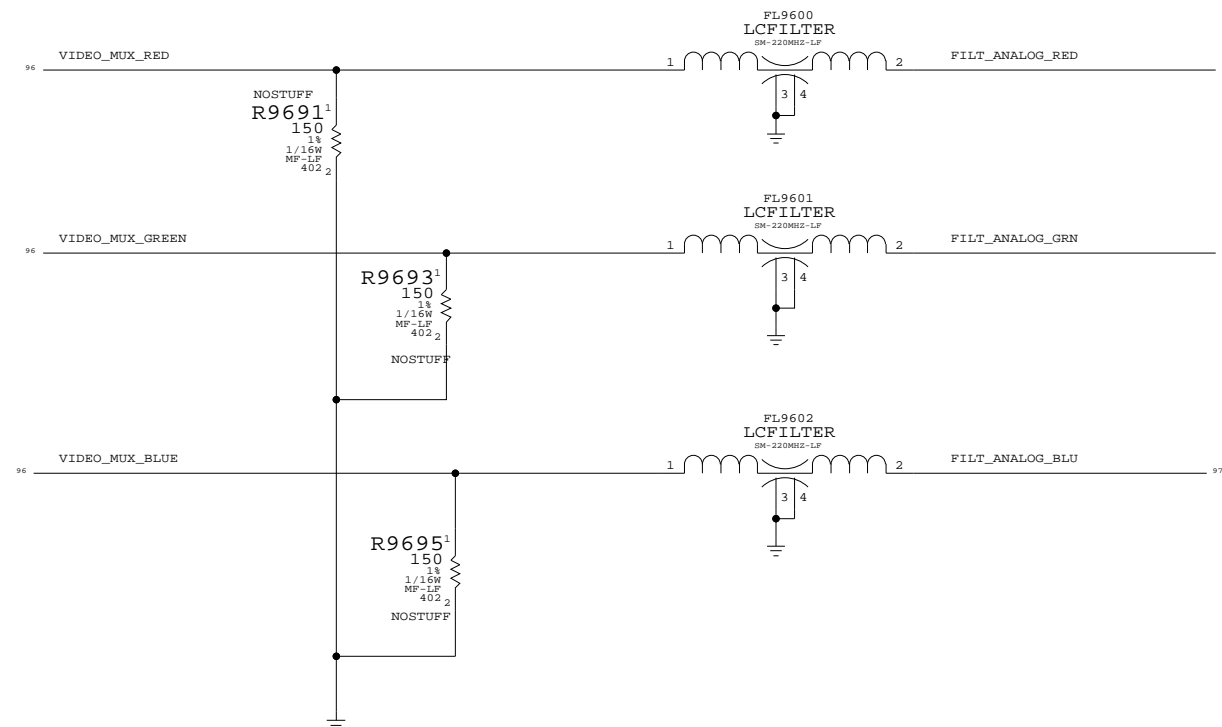


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE



ANALOG FILTERING PLACE BY CONNECTOR

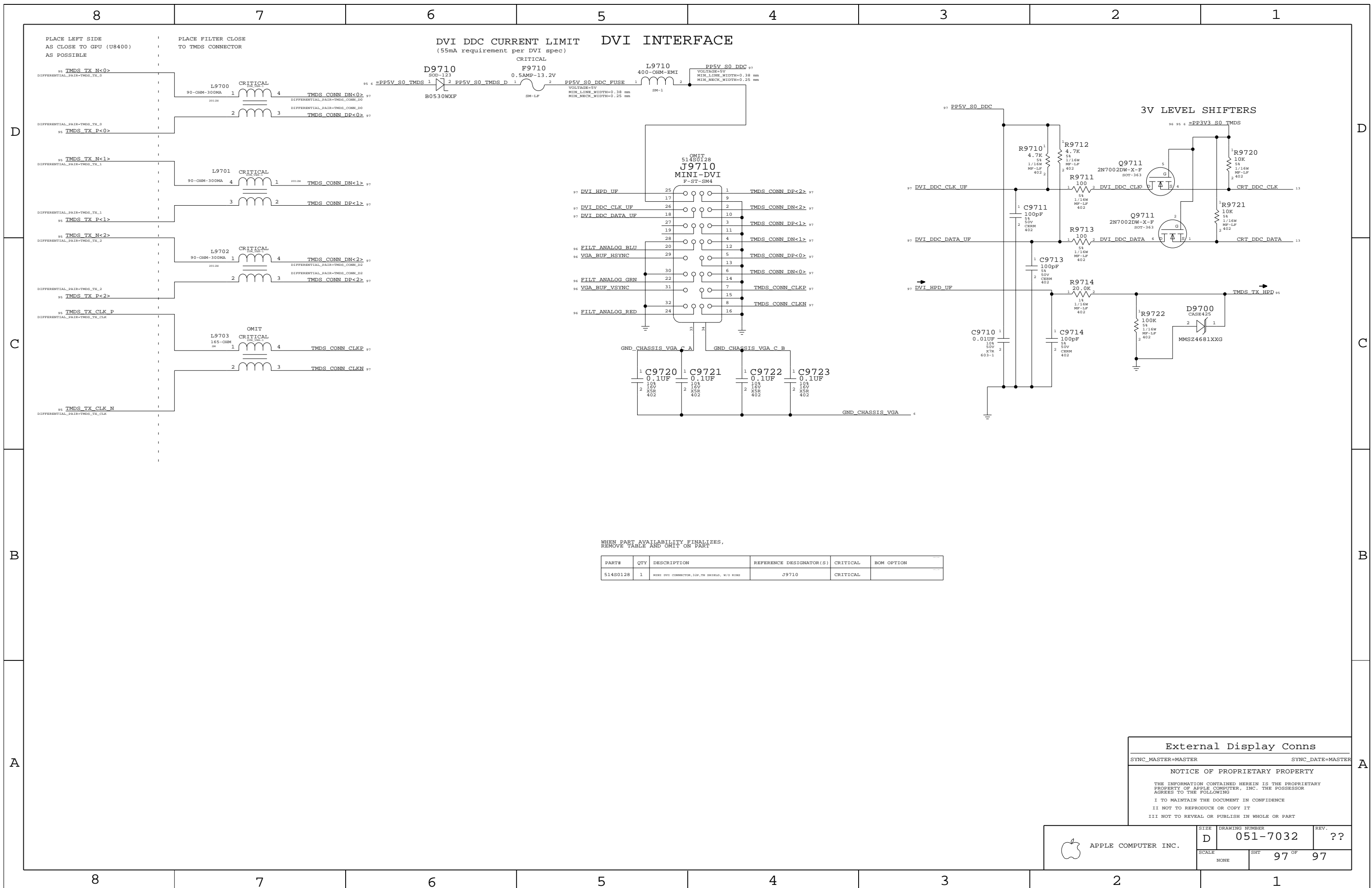


TMDS/Inverter/ExtVGA
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	D	051-7032	??
SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE
(55mA requirement per DVI spec)

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 32P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns
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SCALE	SHT		97 OF 97
NONE			