1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
E		408395	PRODUCTION RELEASED	11/02/05	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6839	1	SCHEM,BOZEMAN,Q41C	SCH1		
820-1810	1	PCBF,BOZEMAN,Q41C	PCB1	CRITICAL	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:SYV]	CRITICAL	EEE_SYV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:TML]	CRITICAL	EEE_TML
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USH]	CRITICAL	EEE_USH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USJ]	CRITICAL	EEE_USJ

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17"

DRAWING NUMBER 051-6839 REV. E

SHT 1 OF 115

Design-Specific Rules

TABLE_SPACING_RULE

TABLE_SPACING_RULE

STANDARD	=DEFAULT	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
BGA_P1MM	10	*	0.10 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM
BGA_P2MM	20	*	0.20 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM
DEFAULT		*	0.1 MM	2.5 MM	0.15 MM	10.0 MM	15.0 MM

TABLE_SPACING_ASSIGNMENT

*	*	1MM	BGA_P1MM
AGP_STB	*	1MM	BGA_P2MM
CLOCK	*	1MM	BGA_P2MM
RAM_DIFF	*	1MM	BGA_P2MM

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.

"BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

TABLE_PHYSICAL_RULE

STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
DEFAULT	*	Y	0.100 MM	0.100 mm	1.25 MM

Layer-specific rules for 90-ohm differential impedance

TABLE_SPACING_RULE

90_OHM_DIFF	TOP,BOTTOM		2.5 MM	0.200 MM	2.5 MM	1.0 MM
90_OHM_DIFF	*		2.5 MM	0.200 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

90_OHM_DIFF	TOP,BOTTOM	Y	0.118 MM	0.1 MM	5 MM
90_OHM_DIFF	*	Y	0.125 MM	0.1 MM	5 MM

Layer-specific rules for 100-ohm differential impedance

TABLE_SPACING_RULE

100_OHM_DIFF	TOP,BOTTOM		2.5 MM	0.200 MM	2.5 MM	1.0 MM
100_OHM_DIFF	*		2.5 MM	0.200 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

100_OHM_DIFF	TOP,BOTTOM	Y	0.092 MM	0.1 MM	5 MM
100_OHM_DIFF	*	Y	0.100 MM	0.1 MM	5 MM

Layer-specific rules for 110-ohm differential impedance

TABLE_SPACING_RULE

110_OHM_DIFF	TOP,BOTTOM		2.5 MM	0.330 MM	2.5 MM	1.0 MM
110_OHM_DIFF	*		2.5 MM	0.300 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

110_OHM_DIFF	TOP,BOTTOM	Y	0.080 MM	0.1 MM	5 MM
110_OHM_DIFF	*	Y	0.085 MM	0.1 MM	5 MM

Portable-specific Override Rules

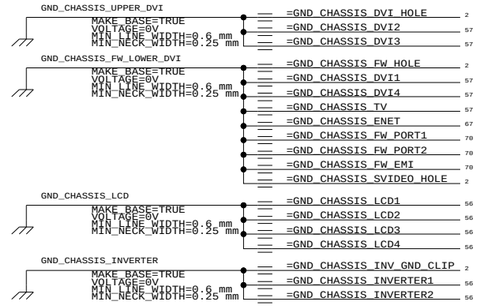
TABLE_SPACING_RULE

AGP	201	*	0.2 MM			
AGP_STB	251	*	0.25 MM			
VGA	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TV	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

TABLE_PHYSICAL_RULE

VGA	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE
TV	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

CHASSIS GND CONNECTIONS



Layer-specific rules for 60-ohm single-ended impedance

TABLE_SPACING_RULE

TABLE_PHYSICAL_RULE

60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE

Layer-specific rules for 50-ohm single-ended impedance

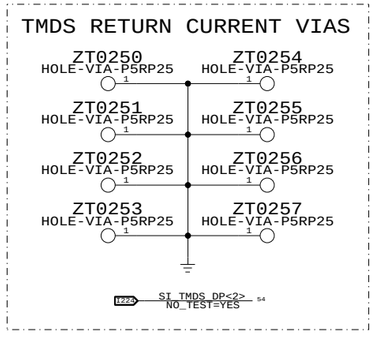
TABLE_SPACING_RULE

50_OHM_SE	*		2.5 MM	0.125 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

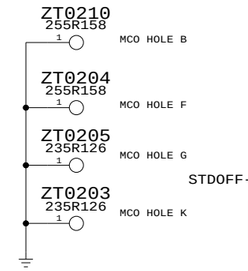
50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM

TMDS RETURN CURRENT VIAS



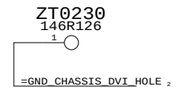
BOARD HOLES

HEATSINK MOUNTS

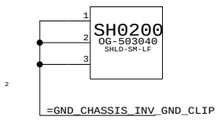


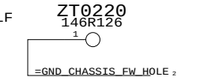
CHASSIS MOUNTS

MECH. HOLES

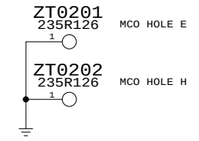


INVERTER

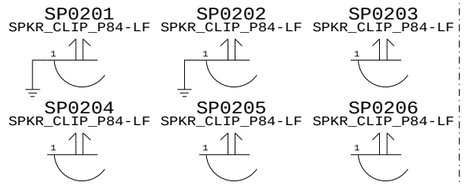




PCB MOUNTS

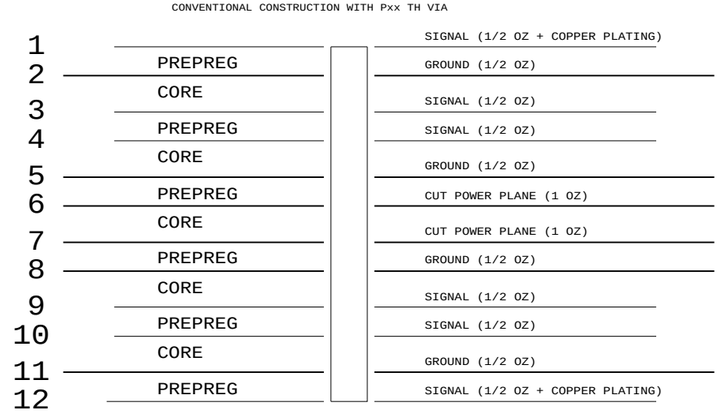


SPEAKER CLIPS



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA



TABLE_BOARD_INFO

TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM NO_TYPE,1MM MM

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7017	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_S,Q41C	COMMON,ALTERNATE,EEE_SYV,GPU_LF,VRAM_SAMSUNG,gQ41C,gCommon
630-7186	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_H,Q41C	COMMON,ALTERNATE,EEE_TML,GPU_LF,VRAM_HYNIX,gQ41C,gCommon
630-7443	PCBA,MLB,BESTMHZ,GPU_EUT,VRAM_S,PB17	COMMON,ALTERNATE,EEE_USH,GPU_EUTECTIC,VRAM_SAMSUNG,gQ41C,gCommon
630-7444	PCBA,MLB,BESTMHZ,GPU_EUT,VRAM_H,PB17	COMMON,ALTERNATE,EEE_USJ,GPU_EUTECTIC,VRAM_HYNIX,gQ41C,gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC,BACKUP_BATT,CPU_A7PM,I2_FW_BETA,I2_MAXBUS_50OHM,MAXBUS_1V8,gCommon1
gCommon1	MMM_ACCEL_KIONIX,GPU_PWRPLAY,GPU_SS,GPU_LVDDR_2V8,GPU_MEMIO_1V8,gCommon2
gCommon2	I2_REV1_NOT,I2_MAXBUS_FBCLK_MATCHED,I2_AGP_FBCLK_MATCHED,I2_PCI_FBCLK_MATCHED,gCommon3
gCommon3	CPU_VCORE_2STATES,I2_MAXBUS_166MHZ,CPU0_BUSRATIO_10.0X,I2VCORE_1V5,I2VCORE_BURST,gCommon4
gCommon4	VESTA_PORT2_DISABLE,DVO_1V8,TMDS_DUAL,VCORE_OFFSET,VCORE_OFFSET_SW,gUSB
gUSB	USB2_NEC,USB1P1_NEC,TPAD_SEQ_PMU
gQ41C	Q41C_PARTS,A7PM_1P67_LGA,BOOTROM_PROG,PMU_PROG,MAXBUS_TBEN_SYNC,gQ41CVcore
gQ41CVcore	CPU0_VCORE_1V30,Q41,CPU0_AVDD_1V30

Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0383	1	IC,ASIC,I2,REV1.2,NB/SB,974 BGA	U2100	CRITICAL	
337S3135	1	IC,PMU05,BLANK,QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC,PMU05,Vxxx,QFP	U2700	CRITICAL	PMU_PROG
337S3181	1	IC,A7PM,R1.5,1.67GHZ,LGA,1.28V,25W,85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC,A8,xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC,GPU,M11P	U5700	CRITICAL	GPU_LF
338S0299	1	IC,GPU,M11P,EUTECTIC	U5700	CRITICAL	GPU_EUTECTIC
335S0088	1	BOOTROM,BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1739	1	IC,BOOTROM,B,Q41C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U8500	CRITICAL	
333S0317	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0388	343S0356	?	U8500	v1.4 is alt to v1.3

Board Information

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 2 OF 115	

J8600
Ethernet Connector P.67
4 DATA PAIRS
J9020
FW - A Connector P.70
2 DATA PAIRS @ 200MHz
J9010
FW - B Connector P.70
2 DATA PAIRS @ 400MHz
U8500
Ethernet P.66
Vesta Combo PHY
FireWire P.69
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ
1394 OHCI
3.3V
8BIT TX/RX
100MHZ
J8200/J8250
HDD/ODD Connectors P.64
UATA
ETHERNET 10/100/1000 P.65
FIREWIRE 800 Mb/S P.68
UATA 100 P.63
UNUSABLE
USB2.0 PORTS A-F P.73
MAXBUS P.32
U2100
I2
I2S X2 P.21
I2C X2 P.21
SCCA P.21
VIA/PMU P.21
BOOTROM P.21
PCI 32BITS 33MHZ P.59
4X AGP P.43
J3320
SW MODEM Connector P.30
JA000
Audio Connector P.74
I2S
I2C
U3000
Fan Circuit P.27
J2690
Serial Debug Connector P.24
U7100
BOOT ROM 1M X 8 P.58
J7300
AIRPORT Connector P.60
J1250
Battery Connector P.12
U1250
BATTERY CURRENT SENSOR P.12
SLEEP LED P.24
SMBUS 3.3V
U2700
PMU P.25
U3220
SMS Sensor P.29
ALS Sensors
J3400
DC-In Connector P.31
Power Supply & Charger P.13-17
J7400
CARDBUS Connector P.61
33MHZ
16/32 BITS
3.3V/5V
U7400
TI PCI1510 CardBus Controller P.61
PCI BUS
32BITS
33MHZ
3.3V
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U5700
ATI M11P P.44-53
MEMORY BUS
1.8V
240MHZ
64BITS
(x2 Channels)
MEMORY CH A U6200/U6250 P.49
MEMORY CH B U6300/U6350 P.50
128MB
U7500
NEC USB2.0 EHCI HC P.62
LEFT USB2 CONN
RIGHT USB2 CONN
BlueTooth (1.1) P.60
Trackpad (1.1) P.30
MAXBUS
1.8V
167MHZ
32BIT ADDR
64BIT DATA
U3600
A7PM CPU (MPC7448) P.33-35
CPU PLL Config P.7
J5000/J5200
MEMORY BUS
1.8V
167MHZ
64BITS
DDR2 SDRAM DIMM 0
DDR2 SDRAM DIMM 1 SO-DIMM Connector P.40/41
DDR2 MEMORY P.47
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1178)
RGB
DDC
J6950
Inverter Connector P.56
J6900
LCD Panel Connector P.56
J7060
S-Video Connector P.57
J7000
DVI-I Connector P.57

System Block Diagram

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 3 OF 115

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN

INRUSH LIMITER

+24V_PBUS

1V20_REF

>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

RUN/SS

BUCK VCC REGULATOR (LTC1625)

AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

RC AT 1M*0.047UF @ 24V

+PBUS

BACKLIGHT INVERTER

5V_PWRON

VCC
MAIN 1.8V/1.5V DC/DC (MAX1715)

PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V
ON1/ON2

MAXBUS
VRAM CORE
VRAM I/O
DDR2 POWER

1V8_PWRON

1V8_1V5_OK

1V5_PWRON

AGP I/O

+PBUS

5V_PWRON

VCC
DC/DC (MAX1717)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.3V)

14V_PBUS

3V3_ALL LDO

+BATT

5V_PWRON

PMU

3V3_ALL

4V6_ALL

RUN/SS - 5V

TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707)

VCC

PGOOD

STBYMD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V

RUN/SS - 3V

5V_PWRON

3V_5V_OK

HOLDS BOTH RUN/SS AT GND
WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS
WHEN IT'S OPEN

3V3_PWRON

RC AT 1M*0.1UF @ 24V

+PBUS

5V_PWRON

EXT_VCC

VCC

DC/DC (LTC1778)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS

GPU_VCORE +1.3V

14V_PBUS

BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3412)

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

2V5_PWRON

DC/DC (LTC3412)

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

I2_CORE +1.5V

BATTERY CHARGER (MAX1772)

+BATT

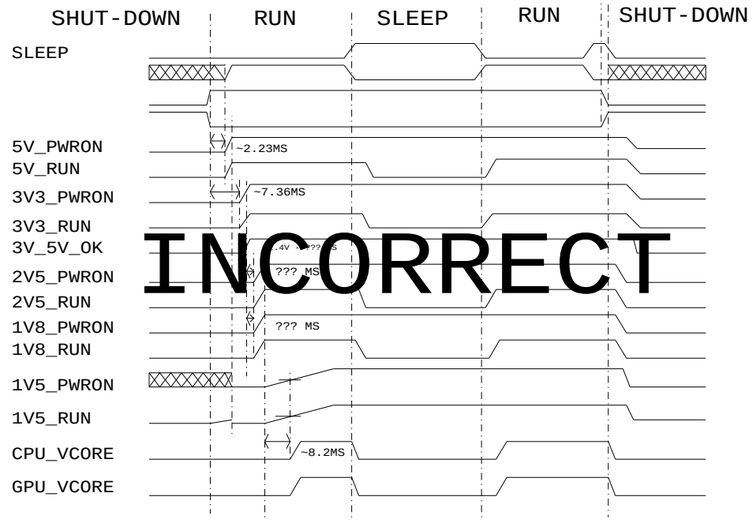
3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH

+PBUS

POWER SEQUENCE
(CONTROLLED BY PMU)



INCORRECT

Power Block Diagram

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE NONE

SHT 4 OF 115

REVISION HISTORY

PROTO

04/05/2005 - Beginning revision history
- Sync'd FB pin swaps from 051-5838
- Pinned out audio connector per flex cable
- Pinned out left USB/ALS connector per flex cable
04/07/2005 - Moved modem connector to non-shared page
- Updated chassis ground connections
- Pin swapped DDR2 according to layout
04/11/2005 - Changed audio caps to X5R (CA033, CA050, CA051).
04/12/2005 - Updated wireless connector pinout according to flex
- Implemented more DDR2 pin swaps
- Implemented pin swaps on FW data lines
- Added RAM_DQS_N pulldowns
04/14/2005 - Corrected mosf line and neck width properties
04/15/2005 - Added CPU_Vcore mux circuit
04/19/2005 - Added NO_TEST property to buses between JTAG enabled devices
- Pinswapped FB Y/P for M11
04/20/2005 - Corrected ENET power rail to PWRON instead of RUN (Wake-on-LAN)
- Corrected Vesta reset and ethernet LOWPWR circuits
- Changed Rs680 to 6.34k to take GPU Vcore to 1.3V/1.05V
- Added page 6 and modified pages 11,35,61 for design specific pin swaps
- Separated gpu_MVREF into two dividers
04/26/2005 - Added 8 vias for TMDS return current
- Added MVS electrical constraints properties
04/27/2005 - Added NO_TEST_PROBE property to SI_TMDS_DBG_RS (no room for TP)
- Changed MIN_NECK_WIDTH property on TMDS power rails to 0.2 mm
- Changed gender of debug connector
- Removed C6367 due to MCO violation
04/29/2005 - Schematic released as REV 01 for PROTO

EVT

05/04/2005 - Added SYNONYMS to allow DVO and USB pulldown pinswaps
05/09/2005 - Added missing pullup to SYS_LID_OPEN
- Added missing pulldown to Vesta LPWR_1394
05/09/2005 - Lead-free resistor replacement on page 86
05/16/2005 - Various lead-free replacements
- Added Hynix VRAM option and PCBA
05/17/2005 - Added 2 0.1uF caps to VGA sync buffers
05/25/2005 - Added NEC USB2 controller and PCI clock buffer
- Various lead-free replacements
- Added pullup to BATT0_DET
05/26/2005 - Removed SMS ptc microcontroller
05/31/2005 - Added 2 0.1uF caps to GPU Vcore output
- Corrected USB diff pair and spacing/physical rules on ports
06/01/2005 - Corrected caps on FireWire v8 rail to 50V
- Various lead-free replacements

DVT

06/28/2005 - Added 10K pullup to VIA_REQ_L
- Changed Q2941 to level shift/pass FET to correct GPU VCore and CPU_Vcore power sequencing
- Moved R2933 to SYS_PWRSEQ_L1 to correct trackpad power state in sleep
- Moved +3V3_SB_SB to RUN rail to correct pumpup problem in sleep
- Changed to USB1P1_REC BOMOPTION
07/06/2005 - Various Pb-free replacements
- Changed TMDS drive strength resistors to 301 ohm, which was built at EVT
- Added FET to allow PMU control of trackpad power sequencing
07/08/2005 - Added resistor mux for I2'S MAXBUS I/O rail (PWRON vs RUN)
07/08/2005 - Changed CPU Vcore to 2-states only (no MUX).
- Removed I2'S connection to TBEN (leakage path)
- Changed 32.768kHz crystal to new ADM specifing 1uW drive parts
- Added line width constraints to LTC1625 and CPU_Vcore gate nodes
07/14/2005 - Added external 1K pullups in parallel with all I2 internal pullups
07/18/2005 - Changed NEC USB2 series R value to 39.2 ohm
- Added 150 ohm pulldowns to FW_CTL lines at Vesta
- Changed TMDS transmitter ferrites to part with higher current rating (1.5A)
- Added BOMOPTIONs for and stuffed CPU Vcore at 1.28V and 1.30V
07/19/2005 - Added audio mute sequencing FETs
- Moved DATA_DSTROBE cap to other side of series resistor
- Released as REV 06 for DVT
07/22/2005 - Changed all external I2_GPIO pullups to 10K
- Stuffed R2452, R2482, R2483 to correct I2 2.5V pullup problem
- Released as REV 04 for DVT
07/25/2005 - Replaced 371s0299 with 371s0300
- Swapped I2_MAXBUS 33OHM and I2_MAXBUS_50OHM_BOMOPTIONs
- Changed to Vesta v1.4 as primary U8500, Vesta v1.3 as alternate
07/26/2005 - Changed PCI_AD6 output series term to 22 ohms
- Swapped locations (i.e. values) of C2500 and C2501
07/29/2005 - Released as REV 05 for DVT
08/03/2005 - Added R3746 on CPU0_TMLG_VCC 10K pull down.
- Added R3065 on CPU0_TMLG_VCC 10K pull down (no stuff).
- Changed C1724 and C2285 to 2200pF.
- Changed C1730 to 5.6pF.
- Changed C1700 and C1701 and C2215 and C2216 to 47uF.
- Changed R1720 and R2205 to 7.5K.
- Released as REV 06 for DVT

Pre-PVT

08/10/2005 - Replaced C3940-C3947 with ceramic caps
08/17/2005 - Changed power supply solder jumpers to shorts
- Added five ceramic caps to Vcore supply input
- Changed D1400,D1401 to 60V schottky to reduce reverse leakage
08/18/2005 - Changed R2958 to 10K to improve power sequencing timing
08/22/2005 - Added FETs to control leakage on Vesta rails
08/24/2005 - Changed C8600-C8603 to 1uF due to FET isolation
- Changed R5922 to 100K for power sequencing improvements
- NO STUFFed R2969 for power sequencing improvements
- Released as REV 07 for Pre-PVT

PVT

08/29/2005 - Released as REV A for PVT/Production
09/02/2005 - Stuffed R8420 with 10K, 5% to ensure MDIO logic levels
- Stuffed R2464 to correct unused GPIO logic level

E

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT	OF
NONE	5	115

I2S Series Rs

MAKE_BASE=TRUE	22	I2S0_SB_TO_DEV_DTO_R	=RP1150P1	11	11	=RP1150P8	I2S0_SB_TO_DEV_DTO	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_BITCLK_R	=RP1150P2	11	11	=RP1150P7	I2S0_BITCLK	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_MCLK_R	=RP1150P3	11	11	=RP1150P6	I2S0_MCLK	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_SYNC_R	=RP1150P4	11	11	=RP1150P5	I2S0_SYNC	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SB_TO_DEV_DTO_R	=RP1151P1	11	11	=RP1151P8	I2S1_SB_TO_DEV_DTO	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SYNC_R	=RP1151P2	11	11	=RP1151P7	I2S1_SYNC	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_MCLK_R	=RP1151P3	11	11	=RP1151P6	I2S1_MCLK	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_BITCLK_R	=RP1151P4	11	11	=RP1151P5	I2S1_BITCLK	30	MAKE_BASE=TRUE

UATA Series Rs

MAKE_BASE=TRUE	63	UATA_DD_R<12>	=RP8150P1	63	63	=RP8150P8	UATA_DD<12>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_CS0_L_R	=RP8150P2	63	63	=RP8150P7	UATA_CS0_L	7 63 64	MAKE_BASE=TRUE	(IDE_CS1FX_L)	
MAKE_BASE=TRUE	63	UATA_DD_R<14>	=RP8150P3	63	63	=RP8150P6	UATA_DD<14>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<11>	=RP8150P4	63	63	=RP8150P5	UATA_DD<11>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<7>	=RP8151P1	63	63	=RP8151P8	UATA_DD<7>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<2>	=RP8151P2	63	63	=RP8151P7	UATA_DD<2>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<3>	=RP8151P3	63	63	=RP8151P6	UATA_DD<3>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<15>	=RP8151P4	63	63	=RP8151P5	UATA_DD<15>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<9>	=RP8152P1	63	63	=RP8152P8	UATA_DD<9>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<4>	=RP8152P2	63	63	=RP8152P7	UATA_DD<4>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<6>	=RP8152P3	63	63	=RP8152P6	UATA_DD<6>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<5>	=RP8152P4	63	63	=RP8152P5	UATA_DD<5>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DA_R<2>	=RP8153P1	63	63	=RP8153P8	UATA_DA<2>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<8>	=RP8153P2	63	63	=RP8153P7	UATA_DD<8>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<10>	=RP8153P3	63	63	=RP8153P6	UATA_DD<10>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DA_R<0>	=RP8153P4	63	63	=RP8153P5	UATA_DA<0>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<13>	=RP8154P1	63	63	=RP8154P8	UATA_DD<13>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<0>	=RP8154P2	63	63	=RP8154P7	UATA_DD<0>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<1>	=RP8154P3	63	63	=RP8154P6	UATA_DD<1>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DA_R<1>	=RP8154P4	63	63	=RP8154P5	UATA_DA<1>	7 63 64	MAKE_BASE=TRUE		

MAXBUS Pullups

MAKE_BASE=TRUE	33 32	MAXBUS_TS_L	=RP3510P1	32	
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BG_L	=RP3510P2	32	
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DBG_L	=RP3510P3	32	
MAKE_BASE=TRUE		NC_MAXBUS_TBEN_I2 NO_TEST=YES	=RP3510P4	32	
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BG_L	=RP3511P1	32	
MAKE_BASE=TRUE	32	MAXBUS_CPU1_HIT_L	=RP3511P2	32	
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_HIT_L	=RP3511P3	32	
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BR_L	=RP3511P4	32	
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BR_L	=RP3512P1	32	
MAKE_BASE=TRUE	33 32	MAXBUS_TA_L	=RP3512P2	32	
MAKE_BASE=TRUE	34 32	MAXBUS_CPU0_INT_L	=RP3512P3	32	
MAKE_BASE=TRUE	32	MAXBUS_CPU1_INT_L	=RP3512P4	32	
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DRDY_L	=RP3513P2	32	
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DRDY_L	=RP3513P3	32	
MAKE_BASE=TRUE	33 32	MAXBUS_AACK_L	=RP3513P4	32	
MAKE_BASE=TRUE	33 32	MAXBUS_ARTRY_L	=RP3514P1	32	
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DBG_L	=RP3514P2	32	
MAKE_BASE=TRUE	33 32	MAXBUS_TEA_L	=RP3514P3	32	

AGP Pullups

MAKE_BASE=TRUE	44 43	AGP_TRDY_L	=RP5610P1	43	
MAKE_BASE=TRUE	44 43	AGP_IRDY_L	=RP5610P2	43	
MAKE_BASE=TRUE	44 43	AGP_REQ_L	=RP5610P3	43	
MAKE_BASE=TRUE	44 43	AGP_RBF_L	=RP5610P4	43	
MAKE_BASE=TRUE	44 43	AGP_FRAME_L	=RP5611P1	43	
MAKE_BASE=TRUE	44 43	AGP_DEVSEL_L	=RP5611P2	43	
MAKE_BASE=TRUE	44 43	AGP_STOP_L	=RP5611P3	43	
MAKE_BASE=TRUE	44 43	AGP_GNT_L	=RP5611P4	43	

PCI Pullups

MAKE_BASE=TRUE	11	PCI_AIRPORT_GNT_L	=RP7250P1	59	
MAKE_BASE=TRUE	60 59 62 61	PCI_TRDY_L	=RP7250P2	59	
MAKE_BASE=TRUE	60 59 62 61	PCI_IRDY_L	=RP7250P3	59	
MAKE_BASE=TRUE	60 59 62 61	PCI_STOP_L	=RP7250P4	59	
MAKE_BASE=TRUE	11	PCI_CBUS_REQ_L	=RP7251P1	59	
MAKE_BASE=TRUE	11	PCI_AIRPORT_REQ_L	=RP7251P2	59	
MAKE_BASE=TRUE	11	PCI_CBUS_GNT_L	=RP7251P3	59	
MAKE_BASE=TRUE	60 59 62 61	PCI_FRAME_L	=RP7251P4	59	

FW Series Rs

MAKE_BASE=TRUE	68 9	FW_D_R<3>	=RP9100P1	71	71	=RP9100P8	FW_D<3>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<1>	=RP9100P2	71	71	=RP9100P7	FW_D<1>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<0>	=RP9100P3	71	71	=RP9100P6	FW_D<0>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<2>	=RP9100P4	71	71	=RP9100P5	FW_D<2>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<7>	=RP9101P1	71	71	=RP9101P8	FW_D<7>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<5>	=RP9101P2	71	71	=RP9101P7	FW_D<5>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<6>	=RP9101P3	71	71	=RP9101P6	FW_D<6>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<4>	=RP9101P4	71	71	=RP9101P5	FW_D<4>	9 69	MAKE_BASE=TRUE

Lower DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<0>	=RP6720P1	54	54	=RP6720P8	GPU_DVOD<0>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<1>	=RP6720P2	54	54	=RP6720P7	GPU_DVOD<1>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<2>	=RP6720P3	54	54	=RP6720P6	GPU_DVOD<2>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<3>	=RP6720P4	54	54	=RP6720P5	GPU_DVOD<3>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<11>	=RP6721P1	54	54	=RP6721P8	GPU_DVOD<11>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<10>	=RP6721P2	54	54	=RP6721P7	GPU_DVOD<10>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<9>	=RP6721P3	54	54	=RP6721P6	GPU_DVOD<9>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<8>	=RP6721P4	54	54	=RP6721P5	GPU_DVOD<8>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<6>	=RP6722P1	54	54	=RP6722P8	GPU_DVOD<6>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<4>	=RP6722P2	54	54	=RP6722P7	GPU_DVOD<4>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<7>	=RP6722P3	54	54	=RP6722P6	GPU_DVOD<7>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<5>	=RP6722P4	54	54	=RP6722P5	GPU_DVOD<5>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_HSYNC_R	=RP6723P1	54	54	=RP6723P8	GPU_DVO_HSYNC	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_VSYNC_R	=RP6723P2	54	54	=RP6723P7	GPU_DVO_VSYNC	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_DE_R	=RP6723P3	54	54	=RP6723P6	GPU_DVO_DE	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_CLKP_R	=RP6723P4	54	54	=RP6723P5	GPU_DVO_CLKP	54 55	MAKE_BASE=TRUE

Upper DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<13>	=RP6821P1	55	55	=RP6821P8	GPU_DVOD<13>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<12>	=RP6821P2	55	55	=RP6821P7	GPU_DVOD<12>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<14>	=RP6821P3	55	55	=RP6821P6	GPU_DVOD<14>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<15>	=RP6821P4	55	55	=RP6821P5	GPU_DVOD<15>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<18>	=RP6822P1	55	55	=RP6822P8	GPU_DVOD<18>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<19>	=RP6822P2	55	55	=RP6822P7	GPU_DVOD<19>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<16>	=RP6822P3	55	55	=RP6822P6	GPU_DVOD<16>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<17>	=RP6822P4	55	55	=RP6822P5	GPU_DVOD<17>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<21>	=RP6823P1	55	55	=RP6823P8	GPU_DVOD<21>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<20>	=RP6823P2	55	55	=RP6823P7	GPU_DVOD<20>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<23>	=RP6823P3	55	55	=RP6823P6	GPU_DVOD<23>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<22>	=RP6823P4	55	55	=RP6823P5	GPU_DVOD<22>	55	MAKE_BASE=TRUE

USB Pulldowns

72	=RP9210P8	USB2_I2_LEFT_PORT_P	11	MAKE_BASE=TRUE
72	=RP9210P7	USB2_I2_LEFT_PORT_N	11	MAKE_BASE=TRUE
72	=RP9210P6	USB2_I2_P<1>	72	MAKE_BASE=TRUE
72	=RP9210P5	USB2_I2_N<1>	72	MAKE_BASE=TRUE
72	=RP9211P8	USB2_I2_RIGHT_PORT_P	11	MAKE_BASE=TRUE
72	=RP9211P7	USB2_I2_RIGHT_PORT_N	11	MAKE_BASE=TRUE
72	=RP9211P6	USB2_I2_P<3>	72	MAKE_BASE=TRUE
72	=RP9211P5	USB2_I2_N<3>	72	MAKE_BASE=TRUE
72	=RP9212P8	USB_I2_BT_P	11	MAKE_BASE=TRUE
72	=RP9212P7	USB_I2_BT_N	11	MAKE_BASE=TRUE
72	=RP9212P6	USB_I2_TPAD_P	11	MAKE_BASE=TRUE
72	=RP9212P5	USB_I2_TPAD_N	11	MAKE_BASE=TRUE
73	=RP9300P8	USB2_NEC_LEFT_PORT_P	11	MAKE_BASE=TRUE
73	=RP9300P7	USB2_NEC_LEFT_PORT_N	11	MAKE_BASE=TRUE
73	=RP9300P6	USB2_NEC_RIGHT_PORT_N	11	MAKE_BASE=TRUE
73	=RP9300P5	USB2_NEC_RIGHT_PORT_P	11	MAKE_BASE=TRUE
73	=RP9301P8	USB_NEC_BT_P	11	MAKE_BASE=TRUE
73	=RP9301P7	USB_NEC_BT_N	11	MAKE_BASE=TRUE
73	=RP9301P6	USB_NEC_TPAD_N	11	MAKE_BASE=TRUE
73	=RP9301P5	USB_NEC_TPAD_P	11	MAKE_BASE=TRUE

Q41C Pin Swaps

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 6 OF 115	

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

POWER

E122	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector
E1	PP24V_ALL_PBUSA	10	FUNC_TEST=YES	
E2	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES	
E4	PPVCORE_RUN_GPU	10	FUNC_TEST=YES	
E3	PPVCORE_RUN_CPU	10	FUNC_TEST=YES	
E6	PP1V8_PWRON	10	FUNC_TEST=YES	Place within 50 mm of power supply.
E5	PP2V5_PWRON	10	FUNC_TEST=YES	
E7	PP5V_PWRON	10	FUNC_TEST=YES	
E8	PP3V3_PWRON	10	FUNC_TEST=YES	
E9	PP5V_RUN	10	FUNC_TEST=YES	
E10	PP3V3_ALL	10	FUNC_TEST=YES	
E102	=FTP_GND	7 10	FUNC_TEST=YES	Place 5-10 GND TPs.

LVDS

E79	LVDS_U0_P	53 56	FUNC_TEST=YES	
E80	LVDS_U0_N	53 56	FUNC_TEST=YES	
E81	LVDS_U1_P	53 56	FUNC_TEST=YES	
E82	LVDS_U1_N	53 56	FUNC_TEST=YES	
E83	LVDS_U2_P	53 56	FUNC_TEST=YES	
E84	LVDS_U2_N	53 56	FUNC_TEST=YES	
E85	CLKLVDS_U_P	53 56	FUNC_TEST=YES	
E86	CLKLVDS_U_N	53 56	FUNC_TEST=YES	
E11	LVDS_L0_P	53 56	FUNC_TEST=YES	
E12	LVDS_L0_N	53 56	FUNC_TEST=YES	Place within 25 mm of LVDS connector.
E13	LVDS_L1_P	53 56	FUNC_TEST=YES	
E14	LVDS_L1_N	53 56	FUNC_TEST=YES	
E16	LVDS_L2_P	53 56	FUNC_TEST=YES	
E15	LVDS_L2_N	53 56	FUNC_TEST=YES	
E17	CLKLVDS_L_P	53 56	FUNC_TEST=YES	
E18	CLKLVDS_L_N	53 56	FUNC_TEST=YES	
E19	LVDS_DDC_CLK	51 56	FUNC_TEST=YES	
E20	LVDS_DDC_DATA	51 56	FUNC_TEST=YES	
E21	=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES	
E63	PP3V3_LCD_CONN	56	FUNC_TEST=YES	

INVERTER

E22	PPBUS_INVERTER	56	FUNC_TEST=YES	
E23	PP5V_INV_SW	56	FUNC_TEST=YES	Place within 25 mm of inverter connector.
E24	BRIGHT_PWM	56	FUNC_TEST=YES	
E24	GND_INVERTER	56	FUNC_TEST=YES	

UATA

E95	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	
E117	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES	
E110	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES	
E32	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES	
E33	UATA_DMARQ	63 64	FUNC_TEST=YES	
E35	UATA_DSTROBE	63 64	FUNC_TEST=YES	
E34	UATA_DMACK_L	63 64	FUNC_TEST=YES	Place within 50 mm of ODD/HDD connector.
E36	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES	
E38	UATA_CS0_L	6 63 64	FUNC_TEST=YES	
E37	UATA_CS1_L	63 64	FUNC_TEST=YES	
E40	UATA_RESET_L	63 64	FUNC_TEST=YES	
E39	UATA_HSTROBE	63 64	FUNC_TEST=YES	
E41	UATA_STOP	63 64	FUNC_TEST=YES	
E42	UATA_INTRQ	63 64	FUNC_TEST=YES	

AUDIO

E72	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	
E60	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
E59	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
E61	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES	
E44	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES	
E45	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES	
E48	I2S0_MCLK	6 74	FUNC_TEST=YES	
E47	I2S0_BITCLK	6 74	FUNC_TEST=YES	
E50	I2S0_SYNC	6 74	FUNC_TEST=YES	
E49	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES	
E51	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES	
E53	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES	Place within 25 mm of audio connector.
E52	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES	
E56	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES	
E55	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES	
E57	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES	
E58	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES	
E107	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
E108	AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
E109	AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES	
E111	AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES	
E113	AUDIO_GPIO_11	22 74	FUNC_TEST=YES	
E114	GND_AUDIO_AGND	74	FUNC_TEST=YES	
E115	GND_AUDIO_PGND	74	FUNC_TEST=YES	

SYSTEM

E76	PP5V_TPAD_F	30	FUNC_TEST=YES	
E77	USB_TPAD_P	11 30	FUNC_TEST=YES	
E78	USB_TPAD_N	11 30	FUNC_TEST=YES	
E88	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES	
E89	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
E43	PP3V3_ALL_HALL_EFFECT_R	30	FUNC_TEST=YES	
E45	SYS_LID_OPEN_F	30	FUNC_TEST=YES	
E30	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES	Place within 25 mm of TPAD connector.
E29	=FTP_SLEEP_LED	74	FUNC_TEST=YES	
E31	SYS_CHARGE_LED_L	24 31	FUNC_TEST=YES	
E87	SYS_ADAPTER_ANALOG_AC_DET	12 31	FUNC_TEST=YES	
E90	KBDLED_ANODE	28 30	FUNC_TEST=YES	
E91	KBDLED_RETURN	28 30	FUNC_TEST=YES	
E105	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES	
E106	=I2C_DS1775_SCL	8 30	FUNC_TEST=YES	

CPU FAN

E100	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	
E98	FAN1_TACH	27 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
E97	FAN1_PWM	27 31	FUNC_TEST=YES	
E119	=FTP_GND	7 10	FUNC_TEST=YES	

GPU FAN

E102	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	
E103	FAN2_TACH	27 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
E104	FAN2_PWM	27 31	FUNC_TEST=YES	
E120	=FTP_GND	7 10	FUNC_TEST=YES	

ALS

E70	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	
E68	ALS_0_OUT	25 31	FUNC_TEST=YES	Place within 25 mm of ALS connector.
E69	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	

SCCA

E72	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm of debug connector.
E71	SCCA_TXD_L	22 24	FUNC_TEST=YES	

BACKUP BATT

E73	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm of battery connector.
E74	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	

RT USB

E64	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of right USB connector.
E65	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
E66	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	

LT USB

E314	=PP5V_PWRON_LEFT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of left USB connector.
E316	USB2_LEFT_PORT_P	11 31	FUNC_TEST=YES	
E315	USB2_LEFT_PORT_N	11 31	FUNC_TEST=YES	

Functional Test Points

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 7 OF 115

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	I2C	I2C		I2C_PMU_SMB_SCL
	I2C	I2C		I2C_PMU_SMB_SDA
	I2C	I2C		I2C_PMU_SCL
	I2C	I2C		I2C_PMU_SDA
I2C_NB	I2C	I2C		I2C_I2_NB_SCL
I2C_NB	I2C	I2C		I2C_I2_NB_SDA
	I2C	I2C		I2C_I2_SB_SCL
	I2C	I2C		I2C_I2_SB_SDA
	I2C	I2C		I2C_GPU_TMDS_SCL
	I2C	I2C		I2C_GPU_TMDS_SDA

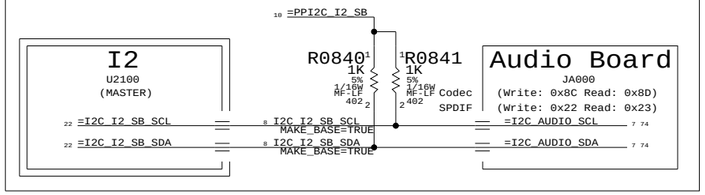
Page Notes

Power aliases required by this page:
(NONE)

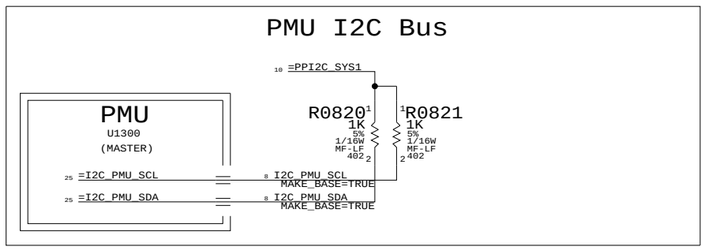
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
  Allows bypassing Governator I2C bus.
  Most devices are connected directly to PMU unstead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
  Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.
  NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.

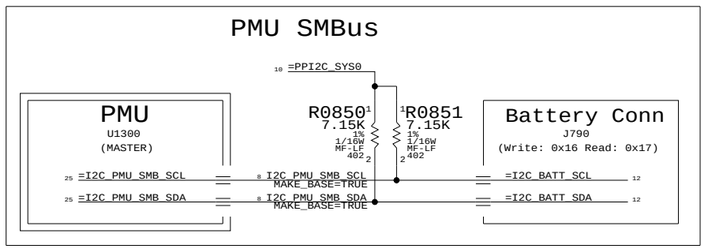
SouthBridge I2C Bus



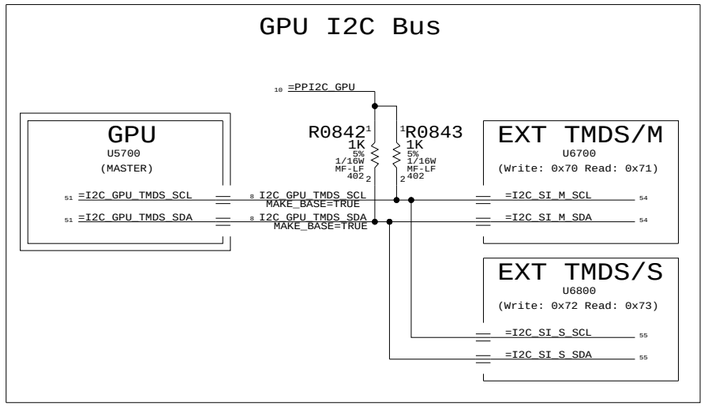
PMU I2C Bus



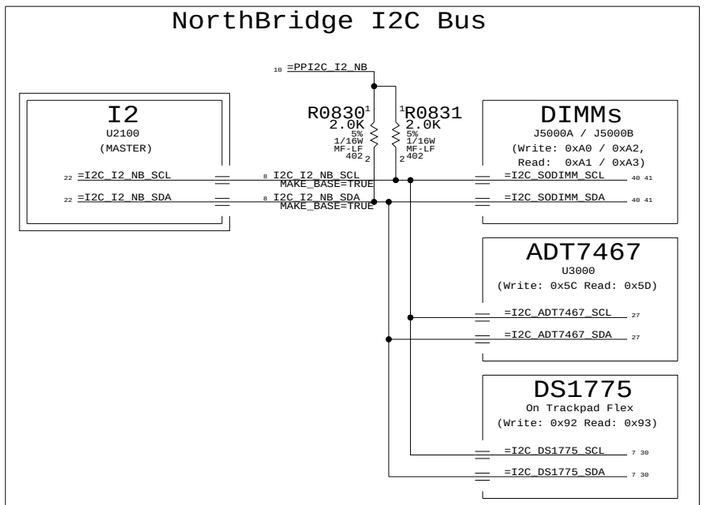
PMU SMBus



GPU I2C Bus



NorthBridge I2C Bus

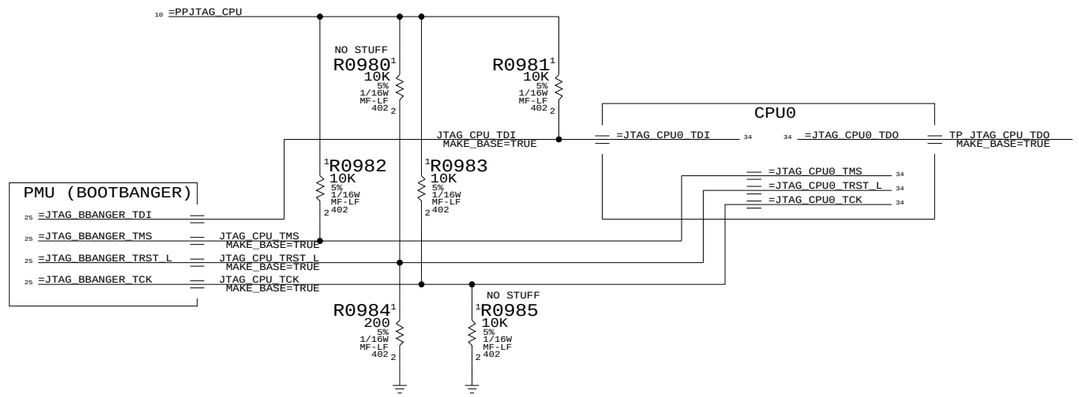


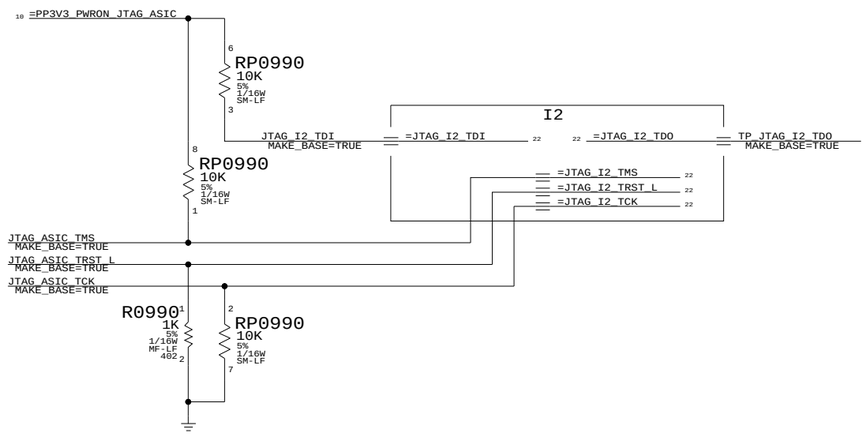
I2C Connections

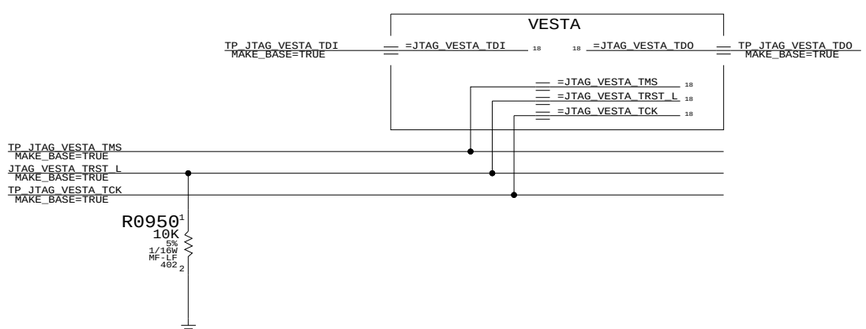
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 8 OF 115	







Nets not requiring TPs due to JTAG

MAXBUS

H6	MAXBUS_DATA<63..0>	21 32 33	NO_TEST=YES
H7	MAXBUS_ADDR<31..0>	32 33	NO_TEST=YES
H8	MAXBUS_CI_L	32 33	NO_TEST=YES
H9	MAXBUS_GBL_L	32 33	NO_TEST=YES
H10	MAXBUS_TBST_L	32 33	NO_TEST=YES
H11	MAXBUS_TSIZ<2..0>	32 33	NO_TEST=YES
H12	MAXBUS_TT<4..0>	32 33	NO_TEST=YES
H13	MAXBUS_WT_L	32 33	NO_TEST=YES
H15	MAXBUS_DTI<2..0>	32 33	NO_TEST=YES

ENET

H66	ENET_MDC	11 65	NO_TEST=YES
H67	ENET_MDIO	11 65	NO_TEST=YES
H68	ENET_TXD<7..0>	11	NO_TEST=YES
H69	ENET_TX_EN	11	NO_TEST=YES
H70	ENET_TX_ER	11	NO_TEST=YES
H62	ENET_RXD<7..0>	11 65	NO_TEST=YES
H61	ENET_RX_DV	11 65	NO_TEST=YES
H63	ENET_RX_ER	11 65	NO_TEST=YES
H64	ENET_COL	11 65	NO_TEST=YES
H65	ENET_CRS	11 65	NO_TEST=YES

FIREWIRE

H66	FW_D_R<7..0>	6 68	NO_TEST=YES
H67	FW_D<7..0>	6 69	NO_TEST=YES
H68	FW_CTL_R<1..0>	68 71	NO_TEST=YES
H69	FW_CTL<1..0>	69 71	NO_TEST=YES
H160	FW_LPS_R	68 71	NO_TEST=YES
H163	FW_LPS	69 71	NO_TEST=YES
H163	FW_LREQ_R	68 71	NO_TEST=YES
H162	FW_LREQ	69 71	NO_TEST=YES

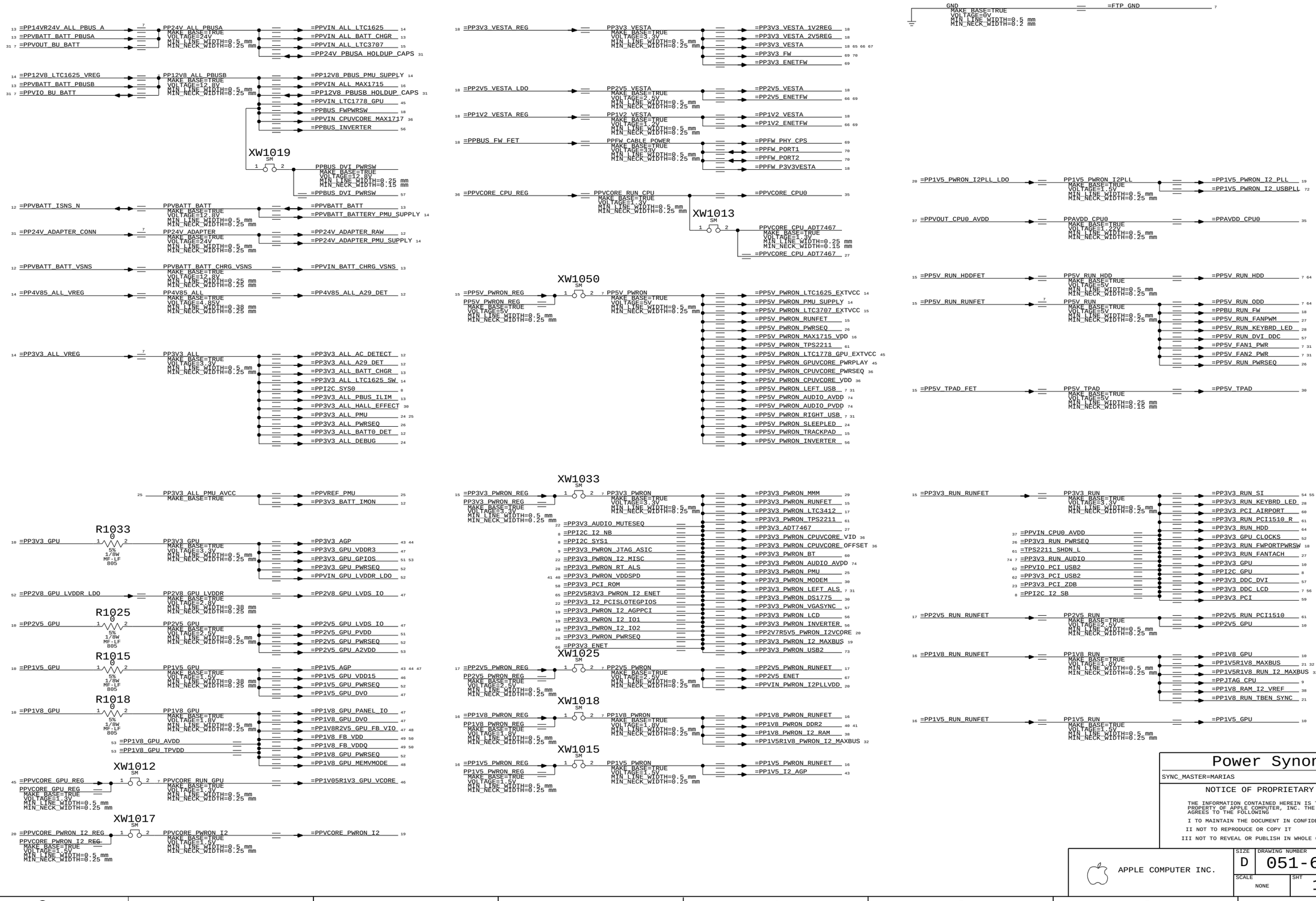
JTAG Connections

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE: NONE SHT 9 OF 115


=PP14VR24V_ALL_PBUS_A
=PPVBATT_BATT_PBUSA
=PPVOUT_BU_BATT
PP24V_ALL_PBUSA
MAKE_BASE=TRUE
VOLTAGE=24V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
=PPVIN_ALL_LTC1625
=PPVIN_ALL_BATT_CHGR
=PPVIN_ALL_LTC3707
=PP24V_PBUSA_HOLDUP_CAPS
=PP12V8_LTC1625_VREG
=PPVBATT_BATT_PBUSB
=PPVIO_BU_BATT
PP12V8_ALL_PBUSB
VOLTAGE=12.8V
=PP12V8_PBUS_PMU_SUPPLY
=PPVIN_ALL_MAX1715
=PP12V8_PBUSB_HOLDUP_CAPS
=PPVIN_LTC1778_GPU
=PPBUS_FWPWRSW
=PPVIN_CPUVCORE_MAX1717
=PPBUS_INVERTER
XW1019
SM
PPBUS_DVI_PWRSW
=PPBUS_DVI_PWRSW
=PPVBATT_ISNS_N
PPVBATT_BATT
=PPVBATT_BATT
=PPVBATT_BATTERY_PMU_SUPPLY
=PP24V_ADAPTER_CONN
PP24V_ADAPTER
=PP24V_ADAPTER_RAW
=PP24V_ADAPTER_PMU_SUPPLY
=PPVBATT_BATT_VSNS
PPVBATT_BATT_CHRG_VSNS
=PPVIN_BATT_CHRG_VSNS
=PP4V85_ALL_VREG
PP4V85_ALL
VOLTAGE=4.85V
MIN_LINE_WIDTH=0.38 mm
=PP4V85_ALL_A29_DET
=PP3V3_ALL_VREG
PP3V3_ALL
VOLTAGE=3.3V
=PP3V3_ALL_AC_DETECT
=PP3V3_ALL_A29_DET
=PP3V3_ALL_BATT_CHGR
=PP3V3_ALL_LTC1625_SW
=PPI2C_SYS0
=PP3V3_ALL_PBUS_ILIM
=PP3V3_ALL_HALL_EFFECT
=PP3V3_ALL_PMU
=PP3V3_ALL_PWRSEQ
=PP3V3_ALL_BATT0_DET
=PP3V3_ALL_DEBUG
PP3V3_ALL_PMU_AVCC
=PPVREF_PMU
=PP3V3_BATT_IMON
R1033
0
5%
1/8W
MF-LF
805
=PP3V3_GPU
PP3V3_GPU
VOLTAGE=3.3V
=PP3V3_AGP
=PP3V3_GPU_VDDR3
=PP3V3_GPU_GPIOS
=PP3V3_GPU_PWRSEQ
=PPVIN_GPU_LVDDR_LDO
=PP2V8_GPU_LVDDR_LDO
PP2V8_GPU_LVDDR
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.38 mm
=PP2V8_GPU_LVDS_IO
R1025
=PP2V5_GPU
PP2V5_GPU
VOLTAGE=2.5V
=PP2V5_GPU_LVDS_IO
=PP2V5_GPU_PVDD
=PP2V5_GPU_PWRSEQ
=PP2V5_GPU_A2VDD
R1015
=PP1V5_GPU
PP1V5_GPU
VOLTAGE=1.5V
=PP1V5_GPU_AGP
=PP1V5_GPU_VDD15
=PP1V5_GPU_PWRSEQ
=PP1V5_GPU_DVO
R1018
=PP1V8_GPU
PP1V8_GPU
VOLTAGE=1.8V
=PP1V8_GPU_PANEL_IO
=PP1V8_GPU_DVO
=PP1V8R2V5_GPU_FB_VIO
=PP1V8_FB_VDD
=PP1V8_GPU_AVDD
=PP1V8_FB_VDDQ
=PP1V8_GPU_TPVDD
=PP1V8_GPU_PWRSEQ
=PP1V8_GPU_MEMVMODE
XW1012
=PPVCORE_GPU_REG
PPVCORE_GPU_REG
VOLTAGE=1.5V
PPVCORE_RUN_GPU
VOLTAGE=1.5V
=PP1V05R1V3_GPU_VCORE
XW1017
=PPVCORE_PWRON_I2_REG
PPVCORE_PWRON_I2_REG
PPVCORE_PWRON_I2
=PPVCORE_PWRON_I2
=PP3V3V3_VESTA_REG
PP3V3_VESTA
VOLTAGE=3.3V
=PP3V3_VESTA_1V2REG
=PP3V3_VESTA_2V5REG
=PP3V3_VESTA
=PP3V3_FW
=PP3V3_ENETFW
=PP2V5_VESTA_LDO
PP2V5_VESTA
VOLTAGE=2.5V
=PP2V5_VESTA
=PP2V5_ENETFW
=PP1V2_VESTA_REG
PP1V2_VESTA
VOLTAGE=1.2V
=PP1V2_VESTA
=PP1V2_ENETFW
=PPBUS_FW_FET
PPFW_CABLE_POWER
VOLTAGE=33V
=PPFW_PHY_CPS
=PPFW_PORT1
=PPFW_PORT2
=PPFW_P3V3VESTA
=PPVCORE_RUN_CPU_REG
PPVCORE_RUN_CPU
=PPVCORE_CPU0
XW1013
PPVCORE_CPU_ADT7467
=PPVCORE_CPU_ADT7467
XW1050
=PP5V_PWRON_REG
PP5V_PWRON_REG
PP5V_PWRON
=PP5V_PWRON_LTC1625_EXTVCC
=PP5V_PWRON_PMU_SUPPLY
=PP5V_PWRON_LTC3707_EXTVCC
=PP5V_PWRON_RUNFET
=PP5V_PWRON_PWRSEQ
=PP5V_PWRON_MAX1715_VDD
=PP5V_PWRON_TPS2211
=PP5V_PWRON_LTC1778_GPU_EXTVCC
=PP5V_PWRON_GPUVCORE_PWRPLAY
=PP5V_PWRON_CPUVCORE_PWRSEQ
=PP5V_PWRON_CPUVCORE_VDD
=PP5V_PWRON_LEFT_USB
=PP5V_PWRON_AUDIO_AVDD
=PP5V_PWRON_AUDIO_PVDD
=PP5V_PWRON_RIGHT_USB
=PP5V_PWRON_SLEEPLED
=PP5V_PWRON_TRACKPAD
=PP5V_PWRON_INVERTER
XW1033
=PP3V3_PWRON_REG
PP3V3_PWRON_REG
PP3V3_PWRON
=PP3V3_PWRON_MMM
=PP3V3_PWRON_RUNFET
=PP3V3_PWRON_LTC3412
=PP3V3_PWRON_TPS2211
=PP3V3_AUDIO_MUTESEQ
=PP3V3_ADT7467
=PPI2C_I2_NB
=PP3V3_PWRON_CPUVCORE_VID
=PPI2C_SYS1
=PP3V3_PWRON_CPUVCORE_OFFSET
=PP3V3_PWRON_JTAG_ASIC
=PP3V3_PWRON_BT
=PP3V3_PWRON_I2_MISC
=PP3V3_PWRON_AUDIO_AVDD
=PP3V3_PWRON_RT_ALS
=PP3V3_PWRON_PMU
=PP3V3_PWRON_VDDSPD
=PP3V3_PWRON_MODEM
=PP3V3_PCI_ROM
=PP2V5R3V3_PWRON_I2_ENET
=PP3V3_PWRON_LEFT_ALS
=PP3V3_I2_PCISLOTEGPIOS
=PP3V3_PWRON_DS1775
=PP3V3_PWRON_I2_AGPPCI
=PP3V3_PWRON_VGASYNC
=PP3V3_PWRON_I2_IO1
=PP3V3_PWRON_LCD
=PP3V3_PWRON_I2_IO2
=PP3V3_PWRON_INVERTER
=PP3V3_PWRON_PWRSEQ
=PP2V7R5V5_PWRON_I2VCORE
=PP3V3_ENET
=PP3V3_PWRON_I2_MAXBUS
=PP3V3_PWRON_USB2
XW1025
=PP2V5_PWRON_REG
PP2V5_PWRON_REG
PP2V5_PWRON
=PP2V5_PWRON_RUNFET
=PP2V5_ENET
=PPVIN_PWRON_I2PLLVDD
XW1018
=PP1V8_PWRON_REG
PP1V8_PWRON_REG
PP1V8_PWRON
=PP1V8_PWRON_RUNFET
=PP1V8_PWRON_DDR2
=PP1V8_PWRON_I2_RAM
=PP1V5R1V8_PWRON_I2_MAXBUS
XW1015
=PP1V5_PWRON_REG
PP1V5_PWRON_REG
PP1V5_PWRON
=PP1V5_PWRON_RUNFET
=PP1V5_I2_AGP
GND
=FTP_GND
=PP1V5_PWRON_I2PLL_LDO
PP1V5_PWRON_I2PLL
=PP1V5_PWRON_I2_PLL
=PP1V5_PWRON_I2_USBPLL
=PPVOUT_CPU0_AVDD
PPAVDD_CPU0
=PPAVDD_CPU0
=PP5V_RUN_HDDFET
PP5V_RUN_HDD
=PP5V_RUN_HDD
=PP5V_RUN_RUNFET
PP5V_RUN
=PP5V_RUN_QDD
=PPBUS_RUN_FW
=PP5V_RUN_FANPWM
=PP5V_RUN_KEYBRD_LED
=PP5V_RUN_DVI_DDC
=PP5V_FAN1_PWR
=PP5V_FAN2_PWR
=PP5V_RUN_PWRSEQ
=PP5V_TPAD_FET
PP5V_TPAD
=PP5V_TPAD
=PP3V3_RUN_RUNFET
PP3V3_RUN
=PP3V3_RUN_SI
=PP3V3_RUN_KEYBRD_LED
=PP3V3_PCI_AIRPORT
=PP3V3_RUN_PCI1510_R
=PP3V3_RUN_HDD
=PPVIN_CPU0_AVDD
=PP3V3_GPU_CLOCKS
=PP3V3_RUN_PWRSEQ
=PP3V3_RUN_FWPORTPWRSW
=TPS2211_SHDN_L
=PP3V3_RUN_FANTACH
=PP3V3_RUN_AUDIO
=PP3V3_GPU
=PPVIO_PCI_USB2
=PPI2C_GPU
=PP3V3_PCI_USB2
=PP3V3_DDC_DVI
=PP3V3_PCI_ZDB
=PP3V3_DDC_LCD
=PPI2C_I2_SB
=PP3V3_PCI
=PP2V5_RUN_RUNFET
PP2V5_RUN
=PP2V5_RUN_PCI1510
=PP2V5_GPU
=PP1V8_RUN_RUNFET
PP1V8_RUN
=PP1V8_GPU
=PP1V5R1V8_MAXBUS
=PP1V5R1V8_RUN_I2_MAXBUS
=PPJTAG_CPU
=PP1V8_RAM_I2_VREF
=PP1V8_RUN_TBEN_SYNC
=PP1V5_RUN_RUNFET
PP1V5_RUN
=PP1V5_GPU
Power Synonyms
SYNC_MASTER=MARIAS
SYNC_DATE=08/24/2005
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APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-6839
REV:
E
SCALE
NONE
SHT
10
OF
115

I2S0 Series Rs

RP1150
33
5%
1/16W
SM-LF

=RP1150P1 — 1 — 8 — =RP1150P8
=RP1150P2 — 2 — 7 — =RP1150P7
=RP1150P3 — 3 — 6 — =RP1150P6
=RP1150P4 — 4 — 5 — =RP1150P5

One resistor for each of:
- I2S0_SB_TO_DEV_DTO(_R)
- I2S0_MCLK(_R)
- I2S0_BITCLK(_R)
- I2S0_SYNC(_R)

I2S1 Series Rs

RP1151
33
5%
1/16W
SM-LF

=RP1151P1 — 1 — 8 — =RP1151P8
=RP1151P2 — 2 — 7 — =RP1151P7
=RP1151P3 — 3 — 6 — =RP1151P6
=RP1151P4 — 4 — 5 — =RP1151P5

One resistor for each of:
- I2S1_SB_TO_DEV_DTO(_R)
- I2S1_MCLK(_R)
- I2S1_BITCLK(_R)
- I2S1_SYNC(_R)

GPU

R1140
22
5%
1/16W
MF-LF
402

AGP_CLK66M_GPU_R → AGP_CLK66M_GPU

PCI_RESET_L → =AGP_GPU_RESET_L
MAKE_BASE=TRUE

AGP_VREF
MAKE_BASE=TRUE → =I2_AGP_VREF
VOLTAGE=0.75V → =AGP_VREF
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.15 mm → =GPU_AGP_VREF

TP_EXTTMDS_RESET_L → SI_TMDS_RESET_L (MAKE_BASE=TRUE) → =SI_TMDS_RESET_L

CPU Clocks

R1110
10
5%
1/16W
MF-LF
402

MAXBUS_CLK_CPU0_R → MAXBUS_CLK_CPU0 (MAKE_BASE=TRUE) → =MAXBUS_CPU0_CLK

MAXBUS_TBEN_SYNC

R1111
10
5%
1/16W
MF-LF
402

TP_MAXBUS_CLK_CPU1_R → MAXBUS_CLK_CPU1_R (MAKE_BASE=TRUE) → MAXBUS_CLK_TBEN_SYNC (MAKE_BASE=TRUE) → =SYSCLK_TBEN_SYNC

USB Controller Mux

R1160 0 5% 1/16W MF-LF 402 — USB2_NEC
USB2_LEFT_PORT_P → USB2_NEC_LEFT_PORT_P

R1161 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB2_LT_PORT
USB2_I2_LEFT_PORT_P

R1162 0 5% 1/16W MF-LF 402 — USB2_NEC
USB2_LEFT_PORT_N → USB2_NEC_LEFT_PORT_N

R1163 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB2_LT_PORT
USB2_I2_LEFT_PORT_N

R1164 0 5% 1/16W MF-LF 402 — USB2_NEC
USB2_RIGHT_PORT_P → USB2_NEC_RIGHT_PORT_P

R1165 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB2_RT_PORT
USB2_I2_RIGHT_PORT_P

R1166 0 5% 1/16W MF-LF 402 — USB2_NEC
USB2_RIGHT_PORT_N → USB2_NEC_RIGHT_PORT_N

R1167 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB2_RT_PORT
USB2_I2_RIGHT_PORT_N

R1170 0 5% 1/16W MF-LF 402 — USB1P1_NEC
USB_BT_P → USB_NEC_BT_P

R1171 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB_BT
USB_I2_BT_P

R1172 0 5% 1/16W MF-LF 402 — USB1P1_NEC
USB_BT_N → USB_NEC_BT_N

R1173 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB_BT
USB_I2_BT_N

R1174 0 5% 1/16W MF-LF 402 — USB1P1_NEC
USB_TPAD_P → USB_NEC_TPAD_P

R1175 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB_TPAD
USB_I2_TPAD_P

R1176 0 5% 1/16W MF-LF 402 — USB1P1_NEC
USB_TPAD_N → USB_NEC_TPAD_N

R1177 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2
NET_PHYSICAL_TYPE=USB2
DIFFERENTIAL_PAIR=USB_TPAD
USB_I2_TPAD_N

PCI

R1120 22 5% 1/16W MF-LF 402
TP_PCI_CLK33M_SLOTA_R → PCI_CLK33M_ZDB_R (MAKE_BASE=TRUE) → PCI_CLK33M_ZDB (MAKE_BASE=TRUE) → =PCI_CLK33M_ZDB_IN

MAXBUS_TBEN_SYNC

R1130 22 5% 1/16W MF-LF 402
TP_PCI_CLK33M_SLOTD_R → PCI_CLK33M_TBEN_SYNC_R (MAKE_BASE=TRUE) → PCI_CLK33M_TBEN_SYNC (MAKE_BASE=TRUE) → =CLK33M_TBEN_SYNC

R1135 22 5% 1/16W MF-LF 402
=PCI_CLK33M_ZDBOUT_R<0> → PCI_CLK33M_AIRPORT_R (MAKE_BASE=TRUE) → PCI_CLK33M_AIRPORT (MAKE_BASE=TRUE) → =PCI_CLK33M_AIRPORT

PCI_SLOTA_REQ_L → PCI_AIRPORT_REQ_L (MAKE_BASE=TRUE) → =PCI_AIRPORT_REQ_L
PCI_SLOTA_GNT_L → PCI_AIRPORT_GNT_L (MAKE_BASE=TRUE) → =PCI_AIRPORT_GNT_L
PCI_SLOTA_INT_L → PCI_AIRPORT_INT_L (MAKE_BASE=TRUE) → =PCI_AIRPORT_INT_L
PCI_AD<17> (MAKE_BASE=TRUE) → =PCI_AIRPORT_IDSEL
PCI_RESET_L (MAKE_BASE=TRUE) → =PCI_AIRPORT_RESET_L

R1136 22 5% 1/16W MF-LF 402
=PCI_CLK33M_ZDBOUT_R<1> → PCI_CLK33M_CBUS_R (MAKE_BASE=TRUE) → PCI_CLK33M_CBUS (MAKE_BASE=TRUE) → =PCI_CLK33M_CBUS

PCI_SLOTD_REQ_L → PCI_CBUS_REQ_L (MAKE_BASE=TRUE) → =PCI_CBUS_REQ_L
PCI_SLOTD_GNT_L → PCI_CBUS_GNT_L (MAKE_BASE=TRUE) → =PCI_CBUS_GNT_L
PCI_SLOTD_INT_L → PCI_CBUS_INT_L (MAKE_BASE=TRUE) → =PCI_CBUS_INT_L
PCI_AD<20> (MAKE_BASE=TRUE) → =PCI_CBUS_IDSEL
PCI_RESET_L (MAKE_BASE=TRUE) → =PCI_CBUS_RESET_L

R1137 22 5% 1/16W MF-LF 402
=PCI_CLK33M_ZDBOUT_R<2> → PCI_CLK33M_USB2_R (MAKE_BASE=TRUE) → PCI_CLK33M_USB2 (MAKE_BASE=TRUE) → =PCI_CLK33M_USB2

PCI_SLOTE_REQ_L → PCI_USB2_REQ_L (MAKE_BASE=TRUE) → =PCI_USB2_REQ_L
PCI_SLOTE_GNT_L → PCI_USB2_GNT_L (MAKE_BASE=TRUE) → =PCI_USB2_GNT_L
PCI_SLOTE_INT_L → PCI_USB2_INT_L (MAKE_BASE=TRUE) → =PCI_USB2_INT_L
PCI_AD<21> (MAKE_BASE=TRUE) → =PCI_USB2_IDSEL
PCI_RESET_L (MAKE_BASE=TRUE) → =PCI_USB2_RESET_L

=PCI_CLK33M_ZDBOUT_R<3> → TP_PCI_CLK33M_ZDBOUT3 (MAKE_BASE=TRUE)

USB Port Assignments

USB2_I2_LEFT_PORT_P (MAKE_BASE=TRUE) — USB2_I2_P<0>
USB2_I2_LEFT_PORT_N (MAKE_BASE=TRUE) — USB2_I2_N<0>
USB2_I2_RIGHT_PORT_P (MAKE_BASE=TRUE) — USB2_I2_P<2>
USB2_I2_RIGHT_PORT_N (MAKE_BASE=TRUE) — USB2_I2_N<2>
USB_I2_BT_P (MAKE_BASE=TRUE) — USB2_I2_P<4>
USB_I2_BT_N (MAKE_BASE=TRUE) — USB2_I2_N<4>
USB_I2_TPAD_P (MAKE_BASE=TRUE) — USB2_I2_P<5>
USB_I2_TPAD_N (MAKE_BASE=TRUE) — USB2_I2_N<5>

USB2_NEC_LEFT_PORT_P (MAKE_BASE=TRUE) — USB2_NEC_P<0>
USB2_NEC_LEFT_PORT_N (MAKE_BASE=TRUE) — USB2_NEC_N<0>
USB2_NEC_RIGHT_PORT_P (MAKE_BASE=TRUE) — USB2_NEC_P<1>
USB2_NEC_RIGHT_PORT_N (MAKE_BASE=TRUE) — USB2_NEC_N<1>
USB_NEC_BT_P (MAKE_BASE=TRUE) — USB2_NEC_P<2>
USB_NEC_BT_N (MAKE_BASE=TRUE) — USB2_NEC_N<2>
USB_NEC_TPAD_P (MAKE_BASE=TRUE) — USB2_NEC_P<3>
USB_NEC_TPAD_N (MAKE_BASE=TRUE) — USB2_NEC_N<3>

PMU Connections

SYS_OVERTEMP_L (MAKE_BASE=TRUE) — =ADT7467_THERM_L
PMU_CHARGE_V (MAKE_BASE=TRUE) — TP_PMU_P7_5
PMU_CPU_HRESET_L (MAKE_BASE=TRUE) — =CPU_HRESET_L
SYS_PMU_ANALOG_AC_DET (MAKE_BASE=TRUE) — TP_PMU_AN_P10_6
GOV_RESET_L — TP_GOV_RESET_L (MAKE_BASE=TRUE)
PMU_CPU_CLK_EN (MAKE_BASE=TRUE) — =I2_STOPCPU_L
PMU_SYS_CLK_EN (MAKE_BASE=TRUE) — =I2_STOPXTAL_L

TP_PMU_P3_0 (MAKE_BASE=TRUE)
TP_PMU_P3_1 (MAKE_BASE=TRUE)
TP_PMU_P3_2 (MAKE_BASE=TRUE)
TP_PMU_P3_3 (MAKE_BASE=TRUE)

SYS_PWRSEQ_TPAD_L (MAKE_BASE=TRUE) — TP_PMU_AN_P0_0
SYS_PWRSEQ_1 (MAKE_BASE=TRUE) — TP_PMU_AN_P0_1
SYS_PWRSEQ_2 (MAKE_BASE=TRUE) — TP_PMU_AN_P0_2
SYS_PWRSEQ_3_L (MAKE_BASE=TRUE) — TP_PMU_AN_P0_3
SYS_PWRSEQ_4 (MAKE_BASE=TRUE) — TP_PMU_AN_P0_4
SYS_PWRSEQ_5 (MAKE_BASE=TRUE) — TP_PMU_AN_P0_5
SYS_PWRSEQ_6_L (MAKE_BASE=TRUE) — TP_PMU_P7_4
SYS_PWRSEQ_FINAL (MAKE_BASE=TRUE) — TP_PMU_AN_P10_5

Vesta Ethernet

ENET_TX_EN_R → ENET_TX_EN (MAKE_BASE=TRUE) → =ENET_TX_EN
ENET_TX_ER_R → ENET_TX_ER (MAKE_BASE=TRUE) → =ENET_TX_ER
ENET_TXD_R<7..0> → ENET_TXD<7..0> (MAKE_BASE=TRUE) → =ENET_TXD<7..0>
ENET_RESET_L

R1185 100K 5% 1/16W MF-LF 402

ENET_RXD<7..0> (MAKE_BASE=TRUE) → =ENET_RXD_R<7..0>
ENET_RX_DV (MAKE_BASE=TRUE) → =ENET_RX_DV_R
ENET_RX_ER (MAKE_BASE=TRUE) → =ENET_RX_ER_R
ENET_COL (MAKE_BASE=TRUE) → =ENET_COL_R
ENET_CRS (MAKE_BASE=TRUE) → =ENET_CRS_R
ENET_CLK125M_GBE_REF (MAKE_BASE=TRUE) → =VESTA_CLK125M_GBE_REF
ENET_CLK125M_RX (MAKE_BASE=TRUE) → =VESTA_CLK125M_RX
ENET_CLK25M_TX (MAKE_BASE=TRUE) → =VESTA_CLK25M_TX
ENET_MDC (MAKE_BASE=TRUE) → =VESTA_MDC
ENET_MDIO (MAKE_BASE=TRUE) → =VESTA_MDIO
TP_ENET_ENERGYDET (MAKE_BASE=TRUE) → =VESTA_ENERGYDET

MISC

PCI_RESET_L (MAKE_BASE=TRUE) → =ROM_PWD_L
TP_MAXBUS_CPU1_QACK_L → NC_MAXBUS_CPU1_QACK_L (MAKE_BASE=TRUE, NO_TEST=YES)

I2_GPIO_EXT_02 → CPU0_VID_AB_SEL (MAKE_BASE=TRUE) → =CPU0_VID_AB_SEL
=SPI_I2_REQ → CPU0_MAX1717_AB_SEL (MAKE_BASE=TRUE) → =CPU0_MAX1717_AB_SEL
=SLEEP_LED_IOUT → SLEEP_LED_IOUT (MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm) → =SLEEP_LED_CONN

Signal Synonyms

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

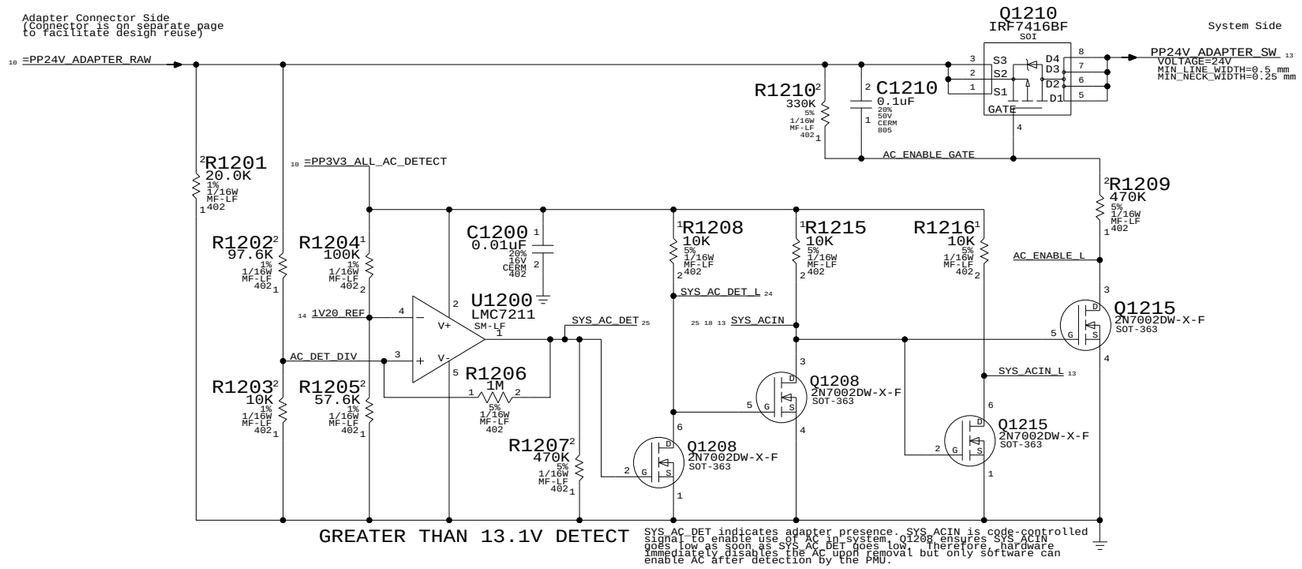
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 11 OF 115

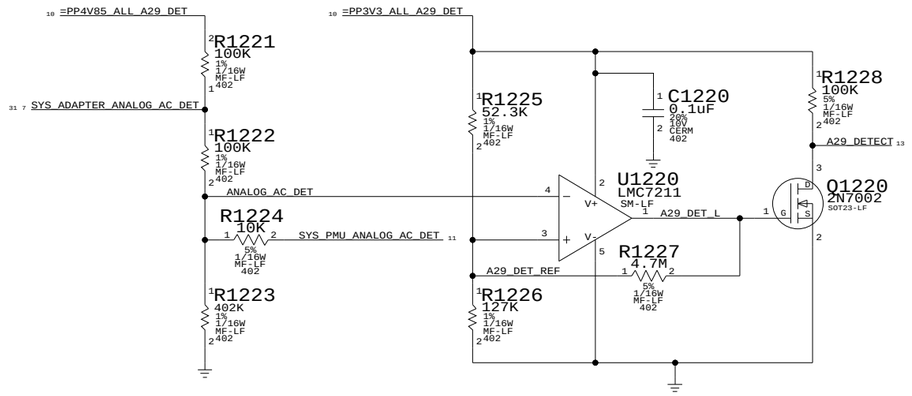
NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
P31V	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINP 12
P30V	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINN 12

ADAPTER INPUT/INRUSH LIMITER



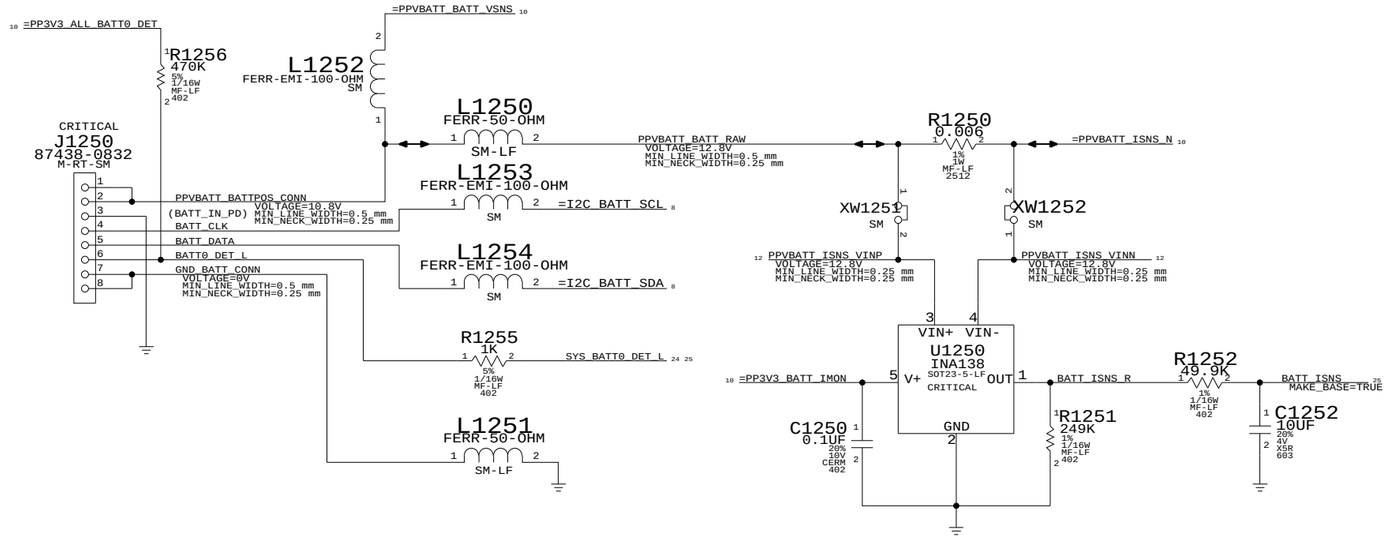
SYS_AC_DET indicates adapter presence. SYS_ACIN is code-controlled signal to enable use of AC as system. Q1208 ensures SYS_ACIN goes low as soon as SYS_AC_DET does low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 12 OF 115	

BACKFEED PROTECTION

PP24V_ADAPTER_SW

Q1360 IRF7416BF SOI — D1 D2 D3 D4 S1 S2 S3 GATE

PP24V_ADAPTER_ILIM_P — VOLTAGE=24V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

R1360 47K 5% 1/16W MF-LF 402

BKFD_PROT_GATE

C1361 0.01UF 20% 50V CERM 603

R1361 68K 5% 1/16W MF-LF 402

BKFD_PROT_EN_L

Q1392 2N7002DW-X-F SOT-363 — SYS_ACIN

PLACE U1370 NEXT TO R1300

C1370 0.01uF 20% 50V CERM 603

U1370 MAX4172 TSSOP-LF — CRITICAL — V+ RS+ RS- NC1 NC2 PG GND OUT NC NC

=PP14VR24V_ALL_PBUS_A

Place close to RS-

C1371 0.1UF 10% 50V X7R 603-1

R1370 2.21K 0.1% 1/16W MF-LF 603 — CRITICAL

MAX4172_OUT

+PBUS CURRENT LIMIT

R1386 1K 1% 1/16W MF-LF 402 — IAC_RC_COMP

C1386 0.1uF 20% 10V CERM 402

=PP3V3_ALL_PBUS_ILIM

C1380 0.1uF 20% 10V CERM 402 — CRITICAL

R1380 42.2K 0.1% 1/16W MF-LF 603 — CRITICAL — IAC_FB

PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

R1385 10K 1% 1/16W MF-LF 402

U1380 LTC1625IS8 SO8

DP1390 BAS16TW-X-F SOT23-5 SOT-363

LTC1625_ITH

R1387 150 1% 1/16W MF-LF 402 — 1625_COMP

ADAPTER_I_REG

CURRENT_THRESHOLD

R1381 42.2K 0.1% 1/16W MF-LF 603 — CRITICAL

R1382 82.5K 0.1% 1/16W MF-LF 603 — CRITICAL

R1383 51.1K 0.1% 1/16W FF-LF 603 — CRITICAL

A29_CURRENT_ADJ

=PP3V3_ALL_PBUS_ILIM

R1384 100K 5% 1/16W MF-LF 402

OVER_18V_ADJ

Q1330 2N7002DW-X-F SOT-363

A29_DETECT

AC_GTR_18V

Q1384 2N7002DW-X-F SOT-363

C1384 1uF 20% 16V CERM 603

1772_ACOK_L

Q1384 2N7002DW-X-F SOT-363

BATTERY SWITCH-OVER CIRCUIT

=PPVBATT_BATT

F1390 5AMP-125V SM-LF

F1395 5AMP-125V SM-LF

=PPVBATT_BATT_PBUSA

=PPVBATT_BATT_PBUSB

PPVBATT_BATT_PBUSA_FUSE — VOLTAGE=14V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

PPVBATT_BATT_PBUSB_FUSE — VOLTAGE=14V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

Q1390 IRF7416BF SOI — CRITICAL — D1 D2 D3 D4 S1 S2 S3 GATE

Q1395 SUD45P03 TO-252-LF — CRITICAL

R1390 47K 5% 1/16W MF-LF 402

R1395 47K 5% 1/16W MF-LF 402

BATT_24V_GATE

BATT_14V_GATE

R1391 10K 5% 1/16W MF-LF 402

R1396 10K 5% 1/16W MF-LF 402

DP1390 BAS16TW-X-F SOT-363

SYS_ACIN_L

DP1390 BAS16TW-X-F SOT-363

R1392 158K 1% 1/16W MF-LF 402

BATT_24PBUS_EN

BATT_14PBUS_EN

Q1392 2N7002DW-X-F SOT-363

SYS_ACIN_L_RC

C1392 10uF 20% 25V X5R 603

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0343	1	RES,20K,1%,1/16W,MF-LF,402	R1345	Q16C_PARTS
114S0382	1	RES,48.7K,1%,1/16W,MF-LF,402	R1345	Q41C_PARTS

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

=PP3V3_ALL_BATT_CHGR

R1341 27.4K 1% 1/16W MF-LF 402

R1344 10K 1% 1/16W MF-LF 402

R1346 10K 1% 1/16W MF-LF 402

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R1342 4.12K 1% 1/16W MF-LF 402

R1345 20.0K 1% 1/16W MF-LF 402 — OMIT

BATTV_HIGH

R1340 100K 5% 1/16W MF-LF 402

Q1340 2N7002DW-X-F SOT-363

R1343 5.23K 1% 1/16W MF-LF 402

BATTV_LOW

Q1340 2N7002DW-X-F SOT-363

PMU_CHARGE_V

=PP3V3_ALL_BATT_CHGR

R1347 100K 5% 1/16W MF-LF 402

Q1347 2N7002DW-X-F SOT-363

CHARGE_DISABLE

Q1347 2N7002DW-X-F SOT-363

PMU_BATT0_CHARGE

V_{BATT} = CELLS X (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

PP24V_ADAPTER_SW

R1321 100K 1% 1/16W MF-LF 402

R1322 12.7K 1% 1/16W MF-LF 402

C1300 1UF 20% 50V CERM 1210

D1303 MMBD914XXG SOT23

R1348 1K 1% 1/16W MF-LF 402

R1323 1K 1% 1/16W MF-LF 402

BATT_LOW_L

Q1348 2N7002DW-X-F SOT-363

Q1348 2N7002DW-X-F SOT-363

R1325 1K 1% 1/16W MF-LF 402

C1325 0.01uF 20% 16V CERM 402

C1326 0.01uF 20% 16V CERM 402

1772_CCV_RC

R1324 1K 1% 1/16W MF-LF 402

C1324 0.1uF 20% 10V CERM 402

C1327 1uF 20% 10V CERM 603

1772_REF

R1328 10K 1% 1/16W MF-LF 402

R1329 4.12K 1% 1/16W MF-LF 402

1772_CLS

VOLTAGE=0V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

1772_GND

R1300 0.025 1% 1W MF 2512-1 — CRITICAL

R1301 4.7 5% 1/16W MF-LF 402

R1302 4.7 5% 1/16W MF-LF 402

1772_CSSP

1772_CSSN

C1301 0.47UF 10% 50V CERM 1206

C1302 0.47UF 10% 50V CERM 1206

U1300 MAX1772 QSOP-LF — CRITICAL — CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT GND

1772_DCIN

1772_ACIN

1772_ACOK_L

(+3V_PMU)

1772_VCTL

1772_ICTL

1772_ICHG

1772_IINP

1772_CCV

1772_CCI

1772_CCS

1772_CELLS

1772_DLOV

1772_BST

1772_DHI

1772_LX

1772_DLO

(GND)

1772_CSIP

1772_CSIN

R1319 33 5% 1/4W MF-LF 1206

D1319 MMBD914XXG SOT23

1772_LDO

1772_BST_ESR

R1317 100K 5% 1/16W MF-LF 402

C1319 0.1uF 20% 25V CERM 603

R1320 4.7 5% 1/10W MF-LF 603

C1320 0.1uF 20% 50V CERM 805

C1321 0.0022UF 10% 50V CERM 402 — NO STUFF

C1322 0.1uF 20% 25V CERM 603

C1323 0.1uF 20% 25V CERM 603

C1317 1uF 20% 25V CERM 603

R1318 100K 5% 1/16W MF-LF 402

XW1300 SM

=PPVIN_ALL_BATT_CHGR

CRITICAL Q1300 RLA130N03 SO8

C1312 2.2UF 10% 50V X7R 1206

C1313 2.2UF 10% 50V X7R 1206

C1314 2.2UF 10% 50V X7R 1206

C1315 2.2UF 10% 50V X7R 1206

C1316 2.2UF 10% 50V X7R 1206

CRITICAL L1300 10uH SM1-LF

PPVOUT_BATT_CHRG_R — VOLTAGE=14V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

R1303 0.05 1% 1W MF 2512

PPVBATT_BATT_PBUSA_FUSE — MAKE_BASE=TRUE

=PPVOUT_BATT_CHRG

CRITICAL Q1301 IRF7811W SO-8-LF

D1300 SMB MBRS140XXG

C1305 4.7uF 20% 25V CERM 1206

C1307 4.7uF 20% 25V CERM 1206

C1309 4.7uF 20% 25V CERM 1206

C1311 33uF 20% 25V ELEC SM1-LF — CRITICAL

R1304 1 5% 1/16W MF-LF 603

R1305 1 5% 1/16W MF-LF 603

C1306 4.7uF 20% 25V CERM 1206

C1308 4.7uF 20% 25V CERM 1206

C1310 4.7uF 20% 25V CERM 1206

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0084	126S0079		C1311	Primary is 260C/Alt is 250C part

R1351 499K 1% 1/16W MF-LF 402

R1352 100K 1% 1/16W MF-LF 402

C1352 0.047uF 10% 10V CERM 402

R1353 100K 1% 1/16W MF-LF 402

R1354 100K 1% 1/16W MF-LF 402

U1350 LMC7211 SM-LF

BATT_LOW

BATT_DIV

1V65_REF

C1350 0.1uF 20% 10V CERM 402

R1330 6.34K 1% 1/16W MF-LF 402

A29_CLS_ADJ

A29_DETECT

Q1330 2N7002DW-X-F SOT-363

=PPVIN_BATT_CHRG_VSNS

Battery Charger

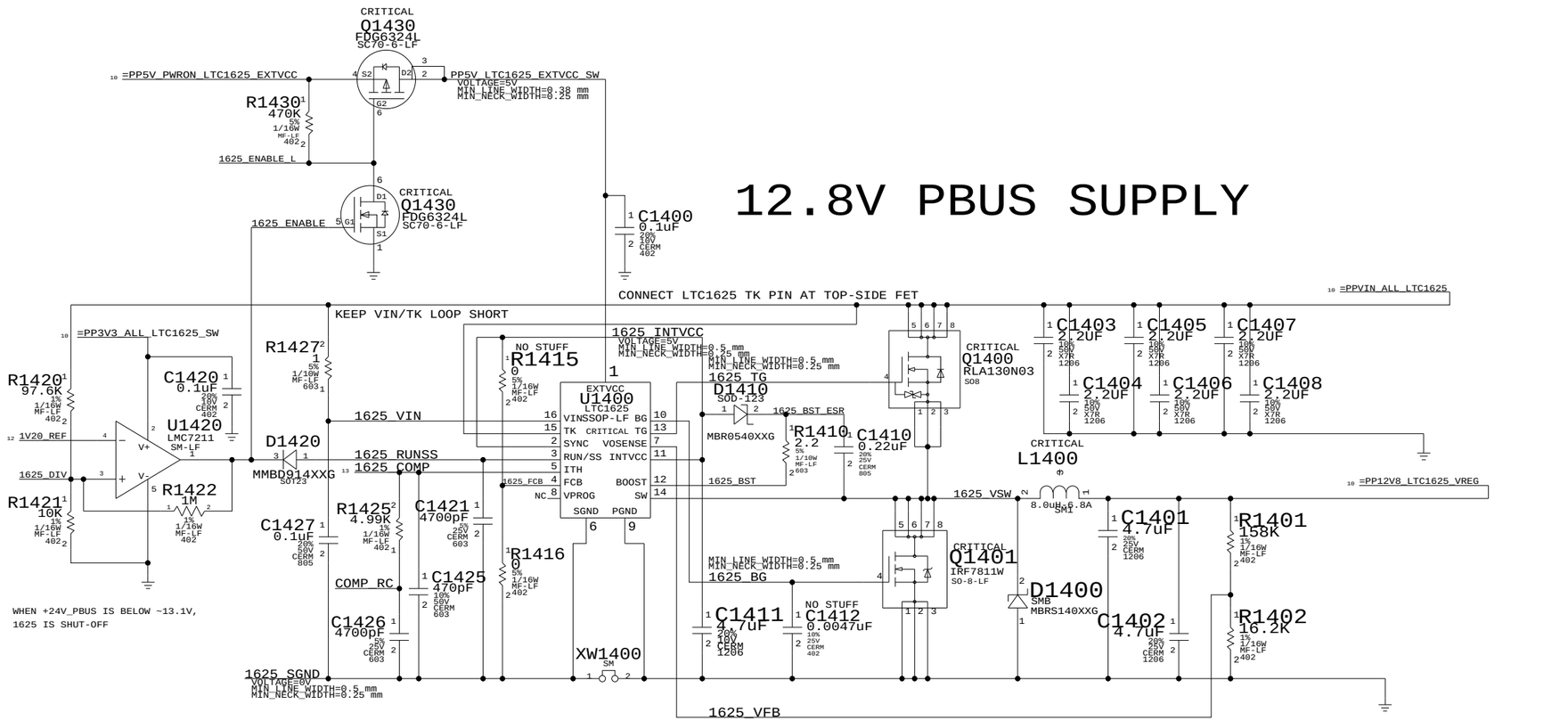
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

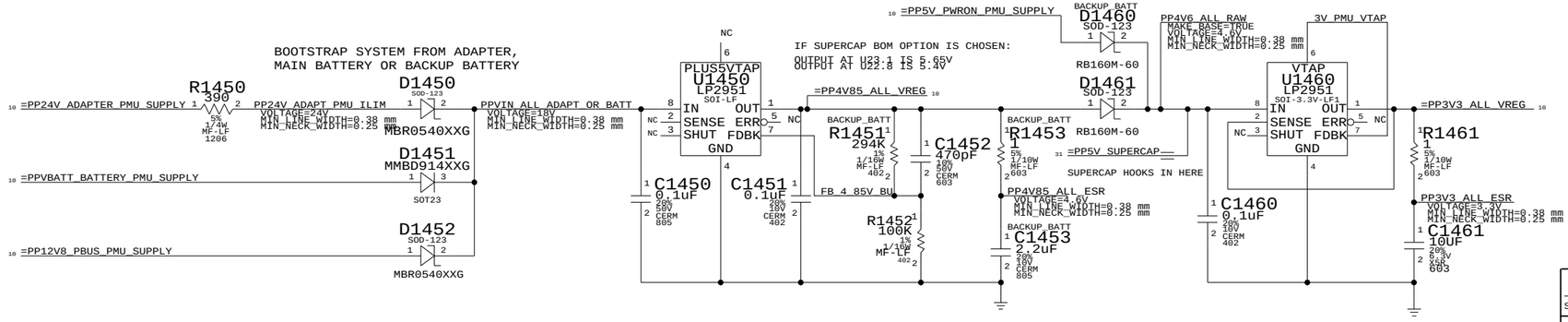
SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 13 OF 115

12.8V PBUS SUPPLY



PMU SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0465	1	RES,MF-LF,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

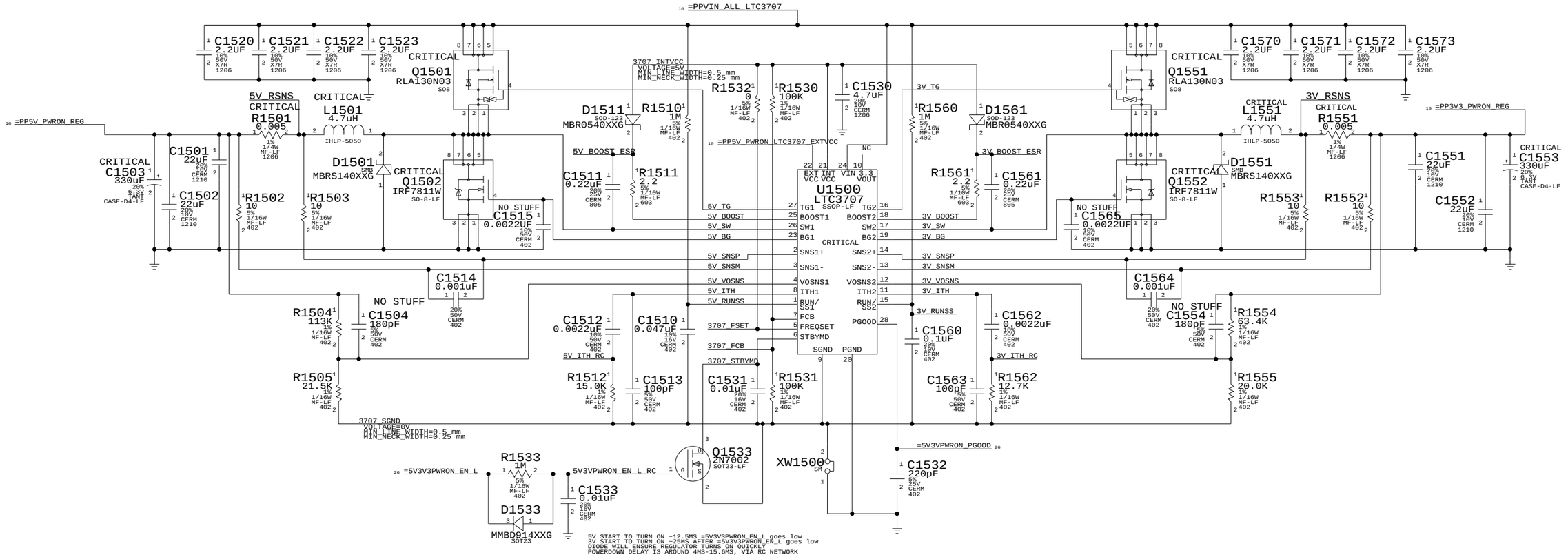
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

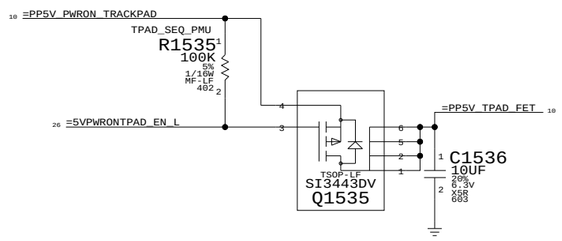
APPLE COMPUTER INC.

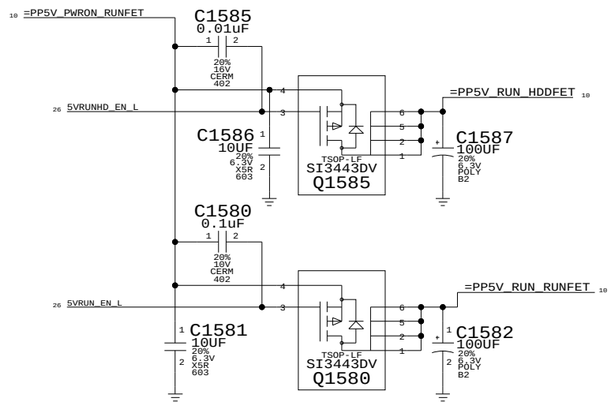
SIZE	DRAWING NUMBER	REV.
D	051-6839	E

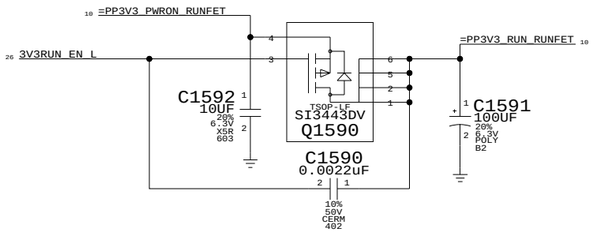
SCALE	SHT
NONE	14 OF 115

3.3V/5V SWITCHER









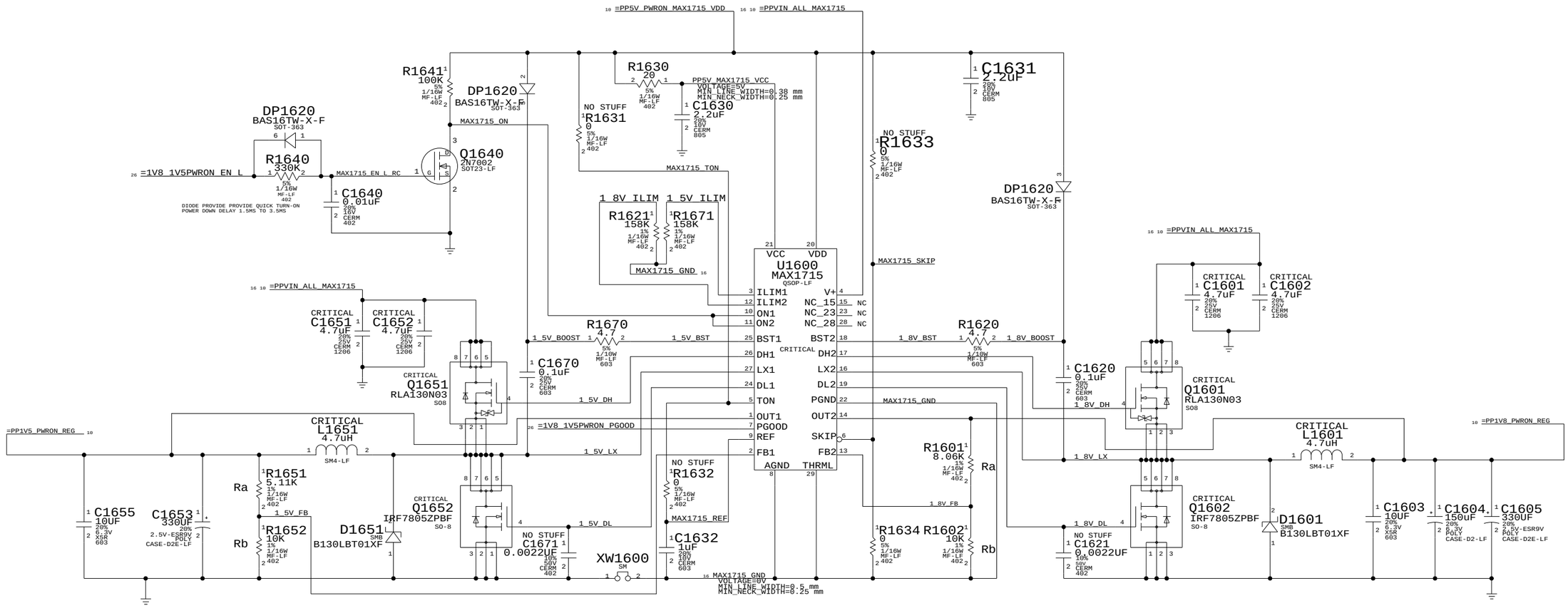
5V/3.3V Supplies

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

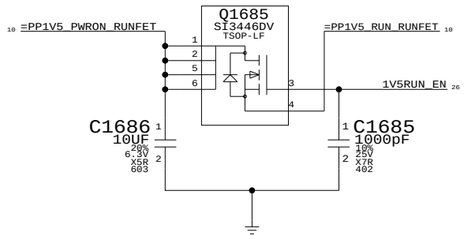
APPLE COMPUTER INC.

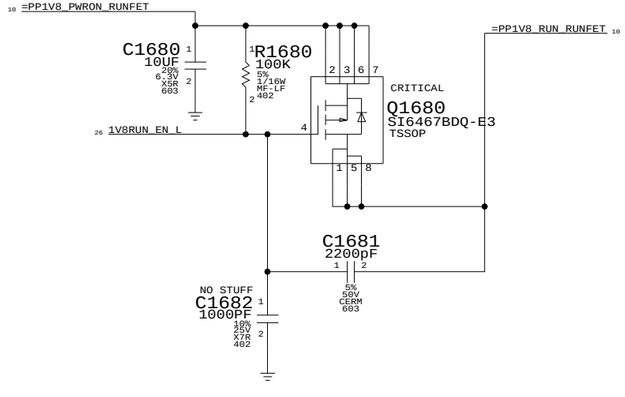
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 15 OF 115	

1.5V/1.8V SWITCHER



Vout = 1.0V * (1 + Ra/Rb)





1.8V/1.5V Supplies

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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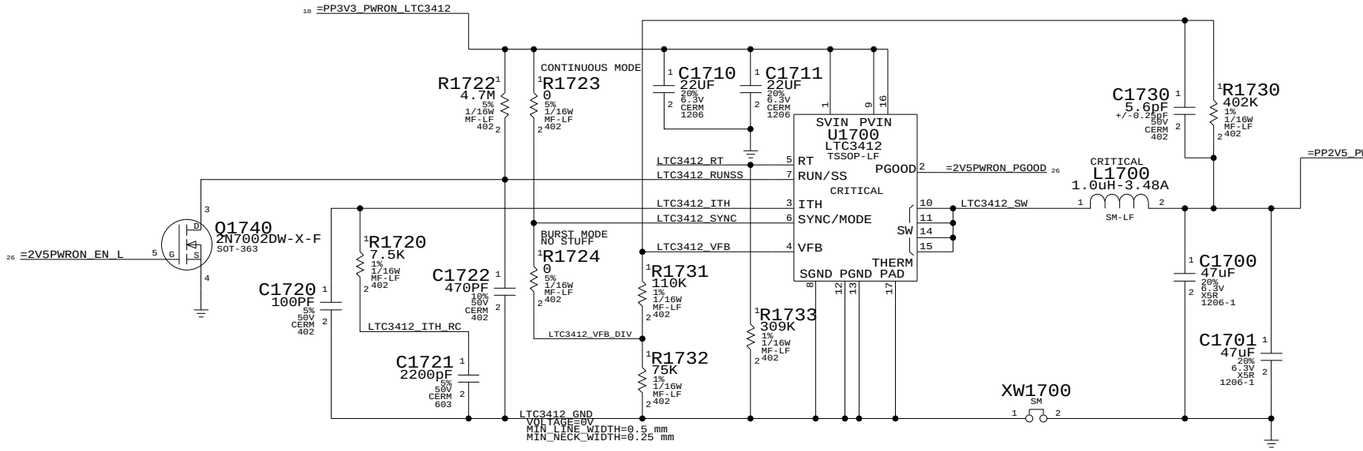
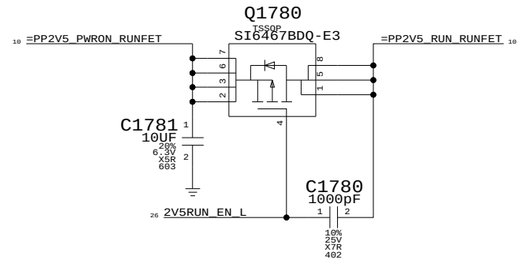
2.5V SWITCHER





2.5V Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
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Page Notes

Power aliases required by this page:
- =PPBUS_FW (system supply for bus power)
- =PPBU_RUN_FW (backup PHY power)
- =PP3V3_RUN_FWPORTPWRSW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

3.3V Regulator

=PPFW_P3V3VESTA → D1975 SC-59 → PPVIN_VESTA3V3 (VOLTAGE=33V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)
=PPBU_RUN_FW → SMD20E40C-X-F → PPVIN_VESTA3V3

CRITICAL U1970 LM2594 SM-LF: VIN, FB, VOUT, GND, ON/OFF

CRITICAL L1970 100uH-0.8A PLC: VESTA3V3_SW (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

=PP3V3_VESTA_REG
Vout = 3.3V @ 500mA

C1970 10uF N20P20% 50V CERM 2320
D1970 SMD MMBRM140XXG
CRITICAL C1971 100UF 20% 6.3V POLY B2

2.5V LDO

=PP3V3_VESTA_2V5REG → CRITICAL U1980 MM1572FN SOT-25A-LF (VIN, VOUT, CONT, NOISE, GND)

VESTA2V5_NOISE (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm)

=PP2V5_VESTA_LDO
Vout = 2.5V @ 150 mA

C1980 1uF 10% 6.3V CERM 402
C1981 0.01uF 20% 16V CERM 402
C1982 10UF 20% 6.3V X5R 603

Port Power Switch

=PPBUS_FWPWRSW → F1965 1.5A-24V MINISMDC → PPBUS_FWPWRSW_F (VOLTAGE=25V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL Q1965 NDS9407 SOI-LF

PPBUS_FW_FET_D (VOLTAGE=25V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL D1965 SMB B340XF → =PPBUS_FW_FET

R1965 470K 5% 1/16W MF-LF 402
C1965 0.01uF 20% 16V CERM 402
FWPWR_EN_L_DIV (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm)
R1966 330K 5% 1/16W MF-LF 402

=PP3V3_RUN_FWPORTPWRSW
R1960 100K 5% 1/16W MF-LF 402
FWPWR_EN_L (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm)
DP1960 BAS16TW-X-F SOT-363
FWPWR_RUN
FWPWR_EN
Q1960 2N7002 SOT23-LF
=FWPWR_PWRON
SYS_ACIN
R1961 10K 5% 1/16W MF-LF 402
FWPWR_ACIN
R1963 470K 5% 1/16W MF-LF 402

If =FWPWR_PWRON is NC:

Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

1.2V Regulator

=PP3V3_VESTA_1V2REG
R1990 10 5% 1/16W MF-LF 402
PPVOUT_VESTA1V2 (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)
C1990 10UF 20% 6.3V XSR 603

Burst Mode VESTA1V2_BURST
R1992 10K 5% 1/16W MF-LF 402
R1991 1M 5% 1/16W MF-LF 402
C1991 1uF 10% 6.3V CERM 402

Pulse Mode VESTA1V2_PULSE
R1993 10K 5% 1/16W MF-LF 402

Continuous Mode
R1994 1M 5% 1/16W MF-LF 402
R1995 324K 1% 1/16W MF-LF 402

SVIN PVIN U1990 LTC3411 MSOP-LF
SHDN/RT, SYNC/MODE, PGOOD, PGND, SGND, SW, VFB, ITH
VESTA1V2_RT, VESTA1V2_MODE, VESTA1V2_SW, VESTA1V2_VFB, VESTA1V2_ITH

CRITICAL L1990 2.2uH SM1-LF (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

=PP1V2_VESTA_REG
Vout = 0.8V * (1 + (R2 / R1))
Vout = 1.199V @ 1.2 A

<R2> R1997 4.99K 1% 1/16W MF-LF 402
C1992 22pF 5% 50V CERM 402
<R1> R1998 10K 1% 1/16W MF-LF 402
C1995 22uF 20% 6.3V X5R 805

CRITICAL
R1996 4.99K 1% 1/16W MF-LF 402
C1993 100pF 5% 50V CERM 402
VESTA1V2_ITH_RC
C1994 0.0033uF 10% 50V CERM 402
XW1990 SM
VESTA1V2_SGND (VOLTAGE=0V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

VESTA MISC

Reset circuit per Vesta design guide

67 66 65 18 10 =PP3V3_VESTA
R1950 20K 5% 1/16W MF-LF 402
R1951 10K 5% 1/16W MF-LF 402
VESTA_RESET_L_RC
VESTA_RESET
C1950 1uF 10% 6.3V CERM 402
Q01950 2N7002DW-X-F SOT-363 (two instances)

VESTA_RESET_L → RESET* (H4) Schmitt trigger (Int PU)

65 18 10 67 66 =PP3V3_VESTA
R1952 10K 5% 1/16W MF-LF 402

=JTAG_VESTA_TDI	D7	TDI
=JTAG_VESTA_TDO	E10	TDO
=JTAG_VESTA_TCK	E7	TCK
=JTAG_VESTA_TMS	E8	TMS
=JTAG_VESTA_TRST_L	D8	TRST*
TP_VESTA_DNC_B9	B9	DNC
TP_VESTA_DNC_C9	C9	DNC
TP_VESTA_DNC_E9	E9	DNC
NC	C3	NC
NC	M13	NC

R1952 to enable wirespeed feature

OMIT
U8500 BCM5462 FBGA-200 1 OF 3

2.5V_EN	M3	TP_VESTA_2_5V_EN
REGSUP1	E1	TP_VESTA_REGSUP1
REGSEN1	F1	TP_VESTA_REGSEN1
REGCTL1	G5	NC? TP_VESTA_REGCTL1
REGSUP2	E2	TP_VESTA_REGSUP2
REGSEN2	F2	TP_VESTA_REGSEN2
REGCTL2	G4	NC? TP_VESTA_REGCTL2

Power rails

=PPBUS_FW → L1900 FERR-EMI-600-OHM SM → =PP1V2_VESTA
PP1V2_VESTA_AVDDL (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

C1908 10UF 20% 6.3V X5R 603
C1900–C1903 0.1uF 20% 10V CERM 402 (L6/M6, L9/M9, N5/N6, N9/N10)
C1910–C1913 0.1uF 20% 10V CERM 402

DVDD (B1, B15, C15, J1) · AVDDL (L6, L9, M6, M9, N5, N6, N9, N10) · AVDD (P4, P5, P10, P11, R3, R12) · PVDD (A15, N4)

C1920–C1925 0.1uF 20% 10V CERM 402 → =PP2V5_VESTA
C1930–C1931 0.1uF 20% 10V CERM 402
C1940–C1943 0.1uF 20% 10V CERM 402 → =PP3V3_VESTA

OVDD (A1, A7, F15, K1)

AGND (H11, H12, J11, J12, L7, L8, M7, M8, N7, N8, P6, P7, P8, P9)
GND (A2, B2, B7, C14, F14, J2, K2)

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SIZE D | DRAWING NUMBER 051-6839 | REV. E
SCALE NONE | SHT 19 OF 115

Page Notes

Power aliases required by this page:
- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.

NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

VCore Bypassing

(25 Balls on I2)

4 X 10uF (0603)
25 X 1uF (0402)

=PPVCORE_PWRON_I2

C2146 10UF 20% 6.3V X5R 603
C2147 10UF 20% 6.3V X5R 603
C2148 10UF 20% 6.3V X5R 603
C2149 10UF 20% 6.3V X5R 603
C2120 1uF 10% 6.3V CERM 402
C2121 1uF 10% 6.3V CERM 402
C2122 1uF 10% 6.3V CERM 402
C2123 1uF 10% 6.3V CERM 402
C2124 1uF 10% 6.3V CERM 402
C2125 1uF 10% 6.3V CERM 402
C2126 1uF 10% 6.3V CERM 402
C2127 1uF 10% 6.3V CERM 402
C2128 1uF 10% 6.3V CERM 402
C2129 1uF 10% 6.3V CERM 402
C2130 1uF 10% 6.3V CERM 402
C2131 1uF 10% 6.3V CERM 402
C2132 1uF 10% 6.3V CERM 402
C2133 1uF 10% 6.3V CERM 402
C2134 1uF 10% 6.3V CERM 402
C2135 1uF 10% 6.3V CERM 402
C2136 1uF 10% 6.3V CERM 402
C2137 1uF 10% 6.3V CERM 402
C2138 1uF 10% 6.3V CERM 402
C2139 1uF 10% 6.3V CERM 402
C2140 1uF 10% 6.3V CERM 402
C2141 1uF 10% 6.3V CERM 402
C2142 1uF 10% 6.3V CERM 402
C2143 1uF 10% 6.3V CERM 402
C2144 1uF 10% 6.3V CERM 402

AA22 VDD15_0
AB21 VDD15_1
AC16 VDD15_2
AC19 VDD15_3
AC24 VDD15_4
AC7 VDD15_5
AD14 VDD15_6
AD17 VDD15_7
AD20 VDD15_8
AD23 VDD15_9
AD4 VDD15_10
AD7 VDD15_11
AE10 VDD15_12
AE13 VDD15_13
AE16 VDD15_14
AE19 VDD15_15
AE22 VDD15_16
AE4 VDD15_17
AE7 VDD15_18
AF15 VDD15_19
AF18 VDD15_20
AF21 VDD15_21
AF24 VDD15_22
AF9 VDD15_23
AG12 VDD15_24
AG17 VDD15_25
AG20 VDD15_26
AG23 VDD15_27
AG4 VDD15_28
AG7 VDD15_29

3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)

=PP3V3_PWRON_I2_IO1
=PP3V3_PWRON_I2_IO2
=PP3V3_PWRON_I2_MAXBUS
=PP3V3_PWRON_I2_AGPPCI

C2150 C2151 C2152 C2153 C2154 C2155 C2156 C2157 C2158 C2159 C2160 C2161 C2162 C2163 C2164 C2165 C2166 C2167 C2168 C2169 C2170 C2171 C2172 C2173 C2174 C2175 C2176 C2177 C2178 C2179 C2180 C2181 C2182 C2183 C2184 C2185 C2186 C2187 C2188 C2189 C2190 C2191 C2192 C2193 C2194 C2195 C2196 C2197
1uF 10% 6.3V CERM 402

C2199 10UF 20% 6.3V X5R 603

OMIT
U2100
I2
BGA
3.3V I/O POWER
(2 of 14)

VDD33_AGP
VDD33_0 AH17
VDD33_1 E3
VDD33_2 F5
VDD33_3 H3
VDD33_4 H6
VDD33_5 J8
VDD33_6 L10
VDD33_7 L3
VDD33_8 L6
VDD33_9 N13
VDD33_10 P12
VDD33_11 P3
VDD33_12 P6
VDD33_13 R14
VDD33_14 T13
VDD33_15 AB13
VDD33_16 AC15
VDD33_17 AC3
VDD33_18 AC6
VDD33_19 AF11
VDD33_20 AF3
VDD33_21 AF6
VDD33_22 AF9
VDD33_23 AJ3
VDD33_24 AJ6
VDD33_25 AM3
VDD33_26 Y13
VDD33_27 M16
VDD33_28 M18
VDD33_29 M22
VDD33_30 AC21
VDD33_31 AD20
VDD33_32 AD22
VDD33_33 AH20
VDD33_34 AH23
VDD33_35 AH24
VDD33_36 AH26
VDD33_37 AH27
VDD33_38 AL23
VDD33_39 AL24
VDD33_40 AL26
VDD33_41 AL27
VDD33_42 AL29
VDD33_43 AL30
VDD33_44 AP23
VDD33_45 AP26
VDD33_46 AP29
VDD33_47 AP32

For USB, Firewire, I2S and some GPIOs
VDD33_IO_1 (14)
For GPIOs, Pwr Mgt
VDD33_IO_2 (12)
VDD33_MAXBUS
VDD33_PCI (10)

OMIT
U2100
I2
BGA
PLL POWER
(3 of 14)

=PP1V5_PWRON_I2_PLL

R2101 4.7 5% 1/16W MF-LF 402
R2102 4.7 5% 1/16W MF-LF 402
R2103 4.7 5% 1/16W MF-LF 402
R2104 4.7 5% 1/16W MF-LF 402
R2105 4.7 5% 1/16W MF-LF 402
R2106 4.7 5% 1/16W MF-LF 402
R2107 4.7 5% 1/16W MF-LF 402
R2109 4.7 5% 1/16W MF-LF 402

C2101 C2102 C2103 C2104 C2105 C2106 C2107 C2109
1uF 10% 6.3V CERM 402

PP1V5_PWRON_I2_PLL1AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL2AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL3AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL4AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL5AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL6AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL7AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm
PP1V5_PWRON_I2_PLL9AVDD VOLTAGE=1.5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.2 mm

AA20 PLL1_AVDD
Y20 PLL1_VSSA
PLL1 32/48 MHZ
AA19 PLL2_AVDD
Y19 PLL2_VSSA
PLL2 45.16 MHZ
AK19 PLL3_AVDD
AJ19 PLL3_VSSA
PLL3 49.15 MHZ
H9 PLL4_AVDD
H10 PLL4_VSSA
PLL4 SYSCLK PCI(SS) AGP(SS)
AD9 PLL5_AVDD
AE9 PLL5_VSSA
PLL5 INT REF PCI AGP ATA
M24 PLL6_AVDD
N24 PLL6_VSSA
PLL6 SYS TRACK
AH22 PLL7_AVDD
AH21 PLL7_VSSA
PLL7 PCI TRACK
AK10 PLL9_AVDD
AL10 PLL9_VSSA
PLL9 AGP TRACK

OMIT
U2100
I2
BGA
CORE POWER & GND
(1 of 14)

AA13 VSS_0
AA15 VSS_1
AA17 VSS_2
AA21 VSS_3
AA25 VSS_4
AA29 VSS_5
AB12 VSS_6
AB15 VSS_7
AB16 VSS_8
AB22 VSS_9
AB24 VSS_10
AC2 VSS_11
AC20 VSS_12
AC25 VSS_13
AC26 VSS_14
AC29 VSS_15
AC32 VSS_16
AC35 VSS_17
AC5 VSS_18
AD16 VSS_19
AD21 VSS_20
AD29 VSS_21
AE14 VSS_22
AE15 VSS_23
AE17 VSS_24
AE19 VSS_25
AE20 VSS_26
AE25 VSS_27
AF10 VSS_28
AF18 VSS_29
AF2 VSS_30
AF27 VSS_31
AF29 VSS_32
AF32 VSS_33
AF35 VSS_34
AF5 VSS_35
AF8 VSS_36
AG11 VSS_37
AG14 VSS_38
AG29 VSS_39
AH14 VSS_40
AJ11 VSS_41
AJ14 VSS_42
AJ17 VSS_43
AJ2 VSS_44
AJ20 VSS_45
AJ23 VSS_46
AJ24 VSS_47
AJ26 VSS_48
AJ27 VSS_49
VSS_50 AJ29
VSS_51 AJ32
VSS_52 AJ35
VSS_53 AJ5
VSS_54 AJ8
VSS_55 AM11
VSS_56 AM14
VSS_57 AM17
VSS_58 AM2
VSS_59 AM20
VSS_60 AM23
VSS_61 AM26
VSS_62 AM29
VSS_63 AM32
VSS_64 AM35
VSS_65 AM5
VSS_66 AM7
VSS_67 AM8
VSS_68 AR11
VSS_69 AR14
VSS_70 AR17
VSS_71 AR2
VSS_72 AR20
VSS_73 AR23
VSS_74 AR26
VSS_75 AR29
VSS_76 AR32
VSS_77 AR35
VSS_78 AR5
VSS_79 AR8
VSS_80 B11
VSS_81 B14
VSS_82 B17
VSS_83 B2
VSS_84 B20
VSS_85 B23
VSS_86 B26
VSS_87 B29
VSS_88 B32
VSS_89 B35
VSS_90 B5
VSS_91 B8
VSS_92 E11
VSS_93 E14
VSS_94 E17
VSS_95 E2
VSS_96 E20
VSS_97 E23
VSS_98 E26
VSS_99 E29
E32 VSS_100
E35 VSS_101
E5 VSS_102
E8 VSS_103
H11 VSS_104
H12 VSS_105
H14 VSS_106
H15 VSS_107
H17 VSS_108
H18 VSS_109
H2 VSS_110
H20 VSS_111
H23 VSS_112
H24 VSS_113
H26 VSS_114
H27 VSS_115
H29 VSS_116
H32 VSS_117
H35 VSS_118
H5 VSS_119
H8 VSS_120
K10 VSS_121
K11 VSS_122
K14 VSS_123
K17 VSS_124
K20 VSS_125
K23 VSS_126
K25 VSS_127
K26 VSS_128
K29 VSS_129
L2 VSS_130
L20 VSS_131
L27 VSS_132
L29 VSS_133
L32 VSS_134
L35 VSS_135
L5 VSS_136
L8 VSS_137
M13 VSS_138
M15 VSS_139
M17 VSS_140
M19 VSS_141
M21 VSS_142
M23 VSS_143
M26 VSS_144
N14 VSS_145
N16 VSS_146
N18 VSS_147
N23 VSS_148
N25 VSS_149
VSS_150 P17
VSS_151 P2
VSS_152 P21
VSS_153 P24
VSS_154 P27
VSS_155 P29
VSS_156 P32
VSS_157 P35
VSS_158 P5
VSS_159 P8
VSS_160 R13
VSS_161 R15
VSS_162 R17
VSS_163 R19
VSS_164 R20
VSS_165 R22
VSS_166 R25
VSS_167 R29
VSS_168 T16
VSS_169 T18
VSS_170 T20
VSS_171 U13
VSS_172 U16
VSS_173 U2
VSS_174 U21
VSS_175 U25
VSS_176 U28
VSS_177 U32
VSS_178 U35
VSS_179 U5
VSS_180 U8
VSS_181 V12
VSS_182 V16
VSS_183 V20
VSS_184 V28
VSS_185 W15
VSS_186 W19
VSS_187 W21
VSS_188 W25
VSS_189 W26
VSS_190 Y11
VSS_191 Y16
VSS_192 Y18
VSS_193 Y2
VSS_194 Y22
VSS_195 Y29
VSS_196 Y32
VSS_197 Y35
VSS_198 Y5
VSS_199 Y8

I2 Power

SYNC_MASTER=MARIAS
SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 21 OF 115	

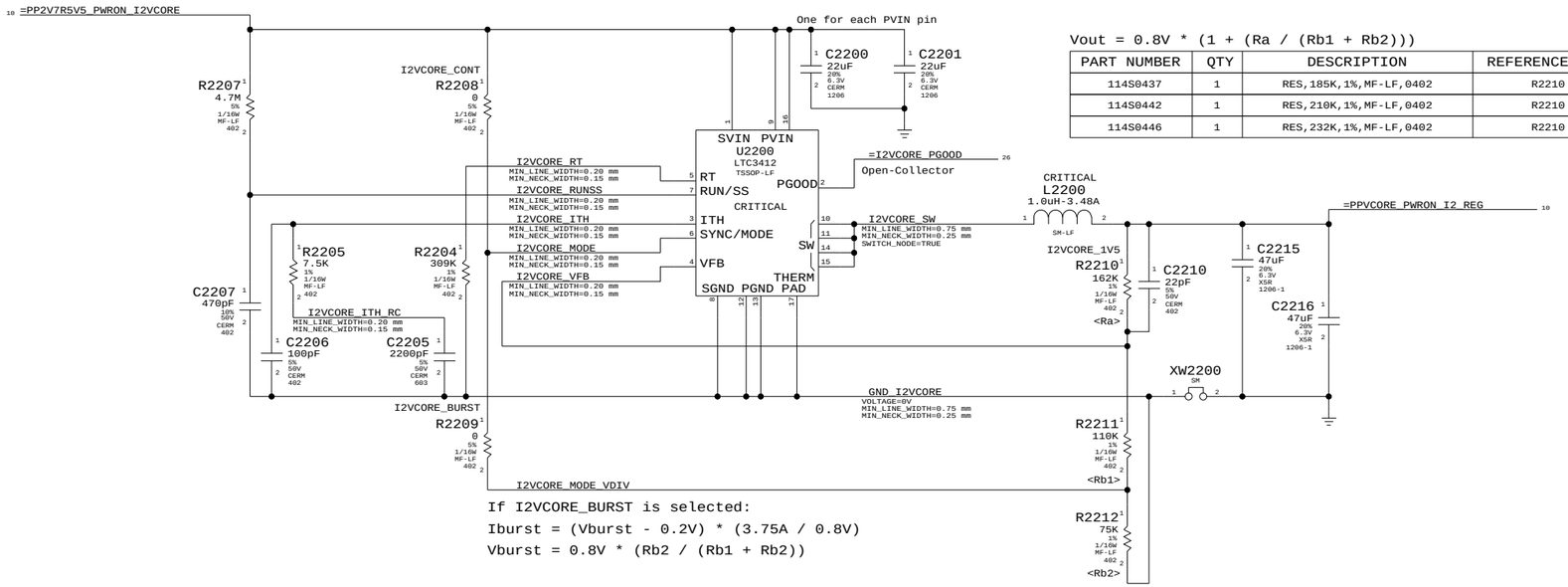
Page Notes

Power aliases required by this page:
- =PP2V7R5V5_PWRON_I2VCORE
- =PPVCORE_PWRON_I2_REG
- =PPVIN_PWRON_I2PLLVDD
- =PP1V5_PWRON_I2PLLVDD_LDO

Signal aliases required by this page:
- =I2VCORE_PGOOD

BOM options provided by this page:
- I2VCORE_CONT / I2VCORE_BURST
  Selects between forced continuous and burst mode for LTC3412 regulator.
- I2VCORE_xVx
  Selects appropriate resistor for the indicated LTC3412 output voltage.

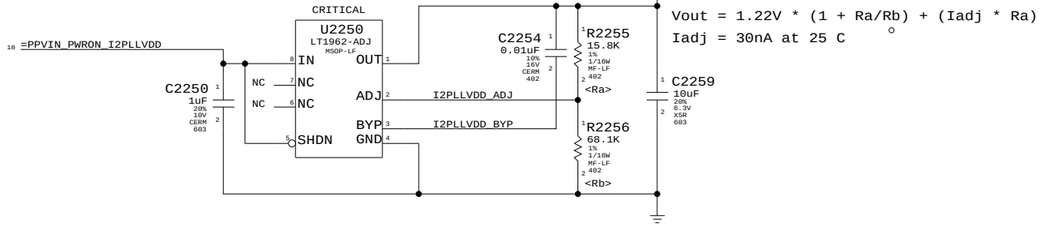
I2 VCore Regulator



Vout = 0.8V * (1 + (Ra / (Rb1 + Rb2)))

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0437	1	RES,185K,1%,MF-LF,0402	R2210		I2VCORE_1V6
114S0442	1	RES,210K,1%,MF-LF,0402	R2210		I2VCORE_1V7
114S0446	1	RES,232K,1%,MF-LF,0402	R2210		I2VCORE_1V8

I2 PLL LDO



I2 Power Supplies

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

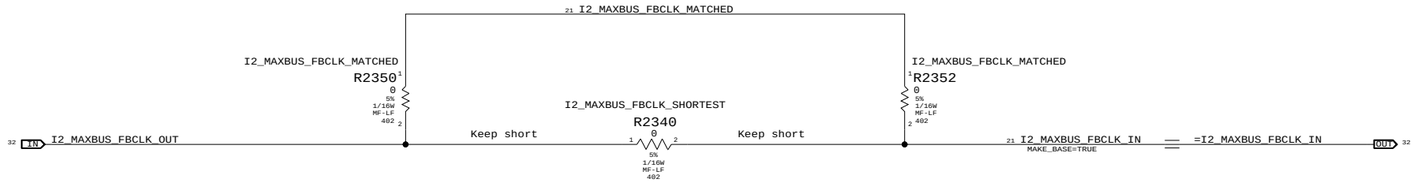
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

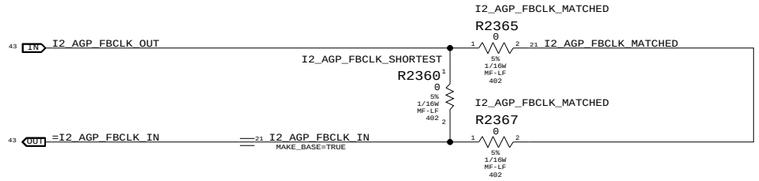
SCALE NONE SHT 22 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_IN 21
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_MATCHED 21
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_IN 21
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_MATCHED 21
I105	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_IN 21
I106	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_MATCHED 21
I119	CLOCK	CLOCK		=CLK33M_TBEN_SYNC 11 21
I120	CLOCK	CLOCK		=SYSCLK_TBEN_SYNC 11 21

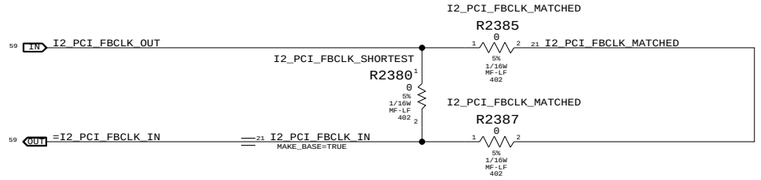
MaxBus Feedback Clock Network



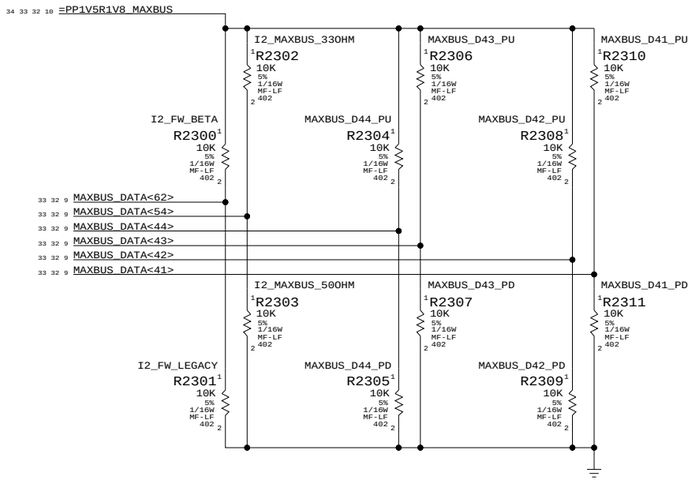
AGP Feedback Clock Ladder

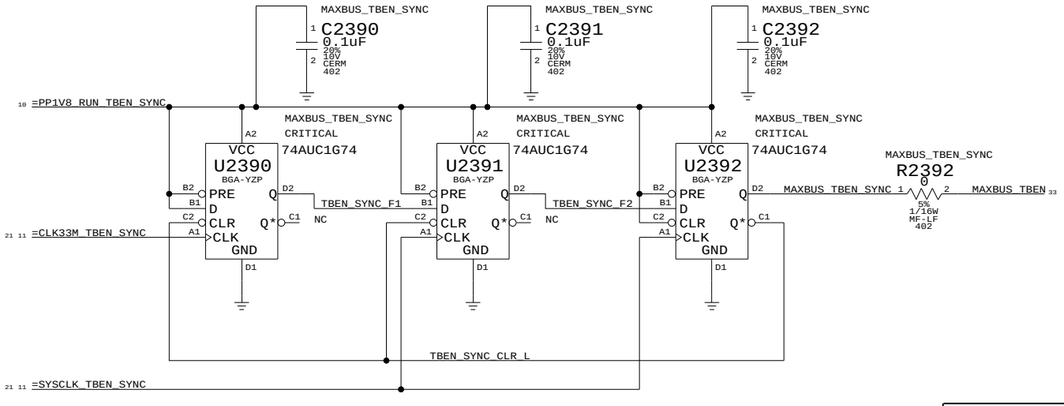


PCI Feedback Clock Ladder



I2 Configuration Straps





Signal	Tied	Description
MAXBUS_DATA<62>	HIGH	1394b Support (Beta Mode)
	LOW	1394a Support (Legacy Mode)
MAXBUS_DATA<54>	HIGH	50-Ohm MaxBus Drivers
	LOW	33-Ohm MaxBus Drivers
MAXBUS_DATA<44:41>	See Table Below	

BOM GROUP	Tied	Description	BOM OPTIONS
I2_MAXBUS_133MHZ	0000	133.12MHz CPU / 266.24MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_150MHZ	1000	149.76MHz CPU / 299.52MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_166MHZ	0100	166.40MHz CPU / 332.80MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_172MHZ	1100	171.95MHz CPU / 342.90MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_177MHZ	0010	177.49MHz CPU / 354.98MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_183MHZ	1010	183.04MHz CPU / 366.08MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_189MHZ	0110	188.59MHz CPU / 377.18MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_194MHZ	1110	194.13MHz CPU / 388.26MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_200MHZ	0001	199.68MHz CPU / 399.36MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD

I2 Supplemental

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 23 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTI	I2S	I2S	
I2S0_DTO	I2S	I2S	
I2S0_MCLK	I2S	I2S	
I2S0_BITCLK	I2S	I2S	
I2S0_SYNC	I2S	I2S	
I2S1_DTI	I2S	I2S	
I2S1_DTO	I2S	I2S	
I2S1_MCLK	I2S	I2S	
I2S1_BITCLK	I2S	I2S	
I2S1_SYNC	I2S	I2S	
I2_XTAL	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	

I2S0_DEV_TO_SB_DTI (7 22 74)
I2S0_SB_TO_DEV_DTO_R (6 22)
I2S0_MCLK_R (6 22)
I2S0_BITCLK_R (6 22)
I2S0_SYNC_R (6 22)
I2S1_DEV_TO_SB_DTI (22 30)
I2S1_SB_TO_DEV_DTO_R (6 22)
I2S1_MCLK_R (6 22)
I2S1_BITCLK_R (6 22)
I2S1_SYNC_R (6 22)
I2_CLK18M_XOUT_R (22)
I2_CLK18M_XOUT (22)
I2_CLK18M_XIN (22)

Page Notes

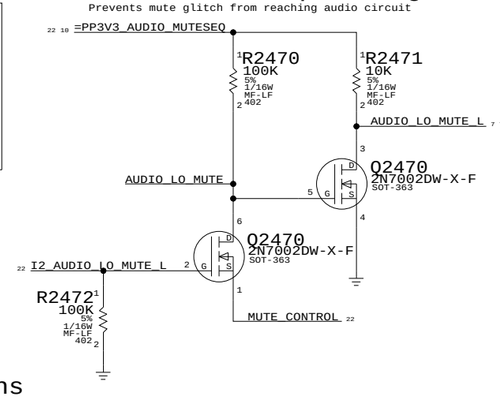
Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

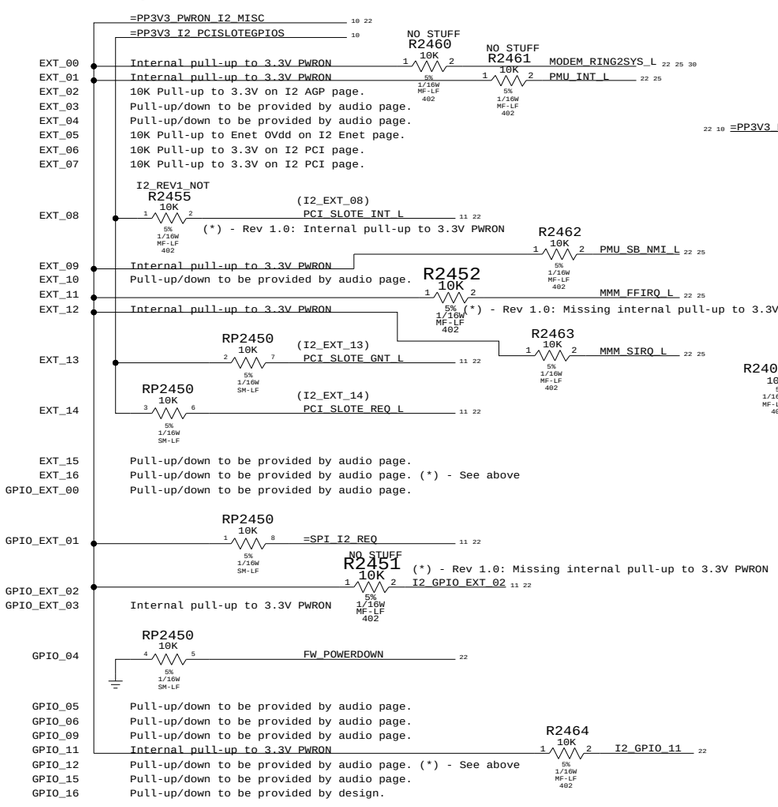
BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0

Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit



GPIO Pull-ups / Pull-downs



Signal Direction / Pin Direction

		Pin	Pin Direction	U2100 I2 BGA MISCELLANEOUS (4 OF 14) GPIO INTERFACE	Pin	Address	MPIC Int	Int PU?	Alt Func
30 25 22	MODEM_RING2SYS_L	AH1		EXT_00_H (Int PU)	EXT_00	0x0_0058	46 (0x2E)	Yes	PCI_REQ_2_L (When PCI1_Slot2En = 10)
25 22	PMU_INT_L	AK4		EXT_01_H (Int PU)	EXT_01	0x0_0059	47 (0x2F)	Yes	
44 43	AGP_INT_L	AT19		EXT_02_H	EXT_02	0x0_005A	48 (0x30)	No	
74 7	AUDIO_LI_OPTICAL_PLUG_L	AH2		EXT_03_H	EXT_03	0x0_005B	49 (0x31)	No	
74 7	AUDIO_LI_DET_L	J2		EXT_04_H	EXT_04	0x0_005C	50 (0x32)	No	
				EXT_05_H - See Ethernet Sym	EXT_05	0x0_005D	51 (0x33)	No	
59 11	PCI_SLOTA_INT_L	AR33		EXT_06_H	EXT_06	0x0_005E	52 (0x34)	No	
59 11	PCI_SLOTD_INT_L	AN33		EXT_07_H	EXT_07	0x0_005F	53 (0x35)	No	
	I2_EXT_08	AG4		EXT_08_H (Int PU - rev 1)	EXT_08	0x0_0060	54 (0x36)	Yes	
25 22	PMU_SB_NMI_L	AK1		EXT_09_H (Int PU)	EXT_09	0x0_0061	55 (0x37)	Yes	
74 7	AUDIO_LO_OPTICAL_PLUG_L	AG1		EXT_10_H	EXT_10	0x0_0062	56 (0x38)	No	
25 22	MMM_FFIRQ_L	AG3		EXT_11_H (Int PU)	EXT_11	0x0_0063	57 (0x39)	Yes	
25 22	MMM_SIRQ_L	AG2		EXT_12_H (Int PU)	EXT_12	0x0_0064	58 (0x3A)	Yes	
	I2_EXT_13	AF1		EXT_13_H	EXT_13	0x0_0065	59 (0x3B)	No	PCI_GNT_2_L (When PCI1_Slot2En = 11)
	I2_EXT_14	AE4		EXT_14_H	EXT_14	0x0_0066	60 (0x3C)	No	PCI_REQ_2_L (When PCI1_Slot2En = 11)
74 7	AUDIO_LO_DET_L	H1		EXT_15_H	EXT_15	0x0_0067	61 (0x3D)	No	
74 7	AUDIO_GPIO_11	G4		EXT_16_H (Int PU - rev 1)	EXT_16	0x0_0068	62 (0x3F)	Yes	
74 7	AUDIO_CODEC_RESET_L	AK2		GPIO_EXT_00_H	GPIO_00	0x0_006A	14 (0x0E)	No	
22 11	=SPI_I2_REQ	AJ1		GPIO_EXT_01_H	GPIO_01	0x0_006B	15 (0x0F)	No	SPIREQ (When SPISReqEn = 1)
22 11	I2_GPIO_EXT_02	AH4		GPIO_EXT_02_H (Int PU)	GPIO_02	0x0_006C	16 (0x10)	Yes	PCI_GNT_2_L (When PCI1_Slot2En = 10)
30	MODEM_RESET_L	AH3		GPIO_EXT_03_H (Int PU)	GPIO_03	0x0_006D	17 (0x11)	Yes	
22	FW_POWERDOWN	M1		GPIO_04_H	GPIO_04	0x0_006E	N/A	No	
22	I2_AUDIO_LO_MUTE_L	G3		GPIO_05_H	GPIO_05	0x0_006F	N/A	No	
22	I2_AUDIO_SPKR_MUTE_L	G1		GPIO_06_H	GPIO_06	0x0_0070	N/A	No	
74 7	AUDIO_I2S_DTIB_SEL	AG8		GPIO_09_H	GPIO_09	0x0_0073	N/A	No	
22	I2_GPIO_11	G2		GPIO_11_H (Int PU)	GPIO_11	0x0_0075	N/A	Yes	
74 7	AUDIO_SPDIFRX_RESET_L	AG7		GPIO_12_H (Int PU - rev 1)	GPIO_12	0x0_0076	N/A	Yes	
74 7	AUDIO_EXT_MCLK_SEL	AG6		GPIO_15_H	GPIO_15	0x0_0079	N/A	No	
				GPIO_16_H - See Ethernet Sym	GPIO_16	0x0_007A	N/A	No	

Alternate GPIO Functions

Use MAKE_BASE to force net name

22 11 PCI_SLOTE_INT_L
22 11 PCI_SLOTE_GNT_L
22 11 PCI_SLOTE_REQ_L

I2C

IIC_CLK_0_H	J1	=I2C_I2_NB_SCL	8
IIC_D_0_H	J3	=I2C_I2_NB_SDA	8
IIC_CLK_2_H	F4	=I2C_I2_SB_SCL	8
IIC_D_2_H	F1	=I2C_I2_SB_SDA	8

I2S 0

74 22 7 I2S0_DEV_TO_SB_DTI	E1	AUD_DTI_A_H	(Master) AUD_DTO_A_H	(Slave) I2S0_SB_TO_DEV_DTO_R 6 22
			C1	
		AUD_CLKOUT_A_H	F2	I2S0_MCLK_R 6 22
		AUD_BITCLK_A_H	F3	I2S0_BITCLK_R 6 22
		AUD_SYNC_A_H	D2	I2S0_SYNC_R 6 22

I2S 1

30 22 I2S1_DEV_TO_SB_DTI	J5	MOD_DTI_B_H	(Master) MOD_DTO_B_H	(Slave) I2S1_SB_TO_DEV_DTO_R 6 22
			G5	
		MOD_CLKOUT_B_H	J6	I2S1_MCLK_R 6 22
		MOD_BITCLK_B_H	J7	I2S1_BITCLK_R 6 22
		MOD_SYNC_B_H	G6	I2S1_SYNC_R 6 22

SCCA

24 7 SCCA_RXD	AG5	SCC_RXDA_H	SCC_TXDA_L	AE5 SCCA_TXD_L 7 24

SCCB/VIA

25 VIA_PMU_TO_SB	AL3	SCC_RXDB_H	SCC_TXDB_L	AL2 VIA_SB_TO_PMU 25
25 VIA_ACK_L	AM1	SCC_GPIOB_L	SCC_RTSB_L	AL4 VIA_REQ_L 25
25 VIA_CLK	AL1	SCC_TRXCB_H		

TEST/JTAG

I2_TST_TEI	AL6	TST_TEI_H		
I2_TST_PLLEN	AL5	TST_PLLEN_H		
=SPI_I2_MOSI				=SPI_I2_MISO
9 =JTAG_I2_TDI	AN6	JTG_TDI_H	JTG_TDO_H	AN4 =JTAG_I2_TDO 9
9 =JTAG_I2_TMS	AN2	JTG_TMS_H		
9 =JTAG_I2_TCK	AN3	JTG_TCK_H		
9 =JTAG_I2_TRST_L	AP1	JTG_TRSTN_L		
=SPI_I2_CLK				

POWER MGMT/CLOCK

62 25 22 SYS_WARM_RESET_L	AK3	REF_PURESET_L	PWR_PCI_PME_L	AK7 SYS_PME_L 25 62
11 =I2_STOPXTAL_L	AH7	PWR_STPXTL_L		
11 =I2_STOPCPU_L	AH6	PWR_STPCPU_L	PWR_INTRWD_H	AL7 SYS_WATCHDOG 25
25 NB_SUSPENDREQ_L	AH5	PWR_SPDREQ_L	PWR_SPDACK_L	AK5 NB_SUSPENDACK_L 25
Put crystal circuit close to I2				
22 I2_CLK18M_XOUT_R	AC12	REF_CLK_OUT	PWR_PENDINT_H	AK6 TP_I2_PENDINT
22 I2_CLK18M_XIN	AC13	REF_CLK_IN		

NO STUFF R2410 10M

R2411 0

CRITICAL Y2410 18.432M 8X4.5MM-SM1

22 I2_CLK18M_XOUT

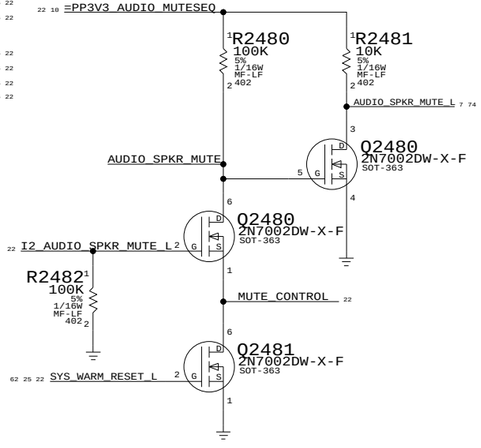
C2411 22pF 5% 50V CERM 402

C2410 22pF 5% 50V CERM 402

Crystal load capacitance is 16pF

Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit



I2 Miscellaneous

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 24 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
T72	CLOCK	CLOCK	
T73 PCI_ZDBOUT0	CLOCK	CLOCK	
T74 PCI_ZDBOUT1	CLOCK	CLOCK	
T75 PCI_ZDBOUT2	CLOCK	CLOCK	
T76 PCI_ZDBOUT3	CLOCK	CLOCK	

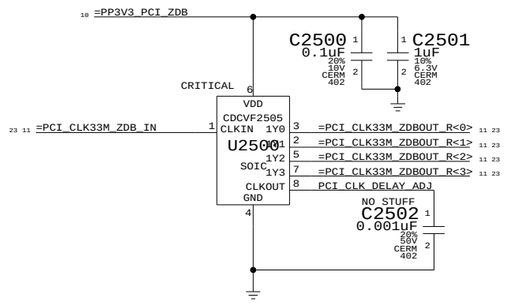
=PCI_CLK33M_ZDB_IN 11 23
=PCI_CLK33M_ZDBOUT_R<0> 11 23
=PCI_CLK33M_ZDBOUT_R<1> 11 23
=PCI_CLK33M_ZDBOUT_R<2> 11 23
=PCI_CLK33M_ZDBOUT_R<3> 11 23

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E
  is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0



PCI Clock Buffer

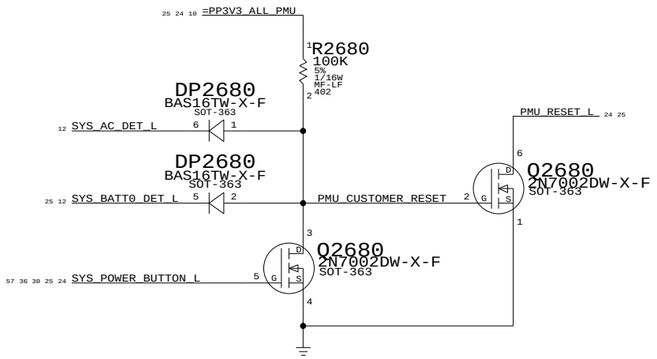
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

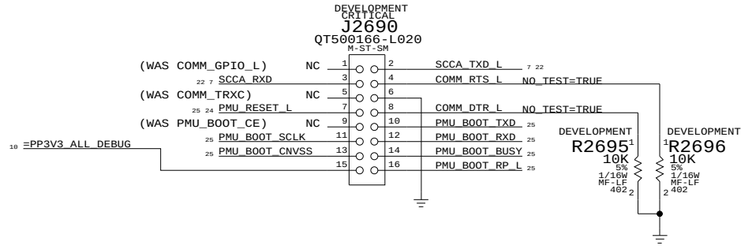
SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT
NONE	25 OF 115

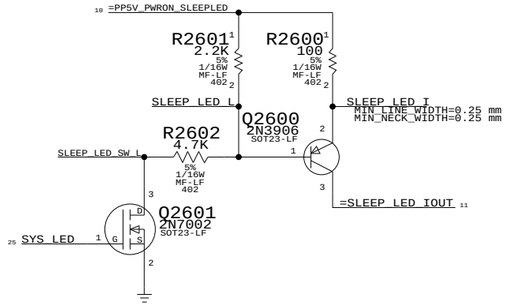
PMU RESET CIRCUIT



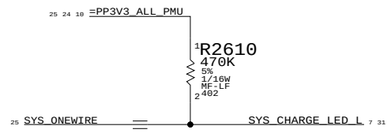
SERIAL DEBUG INTERFACE



SLEEP LED

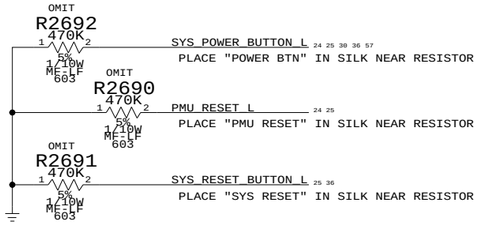


CHARGE LED



DEBUGGING AIDS

PLACE ON TOP SIDE NEAR FRONT EDGE OF BOARD



LEDs/Reset/Debug

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT: 26 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PMU_CLK10M_XTAL	XTAL	XTAL	
	XTAL	XTAL	
	XTAL	XTAL	
PMU_CLK32K_XTAL	XTAL	XTAL	
	XTAL	XTAL	
	XTAL	XTAL	

PMU_CLK10M_XIN 25
PMU_CLK10M_XOUT 25
PMU_CLK10M_XOUT_R 25
PMU_CLK32K_XIN 25
PMU_CLK32K_XOUT 25
PMU_CLK32K_XOUT_R 25

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_PMU
- =PP3V3_PWRON_PMU
- =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:
- =I2C_PMU_SCL
- =I2C_PMU_SDA
- =I2C_PMU_SMB_SCL
- =I2C_PMU_SMB_SDA
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =JTAG_BBANGER_TRST_L

NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page:
(NONE)

NOTE: TP_PMU_Px_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Px_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs

=PP3V3_ALL_PMU 10 24 25
- R2760 10K 5% 1/16W MF-LF 402 — PMU_POWER_UP_L 25 26
- R2761 10K 5% 1/16W MF-LF 402 — SYS_POWER_BUTTON_L 24 25 30 36 57

=PP3V3_PWRON_PMU 10
- R2765 10K 5% 1/16W MF-LF 402 — SYS_PME_L 22 25 62
- R2766 100K 5% 1/16W MF-LF 402 — SYS_RESET_BUTTON_L 24 25 36
- R2767 10K 5% 1/16W MF-LF 402 — SYS_OVERTEMP_L 7 11 25 30
- R2768 10K 5% 1/16W MF-LF 402 — VIA_REQ_L 22 25
- R2770 100K 5% 1/16W MF-LF 402 — SYS_COLD_RESET_L 25
- R2771 100K 5% 1/16W MF-LF 402 — SYS_WARM_RESET_L 22 25 62
- R2772 100K 5% 1/16W MF-LF 402 — PCI_RESET_L 11 25
- R2773 100K 5% 1/16W MF-LF 402 — NB_SUSPENDREQ_L 22 25
- R2774 100K 5% 1/16W MF-LF 402 — SYS_SLEEP 25

Power Management Unit

25 24 10 =PP3V3_ALL_PMU
- C2702 10UF 20% 6.3V X5R 603
- C2701 0.1uF 20% 10V CERM 402
- C2700 0.1uF 20% 10V CERM 402
- R2705 4.7 5% 1/10W MF-LF 402 — PP3V3_ALL_PMU_AVCC 10 (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)
- C2705 1uF 10% 6.3V CERM 402 — GND_PMU_AVSS 25 28 29 31

U2700 M30280F8-LF QFP-80 — VCC 13, AVCC 78

Spares (Analog capable)

11 TP_PMU_AN_P0_0	67	P0[0]	AN00	OMIT	RTS0*/CTS0*	P6[0]	43 GOV_RESET_L 11
11 TP_PMU_AN_P0_1	66	P0[1]	AN01		CLK0	P6[1]	42 PCI_RESET_L 11 25
11 TP_PMU_AN_P0_2	65	P0[2]	AN02		RxD0	P6[2]	41 SYS_WARM_RESET_L 22 25 62
11 TP_PMU_AN_P0_3	64	P0[3]	AN03		TxD0	P6[3]	40 SYS_COLD_RESET_L 25
11 TP_PMU_AN_P0_4	63	P0[4]	AN04		RTS1*/BUSY	P6[4]	31 PMU_BOOT_BUSY 24
11 TP_PMU_AN_P0_5	62	P0[5]	AN05		CLK1	P6[5]	30 PMU_BOOT_SCLK 24
25 TP_PMU_AN_P0_6	61	P0[6]	AN06		RxD1	P6[6]	29 PMU_BOOT_RXD 24
25 TP_PMU_AN_P0_7	60	P0[7]	AN07		TxD1	P6[7]	28 PMU_BOOT_TXD 24
							PMU_BOOT_RP_L 24
25 22 NB_SUSPENDREQ_L	59	P1[0]	AN20		SDA/TxD2/TA0out	P7[0]	27 TP_PMU_P7_0 25
22 NB_SUSPENDACK_L	58	P1[1]	AN21		SCL/RxD2/TA0in	P7[1]	26 TP_PMU_P7_1 25
11 PMU_CPU_CLK_EN	57	P1[2]	AN22		CLK2/TA1out	P7[2]	25 TP_PMU_P7_2 25
11 PMU_SYS_CLK_EN	56	P1[3]	AN23		TA1in	P7[3]	24 SYS_ACIN 12 13 18
36 25 24 SYS_RESET_BUTTON_L	55	P1[4]			TA2out	P7[4]	23 TP_PMU_P7_4 11 25
57 36 30 25 24 SYS_POWER_BUTTON_L	54	P1[5]	INT3*/ADtrig		TA2in	P7[5]	22 TP_PMU_P7_5 11 25
30 SYS_LID_OPEN	53	P1[6]	INT4*		TA3out	P7[6]	21 SYS_KBDLED 28
30 22 MODEM_RING2SYS_L	52	P1[7]	INT5*		TA3in	P7[7]	20 SYS_OVERTEMP_L 7 11 25 30
8 =I2C_PMU_SMB_SDA	51	P2[0]	ICOC0/SDAmm		TA4out	P8[0]	19 SYS_LED 24
8 =I2C_PMU_SMB_SCL	50	P2[1]	ICOC1/SCLmm		TA4in	P8[1]	18 PMU_BATT0_CHARGE 13
8 =I2C_PMU_SDA	49	P2[2]	ICOC2		INT0*	P8[2]	17 SYS_BATT0_DET_L 12 24
8 =I2C_PMU_SCL	48	P2[3]	ICOC3		INT1*	P8[3]	16 SYS_PME_L 22 25 62
9 =JTAG_BBANGER_TRST_L	47	P2[4]	ICOC4		INT2*	P8[4]	15 SYS_AC_DET 12
9 =JTAG_BBANGER_TMS	46	P2[5]	ICOC5		RP/NMI*	P8[5]	14 SYS_ONEWIRE 24
9 =JTAG_BBANGER_TDI	45	P2[6]	ICOC6		CE*/Xcout	P8[6]	8 25 PMU_CLK32K_XOUT_R
9 =JTAG_BBANGER_TCK	44	P2[7]	ICOC7		Xcin	P8[7]	7 25 PMU_CLK32K_XIN
25 11 TP_PMU_P3_0	39	P3[0]	CLK3		TB0in	P9[0]	5 VIA_ACK_L 22
25 11 TP_PMU_P3_1	38	P3[1]	Sin3		TB1in	P9[1]	4 VIA_REQ_L 22 25
25 11 TP_PMU_P3_2	37	P3[2]	Sout3		TB2in	P9[2]	3 PMU_INT_L 22
25 11 TP_PMU_P3_3	36	P3[3]			AN24	P9[3]	2 PMU_SB_NMI_L 22
22 SYS_WATCHDOG	35	P3[4]			CLK4/AN25	P9[5]	1 VIA_CLK 22
11 PMU_CPU_HRESET_L	34	P3[5]			Sout4/AN26	P9[6]	80 VIA_PMU_TO_SB 22
26 25 PMU_POWER_UP_L	33	P3[6]			Sin4//AN27	P9[7]	79 VIA_SB_TO_PMU 22
25 SYS_SLEEP	32	P3[7]					

Spares (Analog capable)

					AN0	P10[0]	76 TP_PMU_AN_P10_0 25
					AN1	P10[1]	74 TP_PMU_AN_P10_1 25
					AN2	P10[2]	73 TP_PMU_AN_P10_2 25
					AN3	P10[3]	72 TP_PMU_AN_P10_3 25
					KI0*/AN4	P10[4]	71 TP_PMU_AN_P10_4 25
					KI1*/AN5	P10[5]	70 TP_PMU_AN_P10_5 11 25
					KI2*/AN6	P10[6]	69 TP_PMU_AN_P10_6 11 25
					KI3*/AN7	P10[7]	68 TP_PMU_AN_P10_7 25

10 =PPVREF_PMU
- 24 PMU_BOOT_CNVSS — 6 PCNVSS
- 24 PMU_RESET_L — 9 RESET*
- 25 PMU_CLK10M_XOUT_R — 10 XOUT
- 25 PMU_CLK10M_XIN — 12 XIN
- 77 VREF

VSS 11, AVSS 75

25 24 10 =PP3V3_ALL_PMU
- D2710 MMBD914XXG SOT23
- R2710 150K 5% 1/16W MF-LF 402
- C2710 0.22uF 10% 6.3V CERM-X5R 402
- R2715 4.7K 5% 1/16W MF-LF 402
- C2720 1uF 10% 6.3V CERM 402
- XW2700 SM
- R2730 4.7K 5% 1/16W MF-LF 402
- NO STUFF R2740 10M 5% 1/16W MF-LF 402
- R2741 0 5% 1/16W MF-LF 402
- CRITICAL Y2740 10.0000M 8X4.5MM-SM1
- C2741 18pF 5% 50V CERM 402
- C2740 18pF 5% 50V CERM 402

25 PMU_CLK10M_XOUT

Keep crystal subcircuit close to PMU.
Y2740's load capacitance is 12pF

GND_PMU_AVSS 25 28 29 31 (VOLTAGE=0V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

NO STUFF R2750 10M 5% 1/16W MF-LF 402
CRITICAL Y2750 32.768K SM1
- R2751 0 5% 1/16W MF-LF 402 — PMU_CLK32K_XOUT 25
- C2750 12pF 5% 50V CERM 402
- C2751 12pF 5% 50V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0163	1	XTAL,32.768KHZ,4.1X1.5X0.9MM,SMD	Y2750	CRITICAL	?

Additional PMU05 "Modules"

MMM

25 TP_PMU_AN_P10_0	MMM_X_AXIS	29
25 TP_PMU_AN_P10_1	MMM_Y_AXIS	29
25 TP_PMU_AN_P10_2	MMM_Z_AXIS	29
25 TP_PMU_P7_0	MMM_FFIRQ_L	22
25 TP_PMU_P7_1	MMM_SIRQ_L	22
25 TP_PMU_AN_P0_7	MMM_ACC_SELFTEST	29
25 TP_PMU_AN_P0_6	MMM_ACC_PWRDOWN	29

ALS

25 TP_PMU_AN_P10_3	ALS_0_OUT	7 31
25 TP_PMU_AN_P10_4	ALS_1_OUT	28
25 TP_PMU_P7_2	ALS_GAIN_BOOST	7 28 31

CPU T-Diodes

25 11 TP_PMU_AN_P10_5	CPU0_TEMP	
25 11 TP_PMU_AN_P10_6	CPU1_TEMP	

SPI Dual Battery Charger

25 11 TP_PMU_P3_0	SPI_PMU_CHGR_CLK	
25 11 TP_PMU_P3_1	SPI_CHGR_TO_PMU_MISO	
25 11 TP_PMU_P3_2	SPI_PMU_TO_CHGR_MOSI	
25 11 TP_PMU_P3_3	SPI_PMU_CHGR_CS	
25 11 TP_PMU_P7_4	PMU_BATT1_DET_L	
25 11 TP_PMU_P7_5	PMU_BATT1_CHARGE	

Battery Current Mon

25 TP_PMU_AN_P10_7	BATT_ISNS	12

Power Management Unit (PMU05)

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 27 OF 115

POWER-UP
SLEEP
WAKE
SHUT-DOWN

ACTIVE-LOW, OUTPUT, OPEN-COLLECTOR
PMU_POWER_UP_L
100K pull-up to 3.3V_ALL on pg 13

R2900 0 5% 1/16W MF-LF 402
R2902 0 5% 1/16W MF-LF 402
5V3V3PWRON_EN_L
MAKE_BASE=TRUE
=5V3V3PWRON_EN_L

SYS_POWER_UP_L

=PP3V3_ALL_PWRSEQ
R2901 100K 5% 1/16W MF-LF 402
SYS_POWERUP
R2903 0 5% 1/16W MF-LF 402
FWPWR_PWRON
MAKE_BASE=TRUE
=FWPWR_PWRON

ACTIVE-HIGH, OUTPUT, PUSH-PULL
SYS_PWRSEQ_1
R2913 100K 5% 1/16W MF-LF 402
=PP5V_PWRON_PWRSEQ
R2929 100K 5% 1/16W MF-LF 402
Q2900 2N7002DW-X-F SOT-363
R2910 100K 5% 1/16W MF-LF 402
R2911 0 5% 1/16W MF-LF 402
1V8_1V5PWRON_EN_L
MAKE_BASE=TRUE
=1V8_1V5PWRON_EN_L
R2912 0 5% 1/16W MF-LF 402
SYS_PWRSEQ_1_L
2V5PWRON_EN_L
MAKE_BASE=TRUE
=2V5PWRON_EN_L

SYS_PWRSEQ_2_L
R2920 100K 5% 1/16W MF-LF 402
5VRUN_EN_L
R2921 100K 5% 1/16W MF-LF 402
5VRUNHD_EN_L
R2922 100K 5% 1/16W MF-LF 402
3V3RUN_EN_L

ACTIVE-HIGH, OUTPUT, PUSH-PULL
SYS_PWRSEQ_2
Q2910 2N7002DW-X-F SOT-363
Q2900 2N7002DW-X-F SOT-363
TPAD_SEQ_HW
R2943 0 5% 1/16W MF-LF 402
5VTPAD_EN_L
MAKE_BASE=TRUE
=5VPWRONTPAD_EN_L

=PP3V3_PWRON_PWRSEQ
TPAD_SEQ_PMU
R2948 100K 5% 1/16W MF-LF 402
Q2948 2N7002 SOT23-LF
SYS_PWRSEQ_TPAD_L

ACTIVE-LOW, OUTPUT, PUSH-PULL
SYS_PWRSEQ_3_L
R2930 0 5% 1/16W MF-LF 402
2V5RUN_EN_L

=PP5V_RUN_PWRSEQ
R2935 100K 5% 1/16W MF-LF 402
SYS_PWRSEQ_3_LS5
R2936 100K 5% 1/16W MF-LF 402
1V5RUN_EN
Q2910 2N7002DW-X-F SOT-363
Q2941 2N7002DW-X-F SOT-363

=PP3V3_PWRON_PWRSEQ
R2941 100K 5% 1/16W MF-LF 402
NO STUFF
R2940 0 5% 1/16W MF-LF 402
VCORE_CPU0_SHDN_L
1V8RUN_EN_L
Q2940 2N7002DW-X-F SOT-363

ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
SYS_PWRSEQ_4
NO STUFF
R2949 0 5% 1/16W MF-LF 402
=PP3V3_RUN_PWRSEQ
=PP3V3_ALL_PWRSEQ
=5V3VPWRON_PGOOD
=1V8_1V5PWRON_PGOOD
=2V5PWRON_PGOOD
=I2VCORE_PGOOD
PWRON_REGS_PGOOD
MAKE_BASE=TRUE
R2958 10K 5% 1/16W MF-LF 402
Q2941 2N7002DW-X-F SOT-363

ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
SYS_PWRSEQ_5
GPUVCORE_SHDN_L
R2951 0 5% 1/16W MF-LF 402
CPU_AVDD_EN

=VCORE_PGOOD
TP_VCORE_PGOOD
MAKE_BASE=TRUE

ACTIVE-LOW, OUTPUT, PUSH-PULL
SYS_PWRSEQ_6_L
=PP5V_RUN_PWRSEQ
R2965 100K 5% 1/16W MF-LF 402
NO STUFF
R2969 0 5% 1/16W MF-LF 402
=GPUVCORE_PGOOD
GPUVCORE_PGOOD
MAKE_BASE=TRUE
SYS_PWRSEQ_6_LS5
MAKE_BASE=TRUE
R2966 100K 5% 1/16W MF-LF 402
GPUVDD15_EN
R2967 0 5% 1/16W MF-LF 402
GPUPVDD_EN
Q2940 2N7002DW-X-F SOT-363

ANALOG INPUT, SENSE > 1.7V
SYS_PWRSEQ_FINAL
XW2970 SM
PP1V8_GPU_PVDD
Used to see if last rail is up

Power Sequencing

SYNC_MASTER=MARIAS
SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 29 OF 115	

FAN CONTROLLER

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
1520	THERM	THERM	THERM1_M	THERM1_M_P
1521	THERM	THERM	THERM1_M	THERM1_M_N
1530	THERM	THERM	THERM2_M	THERM2_M_P
1531	THERM	THERM	THERM2_M	THERM2_M_N
1532	THERM	THERM	THERM1_A	THERM1_A_P
1533	THERM	THERM	THERM1_A	THERM1_A_N
1534	THERM	THERM	THERM2_A	THERM2_A_P
1535	THERM	THERM	THERM2_A	THERM2_A_N
1536	THERM	THERM	THERM_D1	THERM_D1_P
1537	THERM	THERM	THERM_D1	THERM_D1_N
1538	THERM	THERM	THERM_D2	THERM_D2_P
1539	THERM	THERM	THERM_D2	THERM_D2_N

PLACE CLOSE TO CPU
MAIN1

27 THERM1_M_P — Q3001 2N3904LF SOT23 — 27 THERM1_M_N

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2

27 THERM2_M_P — Q3002 2N3904LF SOT23 — 27 THERM2_M_N

PLACE UNDERNEATH UPPER RAM
ALTERNATE1

27 THERM1_A_P — Q3003 2N3904LF SOT23 — 27 THERM1_A_N

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2

27 THERM2_A_P — Q3004 2N3904LF SOT23 — 27 THERM2_A_N

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

R3010	0 5% 1/16W MF-LF 402	27 THERM1_M_P — THERM_D1_P 27
R3011	0 5% 1/16W MF-LF 402	27 THERM1_M_N — THERM_D1_N 27
R3012	0 5% 1/16W MF-LF 402	27 THERM2_M_P — THERM_D2_P 27
R3013	0 5% 1/16W MF-LF 402	27 THERM2_M_N — THERM_D2_N 27

NO STUFF R3020	0 5% 1/16W MF-LF 402	27 THERM1_A_P — THERM_D1_P 27
NO STUFF R3021	0 5% 1/16W MF-LF 402	27 THERM1_A_N — THERM_D1_N 27
NO STUFF R3022	0 5% 1/16W MF-LF 402	27 THERM2_A_P — THERM_D2_P 27
NO STUFF R3023	0 5% 1/16W MF-LF 402	27 THERM2_A_N — THERM_D2_N 27

10 =PP3V3_ADT7467 — R3000 10 5% 1/16W MF-LF 402 — PP3V3_ADT7467 VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C3000 1uF 10% 6.3V CERM 603

C3001 0.1uF 20% 10V CERM 402

R3001 10K 5% 1/16W MF-LF 402

10 =PP5V_RUN_FANPWM — R3002 10K 5% 1/16W MF-LF 402 — R3003 10K 5% 1/16W MF-LF 402

10 =PP3V3_RUN_FANTACH — R3004 10K 5% 1/16W MF-LF 402 — R3005 10K 5% 1/16W MF-LF 402

U3000 ADT7467 QSOP-LF CRITICAL

10 =PPVCORE_CPU_ADT7467	14	VCCP	
8 =I2C_ADT7467_SDA	16	SDA	
8 =I2C_ADT7467_SCL	1	SCL	
27 THERM_D1_P	13	D1+	
27 THERM_D1_N	12	D1-	
27 THERM_D2_P	11	D2+	
27 THERM_D2_N	10	D2-	
	3	VCC	
	2	GND	
FAN1_PWM 7 31	15	PWM1/XTO	
FAN1_TACH 7 31	6	TACH1	
FAN2_PWM 7 31	5	PWM2/SMBALERT#	
FAN2_TACH 7 31	7	TACH2	
ADT7467_ADR_ENABLE_L	8	PWM3	
NC	4	TACH3	
=ADT7467_THERM_L 11	9	TACH4/THERM#/SMBALERT#/GPIO	

C3002 1000pF 10% 25V X7R 402

C3003 1000pF 10% 25V X7R 402

I2C READ ADDR = 0x5C, WRITE ADDR = 0x5D
(Device is connected so as to be backward compatible with the ADT7460.)

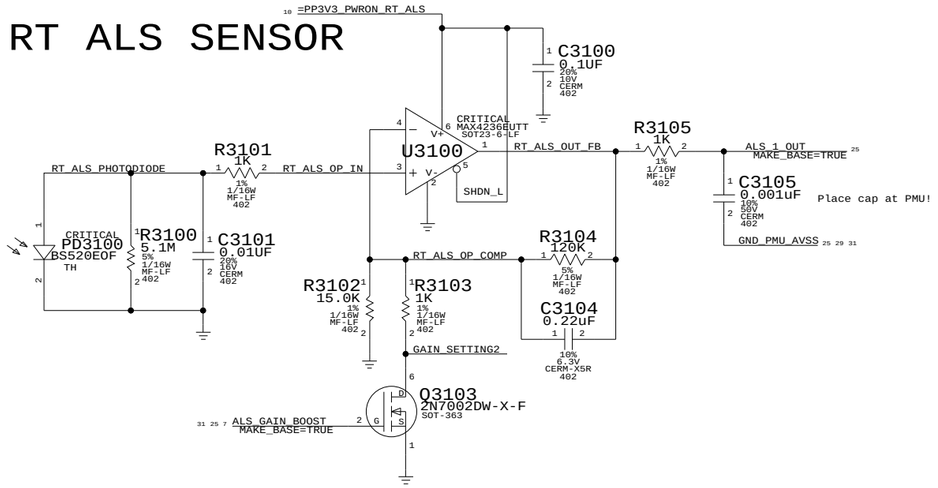
Fan Controller

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

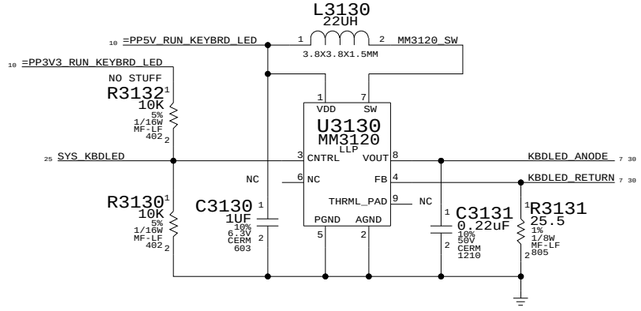
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 30 OF 115	

RT ALS SENSOR



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1191	353S1186		U3100	Primary is unity gain stable/Alt is stable at G=5

Keyboard LED Driver



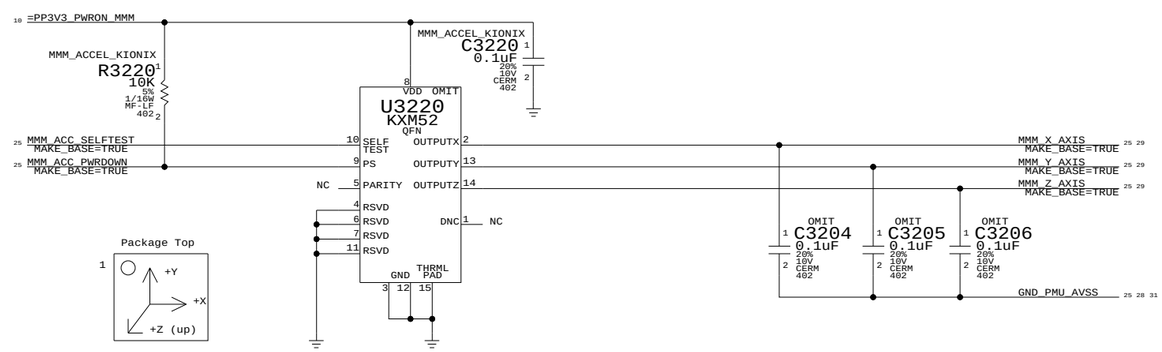
ALS Support

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 31 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I57	THERM	THERM	MMM_X_AXIS
I58	THERM	THERM	MMM_Y_AXIS
I59	THERM	THERM	MMM_Z_AXIS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC,KIONIX,KXM52-2050,3AXIS ACCELEROMETER,SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP,CER,0.033UF,10%,16V,X5R/X7R,0402,SMD	C3204,C3205,C3206	MMM_ACCEL_KIONIX

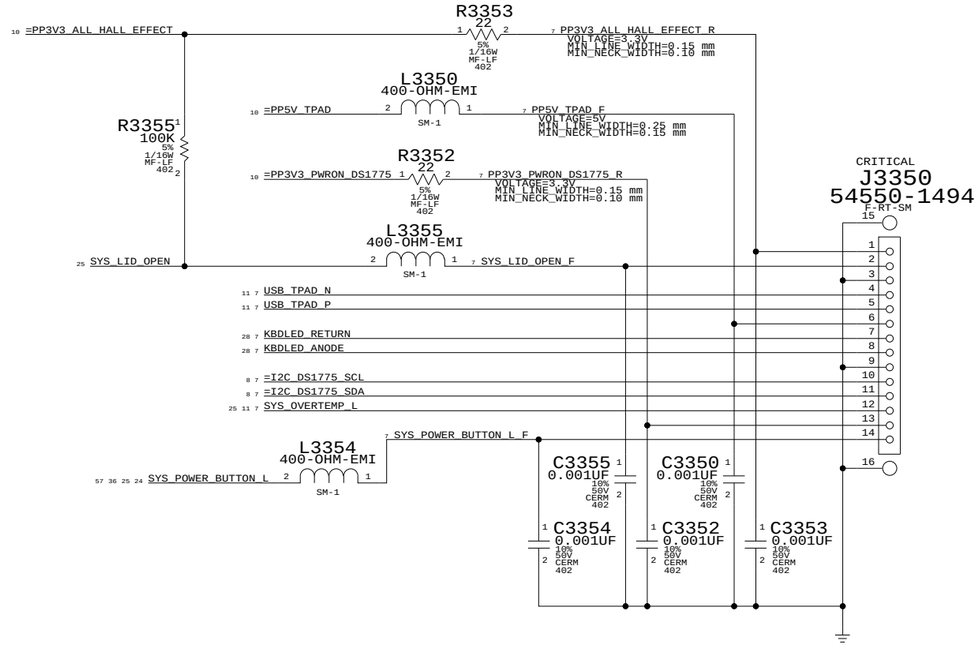
Sudden Motion Sensor

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

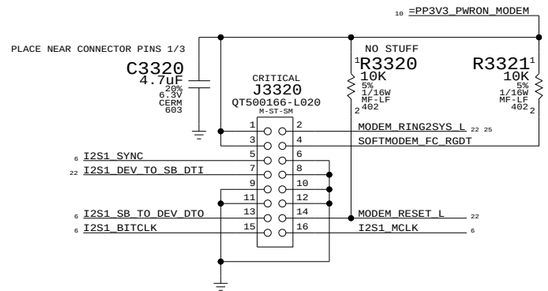
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 32 OF 115	

USB Trackpad Conn



SOFT MODEM CONN



Q41C Internal I/O I

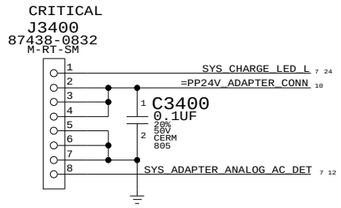
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

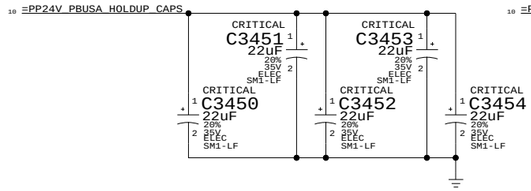
SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT	OF
NONE	33	115

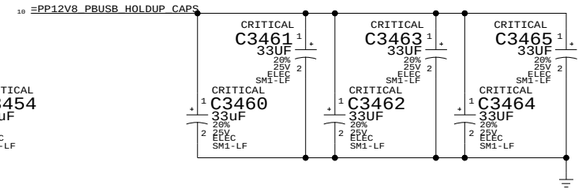
ADAPTER CONNECTOR



PBUS HOLD-UP CAPS

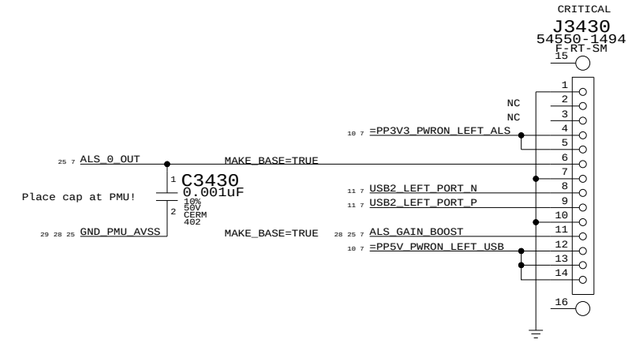


PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0085	126S0080		C3450,C3451,C3452,C3453,C3454	Primary is 260C/Alt is 250C part



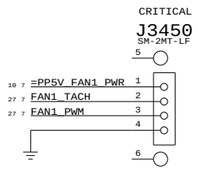
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0084	126S0079		C3460,C3461,C3462,C3463,C3464,C3465	Primary is 260C/Alt is 250C part

LEFT USB/LEFT ALS

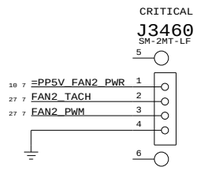


BACKUP BATTERY / RT USB CONNECTOR

CPU FAN



GPU FAN



Q41C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE: NONE

SHT 34 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS_CLK_CPU0	CLOCK	CLOCK	
MAXBUS_CLK_CPU1	CLOCK	CLOCK	
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK	
	I2_FBCLK	I2_FBCLK	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA41	MAXBUS	MAXBUS	
MAXBUS_DATA42	MAXBUS	MAXBUS	
MAXBUS_DATA43	MAXBUS	MAXBUS	
MAXBUS_DATA44	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA54	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA62	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR_R	MAXBUS	MAXBUS	
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS	
MAXBUS_DTI	MAXBUS	MAXBUS	
MAXBUS_GBL_L	MAXBUS	MAXBUS	
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS	
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_WT_L	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_DRDY_L	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS	
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS	
MAXBUS_CPU1_DRDY_L	MAXBUS	MAXBUS	
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS	

MAXBUS_CLK_CPU0_R	11 32
TP_MAXBUS_CLK_CPU1_R	11 32
I2_MAXBUS_FBCLK_OUT_R	32
I2_MAXBUS_FBCLK_OUT	21 32
MAXBUS_ADDR<0..31>	9 32 33
MAXBUS_DATA<0..40>	9 32 33
MAXBUS_DATA<41>	9 21 32 33
MAXBUS_DATA<42>	9 21 32 33
MAXBUS_DATA<43>	9 21 32 33
MAXBUS_DATA<44>	9 21 32 33
MAXBUS_DATA<45..53>	9 32 33
MAXBUS_DATA<54>	9 21 32 33
MAXBUS_DATA<55..61>	9 32 33
MAXBUS_DATA<62>	9 21 32 33
MAXBUS_DATA<63>	9 32 33
MAXBUS_TS_L	6 32 33
MAXBUS_TA_L	6 32 33
MAXBUS_TEA_L	6 32 33
MAXBUS_AACK_L	6 32 33
MAXBUS_ARTRY_L	6 32 33
MAXBUS_CI_L	9 32 33
MAXBUS_DTI<0..2>	9 32 33
MAXBUS_GBL_L	9 32 33
MAXBUS_TBST_L	9 32 33
MAXBUS_TSIZ<0..2>	9 32 33
MAXBUS_TT<0..4>	9 32 33
MAXBUS_WT_L	9 32 33
MAXBUS_CPU0_BG_L	6 32 33
MAXBUS_CPU0_BR_L	6 32 33
MAXBUS_CPU0_DBG_L	6 32 33
MAXBUS_CPU0_DRDY_L	6 32 33
MAXBUS_CPU0_HIT_L	6 32 33
MAXBUS_CPU1_BG_L	6 32
MAXBUS_CPU1_BR_L	6 32
MAXBUS_CPU1_DBG_L	6 32
MAXBUS_CPU1_DRDY_L	6 32
MAXBUS_CPU1_HIT_L	6 32

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_RUN_I2_MAXBUS - =PP1V5R1V8_PWRON_I2_MAXBUS

BOM options provided by this page:
- MAXBUS_1V8 - Provides required voltage divider for FBCLK if MaxBus OVdd=1.8V.

Signal aliases required by this page:
- =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

MaxBus I/O DECOUPLING

(41 Balls on I2)

OMIT
U2100
I2
BGA
MAXBUS POWER
(6 of 14)

VDD18_0	C11
VDD18_1	C14
VDD18_2	C17
VDD18_3	C20
VDD18_4	C23
VDD18_5	C26
VDD18_6	C29
VDD18_7	C3
VDD18_8	C32
VDD18_9	C8
VDD18_10	F11
VDD18_11	F14
VDD18_12	F17
VDD18_13	F20
VDD18_14	F23
VDD18_15	F26
VDD18_16	F29
VDD18_17	F8
VDD18_18	J11
VDD18_19	J12
VDD18_20	J14
VDD18_21	J15
VDD18_22	J17
VDD18_23	J18
VDD18_24	J20
VDD18_25	J23
VDD18_26	J24
VDD18_27	J26
VDD18_28	J27
VDD18_29	L14
VDD18_30	L17
VDD18_31	L23
VDD18_32	M20
VDD18_33	N15
VDD18_34	N19
VDD18_35	N21
VDD18_36	N22
VDD18_37	P14
VDD18_38	P15
VDD18_39	P18
VDD18_40	P22

PP1V5R1V8_I2_MAXBUS
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

1 X 10uF (0603)
41 X 1uF (0402)

C3550–C3590: 1uF 10% 6.3V CERM 402
C3599: 10uF 20% 6.3V X5R 603

R3550 0 5% 1/10W MF-LF 603 — =PP1V5R1V8_RUN_I2_MAXBUS
NO STUFF
R3551 0 5% 1/10W MF-LF 603 — =PP1V5R1V8_PWRON_I2_MAXBUS

I2_ACS_REF — R3500 1K 1% 1/16W MF-LF 402 — ACS_REF_H

21 =I2_MAXBUS_FBCLK_IN — MAXBUS_1V8 — R3506 360 5% 1/16W MF-LF 402 — 1.5V IN — MAX_CLK_FB_IN_H

OMIT
U2100
I2
BGA
PROCESSOR INTERFACE
(5 of 14)

PROCESSOR 0

33 32 MAXBUS_CPU0_QREQ_L	E25	MAX_QREQ_0_L	MAX_QACK_0_L	F18	MAXBUS_CPU0_QACK_L 33
33 32 6 MAXBUS_CPU0_BR_L	F21	MAX_BR_0_L	MAX_BG_0_L	E22	MAXBUS_CPU0_BG_L 6 32 33
33 32 6 MAXBUS_CPU0_DRDY_L	G25	MAX_DRDY_0_L	MAX_DBG_0_L	F24	MAXBUS_CPU0_DBG_L 6 32 33
33 32 6 MAXBUS_CPU0_HIT_L	E21	MAX_HIT_0_L	CPU_INT_0_L	J19	MAXBUS_CPU0_INT_L 6 34
			MAX_CLK_0_H	H21	MAXBUS_CLK_CPU0_R 11 32

PROCESSOR 1

32 MAXBUS_CPU1_QREQ_L	E27	MAX_QREQ_1_L	MAX_QACK_1_L	G18	TP_MAXBUS_CPU1_QACK_L 11
32 6 MAXBUS_CPU1_BR_L	G21	MAX_BR_1_L	MAX_BG_1_L	E24	MAXBUS_CPU1_BG_L 6 32
32 6 MAXBUS_CPU1_DRDY_L	F25	MAX_DRDY_1_L	MAX_DBG_1_L	G24	MAXBUS_CPU1_DBG_L 6 32
32 6 MAXBUS_CPU1_HIT_L	C21	MAX_HIT_1_L	CPU_INT_1_L	H19	MAXBUS_CPU1_INT_L 6
			MAX_CLK_1_H	J21	TP_MAXBUS_CLK_CPU1_R 11 32

MAXBUS INTERFACE

33 32 6 MAXBUS_TS_L	B27	MAX_TS_L	MAX_AACK_L	A31	MAXBUS_AACK_L 6 32 33
33 32 6 MAXBUS_ARTRY_L	C30	MAX_ARTRY_L			
33 32 9 MAXBUS_ADDR<0>	D18	MAX_A_00_H	MAX_D_00_H	D16	MAXBUS_DATA<0> 9 32 33
33 32 9 MAXBUS_ADDR<1>	A28	MAX_A_01_H	MAX_D_01_H	A10	MAXBUS_DATA<1> 9 32 33
33 32 9 MAXBUS_ADDR<2>	A19	MAX_A_02_H	MAX_D_02_H	A9	MAXBUS_DATA<2> 9 32 33
33 32 9 MAXBUS_ADDR<3>	A23	MAX_A_03_H	MAX_D_03_H	D12	MAXBUS_DATA<3> 9 32 33
33 32 9 MAXBUS_ADDR<4>	D21	MAX_A_04_H	MAX_D_04_H	A11	MAXBUS_DATA<4> 9 32 33
33 32 9 MAXBUS_ADDR<5>	A25	MAX_A_05_H	MAX_D_05_H	B10	MAXBUS_DATA<5> 9 32 33
33 32 9 MAXBUS_ADDR<6>	A18	MAX_A_06_H	MAX_D_06_H	C10	MAXBUS_DATA<6> 9 32 33
33 32 9 MAXBUS_ADDR<7>	C28	MAX_A_07_H	MAX_D_07_H	G16	MAXBUS_DATA<7> 9 32 33
33 32 9 MAXBUS_ADDR<8>	D25	MAX_A_08_H	MAX_D_08_H	D9	MAXBUS_DATA<8> 9 32 33
33 32 9 MAXBUS_ADDR<9>	B31	MAX_A_09_H	MAX_D_09_H	C9	MAXBUS_DATA<9> 9 32 33
33 32 9 MAXBUS_ADDR<10>	B24	MAX_A_10_H	MAX_D_10_H	F15	MAXBUS_DATA<10> 9 32 33
33 32 9 MAXBUS_ADDR<11>	G28	MAX_A_11_H	MAX_D_11_H	G15	MAXBUS_DATA<11> 9 32 33
33 32 9 MAXBUS_ADDR<12>	C25	MAX_A_12_H	MAX_D_12_H	B9	MAXBUS_DATA<12> 9 32 33
33 32 9 MAXBUS_ADDR<13>	D31	MAX_A_13_H	MAX_D_13_H	D10	MAXBUS_DATA<13> 9 32 33
33 32 9 MAXBUS_ADDR<14>	F19	MAX_A_14_H	MAX_D_14_H	E15	MAXBUS_DATA<14> 9 32 33
33 32 9 MAXBUS_ADDR<15>	E30	MAX_A_15_H	MAX_D_15_H	C7	MAXBUS_DATA<15> 9 32 33
33 32 9 MAXBUS_ADDR<16>	D27	MAX_A_16_H	MAX_D_16_H	B7	MAXBUS_DATA<16> 9 32 33
33 32 9 MAXBUS_ADDR<17>	A27	MAX_A_17_H	MAX_D_17_H	A8	MAXBUS_DATA<17> 9 32 33
33 32 9 MAXBUS_ADDR<18>	B28	MAX_A_18_H	MAX_D_18_H	F16	MAXBUS_DATA<18> 9 32 33
33 32 9 MAXBUS_ADDR<19>	B25	MAX_A_19_H	MAX_D_19_H	G13	MAXBUS_DATA<19> 9 32 33
33 32 9 MAXBUS_ADDR<20>	E19	MAX_A_20_H	MAX_D_20_H	E13	MAXBUS_DATA<20> 9 32 33
33 32 9 MAXBUS_ADDR<21>	G27	MAX_A_21_H	MAX_D_21_H	E12	MAXBUS_DATA<21> 9 32 33
33 32 9 MAXBUS_ADDR<22>	D30	MAX_A_22_H	MAX_D_22_H	D7	MAXBUS_DATA<22> 9 32 33
33 32 9 MAXBUS_ADDR<23>	C31	MAX_A_23_H	MAX_D_23_H	A7	MAXBUS_DATA<23> 9 32 33
33 32 9 MAXBUS_ADDR<24>	F28	MAX_A_24_H	MAX_D_24_H	G12	MAXBUS_DATA<24> 9 32 33
33 32 9 MAXBUS_ADDR<25>	F27	MAX_A_25_H	MAX_D_25_H	F12	MAXBUS_DATA<25> 9 32 33
33 32 9 MAXBUS_ADDR<26>	B30	MAX_A_26_H	MAX_D_26_H	F13	MAXBUS_DATA<26> 9 32 33
33 32 9 MAXBUS_ADDR<27>	E28	MAX_A_27_H	MAX_D_27_H	A6	MAXBUS_DATA<27> 9 32 33
33 32 9 MAXBUS_ADDR<28>	B18	MAX_A_28_H	MAX_D_28_H	E10	MAXBUS_DATA<28> 9 32 33
33 32 9 MAXBUS_ADDR<29>	C22	MAX_A_29_H	MAX_D_29_H	B6	MAXBUS_DATA<29> 9 32 33
33 32 9 MAXBUS_ADDR<30>	A17	MAX_A_30_H	MAX_D_30_H	C6	MAXBUS_DATA<30> 9 32 33
33 32 9 MAXBUS_ADDR<31>	B19	MAX_A_31_H	MAX_D_31_H	D6	MAXBUS_DATA<31> 9 32 33
			MAX_D_32_H	G7	MAXBUS_DATA<32> 9 32 33
33 32 9 MAXBUS_CI_L	A26	MAX_CI_L	MAX_D_33_H	A3	MAXBUS_DATA<33> 9 32 33
33 32 9 MAXBUS_GBL_L	A24	MAX_GBL_L	MAX_D_34_H	E6	MAXBUS_DATA<34> 9 32 33
33 32 9 MAXBUS_TBST_L	E16	MAX_TBST_L	MAX_D_35_H	F7	MAXBUS_DATA<35> 9 32 33
33 32 9 MAXBUS_TSIZ<0>	D19	MAX_TSIZ_0_H	MAX_D_36_H	C4	MAXBUS_DATA<36> 9 32 33
33 32 9 MAXBUS_TSIZ<1>	C18	MAX_TSIZ_1_H	MAX_D_37_H	D3	MAXBUS_DATA<37> 9 32 33
33 32 9 MAXBUS_TSIZ<2>	B21	MAX_TSIZ_2_H	MAX_D_38_H	G9	MAXBUS_DATA<38> 9 32 33
33 32 9 MAXBUS_TT<0>	B22	MAX_TT_0_H	MAX_D_39_H	D4	MAXBUS_DATA<39> 9 32 33
33 32 9 MAXBUS_TT<1>	D22	MAX_TT_1_H	MAX_D_40_H	B16	MAXBUS_DATA<40> 9 32 33
33 32 9 MAXBUS_TT<2>	E18	MAX_TT_2_H	MAX_D_41_H	C16	MAXBUS_DATA<41> 9 21 32 33
33 32 9 MAXBUS_TT<3>	A21	MAX_TT_3_H	MAX_D_42_H	A13	MAXBUS_DATA<42> 9 21 32 33
33 32 9 MAXBUS_TT<4>	A22	MAX_TT_4_H	MAX_D_43_H	A16	MAXBUS_DATA<43> 9 21 32 33
33 32 9 MAXBUS_WT_L	D24	MAX_WT_L	MAX_D_44_H	C13	MAXBUS_DATA<44> 9 21 32 33
			MAX_D_45_H	B15	MAXBUS_DATA<45> 9 32 33
			MAX_D_46_H	D15	MAXBUS_DATA<46> 9 32 33
			MAX_D_47_H	B12	MAXBUS_DATA<47> 9 32 33
			MAX_D_48_H	A14	MAXBUS_DATA<48> 9 32 33
			MAX_D_49_H	A12	MAXBUS_DATA<49> 9 32 33
			MAX_D_50_H	D13	MAXBUS_DATA<50> 9 32 33
			MAX_D_51_H	B13	MAXBUS_DATA<51> 9 32 33
			MAX_D_52_H	A15	MAXBUS_DATA<52> 9 32 33
			MAX_D_53_H	C15	MAXBUS_DATA<53> 9 32 33
			MAX_D_54_H	C5	MAXBUS_DATA<54> 9 21 32 33
			MAX_D_55_H	C12	MAXBUS_DATA<55> 9 32 33
			MAX_D_56_H	F6	MAXBUS_DATA<56> 9 32 33
			MAX_D_57_H	A5	MAXBUS_DATA<57> 9 32 33
			MAX_D_58_H	F9	MAXBUS_DATA<58> 9 32 33
			MAX_D_59_H	E9	MAXBUS_DATA<59> 9 32 33
			MAX_D_60_H	E7	MAXBUS_DATA<60> 9 32 33
			MAX_D_61_H	G10	MAXBUS_DATA<61> 9 32 33
			MAX_D_62_H	B4	MAXBUS_DATA<62> 9 21 32 33
			MAX_D_63_H	F10	MAXBUS_DATA<63> 9 32 33
			MAX_DTI_0_H	C27	MAXBUS_DTI<0> 9 32 33
			MAX_DTI_1_H	A30	MAXBUS_DTI<1> 9 32 33
			MAX_DTI_2_H	A29	MAXBUS_DTI<2> 9 32 33
			MAX_TA_L	G19	MAXBUS_TA_L 6 32 33
			MAX_TEA_L	D28	MAXBUS_TEA_L 6 32 33
			MAX_TBEN_H	C24	TP_MAXBUS_TBEN_I2
			MAX_FBCLK_OUT_H	J22	32 I2_MAXBUS_FBCLK_OUT_R

1.5V-1.8V OUT (Matches MaxBus OVdd)
Output impedance is 50 Ohms

R3505 10 5% 1/16W MF-LF 402 — I2_MAXBUS_FBCLK_OUT — 21 32

MaxBus Pull-ups / Pull-downs

34 33 21 10 =PP1V5R1V8_MAXBUS

One resistor for each of:
- MAXBUS_TS_L
- MAXBUS_TA_L
- MAXBUS_TEA_L
- MAXBUS_ARTRY_L
- MAXBUS_AACK_L
- (Spare)

6 =RP3510P1	RP3510 10K 5% 1/16W SM-LF
6 =RP3510P2	RP3510 10K 5% 1/16W SM-LF
6 =RP3510P3	RP3510 10K 5% 1/16W SM-LF
6 =RP3510P4	RP3510 10K 5% 1/16W SM-LF
6 =RP3511P1	RP3511 10K 5% 1/16W SM-LF
6 =RP3511P2	RP3511 10K 5% 1/16W SM-LF

I2 CPU0 Support

One resistor for each of:
- MAXBUS_CPU0_BR_L
- MAXBUS_CPU0_BG_L
- MAXBUS_CPU0_DBG_L
- MAXBUS_CPU0_DRDY_L
- MAXBUS_CPU0_HIT_L
- MAXBUS_CPU0_INT_L

6 =RP3511P3	RP3511 10K 5% 1/16W SM-LF
6 =RP3511P4	RP3511 10K 5% 1/16W SM-LF
6 =RP3512P1	RP3512 10K 5% 1/16W SM-LF
6 =RP3512P2	RP3512 10K 5% 1/16W SM-LF
6 =RP3512P3	RP3512 10K 5% 1/16W SM-LF
6 =RP3512P4	RP3512 10K 5% 1/16W SM-LF
33 32 MAXBUS_CPU0_QREQ_L	R3513 10K 5% 1/16W MF-LF 402

I2 CPU1 Support

One resistor for each of:
- MAXBUS_CPU1_BR_L
- MAXBUS_CPU1_BG_L
- MAXBUS_CPU1_DBG_L
- MAXBUS_CPU1_DRDY_L
- MAXBUS_CPU1_HIT_L
- MAXBUS_CPU1_INT_L

6 =RP3513P2	RP3513 10K 5% 1/16W SM-LF
6 =RP3513P3	RP3513 10K 5% 1/16W SM-LF
6 =RP3513P4	RP3513 10K 5% 1/16W SM-LF
6 =RP3514P1	RP3514 10K 5% 1/16W SM-LF
6 =RP3514P2	RP3514 10K 5% 1/16W SM-LF
6 =RP3514P3	RP3514 10K 5% 1/16W SM-LF
32 MAXBUS_CPU1_QREQ_L	R3514 10K 5% 1/16W MF-LF 402

I2 Processor Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 35 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
100R	CLOCK	CLOCK	

=MAXBUS_CPU0_CLK 11 33

Page Notes

Power aliases required by this page:

- =PP1V5R1V8_MAXBUS

Signal aliases required by this page:

- =MAXBUS_CPU0_CLK

BOM options provided by this page:

(NONE)

=PP1V5R1V8_MAXBUS 34 33 32 21 10

U3600 BGA (5 OF 6) XXGHZ-XXV A0-X-X

OVDD: B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8

OVDD: P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14

OMIT CRITICAL

TP_CPU0_OVDDSENSE1 E18 OVDDSENSE1

TP_CPU0_OVDDSENSE2 G18 OVDDSENSE2

(Kelvin sense points)

U3600 BGA (2 OF 6) XXGHZ-XXV A0-X-X

OMIT CRITICAL

32 9 MAXBUS_DATA<0>	R15	D0	
32 9 MAXBUS_DATA<1>	W15	D1	
32 9 MAXBUS_DATA<2>	T14	D2	
32 9 MAXBUS_DATA<3>	V16	D3	
32 9 MAXBUS_DATA<4>	W16	D4	
32 9 MAXBUS_DATA<5>	T15	D5	
32 9 MAXBUS_DATA<6>	U15	D6	
32 9 MAXBUS_DATA<7>	P14	D7	
32 9 MAXBUS_DATA<8>	V13	D8	
32 9 MAXBUS_DATA<9>	W13	D9	
32 9 MAXBUS_DATA<10>	T13	D10	
32 9 MAXBUS_DATA<11>	P13	D11	
32 9 MAXBUS_DATA<12>	U14	D12	
32 9 MAXBUS_DATA<13>	W14	D13	
32 9 MAXBUS_DATA<14>	R12	D14	
32 9 MAXBUS_DATA<15>	T12	D15	
32 9 MAXBUS_DATA<16>	W12	D16	
32 9 MAXBUS_DATA<17>	V12	D17	
32 9 MAXBUS_DATA<18>	N11	D18	
32 9 MAXBUS_DATA<19>	N10	D19	
32 9 MAXBUS_DATA<20>	R11	D20	
32 9 MAXBUS_DATA<21>	U11	D21	
32 9 MAXBUS_DATA<22>	W11	D22	
32 9 MAXBUS_DATA<23>	T11	D23	
32 9 MAXBUS_DATA<24>	R10	D24	
32 9 MAXBUS_DATA<25>	N9	D25	
32 9 MAXBUS_DATA<26>	P10	D26	
32 9 MAXBUS_DATA<27>	U10	D27	
32 9 MAXBUS_DATA<28>	R9	D28	
32 9 MAXBUS_DATA<29>	W10	D29	
32 9 MAXBUS_DATA<30>	U9	D30	
32 9 MAXBUS_DATA<31>	V9	D31	
32 9 MAXBUS_DATA<32>	W5	D32	
32 9 MAXBUS_DATA<33>	U6	D33	
32 9 MAXBUS_DATA<34>	T5	D34	
32 9 MAXBUS_DATA<35>	U5	D35	
32 9 MAXBUS_DATA<36>	W7	D36	
32 9 MAXBUS_DATA<37>	R6	D37	
32 9 MAXBUS_DATA<38>	P7	D38	
32 9 MAXBUS_DATA<39>	V6	D39	
32 9 MAXBUS_DATA<40>	P17	D40	
32 21 9 MAXBUS_DATA<41>	R19	D41	
32 21 9 MAXBUS_DATA<42>	V18	D42	
32 21 9 MAXBUS_DATA<43>	R18	D43	
32 21 9 MAXBUS_DATA<44>	V19	D44	
32 9 MAXBUS_DATA<45>	T19	D45	
32 9 MAXBUS_DATA<46>	U19	D46	
32 9 MAXBUS_DATA<47>	W19	D47	
32 9 MAXBUS_DATA<48>	U18	D48	
32 9 MAXBUS_DATA<49>	W17	D49	
32 9 MAXBUS_DATA<50>	W18	D50	
32 9 MAXBUS_DATA<51>	T16	D51	
32 9 MAXBUS_DATA<52>	T18	D52	
32 9 MAXBUS_DATA<53>	T17	D53	
32 21 9 MAXBUS_DATA<54>	W3	D54	
32 9 MAXBUS_DATA<55>	V17	D55	
32 9 MAXBUS_DATA<56>	U4	D56	
32 9 MAXBUS_DATA<57>	U8	D57	
32 9 MAXBUS_DATA<58>	U7	D58	
32 9 MAXBUS_DATA<59>	R7	D59	
32 9 MAXBUS_DATA<60>	P6	D60	
32 9 MAXBUS_DATA<61>	R8	D61	
32 21 9 MAXBUS_DATA<62>	W8	D62	
32 9 MAXBUS_DATA<63>	T8	D63	

DP0	T3	NC
DP1	W4	NC
DP2	T4	NC
DP3	W9	NC
DP4	M6	NC
DP5	V3	NC
DP6	N8	NC
DP7	W6	NC
DBG*	M2	MAXBUS_CPU0_DBG_L 6 32
DRDY*	R3	MAXBUS_CPU0_DRDY_L_R
DTI0	G1	MAXBUS_EDTI 33
DTI1	K1	MAXBUS_DTI<0> 9 32
DTI2	P1	MAXBUS_DTI<1> 9 32
DTI3	N1	MAXBUS_DTI<2> 9 32
TA*	K6	MAXBUS_TA_L 6 32
TEA*	L1	MAXBUS_TEA_L 6 32
HIT*	B2	MAXBUS_CPU0_HIT_L 6 32

R3600 0 5% 1/10W MF-LF 402 — PLACE RC GLITCH FILTER CLOSE TO CPU PIN

MAXBUS_CPU0_DRDY_L 6 32

C3600 10PF 5% 50V CERM 402

R3601 470 5% 1/10W MF-LF 402

CPU0_PULLDOWN

U3600 BGA (1 OF 6) XXGHZ-XXV A0-X-X

OMIT CRITICAL

32 6 MAXBUS_CPU0_BR_L	D2	BR*	
32 6 MAXBUS_CPU0_BG_L	M1	BG*	
32 6 MAXBUS_TS_L	L4	TS*	
	E11	A0	
	H1	A1	
	C11	A2	
	G3	A3	
32 9 MAXBUS_ADDR<0>	F10	A4	
32 9 MAXBUS_ADDR<1>	L2	A5	
32 9 MAXBUS_ADDR<2>	D11	A6	
32 9 MAXBUS_ADDR<3>	D1	A7	
32 9 MAXBUS_ADDR<4>	C10	A8	
32 9 MAXBUS_ADDR<5>	G2	A9	
32 9 MAXBUS_ADDR<6>	D12	A10	
32 9 MAXBUS_ADDR<7>	L3	A11	
32 9 MAXBUS_ADDR<8>	G4	A12	
32 9 MAXBUS_ADDR<9>	T2	A13	
32 9 MAXBUS_ADDR<10>	F4	A14	
32 9 MAXBUS_ADDR<11>	V1	A15	
32 9 MAXBUS_ADDR<12>	J4	A16	
32 9 MAXBUS_ADDR<13>	R2	A17	
32 9 MAXBUS_ADDR<14>	K5	A18	
32 9 MAXBUS_ADDR<15>	W2	A19	
32 9 MAXBUS_ADDR<16>	J2	A20	
32 9 MAXBUS_ADDR<17>	K4	A21	
32 9 MAXBUS_ADDR<18>	N4	A22	
32 9 MAXBUS_ADDR<19>	J3	A23	
32 9 MAXBUS_ADDR<20>	M5	A24	
32 9 MAXBUS_ADDR<21>	P5	A25	
32 9 MAXBUS_ADDR<22>	N3	A26	
32 9 MAXBUS_ADDR<23>	T1	A27	
32 9 MAXBUS_ADDR<24>	V2	A28	
32 9 MAXBUS_ADDR<25>	U1	A29	
32 9 MAXBUS_ADDR<26>	N5	A30	
32 9 MAXBUS_ADDR<27>	W1	A31	
32 9 MAXBUS_ADDR<28>	B12	A32	
32 9 MAXBUS_ADDR<29>	C4	A33	
32 9 MAXBUS_ADDR<30>	G10	A34	
32 9 MAXBUS_ADDR<31>	B11	A35	

AP0	C1	NC
AP1	E3	NC
AP2	H6	NC
AP3	F5	NC
AP4	G7	NC
TT0	E5	MAXBUS_TT<0> 9 32
TT1	E6	MAXBUS_TT<1> 9 32
TT2	F6	MAXBUS_TT<2> 9 32
TT3	E9	MAXBUS_TT<3> 9 32
TT4	C5	MAXBUS_TT<4> 9 32
TBST*	F11	MAXBUS_TBST_L 9 32
TSIZ0	G6	MAXBUS_TSIZ<0> 9 32
TSIZ1	F7	MAXBUS_TSIZ<1> 9 32
TSIZ2	E7	MAXBUS_TSIZ<2> 9 32
GBL*	E2	MAXBUS_GBL_L 9 32
WT*	D3	MAXBUS_WT_L 9 32
CI*	J1	MAXBUS_CI_L 9 32
AACK*	R1	MAXBUS_AACK_L 6 32
ARTRY*	N2	MAXBUS_ARTRY_L 6 32
SHD0*	E4	MAXBUS_SHD0_L 33
SHD1*	H5	MAXBUS_SHD1_L 33
SYSCLK	A10	=MAXBUS_CPU0_CLK 11 33
CLK_OUT	H2	TP_CPU0_CLKOUT ADD GND TP NEAR CLKOUT TP
TBEN	E1	MAXBUS_TBEN 21
QREQ*	P4	MAXBUS_CPU0_QREQ_L 32
QACK*	G5	MAXBUS_CPU0_QACK_L 32
CKSTP_IN*	A3	
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L 34

=PP1V5R1V8_MAXBUS 10 21 32 33 34

VIO DECOUPLING (28 PINS)

26 X 1UF (0402)
2 X 10UF (0603)

C3670 C3671 C3672 C3673 C3674 C3675 C3676 C3677 C3678 C3679
C3680 C3681 C3682 C3683 C3684 C3685 C3686 C3687 C3688 C3689
C3690 C3691 C3692 C3693 C3694 C3695
C3698 C3699

1uF 10% 6.3V CERM 402

10uF 20% 4V X5R 603

MAXBUS Straps

=PP1V5R1V8_MAXBUS 34 33 32 21 10

R3610 10K 5% 1/16W MF-LF 402 — MAXBUS_SHD0_L 33

R3611 10K 1% 1/16W MF-LF 402 — MAXBUS_SHD1_L 33

R3620 1K 1% 1/16W MF-LF 402 — MAXBUS_EDTI 33

A8 MaxBus (CPU0)

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 36 OF 115	

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS
- =PP3V3_PWRON_PLLSEL

Signal aliases required by this page:
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:
- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
  One of these must be selected to set the Maxbus voltage
  * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
  One of these must be selected to ensure the the above strap is interpreted correctly

U3600

A7PM BVSEL0 BVSEL — BGA (3 OF 6) — XXGHZ-XXV — A8-X.XX

34 CPU_BVSEL<0>	B7	BVSEL0	INT*	D4 MAXBUS_CPU0_INT_L 6 32
34 CPU0_PLL_CFG<0>	B8	PLL_CFG0	SMI*	F9 CPU0_SMI_L 34
34 CPU0_PLL_CFG<1>	C8	PLL_CFG1	MCP*	C9 CPU_MCP_L 34
34 CPU0_PLL_CFG<2>	C7	PLL_CFG2	SRESET*	A2 CPU0_SRESET_L 34
34 CPU0_PLL_CFG<3>	D7	PLL_CFG3	HRESET*	D8 =CPU_HRESET_L 11 34
34 CPU0_PLL_CFG<4>	A7	PLL_CFG4 CFGEXT (A7PM)	PMON_IN*	D9 CPU_PMON_IN_L 34
9 =JTAG_CPU0_TDI	B9	TDI	PMON_OUT*	A9 TP_CPU0_PMON_OUT_L
9 =JTAG_CPU0_TDO	A4	TDO	BMODE0*	G9 CPU0_BMODE0_L 34
9 =JTAG_CPU0_TMS	F1	TMS (OMIT)	BMODE1*	F8 CPU0_BMODE1_L 34
9 =JTAG_CPU0_TCK	C6	TCK	EXT_QUAL	A11 CPU0_EXT_QUAL 34
9 =JTAG_CPU0_TRST_L	A5	TRST* (CRITICAL)		
34 CPU_LSSD_MODE_L	E8	LSSD_MODE*	DFS2*	A12 CPU0_DFS2_L 34
34 CPU0_L1TSTCLK	G8	L1_TSTCLK	LVRAM*	B10 CPU0_LVRAM_L 34
34 CPU0_L2TSTCLK	B3	L2_TSTCLK	BVSEL1	E10 CPU_BVSEL<1> 34
		A7PM TEST0 TEST2 TEST3 TEST1 TEST4	DFS4*	B6 CPU0_DFS4_L 34
			PLL_CFG5	D10 CPU0_PLL_CFG<5> 34
			TEMP_ANODE	N18 TP_CPU0_TEMP_ANODE
			TEMP_CATHODE	N19 TP_CPU0_TEMP_CATHODE
			HPR_N	A6 TP_CPU0_HPR_N

CPU0 PLL CONFIG CIRCUITRY

34 33 32 21 10 =PP1V5R1V8_MAXBUS

CPU0_PLL0_1 R3720 10K 5% 1/16W MF-LF 402	CPU0_PLL1_1 R3722 10K	CPU0_PLL2_1 R3724 10K	CPU0_PLL3_1 R3726 10K	CPU0_PLL4_1 R3728 10K	CPU0_PLL5_1 R3730 10K	CPU0_PLL_CFG<0> 34
CPU0_PLL0_0 R3721 10K	CPU0_PLL1_0 R3723 10K	CPU0_PLL2_0 R3725 10K	CPU0_PLL3_0 R3727 10K	CPU0_PLL4_0 R3729 10K	CPU0_PLL5_0 R3731 10K	CPU0_PLL_CFG<1> 34
						CPU0_PLL_CFG<2> 34
						CPU0_PLL_CFG<3> 34
						CPU0_PLL_CFG<4> 34
						CPU0_PLL_CFG<5> 34

BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE

34 CPU0_BMODE0_L — R3704 22 5% 1/16W MF-LF 402 — =CPU_HRESET_L 11 34

A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

A8

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

MAXBUS VSEL

MAXBUS_1V5: 34 CPU_BVSEL<0> — R3703 10 5% 1/16W MF-LF 402 — =PP1V5R1V8_MAXBUS 10 21 32 33 34

MAXBUS_1V8: R3702 10 5% 1/16W MF-LF 402 2 (SPEC request this pull down resistor should less than 250 ohm)

CPU_A7PM: 34 CPU_BVSEL<1> — R3705 10K 5% 1/16W MF-LF 402 — =PP1V5R1V8_MAXBUS 10 21 32 33 34

CPU_A8: R3706 1K 5% 1/16W MF-LF 402 2

CPU PULLUPS

34 33 32 21 10 =PP1V5R1V8_MAXBUS

33 CPU_CHKSTP_OUT_L	R3752 10K 5% 1/16W MF-LF 402	
34 CPU_LSSD_MODE_L	R3753 10K	
34 CPU_MCP_L	R3756 10K	
34 CPU0_DFS2_L		R3765 10K
34 CPU0_LVRAM_L	R3766 10K	
34 CPU0_DFS4_L		R3767 10K
34 CPU0_L2TSTCLK	R3759 10K	
34 CPU_PMON_IN_L		R3758 10K
34 CPU0_BMODE1_L	R3707 1K PID<0> SELECT	
34 11 =CPU_HRESET_L		R3757 10K

INTERRUPT PULL-UPS

34 33 32 21 10 =PP1V5R1V8_MAXBUS

34 CPU0_SMI_L	R3769 10K 5% 1/16W MF-LF 402
34 CPU0_SRESET_L	R3771 10K 5% 1/16W MF-LF 402

CPU PULLDOWNS

34 CPU0_L1TSTCLK	R3761 1K 5% 1/16W MF-LF 402
34 CPU0_EXT_QUAL	R3772 1K 5% 1/16W MF-LF 402

CPU0 FREQUENCY CONFIGURATION

() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT F/2	DFS SUPPORT F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	-	001100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	-	010000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	-	100000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	-	101000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	-	101100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	100100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	-	110100	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	010100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	-	001000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	000100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	110000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.5X	(4.25X)	-	011000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	011110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_9.5X	(4.75X)	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_10.0X	5.0X	2.5X	101010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_10.5X	(5.25X)	-	100010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	100110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.5X	(5.75X)	-	000000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_12.0X	6.0X	3.0X	101110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_12.5X	(6.25X)	-	111110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	010110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.5X	(6.75X)	-	111000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_14.0X	7.0X	3.5X	110010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	000110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_16.0X	8.0X	4.0X	110110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	000010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_18.0X	9.0X	4.5X	001010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_20.0X	10.0X	5.0X	001110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	010010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_24.0X	12.0X	6.0X	011010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_28.0X	14.0X	7.0X	111010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0

A8 Configuration Straps

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 37 OF 115

Page Notes

Power aliases required by this page:

- =PPVCORE_CPU0

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

VCORE BULK CAPS

35 10 =PPVCORE_CPU0

40 X 1 UF (0402)

C3830 C3831 C3832 C3833 C3834 C3835 C3836 C3837
C3838 C3839 C3840 C3841 C3842 C3843 C3844 C3845
C3846 C3847 C3848 C3849 C3850 C3851 C3852 C3853
C3854 C3855 C3856 C3857 C3858 C3859 C3860 C3861

1UF 10% 6.3V CERM 402

35 10 =PPVCORE_CPU0

24 X 10 UF (0603)

C3800 C3801 C3802 C3803 C3804 C3805 C3806 C3807 C3808 C3809
C3810 C3811 C3812 C3813 C3814 C3815 C3816 C3817 C3818 C3819

10uF 20% 4V X5R 603

C3820 C3821 C3822 C3823

10uF 20% 4V X5R 603

35 10 =PPVCORE_CPU0

U3600
BGA
(4 OF 6)
XXGHZ-XXV
A8-X.X.X

OMIT
CRITICAL

H8			A18
H10			B17
H12			B19
J7			C13
J9			E13
J11			E16
J13			F12
K8			F17
K10			F19
K12			G11
K14	VDD	VDD	G16
L7			H14
L9			H17
L11			H19
L13			M14
M8			M16
M10			M18
M12			N15
A13			P16
A16			P18
TP_CPU0_SENSEVDD1	N12	SENSEVDD1	AVDD A8 =PPAVDD_CPU0 10
TP_CPU0_SENSEVDD2	G13	SENSEVDD2	

(Kelvin sense points)

U3600
BGA
(6 OF 6)
XXGHZ-XXV
A8-X.X.X

OMIT
CRITICAL

B5			P12
C3			R5
D6			R14
D13			R17
E17			T7
F3			T10
G17			U3
H4			U13
H7			U17
H9			V5
H11			V8
H13			V11
J6			V15
J8			A17
J10			A19
J12	GND	GND	B13
K7			B16
K3			B18
K9			E12
K11			E19
K13			F13
L6			F16
L8			F18
L10			G19
L12			H18
M4			J14
M7			L14
M9			M15
M11			M17
M13			M19
N7			N14
P3			N16
P9			P15
			P19
TP_CPU0_SENSEGND1	N13	SENSEGND1	
TP_CPU0_SENSEGND2	G12	SENSEGND2	

(Kelvin sense points)

NC	A14	N/C_1	N/C_21 C17 NC
NC	B14	N/C_2	N/C_22 D17 NC
NC	C14	N/C_3	N/C_23 C18 NC
NC	D14	N/C_4	N/C_24 D18 NC
NC	E14	N/C_5	N/C_25 C19 NC
NC	F14	N/C_6	N/C_26 D19 NC
NC	G14	N/C_7	N/C_27 H16 NC
NC	A15	N/C_8	N/C_28 J16 NC
NC	B15	N/C_9	N/C_29 K16 NC
NC	C15	N/C_10	N/C_30 L16 NC
NC	D15	N/C_11	N/C_31 J17 NC
NC	E15	N/C_12	N/C_32 K17 NC
NC	F15	N/C_13	N/C_33 L17 NC
NC	G15	N/C_14	N/C_34 J18 NC
NC	H15	N/C_15	N/C_35 K18 NC
NC	J15	N/C_16	N/C_36 L18 NC
NC	K15	N/C_17	N/C_37 J19 NC
NC	L15	N/C_18	N/C_38 K19 NC
NC	C16	N/C_19	N/C_39 L19 NC
NC	D16	N/C_20	

A8 Power (CPU0)

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 38 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
14mil	THERM	THERM	
14mil	THERM	THERM	

VCORE_SNS 36
VCORE_GNDSNS 36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0270	1	RES,3.48K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V22
114S0258	1	RES,2.61K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V22
114S0246	1	RES,2.0K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V28
114S0294	1	RES,6.04K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V28
114S0276	1	RES,4.02K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V30
114S0254	1	RES,2.43K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V30
114S0246	1	RES,2.0K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V33
114S0294	1	RES,6.04K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V33

(WITH VCORE OFFSET)

1.5GHZ
1.260V -> 0.940V
(CPU SPEC: 1.220V -> 0.930V)

1.67GHZ
1.320V -> 0.940V
(CPU SPEC: 1.280V -> 0.930V)

1.67GHZ
1.340V -> 0.940V
(CPU SPEC: 1.300V -> 0.930V)

1.67GHZ
1.370V -> 0.940V
(CPU SPEC: 1.330V -> 0.930V)

"Low" and "Mid" States

"High" State

36 10 =PP3V3_PWRON_CPUVCORE_VID

"Low" and "Mid" States				"High" State			
NO STUFF R3980 470K	Q16BST&Q41 R3982 470K	Q16BST&Q41 R3984 470K	Q16BST&Q41 R3986 470K	NO STUFF R3970 470K	NO STUFF R3972 470K	NO STUFF R3974 470K	NO STUFF R3976 470K
VCORE_VID_A<1> 36	VCORE_VID_A<2> 36	VCORE_VID_A<3> 36	VCORE_VID_A<4> 36	VCORE_VID_B<1> 36	VCORE_VID_B<2> 36	VCORE_VID_B<3> 36	VCORE_VID_B<4> 36
Q16BST&Q41 R3981 470K	NO STUFF R3983 470K	NO STUFF R3985 470K	NO STUFF R3987 470K	NO STUFF R3971 470K	NO STUFF R3973 470K	NO STUFF R3975 470K	NO STUFF R3977 470K
<D4>	<D3>	<D2>	<D1>	<D4>	<D3>	<D2>	<D1>

CPU_VCORE_3STATES
CRITICAL
VCC U3990 74CBTLV3257 QSOP SYM_VER-2
A1 B1 A2 B2 A3 B3 A4 B4 SEL OE GND
Y1 Y2 Y3 Y4 VID_MUX_OE_L
36 VCORE_VID_A<1> 2
36 VCORE_VID_B<1> 3
36 VCORE_VID_A<2> 5
36 VCORE_VID_B<2> 6
36 VCORE_VID_A<3> 11
36 VCORE_VID_B<3> 10
36 VCORE_VID_A<4> 14
36 VCORE_VID_B<4> 13
11 =CPU0_VID_AB_SEL 1
15
16
8
4 VCORE_VID<1> 36
7 VCORE_VID<2> 36
9 VCORE_VID<3> 36
12 VCORE_VID<4> 36

CPU_VCORE_3STATES
C3990 0.1uF 20% 10V CERM 402

CPU_VCORE_3STATES
CRITICAL
R3990 1K 5% 1/16W MF-LF 402

Pullup on =CPU0_VID_AB_SEL will set default mux state to VID_B.

CPU_VCORE_2STATES
RP3990 0 5% 1/16W SM-LF
8 7 6 5
1 2 3 4
36 VCORE_VID_A<1>
36 VCORE_VID_A<2>
36 VCORE_VID_A<3>
36 VCORE_VID_A<4>

Keep trace fat (1.00-2.54 mm) and short!!

10 =PPVIN_CPUVCORE_MAX1717

CRITICAL C3937 10uF 10% 25V X5R 1206	CRITICAL C3938 10uF 10% 25V X5R 1206	CRITICAL C3939 10uF 10% 25V X5R 1206	CRITICAL C3940 10uF 10% 25V X5R 1206	CRITICAL C3941 10uF 10% 25V X5R 1206	CRITICAL C3942 10uF 10% 25V X5R 1206	CRITICAL C3943 10uF 10% 25V X5R 1206
CRITICAL C3944 10uF 10% 25V X5R 1206	CRITICAL C3945 10uF 10% 25V X5R 1206	CRITICAL C3946 10uF 10% 25V X5R 1206	CRITICAL C3947 10uF 10% 25V X5R 1206	CRITICAL C3948 10uF 10% 25V X5R 1206	CRITICAL C3949 10uF 10% 25V X5R 1206	

10 =PP5V_PWRON_CPUVCORE_VDD

PLACE CLOSE TO TO PINS 15 & 13
D3901 SOD-123 B0530WXF
VCORE_BOOST

C3900 1UF 20% 10V CERM 603

10 =PP5V_PWRON_CPUVCORE_PWRSEQ
R3965 100K 1% 1/16W MF-LF 402
26 VCORE_CPU0_SHDN_L

R3960 20 5% 1/16W MF-LF 402

VCORE_VCC
VOLTAGE=12.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

R3961 0 5% 1/16W MF-LF 402
C3960 1UF 20% 10V CERM 603

R3962 27.4K 1% 1/16W MF-LF 402

VCC U3900 MAX1717 QSOP-LF
VDD
SKP/SDN
FBS
ILIM
GNDS
A/B
REF
TON
CC
D0
D1
D2
D3
D4
V+
BST
DH
LX
DL
GND
FB
TIME
VGATE

(VCORE_VPLUS)
R3951 2.2 5% 1/16W MF-LF 603
22 VCORE_BST2
24
VCORE_DH
C3951 0.1UF 20% 25V CERM 603
23 VCORE_LX
14 VCORE_DL
13 VCORE_GND
4 VCORE_FB
3 VCORE_TIME
12 =VCORE_PGOOD 26

(VCORE_SNS) 5
(VCORE_GNDSNS) 11
VCORE_ILIM 10
VCORE_REF 9
VCORE_TON 8
VCORE_CC 6

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.15 mm
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.15 mm

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
NO STUFF C3902 0.0047uF 10% 25V CERM 402
CRITICAL Q3900 HAT2168H LFPAK
CRITICAL Q3902 HAT2160H LFPAK
CRITICAL Q3903 HAT2160H LFPAK
C3903 0.0022UF 10% 50V CERM 402

XW3910 SM
R3910 100 5% 1/16W MF-LF 402
C3950 0.001UF 20% 50V CERM 402
XW3911 SM
R3950 390K 5% 1/16W MF-LF 402

Keep trace fat and short!!
CRITICAL L3900 1.0UH-20.5 SM1
CRITICAL D3900 SNM540XF
CPU_VCORE_SNUB
NO STUFF R3901 2.2 5% 1/4W MF-LF 1206
NO STUFF C3901 0.0022UF 10% 50V CERM 603

XW3900 SM
CPUVCORE_VSENSE_R
Keep trace fat and short!!
CRITICAL R3900 0.001 1% 1W MF-LF 2512
=PPVCORE_CPU_REG 10

CRITICAL C3910 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3912 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3914 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3916 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3918 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	
CRITICAL C3911 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3913 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3915 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF	CRITICAL C3917 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF		

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

VCORE_GNDA
VOLTAGE=0V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

11 =CPU0_MAX1717_AB_SEL
36 =PP3V3_PWRON_CPUVCORE_VID
NO STUFF R3988 0 5% 1/16W MF-LF 402
<D0>
MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

36 VCORE_VID<0>
36 VCORE_VID<1>
36 VCORE_VID<2>
36 VCORE_VID<3>
36 VCORE_VID<4>

Q16BST&Q41 R3989 0 5% 1/16W MF-LF 402

C3964 0.01UF 10% 16V CERM 402
R3964 66.5K 1% 1/16W MF-LF 402
R3963 12.7K 1% 1/16W MF-LF 402
C3962 1UF 20% 10V CERM 603
C3963 220PF 5% 25V CERM 402

VCORE_OFFSET_SW
R3943 100K 5% 1/16W MF-LF 402
10 =PP3V3_PWRON_CPUVCORE_OFFSET
VCORE_SEL_OFF_PU

NO STUFF R3940 0 5% 1/16W MF-LF 402
VCORE_SEL_ON
VCORE_OFFSET_SW
R3941 0 5% 1/16W MF-LF 402
AB_SEL_LOW
NO STUFF R3942 100K 5% 1/16W MF-LF 402

VCORE_OFFSET_SW
Q3940 2N7002DW-X-F SOT-363

OMIT R3944 6.04K 1% 1/16W MF-LF 402
VCORE_OFFSET
R3945 162K 1% 1/16W MF-LF 603 R2
VCORE_GNDDIV 36
OMIT R3946 2.0K 1% 1/16W MF-LF 402 R1

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R3945 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT PIN OF 1008UF CAP CLOSEST TO CPU
XW3901 SM
36 VCORE_GNDSNS VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.15 mm
36 VCORE_SNS VOLTAGE=1.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.15 mm

OUTPUT VOLTAGE

VDAC D4=0	VDAC D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

OMIT R3998 2.05K 1% 1/16W MF-LF 402
36 VCORE_GNDDIV

OMIT R3999 100 1% 1/16W MF-LF 402
36 VCORE_GNDSNS

FMAX CONNECTOR

CRITICAL
OMIT J3999 M-ST-SM-52465-1217

1	VCORE_GNDDIV_TEST	12	VCORE_VID<0>
2	VCORE_GNDSNS_TEST	11	VCORE_VID<1> 36
3	SYS_RESET_BUTTON_L 25	10	VCORE_VID<2> 36
4	SYS_POWER_BUTTON_L 24	9	VCORE_VID<3> 36
5	NC (RFU)	8	VCORE_VID<4> 36
6		7	

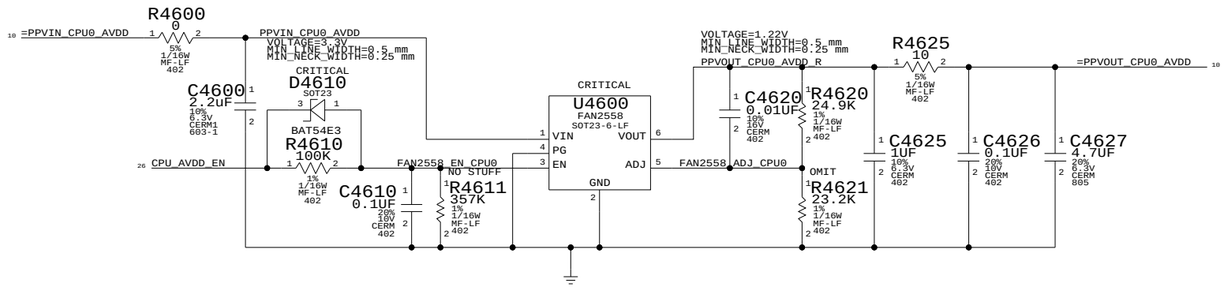
CPU VCore Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 39 OF 115	

CPU PLL POWER SUPPLY



AVDD=0.59*(1+R4620/R4621)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0349	1	RES,23.2K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V22
114S0346	1	RES,21.5K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V28
114S0344	1	RES,20.5K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V30
114S0342	1	RES,19.6K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V33

CPU AVDD Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT OF
NONE	46 OF 115

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_P_R 38 39
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_N_R 38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_P_R 38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_N_R 38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_P_R 38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_N_R 38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_P_R 38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_N_R 38 39
RAM_CKE_0	RAM	RAM		RAM_CKE_R<1..0> 38 39
RAM_CKE_1	RAM	RAM		RAM_CKE_R<3..2> 38 39
RAM_CS_0	RAM	RAM		RAM_CS_L_R<1..0> 38 39
RAM_CS_1	RAM	RAM		RAM_CS_L_R<3..2> 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_ADDR_R<13..0> 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_BA_R<2..0> 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_RAS_L_R 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_CAS_L_R 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_WE_L_R 38 39
RAM_ODT0	RAM	RAM		RAM_ODT_R<0> 38 39
RAM_ODT1	RAM	RAM		RAM_ODT_R<1> 38 39
RAM_DQS0	RAM	RAM		RAM_DQS_P_R<0> 38 39
RAM_DQS1	RAM	RAM		RAM_DQS_P_R<1> 38 39
RAM_DQS2	RAM	RAM		RAM_DQS_P_R<2> 38 39
RAM_DQS3	RAM	RAM		RAM_DQS_P_R<3> 38 39
RAM_DQS4	RAM	RAM		RAM_DQS_P_R<4> 38 39
RAM_DQS5	RAM	RAM		RAM_DQS_P_R<5> 38 39
RAM_DQS6	RAM	RAM		RAM_DQS_P_R<6> 38 39
RAM_DQS7	RAM	RAM		RAM_DQS_P_R<7> 38 39
RAM_DQM0	RAM	RAM		RAM_DQM_R<0> 38 39
RAM_DQM1	RAM	RAM		RAM_DQM_R<1> 38 39
RAM_DQM2	RAM	RAM		RAM_DQM_R<2> 38 39
RAM_DQM3	RAM	RAM		RAM_DQM_R<3> 38 39
RAM_DQM4	RAM	RAM		RAM_DQM_R<4> 38 39
RAM_DQM5	RAM	RAM		RAM_DQM_R<5> 38 39
RAM_DQM6	RAM	RAM		RAM_DQM_R<6> 38 39
RAM_DQM7	RAM	RAM		RAM_DQM_R<7> 38 39
RAM_DATA_0	RAM	RAM		RAM_DATA_R<7..0> 38 39
RAM_DATA_1	RAM	RAM		RAM_DATA_R<15..8> 38 39
RAM_DATA_2	RAM	RAM		RAM_DATA_R<23..16> 38 39
RAM_DATA_3	RAM	RAM		RAM_DATA_R<31..24> 38 39
RAM_DATA_4	RAM	RAM		RAM_DATA_R<39..32> 38 39
RAM_DATA_5	RAM	RAM		RAM_DATA_R<47..40> 38 39
RAM_DATA_6	RAM	RAM		RAM_DATA_R<55..48> 38 39
RAM_DATA_7	RAM	RAM		RAM_DATA_R<63..56> 38 39

Page Notes

Power aliases required by this page:
- =PP1V8_PWRON_I2_RAM
- =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

39 38 RAM_DATA_R<63..0>

OMIT
U2100
I2
BGA
MEMORY INTERFACE
(7 of 14)

AK31	DDR_D_00_H	DDR_A_00_H	R33
AK32	DDR_D_01_H	DDR_A_01_H	R34
AL33	DDR_D_02_H	DDR_A_02_H	R35
AH31	DDR_D_03_H	DDR_A_03_H	T32
AK34	DDR_D_04_H	DDR_A_04_H	R36
AK33	DDR_D_05_H	DDR_A_05_H	T33
AK35	DDR_D_06_H	DDR_A_06_H	T34
AK36	DDR_D_07_H	DDR_A_07_H	T36
AF36	DDR_D_08_H	DDR_A_08_H	T35
AG36	DDR_D_09_H	DDR_A_09_H	U36
AG35	DDR_D_10_H	DDR_A_10_H	P36
AG34	DDR_D_11_H	DDR_A_11_H	V32
AG33	DDR_D_12_H	DDR_A_12_H	V33
AH36	DDR_D_13_H	DDR_A_13_H	N32
AH35	DDR_D_14_H	DDR_BA_0_H	N36
AH34	DDR_D_15_H	DDR_BA_1_H	R32
AE33	DDR_D_16_H	DDR_BA_2_H	V34
AE34	DDR_D_17_H		
AE35	DDR_D_18_H	DDR_CS_0_L	AM36
AD33	DDR_D_19_H	DDR_CS_1_L	AL31
AE36	DDR_D_20_H	DDR_CS_2_L	AL35
AD34	DDR_D_21_H	DDR_CS_3_L	AL32
AD35	DDR_D_22_H		
AD36	DDR_D_23_H	DDR_DQS_0_L	AH30
Y36	DDR_D_24_H	DDR_DQS_1_L	AG32
AA36	DDR_D_25_H	DDR_DQS_2_L	AD32
AA35	DDR_D_26_H	DDR_DQS_3_L	AB33
AA34	DDR_D_27_H	DDR_DQS_4_L	M29
AA33	DDR_D_28_H	DDR_DQS_5_L	J32
AA32	DDR_D_29_H	DDR_DQS_6_L	G35
AB36	DDR_D_30_H	DDR_DQS_7_L	E31
AB34	DDR_D_31_H		
M36	DDR_D_32_H	DDR_DM_0_L	AJ36
M35	DDR_D_33_H	DDR_DM_1_L	AH33
M34	DDR_D_34_H	DDR_DM_2_L	AE32
M33	DDR_D_35_H	DDR_DM_3_L	AB35
M32	DDR_D_36_H	DDR_DM_4_L	N28
L36	DDR_D_37_H	DDR_DM_5_L	K35
M31	DDR_D_38_H	DDR_DM_6_L	F32
M30	DDR_D_39_H	DDR_DM_7_L	C36
K32	DDR_D_40_H		
H36	DDR_D_41_H	DDR_RAS_L	N35
J36	DDR_D_42_H	DDR_CAS_L	N33
J33	DDR_D_43_H	DDR_WE_L	N34
J34	DDR_D_44_H		
J35	DDR_D_45_H	DDR_CKE_0_L	AN35
K33	DDR_D_46_H	DDR_CKE_1_L	AL36
K34	DDR_D_47_H	DDR_CKE_2_L	AP36
G34	DDR_D_48_H	DDR_CKE_3_L	AL34
F36	DDR_D_49_H		
F35	DDR_D_50_H	ODT0	J31
G33	DDR_D_51_H	ODT1	AB30
F34	DDR_D_52_H		
G32	DDR_D_53_H	DDR_MCLK_0_P	W31
E36	DDR_D_54_H	DDR_MCLK_0_N	W30
F33	DDR_D_55_H		
A32	DDR_D_56_H	DDR_MCLK_1_P	V36
A34	DDR_D_57_H	DDR_MCLK_1_N	V35
F30	DDR_D_58_H		
B33	DDR_D_59_H	DDR_MCLK_2_P	W29
C33	DDR_D_60_H	DDR_MCLK_2_N	W28
D33	DDR_D_61_H		
D34	DDR_D_62_H	DDR_MCLK_3_P	W35
D35	DDR_D_63_H	DDR_MCLK_3_N	W34

RAM_ADDR_R<13..0> OUT 38 39
RAM_BA_R<2..0> OUT 38 39
RAM_CS_L_R<3..0> OUT 38 39
RAM_DQS_P_R<7..0> BI 38 39
RAM_DQM_R<7..0> OUT 38 39
RAM_RAS_L_R OUT 38 39
RAM_CAS_L_R OUT 38 39
RAM_WE_L_R OUT 38 39
RAM_CKE_R<3..0> OUT 38 39
RAM_ODT_R<0> OUT 38 39
RAM_ODT_R<1> OUT 38 39
RAM_CLKDDR_0_P_R OUT 38 39
RAM_CLKDDR_0_N_R OUT 38 39
RAM_CLKDDR_1_P_R OUT 38 39
RAM_CLKDDR_1_N_R OUT 38 39
RAM_CLKDDR_2_P_R OUT 38 39
RAM_CLKDDR_2_N_R OUT 38 39
RAM_CLKDDR_3_P_R OUT 38 39
RAM_CLKDDR_3_N_R OUT 38 39

10 =PP1V8_RAM_I2_VREF

R4700 1K 1% 1/16W MF-LF 402
R4701 1K 1% 1/16W MF-LF 402
C4705 0.1UF 20% 10V CERM 402 U2100.AG28
C4706 0.1UF 20% 10V CERM 402 U2100.V21

I2_MEM_VREF
I2_SD_REF
R4710 1K 1% 1/16W MF-LF 402

AG28	DDR_VREF_0_H
Y21	DDR_VREF_1_H
V21	DDR_VREF_2_H
T21	DDR_VREF_3_H
AC22	SD_REF_H

DDR2 I/O DECOUPLING

(40 Balls on I2)

10 =PP1V8_PWRON_I2_RAM

C4749 10UF 20% 6.3V X5R 603

1 X 10uF (0603)
40 X 1uF (0402)

C4750 C4751 C4752 C4753 C4754
C4755 C4756 C4757 C4758 C4759
C4760 C4761 C4762 C4763 C4764
C4765 C4766 C4767 C4768 C4769
C4770 C4771 C4772 C4773 C4774
C4775 C4776 C4777 C4778 C4779
C4780 C4781 C4782 C4783 C4784
C4785 C4786 C4787 C4788 C4789
C4790 C4791 C4792 C4793 C4794
C4795 C4796 C4797

1uF 10% 6.3V CERM 402

OMIT
U2100
I2
BGA
DDR2 POWER
(8 of 14)

AA24	VTT18_0
AA26	VTT18_1
AA28	VTT18_2
AB26	VTT18_3
AC24	VTT18_4
AC27	VTT18_5
AC28	VTT18_6
AC31	VTT18_7
AC34	VTT18_8
AD24	VTT18_9
AD28	VTT18_10
AF28	VTT18_11
AF31	VTT18_12
AF34	VTT18_13
AJ31	VTT18_14
AJ34	VTT18_15
AM34	VTT18_16
AP34	VTT18_17
C34	VTT18_18
E34	VTT18_19
H31	VTT18_20
H34	VTT18_21
K28	VTT18_22
L28	VTT18_23
L31	VTT18_24
L34	VTT18_25
M25	VTT18_26
N26	VTT18_27
P28	VTT18_28
P31	VTT18_29
P34	VTT18_30
R24	VTT18_31
R26	VTT18_32
R28	VTT18_33
T25	VTT18_34
U24	VTT18_35
U27	VTT18_36
U29	VTT18_37
U31	VTT18_38
U34	VTT18_39
V25	VTT18_40
V26	VTT18_41
V29	VTT18_42
W24	VTT18_43
Y25	VTT18_44
Y28	VTT18_45
Y31	VTT18_46
Y34	VTT18_47

I2 Memory Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 47 OF 115	

Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

RAM_ADDR_R<0> — RP4800 pin 3 — 22 — 5% 1/16W SM-LF — RP4800 pin 6 — RAM_ADDR<0>
RAM_ADDR_R<1> — RP4803 pin 2 — 22 — 5% 1/16W SM-LF — RP4803 pin 7 — RAM_ADDR<1>
RAM_ADDR_R<2> — RP4803 pin 4 — 22 — 5% 1/16W SM-LF — RP4803 pin 5 — RAM_ADDR<2>
RAM_ADDR_R<3> — RP4803 pin 1 — 22 — 5% 1/16W SM-LF — RP4803 pin 8 — RAM_ADDR<3>
RAM_ADDR_R<4> — RP4803 pin 3 — 22 — 5% 1/16W SM-LF — RP4803 pin 6 — RAM_ADDR<4>
RAM_ADDR_R<5> — RP4801 pin 4 — 22 — 5% 1/16W SM-LF — RP4801 pin 5 — RAM_ADDR<5>
RAM_ADDR_R<6> — RP4802 pin 1 — 22 — 5% 1/16W SM-LF — RP4802 pin 8 — RAM_ADDR<6>
RAM_ADDR_R<7> — RP4802 pin 4 — 22 — 5% 1/16W SM-LF — RP4802 pin 5 — RAM_ADDR<7>
RAM_ADDR_R<8> — RP4802 pin 3 — 22 — 5% 1/16W SM-LF — RP4802 pin 6 — RAM_ADDR<8>
RAM_ADDR_R<9> — RP4802 pin 2 — 22 — 5% 1/16W SM-LF — RP4802 pin 7 — RAM_ADDR<9>
RAM_ADDR_R<10> — RP4800 pin 2 — 22 — 5% 1/16W SM-LF — RP4800 pin 7 — RAM_ADDR<10>
RAM_ADDR_R<11> — RP4801 pin 3 — 22 — 5% 1/16W SM-LF — RP4801 pin 6 — RAM_ADDR<11>
RAM_ADDR_R<12> — RP4801 pin 2 — 22 — 5% 1/16W SM-LF — RP4801 pin 7 — RAM_ADDR<12>
RAM_ADDR_R<13> — RP4804 pin 4 — 22 — 5% 1/16W SM-LF — RP4804 pin 5 — RAM_ADDR<13>

RAM_BA_R<0> — RP4800 pin 1 — 22 — 5% 1/16W SM-LF — RP4800 pin 8 — RAM_BA<0>
RAM_BA_R<1> — RP4800 pin 4 — 22 — 5% 1/16W SM-LF — RP4800 pin 5 — RAM_BA<1>
RAM_BA_R<2> — RP4801 pin 1 — 22 — 5% 1/16W SM-LF — RP4801 pin 8 — RAM_BA<2>

RAM_RAS_L_R — RP4804 pin 1 — 22 — 5% 1/16W SM-LF — RP4804 pin 8 — RAM_RAS_L
RAM_CAS_L_R — RP4804 pin 3 — 22 — 5% 1/16W SM-LF — RP4804 pin 6 — RAM_CAS_L
RAM_WE_L_R — RP4804 pin 2 — 22 — 5% 1/16W SM-LF — RP4804 pin 7 — RAM_WE_L

RAM_ODT_R<0> — R4810 — 0 — 5% 1/16W MF-LF 402 — RAM_ODT<0>
RAM_ODT_R<1> — R4811 — 0 — 5% 1/16W MF-LF 402 — RAM_ODT<1>

SERIES RESISTORS FOR CLOCKS

RAM_CLKDDR_0_P_R — R4850 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_0_P
RAM_CLKDDR_0_N_R — R4851 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_0_N
RAM_CLKDDR_1_P_R — R4855 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_1_P
RAM_CLKDDR_1_N_R — R4856 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_1_N
RAM_CLKDDR_2_P_R — R4860 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_2_P
RAM_CLKDDR_2_N_R — R4861 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_2_N
RAM_CLKDDR_3_P_R — R4865 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_3_P
RAM_CLKDDR_3_N_R — R4866 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_3_N

SERIES RESISTORS FOR CS / CKE
Do not swap with other RPAKs

RAM_CS_L_R<0> — RP4870 pin 1 — 22 — 5% 1/16W SM-LF — RP4870 pin 4 — RAM_CS_L<0>
RAM_CS_L_R<2> — RP4870 pin 2 — 22 — 5% 1/16W SM-LF — RP4870 pin 3 — RAM_CS_L<2>
RAM_CS_L_R<1> — RP4871 pin 1 — 22 — 5% 1/16W SM-LF — RP4871 pin 4 — RAM_CS_L<1>
RAM_CS_L_R<3> — RP4871 pin 2 — 22 — 5% 1/16W SM-LF — RP4871 pin 3 — RAM_CS_L<3>
RAM_CKE_R<0> — RP4875 pin 1 — 22 — 5% 1/16W SM-LF — RP4875 pin 4 — RAM_CKE<0>
RAM_CKE_R<2> — RP4875 pin 2 — 22 — 5% 1/16W SM-LF — RP4875 pin 3 — RAM_CKE<2>
RAM_CKE_R<1> — RP4876 pin 1 — 22 — 5% 1/16W SM-LF — RP4876 pin 4 — RAM_CKE<1>
RAM_CKE_R<3> — RP4876 pin 2 — 22 — 5% 1/16W SM-LF — RP4876 pin 3 — RAM_CKE<3>

RAM_DATA_R<63..0> — RAM_DATA<63..0> MAKE_BASE=TRUE — RAM_DATA_A<63..0> / RAM_DATA_B<63..0>
RAM_DQM_R<7..0> — RAM_DQM<7..0> MAKE_BASE=TRUE — RAM_DQM_A<7..0> / RAM_DQM_B<7..0>
RAM_DQS_P_R<7..0> — RAM_DQS<7..0> MAKE_BASE=TRUE — RAM_DQS_A_P<7..0> / RAM_DQS_B_P<7..0>

RP4872: 10K 5% 1/16W SM-LF
RAM_DQS_A_N<0> — RAM_DQS_A_N<1> — RAM_DQS_A_N<2> — RAM_DQS_A_N<3>
RP4873: 10K 5% 1/16W SM-LF
RAM_DQS_A_N<4> — RAM_DQS_A_N<5> — RAM_DQS_A_N<6> — RAM_DQS_A_N<7>

RP4877: 10K 5% 1/16W SM-LF
RAM_DQS_B_N<0> — RAM_DQS_B_N<1> — RAM_DQS_B_N<2> — RAM_DQS_B_N<3>
RP4878: 10K 5% 1/16W SM-LF
RAM_DQS_B_N<4> — RAM_DQS_B_N<5> — RAM_DQS_B_N<6> — RAM_DQS_B_N<7>

ECSETs provided by memory controller.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
T190	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P
T194	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N
T195	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P
T193	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N
T197	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P
T199	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N
T198	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P
T200	RAM_DIFF	RAM_DIFF	RAM_CLK_4	RAM_CLKDDR_3_N
T205	RAM	RAM		RAM_CKE<3..0>
T204	RAM	RAM		RAM_CS_L<3..0>
T203	RAM	RAM		RAM_ADDR<13..0>
T202	RAM	RAM		RAM_BA<2..0>
T201	RAM	RAM		RAM_RAS_L
T208	RAM	RAM		RAM_CAS_L
T207	RAM	RAM		RAM_WE_L
T259	RAM	RAM		RAM_ODT<1..0>
T209	RAM	RAM		RAM_DQS<7..0>
T206	RAM	RAM		RAM_DQM<7..0>
T210	RAM	RAM		RAM_DATA<63..0>

Memory Series Termination

SYNC_MASTER=MARIAS-NDIFF SYNC_DATE=N/A

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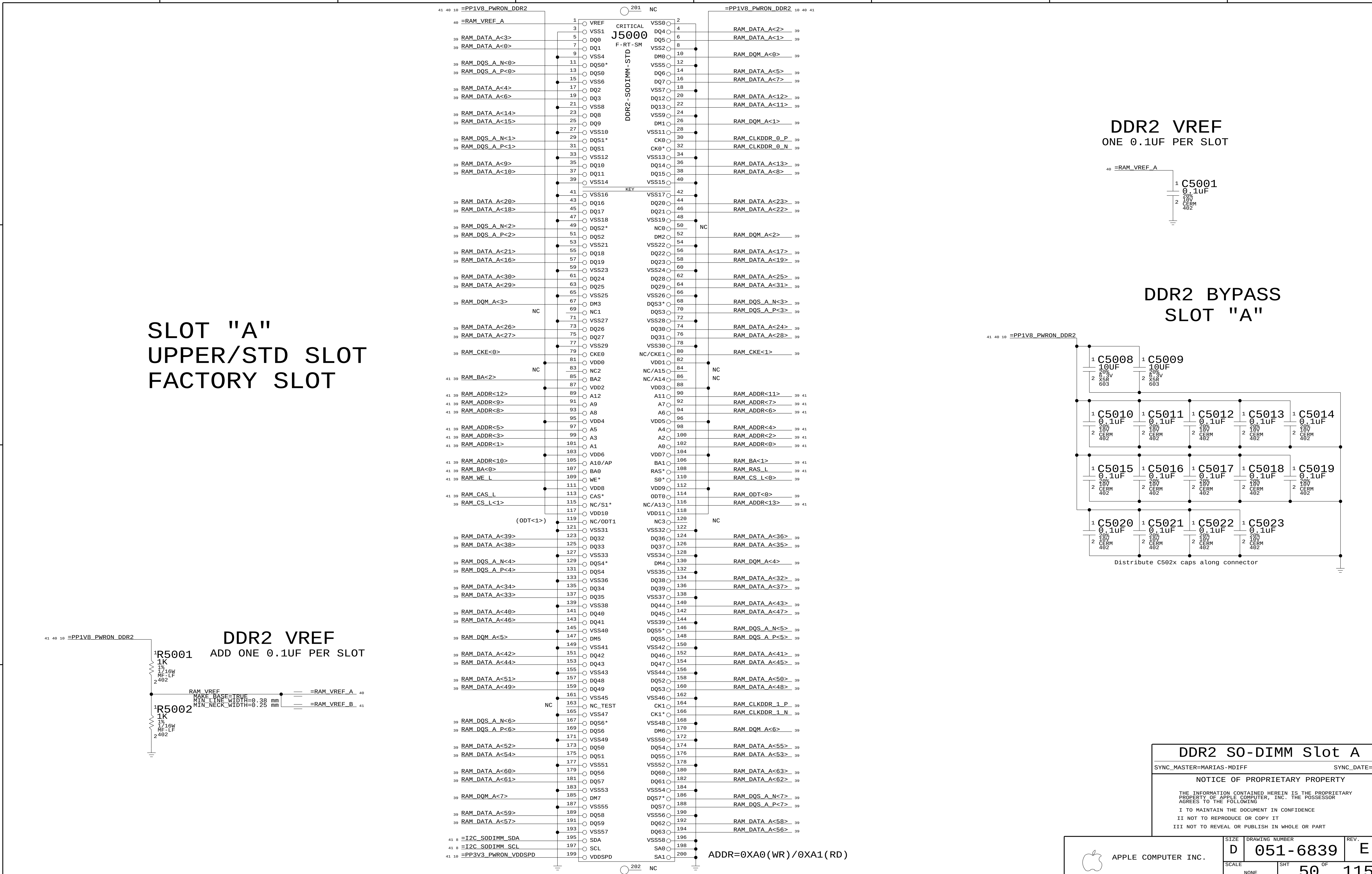
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 48 OF 115	



DDR2 SO-DIMM Slot A

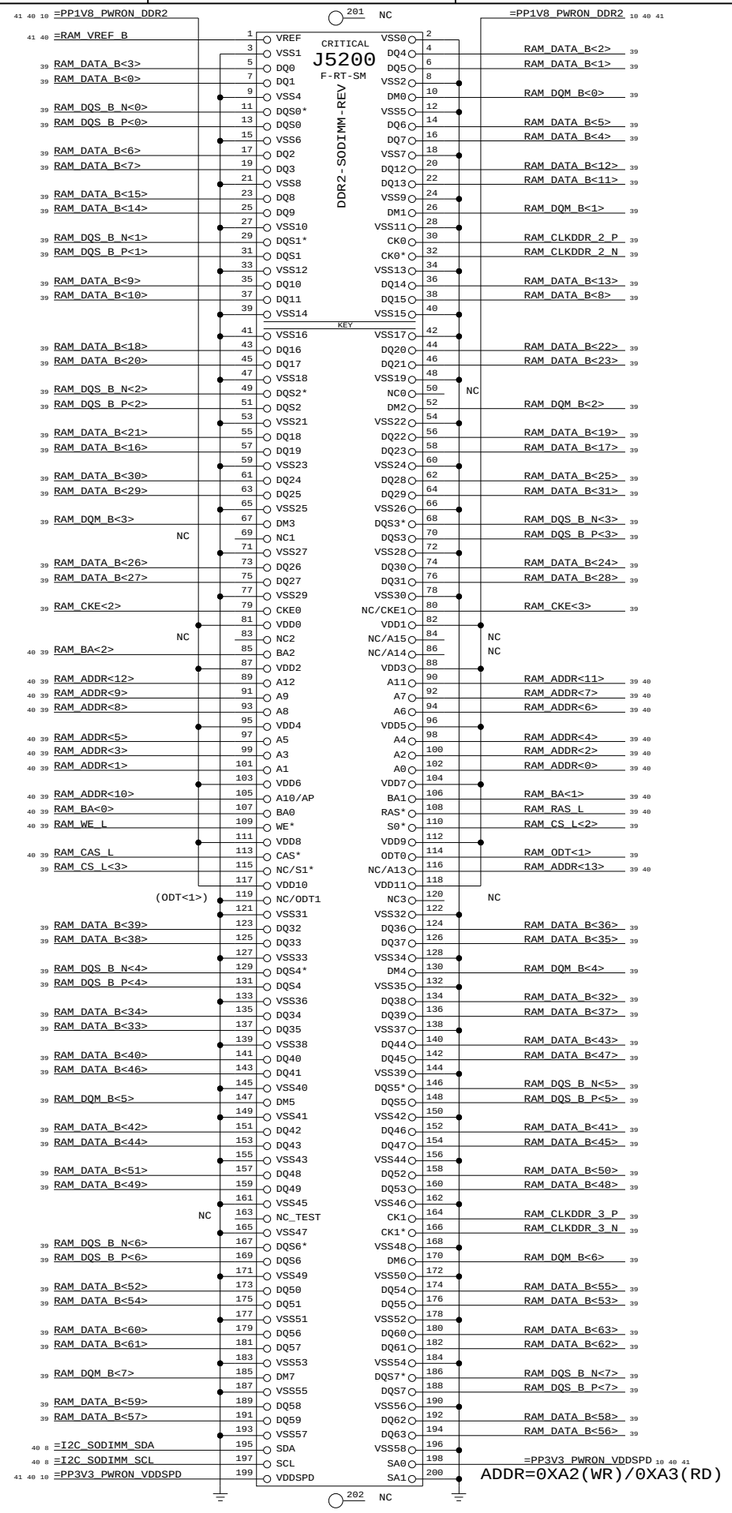
SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

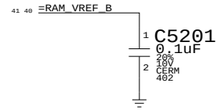
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 50 OF 115	

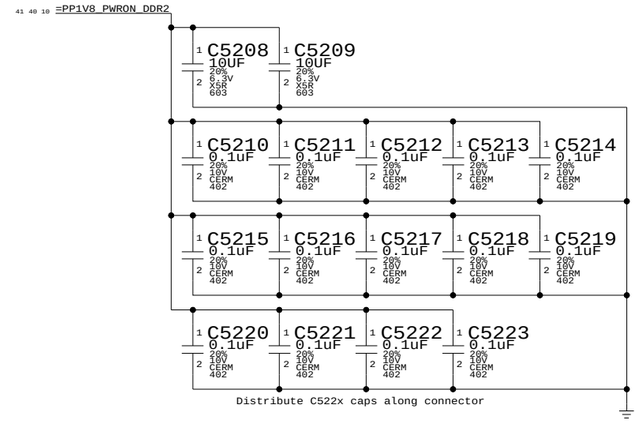
SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT



DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "B"



Distribute C522x caps along connector

DDR2 SO-DIMM Slot B

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 52 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_N_R 48
FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_N_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CKE_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CS_L_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_ADDR_R<12..0> 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_BA_R<2..0> 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_RAS_L_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CAS_L_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_WE_L_R 48
FB_A_DQS0	RAM	RAM		FB_A_DQS_R<0> 48
FB_A_DQS1	RAM	RAM		FB_A_DQS_R<1> 48
FB_A_DQS2	RAM	RAM		FB_A_DQS_R<2> 48
FB_A_DQS3	RAM	RAM		FB_A_DQS_R<3> 48
FB_A_DQS4	RAM	RAM		FB_A_DQS_R<4> 48
FB_A_DQS5	RAM	RAM		FB_A_DQS_R<5> 48
FB_A_DQS6	RAM	RAM		FB_A_DQS_R<6> 48
FB_A_DQS7	RAM	RAM		FB_A_DQS_R<7> 48
FB_A_DQM0	RAM	RAM		FB_A_DQM_R<0> 48
FB_A_DQM1	RAM	RAM		FB_A_DQM_R<1> 48
FB_A_DQM2	RAM	RAM		FB_A_DQM_R<2> 48
FB_A_DQM3	RAM	RAM		FB_A_DQM_R<3> 48
FB_A_DQM4	RAM	RAM		FB_A_DQM_R<4> 48
FB_A_DQM5	RAM	RAM		FB_A_DQM_R<5> 48
FB_A_DQM6	RAM	RAM		FB_A_DQM_R<6> 48
FB_A_DQM7	RAM	RAM		FB_A_DQM_R<7> 48
FB_A_DQ0	RAM	RAM		FB_A_DQ_R<7..0> 48
FB_A_DQ1	RAM	RAM		FB_A_DQ_R<15..8> 48
FB_A_DQ2	RAM	RAM		FB_A_DQ_R<23..16> 48
FB_A_DQ3	RAM	RAM		FB_A_DQ_R<31..24> 48
FB_A_DQ4	RAM	RAM		FB_A_DQ_R<39..32> 48
FB_A_DQ5	RAM	RAM		FB_A_DQ_R<47..40> 48
FB_A_DQ6	RAM	RAM		FB_A_DQ_R<55..48> 48
FB_A_DQ7	RAM	RAM		FB_A_DQ_R<63..56> 48

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_N_R 48
FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_N_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CKE_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CS_L_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_ADDR_R<12..0> 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_BA_R<2..0> 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_RAS_L_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CAS_L_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_WE_L_R 48
FB_B_DQS0	RAM	RAM		FB_B_DQS_R<0> 48
FB_B_DQS1	RAM	RAM		FB_B_DQS_R<1> 48
FB_B_DQS2	RAM	RAM		FB_B_DQS_R<2> 48
FB_B_DQS3	RAM	RAM		FB_B_DQS_R<3> 48
FB_B_DQS4	RAM	RAM		FB_B_DQS_R<4> 48
FB_B_DQS5	RAM	RAM		FB_B_DQS_R<5> 48
FB_B_DQS6	RAM	RAM		FB_B_DQS_R<6> 48
FB_B_DQS7	RAM	RAM		FB_B_DQS_R<7> 48
FB_B_DQM0	RAM	RAM		FB_B_DQM_R<0> 48
FB_B_DQM1	RAM	RAM		FB_B_DQM_R<1> 48
FB_B_DQM2	RAM	RAM		FB_B_DQM_R<2> 48
FB_B_DQM3	RAM	RAM		FB_B_DQM_R<3> 48
FB_B_DQM4	RAM	RAM		FB_B_DQM_R<4> 48
FB_B_DQM5	RAM	RAM		FB_B_DQM_R<5> 48
FB_B_DQM6	RAM	RAM		FB_B_DQM_R<6> 48
FB_B_DQM7	RAM	RAM		FB_B_DQM_R<7> 48
FB_B_DQ0	RAM	RAM		FB_B_DQ_R<7..0> 48
FB_B_DQ1	RAM	RAM		FB_B_DQ_R<15..8> 48
FB_B_DQ2	RAM	RAM		FB_B_DQ_R<23..16> 48
FB_B_DQ3	RAM	RAM		FB_B_DQ_R<31..24> 48
FB_B_DQ4	RAM	RAM		FB_B_DQ_R<39..32> 48
FB_B_DQ5	RAM	RAM		FB_B_DQ_R<47..40> 48
FB_B_DQ6	RAM	RAM		FB_B_DQ_R<55..48> 48
FB_B_DQ7	RAM	RAM		FB_B_DQ_R<63..56> 48

M11 Frame Buffer Constraints

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE NONE SHT 55 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
AGP_CLK	CLOCK	CLOCK	
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK	
I2_FBCLK	I2_FBCLK	I2_FBCLK	
AGP_AD_0	AGP	AGP	
AGP_AD_1	AGP	AGP	
AGP_AD_0	AGP	AGP	
AGP_AD_1	AGP	AGP	
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1
AGP_SBA	AGP	AGP	
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB
AGP_ST	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_PAR	AGP	AGP	
AGP_DEV_CTL	AGP	AGP	
AGP_DEV_CTL	AGP	AGP	
AGP_DEV_CTL	AGP	AGP	
	AGP	AGP	
	AGP	AGP	

AGP_CLK66M_GPU_R 11 43
I2_AGP_FBCLK_OUT_R 43
I2_AGP_FBCLK_OUT 21 43
AGP_AD<15..0> 43 44
AGP_AD<31..16> 43 44
AGP_CBE_L<1..0> 43 44
AGP_CBE_L<3..2> 43 44
AGP_AD_STB0_P 43 44
AGP_AD_STB0_N 43 44
AGP_AD_STB1_P 43 44
AGP_AD_STB1_N 43 44
AGP_SBA<7..0> 43 44
AGP_SB_STB_P 43 44
AGP_SB_STB_N 43 44
AGP_ST<3..0> 43 44
AGP_FRAME_L 6 43 44
AGP_DEVSEL_L 6 43 44
AGP_IRDY_L 6 43 44
AGP_TRDY_L 6 43 44
AGP_STOP_L 6 43 44
AGP_PAR 43 44
AGP_PIPE_L 43
AGP_WBF_L 43 44
AGP_RBF_L 6 43 44
AGP_REQ_L 6 43 44
AGP_GNT_L 6 43 44

Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP
- =PP1V5_I2_AGP

Signal aliases required by this page:
- =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
- =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
(NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

AGP I/O DECOUPLING

(25 Balls on I2)

10 =PP1V5_I2_AGP

C5649 10UF 20% 6.3V XSR 603

C5650 C5651 C5652 C5653 C5654 C5655 C5656
C5657 C5658 C5659 C5660 C5661 C5662 C5663
C5664 C5665 C5666 C5667 C5668 C5669 C5670
C5671 C5672 C5673 C5674

1uF 10% 6.3V CERM 402

1 X 10uF (0603)
25 X 1uF (0402)

OMIT
U2100
I2
BGA
AGP INTERFACE
(9 of 14)

(3.3V SIGNALS)

(VDDAGP SIGNALS)

44 43 AGP_BUSY_L	AP19	AGP_BUSY_L	AGP_CLK_H	AH19	AGP_CLK66M_GPU_R 11 43
44 43 6 AGP_REQ_L	AR19	AGP_REQ_L	AGP_STP_L	AT21	STOP_AGP_L 43 44
			AGP_GNT_L	AL16	AGP_GNT_L 6 43 44
44 43 AGP_PAR	AT15	AGP_PAR_H	AGP_AD_00_H	AP6	AGP_AD<0> 43 44
44 43 6 AGP_FRAME_L	AK16	AGP_FRAME_L	AGP_AD_01_H	AP4	AGP_AD<1> 43 44
44 43 6 AGP_TRDY_L	AM16	AGP_TRDY_L	AGP_AD_02_H	AR4	AGP_AD<2> 43 44
44 43 6 AGP_IRDY_L	AR15	AGP_IRDY_L	AGP_AD_03_H	AT5	AGP_AD<3> 43 44
44 43 6 AGP_STOP_L	AT14	AGP_STOP_L	AGP_AD_04_H	AN7	AGP_AD<4> 43 44
44 43 6 AGP_DEVSEL_L	AP15	AGP_DEVSEL_L	AGP_AD_05_H	AL13	AGP_AD<5> 43 44
43 AGP_PIPE_L	AN19	AGP_PIPE_L	AGP_AD_06_H	AR6	AGP_AD<6> 43 44
44 43 AGP_WBF_L	AT18	AGP_WBF_L	AGP_AD_07_H	AT6	AGP_AD<7> 43 44
44 43 6 AGP_RBF_L	AM19	AGP_RBF_L	AGP_CBE_0_L	AT3	AGP_CBE_L<0> 43 44
44 43 AGP_SBA<0>	AL18	AGP_SBA_0_H	AGP_AD_08_H	AN9	AGP_AD<8> 43 44
44 43 AGP_SBA<1>	AR18	AGP_SBA_1_H	AGP_AD_09_H	AP7	AGP_AD<9> 43 44
44 43 AGP_SBA<2>	AP18	AGP_SBA_2_H	AGP_AD_10_H	AR7	AGP_AD<10> 43 44
44 43 AGP_SBA<3>	AN18	AGP_SBA_3_H	AGP_AD_11_H	AT7	AGP_AD<11> 43 44
44 43 AGP_SBA<4>	AM18	AGP_SBA_4_H	AGP_AD_12_H	AN10	AGP_AD<12> 43 44
44 43 AGP_SBA<5>	AK18	AGP_SBA_5_H	AGP_AD_13_H	AR9	AGP_AD<13> 43 44
44 43 AGP_SBA<6>	AT16	AGP_SBA_6_H	AGP_AD_14_H	AT8	AGP_AD<14> 43 44
44 43 AGP_SBA<7>	AT17	AGP_SBA_7_H	AGP_AD_15_H	AT9	AGP_AD<15> 43 44
			AGP_CBE_1_L	AP9	AGP_CBE_L<1> 43 44
44 43 AGP_SB_STB_P	AH16	AGP_SB_STB_P	AGP_AD_STB0_P	AH9	AGP_AD_STB0_P 43 44
44 43 AGP_SB_STB_N	AJ16	AGP_SB_STB_N	AGP_AD_STB0_N	AJ9	AGP_AD_STB0_N 43 44
	AD15	VDDAGP_0	AGP_AD_16_H	AM12	AGP_AD<16> 43 44
	AD17	VDDAGP_1	AGP_AD_17_H	AP10	AGP_AD<17> 43 44
	AD19	VDDAGP_2	AGP_AD_18_H	AN12	AGP_AD<18> 43 44
	AE13	VDDAGP_3	AGP_AD_19_H	AT10	AGP_AD<19> 43 44
	AE16	VDDAGP_4	AGP_AD_20_H	AK15	AGP_AD<20> 43 44
	AE18	VDDAGP_5	AGP_AD_21_H	AM13	AGP_AD<21> 43 44
	AF14	VDDAGP_6	AGP_AD_22_H	AP12	AGP_AD<22> 43 44
	AG13	VDDAGP_7	AGP_AD_23_H	AT11	AGP_AD<23> 43 44
	AG16	VDDAGP_8	AGP_CBE_2_L	AR10	AGP_CBE_L<2> 43 44
	AH11	VDDAGP_9	AGP_AD_24_H	AL15	AGP_AD<24> 43 44
	AH13	VDDAGP_10	AGP_AD_25_H	AN13	AGP_AD<25> 43 44
	AL11	VDDAGP_11	AGP_AD_26_H	AR12	AGP_AD<26> 43 44
	AL12	VDDAGP_12	AGP_AD_27_H	AT12	AGP_AD<27> 43 44
	AL14	VDDAGP_13	AGP_AD_28_H	AR13	AGP_AD<28> 43 44
	AL17	VDDAGP_14	AGP_AD_29_H	AT13	AGP_AD<29> 43 44
	AL20	VDDAGP_15	AGP_AD_30_H	AM15	AGP_AD<30> 43 44
	AL8	VDDAGP_16	AGP_AD_31_H	AN15	AGP_AD<31> 43 44
	AL9	VDDAGP_17	AGP_CBE_3_L	AP13	AGP_CBE_L<3> 43 44
	AP11	VDDAGP_18	AGP_AD_STB1_P	AK13	AGP_AD_STB1_P 43 44
	AP14	VDDAGP_19	AGP_AD_STB1_N	AJ13	AGP_AD_STB1_N 43 44
	AP17	VDDAGP_20	AGP_ST_0_H	AR16	AGP_ST<0> 43 44
	AP20	VDDAGP_21	AGP_ST_1_H	AN16	AGP_ST<1> 43 44
	AP3	VDDAGP_22	AGP_ST_2_H	AP16	AGP_ST<2> 43 44
	AP5	VDDAGP_23			
	AP8	VDDAGP_24			

11 =I2_AGP_VREF → AD18 AGP_VREF_0_H

47 44 43 10 =PP1V5_AGP → R5600 60.4 1% 1/16W MF-LF 402 → I2_AGP_PVTREF → AJ18 AGP_PVTREF_H

21 =I2_AGP_FBCLK_IN → AM10 AGP_FB_CLK_IN_H

AGP_FBCLK_OUT_H AM9 → 43 I2_AGP_FBCLK_OUT_R → R5605 22 5% 1/16W MF-LF 402 → I2_AGP_FBCLK_OUT 21 43

1.5V IN
1.5V OUT

One resistor for each of:
- AGP_RBF_L
- AGP_GNT_L
- AGP_FRAME_L
- AGP_REQ_L
- AGP_STOP_L
- AGP_DEVSEL_L
- AGP_IRDY_L
- AGP_TRDY_L

AGP PULL-UPS/PULL DOWNS

44 10 =PP3V3_AGP

44 43 AGP_BUSY_L	R5610 10K 5% 1/16W MF-LF 402	
44 43 STOP_AGP_L	R5611 10K 5% 1/16W MF-LF 402	
44 22 AGP_INT_L	R5620 10K 5% 1/16W MF-LF 402	

47 44 43 10 =PP1V5_AGP

6 =RP5610P4	RP5610 10K 5% 1/16W SM-LF	
6 =RP5610P2	RP5610 10K 5% 1/16W SM-LF	
6 =RP5610P3	RP5610 10K 5% 1/16W SM-LF	
6 =RP5611P2	RP5611 10K 5% 1/16W SM-LF	
6 =RP5611P3	RP5611 10K 5% 1/16W SM-LF	
6 =RP5611P4	RP5611 10K 5% 1/16W SM-LF	
6 =RP5611P1	RP5611 10K 5% 1/16W SM-LF	
6 =RP5610P1	RP5610 10K 5% 1/16W SM-LF	
44 43 AGP_WBF_L	R5612 10K 5% 1/16W MF-LF 402	
43 AGP_PIPE_L	R5613 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB0_P	R5614 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB1_P	R5615 10K 5% 1/16W MF-LF 402	
44 43 AGP_SB_STB_P	R5616 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB0_N	R5617 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB1_N	R5618 10K 5% 1/16W MF-LF 402	
44 43 AGP_SB_STB_N	R5619 10K 5% 1/16W MF-LF 402	

I2 AGP Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE: SPACING	NET_TYPE: PHYSICAL	NET_TYPE: DIFFERENTIAL_PAIR
I798	CLOCK	CLOCK	AGP_CLK66M_GPU 11 44

Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP

Signal aliases required by this page:
- =AGP_VREF - VRef divider output for both GPU and NB
- =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
(NONE)

NOTE: AGP 8x signals are not provided by this page.

OMIT
CRITICAL

U5700
BGA
M11P
(1 OF 8)

AGP/PCI INTERFACE

43 AGP_AD<0>	H29	AD_0	
43 AGP_AD<1>	H28	AD_1	
43 AGP_AD<2>	J29	AD_2	
43 AGP_AD<3>	J28	AD_3	
43 AGP_AD<4>	K29	AD_4	
43 AGP_AD<5>	K28	AD_5	
43 AGP_AD<6>	L29	AD_6	
43 AGP_AD<7>	L28	AD_7	
43 AGP_AD<8>	N28	AD_8	
43 AGP_AD<9>	P29	AD_9	
43 AGP_AD<10>	P28	AD_10	
43 AGP_AD<11>	R29	AD_11	
43 AGP_AD<12>	R28	AD_12	
43 AGP_AD<13>	T29	AD_13	
43 AGP_AD<14>	T28	AD_14	
43 AGP_AD<15>	U29	AD_15	
43 AGP_AD<16>	N25	AD_16	
43 AGP_AD<17>	R26	AD_17	
43 AGP_AD<18>	P25	AD_18	
43 AGP_AD<19>	R27	AD_19	
43 AGP_AD<20>	R25	AD_20	
43 AGP_AD<21>	T25	AD_21	
43 AGP_AD<22>	T26	AD_22	
43 AGP_AD<23>	U25	AD_23	
43 AGP_AD<24>	V27	AD_24	
43 AGP_AD<25>	W26	AD_25	
43 AGP_AD<26>	W25	AD_26	
43 AGP_AD<27>	Y26	AD_27	
43 AGP_AD<28>	Y25	AD_28	
43 AGP_AD<29>	AA26	AD_29	
43 AGP_AD<30>	AA25	AD_30	
43 AGP_AD<31>	AA27	AD_31	

AGP ONLY

ATI_DBI_HI_PU	AB25	DBI_HI	AGP 8X
ATI_DBI_LO_PU	AB26	DBI_LO	
AGP8X_DET_PU	AC25	AGP8X_DET*	

43 AGP_SBA<0>	AD28	SBA_0	
43 AGP_SBA<1>	AD29	SBA_1	
43 AGP_SBA<2>	AC28	SBA_2	
43 AGP_SBA<3>	AC29	SBA_3	
43 AGP_SBA<4>	AA28	SBA_4	
43 AGP_SBA<5>	AA29	SBA_5	
43 AGP_SBA<6>	Y28	SBA_6	
43 AGP_SBA<7>	Y29	SBA_7	
GPU_AGPTEST	M27	AGPTEST	

PCICLK	AG30	AGP_CLK66M_GPU	11 44
RST*	AG28	AGP_ATI_RESET_L	
INTA*	AE26	AGP_INT_L	22 43
GNT*	AD26	AGP_GNT_L	6 43
REQ*	AF28	AGP_REQ_L	6 43
FRAME*	W28	AGP_FRAME_L	6 43
TRDY*	V28	AGP_TRDY_L	6 43
IRDY*	W29	AGP_IRDY_L	6 43
DEVSEL*	V29	AGP_DEVSEL_L	6 43
STOP*	N26	AGP_STOP_L	6 43
PAR	M25	AGP_PAR	43
C_BE_0*	N29	AGP_CBE_L<0>	43
C_BE_1*	U28	AGP_CBE_L<1>	43
C_BE_2*	P26	AGP_CBE_L<2>	43
C_BE_3*	U26	AGP_CBE_L<3>	43
RBF*	AE29	AGP_RBF_L	6 43
WBF*	AC26	AGP_WBF_L	43
ST_0	AF29	AGP_ST<0>	43
ST_1	AD27	AGP_ST<1>	43
ST_2	AE28	AGP_ST<2>	43
SB_STBF	AB29	AGP_SB_STB_P	43
SB_STBS	AB28	AGP_SB_STB_N	43
AD_STBF_0	M28	AGP_AD_STB0_P	43
AD_STBS_0	M29	AGP_AD_STB0_N	43
AD_STBF_1	V25	AGP_AD_STB1_P	43
AD_STBS_1	V26	AGP_AD_STB1_N	43
AGPREF	M26	=GPU_AGP_VREF	11
STP_AGP*	AH30	STOP_AGP_L	43
AGP_BUSY*	AH29	AGP_BUSY_L	43
SUS_STAT*	AG26	AGP_SUS_STAT_L_PU	

R5700
47
5%
1/16W
MF-LF
402
11 =AGP_GPU_RESET_L

47 44 43 10 =PP3V3_AGP
R5720 10K 5% 1/10W MF-LF 402
47 44 43 10 =PP1V5_AGP
R5725 47K 5% 1/16W MF-LF 402
R5726 47K 5% 1/16W MF-LF 402

47 44 43 10 =PP1V5_AGP
R5721 47 1% 1/10W MF-LF 402

44 43 10 =PP3V3_AGP
R5722 20K 5% 1/10W MF-LF 402

47 44 43 10 =PP1V5_AGP
CONNECT TO GPU AGP REF
CAN ALSO CONNECT TO NB IF CHIPS ARE CO-LOCATED
R5730 1K 1% 1/10W MF-LF 402
11 =AGP_VREF
C5732 0.1uF 10% 16V X5R 402
C5731 0.1uF 10% 16V X5R 402
R5731 1K 1% 1/10W MF-LF 402
PLACE C5731 AT GPU
PLACE C5732 AT NB
PLACE RESISTORS MIDWAY BETWEEN

GPU (M11) AGP Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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Page Notes

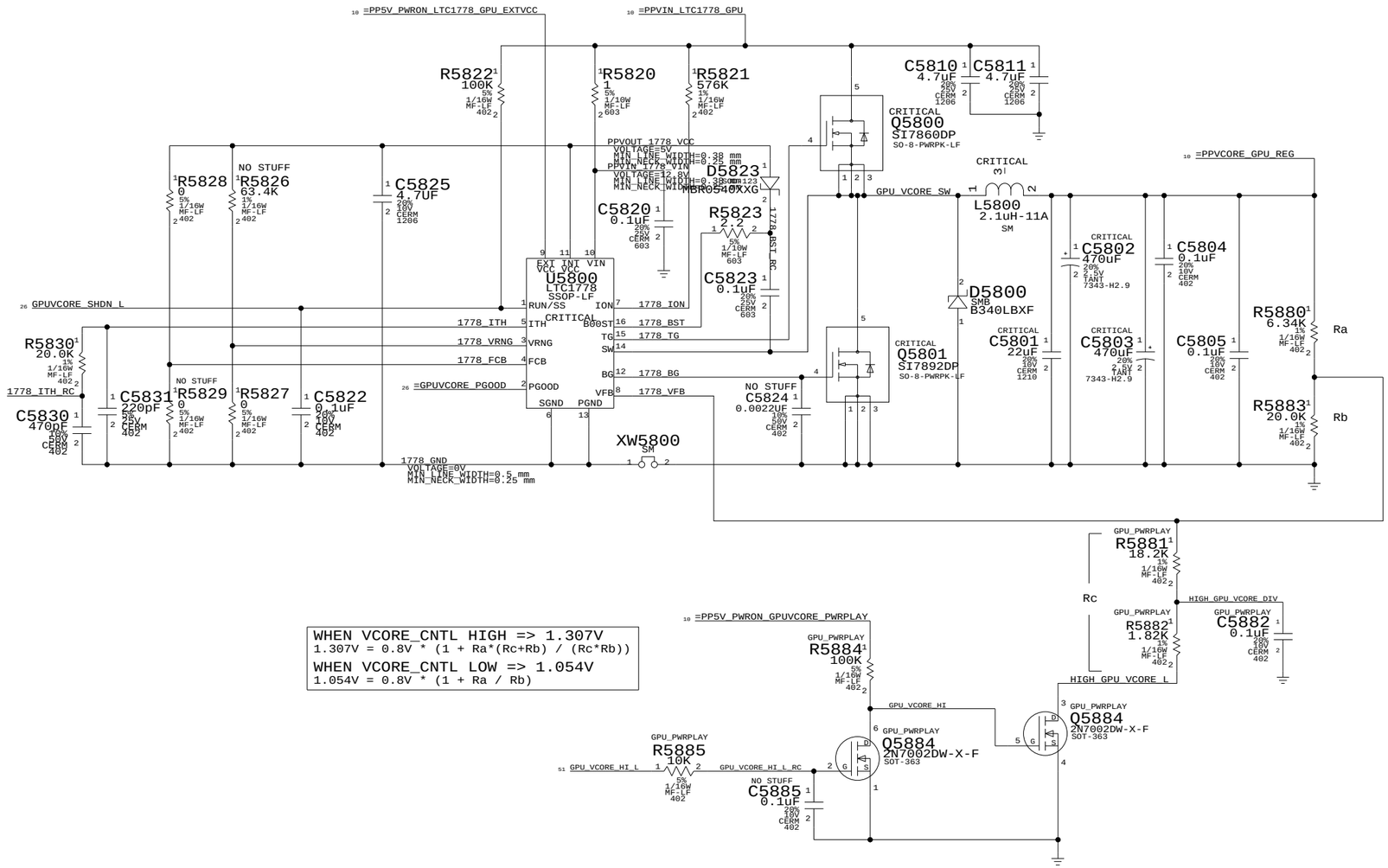
Power aliases required by this page:
- =PPVIN_LTC1778_GPU
- =PP5V_PWRON_LTC1778_GPU_EXTVCC
- =PPVCORE_GPU_REG

Signal aliases required by this page:
- =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

BOM options provided by this page:
- GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCORE SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))
WHEN VCORE_CNTL LOW => 1.054V
1.054V = 0.8V * (1 + Ra / Rb)

GPU VCore Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
CRITICAL
U5700
M11P
BGA
(6 OF 8)

HOST GROUND

CORE GND

I/O GROUND

VSS

H23 H27 H4 H8 H9 K1 K23 K24 K27 K30 K7 K8 L4 M16 M30 M7 M8 N15 N16 N23 N24 N27 P15 P16 P4 R12 R13 R14 R15 R16 R17 R18 R23 R24 R30 R7 R8 T1 T13 T14 T15 T16 T17 T18 T19 T27 U15 U16 U23 U4 U8 V15 V16 V30 W15 W23 W24 W27 W7 W8 Y4

A10 A16 A2 A22 A29 AA30 AB1 AB23 AB24 AB27 AB4 AB7 AB8 AC12 AC14 AC16 AC18 AC4 AD12 AD16 AD18 AD25 AD30 AE27 AG11 AG15 AG18 AG22 AG27 AG5 AG9 AJ1 AJ30 AK2 AK29 C1 C28 C3 C30 D10

D12 D15 D18 D21 D24 D25 D27 D4 D6 D9 E4 F27 G12 G16 G18 G21 G24 G9 H12 H14 H16 H18 H21

GPU VCORE - 1.3V/1.05V

10 =PP1V05R1V3_GPU_VCORE

C5900 10UF 20% 6.3V X5R 603
C5901 10UF 20% 6.3V X5R 603
C5902 0.22UF 10% 6.3V CERM-X5R 402
C5903 0.22UF 10% 6.3V CERM-X5R 402
C5904 0.22UF 10% 6.3V CERM-X5R 402
C5905 0.22UF 10% 6.3V CERM-X5R 402
C5906 0.22UF 10% 6.3V CERM-X5R 402
C5907 0.22UF 10% 6.3V CERM-X5R 402
C5908 0.22UF 10% 6.3V CERM-X5R 402
C5909 0.22UF 10% 6.3V CERM-X5R 402
C5910 0.22UF 10% 6.3V CERM-X5R 402
C5911 0.22UF 10% 6.3V CERM-X5R 402
C5912 0.22UF 10% 6.3V CERM-X5R 402
C5913 0.22UF 10% 6.3V CERM-X5R 402
C5914 0.22UF 10% 6.3V CERM-X5R 402
C5915 0.22UF 10% 6.3V CERM-X5R 402
C5916 0.22UF 10% 6.3V CERM-X5R 402
C5917 0.22UF 10% 6.3V CERM-X5R 402
C5918 0.22UF 10% 6.3V CERM-X5R 402
C5919 0.22UF 10% 6.3V CERM-X5R 402
C5920 0.22UF 10% 6.3V CERM-X5R 402
C5921 0.22UF 10% 6.3V CERM-X5R 402
C5922 0.22UF 10% 6.3V CERM-X5R 402
C5923 0.22UF 10% 6.3V CERM-X5R 402
C5924 0.22UF 10% 6.3V CERM-X5R 402

AC13 AC15 AC17 AD13 AD15 M12 M13 M14 M17 M18 M19 N12 N13 N14 N17 N18 N19 P12 P13 P14 P17 P18 P19 U12 U13 U14 U17 U18 U19 V12 V13 V14 V17 V18 V19 W12 W13 W14 W17 W18 W19

VDDC

Internal I/O - 1.3V/1.05V

OMIT
CRITICAL
U5700
M11P
BGA
(8 OF 8)

L5990
60-OHM-EMI
SM

VDDCI: M15 R19 T12 W16

C5990 10UF 20% 6.3V X5R 603
C5991 0.01uF 20% 16V CERM 402
C5992 0.01uF 20% 16V CERM 402
C5993 0.01uF 20% 16V CERM 402
C5994 0.01uF 20% 16V CERM 402

PP1VR1V3_GPU_VDDCI
VOLTAGE=1.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

VDD15: AC11 AC20 H11 H20 L23 P8 Y23 Y8

Internal I/O - 1.5V

10 =PP1V5_GPU_VDD15

CRITICAL
Q5950
SI3446DV
TSOP-LF

26 GPUVDD15_EN

C5950 1000pF 10% 25V X7R 402

L5950
FERR-220-OHM
0805

PP1V5_GPU_VDD15_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

(500mA)

PP1V5_GPU_VDD15
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C5951 0.01uF 20% 16V CERM 402
C5952 0.01uF 20% 16V CERM 402
C5953 0.01uF 20% 16V CERM 402
C5954 0.01uF 20% 16V CERM 402
C5955 10UF 20% 6.3V X5R 603
C5956 0.01uF 20% 16V CERM 402
C5957 0.01uF 20% 16V CERM 402
C5958 0.01uF 20% 16V CERM 402
C5959 0.01uF 20% 16V CERM 402

GPU (M11) Core Power

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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SCALE: NONE

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Page Notes

Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP3V3_GPU_VDDR3
- =PP1V5_GPU_DVO
- =PP1V8_GPU_DVO
- =PP1V5R3V3_DVO_VREF
- =PP1V8_GPU_PANEL_IO
- =PP1V8_GPU_LVDS_PLL
- =PP2V5_GPU_LVDS_IO
- =PP2V5_GPU_LVDS_IO
- =PP1V5_AGP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- DVO_1V8
- GPU_LVDDR_2V5
- GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

OMIT
CRITICAL
U5700
M11P
BGA
(7 OF 8)

MEMORY I/O - 1.8V/2.5V

L6050
FERR-220-OHM
0805
(1200mA)
=PP1V8R2V5_GPU_FB_VIO
PP1V8R2V5_GPU_FB_VIO
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C6050 C6051 C6052 C6053 C6054 — 10UF 20% 6.3V X5R 603
C6055 C6056 C6057 C6058 C6059 — 0.1UF 20% 10V CERM 402
C6060 C6061 C6062 C6063 C6064 — 0.1UF 20% 10V CERM 402
C6065 C6066 C6067 C6068 C6069 — 10UF 20% 6.3V X5R 603
C6070 C6071 C6072 C6073 C6074 — 0.1UF 20% 10V CERM 402
C6075 C6076 C6077 C6078 C6079 — 0.1UF 20% 10V CERM 402
C6080 C6081 C6082 C6083 C6084 — 10UF 20% 6.3V X5R 603
C6085 C6086 C6087 C6088 C6089 — 0.1UF 20% 10V CERM 402
C6090 C6091 C6092 C6093 C6094 — 0.1UF 20% 10V CERM 402

VDDR1
A15 A21 A28 A3 A9 AA1 AA4 AA7 AA8 AD4 B1 B30 D11 D13 D14 D17 D19 D20 D23 D26 D5 D8 E27 F4 G10 G13 G15 G19 G22 G27 G7 H10 H13 H15 H17 H19 H22 J1 J23 J24 J4 J7 J8 L27 L8 M4 N4 N7 N8 R1 R4 T4 T7 T8 V4 V7 V8

GPIO - 3.3V

L6000
FERR-10-OHM-500MA
=PP3V3_GPU_VDDR3
PP3V3_GPU_VDDR3
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
SM

VDDR3: AC19 AC21 AC22 AC8 AD19 AD21 AD22 AD7
C6000 10UF 20% 6.3V X5R 603
C6001 C6002 C6003 — 0.1UF 20% 10V CERM 402
C6004 C6005 C6006 — 0.1UF 20% 10V CERM 402

DVO I/O (EXT.TMDS) - 1.5V/1.8V

VDDR4: AC10 AC9 AD10 AD9 AG7
C6010 10UF 20% 6.3V X5R 603
C6011 C6012 C6013 — 0.1UF 20% 10V CERM 402
C6014 C6015 — 0.1UF 20% 10V CERM 402

PP1V5R3V3_GPU_VDDR4
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

=PP1V8_GPU_DVO
DVO_1V8
L6010
FERR-10-OHM-500MA
SM

=PP1V5_GPU_DVO
DVO_1V5
L6011
FERR-10-OHM-500MA
SM
=PP1V5R3V3_DVO_VREF

AGP 4X I/O - 1.5V

=PP1V5_AGP
L6020
FERR-10-OHM-500MA
(20mA)
PP1V5_GPU_AGP
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SM

VDDP: AA23 AA24 AB30 AC23 AC27 AE30 AF27 J30 M23 M24 N30 P23 P27 T23 T24 T30 U27 V23 V24 W30 Y27
C6020 0.1UF 20% 10V CERM 402
C6021 C6022 C6023 — 0.1UF 20% 10V CERM 402
C6024 10UF 20% 6.3V X5R 603
C6025 C6026 C6027 C6028 C6029 — 0.01UF 20% 16V CERM 402
C6030 C6031 C6032 C6033 — 0.1UF 20% 10V CERM 402

LVDS PLL - 1.8V

=PP1V8_GPU_LVDS_PLL
L6048
FERR-220-OHM
(40mA)
0402
PP1V8_GPU_LVDS_PLL
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

C6048 10UF 20% 6.3V X5R 603
C6049 0.01UF 20% 16V CERM 402

LVDS I/O - 1.8V

L6043
FERR-220-OHM
0402
=PP1V8_GPU_PANEL_IO
PP1V8_GPU_PANEL_IO
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
ALSO TXVDDR

LPVDD AJ20
LVDDR_18_0 AE15
LVDDR_18_1 AF21
LVDDR_25_0 AE17
LVDDR_25_1 AE20

C6043 10UF 20% 6.3V X5R 603
C6044 C6045 C6046 — 0.1UF 20% 10V CERM 402
C6047 0.01UF 20% 16V CERM 402

(180mA)

LVDS I/O - 2.5V/2.8V

=PP2V5_GPU_LVDS_IO
GPU_LVDDR_2V5
L6040
FERR-10-OHM-500MA
SM
(350mA)
PP2V5R2V8_GPU_LVDS_IO
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
=PP2V8_GPU_LVDS_IO
GPU_LVDDR_2V8
L6041
FERR-10-OHM-500MA
SM

C6040 10UF 20% 6.3V X5R 603
C6041 C6042 — 0.01UF 20% 16V CERM 402

VDDRH1 N6
VDDRH0 F18
VSSRH0 F19
VSSRH1 M6

C6095 10UF 20% 6.3V X5R 603
C6096 C6097 — 0.01UF 20% 16V CERM 402

L6095
FERR-220-OHM
0402
PP1V8_GPU_VDD_MEM_CLK
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

GPU (M11) I/O Power

SYNC_MASTER=MARIAS
SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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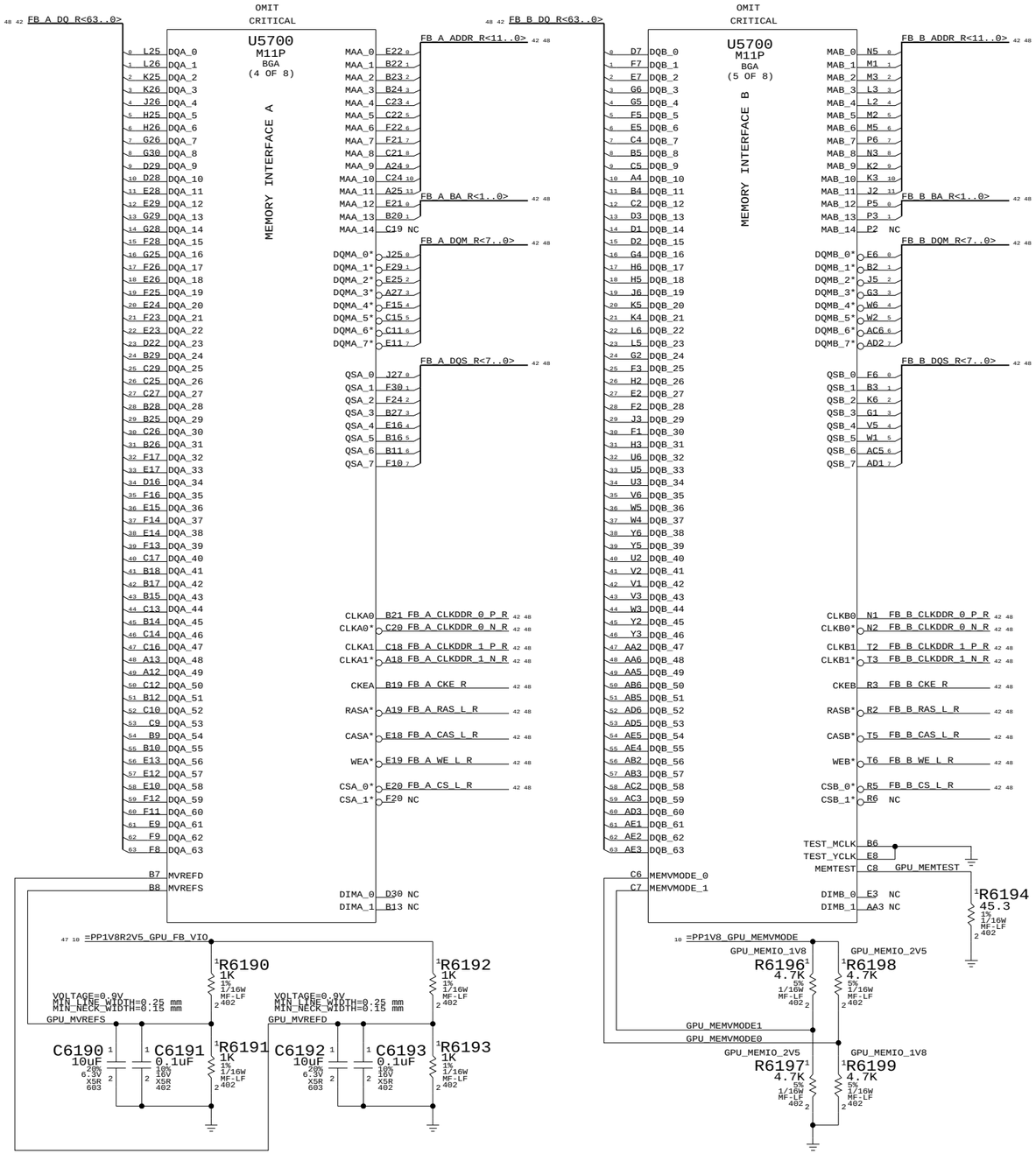
Page Notes

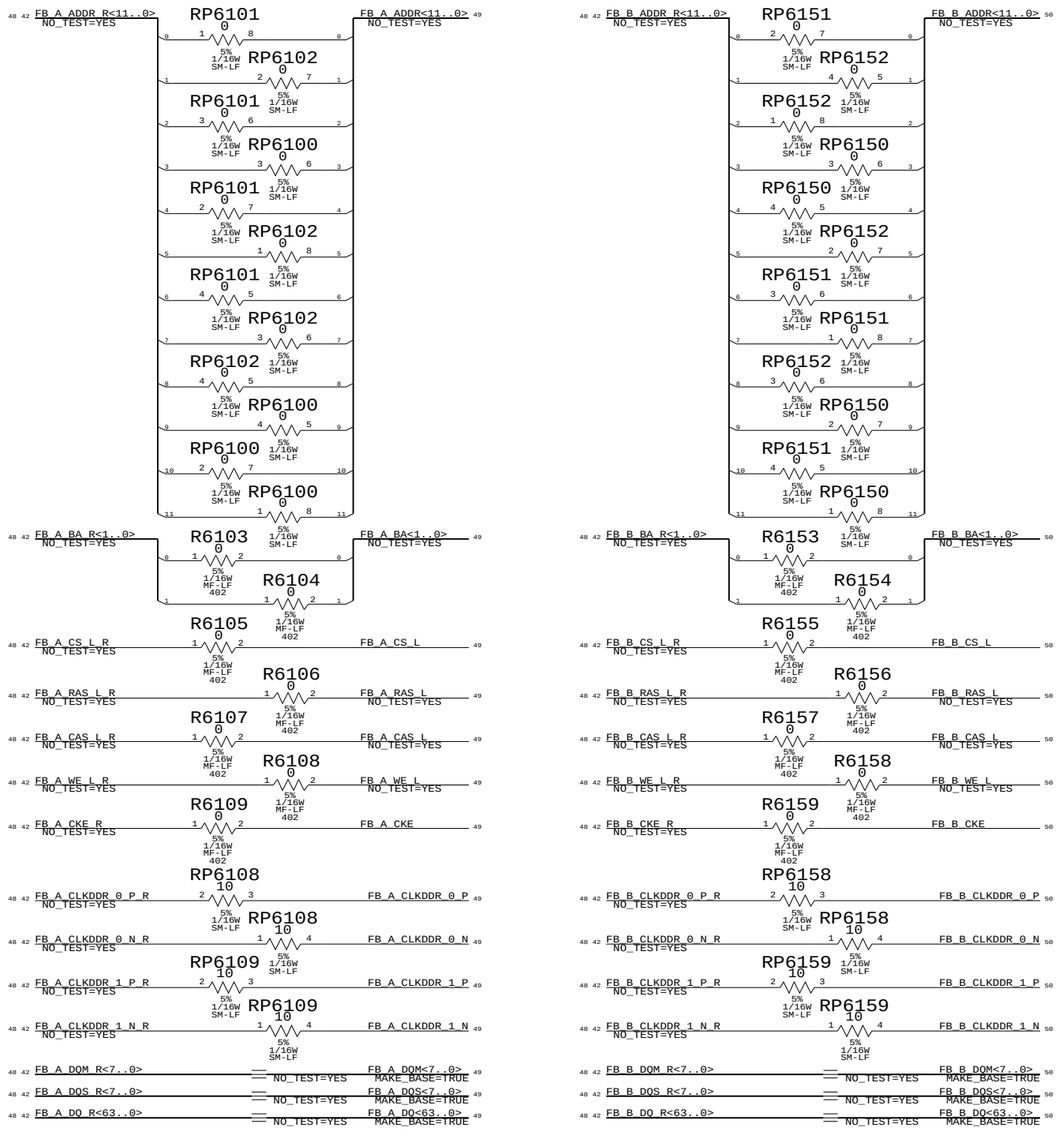
Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_MEMIO_1V8
- GPU_MEMIO_2V5



GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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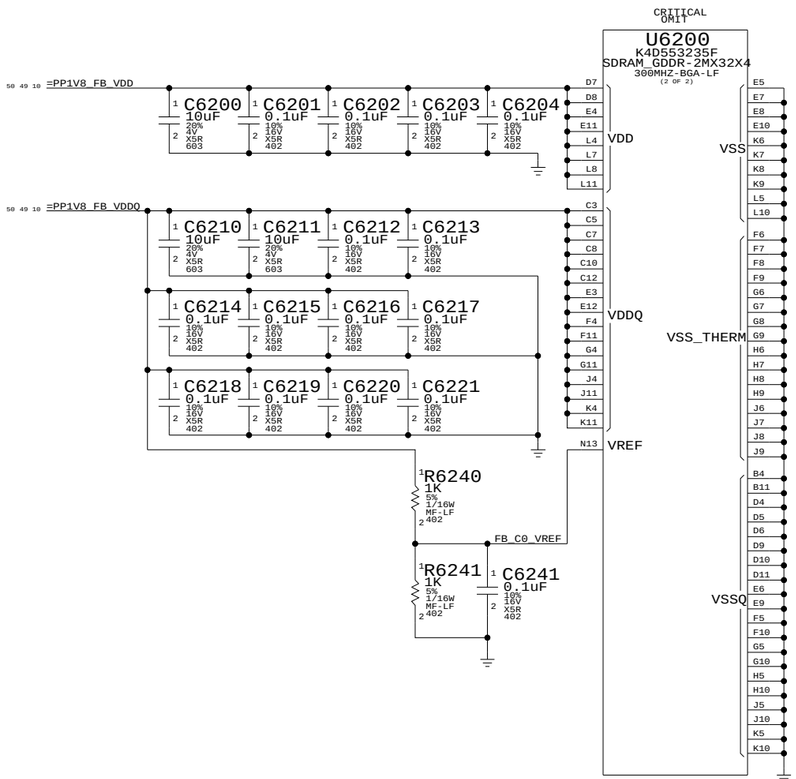
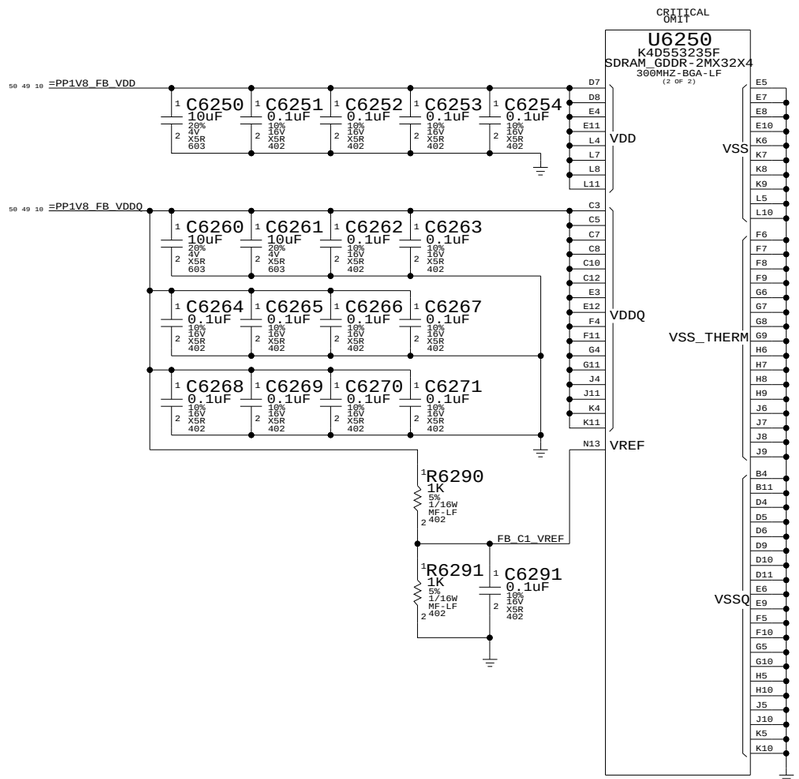
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 61 OF 115	





Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

ECSETs provided by GPU

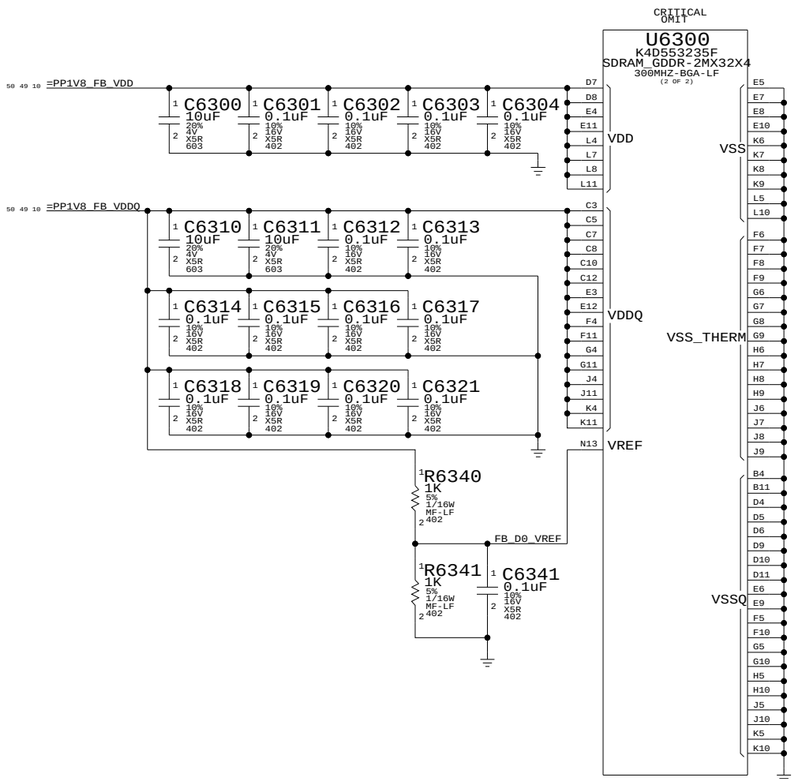
NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
I244	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_P 48 49
I245	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_N 48 49
I246	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_P 48 49
I247	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_N 48 49
I248	RAM	RAM		FB_A_CKE 48 49
I249	RAM	RAM		FB_A_CS_L 48 49
I250	RAM	RAM		FB_A_ADDR<11..0> 48 49
I251	RAM	RAM		FB_A_BA<1..0> 48 49
I253	RAM	RAM		FB_A_RAS_L 48 49
I252	RAM	RAM		FB_A_CAS_L 48 49
I254	RAM	RAM		FB_A_WE_L 48 49
I255	RAM	RAM		FB_A_DQS<7..0> 48 49
I256	RAM	RAM		FB_A_DQM<7..0> 48 49
I257	RAM	RAM		FB_A_DQ<63..0> 48 49

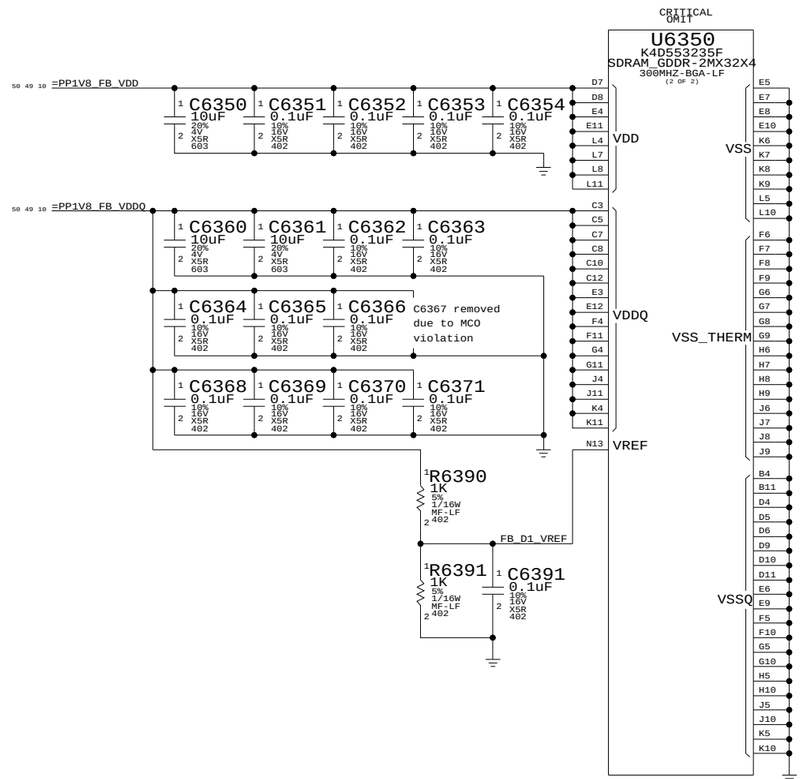
GPU Frame Buffer A

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 62 OF 115	





Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NET_TYPE

ECLECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
ECSETs provided by GPU				
I243	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_P 48 50
I244	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_N 48 50
I245	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_P 48 50
I247	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_N 48 50
I246	RAM	RAM		FB_B_CKE 48 50
I248	RAM	RAM		FB_B_CS_L 48 50
I252	RAM	RAM		FB_B_ADDR<11..0> 48 50
I251	RAM	RAM		FB_B_BA<1..0> 48 50
I249	RAM	RAM		FB_B_RAS_L 48 50
I250	RAM	RAM		FB_B_CAS_L 48 50
I253	RAM	RAM		FB_B_WE_L 48 50
I254	RAM	RAM		FB_B_DQS<7..0> 48 50
I255	RAM	RAM		FB_B_DQM<7..0> 48 50
I256	RAM	RAM		FB_B_DQ<63..0> 48 50

GPU Frame Buffer B

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

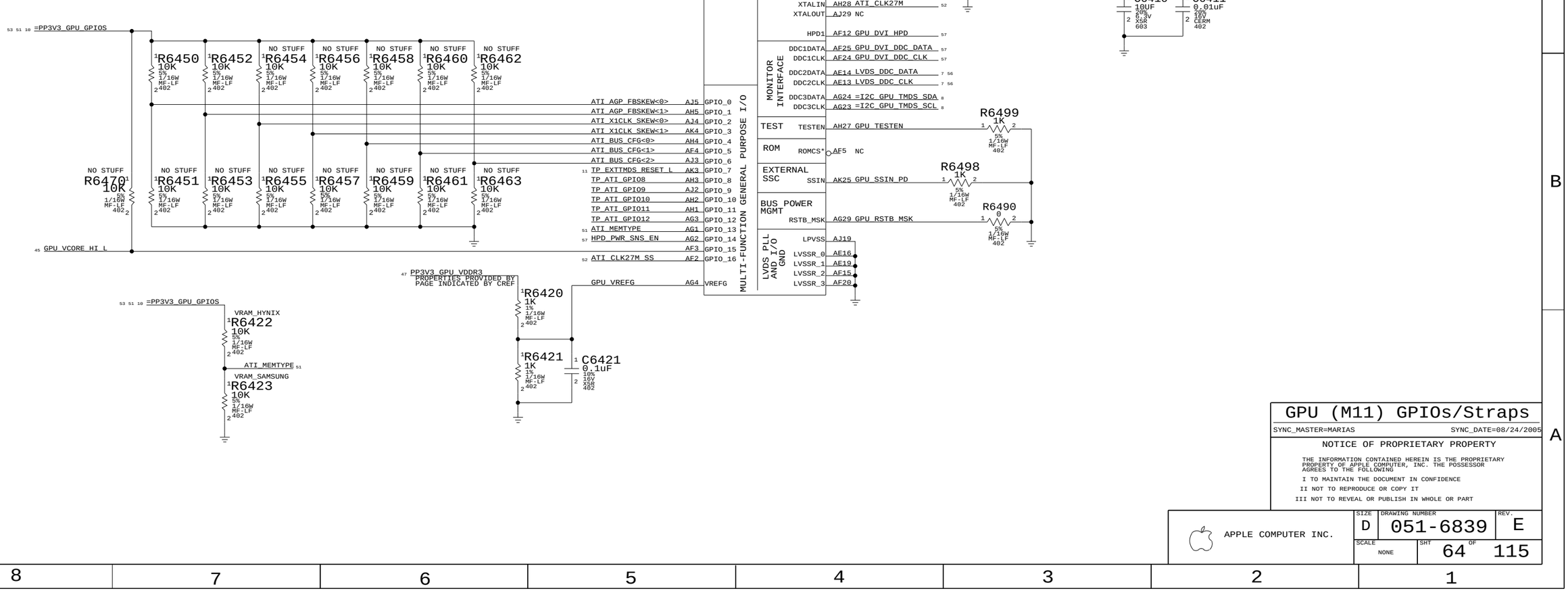
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 63 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



GPU (M11) GPIOs/Straps

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
160 ATI_CLK27M	CLOCK	CLOCK	
164	CLOCK	CLOCK	
165	CLOCK	CLOCK	
161 ATI_CLK27M_SS	CLOCK	CLOCK	
162	CLOCK	CLOCK	

ATI_CLK27M_R 52
ATI_CLK27M 51 52
ATI_CLK27M_SSIN 52
ATI_CLK27M_SS_R 52
ATI_CLK27M_SS 51 52

27M OSC

52 10 =PP3V3_GPU_CLOCKS
L6500 FERR-EMI-100-OHM SM
VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
PP3V3_GPU_OSC
C6500 0.1uF 20% 10V CERM 402
C6501 4.7uF 20% 6.3V CERM 805
R6503 100K 5% 1/16W MF-LF 402 (NO STUFF)
CRITICAL
U6500 27MHZ OSC SM
VCC 14
OE 1
OUT 8
GND 7
ATI_OSC_OE
GPU_SS (PLACE R6500 CLOSE TO OSC)
R6500 0 5% 1/16W MF-LF 402
8 52 ATI_CLK27M_R
ATI_CLK27M_SSIN 52
R6501 287 1% 1/16W MF-LF 402
(PLACE THE OSCILLATOR AND R6501/R6502 CLOSE TO M18 IC)
ATI_CLK27M 51 52
R6502 162 1% 1/16W MF-LF 402

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD

52 10 =PP3V3_GPU_CLOCKS
GPU_SS L6510 FERR-EMI-100-OHM SM
VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
PP3V3_GPU_SS
GPU_SS C6510 10UF 20% 6.3V X5R 603
GPU_SS C6511 0.1UF 20% 10V CERM 402
GPU_SS CRITICAL
U6510 CY25811 SOI-LF
VDD 7
XIN/CLKIN 1
XOUT 8
FRSEL 6
S1 3
S0 4
VSS 2
NC
NC
52 ATI_CLK27M_SSIN
CY25811_S1
CY25811_S0
SSCLK 5
GPU_SS R6510 33 5% 1/16W MF-LF 402
52 ATI_CLK27M_SS_R
ATI_CLK27M_SS 51 52
NO STUFF R6511 0 5% 1/16W MF-LF 402
GPU_SS R6513 0 5% 1/16W MF-LF 402
NO STUFF R6512 0 5% 1/16W MF-LF 402
NO STUFF R6514 0 5% 1/16W MF-LF 402

M11 Power Shutdown Sequencing

10 =PP2V5_GPU_PWRSEQ
XW6590 SM
PP2V5_GPU_PSNECK VOLTAGE=2.5V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
DP6590 BAS16TW-X-F SOT-363
10 =PP3V3_GPU_PWRSEQ
XW6593 SM
PP3V3_GPU_PSNECK VOLTAGE=3.3V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
10 =PP1V8_GPU_PWRSEQ
XW6591 SM
PP1V8_GPU_PSNECK VOLTAGE=1.8V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
DP6590 BAS16TW-X-F SOT-363
10 =PP1V5_GPU_PWRSEQ
XW6592 SM
PP1V5_GPU_PSNECK VOLTAGE=1.5V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
DP6590 BAS16TW-X-F SOT-363

LVDDR 2.8V LDO

GPU_LVDDR_2V8 CRITICAL
U6530 MAX8860EUA27+T UMAX
IN 2
OUT1 1
OUT2 4
SHDN* 7
SET 5
FAULT* 8 MAX8860_FAULT_L
CC 6 MAX8860_CC
GND 3
10 =PPVIN_GPU_LVDDR_LDO
GPU_LVDDR_2V8 C6530 2.2uF 20% 6.3V CERM1 603
GPU_LVDDR_2V8 C6531 0.033uF 20% 10V X7R 402
GPU_LVDDR_2V8 R6530 100K 5% 1/10W MF-LF 402
=PP2V8_GPU_LVDDR_LDO 10
GPU_LVDDR_2V8 C6532 2.2uF 20% 6.3V CERM1 603

PART NUMBER	1S ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1188	353S1140	GPU_LVDDR_2V8	U6530	Primary is 2.77V/Alt is 2.82V

GPU (M11) Clocks/Misc

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

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SCALE: NONE	SHT 65 OF 115	

Page Notes

Power aliases required by this page:
- =PP2V5_GPU_A2VDD
- =PP1V8_GPU_AVDD
- =PP1V8_GPU_TPVDD
- =PP3V3_GPU_GPIOS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- GPU_VDDR4_3V3
- DVO_1V8
- DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	DVO	DVO		GPU_DVOD_R<23..0>
ECSETs provided by SI TMDS	DVO	DVO		GPU_DVO_HSYNC_R
	DVO	DVO		GPU_DVO_VSYNC_R
	DVO	DVO		GPU_DVO_DE_R
	DVO	DVO		GPU_DVO_CLKP_R
LVDS_DATA	LVDS	LVDS	LVDS_U0	LVDS_U0_P
	LVDS	LVDS	LVDS_U0	LVDS_U0_N
LVDS_DATA	LVDS	LVDS	LVDS_U1	LVDS_U1_P
	LVDS	LVDS	LVDS_U1	LVDS_U1_N
LVDS_DATA	LVDS	LVDS	LVDS_U2	LVDS_U2_P
	LVDS	LVDS	LVDS_U2	LVDS_U2_N
LVDS_CLK_UPPER	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_P
	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_N
LVDS_DATA	LVDS	LVDS	LVDS_L0	LVDS_L0_P
	LVDS	LVDS	LVDS_L0	LVDS_L0_N
LVDS_DATA	LVDS	LVDS	LVDS_L1	LVDS_L1_P
	LVDS	LVDS	LVDS_L1	LVDS_L1_N
LVDS_DATA	LVDS	LVDS	LVDS_L2	LVDS_L2_P
	LVDS	LVDS	LVDS_L2	LVDS_L2_N
LVDS_CLK_LOWER	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_P
	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_N
	VGA	VGA		GPU_VGA_R
	VGA	VGA		GPU_VGA_G
	VGA	VGA		GPU_VGA_B
	VGA_CONN	VGA_CONN		VGA_R
	VGA_CONN	VGA_CONN		VGA_G
	VGA_CONN	VGA_CONN		VGA_B
	TV	TV		GPU_TV_Y
	TV	TV		GPU_TV_C
	TV	TV		GPU_TV_COMP
	TV_CONN	TV_CONN		TV_Y
	TV_CONN	TV_CONN		TV_C
	TV_CONN	TV_CONN		TV_COMP

OMIT
CRITICAL

U5700
M11P
BGA
(3 OF 8)

INTEGRATED TMDS
VIP HOST/ EXTERNAL TMDS
DAC/CRT
DAC2
(TV/CRT2)
LVDS CHANNEL
CONTROL AND
EXTERNAL SSC

PP1V5R3V3_GPU_VDDR4
DVO_1V5&DVO_1V8
DVO_3V3&GPU_VDDR4_3V3
R6640 10K 5% 1/16W MF-LF 402
R6641 10K 5% 1/16W MF-LF 402
GPU_DVOVMODE AE10 DVOVMODE

GPU_DVO_VSYNC_R AJ10 ZV_LCDCNTL_0
GPU_DVO_HSYNC_R AK10 ZV_LCDCNTL_1
GPU_DVO_DE_R AJ11 ZV_LCDCNTL_2
GPU_DVO_CLKP_R AH11 ZV_LCDCNTL_3
GPU_DVOD_R<0> AH6 ZV_LCDDATA_0
GPU_DVOD_R<1> AJ6 ZV_LCDDATA_1
GPU_DVOD_R<2> AK6 ZV_LCDDATA_2
GPU_DVOD_R<3> AH7 ZV_LCDDATA_3
GPU_DVOD_R<4> AK7 ZV_LCDDATA_4
GPU_DVOD_R<5> AJ7 ZV_LCDDATA_5
GPU_DVOD_R<6> AH8 ZV_LCDDATA_6
GPU_DVOD_R<7> AJ8 ZV_LCDDATA_7
GPU_DVOD_R<8> AH9 ZV_LCDDATA_8
GPU_DVOD_R<9> AJ9 ZV_LCDDATA_9
GPU_DVOD_R<10> AK9 ZV_LCDDATA_10
GPU_DVOD_R<11> AH10 ZV_LCDDATA_11
GPU_DVOD_R<12> AE6 ZV_LCDDATA_12
GPU_DVOD_R<13> AG6 ZV_LCDDATA_13
GPU_DVOD_R<14> AF6 ZV_LCDDATA_14
GPU_DVOD_R<15> AE7 ZV_LCDDATA_15
GPU_DVOD_R<16> AF7 ZV_LCDDATA_16
GPU_DVOD_R<17> AE8 ZV_LCDDATA_17
GPU_DVOD_R<18> AG8 ZV_LCDDATA_18
GPU_DVOD_R<19> AF8 ZV_LCDDATA_19
GPU_DVOD_R<20> AE9 ZV_LCDDATA_20
GPU_DVOD_R<21> AF9 ZV_LCDDATA_21
GPU_DVOD_R<22> AG10 ZV_LCDDATA_22
GPU_DVOD_R<23> AF10 ZV_LCDDATA_23

INV_ON_PWM AG12 BLON
PANEL_PWR_EN AE12 DIGON
NC AJ25 SSOUT
R6680 10K 5% 1/16W MF-LF 402
R6681 10K 5% 1/16W MF-LF 402

LVDS_U0_P AF16 TXOUT_U0P
LVDS_U0_N AG16 TXOUT_U0N
LVDS_U1_P AF17 TXOUT_U1P
LVDS_U1_N AG17 TXOUT_U1N
LVDS_U2_P AE18 TXOUT_U2P
LVDS_U2_N AF18 TXOUT_U2N
NO_TEST=YES TP_LVDS_U3_P AG20 TXOUT_U3P
NO_TEST=YES TP_LVDS_U3_N AH20 TXOUT_U3N
CLKLVDS_U_P AG19 TXCLK_UP
CLKLVDS_U_N AF19 TXCLK_UN
LVDS_L0_P AH16 TXOUT_L0P
LVDS_L0_N AK16 TXOUT_L0N
LVDS_L1_P AJ16 TXOUT_L1P
LVDS_L1_N AH17 TXOUT_L1N
LVDS_L2_P AJ17 TXOUT_L2P
LVDS_L2_N AH18 TXOUT_L2N
NO_TEST=YES TP_LVDS_L3_P AH19 TXOUT_L3P
NO_TEST=YES TP_LVDS_L3_N AK19 TXOUT_L3N
CLKLVDS_L_P AJ18 TXCLK_LP
CLKLVDS_L_N AK18 TXCLK_LN

TXCM AH13 NC
TXCP AK13 NC
TX0M AJ13 NC
TX0P AH14 NC
TX1M AJ14 NC
TX1P AH15 NC
TX2M AJ15 NC
TX2P AK15 NC
TPVDD AK12
TPVSS AJ12
TXVDDR1 AF14
TXVDDR0 AF13
TXVSSR0 AG13
TXVSSR1 AG14
TXVSSR2 AH12

R AK27 GPU_VGA_R
G AJ27 GPU_VGA_G
B AJ26 GPU_VGA_B
HSYNC AG25 GPU_VGA_HSYNC
VSYNC AH25 GPU_VGA_VSYNC
AUXWIN AF26 GPU_AUXWIN_PU
RSET AH26 ATI_RSET
AVDD AH24 (PP1V8_GPU_AVDD)
AVSSQ AD24
AVSSN AH23
VDD1DI AE24 (PP1V8_GPU_VDDDI)
VSS1DI AE23

H2SYNC AJ24 NC
V2SYNC AK24 NC
Y_G AJ22 GPU_TV_Y
C_R AJ23 GPU_TV_C
COMP_B AK22 GPU_TV_COMP
R2SET AK21 ATI_R2SET
A2VDD0 AG21 (PP2V5_GPU_A2VDD)
A2VDD1 AH21
A2VSSN0 AH22
A2VSSN1 AJ21
A2VDDQ AF22 (PP1V8_GPU_A2VDDQ)
A2VSSQ AF23
VDD2DI AE22 (PP1V8_GPU_VDDDI)
VSS2DI AE21

L6600 FERR-220-OHM 0402
PP1V8_GPU_TPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
C6600 1uF 10% 6.3V CERM 402
C6601 0.01uF 20% 16V CERM 402
C6605 0.1uF 20% 10V CERM 402
C6606 0.1uF 20% 10V CERM 402
C6607 0.01uF 20% 16V CERM 402
PP1V8_GPU_PANEL_IO PROPERTIES PROVIDED BY PAGE INDICATED BY CREF

R6690 10K 5% 1/16W MF-LF 402
GPU_AUXWIN_PU

R6650 499 1% 1/16W MF-LF 402
R6660 75 1% 1/16W MF-LF 402
R6661 75 1% 1/16W MF-LF 402
R6662 75 1% 1/16W MF-LF 402
R6651 715 1% 1/16W MF-LF 402
R6670 75 1% 1/16W MF-LF 402
R6671 75 1% 1/16W MF-LF 402
R6672 75 1% 1/16W MF-LF 402

L6610 FERR-220-OHM 0402
PP1V8_GPU_AVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
C6610 10UF 20% 6.3V X5R 603
C6611 0.01uF 20% 16V CERM 402
(AVDD+VDDDI=75mA)

L6615 FERR-220-OHM 0402
PP1V8_GPU_VDDDI VOLTAGE=1.8V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
C6615 10UF 20% 6.3V X5R 603
C6616 0.01uF 20% 16V CERM 402
C6617 0.01uF 20% 16V CERM 402

L6620 FERR-220-OHM 0402
(140mA)
PP2V5_GPU_A2VDD VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
C6620 10UF 20% 6.3V X5R 603
C6621 0.01uF 20% 16V CERM 402
C6622 0.01uF 20% 16V CERM 402

L6625 FERR-220-OHM 0402
(2mA)
PP1V8_GPU_A2VDDQ VOLTAGE=1.8V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
C6625 10UF 20% 6.3V X5R 603
C6626 0.01uF 20% 16V CERM 402

GPU (M11) DVI/DAC Outputs

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
- =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
- =SI_I2C_CLK
- =SI_I2C_DATA

BOM options provided by this page:
- TMDS_EXT - DVO_1V5 - DVO_3V3
- TMDS_DUAL - DVO_1V8

Net Spacing Type: TMDS

Net Physical Type: TMDS

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
GPU_DVO_LOWER	DVO	DVO		GPU_DVOD<0..11>	6 54
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_HSYNC	6 54 55
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_VSYNC	6 54 55
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_DE	6 54 55
GPU_DVO_CLKP	DVO	DVO		GPU_DVO_CLKP	6 54 55
TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKP	54
TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKN	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DP<0>	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DN<0>	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DP<1>	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DN<1>	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DP<2>	2 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DN<2>	54

Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>, GPU_DVO_HSYNC, GPU_DVO_VSYNC, GPU_DVO_DE, GPU_DVO_CLKP

RP6720 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- =RP6720P1 — 1 — 8 — =RP6720P8
- =RP6720P2 — 2 — 7 — =RP6720P7
- =RP6720P3 — 3 — 6 — =RP6720P6
- =RP6720P4 — 4 — 5 — =RP6720P5

RP6721 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- =RP6721P1 — 1 — 8 — =RP6721P8
- =RP6721P2 — 2 — 7 — =RP6721P7
- =RP6721P3 — 3 — 6 — =RP6721P6
- =RP6721P4 — 4 — 5 — =RP6721P5

RP6722 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- =RP6722P1 — 1 — 8 — =RP6722P8
- =RP6722P2 — 2 — 7 — =RP6722P7
- =RP6722P3 — 3 — 6 — =RP6722P6
- =RP6722P4 — 4 — 5 — =RP6722P5

RP6723 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- =RP6723P1 — 1 — 8 — =RP6723P8
- =RP6723P2 — 2 — 7 — =RP6723P7
- =RP6723P3 — 3 — 6 — =RP6723P6
- =RP6723P4 — 4 — 5 — =RP6723P5

SILICON IMAGE TMDS

RP6707 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_CLKN — 1 — 4 — TMDS_CLKN 54 57

RP6707 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_CLKP — 2 — 3 — TMDS_CLKP 54 57

RP6708 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_DN<0> — 1 — 4 — TMDS_DN<0> 54 57

RP6708 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_DP<0> — 2 — 3 — TMDS_DP<0> 54 57

RP6709 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_DN<1> — 2 — 3 — TMDS_DN<1> 54 57

RP6709 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_DP<1> — 1 — 4 — TMDS_DP<1> 54 57

RP6710 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 SI_TMDS_DN<2> — 2 — 3 — TMDS_DN<2> 54 57

RP6710 10 5% 1/16W SM-LF — TMDS_EXT&TMDS_DUAL
- 54 2 SI_TMDS_DP<2> — 1 — 4 — TMDS_DP<2> 54 57

EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN

EXT_TMDS_CLK_CMF
- R6760 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 57 54 TMDS_CLKP
- R6761 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — TMDS_CLKN 54 57
- C6760 0.001uF 10% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

EXT_TMDS_D0_CMF
- R6762 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 57 54 TMDS_DP<0>
- R6763 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — TMDS_DN<0> 54 57
- C6762 0.001uF 10% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

EXT_TMDS_D1_CMF
- R6764 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 57 54 TMDS_DP<1>
- R6765 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — TMDS_DN<1> 54 57
- C6764 0.001uF 10% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

EXT_TMDS_D2_CMF
- R6766 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 57 54 TMDS_DP<2>
- R6767 49.9 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — TMDS_DN<2> 54 57
- C6766 0.001uF 10% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

L6720 180-OHM-1.5A 0603 — TMDS_EXT&TMDS_DUAL — =PP3V3_RUN_SI 10 54 55
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
VOLTAGE=3.3V
PP3V3_SI_M_VCC
- C6720 10UF 10% 6.3V X5R 805 — TMDS_EXT&TMDS_DUAL
- C6721 100pF 5% 50V CERM 402 — TMDS_EXT&TMDS_DUAL
- C6722 100pF 5% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

L6723 180-OHM-1.5A 0603 — TMDS_EXT&TMDS_DUAL — =PP3V3_RUN_SI 10 54 55
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
VOLTAGE=3.3V
PP3V3_SI_M_AVCC
- C6723 10UF 10% 6.3V X5R 805 — TMDS_EXT&TMDS_DUAL
- C6724 100pF 5% 50V CERM 402 — TMDS_EXT&TMDS_DUAL
- C6725 100pF 5% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

L6726 180-OHM-1.5A 0603 — TMDS_EXT&TMDS_DUAL — =PP3V3_RUN_SI 10 54 55
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
VOLTAGE=3.3V
PP3V3_SI_M_PVCC
- C6726 10UF 10% 6.3V X5R 805 — TMDS_EXT&TMDS_DUAL
- C6727 100pF 5% 50V CERM 402 — TMDS_EXT&TMDS_DUAL
- C6728 10UF 10% 6.3V X5R 805 — TMDS_EXT&TMDS_DUAL
- C6729 100pF 5% 50V CERM 402 — TMDS_EXT&TMDS_DUAL

Place C6726/C6727 at pin 28

Place C6728/C6729 at pin 46

R6734 10K 5% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 2

R6752 301 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 2

NO STUFF — R6754 4.99K 1% 1/16W MF-LF 402 — 2

U6700 CRITICAL — SIL1178CS48 TSSOP — TMDS_EXT&TMDS_DUAL

=I2C_SI_M_SCL	8	27	SCL
=I2C_SI_M_SDA	8	26	SDA
SI_M_A1		24	CTL3/A1
=SI_TMDS_RESET_L	55 11	25	RST*
SI_SYNC	55	47	SYNCO/SYNCI
SI_HTPLG	55	44	EHTPLG
GPU_DVOD<0>	54 6	18	D0
GPU_DVOD<1>	54 6	17	D1
GPU_DVOD<2>	54 6	16	D2
GPU_DVOD<3>	54 6	15	D3
GPU_DVOD<4>	54 6	14	D4
GPU_DVOD<5>	54 6	13	D5
GPU_DVOD<6>	54 6	10	D6
GPU_DVOD<7>	54 6	9	D7
GPU_DVOD<8>	54 6	8	D8
GPU_DVOD<9>	54 6	7	D9
GPU_DVOD<10>	54 6	6	D10
GPU_DVOD<11>	54 6	5	D11
GPU_DVO_DE	55 54 6	19	DE
GPU_DVO_HSYNC	55 54 6	20	HSYNC
GPU_DVO_VSYNC	55 54 6	21	VSYNC
GPU_DVO_CLKP	55 54 6	12	IDCK+
SI_IDCK_N	55 54	11	IDCK-
		28	PVCC1
		46	PVCC2
		40	AVCC
		34	AVCC
		22	VCC
		35	VCC
		29	PGND
		45	PGND
		31	AGND
		43	AGND
		37	AGND
		1	GND
		23	GND
		4	GND
		49	THRML PAD
SI_M_MSEN		48	MSEN
SI_TMDS_CLKP		33	TXC+
SI_TMDS_CLKN		32	TXC-
SI_TMDS_DP<0>		36	TX0+
SI_TMDS_DN<0>		35	TX0-
SI_TMDS_DP<1>		39	TX1+
SI_TMDS_DN<1>		38	TX1-
SI_TMDS_DP<2>	2 54	42	TX2+
SI_TMDS_DN<2>	54	41	TX2-
SI_M_EXTSWING		30	EXT_SWING
SI_VREF		2	VREF

DVO_3V3 — R6733 1K 5% 1/16W MF-LF 402 — 2

R6730 10K 5% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 2

NO STUFF — R6732 100K 5% 1/16W MF-LF 402 — 2

R6731 10K 5% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 2

The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.

=PP1V5R3V3_DVO_VREF 47

DVO_1V5&DVO_1V8 — R6740 1K 1% 1/16W MF-LF 402 — TMDS_EXT&TMDS_DUAL — 2

DVO_1V5&DVO_1V8 — R6741 1K 1% 1/16W MF-LF 402 — 2

DVO_1V5&DVO_1V8 — R6742 0 5% 1/16W MF-LF 402 — 2 — 1 — 55 54 SI_IDCK_N

55 54 SI_VREF

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

C6740 0.1uF 20% 10V CERM 402 — TMDS_EXT&TMDS_DUAL

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
TMDS_CLK	TMDS	TMDS	TMDS_CLK	TMDS_CLKP	54 57
TMDS_CLK	TMDS	TMDS	TMDS_CLK	TMDS_CLKN	54 57
TMDS_DATA	TMDS	TMDS	TMDS_D0	TMDS_DP<0>	54 57
TMDS_DATA	TMDS	TMDS	TMDS_D0	TMDS_DN<0>	54 57
TMDS_DATA	TMDS	TMDS	TMDS_D1	TMDS_DP<1>	54 57
TMDS_DATA	TMDS	TMDS	TMDS_D1	TMDS_DN<1>	54 57
TMDS_DATA	TMDS	TMDS	TMDS_D2	TMDS_DP<2>	54 57
TMDS_DATA	TMDS	TMDS	TMDS_D2	TMDS_DN<2>	54 57

Lower TMDS Transmitter

SYNC_MASTER=MARIAS — SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 67 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI

Signal aliases required by this page:
- =SI_I2C_CLK
- =SI_I2C_DATA
- =SI_TMDS_RESET_L
- =RP68xxPy (pinswappable series R)

BOM options provided by this page:
- TMDS_DUAL

Net Spacing Type: TMDS

Net Physical Type: TMDS

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
164	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<12..19> 6 55
165	GPU_DVOD20	DVO	DVO		GPU_DVOD<20> 6 55
166	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<21..23> 6 55
167		PROVIDED BY LOWER TXMR			GPU_DVO_VSYNC 6 54 55
168		PROVIDED BY LOWER TXMR			GPU_DVO_DE 6 54 55
169		PROVIDED BY LOWER TXMR			GPU_DVO_CLKP 6 54 55
174	TMDS_DATA	TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DP<3> 55
175		TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DN<3> 55
176	TMDS_DATA	TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DP<4> 55
177		TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DN<4> 55
178	TMDS_DATA	TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DP<5> 55
179		TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DN<5> 55
180		TMDS	TMDS	TMDS_D3	TMDS_DP<3> 55 57
181		TMDS	TMDS	TMDS_D3	TMDS_DN<3> 55 57
182		TMDS	TMDS	TMDS_D4	TMDS_DP<4> 55 57
183		TMDS	TMDS	TMDS_D4	TMDS_DN<4> 55 57
184		TMDS	TMDS	TMDS_D5	TMDS_DP<5> 55 57
185		TMDS	TMDS	TMDS_D5	TMDS_DN<5> 55 57

Upper DVO series termination

Place close to GPU

One for each of: GPU_DVOD<12..23>

TMDS_DUAL RP6821 10 — =RP6821P1 (1) — (8) =RP6821P8
TMDS_DUAL RP6821 10 — =RP6821P2 (2) — (7) =RP6821P7
TMDS_DUAL RP6821 10 — =RP6821P3 (3) — (6) =RP6821P6
TMDS_DUAL RP6821 10 — =RP6821P4 (4) — (5) =RP6821P5
TMDS_DUAL RP6822 10 — =RP6822P1 (1) — (8) =RP6822P8
TMDS_DUAL RP6822 10 — =RP6822P2 (2) — (7) =RP6822P7
TMDS_DUAL RP6822 10 — =RP6822P3 (3) — (6) =RP6822P6
TMDS_DUAL RP6822 10 — =RP6822P4 (4) — (5) =RP6822P5
TMDS_DUAL RP6823 10 — =RP6823P1 (1) — (8) =RP6823P8
TMDS_DUAL RP6823 10 — =RP6823P2 (2) — (7) =RP6823P7
TMDS_DUAL RP6823 10 — =RP6823P3 (3) — (6) =RP6823P6
TMDS_DUAL RP6823 10 — =RP6823P4 (4) — (5) =RP6823P5

(all: 5% 1/16W SM-LF)

VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
PP3V3_SI_S_PVCC

TMDS_DUAL L6836 180-OHM-1.5A 0603 — =PP3V3_RUN_SI 10 54 55

TMDS_DUAL C6836 10UF 10% 6.3V X5R 805 — Place C6836/C6837 at pin 28.
TMDS_DUAL C6837 100pF 5% 50V CERM 402
TMDS_DUAL C6838 10UF 10% 6.3V X5R 805
TMDS_DUAL C6839 100pF 5% 50V CERM 402 — Place C6838/C6839 at pin 46.

TMDS_DUAL L6833 180-OHM-1.5A 0603 — =PP3V3_RUN_SI 10 54 55

PP3V3_SI_S_AVCC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

TMDS_DUAL C6833 10UF 10% 6.3V X5R 805
TMDS_DUAL C6834 100pF 5% 50V CERM 402
TMDS_DUAL C6835 100pF 5% 50V CERM 402

TMDS_DUAL L6830 180-OHM-1.5A 0603 — =PP3V3_RUN_SI 10 54 55

PP3V3_SI_S_VCC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

TMDS_DUAL C6830 10UF 10% 6.3V X5R 805
TMDS_DUAL C6831 100pF 5% 50V CERM 402
TMDS_DUAL C6832 100pF 5% 50V CERM 402

TMDS_DUAL R6880 10K 5% 1/16W MF-LF 402
TMDS_DUAL R6881 301 1% 1/16W MF-LF 402
NO STUFF R6882 4.99K 1% 1/16W MF-LF 402

PVCC1 (28), PVCC2 (46), AVCC (40), AVCC (34), VCC (22), VCC (5)

8	=I2C_SI_S_SCL	27	SCL	
8	=I2C_SI_S_SDA	26	SDA	
	SI_S_A1	24	CTL3/A1	
54 11	=SI_TMDS_RESET_L	25	RST*	
	SI_SYNC	47	SYNCO/SYNCI	
54	SI_HTPLG	44	EHTPLG	
55 6	GPU_DVOD<12>	18	D0	
55 6	GPU_DVOD<13>	17	D1	
55 6	GPU_DVOD<14>	16	D2	
55 6	GPU_DVOD<15>	15	D3	
55 6	GPU_DVOD<16>	14	D4	
55 6	GPU_DVOD<17>	13	D5	
55 6	GPU_DVOD<18>	10	D6	
55 6	GPU_DVOD<19>	9	D7	
55 6	GPU_DVOD<20>	8	D8	
55 6	GPU_DVOD<21>	7	D9	
55 6	GPU_DVOD<22>	6	D10	
55 6	GPU_DVOD<23>	5	D11	
55 54 6	GPU_DVO_DE	19	DE	
54 6	GPU_DVO_HSYNC	20	HSYNC	
55 54 6	GPU_DVO_VSYNC	21	VSYNC	
55 54 6	GPU_DVO_CLKP	12	IDCK+	
54	SI_IDCK_N	11	IDCK-	

CRITICAL U6800 SIL1178CS48 TSSOP

MSEN	48		SI_S_MSEN
TXC+	33	NC	
TXC-	32	NC	
TX0+	36		SI_TMDS_DP<3> 55
TX0-	35		SI_TMDS_DN<3> 55
TX1+	39		SI_TMDS_DP<4> 55
TX1-	38		SI_TMDS_DN<4> 55
TX2+	42		SI_TMDS_DP<5> 55
TX2-	41		SI_TMDS_DN<5> 55
EXT_SWING	30		SI_S_EXTSWING
VREF	2		SI_VREF 54

PGND (29), PGND (45), AGND (31), AGND (43), AGND (37), GND (1), GND (23), GND (4), THRMHL PAD (49)

Upper Channel Series Termination

TMDS_DUAL RP6811 10 — 55 SI_TMDS_DN<3> — TMDS_DN<3> 55 57
TMDS_DUAL RP6811 10 — 55 SI_TMDS_DP<3> — TMDS_DP<3> 55 57
TMDS_DUAL RP6812 10 — 55 SI_TMDS_DN<4> — TMDS_DN<4> 55 57
TMDS_DUAL RP6812 10 — 55 SI_TMDS_DP<4> — TMDS_DP<4> 55 57
TMDS_DUAL RP6813 10 — 55 SI_TMDS_DN<5> — TMDS_DN<5> 55 57
TMDS_DUAL RP6813 10 — 55 SI_TMDS_DP<5> — TMDS_DP<5> 55 57

(all: 5% 1/16W SM-LF)

Upper Channel Common-mode Termination

TMDS_D3_CMF
TMDS_DUAL R6804 49.9 1% 1/16W MF-LF 402 — 57 55 TMDS_DP<3>
TMDS_DUAL R6805 49.9 1% 1/16W MF-LF 402 — TMDS_DN<3> 55 57
TMDS_DUAL C6804 0.001uF 10% 50V CERM 402

TMDS_D4_CMF
TMDS_DUAL R6802 49.9 1% 1/16W MF-LF 402 — 57 55 TMDS_DP<4>
TMDS_DUAL R6803 49.9 1% 1/16W MF-LF 402 — TMDS_DN<4> 55 57
TMDS_DUAL C6802 0.001uF 10% 50V CERM 402

TMDS_D5_CMF
TMDS_DUAL R6800 49.9 1% 1/16W MF-LF 402 — 57 55 TMDS_DP<5>
TMDS_DUAL R6801 49.9 1% 1/16W MF-LF 402 — TMDS_DN<5> 55 57
TMDS_DUAL C6800 0.001uF 10% 50V CERM 402

Upper TMDS Transmitter

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE: NONE

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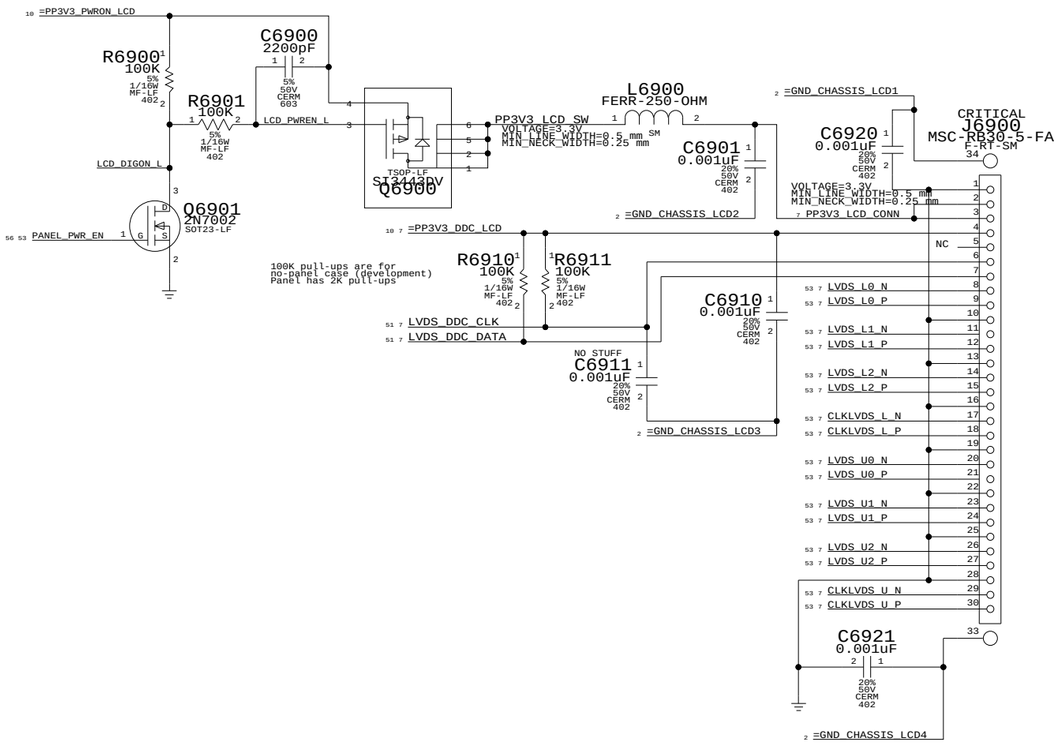
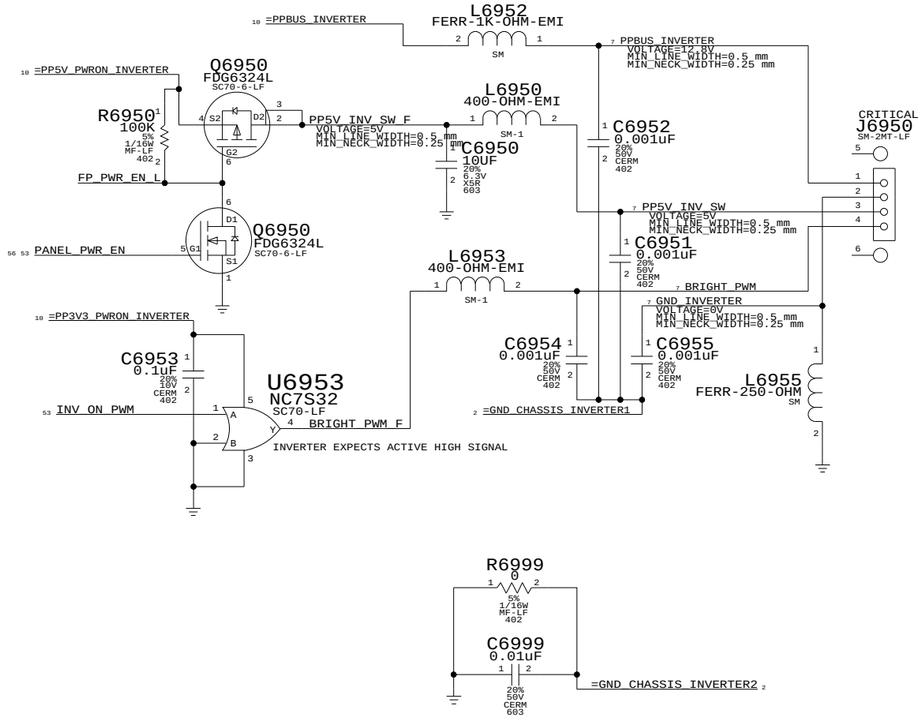
LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 69 OF 115	

DVI INTERFACE

ELECTRICAL_CONSTRAINT_SET

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
1610	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKP
1610	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKN
1606	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DP<0>
1603	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DN<0>
1602	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DP<1>
1605	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DN<1>
1604	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DP<2>
1601	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DN<2>
1609	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DP<3>
1608	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DN<3>
1600	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DP<4>
1607	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DN<4>
1597	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DP<5>
1598	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DN<5>

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L7000 CRITICAL 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
- 54 TMDS_DN<0> 1 — 4 TMDS_CONN_DN<0> 57
- 54 TMDS_DP<0> 2 — 3 TMDS_CONN_DP<0> 57

L7001 CRITICAL 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
- 54 TMDS_DN<1> 1 — 4 TMDS_CONN_DN<1> 57
- 54 TMDS_DP<1> 2 — 3 TMDS_CONN_DP<1> 57

L7002 CRITICAL 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
- 54 TMDS_DN<2> 1 — 4 TMDS_CONN_DN<2> 57
- 54 TMDS_DP<2> 2 — 3 TMDS_CONN_DP<2> 57

L7006 CRITICAL 370-OHM SM SYM_VER-1 — TMDS_EXT&TMDS_DUAL
- 54 TMDS_CLKP 1 — 4 TMDS_CONN_CLKP 57
- 54 TMDS_CLKN 2 — 3 TMDS_CONN_CLKN 57

L7003 CRITICAL 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
- 55 TMDS_DN<3> 1 — 4 TMDS_CONN_DN<3> 57
- 55 TMDS_DP<3> 2 — 3 TMDS_CONN_DP<3> 57

L7004 CRITICAL 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
- 55 TMDS_DN<4> 1 — 4 TMDS_CONN_DN<4> 57
- 55 TMDS_DP<4> 2 — 3 TMDS_CONN_DP<4> 57

L7005 CRITICAL 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
- 55 TMDS_DN<5> 1 — 4 TMDS_CONN_DN<5> 57
- 55 TMDS_DP<5> 2 — 3 TMDS_CONN_DP<5> 57

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

F7010 CRITICAL 0.5AMP-13.2V SM-LF
- 10 =PP5V_RUN_DVI_DDC — 1 — 2 PP5V_RUN_DDC_FUSE VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

L7010 400-OHM-EMI SM-1
- 1 — 2 PP5V_RUN_DDC 57 VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

Isolation required for DVI power switch

D7010 SOD-123
- 1 — 2 B0530WXF
- R7010[1] 4.7K 5% 1/16W MF-LF 402 2

PP5V_RUN_DDC_PULLUPS VOLTAGE=5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

3V LEVEL SHIFTERS

R7012 4.7K 5% 1/16W MF-LF 402 — Q7011 2N7002DW-X-F SOT-363
- R7011 100 5% 1/16W MF-LF 402 — 2 DVI_DDC_CLK — D S 4 — R7020 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_CLK 51
- C7011 100pF 5% 50V CERM 402
- R7013 100 5% 1/16W MF-LF 402 — 2 DVI_DDC_DATA — D S 1 — R7021 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_DATA 51
- C7013 100pF 5% 50V CERM 402
- R7014 100 5% 1/16W MF-LF 402 — 2 DVI_HPD — 3 D S 4 — R7022 100K 5% 1/16W MF-LF 402 — GPU_DVI_HPD 51

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

J7000 CRITICAL QH81127-CK1 F-RT-TH-LF 36 pins

57 TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2> 57
57 TMDS_CONN_DP<0>	18	9	TMDS_CONN_DN<1> 57
		2	TMDS_CONN_DP<2> 57
		10	TMDS_CONN_DP<1> 57
57 TMDS_CONN_DN<5>	20	4	TMDS_CONN_DN<4> 57
57 TMDS_CONN_DP<5>	21	12	TMDS_CONN_DN<3> 57
		5	TMDS_CONN_DP<4> 57
		13	TMDS_CONN_DP<3> 57
	22	6	57 DVI_DDC_CLK_UF
		14	(PP5V_RUN_DDC)
57 TMDS_CONN_CLKP	23	7	DVI_DDC_DATA_UF
57 TMDS_CONN_CLKN	24	8	VGA_VSYNC 57
		16	57 DVI_HPD_UF
57 53 VGA_B	C3	C1	VGA_R 53 57
	C5B	C5A	
57 VGA_HSYNC	C4	C2	VGA_G 53 57
	34	32	
		35	

=GND_CHASSIS_DVI2 2

C7010 0.01uF 20% 50V CERM 603 — PLACE NEAR C5A & C5B

R7030 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_DVI3 2

C7014 100pF 5% 50V CERM 402

R7031 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_DVI4 2

PLACE NEAR 3, 11 & 19

VGA SYNC BUFFERS

C7050 0.1uF — 57 10 =PP3V3_PWRON_VGASYNC

U7050 74AHC1G32 SM-LF — 53 GPU_VGA_VSYNC 1 — 4 GPU_VSYNC_BUF — R7050 33 5% 1/16W MF-LF 402 — VGA_VSYNC 57

PLACE R7050 & R7051 CLOSE TO DVI CONNECTOR

C7051 0.1uF — 57 10 =PP3V3_PWRON_VGASYNC

U7051 74AHC1G32 SM-LF — 53 GPU_VGA_HSYNC 1 — 4 GPU_HSYNC_BUF — R7051 33 5% 1/16W MF-LF 402 — VGA_HSYNC 57

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

FL7040 CRITICAL LCFILTER SM-220MHZ-LF — 53 GPU_VGA_B 1 — 2 VGA_B 53 57
- C7040 3.3pF 0.25% 50V CERM 402
- R7040 75 1% 1/16W MF-LF 402 — NO STUFF

FL7041 CRITICAL LCFILTER SM-220MHZ-LF — 53 GPU_VGA_G 1 — 2 VGA_G 53 57
- C7041 3.3pF 0.25% 50V CERM 402
- R7041 75 1% 1/16W MF-LF 402 — NO STUFF

FL7042 CRITICAL LCFILTER SM-220MHZ-LF — 53 GPU_VGA_R 1 — 2 VGA_R 53 57
- C7042 3.3pF 0.25% 50V CERM 402
- R7042 75 1% 1/16W MF-LF 402 — NO STUFF

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW7060 SM — GND_GPU_TV1 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

L7060 FERR-10-OHM-500MA SM — GND_TV1 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C7060 0.01uF 20% 50V CERM 603

L7062 3.3uH 0603 — 53 GPU_TV_Y — 53 TV_Y
- C7062 560pF 10% 50V CERM 402
- C7063 560pF 10% 50V CERM 402

L7064 3.3uH 0603 — 53 GPU_TV_C — 53 TV_C
- C7064 560pF 10% 50V CERM 402
- C7065 560pF 10% 50V CERM 402

L7066 3.3uH 0603 — 53 GPU_TV_COMP — 53 TV_COMP
- C7066 560pF 10% 50V CERM 402
- C7067 560pF 10% 50V CERM 402

CRITICAL J7060 MINIDIN RT-TH-LF MH11773-MR8N-7F — pins 1 2 3 4 5 8 9 10 11

Q16C/514-0265/MH11773-MR8A-7F
Q41C/514-0256/MH11773-MR8N-7F

XW7061 SM — GND_GPU_TV2 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

L7061 FERR-10-OHM-500MA SM — GND_TV2 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C7061 0.01uF 20% 50V CERM 603

2 =GND_CHASSIS_TV

Place GND shorts at graphics controller

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from GPU during shutdown. When power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

57 PP5V_RUN_DDC — Q7081 TP0610 SOT23-3
- 57 DVI_DDC_CLK_UF 2 — G S D 3 — DVI_TURN_ON
- R7081 680 5% 1/16W MF-LF 402 — DVI_TURN_ON — 1 DVI_TURN_ON_ILIM
- R7083 10K 5% 1/16W MF-LF 402 — DVI_TURN_ON_ILIM — 2 DVI_TURN_ON_BASE — Q7080 MMDT3904XF SOT-363-LF — SYS_POWER_BUTTON_L 24 25 30 36
- R7082[1] 330 5% 1/16W MF-LF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. Comparator output enabled by GPU.

57 10 =PP3V3_DDC_DVI
- C7070 0.1uF 20% 10V CERM 402
- R7072[1] 68.1K 1% 1/16W MF-LF 402 — HPD_4V_REF

U7070 LMC7211 SM-LF — V+ 4, V- 5, 2, 1 HPD_PWR_SW

57 DVI_HPD_UF — R7070 10K 1% 1/16W MF-LF 402 — DVI_HPD_DIV
- R7071[1] 10K 1% 1/16W MF-LF 402
- R7073[1] 100K 1% 1/16W MF-LF 402 — 10 =PPBUS_DVI_PWRSW

Q7076 2N7002DW-X-F SOT-363 — 3 HPD_ON — 4 D S G
- R7078 330 5% 1/16W MF-LF 402 — HPD_ON — 1 HPD_ON_RC
- C7079 47UF 20% 6.3V CERM 1210
- R7080 20K 5% 1/16W MF-LF 402 — HPD_ON_RC — 1 HPD_BASE — Q7080 MMDT3904XF SOT-363-LF
- R7079[1] 68K 5% 1/16W MF-LF 402

Q7075 TP0610 SOT23-3 — S D G
- R7075[1] 100K 5% 1/16W MF-LF 402 — COMP_DISABLE
- R7077[1] 100K 5% 1/16W MF-LF 402 — COMP_ENABLE

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

Q7076 2N7002DW-X-F SOT-363 — 51 HPD_PWR_SNS_EN 2 — G S D
- R7076[1] 100K 5% 1/16W MF-LF 402

External Display Conns

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 70 OF 115	

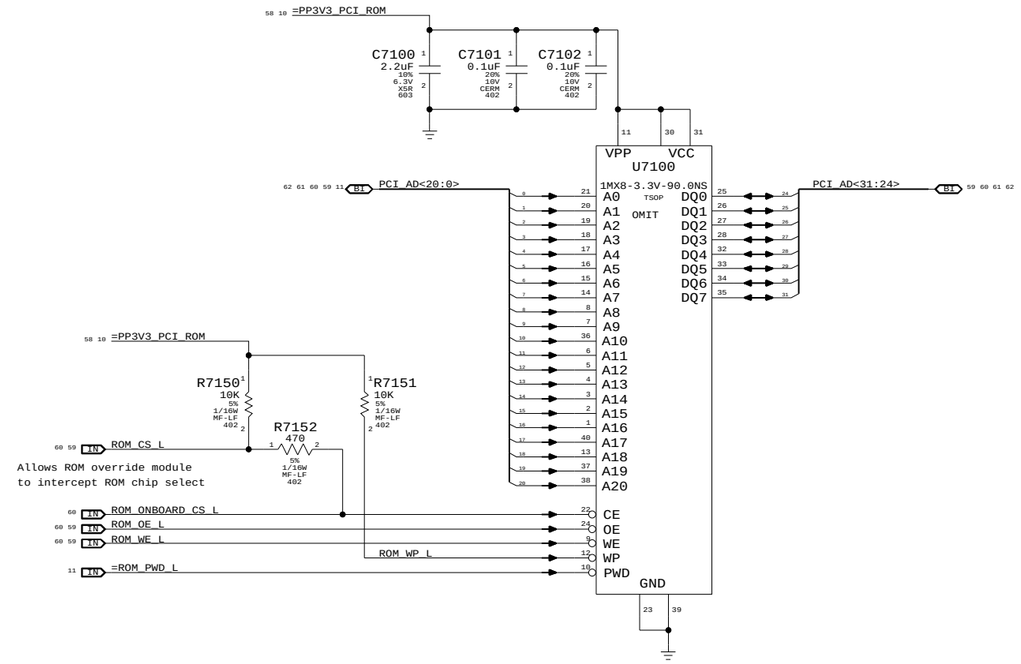
Page Notes

Power aliases required by this page:
- =PP3V3_PCI_ROM

Signal aliases required by this page:
- =ROM_PWD_L

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a
BootROM part number. Must use a
TABLE_x_ITEM symbol to declare
U7100 part number.



BootROM

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE: NONE

SHT 71 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI_CLK_SLOTA	CLOCK	CLOCK	
PCI_CLK_SLOTD	CLOCK	CLOCK	
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK	
	I2_FBCLK	I2_FBCLK	
PCI_AD16_0	PCI	PCI	
PCI_AD17	PCI	PCI	
PCI_AD19_18	PCI	PCI	
PCI_AD20	PCI	PCI	
PCI_AD21	PCI	PCI	
PCI_AD23_22	PCI	PCI	
PCI_AD31_24	PCI	PCI	
PCI_CBE	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_PAR	PCI	PCI	
	PCI	PCI	
	PCI	PCI	
	PCI	PCI	
	PCI	PCI	

TP_PCI_CLK33M_SLOTA_R 11 59
TP_PCI_CLK33M_SLOTD_R 11 59
I2_PCI_FBCLK_OUT_R 59
I2_PCI_FBCLK_OUT 21 59
PCI_AD<16..0> 58 59 60 61 62 (BOOTROM ADDR)
PCI_AD<17> 11 58 59 60 61 (BOOTROM ADDR/SLOT A IDSEL)
PCI_AD<19..18> 58 59 60 61 62 (BOOTROM ADDR)
PCI_AD<20> 11 58 59 60 61 62 (SLOT D IDSEL)
PCI_AD<21> 11 59 60 61 62 (SLOT E IDSEL)
PCI_AD<23..22> 59 60 61 62 (PCI ONLY)
PCI_AD<31..24> 58 59 60 61 62 (BOOTROM DATA)
PCI_CBE_L<3..0> 59 60 61 62
PCI_FRAME_L 6 59 60 61 62
PCI_DEVSEL_L 59 60 61 62
PCI_IRDY_L 6 59 60 61 62
PCI_TRDY_L 6 59 60 61 62
PCI_STOP_L 6 59 60 61 62
PCI_PAR 59 60 61 62
PCI_SLOTA_REQ_L 11 59
PCI_SLOTA_GNT_L 11 59
PCI_SLOTD_REQ_L 11 59
PCI_SLOTD_GNT_L 11 59

Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
- =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
(NONE)

OMIT
U2100
I2
BGA
PCI/ROM INTERFACE
(10 of 14)

ROM INTERFACE
ROM_CS_L AP33 → ROM_CS_L 58 60
ROM_OE_L AM31 → ROM_OE_L 58 60
ROM_WE_L AN34 → ROM_WE_L 58 60

PCI DEVICE 0
PCI_CLK_0_H AL25 → TP_PCI_CLK33M_SLOTA_R 11 59
59 11 PCI_SLOTA_REQ_L → AR21 PCI_REQ_0_L
"Slot A" - AD17
PCI_GNT_0_L AL19 → PCI_SLOTA_GNT_L 11 59

PCI DEVICE 1
PCI_CLK_1_H AR27 → TP_PCI_CLK33M_SLOTD_R 11 59
59 11 PCI_SLOTD_REQ_L → AT20 PCI_REQ_1_L
"Slot D" - AD20
PCI_GNT_1_L AN21 → PCI_SLOTD_GNT_L 11 59

PCI INTERFACE
62 61 60 59 PCI_PAR ↔ AP28 PCI_PAR_H
62 61 60 59 6 PCI_FRAME_L ↔ AT24 PCI_FRAME_L
62 61 60 59 6 PCI_TRDY_L ↔ AN24 PCI_TRDY_L
62 61 60 59 6 PCI_IRDY_L ↔ AR25 PCI_IRDY_L
62 61 60 59 6 PCI_STOP_L ↔ AP27 PCI_STOP_L
62 61 60 59 PCI_DEVSEL_L ↔ AM25 PCI_DEVSEL_L

PCI_AD_00_H AP31 ↔ PCI_AD<0> 58 59 60 61 62
PCI_AD_01_H AT32 ↔ PCI_AD<1> 58 59 60 61 62
PCI_AD_02_H AT31 ↔ PCI_AD<2> 58 59 60 61 62
PCI_AD_03_H AP30 ↔ PCI_AD<3> 58 59 60 61 62
PCI_AD_04_H AN28 ↔ PCI_AD<4> 58 59 60 61 62
PCI_AD_05_H AT34 ↔ PCI_AD<5> 58 59 60 61 62
PCI_AD_06_H AN30 ↔ PCI_AD<6> 58 59 60 61 62
PCI_AD_07_H AR31 ↔ PCI_AD<7> 58 59 60 61 62
PCI_CBE_0_L AR30 ↔ PCI_CBE_L<0> 59 60 61 62

PCI_AD_08_H AM27 ↔ PCI_AD<8> 58 59 60 61 62
PCI_AD_09_H AM30 ↔ PCI_AD<9> 58 59 60 61 62
PCI_AD_10_H AT28 ↔ PCI_AD<10> 58 59 60 61 62
PCI_AD_11_H AT30 ↔ PCI_AD<11> 58 59 60 61 62
PCI_AD_12_H AN27 ↔ PCI_AD<12> 58 59 60 61 62
PCI_AD_13_H AT27 ↔ PCI_AD<13> 58 59 60 61 62
PCI_AD_14_H AN25 ↔ PCI_AD<14> 58 59 60 61 62
PCI_AD_15_H AR28 ↔ PCI_AD<15> 58 59 60 61 62
PCI_CBE_1_L AT29 ↔ PCI_CBE_L<1> 59 60 61 62

PCI_AD_16_H AP25 ↔ PCI_AD<16> 58 59 60 61 62
PCI_AD_17_H AL22 ↔ PCI_AD<17> 11 58 59 60 61 62
PCI_AD_18_H AT26 ↔ PCI_AD<18> 58 59 60 61 62
PCI_AD_19_H AP24 ↔ PCI_AD<19> 58 59 60 61 62
PCI_AD_20_H AR24 ↔ PCI_AD<20> 11 58 59 60 61 62
PCI_AD_21_H AT25 ↔ PCI_AD<21> 11 59 60 61 62
PCI_AD_22_H AK22 ↔ PCI_AD<22> 59 60 61 62
PCI_AD_23_H AT23 ↔ PCI_AD<23> 59 60 61 62
PCI_CBE_2_L AM24 ↔ PCI_CBE_L<2> 59 60 61 62

PCI_AD_24_H AM21 ↔ PCI_AD<24> 58 59 60 61 62
PCI_AD_25_H AP22 ↔ PCI_AD<25> 58 59 60 61 62
PCI_AD_26_H AN22 ↔ PCI_AD<26> 58 59 60 61 62
PCI_AD_27_H AR22 ↔ PCI_AD<27> 58 59 60 61 62
PCI_AD_28_H AK21 ↔ PCI_AD<28> 58 59 60 61 62
PCI_AD_29_H AL21 ↔ PCI_AD<29> 58 59 60 61 62
PCI_AD_30_H AT22 ↔ PCI_AD<30> 58 59 60 61 62
PCI_AD_31_H AP21 ↔ PCI_AD<31> 58 59 60 61 62
PCI_CBE_3_L AM22 ↔ PCI_CBE_L<3> 59 60 61 62

21 =I2_PCI_FBCLK_IN → AM28 PCI_FB_CLK_IN_H
PCI_FBCLK_OUT_H AE23 → R7205 33 5% 1/16W MF-LF 402 → 59 I2_PCI_FBCLK_OUT_R
1 2 I2_PCI_FBCLK_OUT 21 59
3.3V IN
3.3V OUT
Output Impedance is about 20 Ohms

PCI PULL-UPS

10 =PP3V3_PCI

One resistor for each of:
- PCI_FRAME_L
- PCI_TRDY_L
- PCI_IRDY_L
- PCI_STOP_L

6 =RP7250P1 — RP7250 10K 5% 1/16W SM-LF (1, 8)
6 =RP7250P2 — RP7250 10K 5% 1/16W SM-LF (2, 7)
6 =RP7250P3 — RP7250 10K 5% 1/16W SM-LF (3, 6)
6 =RP7250P4 — RP7250 10K 5% 1/16W SM-LF (4, 5)

62 61 60 59 PCI_DEVSEL_L — R7252 10K 5% 1/16W MF-LF 402 (1, 2)

22 11 PCI_SLOTA_INT_L — R7253 10K 5% 1/16W MF-LF 402 (1, 2)
22 11 PCI_SLOTD_INT_L — R7254 10K 5% 1/16W MF-LF 402 (1, 2)

One resistor for each of:
- PCI_SLOTA_GNT_L
- PCI_SLOTA_REQ_L
- PCI_SLOTD_GNT_L
- PCI_SLOTD_REQ_L

6 =RP7251P2 — RP7251 10K 5% 1/16W SM-LF (2, 7)
6 =RP7251P1 — RP7251 10K 5% 1/16W SM-LF (1, 8)
6 =RP7251P3 — RP7251 10K 5% 1/16W SM-LF (3, 6)
6 =RP7251P4 — RP7251 10K 5% 1/16W SM-LF (4, 5)

SLOT E REQ/GNT pull-ups
not provided by this page.

I2 PCI Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 72 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

Power aliases required by this page:
- =PP3V3_PCI (802.11g Power)
- =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
- =PCI_CLK33M_AIRPORT (33MHz PCI clock)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =USB_BT_P (Bluetooth USB D+)
- =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

CRITICAL
J7300
CPB7280-1210
M-ST-SM-LF

10	=PP3V3_PWRON_BT	81			=PP3V3_PCI_AIRPORT 10
		1	2	PCI_AD<31>	58 59 61 62
62 61 59 58	PCI_AD<30>	3	4	AIRPORT_CLKRUN_L_PD	
		5	6	TP_AIRPORT_PME_L	
62 61 59 58	PCI_AD<27>	7	8	=PCI_AIRPORT_GNT_L	11
11	=PCI_AIRPORT_REQ_L	9	10		
62 61 59 58	PCI_AD<25>	11	12		
62 61 59 58	PCI_AD<29>	13	14	PCI_AD<24>	58 59 61 62
		15	16	=PCI_AIRPORT_RESET_L	11
62 61 59	PCI_CBE_L<3>	17	18	PCI_AD<28>	58 59 61 62
62 61 59 58	PCI_AD<26>	19	20		
62 61 59	PCI_AD<22>	21	22	PCI_AD<23>	59 61 62
11	=PCI_AIRPORT_IDSEL	23	24		
		25	26	PCI_AD<20>	11 58 59 61 62
62 61 59 58	PCI_AD<19>	27	28	PCI_FRAME_L	6 59 61 62
62 61 59 11	PCI_AD<21>	29	30	PCI_AD<17>	11 58 59 61 62
62 61 59 6	PCI_IRDY_L	31	32		
62 61 59 58	PCI_AD<18>	33	34	PCI_TRDY_L	6 59 61 62
62 61 59	PCI_DEVSEL_L	35	36		
		37	38	PCI_CBE_L<2>	59 61 62
60 11	=PCI_CLK33M_AIRPORT	39	40	PCI_AD<16>	58 59 61 62
62 61 59 6	PCI_STOP_L	41	42		
62 61 59 58	PCI_AD<12>	43	44	NC	
62 61 59	PCI_PAR	45	46		
		47	48	PCI_AD<14>	58 59 61 62
62 61 59 58	PCI_AD<8>	49	50	PCI_AD<13>	58 59 61 62
62 61 59 58	PCI_AD<9>	51	52		
62 61 59	PCI_CBE_L<0>	53	54	PCI_AD<10>	58 59 61 62
		55	56	PCI_AD<15>	58 59 61 62
62 61 59 58	PCI_AD<7>	57	58	TP_AIRPORT_ALT_ANTENNA	
62 61 59 58	PCI_AD<3>	59	60	PCI_CBE_L<1>	59 61 62
62 61 59 58	PCI_AD<6>	61	62	PCI_AD<4>	58 59 61 62
		63	64		
62 61 59 58	PCI_AD<1>	65	66	PCI_AD<11>	58 59 61 62
62 61 59 58	PCI_AD<5>	67	68	ROM_WE_L	58 59
62 61 59 58	PCI_AD<0>	69	70	PCI_AD<2>	58 59 61 62
11	USB_BT_P	71	72		
11	USB_BT_N	73	74	=PCI_AIRPORT_INT_L	11
		75	76	ROM_OE_L	58 59
		77	78	ROM_ONBOARD_CS_L	58
		79	80	ROM_CS_L	58 59
		82			

R7300
22
5%
1/16W
MF-LF
402
11 =PCI_AIRPORT_IDSEL 1 2

R7305
10K
5%
1/16W
MF-LF
402
1 2

Q85 Connector
Q16C/516S0361/F-ST-SM
Q41C/516S0352/M-ST-SM-LF

Q85 AIRPORT/BT CONN

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT	OF
NONE	73	115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	CLOCK	CLOCK	

=PCI_CLK33M_CBUS 11 61

10 =PP3V3_RUN_PCI1510_R

R7400 0 5% 1/10W MF-LF 603

61 PP3V3_RUN_PCI1510 VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C7400 10UF 20% 6.3V X5R 603
C7401 10UF 20% 6.3V X5R 603
C7402 0.22UF 10% 6.3V CERM-X5R 402
C7403 0.22UF 10% 6.3V CERM-X5R 402
C7404 0.22UF 10% 6.3V CERM-X5R 402
C7405 0.22UF 10% 6.3V CERM-X5R 402
C7406 0.22UF 10% 6.3V CERM-X5R 402
C7407 0.22UF 10% 6.3V CERM-X5R 402
C7408 0.22UF 10% 6.3V CERM-X5R 402

R7410 10K 5% 1/10W MF-LF 402

10 =PP2V5_RUN_PCI1510

C7410 4.7uF 20% 6.3V CERM 805
C7411 0.22UF 10% 6.3V CERM-X5R 402

A7 C13 D5 E1 M1 N7 N11
VCC

10 =PPBV_PWRON_TPS2211
10 =PP3V3_PWRON_TPS2211

10 =TPS2211_SHDN_L

R7450 0 5% 1/10W MF-LF 402

TPS2211_SHTDWN_L

U7450 TPS2211

NC 9	V_12	SSOI	AVPP 10
5	V_5_1		
6	V_5_2	AVCC0	11
3	V_3_1	AVCC1	12
4	V_3_2	AVCC2	13
1	VCCD0		
2	VCCD1		
15	VPPD0		
14	VPPD1		
16	SHTDWN		
7	GND	OC	8 NC

C7450 0.1uF 20% 10V CERM 402
C7451 0.1uF 20% 10V CERM 402

PPVPP_CBUS_SW 61 VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
PPVCC_CBUS_SW 61 VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON PPVCC_CBUS_SW

C7490 2.2uF 10% 6.3V X5R 603
C7491 2.2uF 10% 6.3V X5R 603

U7400 PCI1510ZGU BGA-LF

NC H10	CLK_48_RSVD/NC		
PCI1510_VR_EN_L D4	VR_EN*	CRITICAL	CLAMP FOR PC-CARD VCCCB B11
L8	VR_PORT	CLAMP FOR PCI	VCCP L3
62 60 59 58 PCI_AD<0> N8	AD0	VCCD0* N13	CBUS_VCCD0_L
62 60 59 58 PCI_AD<1> M7	AD1	VCCD1* L12	CBUS_VCCD1_L
62 60 59 58 PCI_AD<2> L7	AD2		
62 60 59 58 PCI_AD<3> N6	AD3	VPPD0 K9	CBUS_VPPD0
62 60 59 58 PCI_AD<4> K4	AD4	VPPD1 M11	CBUS_VPPD1
62 60 59 58 PCI_AD<5> M6	AD5		
62 60 59 58 PCI_AD<6> L6	AD6	CD1*/CCD1* L13	CBUS_DET_1_L 61
62 60 59 58 PCI_AD<7> N5	AD7	CD2*/CCD2* B5	CBUS_DET_2_L 61
62 60 59 58 PCI_AD<8> N4	AD8	IORD*/CAD13 F12	CBUS_IORD_L 61
62 60 59 58 PCI_AD<9> M2	AD9	IOWR*/CAD15 C11	CBUS_IOWR_L 61
62 60 59 58 PCI_AD<10> M5	AD10	OE*/CAD11 G10	CBUS_OE_L 61
62 60 59 58 PCI_AD<11> L4	AD11	CE1*/CC/BE0* H13	CBUS_CE1_L 61
62 60 59 58 PCI_AD<12> N3	AD12	VS1*/CVS1 B2	CBUS_VS1 61
62 60 59 58 PCI_AD<13> K5	AD13	VS2*/CVS2 A9	CBUS_VS2 61
62 60 59 58 PCI_AD<14> L5	AD14	WE*/CGNT* D13	CBUS_WE_L 61
62 60 59 58 PCI_AD<15> M4	AD15	RDY/IREQ*/CINT* A6	CBUS_READY 61
62 60 59 58 PCI_AD<16> J4	AD16	RESET/CRST* D8	CBUS_RESET_L 61
62 60 59 58 11 PCI_AD<17> H1	AD17	REG*/CC/BE3* A8	CBUS_REG_L 61
62 60 59 58 PCI_AD<18> H3	AD18	BVD1/CSTSCHG/STSCHG*/RI* C6	CBUS_BVD1_L 61
62 60 59 58 PCI_AD<19> H2	AD19	BVD2/SPKR*/CAUDIO D6	CBUS_BVD2_L 61
62 60 59 58 11 PCI_AD<20> G2	AD20	INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN* A5	CBUS_WP_L 61
62 60 59 11 PCI_AD<21> G4	AD21	CE2/CAD10* G13	CBUS_CE2_L 61
62 60 59 PCI_AD<22> F1	AD22	INPACK/CREQ* B8	CBUS_INPACK_L 61
62 60 59 PCI_AD<23> C3	AD23	WAIT/CSERR* B6	CBUS_WAIT_L 61
62 60 59 58 PCI_AD<24> F3	AD24		
62 60 59 58 PCI_AD<25> E2	AD25	A0/CAD26 C7	CBUS_ADDR<0> 61
62 60 59 58 PCI_AD<26> F4	AD26	A1/CAD25 D7	CBUS_ADDR<1> 61
62 60 59 58 PCI_AD<27> B1	AD27	A2/CAD24 B7	CBUS_ADDR<2> 61
62 60 59 58 PCI_AD<28> D2	AD28	A3/CAD23 D10	CBUS_ADDR<3> 61
62 60 59 58 PCI_AD<29> E4	AD29	A4/CAD22 B12	CBUS_ADDR<4> 61
62 60 59 58 PCI_AD<30> D3	AD30	A5/CAD21 C8	CBUS_ADDR<5> 61
62 60 59 58 PCI_AD<31> E3	AD31	A6/CAD20 C9	CBUS_ADDR<6> 61
		A7/CAD18 A12	CBUS_ADDR<7> 61
62 60 59 PCI_CBE_L<0> K6	C/BE0*	A8/CC/BE1* E11	CBUS_ADDR<8> 61
62 60 59 PCI_CBE_L<1> M3	C/BE1*	A9/CAD14 F11	CBUS_ADDR<9> 61
62 60 59 PCI_CBE_L<2> J2	C/BE2*	A10/CAD9 G11	CBUS_ADDR<10> 61
62 60 59 PCI_CBE_L<3> A1	C/BE3*	A11/CAD12 G12	CBUS_ADDR<11> 61
		A12/CC/BE2* D9	CBUS_ADDR<12> 61
62 60 59 PCI_PAR N1	PAR	A13/CPAR E12	CBUS_ADDR<13> 61
62 60 59 6 PCI_IRDY_L K1	IRDY	A14/CPERR* D12	CBUS_ADDR<14> 61
61 PCI_SERR_L L2	SERR	A15/CIRDY* C10	CBUS_ADDR<15> 61
PCI_CBUS_IDSEL F2	IDSEL	A16/CCLK B13	CBUS_ADDR_16_R
61 PCI_PERR_L K3	PERR	A17/CAD16 F10	CBUS_ADDR<17> 61
62 60 59 6 PCI_FRAME_L J1	FRAME	A18/RSVD E13	CBUS_ADDR<18> 61
62 60 59 6 PCI_STOP_L L1	STOP	A19/CBLOCK* A13	CBUS_ADDR<19> 61
62 60 59 6 PCI_TRDY_L J3	TRDY	A20/CSTOP* E10	CBUS_ADDR<20> 61
62 60 59 PCI_DEVSEL_L K2	DEVSEL	A21/CDEVSEL* D11	CBUS_ADDR<21> 61
PCI_CBUS_RESET_L M1	PRST	A22/CTRDY* C12	CBUS_ADDR<22> 61
11 =PCI_CBUS_REQ_L C2	REQ	A23/CFRAME* A10	CBUS_ADDR<23> 61
11 =PCI_CBUS_GNT_L C1	GNT	A24/CAD17 B10	CBUS_ADDR<24> 61
61 11 =PCI_CLK33M_CBUS J1	PCLK	A25/CAD19 B9	CBUS_ADDR<25> 61
		D0/CAD27 A4	CBUS_DATA<0> 61
NC M9	SPKROUT	D1/CAD29 C4	CBUS_DATA<1> 61
NC M8	RI_OUT/PME	D2/RSVD A3	CBUS_DATA<2> 61
61 CBUS_SUSPEND_PU M10	SUSPEND	D3/CAD0 K11	CBUS_DATA<3> 61
		D4/CAD1 K12	CBUS_DATA<4> 61
11 =PCI_CBUS_INT_L K7	MFUNC0	D5/CAD3 J13	CBUS_DATA<5> 61
61 CBUS_MFUNC1_PD N9	MFUNC1	D6/CAD5 J10	CBUS_DATA<6> 61
61 CBUS_MFUNC2_PD L9	MFUNC2	D7/CAD7 H12	CBUS_DATA<7> 61
61 CBUS_MFUNC3_PD K10	MFUNC3	D8/CAD28 C5	CBUS_DATA<8> 61
61 CBUS_MFUNC4_PD M10	MFUNC4	D9/CAD30 B4	CBUS_DATA<9> 61
61 CBUS_MFUNC5_PD N12	MFUNC5	D10/CAD31 B3	CBUS_DATA<10> 61
61 CBUS_MFUNC6_PD L10	MFUNC6	D11/CAD2 M12	CBUS_DATA<11> 61
		D12/CAD4 J11	CBUS_DATA<12> 61
L11	GRST	D13/CAD6 K13	CBUS_DATA<13> 61
		D14/RSVD J12	CBUS_DATA<14> 61
		D15/CAD8 H11	CBUS_DATA<15> 61

GND
A2 A11 D1 F13 H4 K8 M13 N2

R7424 47 5% 1/16W MF-LF 402
11 =PCI_CBUS_RESET_L

R7423 22 5% 1/16W MF-LF 402
11 =PCI_CBUS_IDSEL

R7430 47 5% 1/16W MF-LF 402
CBUS_ADDR<16> 61

PCI1510 PULL-UPS

PP3V3_RUN_PCI1510 61

R7420 10K 5% 1/16W MF-LF 402 — PCI_PERR_L 61
R7421 10K 5% 1/16W MF-LF 402 — PCI_SERR_L 61
R7422 10K 5% 1/16W MF-LF 402 — CBUS_SUSPEND_PU 61

RP7410 10K 5% SM-LF
1 CBUS_MFUNC5_PD 61
2 CBUS_MFUNC6_PD 61
3 CBUS_MFUNC3_PD 61
4 CBUS_MFUNC1_PD 61
8 7 6 5

R7411 10K 5% 1/16W MF-LF 402 — CBUS_MFUNC4_PD 61
R7412 10K 5% 1/16W MF-LF 402 — CBUS_MFUNC2_PD 61

PC CARD/CARDBUS CONNECTOR

CRITICAL
J7490 QT500806-L121-9F M-ST-SM

	84	81	
	2	1	CBUS_DATA<3> 61
61 CBUS_DET_1_L	4	3	CBUS_DATA<4> 61
61 CBUS_DATA<11>	6	5	CBUS_DATA<5> 61
61 CBUS_DATA<12>	8	7	CBUS_DATA<6> 61
61 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 61
61 CBUS_DATA<14>	14	13	CBUS_CE1_L 61
61 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 61
61 CBUS_CE2_L	18	17	CBUS_OE_L 61
61 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 61
61 CBUS_IORD_L	24	23	CBUS_ADDR<9> 61
61 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 61
61 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 61
61 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 61
61 CBUS_ADDR<19>	34	33	CBUS_WE_L 61
61 CBUS_ADDR<20>	36	35	CBUS_READY 61
61 CBUS_ADDR<21>	38	37	PPVCC_CBUS_SW 61
61 PPVCC_CBUS_SW	40	39	
	42	41	PPVPP_CBUS_SW 61
61 PPVPP_CBUS_SW	44	43	CBUS_ADDR<16> 61
61 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 61
61 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 61
61 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 61
61 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 61
61 CBUS_VS2	56	55	CBUS_ADDR<5> 61
61 CBUS_RESET_L	58	57	CBUS_ADDR<4> 61
61 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 61
61 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 61
61 CBUS_REG_L	66	65	CBUS_ADDR<1> 61
61 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 61
61 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 61
61 CBUS_DATA<8>	74	73	CBUS_DATA<1> 61
61 CBUS_DATA<9>	76	75	CBUS_DATA<2> 61
61 CBUS_DATA<10>	78	77	CBUS_WP_L 61
61 CBUS_DET_2_L	80	79	
	83	82	

Cardbus

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 74 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

Power aliases required by this page:
- =PPVIO_PCI (to 3.3V or 5V)
- =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
- =PCI_CLK33M_USB2
- =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
- =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
- =PCI_USB2_INT_L

BOM options provided by this page:
- USB2_NEC

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

10 =PPVIO_PCI_USB2

USB2_NEC C7500 0.1uF 20% 10V CERM 402

VDD_PCI

USB2_NEC CRITICAL U7500 NEC_uPD720101_USB2 FBGA-LF

61 60 59 58 PCI_AD<0>	M5	AD0	
61 60 59 58 PCI_AD<1>	P5	AD1	
61 60 59 58 PCI_AD<2>	N5	AD2	
61 60 59 58 PCI_AD<3>	P4	AD3	
61 60 59 58 PCI_AD<4>	N4	AD4	
61 60 59 58 PCI_AD<5>	M3	AD5	
61 60 59 58 PCI_AD<6>	N3	AD6	
61 60 59 58 PCI_AD<7>	M1	AD7	
61 60 59 58 PCI_AD<8>	L2	AD8	
61 60 59 58 PCI_AD<9>	L1	AD9	
61 60 59 58 PCI_AD<10>	K2	AD10	
61 60 59 58 PCI_AD<11>	L3	AD11	
61 60 59 58 PCI_AD<12>	K1	AD12	
61 60 59 58 PCI_AD<13>	K3	AD13	
61 60 59 58 PCI_AD<14>	J2	AD14	
61 60 59 58 PCI_AD<15>	J1	AD15	
61 60 59 58 PCI_AD<16>	F2	AD16	
61 60 59 58 11 PCI_AD<17>	E3	AD17	
61 60 59 58 PCI_AD<18>	E1	AD18	
61 60 59 58 PCI_AD<19>	D3	AD19	
61 60 59 58 11 PCI_AD<20>	D1	AD20	
61 60 59 11 PCI_AD<21>	D2	AD21	
61 60 59 PCI_AD<22>	C2	AD22	
61 60 59 PCI_AD<23>	C1	AD23	
61 60 59 58 PCI_AD<24>	B4	AD24	
61 60 59 58 PCI_AD<25>	A4	AD25	
61 60 59 58 PCI_AD<26>	B5	AD26	
61 60 59 58 PCI_AD<27>	C4	AD27	
61 60 59 58 PCI_AD<28>	A5	AD28	
61 60 59 58 PCI_AD<29>	C5	AD29	
61 60 59 58 PCI_AD<30>	B6	AD30	
61 60 59 58 PCI_AD<31>	A6	AD31	
61 60 59 PCI_CBE_L<0>	M2	CBE0	
61 60 59 PCI_CBE_L<1>	J3	CBE1	
61 60 59 PCI_CBE_L<2>	F1	CBE2	
61 60 59 PCI_CBE_L<3>	C3	CBE3	
61 60 59 PCI_PAR	J4	PAR	
61 60 59 6 PCI_FRAME_L	F3	FRAME	
61 60 59 6 PCI_IRDY_L	F4	IRDY	
61 60 59 6 PCI_TRDY_L	G1	TRDY	
61 60 59 6 PCI_STOP_L	G3	STOP	
PCI_USB2_IDSEL	B3	IDSEL	
61 60 59 PCI_DEVSEL_L	G2	DEVSEL	
11 =PCI_USB2_REQ_L	C6	REQ	
11 =PCI_USB2_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR OD	
NEC_INTA_L	C7	INTA OD	
NEC_INTB_L	B7	INTB OD	
NEC_INTC_L	A7	INTC OD	
62 11 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D9	PME OD	
NEC_VCCRST_L	C9	VCCRST(PCI RESET)	
TP_NEC_SMI_L	L6	SMI OD	
NEC_LEGC_PD	L7	LEGC	

IPD NTEST1	M8	TP_NEC_NTEST1	
IPD SMC	M7	TP_NEC_SMC	
IPD TEB	N7	TP_NEC_TEB	
IPD AMC	P7	TP_NEC_AMC	
IPD TEST	L8	TP_NEC_TEST	
NANDTEST	M10	TP_NEC_NANDTEST	
SRCLK	M9	TP_NEC_SRCLK	
SRDTA	N9	TP_NEC_SRDATA	
IPD SRMOD	P9	TP_NEC_SRMOD	

11 =PCI_USB2_IDSEL

USB2_NEC R7500 22 5% 1/16W MF-LF 402

16 =PP3V3_PCI_USB2

USB2_NEC R7501 10K 5% 1/16W MF-LF 402

USB2_NEC R7502 10K 5% 1/16W MF-LF 402

USB2_NEC RP7510 47 5% 1/16W SM-LF

USB2_NEC RP7510 47 5% 1/16W SM-LF

USB2_NEC RP7510 47 5% 1/16W SM-LF

11 =PCI_USB2_INT_L

25 22 SYS_WARM_RESET_L

USB2_NEC R7510 47 5% 1/16W MF-LF 402

25 22 SYS_PME_L

USB2_NEC R7511 47 5% 1/16W MF-LF 402

11 =PCI_USB2_RESET_L

USB2_NEC R7512 47 5% 1/16W MF-LF 402

RP7510 & R7510-12 required to facilitate NAND-tree testing

USB2_NEC R7503 4.7K 5% 1/16W MF-LF 402

USB2_NEC R7504 47 5% 1/16W MF-LF 402

NEC USB2

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 75 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
UATA_DD	UATA	UATA	
UATA_DD2	UATA	UATA	
UATA_DD	UATA	UATA	
UATA_HOST	UATA	UATA	
UATA_HOST	UATA	UATA	
UATA_HOST	UATA	UATA	
UATA_HSTROBE	UATA	UATA	
UATA_HOST	UATA	UATA	
UATA_HOST_R	UATA	UATA	
UATA_HOST_R	UATA	UATA	
UATA_DSTROBE	UATA	UATA	
UATA_DEV_R	UATA	UATA	
UATA_DEV_R	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	
	UATA	UATA	

UATA_DD R<15..8>	6 63
UATA_DD R<7>	6 63
UATA_DD R<6..0>	6 63
UATA_DA R<2..0>	6 63
UATA_CS0_L_R	6 63
UATA_CS1_L_R	63
UATA_HSTROBE_R	63
UATA_STOP_R	63
UATA_DMACK_L_R	63
UATA_RESET_L_R	63
UATA_DSTROBE_R	63
UATA_DMARQ_R	63
UATA_INTRQ_R	63
UATA_DD<15..0>	6 7 64
UATA_DA<2..0>	6 7 64
UATA_CS0_L	6 7 64
UATA_CS1_L	7 63 64
UATA_HSTROBE	7 63 64
UATA_STOP	7 63 64
UATA_DMACK_L	7 63 64
UATA_RESET_L	7 63 64
UATA_DSTROBE	7 63 64
UATA_DMARQ	7 63 64
UATA_INTRQ	7 63 64

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U2100
I2
BGA
UATA INTERFACE
(11 of 14)

ATA_D_00_H	AB6	UATA_DD R<15..0> 6 63
ATA_D_01_H	AB5	
ATA_D_02_H	AD6	
ATA_D_03_H	AD5	
ATA_D_04_H	AD7	
ATA_D_05_H	AE7	
ATA_D_06_H	AE8	
ATA_D_07_H	AD8	
ATA_D_08_H	AB4	
ATA_D_09_H	AE1	
ATA_D_10_H	AD2	
ATA_D_11_H	AE2	
ATA_D_12_H	AD4	
ATA_D_13_H	AA6	
ATA_D_14_H	AD1	
ATA_D_15_H	AB7	
ATA_A_0_H	AC1	UATA_DA R<2..0> 6 63
ATA_A_1_H	AB3	
ATA_A_2_H	AB2	
ATA_RST_L	AE6	UATA_RESET_L_R 63
ATA_WR_L	AB8	UATA_STOP_R 63
ATA_RD_L	AA8	UATA_HSTROBE_R 63
ATA_CS0_L	AE3	UATA_CS0_L_R 6 63
ATA_CS1_L	AA4	UATA_CS1_L_R 63
ATA_DMACK_L	AA7	UATA_DMACK_L_R 63
ATA_VREF_H	AA9	I2_UATA_VREF
ATA_CHRDY_H	AA5	UATA_DSTROBE_R 63
ATA_INTRQ_H	AB1	UATA_INTRQ_R 63
ATA_DMARQ_H	Y9	UATA_DMARQ_R 63

R8100 1K 1% 1/16W MF-LF 402
R8151 10K 5% 1/16W MF-LF 402

UATA100 SERIES TERMINATION

PLACE CLOSE TO I2

One resistor for each of:
- UATA_DD<15..0>(_R)
- UATA_DA<2..0>(_R)
- UATA_CS0_L(_R)
- UATA_CS1_L(_R)

RP8150	=RP8150P1	=RP8150P8 BI 6
RP8150	=RP8150P2	=RP8150P7 BI 6
RP8150	=RP8150P3	=RP8150P6 BI 6
RP8150	=RP8150P4	=RP8150P5 BI 6
RP8151	=RP8151P1	=RP8151P8 BI 6
RP8151	=RP8151P2	=RP8151P7 BI 6
RP8151	=RP8151P3	=RP8151P6 BI 6
RP8151	=RP8151P4	=RP8151P5 BI 6
RP8152	=RP8152P1	=RP8152P8 BI 6
RP8152	=RP8152P2	=RP8152P7 BI 6
RP8152	=RP8152P3	=RP8152P6 BI 6
RP8152	=RP8152P4	=RP8152P5 BI 6
RP8153	=RP8153P1	=RP8153P8 BI 6
RP8153	=RP8153P2	=RP8153P7 BI 6
RP8153	=RP8153P3	=RP8153P6 BI 6
RP8153	=RP8153P4	=RP8153P5 BI 6
RP8154	=RP8154P1	=RP8154P8 OUT 6
RP8154	=RP8154P2	=RP8154P7 OUT 6
RP8154	=RP8154P3	=RP8154P6 OUT 6
RP8154	=RP8154P4	=RP8154P5 OUT 6

All RP8150–RP8154: 33, 5%, 1/16W, SM-LF

R8160	UATA_CS1_L_R 63	UATA_CS1_L OUT 7 63 64
R8161	UATA_RESET_L_R 63	UATA_RESET_L OUT 7 63 64
R8162	UATA_DMACK_L_R 63	UATA_DMACK_L OUT 7 63 64
R8163	UATA_HSTROBE_R 63	UATA_HSTROBE OUT 7 63 64
R8164	UATA_STOP_R 63	UATA_STOP OUT 7 63 64
R8165	UATA_DMARQ_R 63	UATA_DMARQ IN 7 63 64
R8166	UATA_DSTROBE_R 63	UATA_DSTROBE IN 7 63 64
R8167	UATA_INTRQ_R 63	UATA_INTRQ IN 7 63 64

R8160–R8167: 33 / 22 / 82, 5%, 1/16W, MF-LF 402

(IDE_CS3FX_L)
(IDE_CS1FX_L)
(IDE_DIOR_L)
(IDE_DIOW_L)
(IDE_IORDY)

C8166 10pF 5% 50V CERM 402

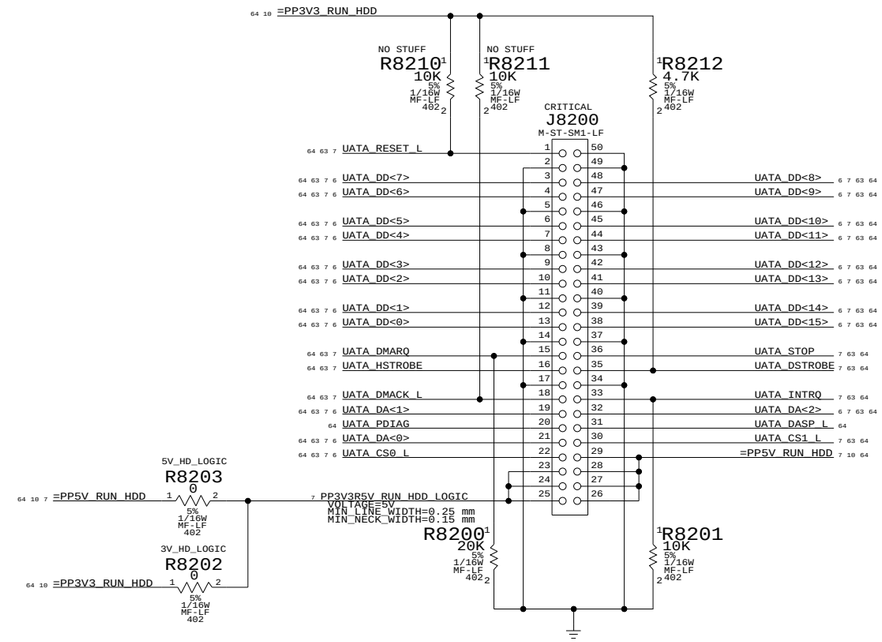
I2 UATA Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

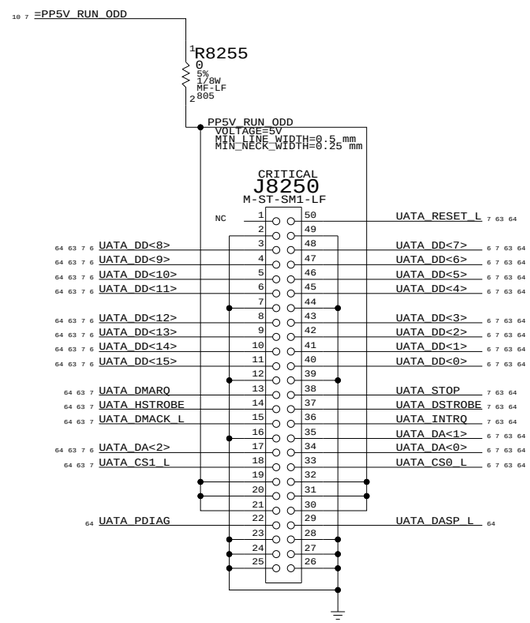
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 81 OF 115	

HDD CONNECTOR



ODD CONNECTOR



ATA Connectors
Q16C/516S0357/M-ST-SM2-LF
Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 82 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ENET_RX_CLK25M	CLOCK	CLOCK	
ENET_RX_CLK125M	CLOCK	CLOCK	
ENET_GBE_REF	CLOCK	CLOCK	
ENET_TX_CLK	CLOCK	CLOCK	
ENET_RXD3_0	ENET	ENET	
ENET_RXD7_4	ENET	ENET	
ENET_RX_DV	ENET	ENET	
ENET_RX_CTL	ENET	ENET	
ENET_TXD3_0	ENET	ENET	
ENET_TXD7_4	ENET	ENET	
ENET_TX_EN	ENET	ENET	
ENET_TX_ER	ENET	ENET	
ENET_COL	ENET	ENET	
ENET_RX_CTL	ENET	ENET	
ENET_MDC	ENET	ENET	
ENET_MDIO	ENET	ENET	
	ENET	ENET	

ENET_CLK25M_TX 11 65
ENET_CLK125M_RX 11 65
ENET_CLK125M_GBE_REF 11 65
ENET_CLK125M_GTX_R 65 66
ENET_RXD<3..0> 9 11 65
ENET_RXD<7..4> 9 11 65
ENET_RX_DV 9 11 65
ENET_RX_ER 9 11 65
ENET_TXD_R<3..0> 11 65
ENET_TXD_R<7..4> 11 65
ENET_TX_EN_R 11 65
ENET_TX_ER_R 11 65
ENET_COL 9 11 65
ENET_CRS 9 11 65
ENET_MDC 9 11 65
ENET_MDIO 9 11 65
I2_ENET_MDIO 65

Page Notes

Power aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.

65 10 =PP2V5R3V3_PWRON_I2_ENET

C8459 10uF 20% 6.3V X5R 603
C8450 1uF 10% 6.3V CERM 402
C8451 1uF 10% 6.3V CERM 402
C8452 1uF 10% 6.3V CERM 402
C8453 1uF 10% 6.3V CERM 402
C8454 1uF 10% 6.3V CERM 402
C8455 1uF 10% 6.3V CERM 402
C8456 1uF 10% 6.3V CERM 402

OMIT
U2100
I2
BGA
ETHERNET INTERFACE
(12 of 14)

U3 VDD25_0
U6 VDD25_1
U9 VDD25_2
V13 VDD25_3
W14 VDD25_4
Y3 VDD25_5
Y6 VDD25_6

65 11 ENET_CLK25M_TX — W7 ETH_TXCLK_H
65 11 ENET_CLK125M_RX — W8 ETH_RXCLK_H

65 11 9 ENET_RXD<0> — W2 ETH_RXD_0_H
65 11 9 ENET_RXD<1> — W3 ETH_RXD_1_H
65 11 9 ENET_RXD<2> — V2 ETH_RXD_2_H
65 11 9 ENET_RXD<3> — U1 ETH_RXD_3_H
65 11 9 ENET_RXD<4> — V3 ETH_RXD_4_H
65 11 9 ENET_RXD<5> — V1 ETH_RXD_5_H
65 11 9 ENET_RXD<6> — T1 ETH_RXD_6_H
65 11 9 ENET_RXD<7> — T3 ETH_RXD_7_H

65 11 9 ENET_RX_DV — W9 ETH_RXDV_H
65 11 9 ENET_RX_ER — W1 ETH_RXER_H

65 11 9 ENET_COL — AA3 ETH_COL_H
65 11 9 ENET_CRS — W5 ETH_CRS_H

65 11 ENET_CLK125M_GBE_REF — AA2 ETH_GREFCLK_H

ENET_ENERGYDET — Signal — Pin — Y1 EXT_05_H

I2_ENET_PVT — U10 ETH_PVT_H

R8400 1K 1% 1/16W MF-LF 402

ETH_MDC_H — W4 — ENET_MDC 9 11 65
ETH_MDIO_H — W6 — 65 I2_ENET_MDIO

ETH_TXD_0_H — V8 — ENET_TXD_R<0> 11 65
ETH_TXD_1_H — V4 — ENET_TXD_R<1> 11 65
ETH_TXD_2_H — V7 — ENET_TXD_R<2> 11 65
ETH_TXD_3_H — V6 — ENET_TXD_R<3> 11 65
ETH_TXD_4_H — V5 — ENET_TXD_R<4> 11 65
ETH_TXD_5_H — T4 — ENET_TXD_R<5> 11 65
ETH_TXD_6_H — T5 — ENET_TXD_R<6> 11 65
ETH_TXD_7_H — T6 — ENET_TXD_R<7> 11 65

ETH_TXEN_H — T7 — ENET_TX_EN_R 11 65
ETH_TXER_H — T8 — ENET_TX_ER_R 11 65

ETH_GTXCLK_H — V9 — ENET_CLK125M_GTX_R 65 66

GPIO_16_H — AA1 — Pin — Signal — ENET_RESET_L 11

These GPIOs are referenced to the Ethernet I/O rail

=PP2V5R3V3_PWRON_I2_ENET 10 65
R8405 1.5K 5% 1/16W MF-LF 402

67 66 18 10 =PP3V3_VESTA
R8420 10K 5% 1/16W MF-LF 402
Q8420 2N7002DW-X-F SOT-363
ENET_MDIO 9 11 65

NO STUFF
R8421 0 5% 1/16W MF-LF 402

I2 Ethernet Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 84 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_GBE_REF_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_RX_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK25M_TX_R 66
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_N 66 67
VESTA_CLK25M_XTAL	XTAL	XTAL		VESTA_CLK25M_XTALI 66
	XTAL	XTAL		VESTA_CLK25M_XTALO 66
	XTAL	XTAL		VESTA_CLK25M_XTALO_R 66

Page Notes

Power aliases required by this page:
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET_MDI

Line To Line:	0.38 mms
Length Tolerance:	50 mils
Primary Max Sep:	5 mils
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr

Disables Vesta Ethernet Circuit

67 65 18 10 =PP3V3_VESTA

10 =PP3V3_ENET

R8580 1K 5% 1/16W MF-LF 402

RC time constant not critical. R < 3.9K to counter internal pulldown.

Q8580 2N7002DW-X-F SOT-363

Q8580 2N7002DW-X-F SOT-363

C8580 0.1uF 20% 10V CERM 402

18 IN VESTA_RESET

Circuit ensures Vesta LOWPWR signal is low when Vesta RESET* is asserted, and allows LOWPWR to assert when ethernet link is unpowered.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

L8520 FERR-EMI-600-OHM SM =PP2V5_ENETFW 10 69

PP2V5_VESTA_XTALVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C8520 0.001uF 20% 50V CERM 402

C8521 10UF 20% 6.3V X5R 603

L8510 FERR-EMI-600-OHM SM

PP2V5_VESTA_BIASVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C8510 0.1uF 20% 10V CERM 402

L8530 FERR-EMI-600-OHM SM =PP1V2_ENETFW 10 69

PP1V2_VESTA_PLLVDD1 VOLTAGE=1.2V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C8530 0.001uF 20% 50V CERM 402

C8531 10UF 20% 6.3V CERM 1206-1

ESR < 0.5 ohms

Place close to link

R8569 0 5% 1/16W MF-LF 402

65 IN ENET_CLK125M_GTX_R — ENET_CLK125M_GTX — A4 GTXCLK

XTALVDD1 BIASVDD1 PLLVDD1

OMIT

VESTA ENET

U8500 BCM5462 FBGA-200 2 OF 3

			CLK125 D1	66 ENET_CLK125M_GBE_REF_R
11 IN =ENET_TXD<0>	B6	TXD[0]	TXC A6	66 ENET_CLK25M_TX_R
11 IN =ENET_TXD<1>	C6	TXD[1]	RXC C1	66 ENET_CLK125M_RX_R
11 IN =ENET_TXD<2>	C7	TXD[2]	RXD[0] F4	=ENET_RXD_R<0> OUT 11
11 IN =ENET_TXD<3>	D6	TXD[3]	RXD[1] F5	=ENET_RXD_R<1> OUT 11
11 IN =ENET_TXD<4>	E6	TXD[4]	RXD[2] E5	=ENET_RXD_R<2> OUT 11
11 IN =ENET_TXD<5>	C5	TXD[5]	RXD[3] E4	=ENET_RXD_R<3> OUT 11
11 IN =ENET_TXD<6>	B5	TXD[6]	RXD[4] E3	=ENET_RXD_R<4> OUT 11
11 IN =ENET_TXD<7>	A5	TXD[7]	RXD[5] D5	=ENET_RXD_R<5> OUT 11
			RXD[6] D4	=ENET_RXD_R<6> OUT 11
			RXD[7] D3	=ENET_RXD_R<7> OUT 11
11 IN =ENET_TX_EN	B4	TX_EN	RX_DV D2	=ENET_RX_DV_R OUT 11
11 IN =ENET_TX_ER	C4	TX_ER	RX_ER C2	=ENET_RX_ER_R OUT 11
11 IN =VESTA_MDC	G1	MDC	COL F3	=ENET_COL_R OUT 11
11 BI =VESTA_MDIO	G2	MDIO	CRS G3	=ENET_CRS_R OUT 11
VESTA_ENET_LOWPWR	H5	LOWPWR	RBC0 A3	NC? TP_VESTA_RBC0
			RBC1 B3	NC? TP_VESTA_RBC1
TP_VESTA_PHYA<0>	L5	PHYA[0]	TRD+[0] R4	ENETCONN_0_P BI 66 67
TP_VESTA_PHYA<1>	L4	PHYA[1]	TRD-[0] R5	ENETCONN_0_N BI 66 67
TP_VESTA_PHYA<2>	L3	PHYA[2]	TRD+[1] R7	ENETCONN_1_P BI 66 67
TP_VESTA_PHYA<3>	L2	PHYA[3]	TRD-[1] R6	ENETCONN_1_N BI 66 67
TP_VESTA_PHYA<4>	L1	PHYA[4]	TRD+[2] R8	ENETCONN_2_P BI 66 67
			TRD-[2] R9	ENETCONN_2_N BI 66 67
TP_VESTA_EN_10B	K3	EN_10B	TRD+[3] R11	ENETCONN_3_P BI 66 67
TP_VESTA_RGMIIEN	B8	RGMIIEN	TRD-[3] R10	ENETCONN_3_N BI 66 67
TP_VESTA_FDX	C8	FDX	INTR*/ENERGYDET D10	=VESTA_ENERGYDET OUT 11
TP_VESTA_F1000	K4	F1000	SLAVE*/AN_EN C10	TP_VESTA_AN_EN
TP_VESTA_SPD0	K5	SPD0	QUALITY*/TXC_RXC_DELAY A8	TP_VESTA_TXC_RXC_DELAY
TP_VESTA_MANMS	D9	MANMS	LINK1* A10	TP_VESTA_LINKSPD1_L
TP_VESTA_HUB	A9	HUB	LINK2* B11	TP_VESTA_LINKSPD2_L
TP_VESTA_ER	H3	ER	FDXLED* B10	TP_VESTA_FDXLED_L
			XMTLED* B12	TP_VESTA_XMTLED_L
TP_VESTA_TEST<0>	M4	TEST[0]	ACTLED* A11	TP_VESTA_ACTLED_L
TP_VESTA_TEST<1>	M5	TEST[1]	RDAC1 R1	VESTA_RDAC1_PD
TP_VESTA_TVCO	N3	TVCO		
VESTA_CLK25M_XTALI	N2	XTALI		
VESTA_CLK25M_XTALO_R	P2	XTALO		

XTALGND BIASGND PLLGND1

R8509 1.24K 1% 1/16W MF-LF 402

Place close to PHY

R8560 0 5% 1/16W MF-LF 402 — =VESTA_CLK125M_GBE_REF OUT 11

R8561 0 5% 1/16W MF-LF 402 — =VESTA_CLK25M_TX OUT 11

R8562 0 5% 1/16W MF-LF 402 — =VESTA_CLK125M_RX OUT 11

I2BORG SPECIFIC

Not convention-compliant, '=VESTA_' should be replaced with 'ENET_' (6 nets)

Put crystal circuit close to PHY

66 VESTA_CLK25M_XTALI

66 VESTA_CLK25M_XTALO_R

R8501 0 5% 1/16W MF-LF 402

CRITICAL Y8500 25.0000M 8X4.5MM-SM2

VESTA_CLK25M_XTALO 66

C8500 33pF 5% 50V CERM 402

C8501 33pF 5% 50V CERM 402

CRYSTAL LOAD CAPACITANCE IS 20PF

R8590 49.9 1% 1/16W MF-LF 402 — ENET_MDI0

R8591 49.9 1% 1/16W MF-LF 402

R8592 49.9 1% 1/16W MF-LF 402 — ENET_MDI1

R8593 49.9 1% 1/16W MF-LF 402

R8594 49.9 1% 1/16W MF-LF 402 — ENET_MDI2

R8595 49.9 1% 1/16W MF-LF 402

R8596 49.9 1% 1/16W MF-LF 402 — ENET_MDI3

R8597 49.9 1% 1/16W MF-LF 402

C8590 0.01UF 20% 16V CERM 402

C8592 0.01UF 20% 16V CERM 402

C8594 0.01UF 20% 16V CERM 402

C8596 0.01UF 20% 16V CERM 402

PLACE RESISTORS CLOSE TO PHY

Vesta Ethernet PHY

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 85 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PROVIDED BY ETHERNET PHY	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_P
	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_N
	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_P
	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_N
	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_P
	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_N
	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_P
	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_N

Page Notes

Power aliases required by this page:
- _PP2V5_ENET
- _GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

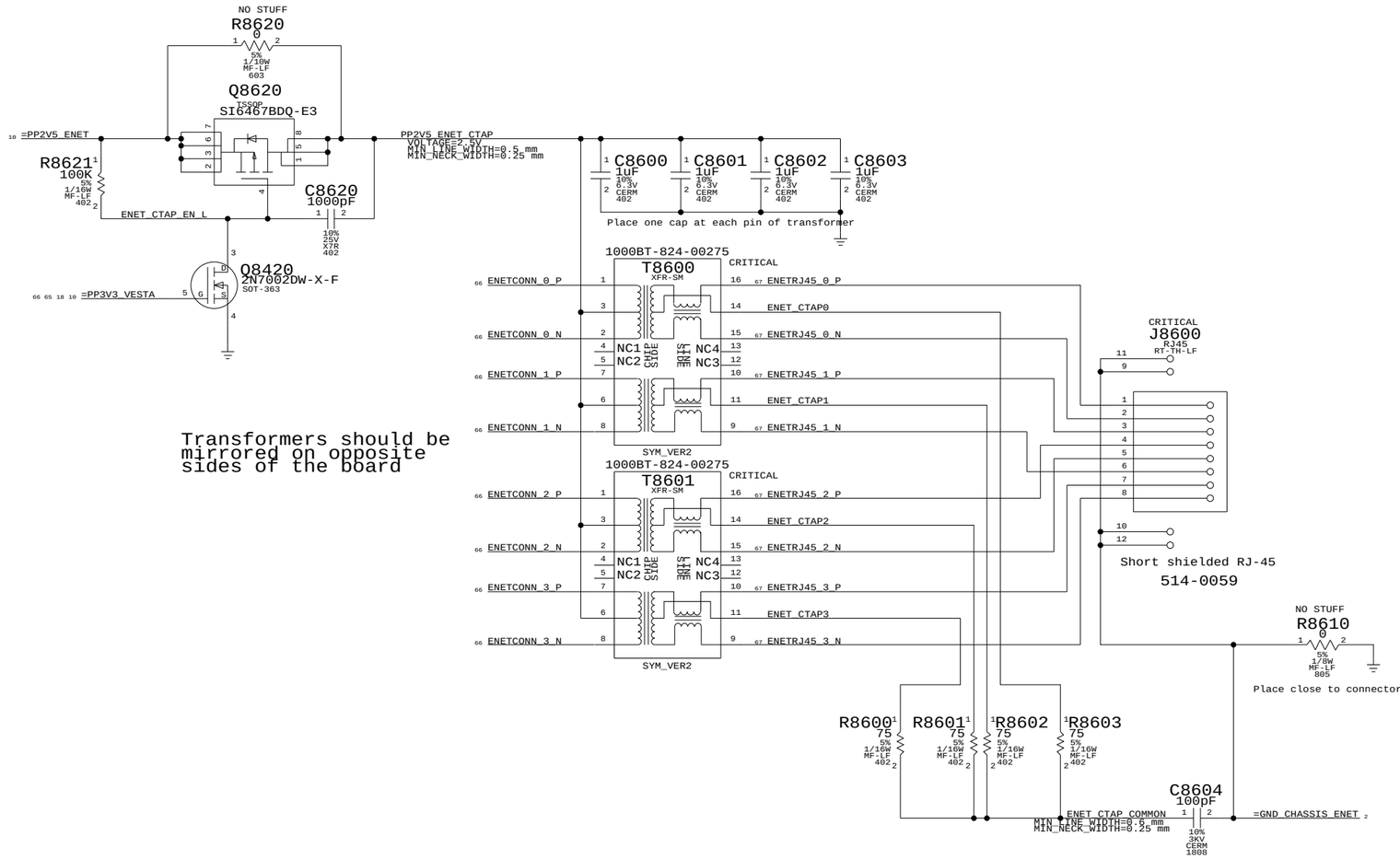
BOM options provided by this page:
(NONE)

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



Transformers should be mirrored on opposite sides of the board

Ethernet Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 86 OF 115	

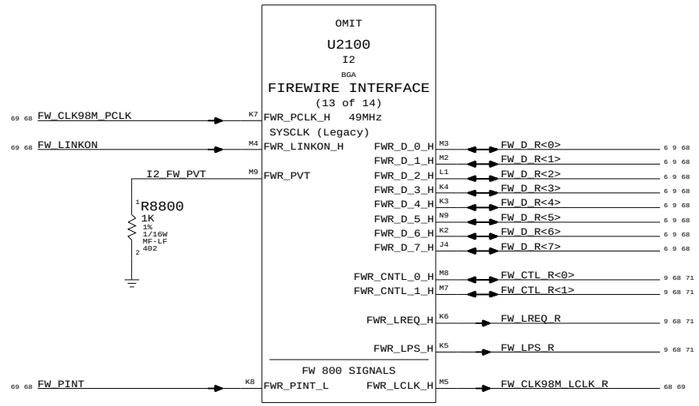
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FW_D	FW	FW		FW_D_R<7..0>	6 9 68
FW_CTL	FW	FW		FW_CTL_R<1..0>	9 68 71
FW_LREQ	FW	FW		FW_LREQ_R	9 68 71
	FW	FW		FW_LPS_R	9 68 71
	FW	FW		FW_LINKON	68 69
FW_PCLK	CLOCK	CLOCK		FW_CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW_CLK98M_LCLK_R	68 69
FW_PINT	FW	FW		FW_PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 88 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		FW_CLK98M_PCLK_R 69
	CLOCK	CLOCK		FW_CLK98M_LCLK 69
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_P 69 70
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_N 69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_P 69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_N 69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_P 69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_N 69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_P 69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_N 69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_P 69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_N 69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_P 69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_N 69 70
VESTA_CLK24M_XTAL	XTAL	XTAL		VESTA_CLK24M_XTALI 69
	XTAL	XTAL		VESTA_CLK24M_XTALO 69
	XTAL	XTAL		VESTA_CLK24M_XTALO_R 69

Page Notes

Power aliases required by this page:
- =PPFW_PHY_CPS
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
- NONE

BOM options provided by this page:
- VESTA_BILINGUAL_EN12
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PORT1_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PORT2_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

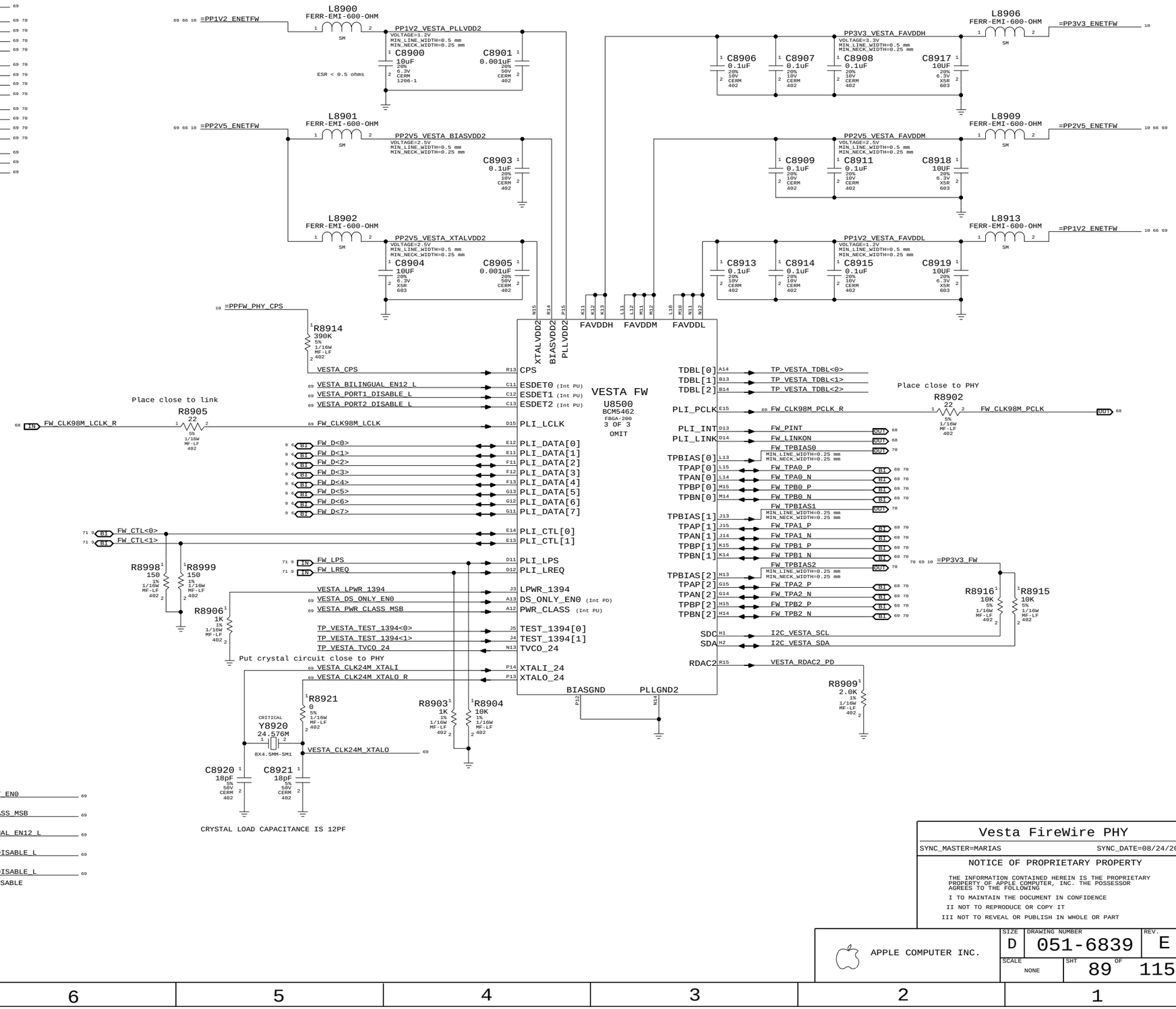
Net Spacing Type: FW_TP

Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

DS_ONLY_EN12 - Port 1&2 Data/Strobe
1 - Port 1&2 Data/Strobe mode only
0 - Port 1&2 Bilingual mode
(Internal Pull-up)
DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)
PORT1_ENABLE - Port 1 Enable
1 - Port 1 Enabled
0 - Port 1 Disabled (saves power)
(Internal Pull-up)
PORT2_ENABLE - Port 2 Enable
1 - Port 2 Enabled
0 - Port 2 Disabled (saves power)
(Internal Pull-up)
PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)



Vesta FireWire PHY

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 89 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED BY PHY PAGE	FW	FW	FW_PORT1_TPA_FL
	FW	FW	FW_PORT1_TPA_FL
	FW	FW	FW_PORT1_TPB_FL
	FW	FW	FW_PORT1_TPB_FL
	FW	FW	FW_PORT2_TPA_FL
	FW	FW	FW_PORT2_TPA_FL
	FW	FW	FW_PORT2_TPB_FL
	FW	FW	FW_PORT2_TPB_FL

FW_PORT1_TPA_P_FL
FW_PORT1_TPA_N_FL
FW_PORT1_TPB_P_FL
FW_PORT1_TPB_N_FL
FW_PORT2_TPA_P_FL
FW_PORT2_TPA_N_FL
FW_PORT2_TPB_P_FL
FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

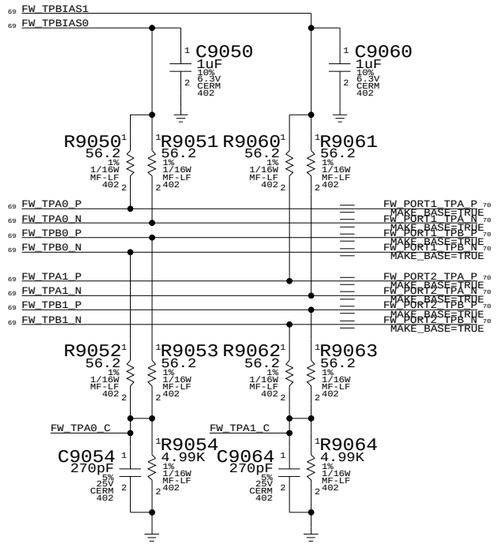
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

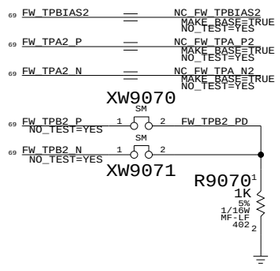
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

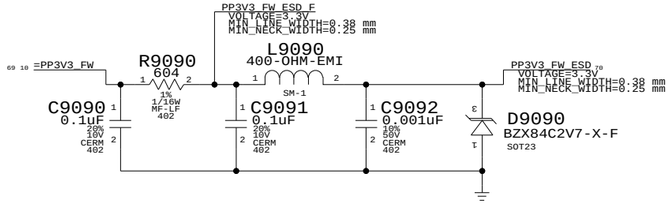
Place close to FireWire PHY



3rd TPA/TPB pair unused

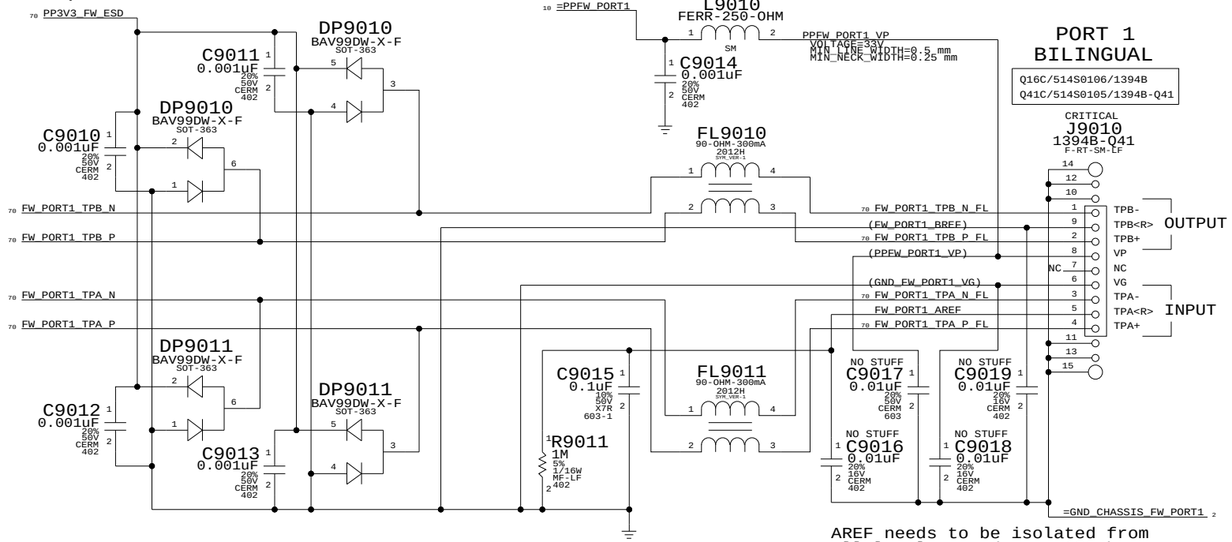


ESD Rail



Cable Power

"Snapback" & "Late VG" Protection

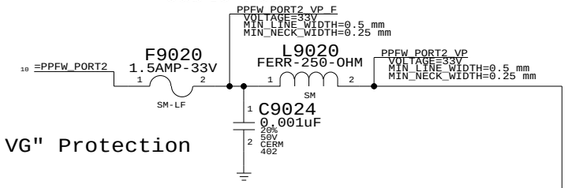


AREF needs to be isolated from all local grounds per 1394b spec

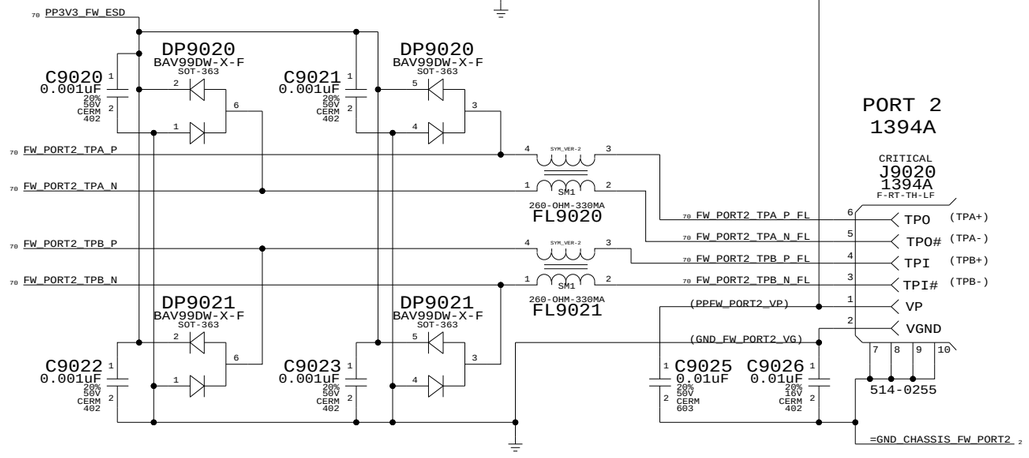
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

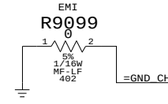
BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



"Snapback" & "Late VG" Protection





FireWire Ports

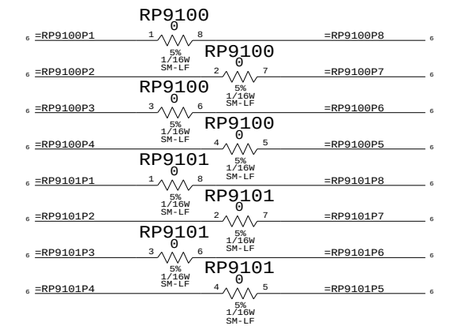
SYNC_MASTER=MARIAS-PDIFF
SYNC_DATE=06/02/2005

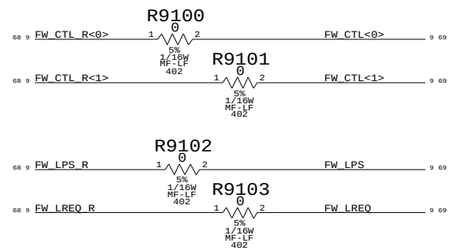
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 90 OF 115	

DRAWING
TITLE=PLASMA
ABBREV=DRAWING
LAST_MODIFIED=Wed Nov 2 16:09:22 2005

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.).





FireWire Series Term

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT
NONE	91 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: SPACING	NET_TYPE: PHYSICAL	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2_P<0> 11 72
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2_N<0> 11 72
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2_P<1> 6 72
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2_N<1> 6 72
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2_P<2> 11 72
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2_N<2> 11 72
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2_P<3> 6 72
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2_N<3> 6 72
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2_P<4> 11 72
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2_N<4> 11 72
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2_P<5> 11 72
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2_N<5> 11 72
USB2_I2_XTAL	XTAL	XTAL		I2_CLK30M_USB2_XOUT_R 72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XOUT 72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XIN 72

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

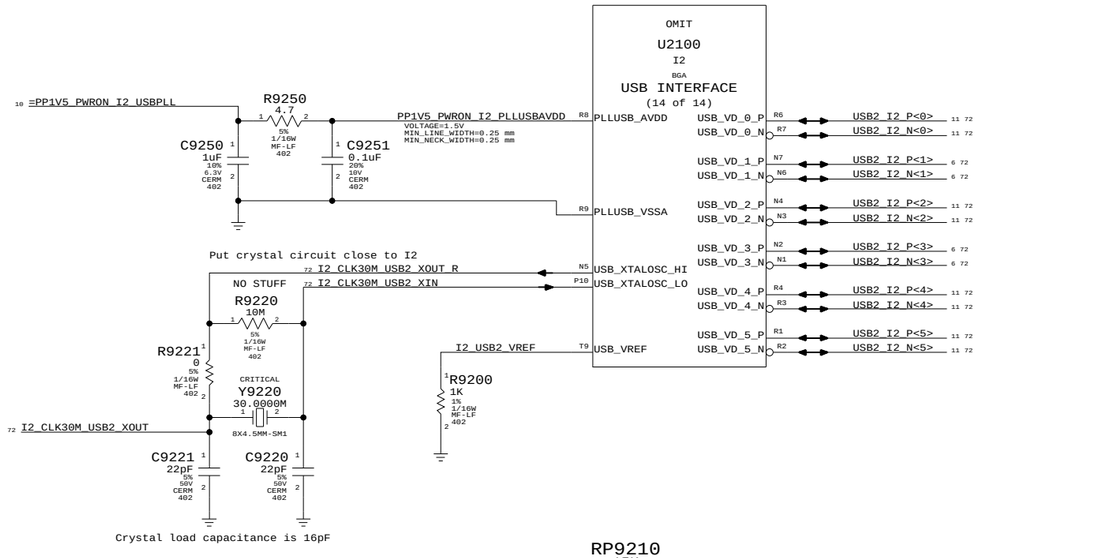
Signal aliases required by this page:
- =RP92xxPy (pinswappable USB pulldowns)

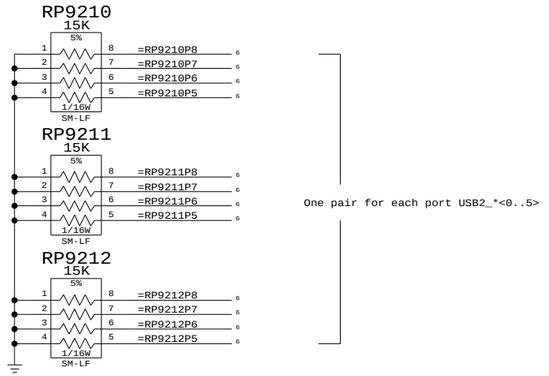
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





I2 USB Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 92 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
J30	USB2	USB2	USB2_NEC_0	USB2_NEC_P<0> 11 73
J31	USB2	USB2	USB2_NEC_0	USB2_NEC_N<0> 11 73
J34	USB2	USB2	USB2_NEC_1	USB2_NEC_P<1> 11 73
J32	USB2	USB2	USB2_NEC_1	USB2_NEC_N<1> 11 73
J33	USB2	USB2	USB2_NEC_2	USB2_NEC_P<2> 11 73
J35	USB2	USB2	USB2_NEC_2	USB2_NEC_N<2> 11 73
J36	USB2	USB2	USB2_NEC_3	USB2_NEC_P<3> 11 73
J37	USB2	USB2	USB2_NEC_3	USB2_NEC_N<3> 11 73
ELECTRICAL_CONSTRAINT_SET PROVIDED BY I2 PAGES				
J40 USB2_NEC_XTAL	XTAL	XTAL		NEC_CLK30M_XT1 73
J41	XTAL	XTAL		NEC_CLK30M_XT2 73
J42	XTAL	XTAL		NEC_CLK30M_XT2_R 73

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB2

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,30.0000MHZ,LW PROF,8X4.5MM,SMD	Y9345	CRITICAL	USB2_NEC

Y9345 LOAD CAPACITANCE IS 16pF

USB2_NEC
L9335
FERR-EMI-100-OHM
SM
73 10 =PP3V3_PWRON_USB2
PP3V3_PWRON_NEC_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

USB2_NEC R9335 4.7 5% 1/10W MF-LF 603

USB2_NEC C9335 10uF 20% 6.3V X5R 603
USB2_NEC C9336 0.1uF 20% 10V CERM 402
USB2_NEC C9937 0.1uF 20% 10V CERM 402

USB2_NEC C9320 10uF 20% 6.3V X5R 603
USB2_NEC C9321 0.1uF 20% 10V CERM 402
USB2_NEC C9322 0.1uF 20% 10V CERM 402
USB2_NEC C9323 0.1uF 20% 10V CERM 402
USB2_NEC C9324 0.1uF 20% 10V CERM 402
USB2_NEC C9325 0.1uF 20% 10V CERM 402
USB2_NEC C9326 0.1uF 20% 10V CERM 402
USB2_NEC C9327 0.1uF 20% 10V CERM 402
USB2_NEC C9328 0.1uF 20% 10V CERM 402
USB2_NEC C9329 0.1uF 20% 10V CERM 402
USB2_NEC C9330 0.1uF 20% 10V CERM 402

P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 → VDD
N10 N12 → AVDD

USB2_NEC CRITICAL U7500 NEC_uPD720101_USB2 FBGA-LF

73 10 =PP3V3_PWRON_USB2
USB2_NEC R9310 10K 5% 1/10W MF-LF 402
USB2_NEC RP9310 10K 5% 1/10W SM-LF

USB2_OC<0> B12 OCI1
USB2_OC<1> B11 OCI2
USB2_OC<2> B10 OCI3
USB2_OC<3> A10 OCI4
USB2_OC<4> B9 OCI5

TP_USB2_PWREN<0> C12 PPON1
TP_USB2_PWREN<1> A11 PPON2
TP_USB2_PWREN<2> C11 PPON3
TP_USB2_PWREN<3> C10 PPON4
TP_USB2_PWREN<4> A9 PPON5

73 10 =PP3V3_PWRON_USB2
USB2_NEC R9340 1.5K 5% 1/16W MF-LF 402
USB2_NEC R9341 1.5K 5% 1/16W MF-LF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

73 NEC_CLK30M_XT1 L9 XT1/SCLK
73 NEC_CLK30M_XT2_R P8 XT2

USB2_NEC R9345 100 5% 1/16W MF-LF 402
OMIT CRITICAL Y9345 30.0000M 8X4.5MM-SM
NEC_CLK30M_XT2 73

USB2_NEC C9345 22pF 5% 50V CERM 402
USB2_NEC C9346 22pF 5% 50V CERM 402

B1 N1 P10 K14 H14 B14 A2 D2 N2 N14 B13 M11 L12 H12 D12 G4 J11 F11 D8 → VSS

RREF P11 NEC_RREF_PD
USB2_NEC R9338 9.09K 1% 1/10W MF-LF 402
Tie to GND at ball N11
GND_NEC_AVSS_R
VOLTAGE=0V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

AVSS AVSS(R) P14 M12 N11 → R9339 0 5% 1/10W MF-LF 603 → USB2_NEC

RSDM1 M14 USB_NEC_N<0>
DM1 M13 (USB2_NEC_N<0>)
DP1 L14 (USB2_NEC_P<0>)
RSDP1 K13 USB_NEC_P<0>
USB2_NEC R9300 39.2 1% 1/10W MF-LF 402
USB2_NEC R9301 39.2 1% 1/10W MF-LF 402
USB2_NEC_N<0> 11 73
USB2_NEC_P<0> 11 73

RSDM2 K14 USB_NEC_N<1>
DM2 K12 (USB2_NEC_N<1>)
DP2 J14 (USB2_NEC_P<1>)
RSDP2 J12 USB_NEC_P<1>
USB2_NEC R9302 39.2 1% 1/10W MF-LF 402
USB2_NEC R9303 39.2 1% 1/10W MF-LF 402
USB2_NEC_N<1> 11 73
USB2_NEC_P<1> 11 73

RSDM3 H11 USB_NEC_N<2>
DM3 G11 (USB2_NEC_N<2>)
DP3 G13 (USB2_NEC_P<2>)
RSDP3 G14 USB_NEC_P<2>
USB2_NEC R9304 36 1% 1/10W MF-LF 402
USB2_NEC R9305 36 1% 1/10W MF-LF 402
USB2_NEC_N<2> 11 73
USB2_NEC_P<2> 11 73

RSDM4 F12 USB_NEC_N<3>
DM4 F14 (USB2_NEC_N<3>)
DP4 E12 (USB2_NEC_P<3>)
RSDP4 E14 USB_NEC_P<3>
USB2_NEC R9306 36 1% 1/10W MF-LF 402
USB2_NEC R9307 36 1% 1/10W MF-LF 402
USB2_NEC_N<3> 11 73
USB2_NEC_P<3> 11 73

RSDM5 E13 NC
DM5 D14
DP5 C13
RSDP5 C14 NC

USB2_NEC RP9300 15K 5%
=RP9300P8 =RP9300P7 =RP9300P6 =RP9300P5 6
1/16W SM-LF

USB2_NEC RP9301 15K 5%
=RP9301P8 =RP9301P7 =RP9301P6 =RP9301P5 6
1/16W SM-LF

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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

NEC USB2 Interface

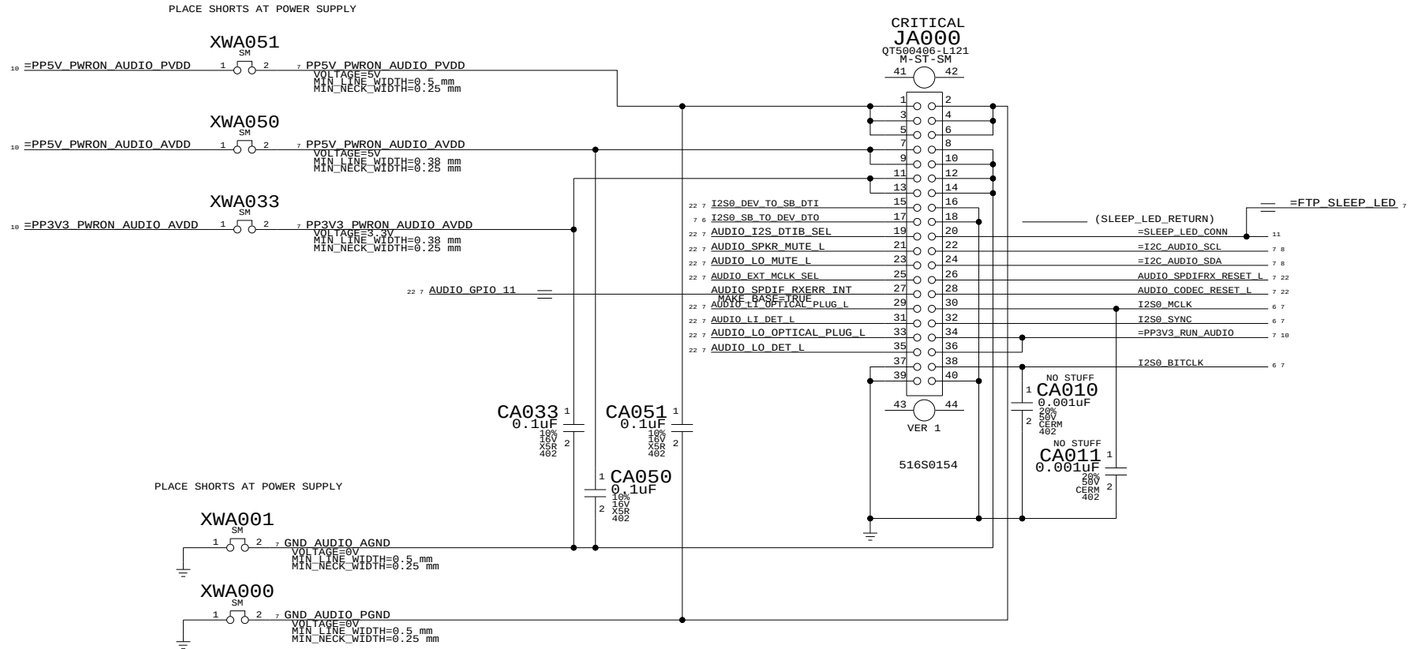
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 93 OF 115	

AUDIO BOARD CONNECTOR

Place all shorts at output of 3.3V and 5V regulator



Audio Board Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE: NONE	SHT 100 OF 115	

AGP

TABLE_SPACING_RULE

TABLE_SPACING_RULE

AGP	401	*	0.4 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_SPACING_RULE

AGP_STB	601	*	0.6 MM	2.5 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

AGP	*	=STANDARD	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

TABLE_PHYSICAL_RULE

AGP_STB	*	=STANDARD	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

CLOCK

TABLE_SPACING_RULE

TABLE_SPACING_RULE

CLOCK	251	*	0.25 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

CLOCK	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

ENET (Ethernet Digital)

TABLE_SPACING_RULE

TABLE_SPACING_RULE

ENET_SELF	=STANDARD	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	ENET	ENET	*	ENET_SELF

TABLE_SPACING_RULE

ENET	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

ENET	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT

FW (FireWire Digital)

TABLE_SPACING_RULE

TABLE_SPACING_RULE

FW_SELF	=STANDARD	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	FW	FW	*	FW_SELF

TABLE_SPACING_RULE

FW	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

FW	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

I2C

TABLE_SPACING_RULE

TABLE_SPACING_RULE

I2C	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

I2C	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

MaxBus

TABLE_SPACING_RULE

TABLE_SPACING_RULE

MAXBUS	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

MAXBUS	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

PCI

TABLE_SPACING_RULE

TABLE_SPACING_RULE

PCI	=STANDARD	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

PCI	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

RAM

TABLE_SPACING_RULE

TABLE_SPACING_RULE

RAM	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_SPACING_RULE

RAM_DIFF	251	*	0.25 MM	2.5 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

RAM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

TABLE_PHYSICAL_RULE

RAM_DIFF	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

UATA

TABLE_SPACING_RULE

TABLE_SPACING_RULE

UATA	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

UATA	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

USB2

TABLE_SPACING_RULE

TABLE_SPACING_RULE

USB2	501	*	0.50 MM	3.81 MM	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

USB2	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

AUDIO

TABLE_SPACING_RULE

TABLE_SPACING_RULE

AUDIO	251	*	0.25 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

AUDIO	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

I2S

TABLE_SPACING_RULE

TABLE_SPACING_RULE

I2S	251	*	0.25 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

I2S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

ENETCONN

TABLE_SPACING_RULE

TABLE_SPACING_RULE

ENETCONN	501	*	0.50 MM	3.81 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

ENETCONN	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

FW_TP

TABLE_SPACING_RULE

TABLE_SPACING_RULE

FW_TP	501	*	0.50 MM	3.81 MM	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

FW_TP	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

I2_FBCLK / XTAL

TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT

I2_FBCLK	*	*	CLOCK

TABLE_SPACING_ASSIGNMENT

XTAL	*	*	CLOCK

TABLE_PHYSICAL_ASSIGNMENT

TABLE_PHYSICAL_ASSIGNMENT

I2_FBCLK	*	CLOCK

TABLE_PHYSICAL_ASSIGNMENT

XTAL	*	CLOCK

Spacing & Physical Constraints

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE	SHT OF
NONE	110 115

TABLE_SPACING_RULE

TABLE_SPACING_RULE

DVO	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

DVO

DVO	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

TABLE_SPACING_RULE

TABLE_SPACING_RULE

TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_SPACING_RULE

TV_CONN	151	*	=TV	=TV	=TV	=TV	=TV

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

S-VIDEO

TABLE_PHYSICAL_RULE

TV	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_PHYSICAL_RULE

TV_CONN	*	=TV	=TV	=TV	=TV

TABLE_SPACING_RULE

TABLE_SPACING_RULE

VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_SPACING_RULE

VGA_CONN	151	*	=VGA	=VGA	=VGA	=VGA	=VGA

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

VGA

TABLE_PHYSICAL_RULE

VGA	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_PHYSICAL_RULE

VGA_CONN	*	=VGA	=VGA	=VGA	=VGA

TABLE_SPACING_RULE

TABLE_SPACING_RULE

LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

LVDS

LVDS	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_SPACING_RULE

TABLE_SPACING_RULE

TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_SPACING_RULE

TMDS_CONN	=TMDS	*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

TMDS

TMDS	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TMDS_CONN	*	=TMDS	=TMDS	=TMDS	=TMDS

TABLE_SPACING_RULE

TABLE_SPACING_RULE

THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

THERM

THERM	*	Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF

Spacing & Physical Constraints 2

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 111 OF 115

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*** Signal Cross-Reference for the entire design ***

1V5RUN_EN           16A6<> 26C6<
1V8RUN_EN_L         16A4<> 26B4<>
1V8_1V5PWRON_EN_L   26D4<
1V20_REF            12C7< 14C8<
1V65_REF            13A5<
1_5V_BOOST          16C6<>
1_5V_BST            16C5<>
1_5V_DH             16C6<>
1_5V_DL             16B6<>
1_5V_FB             16B7<
1_5V_ILIM           16C5<>
1_5V_LX             16B5<>
1_8V_BOOST          16C4<>
1_8V_BST            16C4<>
1_8V_DH             16C3<>
1_8V_DL             16B3<>
1_8V_FB             16B4<
1_8V_ILIM           16C5<>
1_8V_LX             16B3<>
1_8V_PVDD_STD       51C1<
2V5PWRON_EN_L       26D4<
2V5RUN_EN_L         17A5<> 26C6<
3V3RUN_EN_L         15B3<> 26C5<
3V_BG               15C4<>
3V_BOOST            15C4<>
3V_BOOST_ESR        15D3<>
3V_ITH              15C4<>
3V_ITH_RC           15C3<
3V_PMU_VTAP         14B3<
3V_RSNS             15D2<
3V_RUNSS            15C4<
3V_SNSM             15C4<
3V_SNSP             15C4<
3V_SW               15C4<>
3V_TG               15D4<>
3V_VOSNS            15C4<>
5V3V3PWRON_EN_L     26D6<
5V3VPWRON_EN_L_RC   15B6<
5VRUNHD_EN_L        15B5<> 26D5<
5VRUN_EN_L          15A5<> 26D5<
5VTPAD_EN_L         26D4<
5V_BG               15C5<>
5V_BOOST            15C5<>
5V_BOOST_ESR        15D6<>
5V_ITH              15C5<>
5V_ITH_RC           15C6<
5V_RSNS             15D7<
5V_RUNSS            15C5<
5V_SNSM             15C5<
5V_SNSP             15C5<
5V_SW               15C5<>
5V_TG               15C5<>
5V_VOSNS            15C5<>
1625_BG             14C5<>
1625_BST            14C5<
1625_BST_ESR        14C5<>
1625_COMP           13D2< 14C6<
1625_DIV            14C8<
1625_ENABLE         14D7<>
1625_ENABLE_L       14D7<>
1625_FCB            14C6<
1625_INTVCC         14C5<>
1625_RUNSS          14C6<
1625_SGND           14B7<>
1625_TG             14C5<>
1625_VFB            14B5<>
1625_VIN            14C6<
1625_VSW            14C4<>
1772_ACIN           13B5<
1772_ACOK_L         13B5<> 13C4<>
1772_BST            13B4<>
1772_BST_ESR        13C3<
1772_CCI            13B5<>
1772_CCS            13B5<
1772_CCV            13B5<>
1772_CCV_RC         13B5<
1772_CELLS          13B4<
1772_CLS            13A4<
1772_CSIN           13B4<>
1772_CSIP           13B4<>
1772_CSSN           13C5<
1772_CSSP           13C5<
1772_DCIN           13B5<
1772_DHI            13B4<>
1772_DLO            13B4<>
1772_DLOV           13B4<>
1772_GND            13A5<>
1772_ICHG           13B5<>
1772_ICTL           13B5<>
1772_IINP           13B5<
1772_LDO            13C4<>
1772_LX             13B4<>
1772_REF            13B5<>
1772_VCTL           13B5<
1778_BG             45C5<>
1778_BST            45C5<>
1778_BST_RC         45C4<>
1778_FCB            45C6<
1778_GND            45B6<>
1778_ION            45C5<
1778_ITH            45C6<>
1778_ITH_RC         45C7<
1778_TG             45C5<>
1778_VFB            45C5<
1778_VRNG           45C6<
3707_FCB            15C5<
3707_FSET           15C5<
3707_INTVCC         15D5<>
3707_SGND           15C7<>
3707_STBYMD         15C5<>
=1V8_1V5PWRON_EN_L  16C8<> 26D3>
=1V8_1V5PWRON_PGOOD  16C6> 26B8<
=2V5PWRON_EN_L   17C7<> 26D3>
=2V5PWRON_PGOOD  17C4> 26B8<
=5V3V3PWRON_EN_L  15B6< 26D5>
=5V3VPWRON_PGOOD  15C4<> 26B8<
=5VPWRONTPAD_EN_L  15A8<> 26D3>
=ADT7467_THERM_L  11B3> 27C2<
=AGP_GPU_RESET_L  11C7> 44D4<
=AGP_VREF         11C7> 44B2<
=CLK33M_TBEN_SYNC  11D1> 21A5< 21D6>
=CPU0_MAX1717_AB_SEL  11A3> 36A7< 36C7<
=CPU0_VID_AB_SEL  11A3> 36D3<>
=CPU_HRESET_L     11B3> 34A8< 34C6< 34D4<
=ENET_COL_R       11A6> 66B3>
=ENET_CRS_R       11A6> 66B3>
=ENET_RXD_R<0>    66C3>
=ENET_RXD_R<7..0>  11A6>
=ENET_RXD_R<1>    66C3>
=ENET_RXD_R<2>    66C3>
=ENET_RXD_R<3>    66C3>
=ENET_RXD_R<4>    66C3>
=ENET_RXD_R<5>    66C3>
=ENET_RXD_R<6>    66C3>
=ENET_RXD_R<7>    66C3>
=ENET_RX_DV_R     11A6> 66C3>
=ENET_RX_ER_R     11A6> 66B3>
=ENET_TXD<0>      66C6<
=ENET_TXD<7..0>   11A6>
=ENET_TXD<1>      66C6<
=ENET_TXD<2>      66C6<
=ENET_TXD<3>      66C6<
=ENET_TXD<4>      66C6<
=ENET_TXD<5>      66C6<
=ENET_TXD<6>      66C6<
=ENET_TXD<7>      66C6<
=ENET_TX_EN       11A6> 66C6<
=ENET_TX_ER       11A6> 66B6<
=FTP_GND          7C5> 7C5> 7C7> 10D2>
=FTP_SLEEP_LED    7C5> 74C2>
=FWPWR_PWRON      18C8<> 26D3>
=GND_CHASSIS_DVI1  2D4> 57D3<>
=GND_CHASSIS_DVI2  2D4> 57C3<>
=GND_CHASSIS_DVI3  2D4> 57C2<
=GND_CHASSIS_DVI4  2D4> 57B2<
=GND_CHASSIS_DVI_HOLE  2D2<> 2D4>
=GND_CHASSIS_ENET  2D4> 67A2<>
=GND_CHASSIS_FW_EMI  2D4> 70A1<
=GND_CHASSIS_FW_HOLE  2D1<> 2D4>
=GND_CHASSIS_FW_PORT1  2D4> 70C1<>
=GND_CHASSIS_FW_PORT2  2D4> 70A2<>
=GND_CHASSIS_INVERTER1  2C4> 56B3<
=GND_CHASSIS_INVERTER2  2C4> 56A2<
=GND_CHASSIS_INV_GND_CLIP  2D1<> 2D4>
=GND_CHASSIS_LCD1  2D4> 56C5<>
=GND_CHASSIS_LCD2  2D4> 56C6<

=GND_CHASSIS_LCD3  2D4> 56B6<
=GND_CHASSIS_LCD4  2D4> 56A5<>
=GND_CHASSIS_SVIDEO_HOLE  2D1<> 2D4>
=GND_CHASSIS_TV  2D4> 57A7<>
=GPUVCORE_PGOOD  26A8< 45C6>
=GPU_AGP_VREF     11C7> 44B4<
=I2C_ADT7467_SCL  8B1> 27C4<
=I2C_ADT7467_SDA  8B1> 27C4<>
=I2C_AUDIO_SCL    7A7> 8D1> 74B3<>
=I2C_AUDIO_SDA    7A7> 8D1> 74B3<>
=I2C_BATT_SCL     8B4> 12A5<
=I2C_BATT_SDA     8B4> 12A5<
=I2C_DS1775_SCL   7C5> 8B1> 30C6<>
=I2C_DS1775_SDA   7C5> 8B1> 30C6<>
=I2C_GPU_TMDS_SCL  8A5< 51B3<>
=I2C_GPU_TMDS_SDA  8A5< 51B3<>
=I2C_I2_NB_SCL    8C3< 22C2<
=I2C_I2_NB_SDA    8C3< 22C2<
=I2C_I2_SB_SCL    8D3< 22C2<
=I2C_I2_SB_SDA    8D3< 22B2<
=I2C_PMU_SCL      8C5< 25C5<>
=I2C_PMU_SDA      8C5< 25C5<>
=I2C_PMU_SMB_SCL  8B5< 25C5<>
=I2C_PMU_SMB_SDA  8B5< 25C5<>
=I2C_SI_M_SCL     8A4> 54B6<
=I2C_SI_M_SDA     8A4> 54B6<
=I2C_SI_S_SCL     8A4> 55B6<
=I2C_SI_S_SDA     8A4> 55B6<
=I2C_SODIMM_SCL  8C1> 40A6<> 41A6<>
=I2C_SODIMM_SDA  8C1> 40A6<> 41A6<>
=I2VCORE_PGOOD   20C4> 26B8<
=I2_AGP_FBCLK_IN  21C5> 43A5<
=I2_AGP_VREF      11C7> 43B5<
=I2_MAXBUS_FBCLK_IN  21D1> 32A6<
=I2_PCI_FBCLK_IN  21B5> 59A5<
=I2_STOPCPU_L     11B3> 22A5<
=I2_STOPXTAL_L    11B3> 22A5<
=JTAG_BBANGER_TCK  9D8> 25B5<>
=JTAG_BBANGER_TDI  9D8> 25B5<>
=JTAG_BBANGER_TMS  9D8> 25B5<>
=JTAG_BBANGER_TRST_L  9D8> 25C5<>
=JTAG_CPU0_TCK    9D5> 34D6<
=JTAG_CPU0_TDI    9D6> 34D6<
=JTAG_CPU0_TDO    9D6< 34D6>
=JTAG_CPU0_TMS    9D5> 34D6<
=JTAG_CPU0_TRST_L  9D5> 34D6<
=JTAG_I2_TCK      9B6> 22B5<
=JTAG_I2_TDI      9C6> 22B5<
=JTAG_I2_TDO      9C6< 22B2>
=JTAG_I2_TMS      9B6> 22B5<
=JTAG_I2_TRST_L   9B6> 22A5<
=JTAG_VESTA_TCK   9A6> 18A6<
=JTAG_VESTA_TDI   9A6> 18A6<
=JTAG_VESTA_TDO   9A6< 18A6>
=JTAG_VESTA_TMS   9A6> 18A6<
=JTAG_VESTA_TRST_L  9A6> 18A6<
=MAXBUS_CPU0_CLK  11D4> 33C1< 33D6>
=PCI_AIRPORT_GNT_L  11D1> 60C3<>
=PCI_AIRPORT_IDSEL  11C1> 60C7<
=PCI_AIRPORT_INT_L  11C1> 60B3<>
=PCI_AIRPORT_REQ_L  11D1> 60C5<>
=PCI_AIRPORT_RESET_L  11C1> 60C3<>
=PCI_CBUS_GNT_L  11C1> 61A7<
=PCI_CBUS_IDSEL  11C1> 61B8<
=PCI_CBUS_INT_L  11C1> 61A7<>
=PCI_CBUS_REQ_L  11C1> 61A7<
=PCI_CBUS_RESET_L  11C1> 61A7<
=PCI_CLK33M_AIRPORT  11D1> 60B5<> 60D6>
=PCI_CLK33M_CBUS  11C1> 61A7< 61D1>
=PCI_CLK33M_USB2  11C1> 62B5< 62D6>
=PCI_CLK33M_ZDBOUT_R<0>  11D4< 23B4> 23D6>
=PCI_CLK33M_ZDBOUT_R<1>  11C4< 23B4> 23D6>
=PCI_CLK33M_ZDBOUT_R<2>  11C4< 23B4> 23D6>
=PCI_CLK33M_ZDBOUT_R<3>  11B4< 23B4> 23D6>
=PCI_CLK33M_ZDB_IN  11D1> 23B5< 23D6>
=PCI_USB2_GNT_L  11C1> 62B5<
=PCI_USB2_IDSEL  11B1> 62B6<
=PCI_USB2_INT_L  11B1> 62B7<
=PCI_USB2_REQ_L  11C1> 62B5>
=PCI_USB2_RESET_L  11B1> 62A7<
=PP1V2_ENETFW     10D4> 66D2< 69C1< 69D5<
=PP1V2_VESTA      10D4> 18B7<
=PP1V2_VESTA_REG  10D6< 18C1<
=PP1V05R1V3_GPU_VCORE  10A6> 46D6<
=PP1V5R1V8_MAXBUS  10A1> 21C8< 32D1< 33A5< 33B8<
            33C8< 34B5< 34B7< 34C4< 34C4< 34D4<
=PP1V5R1V8_PWRON_I2_MAXBUS  10A4> 32A5<
=PP1V5R1V8_RUN_I2_MAXBUS  10A1> 32B5<
=PP1V5R3V3_DVO_VREF  47C1> 54A2<
=PP1V5_AGP        10A6> 43A5< 43C1< 44B2< 44B7<
            44C6< 47C2<
=PP1V5_GPU        10A1> 10A8<
=PP1V5_GPU_DVO    10A6> 47C2<
=PP1V5_GPU_PWRSEQ  10A6> 52C4<>
=PP1V5_GPU_VDD15  10A6> 46B5<>
=PP1V5_I2_AGP     10A4> 43C7<
=PP1V5_PWRON_I2PLL_LDO  10D3< 20B3<>
=PP1V5_PWRON_I2_PLL  10D1> 19C5<
=PP1V5_PWRON_I2_USBPLL  10D1> 72C7<
=PP1V5_PWRON_REG  10A6<> 16B8<>
=PP1V5_PWRON_RUNFET  10A4> 16A8<>
=PP1V5_RUN_RUNFET  10A3< 16A6<>
=PP1V8R2V5_GPU_FB_VIO  10A6> 47C8< 48A8<
=PP1V8_FB_VDD     10A6> 49D5< 49D8< 50D5< 50D8<
=PP1V8_FB_VDDQ    10A6> 49D5< 49D8< 50D5< 50D8<
=PP1V8_GPU        10A1> 10A8<
=PP1V8_GPU_AVDD   10A8< 53C2<
=PP1V8_GPU_DVO    10A6> 47C2<
=PP1V8_GPU_LVDS_PLL  47C2< 51D1>
=PP1V8_GPU_MEMVMODE  10A6> 48A6<
=PP1V8_GPU_PANEL_IO  10A6> 47B2<
=PP1V8_GPU_PWRSEQ  10A6> 52D4<>
=PP1V8_GPU_TPVDD  10A8< 53D4<
=PP1V8_PWRON_DDR2  10A4> 40B8< 40C3< 40D4<> 40D6<>
            41C3< 41D4<> 41D6<>
=PP1V8_PWRON_I2_RAM  10A4> 38D3<
=PP1V8_PWRON_REG  10A6<> 16C1<>
=PP1V8_PWRON_RUNFET  10A4> 16B5<>
=PP1V8_RAM_I2_VREF  10A1> 38A6<
=PP1V8_RUN_RUNFET  10A3< 16A3<>
=PP1V8_RUN_TBEN_SYNC  10A1> 21B5<
=PP2V5R3V3_PWRON_I2_ENET  10B5< 65B6< 65C3< 65C7<
=PP2V5_ENET       10A4> 67C6<>
=PP2V5_ENETFW     10D4> 66D2< 69D1< 69D5<
=PP2V5_GPU        10B1> 10B8<
=PP2V5_GPU_A2VDD  10A6> 53B2<
=PP2V5_GPU_LVDS_IO  10B6> 47B1<
=PP2V5_GPU_PVDD  10B6> 51D3<
=PP2V5_GPU_PWRSEQ  10B6> 52D4<>
=PP2V5_PWRON_REG  10A6<> 17C2<
=PP2V5_PWRON_RUNFET  10A4> 17B5<>
=PP2V5_RUN_PCI1510  10B1> 61C8<
=PP2V5_RUN_RUNFET  10B3< 17B4<>
=PP2V5_VESTA      10D4> 18B2<
=PP2V5_VESTA_LDO  10D6< 18D1<>
=PP2V7R5V5_PWRON_I2VCORE  10B4> 20D7<
=PP2V8_GPU_LVDDR_LDO  10B8< 52B1<>
=PP2V8_GPU_LVDS_IO  10B6> 47A1<
=PP3V3_ADT7467    10B4> 27D5<
=PP3V3_AGP        10B6> 43D1< 44B4< 44C7<
=PP3V3_ALL_A29_DET  10C6> 12D3<>
=PP3V3_ALL_AC_DETECT  10C6> 12C7<>
=PP3V3_ALL_BATT0_DET  10B6> 12B7<
=PP3V3_ALL_BATT_CHGR  10C6> 13A6<> 13A8< 13C8<
=PP3V3_ALL_DEBUG  10B6> 24C3<>
=PP3V3_ALL_HALL_EFFECT  10C6> 30D6<
=PP3V3_ALL_LTC1625_SW  10C6> 14C7<>
=PP3V3_ALL_PBUS_ILIM  10C6> 13C3< 13D4<
=PP3V3_ALL_PMU    10C6> 24A7< 24D7< 25B6< 25C8<
            25D5<
=PP3V3_ALL_PWRSEQ  10B6> 26B7<> 26D5<
=PP3V3_ALL_VREG   10C8< 14A2<
=PP3V3_AUDIO_MUTESEQ  10B5< 22B2< 22D7<
=PP3V3_BATT_IMON  10B6> 12A5<
=PP3V3_DDC_DVI    10B1> 57B4<> 57D2<>
=PP3V3_DDC_LCD    7B7> 10B1> 56C7<>
=PP3V3_ENET       10A5< 66B7<>
=PP3V3_ENETFW     10D4> 69D1<
=PP3V3_FW         10D4> 69A8< 69B2< 70A8<
=PP3V3_GPU        10B1> 10B8<
=PP3V3_GPU_CLOCKS  10B1> 52B8< 52C8<
=PP3V3_GPU_GPIOS  10B6> 51A7< 51B8< 53C4<
=PP3V3_GPU_PWRSEQ  10B6> 52D2<>
=PP3V3_GPU_VDDR3  10B6> 47D3<
=PP3V3_I2_PCISLOTEGPIOS  10B5< 22B7<
=PP3V3_PCI        10B1> 59D1<
=PP3V3_PCI_AIRPORT  10B1> 60C3<>
=PP3V3_PCI_ROM    10B5< 58B6< 58C5<>

=PP3V3_PCI_USB2  10B3< 62B6<
=PP3V3_PCI_ZDB   10B3< 23C5<
=PP3V3_PWRON_AUDIO_AVDD  10B4> 74B7<>
=PP3V3_PWRON_BT  10B4> 60C6<>
=PP3V3_PWRON_CPUVCORE_OFFSET  10B3> 36B7<
=PP3V3_PWRON_CPUVCORE_VID  10B4> 36C8< 36D6<
=PP3V3_PWRON_DS1775  10B4> 30D6<
=PP3V3_PWRON_I2_AGPPCI  10B5< 19A5<
=PP3V3_PWRON_I2_IO1  10B5< 19C5<
=PP3V3_PWRON_I2_IO2  10B5< 19B5<
=PP3V3_PWRON_I2_MAXBUS  10B4> 19B5<
=PP3V3_PWRON_I2_MISC  10B5< 22B6< 22C7<
=PP3V3_PWRON_INVERTER  10B4> 56B4<
=PP3V3_PWRON_JTAG_ASIC  9C8< 10B5<
=PP3V3_PWRON_LCD  10B4> 56C8<
=PP3V3_PWRON_LEFT_ALS  7B5> 10B4> 31C3<>
=PP3V3_PWRON_LTC3412  10B4> 17D6<
=PP3V3_PWRON_MMM  10B4> 29C6<
=PP3V3_PWRON_MODEM  10B4> 30B4<>
=PP3V3_PWRON_PMU  10B4> 25B8<
=PP3V3_PWRON_PWRSEQ  10B5< 26C5< 26C7<>
=PP3V3_PWRON_REG  10B6<> 15D1<
=PP3V3_PWRON_RT_ALS  10B5< 28D5<
=PP3V3_PWRON_RUNFET  10B4> 15B2<>
=PP3V3_PWRON_TPS2211  10B4> 61D4<
=PP3V3_PWRON_USB2  10A4> 73B6< 73C6< 73D5<
=PP3V3_PWRON_VDDSPD  10B5< 40A6<> 41A4<> 41A6<>
=PP3V3_PWRON_VGASYNC  10B4> 57C2< 57C2<
=PP3V3_RUN_AUDIO  7A7> 10B3< 74B3<>
=PP3V3_RUN_FANTACH  10B1> 27D2<
=PP3V3_RUN_FWPORTPWRSW  10B1> 18C8<
=PP3V3_RUN_HDD    10B1> 64B8< 64C7<
=PP3V3_RUN_KEYBRD_LED  10B1> 28B6<
=PP3V3_RUN_PCI1510_R  10B1> 61D7<
=PP3V3_RUN_PWRSEQ  10B3< 26B7<
=PP3V3_RUN_RUNFET  10B3< 15B1<>
=PP3V3_RUN_SI     10B1> 54C2< 54C3< 54C5< 55C3<
            55D3< 55D3<
=PP3V3_VESTA      10D4> 18A2< 18A6< 18A8< 65C2<>
            66C7< 67C6<>
=PP3V3_VESTA_1V2REG  10D4> 18C5<
=PP3V3_VESTA_2V5REG  10D4> 18D3<>
=PP3V3_VESTA_REG  10D6< 18D3<
=PP4V85_ALL_A29_DET  10C6> 12D4<
=PP4V85_ALL_VREG  10C8< 14B4<>
=PP5V_FAN1_PWR    7C5> 10C1> 31B4<>
=PP5V_FAN2_PWR    7C5> 10C1> 31B3<>
=PP5V_PWRON_AUDIO_AVDD  10C4> 74C7<>
=PP5V_PWRON_AUDIO_PVDD  10C4> 74C7<>
=PP5V_PWRON_CPUVCORE_PWRSEQ  10C3> 36C8<
=PP5V_PWRON_CPUVCORE_VDD  10C4> 36C6<>
=PP5V_PWRON_GPUVCORE_PWRPLAY  10C3> 45B5<
=PP5V_PWRON_INVERTER  10B4> 56C4<>
=PP5V_PWRON_LEFT_USB  7B5> 10C4> 31B3<>
=PP5V_PWRON_LTC1625_EXTVCC  10C4> 14D7<>
=PP5V_PWRON_LTC1778_GPU_EXTVCC  10C3> 45D6<
=PP5V_PWRON_LTC3707_EXTVCC  10C4> 15D5<
=PP5V_PWRON_MAX1715_VDD  10C4> 16D5<>
=PP5V_PWRON_PMU_SUPPLY  10C4> 14B4<>
=PP5V_PWRON_PWRSEQ  10C4> 26D7<
=PP5V_PWRON_REG  10C6<> 15D8<
=PP5V_PWRON_RIGHT_USB  7B5> 10C4> 31B7<>
=PP5V_PWRON_RUNFET  10C4> 15B5<>
=PP5V_PWRON_SLEEPLED  10B4> 24B7<
=PP5V_PWRON_TPS2211  10C4> 61D4<
=PP5V_PWRON_TRACKPAD  10B4> 15B8<>
=PP5V_RUN_DVI_DDC  10C1> 57D4<
=PP5V_RUN_FANPWM  10C1> 27D2<
=PP5V_RUN_HDD     7B7> 10C1> 64B5<> 64B8<
=PP5V_RUN_HDDFET  10C3< 15B4<>
=PP5V_RUN_KEYBRD_LED  10C1> 28B5<
=PP5V_RUN_ODD     7B7> 10C1> 64C4<
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=PP5V_RUN_RUNFET  10C3< 15A4<>
=PP5V_SUPERCAP    14A4< 31A6<
=PP5V_TPAD        10C1> 30D6<
=PP5V_TPAD_FET    10C3< 15A6<>
=PP12V8_LTC1625_VREG  10D8< 14C3<>
=PP12V8_PBUSB_HOLDUP_CAPS  10D6> 31D3<
=PP12V8_PBUS_PMU_SUPPLY  10D6> 14A7<>
=PP14VR24V_ALL_PBUS_A  10D8< 13D5<
=PP24V_ADAPTER_CONN  10C8< 31D7<>
=PP24V_ADAPTER_PMU_SUPPLY  10C6> 14A7<
=PP24V_ADAPTER_RAW  10C6> 12D8<>
=PP24V_PBUSA_HOLDUP_CAPS  10D6> 31D5<
=PPAVDD_CPU0      10C1> 35B6<
=PPBUS_DVI_PWRSW  10C6> 57A4<>
=PPBUS_FWPWRSW    10D6> 18D8<
=PPBUS_FW_FET     10D6> 18D5<>
=PPBUS_INVERTER   10D6> 56C3<
=PPBU_RUN_FW      10C1> 18D6<>
=PPFW_P3V3VESTA   10D4> 18D6<>
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=PPI2C_I2_SB      8D2< 10B3<
=PPI2C_SYS0       8B5< 10C6>
=PPI2C_SYS1       8C5< 10B5<
=PPJTAG_CPU       9D8< 10A1>
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=PPVBATT_BATTERY_PMU_SUPPLY  10C6> 14A7<
=PPVBATT_BATT_PBUSA  10D8< 13D2<>
=PPVBATT_BATT_PBUSB  10D8< 13D1<>
=PPVBATT_BATT_VSNS  10C8< 12B6<
=PPVBATT_ISNS_N   10C8< 12B4<>
=PPVCORE_CPU0     10C4> 35C4< 35C8< 35D4<
=PPVCORE_CPU_ADT7467  10C4> 27C4<
=PPVCORE_CPU_REG  10C6> 36C1<
=PPVCORE_GPU_REG  10A8< 45C3<>
=PPVCORE_PWRON_I2  10A6> 19D6<
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=PPVIN_ALL_LTC1625  10D6> 14D3<>
=PPVIN_ALL_LTC3707  10D6> 15D5<>
=PPVIN_ALL_MAX1715  10D6> 16C3<> 16C7<> 16D5<
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=PPVIN_CPUVCORE_MAX1717  10D6> 36D4<>
=PPVIN_GPU_LVDDR_LDO  10B6> 52B4<
=PPVIN_LTC1778_GPU  10D6> 45D5<>
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=SLEEP_LED_CONN  11A3> 74B3<>
=SLEEP_LED_IOUT  11A5< 24B6<
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=SPI_I2_MISO      22B2>
=SPI_I2_MOSI      22B5<
=SPI_I2_REQ       11A5< 22A7< 22C5<
=SYSCLK_TBEN_SYNC  11D4> 21A5< 21D6>
=TPS2211_SHDN_L  10B3< 61D5<
=VCORE_PGOOD      26B5< 36B4>
=VESTA_CLK25M_TX  11A6> 66C2>
=VESTA_CLK125M_GBE_REF  11A6> 66C2>
=VESTA_CLK125M_RX  11A6> 66C2>
=VESTA_ENERGYDET  11A6> 66B3>
=VESTA_MDC        11A6> 66B6>
=VESTA_MDIO       11A6> 66B6<>
A29_CLS_ADJ       13A5<>
A29_CURRENT_ADJ  13C4<>
A29_DETECT        12D1< 13A5<> 13C4<>
A29_DET_L         12C2<
A29_DET_REF       12C2<
AB_SEL_LOW        36A6<>

AC_DET_DIV        12C7<
AC_ENABLE_GATE    12D5<>
AC_ENABLE_L       12C5<>
AC_GTR_18V        13C3<>
ADAPTER_I_REG     13D3<>
ADT7467_ADR_ENABLE_L  27C2<>
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AGP_AD<3>         43C3< 44C6<>
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AGP_AD<31>        43B3< 44B6<>
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AGP_AD_STB0_P     43B2< 43C3< 43D6> 44B4<>
AGP_AD_STB1_N     43A2< 43B3< 43D6> 44B4<>
AGP_AD_STB1_P     43B2< 43B3< 43D6> 44B4<>
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AGP_BUSY_L        43D2< 43D5< 44B4>
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AGP_CBE_L<1..0>  43D6>
AGP_CBE_L<1>      43C3< 44C4<>
AGP_CBE_L<2>      43B3< 44C4<>
AGP_CBE_L<3..2>  43D6>
AGP_CBE_L<3>      43B3< 44C4<>
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AGP_CLK66M_GPU_R  11C8< 43D3< 43D6>
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AGP_FRAME_L       6B6< 43D5< 43D6> 44C4<>
AGP_GNT_L         6B6< 43C6> 43D3< 44C4<
AGP_INT_L         22D5< 43C2< 44C4>
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AGP_REQ_L         6B6< 43C6> 43D5< 44C4<>
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AGP_SBA<1>        43C5< 44B6>
AGP_SBA<2>        43C5< 44B6>
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AGP_SB_STB_P      43B2< 43C5< 43D6> 44B4<>
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AGP_ST<3..0>      43D6>
AGP_ST<1>         43B3< 44B4<
AGP_ST<2>         43B3< 44B4<
AGP_STOP_L        6B6< 43C5< 43C6> 44C4<>
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AGP_TRDY_L        6B6< 43C5< 43C6> 44C4<>
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AGP_WBF_L         43B2< 43C5< 43C6> 44B4>
AIRPORT_CLKRUN_L_PD  60C4<>
ALS_0_OUT         7B5> 25A6> 31C4<>
ALS_1_OUT         25A6> 28D3<
ALS_GAIN_BOOST    7B5> 25A6> 28C5<> 31B3<>
ANALOG_AC_DET     12C3<
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ATI_BUS_CFG<1>   51B5<>
ATI_BUS_CFG<2>   51B5<>
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ATI_CLK27M_R      52C6< 52D6>
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ATI_CLK27M_SSIN  52A6< 52C5< 52D6>
ATI_CLK27M_SS_R  52A6<> 52D6>
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ATI_DBI_LO_PU     44B6<>
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ATI_OSC_OE        52C7<
ATI_PVDD_BYP      51D2<>
ATI_R2SET         53B6<>
ATI_RSET          53B6<>
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AUDIO_CODEC_RESET_L  7A7> 22C5< 74B3<>
AUDIO_EXT_MCLK_SEL  7A7> 22C5< 74B4<>
AUDIO_GPIO_11     7A7> 22C5< 74B5<
AUDIO_I2S_DTIB_SEL  7A7> 22C5< 74B4<>
AUDIO_LI_DET_L   7A7> 22D5< 74B4<>
AUDIO_LI_OPTICAL_PLUG_L  7A7> 22D5< 74B4<>
AUDIO_LO_DET_L   7A7> 22C5< 74B4<>
AUDIO_LO_MUTE     22C7<>
AUDIO_LO_MUTE_L  7A7> 22C6<> 74B4<>
AUDIO_LO_OPTICAL_PLUG_L  7A7> 22C5< 74B4<>
AUDIO_SPDIFRX_RESET_L  7A7> 22C5< 74B3<>
AUDIO_SPDIF_RXERR_INT  74B4<>
AUDIO_SPKR_MUTE  22B2<>
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BATT0_DET_L       12A7<>
BATTV_HIGH        13B7<>
BATTV_LOW         13B8<>
BATT_14PBUS_EN    13C1<>
BATT_14V_GATE     13C1<>
BATT_24PBUS_EN    13C2<>
BATT_24V_GATE     13C1<>
BATT_CLK          12A7<>
BATT_DATA         12A7<>
BATT_DIV          13A5<
BATT_ISNS         12A3<> 25A3>
BATT_ISNS_R       12A4<>
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BKFD_PROT_EN_L    13C8<>
BKFD_PROT_GATE    13D8<>
BRIGHT_PWM        7B7> 56B2<>
BRIGHT_PWM_F      56B3<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 113	OF 115

*** Part Cross-Reference for the entire design ***

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T8601	XFR_1000BT_82400275	67
U1200	COMPARATOR_LMC7211	12
U1220	COMPARATOR_LMC7211	12
U1250	INA138	12
U1300	MAX1772	13
U1350	COMPARATOR_LMC7211	13
U1370	AMP_MAX4172	13
U1380	OPAMP_LMC7111	13
U1400	LTC1625	14
U1420	COMPARATOR_LMC7211	14
U1450	VREG_LP2951	14
U1460	VREG_LP2951	14
U1500	LTC3707	15
U1600	MAX1715	16
U1700	LTC3412	17
U1970	VREG_LM2594	18
U1980	VREG_MM1572FN	18
U1990	LTC3411	18
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U3000	ADT7467	27
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U3130	MM3120	28
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U5800	LTC1778	45
U6200	SDRAM_DDR_K4D553235F	49
U6250	SDRAM_DDR_K4D553235F	49
U6300	SDRAM_DDR_K4D553235F	50
U6350	SDRAM_DDR_K4D553235F	50
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U6510	CLK_GEN_CY25811	52
U6530	MAX8860	52
U6700	SIL1178CS48	54
U6800	SIL1178CS48	55
U6953	NCTS32	56
U7050	741G32	57
U7051	741G32	57
U7070	COMPARATOR_LMC7211	57
U7100	FEPR_1MX8	58
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U7450	PWR_CNTRL_TPS2211	61
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Y8920	CRYSTAL	69
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Y9345	CRYSTAL	73

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