1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

10/15/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		328536	PRODUCTION RELEASED	05/19/04	

SCHEM,SAPPHIRE,Q41B

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	CTO	✓
INT_TMDS	✓	CTO
NO_4XVCORE	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,SAPPHIRE,Q41B	SCH1	
820-1688	1	PCBF,SAPPHIRE,Q41B	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK / ENG APPD / MFG APPD / QA APPD / DESIGNER / RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

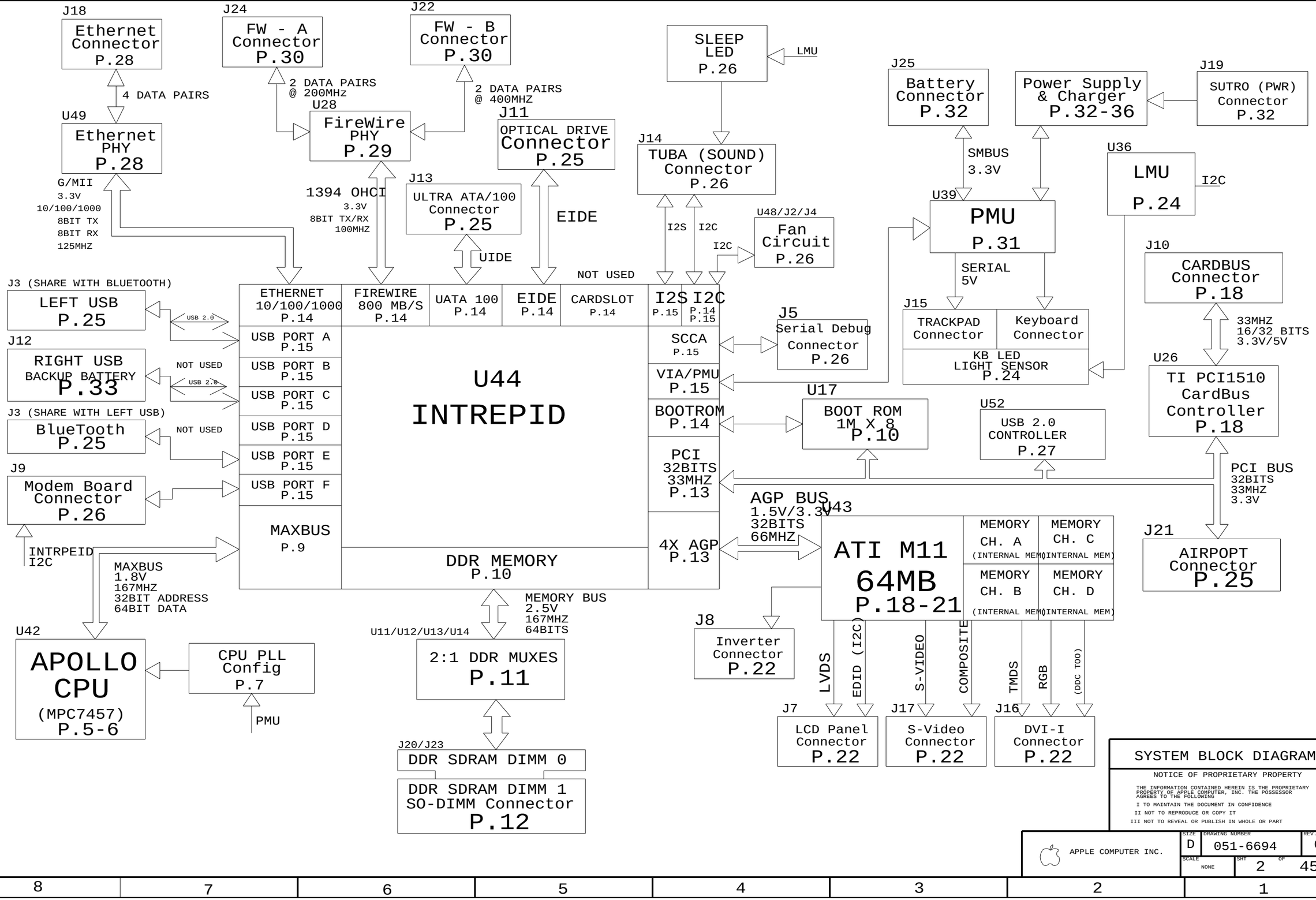
SIZE D

Apple Computer Inc.

TITLE
SCHEM,SAPPHIRE,Q41B

DRAWING NUMBER 051-6694 REV. 02

SHT 1 OF 45



SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	2	45

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
PG 31

INRUSH LIMITER
PG 30

+24V_PBUS

1V20_REF
U21
PG 31
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

RUN/SS
BUCK VCC REGULATOR (LTC1625)
PG 32
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO
PG 32
+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715)
PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE
(+1.4V/+1.5V)

DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707)
PG 33
VCC
STBYMD
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

+5V_MAIN
3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+PBUS (12.8V)

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778)
PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS

GPU_VCORE
+1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT
PG 32

+PBUS
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

+24V_PBUS

BATTERY CHARGER
(MAX1772)
PG 31

+BATT

DC/DC (LTC3411)
PG 35
+1.8V_MAIN
MAXBUS
BROADCOM
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

3S 3P PRISMATIC CELLS

BATTERY VOLTAGE FEED-IN PATH
PG 31
+PBUS

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN ~11MS
+5V_SLEEP
+3V_MAIN ~13.5MS
+3V_SLEEP
3V_5V_OK 2.4V - ??? MS
+2_5V_MAIN 2.6 MS
+2_5V_SLEEP
+1_5V_MAIN 2.6 MS
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS) ~???MS
GPU_VCORE (D3HOT)
GPU_VCORE (D3COLD)
+1_8V_MAIN 1.9 MS

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	3	45

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

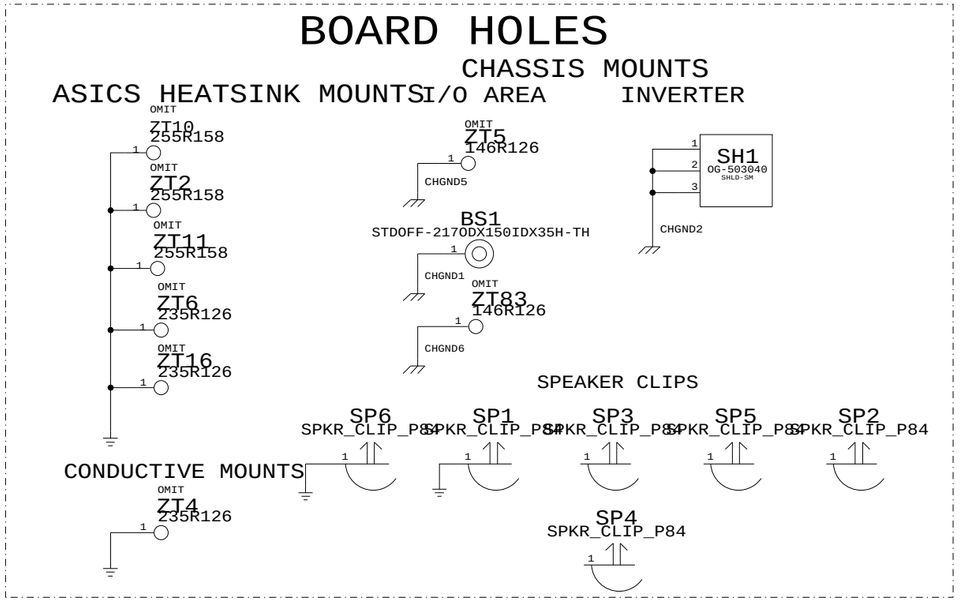
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



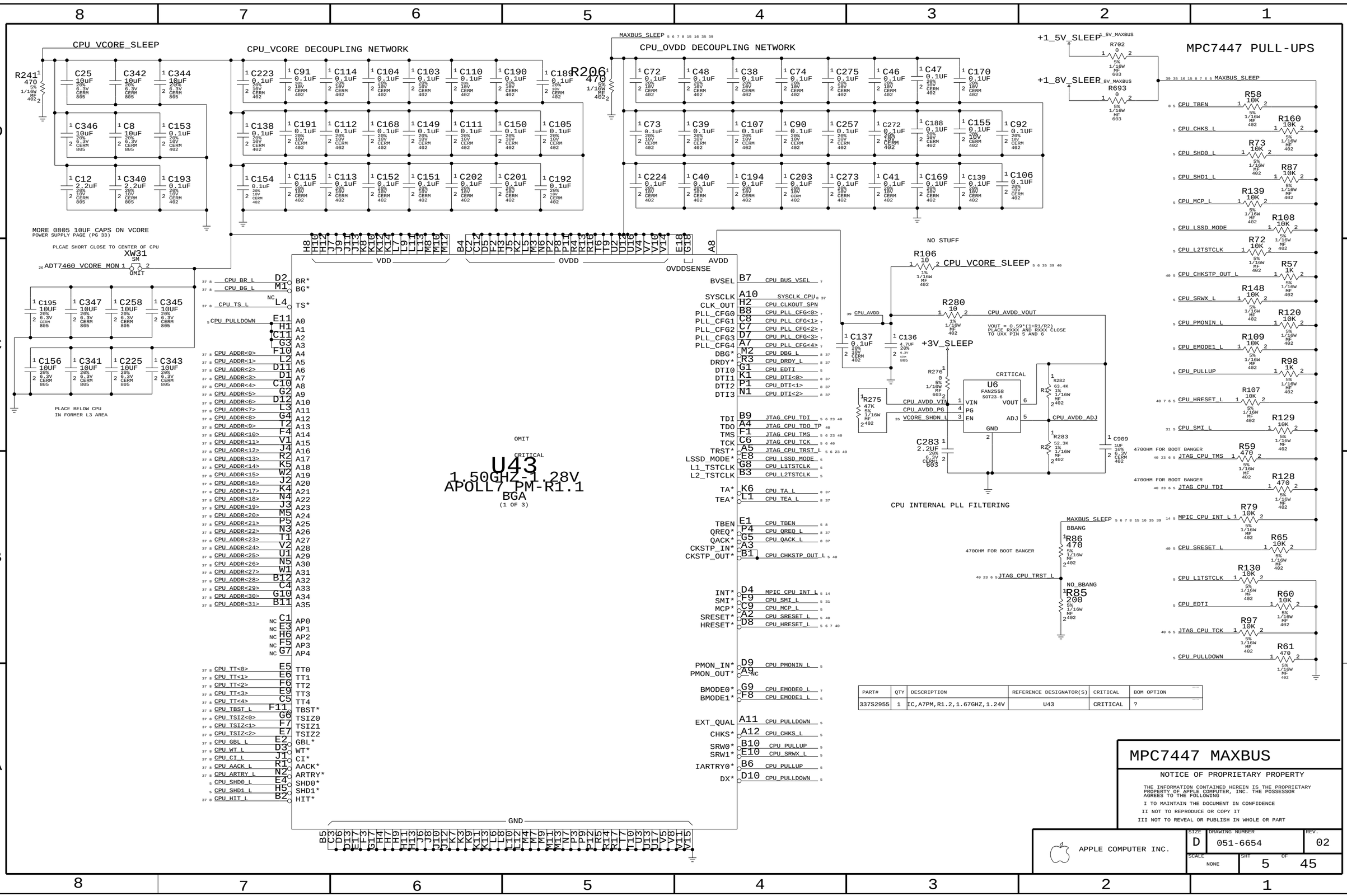
GROUND VIAS

ZT77, ZT81, ZT24, ZT38, ZT36, ZT27, ZT40, ZT39, ZT37, ZT28, ZT30, ZT34, ZT33, ZT43, ZT46
ZT35, ZT50, ZT44, ZT66, ZT67, ZT52, ZT53, ZT70, ZT71, ZT78, ZT69, ZT65, ZT47, ZT45, ZT49
ZT48, ZT56, ZT72, ZT55, ZT29, ZT74, ZT82, ZT79, ZT68, ZT60, ZT58, ZT41, ZT9, ZT7, ZT8
ZT57, ZT1, ZT80, ZT73, ZT75, ZT63, ZT61, ZT54, ZT51, ZT42, ZT64, ZT76, ZT62, ZT59, ZT21
ZT22, ZT25, ZT3, ZT32, ZT31, ZT26, ZT23, ZT19, ZT17, ZT15, ZT13, ZT12, ZT14, ZT18, ZT20
(all HOLE-VIA-20R10)

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 4 OF 45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,R1.2,1.67GHZ,1.24V	U43	CRITICAL	?

MPC7447 MAXBUS

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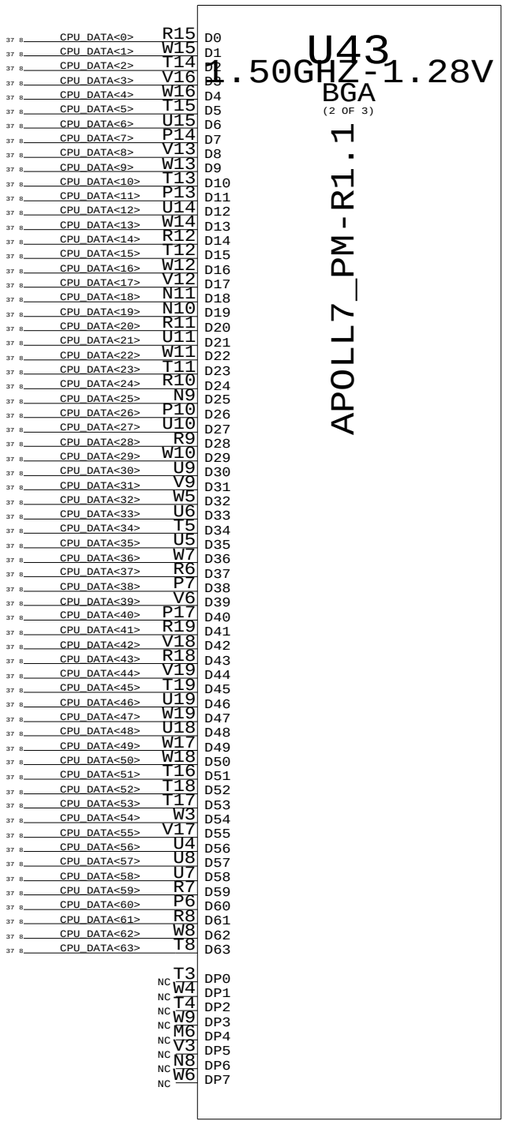
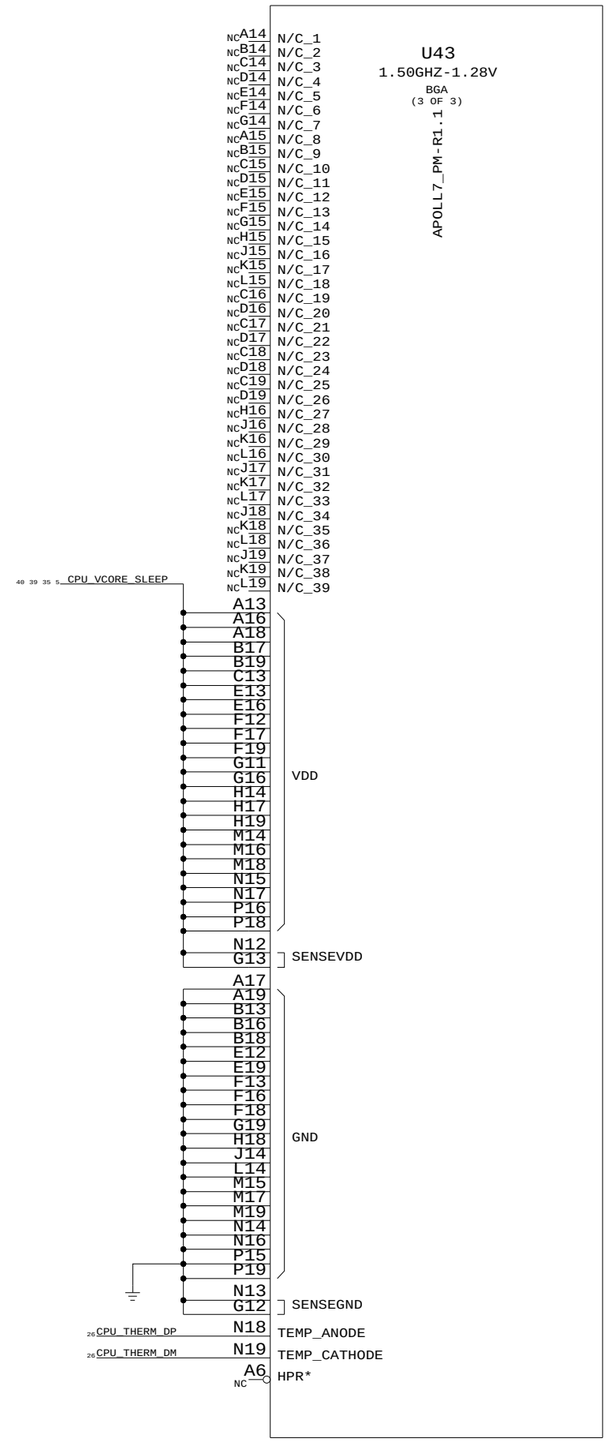
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	02

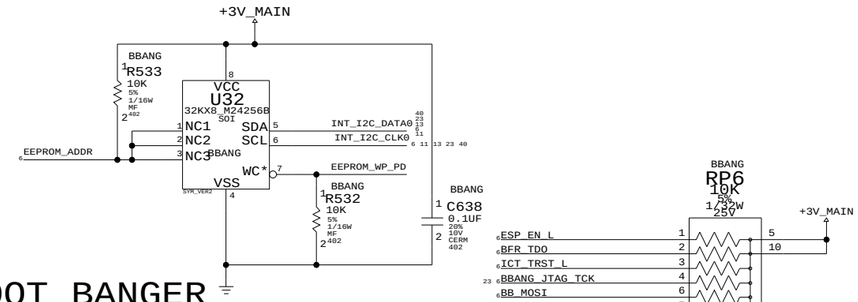
SCALE: NONE

SHT 5 OF 45

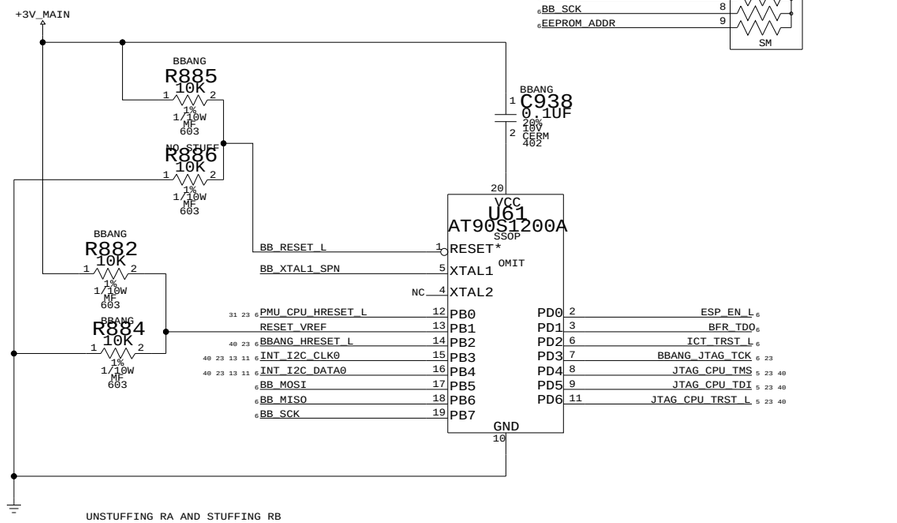




BOOT BANGER E2PROM

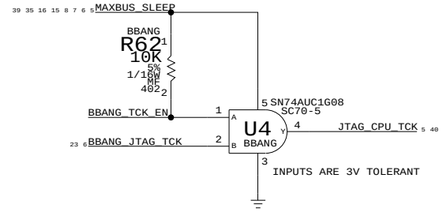


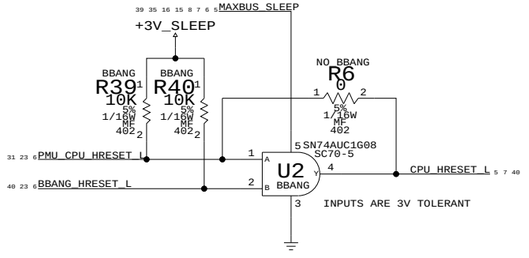
BOOT BANGER



UNSTUFFING RA AND STUFFING RB
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	009-6240 FW GT4 BBANGER MCU,PROGRAMMED W/	U54	BBANG





BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

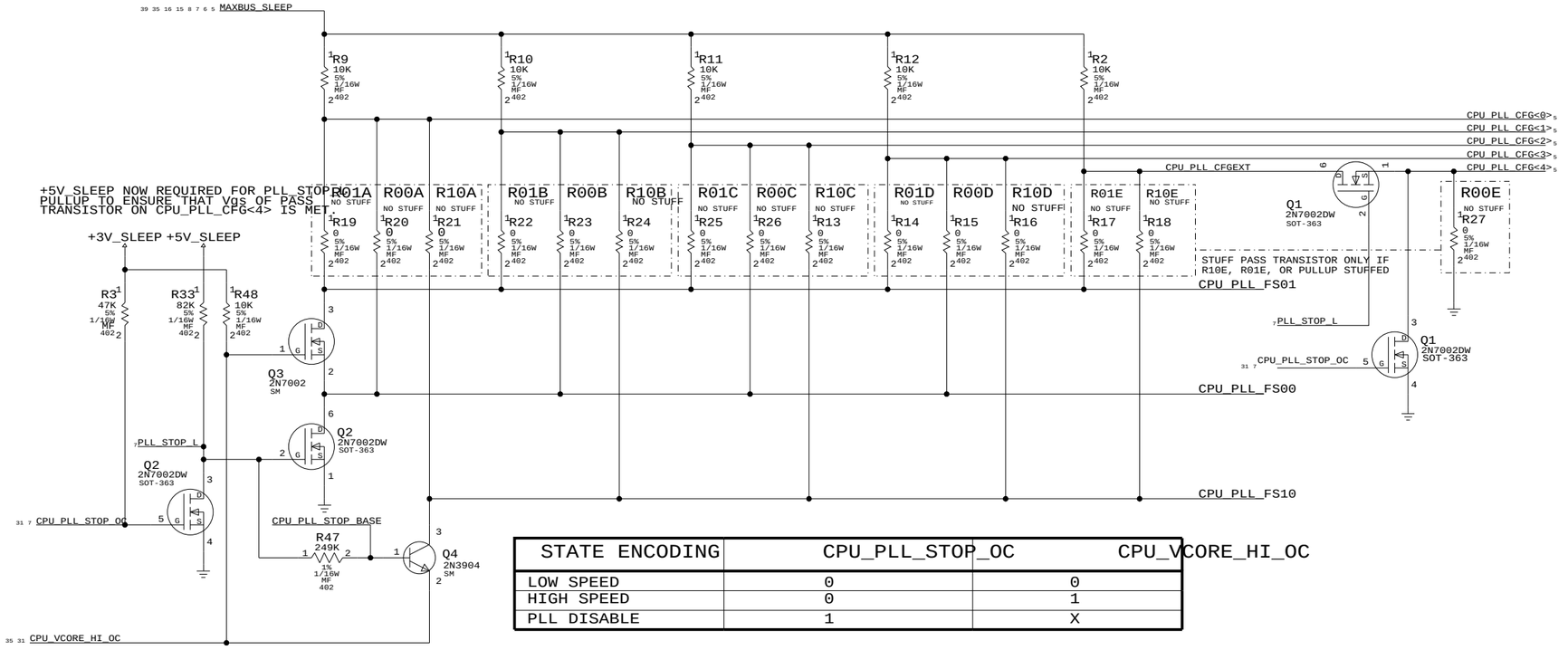
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	02

SCALE: NONE

SHT 6 OF 45

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

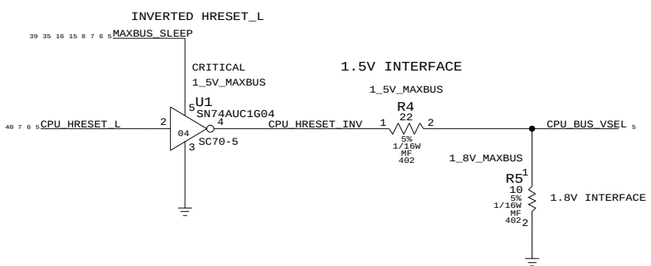
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	7	45

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
R642[1] 10K	R135[1] 10K	R123[1] 10K	R153[1] 10K	R166[1] 10K	R179[1] 10K	R651[1] 10K	R178[1] 10K
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

NO STUFF

R136[1] 10K	R643[1] 10K	R639[1] 10K	R657[1] 10K	R664[1] 10K	R673[1] 10K	R143[1] 10K	R674[1] 10K
0: Normal operation; 1: Tri-state all outputs (Hi-Z)	0: Inactive; 1: Activate	0: Pin active low; 1: Pin active high	0: Active low; 1: Active high	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
R122[1] 10K	R142[1] 10K	R164[1] 10K	R134[1] 10K	R184[1] 10K	R177[1] 10K	R152[1] 10K	R165[1] 10K
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

INT_CLK	INT_CLK	EXT_CLK	EXT_CLK	EXT_CLK
R640[1] 10K	R652[1] 10K	R665[1] 10K	R644[1] 10K	R683[1] 10K	R675[1] 10K	R658[1] 10K	R666[1] 10K
Spare	Spare	BIT2	BIT1	BIT0	1: Internal Spread Clock Active	0: PCI1_PLL1 Source Clock (NO SPREAD)	0: PCI0_PLL1 Source Clock (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

EXT_CLK	EXT_CLK	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
R133[1] 10K	R121[1] 10K	R163[1] 10K	R151[1] 10K	R162[1] 10K	R141[1] 10K	R183[1] 10K	R176[1] 10K
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

INT_CLK	INT_CLK	NO STUFF	NO STUFF
R645[1] 10K	R641[1] 10K	R668[1] 10K	R659[1] 10K	R667[1] 10K	R653[1] 10K	R684[1] 10K	R676[1] 10K
1: Active	1: External source	Spare	1: 139dB workaround; 0: No 139dB workaround	BIT2	BIT1	BIT0	Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R227 4.7 5% 1/16W MF 402

+1_5V_INTREPID_PLL → R227 → +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) CRITICAL

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

U45 INTREPID-REV2.1 BGA (1 OF 9)

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	

MAXBUS INTERFACE

CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - ? / NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU / NO BUS KEEPER - PU

INTREPID OUTPUTS HIGH BY DEFAULT

R197 511 1% 1/16W MF 402
R144 0 5% 1/16W MF 402 (SYSCLK_CPU1 → SYSCLK_CPU_UF)
R137 1K 1% 1/16W MF 402

H25 VSSA_7 (PLL6)

D_0	D10	CPU_DATA<0>	
D_1	G12	CPU_DATA<1>	
D_2	E11	CPU_DATA<2>	
D_3	H11	CPU_DATA<3>	
D_4	B9	CPU_DATA<4>	
D_5	B8	CPU_DATA<5>	
D_6	A9	CPU_DATA<6>	
D_7	A8	CPU_DATA<7>	
D_8	E12	CPU_DATA<8>	
D_9	D11	CPU_DATA<9>	
D_10	B10	CPU_DATA<10>	
D_11	J13	CPU_DATA<11>	
D_12	A10	CPU_DATA<12>	
D_13	D12	CPU_DATA<13>	
D_14	E13	CPU_DATA<14>	
D_15	G13	CPU_DATA<15>	
D_16	B11	CPU_DATA<16>	
D_17	D13	CPU_DATA<17>	
D_18	A11	CPU_DATA<18>	
D_19	G14	CPU_DATA<19>	
D_20	H14	CPU_DATA<20>	
D_21	E14	CPU_DATA<21>	
D_22	B12	CPU_DATA<22>	
D_23	G15	CPU_DATA<23>	
D_24	B13	CPU_DATA<24>	
D_25	H15	CPU_DATA<25>	
D_26	D14	CPU_DATA<26>	
D_27	B14	CPU_DATA<27>	
D_28	A12	CPU_DATA<28>	
D_29	G16	CPU_DATA<29>	
D_30	E15	CPU_DATA<30>	
D_31	J16	CPU_DATA<31>	
D_32	D15	CPU_DATA<32>	
D_33	A14	CPU_DATA<33>	
D_34	A13	CPU_DATA<34>	
D_35	D16	CPU_DATA<35>	
D_36	E16	CPU_DATA<36>	
D_37	G17	CPU_DATA<37>	
D_38	B15	CPU_DATA<38>	
D_39	H17	CPU_DATA<39>	
D_40	A15	CPU_DATA<40>	
D_41	B16	CPU_DATA<41>	
D_42	E17	CPU_DATA<42>	
D_43	A16	CPU_DATA<43>	
D_44	J18	CPU_DATA<44>	
D_45	H18	CPU_DATA<45>	
D_46	D17	CPU_DATA<46>	
D_47	G18	CPU_DATA<47>	
D_48	A17	CPU_DATA<48>	
D_49	B17	CPU_DATA<49>	
D_50	E18	CPU_DATA<50>	
D_51	B18	CPU_DATA<51>	
D_52	D18	CPU_DATA<52>	
D_53	A18	CPU_DATA<53>	
D_54	A19	CPU_DATA<54>	
D_55	H19	CPU_DATA<55>	
D_56	B19	CPU_DATA<56>	
D_57	J19	CPU_DATA<57>	
D_58	A20	CPU_DATA<58>	
D_59	D19	CPU_DATA<59>	
D_60	E19	CPU_DATA<60>	
D_61	G19	CPU_DATA<61>	
D_62	B20	CPU_DATA<62>	
D_63	G20	CPU_DATA<63>	
DBG	A30	CPU_DBG_L	
DRDY	G28	CPU_DRDY_L	
DTI_0	K25	CPU_DTI<0>	
DTI_1	D29	CPU_DTI<1>	
DTI_2	B30	CPU_DTI<2>	
TA	E27	CPU_TA_L	
TEA	E28	CPU_TEA_L	

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R167 0 5% 1/16W MF 402 (INT_CPUFB_OUT2 → INT_CPUFB_OUT_SHORT)
R215 0 5% 1/16W MF 402 (INT_CPUFB_OUT_SHORT → INT_CPUFB_OUT_NORM)
R207 0 5% 1/16W MF 402 (INT_CPUFB_OUT_NORM → INT_CPUFB_LONG)
NO STUFF R225 0 5% 1/16W MF 402 (INT_CPUFB_OUT_SHORT → INT_CPUFB_IN)
R208 0 5% 1/16W MF 402 (INT_CPUFB_OUT_NORM → INT_CPUFB_IN_NORM)
R226 0 5% 1/16W MF 402 (INT_CPUFB_IN → INT_CPUFB_IN_NORM)
NO STUFF R196 0 5% 1/16W MF 402 (INT_CPUFB_IN_NORM → INT_CPUFB_LONG)

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K	2 7
CPU_TA_L	RP21 10K	1 8
CPU_ARTRY_L	RP21 10K	4 5
CPU_BR_L	RP23 10K	1 8
CPU_HIT_L	RP24 10K	3 6
CPU_DRDY_L	RP23 10K	3 6
CPU_TEA_L	RP23 10K	4 5
CPU_AACK_L	RP23 10K	2 7
CPU_DBG_L	RP24 10K	4 5
CPU_BG_L	RP21 10K	3 6
CPU_QREQ_L	RP24 10K	2 7

All: 5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
R140[1] 10K	R161[1] 10K	R175[1] 10K	R132[1] 10K	R131[1] 10K	R150[1] 10K	R174[1] 10K	R182[1] 10K
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

NO STUFF

R654[1] 10K	R669[1] 10K	R677[1] 10K	R646[1] 10K	R647[1] 10K	R660[1] 10K	R678[1] 10K	R685[1] 10K
Spare	Spare	Spare	0: PCI1_REQ1_L / GPIO6; 1: PCI1_GNT2_L	0: PCI1_REQ1_L / GPIO5; 1: PCI1_GNT1_L	0: PCI1_REQ0_L / GPIO4; 1: PCI1_GNT0_L	0: Legacy PHY interface; 1: B-mode interface	0: Processor Bus Mode; 1: 60x Bus (603)

All: 5% 1/16W MF 402

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 8 OF 45	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

CRITICAL
U45
INTREPID-REV2.1
BGA
(2 OF 9)

MEM_DATA<0>	AK32	DDR_DATA_0	H35	DDR_A_0	MEM_ADDR<0>
MEM_DATA<1>	AK33	DDR_DATA_1	G35	DDR_A_1	MEM_ADDR<1>
MEM_DATA<2>	AK31	DDR_DATA_2	G36	DDR_A_2	MEM_ADDR<2>
MEM_DATA<3>	AK35	DDR_DATA_3	F36	DDR_A_3	MEM_ADDR<3>
MEM_DATA<4>	AK36	DDR_DATA_4	F35	DDR_A_4	MEM_ADDR<4>
MEM_DATA<5>	AJ32	DDR_DATA_5	E35	DDR_A_5	MEM_ADDR<5>
MEM_DATA<6>	AJ35	DDR_DATA_6	E36	DDR_A_6	MEM_ADDR<6>
MEM_DATA<7>	AJ36	DDR_DATA_7	G32	DDR_A_7	MEM_ADDR<7>
MEM_DATA<8>	AG33	DDR_DATA_8	D36	DDR_A_8	MEM_ADDR<8>
MEM_DATA<9>	AG35	DDR_DATA_9	H36	DDR_A_9	MEM_ADDR<9>
MEM_DATA<10>	AH35	DDR_DATA_10	G33	DDR_A_10	MEM_ADDR<10>
MEM_DATA<11>	AG36	DDR_DATA_11	H33	DDR_A_11	MEM_ADDR<11>
MEM_DATA<12>	AH36	DDR_DATA_12	D35	DDR_A_12	MEM_ADDR<12>
MEM_DATA<13>	AH32	DDR_DATA_13	L30	DDR_BA_0	MEM_BA<0>
MEM_DATA<14>	AG32	DDR_DATA_14	M29	DDR_BA_1	MEM_BA<1>
MEM_DATA<15>	AG31	DDR_DATA_15			
MEM_DATA<16>	AE32	DDR_DATA_16	AN34	DDRCS_0	MEM_CS_L<0>
MEM_DATA<17>	AF35	DDR_DATA_17	AN36	DDRCS_1	MEM_CS_L<1> '0' & '1' GO TO SLOT A
MEM_DATA<18>	AF36	DDR_DATA_18	AL35	DDRCS_2	MEM_CS_L<2> '2' & '3' GO TO SLOT B
MEM_DATA<19>	AE36	DDR_DATA_19	AL33	DDRCS_3	MEM_CS_L<3>
MEM_DATA<20>	AE35	DDR_DATA_20	AJ31	DDR_DQS_0	MEM_DQS<0>
MEM_DATA<21>	AE33	DDR_DATA_21	AH31	DDR_DQS_1	MEM_DQS<1>
MEM_DATA<22>	AD36	DDR_DATA_22	AD32	DDR_DQS_2	MEM_DQS<2>
MEM_DATA<23>	AD35	DDR_DATA_23	AB30	DDR_DQS_3	MEM_DQS<3>
MEM_DATA<24>	AA36	DDR_DATA_24	V30	DDR_DQS_4	MEM_DQS<4>
MEM_DATA<25>	AA35	DDR_DATA_25	P32	DDR_DQS_5	MEM_DQS<5>
MEM_DATA<26>	AA33	DDR_DATA_26	N29	DDR_DQS_6	MEM_DQS<6>
MEM_DATA<27>	AB36	DDR_DATA_27	L32	DDR_DQS_7	MEM_DQS<7>
MEM_DATA<28>	AB35	DDR_DATA_28	AJ33	DDR_DM_0	MEM_DQM<0>
MEM_DATA<29>	AC36	DDR_DATA_29	AH33	DDR_DM_1	MEM_DQM<1>
MEM_DATA<30>	AA32	DDR_DATA_30	AD33	DDR_DM_2	MEM_DQM<2>
MEM_DATA<31>	AB33	DDR_DATA_31	AC35	DDR_DM_3	MEM_DQM<3>
MEM_DATA<32>	V36	DDR_DATA_32	T35	DDR_DM_4	MEM_DQM<4>
MEM_DATA<33>	U33	DDR_DATA_33	T33	DDR_DM_5	MEM_DQM<5>
MEM_DATA<34>	U32	DDR_DATA_34	N32	DDR_DM_6	MEM_DQM<6>
MEM_DATA<35>	V35	DDR_DATA_35	L33	DDR_DM_7	MEM_DQM<7>
MEM_DATA<36>	T30	DDR_DATA_36	L29	DDRRAS	MEM_RAS_L
MEM_DATA<37>	U36	DDR_DATA_37	H32	DDRCAS	MEM_CAS_L
MEM_DATA<38>	U35	DDR_DATA_38	K30	DDRWE	MEM_WE_L
MEM_DATA<39>	T36	DDR_DATA_39	AN35	DDRCKE0	MEM_CKE<0>
MEM_DATA<40>	P33	DDR_DATA_40	AM35	DDRCKE1	MEM_CKE<1> '0' & '1' GO TO SLOT A
MEM_DATA<41>	R30	DDR_DATA_41	AM36	DDRCKE2	MEM_CKE<2> '2' & '3' GO TO SLOT B
MEM_DATA<42>	P35	DDR_DATA_42	AL36	DDRCKE3	MEM_CKE<3>
MEM_DATA<43>	P36	DDR_DATA_43	AB32	DDR_SELHI_0	MEM_MUXSEL_H<0>
MEM_DATA<44>	R36	DDR_DATA_44	AE29	DDR_SELHI_1	MEM_MUXSEL_H<1> '0'S ARE SAME POLARITY (ACTIVE-LO)
MEM_DATA<45>	R35	DDR_DATA_45	N30	DDR_SELLO_0	MEM_MUXSEL_L<0> '1'S ARE SAME POLARITY (ACTIVE-HI)
MEM_DATA<46>	R33	DDR_DATA_46	T32	DDR_SELLO_1	MEM_MUXSEL_L<1>
MEM_DATA<47>	R32	DDR_DATA_47	Y32	DDR_MCLK_0_P	SYSCLK_DDRCLK_A0_UF
MEM_DATA<48>	N35	DDR_DATA_48	Y33	DDR_MCLK_0_N	SYSCLK_DDRCLK_A0_L_UF
MEM_DATA<49>	M36	DDR_DATA_49	Y35	DDR_MCLK_1_P	SYSCLK_DDRCLK_A1_UF
MEM_DATA<50>	L35	DDR_DATA_50	Y36	DDR_MCLK_1_N	SYSCLK_DDRCLK_A1_L_UF
MEM_DATA<51>	M35	DDR_DATA_51	Y30	DDR_MCLK_2_P	INT_DDRCLK2_P_TP
MEM_DATA<52>	M33	DDR_DATA_52	W30	DDR_MCLK_2_N	INT_DDRCLK2_N_TP
MEM_DATA<53>	L36	DDR_DATA_53	W32	DDR_MCLK_3_P	SYSCLK_DDRCLK_B0_UF
MEM_DATA<54>	N33	DDR_DATA_54	W33	DDR_MCLK_3_N	SYSCLK_DDRCLK_B0_L_UF
MEM_DATA<55>	M30	DDR_DATA_55	V33	DDR_MCLK_4_P	SYSCLK_DDRCLK_B1_UF
MEM_DATA<56>	J32	DDR_DATA_56	V32	DDR_MCLK_4_N	SYSCLK_DDRCLK_B1_L_UF
MEM_DATA<57>	J33	DDR_DATA_57	W35	DDR_MCLK_5_P	INT_DDRCLK5_P_TP
MEM_DATA<58>	J35	DDR_DATA_58	W36	DDR_MCLK_5_N	INT_DDRCLK5_N_TP
MEM_DATA<59>	K32	DDR_DATA_59	AA22	DDR_REF	INT_MEM_REF_H
MEM_DATA<60>	K33	DDR_DATA_60	Y22	DDR_VREF_0	INT_MEM_VREF
MEM_DATA<61>	J36	DDR_DATA_61	T22	DDR_VREF_1	
MEM_DATA<62>	K36	DDR_DATA_62			
MEM_DATA<63>	K35	DDR_DATA_63			

DDR MEMORY INTERFACE

MEM_VREF

+2_5V_INTREPID

R198 10K 1% 1/16W MF 402

R191 10K 1% 1/16W MF 402

C245 0.1UF 20% 10V CERM 402

INT_MEM_VREF

R199 1K 1% 1/16W MF 402

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33	22	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP33	22	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP34	22	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP34	22	SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP33	22	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP33	22	SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP34	22	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP34	22	SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP36	22	RAM_CS_L<0>
MEM_CS_L<1>	RP36	22	RAM_CS_L<1>
MEM_CS_L<2>	RP35	22	RAM_CS_L<2>
MEM_CS_L<3>	RP35	22	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP36	22	RAM_CKE<0>
MEM_CKE<1>	RP36	22	RAM_CKE<1>
MEM_CKE<2>	RP35	22	RAM_CKE<2>
MEM_CKE<3>	RP35	22	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP31	22	RAM_ADDR<0>
MEM_ADDR<1>	RP25	22	RAM_ADDR<1>
MEM_ADDR<2>	RP25	22	RAM_ADDR<2>
MEM_ADDR<3>	RP25	22	RAM_ADDR<3>
MEM_ADDR<4>	RP25	22	RAM_ADDR<4>
MEM_ADDR<5>	RP30	22	RAM_ADDR<5>
MEM_ADDR<6>	RP30	22	RAM_ADDR<6>
MEM_ADDR<7>	RP31	22	RAM_ADDR<7>
MEM_ADDR<8>	RP30	22	RAM_ADDR<8>
MEM_ADDR<9>	RP31	22	RAM_ADDR<9>
MEM_ADDR<10>	RP31	22	RAM_ADDR<10>
MEM_ADDR<11>	RP26	22	RAM_ADDR<11>
MEM_ADDR<12>	RP30	22	RAM_ADDR<12>

BA

MEM_BA<0>	RP26	22	RAM_BA<0>
MEM_BA<1>	RP26	22	RAM_BA<1>

CNTL

MEM_WE_L	RP26	22	RAM_WE_L
MEM_CAS_L	R250	22	RAM_CAS_L
MEM_RAS_L	R238	22	RAM_RAS_L

All RP22 resistors: 5% 1/16W SM1

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805

C470 0.1UF 20% 10V CERM 402

C479 0.1UF 20% 10V CERM 402

U17
FEPR-1MX8
3.3V
TSOP
OMIT

PCI_AD<0>	21	A0	DQ0
PCI_AD<1>	20	A1	DQ1
PCI_AD<2>	19	A2	DQ2
PCI_AD<3>	18	A3	DQ3
PCI_AD<4>	17	A4	DQ4
PCI_AD<5>	16	A5	DQ5
PCI_AD<6>	15	A6	DQ6
PCI_AD<7>	14	A7	DQ7
PCI_AD<8>	8	A8	
PCI_AD<9>	7	A9	
PCI_AD<10>	36	A10	
PCI_AD<11>	6	A11	
PCI_AD<12>	5	A12	
PCI_AD<13>	4	A13	
PCI_AD<14>	3	A14	
PCI_AD<15>	2	A15	
PCI_AD<16>	1	A16	
PCI_AD<17>	40	A17	
PCI_AD<18>	13	A18	
PCI_AD<19>	37	A19	
PCI_AD<20>	38	A20	
ROM_ONBOARD_CS_L	22	CE	
ROM_OE_L	24	OE	
ROM_RW_L	9	WE	
ROM_WP_L	12	WP	
INT_RESET_L	10	PWD	
	23, 39	GND	

VPP = 11, VCC = 30, 31

+3V_MAIN

R338 10K 5% 1/16W MF 402

R386 10K 5% 1/16W MF 402

R357 1K 5% 1/16W MF 402

ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1556	1	IC,BOOTROM,Q41B	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R500 10K 5% 1/16W MF 402

R439 10K 5% 1/16W MF 402

R409 10K 5% 1/16W MF 402

R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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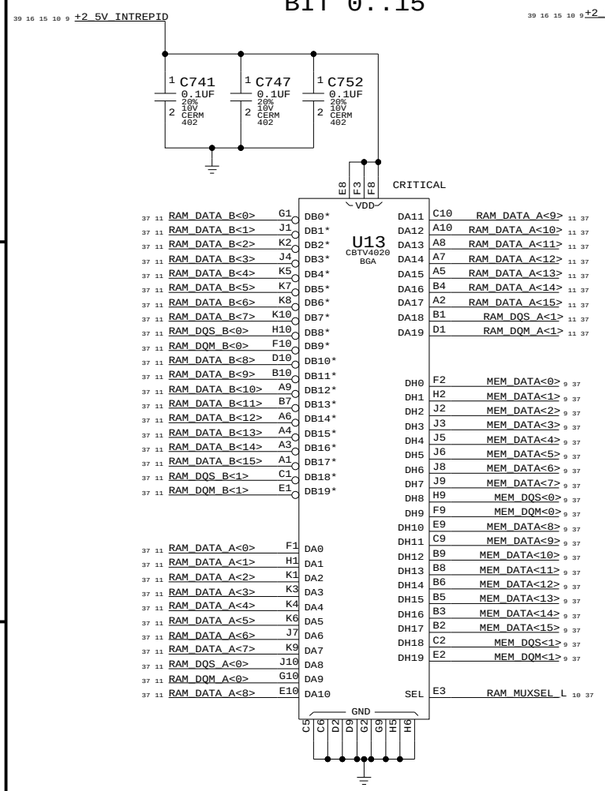
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE: NONE

SHT 9 OF 45



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND

SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW

MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

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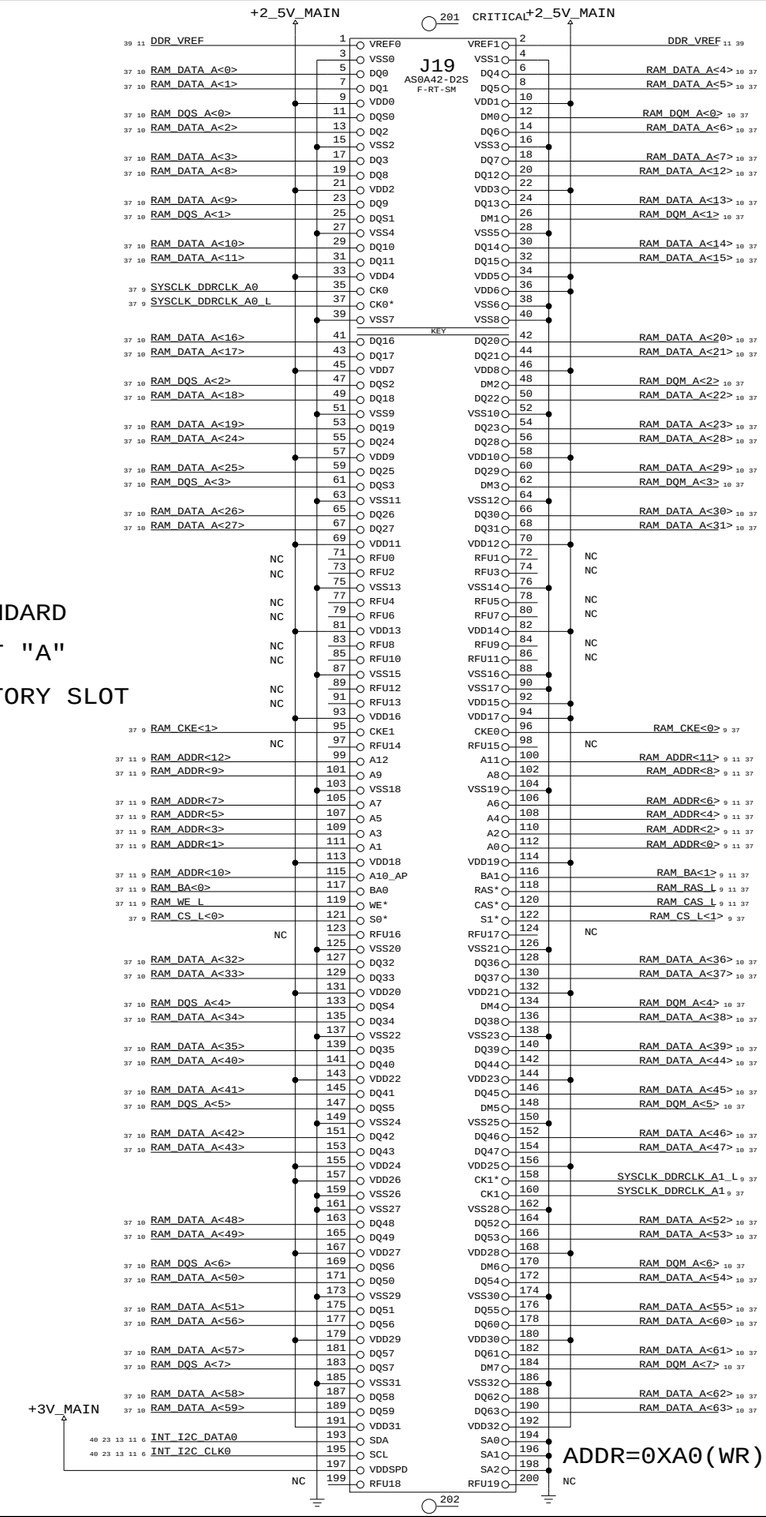
SIZE	DRAWING NUMBER	REV.
D	051-6694	02

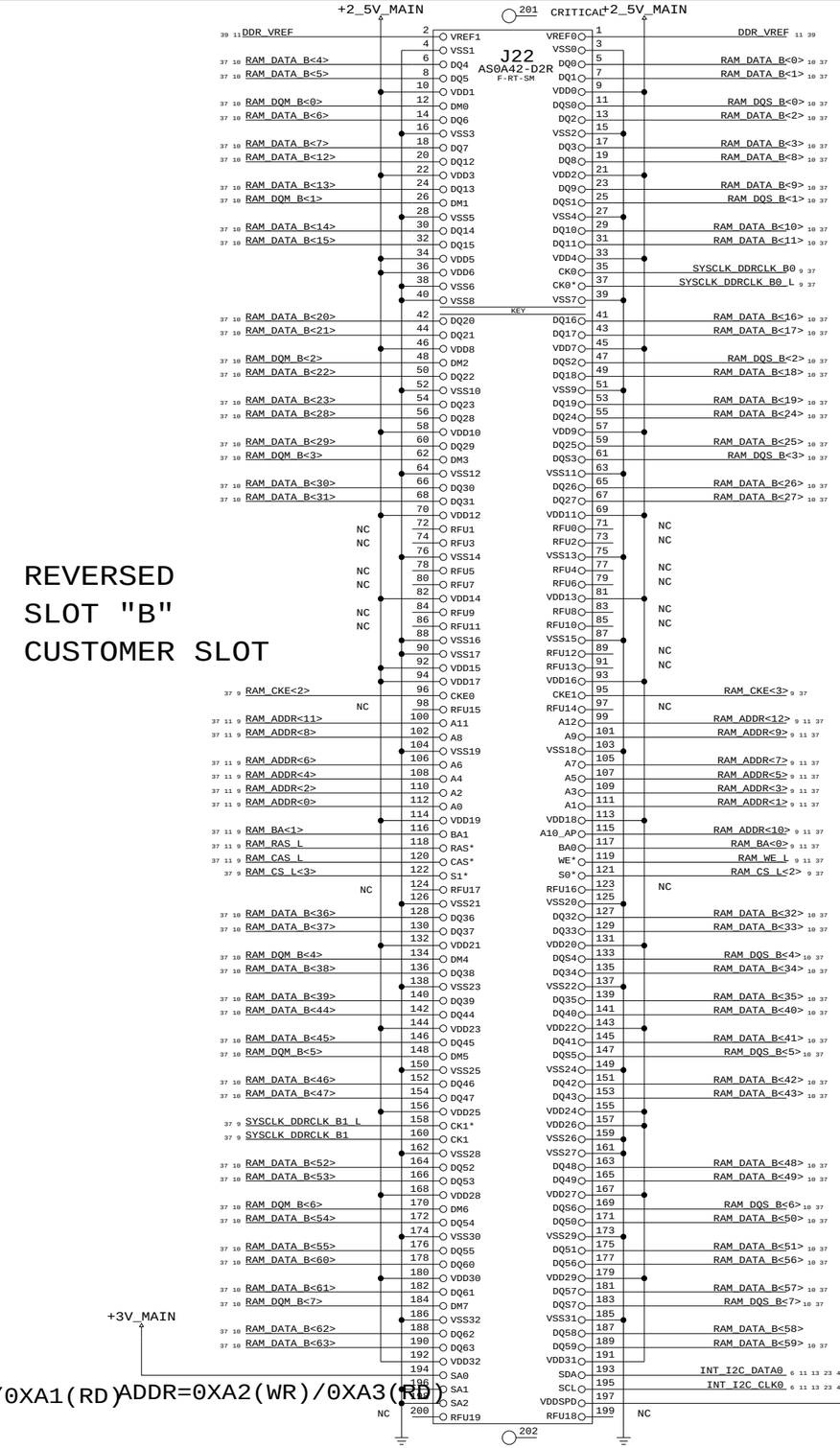
SCALE	SHT	OF
NONE	10	45



STANDARD

SLOT "A"

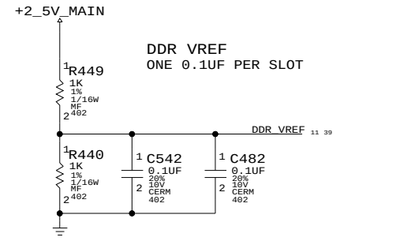
FACTORY SLOT

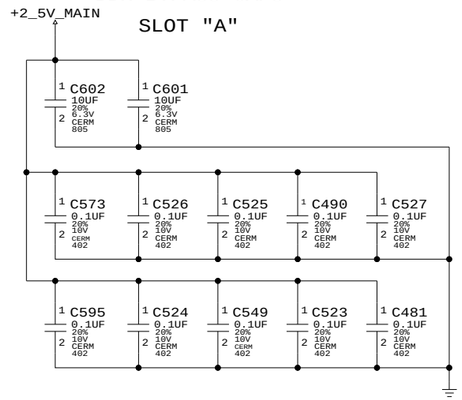


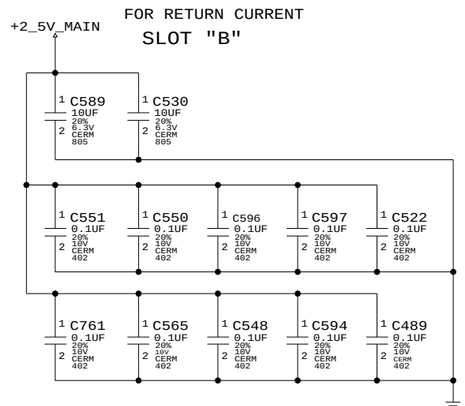
REVERSED

SLOT "B"

CUSTOMER SLOT







DDR SODIMM CONNS

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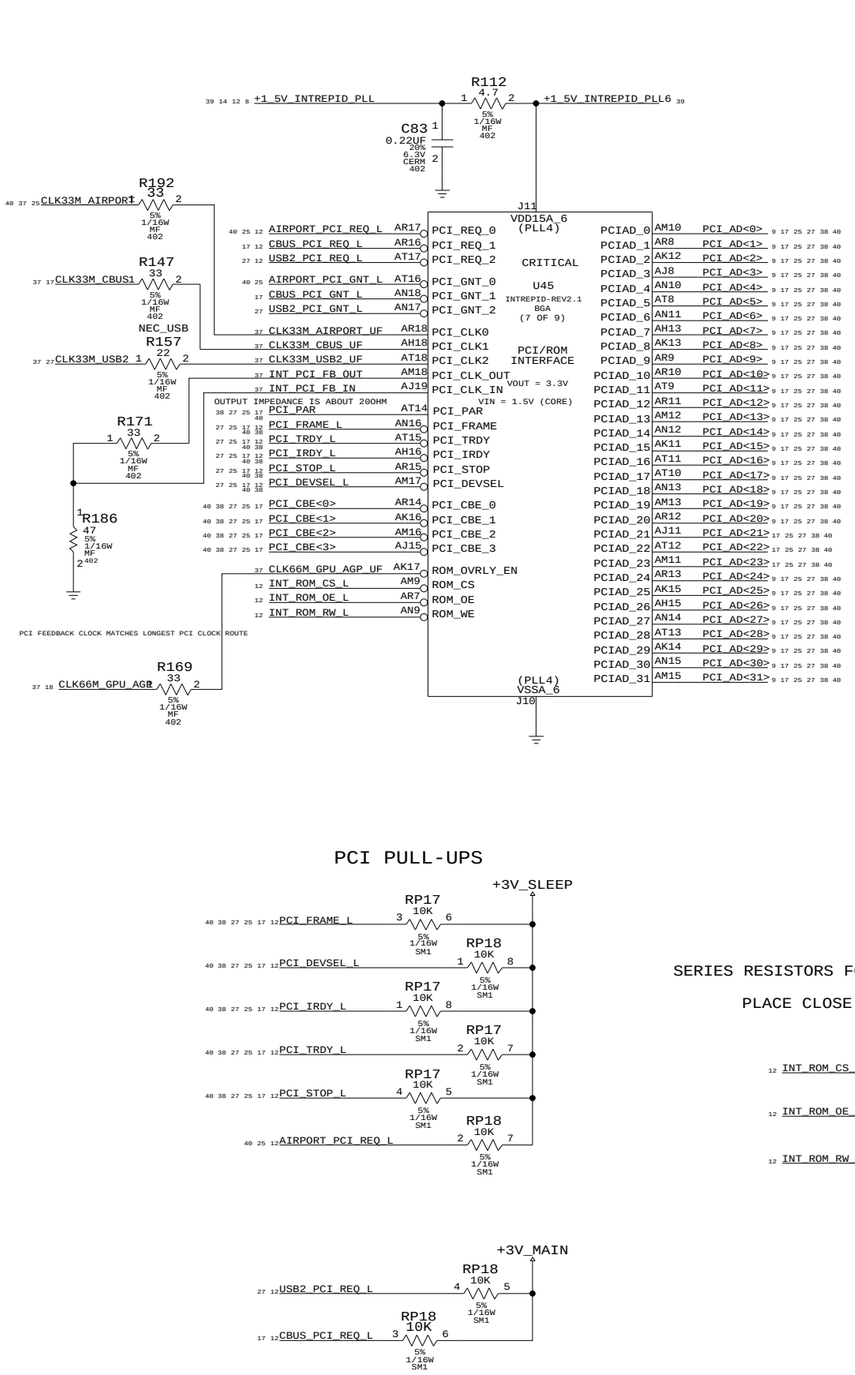
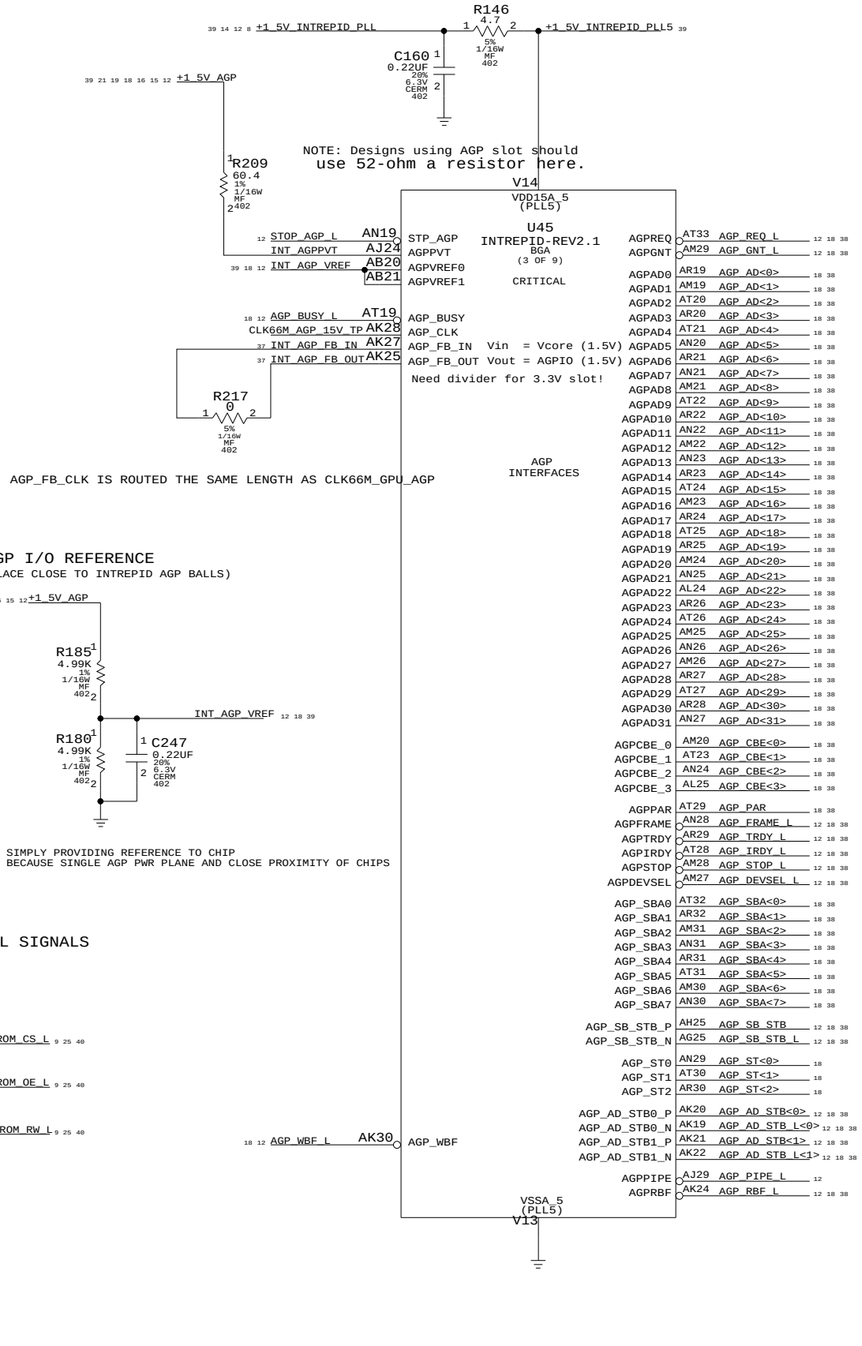
APPLE COMPUTER INC.

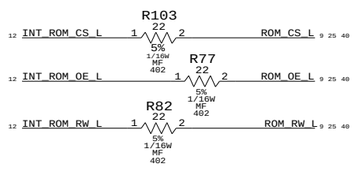
SIZE	DRAWING NUMBER	REV.
D	051-6694	02

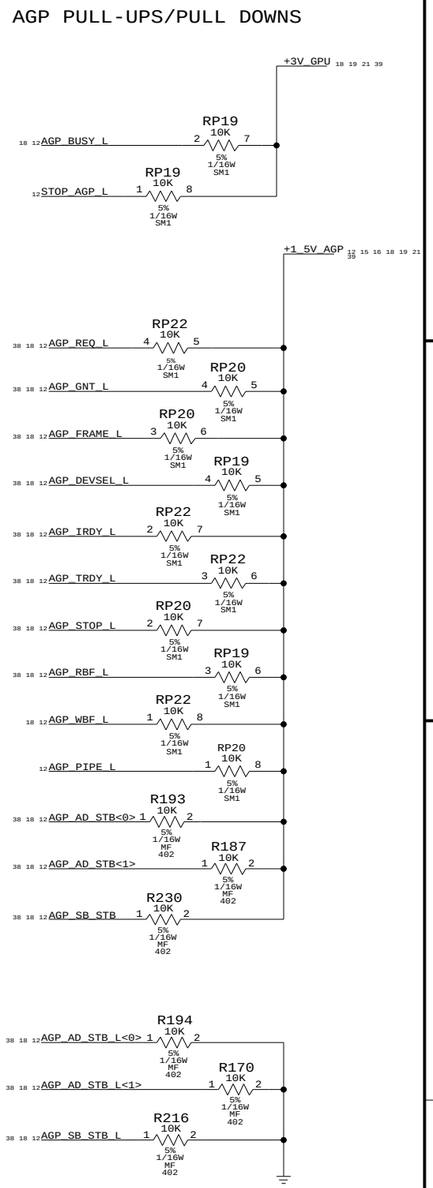
SCALE: NONE

SHT 11 OF 45









USB2 AND CBUS REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP

INTREPID AGP/PCI

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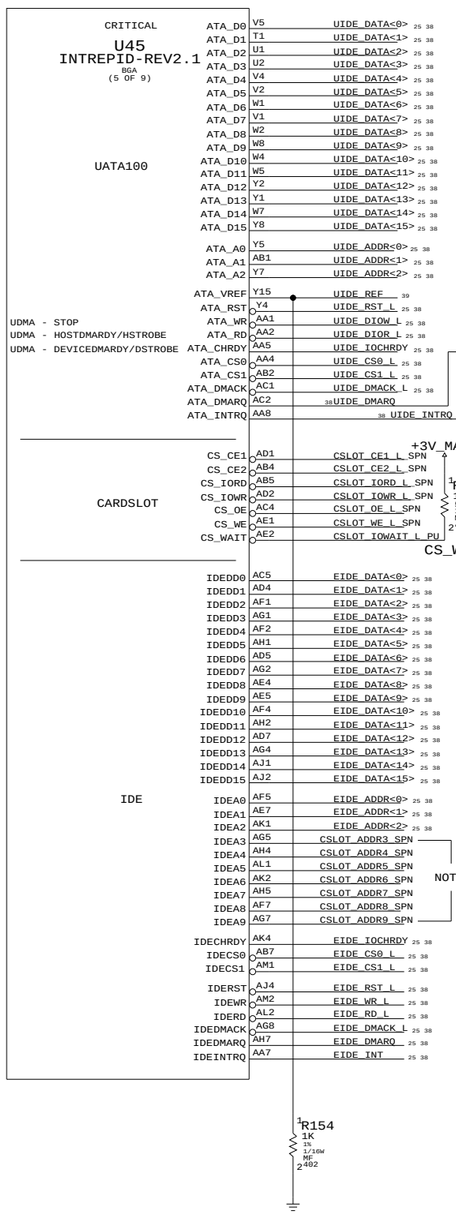
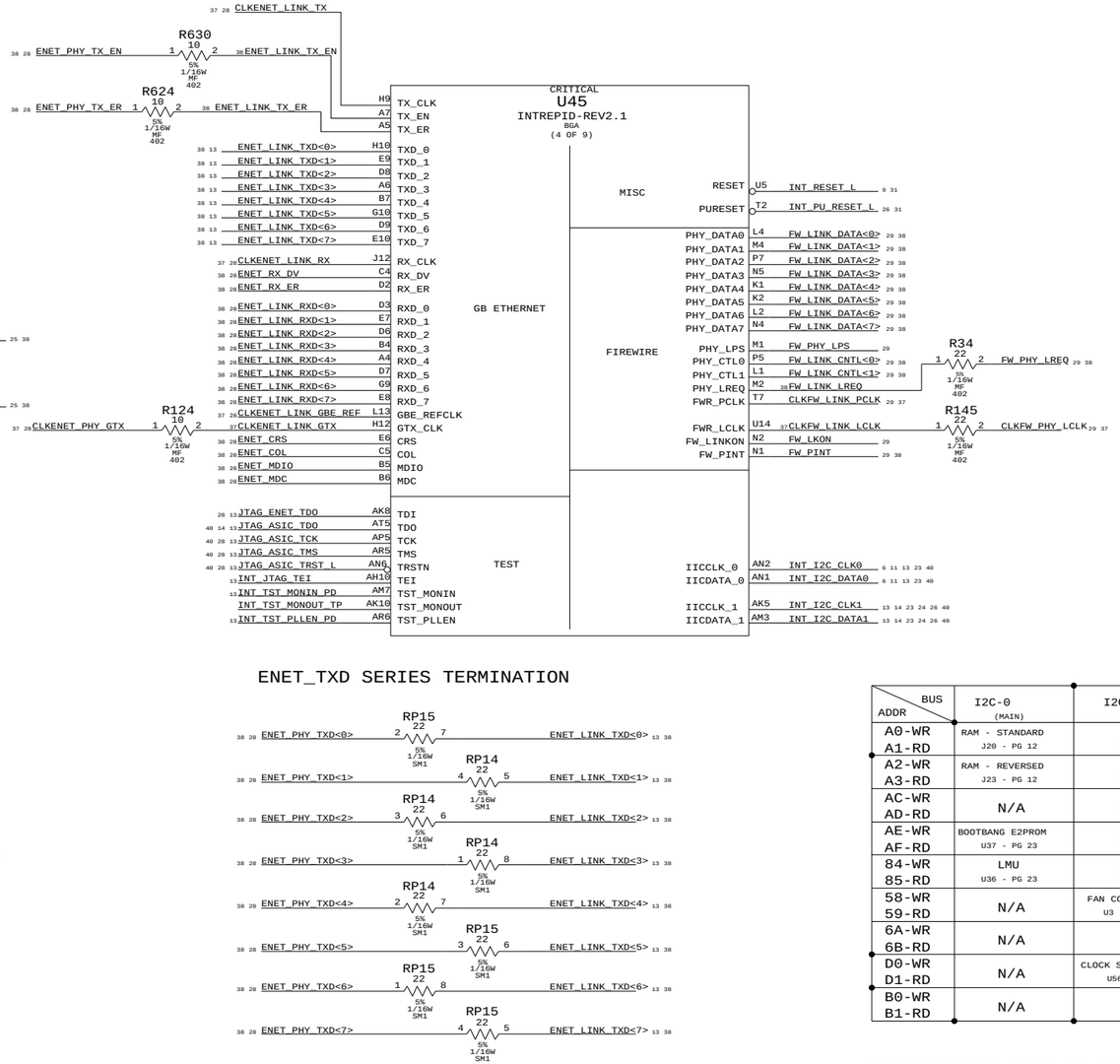
APPLE COMPUTER INC.

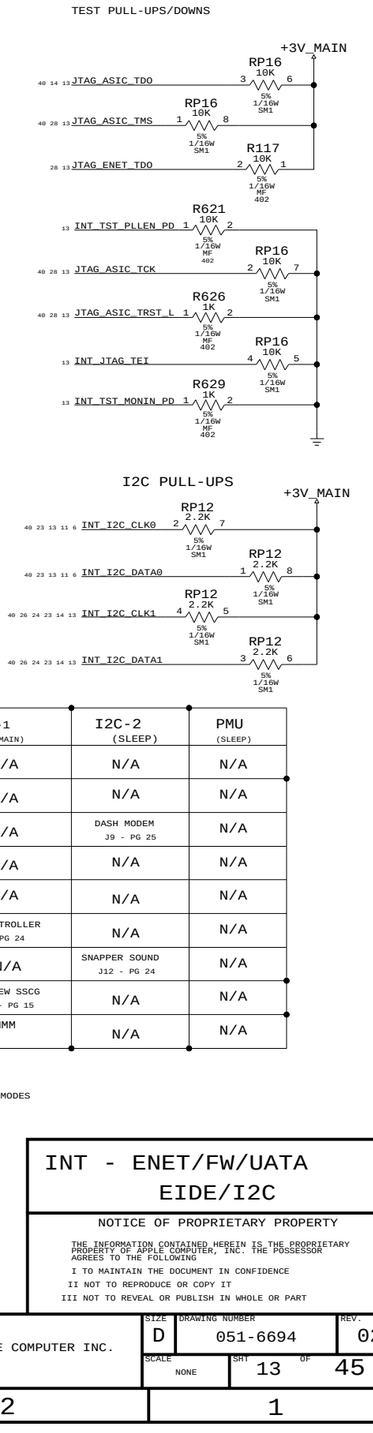
SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE: NONE

SHT 12 OF 45







ENET_TXD SERIES TERMINATION

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
B0-WR B1-RD	N/A	MMM	N/A	N/A

ADDR LSB INDICATES READ (‘1’) OR WRITE (‘0’) MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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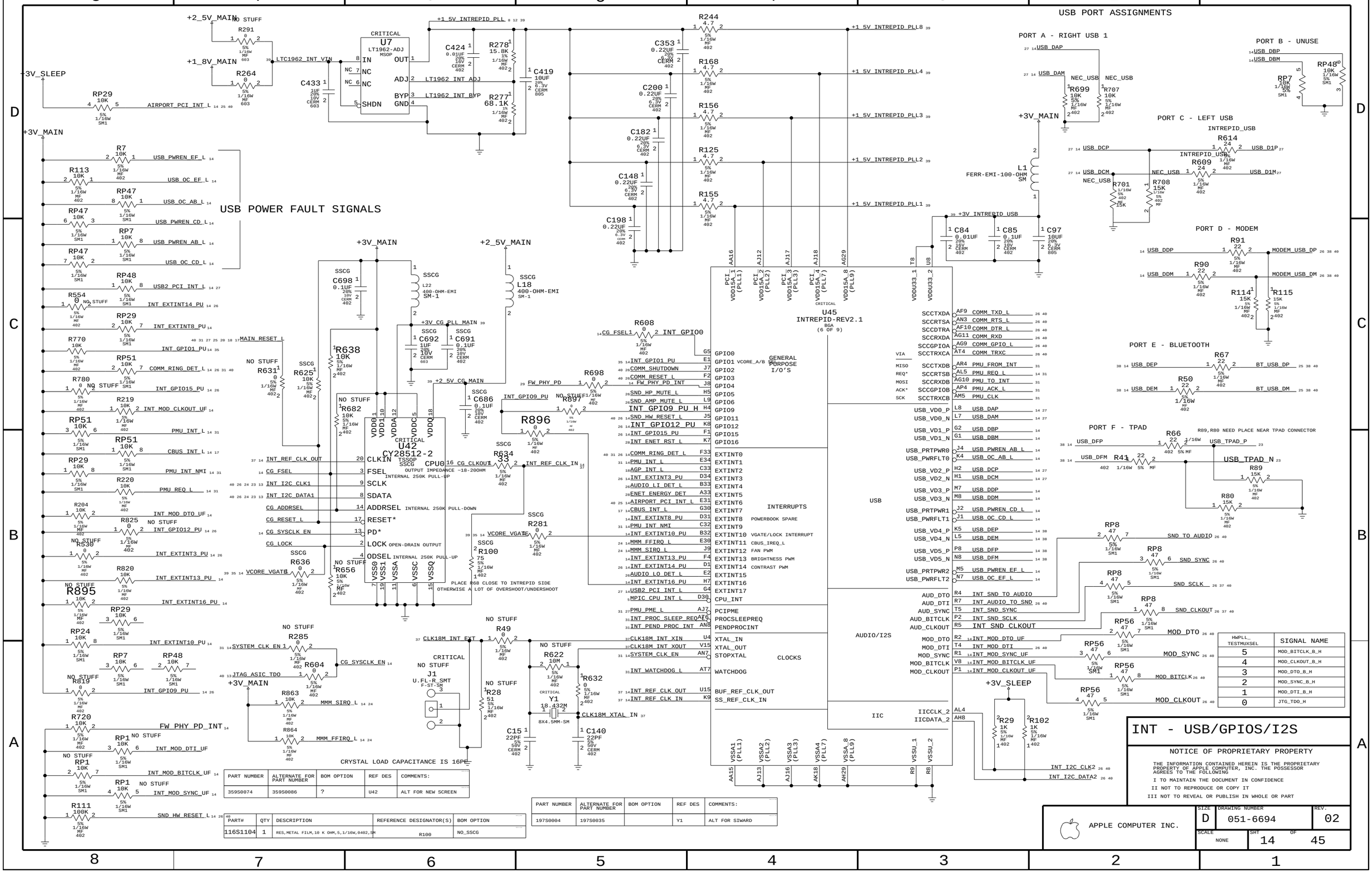
D	051-6694	02

SCALE: NONE

SHT 13 OF 45

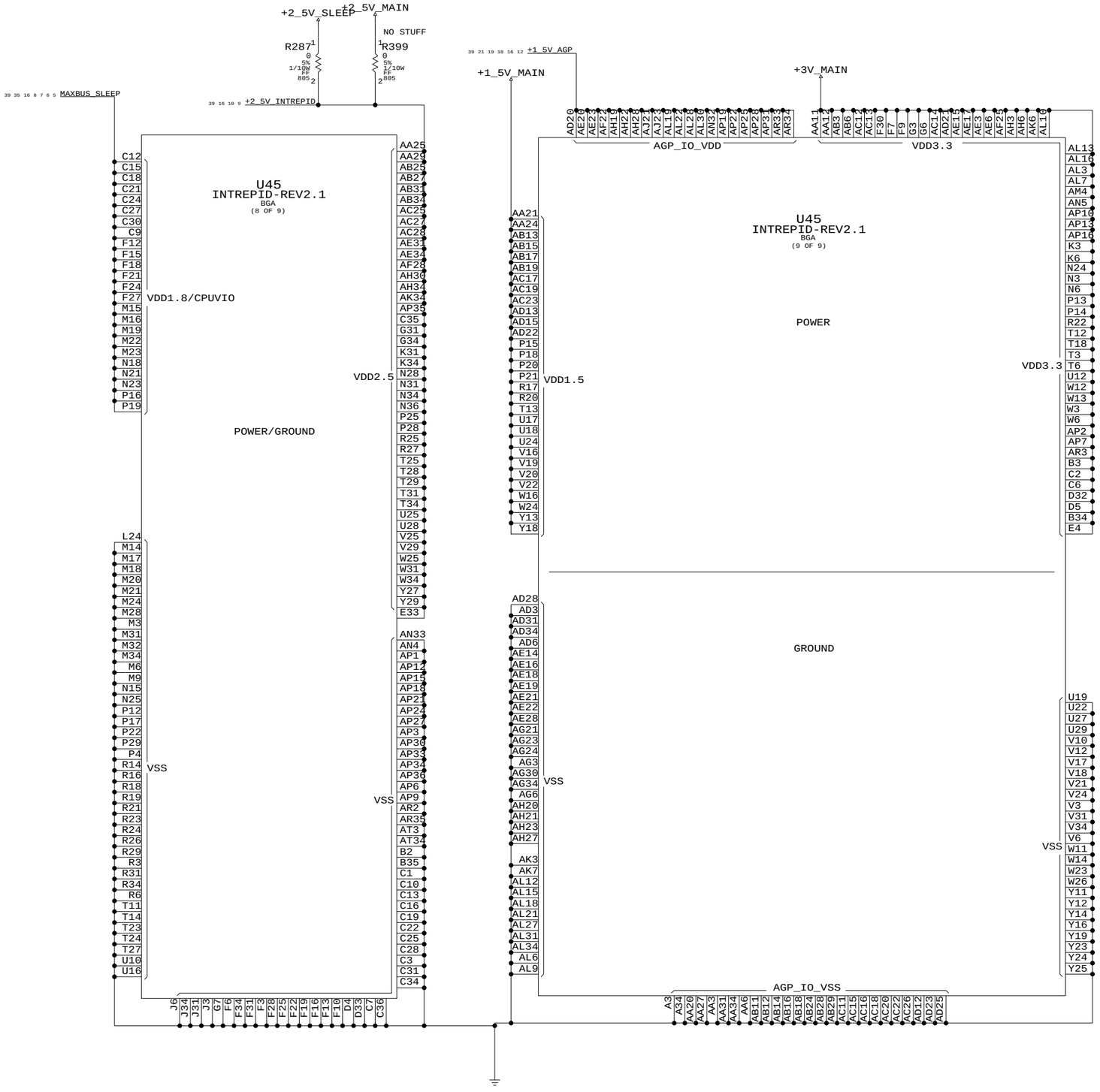


HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG



Intrepid Power

APPLE COMPUTER INC.

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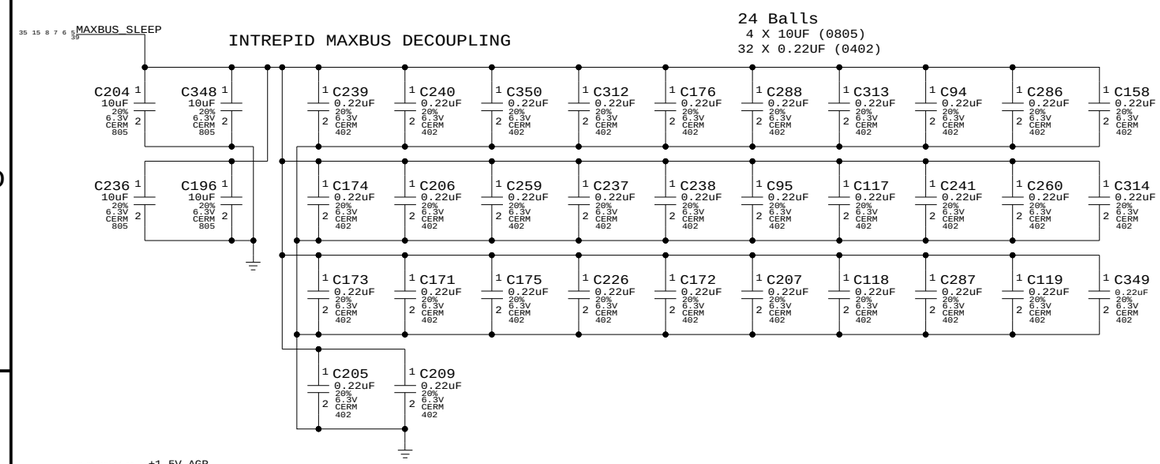
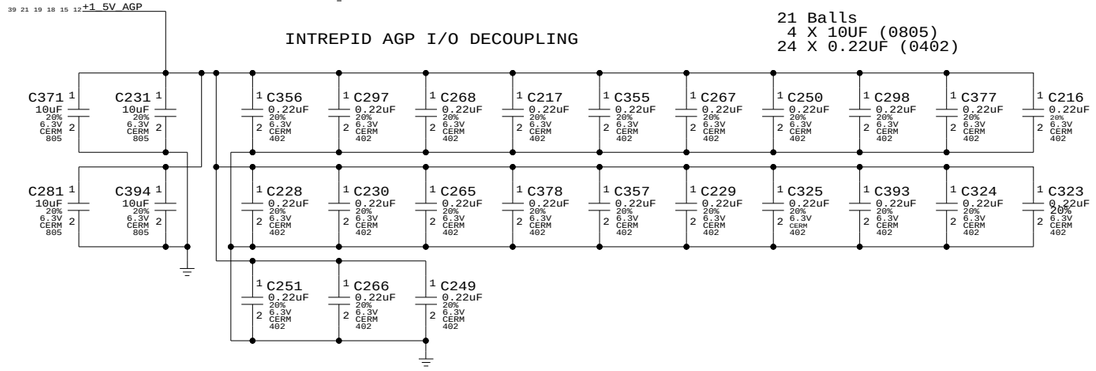
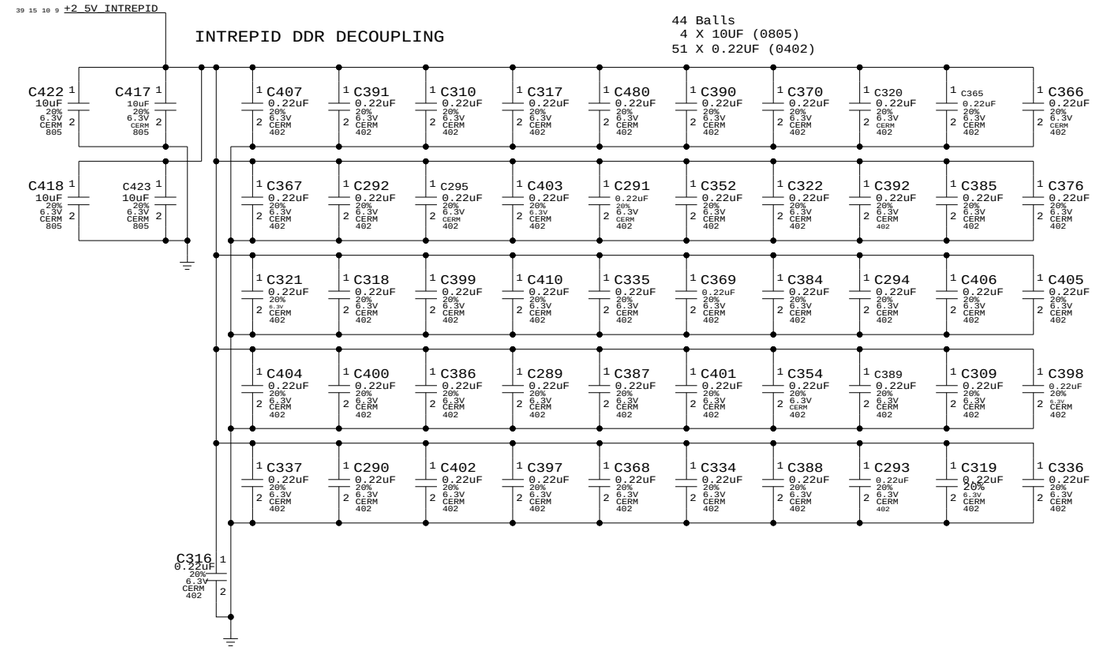
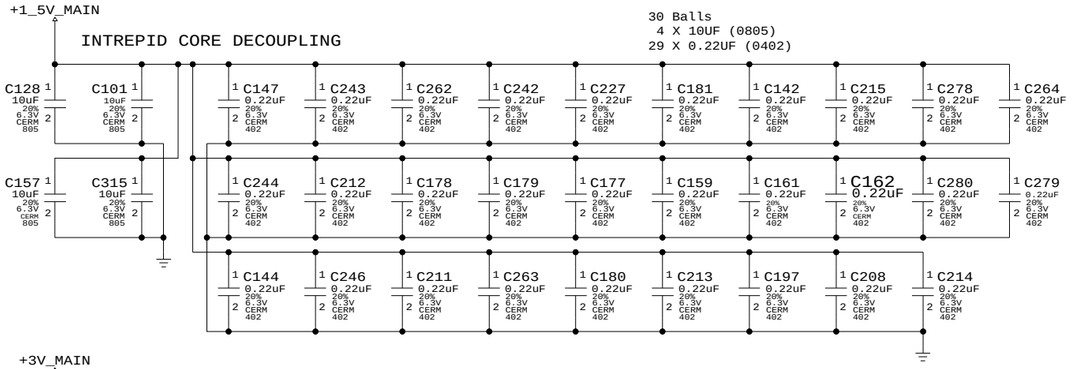
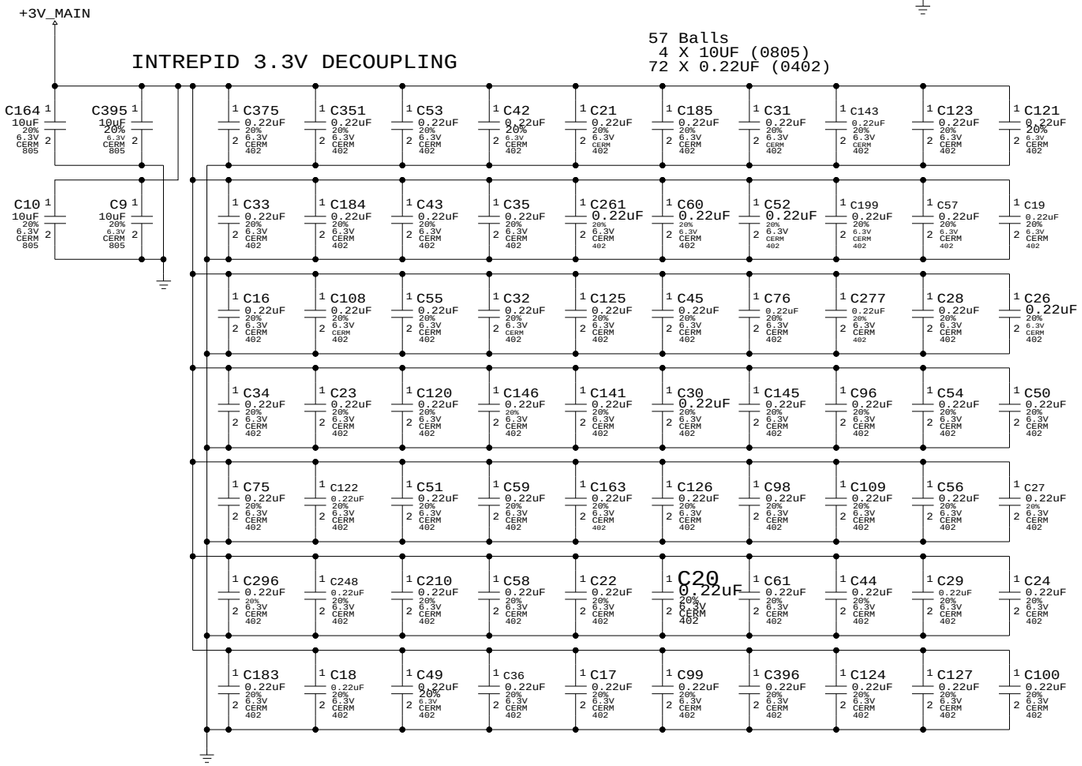
D	051-6694	02
SCALE: NONE	SHT 15 OF 45	











Intrepid Decoupling

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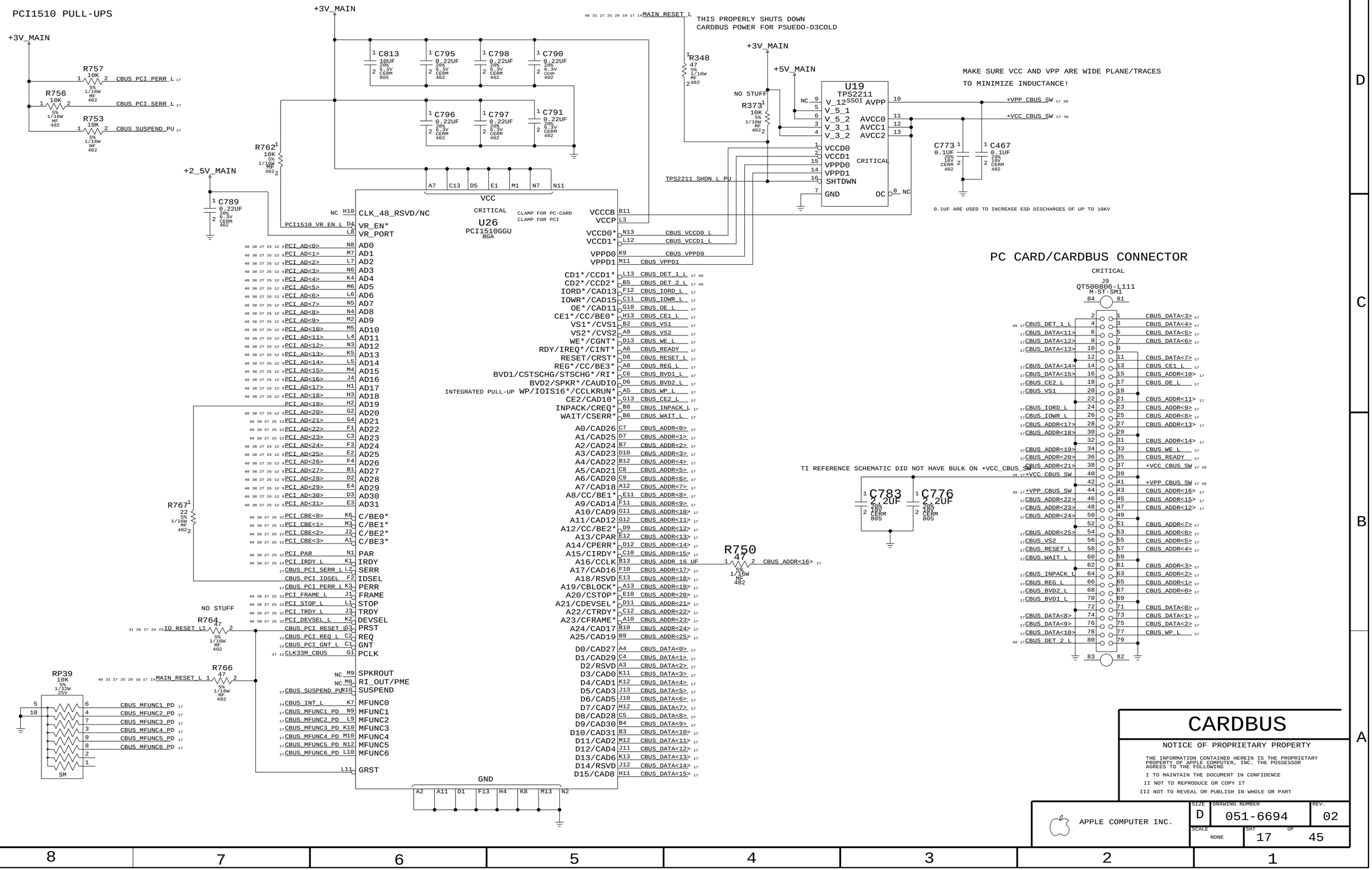
SCALE	SHT	OF
NONE	16	45


PCI1510 PULL-UPS
+3V_MAIN
R757 10K 5% 1/16W MF 402 CBUS_PCI_PERR_L
R756 10K 5% 1/16W MF 402 CBUS_PCI_SERR_L
R753 10K 5% 1/16W MF 402 CBUS_SUSPEND_PU
+3V_MAIN
C813 10UF 20% 6.3V CERM 805
C795 0.22UF 20% 6.3V CERM 402
C798 0.22UF 20% 6.3V CERM 402
C790 0.22UF 20% 6.3V CERM 402
C796 0.22UF 20% 6.3V CERM 402
C797 0.22UF 20% 6.3V CERM 402
C791 0.22UF 20% 6.3V CERM 402
R762 10K 5% 1/16W MF 402
+2_5V_MAIN
C789 0.22UF 20% 6.3V CERM 402
A7 C13 D5 E1 M1 N7 N11
VCC
NC H10 CLK_48_RSVD/NC
PCI1510_VR_EN_L D4 VR_EN*
L8 VR_PORT
CRITICAL
U26
PCI1510GGU
BGA
CLAMP FOR PC-CARD
CLAMP FOR PCI
PCI_AD<0> N8 AD0
PCI_AD<1> M7 AD1
PCI_AD<2> L7 AD2
PCI_AD<3> N6 AD3
PCI_AD<4> K4 AD4
PCI_AD<5> M6 AD5
PCI_AD<6> L6 AD6
PCI_AD<7> N5 AD7
PCI_AD<8> N4 AD8
PCI_AD<9> M2 AD9
PCI_AD<10> M5 AD10
PCI_AD<11> L4 AD11
PCI_AD<12> N3 AD12
PCI_AD<13> K5 AD13
PCI_AD<14> L5 AD14
PCI_AD<15> M4 AD15
PCI_AD<16> J4 AD16
PCI_AD<17> H1 AD17
PCI_AD<18> H3 AD18
PCI_AD<19> H2 AD19
PCI_AD<20> G2 AD20
PCI_AD<21> G4 AD21
PCI_AD<22> F1 AD22
PCI_AD<23> C3 AD23
PCI_AD<24> F3 AD24
PCI_AD<25> E2 AD25
PCI_AD<26> F4 AD26
PCI_AD<27> B1 AD27
PCI_AD<28> D2 AD28
PCI_AD<29> E4 AD29
PCI_AD<30> D3 AD30
PCI_AD<31> E3 AD31
R767 22 5% 1/16W MF 402
PCI_CBE<0> K6 C/BE0*
PCI_CBE<1> M3 C/BE1*
PCI_CBE<2> J2 C/BE2*
PCI_CBE<3> A1 C/BE3*
PCI_PAR N1 PAR
PCI_IRDY_L K1 IRDY
CBUS_PCI_SERR_L L2 SERR
CBUS_PCI_IDSEL F2 IDSEL
CBUS_PCI_PERR_L K3 PERR
PCI_FRAME_L J1 FRAME
PCI_STOP_L L1 STOP
PCI_TRDY_L J3 TRDY
PCI_DEVSEL_L K2 DEVSEL
NO STUFF
R764 47 5% 1/16W MF 402
IO_RESET_L1
CBUS_PCI_RESET_L G3 PRST
CBUS_PCI_REQ_L C2 REQ
CBUS_PCI_GNT_L C1 GNT
CLK33M_CBUS G1 PCLK
R766 47 5% 1/16W MF 402
MAIN_RESET_L 1
NC M9 SPKROUT
NC M8 RI_OUT/PME
CBUS_SUSPEND_PU N10 SUSPEND
CBUS_INT_L K7 MFUNC0
CBUS_MFUNC1_PD N9 MFUNC1
CBUS_MFUNC2_PD L9 MFUNC2
CBUS_MFUNC3_PD K10 MFUNC3
CBUS_MFUNC4_PD M10 MFUNC4
CBUS_MFUNC5_PD N12 MFUNC5
CBUS_MFUNC6_PD L10 MFUNC6
L11 GRST
RP39 10K 5% 1/32W 25V
CBUS_MFUNC1_PD
CBUS_MFUNC2_PD
CBUS_MFUNC3_PD
CBUS_MFUNC4_PD
CBUS_MFUNC5_PD
CBUS_MFUNC6_PD
SM
GND
A2 A11 D1 F13 H4 K8 M13 N2
MAIN_RESET_L
THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD
R348 47 5% 1/16W MF 402
+3V_MAIN
+5V_MAIN
NO STUFF
R373 10K 5% 1/16W MF 402
U19
TPS2211
SSOI
V_12 V_5_1 V_5_2 V_3_1 V_3_2
AVPP AVCC0 AVCC1 AVCC2
VCCD0 VCCD1 VPPD0 VPPD1 SHTDWN
GND OC
CRITICAL
TPS2211_SHDN_L_PU
MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!
+VPP_CBUS_SW
+VCC_CBUS_SW
C773 0.1UF 20% 10V CERM 402
C467 0.1UF 20% 10V CERM 402
0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV
VCCCB B11
VCCP L3
VCCD0* N13 CBUS_VCCD0_L
VCCD1* L12 CBUS_VCCD1_L
VPPD0 K9 CBUS_VPPD0
VPPD1 M11 CBUS_VPPD1
CD1*/CCD1* L13 CBUS_DET_1_L
CD2*/CCD2* B5 CBUS_DET_2_L
IORD*/CAD13 F12 CBUS_IORD_L
IOWR*/CAD15 C11 CBUS_IOWR_L
OE*/CAD11 G10 CBUS_OE_L
CE1*/CC/BE0* H13 CBUS_CE1_L
VS1*/CVS1 B2 CBUS_VS1
VS2*/CVS2 A9 CBUS_VS2
WE*/CGNT* D13 CBUS_WE_L
RDY/IREQ*/CINT* A6 CBUS_READY
RESET/CRST* D8 CBUS_RESET_L
REG*/CC/BE3* A8 CBUS_REG_L
BVD1/CSTSCHG/STSCHG*/RI* C6 CBUS_BVD1_L
BVD2/SPKR*/CAUDIO D6 CBUS_BVD2_L
INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN* A5 CBUS_WP_L
CE2/CAD10* G13 CBUS_CE2_L
INPACK/CREQ* B8 CBUS_INPACK_L
WAIT/CSERR* B6 CBUS_WAIT_L
A0/CAD26 C7 CBUS_ADDR<0>
A1/CAD25 D7 CBUS_ADDR<1>
A2/CAD24 B7 CBUS_ADDR<2>
A3/CAD23 D10 CBUS_ADDR<3>
A4/CAD22 B12 CBUS_ADDR<4>
A5/CAD21 C8 CBUS_ADDR<5>
A6/CAD20 C9 CBUS_ADDR<6>
A7/CAD18 A12 CBUS_ADDR<7>
A8/CC/BE1* E11 CBUS_ADDR<8>
A9/CAD14 F11 CBUS_ADDR<9>
A10/CAD9 G11 CBUS_ADDR<10>
A11/CAD12 G12 CBUS_ADDR<11>
A12/CC/BE2* D9 CBUS_ADDR<12>
A13/CPAR E12 CBUS_ADDR<13>
A14/CPERR* D12 CBUS_ADDR<14>
A15/CIRDY* C10 CBUS_ADDR<15>
A16/CCLK B13 CBUS_ADDR_16_UF
A17/CAD16 F10 CBUS_ADDR<17>
A18/RSVD E13 CBUS_ADDR<18>
A19/CBLOCK* A13 CBUS_ADDR<19>
A20/CSTOP* E10 CBUS_ADDR<20>
A21/CDEVSEL* D11 CBUS_ADDR<21>
A22/CTRDY* C12 CBUS_ADDR<22>
A23/CFRAME* A10 CBUS_ADDR<23>
A24/CAD17 B10 CBUS_ADDR<24>
A25/CAD19 B9 CBUS_ADDR<25>
D0/CAD27 A4 CBUS_DATA<0>
D1/CAD29 C4 CBUS_DATA<1>
D2/RSVD A3 CBUS_DATA<2>
D3/CAD0 K11 CBUS_DATA<3>
D4/CAD1 K12 CBUS_DATA<4>
D5/CAD3 J13 CBUS_DATA<5>
D6/CAD5 J10 CBUS_DATA<6>
D7/CAD7 H12 CBUS_DATA<7>
D8/CAD28 C5 CBUS_DATA<8>
D9/CAD30 B4 CBUS_DATA<9>
D10/CAD31 B3 CBUS_DATA<10>
D11/CAD2 M12 CBUS_DATA<11>
D12/CAD4 J11 CBUS_DATA<12>
D13/CAD6 K13 CBUS_DATA<13>
D14/RSVD J12 CBUS_DATA<14>
D15/CAD8 H11 CBUS_DATA<15>
R750 47 5% 1/16W MF 402 CBUS_ADDR<16>
PC CARD/CARDBUS CONNECTOR
CRITICAL
J9
QT500806-L111
M-ST-SM1
CBUS_DATA<3> CBUS_DATA<4> CBUS_DATA<5> CBUS_DATA<6> CBUS_DATA<7>
CBUS_CE1_L CBUS_ADDR<10> CBUS_OE_L CBUS_ADDR<11> CBUS_ADDR<9>
CBUS_ADDR<8> CBUS_ADDR<13> CBUS_WE_L CBUS_READY +VCC_CBUS_SW
+VPP_CBUS_SW CBUS_ADDR<16> CBUS_ADDR<15> CBUS_ADDR<12>
CBUS_ADDR<7> CBUS_ADDR<6> CBUS_ADDR<5> CBUS_ADDR<4>
CBUS_ADDR<3> CBUS_ADDR<2> CBUS_ADDR<1> CBUS_ADDR<0>
CBUS_DATA<0> CBUS_DATA<1> CBUS_DATA<2>
CBUS_WP_L
CBUS_DET_1_L CBUS_DATA<11> CBUS_DATA<12> CBUS_DATA<13>
CBUS_DATA<14> CBUS_DATA<15> CBUS_CE2_L CBUS_VS1
CBUS_IORD_L CBUS_IOWR_L CBUS_ADDR<17> CBUS_ADDR<18>
CBUS_ADDR<19> CBUS_ADDR<20> CBUS_ADDR<21> +VCC_CBUS_SW
+VPP_CBUS_SW CBUS_ADDR<22> CBUS_ADDR<23> CBUS_ADDR<24>
CBUS_ADDR<25> CBUS_VS2 CBUS_RESET_L CBUS_WAIT_L
CBUS_INPACK_L CBUS_REG_L CBUS_BVD2_L CBUS_BVD1_L
CBUS_DATA<8> CBUS_DATA<9> CBUS_DATA<10> CBUS_DET_2_L
TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW
C783 2.2UF 20% 16V CERM 805
C776 2.2UF 20% 16V CERM 805
CARDBUS
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SIZE D
DRAWING NUMBER 051-6694
REV. 02
SCALE NONE
SHT 17 OF 45

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHSCTLR,667BGA	U44	CRITICAL	M11_CSP64

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0182	338S0158	M11_CSP128	U44	ALT FOR A16
338S0183	338S0154	M11_CSP64	U44	ALT FOR A16

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP — L4 FERR-EMI-100-OHM (SM) — +3V ATI OSC SLEEP

C77 0.1uF 20% 10V CERM 402 — C78 4.7uF 20% 6.3V CERM 805

R188 100K 5% 1/16W MF 402 (NO STUFF)

G2 27.0000M OSC SM-1 (CRITICAL): VCC, OE, OUT, GND

ATI OSC OE — OE; OUT — ATI CLK27M OSC

(PLACE R200 CLOSE TO OSC) R200 0 5% 1/16W MF 402 (GPU_SS) — ATI CLK27M OSC SS

R189 287 1% 1/16W MF 402 — ATI CLK27M_IN

R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD

SPREAD SPECTRUM SUPPORT

+3V_SLEEP — L3 FERR-EMI-100-OHM (SM) (GPU_SS) — +3V ATI SS

C70 10uF 20% 6.3V CERM 805 (GPU_SS) — C71 0.1uF 20% 10V CERM 402 (GPU_SS)

R173 0 5% 1/16W MF 402 (NO STUFF)

R181 0 5% 1/16W MF 402 (GPU_SS) — ATI CLK27M OSC SS

U47 CY25811 SOI (CRITICAL, VDD): XIN/CLKIN, XOUT, NC, NC, FRSEL, S1, S0, VSS, SSCLK

CY25811 S1; CY25811 S0

ATI SSCLK UF — R201 33 5% 1/16W MF 402 (GPU_SS) — ATI SSCLK IN

R37 0 5% 1/16W MF 402 (NO STUFF)

R38 0 5% 1/16W MF 402 (NO STUFF)

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (1 OF 6)

AGP AD<31:0> — AD31 … AD0

AGP AD STB0 — AD_STB0 — N29

AGP AD STB1 — AD_STB1 — W29

AGP AD STB0_L — AD_STBB0 — M28

AGP AD STB1_L — AD_STBB1 — Y29

AGP_BUSYB — AG28 — AGP BUSY_L

AGPREF — K30

AGPTEST — K29 — GPU AGP TEST

AGP8X_DETB — U25 — AGP8X DET PU

SUS_STAT — AJ28 — AGP SUS STAT L PU

ST0 — AF30 — AGP ST<0>

ST1 — AF28 — AGP ST<1>

ST2 — AE29 — AGP ST<2>

SBA7 — AC28 — AGP SBA<7>

SBA6 — AB29 — AGP SBA<6>

SBA5 — AC27 — AGP SBA<5>

SBA4 — AC30 — AGP SBA<4>

SBA3 — AD27 — AGP SBA<3>

SBA2 — AD30 — AGP SBA<2>

SBA1 — AE28 — AGP SBA<1>

SBA0 — AD29 — AGP SBA<0>

RBFB — AE30 — AGP RBF_L

STP_AGPB — AG29 — AGP STP_L

SB_STB — AC29 — AGP SB STB

SB_STBS — AD28 — AGP SB STB_L

RSTB_MSK — AD24 — ATI RSTB MSK

DBI_LO — Y25 — ATI DBI LO PU

DBI_HI — Y27 — ATI DBI HI PU

CLK66M_GPU_AGP — AG30 — PCICLK

AGP_FRAME_L — U27 — FRAMEB

AGP_IRDY_L — T30 — IRDYB

AGP_TRDY_L — T28 — TRDYB

AGP_STOP_L — T27 — STOPB

AGP_DEVSEL_L — T29 — DEVSELB

AGP_PAR — R28 — PAR

AGP_REQ_L — AF29 — REQB

AGP_GNT_L — AF27 — GNTB

AGP_INT_L — AH29 — INTAB

AGP_ATI_RESET — AH30 — RSTB

AGP_WBF_L — AE27 — WBF

AGP_ATI_VREFG — AK3 — VREFG

AGP_ATI_VREF — D8 — MVREF

C19, P2, B18, P4, A19, R3, A18, R4, D19, P1, G29, G27, B29, C26, C16, A15, C11 — VSS

OMIT

+3V_GPU — R119 47 5% 1/16W MF 402; R127 10K 5% 1/16W MF 402; R159 20K 5% 1/16W MF 402

+1.5V_AGP

INT_AGP_VREF — C62 0.1uF 20% 10V CERM 402; C63 0.01uF 20% 16V CERM 402 (PLACE C1002 CLOSE TO AGPREF PIN)

+3V_GPU — R172 20K 5% 1/16W MF 402

R158 0 5% 1/16W MF 402

+1.5V_AGP — R126 47K 5% 1/16W MF 402; R138 47K 5% 1/16W MF 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (6 OF 6)

OMIT

M2, P3, A21, B19, M15, N15, P15, R15, T15, T12, T13, T14, W16, V16, U16, T16, R16, R17, R18, R19 — VSS

U6, AE15, F18, P25 — VDDCI

A10, C5, A3, G4, E2, U2, V4, AB2, AC4, B23, K2, A23, K1, B22, L2, A22, L1 — VSS

GPU_VCORE — L2 60-OHM-EMI (SM) — GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402; C67 10uF 20% 6.3V CERM 805

C65 0.01uF 20% 16V CERM 402; C68 0.01uF 20% 16V CERM 402

C66 0.01uF 20% 16V CERM 402; C69 0.01uF 20% 16V CERM 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (2 OF 6)

B26, A26, B25, A25, C22, D21, C21, D20, C20, D22, C23, D23, A27, B27, H2, H1, J2, J1, K4, K3, L4, M3, L3, M4, N2, N1, N4, N3, G30, G28, B30, D26, D16, B15, D11, B10, D5, B3, G3, E1, U1, V3, AB1, AC3, J30, J29, H30, H29, F30, F29, E30, E29, J28, J27, H28, H27, F28, F27, E28, E27, D30, D29, C30, C29, A30, A29, A28, B28, D28, C28, D27, C27, D25, C25, D24, C24, D18, C18, D17, C17, D15, C15, D14, C14, B17 — VSS

OMIT

A17, B16, A16, B14, A14, B13, A13, D13, C13, D12, C12, D10, C10, D9, C9, B12, A12, B11, A11, B9, A9, B8, A8, C7, D7, C6, D6, C4, D4, C3, D3, A5, B5, A4, B4, A2, B2, A1, B1, E4, E3, F3, F4, H3, H4, J3, J4, C1, C2, D1, D2, F1, F2, G1, G2, R1, R2, T1, T2, V1, V2, W1, W2, T3, T4, U3, U4, W3, W4, Y3, Y4, Y1, Y2, AA1, AA2, AC1, AC2, AD1, AD2, AA3, AA4, AB3, AB4, AD3, AD4, AE3, AE4 — VSS

+3V_GPU — R43 1K 1% 1/16W MF 402; R44 1K 1% 1/16W MF 402 (+GPU_MEM); R45 1K 1% 1/16W MF 402; R46 1K 1% 1/16W MF 402

MAIN_RESET_L IS TOGGLED FOR SLEEP

MAIN_RESET_L — R53 47 5% 1/16W MF 402 — R54 10K 5% 1/16W MF 402 (+3V_GPU)

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

C11 0.1uF 20% 10V CERM 402; C37 10uF 20% 6.3V CERM 805

+1.8V_GPU — R104 4.7K 5% 1/16W MF 402 (ATI_MEMIO_HI); R105 4.7K 5% 1/16W MF 402 (ATI_MEMIO_LO); R55 4.7K 5% 1/16W MF 402 (ATI_MEMIO_LO); R70 4.7K 5% 1/16W MF 402 (ATI_MEMIO_HI)

ATI_MEMVMODE0 — B7 — MEMVMODE0

ATI_MEMVMODE1 — B6 — MEMVMODE1

FOR 2.5 VDDR1: MEMVMODE0=1.8V, MEMVMODE1=GND

FOR 1.8 VDDR1: MEMVMODE0=GND, MEMVMODE1=1.8V

GPU_THERM_DP_TP — D+ — AC10

GPU_THERM_DM_TP — D- — AC11

+GPU_MEM — E8 — TEST_YCLK

(PULL-UP to GPU_MEM_IO) — J6 — TEST_MLCK

ATI_MEMTEST — C8 — MEMTEST

AC22 — NC — PLLTEST

R118 45.3 1% 1/16W MF 402

M10 AGP INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE: NONE — SHT 18 OF 45

M10 CORE PWR/LVDS/TMDS

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APPLE COMPUTER INC.

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D	051-6694	02

SCALE: NONE

SHT 19 OF 45

U44 RAGE MOBILITY M11-CSP64 64MB BGA (3 OF 6)

U44 RAGE MOBILITY M11-CSP64 64MB BGA (5 OF 6)

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

M10 Power Shut down Sequencing

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

R210,R99,R110 PLACE NEAR ATI CHIP

OMIT

Page Notes

Power aliases required by this page:
(None)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: TMDS

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils
Secondary Max Sep:	100 mils
Secondary Length:	250 mils

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

INTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

EXTERNAL TMDS TERMINATION

L13,L14,L15 PLACE NEAR DVI CONNECTOR

SILICON IMAGE TMDS

I2C ADDR. MASTER = 0X70

I2C ADDR. SLAVE = 0X72

SIL_178

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D	051-6694	02
SCALE: NONE	SHT 20 OF 45	

GPU PLL - 1.8V

AGP 4X I/O - 1.5V

MEMORY CORE - 2.5V

LVDS PLL - 1.8V

MEMORY PLL - 1.8V

LVDS - 2.5V

LVDS/TMDS - 1.8V

MEMORY I/O

3.3V IO SUPPLY

(Max Current varies, depends on usage)

M10 SHUT DOWN POWER SEQUENCING

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

1.5V

1.8V

1.8V

2.5V

2.5V

3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

M10 POWER

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SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 21 OF 45	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING — PLACE CLOSE TO CONNECTOR

FL2 LCFILTER SM-220MHZ (CRITICAL) — GPU_B → VGA_B
FL1 LCFILTER SM-220MHZ (CRITICAL) — GPU_G → VGA_G
FL3 LCFILTER SM-220MHZ (CRITICAL) — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

+3V_MAIN

VGA VSYNC BUFFERS

U56 74AHC1G32 SM (CRITICAL) — ATI_HSYNC → R718 33 5% 1/10W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
U57 74AHC1G32 SM (CRITICAL) — ATI_VSYNC → R687 33 5% 1/10W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM (CRITICAL) → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 MBR0530 SM — DDC_CLK_ISO
R655 4.7K 5% 1/16W MF 402
R661 4.7K 5% 1/16W MF 402

J14 QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	9	TMDS_CONN_DN<1>
	19	2	TMDS_CONN_DP<2>
TMDS_CONN_DN<5>	20	10	TMDS_CONN_DP<1>
TMDS_CONN_DP<5>	21	3	
	22	11	TMDS_CONN_DN<4>
TMDS_CONN_CLKP	23	4	TMDS_CONN_DN<3>
TMDS_CONN_CLKN	24	12	TMDS_CONN_DP<4>
VGA_B	C3	5	TMDS_CONN_DP<3>
VGA_HSYNC	C5B	13	DVI_DDC_CLK_UF
	C4	6	(+5V_DDC_SLEEP)
	33	14	DVI_DDC_DATA_UF
	34	7	
		15	VGA_VSYNC
		8	DVI_HPD_UF
		16	
		C1	VGA_R
		C5A	VGA_G
		C2	
		32	
		35	

R670 100 5% 1/16W MF 402 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD → GPU_HPD
C706 100PF 5% 50V CERM 402
C669 100PF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C1 100PF 5% 50V CERM 402
R706 0 5% 1/16W MF 402
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
PLACE NEAR 3, 11 & 19
CHGND1

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 (DVI_DDC_CLK)
Q38 2N7002DW SOT-363 (DVI_DDC_DATA)
Q35 2N7002DW SOT-363 (DVI_HPD)
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 TP0610 SM
R690 680 5% 1/16W MF 402 — DVI_TURN_ON → DVI_TRUN_ON_ILIM
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
Q42 2N3904 SM — SOFT_PWR_ON_L
DVI_DDC_CLK_UF, +5V_DDC_SLEEP

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF
U46 LMC7211 SM (CRITICAL)
DVI_HPD_UF1 → R663 10K 1% 1/16W MF 402 → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
HPD_PWR_SW
Q41 2N7002DW SOT-363 — HPD_ON
+PBUS
Q45 TP0610 SM
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_ENABLE
COMP_DISABLE
HPD_ON_RC
R703 330 5% 1/16W MF 402
R700 20K 5% 1/16W MF 402
HPD_BASE
Q44 2N3904 SM
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN
R213 100K 5% 1/16W MF 402
Q41 2N7002DW SOT-363

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6
R317 100K 5% 1/16W MF 402 — FP_PWR_EN
+5V_INV_UF_SW
L32 400-OHM-EMI SM-1
C440 10UF 20% 6.3V CERM 805
+5V_INV_SW
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
J7 SM-2MT (CRITICAL)
Q7 FDG6324L SC70-6 — FP_PWR_EN
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
+3V_PMU
C552 0.1UF 20% 10V CERM 402
INV_ON_PWM
U24 74LVC32 TSSOP — BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
CHGND2

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402 — LVDS_DDC_CLK
R320 100K 5% 1/16W MF 402 — LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402
C416 0.001uF 20% 50V CERM 402
CHGND4

J6 G-501973 F-RT-SM (CRITICAL)
+3V_LCD
(LVDS DDC POWER)
NC
LVDS_L0N, LVDS_L0P
LVDS_L1N, LVDS_L1P
LVDS_L2N, LVDS_L2P
CLKLVDS_LN, CLKLVDS_LP
LVDS_U0N, LVDS_U0P
LVDS_U1N, LVDS_U1P
LVDS_U2N, LVDS_U2P
CLKLVDS_UN, CLKLVDS_UP
C500 0.001uF 20% 50V CERM 402

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_DIGON, LCD_PWREN_L
TSOP SI3443DV Q11
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402
Q8 2N7002 SM — FP_PWR_EN
CHGND4

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01UF 20% 50V CERM 603
CHGND2

TMDS FILTERING

PLACE CLOSE TO CONNECTOR

L72 90-OHM-300MA 2012H (CRITICAL) — TMDS_DN<0> → TMDS_CONN_DN<0>; TMDS_DP<0> → TMDS_CONN_DP<0>
L21 165-OHM SM (CRITICAL) — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
L73 90-OHM-300MA 2012H — TMDS_DN<1> → TMDS_CONN_DN<1>; TMDS_DP<1> → TMDS_CONN_DP<1>
L74 90-OHM-300MA 2012H — TMDS_DN<2> → TMDS_CONN_DN<2>; TMDS_DP<2> → TMDS_CONN_DP<2>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → TV_GND1
L26 FERR-10-OHM-500MA SM
C712 0.01UF 20% 50V CERM 603

L25 3.3UH 0603 — GPU_Y
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
L29 3.3UH 0603 — GPU_C
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
L27 3.3UH 0603 — GPU_COMP
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402

J15 MINIDIN RT-TH MH1177 (CRITICAL) — TV_C, TV_Y, TV_COMP
CHGND1

XW13 SM — GPU_TV_GND2 → TV_GND2
L28 FERR-10-OHM-500MA SM
C717 0.01UF 20% 50V CERM 603

Place GND shorts at graphics controller

TITLE	VIDEO CONNECTORS
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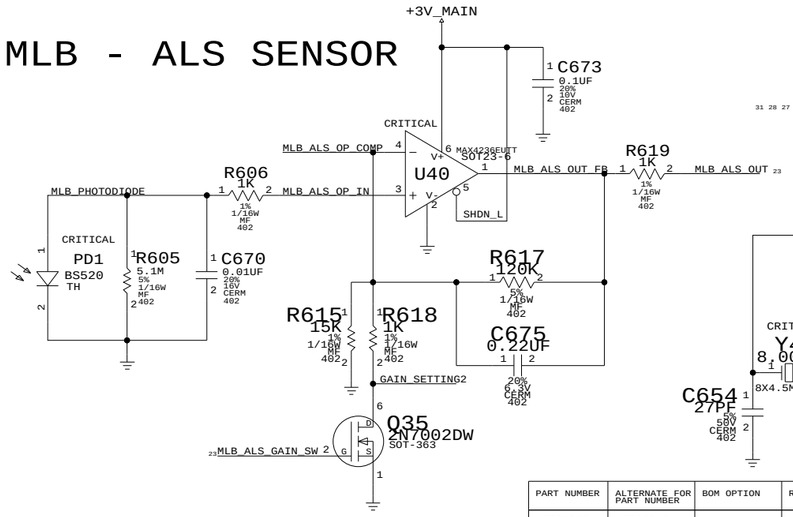
APPLE COMPUTER INC.	
SIZE	D
DRAWING NUMBER	051-6694
REV.	02
SCALE	NONE
SHT	22
OF	45

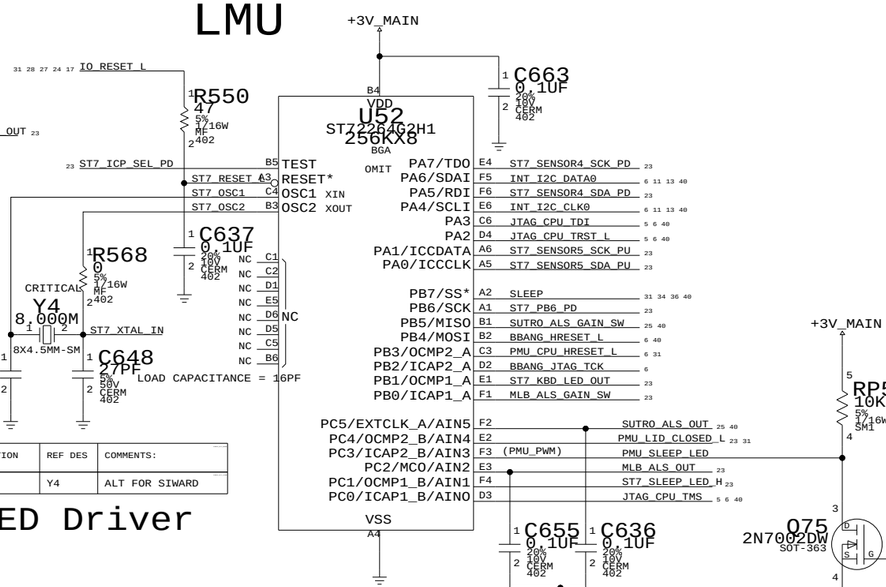
MLB - ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

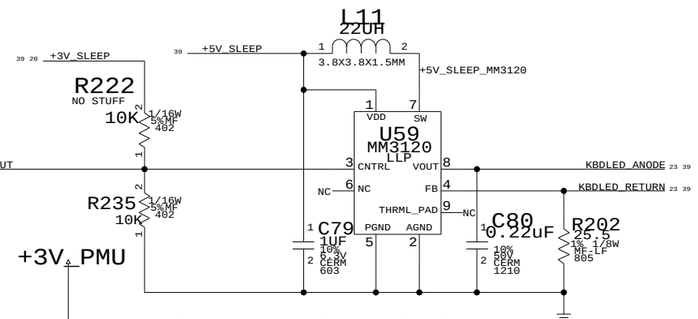
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

LMU

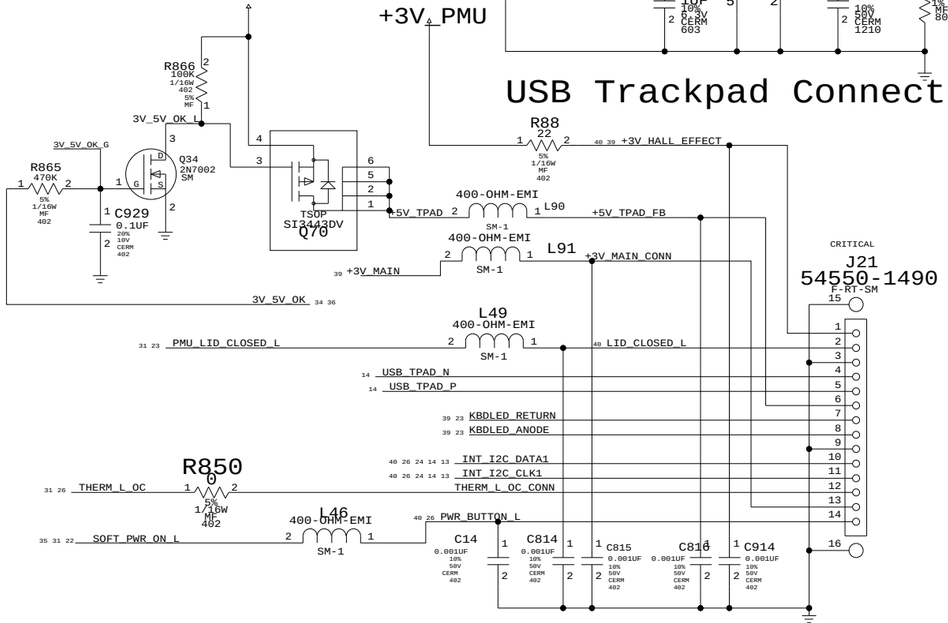


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

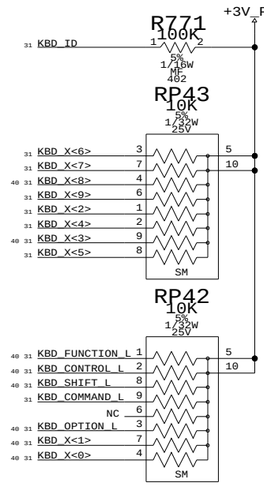
Keyboard LED Driver



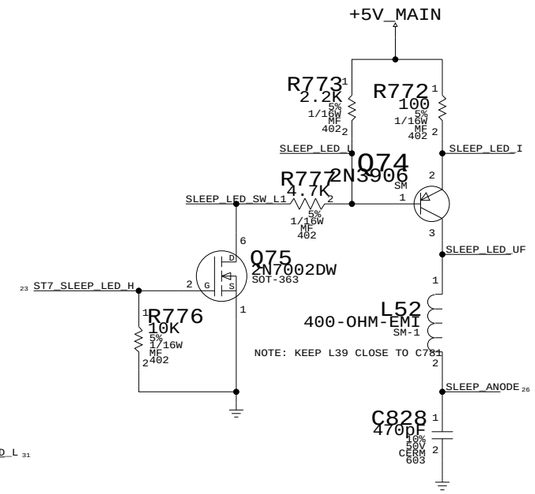
USB Trackpad Connector



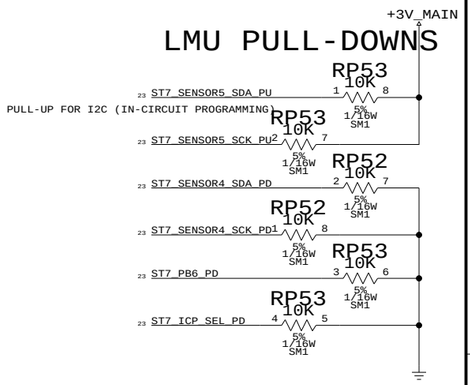
KEYBOARD PULLUPS



SLEEP LED



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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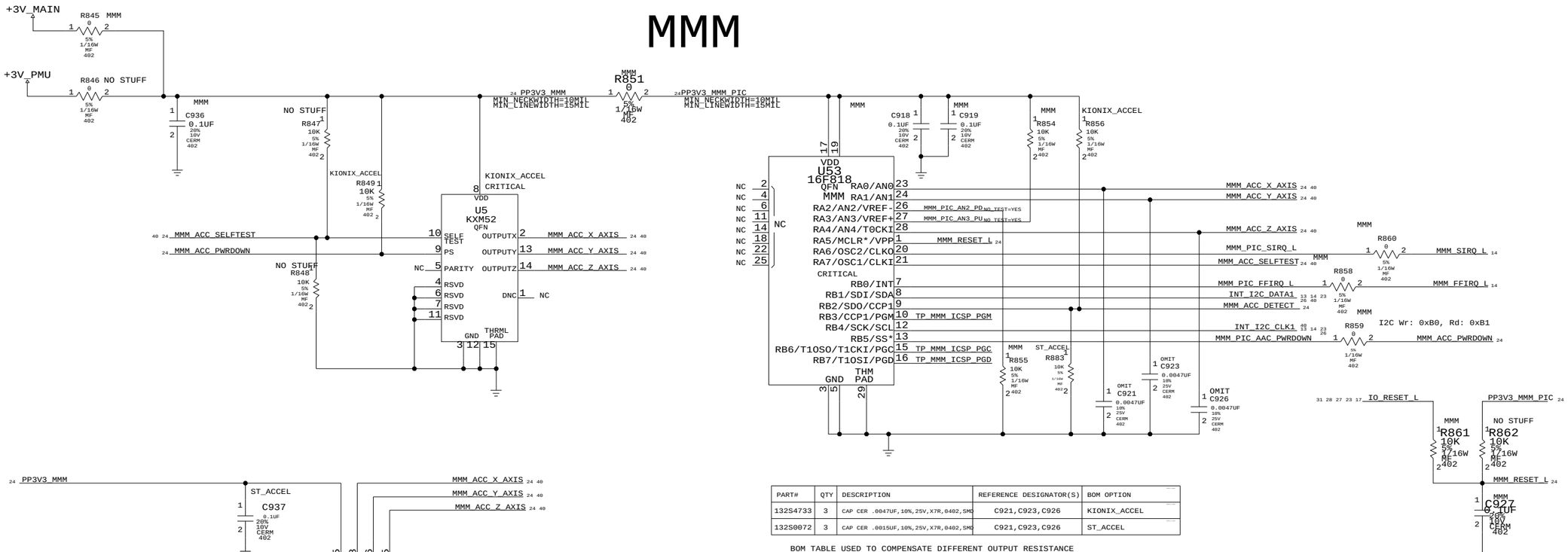
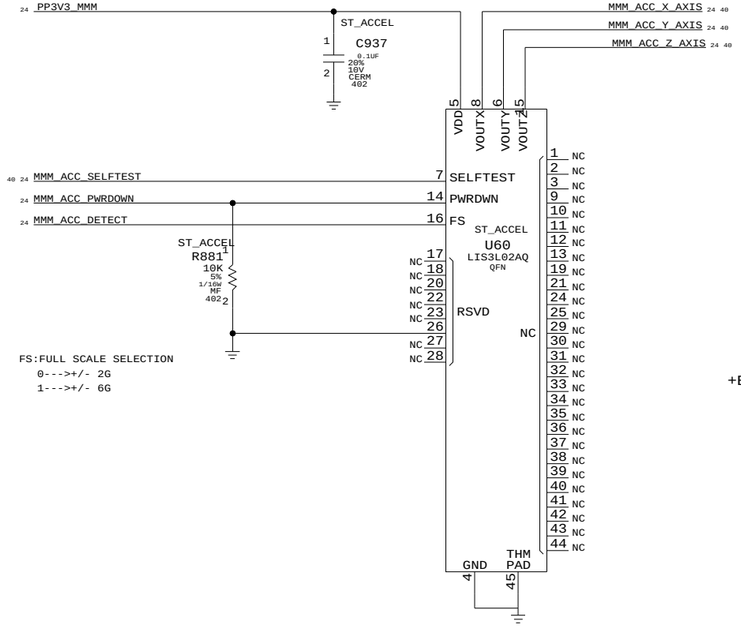
SIZE	DRAWING NUMBER	REV.
D	?	02
SCALE: NONE	SHT 23 OF 45	

MMM

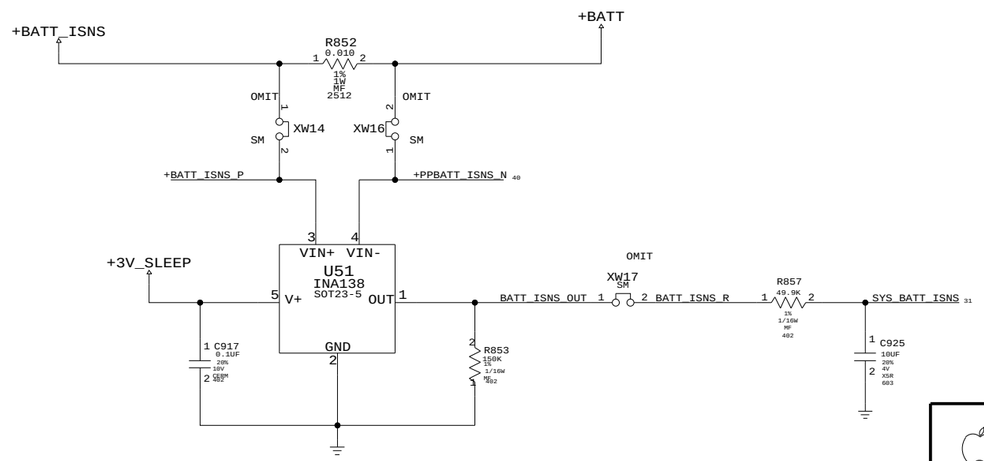




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP CER .0047UF,10%,25V,X7R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



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SIZE	DRAWING NUMBER	REV.
D	?	02
SCALE: NONE	SHT 24 OF 45	

OPTICAL DRIVE INTERFACE (EIDE)

EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

RP50 33 5% 1/16W SM1
- 38 13 EIDE_DATA<8> — 1 — 8 — EIDE_OPTICAL_DATA<8> 25 38 40

RP13 33 5% 1/16W SM1
- 38 13 EIDE_DATA<10> — 1 — 8 — EIDE_OPTICAL_DATA<10> 25 38 40

RP13 33 5% 1/16W SM1
- 38 13 EIDE_DATA<9> — 2 — 7 — EIDE_OPTICAL_DATA<9> 25 38 40

RP49 33 5% 1/16W SM1
- 38 13 EIDE_DATA<11> — 3 — 6 — EIDE_OPTICAL_DATA<11> 25 38 40

RP13 33 5% 1/16W SM1
- 38 13 EIDE_DATA<12> — 4 — 5 — EIDE_OPTICAL_DATA<12> 25 38 40

RP10 33 5% 1/16W SM1
- 38 13 EIDE_DATA<14> — 3 — 6 — EIDE_OPTICAL_DATA<14> 25 38 40

RP50 33 5% 1/16W SM1
- 38 13 EIDE_DATA<13> — 3 — 6 — EIDE_OPTICAL_DATA<13> 25 38 40

RP10 33 5% 1/16W SM1
- 38 13 EIDE_DATA<15> — 1 — 8 — EIDE_OPTICAL_DATA<15> 25 38 40

RP10 33 5% 1/16W SM1
- 38 13 EIDE_DATA<2> — 7 — 2 — EIDE_OPTICAL_DATA<2> 25 38 40

RP50 33 5% 1/16W SM1
- 38 13 EIDE_DATA<1> — 5 — 4 — EIDE_OPTICAL_DATA<1> 25 38 40

RP50 33 5% 1/16W SM1
- 38 13 EIDE_DATA<0> — 7 — 2 — EIDE_OPTICAL_DATA<0> 25 38 40

RP10 33 5% 1/16W SM1
- 38 13 EIDE_DATA<3> — 5 — 4 — EIDE_OPTICAL_DATA<3> 25 38 40

RP13 33 5% 1/16W SM1
- 38 13 EIDE_DATA<6> — 6 — 3 — EIDE_OPTICAL_DATA<6> 25 38 40

RP49 33 5% 1/16W SM1
- 38 13 EIDE_DATA<7> — 8 — 1 — EIDE_OPTICAL_DATA<7> 25 38 40

RP49 33 5% 1/16W SM1
- 38 13 EIDE_DATA<4> — 7 — 2 — EIDE_OPTICAL_DATA<4> 25 38 40

RP49 33 5% 1/16W SM1
- 38 13 EIDE_DATA<5> — 5 — 4 — EIDE_OPTICAL_DATA<5> 25 38 40

RP11 33 5% 1/16W SM1
- 38 13 EIDE_CS0_L — 3 — 6 — EIDE_OPTICAL_CS0_L 25 38 40

RP11 33 5% 1/16W SM1
- 38 13 EIDE_ADDR<1> — 1 — 8 — EIDE_OPTICAL_ADDR<1> 25 38 40

RP11 33 5% 1/16W SM1
- 38 13 EIDE_ADDR<2> — 4 — 5 — EIDE_OPTICAL_ADDR<2> 25 38 40

RP11 33 5% 1/16W SM1
- 38 13 EIDE_ADDR<0> — 2 — 7 — EIDE_OPTICAL_ADDR<0> 25 38 40

R36 10K 5% 1/16W MF 402
- 1 — 2 — 402

R31 33 5% 1/16W MF 402
- 38 13 EIDE_CS1_L — 1 — 2 — EIDE_OPTICAL_CS1_L 25 38 40

R116 82 5% 1/16W MF 402
- 38 13 EIDE_DMARQ — 1 — 2 — EIDE_OPTICAL_DMA_RQ 25 38 40

R95 22 5% 1/16W MF 402
- 38 13 EIDE_DMACK_L — 1 — 2 — EIDE_OPTICAL_DMAACK_L 25 38 40

R30 22 5% 1/16W MF 402
- 38 13 EIDE_RD_L — 1 — 2 — EIDE_OPTICAL_RD_L 25 38 40

R32 22 5% 1/16W MF 402
- 38 13 EIDE_WR_L — 1 — 2 — EIDE_OPTICAL_WR_L 25 38 40

R76 82 5% 1/16W MF 402
- 38 13 EIDE_IOCHRDY — 1 — 2 — EIDE_OPTICAL_IOCHRDY 25 38 40

R81 82 5% 1/16W MF 402
- 38 13 EIDE_INT — 1 — 2 — EIDE_OPTICAL_INT 25 38 40

R69 33 5% 1/16W MF 402
- 38 13 EIDE_RST_L — 1 — 2 — EIDE_OPTICAL_RST_L 25 38 40

WIRELESS INTERFACE

CONNECTOR HAS CHANGED

J20 CPB-7280-1210 M-ST-SM

+3V_SLEEP

	MAIN_RESET_L	1	2	
	RF_DISABLE_L_SPN	3	4	CLK33M_AIRPORT 12 37 40
40 12	AIRPORT_PCI_REQ_L	5	6	
40 38 27 17 12 9	PCI_AD<31>	7	8	AIRPORT_PCI_GNT_L 12 40
		9	10	AIRPORT_PME_L_TP
		11	12	AIRPORT_PCI_INT_L 14 40
40 38 27 17 12 9	PCI_AD<29>	13	14	PCI_AD<30> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<27>	15	16	
40 38 27 17 12 9	PCI_AD<25>	17	18	PCI_AD<28> 9 12 17 27 38 40
		19	20	PCI_AD<26> 9 12 17 27 38 40
40 38 27 17 12	PCI_CBE<3>	21	22	PCI_AD<24> 9 12 17 27 38 40
		23	24	40 AIRPORT_IDSEL
40 38 27 17 12	PCI_AD<23>	25	26	
40 38 27 17 12	PCI_AD<21>	27	28	PCI_AD<22> 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<19>	29	30	PCI_AD<20> 9 12 17 27 38 40
		31	32	PCI_PAR 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<17>	33	34	PCI_AD<18> 9 12 17 25 27 38 40
		35	36	PCI_AD<16> 9 12 17 27 38 40
40 38 27 17 12	PCI_CBE<2>	37	38	
40 38 27 17 12	PCI_IRDY_L	39	40	PCI_FRAME_L 12 17 27 38 40
		41	42	PCI_TRDY_L 12 17 27 38 40
40	AIRPORT_CLKRUN_L	43	44	PCI_STOP_L 12 17 27 38 40
		45	46	PCI_DEVSEL_L 12 17 27 38 40
40 38 27 17 12	PCI_CBE<1>	47	48	PCI_AD<15>
40 38 27 17 12 9	PCI_AD<14>	49	50	9 12 17 27 38 40
		51	52	PCI_AD<13> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<12>	53	54	PCI_AD<11> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<10>	55	56	
40 12 9	ROM_RW_L	57	58	PCI_AD<9> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<8>	59	60	PCI_CBE<0> 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<7>	61	62	ROM_OE_L 9 12 40
		63	64	PCI_AD<6> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<5>	65	66	
40 9	ROM_ONBOARD_CS_L	67	68	PCI_AD<4> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<3>	69	70	PCI_AD<2> 9 12 17 27 38 40
		71	72	PCI_AD<0> 9 12 17 27 38 40
40 38 27 17 12 9	PCI_AD<1>	73	74	
40 12 9	ROM_CS_L	75	76	NC
		77	78	NC
		NC 79	80	NC
		81	82	

R730 10K 5% 1/16W MF 402 — 1 — 2

R745 22 5% 1/16W MF 402 — 2 — 1 — PCI_AD<18> 9 12 17 25 27 38 40

PLACE SERIES R CLOSE TO INTERPID

R8 10K 5% 1/16W MF 402 — 1 — 2

38 13 UIDE_DATA<11>	RP2 33 5% 1/16W SM1	4 — 5	HD_DATA<11> 25 38
38 13 UIDE_DATA<3>	RP9 33 5% 1/16W SM1	2 — 7	HD_DATA<3> 25 38
38 13 UIDE_DATA<1>	RP9 33 5% 1/16W SM1	1 — 8	HD_DATA<1> 25 38
38 13 UIDE_DATA<2>	RP9 33 5% 1/16W SM1	3 — 6	HD_DATA<2> 25 38
38 13 UIDE_DATA<0>	RP2 33 5% 1/16W SM1	1 — 8	HD_DATA<0> 25 38
38 13 UIDE_DATA<7>	RP9 33 5% 1/16W SM1	4 — 5	HD_DATA<7> 25 38
38 13 UIDE_DATA<5>	RP2 33 5% 1/16W SM1	3 — 6	HD_DATA<5> 25 38
38 13 UIDE_DATA<4>	RP2 33 5% 1/16W SM1	2 — 7	HD_DATA<4> 25 38
38 13 UIDE_DATA<6>	RP3 33 5% 1/16W SM1	1 — 8	HD_DATA<6> 25 38
38 13 UIDE_DATA<8>	RP3 33 5% 1/16W SM1	2 — 7	HD_DATA<8> 25 38
38 13 UIDE_DATA<9>	RP4 33 5% 1/16W SM1	4 — 5	HD_DATA<9> 25 38
38 13 UIDE_DATA<10>	RP3 33 5% 1/16W SM1	3 — 6	HD_DATA<10> 25 38
38 13 UIDE_DATA<14>	RP4 33 5% 1/16W SM1	2 — 7	HD_DATA<14> 25 38
38 13 UIDE_ADDR<0>	RP4 33 5% 1/16W SM1	3 — 6	HD_ADDR<0> 25 38
38 13 UIDE_CS0_L	RP5 33 5% 1/16W SM1	2 — 7	HD_CS0_L 25 38
38 13 UIDE_ADDR<1>	RP5 33 5% 1/16W SM1	1 — 8	HD_ADDR<1> 25 38
38 13 UIDE_DATA<15>	RP5 33 5% 1/16W SM1	4 — 5	HD_DATA<15> 25 38
38 13 UIDE_DATA<13>	RP3 33 5% 1/16W SM1	4 — 5	HD_DATA<13> 25 38
38 13 UIDE_DATA<12>	RP4 33 5% 1/16W SM1	1 — 8	HD_DATA<12> 25 38
38 13 UIDE_ADDR<2>	RP5 33 5% 1/16W SM1	3 — 6	HD_ADDR<2> 25 38
UIDE_CS1_L	R75 33 5% 1/16W MF 402	2 — 1	HD_CS1_L 25 38

+5V_SLEEP

NO STUFF

R452 100K 5% 1/16W MF 402 — 1 — 2

R442 10K 5% 1/16W MF 402 — 1 — 2

NO STUFF

R411 10K 5% 1/16W MF 402 — 1 — 2

CRITICAL

J10 M-ST-SM1

	NC	1	50	EIDE_OPTICAL_RST_L 25 38 40
		2	49	
40 38 25	EIDE_OPTICAL_DATA<8>	3	48	EIDE_OPTICAL_DATA<7> 25 38 40
40 38 25	EIDE_OPTICAL_DATA<9>	4	47	EIDE_OPTICAL_DATA<6> 25 38 40
40 38 25	EIDE_OPTICAL_DATA<10>	5	46	EIDE_OPTICAL_DATA<5> 25 38 40
40 38 25	EIDE_OPTICAL_DATA<11>	6	45	EIDE_OPTICAL_DATA<4> 25 38 40
		7	44	
40 38 25	EIDE_OPTICAL_DATA<12>	8	43	EIDE_OPTICAL_DATA<3> 25 38 40
40 38 25	EIDE_OPTICAL_DATA<13>	9	42	EIDE_OPTICAL_DATA<2> 25 38 40
40 38 25	EIDE_OPTICAL_DATA<14>	10	41	EIDE_OPTICAL_DATA<1> 25 38 40
40 38 25	EIDE_OPTICAL_DATA<15>	11	40	EIDE_OPTICAL_DATA<0> 25 38 40
		12	39	
40 38 25	EIDE_OPTICAL_DMA_RQ	13	38	EIDE_OPTICAL_WR_L 25 38 40
40 38 25	EIDE_OPTICAL_RD_L	14	37	EIDE_OPTICAL_IOCHRDY 25 38 40
40 38 25	EIDE_OPTICAL_DMAACK_L	15	36	EIDE_OPTICAL_INT 25 38 40
		16	35	EIDE_OPTICAL_ADDR<1> 25 38 40
40 38 25	EIDE_OPTICAL_ADDR<2>	17	34	EIDE_OPTICAL_ADDR<0> 25 38 40
40 38 25	EIDE_OPTICAL_CS1_L	18	33	EIDE_OPTICAL_CS0_L 25 38 40
		19	32	
		20	31	
		21	30	
	NC	22	29	NC
		23	28	
		24	27	
		25	26	

R441 20K 5% 1/16W MF 402 — 1 — 2

R458 10K 5% 1/16W MF 402 — 1 — 2

PLACE PULLUP RESISTORS CLOSE TO INTREPID

+3V_SLEEP

R63 10K 5% 1/16W MF 402 — 1 — 2

R612 10K 5% 1/16W MF 402 — 1 — 2

R94 10K 5% 1/16W MF 402 — 1 — 2

38 13 UIDE_RST_L	R74 33 5% 1/16W MF 402	1 — 2	HD_RESET_L 25 38
38 13 UIDE_DMACK_L	R613 22 5% 1/16W MF 402	1 — 2	HD_DMACK_L 25 38
38 13 UIDE_DIOR_L	R35 22 5% 1/16W MF 402	1 — 2	HD_DIOR_L 25 38
38 13 UIDE_DIOW_L	R68 22 5% 1/16W MF 402	1 — 2	HD_DIOW_L 25 38
38 13 UIDE_IOCHRDY	R93 82 5% 1/16W MF 402	1 — 2	HD_IOCHRDY 25 38

C86 10PF 5% 50V CERM 402 — 1 — 2

IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)

+3V_SLEEP

+5V_HD_SLEEP 34 39

3V_HD_LOGIC

R602 0 5% 1/16W MF 402 — 1 — 2

5V_HD_LOGIC

R601 0 5% 1/16W MF 402 — 1 — 2

CRITICAL

J13 M-ST-SM1

38 25	HD_RESET_L	1	50	
		2	49	
38 25	HD_DATA<7>	3	48	HD_DATA<8> 25 38
38 25	HD_DATA<6>	4	47	HD_DATA<9> 25 38
		5	46	
38 25	HD_DATA<5>	6	45	HD_DATA<10> 25 38
38 25	HD_DATA<4>	7	44	HD_DATA<11> 25 38
		8	43	
38 25	HD_DATA<3>	9	42	HD_DATA<12> 25 38
38 25	HD_DATA<2>	10	41	HD_DATA<13> 25 38
		11	40	
38 25	HD_DATA<1>	12	39	HD_DATA<14> 25 38
38 25	HD_DATA<0>	13	38	HD_DATA<15> 25 38
		14	37	
38 13	HD_DMARQ	15	36	HD_DIOW_L 25 38
38 25	HD_DIOR_L	16	35	HD_IOCHRDY 25 38
		17	34	
38 25	HD_DMACK_L	18	33	HD_INTRQ 13 38
38 25	HD_ADDR<1>	19	32	HD_ADDR<2> 25 38
		20	31	
38 25	HD_ADDR<0>	21	30	HD_CS1_L 25 38
38 25	HD_CS0_L	22	29	
		23	28	
		24	27	
39	+HD_LOGIC_SLEEP	25	26	

R603 20K 5% 1/16W MF 402 — 1 — 2

R101 10K 5% 1/16W MF 402 — 1 — 2

ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB

CRITICAL

+5V_MAIN +3V_MAIN J3 54550-1490 F-RT-SM

40 38 14	BT_USB_DP	15	1
40 38 14	BT_USB_DM		2
			3
			4
40 38 27	LEFT_USB_DP		5
40 38 27	LEFT_USB_DM		6
			7
40 27	NEC_LEFT_USB_PWREN		8
40 25	SUTRO_ALS_OUT		9
40 27	NEC_LEFT_USB_OVERCURRENT		10
40 25	SUTRO_ALS_GAIN_SW		11
			12
			13
			14
		16	

R71 15K 5% 1/16W MF 402 — 1 — 2

R64 15K 5% 1/16W MF 402 — 1 — 2

INTERNAL I/O CONNECTORS

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D	051-6694	02
SCALE: NONE	SHT 25 OF 45	

SOUND BOARD (SOUSAPHONE)

AUDIO - KAZOO SND - INTREPID

Sound Board Connector

Place shorts at 3.3V and 5V regulators

This is an internal board short

This is an internal board short

This is an internal board short

CRITICAL

J12 QT500406-L111 M-ST-SM1

516S0154

VER 1

CAPS FOR EMI EXPERIMENTATION ONLY

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

PLACE XW9 CLOSE TO 5V SWITCHER (U27)

PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

PLACE UNDERNEATH UPPER RAM

ALTERNATE1

PLACE CLOSE TO CPU

MAIN2

PLACE CLOSE TO BATTERY CHARGER/VCORE

ALTERNATE2

FAN INTERFACE

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

CRITICAL

J8 QT510166-L010 P-ST-SM1

SERIAL DEBUG INTERFACE

SERIAL_DEBUG

CRITICAL

J16 M-ST-5087 SM

DEBUG POWER BUTTON

NO STUFF

DEBUG JUMPERS

FAN CONTROLLER

CRITICAL

U3 ADT7460 QSOP

CRITICAL

J4 SM-2MT

PLACE CLOSE TO CONNECTOR

RIGHT FAN (GPU)

CRITICAL

J2 SM-2MT

PLACE CLOSE TO CONNECTOR

LEFT FAN (CPU)

THERM ISOLATION

FAN/MODEM/SOUND/SLEEP LED/DEBUG

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D	051-6694	02
SCALE: NONE	SHT 26 OF 45	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

Low/Full/High Speed (External)

Low/Full/High Speed (External)

Tie to GND at ball N11

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 27
USB_D1P	USB_D1	5 MIL SPACING	14 27
USB_D2M	USB_D2	5 MIL SPACING	
USB_D2P	USB_D2	5 MIL SPACING	

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 27 OF 45	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

R633 10K 5% 1/16W MF 402

JTAG_ASIC_TDI 28 40

+3V_MAIN

C442 10uF 20% 6.3V CERM 805

NO STUFF R333 0 5% 1/16W MF 402

3405_MODE

R319 0 5% 1/16W MF 402

U14 LTC3405 SOT23-6

VIN RUN MODE GND SW VFB

CRITICAL

LTC3405_SW 39

CRITICAL L5 3.3uH SM1

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

3405_VFB

R362 182K 1% 1/16W MF 402 R1

C486 10uF 20% 6.3V CERM 805

+1_0V_MARVELL 39

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402

R353 0 5% 1/16W MF 402

R344 0 5% 1/16W MF 402

37 13 CLKENET_LINK_TX — 37 CLKENET_PHY_TX

37 13 CLKENET_LINK_RX — 37 CLKENET_PHY_RX

37 13 CLKENET_LINK_GBE_REF — 37 CLKENET_PHY_GBE_REF

TX_CLK, RX_CLK, 125CLK

CRITICAL U49 88E1111 BCC

CTRL10 51 NC

DVDD: 1, 6, 10, 15, 57, 62, 67, 71, 85

C492 0.1UF 20% 10V CERM 402

C511 0.01UF 20% 10V CERM 402

C517 0.1UF 20% 10V CERM 402

C502 0.01UF 20% 10V CERM 402

C465 0.1UF 20% 10V CERM 402

C475 0.01UF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

VDDO: 5, 21, 88, 96

39 28 +2_5V_MARVELL

C464 0.1UF 20% 10V CERM 402

C472 0.01UF 20% 10V CERM 402

C453 0.1UF 20% 10V CERM 402

C503 0.01UF 20% 10V CERM 402

C501 0.1UF 20% 10V CERM 402

C496 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

VDDOH: 52, 66, 72

VDDOX: 26, 48

39 +2_5V_MARVELL_AVDD

L34 FERR-EMI-600-OHM SM

AVDD: 32, 35, 36, 40, 45, 78

C497 0.1UF 20% 10V CERM 402

C504 0.01UF 20% 10V CERM 402

C487 0.1UF 20% 10V CERM 402

C476 0.01UF 20% 10V CERM 402

C754 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MARVELL

R465 0 5% 1/16W MF 805

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/16W MF 805

CHGND1

C488 0.1UF 20% 10V CERM 402

C466 0.1UF 20% 10V CERM 402

C506 0.1UF 20% 10V CERM 402

C520 0.1UF 20% 10V CERM 402

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

CRITICAL J17 RJ45 RT-TH

XFR-ENET-1000BT T1 CRITICAL

RJ45_DP<0> RJ45_C0_PD RJ45_DN<0> RJ45_DP<1> RJ45_C1_PD RJ45_DN<1> RJ45_DP<2> RJ45_C2_PD RJ45_DN<2> RJ45_DP<3> RJ45_C3_PD RJ45_DN<3>

Short shielded RJ-45

CHGND1

R735 75 5% 1/16W MF 402

R733 75 5% 1/16W MF 402

R382 75 5% 1/16W MF 402

R347 75 5% 1/16W MF 402

ENET_CTAP_CHGND 39

C457 100pF 10% 3KV CERM 1808

CHGND1

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-

38 MDI_P<0> 38 MDI_M<0> 38 MDI_P<1> 38 MDI_M<1> 38 MDI_P<2> 38 MDI_M<2> 38 MDI_P<3> 38 MDI_M<3>

R346 49.9 1% 1/16W MF 402

R372 49.9 1% 1/16W MF 402

R404 49.9 1% 1/16W MF 402

R413 49.9 1% 1/16W MF 402

R355 49.9 1% 1/16W MF 402 MDI0_PD

R381 49.9 1% 1/16W MF 402 MDI1_PD

R406 49.9 1% 1/16W MF 402 MDI2_PD

R428 49.9 1% 1/16W MF 402 MDI3_PD

C454 0.01UF 20% 10V CERM 402

C477 0.01UF 20% 10V CERM 402

C493 0.01UF 20% 10V CERM 402

C505 0.01UF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO PHY

LED_LINK10 76 — LED_LINK10

LED_LINK100 74 — LED_LINK100

LED_LINK1000 73 NC

LED_DUPLEX 70 NC

LED_RX 69 — LED_RX_SPN

LED_TX 68 NC

CONFIG0 65 (000)
CONFIG1 64 (000)
CONFIG2 63 (111)
CONFIG3 61 (110)
CONFIG4 60 (111)
CONFIG5 59 (101)
CONFIG6 58 (000)

SEE CONFIG TABLES (BELOW)

TDI 44 — JTAG_ASIC_TDI 28 40
TDO 50 — JTAG_ENET_TDO 13
TCK 49 — JTAG_ASIC_TCK 13 40
TMS 46 — JTAG_ASIC_TMS 13 40
TRST 47 — JTAG_ASIC_TRST_L 13 40

RSET 30 — ENET_RSET

SEL_OSC 56 NC
SEL_2.5V 13

GND 97

RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7

38 13 ENET_LINK_RXD<0> 95
38 13 ENET_LINK_RXD<1> 92
38 13 ENET_LINK_RXD<2> 93
38 13 ENET_LINK_RXD<3> 91
38 13 ENET_LINK_RXD<4> 90
38 13 ENET_LINK_RXD<5> 89
38 13 ENET_LINK_RXD<6> 87
38 13 ENET_LINK_RXD<7> 86

RX_DV RX_ER

38 13 ENET_RX_DV 94
38 13 ENET_RX_ER 3

CRS COL

38 13 ENET_CRS 84
38 13 ENET_COL 83

MDC MDIO

38 13 ENET_MDC 25
38 13 ENET_MDIO 24

INT-/INT+

14 ENET_ENERGY_DET 23

RESET

31 27 24 23 17 IO_RESET_L — ENET_RST_L 28

COMA

ENET_COMA 27

S_IN+ S_IN- S_OUT+ S_OUT- S_CLK+ S_CLK-

NC 82 NC 81 NC 77 NC 75 NC 79 NC 80

HSDAC+ HSDAC-

ENET_HSDACP 37
ENET_HSDACM 38

XTAL1 XTAL2

37 CLK25M_ENET_XIN 55
37 CLK25M_ENET_XOUT 54

VSSC

ENET_VSSC 53

TX_EN TX_ER GTX_CLK

38 13 ENET_PHY_TX_EN 9
38 13 ENET_PHY_TX_ER 7
37 13 CLKENET_PHY_GTX 8

TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7

38 13 ENET_PHY_TXD<0> 11
38 13 ENET_PHY_TXD<1> 12
38 13 ENET_PHY_TXD<2> 14
38 13 ENET_PHY_TXD<3> 16
38 13 ENET_PHY_TXD<4> 17
38 13 ENET_PHY_TXD<5> 18
38 13 ENET_PHY_TXD<6> 19
38 13 ENET_PHY_TXD<7> 20

39 28 +2_5V_MARVELL

R371 10K 5% 1/16W MF 402

R345 10K 5% 1/16W MF 402

R354 1.5K 5% 1/16W MF 402

R343 1K 5% 1/16W MF 402

14 INT_ENET_RST_L1

D1 1N914 SOT23

C755 2.2uF 20% 10V CERM 805

Q15 2N7002DW SOT-363

32 31 30 AC_IN

Q15 2N7002DW SOT-363

36 35 34 19 SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R435 20K 5% 1/16W MF 402

R427 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM

CLK25M_XTAL_IN

C555 33pF 5% 50V CERM 402

C491 33pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 49.9 1% 1/16W MF 402

NO STUFF R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

R380 4.99K 1% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037		Y3	
197S0603	197S0037		Y3	ALT FOR SIWARD

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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SIZE	DRAWING NUMBER	REV.
D	051-6694	02
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

FIREWIRE

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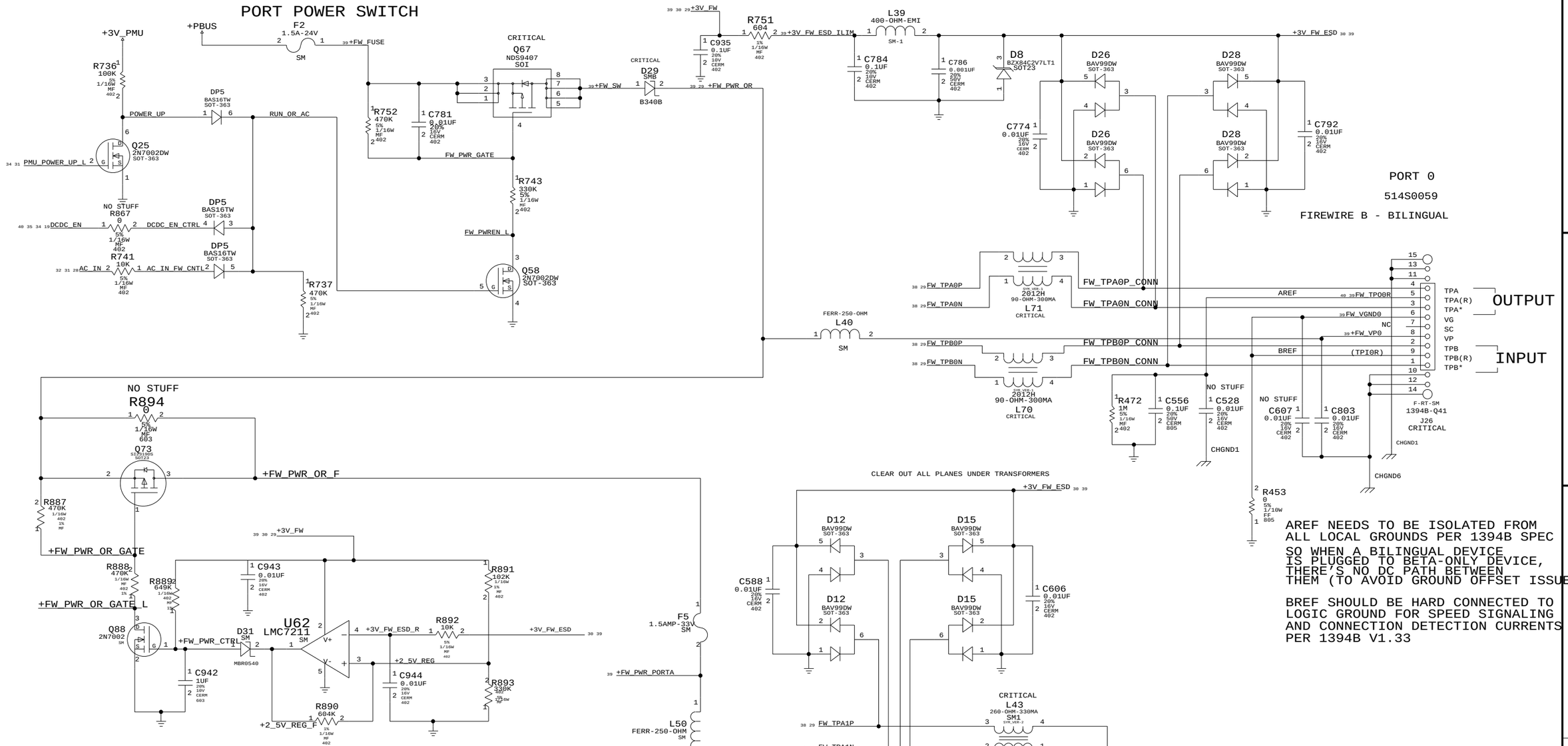
PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS

RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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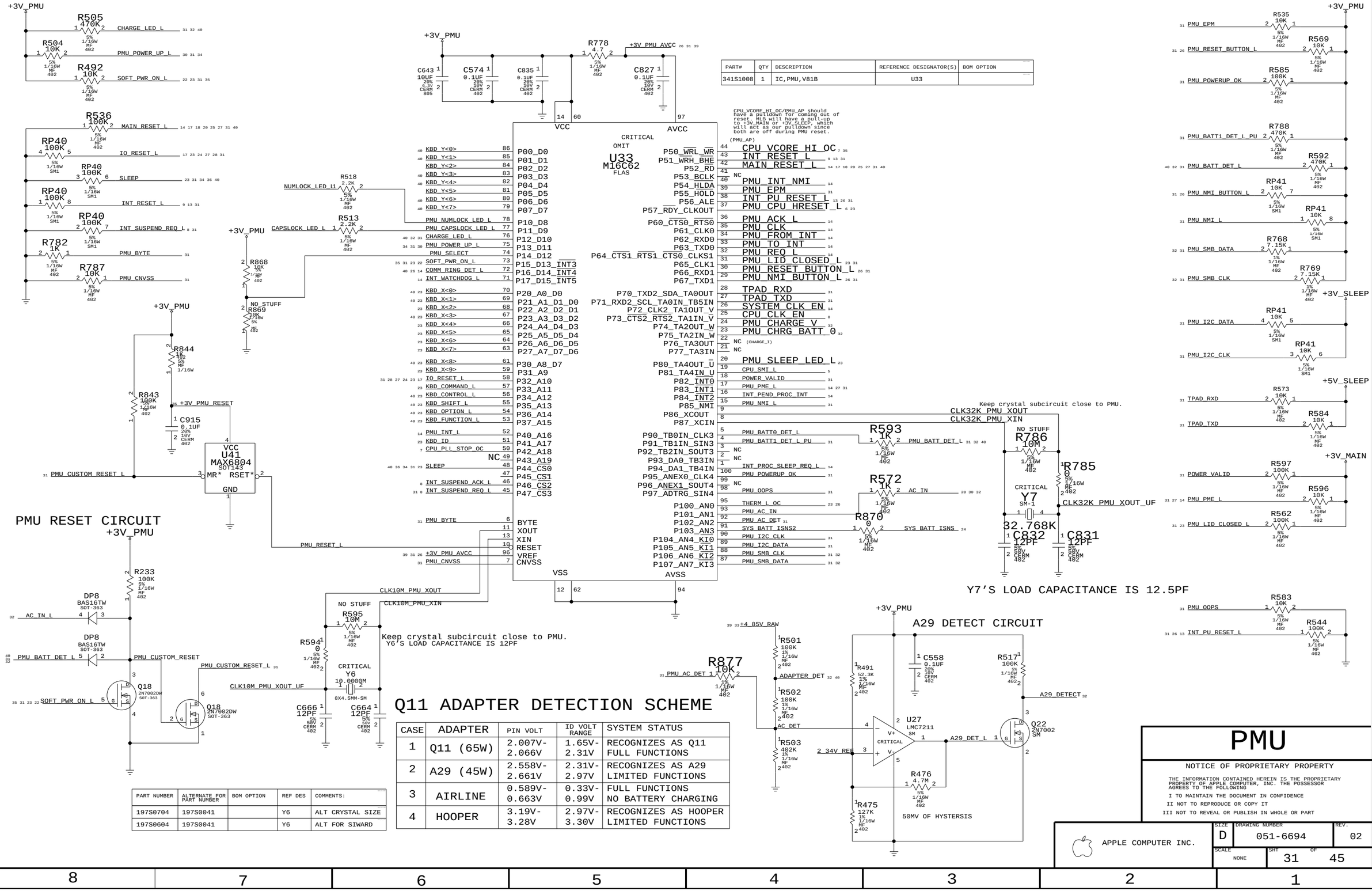

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

PMU

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D	051-6694	02
SCALE: NONE	SHT 31 OF 45	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805
PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

Q13 SI4435DY SOI
Q16 SI4435DY SOI
+ADAPTER SW
+ADAPTER SENSE
GATE
AC_ENABLE_GATE
AC_ENABLE_L

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805
R374 470K 5% 1/16W MF 402
Q10 2N7002DW SOT-363

BCKFD_PROT_GATE
C592 0.01UF 20% 50V CERM 603
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q21 2N7002DW SOT-363
AC_IN

+3V_PMU
R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 603
R363 10K 5% 1/16W MF 402
1V20_REF
U15 LMC7211 SM
CRITICAL
AC_DIV
AC_IN
R394 1M 5% 1/16W MF 402
AC_IN_L
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402
Q10 2N7002DW SOT-363
R383 470K 5% 1/16W MF 402
GREATER THAN 13.5V DETECT

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

U23 MAX4172 TSSOP
RS+ RS-
NC1 PG
NC2 OUT
GND
CRITICAL
NC NC
MAX4172_OUT

+24V_PBUS
R466 10K 1% 1/10W MF 402
R454 2.21K 0.1% 1/10W MF 603
C883 0.1UF 10% 50V X7R 603-1

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
IAC_RC_COMP
C771 0.1UF 20% 10V CERM 402
+3V_PMU
C772 0.1UF 20% 10V CERM 402
R747 42.2K 0.1% 1/16W FF 603
IAC_FB
U50 LMC7111 SOT23-5
CRITICAL
ADAPTER_I_REG
DP4 BAS16TW SOT-363
LTC1625_ITH
R358 150 1% 1/16W MF 402
1625_COMP

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

CURRENT_THRESHOLD
R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603
A29_CURRENT_ADJ
Q20 2N7002DW SOT-363
A29_DETECT
R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
R748 100K 5% 1/16W MF 402
OVER_18V_ADJ
Q20 2N7002DW SOT-363
AC_GTR_18V
C775 1UF 20% 10V CERM 603
1772_ACOK
Q65 2N7002DW SOT-363

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R460 0.025 1% 1W MF 2512
R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
C578 0.47UF 20% 25V CERM 1206
C579 0.47UF 20% 25V CERM 1206

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE
CRITICAL
Q24 SI4435DY SOI
Q76 SUD45P03 TO-252
GATE
R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_24V_GATE
BATT_14V_GATE
R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
Q21 2N7002DW SOT-363
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU
R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
BATTV_HIGH
R561 100K 5% 1/16W MF 402
Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
BATTV_LOW
Q27 2N7002DW SOT-363
PMU_CHARGE_V

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R566 1K 1% 1/16W MF 402
BATT_LOW
Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363
R542 1K 1% 1/16W MF 402

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CCV_RC
1772_REF
1772_GND

U31 MAX1772 QSOP
CRITICAL
CSSP CSSN
DCIN CELLS
ACIN LDO
ACOK DLOV
RFIN BST
VCTL DHI
ICTL LX
ICHG DLO
IINP PGND
CCV CSIP
CCI CSIN
CCS BATT
REF = 4.096V
REF_CLS GND

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS

C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603
R559 100K 5% 1/16W MF 402
XW19
NO STUFF
C906 0.0022UF 10% 50V CERM 402

R571 33 1% 1W 2512
D10 1N914 SOT23
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 25V CERM 805

+24V_PBUS
Q63 IRF7805 SM
Q64 IRF7811W SO-8
CRITICAL
C547 2.2UF 20% 16V CERM 1812
C562 2.2UF 20% 16V CERM 1812
C563 2.2UF 20% 16V CERM 1812
C557 2.2UF 20% 16V CERM 1812
C564 2.2UF 20% 16V CERM 1812
+BATT_RSNS
L42 10UH SM1
R763 0.05 1% 1W MF 2512
D30 SM MBRS140T3
C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603

R754 100K 5% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210
1772_DCIN

+3V_PMU
C615 0.1UF 20% 10V CERM 402
U38 LMC7211 SM
CRITICAL
BATT_LOW
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402

R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q30 2N7002DW SOT-363
Q30 2N7002DW SOT-363
PMU_CHRG_BATT_O

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q65 2N7002DW SOT-363
A29_DETECT

+BATT_VSNS

BATTERY CONNECTOR
CRITICAL
J25
87438-0833
M-RT-SM
+BATT_POS (BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

+BATT_ISNS

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$
For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN
$I_{CHG} = (0.2048 / R_{62}) * (V_{ICTL} / V_{REFIN})$

BATTERY CHARGER

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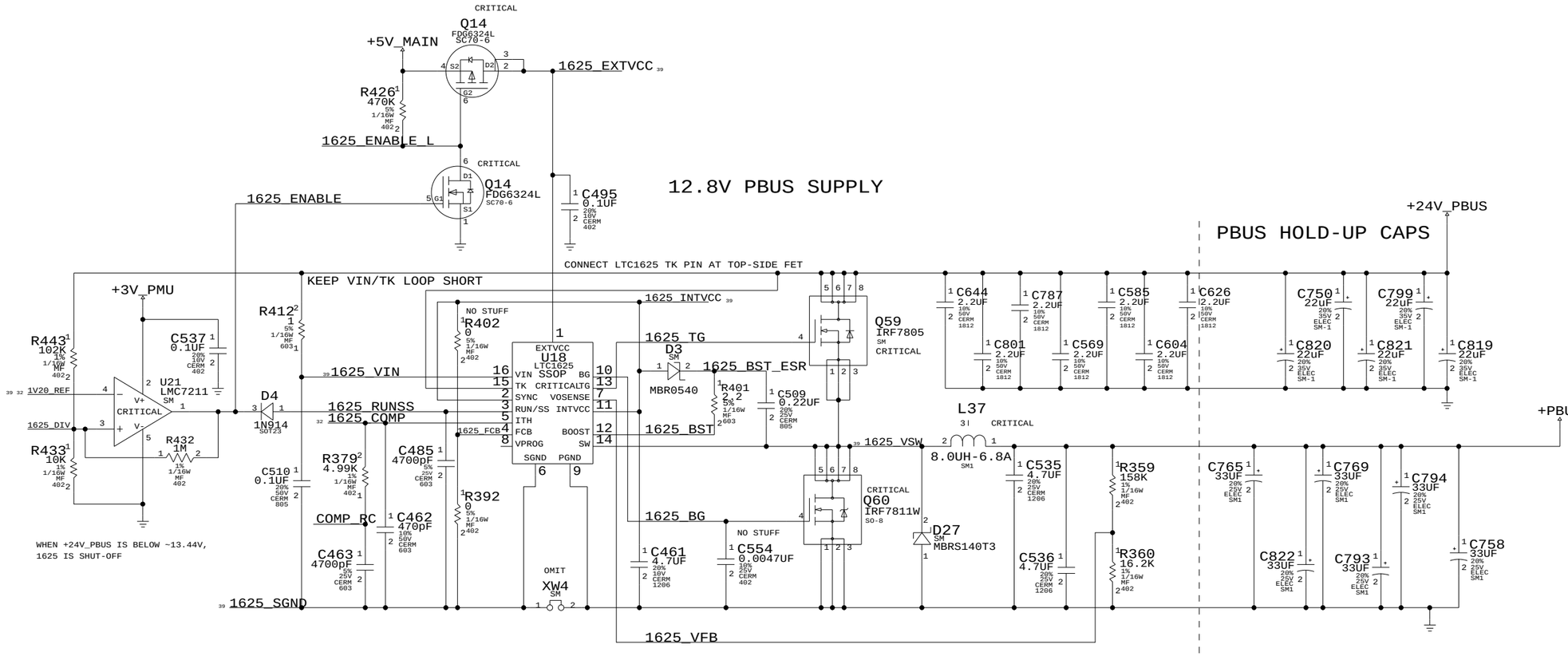
12.8V PBUS SUPPLY
PBUS HOLD-UP CAPS
+5V_MAIN
+24V_PBUS
+PBUS
1625_EXTVCC
1625_ENABLE_L
1625_ENABLE
CRITICAL
Q14
FDG6324L
SC70-6
R426 470K
C495 0.1UF
KEEP VIN/TK LOOP SHORT
CONNECT LTC1625 TK PIN AT TOP-SIDE FET
+3V_PMU
R443 102K
C537 0.1UF
U21 LMC7211
1V20_REF
1625_DIV
R433 10K
R432 1M
R412
R402 0
D4 1N914
1625_VIN
1625_RUNSS
1625_COMP
1625_FCB
C510 0.1UF
R379 4.99K
C485 4700pF
R392 0
COMP_RC
C462 470pF
C463 4700pF
WHEN +24V_PBUS IS BELOW ~13.44V,
1625 IS SHUT-OFF
U18
LTC1625
EXTVCC
VIN SSOP BG
TK CRITICALTG
SYNC VOSENSE
RUN/SS INTVCC
ITH
FCB BOOST
VPROG SW
SGND PGND
OMIT
XW4
1625_SGND
1625_INTVCC
1625_TG
1625_BST_ESR
D3 MBR0540
R401 2.2
C509 0.22UF
1625_BST
1625_VSW
Q59 IRF7805
L37 8.0UH-6.8A
Q60 IRF7811W
D27 MBRS140T3
1625_BG
C461 4.7UF
C554 0.0047UF
1625_VFB
C644 C787 C585 C626 2.2UF
C801 C569 C604 2.2UF
C750 C799 22UF
C820 C821 C819 22UF
C535 4.7UF
C536 4.7UF
R359 158K
R360 16.2K
C765 C769 C794 33UF
C822 C793 C758 33UF
BACKUP BATTERY / USB CONNECTOR
BOOTSTRAP SYSTEM FROM
ADAPTER OR BATTERY
J11
54550-1490
+5V_MAIN
+ADAPTER
+ADAPTER_ILIM
R508 390
D17 MBR0540
+PBUS
+BATT
D18 1N914
D19 MBR0540
+ADAPTER_OR_BATT
NEC_RIGHT_USB_OVERCURRENT
RIGHT_USB_DM
RIGHT_USB_DP
NEC_RIGHT_USB_PWREN
NC
+24V_PBUS_CONN
R880 0
BACKUP_BATT
+PBUS IS BOTH AN INPUT AND OUTPUT TO BUBBA
24V IS AN OUTPUT FROM BUBBA
R871 0
SUPERCAP
PMU SUPPLY
PLUS5VTAP
U30
LP2951
SOI
IN OUT
SENSE ERR
SHUT FDBK
GND
+4_85V_RAW
R521 294K
C613 470PF
R483 1
FB_4_85V_BU
R541 100K
C599 0.1UF
C625 0.1UF
+4_85V_ESR
C568 2.2UF
D7 MBR0520LT
D11 MBR0520LT
(+4_6V_BU)
+4_6V_BU
C553 0.1UF
3V_PMU_VTAP
VTAP
U25
LP2951
SOI-3.3V
3V_PMU_SENSE
R468 1
+3V_PMU_ESR
C584 10UF
12.8V REGULATOR
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REV. 02
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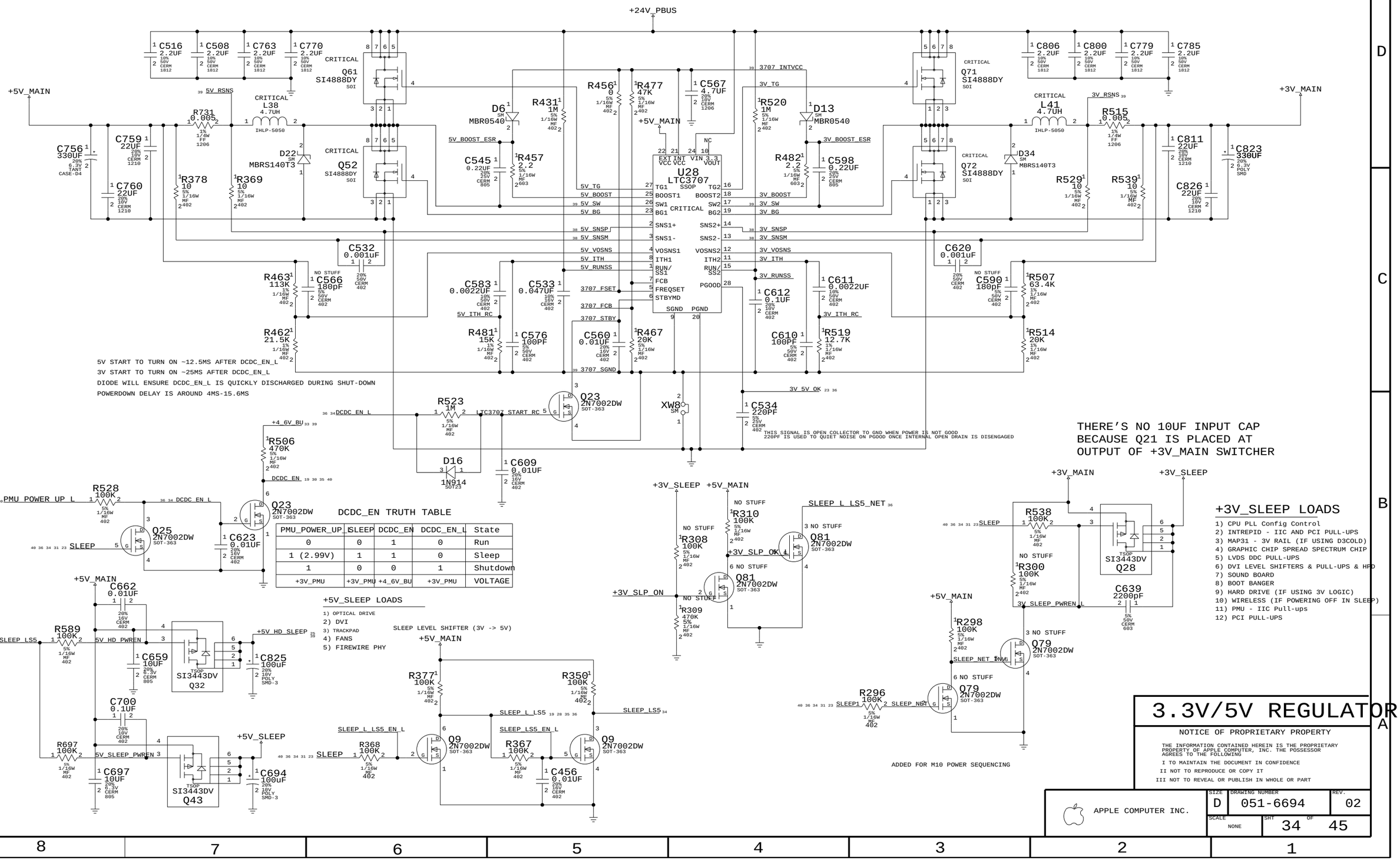
3.3V/5V MAIN SUPPLY



5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

THERE'S NO 10UF INPUT CAP
BECAUSE Q21 IS PLACED AT
OUTPUT OF +3V_MAIN SWITCHER

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

+5V_SLEEP LOADS

1) OPTICAL DRIVE
2) DVI
3) TRACKPAD
4) FANS
5) FIREWIRE PHY

+3V_SLEEP LOADS

1) CPU PLL Config Control
2) INTREPID - IIC AND PCI PULL-UPS
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
7) SOUND BOARD
8) BOOT BANGER
9) HARD DRIVE (IF USING 3V LOGIC)
10) WIRELESS (IF POWERING OFF IN SLEEP)
11) PMU - IIC Pull-ups
12) PCI PULL-UPS

SLEEP LEVEL SHIFTER (3V -> 5V)

ADDED FOR M10 POWER SEQUENCING

3.3V/5V REGULATOR

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SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 34 OF 45	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 0.975V

+5V_MAIN

MAXBUS_SLEEP

CPU_VCORE_PWR_SEQ

CPU_VCORE_SEQ_L

CPU_VCORE_SEQ

R408 100K 5% 1/16W MF 402
R398 100K 5% 1/16W MF 402
R356 100K 1% 1/16W MF 402
R267 10K 5% 1/16W MF 402
DP2 BAS16TW SOT-363
Q12 2N3904 SM
Q17 2N3904 SM

SLEEP_L_LS

DCDC_EN

DP2 BAS16TW SOT-363

NO STUFF R318 0 5% 1/16W MF 402
CPU_VCORE_HI_OC1

R297 R314 R328 R324 R876 R304 R329 R325 470K 5% 1/16W MF 402
R322 10K 5% 1/16W MF 402
R303 R313 R327 R323 R301 R305 R330 R326 470K 5% 1/16W MF 402
R302 1K 5% 1/16W MF 402

<D4> <D3> <D2> <D1> <D4> <D3> <D2> <D1>

VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>

VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>

VCORE_MUX_SEL
VCORE_MUX_EN

U11 PI3B3257 QSOP
VCC GND A1 B1 A2 B2 A3 B3 A4 B4 OE SEL Y1 Y2 Y3 Y4
CRITICAL

SEL = 0; Y1=A1
SEL = 1; Y1=B1

NO STUFF C439 0.1UF 20% 16V CERM 402

VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

NO_4XVCORE
R288 0 5% 1/16W MF 402
R289 0 5% 1/16W MF 402
R290 0 5% 1/16W MF 402
R292 0 5% 1/16W MF 402

VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>

CPU_VCORE_SLEEP

C2 C689 C5 C699 C234 C682 C674 C274 C7 C680 C693 C13 C116 C6 C695 C679 C285 C4 C3 C687
10UF 20% 6.3V CERM 805

Keep trace fat (40-100 mils) and short!!

+PBUS

CRITICAL C427 C431 C443 C430 C432 C441 C444 C445 8.2UF 20% 16V TANT CASE-D

+5V_MAIN

VCORE_VCC

PLACE C423 CLOSE TO PINS 15 & 13!!!
C498 1UF 20% 10V CERM 603
D2 SM MBR0530
VCORE_BOOST

R349 20 5% 1/16W MF 402
R407 0 5% 1/16W MF 402
C507 1UF 20% 10V CERM 603

U20 MAX1717 QSOP

SKP/SDN	2	V+	1
FBS	5	BST	22
ILIM	10	DH	24
GNDS	11	LX	23
A/B	16	DL	14
REF	9	GND	13
TON	8	FB	4
CC	6	TIME	3
D0	21	VGATE	12
D1	20	VCC	7
D2	19	VDD	15
D3	18		
D4	17		

CRITICAL

VCORE_VPLUS
VCORE_BST2
VCORE_DH
VCORE_LX
VCORE_DL
VCORE_GND
VCORE_FB
VCORE_TIME
VCORE_VGATE

NO STUFF C455 0.0047uF 10% 25V CERM 402
R429 2.2 5% 1/16W MF 603
C518 0.1UF 20% 25V CERM 603
C521 0.001UF 20% 50V CERM 402
C768 0.0047uF 10% 25V CERM 402
R434 390K 5% 1/16W MF 402
R415 100 5% 1/16W MF 402
XW5 SM
XW7 SM

CRITICAL Q50 SI7860DP SO-8-PWRPK
CRITICAL Q49 SI7860DP SO-8-PWRPK
CRITICAL Q54 IRF7832 SO-8
CRITICAL Q55 IRF7832 SO-8
CRITICAL Q53 IRF7832 SO-8

Keep trace fat and short!!

CRITICAL L36 1.2UH-18.3A SM1
CRITICAL D25 B540C SM

CPU_VCORE_SLEEP_F
XW15 SM
CPU_VCORE_SLEEP

CRITICAL R331 0.001 1% 1W MF 2512

CRITICAL C728 C734 C733 C732 C885 C731 C730 C729 C884 220UF 20% 2V TANT 7343

NO STUFF R732 2.2 5% 1/4W MF 1210
NO STUFF CPU_VCORE_SNUB
NO STUFF C764 0.0022UF 10% 50V CERM 603

Keep trace fat and short!!

R397 27.4K 1% 1/16W MF 402
C397 1UF 20% 10V CERM 603

NO STUFF R384 0 5% 1/16W MF 402
CPU_VCORE_HI_OC

R366 0 5% 1/16W MF 402
INT_GPIO1_PU

NO STUFF R337 470K 5% 1/16W MF 402
<D0>

VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

R336 0 5% 1/16W MF 402
C529 0.01UF 20% 16V CERM 402
R448 66.5K 1% 1/16W MF 402
R385 12.7K 1% 1/16W MF 402
C459 1UF 20% 10V CERM 603
C512 220PF 5% 25V CERM 402

VCORE_SHDN_L
VCORE_ILIM
MAX1717_AB_SEL
VCORE_REF
VCORE_TON
VCORE_CC
VCORE_GNDA
VCORE_GNDSNS
VCORE_SNS

MIN_LINE_WIDTH=10

+5V_MAIN

VCORE_OFFSET_SW
R805 100K 5% 1/16W MF 402
VCORE_SEL_OFF_PU

R809 1.5K 1% 1/16W MF 402
R376 162K 1% 1/16W MF 603 R2
R321 2K 1% 1/16W MF 402 R1
VCORE_GNDDIV
VCORE_OFFSET

VCORE_SEL_ON

NO STUFF R806 0 5% 1/16W MF 402
R807 0 5% 1/16W MF 402
AB_SEL_LOW
MAX1717_AB_SEL
VCORE_OFFSET_SW

Q86 2N7002DW SOT-363

NO STUFF R808 100K 5% 1/16W MF 402

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU
XW3 SM

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, V B= V .

FMAX CONNECTOR

NO STUFF R315 2.05K 1% 1/16W MF 402
VCORE_GNDDIV

NO STUFF R312 100 1% 1/16W MF 402
VCORE_GNDSNS

VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)

CRITICAL NO STUFF J5 M-ST-SM-52465-1217

VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

VCORE SUPPLY

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02

SCALE NONE | SHT 35 OF 45

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02
SCALE NONE | SHT 36 OF 45

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
CONTROL	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING		12 25 40
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10 MIL SPACING		12 27
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		28
	CLK25M_ENET_XOUT						10 MIL SPACING		28
	NEC_XT1						10 MIL SPACING		27
	NEC_XT2	THERE'S ANOTHER 280MIL LEG					10 MIL SPACING		27
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 26 40
	SND_CLKOUT					200.0000	10 MIL SPACING		14 26 40
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			28
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_GBE_REF					200.0000			28
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_TX					200.0000			28
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 28
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 28
FIREWIRE	CLKFW_PHY_PCLK					200.0000			29
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 29
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 29
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		29
	FW_OSC					200.0000	10 MIL SPACING		29

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE: D | DRAWING NUMBER: 051-6694 | REV.: 02

SCALE: NONE | SHT: 37 OF 45

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHZ	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHZ	12 18
	AGP_AD_STB<0>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHZ	12 18
	AGP_CBE<3..2>		5	100				66 MHZ	12 18
	AGP_AD_STB<1>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHZ	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..23>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHZ	9 12 17 25 27 40
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHZ	12 17 25 27 40
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_PAR					MIN_DAISY_CHAIN			12 17 25 27 40
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 25
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200				13 25
	UIDE_DATA<6..0>				200			100 MHZ	13 25
	UIDE_ADDR<2..0>				200			100 MHZ	13 25
	UIDE_RST_L				200.0000				13 25
	UIDE_DIOW_L				200.0000				13 25
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 25
	UIDE_DMACK_L				200.0000				13 25
	UIDE_CS0_L				200.0000				13 25
	UIDE_CS1_L				200.0000				13 25
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 25
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	25
	HD_ADDR<2..0>		5		200			100 MHZ	25
	HD_RESET_L		5		200.0000				25
	HD_DIOW_L		5		200.0000				25
	HD_DIOR_L		5	10 MIL SPACING	200.0000				25
	HD_DMACK_L		5		200.0000				25
	HD_CS0_L		5		200.0000				25
	HD_CS1_L		5		200.0000				25
	HD_DMARQ				200.0000				13 25
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				25
	HD_INTRQ		5						13 25
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 25
	EIDE_ADDR<2..0>							33 MHZ	13 25
	EIDE_CS0_L								13 25
	EIDE_CS1_L								13 25
	EIDE_RD_L								13 25
	EIDE_WR_L								13 25
	EIDE_IOCHRDY								13 25
	EIDE_INT								13 25
	EIDE_RST_L								13 25
	EIDE_DMACK_L								13 25
	EIDE_DMARQ								13 25
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	25 40
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	25 40
	EIDE_OPTICAL_CS0_L								25 40
	EIDE_OPTICAL_CS1_L								25 40
	EIDE_OPTICAL_RD_L								25 40
	EIDE_OPTICAL_WR_L								25 40
	EIDE_OPTICAL_IOCHRDY								25 40
	EIDE_OPTICAL_INT								25 40
	EIDE_OPTICAL_RST_L								25 40
	EIDE_OPTICAL_DMAACK_L								25 40
	EIDE_OPTICAL_DMA_RQ								25 40
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 28
	ENET_RX_DV								13 28
	ENET_RX_ER								13 28
	ENET_PHY_TXD<7..0>		5						13 28
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 28
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 28
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 28
	ENET_MDC								13 28
	ENET_COL								13 28
	ENET_CRS								13 28
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 29
	FW_PHY_DATA<7..0>		5						29
	FW_LINK_CNTL<1..0>								13 29
	FW_PHY_CNTL<1..0>								29
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 29
	FW_PINT								13 29

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				28
	MDI_P<0>	ENET_MDI0				28
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			28
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			28
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			28
	MDI_P<2>	ENET_MDI2				28
	MDI_M<3>	ENET_MDI3				28
	MDI_P<3>	ENET_MDI3				28
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		28 40
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		28 40
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPA0P	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB0P	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPA1P	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB1P	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
	FW_TPI1P	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
	FW_TPO1P	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	19 22 40
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 40
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 40
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 40
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 40
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 40
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 40
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 40
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 25 40
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 25 40
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 26 40
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 26 40
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
POWER SUPPLIES	1772_CSSN	1772_CSS		DIFF		32
	1772_CSSP	1772_CSS		DIFF		32
	1772_CSIN	1772_CSI		DIFF		32
	1772_CSIP	1772_CSI		DIFF		32
	3V_SNSM	3V_SNS		DIFF		34
	3V_SNSP	3V_SNS		DIFF		34
	5V_SNSM	5V_SNS		DIFF		34
	5V_SNSP	5V_SNS		DIFF		34
THERMOSTAT	THERM1_DM	THERM1		DIFF		26
	THERM1_DP	THERM1		DIFF		26
	THERM2_DM	THERM2		DIFF		26
	THERM2_DP	THERM2		DIFF		26
	THERM1_M_DM	THERM1_MAIN		DIFF		
	THERM1_M_DP	THERM1_MAIN		DIFF		
	THERM2_M_DM	THERM2_MAIN		DIFF		
	THERM2_M_DP	THERM2_MAIN		DIFF		
	THERM1_A_DM	THERM1_ALT		DIFF		26
	THERM1_A_DP	THERM1_ALT		DIFF		26
	THERM2_A_DM	THERM2_ALT		DIFF		26
	THERM2_A_DP	THERM2_ALT		DIFF		26

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE: NONE | SHT 38 OF 45

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	20 23
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	40
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 33
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 40
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 40
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	26 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 40
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 40
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
KB LED	KBDLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23
	KBDLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 40
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 40
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	26

I/O AREA	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 40
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	28

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 35 40
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 35
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	11
INTREPID PLLS	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 40
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDCI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_VCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_VCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
FW	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
USB 2.0 INTREPID SSCG	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 40
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

MIN_NECK_WIDTH REDUCED FOR TESTPOINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	32 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	34
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	35
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35 40
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15	35
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19 40
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 39 OF 45	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 28

FUNC_TEST=YES JTAG_ASIC_TDI 28

FUNC_TEST=YES JTAG_ASIC_TDO 13 14

FUNC_TEST=YES JTAG_ASIC_TCK 13 28

FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28

FUNC_TEST=YES CPU_CHKSTP_OUT_L 5

FUNC_TEST=YES CPU_SRESET_L 5

FUNC_TEST=YES CPU_HRESET_L 5 6 7

FUNC_TEST=YES JTAG_CPU_TMS 5 6 23

FUNC_TEST=YES JTAG_CPU_TDI 5 6 23

FUNC_TEST=YES JTAG_CPU_TDO_TP 5

FUNC_TEST=YES JTAG_CPU_TCK 5 6

FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 23 40

FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23

FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23

FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26

FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26

FUNC_TEST=YES CBUS_DET_1_L 17

FUNC_TEST=YES CBUS_DET_2_L 17

FUNC_TEST=YES TMDS_DN<0> 20 22 38

FUNC_TEST=YES TMDS_DP<0> 20 22 38

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FUNC_TEST=YES TMDS_DN<2> 20 22 38

FUNC_TEST=YES TMDS_DP<2> 20 22 38

FUNC_TEST=YES TMDS_CONN_CLKN 22 38

FUNC_TEST=YES TMDS_CONN_CLKP 22 38

FUNC_TEST=YES VGA_R 22

FUNC_TEST=YES VGA_G 22

FUNC_TEST=YES VGA_B 22

FUNC_TEST=YES VGA_VSYNC 22

FUNC_TEST=YES VGA_HSYNC 22

FUNC_TEST=YES DVI_DDC_CLK_UF 22

FUNC_TEST=YES DVI_DDC_DATA_UF 22

FUNC_TEST=YES DVI_HPD_UF 22

FUNC_TEST=YES LVDS_L0N 19 22 38

FUNC_TEST=YES LVDS_L0P 19 22 38

FUNC_TEST=YES LVDS_L1N 19 22 38

FUNC_TEST=YES LVDS_L1P 19 22 38

FUNC_TEST=YES LVDS_L2N 19 22 38

FUNC_TEST=YES LVDS_L2P 19 22 38

FUNC_TEST=YES CLKLVDS_LN 19 22 38

FUNC_TEST=YES CLKLVDS_LP 19 22 38

FUNC_TEST=YES LVDS_U0N 19 22 38

FUNC_TEST=YES LVDS_U0P 19 22 38

FUNC_TEST=YES LVDS_U1N 19 22 38

FUNC_TEST=YES LVDS_U1P 19 22 38

FUNC_TEST=YES LVDS_U2N 19 22 38

FUNC_TEST=YES LVDS_U2P 19 22 38

FUNC_TEST=YES CLKLVDS_UN 19 22 38

FUNC_TEST=YES CLKLVDS_UP 19 22 38

FUNC_TEST=YES LVDS_DDC_CLK 19 22

FUNC_TEST=YES LVDS_DDC_DATA 19 22

FUNC_TEST=YES BRIGHT_PWM 22

FUNC_TEST=YES TV_GND1 22 39

FUNC_TEST=YES TV_GND2 22 39

FUNC_TEST=YES TV_C 22

FUNC_TEST=YES TV_Y 22

FUNC_TEST=YES TV_COMP 22

FUNC_TEST=YES SND_TO_AUDIO 14 26

FUNC_TEST=YES SND_SYNC 14 26

FUNC_TEST=YES SND_CLKOUT 14 26 37

FUNC_TEST=YES INT_AUDIO_TO_SND 14 26

FUNC_TEST=YES SND_SCLK 14 26 37

FUNC_TEST=YES SND_HW_RESET_L 14 26

FUNC_TEST=YES SND_HP_SENSE_L

FUNC_TEST=YES SND_LIN_SENSE_L

FUNC_TEST=YES INT_I2C_DATA2 14 26

FUNC_TEST=YES INT_I2C_CLK2 14 26

I203 CHGND4 39

I204 SLEEP_LED

FUNC_TEST=YES BT_USB_DM 14 25 38

FUNC_TEST=YES BT_USB_DP 14 25 38

FUNC_TEST=YES MODEM_USB_DM 14 26 38

FUNC_TEST=YES MODEM_USB_DP 14 26 38

FUNC_TEST=YES PCI_AD<0> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<1> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<2> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<3> 9 12 17 25 27 38

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FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38

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FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38

FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38

FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38

FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38

FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38

FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38

FUNC_TEST=YES PCI_PAR 12 17 25 27 38

FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38

FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38

FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38

FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38

FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25

FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25

FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25

FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38

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FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38

FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38

FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38

FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38

FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38

FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38

FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38

FUNC_TEST=YES SND_AMP_MUTE 26

FUNC_TEST=YES SND_HP_MUTE_INV

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38

FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38

FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38

FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38

FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 25 38

FUNC_TEST=YES EIDE_OPTICAL_INT 25 38

FUNC_TEST=YES TPAD_F_TXD

FUNC_TEST=YES TPAD_F_RXD

FUNC_TEST=YES LID_CLOSED_L 23

FUNC_TEST=YES COMM_RESET_L 14 26

FUNC_TEST=YES COMM_SHUTDOWN 14 26

FUNC_TEST=YES COMM_RING_DET_L 14 26 31

FUNC_TEST=YES +5V_TPAD_SLEEP

FUNC_TEST=YES +3V_HALL_EFFECT 23 39

FUNC_TEST=YES KBD_CAPSLOCK_LED

FUNC_TEST=YES KBD_FUNCTION_L 23 31

FUNC_TEST=YES KBD_CONTROL_L 23 31

L295 FUNC_TEST=YES +PPBATT_ISNS_N 24

FUNC_TEST=YES KBD_OPTION_L 23 31

FUNC_TEST=YES KBD_SHIFT_L 23 31

FUNC_TEST=YES KBD_X<0> 23 31

FUNC_TEST=YES KBD_X<1> 23 31

FUNC_TEST=YES KBD_X<3> 23 31

L296 FUNC_TEST=YES MMM_ACC_SELFTEST 24

L297 FUNC_TEST=YES MMM_ACC_X_AXIS 24

L298 FUNC_TEST=YES MMM_ACC_Y_AXIS 24

L299 FUNC_TEST=YES MMM_ACC_Z_AXIS 24

FUNC_TEST=NO KBD_X<8> 23 31

L287 FUNC_TEST=YES SRCLK_TP 27

L288 FUNC_TEST=YES SRMOD_TP 27

L289 FUNC_TEST=YES TEB_TP 27

L290 FUNC_TEST=YES TEST_TP 27

FUNC_TEST=YES KBD_Y<0> 31

FUNC_TEST=YES KBD_Y<1> 31

FUNC_TEST=YES KBD_Y<3> 31

FUNC_TEST=YES KBD_Y<4> 31

FUNC_TEST=YES KBD_Y<6> 31

FUNC_TEST=YES KBD_Y<7> 31

FUNC_TEST=YES KBD_NUMLOCK_LED

FUNC_TEST=YES +BATT_POS 32 39

FUNC_TEST=YES BATT_CLK 32

FUNC_TEST=YES BATT_DATA 32

FUNC_TEST=YES BATT_NEG 32 39

FUNC_TEST=YES PMU_BATT_DET_L 31 32

FUNC_TEST=YES FANR_GND 26 39

FUNC_TEST=YES FANL_GND 26 39

FUNC_TEST=YES FANL_TACH 26

L277 FUNC_TEST=YES FANR_PWM 26

L277 FUNC_TEST=YES FANL_PWM 26

FUNC_TEST=YES RJ45_DP<0> 28 38

FUNC_TEST=YES RJ45_DN<0> 28 38

FUNC_TEST=YES RJ45_DP<1> 28 38

FUNC_TEST=YES RJ45_DN<1> 28 38

FUNC_TEST=YES RJ45_DP<2> 28 38

FUNC_TEST=YES RJ45_DN<2> 28 38

FUNC_TEST=YES RJ45_DP<3> 28 38

FUNC_TEST=YES RJ45_DN<3> 28 38

FUNC_TEST=YES FW_TPO0R 30 39

L281 FUNC_TEST=YES VCORE_VID0

L282 FUNC_TEST=YES VCORE_VID1

L283 FUNC_TEST=YES VCORE_VID2

L285 FUNC_TEST=YES VCORE_VID3

L284 FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 30 38

FUNC_TEST=YES FW_TPO1N 30 38

FUNC_TEST=YES FW_TPI1P 30 38

FUNC_TEST=YES FW_TPI1N 30 38

FUNC_TEST=YES CHARGE_LED_L 31 32

FUNC_TEST=YES ADAPTER_DET 31 32

FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25

FUNC_TEST=YES SUTRO_ALS_OUT 23 25

FUNC_TEST=YES KBD_LED1_OUT

FUNC_TEST=YES KBD_LED2_OUT

FUNC_TEST=YES COMM_TXD_L 14 26

FUNC_TEST=YES COMM_TRXC 14 26

FUNC_TEST=YES COMM_GPIO_L 14 26

FUNC_TEST=YES COMM_DTR_L 14 26

FUNC_TEST=YES COMM_RTS_L 14 26

FUNC_TEST=YES COMM_RXD 14 26

FUNC_TEST=YES PMU_KB_RESET_L

FUNC_TEST=YES PWR_BUTTON_L 23 26

FUNC_TEST=YES +PBUS 39

FUNC_TEST=YES +24V_PBUS 39

FUNC_TEST=YES GPU_VCORE 18 19 39

FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39

FUNC_TEST=YES VCORE_FB 35 39

FUNC_TEST=YES +1_8V_MAIN 39

FUNC_TEST=YES +3V_PMU 39

FUNC_TEST=YES +5V_DDC_SLEEP 22 39

FUNC_TEST=YES +12_8V_INV 22 39

L286 FUNC_TEST=YES VCORE_MUX_EN 35

FUNC_TEST=YES +5V_INV_SW 22 39

FUNC_TEST=YES LEFT_USB_DM 25 27 38

FUNC_TEST=YES LEFT_USB_DP 25 27 38

FUNC_TEST=YES RIGHT_USB_DM 27 33 38

FUNC_TEST=YES RIGHT_USB_DP 27 33 38

FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27

FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27

FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33

FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33

FUNC_TEST=YES DCDC_EN 19 30 34 35

FUNC_TEST=YES BBANG_HRESET_L 6 23

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31

FUNC_TEST=YES RF_DISABLE_L_SPN 25

FUNC_TEST=YES AIRPORT_CLKRUN_L 25

FUNC_TEST=YES ROM_RW_L 9 12 25

FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25

FUNC_TEST=YES ROM_CS_L 9 12 25

FUNC_TEST=YES CLK33M_AIRPORT 12 25 37

FUNC_TEST=YES AIRPORT_IDSEL 25

FUNC_TEST=YES ROM_OE_L 9 12 25

L277 FUNC_TEST=YES INT_MOD_DTI 14 26

L277 FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 23 40

L277 FUNC_TEST=YES MOD_BITCLK 14 26

L276 FUNC_TEST=YES MOD_CLKOUT 14 26

L277 FUNC_TEST=YES MOD_DTO 14 26

L276 FUNC_TEST=YES MOD_SYNC 14 26

L276 FUNC_TEST=YES SLEEP 23 31 34 36

L285 FUNC_TEST=YES 1778_VFB 19 39

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02

SCALE NONE | SHT 40 OF 45

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U41 TO M1T-CSP64 SYMBOL
5) ADDED CPU AVDD LDO (D5)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OE_U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R888 TO DISCONNECT INT_GPIO0 FROM CC FSE
8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DN TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXIPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NET_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R867 TO STUFFED AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16 M1T'S
28) CHANGED TMDS SERIES RPAIRS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) ADD C935 (0.1UF)
5) ADD R867 (0 OHM) FOR IPOD ACTION
6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
8) ADD R869 (10K OHM) PULL DOWN TO GND
9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
10)ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
11)ADD U51 (INA138)
12)ADD R852 (0.010 OHM),R853 (150K OHM) AND R857(49.9 OHM)
13)ADD C917 (0.1UF) AND C925 (10UF)
14)ADD DESCRIPTION FOR MMM I2C BUS
15)MMM I2C BUS LINK TO INTREPID :INT_I2C_CLK1 AND INT_I2C_DATA1
16)CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
17)CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
18)ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L&MMM_SIRQ_L PULL UP TO +3V_MAIN
19)ADD U53 (16F818) AND U5 (KXM52)
20)ADD R845 (0 OHM),R846 (0 OHM;NO_STUFF),R847 (10K OHM;NO_STUFF),R848 (10K OHM;NO_STUFF)
21)ADD R849 (10K OHM),R850 (10K OHM;NO_STUFF),R851(0 OHM),R854 (10K OHM),R856 (10K OHM),
22)ADD R860 (0 OHM),R858 (0 OHM),R859 (0 OHM),R855 (10K OHM),R861 (10K OHM),R862(10K OHM;NO_STUFF)
23)ADD C936(0.1UF),C918(0.1UF),C919(0.1UF),C921(0.0047UF),C923(0.0047UF),C926(0.0047UF),C927(0.1UF)
24)DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
25)ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
26)ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80;5.5V;ELEC;0.33F)
27)J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
28)J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
29)J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
30)C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%,50V,0603)
31)U59 FROM MP1518DJ CHANGE TO MM3120
32)L11 CHANGE TO 152S0235 (22UH;3.8*3.8*1.5MM)
33)DEL D31
34)R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
35)C79 VALUE FROM 2.2UF CHANGE TO 1UF
36)ADD Q70 (SI3443), Q34 (2N7002)
37)ADD R866 (100K OHM),R865 (4.7 OHM),C929 (0.022UF)

09/20/2004

1) ADD R877 (10K OHM)
2) ADD R876 (470K OHM;NO_STUFF)

09/21/2004

1) ADD R878 AND R879 (0 OHM;NO_STUFF)[ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

1) ADD NC NETNAME AT U59 PIN6 AND PIN9
2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
2) ADD R880 AND R871 (0 OHM;BOM_OPTIOM;FOR SUPERCAP AND BACKUP BATTERY SWITCH)
3) ADD U60 (LIS3L02AQ;ST SENSOR)
4) ADD R881 (10K OHM) ,R882 (10K OHM), R883 (10K OHM)
5) ADD C937 (0.1UF,10V,20%,0402)
6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD,MMM_PIC_AN3_PU)

10/05/2004

1) ADD R850 (0 OHM)

QUANTA EE, PLEASE ADD SCHEMATIC UPDATE DETAILS HERE.

10/15/2004

1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02

SCALE NONE | SHT 41 OF 45

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL      28D2< 39B3>
+1_5V_AGP          12C5< 12D1< 12D4< 15D6< 16C8<
                 18C6< 18D6< 19A8< 19B4<> 19D5<>
                 21B8< 21D6< 39C3>
+1_5V_AGP_GPU      21C5< 39C3>
+1_5V_AGP_NECK     19B4<> 39B3>
+1_5V_GPU_VDD15    19D3< 39C3>
+1_5V_INTREPID_PLL   8D6< 12D4< 12D8< 14D6<> 39D3>
+1_5V_INTREPID_PLL1  14C3< 39D3>
+1_5V_INTREPID_PLL2  14D3< 39D3>
+1_5V_INTREPID_PLL3  14D3< 39D3>
+1_5V_INTREPID_PLL4  14D3< 39D3>
+1_5V_INTREPID_PLL5  12D3< 39D3>
+1_5V_INTREPID_PLL6  12D6< 39D3>
+1_5V_INTREPID_PLL7  8D5< 39D3>
+1_5V_INTREPID_PLL8  14D3< 39D3>
+1_5V_LDO          36D8< 39D6>
+1_5V_MAIN         39D6>
+1_5V_SLEEP        39D6>
+1_5V_SLEEP_NECK   21A3<> 39B3>
+1_5V_SLEEP_VIN    36D8<> 39D6>
+1_8V_ATI_PVDD     19C5<> 21B6< 21B6< 21D6<> 39C3>
+1_8V_ATI_TPVDD    21D2<>
+1_8V_DVO_F        21B2<
+1_8V_GPU          18A7< 19C8< 20A8< 21A2< 21A6<
                 21B1< 21B6< 21C8< 21D6< 21D8< 39C3>
+1_8V_GPU_AVDD     21D5< 39C3>
+1_8V_GPU_AVDDQ    21D4< 21D7< 39C3>
+1_8V_GPU_MEMPLL   21B5< 39C3>
+1_8V_GPU_PLL      21D5< 39C3>
+1_8V_GPU_PNLIO    21A5< 39C3>
+1_8V_GPU_PNLPLL   21B5< 39C3>
+1_8V_GPU_TP_PLL   21B4< 21D1<
+1_8V_GPU_VDDDI    21C7< 21D4< 39C3>
+1_8V_MAIN         39D6> 40A2>
+1_8V_PVDD_NECK    19B5<> 39B3>
+1_8V_SLEEP        39D6>
+1_8V_SLEEP_NECK   21A3<> 39B3>
+1_95V_FW_DVDD     29C4< 29C7<> 29D5< 39A3>
+1_95V_FW_DVDD_PORT1  29D6< 39A3>
+1_95V_FW_DVDD_RX0  29C5< 39A3>
+1_95V_FW_DVDD_TX0  29C5< 39A3>
+1_95V_FW_PLL400VDD  29D5< 39A3>
+1_95V_FW_PLL500VDD  29D5< 39A3>
+1_95V_FW_PLLVDD   29D5< 29D7<> 39A3>
+2_5V_CG_MAIN      14C6< 39A3>
+2_5V_GPU          21A8< 21B6< 21D3< 21D7< 21D8<
                 39B3>
+2_5V_GPU_A2VDD    21D4< 21D7< 39C3>
+2_5V_GPU_PNLIO    21A5< 39C3>
+2_5V_INTREPID     9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
                 16B8< 39D3>
+2_5V_MAIN         39D6>
+2_5V_MARVELL      28B8< 28C4<> 39B3>
+2_5V_MARVELL_AVDD  28C4< 39B3>
+2_5V_REG          30B6<
+2_5V_REG_F        30A7<>
+2_5V_SLEEP        39D6>
+2_5V_SLEEP_NECK1  19C4<> 39B3>
+2_5V_SLEEP_NECK2  21A3<> 39B3>
+2_8V_GPU_LVDS_LDO  21A6<>
+3V_ATI_OSC_SLEEP  18D2< 39C3>
+3V_ATI_SS         18B2< 39C3>
+3V_CG_PLL_MAIN    14C6< 39A3>
+3V_FW             29A3< 29D7<> 30B7<> 30D5< 39A3>
+3V_FW_AVDD        29C6< 39A3>
+3V_FW_AVDD_PORT0  29C6< 39A3>
+3V_FW_AVDD_PORT1  29C6< 39A3>
+3V_FW_AVDD_PORT2  29D6< 39A3>
+3V_FW_ESD         30B3<> 30B5< 30D2<> 39B3>
+3V_FW_ESD_ILIM    30D4< 39B3>
+3V_FW_ESD_R       30B6<
+3V_FW_UF          29D7<> 39A3>
+3V_GPU            12D1< 18B8< 18C5< 18C7< 18D6<
                 19C4< 19C5< 19C7< 19D8< 21A7< 21B1<
                 21B8< 39C3>
+3V_GPU_FLT        21B2< 39C3>
+3V_HALL_EFFECT    23B6<> 39B6> 40C4>
+3V_INTREPID_USB   14C3< 39D3>
+3V_LCD            22B4<> 39B6>
+3V_LCD_SW         22A4<> 39B6>
+3V_MAIN           23A7< 39D6>
+3V_MAIN_CONN      23A6<>
+3V_NEC_VDD        27D7< 27D7< 39A3>
+3V_PMU            39D6> 40A2>
+3V_PMU_AVCC       26A4< 31B6< 31D5<> 39C6>
+3V_PMU_ESR        33A2< 39C6>
+3V_PMU_RESET      31C7< 35A3<>
+3V_SLEEP          20C4< 20D5< 23C7< 39D6>
+3V_SLEEP_AUDIO    26D6<> 26D7<>
+3V_SLEEP_NECK     21A3<> 39B3>
+3V_SLP_OK_L       34B4<>
+3V_SLP_ON         34A5<>
+4_6V_BU           33A3<> 34B6< 39C6>
+4_85V_ESR         33A4< 39C6>
+4_85V_RAW         31B4< 33A4<> 39C6>
+5V_DDC_SLEEP      22D3<> 22D5<> 39B6> 40A2>
+5V_DDC_SLEEP_UF   22D6< 39B6>
+5V_HD_SLEEP       25D1<> 34A7<> 39C6>
+5V_INV_SW         22B2<> 39B6> 40D1>
+5V_INV_UF_SW      22B2<> 39B6>
+5V_MAIN           39D6>
+5V_MAIN_AUDIO     26D7<>
+5V_MAIN_CONN      39B6>
+5V_SLEEP          23C7< 39D6>
+5V_SLEEP_MM3120   23C6<>
+5V_SOUND_SLEEP    39B6>
+5V_TPAD           23B7<>
+5V_TPAD_FB        23B6<>
+5V_TPAD_SLEEP     40C4>
+12_8V_INV         22B1<> 39B6> 40A2>
+24V_PBUS          39D6> 40B2>
+24V_PBUS_CONN     33A8<>
+ADAPTER           32D8<> 33B7< 39D6>
+ADAPTER_ILIM      33B6<> 39C6>
+ADAPTER_OR_BATT   33A5<> 39C6>
+ADAPTER_SENSE     32D5<> 39C6>
+ADAPTER_SW        32D6<> 39C6>
+BATT              39D6>
+BATT_14V_FUSE     32D1<> 39C6>
+BATT_24V_FUSE     32B1< 32D2<> 39C6>
+BATT_ISNS_P       24A5<>
+BATT_POS          32A4<> 39C6> 40C3>
+BATT_RSNS         32B2< 39C6>
+BATT_VSNS         32A4< 39C6>
+FW_FUSE           30D7<> 39A3>
+FW_PWR_CTRL       30B7<>
+FW_PWR_OR         29B8< 29D8<> 30D5<> 39A3>
+FW_PWR_OR_F       30B7<>
+FW_PWR_OR_GATE    30B8<>
+FW_PWR_OR_GATE_L  30B8<
+FW_PWR_PORTA      30B5< 39A3>
+FW_SW             30D5<> 39A3>
+FW_VP0            30C2<> 39A3>
+FW_VP1            30A3<> 39A3>
+GPU_MCLK          21C7< 21D4< 39C3>
+GPU_MEM           18A6<> 18B8< 21B4< 21B7< 21C6<
                 21C8< 21D2< 39C3>
+GPU_MEMCORE       21C5< 39C3>
+GPU_VDD15_NECK    19B5<> 39B3>
+GPU_VDD15_UF      19B5<> 19D4<> 39C3>
+HD_LOGIC_SLEEP    25C2<> 39C6>
+PBUS              39D6> 40B2>
+PPBATT_ISNS_N     24A4<> 40B4>
+VCC_CBUS_SW       17B1< 17B2< 17D2<> 39D3>
+VPP_CBUS_SW       17B1< 17B2< 17D2<> 39C3>
1V20_REF           32C7< 33C8< 39D1>
1V65_REF           32A5<
1_5V_2_5V_OK       36C5< 39B1>
1_5V_BOOST         36C6<> 39C1>
1_5V_BST           36C5<> 39C1>
1_5V_DH            36C5<> 39C1>
1_5V_DL            36B5<> 39C1>
1_5V_FB            36B5< 36B7<> 39C1>
1_5V_ILIM          36C5<> 39C1>
1_5V_LX            36B5<> 39C1>
1_5V_SLEEP_EN_L    36C7<> 36D7<>
1_8V_SLEEP_PWREN_L  36A3<>
1_8V_SW            36A5<> 39A1>
1_8V_VFB           39A1>
2_5V_BOOST         36C4<> 39D1>
2_5V_BST           36C4<> 39D1>
2_5V_DH            36C4<> 39D1>
2_5V_DL            36B4<> 39D1>
2_5V_ILIM          36C5<> 39C1>
2_5V_LX            36B4<> 39D1>

2_5V_SLEEP_PWREN_L  36C2<>
2_34V_REF          31A4<
3V_5V_OK           23A7< 34B4<> 36A8<> 36D6<
3V_5V_OK_G         23B8<
3V_5V_OK_INV       36A8<>
3V_5V_OK_L         23B8<>
3V_BG              34C4<>
3V_BOOST           34C4<>
3V_BOOST_ESR       34D3<>
3V_ITH             34C4<>
3V_ITH_RC          34C3<
3V_PMU_VTAP        33B3<
3V_RSNS            34D2< 39D1>
3V_RUNSS           34C4<
3V_SLEEP_PWREN_L   34A3<>
3V_SNSM            34C4< 38A2>
3V_SNSP            34C4< 38A2>
3V_SW              34C4<> 39D1>
3V_TG              34D4<>
3V_VOSNS           34C4<>
5V_BG              34C5<>
5V_BOOST           34C5<>
5V_BOOST_ESR       34D6<>
5V_HD_PWREN        34A8<>
5V_ITH             34C5<>
5V_ITH_RC          34C6<
5V_RSNS            34D7<> 39D1>
5V_RUNSS           34C5<
5V_SLEEP_PWREN     34A8<>
5V_SNSM            34C5< 38A2>
5V_SNSP            34C5< 38A2>
5V_SW              34C5<> 39D1>
5V_TG              34C5<>
5V_VOSNS           34C5<>
1625_BG            33C5<>
1625_BST           33C5<
1625_BST_ESR       33C5<>
1625_COMP          32D2< 33C6<
1625_DIV           33C8<
1625_ENABLE        33D7<>
1625_ENABLE_L      33D6<>
1625_EXTVCC        33D5<> 39D1>
1625_FCB           33C6<
1625_INTVCC        33C5<> 39D1>
1625_RUNSS         33C6<
1625_SGND          33B7<> 39D1>
1625_TG            33C5<>
1625_VFB           33B5<>
1625_VIN           33C6< 39D1>
1625_VSW           33C4<> 39D1>
1772_ACIN          32B5<
1772_ACOK_L        32B5<> 32C4<>
1772_BST           32B4<>
1772_BST_ESR       32C3<
1772_CCI           32B5<>
1772_CCS           32B5<>
1772_CCV           32B5<>
1772_CCV_RC        32B5<
1772_CELLS         32B4<
1772_CLS           32A4<
1772_CSIN          32B4<> 38A2>
1772_CSIP          32B4<> 38A2>
1772_CSSN          32C5< 38A2>
1772_CSSP          32C5< 38A2>
1772_DCIN          32B5< 39C6>
1772_DHI           32B4<>
1772_DLO           32B4<>
1772_DLOV          32B4<> 39C6>
1772_GND           32A5<> 39C6>
1772_ICHG          32B5<>
1772_ICTL          32B5<>
1772_IINP          32B5<
1772_LDO           32C4<> 39C6>
1772_LX            32B4<> 39C6>
1772_REF           32B5<>
1772_VCTL          32B5<
1778_BG            19A5<> 39B1>
1778_BST           19A5<> 39B1>
1778_BST_RC        19A4<> 39B1>
1778_FCB           19A5<> 39B1>
1778_GND           19A5< 19A7<> 39B1>
1778_ION           19A5<> 39B1>
1778_ITH           19A5<> 39B1>
1778_ITH_RC        19A7<> 39B1>
1778_SHDN_L        19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG            19A5<> 39B1>
1778_VCC           19A5<> 39B1>
1778_VFB           19A2< 19A5<> 39B1> 40A1>
1778_VIN           19A5<> 39B1>
1778_VRNG          19A5< 39B1>
3405_MODE          28D5<
3405_VFB           28D4<>
3707_FCB           34C5<
3707_FSET          34C5<
3707_INTVCC        34D4<> 39D1>
3707_SGND          34B5<> 39D1>
3707_STBY          34C5<>
A29_CLS_ADJ        32A5<>
A29_CURRENT_ADJ    32C4<>
A29_DETECT         31A2< 32A5<> 32C4<>
A29_DET_L          31A3<
AB_SEL_LOW         35A6<>
AC_DET             31A4<
AC_DIV             32C8<
AC_ENABLE_GATE     32D6<>
AC_ENABLE_L        32C6<>
AC_GTR_18V         32C4<>
AC_IN              28B8<> 30C8< 31B3< 32C5<> 32C7<>
AC_IN_FW_CNTL      30C8<>
AC_IN_L            31B8<> 32C2<> 32C6<>
AC_IN_L_RC         32C2<>
ADAPTER_DET        31A4< 32D8<> 40C2>
ADAPTER_I_REG      32D3<>
ADT7460_ADR_EN_L   26B3<>
ADT7460_FAN1_PWM   26B3<>
ADT7460_FAN2_PWM   26B3<>
ADT7460_THERM      26A5<> 26B3<>
ADT7460_VCC        26C3<
ADT7460_VCORE_MON  5C8<> 26B4<>
AGP8X_DET_PU       18C6<>
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AGP_AD<2>          12C2<> 18C7<>
AGP_AD<3>          12C2<> 18C7<>
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AGP_AD<12>         12C2<> 18C7<>
AGP_AD<13>         12C2<> 18C7<>
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AGP_AD<16>         12C2<> 18C7<>
AGP_AD<31..16>     38D5>
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AGP_AD<18>         12C2<> 18C7<>
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AGP_AD<22>         12C2<> 18C7<>
AGP_AD<23>         12C2<> 18C7<>
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AGP_AD<25>         12C2<> 18D7<>
AGP_AD<26>         12C2<> 18D7<>
AGP_AD<27>         12B2<> 18D7<>
AGP_AD<28>         12B2<> 18D7<>
AGP_AD<29>         12B2<> 18D7<>
AGP_AD<30>         12B2<> 18D7<>
AGP_AD<31>         12B2<> 18D7<>
AGP_AD_STB<0>      12A2<> 12B2< 18D6<> 38D5>
AGP_AD_STB<1>      12A2<> 12B2< 18D6<> 38D5>
AGP_AD_STB_L<0>    12A2<> 12B2< 18D6<> 38D5>
AGP_AD_STB_L<1>    12A2<> 12A2< 18D6<> 38D5>
AGP_ATI_RESET_L    18B7<
AGP_ATI_VREF       18B7<
AGP_ATI_VREFG      18B7<
AGP_BUSY_L         12C4<> 12D2< 18D6>
AGP_CBE<0>         12B2<> 18B7<>
AGP_CBE<1..0>      38D5>
AGP_CBE<1>         12B2<> 18B7<>
AGP_CBE<2>         12B2<> 18B7<>
AGP_CBE<3..2>      38D5>

AGP_CBE<3>         12B2<> 18C7<>
AGP_DEVSEL_L       12B2<> 12C2< 18B7<> 38D5>
AGP_FRAME_L        12B2<> 12C2< 18B7<> 38D5>
AGP_GNT_L          12C2< 12D2< 18B7< 38D5>
AGP_INT_L          14B5<> 18B7<>
AGP_IRDY_L         12B2<> 12C2< 18B7<> 38D5>
AGP_PAR            12B2<> 18B7> 38D5>
AGP_PIPE_L         12A2<> 12B2<
AGP_RBF_L          12A2<> 12C2< 18C6<> 38D5>
AGP_REQ_L          12C2< 12D2<> 18B7<> 38D5>
AGP_SBA<0>         12B2<> 18C6<
AGP_SBA<7..0>      38D5>
AGP_SBA<1>         12B2<> 18C6<
AGP_SBA<2>         12B2<> 18C6<
AGP_SBA<3>         12B2<> 18C6<
AGP_SBA<4>         12B2<> 18C6<
AGP_SBA<5>         12B2<> 18C6<
AGP_SBA<6>         12B2<> 18C6<
AGP_SBA<7>         12B2<> 18C6<>
AGP_SB_STB         12B2<> 12B2< 18C6<> 38D5>
AGP_SB_STB_L       12A2<> 12A2< 18C6<> 38D5>
AGP_ST<0>          12A2<> 18C6<
AGP_ST<1>          12A2<> 18C6<
AGP_ST<2>          12A2<> 18C6<
AGP_STOP_L         12B2<> 12C2< 18B7<> 38D5>
AGP_STP_L          18C6<
AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L         12B2<> 12C2< 18B7<> 38D5>
AGP_WBF_L          12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L   25C6<> 40C1>
AIRPORT_IDSEL      25C5<> 40B1>
AIRPORT_PCI_GNT_L  12D7<> 25D5<> 40C4>
AIRPORT_PCI_INT_L  14B5<> 14D7<> 25D5<> 40C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 25D6<> 40D4>
AIRPORT_PME_L_TP   25D5<>
AMP_CONTROL        26C5<> 26D4<>
ATI_AGP_FBSKEW<0>  19C2< 19C7<>
ATI_AGP_FBSKEW<1>  19C2< 19C7<>
ATI_BUS_CFG<0>     19B2< 19C7<>
ATI_BUS_CFG<1>     19B2< 19C7<>
ATI_BUS_CFG<2>     19B2< 19C7<>
ATI_CLK27M_IN      18C1< 19B7<
ATI_CLK27M_OSC     18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU      18C6<>
ATI_DBI_LO_PU      18C6<>
ATI_DVOVMODE       21A2<
ATI_GPIO7          19C7<>
ATI_GPIO8_PD       19C7<>
ATI_GPIO9_SPN      19C7<>
ATI_GPIO10_SPN     19C7<>
ATI_GPIO11_SPN     19C7<>
ATI_GPIO12_SPN     19C7<>
ATI_GPIO13_SPN     19C7<>
ATI_HSYNC          19D5<> 22C8<
ATI_MEMTEST        18A6<>
ATI_MEMVMODE0      18A7<
ATI_MEMVMODE1      18A7<
ATI_OSC_OE         18D3<
ATI_PVDD_BYP       21D6<>
ATI_R2SET          19D6<>
ATI_RSET           19D6<>
ATI_RSTB_MSK       18C6<>
ATI_SSCLK_IN       18B1< 19B7<>
ATI_SSCLK_UF       18B1<>
ATI_TESTEN         19B7<
ATI_TMDS_CLKN      19B7> 20D4<
ATI_TMDS_CLKP      19B7> 20D4<
ATI_TMDS_DN<0>     19B7> 20D4<
ATI_TMDS_DN<1>     19B7> 20C4<
ATI_TMDS_DN<2>     19B7> 20C3<
ATI_TMDS_DP<0>     19B7> 20D4<
ATI_TMDS_DP<1>     19B7> 20C4<
ATI_TMDS_DP<2>     19B7> 20C3<
ATI_TPVDD_BYP      21D1<>
ATI_VSYNC          19D5<> 22C8<
ATI_X1CLK_SKEW<0>  19C2< 19C7<>
ATI_X1CLK_SKEW<1>  19B2< 19C7<>
AUDIO_EXT_MCLK_SEL  26C7<> 26D7<
AUDIO_GPIO_11      26D7<> 26D7<
AUDIO_LI_DET_L     14B5<> 26C5<>
AUDIO_LI_OPTICAL_PLUG_L  26C5<> 26D7<
AUDIO_LO_DET_L     14B5<> 26D5<>
AUDIO_LO_MUTE_L    26C5<> 26C7<>
AUDIO_LO_OPTICAL_PLUG_L  26D5<> 26D7<
AUDIO_SPKR_MUTE_L_F  26C5<> 26C7<
BATTV_HIGH         32B7<>
BATTV_LOW          32B8<>
BATT_14PBUS_EN     32C1<>
BATT_14V_GATE      32C1<>
BATT_24PBUS_EN     32C2<>
BATT_24V_GATE      32C1<>
BATT_CLK           32A4<> 40C3>
BATT_DATA          32A4<> 40C3>
BATT_DIV           32A5<
BATT_ISNS_OUT      24A4<>
BATT_ISNS_R        24A3<>
BATT_LOW           32A6<>
BATT_LOW_L         32B6<>
BATT_NEG           32A4<> 39C6> 40C3>
BBANG_HRESET_L     6A2< 6B3<> 23C4<> 40C1>
BBANG_JTAG_TCK     6A4< 6B1<> 6C2< 23C4<>
BBANG_TCK_EN       6A4<
BB_MISO            6B3<> 6C2<
BB_MOSI            6B3<> 6C2<
BB_RESET_L         6C3<
BB_SCK             6B3<> 6C2<
BB_XTAL1_SPN       6C3<>
BCKFD_PROT_EN_L    32C6<>
BCKFD_PROT_GATE    32D6<>
BFR_TDO            6C1<> 6D2<
BRIGHT_PWM         22A1<> 40A7>
BRIGHT_PWM_UF      22A2<>
BT_USB_DM          14C1< 25B2<> 38B2> 40B6>
BT_USB_DP          14C1< 25B2<> 38B2> 40B6>
CAPSLOCK_LED_L     31C7<
CBUS_ADDR<0>       17B1< 17B4>
CBUS_ADDR<1>       17B1< 17B4>
CBUS_ADDR<2>       17B1< 17B4>
CBUS_ADDR<3>       17B1< 17B4>
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CBUS_ADDR<6>       17B1< 17B4>
CBUS_ADDR<7>       17B1< 17B4>
CBUS_ADDR<8>       17B1< 17B4>
CBUS_ADDR<9>       17B1< 17B4>
CBUS_ADDR<10>      17B4> 17C1<
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CBUS_ADDR<12>      17B1< 17B4>
CBUS_ADDR<13>      17B1< 17B4>
CBUS_ADDR<14>      17B1< 17B4>
CBUS_ADDR<15>      17B1< 17B4>
CBUS_ADDR<16>      17B1< 17B4<
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CBUS_ADDR<18>      17B2< 17B4>
CBUS_ADDR<19>      17B2< 17B4>
CBUS_ADDR<20>      17B2< 17B4>
CBUS_ADDR<21>      17B2< 17B4>
CBUS_ADDR<22>      17A4> 17B2<
CBUS_ADDR<23>      17A4> 17B2<
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CBUS_ADDR<25>      17A4> 17B2<
CBUS_ADDR_16_UF    17B5<>
CBUS_BVD1_L        17B2< 17C4<
CBUS_BVD2_L        17B2< 17C4<
CBUS_CE1_L         17C1< 17C4>
CBUS_CE2_L         17B4> 17C2<
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CBUS_DATA<1>       17A1< 17A4<>
CBUS_DATA<2>       17A1< 17A4<>
CBUS_DATA<3>       17A4<> 17C1<
CBUS_DATA<4>       17A4<> 17C1<
CBUS_DATA<5>       17A4<> 17C1<
CBUS_DATA<6>       17A4<> 17C1<
CBUS_DATA<7>       17A4<> 17C1<
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CBUS_DATA<9>       17A2< 17A4<>
CBUS_DATA<10>      17A2< 17A4<>
CBUS_DATA<11>      17A4<> 17C2<
CBUS_DATA<12>      17A4<> 17C2<
CBUS_DATA<13>      17A4<> 17C2<
CBUS_DATA<14>      17A4<> 17C2<
CBUS_DATA<15>      17A4<> 17C2<
CBUS_DET_1_L       17C2< 17C4< 40B8>
CBUS_DET_2_L       17A2< 17C4< 40B8>
CBUS_INPACK_L      17B2< 17B4<
CBUS_INT_L         14B5<> 14B7< 17A7<>
CBUS_IORD_L        17B2< 17C4>

CBUS_IOWR_L        17B2< 17C4>
CBUS_MFUNC1_PD     17A7<> 17A7<
CBUS_MFUNC2_PD     17A7<> 17A7<
CBUS_MFUNC3_PD     17A7<> 17A7<
CBUS_MFUNC4_PD     17A7<> 17A7<
CBUS_MFUNC5_PD     17A7<> 17A7<
CBUS_MFUNC6_PD     17A7< 17A7<>
CBUS_OE_L          17C1< 17C4>
CBUS_PCI_GNT_L     12D7<> 17A7<
CBUS_PCI_IDSEL     17B7<
CBUS_PCI_PERR_L    17B7<> 17D7<
CBUS_PCI_REQ_L     12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L   17A7<
CBUS_PCI_SERR_L    17B7> 17D7<
CBUS_READY         17B1< 17C4<
CBUS_REG_L         17B2< 17C4>
CBUS_RESET_L       17B2< 17C4>
CBUS_SUSPEND_PU    17A7< 17D7<
CBUS_VCCD0_L       17C4<>
CBUS_VCCD1_L       17C4<>
CBUS_VPPD0         17C4<>
CBUS_VPPD1         17C5<>
CBUS_VS1           17B2< 17C4<>
CBUS_VS2           17B2< 17C4<>
CBUS_WAIT_L        17B2< 17B4<
CBUS_WE_L          17B1< 17C4>
CBUS_WP_L          17A1< 17B4<
CG_ADDRSEL         14B7<
CG_CLKOUT          14B6<>
CG_FSEL            14B7< 14C5<
CG_LOCK            14B7<>
CG_RESET_L         14B7<
CG_SYSCLK_EN       14A6< 14B7<
CHARGE_DISABLE     32A7<>
CHARGE_LED_L       31C6<> 31D7< 32D8<> 40D2>
CHGND1             39A6>
CHGND2             39A6>
CHGND3             39A6>
CHGND4             39A6> 40B6>
CHGND5             39A6>
CHGND6             39A6>
CLK10M_PMU_XIN     31B6<
CLK10M_PMU_XOUT    31B6<
CLK10M_PMU_XOUT_UF  31A7<
CLK18M_INT_EXT     14A6<> 37B1>
CLK18M_INT_XIN     14A5< 37B1>
CLK18M_INT_XOUT    14A5<> 37B1>
CLK18M_XTAL_IN     14A5< 37B1>
CLK25M_ENET_XIN    28A7< 37B1>
CLK25M_ENET_XOUT   28A7<> 37B1>
CLK25M_XTAL_IN     28A7<
CLK27M_GPU_XIN     37B1>
CLK27M_GPU_XOUT    37B1>
CLK27M_XTAL_IN     37B1>
CLK32K_PMU_XIN     31B3<>
CLK32K_PMU_XOUT    31B3<>
CLK32K_PMU_XOUT_UF  31B2<>
CLK33M_AIRPORT     12D8< 25D5<> 37C1> 40B1>
CLK33M_AIRPORT_UF  12C7<> 37C1>
CLK33M_CBUS        12D8< 17A7< 37C1>
CLK33M_CBUS_UF     12C7<> 37C1>
CLK33M_USB2        12C8< 27B7<> 37C1>
CLK33M_USB2_UF     12C7<> 37C1>
CLK66M_AGP_15V_TP  12C4<
CLK66M_GPU_AGP     12C8< 18B7<> 37C1>
CLK66M_GPU_AGP_UF  12C7<> 37C1>
CLKENET_LINK_GBE_REF  13C5< 28C8< 37B1>
CLKENET_LINK_GTX   13C5<> 37A1>
CLKENET_LINK_RX    13D5< 28C8< 37B1>
CLKENET_LINK_TX    13D5< 28D8< 37A1>
CLKENET_PHY_GBE_REF  28C7<> 37B1>
CLKENET_PHY_GTX    13C6< 28C7< 37A1>
CLKENET_PHY_RX     28C7<> 37B1>
CLKENET_PHY_TX     28D7<> 37B1>
CLKFW_LINK_LCLK    13C3<> 37A1>
CLKFW_LINK_PCLK    13C3<> 29C3< 37A1>
CLKFW_PHY_LCLK     13C2< 29B8< 37A1>
CLKFW_PHY_PCLK     29B4> 29C3< 37A1>
CLKLVDS_LN         19B5> 22A4<> 38C2> 40B7>
CLKLVDS_LP         19B5> 22A4<> 38C2> 40B7>
CLKLVDS_UN         19B5> 22A4<> 38C2> 40B7>
CLKLVDS_UP         19B5> 22A4<> 38C2> 40A7>
COMM_DTR_L         14C2> 26D1<> 40B2>
COMM_GPIO_L        14C2<> 26D2<> 40C2>
COMM_RESET_L       14C5<> 26D3<> 40C4>
COMM_RING_DET_L    14B5<> 14C7<> 26C2<> 31C6<> 40C4>
COMM_RTS_L         14C2> 26D1<> 40B2>
COMM_RXD           14C2<> 26D1<> 40B2>
COMM_SHUTDOWN      14C5<> 26D3<> 40C4>
COMM_TRXC          14C2<> 26D2<> 40C2>
COMM_TXD_L         14C2<> 26D2<> 40C2>
COMP_DISABLE       22C2<>
COMP_ENABLE        22C1<>
COMP_RC            33C6<
CPU_AACK_L         5A7< 8B6<> 8C2< 37D5>
CPU_ADDR<0>        5C7<> 8D6<>
CPU_ADDR<0..31>    37D5>
CPU_ADDR<1>        5C7<> 8D6<>
CPU_ADDR<2>        5C7<> 8D6<>
CPU_ADDR<3>        5C7<> 8D6<>
CPU_ADDR<4>        5C7<> 8D6<>
CPU_ADDR<5>        5C7<> 8C6<>
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CPU_ADDR<7>        5C7<> 8C6<>
CPU_ADDR<8>        5C7<> 8C6<>
CPU_ADDR<9>        5C7<> 8C6<>
CPU_ADDR<10>       5B7<> 8C6<>
CPU_ADDR<11>       5B7<> 8C6<>
CPU_ADDR<12>       5B7<> 8C6<>
CPU_ADDR<13>       5B7<> 8C6<>
CPU_ADDR<14>       5B7<> 8C6<>
CPU_ADDR<15>       5B7<> 8C6<>
CPU_ADDR<16>       5B7<> 8C6<>
CPU_ADDR<17>       5B7<> 8C6<>
CPU_ADDR<18>       5B7<> 8C6<>
CPU_ADDR<19>       5B7<> 8C6<>
CPU_ADDR<20>       5B7<> 8C6<>
CPU_ADDR<21>       5B7<> 8C6<>
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CPU_ADDR<29>       5B7<> 8C6<>
CPU_ADDR<30>       5B7<> 8C6<>
CPU_ADDR<31>       5B7<> 8B6<>
CPU_ARTRY_L        5A7<> 8B6<> 8D2< 37D5>
CPU_AVDD           5C3< 39D3>
CPU_AVDD_ADJ       5C2<>
CPU_AVDD_PG        5C3<>
CPU_AVDD_VIN       5C3<
CPU_AVDD_VOUT      5C3<>
CPU_BG_L           5C7< 8C2< 8D6<> 37D5>
CPU_BR_L           5C7> 8D2< 8D6<> 37D5>
CPU_BUS_VSEL       5C4< 7A6<
CPU_CHKSTP_OUT_L   5B4<> 5C2< 40D8>
CPU_CHKS_L         5A4< 5D2<
CPU_CI_L           5A7> 8B6<> 37D5>
CPU_CLKOUT_SPN     5C4>
CPU_CLK_EN         8A6< 31C4<>
CPU_DATA<0>        6D8<> 8D4<>
CPU_DATA<0..31>    37D5>
CPU_DATA<1>        6D8<> 8D4<>
CPU_DATA<2>        6D8<> 8D4<>
CPU_DATA<3>        6D8<> 8D4<>
CPU_DATA<4>        6D8<> 8D4<>
CPU_DATA<5>        6D8<> 8D4<>
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CPU_DATA<7>        6D8<> 8D4<>
CPU_DATA<8>        6D8<> 8D4<>
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CPU_DATA<10>       6C8<> 8D4<>
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CPU_DATA<53>       6B8<> 8A8< 8B4<>
CPU_DATA<54>       6B8<> 8A8< 8B4<>
CPU_DATA<55>       6B8<> 8A8< 8B4<>
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CPU_DATA<57>       6B8<> 8B3< 8B4<>
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CPU_DATA<63>       6A8<> 8B3< 8B4<>
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CPU_DRDY_L_UF      37D5>
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CPU_EMODE1_L       5A4< 5C2<
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CPU_HIT_L          5A7> 8B6< 8D2< 37D5>
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CPU_HRESET_L       5B4< 5C2< 6A1<> 7A5< 7A8< 40C8>
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CPU_L2TSTCLK       5B4< 5C2<
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CPU_M_DP           26A7< 26B6<
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CPU_PLL_FS01       7C4<
CPU_PLL_FS10       7C4<
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CPU_PULLUP         5A4< 5A4< 5C2<
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CPU_SRWX_L         5A4< 5C2<
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CPU_TBEN           5B4< 5D2< 8A6<>
CPU_TBST_L         5A7> 8B6<> 37D5>
CPU_TEA_L          5B4< 8A4<> 8C2< 37D5>
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CPU_THERM_DP       6A6<> 26A6<
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CPU_TSIZ<1>        5A7> 8B6<>
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CPU_VCORE_SEQ_L    35D8<
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CPU_VCORE_SNUB     35B3<
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CSLOT_ADDR4_SPN    13B7>
CSLOT_ADDR5_SPN    13B7>
CSLOT_ADDR6_SPN    13B7>
CSLOT_ADDR7_SPN    13B7>
CSLOT_ADDR8_SPN    13B7>
CSLOT_ADDR9_SPN    13B7>
CSLOT_CE1_L_SPN    13C7>
CSLOT_CE2_L_SPN    13C7>
CSLOT_IORD_L_SPN   13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN   13C7>
CSLOT_OE_L_SPN     13C7>
CSLOT_WE_L_SPN     13C7>
CURRENT_THRESHOLD  32C4<
CY25811_S0         18B2<
CY25811_S1         18B2<
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DCDC_EN_CTRL       30C8<>
DCDC_EN_L          34B6< 34B7<> 36C7<>
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DDR_VREF           11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                 39D3>
DVI_DDC_CLK        22D4<>
DVI_DDC_CLK_UF     22C5<> 22D3<> 40C7>
DVI_DDC_DATA       22C4<>
DVI_DDC_DATA_UF    22C5<> 40C7>
DVI_HPD            22C4<>
DVI_HPD_DIV        22C3<
DVI_HPD_UF         22C3< 22C5<> 40C7>
DVI_TRUN_ON_ILIM   22D2<
DVI_TURN_ON        22D3<>
DVI_TURN_ON_BASE   22D2<
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EIDE_DATA<12>      13B7<> 25D8<
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ENET_LINK_TX_ER    13D5<> 38A5>
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ENET_RX_ER         13C5< 28B7> 38A5>
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FANL_PWM           26A3<> 26C2<> 40B3>
FANL_TACH          26A3<> 26B2< 40B3>
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FP_PWR_EN_L        22B3<
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FW_PHY_DATA<7..0>  38A5>
FW_PHY_DATA<1>     29B8<>
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FW_R1              29A5<>
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FW_TPA0P           29B1<> 30C4<> 38D2>
FW_TPA0P_CONN      30C3<>
FW_TPA1N           29B1<> 30A4<> 38C2>
FW_TPA1P           29B1<> 30A4<> 38C2>
FW_TPB0N           29B1<> 30C4<> 38D2>
FW_TPB0N_CONN      30C3<>
FW_TPB0P           29B1<> 30C4<> 38D2>
FW_TPB0P_CONN      30C3<>
FW_TPB1N           29B1<> 30A4<> 38C2>
FW_TPB1P           29B1<> 30A4<> 38C2>
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FW_TPO0P           38C2>
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FW_TPO1N           30A3<> 38C2> 40D2>
FW_TPO1P           30A3<> 38C2> 40D2>
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FW_VGND1           30A3<> 39A3>
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FW_XI              29A5<> 37A1>

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GPU_AUXWIN         19C5<>
GPU_B              19D6<> 22D8<
GPU_C              19D6<> 22A8<
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GPU_CLK27M_UF      37C1>
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GPU_DVI_DDC_DATA   19C5<> 22C3<>
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GPU_DVOD<1>        19D7<> 20C8<
GPU_DVOD<2>        19D7<> 20C8<
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GPU_DVO_CLKP_R1    19C8< 20B8<
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GPU_DVO_VSYNC      19C7<> 20A7< 20B8< 38C5>
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GPU_FBCLK0_L       37B1>
GPU_FBCLK1         37B1>
GPU_FBCLK1_L       37B1>
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GPU_HPD            19C5<> 22C3<>
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GPU_MEM_IO_FLT     21C2< 39C3>
GPU_R              19D6<> 22D8<
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GPU_SSCLK_UF       37C1>
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GPU_TV_GND2        22A8<> 39B6>
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GPU_VCORE_NECK     19B5<> 39B3>
GPU_VCORE_PWR_SEQ  19A8<>
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GPU_VCORE_SEQ_L    19A8<
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HD_ADDR<2..0>      38C5>
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HD_CS1_L           25B3< 25C1<> 38B5>
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HD_DATA<14>        25C1<> 25C3<
HD_DATA<15>        25B3< 25C1<>
HD_DIOR_L          25A3< 25C2<> 38B5>
HD_DIOW_L          25A3< 25C1<> 38B5>
HD_DMACK_L         25A3< 25C2<> 38B5>
HD_DMARQ           13C6< 25C2<> 38B5>
HD_INTRQ           13C6< 25C1<> 38B5>
HD_IOCHRDY         25A3< 25C1<> 38B5>
HD_RESET_L         25A3< 25D2<> 38B5>
HIGH_VCORE         19A2<>
HIGH_VCORE_DIV     19A3<
HPD_4V_REF         22C3<
HPD_BASE           22C1<
HPD_ON             22C2<>
HPD_ON_RC          22C2<
HPD_PWR_SNS_EN     19C7<> 22C3<>
HPD_PWR_SW         22C2<>
I2S0_BITCLK_F      26C7<> 26C7<
I2S0_DEV_TO_SB_DTI_F  26C7<> 26C7<
I2S0_MCLK_F        26C7<> 26D7<
I2S0_RESET_L_F     26C5<> 26C7<
I2S0_SB_TO_DEV_DTO_F  26C7< 26C7<>
I2S0_SYNC_F        26C7<> 26D7<
I2S2_BITCLK_F      26B7<> 26C7<
I2S2_DEV_TO_SB_DTI_F  26C6<> 26C7<>
I2S2_RESET_L_F     26B6<> 26C5<>
I2S2_SYNC_F        26B7<> 26C7<>
IAC_FB             32D4<
IAC_RC_COMP        32D4<
ICT_TRST_L         6B1<> 6D2<
INTREPID_ACS_REF   8A6<
INT_AGPPVT         12D4<>
INT_AGP_FB_IN      12C4< 37C1>
INT_AGP_FB_OUT     12C4<> 37C1>
INT_AGP_VREF       12B4<> 12D4<> 18D5< 39D3>
INT_AUDIO_TO_SND   14B2< 26C8< 40C6>
INT_CPUFB_IN       8A6<> 8B6< 37D1>
INT_CPUFB_IN_NORM  8A4< 37D1>
INT_CPUFB_LONG     8A4< 37D1>
INT_CPUFB_OUT      8A6<> 8A6< 37D1>
INT_CPUFB_OUT_NORM  8A4< 37D1>
INT_CPUFB_OUT_SHORT  8A5< 37D1>
INT_DDRCLK2_N_TP   9B6<>
INT_DDRCLK2_P_TP   9B6<>
INT_DDRCLK5_N_TP   9B6<>
INT_DDRCLK5_P_TP   9B6<>
INT_ENET_RST_L     14B5<> 28B8<
INT_EXTINT3_PU     14B5<> 14B7< 26D8<
INT_EXTINT8_PU     14B5<> 14C7<
INT_EXTINT10_PU    14A7< 14B5<>
INT_EXTINT13_PU    14B5<> 14B7<
INT_EXTINT14_PU    14B5<> 14C7< 26D8<
INT_EXTINT16_PU    14B5<> 14B7<
INT_GPIO0          14C5<>
INT_GPIO1_PU       14C5<> 14C7< 35C8<
INT_GPIO9_PU       14A7< 14C5< 26D8<
INT_GPIO9_PU_H     14B5<>
INT_GPIO12_PU      14B5<> 14B7< 26B7<
INT_GPIO15_PU      14B5<> 14C7< 26D8<
INT_I2C_CLK0       6B3<> 6D2< 11A3<> 11A8<> 13C2<
                 13C3<> 23D4<> 40B8>
INT_I2C_CLK1       13C2< 13C3<> 14B7< 23A7<> 24C2<>
                 26B4<> 40B8>
INT_I2C_CLK2       14A2<> 26C5<> 26D3<> 40C6>
INT_I2C_DATA0      6B3<> 6D2<> 11A3<> 11A8<> 13C2<
                 13C3<> 23D4<> 40B8>
INT_I2C_DATA1      13B2< 13C3<> 14B7< 23A7<> 24C2<>
                 26B4<> 40B8>
INT_I2C_DATA2      14A2<> 26C3<> 26C5<> 40C6>
INT_JTAG_TEI       13C2< 13C5<
INT_MEM_REF_H      9B6< 39D3>
INT_MEM_VREF       9A7< 9B6<> 39D3>
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT_UF  14A3<> 14B7<
INT_MOD_DTI        14A2< 26C7< 26D2<> 40B1>
INT_MOD_DTI_UF     14A7<
INT_MOD_DTO_UF     14A3<> 14B7<
INT_MOD_SYNC_UF    14A3<> 14A7<

INT_PCI_FB_IN      12C7< 37C1>
INT_PCI_FB_OUT     12C7<> 37C1>
INT_PEND_PROC_INT  14A5> 31C4<>
INT_PROC_SLEEP_REQ_L  14A5< 31B4<>
INT_PU_RESET_L     13D3< 26D3<> 31A2< 31C4<>
INT_REF_CLK_IN     14A5< 14B5< 37C1>
INT_REF_CLK_OUT    14A5> 14B7< 37C1>
INT_RESET_L        9B3< 13D3< 31C7< 31D4<>
INT_ROM_CS_L       12A6< 12C7>
INT_ROM_OE_L       12A6< 12C7>
INT_ROM_RW_L       12A6< 12C7>
INT_SND_CLKOUT     14A3<>
INT_SND_SCLK       14A3<>
INT_SND_SYNC       14B3<>
INT_SND_TO_AUDIO   14B3<>
INT_SUSPEND_ACK_L  8B6> 31B6<>
INT_SUSPEND_REQ_L  8B6< 31B6<> 31C7<
INT_TST_MONIN_PD   13C2< 13C5<
INT_TST_MONOUT_TP  13C5>
INT_TST_PLLEN_PD   13C5< 13D2<
INT_WATCHDOG_L     14A5> 31C6<>
INV_ON_PWM         19C6<> 22A3<
IO_RESET_L         17A7< 23D6< 24C2< 27B8< 28B8<
                 31C6<> 31D7<
JTAG_ASIC_TCK      13C5< 13D2< 28A5< 40D8>
JTAG_ASIC_TDI      28A5< 28D7< 40D8>
JTAG_ASIC_TDO      13C5> 13D2< 14A7< 40D8>
JTAG_ASIC_TMS      13C5< 13D2< 28A5< 40D8>
JTAG_ASIC_TRST_L   13C2< 13C5< 28A5< 40D8>
JTAG_CPU_TCK       5B2< 5B4< 6A3> 40C8>
JTAG_CPU_TDI       5B2< 5C4< 6B1<> 23D4<> 40C8>
JTAG_CPU_TDO_TP    5C4> 40C8>
JTAG_CPU_TMS       5B2< 5B4< 6B1<> 23C4<> 40C8>
JTAG_CPU_TRST_L    5B3< 5B4< 6B1<> 23D4<> 40B1> 40C8>

JTAG_ENET_TDO      13C5< 13D2< 28A5>
KBDLED_ANODE       23A7<> 23B5<> 39B6>
KBDLED_RETURN      23A7<> 23B5<> 39B6>
KBD_CAPSLOCK_LED   40B4>
KBD_COMMAND_L      23A4< 31C6<>
KBD_CONTROL_L      23A4< 31C6<> 40B4>
KBD_FUNCTION_L     23A4< 31C6<> 40B4>
KBD_ID             23B4< 31B6<>
KBD_LED1_OUT       40C2>
KBD_LED2_OUT       40C2>
KBD_NUMLOCK_LED    40C3>
KBD_OPTION_L       23A4< 31B6<> 40B4>
KBD_SHIFT_L        23A4< 31C6<> 40B4>
KBD_X<0>           23A4< 31C6<> 40B4>
KBD_X<1>           23A4< 31C6<> 40B4>
KBD_X<2>           23A4< 31C6<>
KBD_X<3>           23A4< 31C6<> 40B4>
KBD_X<4>           23A4< 31C6<>
KBD_X<5>           23B4< 31C6<>
KBD_X<6>           23B4< 31C6<>
KBD_X<7>           23B4< 31C6<>
KBD_X<8>           23B4< 31C6<> 40A4>
KBD_X<9>           23A4< 31C6<>
KBD_Y<0>           31D6<> 40D3>
KBD_Y<1>           31D6<> 40D3>
KBD_Y<2>           31D6<>
KBD_Y<3>           31D6<> 40D3>
KBD_Y<4>           31D6<> 40D3>
KBD_Y<5>           31D6<>
KBD_Y<6>           31C6<> 40C3>
KBD_Y<7>           31C6<> 40C3>
LCD_DIGON_L        22A6<
LCD_PWREN_L        22A5<>
LED_LINK10         28B5<>
LED_LINK100        28B5<>
LED_RX_SPN         28B5>
LEFT_USB_DM        25B2<> 27B3< 38A2> 40D1>
LEFT_USB_DP        25B2<> 27A3< 38A2> 40D1>
LID_CLOSED_L       23A6<> 40C4>
LM2594_IN          29D8<> 39B3>
LT1962_INT_ADJ     14D6<
LT1962_INT_BYP     14D6<>
LTC1625_ITH        32D3<>
LTC1962_1V5_VIN    39A1>
LTC1962_1V5_VOUT   39A1>
LTC1962_INT_VIN    14D7<> 39A1>
LTC1962_L3_VIN     39A1>
LTC1962_L3_VOUT    39A1>
LTC3405_SW         28D4<> 39B3>
LTC3411_GND        39A1>
LTC3411_ITH        39A1>
LTC3411_ITH_RC     39A1>
LTC3411_SHDN       39A1>
LTC3411_SYNC       39A1>
LTC3411_VCC        39B1>
LTC3412_GND        36A6<>
LTC3412_ITH        36A6<>
LTC3412_ITH_RC     36A6<
LTC3412_PGOOD      36A4<>
LTC3412_RT         36A6<
LTC3412_RUNSS      36A6<>
LTC3412_SYNC       36A6<>
LTC3412_VFB        36A6<>
LTC3412_VFB_DIV    36A6<
LTC3707_START_RC   34B6<>
LVDS_DDC_CLK       19C5<> 22B5<> 40A7>
LVDS_DDC_DATA      19C5<> 22B5<> 40A7>
LVDS_L0N           19B5> 22B4<> 38C2> 40C7>
LVDS_L0P           19B5> 22B4<> 38C2> 40C7>
LVDS_L1N           19B5> 22B4<> 38C2> 40C7>
LVDS_L1P           19B5> 22B4<> 38C2> 40C7>
LVDS_L2N           19B5> 22B4<> 38C2> 40C7>
LVDS_L2P           19B5> 22B4<> 38C2> 40C7>
LVDS_L3N_TP        19B5>
LVDS_L3P_TP        19B5>
LVDS_U0N           19C5> 22A4<> 38C2> 40B7>
LVDS_U0P           19C5> 22A4<> 38C2> 40B7>
LVDS_U1N           19C5> 22A4<> 38C2> 40B7>
LVDS_U1P           19C5> 22A4<> 38C2> 40B7>
LVDS_U2N           19B5> 22A4<> 38B2> 40B7>
LVDS_U2P           19B5> 22A4<> 38B2> 40B7>
LVDS_U3N_TP        19B5>
LVDS_U3P_TP        19B5>
MAIN_RESET_L       14C7< 17A7< 17D5< 18C8< 20C3<
                 25D6<> 27B8< 31D4<> 31D7< 40C1>
MASTER_SWING       20B7<
MAX1715_FB2        36B1< 36B4<
MAX1715_GND        36B5<> 36C5< 39C1>
MAX1715_ON_RC      36C7<>
MAX1715_REF        36B5<> 39C1>
MAX1715_SKIP       36C4< 39C1>
MAX1715_TON        36C5< 39C1>
MAX1715_VCC        36D5< 39C1>
MAX1717_AB_SEL     35A7< 35C6<
MAX4172_OUT        32D4<>
MAX8860_CC         21A6<>
MAX8860_FAULT      21A6<>
MAXBUS_SLEEP       5B2< 5D1< 5D5< 6B2< 6B4< 7B7< 7D8<
                 8B8< 8C3< 8C8< 8D1< 8D8< 15D8< 16D8<
                 35D8< 39D3>
MDI0_PD            28B4<
MDI1_PD            28B4<
MDI2_PD            28B4<
MDI3_PD            28B3<
MDI_M<0>           28B5<> 38D2>
MDI_M<1>           28B5<> 38D2>
MDI_M<2>           28B5<> 38D2>
MDI_M<3>           28B5<> 38D2>
MDI_P<0>           28B5<> 38D2>
MDI_P<1>           28B5<> 38D2>
MDI_P<2>           28B5<> 38D2>
MDI_P<3>           28B5<> 38D2>
MEM_ADDR<0>        9B5< 9D6<>
MEM_ADDR<12..0>    37A5>
MEM_ADDR<1>        9B5< 9D6<>
MEM_ADDR<2>        9B5< 9D6<>
MEM_ADDR<3>        9B5< 9D6<>
MEM_ADDR<4>        9B5< 9D6<>
MEM_ADDR<5>        9B5< 9D6<>
MEM_ADDR<6>        9B5< 9D6<>
MEM_ADDR<7>        9B5< 9D6<>
MEM_ADDR<8>        9B5< 9D6<>
MEM_ADDR<9>        9A5< 9D6<>
MEM_ADDR<10>       9A5< 9D6<>
MEM_ADDR<11>       9A5< 9D6<>
MEM_ADDR<12>       9A5< 9D6<>
MEM_BA<0>          9A5< 9D6<>
MEM_BA<1..0>       37A5>
MEM_BA<1>          9A5< 9C6<>
MEM_CAS_L          9A5< 9C6<> 37A5>
MEM_CKE<0>         9B6<> 9C5<
MEM_CKE<3..0>      37A5>
MEM_CKE<1>         9B6<> 9C5<

MEM_CKE<2>         9B6<> 9C5<
MEM_CKE<3>         9B6<> 9C5<
MEM_CS_L<0>        9C5< 9C6<>
MEM_CS_L<3..0>     37A5>
MEM_CS_L<1>        9C5< 9C6<>
MEM_CS_L<2>        9C5< 9C6<>
MEM_CS_L<3>        9C5< 9C6<>
MEM_DATA<0>        9D8<> 10C7<>
MEM_DATA<7..0>     37C5>
MEM_DATA<1>        9D8<> 10C7<>
MEM_DATA<2>        9D8<> 10C7<>
MEM_DATA<3>        9D8<> 10C7<>
MEM_DATA<4>        9D8<> 10C7<>
MEM_DATA<5>        9D8<> 10C7<>
MEM_DATA<6>        9D8<> 10C7<>
MEM_DATA<7>        9D8<> 10C7<>
MEM_DATA<8>        9D8<> 10C7<>
MEM_DATA<15..8>    37C5>
MEM_DATA<9>        9D8<> 10C7<>
MEM_DATA<10>       9D8<> 10C7<>
MEM_DATA<11>       9D8<> 10C7<>
MEM_DATA<12>       9D8<> 10B7<>
MEM_DATA<13>       9C8<> 10B7<>
MEM_DATA<14>       9C8<> 10B7<>
MEM_DATA<15>       9C8<> 10B7<>
MEM_DATA<16>       9C8<> 10C5<>
MEM_DATA<31..16>   37C5>
MEM_DATA<17>       9C8<> 10C5<>
MEM_DATA<18>       9C8<> 10C5<>
MEM_DATA<19>       9C8<> 10C5<>
MEM_DATA<20>       9C8<> 10C5<>
MEM_DATA<21>       9C8<> 10C5<>
MEM_DATA<22>       9C8<> 10C5<>
MEM_DATA<23>       9C8<> 10C5<>
MEM_DATA<24>       9C8<> 10C5<>
MEM_DATA<25>       9C8<> 10C5<>
MEM_DATA<26>       9C8<> 10C5<>
MEM_DATA<27>       9C8<> 10C5<>
MEM_DATA<28>       9C8<> 10C5<>
MEM_DATA<29>       9C8<> 10B5<>
MEM_DATA<30>       9C8<> 10B5<>
MEM_DATA<31>       9C8<> 10B5<>
MEM_DATA<32>       9C8<> 10C3<>
MEM_DATA<47..32>   37B5>
MEM_DATA<33>       9C8<> 10C3<>
MEM_DATA<34>       9C8<> 10C3<>
MEM_DATA<35>       9C8<> 10C3<>
MEM_DATA<36>       9C8<> 10C3<>
MEM_DATA<37>       9C8<> 10C3<>
MEM_DATA<38>       9C8<> 10C3<>
MEM_DATA<39>       9B8<> 10C3<>
MEM_DATA<40>       9B8<> 10C3<>
MEM_DATA<41>       9B8<> 10C3<>
MEM_DATA<42>       9B8<> 10C3<>
MEM_DATA<43>       9B8<> 10C3<>
MEM_DATA<44>       9B8<> 10C3<>
MEM_DATA<45>       9B8<> 10B3<>
MEM_DATA<46>       9B8<> 10B3<>
MEM_DATA<47>       9B8<> 10B3<>
MEM_DATA<48>       9B8<> 10C1<>
MEM_DATA<55..48>   37B5>
MEM_DATA<49>       9B8<> 10C1<>
MEM_DATA<50>       9B8<> 10C1<>
MEM_DATA<51>       9B8<> 10C1<>
MEM_DATA<52>       9B8<> 10C1<>
MEM_DATA<53>       9B8<> 10C1<>
MEM_DATA<54>       9B8<> 10C1<>
MEM_DATA<55>       9B8<> 10C1<>
MEM_DATA<56>       9B8<> 10C1<>
MEM_DATA<63..56>   37A5>
MEM_DATA<57>       9B8<> 10C1<>
MEM_DATA<58>       9B8<> 10C1<>
MEM_DATA<59>       9B8<> 10C1<>
MEM_DATA<60>       9B8<> 10C1<>
MEM_DATA<61>       9B8<> 10B1<>
MEM_DATA<62>       9B8<> 10B1<>
MEM_DATA<63>       9B8<> 10B1<>
MEM_DQM<0>         9C6<> 10C7<> 37C5>
MEM_DQM<1>         9C6<> 10B7<> 37C5>
MEM_DQM<2>         9C6<> 10C5<>
MEM_DQM<3..2>      37B5>
MEM_DQM<3>         9C6<> 10B5<>
MEM_DQM<4>         9C6<> 10C3<>
MEM_DQM<5..4>      37B5>
MEM_DQM<5>         9C6<> 10B3<>
MEM_DQM<6>         9C6<> 10C1<> 37B5>
MEM_DQM<7>         9C6<> 10B1<> 37A5>
MEM_DQS<0>         9C6<> 10C7<> 37C5>
MEM_DQS<1>         9C6<> 10B7<> 37C5>
MEM_DQS<2>         9C6<> 10C5<>
MEM_DQS<3..2>      37B5>
MEM_DQS<3>         9C6<> 10B5<>
MEM_DQS<4>         9C6<> 10C3<>
MEM_DQS<5..4>      37B5>
MEM_DQS<5>         9C6<> 10B3<>
MEM_DQS<6>         9C6<> 10C1<> 37B5>
MEM_DQS<7>         9C6<> 10B1<> 37A5>
MEM_MUXSEL_H<0>    9B6<> 10A6<
MEM_MUXSEL_H<1..0>  37A5>
MEM_MUXSEL_H<1>    9B6<> 10A4<
MEM_MUXSEL_L<0>    9B6<> 10A6<
MEM_MUXSEL_L<1..0>  37A5>
MEM_MUXSEL_L<1>    9B6<> 10A4<
MEM_RAS_L          9A5< 9C6<> 37A5>
MEM_WE_L           9A5< 9C6<> 37A5>
MLB_ALS_GAIN_SW    23C4<> 23C8<>
MLB_ALS_OP_COMP    23D7<
MLB_ALS_OP_IN      23D7<
MLB_ALS_OUT        23C4<> 23D6<
MLB_ALS_OUT_FB     23D7<>
MLB_PHOTODIODE     23D8<>
MMM_ACC_DETECT     24B8<> 24C2<>
MMM_ACC_PWRDOWN    24B8<> 24C1< 24C7<>
MMM_ACC_SELFTEST   24B8<> 24C2<> 24C7<> 40A4>
MMM_ACC_X_AXIS     24C5< 24C5> 24D2<> 40A4>
MMM_ACC_Y_AXIS     24C5< 24C5> 24D2<> 40A4>
MMM_ACC_Z_AXIS     24B5< 24C2<> 24C5> 40A4>
MMM_FFIRQ_L        14A6< 14B5<> 24C1<
MMM_PIC_AAC_PWRDOWN  24C3<>
MMM_PIC_AN2_PD     24D4<>
MMM_PIC_AN3_PU     24C4<>
MMM_PIC_FFIRQ_L    24C2<>
MMM_PIC_SIRQ_L     24C2<>
MMM_RESET_L        24C1< 24C3<>
MMM_SIRQ_L         14A6< 14B5<> 24C1<
MODEM_USB_DM       14C1< 26D2<> 38A2> 40B6>
MODEM_USB_DP       14C1< 26D2<> 38A2> 40B6>
MOD_BITCLK         14A2< 26B8< 26D2<> 40B1>
MOD_CLKOUT         14A2< 26D3<> 40A1>
MOD_DTO            14A2< 26D3<> 40A1>
MOD_SYNC           14A2< 26B8< 26D2<> 40A1>
MPIC_CPU_INT_L     5B2< 5B4< 14B5>
MSEN_PULL_UP_MASTER  20C6<>
MSEN_PULL_UP_SLAVE  20B5<>
NEC_AMC_TP         27A5<
NEC_AVDD           27D6> 39A3>
NEC_AVSS_F         27A5< 27B4<
NEC_CRUN_L         27A7<>
NEC_IDSEL          27B7<
NEC_IO_RESET_L     27B7< 27B7<
NEC_LEFT_USB_OVERCURRENT  25B2<> 27D1< 40D1>
NEC_LEFT_USB_PWREN  25B2<> 27B5<> 40D1>
NEC_LEGC           27A7<
NEC_MAIN_RESET_L   27A7< 27B7<
NEC_NANDTESTEN_TP  27A5<
NEC_NANDTESTOUT_TP  27A4<>
NEC_NC1_TP         27B5<>
NEC_NC2_TP         27B5<>
NEC_OCI<1>         27B5< 27D2<
NEC_OCI<2>         27B5< 27D2<
NEC_OCI<3>         27B5<
NEC_OCI<4>         27B5<
NEC_OCI<5>         27B5<
NEC_PCI_INTA_L     27A7< 27B7>
NEC_PCI_INTB_L     27A7< 27B7>
NEC_PCI_INTC_L     27A7< 27B7>
NEC_PCI_PERR_L     27B7<> 27C8<
NEC_PCI_SERR_L     27B7> 27C8<
NEC_PME_L          27A7> 27B7<
NEC_PPON3_TP       27B5>
NEC_PPON4_TP       27B5>
NEC_PPON5_TP       27B5>
NEC_RIGHT_USB_OVERCURRENT  27D1< 33B7<> 40C1>
NEC_RIGHT_USB_PWREN  27B5<> 33A7<> 40C1>
NEC_RREF           27B5<>
NEC_SMI_L_TP       27A7>
NEC_USB_DAM        27B4< 27C2<> 38B2>
NEC_USB_DAP        27A4< 27C2<> 38B2>
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NEC_USB_DBM        27A4< 27C2<> 38B2>
NEC_USB_DBP        27A4< 27C2<> 38B2>
NEC_USB_RSDM1      27C5<> 38B2>
NEC_USB_RSDM2      27C5<> 38B2>
NEC_USB_RSDP1      27C5<> 38B2>
NEC_USB_RSDP2      27C5<> 38B2>
NEC_XT1            27D5< 37B1>
NEC_XT2            27D5<> 37B1>
NEC_XT2_R          27D4<
NTEST1_TP          27B5<
NUMLOCK_LED_L      31D7<
OVER_18V_ADJ       32C3<>
PCI1510_VR_EN_L    17C7<
PCI_AD<0>          9C3< 12D6<> 17C7<> 25B5<> 27D7<>
                 40B6>
PCI_AD<31..0>      38C5>
PCI_AD<1>          9C3< 12D6<> 17C7<> 25B6<> 27D7<>
                 40A6>
PCI_AD<2>          9C3< 12D6<> 17C7<> 25C5<> 27D7<>
                 40A6>
PCI_AD<3>          9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                 40A6>
PCI_AD<4>          9C3< 12D6<> 17C7<> 25C5<> 27C7<>
                 40A6>
PCI_AD<5>          9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                 40A6>
PCI_AD<6>          9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                 40A6>
PCI_AD<7>          9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                 40D5>
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PCI_AD<14>         9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                 40C5>
PCI_AD<15>         9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                 40C5>
PCI_AD<16>         9C3< 12C6<> 17C7<> 25C5<> 27C7<>
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PCI_AD<18>         9C3< 12C6<> 17B7<> 25C5<> 25D4<
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PCI_AD<19>         9C3< 12C6<> 17B7<> 25C6<> 27C7<>
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PCI_AD<20>         9B3< 12C6<> 17B7<> 25C5<> 27C7<>
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PCI_AD<21>         12C6<> 17B7<> 25C6<> 27C7<> 40C5>
PCI_AD<22>         12C6<> 17B7<> 25C5<> 27C7<> 40B5>
PCI_AD<23>         12C6<> 17B7<> 25C6<> 27C7<> 40B5>
PCI_AD<24>         9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
                 40B5>
PCI_AD<25>         9C1<> 12C6<> 17B7<> 25D6<> 27C7<>
                 40B5>
PCI_AD<26>         9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
                 40B5>
PCI_AD<27>         9C1<> 12C6<> 17B7<> 25D6<> 27C8<>
                 40B5>
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                 40B5>
PCI_AD<31>         9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
                 40A5>
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PCI_CBE<3..0>      38C5>
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PCI_CBE<2>         12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<3>         12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_DEVSEL_L       12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                 38C5> 40A5>
PCI_FRAME_L        12B7< 12C7<> 17B7<> 25C5<> 27B7<>
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PCI_IRDY_L         12B7< 12C7<> 17B7<> 25C6<> 27B7<>
                 38C5> 40A5>
PCI_PAR            12C7<> 17B7<> 25C5<> 27B7<> 38C5>
                 40D4>
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                 38C5> 40A5>
PCI_TRDY_L         12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                 38C5> 40A5>
PLL_STOP_L         7C4<> 7C8<>
PMU_ACK_L          14C2< 31C4<>
PMU_AC_DET         31A5< 31B4<>
PMU_AC_IN          31B4<>
PMU_BATT0_DET_L    31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L     31A8<> 31B3< 31D2< 32A4<> 40C3>
PMU_BYTE           31B6< 31C7<
PMU_CAPSLOCK_LED_L  31C6<>
PMU_CHARGE_V       31C4<> 32B8<>
PMU_CHRG_BATT_0    31C4<> 32A8<>
PMU_CLK            14C2<> 31C4<>
PMU_CNVSS          31B6< 31C7<
PMU_CPU_HRESET_L   6A2< 6C3<> 23C4<> 31C4<>
PMU_CUSTOM_RESET   31A8<>
PMU_CUSTOM_RESET_L  31A7<> 31B8<
PMU_EPM            31D2< 31D4<>
PMU_FROM_INT       14C2<> 31C4<>
PMU_I2C_CLK        31B4<> 31C2<
PMU_I2C_DATA       31B4<> 31C2<
PMU_INT_L          14B5<> 14B7< 31B6<>
PMU_INT_NMI        14B5<> 14B7< 31D4<>
PMU_KB_RESET_L     40B2>
PMU_LID_CLOSED_L   23A8< 23C4<> 31B2< 31C4<>
PMU_NMI_BUTTON_L   26B3< 31C2< 31C4<>
PMU_NMI_L          31C2< 31C4<>
PMU_NUMLOCK_LED_L  31C6<>
PMU_OOPS           31B2< 31B4<>
PMU_PME_L          14B5<> 27B8< 31B2< 31C4<>
PMU_POWERUP_OK     31B4<> 31D2<
PMU_POWER_UP_L     30D8<> 31C6<> 31D7< 34B8<
PMU_REQ_L          14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  26B3< 31C4<> 31D2<
PMU_RESET_L        31B7<>
PMU_SELECT         31C6<>
PMU_SLEEP_LED      23C4<>
PMU_SLEEP_LED_L    23C2<> 31C4<>
PMU_SMB_CLK        31B4<> 31C2< 32A3<
PMU_SMB_DATA       31B4<> 31C2< 32A2<
PMU_TO_INT         14C2<> 31C4<>
POWER_UP           30D8<>
POWER_VALID        31B2< 31C4<>
PP3V3_MMM          24C8< 24D6<
PP3V3_MMM_PIC      24C1< 24D5<
PP3V3_SI_AVCC1     20D7< 39B3>
PP3V3_SI_AVCC2     20C5< 39B3>
PP3V3_SI_PVCC1     20C7< 39B3>
PP3V3_SI_PVCC2     20C5< 39B3>
PP3V3_SI_VCC1      20D7< 39B3>
PP3V3_SI_VCC2      20C5< 39B3>
PWR_BUTTON_L       23A7<> 26C1< 40B2>
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RAM_ADDR<12..0>    37A5>
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RAM_ADDR<2>        9B4< 11B5<> 11B6<>
RAM_ADDR<3>        9B4< 11B3<> 11B8<>
RAM_ADDR<4>        9B4< 11B5<> 11B6<>
RAM_ADDR<5>        9B4< 11B3<> 11B8<>
RAM_ADDR<6>        9B4< 11B5<> 11B6<>
RAM_ADDR<7>        9B4< 11B3<> 11B8<>
RAM_ADDR<8>        9B4< 11B5<> 11B6<>
RAM_ADDR<9>        9A4< 11B3<> 11B8<>
RAM_ADDR<10>       9A4< 11B3<> 11B8<>
RAM_ADDR<11>       9A4< 11B5<> 11B6<>
RAM_ADDR<12>       9A4< 11B3<> 11B8<>
RAM_BA<0>          9A4< 11B3<> 11B8<>
RAM_BA<1..0>       37A5>
RAM_BA<1>          9A4< 11B5<> 11B6<>
RAM_CAS_L          9A4< 11B5<> 11B6<> 37A5>
RAM_CKE<0>         9A3< 9C4< 11B6<>
RAM_CKE<3..0>      37A5>
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RAM_CKE<2>         9A3< 9C4< 11C5<>
RAM_CKE<3>         9A3< 9C4< 11C3<>
RAM_CS_L<0>        9C4< 11B8<>
RAM_CS_L<3..0>     37A5>
RAM_CS_L<1>        9C4< 11B6<>
RAM_CS_L<2>        9C4< 11B3<>
RAM_CS_L<3>        9C4< 11B5<>
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RAM_DATA_A<7..0>   37C5>
RAM_DATA_A<1>      10C8<> 11D8<>
RAM_DATA_A<2>      10C8<> 11D8<>
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RAM_DATA_A<10>     10C7<> 11D8<>
RAM_DATA_A<11>     10C7<> 11D8<>
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RAM_DATA_A<15>     10C7<> 11D6<>
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RAM_DATA_A<22>     10B6<> 11C6<>
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RAM_DATA_A<29>     10C5<> 11C6<>
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RAM_DATA_A<31>     10C5<> 11C6<>
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RAM_DATA_A<47..32>  37B5>
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RAM_DATA_A<34>     10C4<> 11B8<>
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RAM_DATA_A<37>     10B4<> 11B6<>
RAM_DATA_A<38>     10B4<> 11B6<>
RAM_DATA_A<39>     10B4<> 11B6<>
RAM_DATA_A<40>     10B4<> 11B8<>
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RAM_DATA_B<8>      10C8<> 11D3<>
RAM_DATA_B<15..8>  37C5>
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RAM_DATA_B<10>     10C8<> 11D3<>
RAM_DATA_B<11>     10C8<> 11D3<>
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RAM_DATA_B<15>     10C8<> 11D5<>
RAM_DATA_B<16>     10C6<> 11D3<>
RAM_DATA_B<31..16>  37B5>
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RAM_DATA_B<18>     10C6<> 11C3<>
RAM_DATA_B<19>     10C6<> 11C3<>
RAM_DATA_B<20>     10C6<> 11D5<>
RAM_DATA_B<21>     10C6<> 11C5<>
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RAM_DATA_B<27>     10C6<> 11C3<>
RAM_DATA_B<28>     10C6<> 11C5<>
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RAM_DATA_B<30>     10C6<> 11C5<>
RAM_DATA_B<31>     10C6<> 11C5<>
RAM_DATA_B<32>     10D4<> 11B3<>
RAM_DATA_B<47..32>  37B5>
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RAM_DATA_B<35>     10C4<> 11B3<>
RAM_DATA_B<36>     10C4<> 11B5<>
RAM_DATA_B<37>     10C4<> 11B5<>
RAM_DATA_B<38>     10C4<> 11B5<>
RAM_DATA_B<39>     10C4<> 11B5<>
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RAM_DATA_B<41>     10C4<> 11B3<>
RAM_DATA_B<42>     10C4<> 11A3<>
RAM_DATA_B<43>     10C4<> 11A3<>
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RAM_DQM_A<2>       10B6<> 11C6<>
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RAM_DQM_A<7>       10C1<> 11A6<> 37A5>
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RAM_DQM_B<4>       10C4<> 11B5<>
RAM_DQM_B<5..4>    37B5>
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RAM_DQM_B<7>       10C2<> 11A5<> 37A5>
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RAM_DQS_A<1>       10C7<> 11D8<> 37C5>
RAM_DQS_A<2>       10B6<> 11C8<>
RAM_DQS_A<3..2>    37B5>
RAM_DQS_A<3>       10C5<> 11C8<>
RAM_DQS_A<4>       10B4<> 11B8<>
RAM_DQS_A<5..4>    37B5>
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RAM_DQS_A<6>       10B2<> 11A8<> 37B5>
RAM_DQS_A<7>       10C1<> 11A8<> 37A5>
RAM_DQS_B<0>       10C8<> 11D3<> 37C5>
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RAM_DQS_B<2>       10C6<> 11C3<>
RAM_DQS_B<3..2>    37B5>
RAM_DQS_B<3>       10C6<> 11C3<>
RAM_DQS_B<4>       10C4<> 11B3<>
RAM_DQS_B<5..4>    37B5>
RAM_DQS_B<5>       10C4<> 11B3<>
RAM_DQS_B<6>       10C2<> 11A3<> 37B5>
RAM_DQS_B<7>       10C2<> 11A3<> 37A5>
RAM_MUXSEL_H       10A3< 10A5< 10B1<> 10B3<> 37A5>
RAM_MUXSEL_L       10A3< 10A5< 10B5<> 10B7<> 37A5>
RAM_RAS_L          9A4< 11B5<> 11B6<> 37A5>
RAM_WE_L           9A4< 11B3<> 11B8<> 37A5>
RESET_VREF         6C3<>
RF_DISABLE_L_SPN   25D6<> 40C1>
RIGHT_USB_DM       27A3< 33A7<> 38A2> 40D1>
RIGHT_USB_DP       27A3< 33A7<> 38A2> 40D1>
RJ45_C0_PD         28B2<>
RJ45_C1_PD         28B2<>
RJ45_C2_PD         28B2<>
RJ45_C3_PD         28B2<>
RJ45_DN<0>         28B2<> 38D2> 40B3>
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RJ45_DP<2>         28B2<> 38D2> 40A3>
RJ45_DP<3>         28B2<> 38D2> 40A3>
ROM_CS_L           9B3< 12A5< 25B6<> 40B1>
ROM_OE_L           9B3< 12A5< 25C5<> 40B1>
ROM_ONBOARD_CS_L   9B3< 25C6<> 40B1>
ROM_RW_L           9B3< 12A5< 25C6<> 40B1>
ROM_WP_L           9B3<
RSDM3_TP           27C5>
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RSDM5_TP           27C5>
RSDP3_TP           27C5>
RSDP4_TP           27C5>
RSDP5_TP           27C5>
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SI_I2C_DATA        19C5<> 20B5<> 20C7<>
SI_MASTER          20B8<
SI_M_HTPLG         20B7<
SI_RESET_L         19C8< 20B5< 20C3< 20C7<
SI_SECONDARY       20A7<
SI_S_HTPLG         20A5<
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SI_TMDS_DN<2>      20A5< 20B7<
SI_TMDS_DN<3>      20A5< 20A5<
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SI_TMDS_DP<4>      20A5< 20A5<
SI_TMDS_DP<5>      20A5< 20A5<
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SLAVE_SWING        20A5<
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                 34B3< 34B8<> 36B3< 36D2< 40A1>
SLEEP_ANODE        23C1< 26C5<>
SLEEP_LED          40B6>
SLEEP_LED_I        23D1<
SLEEP_LED_L        23D2<
SLEEP_LED_SW_L     23C2<>
SLEEP_LED_UF       23C1<
SLEEP_LS5          34A5<> 34A8<
SLEEP_LS5_EN_L     34A5<>
SLEEP_L_LS5        19A7<> 28A8<> 34A5<> 35C8<> 36C8<
SLEEP_L_LS5_EN_L   34A6<>
SLEEP_L_LS5_INV    36A3< 36C2< 36C8<>
SLEEP_L_LS5_NET    34B3<> 36C8<>
SLEEP_NET          34A3<>
SLEEP_NET_INV      34A3<>
SMC_TP             27B5<
SND_AGND           26C6<> 39B6>
SND_AMP_MUTE       26D4<> 26D4< 40A4>
SND_AMP_MUTE_INV   26C8< 26D5<
SND_AMP_MUTE_L     14C5<> 26D3<>
SND_CLKOUT         14B1< 26D8< 37B1> 40D6>
SND_HP_MUTE        26C4<>
SND_HP_MUTE_INV    40A4>
SND_HP_MUTE_L      14C5<> 26C4<>
SND_HP_SENSE_L     40C6>
SND_HW_RESET_L     14A7< 14B5<> 26C8< 40C6>
SND_LIN_SENSE_L    40C6>
SND_SCLK           14B1< 26C8< 37B1> 40C6>
SND_SYNC           14B1< 26D8< 40D6>
SND_TO_AUDIO       14B1< 26C8< 40D6>
SOFT_PWR_ON_L      22D1< 23A8< 31A8<> 31C6<> 31D7<
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SRCLK_TP           27A5> 40A4>
SRMOD_TP           27A5> 40A4>
ST7_ICP_SEL_PD     23A2< 23D6<
ST7_KBD_LED_OUT    23B8<> 23C4<>
ST7_OSC1           23D5<
ST7_OSC2           23D5<>
ST7_PB6_PD         23B2< 23C4<>
ST7_RESET_L        23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H    23C2<> 23C4<>
ST7_XTAL_IN        23C5<
STOP_AGP_L         12D2< 12D4<>
SUPPLY_M_DM        26A8< 26B6<
SUPPLY_M_DP        26B6< 26B8<
SUTRO_ALS_GAIN_SW  23C4<> 25B2<> 40C2>
SUTRO_ALS_OUT      23C4<> 25B2<> 40C2>
SYSCLK_CPU         5C4< 8A6< 37D1>
SYSCLK_CPU_UF      8A6<> 37D1>
SYSCLK_DDRCLK_A0   9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1   9D4< 11A6<> 37D1>
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SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B0   9D4< 11D3<> 37D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
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SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 37D1>
SYSCLK_LA_TP       8A6<>
SYSTEM_CLK_EN      14A5< 14A7< 31C4<>
SYS_BATT_ISNS      24A2< 31B3<
SYS_BATT_ISNS2     31B4<>
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TEST_TP            27A5< 40A4>
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THERM1_M_DP        38A2>
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THERM2_A_DP        26A6< 26A7< 38A2>
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THERM2_M_DP        38A2>
THERM_INV          26A5<>
THERM_L_OC         23A8< 26A4<> 31B4<>
THERM_L_OC_CONN    23A7<>
TMDS_CLKN          20B3< 20B4< 20D2< 22B7<> 38B2>
TMDS_CLKP          20B4< 20B4< 20D2< 22C7<> 38B2>
TMDS_CLK_CMF       20B3<
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TMDS_CONN_CLKP     22C6<> 22C7<> 38B2> 40D7>
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TMDS_D5_CMF        20B1<
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TMDS_DN<3>         20A4< 20C1< 20D2<>
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TPAD_F_TXD         40C4>
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TPAD_TXD           31B2< 31C4<>
TPS2211_SHDN_L_PU  17C4<
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TP_MMM_ICSP_PGD    24C3<>
TP_MMM_ICSP_PGM    24C3<>
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TV_COMP            22A6<> 40D6>
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TV_GND2            22A6<> 39B6> 40A7>
TV_Y               22A6<> 40D6>
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UIDE_DIOW_L        13C7<> 25A4< 38C5>
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UIDE_INTRQ         13C7< 38C5>
UIDE_IOCHRDY       13C7< 25A4< 38C5>
UIDE_REF           13C7<> 39D3>
UIDE_RST_L         13C7<> 25A4< 38C5>
USB2_PCI_GNT_L     12C7<> 27B7<
USB2_PCI_INT_L     14B5<> 14C7< 27A8<
USB2_PCI_REQ_L     12A7< 12D7<> 27B7>
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USB_D1P            14D1< 27A4< 27A5>
USB_D2M            27A5>
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USB_DCP            14B2<> 14D2< 27A5>
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USB_DDP            14B2<> 14C2<
USB_DEM            14B2<> 14C2< 38B2>
USB_DEP            14B2<> 14C2< 38B2>
USB_DFM            14B2<> 14B2< 38B2>
USB_DFP            14B2<> 14B2< 38B2>
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USB_OC_CD_L        14B2< 14C7<
USB_OC_EF_L        14B2< 14D7<
USB_PWREN_AB_L     14B2<> 14C7<
USB_PWREN_CD_L     14B2<> 14C7<
USB_PWREN_EF_L     14B2<> 14D7<
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USB_TPAD_P         14B1< 23A7<>
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VCORE_BST          35C5<> 39C1>
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VCORE_CNTL_RC      19A3<>
VCORE_DH           35B5<> 39C1>
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VCORE_GND          35B5<> 39B1>
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VCORE_GNDDIV       35A4< 35B5< 39B1>
VCORE_GNDDIV_TEST  35A3<>
VCORE_GNDSNS       35A2<> 35A4< 39B1>
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VCORE_TON          35B6< 39C1>
VCORE_VCC          35C6< 39C1>
VCORE_VGATE        14B6< 14B7< 35B4> 39B1>
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VGA_G              22C5<> 22D7< 40D7>
VGA_HSYNC          22C6<> 22C7< 40D7>
VGA_HSYNC_BUF      22C8<>
VGA_R              22C5<> 22D7< 40D7>
VGA_VSYNC          22C5<> 22C7< 40D7>
VGA_VSYNC_BUF      22C8<>
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APPLE COMPUTER INC.

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SCALE NONE | SHT 43 OF ?

*** Part Cross-Reference for the entire design ***

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U4	SN74AUC1G08 6
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U6	FAN2558 5
U7	VREG_LT1962 14
U8	MAX8860 21
U9	CBTV4020 10
U10	CBTV4020 10
U11	PI3B3257 35
U12	CBTV4020 10
U13	CBTV4020 10
U14	LTC3405 28
U15	COMPARATOR_LMC7211 32
U16	LTC1778 19
U17	FEPR_1MX8 9
U18	LTC1625 33

U19	PWR_CNTRL_TPS2211 17
U20	MAX1717 35
U21	COMPARATOR_LMC7211 33
U22	MAX1715 36
U23	AMP_MAX4172 32
U24	7432 22
U25	VREG_LP2951 33
U26	PCI1510GGU 17
U27	COMPARATOR_LMC7211 31
U28	LTC3707 34
U29	TSB81BA3A 29
U30	VREG_LP2951 33
U31	MAX1772 32
U32	EEPROM_32KX8_M24256B 6
U33	M16C62 31
U34	VREG_LM2594 29
U35	SIL178 20
U36	LTC1761 29
U37	VREG_LT1962 29
U38	COMPARATOR_LMC7211 32
U39	UPD720101_FBGA 27
U40	OPAMP_MAX4236EUTT 23
U41	MAX6804 31
U42	CLK_GEN_CY28512 14
U43	APOLLO_MPC7447A_360 5 6
U44	RAGE_MBLTY_M11_CSP64_667 18 19 21
U45	INTREPID 8 9 12 13 14 15
U46	COMPARATOR_LMC7211 22
U47	CLK_GEN_CY25811 18
U48	SIL178 20
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U50	OPAMP_LMC7111 32
U51	INA138 24
U52	FEPR_256KX8_ST72264_BGA 23
U53	PIC16F818_QFN 24
U54	VREG_MM1571J 21
U55	VREG_MM1571J 21
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U57	741G32 22
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U59	MM3120 23
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Y5	CRYSTAL 27
Y6	CRYSTAL 31
Y7	CRYSTAL_4PIN 31
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