

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
01		308060	ENGINEERING RELEASED	12/19/03	?

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15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL1162 TMDS TRANSMITTER
21	M10 ANALOG, POWER, GND

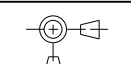
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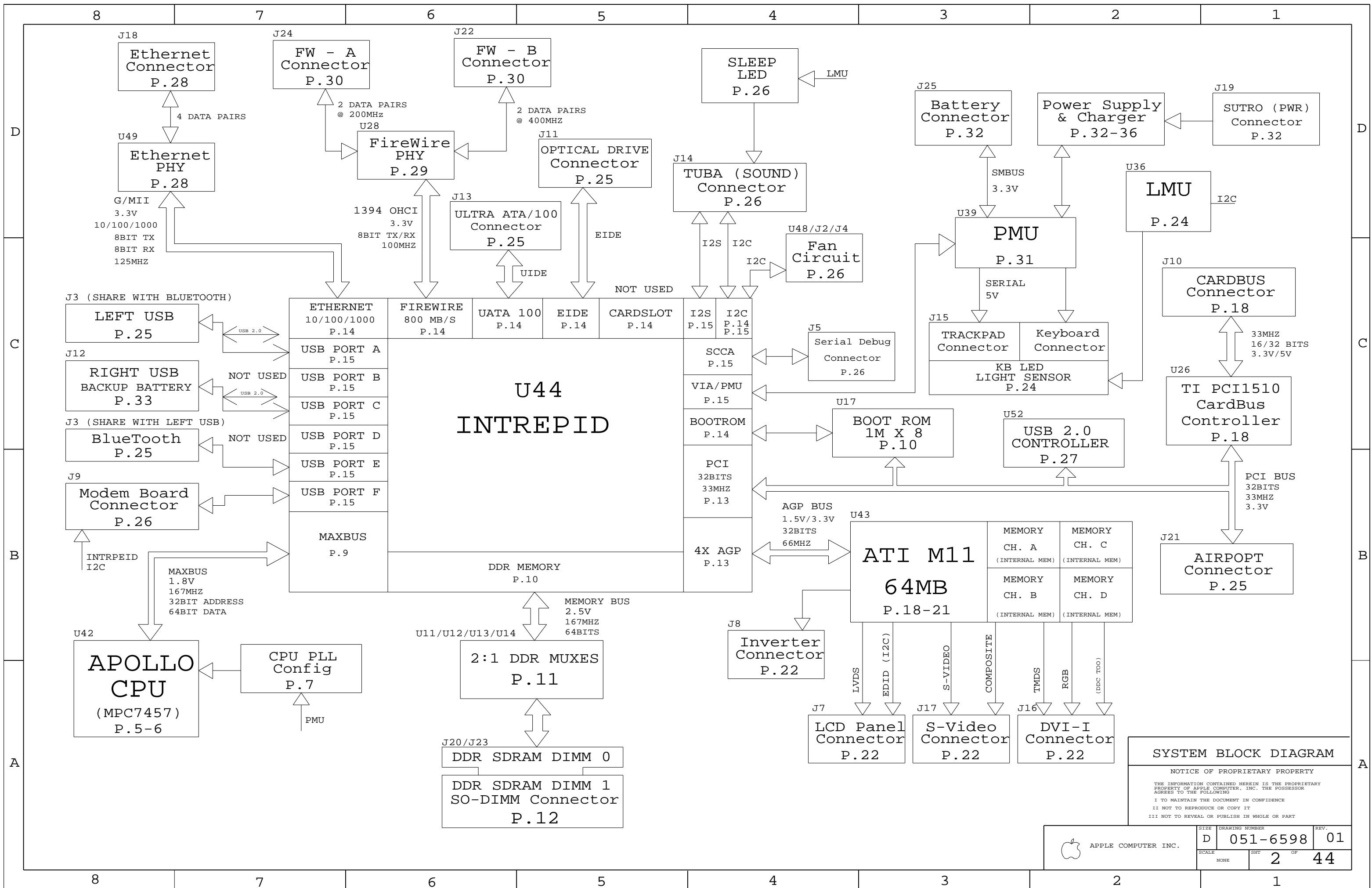
SINCLAIR Q41A

12/18/2003

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS		✓
INT_TMDS	✓	
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6598	1	SCHEM,MLB,Q41A	SCH1	
820-1615	1	PCBF,MLB,Q41A	PCB1	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
xx : _____	_____	DRAPTR	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
x.xx : _____	_____	ENG APPD	MFG APPD		
x.xxx : _____	_____	QA APPD	DESIGNER		
ANGLES : _____	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-6598
				REV. 01	SHT 1 OF 44

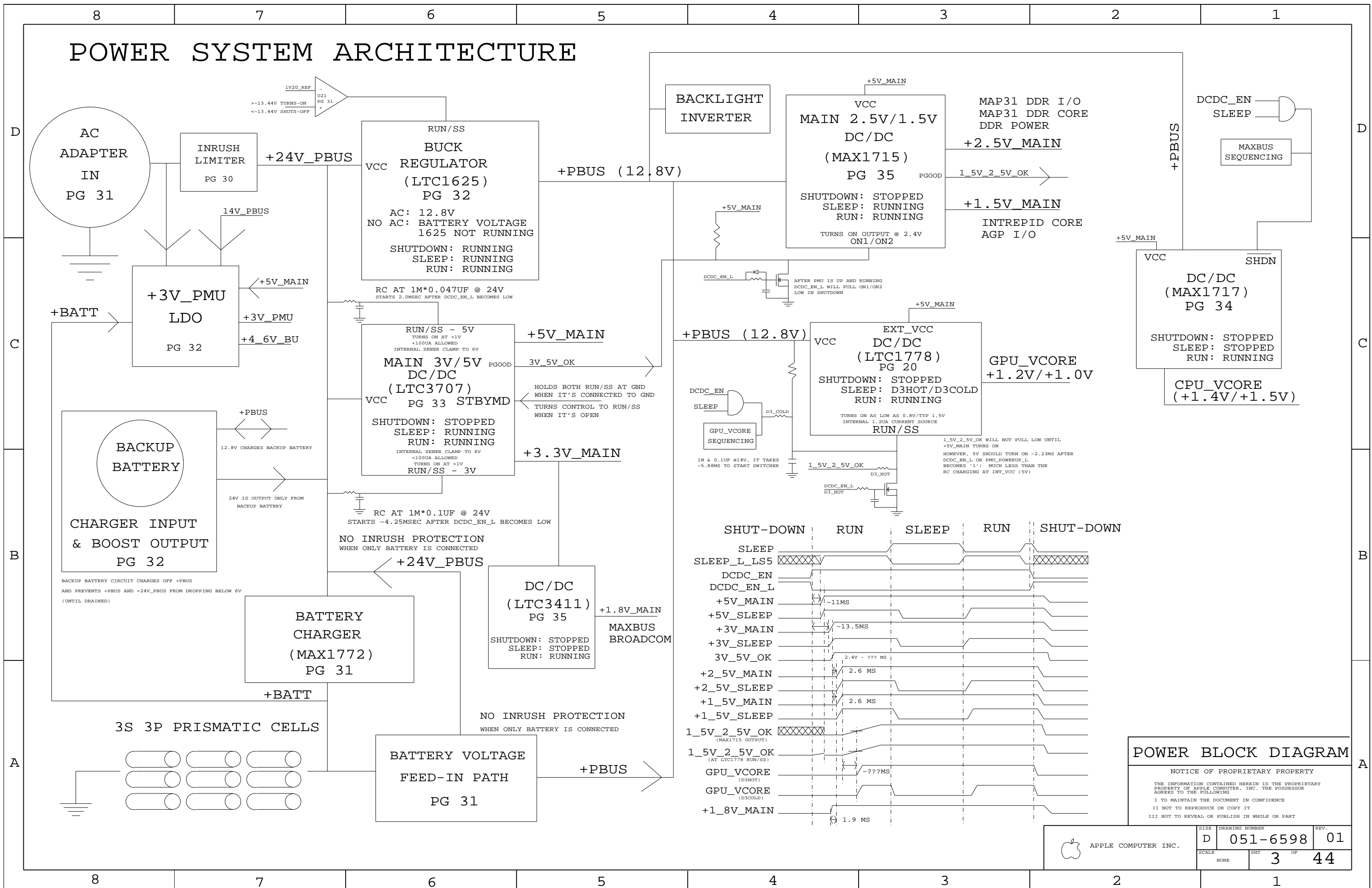


SYSTEM BLOCK DIAGRAM

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	NONE	D 051-6598	01
SCALE		SHT	OF
NONE		2	44

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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	D	051-6598	01
SCALE	NONE	SHT	3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

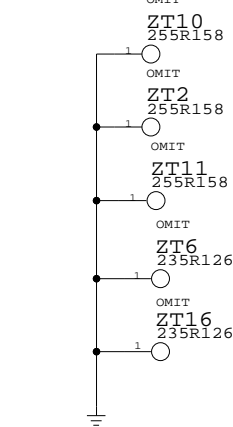
BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

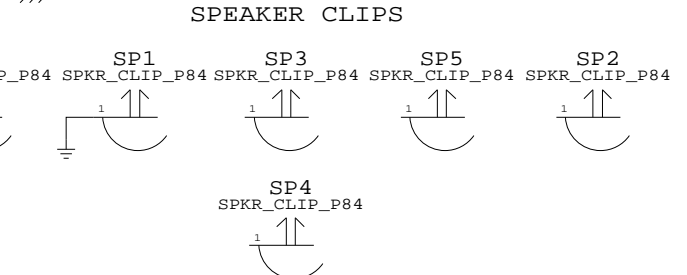
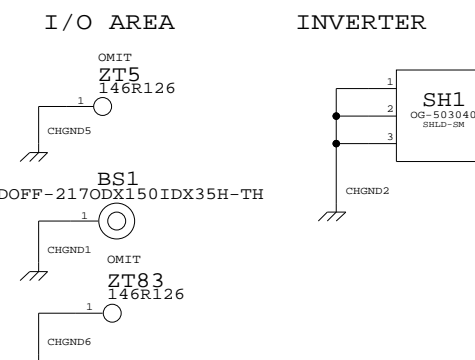
1	SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL) GROUND (1/2 OZ)
3	LAMINATE (4MIL) SIGNAL (1/2 OZ)
4	PREPREG (3MIL) SIGNAL (1/2 OZ)
5	LAMINATE (4MIL) GROUND (1/2 OZ)
6	PREPREG (2MIL) CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL) CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL) GROUND (1/2 OZ)
9	LAMINATE (4MIL) SIGNAL (1/2 OZ)
10	PREPREG (3MIL) SIGNAL (1/2 OZ)
11	LAMINATE (4MIL) GROUND (1/2 OZ)
12	PREPREG (3MIL) SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

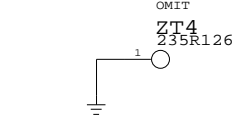
ASICS HEATSINK MOUNTS



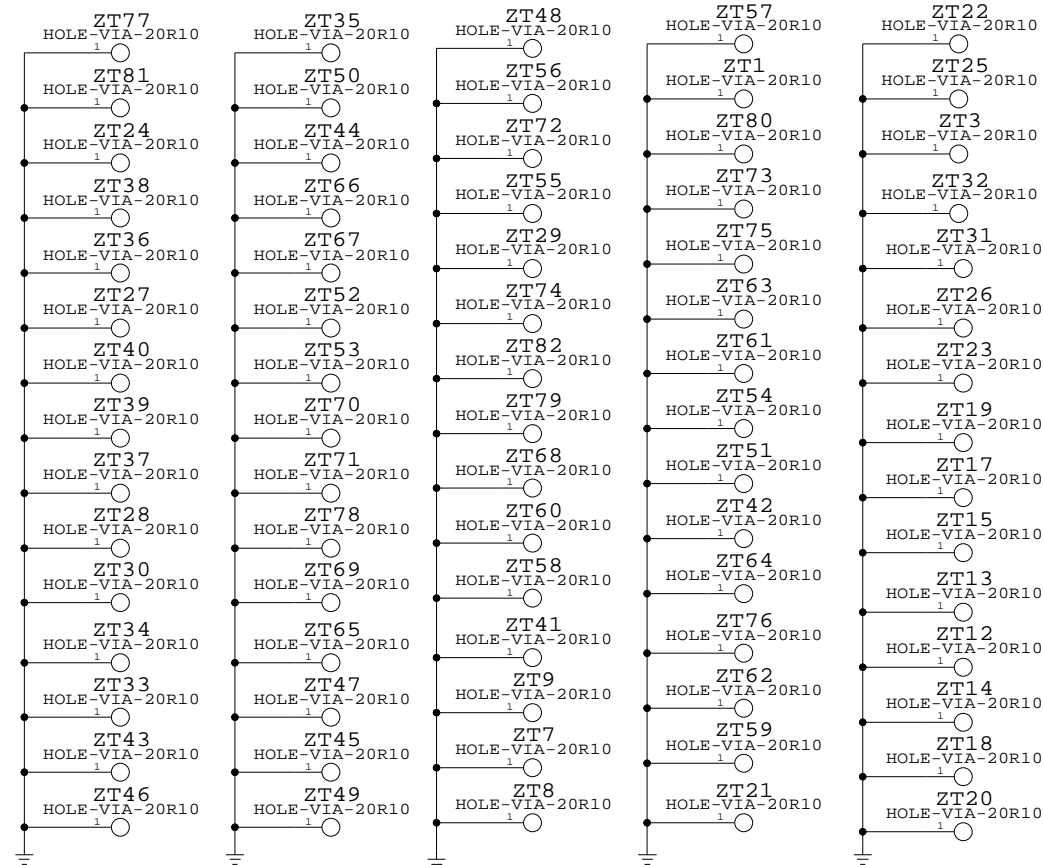
CHASSIS MOUNTS



CONDUCTIVE MOUNTS



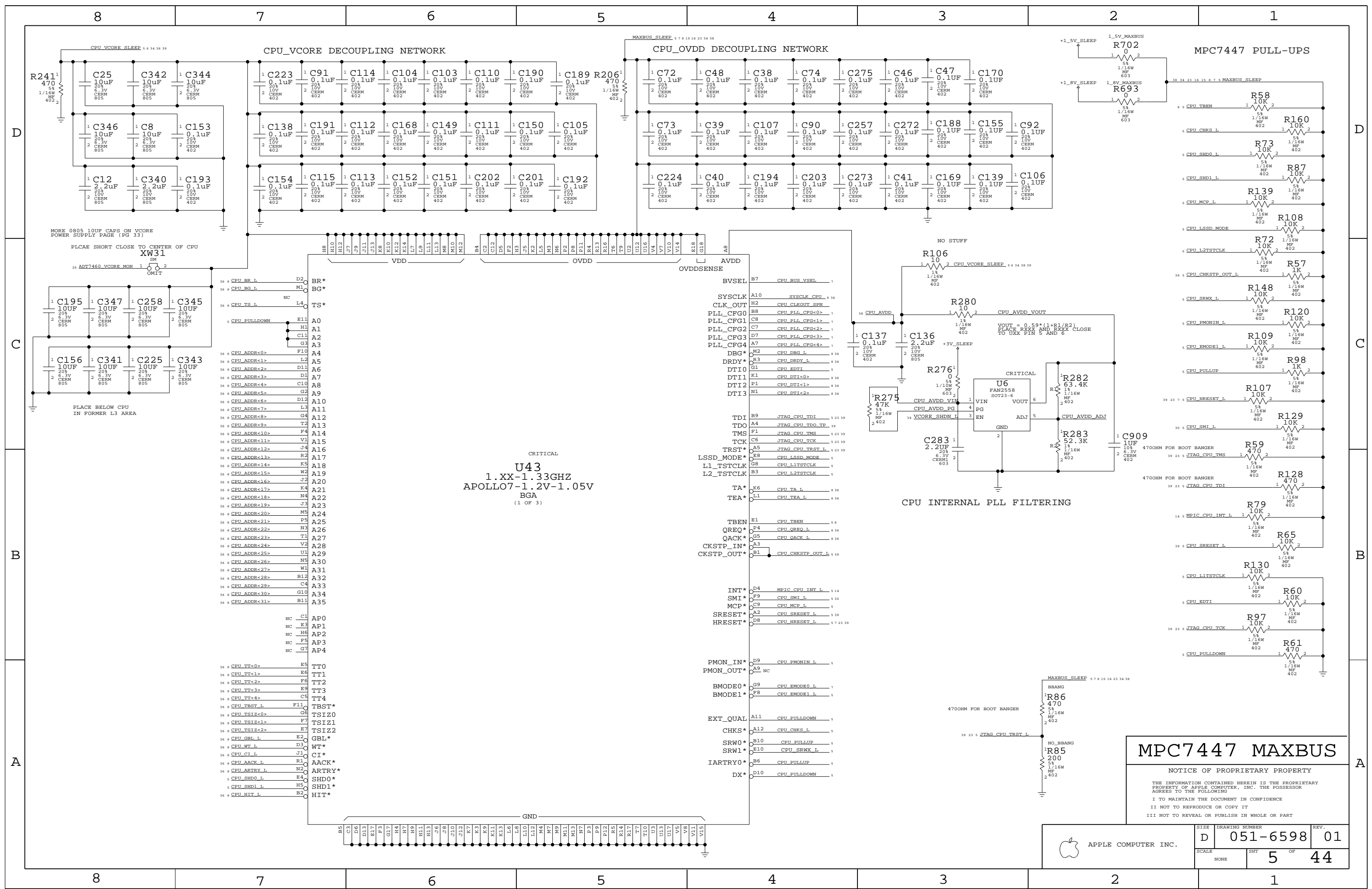
GROUND VIAS



BOARD INFORMATION

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SCALE	NONE	SHT	4 OF 44



MPC7447 MAXBUS

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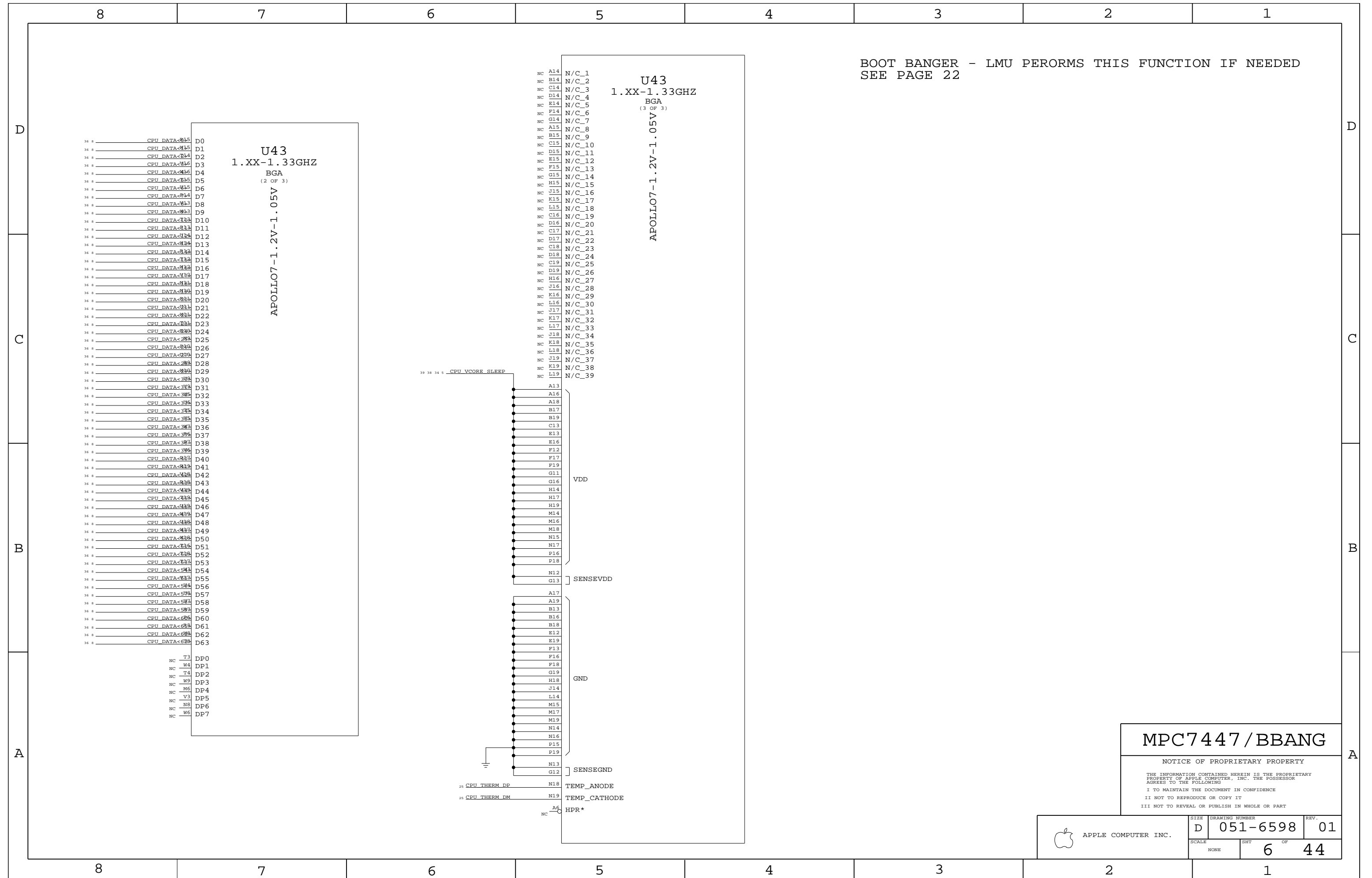
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6598	REV.: 01
	SCALE: NONE	SHEET: 5	OF: 44

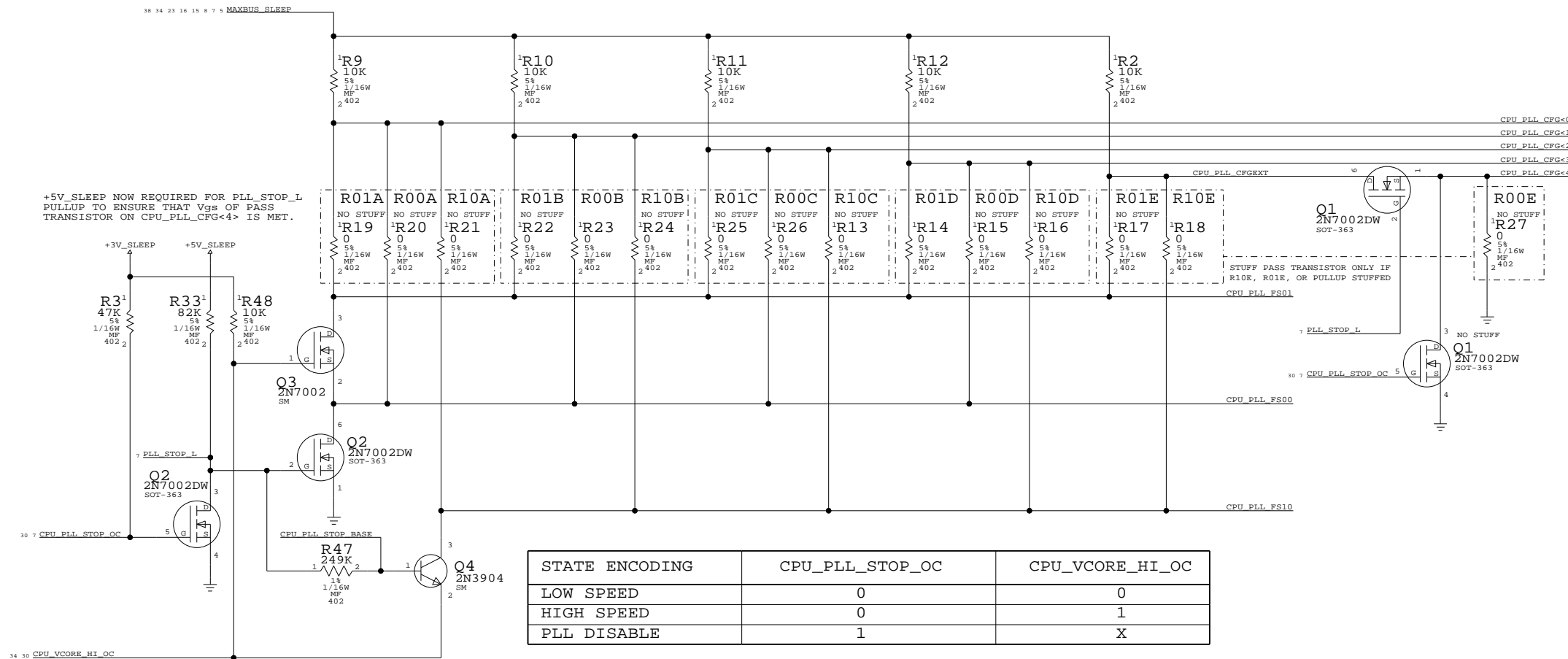


MPC7447/BBang

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6598	REV. 01
	SCALE NONE	SHT 6	OF 44

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

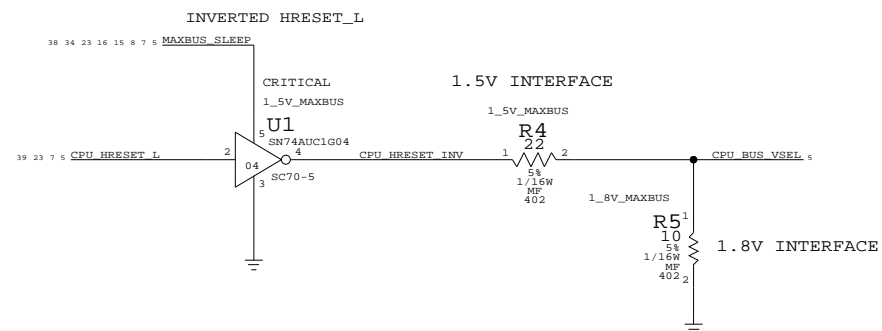
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG E ABCD HEX
	167MHZ	133MHZ	
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

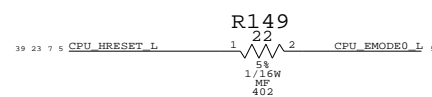
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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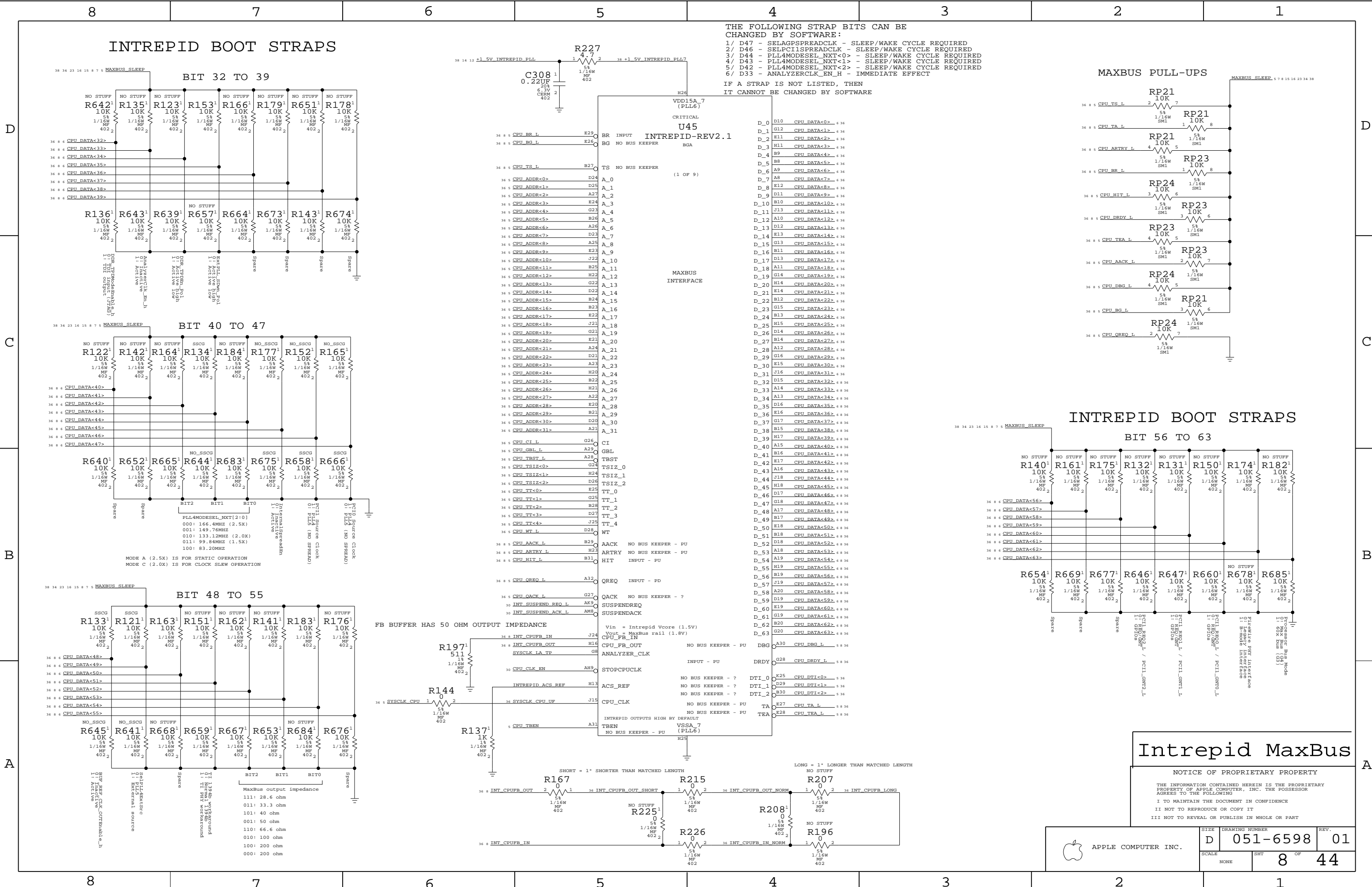
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	NONE	SHT	7 OF 44

INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

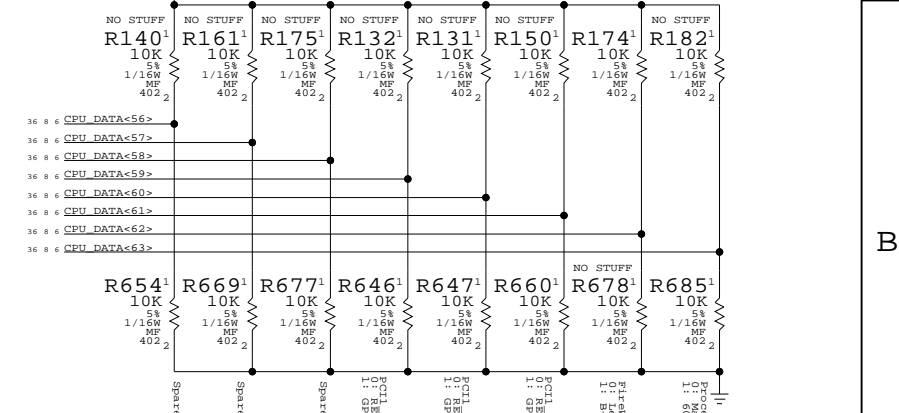
- 1/ D47 - SELAGPSREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D46 - SELPCILSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE



INTREPID BOOT STRAPS

BIT 56 TO 63



Intrepid MaxBus

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	SHT	OF	
NONE	8	44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

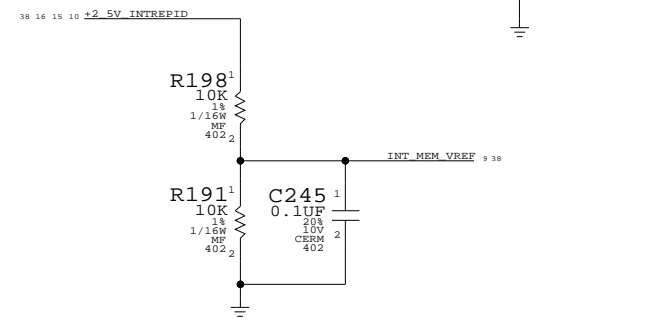
PINS ARE SWAPABLE FOR RPAKS

MEM_DATA<0>	AK32	DDR_DATA_0	DDR_A_0	H35	MEM_ADDR<0>
MEM_DATA<1>	AK33	DDR_DATA_1	DDR_A_1	G35	MEM_ADDR<1>
MEM_DATA<2>	AK31	DDR_DATA_2	DDR_A_2	G36	MEM_ADDR<2>
MEM_DATA<3>	AK35	DDR_DATA_3	DDR_A_3	F35	MEM_ADDR<3>
MEM_DATA<4>	AK36	DDR_DATA_4	DDR_A_4	F35	MEM_ADDR<4>
MEM_DATA<5>	AJ32	DDR_DATA_5	DDR_A_5	E35	MEM_ADDR<5>
MEM_DATA<6>	AJ35	DDR_DATA_6	DDR_A_6	E36	MEM_ADDR<6>
MEM_DATA<7>	AJ36	DDR_DATA_7	DDR_A_7	G32	MEM_ADDR<7>
MEM_DATA<8>	AG33	DDR_DATA_8	DDR_A_8	D36	MEM_ADDR<8>
MEM_DATA<9>	AG35	DDR_DATA_9	DDR_A_9	H36	MEM_ADDR<9>
MEM_DATA<10>	AH35	DDR_DATA_10	DDR_A_10	G33	MEM_ADDR<10>
MEM_DATA<11>	AG36	DDR_DATA_11	DDR_A_11	H33	MEM_ADDR<11>
MEM_DATA<12>	AH36	DDR_DATA_12	DDR_A_12	D35	MEM_ADDR<12>
MEM_DATA<13>	AH32	DDR_DATA_13	DDR_BA_0	L30	MEM_BA<0>
MEM_DATA<14>	AG32	DDR_DATA_14	DDR_BA_1	M29	MEM_BA<1>
MEM_DATA<15>	AG31	DDR_DATA_15	DDRC_S_0	AN34	MEM_CS_L<0>
MEM_DATA<16>	AE32	DDR_DATA_16	DDRC_S_1	AN36	MEM_CS_L<1>
MEM_DATA<17>	AF35	DDR_DATA_17	DDRC_S_2	AL35	MEM_CS_L<2>
MEM_DATA<18>	AF36	DDR_DATA_18	DDRC_S_3	AL33	MEM_CS_L<3>
MEM_DATA<19>	AE36	DDR_DATA_19	DDR_DQS_0	AJ31	MEM_DQS<0>
MEM_DATA<20>	AE35	DDR_DATA_20	DDR_DQS_1	AH31	MEM_DQS<1>
MEM_DATA<21>	AE33	DDR_DATA_21	DDR_DQS_2	AD32	MEM_DQS<2>
MEM_DATA<22>	AD36	DDR_DATA_22	DDR_DQS_3	AB30	MEM_DQS<3>
MEM_DATA<23>	AD35	DDR_DATA_23	DDR_DQS_4	V30	MEM_DQS<4>
MEM_DATA<24>	AA36	DDR_DATA_24	DDR_DQS_5	F32	MEM_DQS<5>
MEM_DATA<25>	AA35	DDR_DATA_25	DDR_DQS_6	M29	MEM_DQS<6>
MEM_DATA<26>	AA33	DDR_DATA_26	DDR_DQS_7	L32	MEM_DQS<7>
MEM_DATA<27>	AB36	DDR_DATA_27	DDR_DM_0	AJ33	MEM_DQM<0>
MEM_DATA<28>	AB35	DDR_DATA_28	DDR_DM_1	AH33	MEM_DQM<1>
MEM_DATA<29>	AC36	DDR_DATA_29	DDR_DM_2	AD33	MEM_DQM<2>
MEM_DATA<30>	AA32	DDR_DATA_30	DDR_DM_3	AC35	MEM_DQM<3>
MEM_DATA<31>	AB33	DDR_DATA_31	DDR_DM_4	F35	MEM_DQM<4>
MEM_DATA<32>	V36	DDR_DATA_32	DDR_DM_5	F33	MEM_DQM<5>
MEM_DATA<33>	U33	DDR_DATA_33	DDR_DM_6	G32	MEM_DQM<6>
MEM_DATA<34>	U32	DDR_DATA_34	DDR_DM_7	L33	MEM_DQM<7>
MEM_DATA<35>	V35	DDR_DATA_35	DDRRAS	L29	MEM_RAS_L
MEM_DATA<36>	T30	DDR_DATA_36	DDRCAS	H32	MEM_CAS_L
MEM_DATA<37>	U36	DDR_DATA_37	DDRWE	K30	MEM_WE_L
MEM_DATA<38>	U35	DDR_DATA_38	DDRCKE0	AN35	MEM_CKE<0>
MEM_DATA<39>	T36	DDR_DATA_39	DDRCKE1	AM35	MEM_CKE<1>
MEM_DATA<40>	F33	DDR_DATA_40	DDRCKE2	AM36	MEM_CKE<2>
MEM_DATA<41>	R30	DDR_DATA_41	DDRCKE3	AL36	MEM_CKE<3>
MEM_DATA<42>	F35	DDR_DATA_42	DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>
MEM_DATA<43>	F36	DDR_DATA_43	DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>
MEM_DATA<44>	R36	DDR_DATA_44	DDR_SELLO_0	N30	MEM_MUXSEL_L<0>
MEM_DATA<45>	R35	DDR_DATA_45	DDR_SELLO_1	T32	MEM_MUXSEL_L<1>
MEM_DATA<46>	R33	DDR_DATA_46	DDR_MCLK_0_P	Y32	SYSLCK_DDRCLK_A0_UF
MEM_DATA<47>	R32	DDR_DATA_47	DDR_MCLK_0_N	Y33	SYSLCK_DDRCLK_A0_L_UF
MEM_DATA<48>	N35	DDR_DATA_48	DDR_MCLK_1_P	Y35	SYSLCK_DDRCLK_A1_UF
MEM_DATA<49>	M36	DDR_DATA_49	DDR_MCLK_1_N	Y36	SYSLCK_DDRCLK_A1_L_UF
MEM_DATA<50>	L35	DDR_DATA_50	DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP
MEM_DATA<51>	M35	DDR_DATA_51	DDR_MCLK_2_N	Y30	INT_DDRCLK2_N_TP
MEM_DATA<52>	M33	DDR_DATA_52	DDR_MCLK_3_P	W32	SYSLCK_DDRCLK_B0_UF
MEM_DATA<53>	L36	DDR_DATA_53	DDR_MCLK_3_N	W33	SYSLCK_DDRCLK_B0_L_UF
MEM_DATA<54>	N33	DDR_DATA_54	DDR_MCLK_4_P	Y32	SYSLCK_DDRCLK_B1_UF
MEM_DATA<55>	M30	DDR_DATA_55	DDR_MCLK_4_N	Y32	SYSLCK_DDRCLK_B1_L_UF
MEM_DATA<56>	J32	DDR_DATA_56	DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP
MEM_DATA<57>	J33	DDR_DATA_57	DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP
MEM_DATA<58>	J35	DDR_DATA_58	DDR_REF	AA22	INT_MEM_REF_H
MEM_DATA<59>	K32	DDR_DATA_59	DDR_VREF_0	Y22	INT_MEM_VREF
MEM_DATA<60>	K33	DDR_DATA_60	DDR_VREF_1	T22	
MEM_DATA<61>	J36	DDR_DATA_61			
MEM_DATA<62>	K36	DDR_DATA_62			
MEM_DATA<63>	K35	DDR_DATA_63			

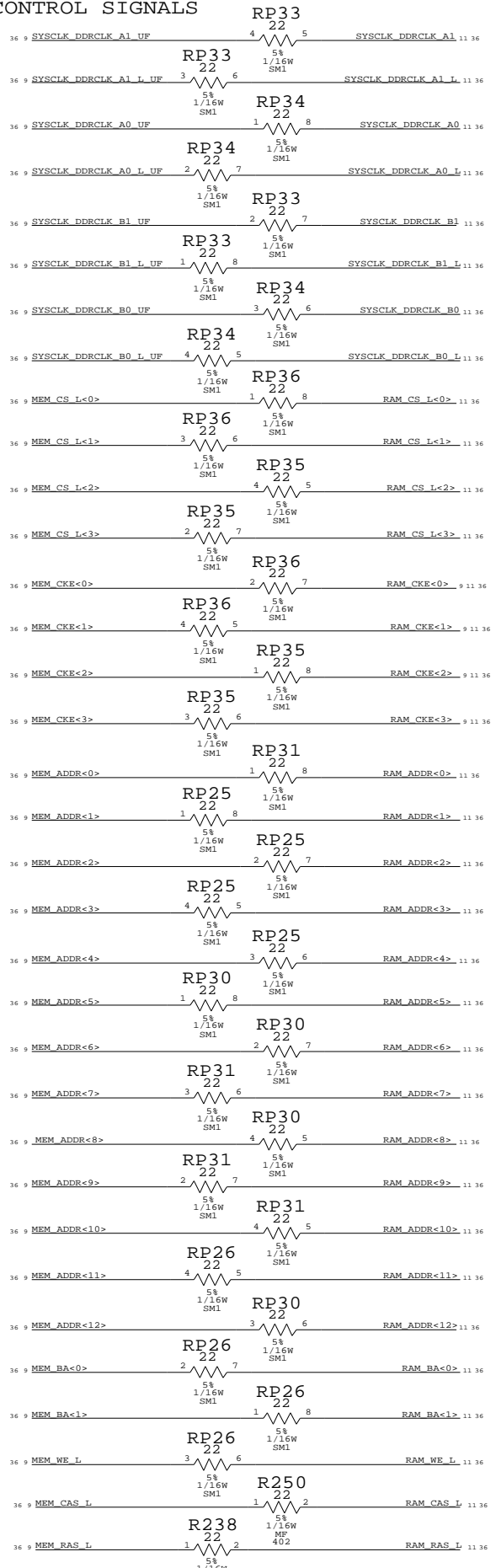
CRITICAL
U45
INTREPID-REV2.1
BGA
(2 OF 9)

DDR MEMORY INTERFACE

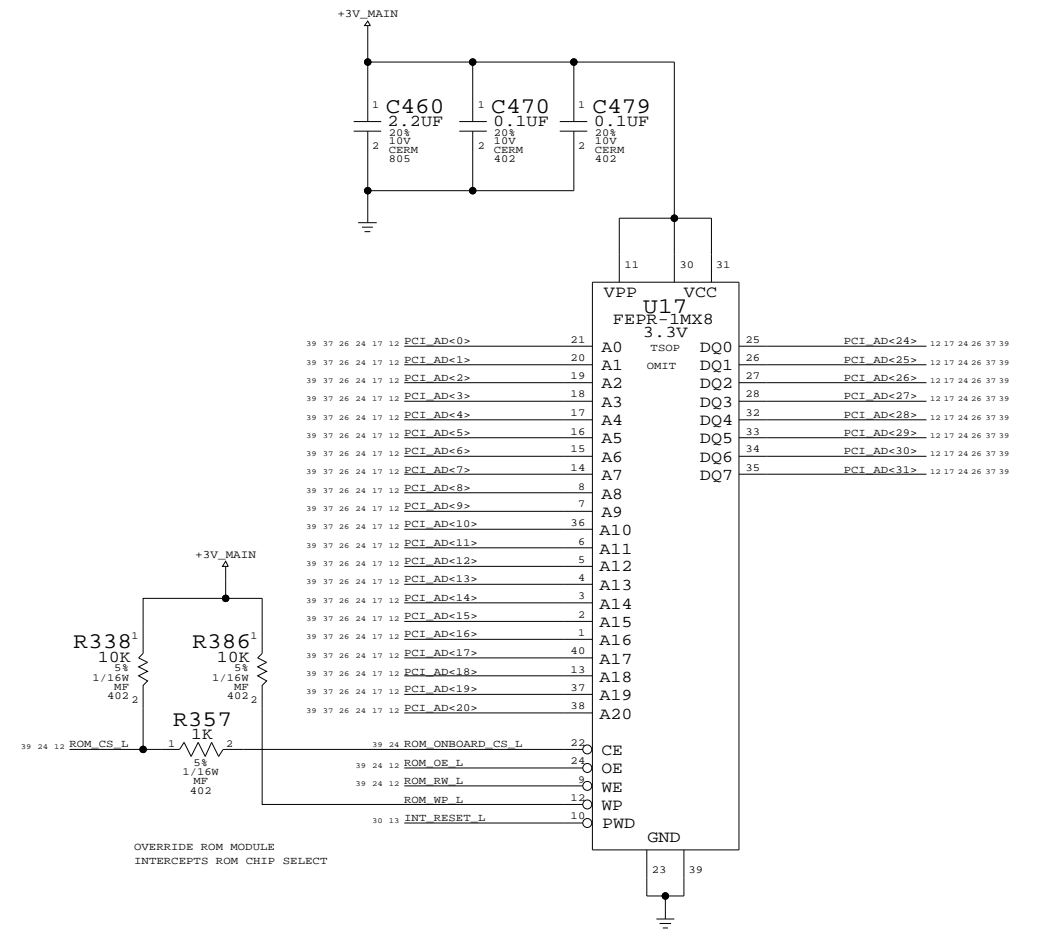
MEM_VREF



CLOCKS
CS
CKE
ADDR
BA
CNTL

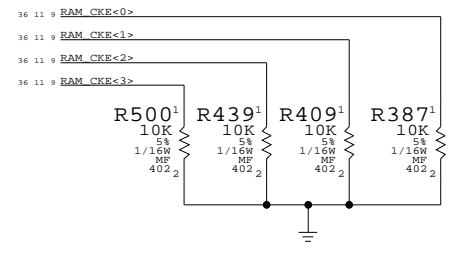


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1464	1	BOOTROM,PROTO,Q41A	U17	CRITICAL	?

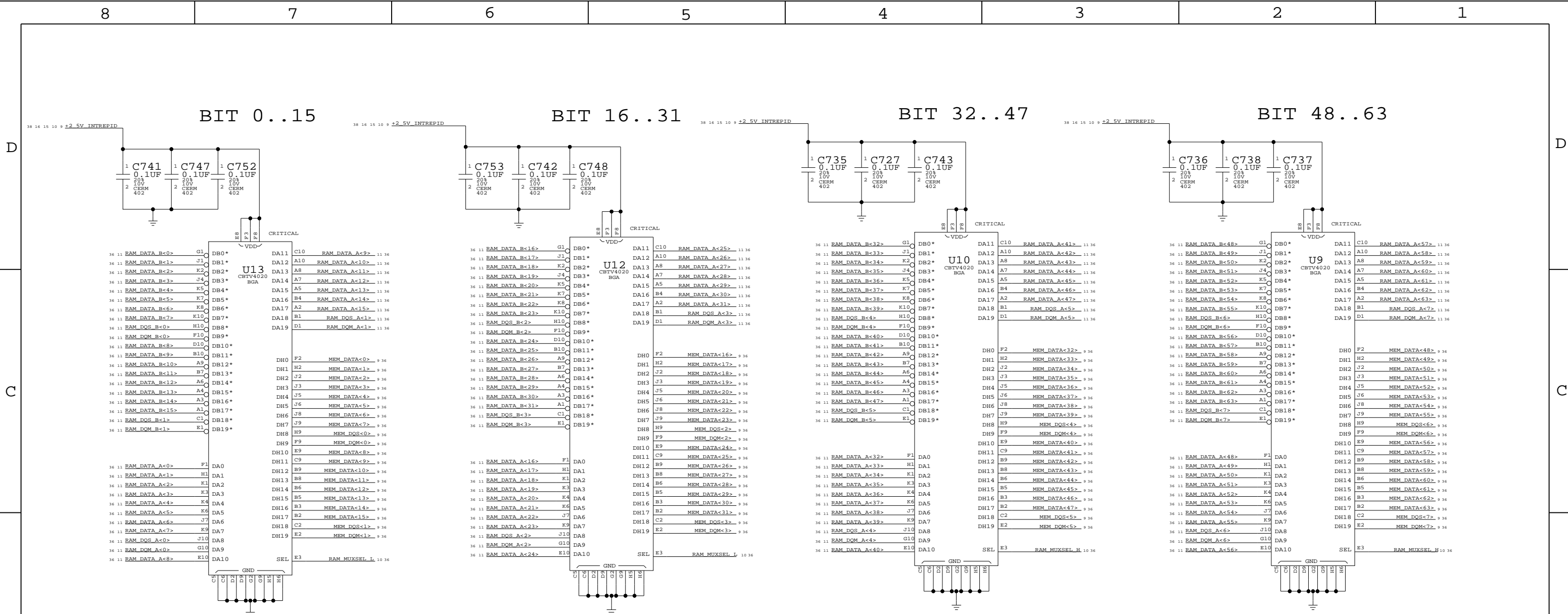
PULL-DOWN RESISTORS TO ENSURE CKE STAYS LOW AFTER INTREPID 2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6598	01
		SHT	OF
		9	44



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
 SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
 MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
 MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

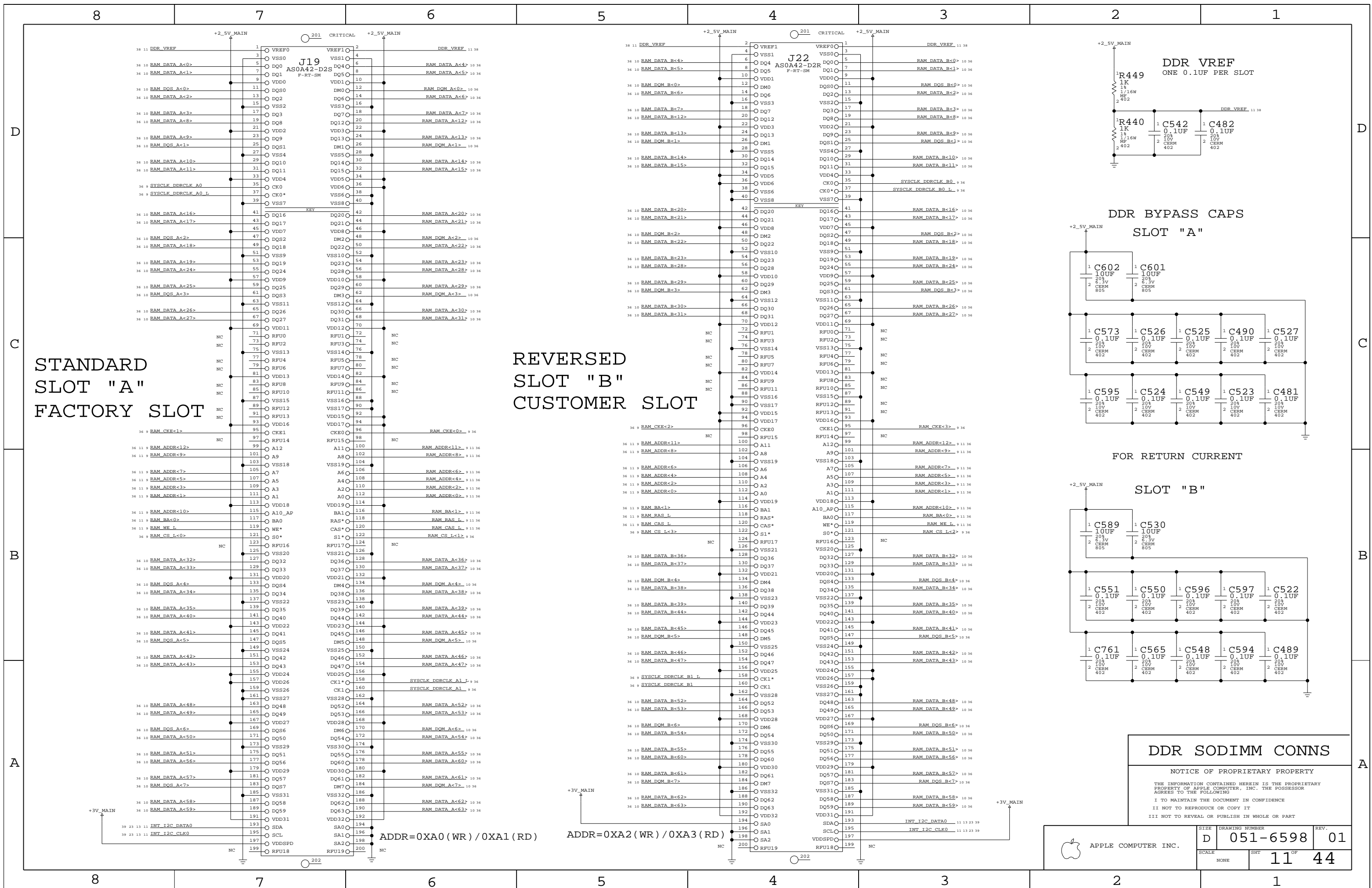
ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



16BIT 2:1 DDR MUXES

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	D	051-6598	01
SCALE	SHT	10 ^{OF} 44	
NONE			



STANDARD
SLOT "A"
FACTORY SLOT

REVERSED
SLOT "B"
CUSTOMER SLOT

DDR VREF
ONE 0.1UF PER SLOT

DDR BYPASS CAPS
SLOT "A"

FOR RETURN CURRENT

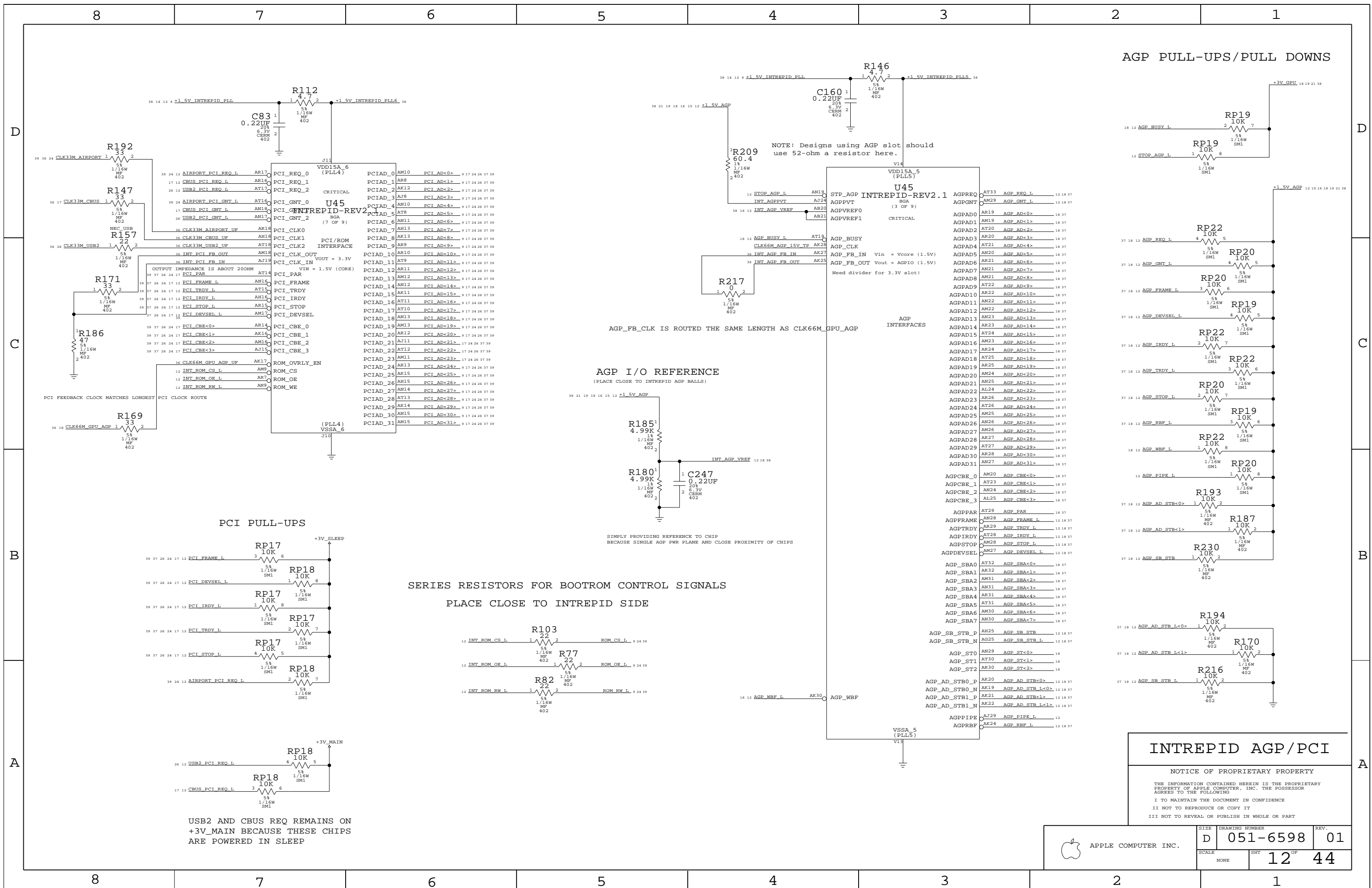
SLOT "B"

DDR SODIMM CONNS

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SCALE	SHT	11 OF 44	
NONE			



AGP PULL-UPS/PULL DOWNS

AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)

PCI PULL-UPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE

USB2 AND CBUS REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP

AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP

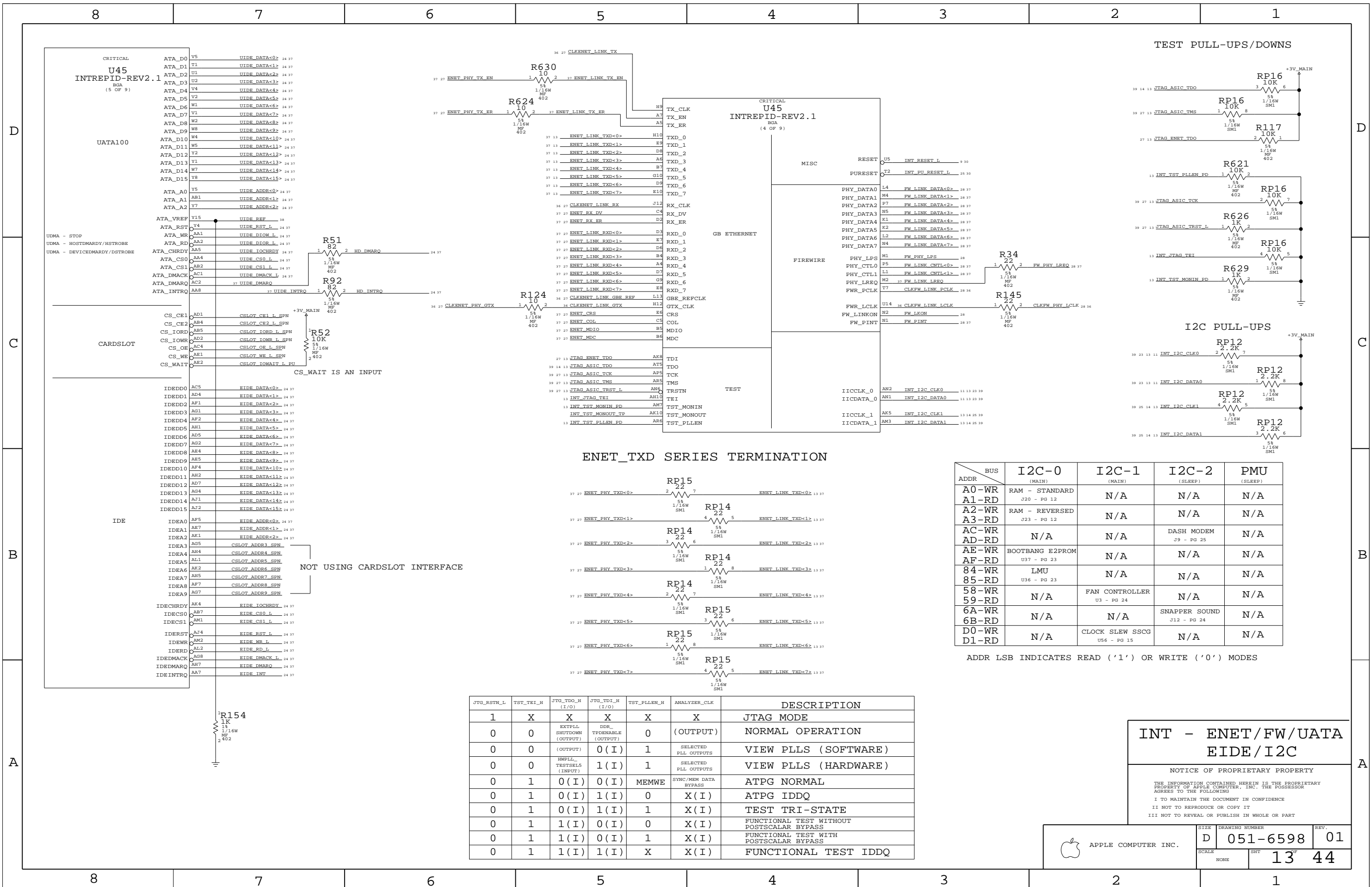
NOTE: Designs using AGP slot should use 52-ohm a resistor here.

INTREPID AGP/PCI

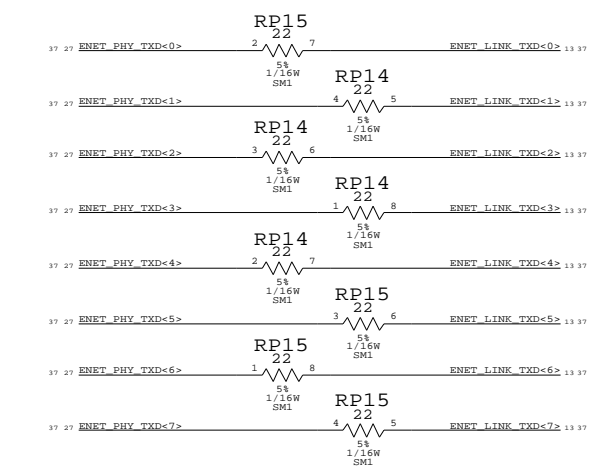
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	D	051-6598	01
SCALE	SHT	REV.	
NONE	12 OF	44	



ENET_TXD SERIES TERMINATION



ADDR	BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR	RAM - STANDARD	J20 - PG 12	N/A	N/A	N/A
A1-RD					
A2-WR	RAM - REVERSED	J23 - PG 12	N/A	N/A	N/A
A3-RD					
AC-WR				DASH MODEM	N/A
AD-RD				J9 - PG 25	N/A
AE-WR	BOOTBANG E2PROM	U37 - PG 23	N/A	N/A	N/A
AF-RD					
84-WR	LMU	U36 - PG 23	N/A	N/A	N/A
85-RD					
58-WR		FAN CONTROLLER	N/A	N/A	N/A
59-RD		U3 - PG 24			
6A-WR				SNAPPER SOUND	N/A
6B-RD				J12 - PG 24	
D0-WR			CLOCK SLEW SSCG	N/A	N/A
D1-RD			U56 - PG 15		

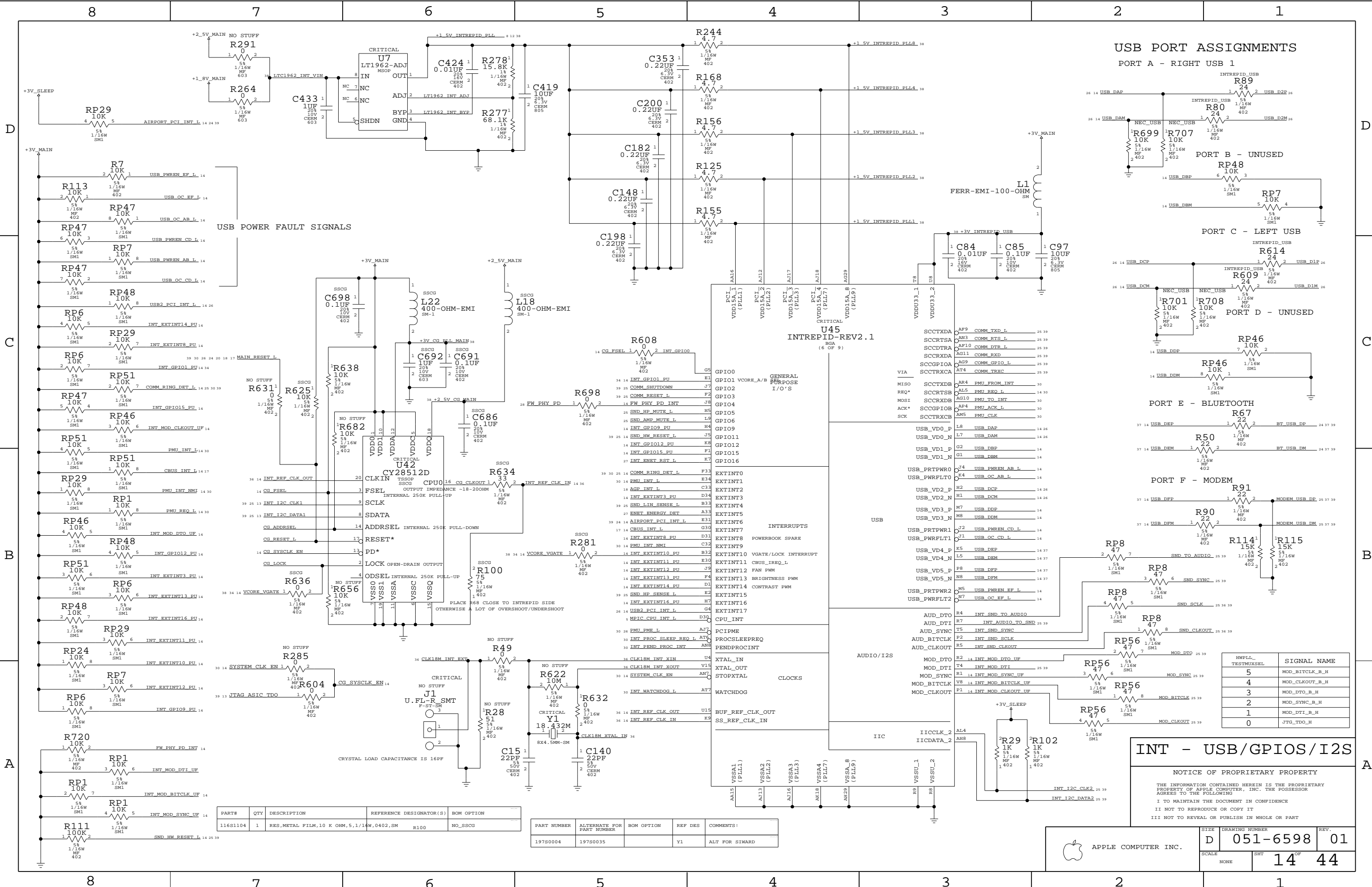
ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TRI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0 (I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_TESTSEL5 (INPUT)	1 (I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0 (I)	0 (I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0 (I)	1 (I)	0	X (I)	ATPG IDDQ
0	1	0 (I)	1 (I)	1	X (I)	TEST TRI-STATE
0	1	1 (I)	0 (I)	0	X (I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1 (I)	0 (I)	1	X (I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1 (I)	1 (I)	X	X (I)	FUNCTIONAL TEST IDDQ

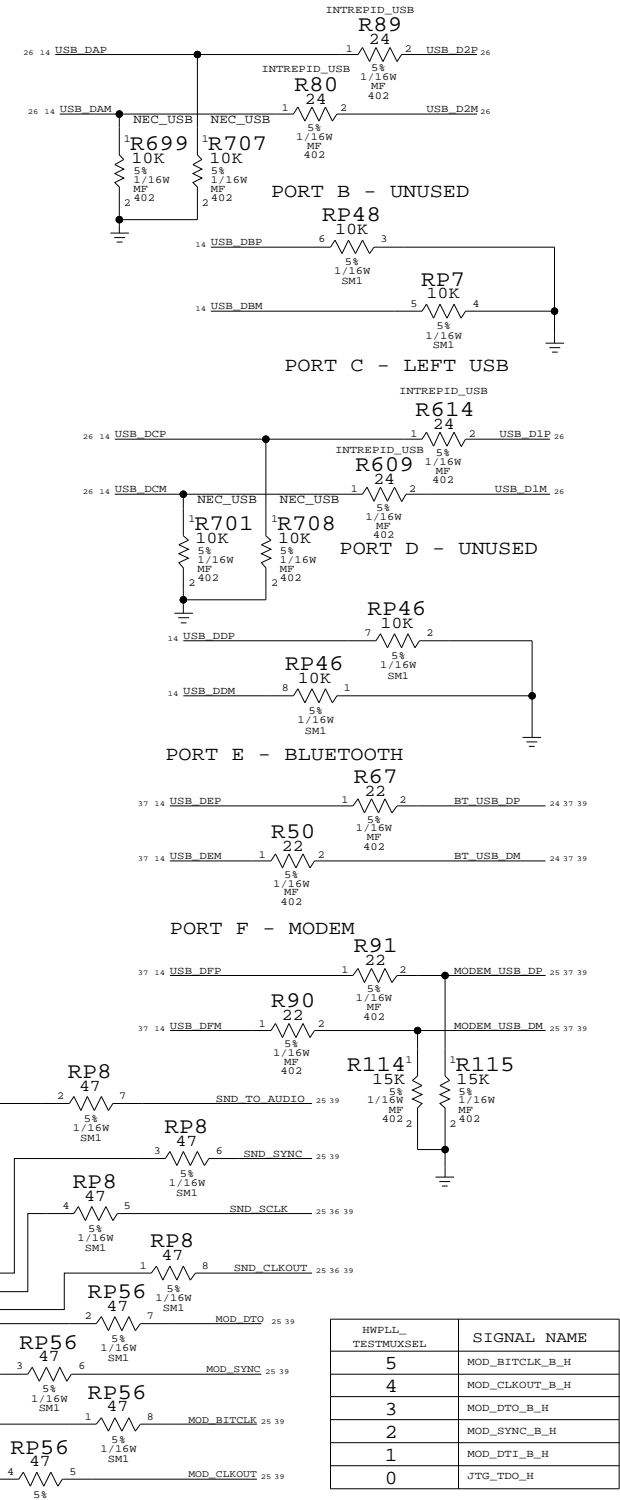
INT - ENET/FW/UATA EIDE/I2C

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SCALE	NONE	SHT	13 44



USB PORT ASSIGNMENTS



INT - USB/GPIOS/I2S

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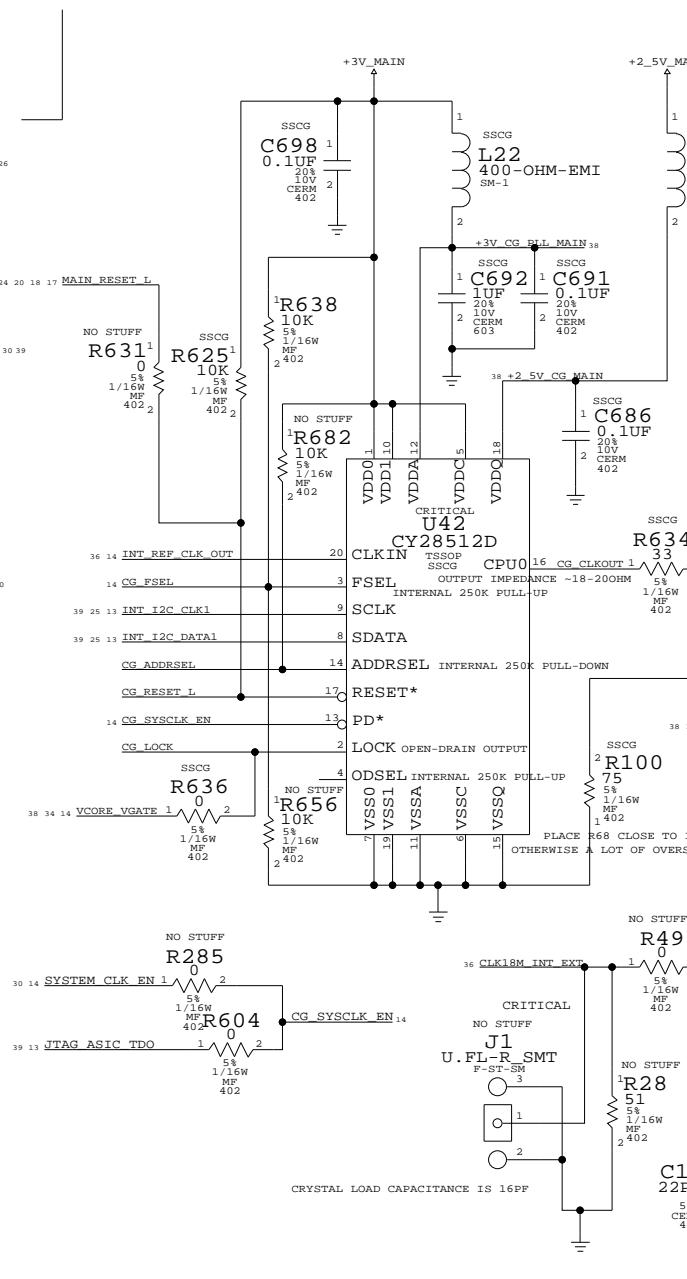
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USB POWER FAULT SIGNALS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES, METAL FILM, 10 K OHM, 5, 1/16W, 0402, SM	R100	NO_SSCG

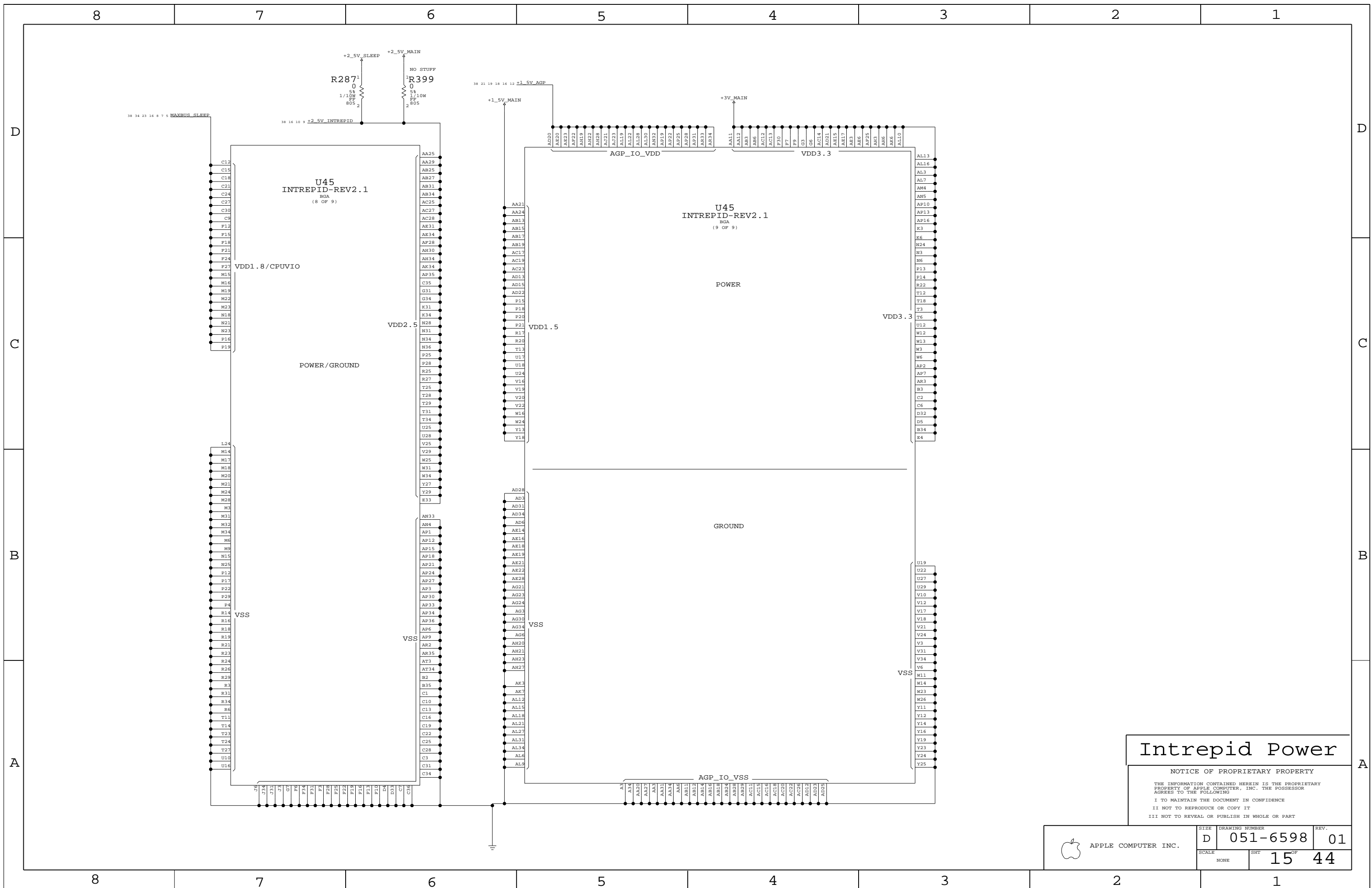
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

APPLE COMPUTER INC.

SIZE: **D** DRAWING NUMBER: **051-6598** REV.: **01**

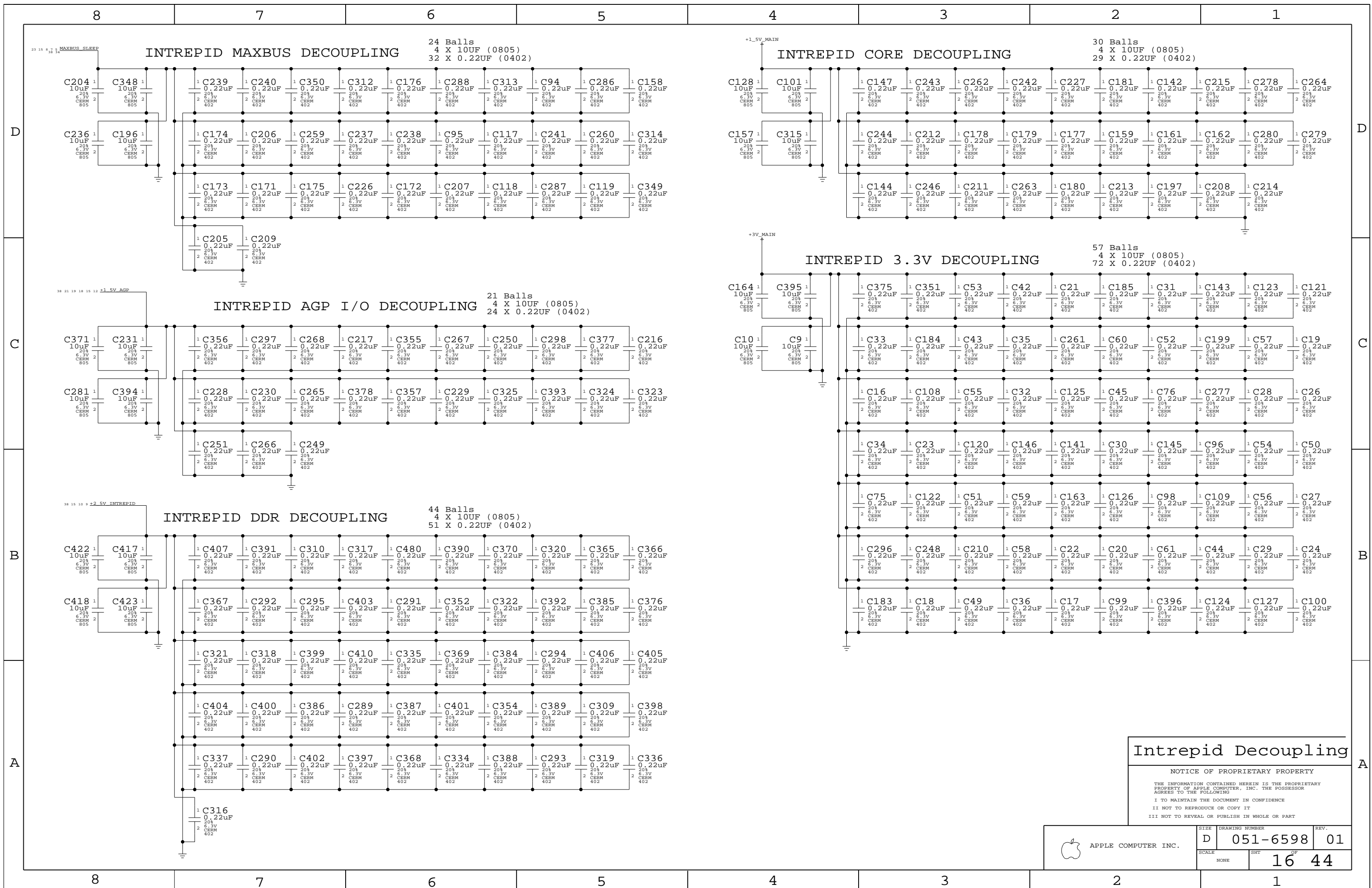
SCALE: NONE SHEET: **14** OF **44**



Intrepid Power

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Intrepid Decoupling

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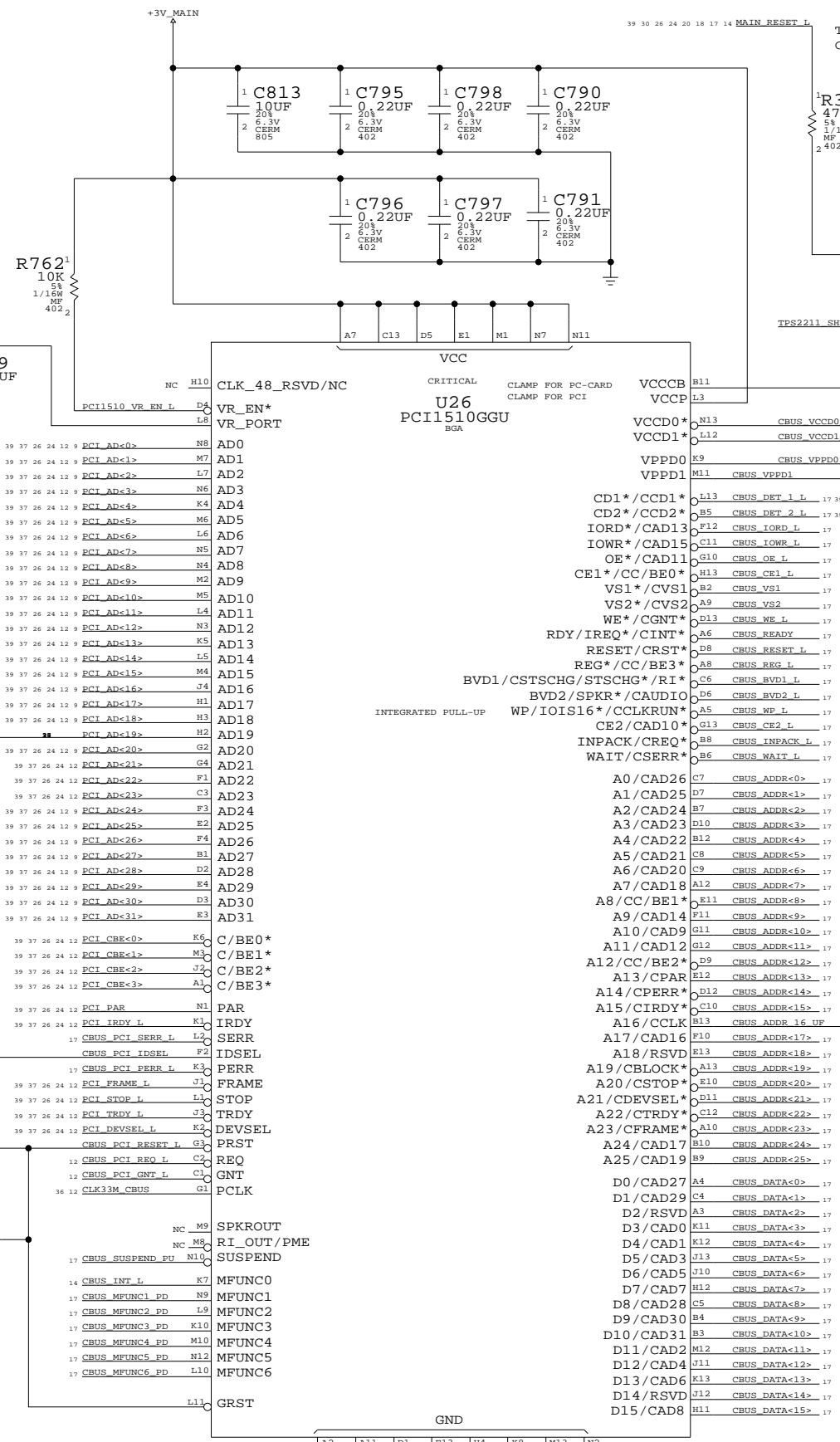
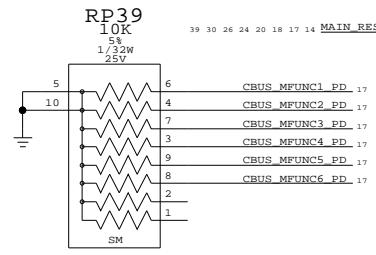
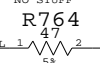
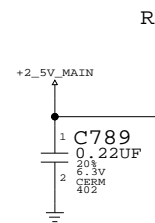
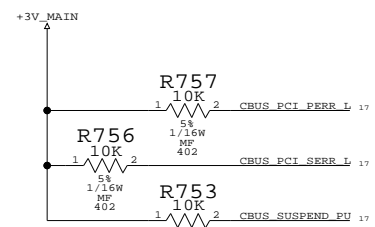
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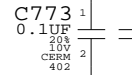
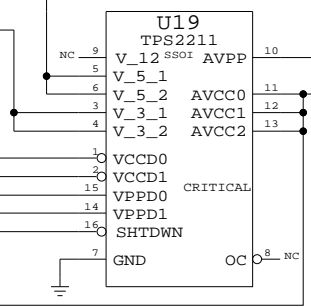
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	D	051-6598	01
SCALE	SHT	OF	
NONE	16	44	

PCI1510 PULL-UPS



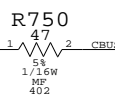
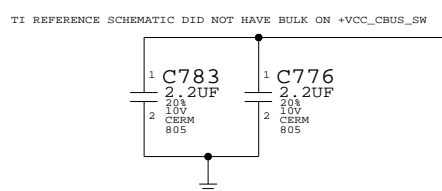
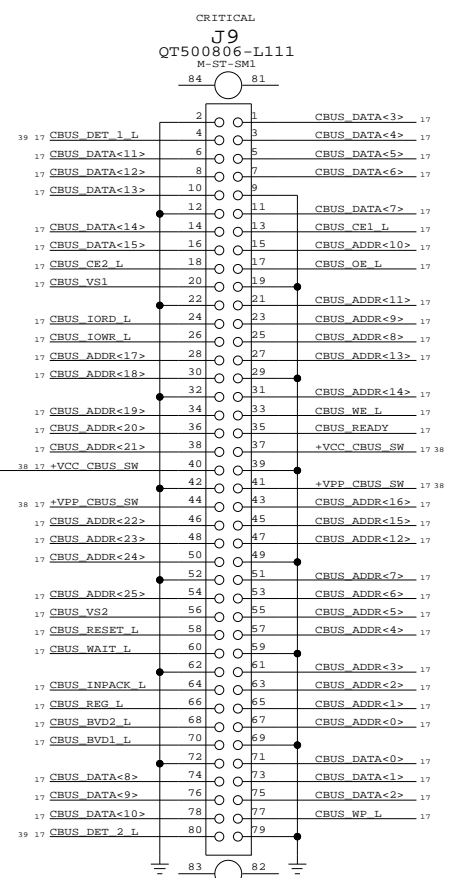
THIS PROPERLY SHUTS DOWN CARDBUS POWER FOR PSUEDO-D3COLD



MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

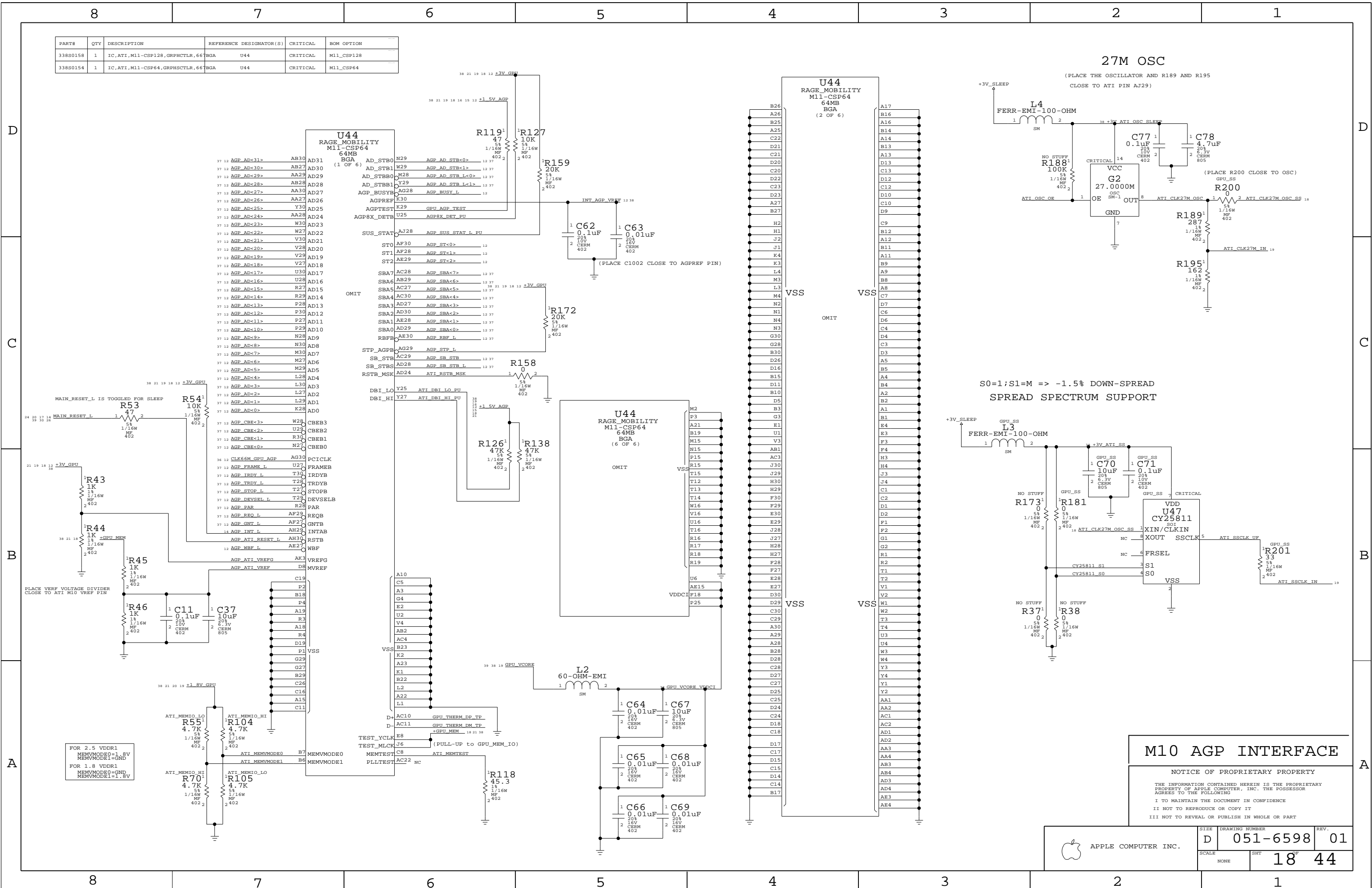
PC CARD/CARDBUS CONNECTOR



CARDBUS
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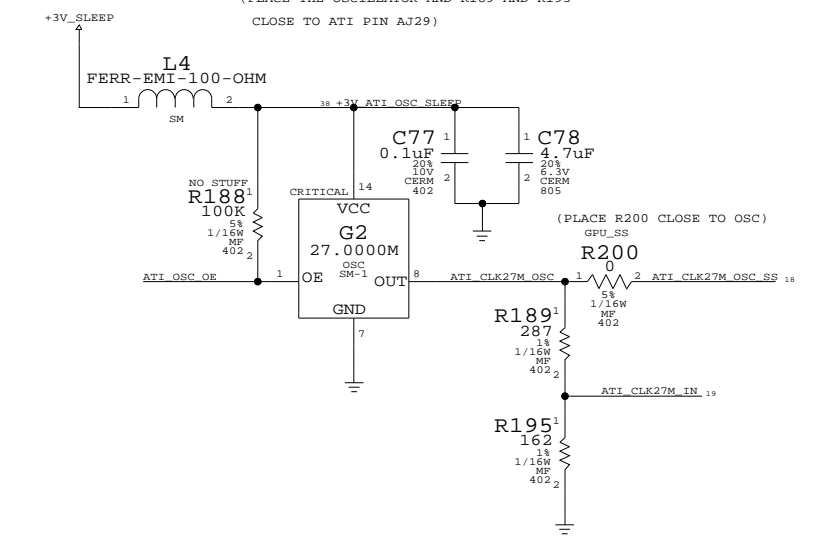
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	NONE	SHT	17 OF 44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTLR,66	BGA U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHCTLR,66	BGA U44	CRITICAL	M11_CSP64

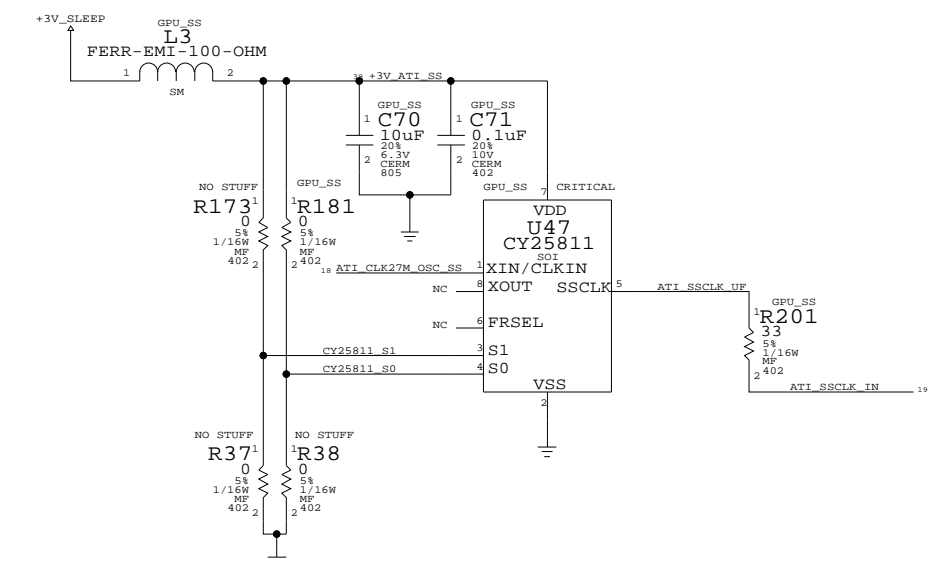


27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)



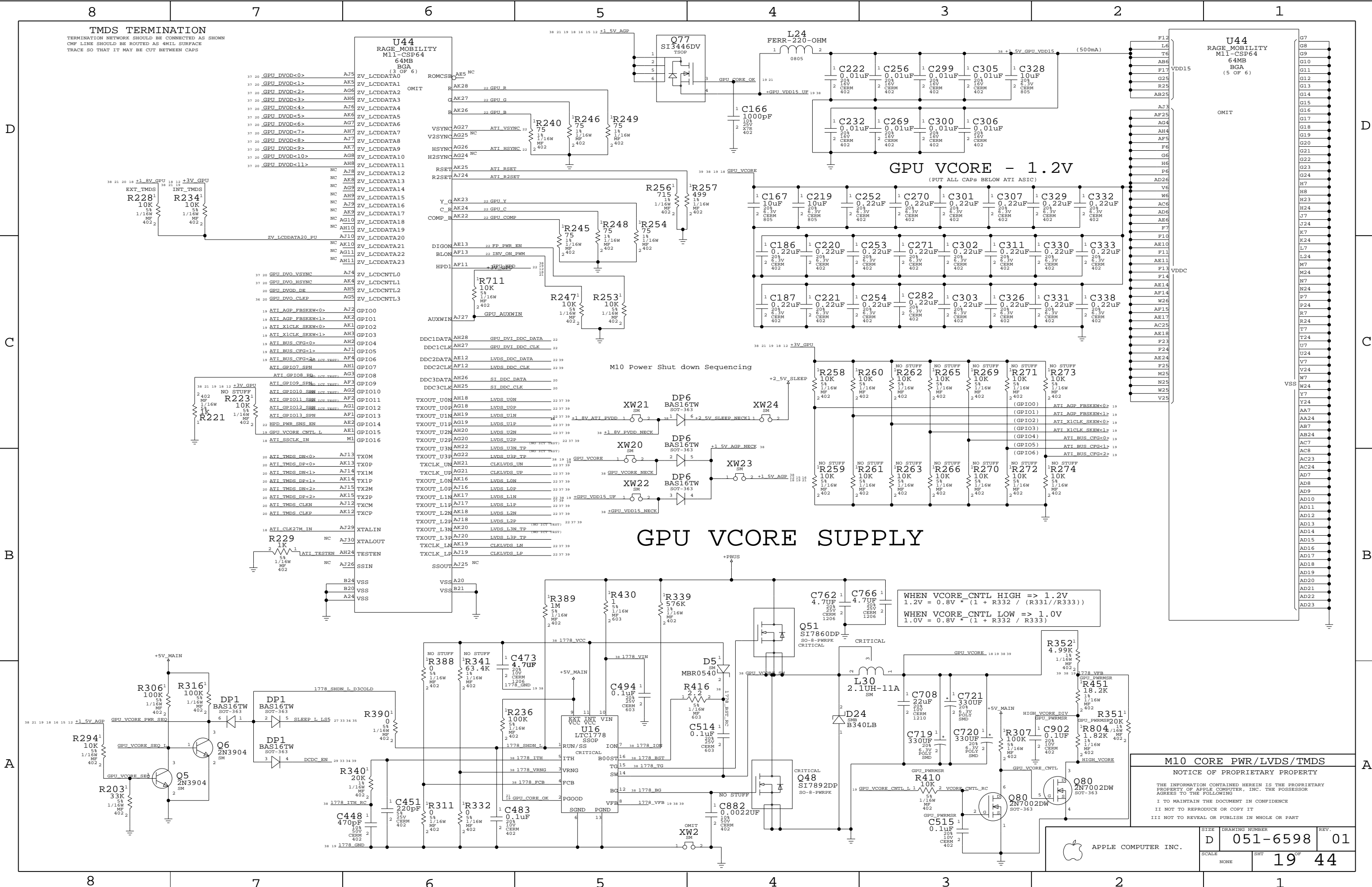
S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT



M10 AGP INTERFACE

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SCALE	SHT	18 OF 44	
NONE			



TMD5 TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMP LINE SHOULD BE ROUTED AS 4MIL SURFACE TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU Pin	GPU Label	GPU Label	GPU Label
37 20	GPU_DVOD<0>	AJ5	ZV_LCDDATA0
37 20	GPU_DVOD<1>	AK5	ZV_LCDDATA1
37 20	GPU_DVOD<2>	AG6	ZV_LCDDATA2
37 20	GPU_DVOD<3>	AH6	ZV_LCDDATA3
37 20	GPU_DVOD<4>	AJ6	ZV_LCDDATA4
37 20	GPU_DVOD<5>	AK6	ZV_LCDDATA5
37 20	GPU_DVOD<6>	AG7	ZV_LCDDATA6
37 20	GPU_DVOD<7>	AH7	ZV_LCDDATA7
37 20	GPU_DVOD<8>	AJ7	ZV_LCDDATA8
37 20	GPU_DVOD<9>	AK7	ZV_LCDDATA9
37 20	GPU_DVOD<10>	AG8	ZV_LCDDATA10
37 20	GPU_DVOD<11>	AH8	ZV_LCDDATA11
		AJ8	ZV_LCDDATA12
		AK8	ZV_LCDDATA13
		AG9	ZV_LCDDATA14
		AH9	ZV_LCDDATA15
		AJ9	ZV_LCDDATA16
		AK9	ZV_LCDDATA17
		AG10	ZV_LCDDATA18
		AH10	ZV_LCDDATA19
		AJ10	ZV_LCDDATA20
		AK10	ZV_LCDDATA21
		AG11	ZV_LCDDATA22
		AH11	ZV_LCDDATA23
			ZV_LCDDATA20_PU
			ZV_LCDDATA21
			ZV_LCDDATA22
			ZV_LCDDATA23
37 20	GPU_DVO_VSYNC	AJ4	ZV_LCDCNTL0
37 20	GPU_DVO_HSYNC	AK4	ZV_LCDCNTL1
37 20	GPU_DVO_DE	AH5	ZV_LCDCNTL2
37 20	GPU_DVO_CLKP	AG5	ZV_LCDCNTL3
19	ATI_AGP_FB_SKEW<0>	AJ2	GPIO0
19	ATI_AGP_FB_SKEW<1>	AK2	GPIO1
19	ATI_X1CLK_SKEW<0>	AK1	GPIO2
19	ATI_X1CLK_SKEW<1>	AH3	GPIO3
19	ATI_BUS_CFG<0>	AH2	GPIO4
19	ATI_BUS_CFG<1>	AJ1	GPIO5
19	ATI_BUS_CFG<2>	AF4	GPIO6
19	ATI_GPIO7_SEN	AH1	GPIO7
19	ATI_GPIO8_BD	AG3	GPIO8
19	ATI_GPIO9_SFN	AF3	GPIO9
19	ATI_GPIO10_SFN	AG2	GPIO10
19	ATI_GPIO11_SFN	AF2	GPIO11
19	ATI_GPIO12_SFN	AG1	GPIO12
19	ATI_GPIO13_SFN	AF1	GPIO13
19	HDD_PWR_SNS_EN	AE2	GPIO14
19	GPU_VCORE_CNTL_L	AE1	GPIO15
18	ATI_SSCLK_IN	M1	GPIO16
			TXOM
20	ATI_TMD5_DN<0>	AJ13	TXOP
20	ATI_TMD5_DP<0>	AK13	TXIM
20	ATI_TMD5_DN<1>	AJ14	TXIP
20	ATI_TMD5_DP<1>	AK14	TX2M
20	ATI_TMD5_DN<2>	AJ15	TX2P
20	ATI_TMD5_DP<2>	AK15	TXCM
20	ATI_TMD5_CLKN	AJ12	TXCP
20	ATI_TMD5_CLKP	AK12	
18	ATI_CLK27M_IN	AJ29	XTALIN
		AJ30	XTALOUT
		AH24	TESTEN
		AJ26	SSOUT
			VSS
			VSS
			VSS

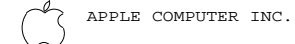
GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

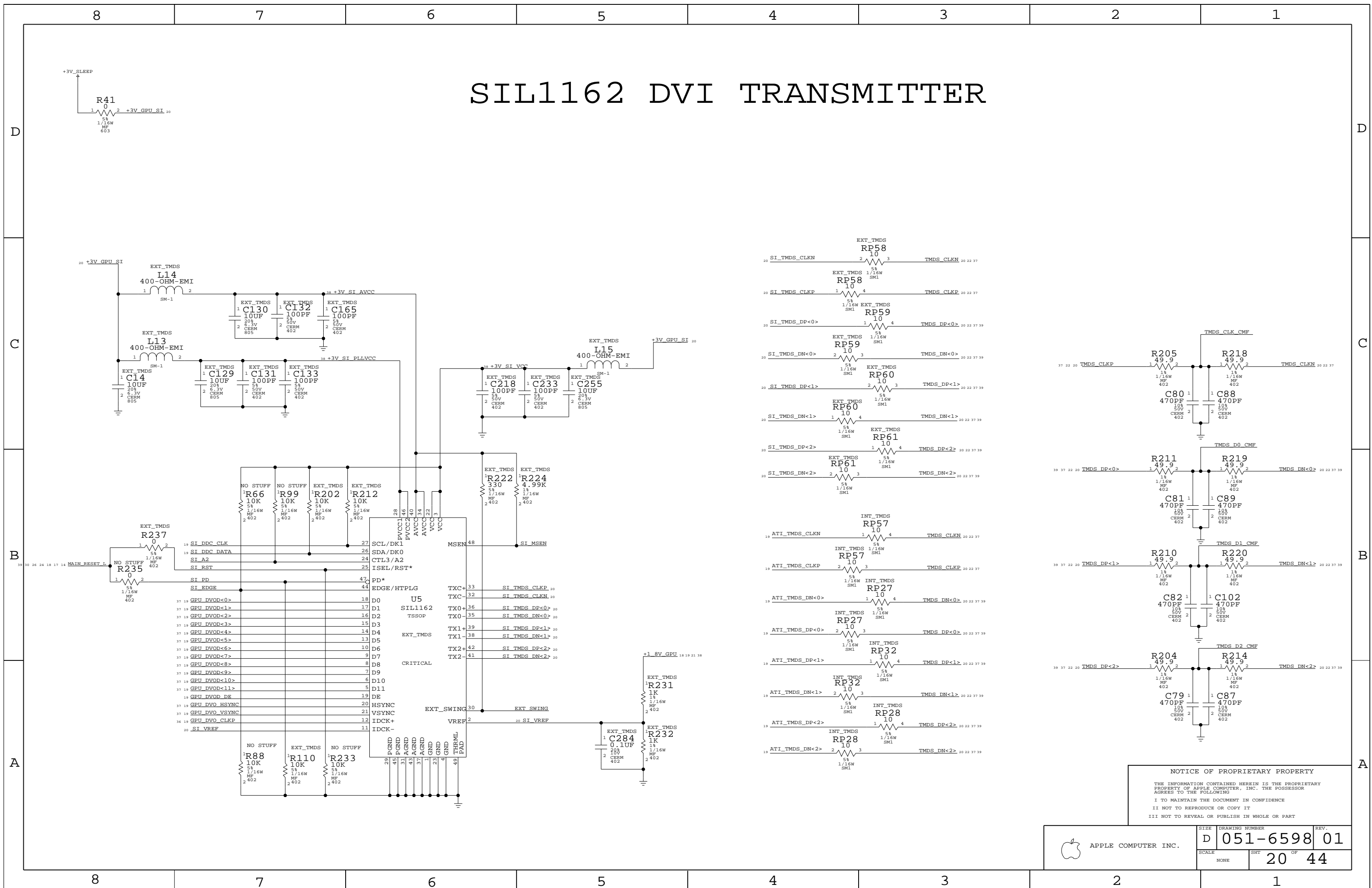
M10 CORE PWR/LVDS/TMD5

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SCALE	SHT	19 OF 44

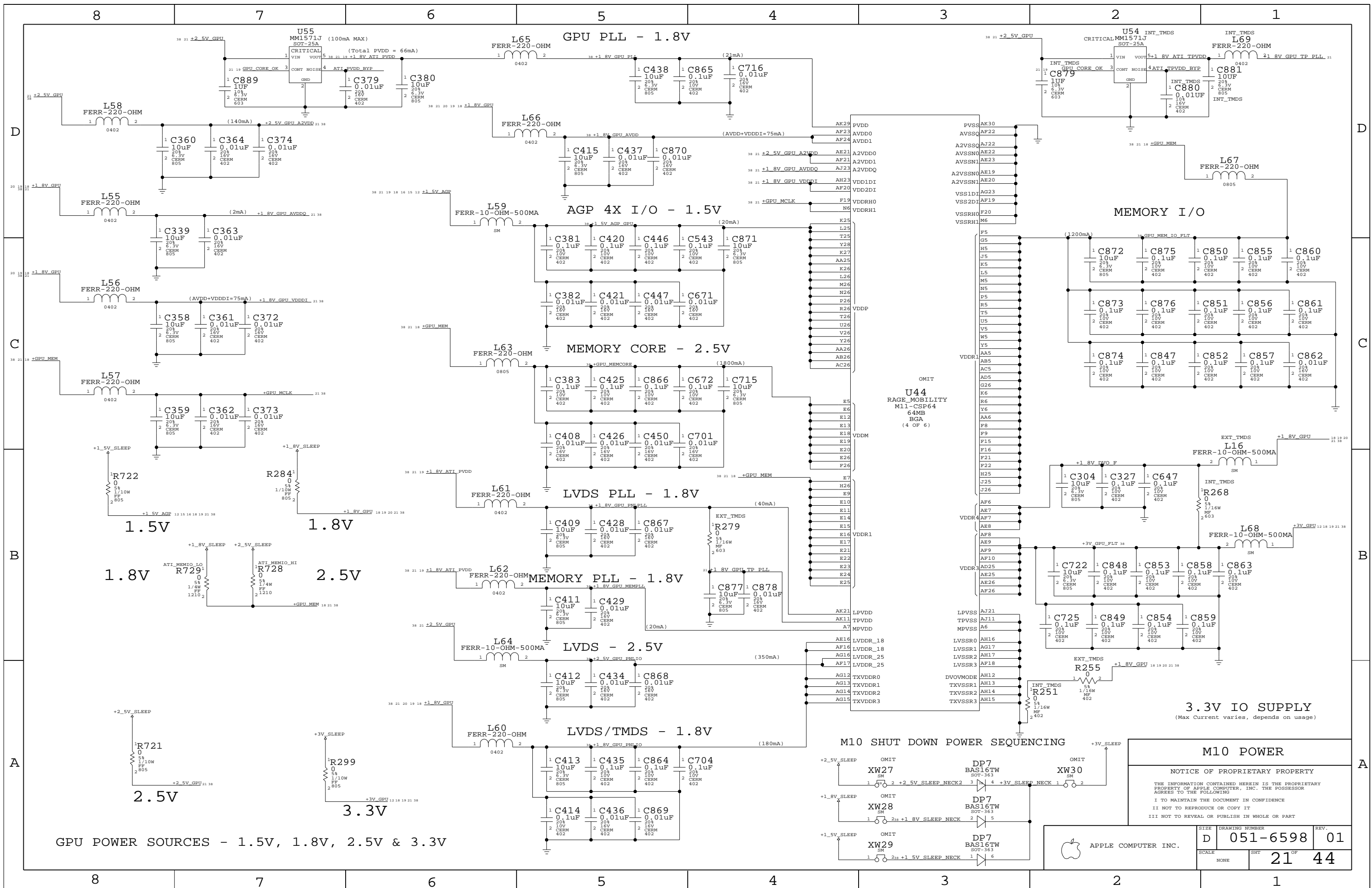


SIL1162 DVI TRANSMITTER



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SCALE		SHT	OF
NONE		20	44



GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

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D	051-6598	01
SCALE	SHT	OF
NONE	21	44

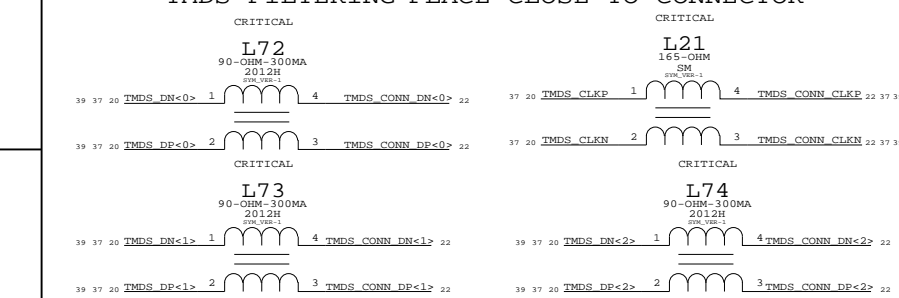
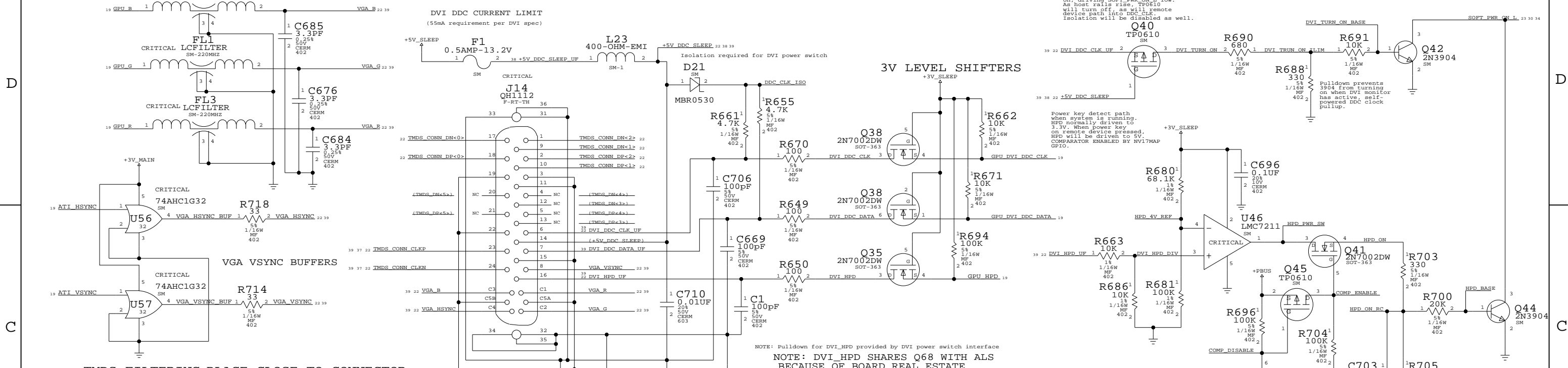


APPLE COMPUTER INC.

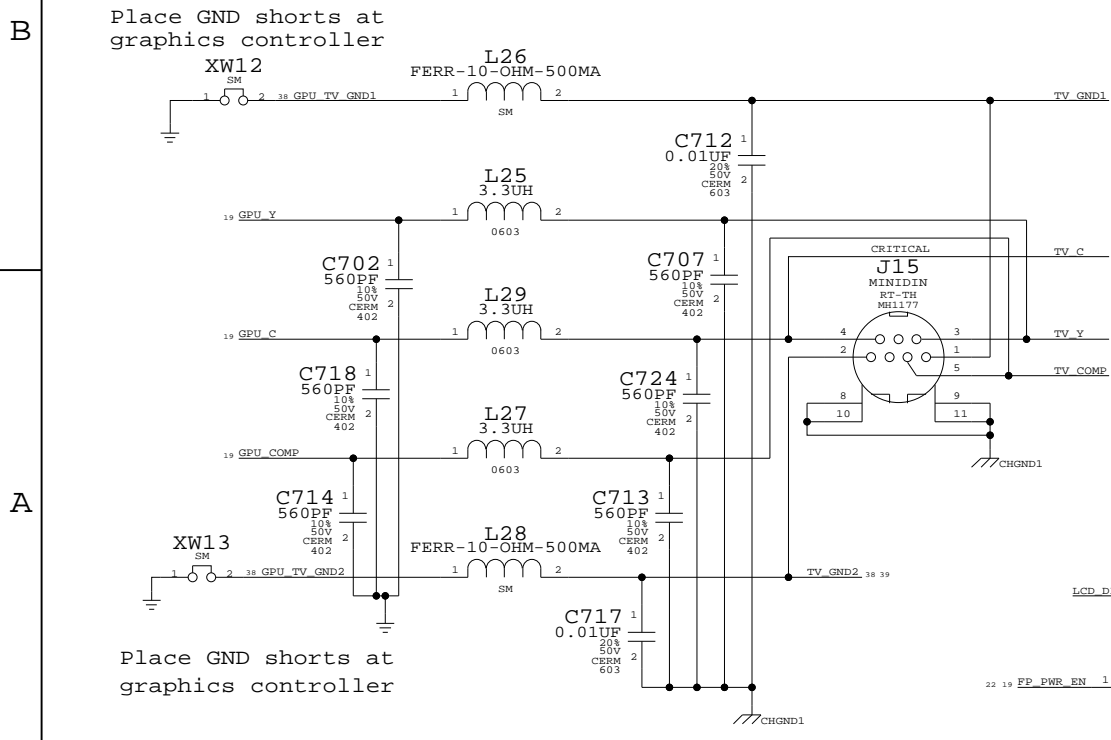
ANALOG FILTERING PLACE CLOSE TO CONNECTOR

EXTERNAL VIDEO (DVI) INTERFACE

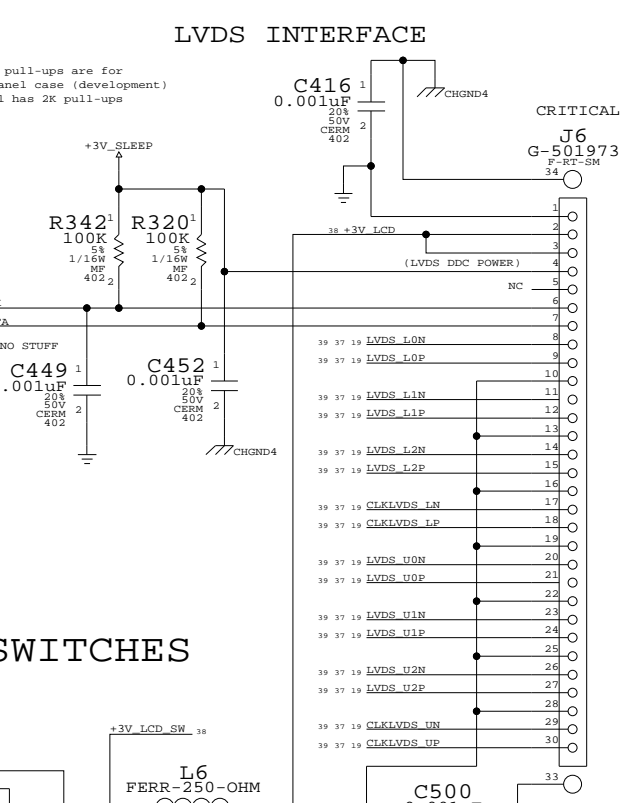
DVI POWER SWITCH



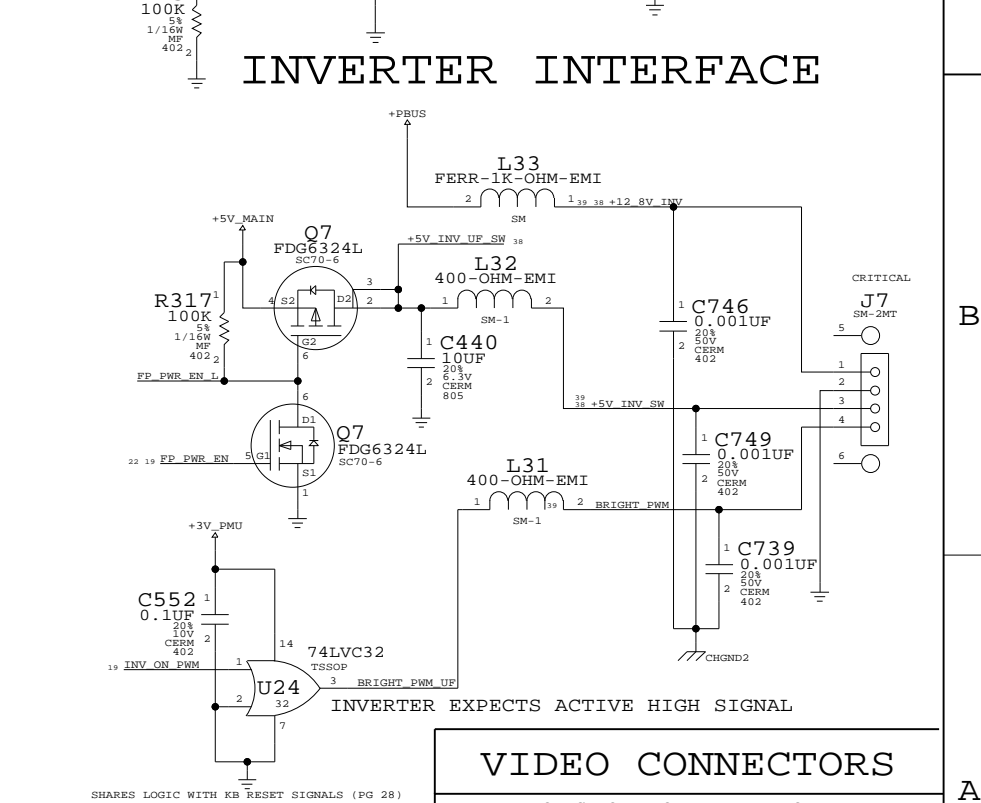
S-VIDEO/COMP OUT INTERFACE



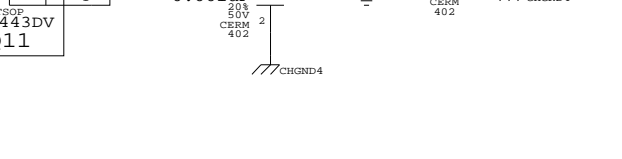
LCD INTERFACE



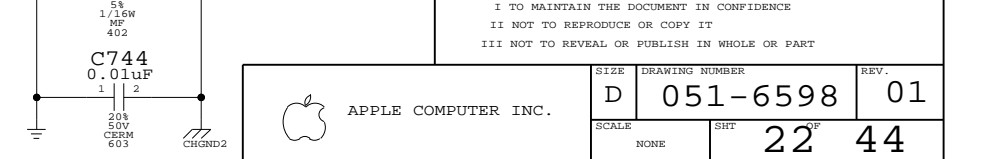
INVERTER INTERFACE



LCD POWER SWITCHES



VIDEO CONNECTORS



Place GND shorts at graphics controller

Place GND shorts at graphics controller

Place GND shorts at graphics controller

Place GND shorts at graphics controller

Place GND shorts at graphics controller

Place GND shorts at graphics controller

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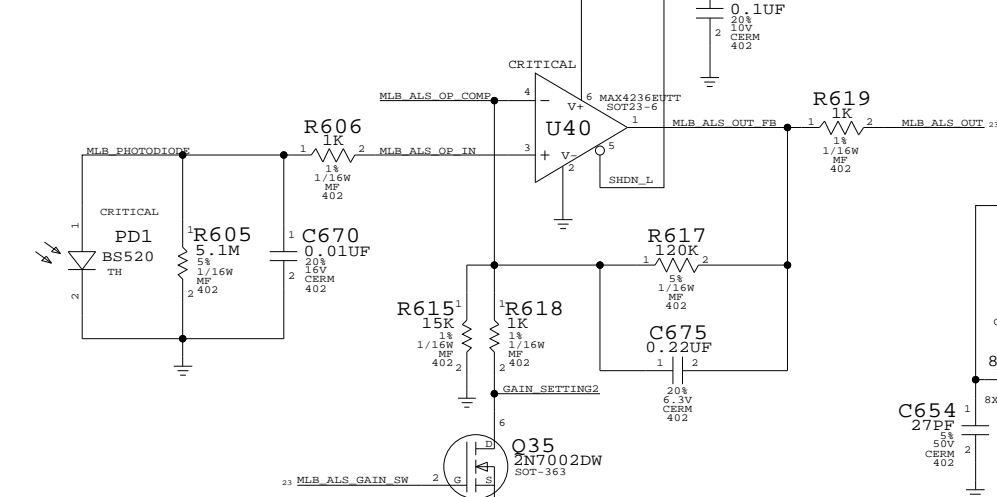
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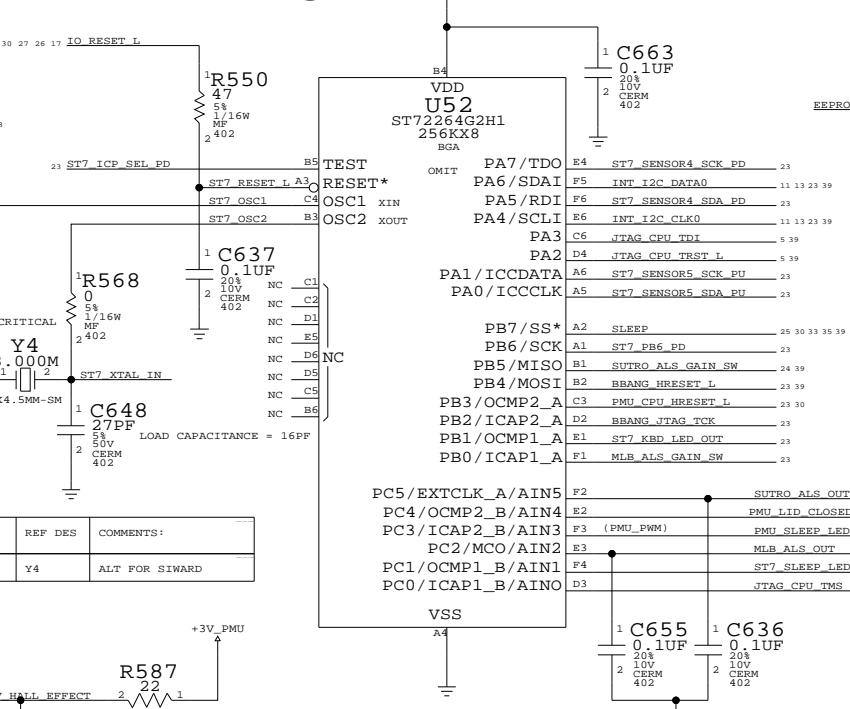
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	SHT	REV.	
NONE	22	44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR

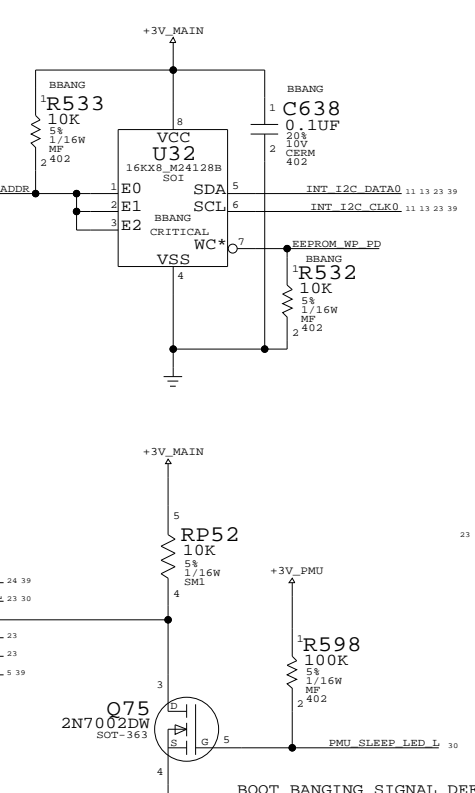


LMU

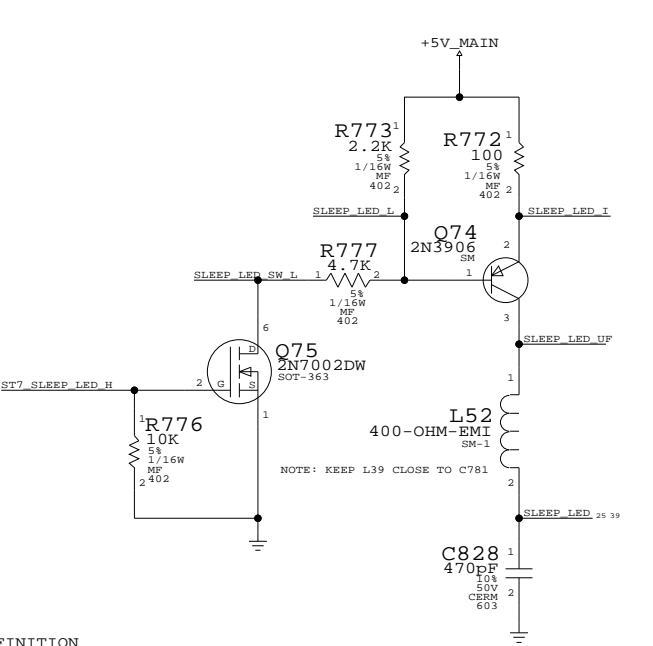


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIMARD

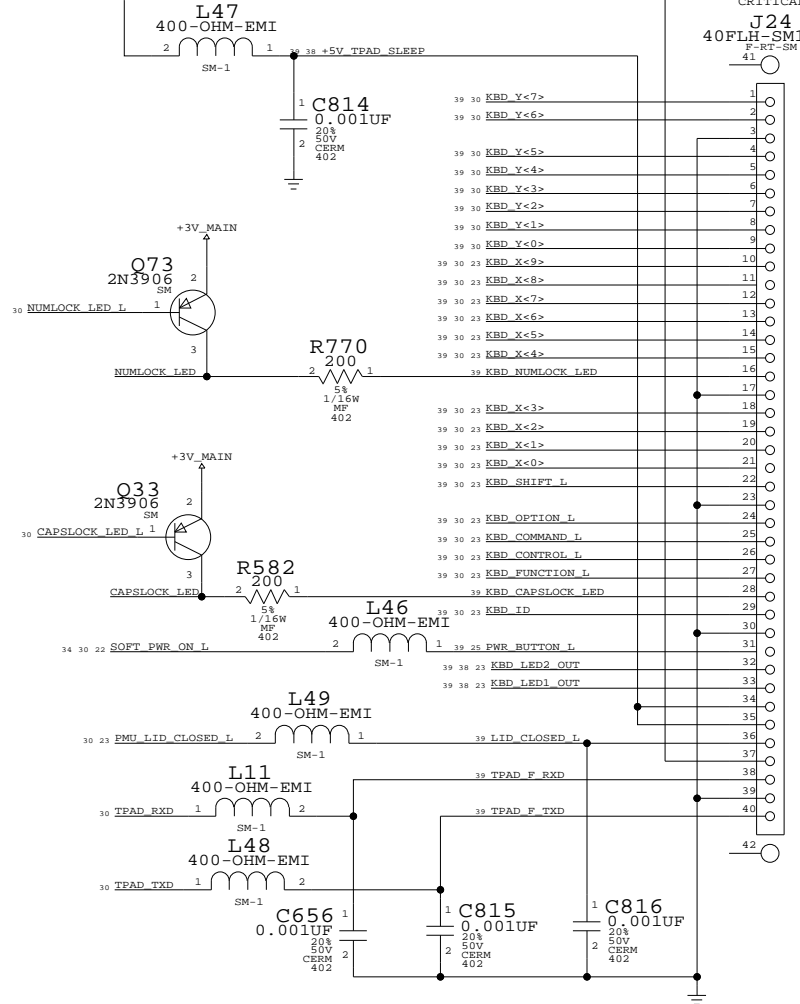
BOOT BANGER E2PROM



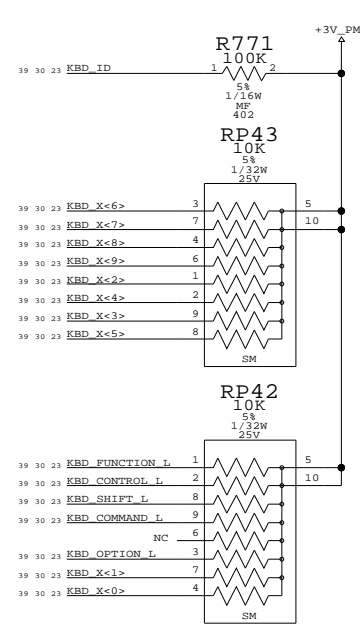
SLEEP LED



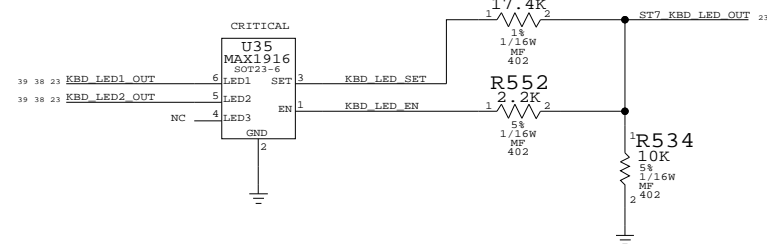
SPIDEY FLEX



KEYBOARD PULLUPS

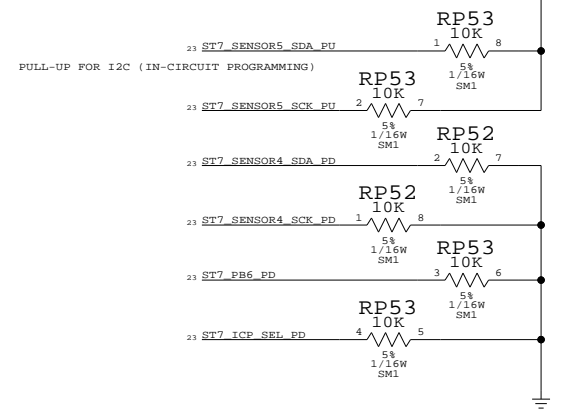


KB LED DRIVER



- BOOT BANGING SIGNAL DEFINITION**
- 1/ B Bang_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
 - 2/ PMU_HRESET_L (3V INPUT INTO LMU)
 - 3/ B Bang_JTAG_TCK (REGULAR OUTPUT)
 - 4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
 - 5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
 - 6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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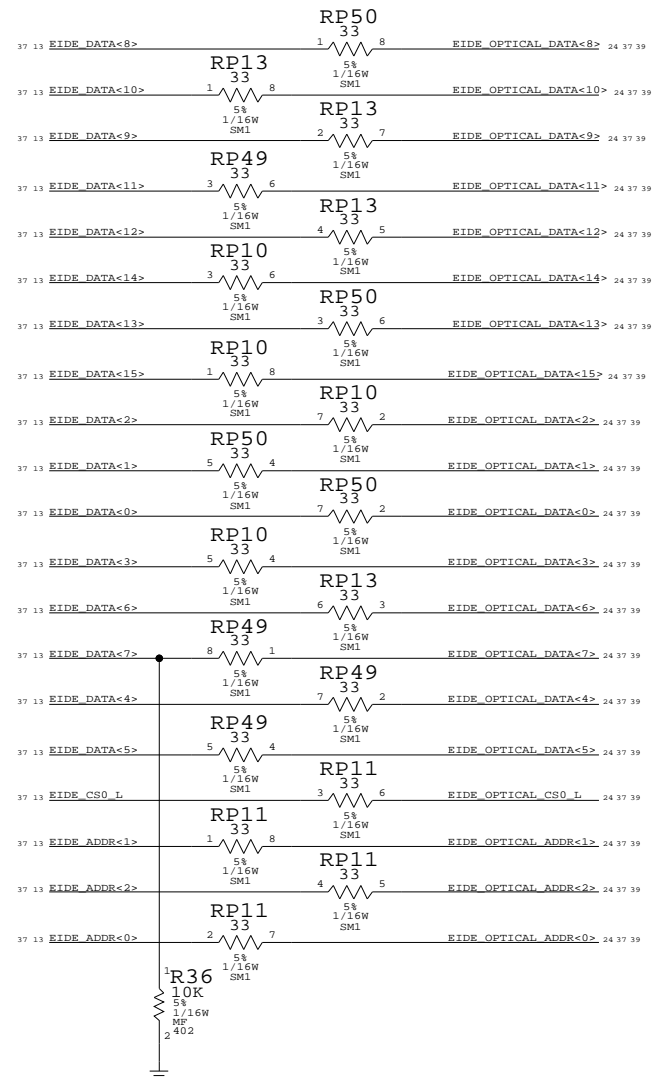
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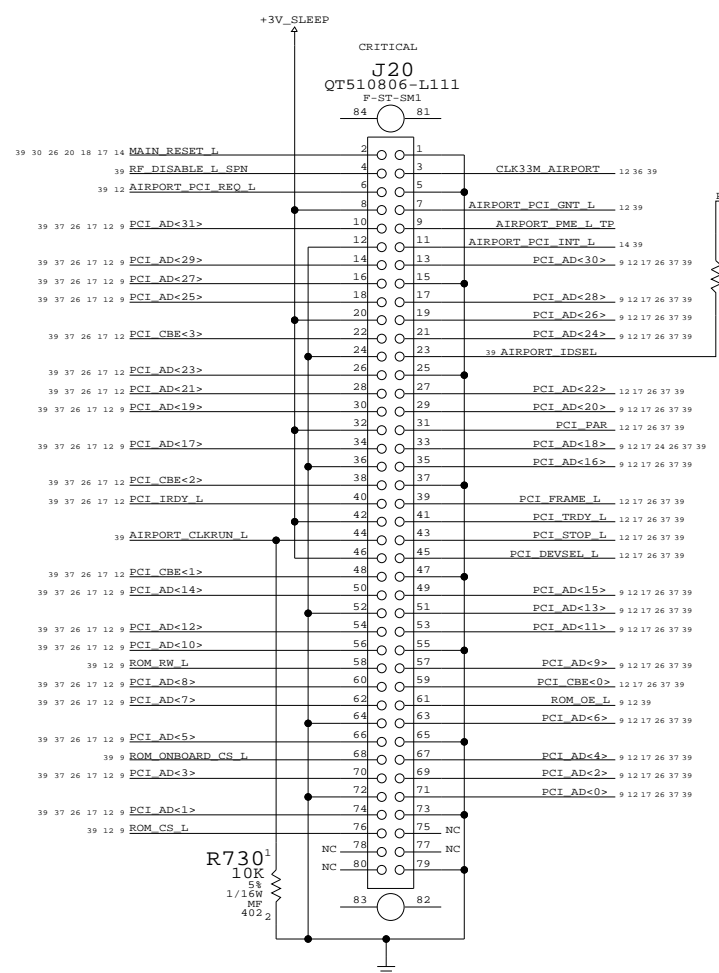
APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	23	01
D	051-6598	OF	44

HARD DRIVE INTERFACE (UATA100)

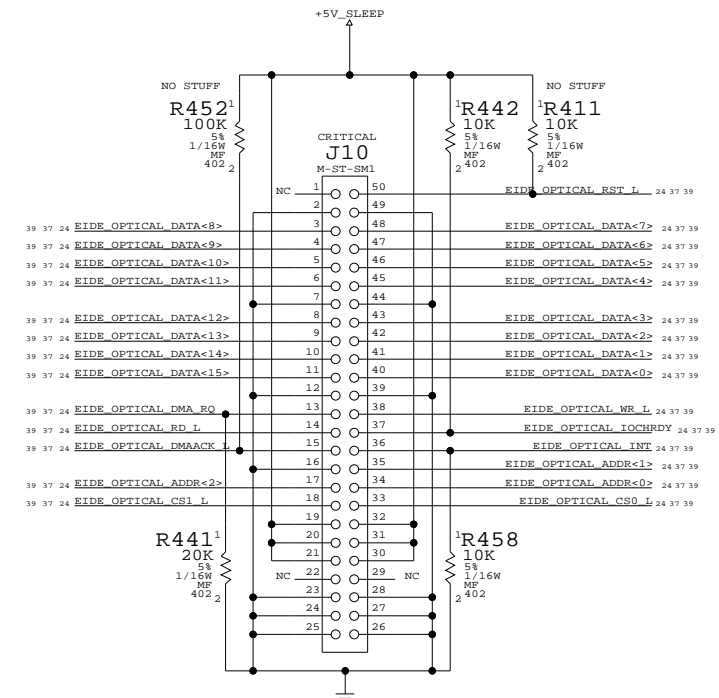
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID



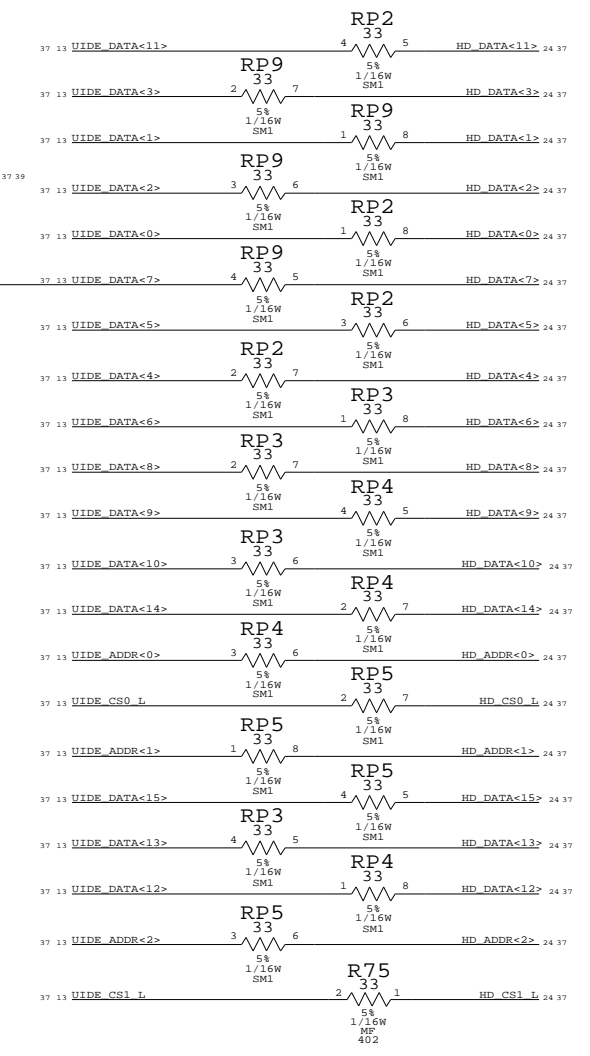
WIRELESS INTERFACE



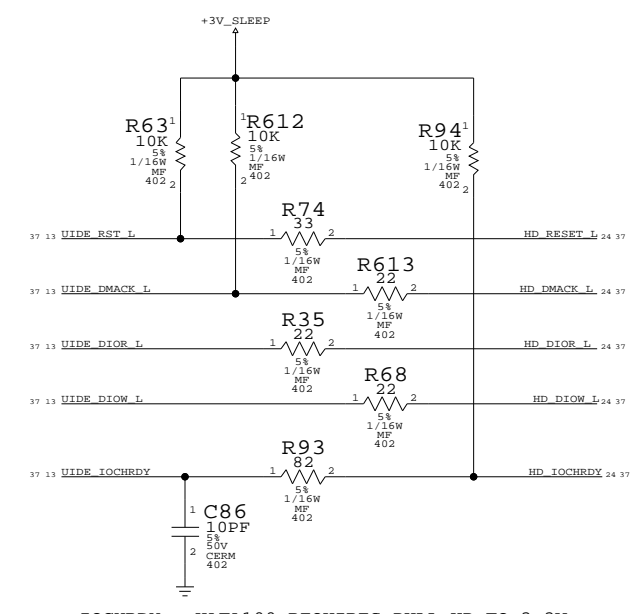
OPTICAL DRIVE INTERFACE (EIDE)



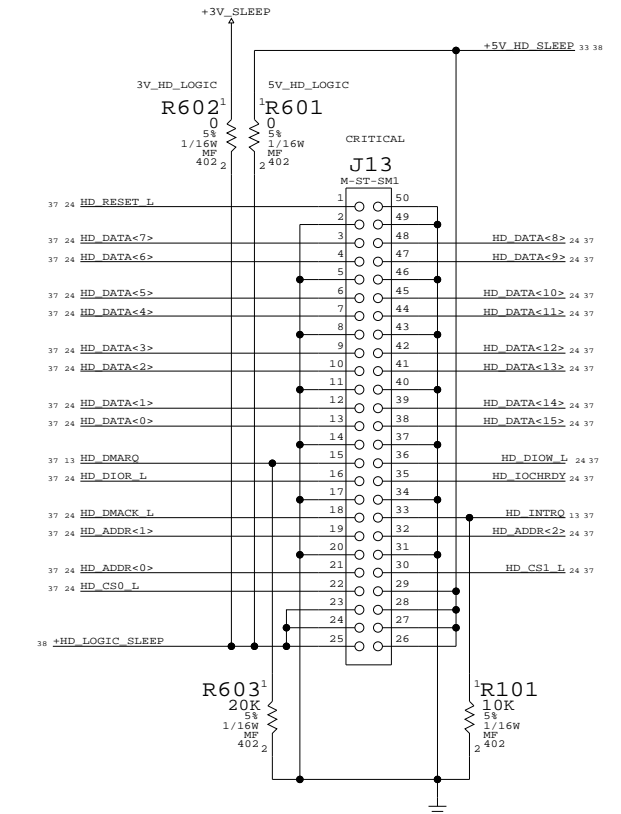
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

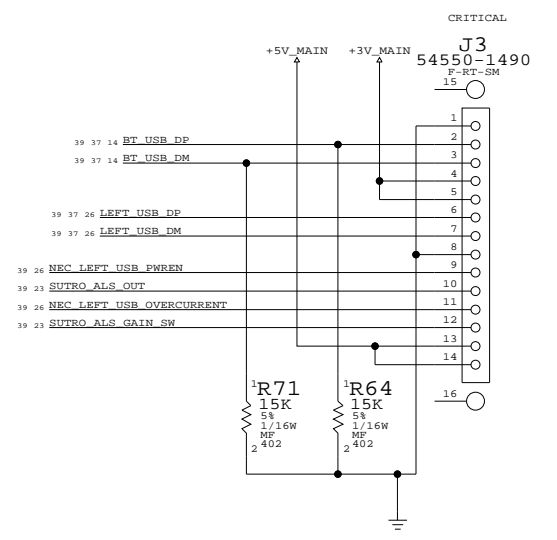


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP?

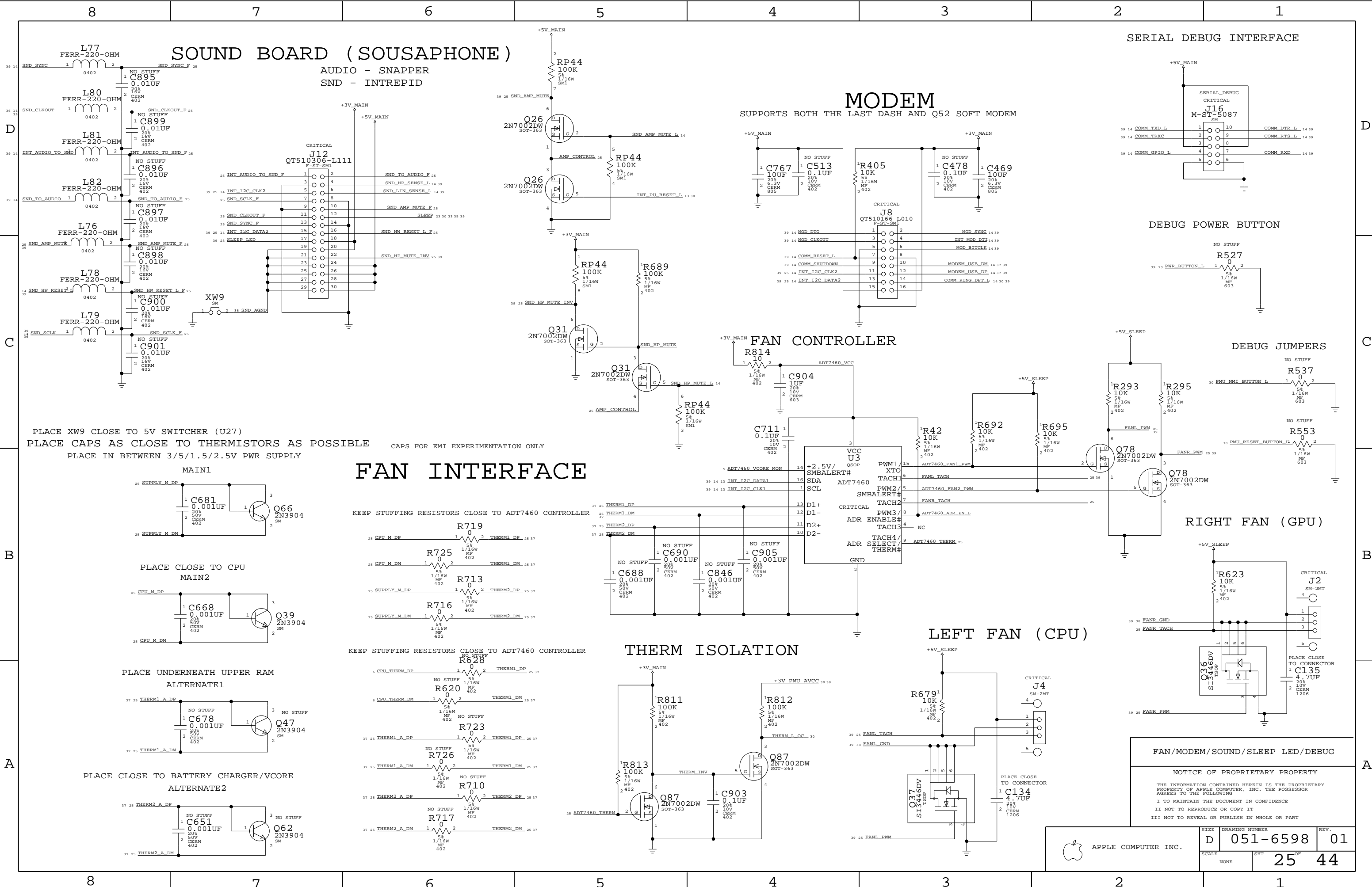
BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

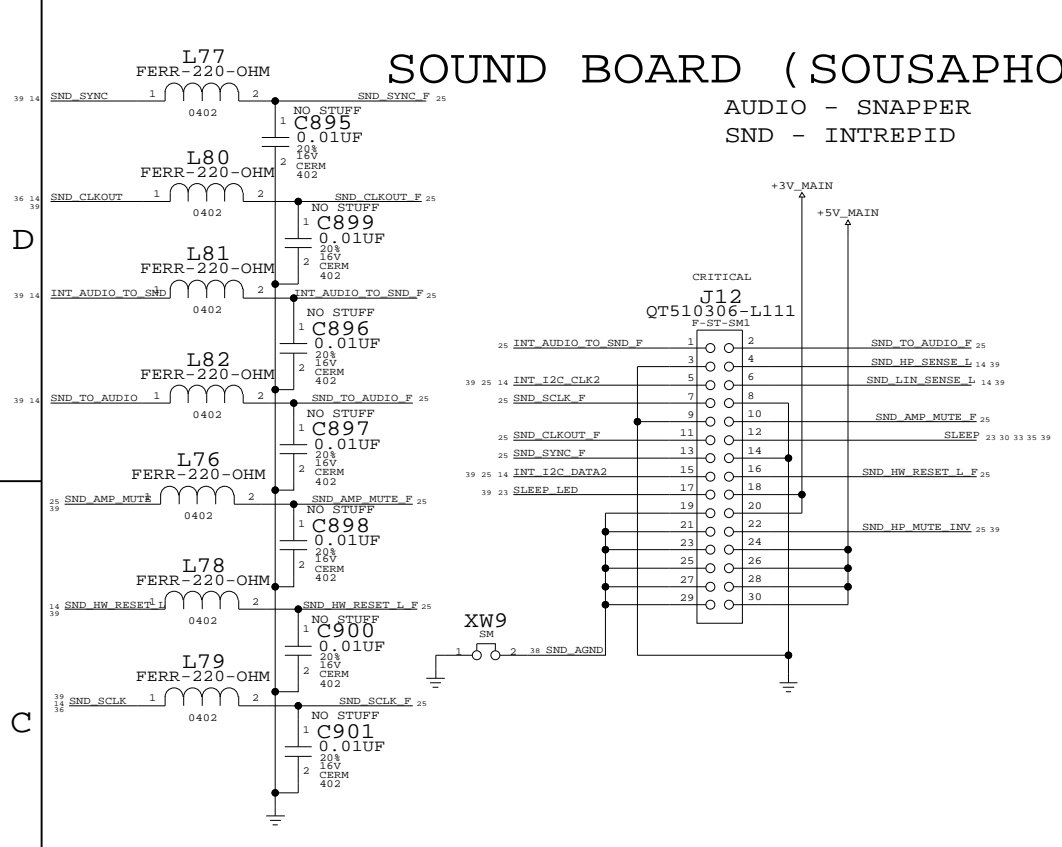
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	NONE	SHT	24 OF 44



SOUND BOARD (SOUSAPHONE)

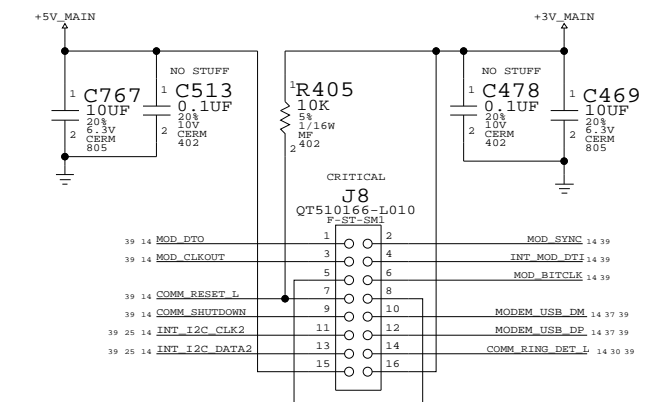
AUDIO - SNAPPER
SND - INTREPID



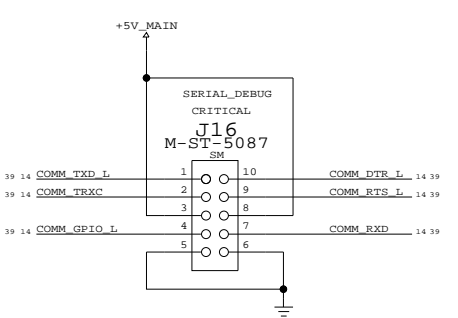
PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

MODEM

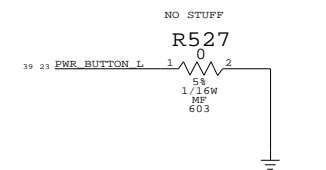
SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM



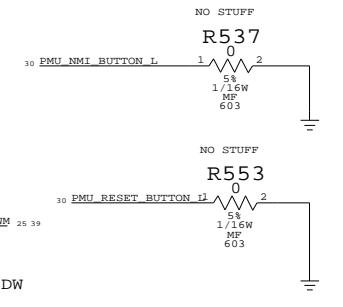
SERIAL DEBUG INTERFACE



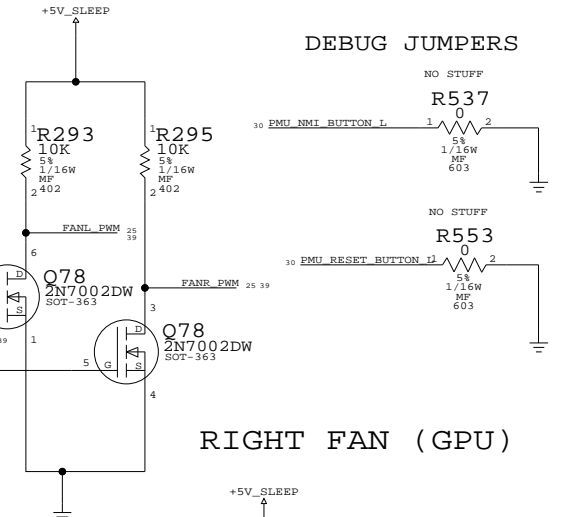
DEBUG POWER BUTTON



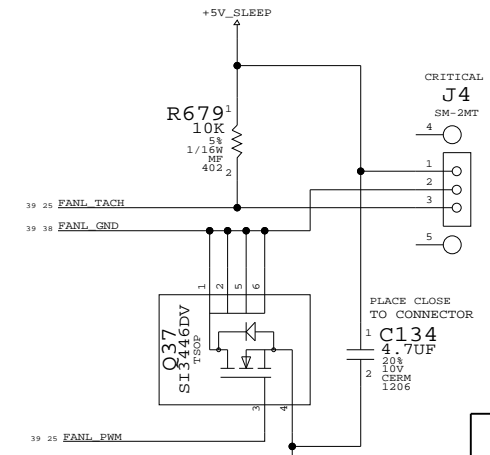
DEBUG JUMPERS



RIGHT FAN (GPU)

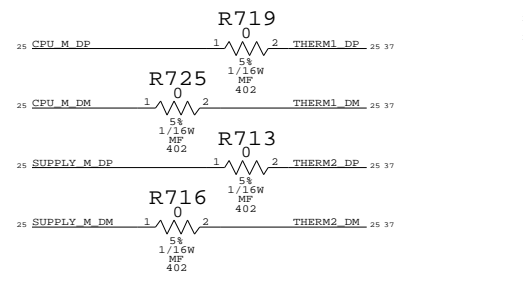


LEFT FAN (CPU)

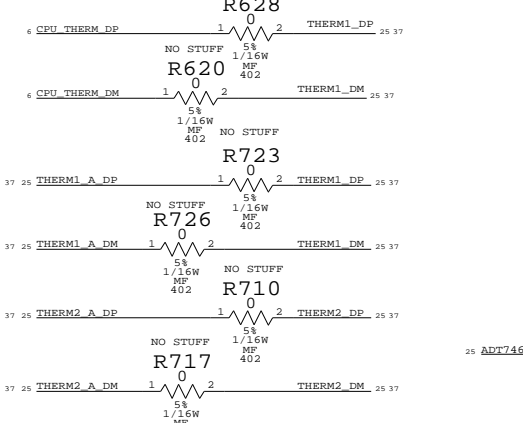


FAN INTERFACE

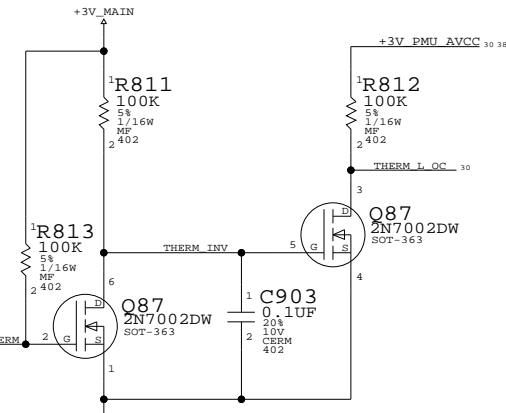
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



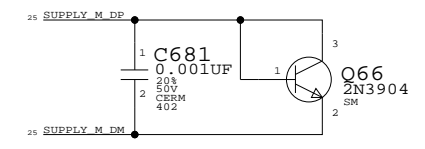
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



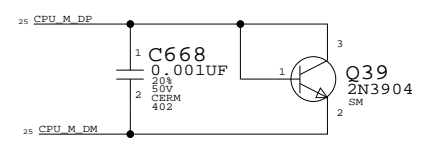
THERM ISOLATION



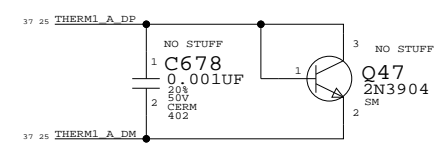
MAIN1



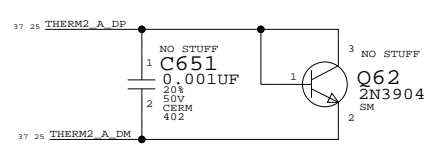
PLACE CLOSE TO CPU MAIN2



PLACE UNDERNEATH UPPER RAM ALTERNATE1



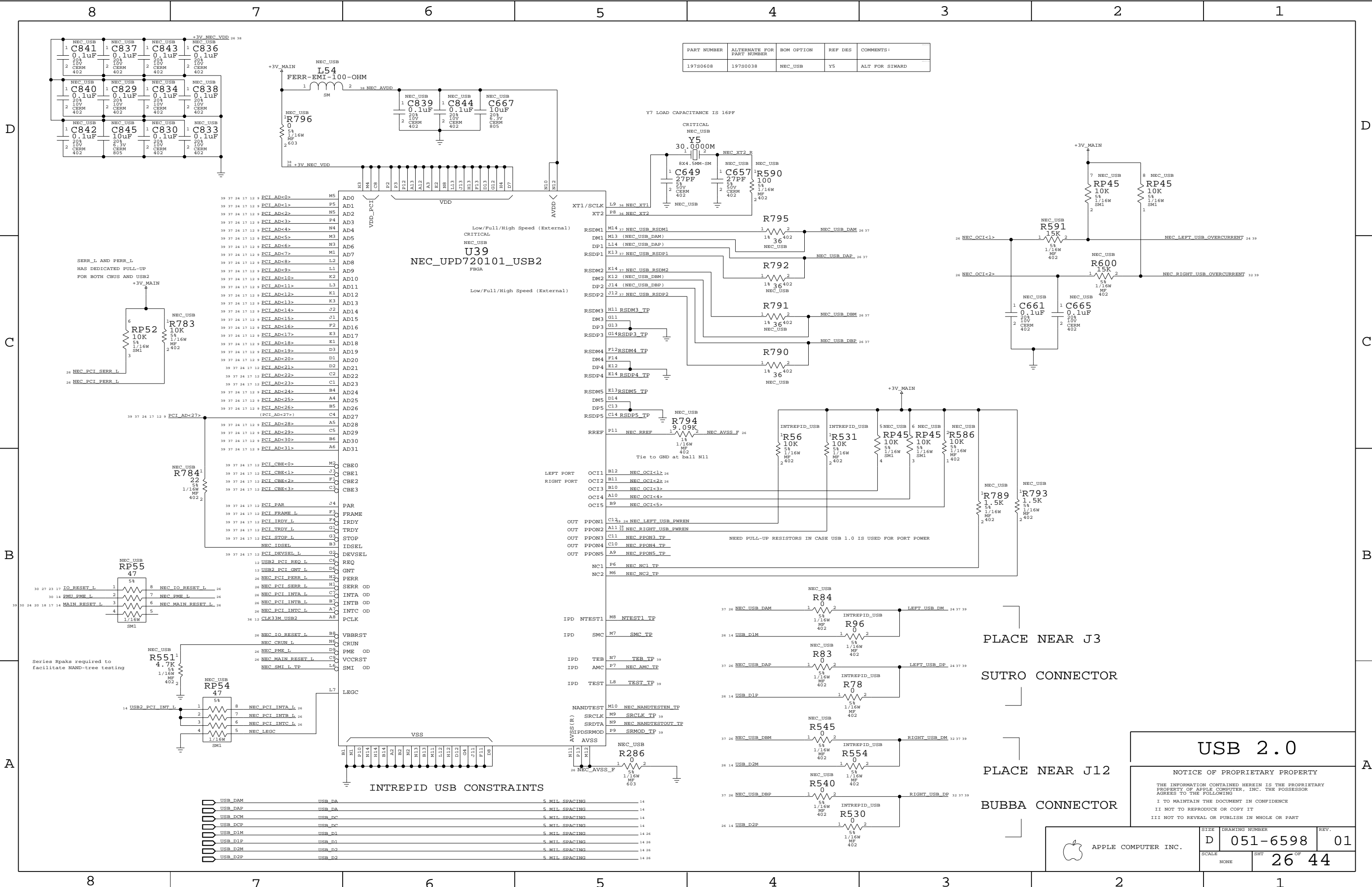
PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2



FAN/MODEM/SOUND/SLEEP LED/DEBUG

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	D	051-6598	01
SCALE	SHT	25 OF 44	
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

INTREPID USB CONSTRAINTS

Signal	Pin	Constraint
USB_DAM	USB_DA	5 MIL SEACING
USB_DAP	USB_DA	5 MIL SEACING
USB_DCM	USB_DC	5 MIL SEACING
USB_DCP	USB_DC	5 MIL SEACING
USB_DIM	USB_D1	5 MIL SEACING
USB_DIP	USB_D1	5 MIL SEACING
USB_D2M	USB_D2	5 MIL SEACING
USB_D2P	USB_D2	5 MIL SEACING

USB 2.0

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APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	26 OF 44	01

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

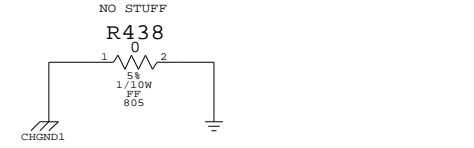
Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

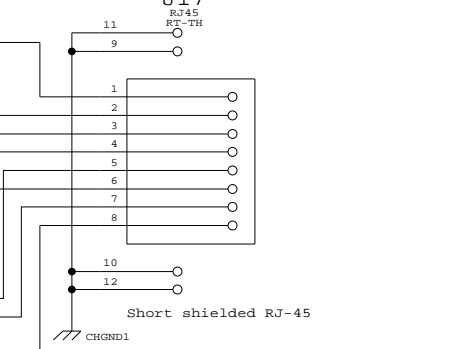
Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE CLOSE TO ETHERNET CONNECTOR



CRITICAL



Short shielded RJ-45

MARVELL 88E1111

10/100/1000 ETHERNET

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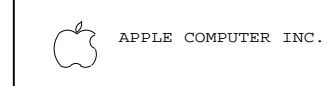
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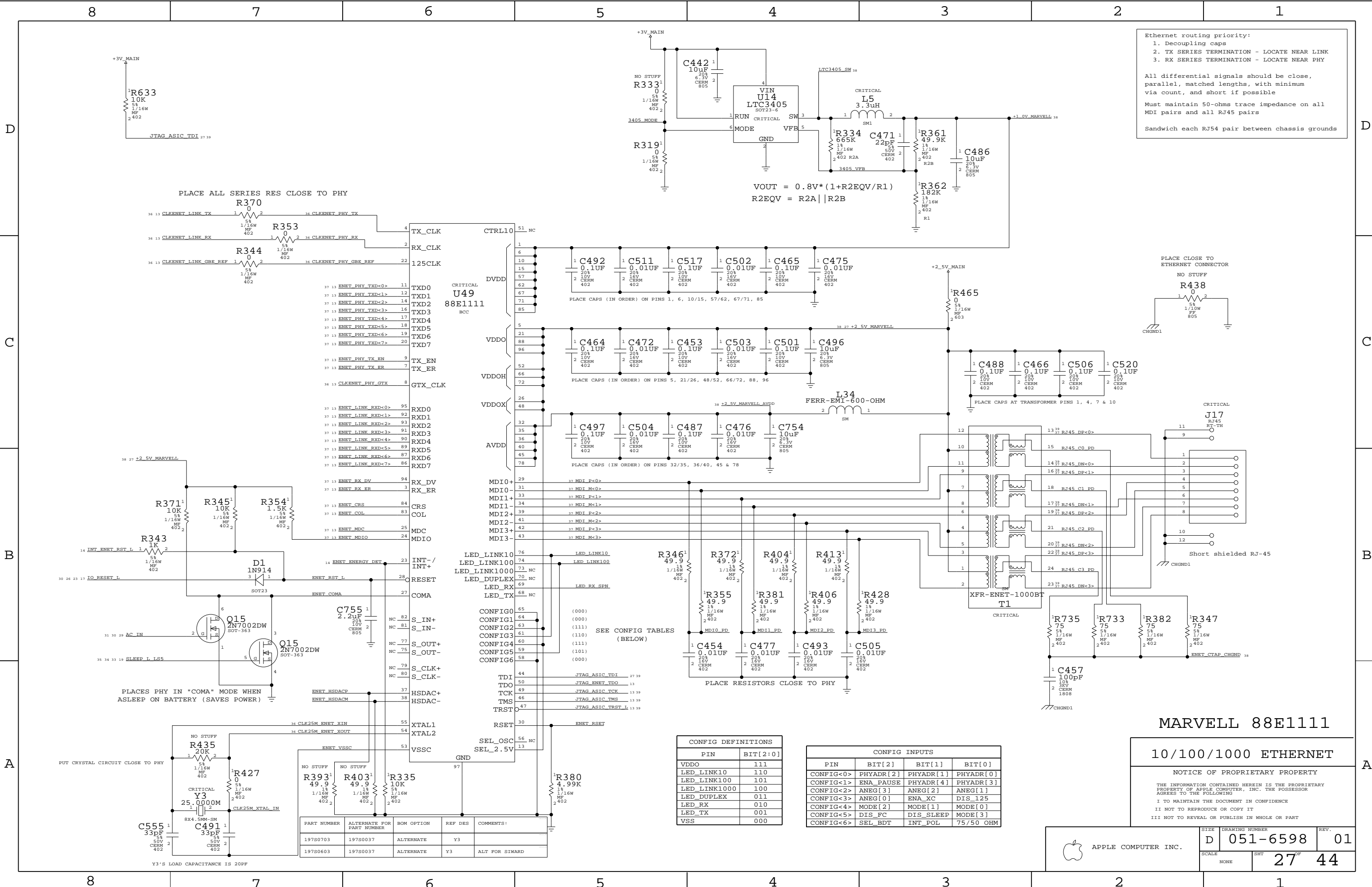
SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE	SHT	
NONE	27	44



CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD



PLACE ALL SERIES RES CLOSE TO PHY

$$V_{OUT} = 0.8V * (1 + R2EQV/R1)$$

$$R2EQV = R2A || R2B$$

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

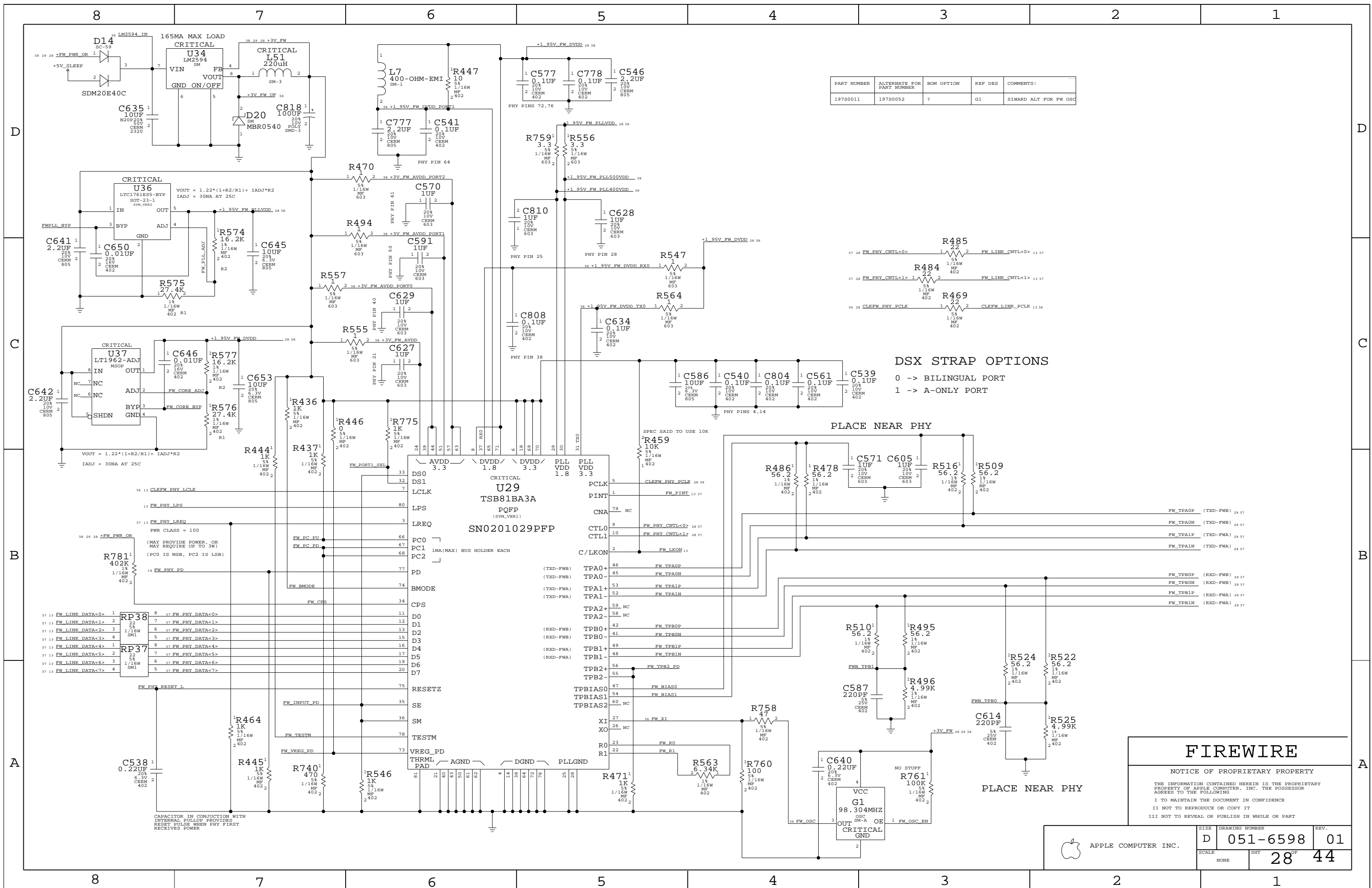
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y3'S LOAD CAPACITANCE IS 20PF



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

- 0 -> BILINGUAL PORT
- 1 -> A-ONLY PORT

FIREWIRE

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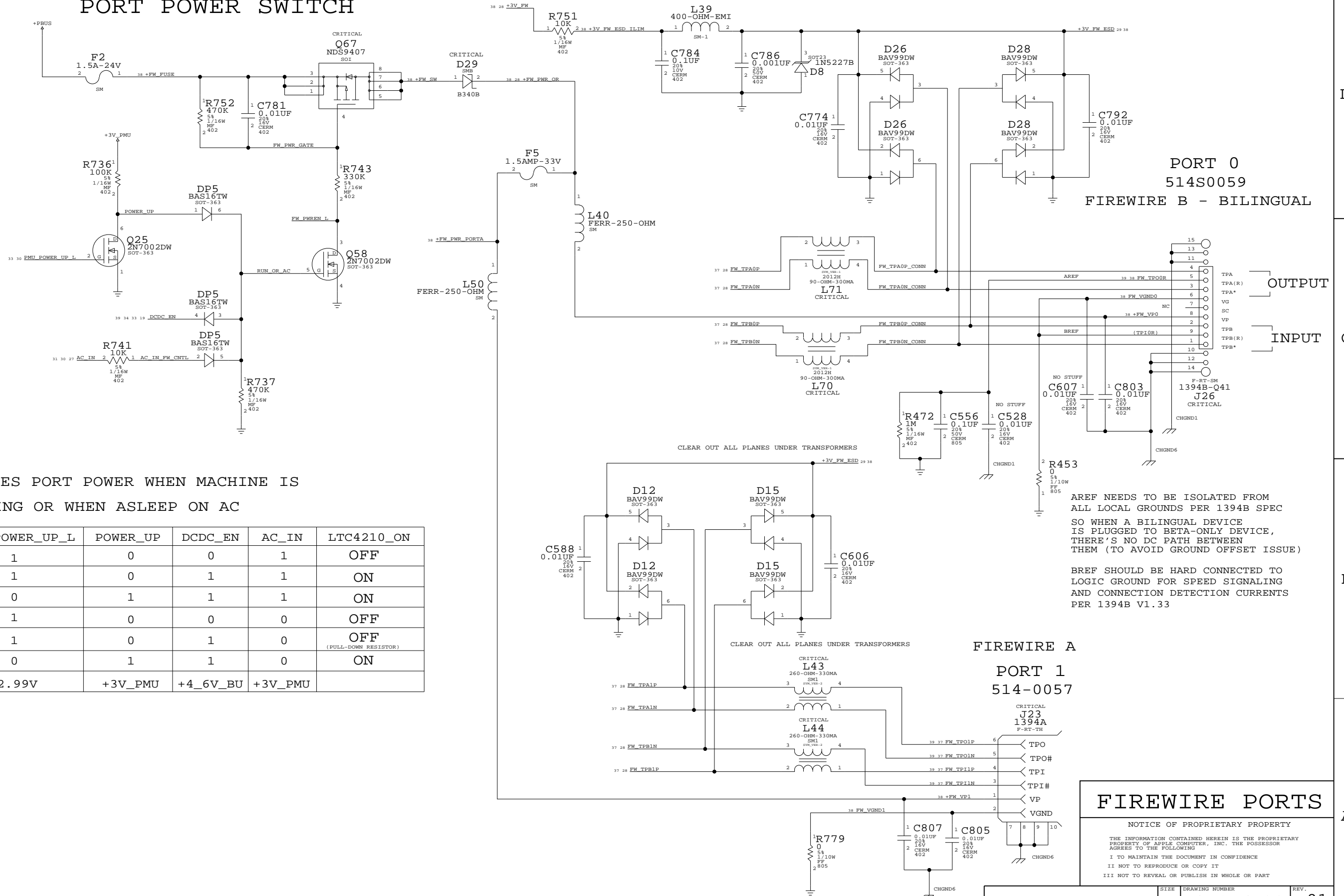
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	DRAWING NUMBER		REV.
	D	051-6598	01
SCALE		SHT	OF
NONE		28	44

PORT POWER SWITCH



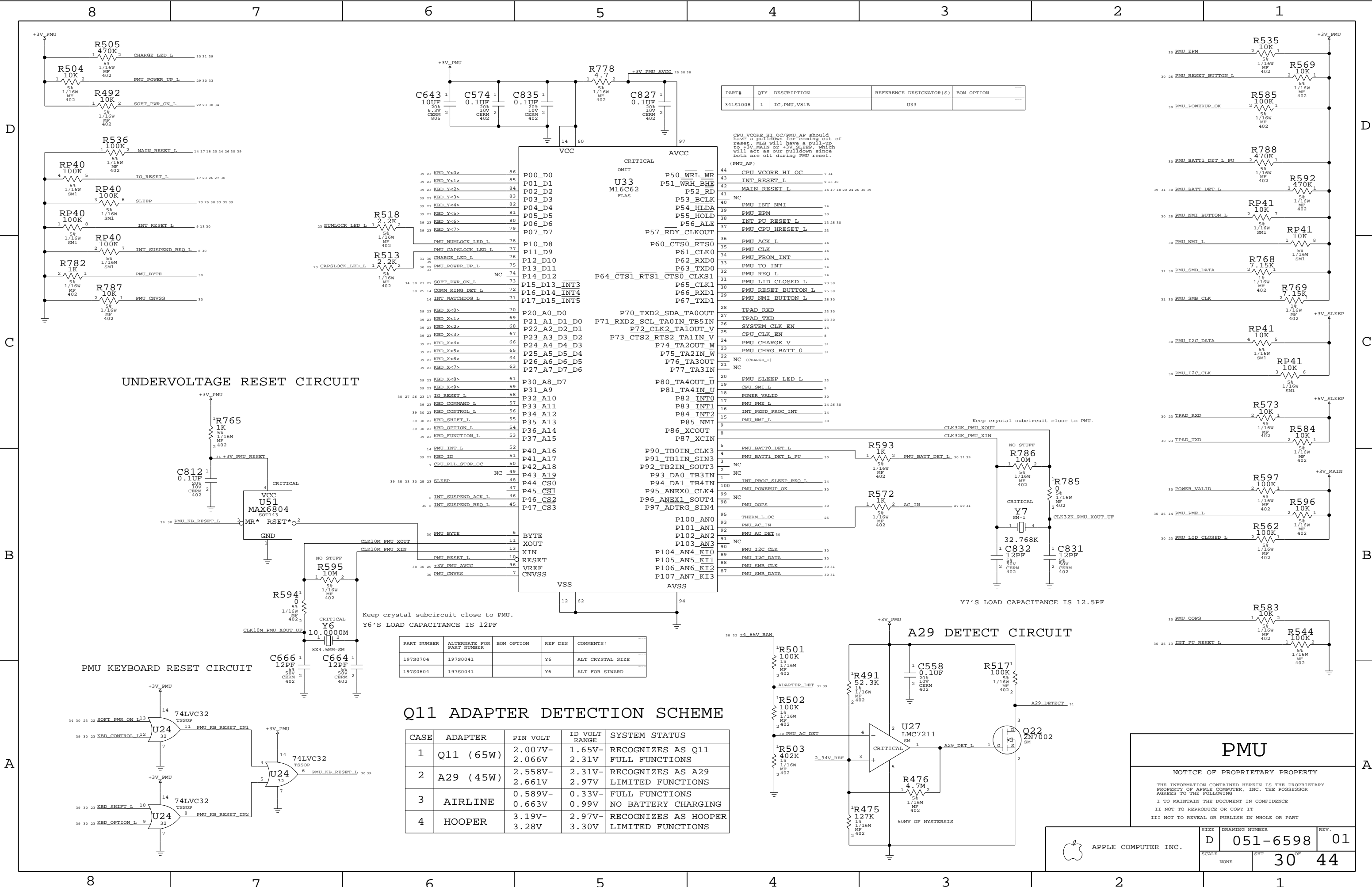
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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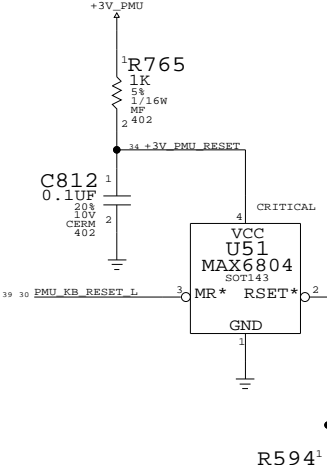
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	NONE	SHT	29 OF 44



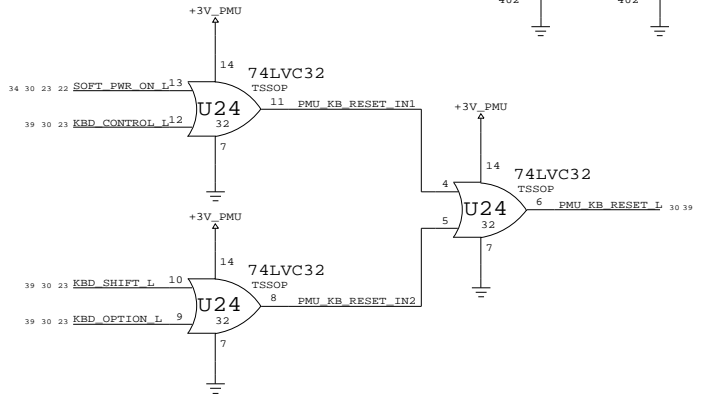
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC, PMU, V81B	U33	

CPU VCORE HI_OC/PMU_AP should have a pullup for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

UNDERVOLTAGE RESET CIRCUIT



PMU KEYBOARD RESET CIRCUIT



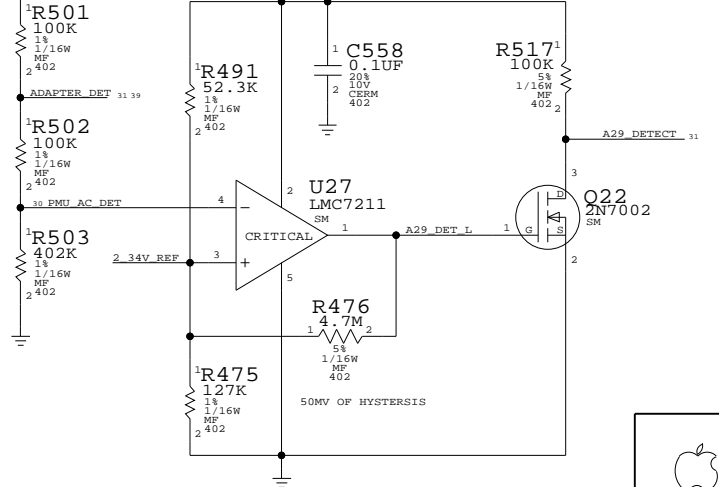
Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT



PMU

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DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

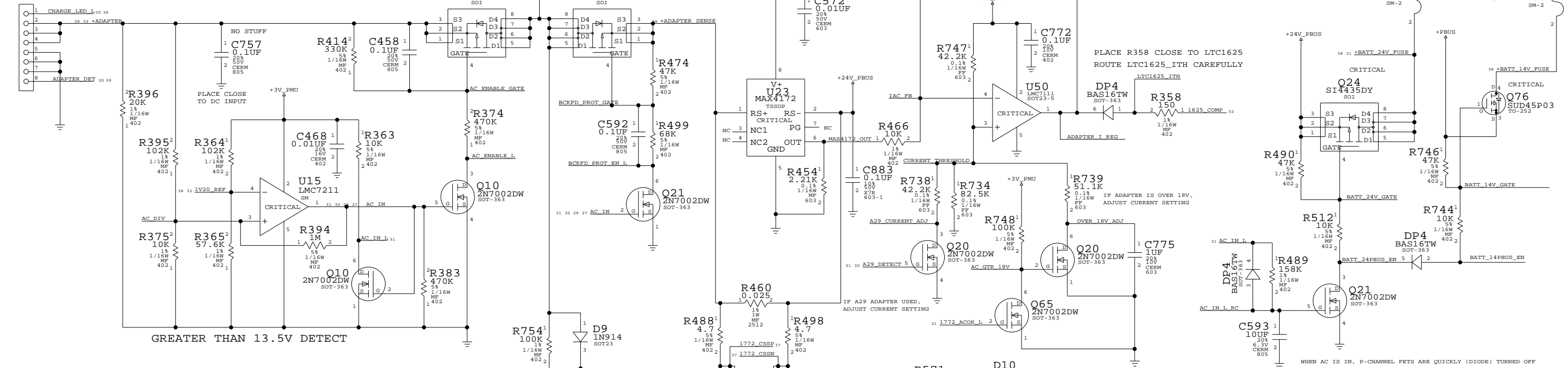
DC INRUSH LIMITER

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

1MSEC INTEGRATION TIME

BATTERY SWITCH-OVER CIRCUIT

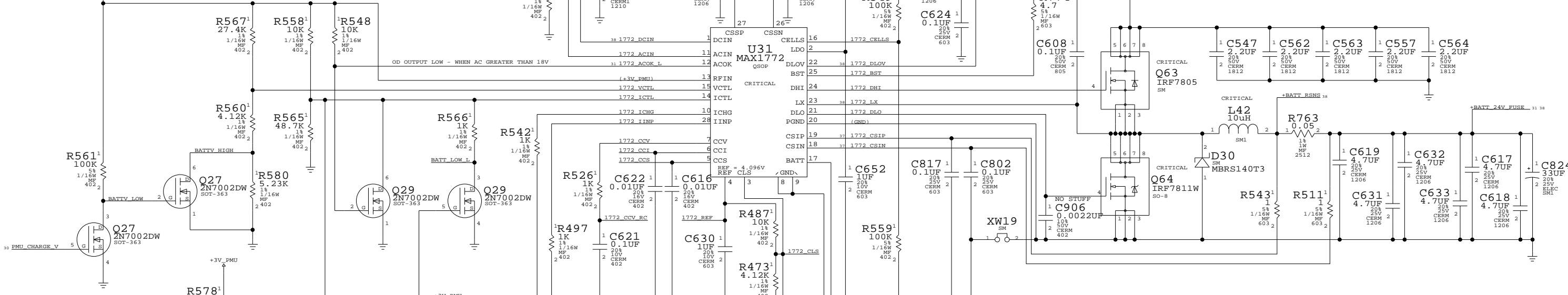


SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE



BATTERY CONNECTOR

J25
87438-0833
M-RT-SM

BATTERY CHARGER

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$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048 / R_{62}) \times (V_{ICL} / V_{REFIN})$$

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6598	01
SCALE	SHT	31 OF 44	
NONE			

D

D

C

C

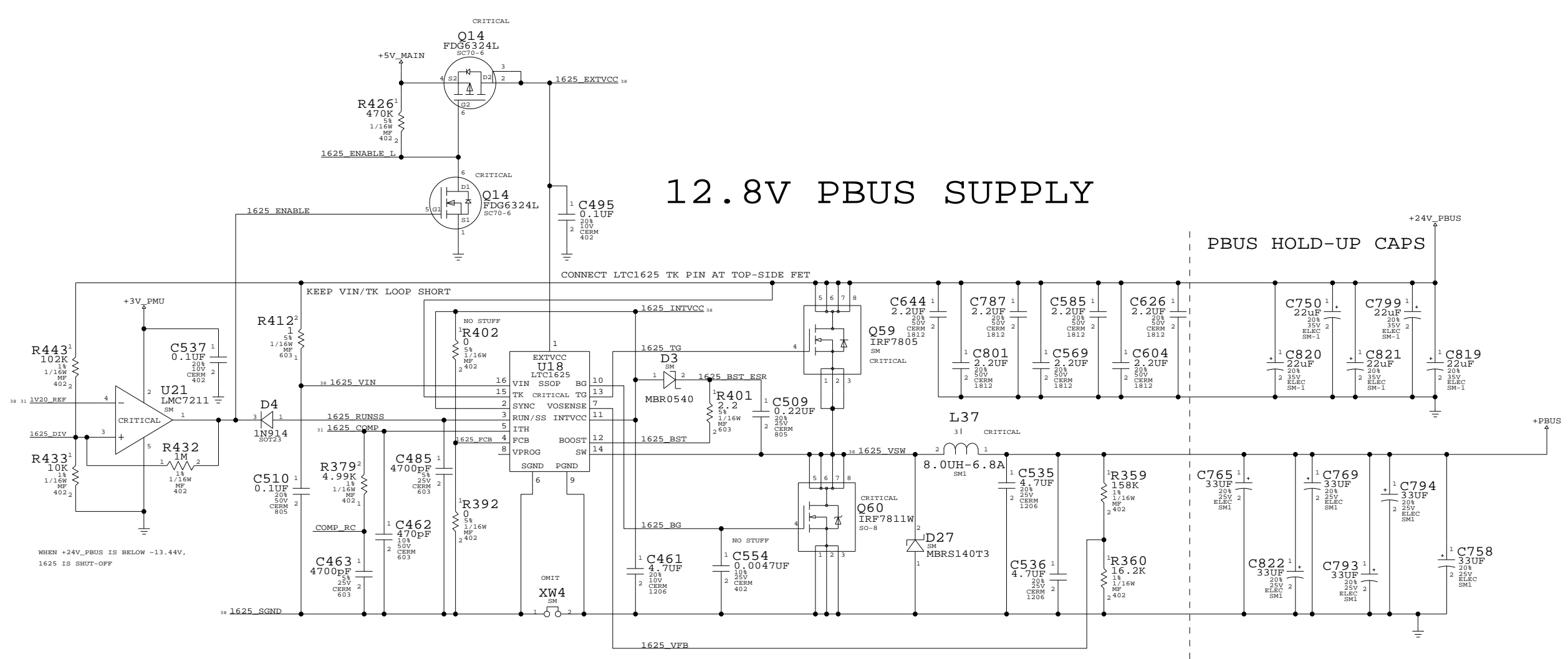
B

B

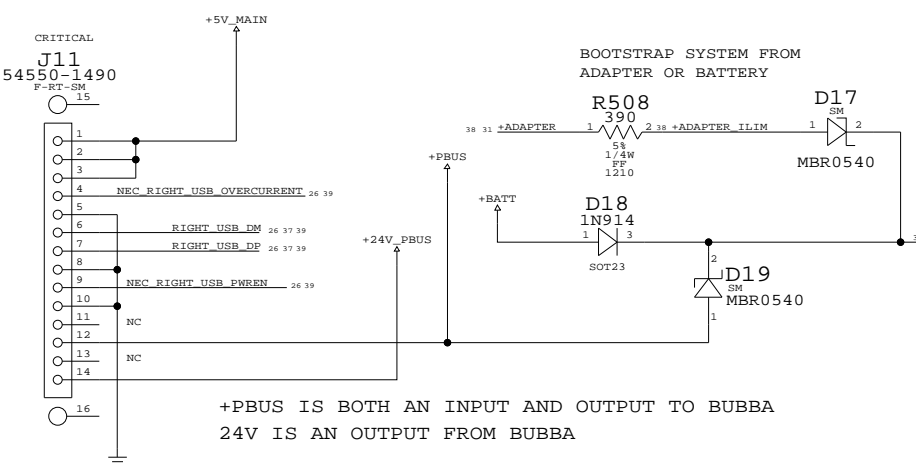
A

A

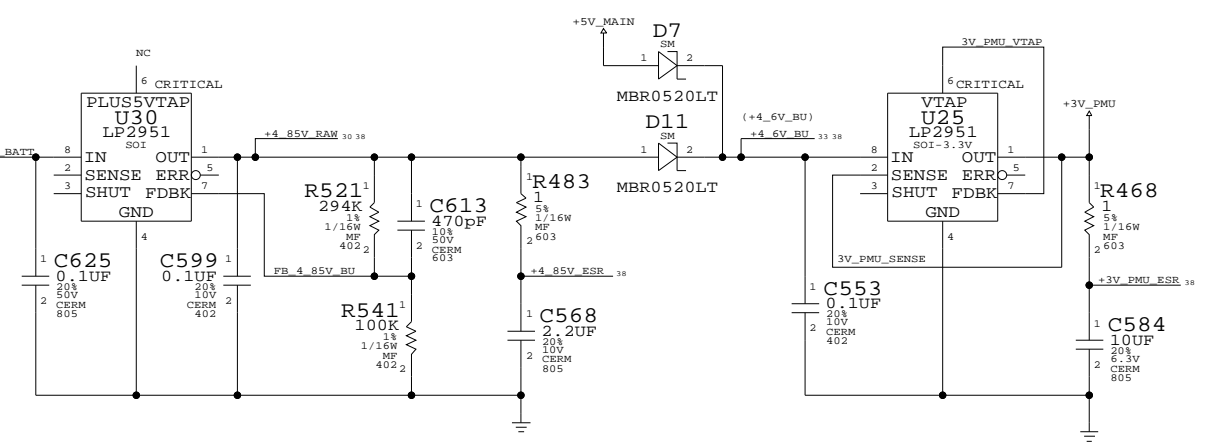
12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY

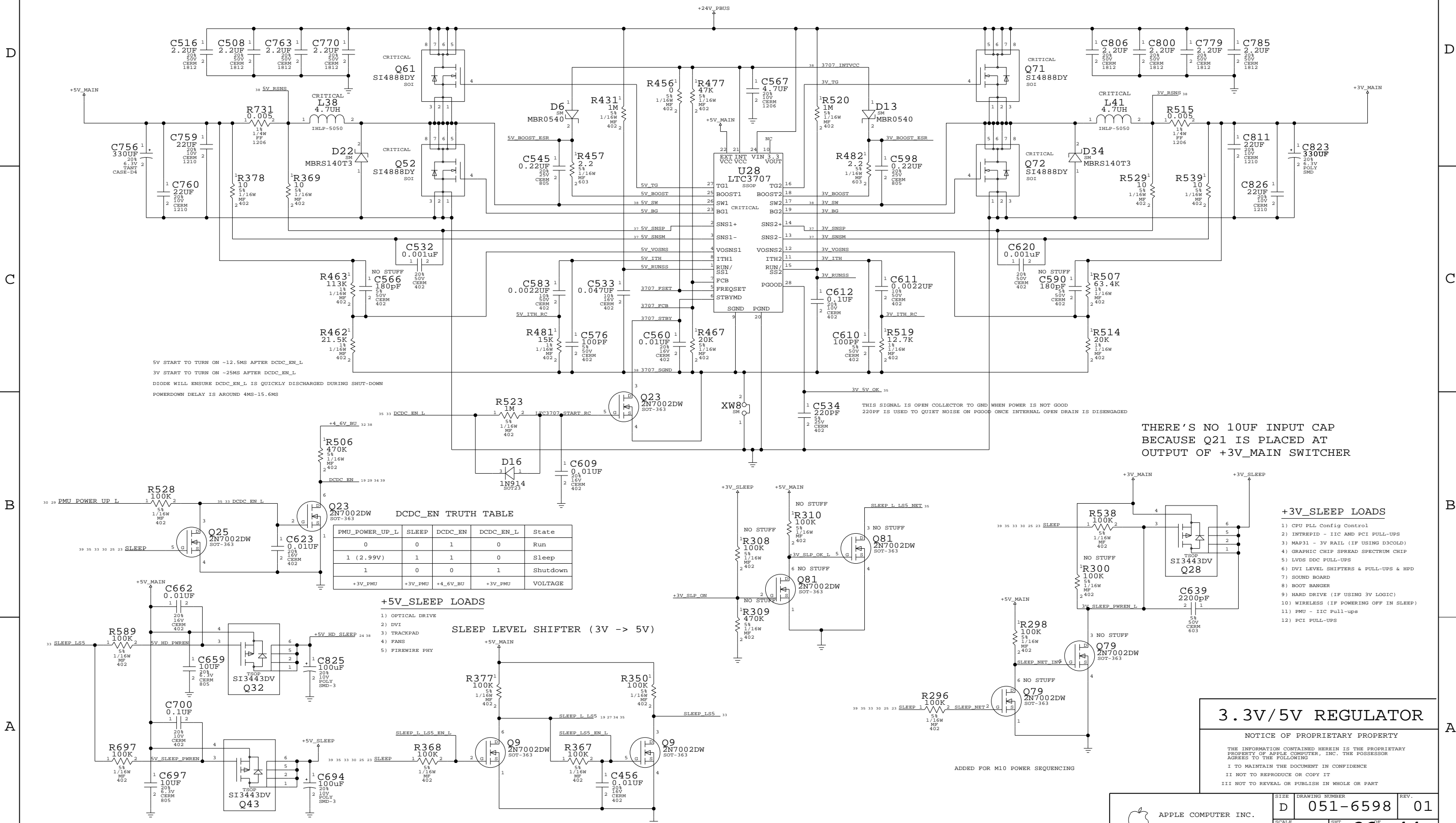


12.8V REGULATOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6598	01
SCALE		SHT	
NONE		32	44

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

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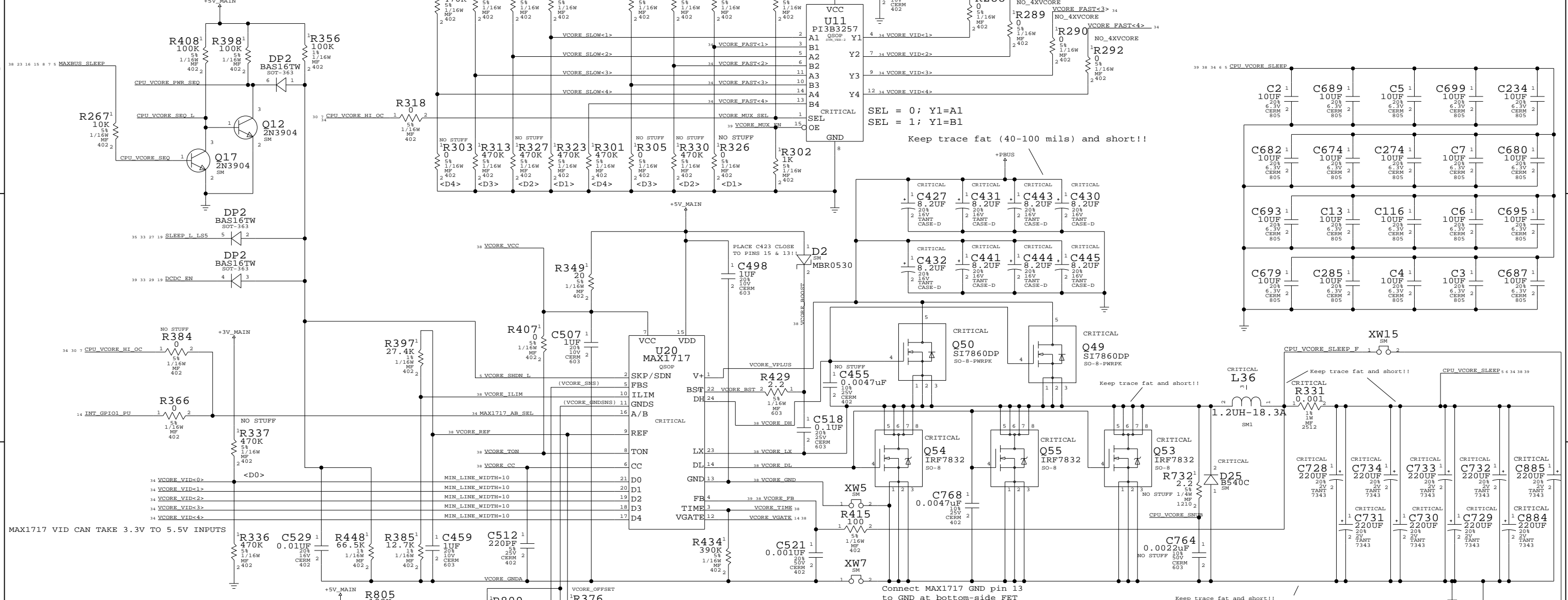
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NONE			

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage (approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V



Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Keep trace fat and short!!

GROUND SENSE VOLTAGE DIVIDER
This allows for an offset to the ground sense to adjust the output voltage.
 $V_{REF} = 2.0V$, HENCE $V_{OFFSET} = 2.0V * (R1/(R1+R2))$ AND $V_{CORE} = V_{DAC} + V_{OFFSET}$.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11484023	1	RESISTOR	R321	?	1_30_VCORE
11486343	1	RESISTOR	R321	?	1_32_VCORE

OUTPUT VOLTAGE

V_{DAC}		D3	D2	D1	D0
D4=0	D4=1				
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

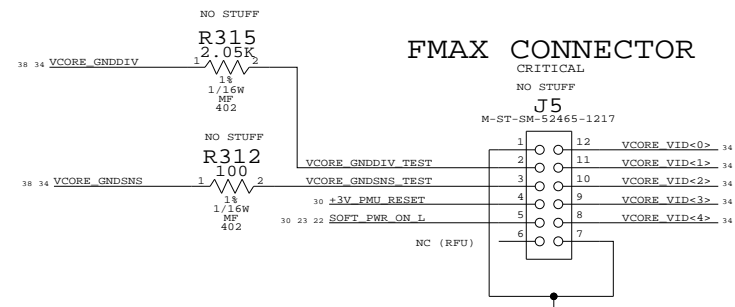
FOR V-STEP:

D<4..0>	A/B_ =	
	Hs/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

FMAX CONNECTOR



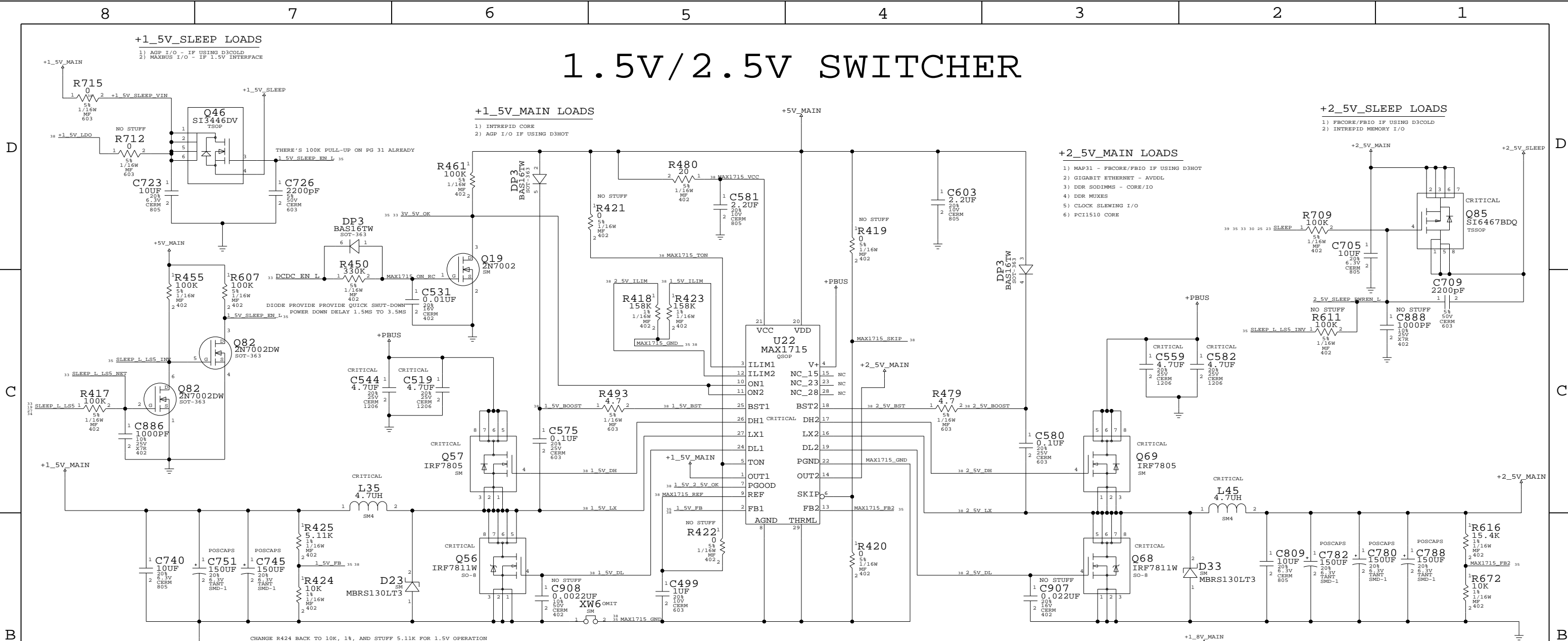
VCORE SUPPLY

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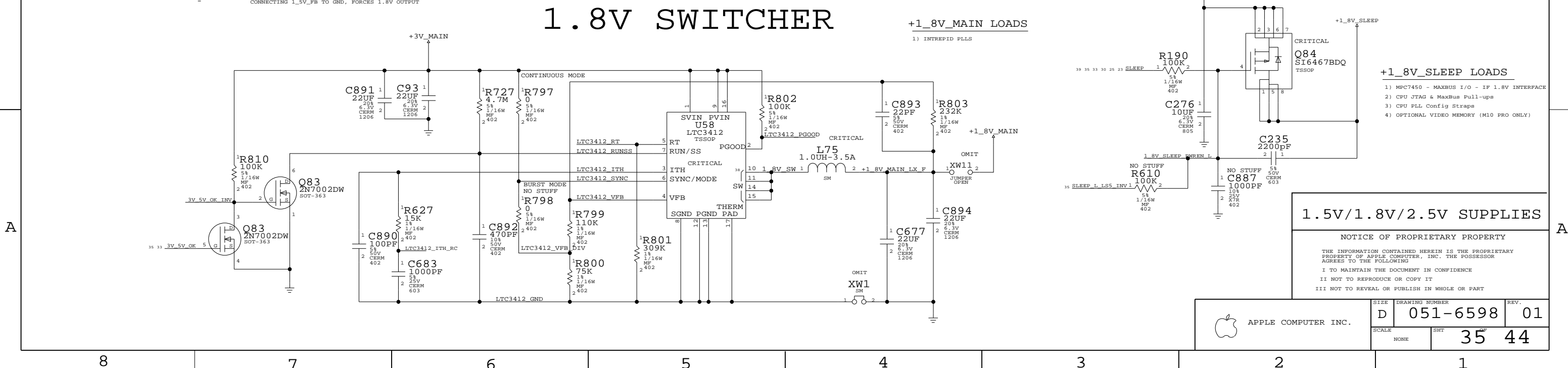
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1.5V/2.5V SWITCHER



1.8V SWITCHER



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NONE			

FUNCTIONAL TEST POINTS

8	7	6	5	4	3	2	1
FUNC_TEST=YES JTAG ASIC TMS 13 27	FUNC_TEST=YES TMS_CONN_CLKP 22 37	FUNC_TEST=YES TV_C 22	FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37	FUNC_TEST=YES PCI_PAR 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37	FUNC_TEST=YES KBD_X<9> 23 30	FUNC_TEST=YES +5V_INV_SW 22 36
FUNC_TEST=YES JTAG ASIC TDI 27	FUNC_TEST=YES VGA_R 22	FUNC_TEST=YES TV_Y 22	FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37	FUNC_TEST=YES KBD_Y<0> 23 30	FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES JTAG ASIC TDO 13 14	FUNC_TEST=YES VGA_G 22	FUNC_TEST=YES TV_COMP 22	FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37	FUNC_TEST=YES KBD_Y<1> 23 30	FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES JTAG ASIC TCK 13 27	FUNC_TEST=YES VGA_B 22	FUNC_TEST=YES SND_TO_AUDIO 14 25	FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37	FUNC_TEST=YES KBD_Y<2> 23 30	FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES JTAG ASIC TRST_L 13 27	FUNC_TEST=YES VGA_VSYNC 22	FUNC_TEST=YES SND_SYNC 14 25	FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37	FUNC_TEST=YES KBD_Y<3> 23 30	FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5	FUNC_TEST=YES VGA_HSYNC 22	FUNC_TEST=YES SND_CLKOUT 14 25 36	FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37	FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24	FUNC_TEST=YES EIDE_OPTICAL_INT 24 37	FUNC_TEST=YES KBD_Y<4> 23 30	FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES CPU_SRESET_L 5	FUNC_TEST=YES DVI_DDC_CLK_UP 22		FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37	FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24	FUNC_TEST=YES TPAD_F_TXD 23	FUNC_TEST=YES KBD_Y<5> 23 30	FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES CPU_HRESET_L 5 7 23	FUNC_TEST=YES DVI_DDC_DATA_UP 22		FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37	FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24	FUNC_TEST=YES TPAD_F_RXD 23	FUNC_TEST=YES KBD_Y<6> 23 30	FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES JTAG_CPU_TMS 5 23	FUNC_TEST=YES DVI_HPD_UP 22	FUNC_TEST=YES INT_AUDIO_TO_SND 14 25	FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37	FUNC_TEST=YES LID_CLOSED_L 23	FUNC_TEST=YES KBD_Y<7> 23 30	FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES JTAG_CPU_TDI 5 23	FUNC_TEST=YES LVDS_L0N 19 22 37	FUNC_TEST=YES SND_SCLK 14 25 36	FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37	FUNC_TEST=YES COMM_RESET_L 14 25	FUNC_TEST=YES KBD_NUMLOCK_LED 23	FUNC_TEST=YES DCDC_EN 19 29 33 34
FUNC_TEST=YES JTAG_CPU_TDO_TP 5	FUNC_TEST=YES LVDS_L0P 19 22 37	FUNC_TEST=YES SND_HW_RESET_L 14 25	FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37	FUNC_TEST=YES COMM_SHUTDOWN 14 25	FUNC_TEST=YES +BATT_POS 31 38	FUNC_TEST=YES BRANG_HRESET_L 23
FUNC_TEST=YES JTAG_CPU_TCK 5 23	FUNC_TEST=YES LVDS_L1N 19 22 37	FUNC_TEST=YES SND_HP_SENSE_L 14 25	FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37	FUNC_TEST=YES COMM_RING_DET_L 14 25 30	FUNC_TEST=YES BATT_CLK 31	FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES JTAG_CPU_TEST_L 5 23 39	FUNC_TEST=YES LVDS_L1P 19 22 37	FUNC_TEST=YES SND_LIN_SENSE_L 14 25	FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37	FUNC_TEST=YES KBD_ID 23 30	FUNC_TEST=YES BATT_DATA 31	FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
	FUNC_TEST=YES LVDS_L2N 19 22 37	FUNC_TEST=YES INT_I2C_DATA2 14 25	FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37	FUNC_TEST=YES +SV_TPAD_SLEEP 23 38	FUNC_TEST=YES BATT_NEG 23 38	FUNC_TEST=YES RF_DISABLE_L_SPN 24
	FUNC_TEST=YES LVDS_L2P 19 22 37	FUNC_TEST=YES INT_I2C_CLK2 14 25	FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37	FUNC_TEST=YES +3V_HALL_EFFECT 23 38	FUNC_TEST=YES PMU_BATT_DET_L 30 31	FUNC_TEST=YES AIRPORT_CLKRUN_L 24
	FUNC_TEST=YES CLKLVDS_IN 19 22 37	FUNC_TEST=YES CHGND4 38	FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37	FUNC_TEST=YES KBD_CAPSLOCK_LED 23	FUNC_TEST=YES FANR_GND 25 38	FUNC_TEST=YES ROM_RW_L 9 12 24
	FUNC_TEST=YES CLKLVDS_LP 19 22 37	FUNC_TEST=YES SLEEP_LED 23 25	FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37	FUNC_TEST=YES KBD_FUNCTION_L 23 30	FUNC_TEST=YES COMM_RTS_L 14 25	FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES INT_I2C_CLK0 11 13 23	FUNC_TEST=YES LVDS_U0N 19 22 37		FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37	FUNC_TEST=YES KBD_CONTROL_L 23 30	FUNC_TEST=YES FANL_GND 25 38	FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES INT_I2C_DATA0 11 13 23	FUNC_TEST=YES LVDS_U0P 19 22 37		FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37	FUNC_TEST=YES KBD_COMMAND_L 23 30	FUNC_TEST=YES FANL_TACH 25	FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES INT_I2C_CLK1 13 14 25	FUNC_TEST=YES LVDS_U1N 19 22 37	FUNC_TEST=YES BT_USB_DM 14 24 37	FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37	FUNC_TEST=YES KBD_OPTION_L 23 30	FUNC_TEST=YES FANR_PWM 25	FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES INT_I2C_DATA1 13 14 25	FUNC_TEST=YES LVDS_U1P 19 22 37	FUNC_TEST=YES BT_USB_DP 14 24 37	FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37	FUNC_TEST=YES KBD_SHIFT_L 23 30	FUNC_TEST=YES FANL_PWM 25	FUNC_TEST=YES ROM_0E_L 9 12 24
FUNC_TEST=YES CBUS_DET_1_L 17	FUNC_TEST=YES LVDS_U2N 19 22 37	FUNC_TEST=YES MODEM_USB_DM 14 25 37	FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37	FUNC_TEST=YES KBD_X<0> 23 30	FUNC_TEST=YES RJ45_DP<0> 27 37	FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES CBUS_DET_2_L 17	FUNC_TEST=YES LVDS_U2P 19 22 37	FUNC_TEST=YES MODEM_USB_DP 14 25 37	FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37	FUNC_TEST=YES KBD_X<1> 23 30	FUNC_TEST=YES RJ45_DP<1> 27 37	FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES TMS_DN<0> 20 22 37	FUNC_TEST=YES CLKLVDS_UN 19 22 37	FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37	FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37	FUNC_TEST=YES KBD_X<2> 23 30	FUNC_TEST=YES RJ45_DN<0> 27 37	FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES TMS_DP<0> 20 22 37	FUNC_TEST=YES CLKLVDS_UP 19 22 37	FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37	FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37	FUNC_TEST=YES KBD_X<3> 23 30	FUNC_TEST=YES RJ45_DP<2> 27 37	FUNC_TEST=YES CPU_VCORE_SLEEP 6 6 34 38
FUNC_TEST=YES TMS_DN<1> 20 22 37	FUNC_TEST=YES LVDS_DDC_CLK 19 22	FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37	FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37	FUNC_TEST=YES KBD_X<4> 23 30	FUNC_TEST=YES RJ45_DN<2> 27 37	FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES TMS_DP<1> 20 22 37	FUNC_TEST=YES LVDS_DDC_DATA 19 22	FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37	FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DMA_ACK_L 24 37	FUNC_TEST=YES KBD_X<5> 23 30	FUNC_TEST=YES RJ45_DP<3> 27 37	FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES TMS_DN<2> 20 22 37	FUNC_TEST=YES BRIGHT_PWM 22	FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37	FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37	FUNC_TEST=YES KBD_X<6> 23 30	FUNC_TEST=YES RJ45_DN<3> 27 37	FUNC_TEST=YES MOD_DTD 14 25
FUNC_TEST=YES TMS_DP<2> 20 22 37	FUNC_TEST=YES TV_GND1 22 38	FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37	FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37	FUNC_TEST=YES KBD_X<7> 23 30	FUNC_TEST=YES RJ45_DP<4> 27 37	FUNC_TEST=YES +1.8V_MAIN 38
FUNC_TEST=YES TMS_CONN_CLKN 22 37	FUNC_TEST=YES TV_GND2 22 38	FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37	FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37	FUNC_TEST=YES KBD_X<8> 23 30	FUNC_TEST=YES RJ45_DN<4> 27 37	FUNC_TEST=YES +3V_PMU 38
				FUNC_TEST=YES SND AMP MUTE 25	FUNC_TEST=YES SRCLK_TP 26	FUNC_TEST=YES RJ45_DP<5> 27 37	FUNC_TEST=YES SLEEP 23 25 30 33 35
				FUNC_TEST=YES SND_HP_MUTE_INV 25	FUNC_TEST=YES SRMOD_TP 26	FUNC_TEST=YES RJ45_DN<5> 27 37	FUNC_TEST=YES +5V_DDC_SLEEP 22 38
					FUNC_TEST=YES TEB_TP 26	FUNC_TEST=YES RJ45_DP<6> 27 37	FUNC_TEST=YES +12.8V_INV 22 38
					FUNC_TEST=YES TEST_TP 26	FUNC_TEST=YES VCORE_VID0	FUNC_TEST=YES VCORE_MUX_EN 34
						FUNC_TEST=YES VCORE_VID1	
						FUNC_TEST=YES VCORE_VID2	
						FUNC_TEST=YES VCORE_VID3	
						FUNC_TEST=YES VCORE_VID4	

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8

7

6

5

4

3

2

1

REVISION HISTORY

12/11/03

- 1) IMPORTED 041 PRODUCTION RELEASE SCHEMATIC
- 2) CHANGED CPU (U43) TO A7PM
- 3) CHANGED PLL CONFIG STEERING FOR NEW CPU
- 4) CHANGED U44 TO M1-SC854 SYMBOL
- 5) ADDED CPU_AVDD_LDO (U6)
- 6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
- 7) ADDED R608 TO DISCONNECT INT_GPIOD FROM OC_FSEL
- 8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
- 9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

- 10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
- 11) CHANGED PIN 11 OF J11 TO NC

12/16/03

- 12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
- 13) CHANGED CPU_TEMP_DM TO CPU_TEMP_DM
- 14) CHANGED CPU_TEMP_DP TO CPU_TEMP_DP
- 15) CHANGED GPU_TEMP_DP TO GPU_TEMP_DP_TP
- 16) CHANGED GPU_TEMP_DM TO GPU_TEMP_DM_TP
- 19) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

- 18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
- 19) UPDATE DIFF NET SPACING TIE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
- 20) CHANGED FIREWIRE_OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

- 21) CHANGED MAX VIA COUNT ON ALL AGP_STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

D

D

C

C

B

B

A

A


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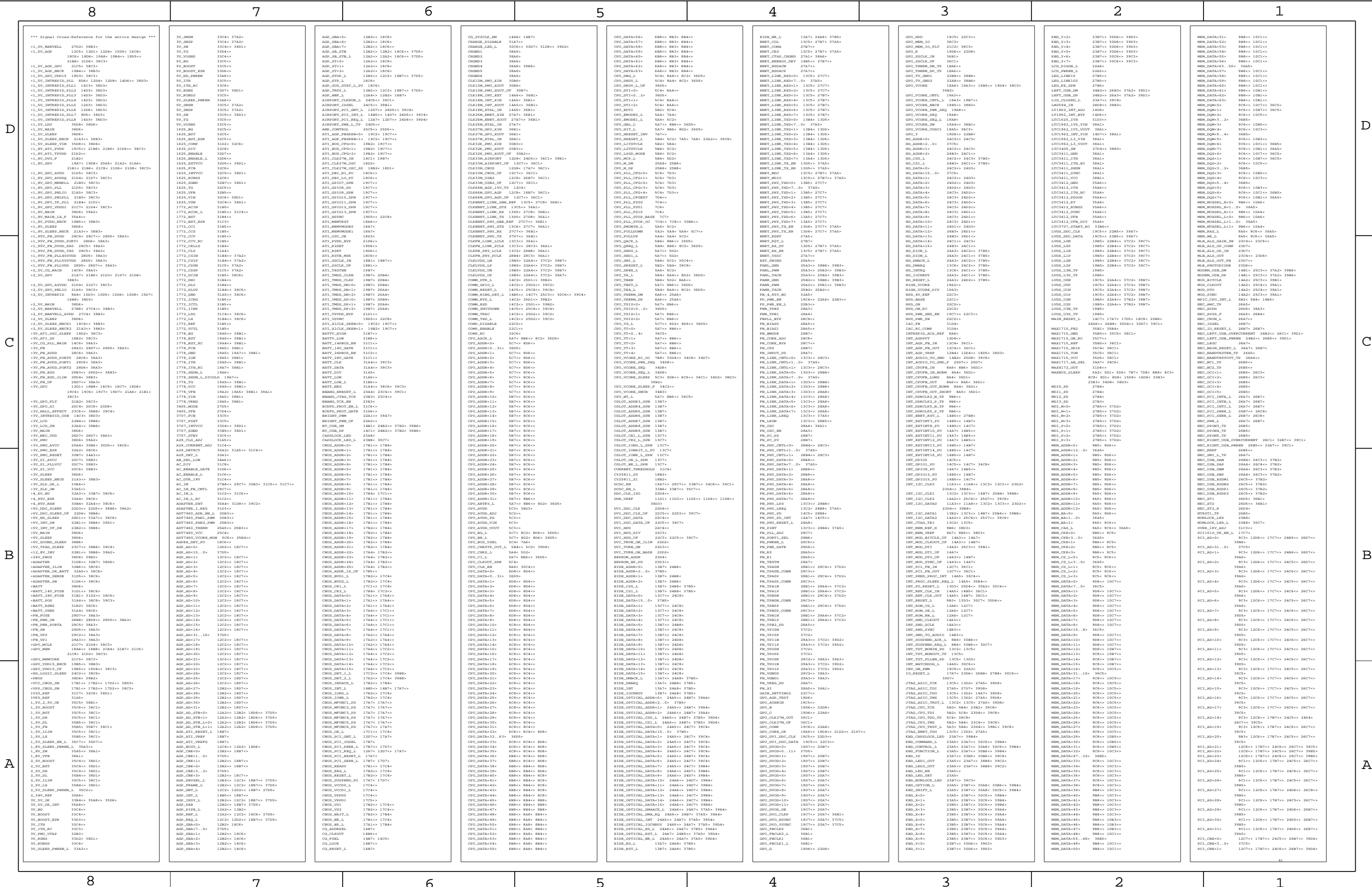
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4

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1



D

C


B

A

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A

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