

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

|     |            |                         |            |
|-----|------------|-------------------------|------------|
| REV | ECN        | DESCRIPTION OF REVISION | CK APPD    |
| C   | 0000813234 | PRODUCTION RELEASED     | 2009-11-01 |

# K84 MLB SCHEMATIC

## PROD OK2FAB 11/01/2009

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| 30   | X16 WIRELESS CONNECTOR       | K24_MLB 01/27/2009 |
| 31   | Ethernet PHY (RTL8211CL)     | K24_MLB 04/06/2009 |
| 32   | Ethernet & AirPort Support   | K24_MLB 04/06/2009 |
| 33   | ETHERNET CONNECTOR           | K24_MLB 04/06/2009 |
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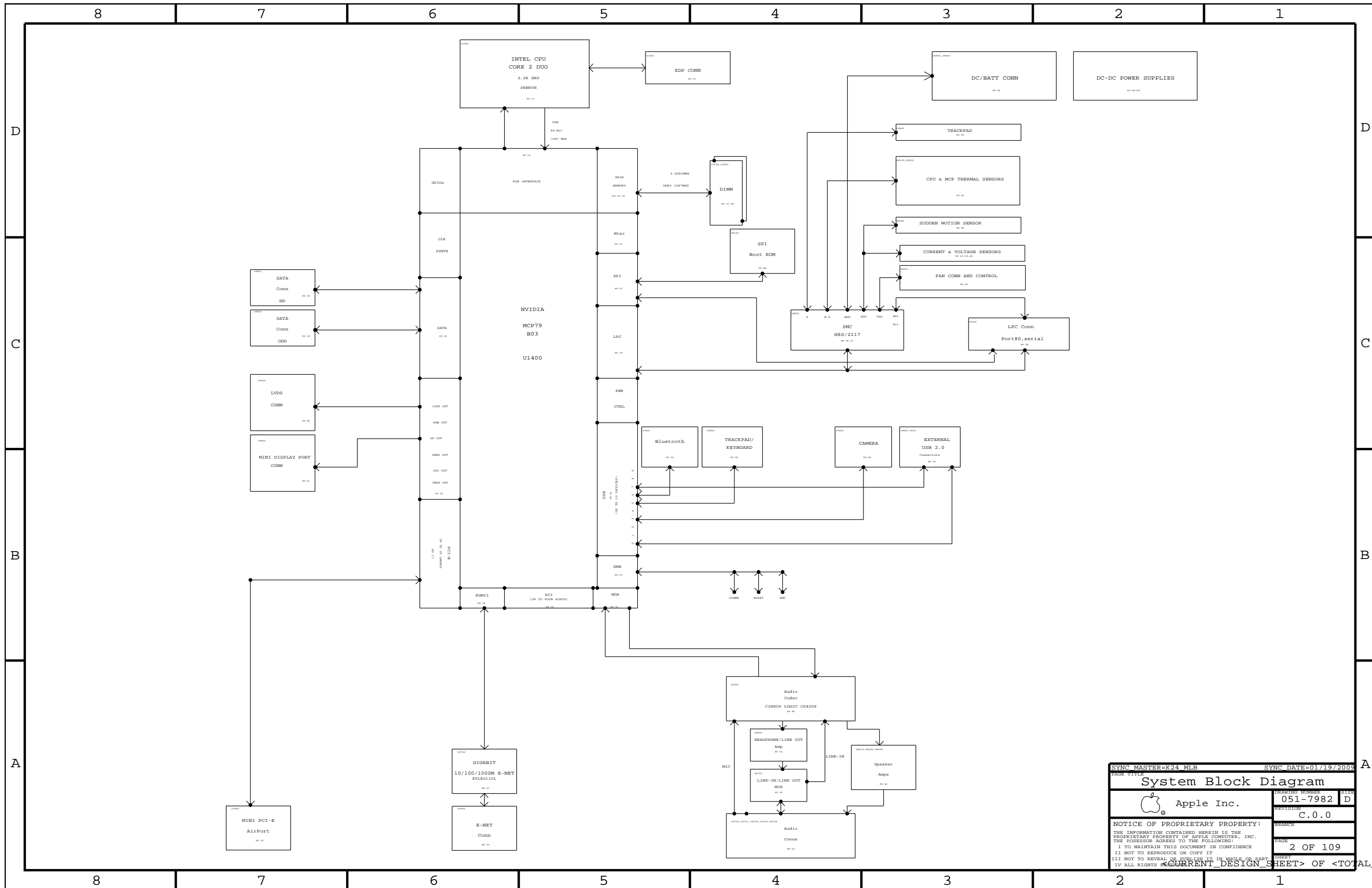
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| 57   | 5V/3.3V SUPPLY                 | K24_MLB 02/05/2009     |
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Schematic / PCB #'s

| PART NUMBER | QTY | DESCRIPTION   | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------|---------------|----------|------------|
| 051-7982    | 1   | SCHEM_MLB_K84 | SCM           | CRITICAL |            |
| 820-2567    | 1   | PCBP_MLB_K84  | PCB           | CRITICAL |            |

|   |                |               |        |
|---|----------------|---------------|--------|
| DRAWING TITLE   |                | SCHEM,MLB,K84 |        |
| Apple Inc.  | DRAWING NUMBER | 051-7982      | SIZE D |
|   | REVISION       | C.0.0         |        |
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|   |  |                                   |  |
|---|--|-----------------------------------|--|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=01/19/2009              |  |
| <b>System Block Diagram</b>   |  |                                   |  |
|   |  | DRAWING NUMBER<br><b>051-7982</b> | SHEET<br><b>D</b>                          |
|   |  | REVISION<br><b>C.0.0</b>          |  |
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**BOM Variants**

| BOM NUMBER | BOM NAME                      | BOM OPTIONS                                    |
|------------|-------------------------------|--|
| 639-0035   | PCBA_MLB_FOX_DDR_CONN_K84     | K84_COMMON_CPU_2_0GHZ_FOX_DDR_CONN_EEE_B0G     |
| 639-0254   | PCBA_MLB_MLX_DDR_CONN_K84     | K84_COMMON_CPU_2_0GHZ_MLX_DDR_CONN_EEE_A36     |
| 085-0748   | K84_MLB_DEVELOPMENT_BOM       | K84_DEVEL_BOM                                  |
| 639-0554   | PCBA_MLB_FOX_DDR_CONN_PVT_K84 | K84_COMMON_PVT_CPU_2_0GHZ_FOX_DDR_CONN_EEE_CXR |
| 639-0555   | PCBA_MLB_MLX_DDR_CONN_PVT_K84 | K84_COMMON_PVT_CPU_2_0GHZ_MLX_DDR_CONN_EEE_CV1 |
| 085-1076   | K84_MLB_DEVELOPMENT_PVT       | K84_DEVEL_PVT                                  |

**Bar Code Labels / EEE #'s**

| PART NUMBER | QTY | DESCRIPTION                     | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------------------|---------------|----------|------------|
| 826-4393    | 1   | LABEL_P/N LABEL_PCB_20MM X 6 MM | [EEE:B0G]     | CRITICAL | EEE_B0G    |
| 826-4393    | 1   | LABEL_P/N LABEL_PCB_20MM X 6 MM | [EEE:A36]     | CRITICAL | EEE_A36    |
| 826-4393    | 1   | LABEL_P/N LABEL_PCB_20MM X 6 MM | [EEE:CXR]     | CRITICAL | EEE_CXR    |
| 826-4393    | 1   | LABEL_P/N LABEL_PCB_20MM X 6 MM | [EEE:CV1]     | CRITICAL | EEE_CV1    |

**BOM Groups**

| BOM GROUP      | BOM OPTIONS  |
|----------------|--|
| K84_COMMON     | COMMON.ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_PROD,K84_PRODPARTS                                       |
| K84_COMMON_PVT | COMMON.ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_PROD,K84_PRODPARTS                                       |
| K84_MCP        | MCP_B03,BOOT_MODE_USER,MCPREQ_SMC  |
| K84_MISC       | ONWIRE_FU_DP_ESD,MIKEY_LDO_NO_MEM_SENSE,1P08_HIGH_SIDE_SENSE,MCP_T_DIODE_SENSOR,MCP_SMC_DIGITEMP_YES |
| K84_PRODPARTS  | BOOTROM_PROD_SMC_PROD,WELLSRING_PROD   |
| K84_DEBUG_PROD | DEVEL_BOM_SMC_DEBUG_YES,XDP  |
| K84_DEBUG_PVT  | DEVEL_BOM_PVT_SMC_DEBUG_YES,XDP_NO_VREFMIGN  |
| K84_DEBUG_PROD | SMC_DEBUG_YES,XDP,LPCPLUS_NOT_NO_VREFMIGN  |
| K84_DEVEL_PROD | DEBUG_ADC_XDP_CONN,LPCPLUS,VREFMIGN  |
| K84_DEVEL_PVT  | XDP_CONN,LPCPLUS   |

**Module Parts**

| PART NUMBER | QTY | DESCRIPTION                             | REFERENCE DES                      | CRITICAL | BOM OPTION   |
|-------------|-----|---|------------------------------------|----------|--------------|
| 33783769    | 1   | CPU_020V_2.0GHZ_1000_90_90_90A_97086    | U1000                              | CRITICAL | CPU_2_0GHZ   |
| 33880710    | 1   | IC_SMC_MCP79_353398M_80A1477_803        | U1400                              | CRITICAL | MCP_B03      |
| 51680706    | 1   | CONN_204P_S0029M_SOCKET_DDR3_SAM_80A    | J3200                              | CRITICAL | FOX_DDR_CONN |
| 516-0201    | 1   | CONN_204P_S0029M_P+G_08M                | J3100                              | CRITICAL | FOX_DDR_CONN |
| 51680790    | 1   | CONN_204P_S0029M_SOCKET_DDR3_SAM_80M/IC | J3200                              | CRITICAL | MLX_DDR_CONN |
| 516-0213    | 1   | CONN_204P_S0029M_P+G_08M_8P             | J3100                              | CRITICAL | MLX_DDR_CONN |
| 452-1708    | 4   | SCR_N3_030_1308_0.04_0.04_0.3_MLX_187   | SCREW1,SCREW2,SCREW3,SCREW4        | CRITICAL |              |
| 514-0704    | 1   | CONN_S0PT_RJ45_PLASTIC_WF_E83/E84       | J3900                              | CRITICAL |              |
| 514-0705    | 2   | CONN_S0PT_USB_4P_PLASTIC_WF_E83/E84     | J4600,J4610                        | CRITICAL |              |
| 514-0706    | 1   | CONN_S0PT_MINI_DP_PLASTIC_WF_E83/E84    | J9400                              | CRITICAL |              |
| 514-0718    | 1   | CONN_S0PT_5_P01P_TX_RX_SF_CPL_E83/E84   | J6700                              | CRITICAL |              |
| 35382718    | 1   | IC_16L88042_4X_9_W0878_2_78/2_88V_T0988 | U7870                              | CRITICAL |              |
| 870-1885    | 4   | POSD_P18_MED_M018-IMPROVED_K84          | Z80900,Z80901,Z80902,Z80903        | CRITICAL |              |
| 870-1885    | 3   | POSD_P18_MED_M018-IMPROVED_K84          | Z80908,Z80909,Z80911               | CRITICAL |              |
| 870-1886    | 5   | POSD_P18_TALL_M018-IMPROVED_K84         | Z80904,Z80905,Z80906,Z80907,Z80910 | CRITICAL |              |
| 870-1886    | 5   | POSD_P18_TALL_M018-IMPROVED_K84         | Z80912,Z80913,Z80914,Z80915,Z80919 | CRITICAL |              |
| 870-1887    | 3   | POSD_P18_THIN_M018-IMPROVED_K84         | Z80917,Z80918,Z80916               | CRITICAL |              |
| 10480033    | 4   | RES_SF_1/4W_5_R03M_51_0805_080          | R6612,R6617,R6630,R6633            | CRITICAL |              |
| 51880774    | 1   | CONN_S0PT_60P_P+G_4_02M_WF_1.0          | J1300                              | CRITICAL | XDP_CONN     |

35382718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE  
 514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR  
 514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS  
 514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR  
 514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

**DEVELOPMENT BOM**

| PART NUMBER | QTY | DESCRIPTION             | REFERENCE DES | CRITICAL | BOM OPTION    |
|-------------|-----|-------------------------|---------------|----------|---------------|
| 085-0748    | 1   | K84_MLB_DEVELOPMENT_BOM | DEVEL         | CRITICAL | DEVEL_BOM     |
| 085-1076    | 1   | K84_MLB_DEVELOPMENT_PVT | DEVEL_PVT     | CRITICAL | DEVEL_BOM_PVT |

**Programmable Parts**

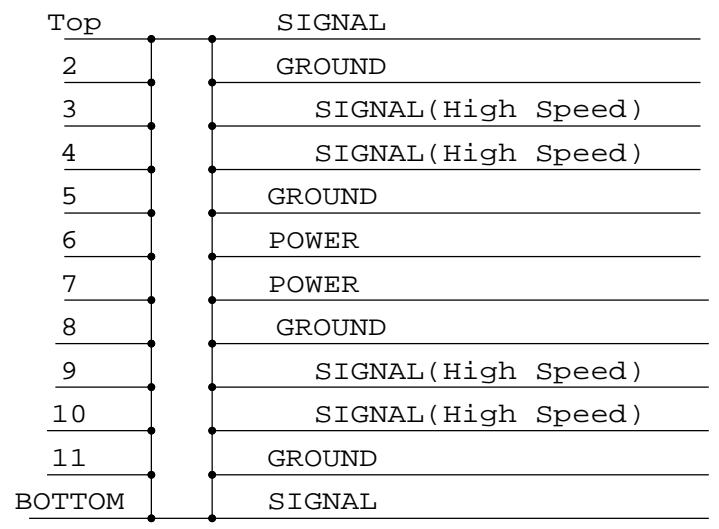
| PART NUMBER | QTY | DESCRIPTION                         | REFERENCE DES | CRITICAL | BOM OPTION      |
|-------------|-----|-------------------------------------|---------------|----------|-----------------|
| 33880563    | 1   | IC_SMC_M07/2117_8398M_TLP_SF        | U4900         | CRITICAL | SMC_BLANK       |
| 34182486    | 1   | IC_SMC_K84                          | U4900         | CRITICAL | SMC_PROD        |
| 33580610    | 1   | IC_FLASH_S01_138817_3_BY_8M8M_8-00P | U6100         | CRITICAL | BOOTROM_BLANK   |
| 34182487    | 1   | IC_FLASH_S01_138817_3_BY_8M8M_8-00P | U6100         | CRITICAL | BOOTROM_PROD    |
| 33782883    | 1   | IC_PSD07_W_038_54_P18_M0P_C78C4794  | U5701         | CRITICAL | WELLSRING_BLANK |
| 34182491    | 1   | IC_WELLSRING_CONTROLLER_K84         | U5701         | CRITICAL | WELLSRING_PROD  |

LOCKED BOOTROM APN IS 34182488

**Alternate Parts**

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:                          |
|-------------|---------------------------|------------|---------|------------------------------------|
| 15280693    | 15280778                  |            | ALL     | DATE/VERSION MISMATCH AS ALTERNATE |
| 15280796    | 15280685                  |            | ALL     | CUSTOM AS ALTERNATE                |
| 15780058    | 15780055                  |            | ALL     | DELTA AS ALTERNATE                 |
| 13880603    | 13880602                  |            | ALL     | MURATA AS ALTERNATE                |
| 12880093    | 12880218                  |            | ALL     | FORMET AS ALTERNATE                |
| 15280874    | 15280516                  |            | ALL     | MURATA AS ALTERNATE                |
| 15280847    | 15280586                  |            | ALL     | MURATA AS ALTERNATE                |
| 10480018    | 10480023                  |            | ALL     | DATE/VERSION MISMATCH AS ALTERNATE |

**K84 BOARD STACK-UP**



SYNC MASTER=K24\_MLB SYNC DATE=01/19/2009

**BOM Configuration**

Apple Inc.

051-7982 D

REVISION C.0.0

BRANCH

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

4/2/2009: RELEASE 9.3.0 (MAJOR):
- PAGE 4: DELETED S250694 ALTERNATE ENTRY FOR 15250138 AS IT IS NOT USED
- PAGE 5: CHANGED R5412 TO 1.50HM (1.450127)
- PAGE 75: CHANGED L7660 TO APN 15250526 - 0.68HM, 3.5MOHM, 16A - AS PER DAYU
- PAGE 97: CHANGED R9716 FROM 226K TO 243K TO CHANGE THE OVP POINT TO 35.3V AS PER KIRAN

05/08/2009: RELEASE 12.12.0 (MAJOR & WEEKLY ECO):
- PAGE 4: DELETED SANYO 6.00HM OSCON CAPS 128S0248 & 128S0271 FROM THE ALTERNATES TABLE (MAKING ALTERNATES AS PRIMARY)
- PAGE 4: TURNING ON BOM OPT FOR MICRSC DIGITIMP YES AS POR IS TO CONNECT MIKEY TO PC70 SMBUS 0 INSTEAD OF SMBUS 1 AND TO CONNECT
- PAGE 50: CHANGED R5030 TO 63.4 OHMS APN 11450102 TO INCREASE THE SIL CURRENT PER REAR-7/PROBLEM/68282

08/31/2009: RELEASE 16.1.0 (MAJOR)-
- PAGE 4: REMOVED 138S0606 FROM THE ALTERNATES TABLE AS IT DOESN'T PERTAIN TO K84
- PAGE 4: REPLACED CPU APN 33753704 WITH 33753769 IN MODULE PARTS TABLE AND REMOVED 33753704 FROM THE ALTERNATES TABLE AS POR IS 23753769 (P7550)
- PAGE 4: REMOVED 870-1794, 870-1698 & 870-1820 FROM THE ALTERNATES TABLE AS POR IS LOW NOISE POGO PINS

Revision History table with columns: DATE, DESCRIPTION, REVISION, and STATUS. Includes a table with columns: DATE, REVISION, and STATUS. Also includes a footer with 'Apple Inc.', 'C.0.0', and '6 OF 109'.

D

D

C

C

B

B

A

A

# Functional Test Points

## FAN CONNECTORS FUNC\_TEST

8277 TRUE PP5VRT S0 7 8  
 8278 TRUE FAN RT PWM 43  
 8279 TRUE FAN RT TACH 43  
 (NEED TO ADD 1 GND TP)

## MIC FUNC\_TEST

8280 TRUE BI MIC LO 53 54  
 8281 TRUE BI MIC HI 53 54  
 8282 TRUE BI MIC SHIELD 53 54

## SPEAKER FUNC\_TEST

8283 TRUE SPKRAMP L N\_OUT 52 53  
 8284 TRUE SPKRAMP L P\_OUT 52 53  
 8285 TRUE SPKRAMP R N\_OUT 52 53  
 8286 TRUE SPKRAMP R P\_OUT 52 53  
 8287 TRUE SPKRAMP SUB N\_OUT 52 53  
 8288 TRUE SPKRAMP SUB P\_OUT 52 53

## LVDS FUNC\_TEST

8289 TRUE PP3V3\_LCDVDD\_SW\_F 7 65 (NEED 2 TP)  
 8290 TRUE PP3V3\_S0\_LCD\_F 65  
 8291 TRUE PPVOUT\_S0\_LCDBKLT 7 47 65 68 (NEED 2 TP)  
 8292 TRUE LVDS\_IG\_DDC\_CLK 18 65  
 8293 TRUE LVDS\_IG\_DDC\_DATA 18 65  
 8294 TRUE LVDS\_IG\_A\_DATA\_N<0> 18 65 72  
 8295 TRUE LVDS\_IG\_A\_DATA\_P<0> 18 65 72  
 8296 TRUE LVDS\_IG\_A\_DATA\_N<1> 18 65 72  
 8297 TRUE LVDS\_IG\_A\_DATA\_P<1> 18 65 72  
 8298 TRUE LVDS\_IG\_A\_DATA\_N<2> 18 65 72  
 8299 TRUE LVDS\_IG\_A\_DATA\_P<2> 18 65 72  
 8300 TRUE LVDS\_IG\_A\_CLK\_F\_N 65 72  
 8301 TRUE LVDS\_IG\_A\_CLK\_F\_P 65 72  
 8302 TRUE LED\_RETURN\_1 65 68  
 8303 TRUE LED\_RETURN\_2 65 68  
 8304 TRUE LED\_RETURN\_3 65 68  
 8305 TRUE LED\_RETURN\_4 65 68  
 8306 TRUE LED\_RETURN\_5 65 68  
 8307 TRUE LED\_RETURN\_6 65 68  
 8308 TRUE PP5V\_S3\_CAMERA\_F 7 65  
 8309 TRUE USB\_CAMERA\_CONN\_P 65 73  
 8310 TRUE USB\_CAMERA\_CONN\_N 65 73  
 (NEED TO ADD 5 GND TP)

## SATA ODD CONN FUNC\_TEST

8311 TRUE PP5V\_SW\_ODD (NEED 2 TP) 7 34 47  
 8312 TRUE SMC\_ODD\_DETECT 34 36  
 8313 TRUE SATA\_ODD\_D2R\_C\_P 34 72  
 8314 TRUE SATA\_ODD\_D2R\_C\_N 34 72  
 8315 TRUE SATA\_ODD\_R2D\_P 34 72  
 8316 TRUE SATA\_ODD\_R2D\_N 34 72  
 (NEED TO ADD 2 GND TP)

## SATA HDD/SIL FUNC\_TEST

8317 TRUE PP5V\_S0\_HDD\_FLT (NEED 2 TP) 7 34  
 8318 TRUE SATA\_HDD\_R2D\_P 34 72  
 8319 TRUE SATA\_HDD\_R2D\_N 34 72  
 8320 TRUE SATA\_HDD\_D2R\_C\_P 34 72  
 8321 TRUE SATA\_HDD\_D2R\_C\_N 34 72  
 8322 TRUE SYS\_LED\_ANODE\_R 34  
 (NEED TO ADD 3 GND TP)

## BATT POWER CONN FUNC\_TEST

8323 TRUE SMBUS\_SMC\_BSA\_SCL 39 75  
 8324 TRUE SMBUS\_SMC\_BSA\_SDA 39 75  
 8325 TRUE SYS\_DETECT\_L 55  
 8326 TRUE BATT\_POS\_F 55 56 (NEED 2 TP)  
 (NEED TO ADD 2 GND TP)

## HALL EFFECT CONNECTOR FUNC\_TEST

8327 TRUE PP3V42\_G3H 7 8  
 8328 TRUE SMC\_LID\_R 55

## X16 WIRELESS CONN FUNC\_TEST

8329 TRUE PP3V3\_S3\_BT\_F 30  
 8330 TRUE CONN\_PCIE\_MINI\_D2R\_P 30 72  
 8331 TRUE CONN\_PCIE\_MINI\_D2R\_N 30 72  
 8332 TRUE CONN\_PCIE\_MINI\_R2D\_P 30 72  
 8333 TRUE CONN\_PCIE\_MINI\_R2D\_N 30 72  
 8334 TRUE PCIE\_CLK100M\_MINI\_CONN\_P 30 72  
 8335 TRUE PCIE\_CLK100M\_MINI\_CONN\_N 30 72  
 8336 TRUE PP3V3\_WLAN 7 30 (NEED 2 TP)  
 8337 TRUE PCIE\_WAKE\_L 17 30  
 8338 TRUE CONN\_USB2\_BT\_P 30 73  
 8339 TRUE CONN\_USB2\_BT\_N 30 73  
 8340 TRUE MINI\_CLKREQ\_Q\_L 30  
 8341 TRUE MINI\_RESET\_CONN\_L 30  
 (NEED TO ADD 2 GND TP)

## IPD\_FLEX\_CONN FUNC\_TEST

8342 TRUE PP3V3\_S3\_LDO 7 45  
 8343 TRUE PP18V5\_S3 7 45  
 8344 TRUE Z2\_CS\_L 44 45  
 8345 TRUE Z2\_DEBUG3 44 45  
 8346 TRUE Z2\_MOS1 44 45  
 8347 TRUE Z2\_SCLK 44 45  
 8348 TRUE Z2\_BOOST\_EN 45  
 8349 TRUE Z2\_HOST\_INTN 44 45  
 8350 TRUE Z2\_CLKIN 44 45  
 8351 TRUE Z2\_KEY\_ACT\_L 44 45  
 8352 TRUE Z2\_RESET 44 45  
 8353 TRUE PSOC\_MISO 44 45  
 8354 TRUE PSOC\_MOSI 44 45  
 8355 TRUE PSOC\_SCLK 44 45  
 8356 TRUE SMBUS\_SMC\_A\_S3\_SDA 39 75  
 8357 TRUE SMBUS\_SMC\_A\_S3\_SCL 39 75  
 8358 TRUE PSOC\_F\_CS\_L 44 45  
 8359 TRUE PICKB\_L 44 45  
 (NEED TO ADD 2 GND TP)

## KEYBOARD CONN FUNC\_TEST

8360 TRUE PP3V3\_S3 7 8  
 8361 TRUE PP3V42\_G3H 7 8  
 8362 TRUE WS\_KBD1 44  
 8363 TRUE WS\_KBD2 44  
 8364 TRUE WS\_KBD3 44  
 8365 TRUE WS\_KBD4 44  
 8366 TRUE WS\_KBD5 44  
 8367 TRUE WS\_KBD6 44  
 8368 TRUE WS\_KBD7 44  
 8369 TRUE WS\_KBD8 44  
 8370 TRUE WS\_KBD9 44  
 8371 TRUE WS\_KBD10 44  
 8372 TRUE WS\_KBD11 44  
 8373 TRUE WS\_KBD12 44  
 8374 TRUE WS\_KBD13 44  
 8375 TRUE WS\_KBD14 44  
 8376 TRUE WS\_KBD15\_CAP 44  
 8377 TRUE WS\_KBD16\_NUM 44  
 8378 TRUE WS\_KBD17 44  
 8379 TRUE WS\_KBD18 44  
 8380 TRUE WS\_KBD19 44  
 8381 TRUE WS\_KBD20 44  
 8382 TRUE WS\_KBD21 44  
 8383 TRUE WS\_KBD22 44  
 8384 TRUE WS\_KBD23 44  
 8385 TRUE WS\_KBD\_ONOFF\_L 44  
 8386 TRUE WS\_LEFT\_SHIFT\_KBD 44  
 8387 TRUE WS\_LEFT\_OPTION\_KBD 44  
 8388 TRUE WS\_CONTROL\_KBD 44  
 (NEED TO ADD 1 GND TP)

## POWER NETS FUNC\_TEST

8389 TRUE PPVCORE\_S0\_CPU 8  
 8390 TRUE PPVCORE\_S0\_MCP 8  
 8391 TRUE PP0V75\_S0 8  
 8392 TRUE PP1V05\_S0 8  
 8393 TRUE PP1V5\_S0 8  
 8394 TRUE PP1V8\_S0 8  
 8395 TRUE PP5VLT\_S0 8  
 8396 TRUE PP5VRT\_S0 7 8  
 8397 TRUE PP3V3\_S0 8  
 8398 TRUE PP1V5\_S3 8  
 8399 TRUE PP3V3\_S3 7 8  
 8400 TRUE PP5V\_S3 8  
 8401 TRUE PP1V1R1V05\_S5 8  
 8402 TRUE PP3V3\_S5 8  
 8403 TRUE PP3V42\_G3H 7 8  
 8404 TRUE PPBUS\_G3H 8  
 8405 TRUE PP3V3\_ENET\_PHY 8  
 8406 TRUE PP1V2R1V05\_ENET 8  
 8407 TRUE PP3V3\_G3\_RTC 21 22 25  
 8408 TRUE PP3V3\_WLAN 7 30  
 8409 TRUE PP5V\_SW\_ODD 7 34 47  
 8410 TRUE PP5V\_S0\_HDD\_FLT 7 34  
 8411 TRUE PP3V3\_S5\_AVREF\_SMC 36 37  
 8412 TRUE PP18V5\_S3 7 45  
 8413 TRUE PP3V3\_S3\_LDO 7 45  
 8414 TRUE PP3V3\_LCDVDD\_SW\_F 7 65  
 8415 TRUE PPVOUT\_S0\_LCDBKLT 7 47 65 68  
 8416 TRUE PP4V5\_AUDIO\_ANALOG 49  
 8417 TRUE SMC\_PM\_G2\_EN 36 57 63  
 8418 TRUE PM\_SLP\_S4\_L 21 32 36 63 67  
 8419 TRUE PM\_SLP\_S3\_L 21 32 36 63 67  
 8420 TRUE PP5V\_S3\_CAMERA\_F 7 65  
 (NEED TO ADD 1 GND TP)

## DC POWER CONN FUNC\_TEST

8421 TRUE PP18V5\_DCIN\_FUSE (NEED 2 TP) 55  
 8422 TRUE ADAPTER\_SENSE 55  
 (NEED TO ADD 2 GND TP)

SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

## FUNC TEST



Apple Inc.

DRAWING NUMBER 051-7982 D  
 REVISION C.0.0

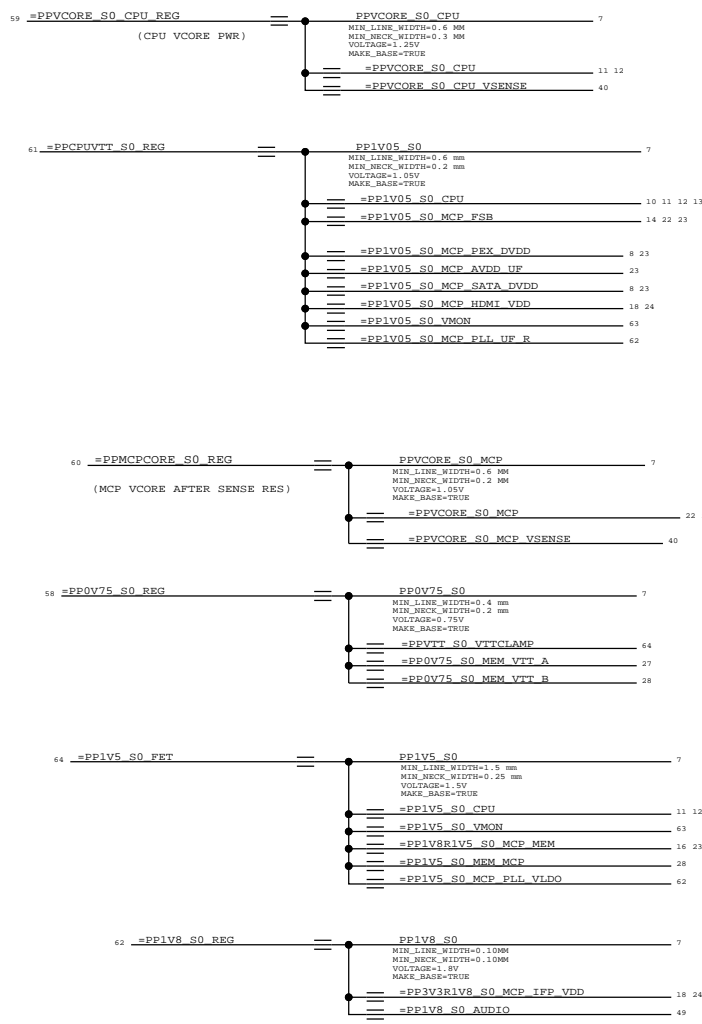
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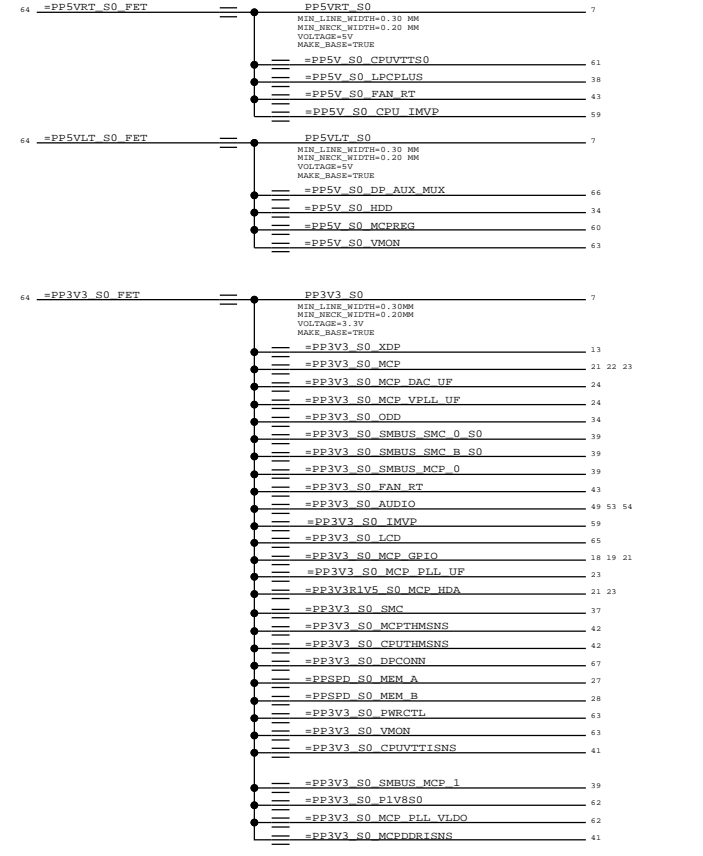
BRANCH  
 PAGE 7 OF 109 SHEET

<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

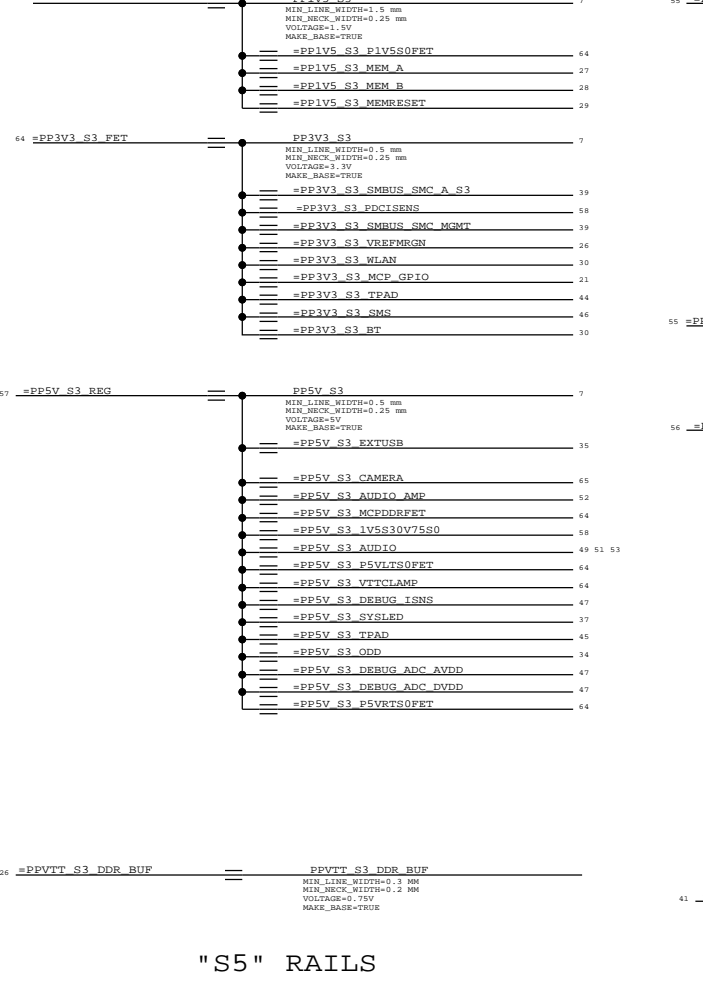
"S0,S0M" RAILS



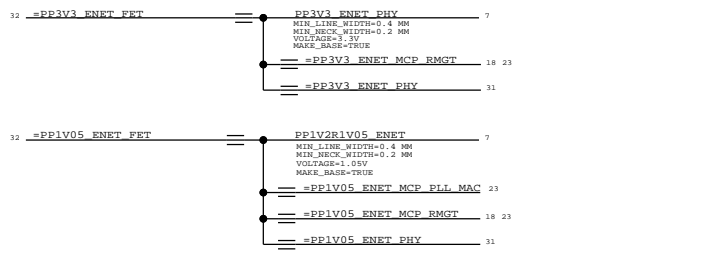
"S3" RAILS



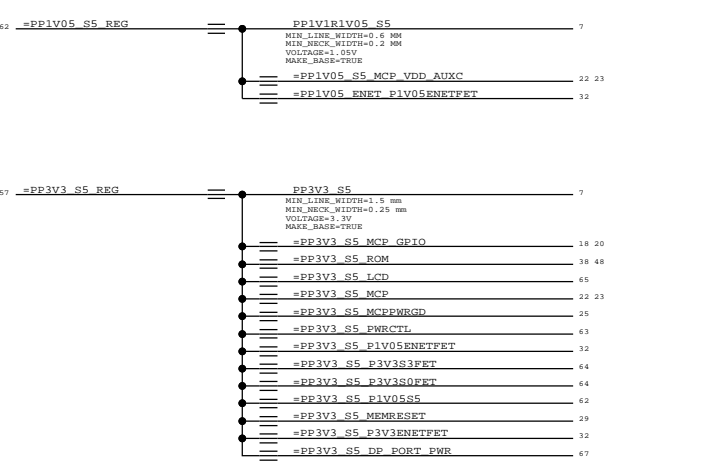
"G3H" RAILS



"ENET" RAILS



"S5" RAILS



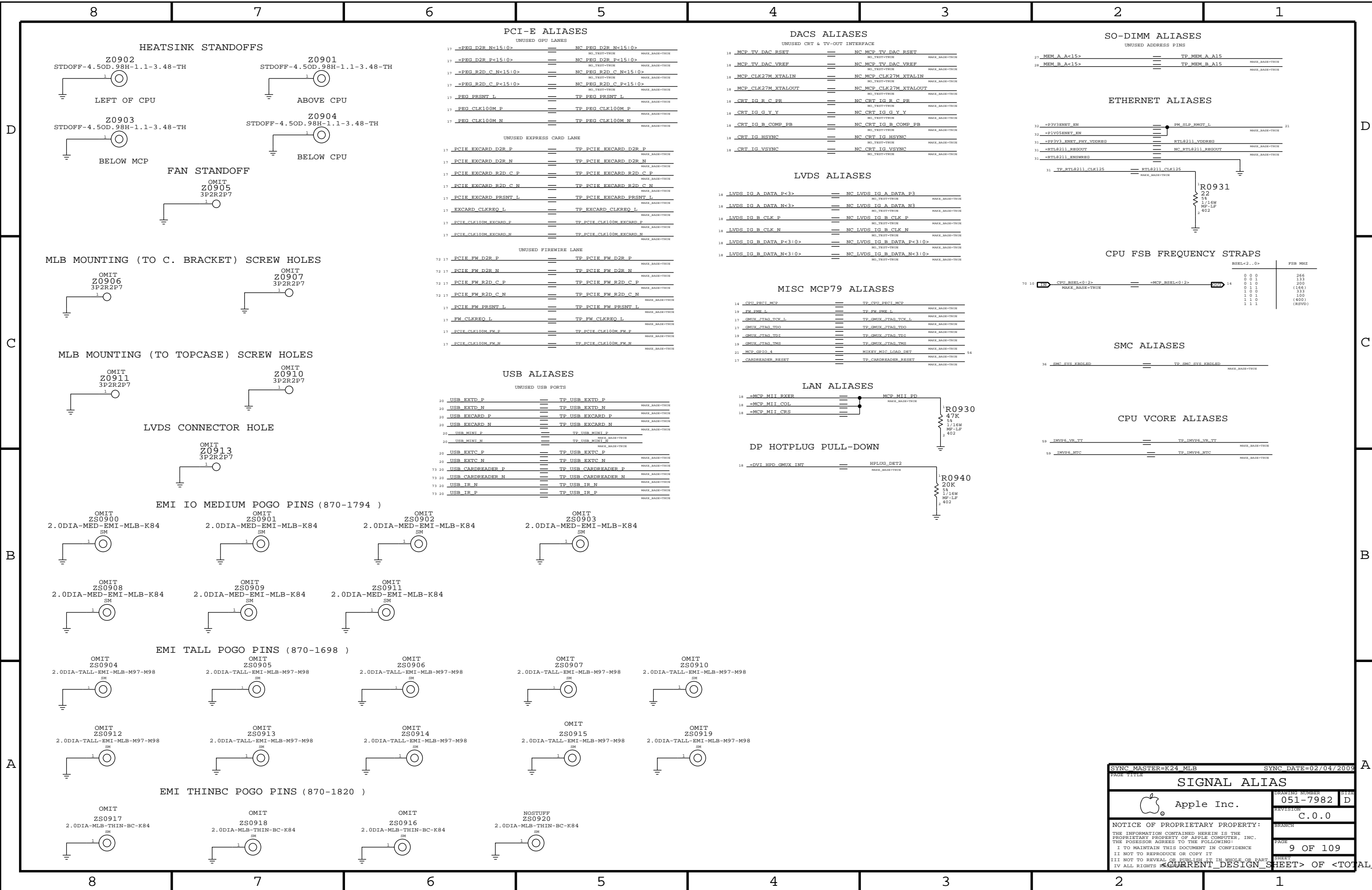
PEX & SATA AVDD/DVDD aliases



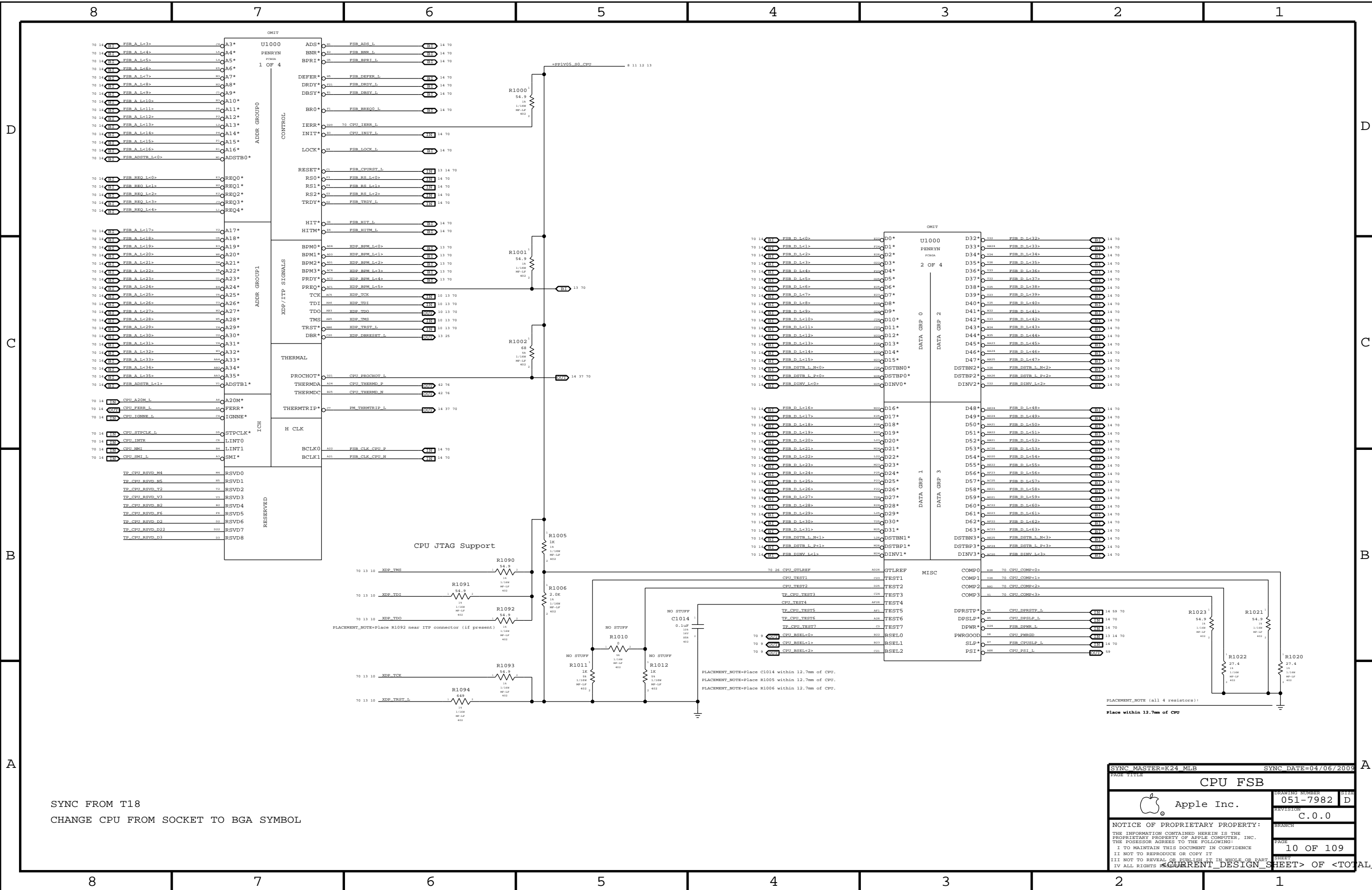
SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

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|---|--|--------------------------------|----------|
| Power Aliases   |  | DRAWING NUMBER                 | 051-7982 |
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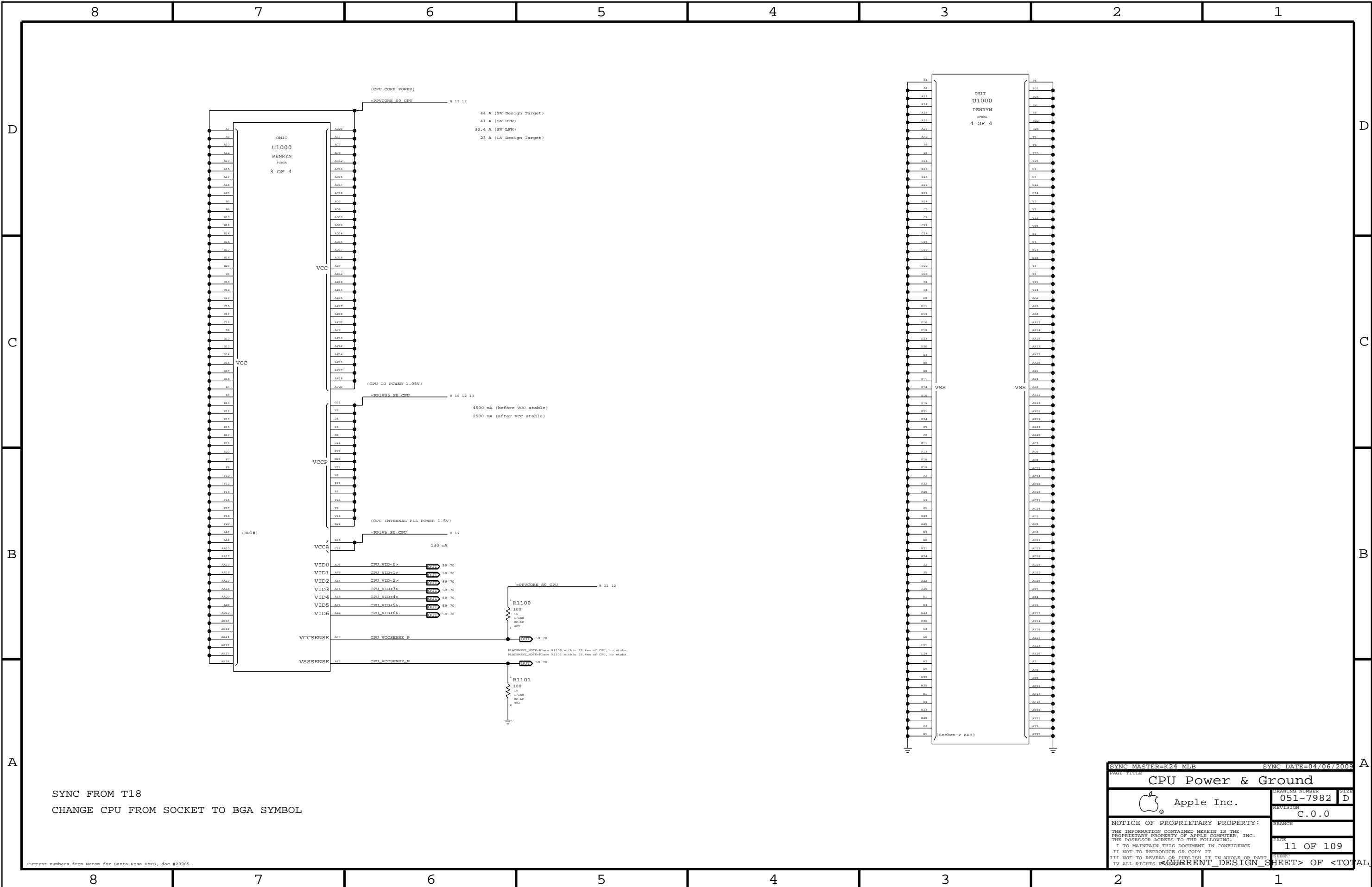


SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

|                           |                                   |
|---------------------------|-----------------------------------|
| <b>CPU FSB</b>            |                                   |
| Apple Inc.                | DRAWING NUMBER<br><b>051-7982</b> |
| REVISION<br><b>C.0.0</b>  |                                   |
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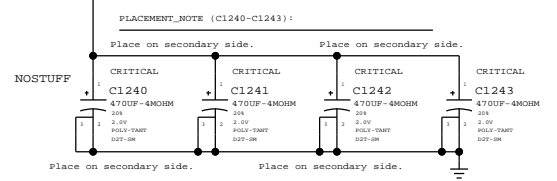
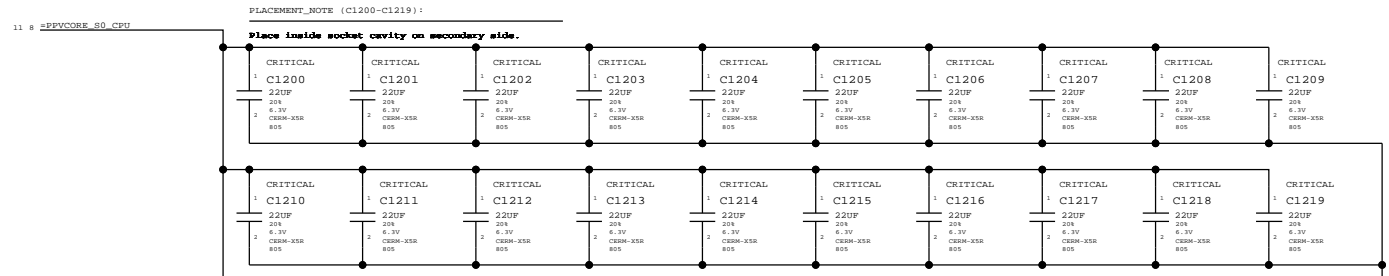
SYNC FROM T18  
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

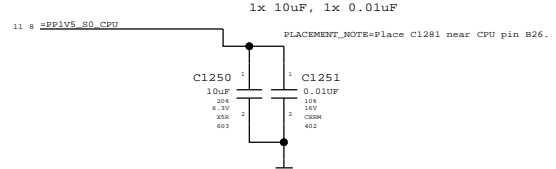
|   |  |                 |          |           |   |
|---|--|-----------------|----------|-----------|---|
| CPU Power & Ground  |  | CREATION NUMBER | 051-7982 | REVISION  | D |
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Current numbers from Merom for Santa Rosa KMTS, doc #20905.

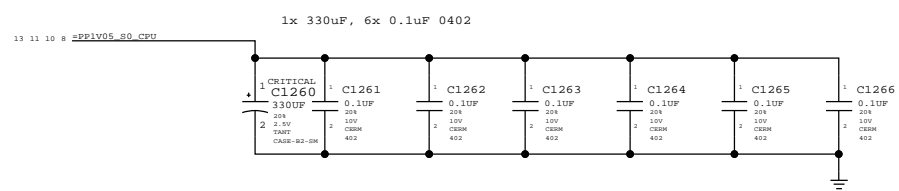
CPU VCore HF and Bulk Decoupling  
4x 330uF, 20x 22uF 0805



VCCA (CPU AVdd) DECOUPLING



VCCP (CPU I/O) DECOUPLING



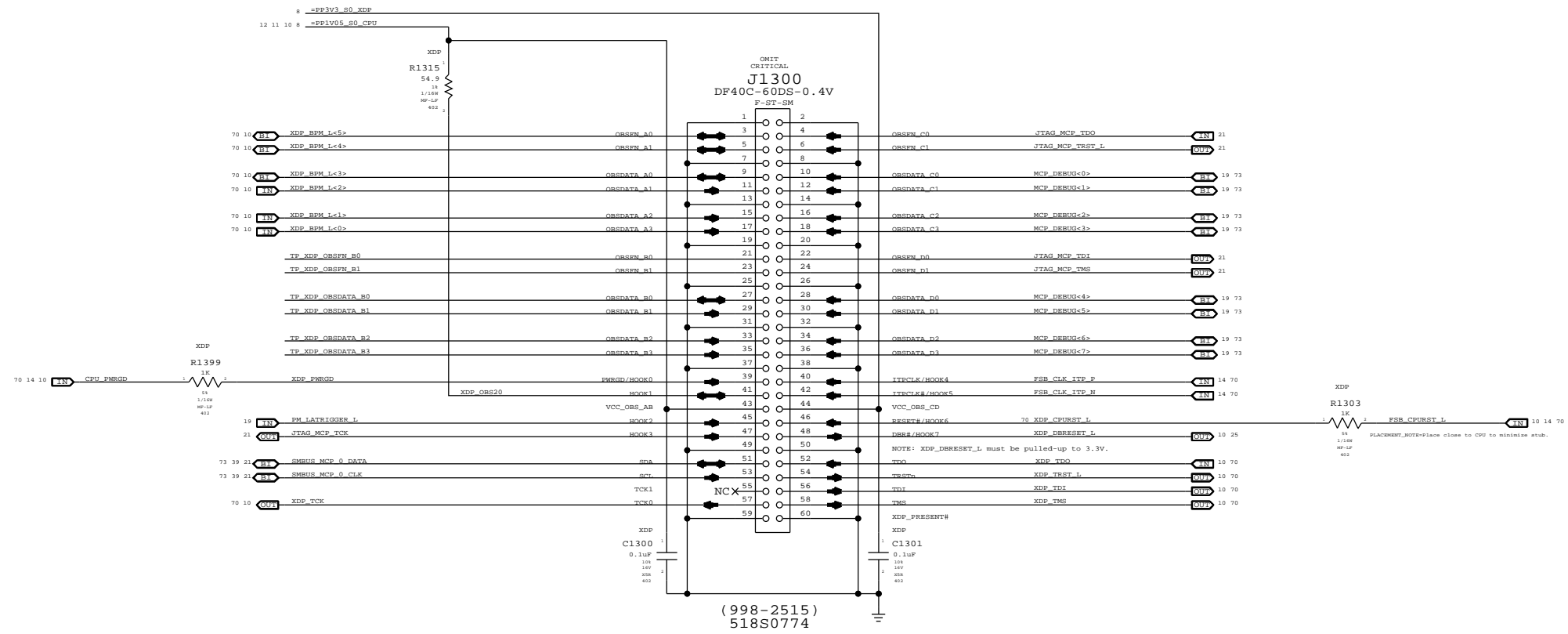
SYNC FROM T18  
REMOVE NO STUFF CAPS C1220 TO C1231  
REMOVE C1244 & C1245  
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

|   |  |                             |                   |
|---|--|-----------------------------|-------------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=03/30/2009        |                   |
| PAGE TITLE<br>CPU Decoupling  |  |                             |                   |
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### Mini-XDP Connector

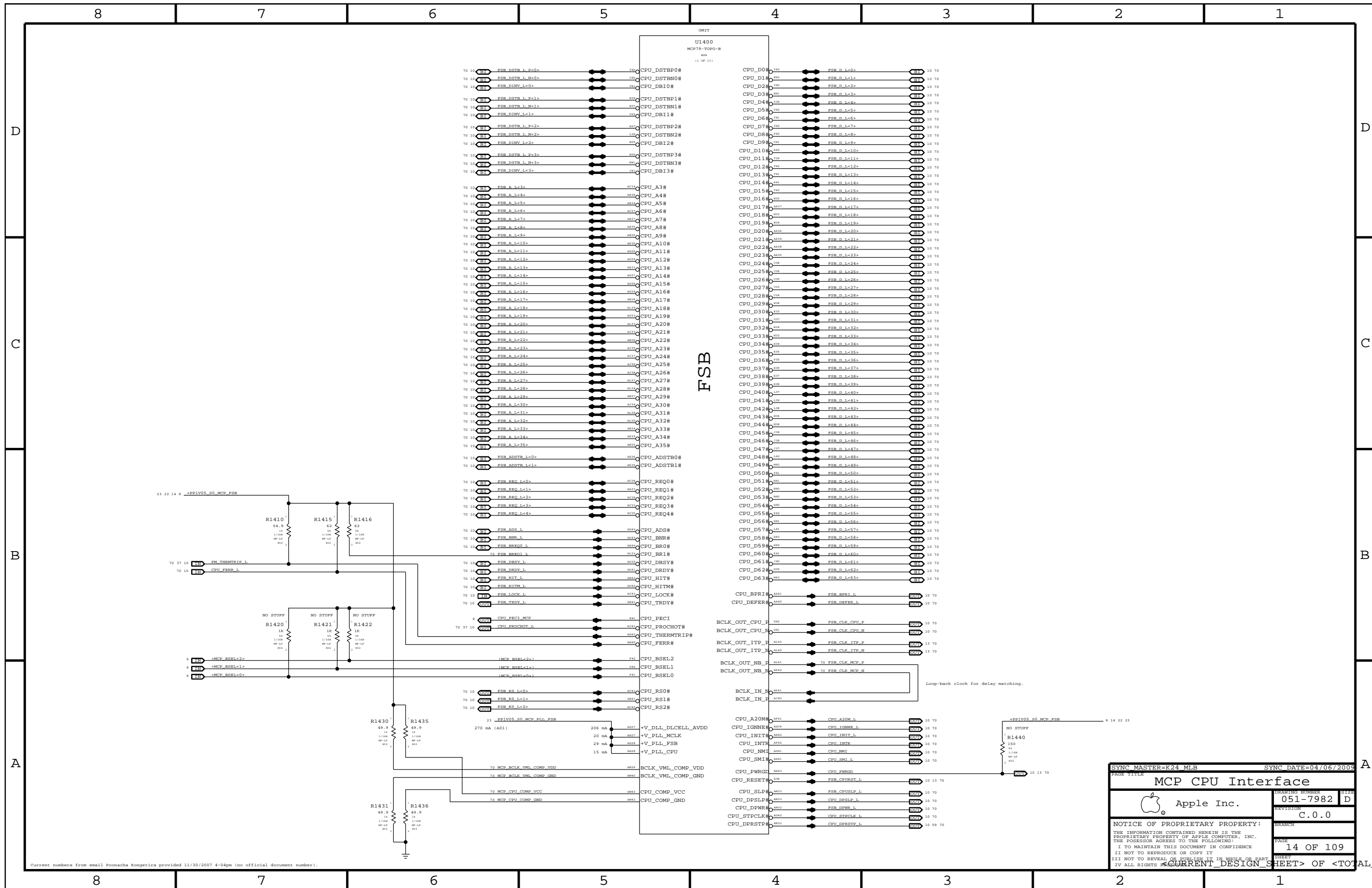
NOTE: This is not the standard XDP pinout.  
USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

### MCP79-specific pinout



← Direction of XDP module  
Please avoid any obstructions  
ON ODD-NUMBERED SIDE OF J1300

|   |  |                      |   |
|---|--|----------------------|---|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=02/25/2009 |   |
| eXtended Debug Port (MiniXDP)   |  |                      |   |
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SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

MCP CPU Interface

Apple Inc.

051-7982 D

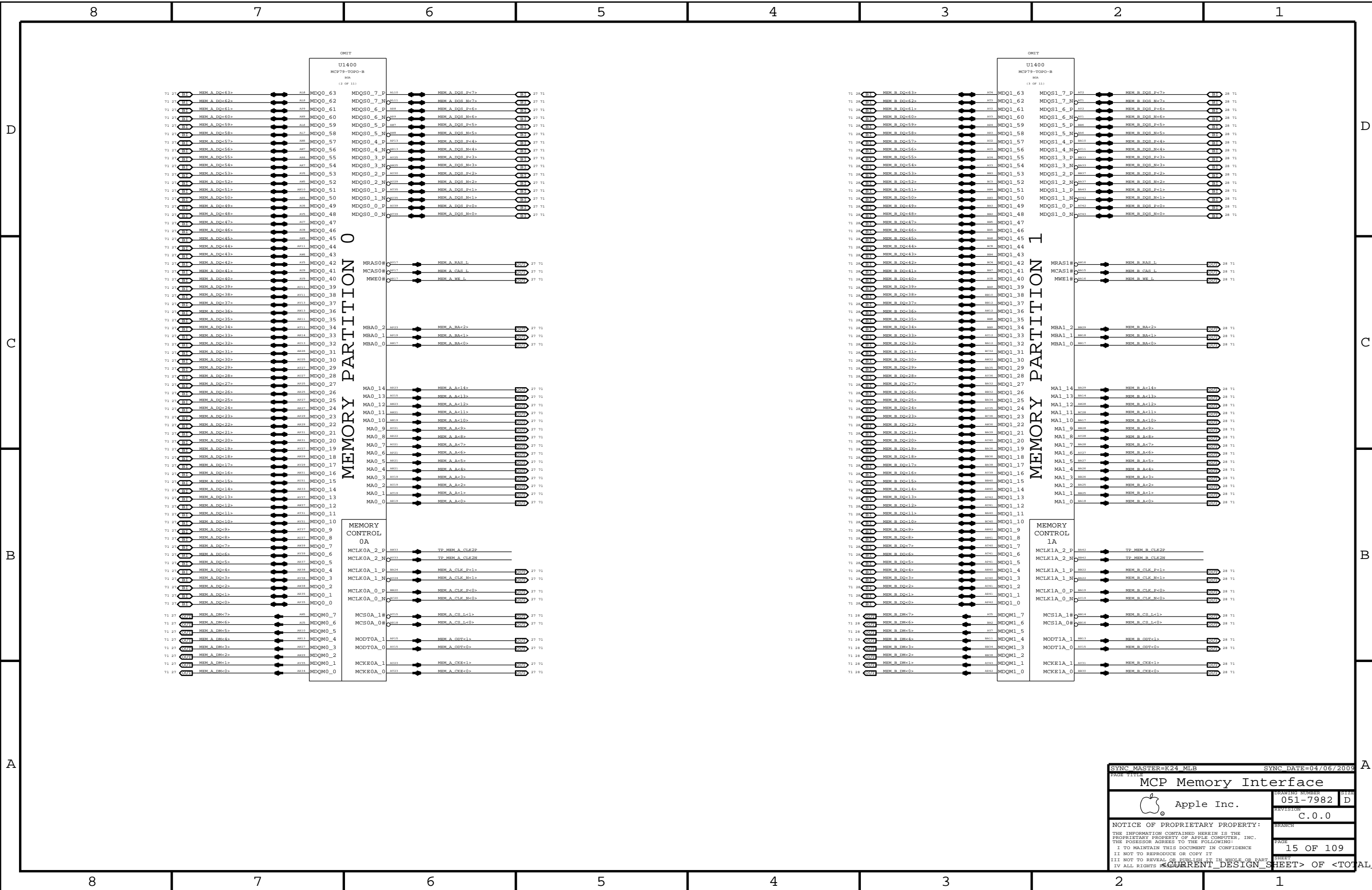
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SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

**MCP Memory Interface**

Apple Inc.

051-7982 D

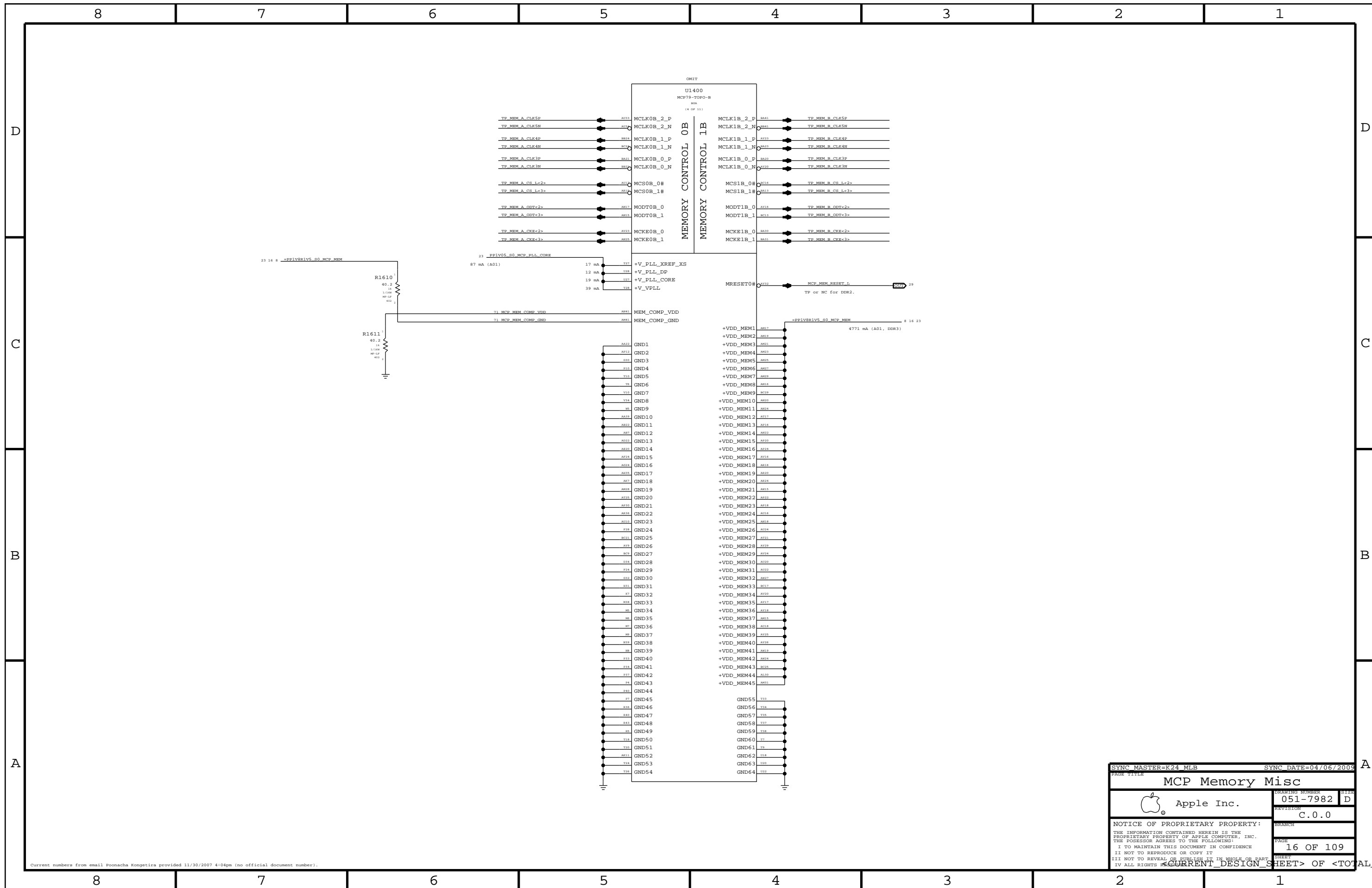
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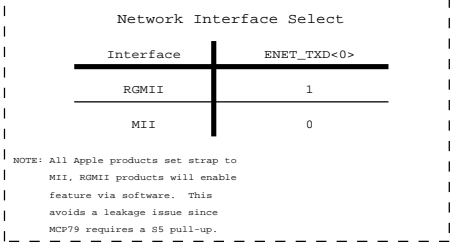
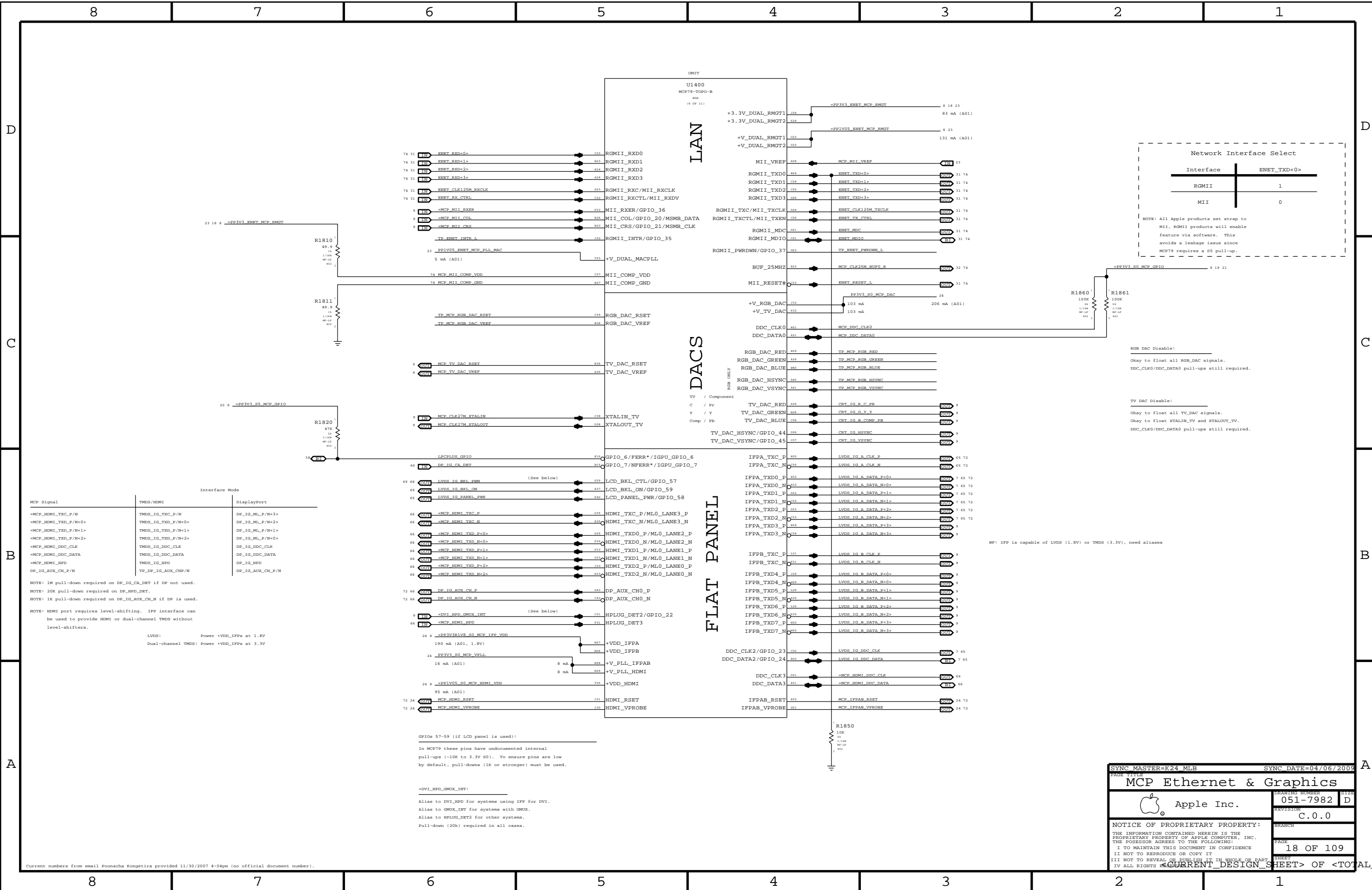


|   |  |   |            |
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| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009                        |            |
| MCP Memory Misc   |  |   |            |
| Apple Inc.  |  | DRAWING NUMBER                              | 051-7982 D |
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RGB DAC Disable: \_\_\_\_\_  
 Okay to float all RGB\_DAC signals.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

TV DAC Disable: \_\_\_\_\_  
 Okay to float all TV\_DAC signals.  
 Okay to float XTALIN\_TV and XTALOUT\_TV.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

WP: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

| MCP Signal           | TMDS/HDMI           | DisplayPort      |
|----------------------|---------------------|------------------|
| =MCP_HDMI_TXC_P/N    | TMDS_IG_TXC_P/N     | DP_IG_ML_P/N<3>  |
| =MCP_HDMI_TXD_P/N<0> | TMDS_IG_TXD_P/N<0>  | DP_IG_ML_P/N<2>  |
| =MCP_HDMI_TXD_P/N<1> | TMDS_IG_TXD_P/N<1>  | DP_IG_ML_P/N<1>  |
| =MCP_HDMI_TXD_P/N<2> | TMDS_IG_TXD_P/N<2>  | DP_IG_ML_P/N<0>  |
| =MCP_HDMI_DDC_CLK    | TMDS_IG_DDC_CLK     | DP_IG_DDC_CLK    |
| =MCP_HDMI_DDC_DATA   | TMDS_IG_DDC_DATA    | DP_IG_DDC_DATA   |
| =MCP_HDMI_HPD        | TMDS_IG_HPD         | DP_IG_HPD        |
| DP_IG_AUX_CH_P/N     | TP_DP_IG_AUX_CH_P/N | DP_IG_AUX_CH_P/N |

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
 NOTE: 20k pull-down required on DP\_HPD\_DET.  
 NOTE: 1k pull-down required on DP\_IG\_AUX\_CH\_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD\_IFPx at 1.8V  
 Dual-channel TMDS: Power +VDD\_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):  
 In MCP79 these pins have undocumented internal pull-ups (-10k to 3.3V 50). To ensure pins are low by default, pull-downs (1k or stronger) must be used.

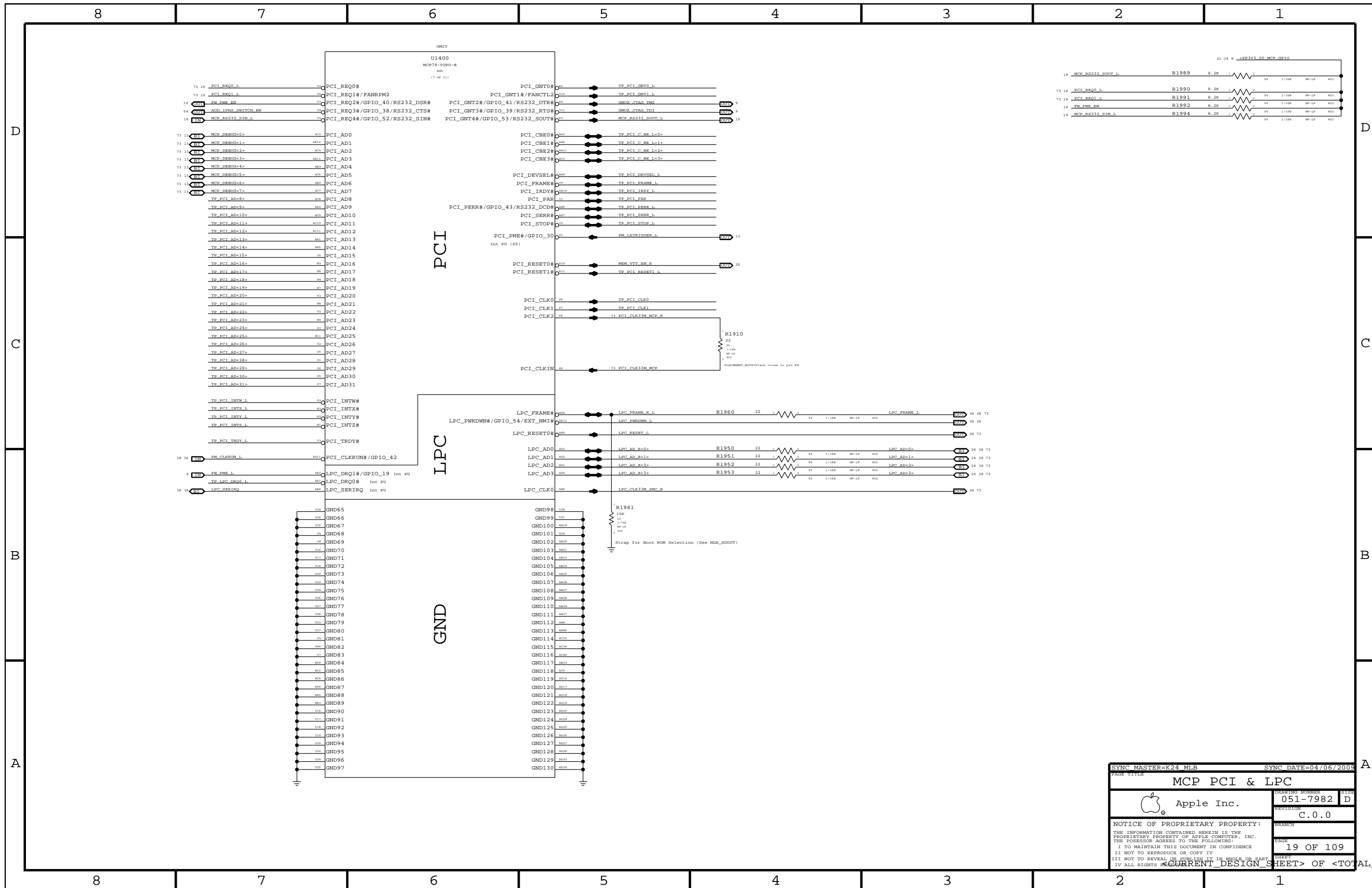
=DVI\_HPD\_GMIX\_INT:  
 Alias to DVI\_HPD for systems using IFP for DVI.  
 Alias to GMIX\_INT for systems with GMIX.  
 Alias to HPLUG\_DET2 for other systems.  
 Pull-down (20k) required in all cases.

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

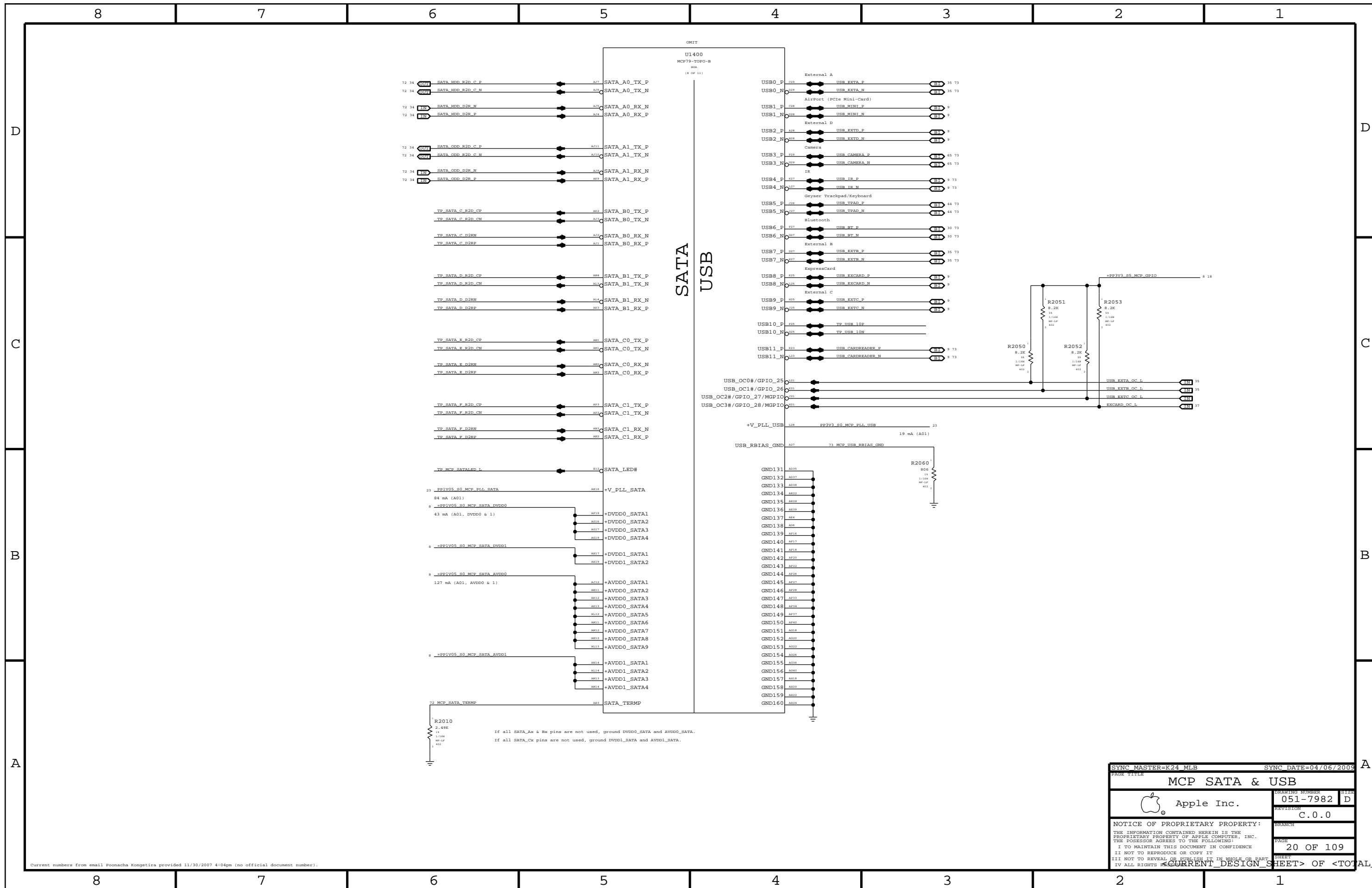
MCP Ethernet & Graphics

Apple Inc.  
 CREATION NUMBER: 051-7982 D  
 REVISION: C.0.0

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|   |  |                      |            |
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| <b>MCP PCI &amp; LPC</b>  |  |                      |            |
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|   |  |                      |            |
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| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009 |            |
| MCP SATA & USB  |  |                      |            |
| Apple Inc.  |  | DRAWING NUMBER       | 051-7982 D |
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D

D

C

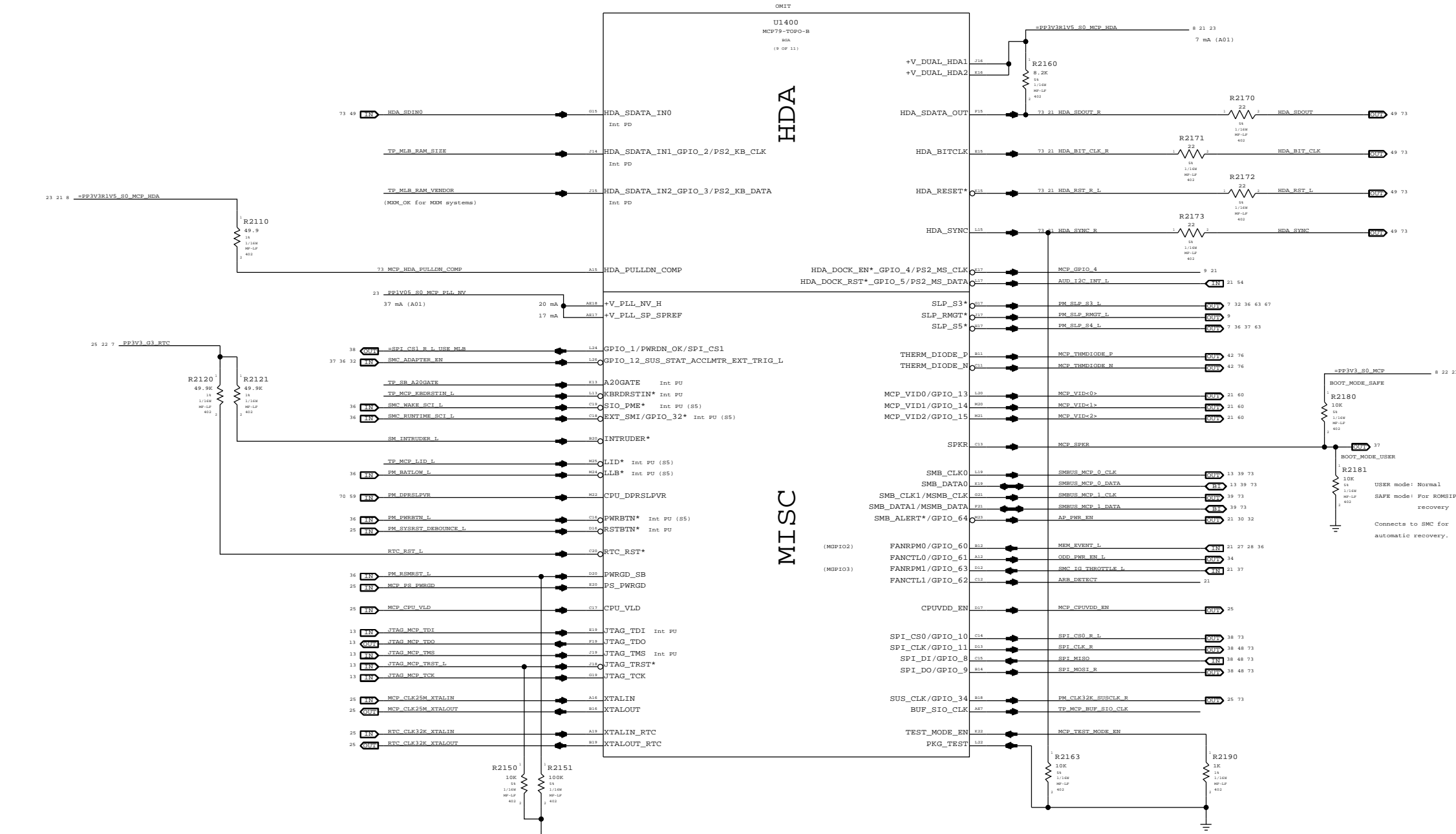
C

B

B

A

A



BIOS Boot Select

| I/F  | HDA_SDOUT | LPC_FRAME# |
|------|-----------|------------|
| LPC  | 0         | 0          |
| PCI  | 0         | 1          |
| SPI0 | 1         | 0          |
| SPI1 | 1         | 1          |

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L  
 R1961 and R2160 selects SPI0 ROM by default. LPC debug card pulls LPC\_FRAME# high for SPI1 ROM override.  
 NOTE: MCP9798 does not support FW, only LPC ROMs. So Apple designs will not use LPC for BootROM override.  
 NOTE: MCP9798 rev A01 does not support SPI1 option. Rev B01 will.

BUF\_SIO\_CLK Frequency

| Frequency    | HDA_SYNC |
|--------------|----------|
| 24 MHz       | 1        |
| 14.31818 MHz | 0        |

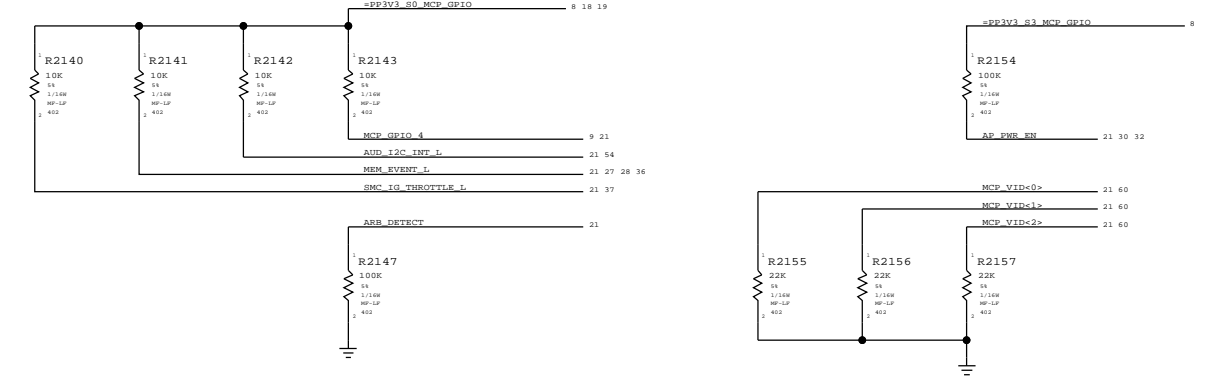
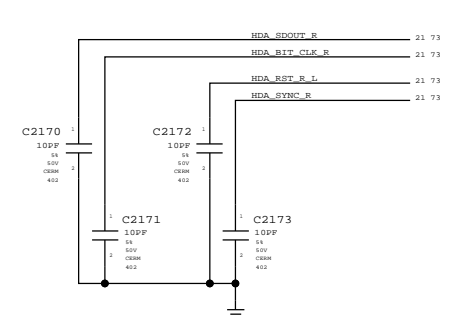
SPI Frequency Select

| Frequency | SPI_DO | SPI_CLK |
|-----------|--------|---------|
| 31 MHz    | 0      | 0       |
| 42 MHz    | 0      | 1       |
| 25 MHz    | 1      | 0       |
| 1 MHz     | 1      | 1       |

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



SYNC MASTER=K24 MLB SYNC DATE=03/24/2009

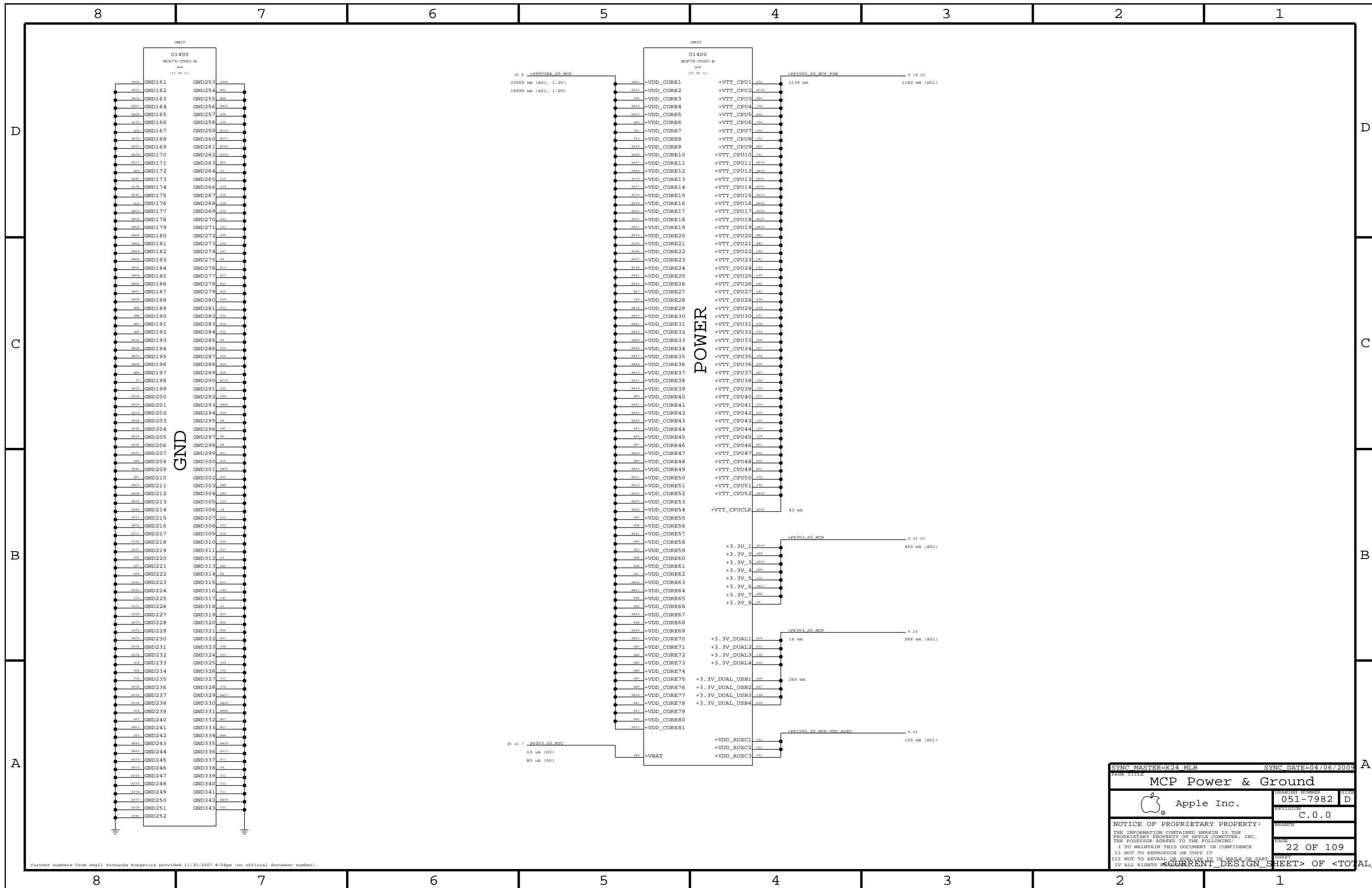
MCP HDA & MISC

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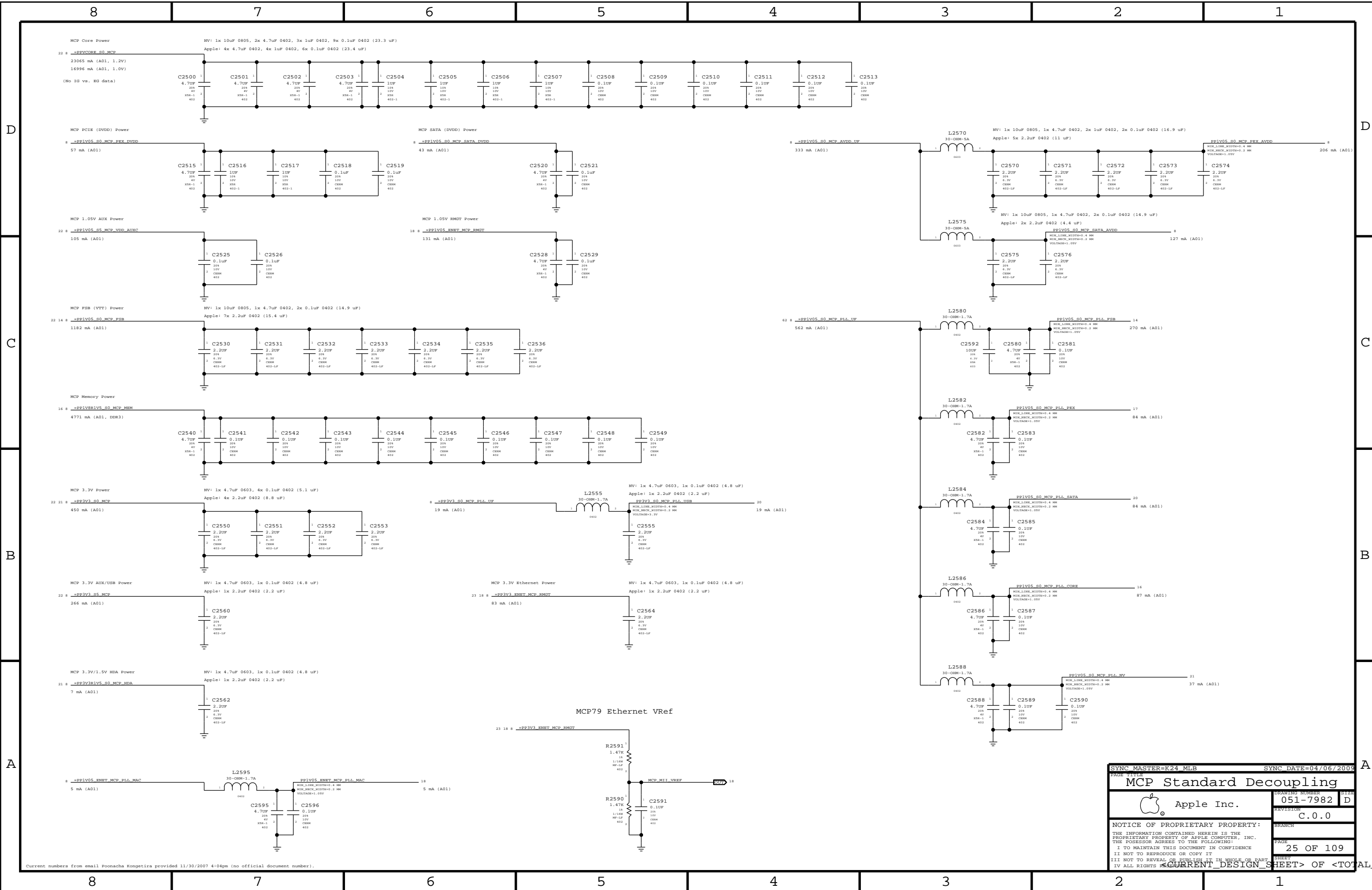
CREATING NUMBER: 051-7982 D  
 REVISION: C.0.0  
 PAGE: 21 OF 109  
 SHEET: 21 OF 109

Current numbers from email Poonacha Kongtira provided 11/30/2007 4:04pm (no official document number).



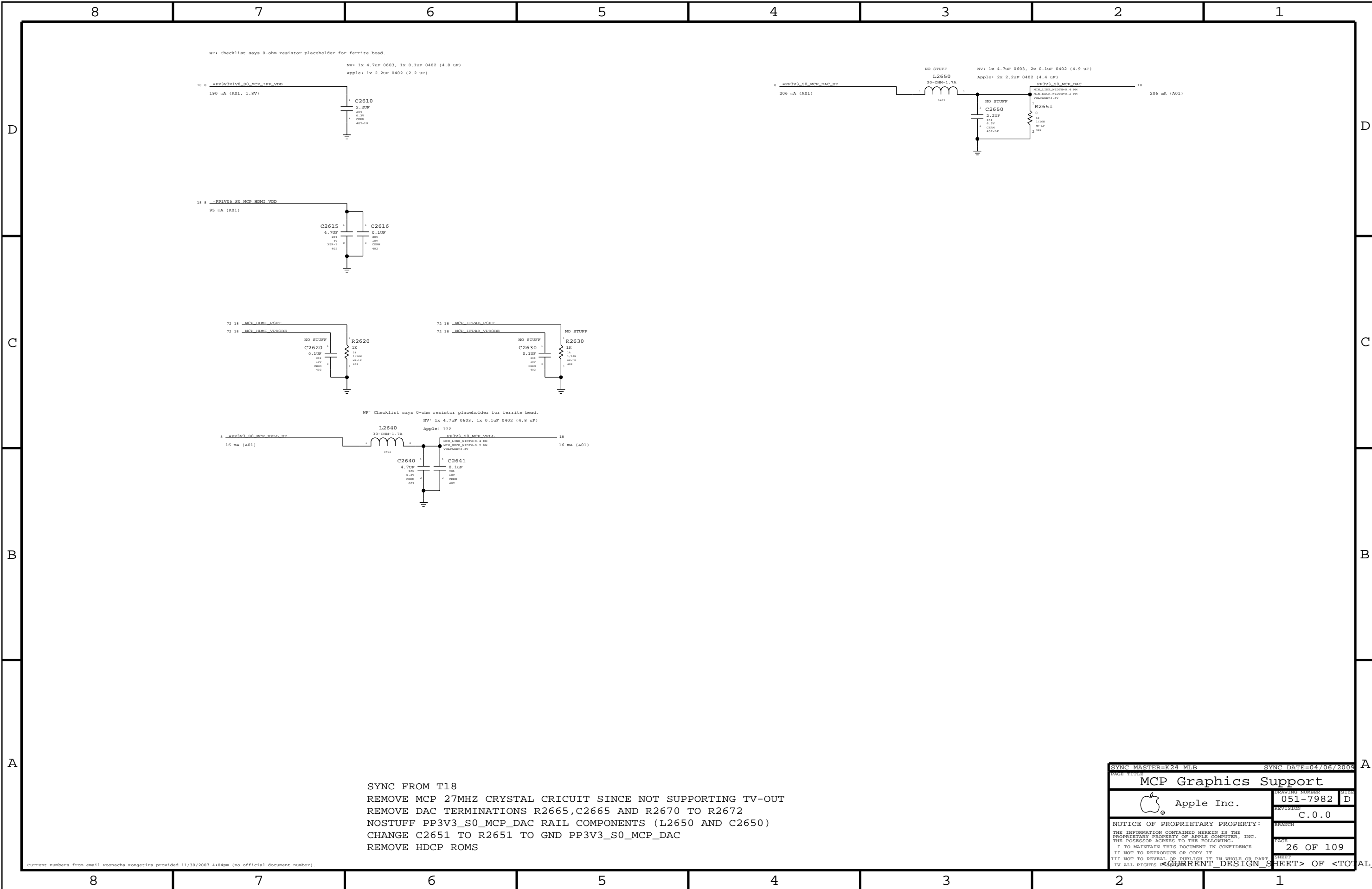
|   |  |   |            |
|---|--|---|------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009                        |            |
| PAGE TITLE  |  |   |            |
| <b>MCP Power &amp; Ground</b>   |  |   |            |
| Apple Inc.  |  | CREATION NUMBER                             | 051-7982 D |
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|   |  |                      |            |
|---|--|----------------------|------------|
| PAGE TITLE  |  | SYNC DATE=04/06/2009 |            |
| <b>MCP Standard Decoupling</b>  |  |                      |            |
| Apple Inc.  |  | CREATING NUMBER      | 051-7982 D |
|   |  | REVISION             | C.0.0      |
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|   |  | PAGE                 | 25 OF 109  |
|   |  | SHEET                |            |

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WP: Checklist says 0-ohm resistor placeholder for ferrite bead.  
 NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
 Apple: 1x 2.2uF 0402 (2.2 uF)

NO STUFF  
 L2650  
 30-ohm-1.7A  
 NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)  
 Apple: 2x 2.2uF 0402 (4.4 uF)

WP: Checklist says 0-ohm resistor placeholder for ferrite bead.  
 NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
 Apple: 799

SYNC FROM T18  
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT  
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672  
 NOSTUFF PP3V3\_S0\_MCP\_DAC RAIL COMPONENTS (L2650 AND C2650)  
 CHANGE C2651 TO R2651 TO GND PP3V3\_S0\_MCP\_DAC  
 REMOVE HDCP ROMS

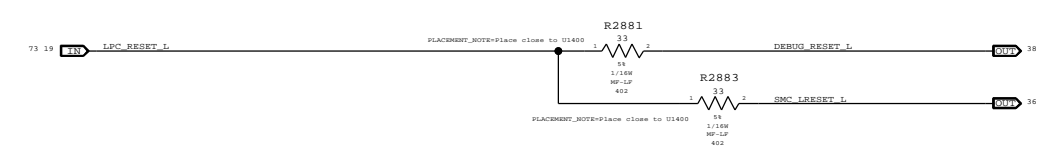
|   |  |                      |   |
|---|--|----------------------|---|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009 |   |
| MCP Graphics Support  |  |                      |   |
| Apple Inc.  |  | 051-7982             | D |
|   |  | C.0.0                |   |
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|   |  | 26 OF 109            |   |

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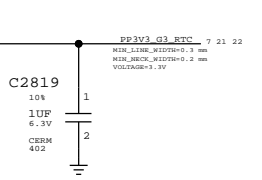
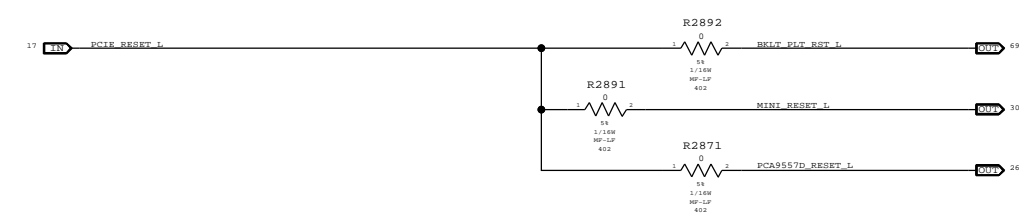


### Platform Reset Connections

#### LPC Reset (Unbuffered)

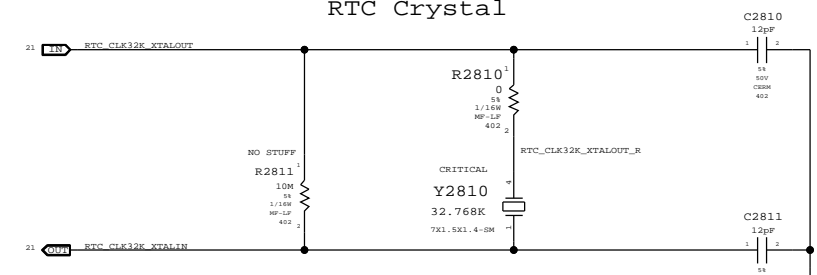


#### PCIE Reset (Unbuffered)

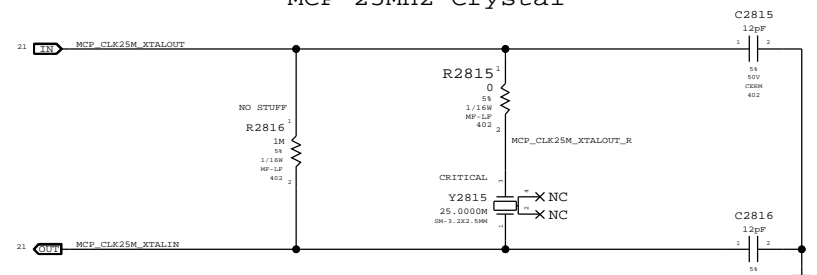


PLACEMENT\_NOTE=PLACE C2819 CLOSE TO MCP79  
PLACE C2819 CLOSE TO MCP79

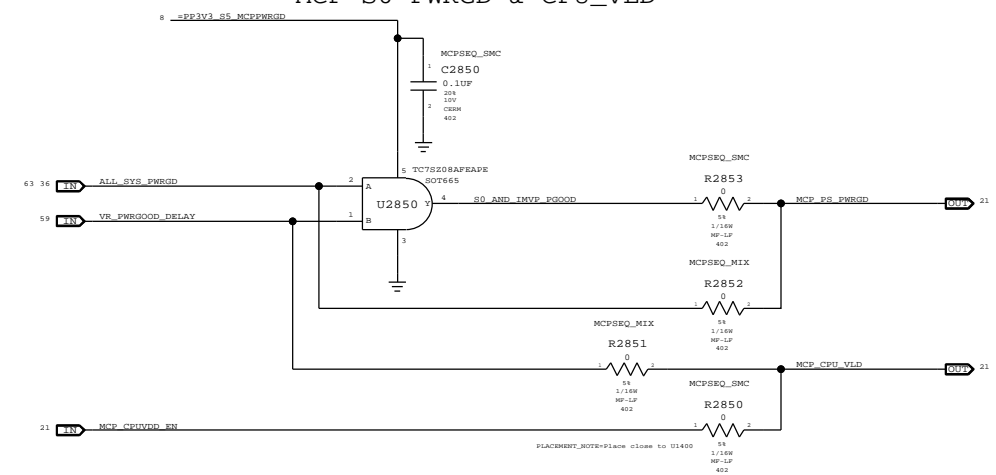
#### RTC Crystal



#### MCP 25MHz Crystal



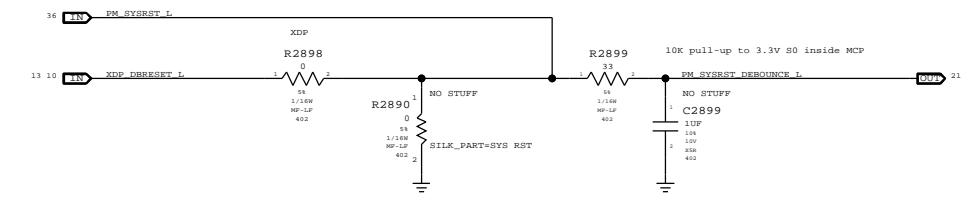
#### MCP S0 PWRGD & CPU\_VLD



MCPSEQ\_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.  
MCPSEQ\_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP PSB I/O interface initialization.  
SMC 99ms delay from ALL\_SYS\_PWRGD to INV6\_VR\_ON plus INV6 delay for VR\_PWRGD\_DELAY should guarantee CPU\_VLD does not go high before CPUVDD\_EN (which is 40-100ms after PS\_PWRGD assertion).  
NOTE: If CPU\_VLD deasserts during S0 MCP79 will take system to S5 immediately.

SYNC FROM T18  
CHANGE RESET BUTTON TO RESET PADS  
REMOVE UNUSED PCIE RESET SIGNALS  
REMOVE R2824 AND NET PCI\_CLK33M\_SLOT\_A  
CHANGE RTC COIN CELL TO LDO & SUPERCAP  
ALIAS MEM\_VTT\_EN TO =DDRVTT\_EN  
CHANGE Y2810 AND U2850 TO SMALLER PARTS

#### Reset Button



SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

|   |  |           |   |
|---|--|-----------|---|
| PAGE TITLE  |  | SB Misc   |   |
| DRAWING NUMBER                                      |  | 051-7982  | D |
| REVISION  |  | C.0.0     |   |
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| PAGE  |  | 28 OF 109 |   |
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Page Notes

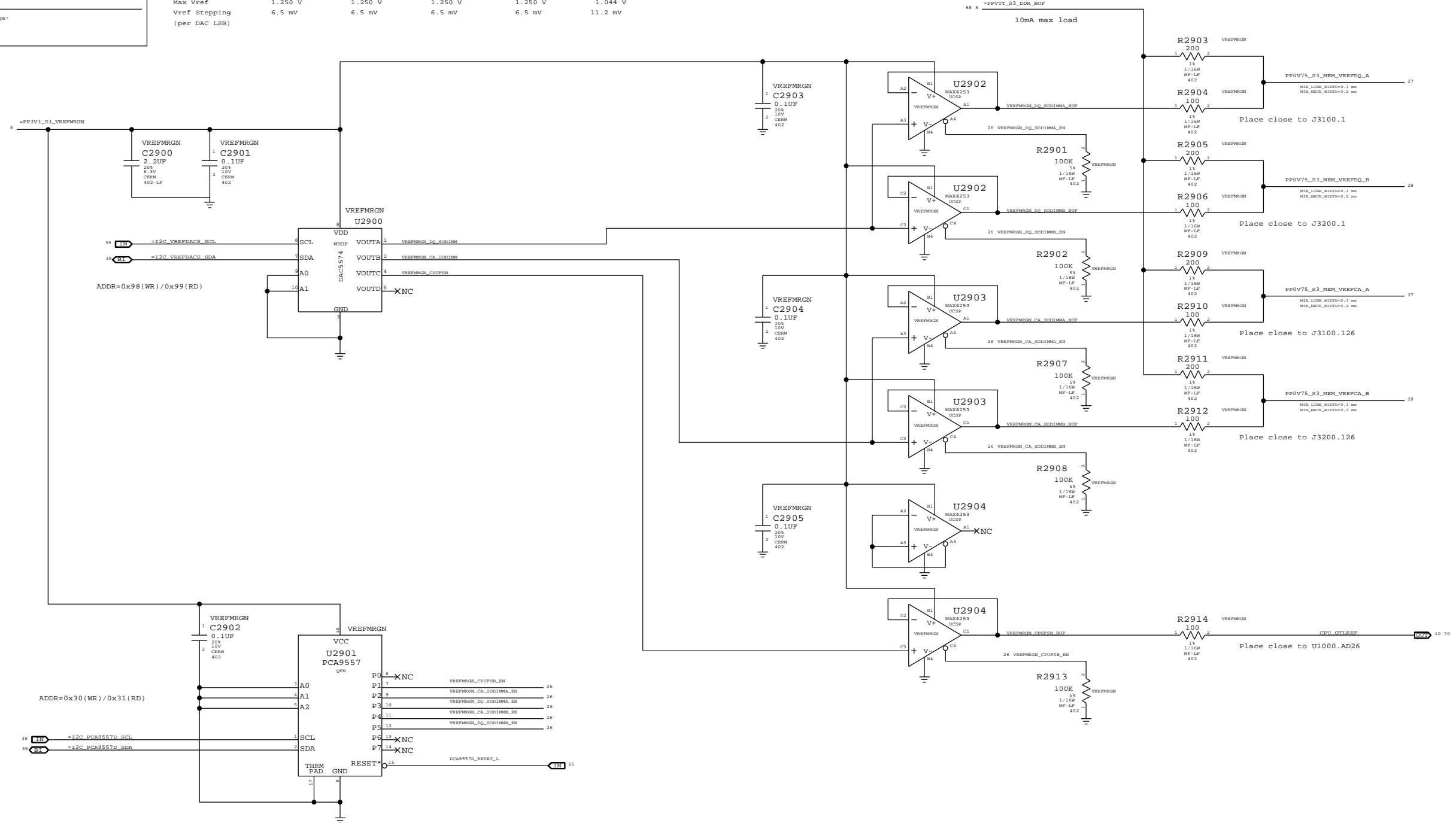
Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMRGN  
 - =PP3V3\_S5\_VREFMRGN  
 - =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
 - =I2C\_VREFDAC5\_SCL  
 - =I2C\_VREFDAC5\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
 VREFMRGN  
 NO\_VREFMRGN

| DAC channel                    | MEM A VREF DQ |          | MEM A VREF CA |          | MEM B VREF DQ |          | MEM B VREF CA |      | CPU FSB VREF |
|--------------------------------|---------------|----------|---------------|----------|---------------|----------|---------------|------|--------------|
|                                | A             | B        | A             | B        | A             | B        | C             |      |              |
| Min DAC code                   | 0x00          | 0x00     | 0x00          | 0x00     | 0x00          | 0x00     | 0x00          | 0x55 |              |
| Max DAC code                   | 0x87          | 0x87     | 0x87          | 0x87     | 0x87          | 0x87     | 0x87          | 0x55 |              |
| Max sink I                     | -3.75 mA      | -3.75 mA | -3.75 mA      | -3.75 mA | -3.75 mA      | -3.75 mA | -0.91 mA      |      |              |
| Max source I                   | 5 mA          | 5 mA     | 5 mA          | 5 mA     | 5 mA          | 5 mA     | 0.52 mA       |      |              |
| Nominal Vref                   | 0.75 V        | 0.75 V   | 0.75 V        | 0.75 V   | 0.75 V        | 0.75 V   | 0.70 V        |      |              |
| Min Vref                       | 0.375 V       | 0.375 V  | 0.375 V       | 0.375 V  | 0.375 V       | 0.375 V  | 0.091 V       |      |              |
| Max Vref                       | 1.250 V       | 1.250 V  | 1.250 V       | 1.250 V  | 1.250 V       | 1.250 V  | 1.044 V       |      |              |
| Vref Stepping<br>(per DAC LSB) | 6.5 mV        | 6.5 mV   | 6.5 mV        | 6.5 mV   | 6.5 mV        | 6.5 mV   | 11.2 mV       |      |              |

SO-DIMM A and SO-DIMM B Vref settings should be margined separately  
 (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

| PART NUMBER | QTY | DESCRIPTION                  | REFERENCE DES | CRITICAL | BOM OPTION  |
|-------------|-----|------------------------------|---------------|----------|-------------|
| 116S0004    | 1   | RES.MTL.FILM,0.5%,0402,SM,LP | R2903         | CRITICAL | NO_VREFMRGN |
| 116S0004    | 1   | RES.MTL.FILM,0.5%,0402,SM,LP | R2905         | CRITICAL | NO_VREFMRGN |
| 116S0004    | 1   | RES.MTL.FILM,0.5%,0402,SM,LP | R2909         | CRITICAL | NO_VREFMRGN |
| 116S0004    | 1   | RES.MTL.FILM,0.5%,0402,SM,LP | R2911         | CRITICAL | NO_VREFMRGN |

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

FSB/DDR3 Vref Margining

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Page Notes

Power aliases required by this page:

- PP1V5\_S0\_MEM\_A
- PP1V5\_S1\_MEM\_A
- PP0V75\_S0\_MEM\_VTT\_A
- PP0V75\_S1\_MEM\_VTT\_A
- PP0V75\_S0\_MEM\_A (2.5 - 3.3V)

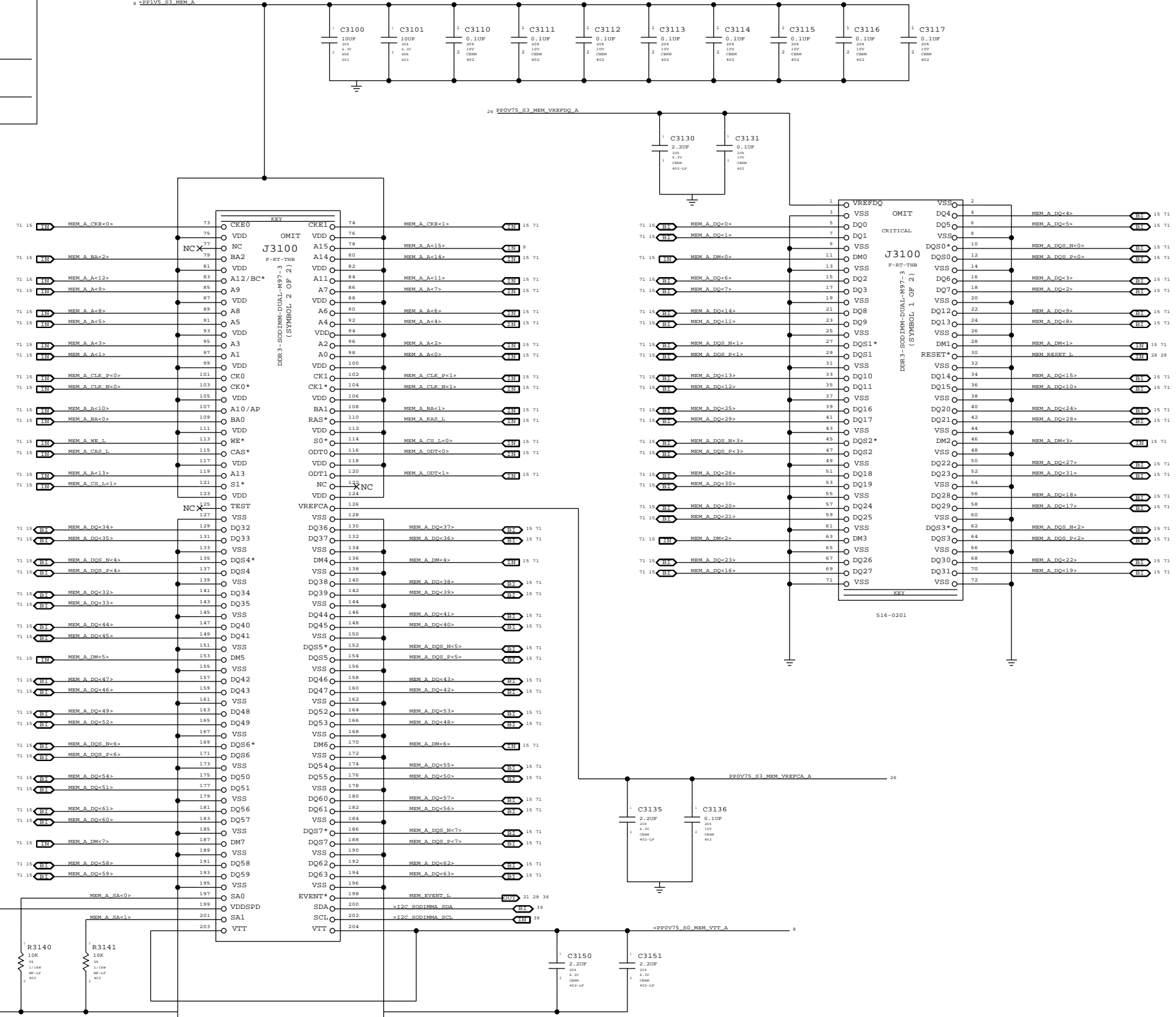
Signal aliases required by this page:

- I2C\_S0D19MA\_SCL
- I2C\_S0D19MA\_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



\*Factory\* (top) slot

SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

DDR3 SO-DIMM Connector A

Apple Inc.

051-7982 D

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BRANCH

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516-0201  
 SPD ADDR=Dx0(WR)/DxA1(RD)

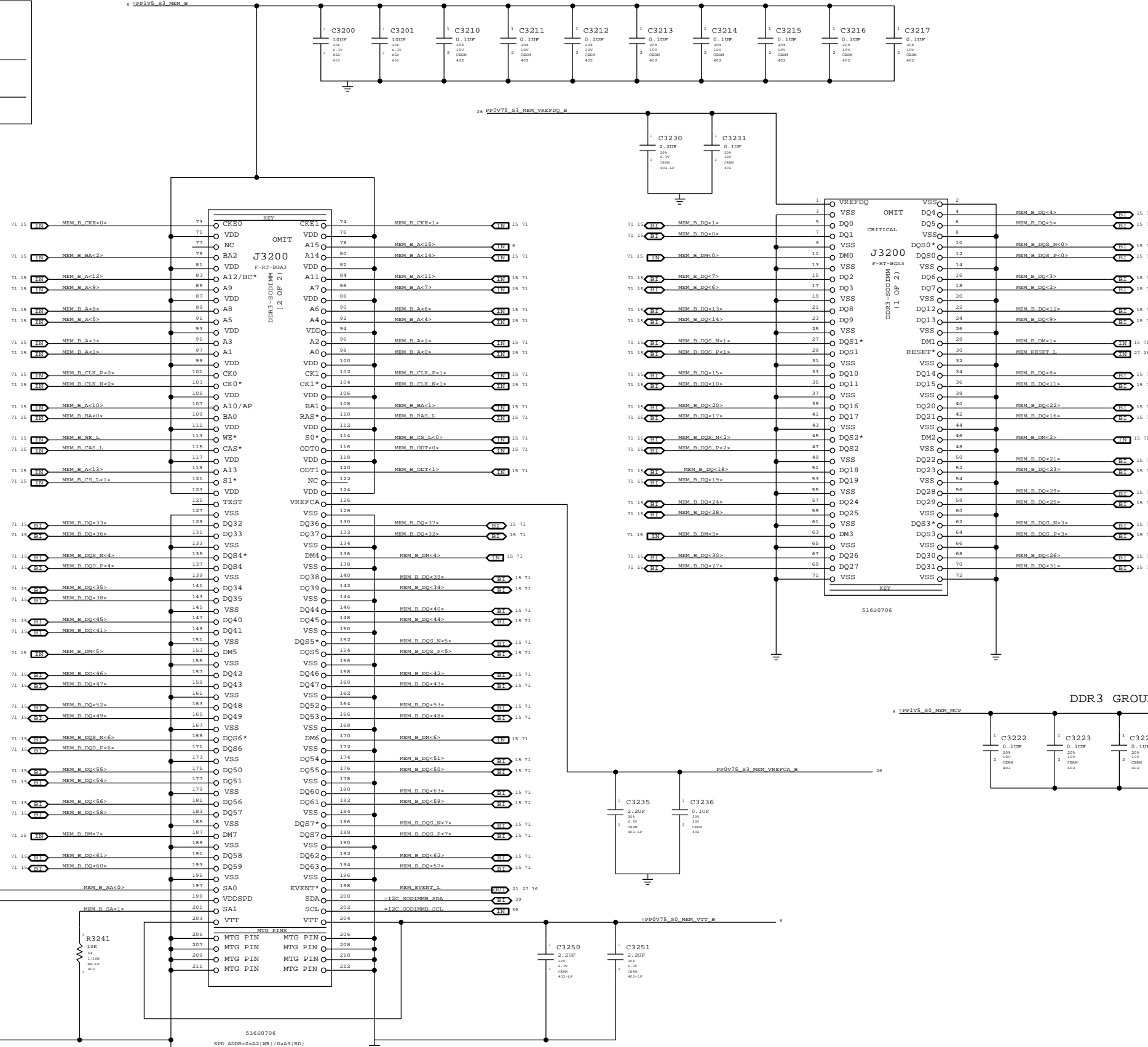
Page Notes

Power Alliances required by this page:  
 ->PP1V5\_E3\_MEM\_B  
 ->PP1V5\_E3\_MEM\_B  
 ->PP0V75\_E3\_MEM\_VTT\_B  
 ->PP0V75\_E3\_MEM\_VTT\_B  
 ->PP0V75\_E3\_MEM\_B (2.5 - 3.3V)

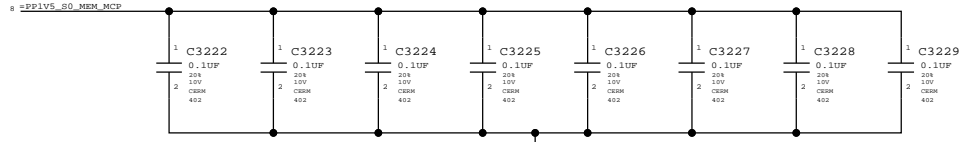
Signal Alliances required by this page:  
 ->I2C\_S0D1MM\_S0L  
 ->I2C\_S0D1MM\_S0A

ROM options provided by this page:  
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)



"Expansion" (bottom) slot

SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

**DDR3 SO-DIMM Connector B**

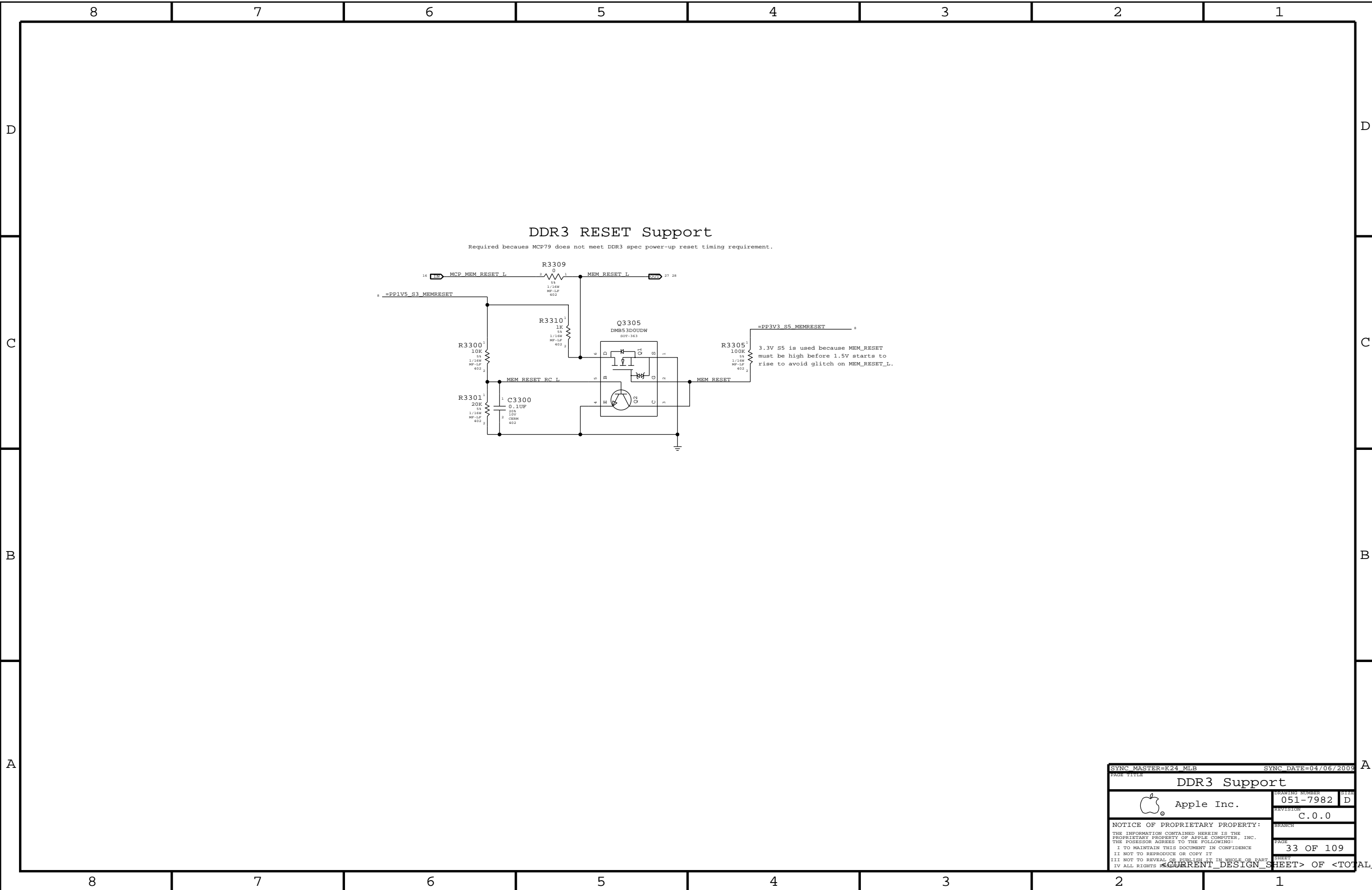
Apple Inc.

051-7982 D

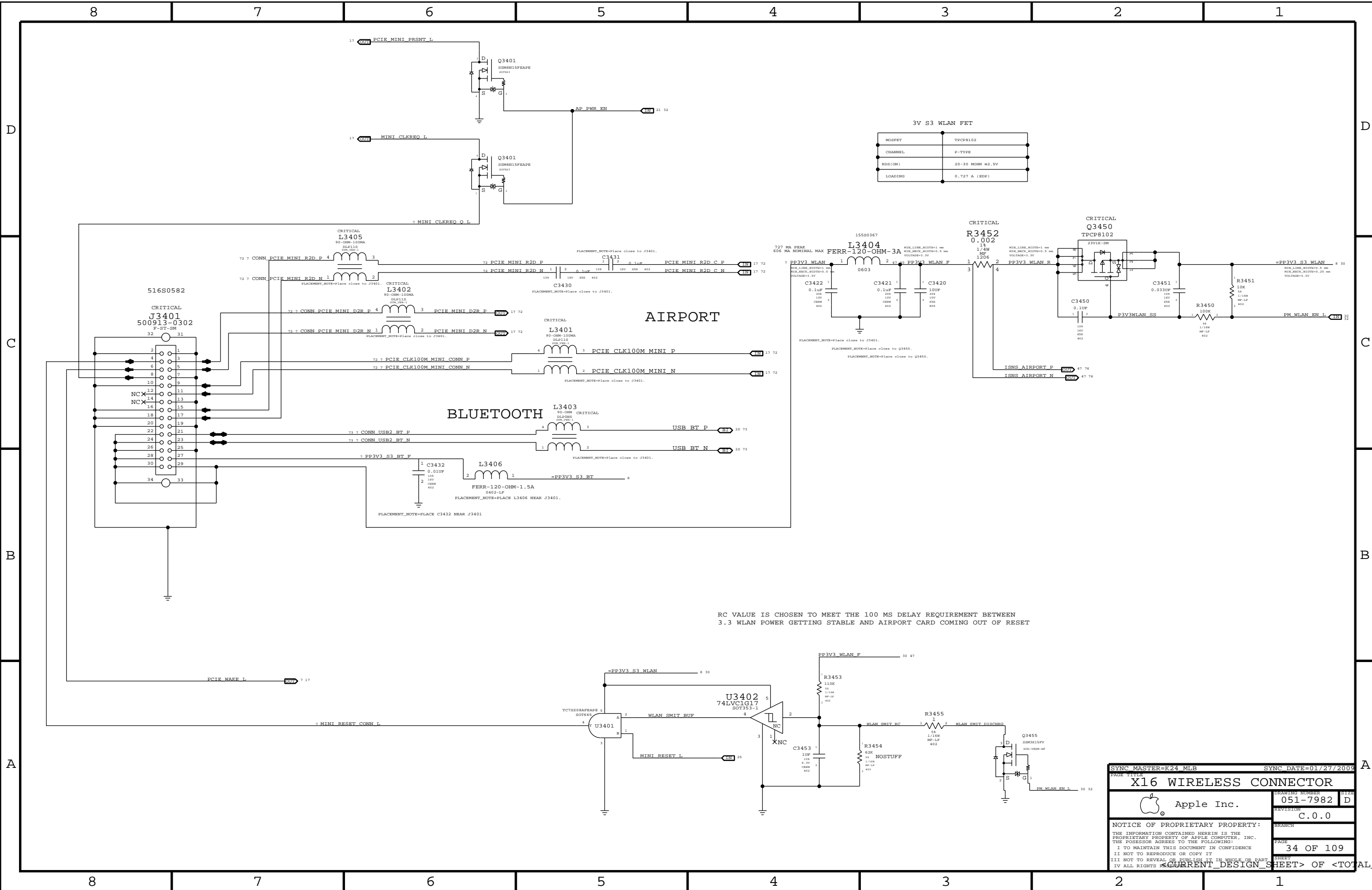
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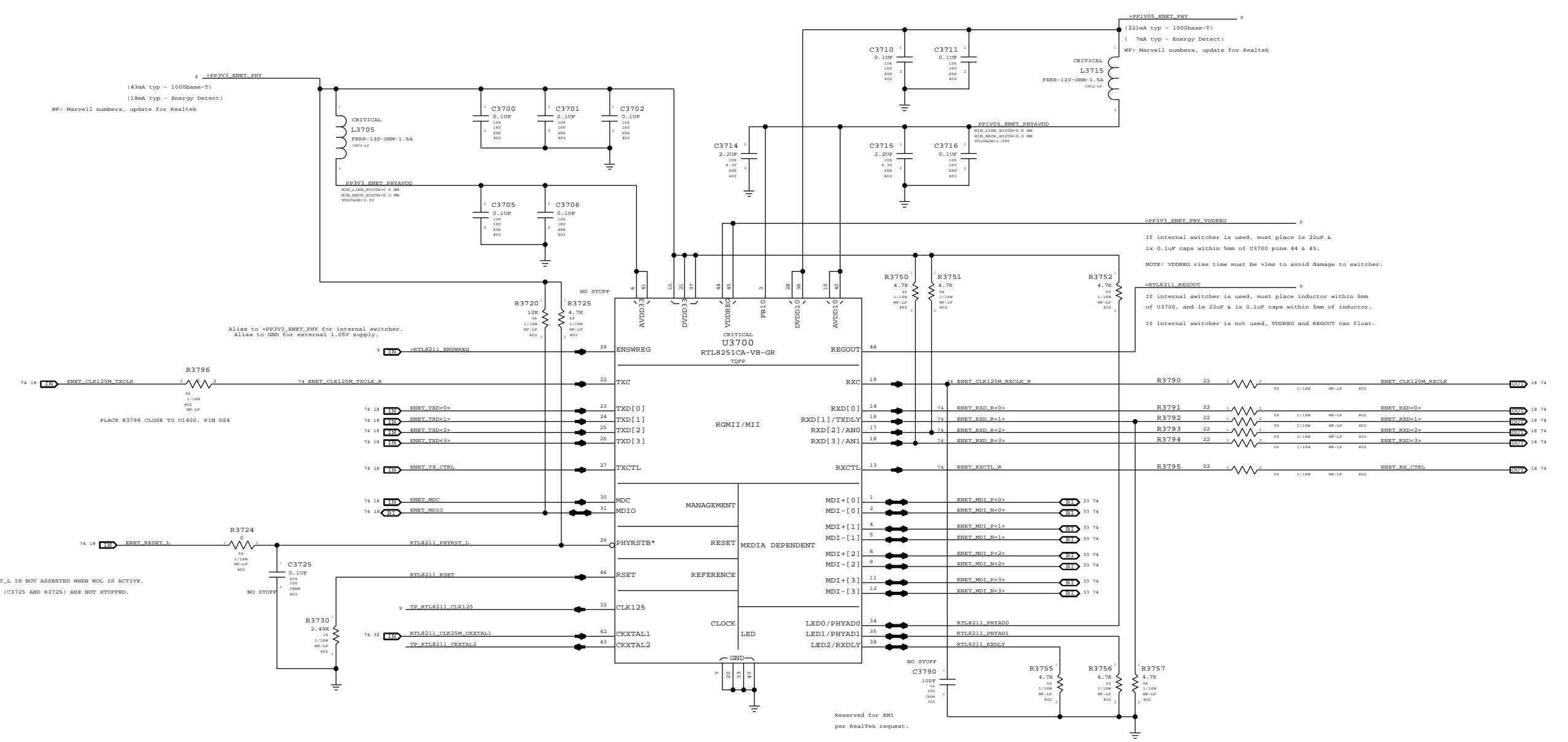


|   |  |                          |      |
|---|--|--------------------------|------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009     |      |
| DDR3 Support  |  |                          |      |
| Apple Inc.  |  | DESIGN NUMBER            | SIZE |
|   |  | 051-7982                 | D    |
|   |  | REVISION                 |      |
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RC VALUE IS CHOSEN TO MEET THE 100 MS DELAY REQUIREMENT BETWEEN 3.3 WLAN POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET

|   |  |   |            |
|---|--|---|------------|
| PAGE TITLE  |  | SYNC DATE=01/27/2009                        |            |
| X16 WIRELESS CONNECTOR  |  |   |            |
| Apple Inc.  |  | DRAWING NUMBER                              | 051-7982 D |
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=PP3V3\_ENET\_PHY  
 (43mA typ - 1000base-T)  
 (19mA typ - Energy Detect)  
 MF: Marvell numbers, update for Realtek

=PP1V05\_ENET\_PHY  
 (221mA typ - 1000base-T)  
 ( 7mA typ - Energy Detect)  
 MF: Marvell numbers, update for Realtek

Alias to =PP3V3\_ENET\_PHY for internal switcher.  
 Alias to GND for external 1.05V supply.

=PP1V05\_ENET\_PHY\_VDDREG  
 If internal switcher is used, must place 1x 22uF & 1x 0.1uF caps within 5mm of U3700 pins 44 & 45.  
 NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

=RTL8211\_RKQOUT  
 If internal switcher is used, must place inductor within 5mm of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.  
 If internal switcher is not used, VDDREG and RKQOUT can float.

PLACE R3796 CLOSE TO U1400, PIN D24

ENET\_RESET\_L IS NOT ASSERTED WHEN WOL IS ACTIVE.  
 HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.

Reserved for EMI  
 per Realtek request.

Configuration Settings:  
 PHYAD = 01 (PHY Address 00001)  
 AN[1:0] = 11 (Full auto-negotiation)  
 RXDLY = 0 (RXCLK transitions with data)  
 TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

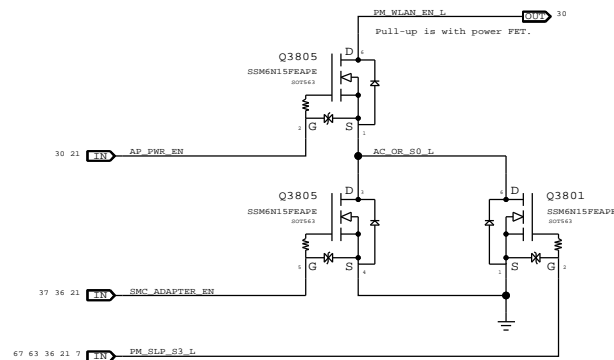
Ethernet PHY (RTL8211CL)

Apple Inc.  
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 SHEET: 1

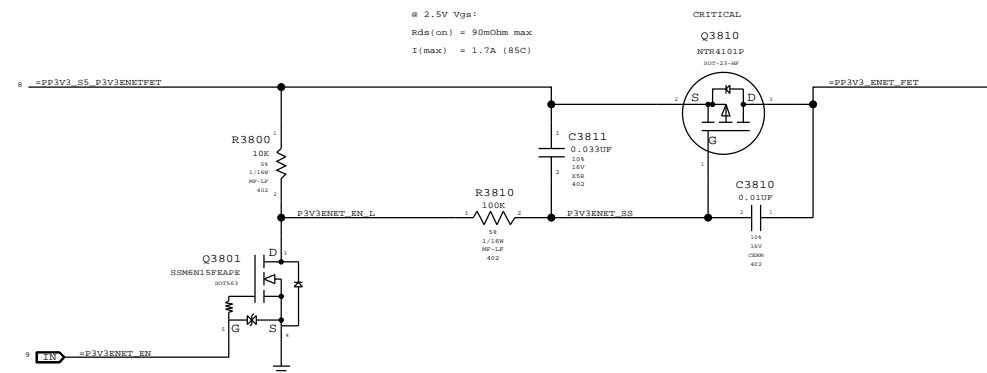
### WLAN Enable Generation

\*WLAN\* = (\*S3\* && \*AP\_PWR\_EN\* && (\*AC\* || \*SD\*))  
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP\_PWR\_EN signal.



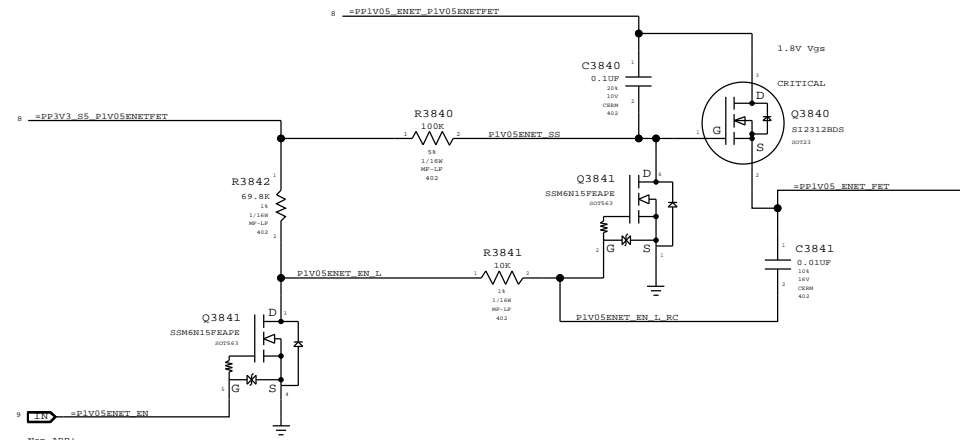
### 3.3V ENET FET

@ 2.5V Vgs!  
 Rds(on) = 90mOhm max  
 I(max) = 1.7A (85C)



MOBILE:  
 Recommend aliasing PM\_SLP\_RMOT\_L and  
 =PIV3ENET\_EN. Nets separated on  
 ARB for alternate power options.

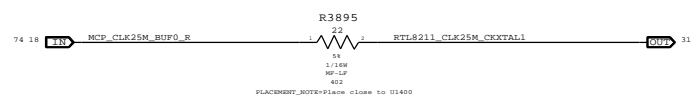
### 1.05V ENET FET



Non-ARB:  
 Recommend aliasing PM\_SLP\_RMOT\_L and  
 =PIV05ENET\_EN. Nets separated on  
 ARB for alternate power options.

### RTL8211 25MHz Clock

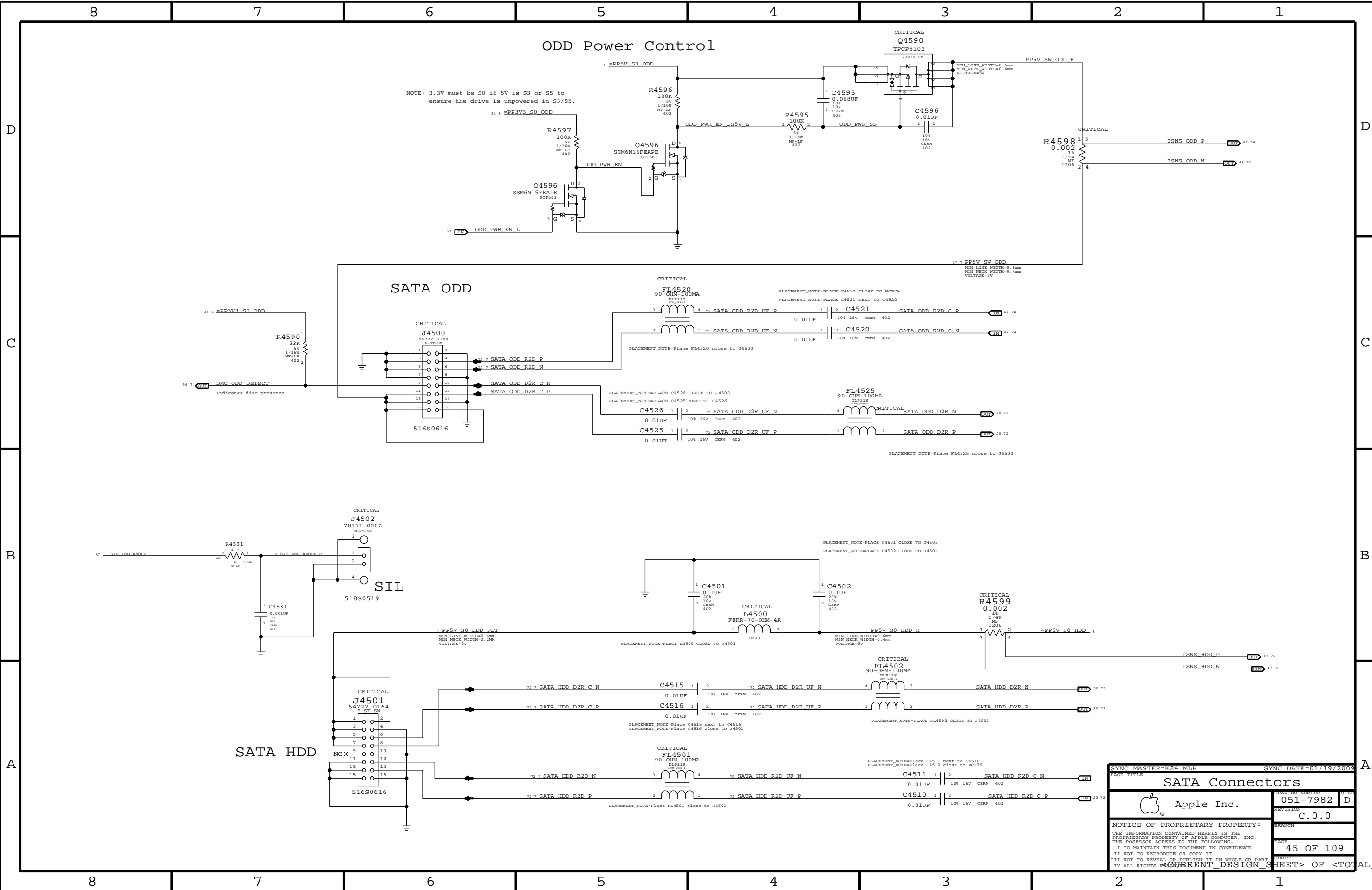
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMOT rails are powered.  
 Designs must ensure PHY is powered whenever RMOT rails are, or use separate crystal.



|   |  |                      |                   |
|---|--|----------------------|-------------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009 |                   |
| Ethernet & AirPort Support  |  |                      |                   |
| Apple Inc.  |  | 051-7982             | D                 |
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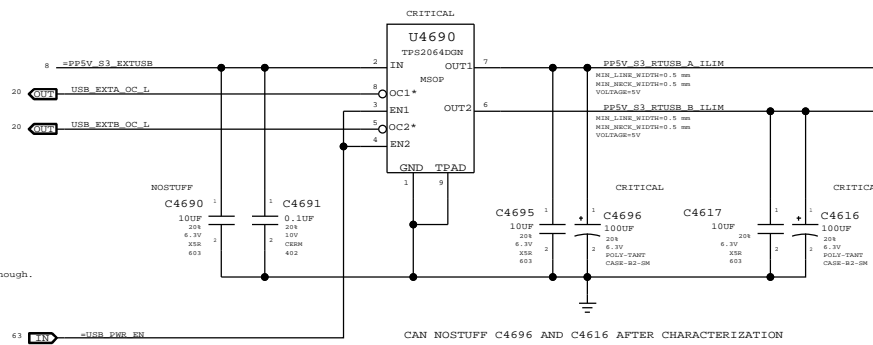
SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

**SATA Connectors**

|   |                                   |
|---|-----------------------------------|
| Apple Inc.  | DRAWING NUMBER<br><b>051-7982</b> |
| REVISION<br><b>C.0.0</b>  | SHEET<br><b>D</b>                 |
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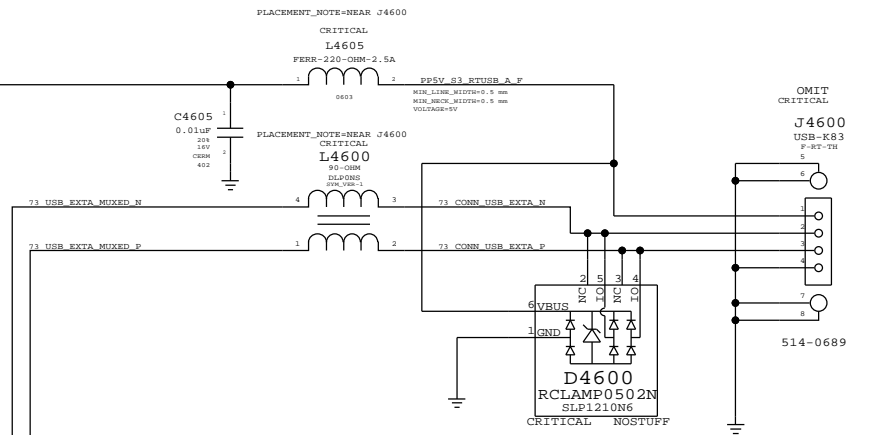
POR IS PLASTIC USB CONNECTOR PARTS BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS HAVE BEEN USED AS ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

### Port Power Switch



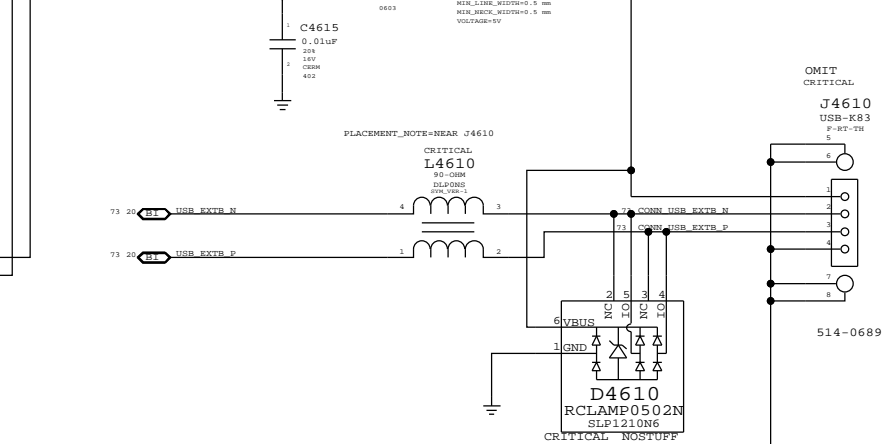
We can remove C4690 later if the output cap of the 5V\_S5 regulator is close enough.

### USB PORT A (FRONT PORT)

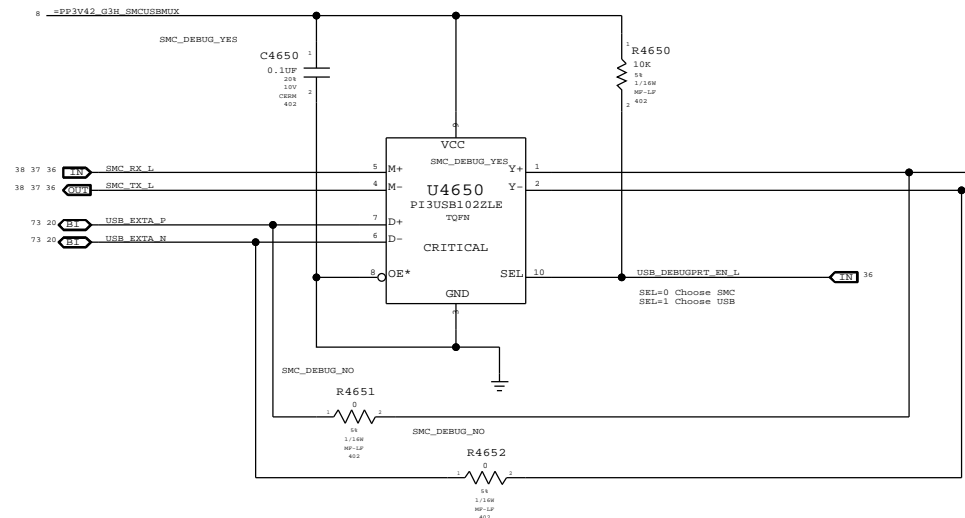


We can add protection to 5v if we want, but leaving NC for now

### USB PORT B (BACK PORT)



### USB/SMC Debug Mux

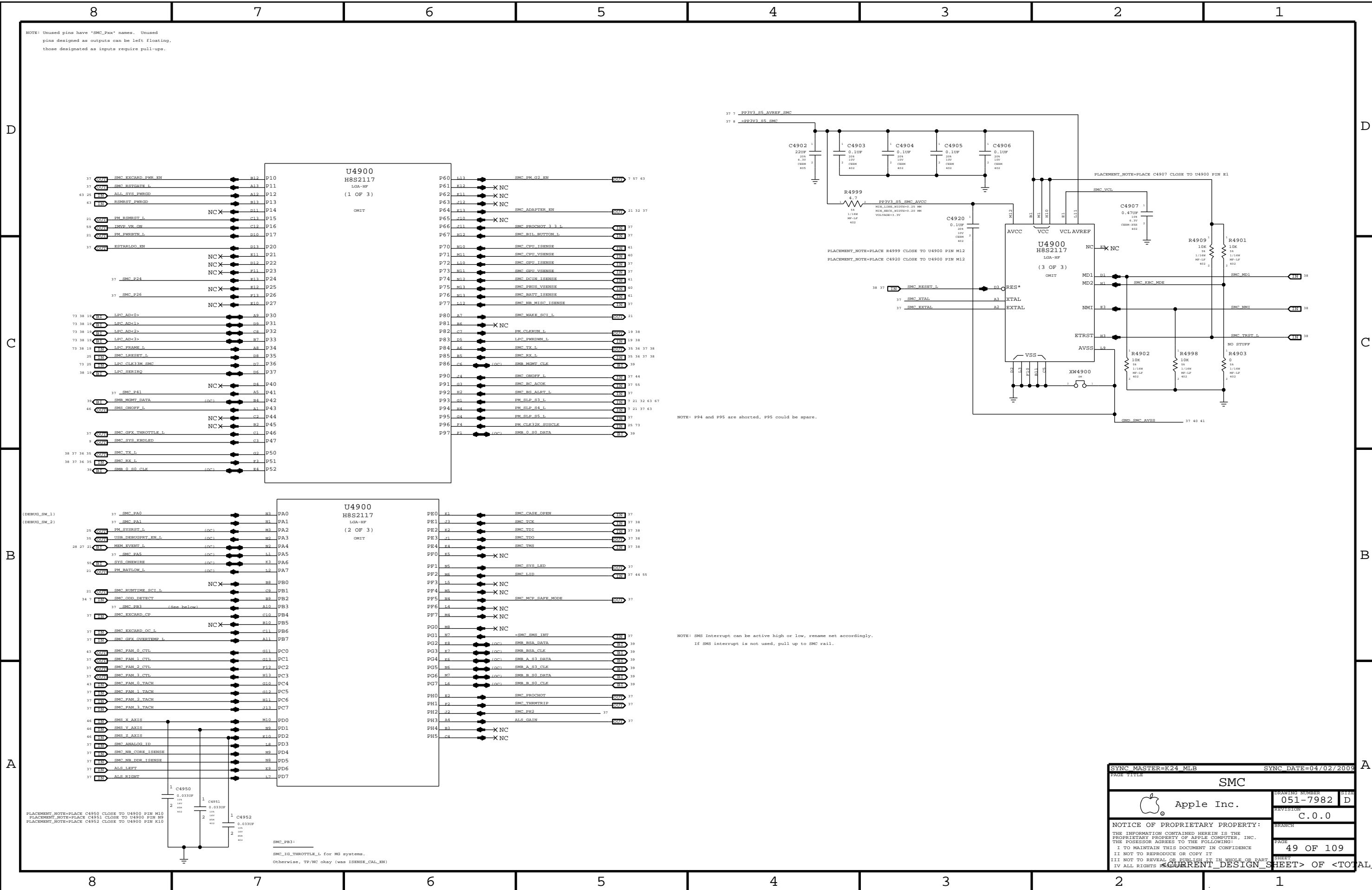


SYNC MASTER=K24 MLB SYNC DATE=02/05/2009

### External USB Connectors

|            |  |                |           |
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| Apple Inc. |  | DRAWING NUMBER | 051-7982  |
|            |  | REVISION       | C.0.0     |
|            |  | PAGE           | 46 OF 109 |
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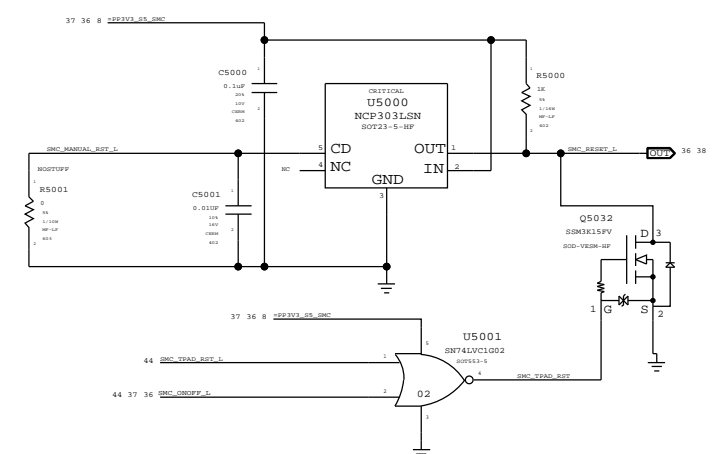
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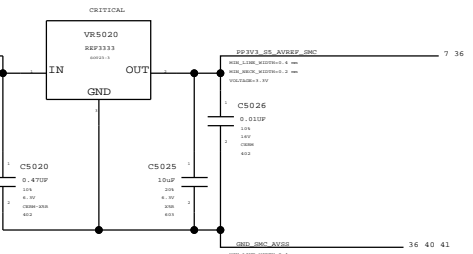
SYNC MASTER=K24 MLB SYNC DATE=04/02/2009

|   |  |                |           |
|---|--|----------------|-----------|
| SMC   |  | DRAWING NUMBER | M122      |
| Apple Inc.  |  | 051-7982       | D         |
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### SMC Reset "Button" / Brownout Detect

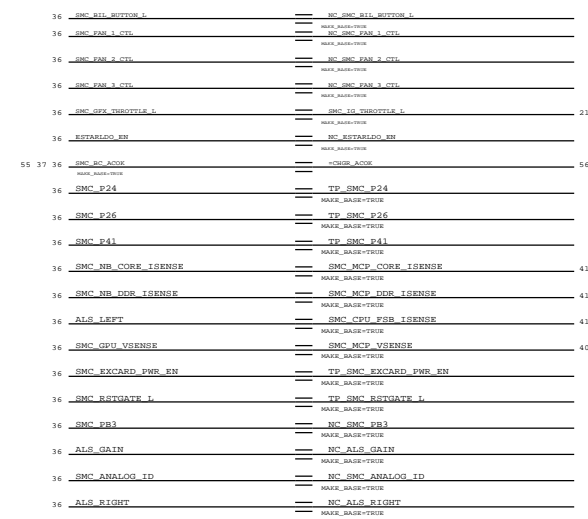
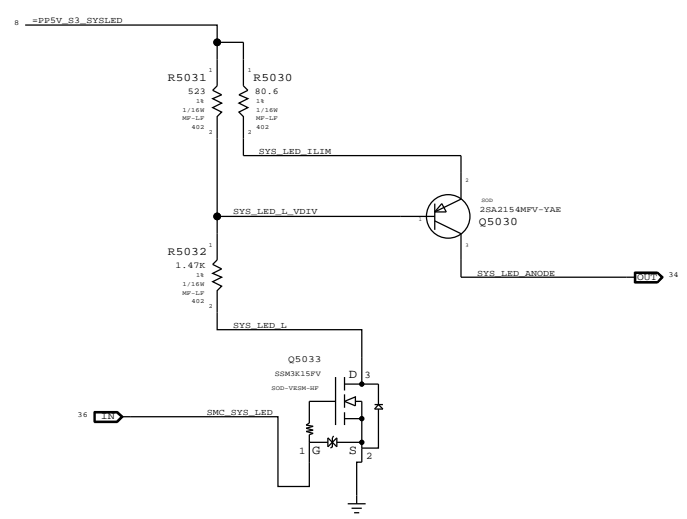


### SMC AVREF Supply

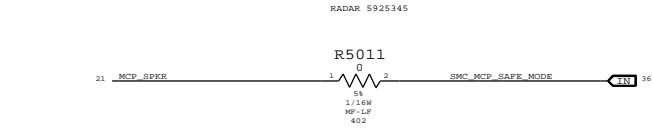


| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:            |
|-------------|---------------------------|------------|---------|----------------------|
| 35301381    | 35301912                  |            | ALL     | 18L6002-13, INTERSIL |

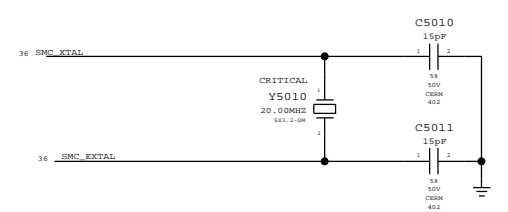
### System (Sleep) LED Circuit



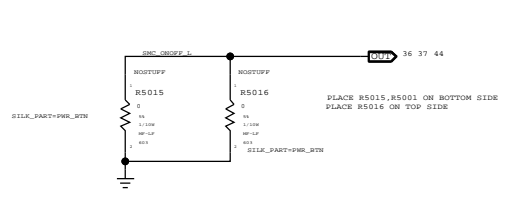
### MCP\_SAFE\_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE



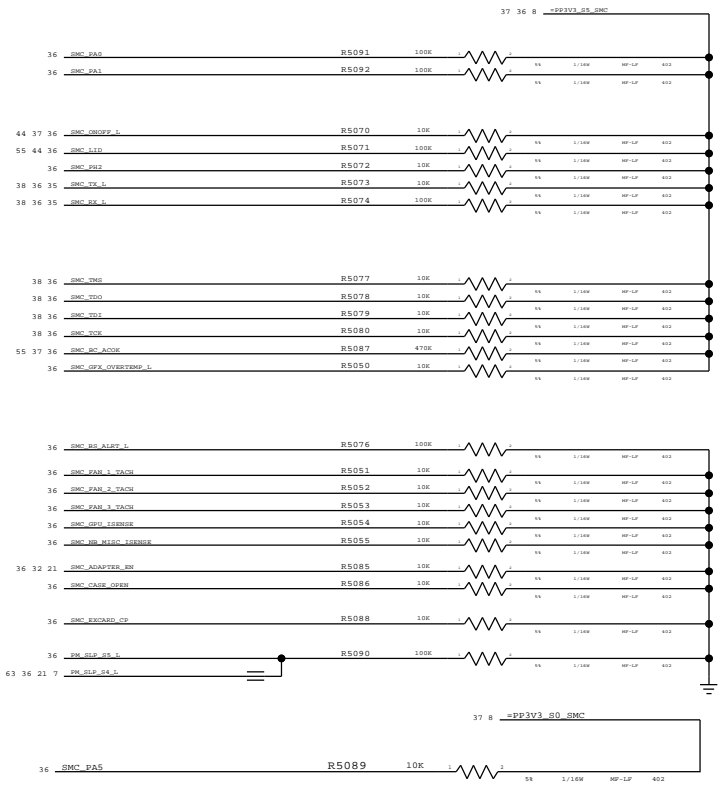
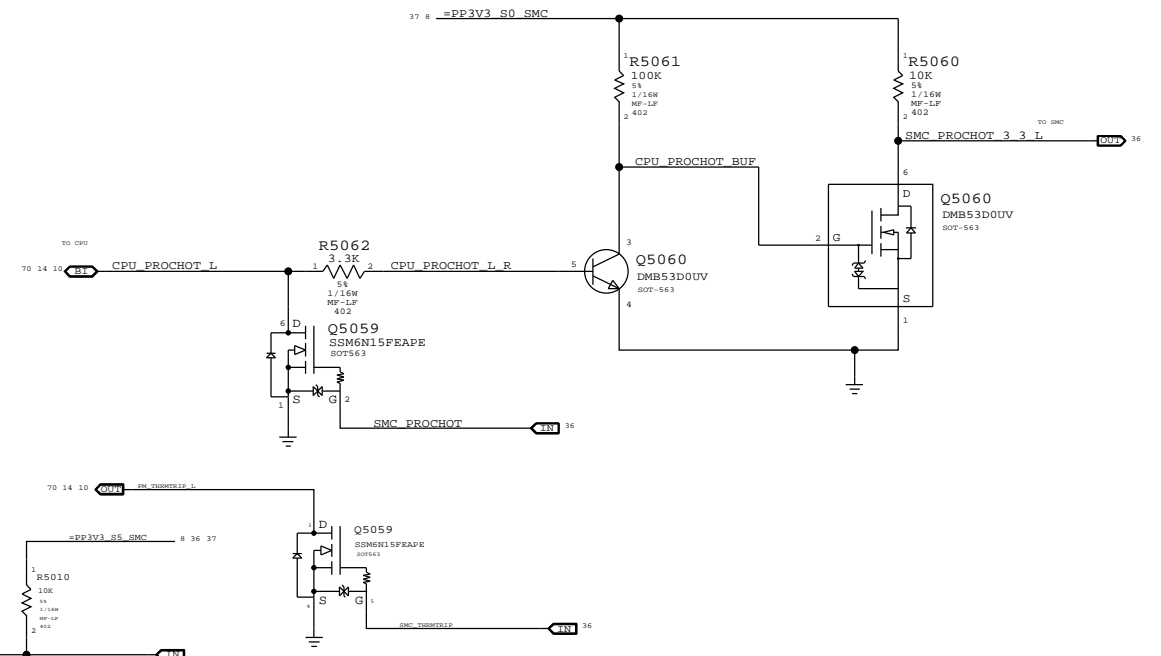
### SMC Crystal Circuit



### Debug Power "Button"



### SMC FSB to 3.3V Level Shifting

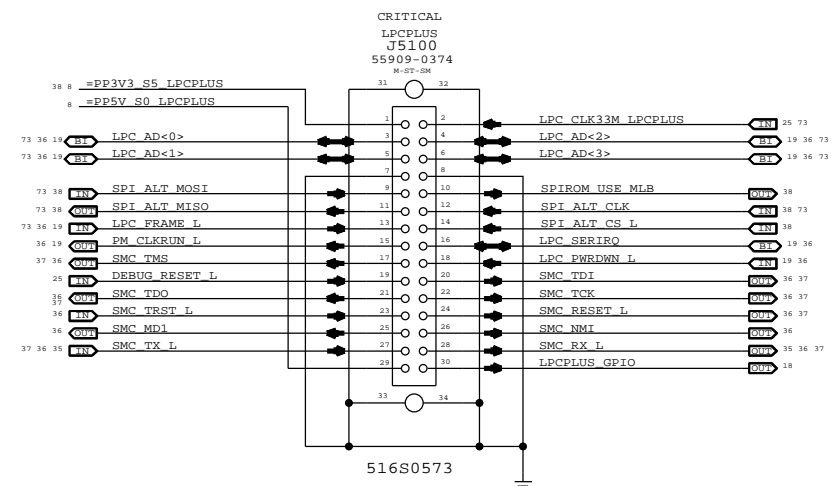


SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

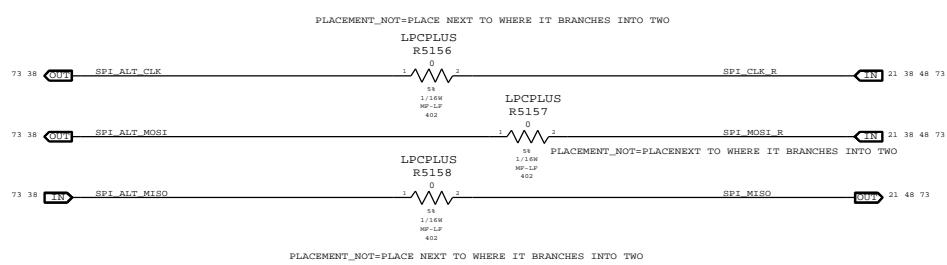
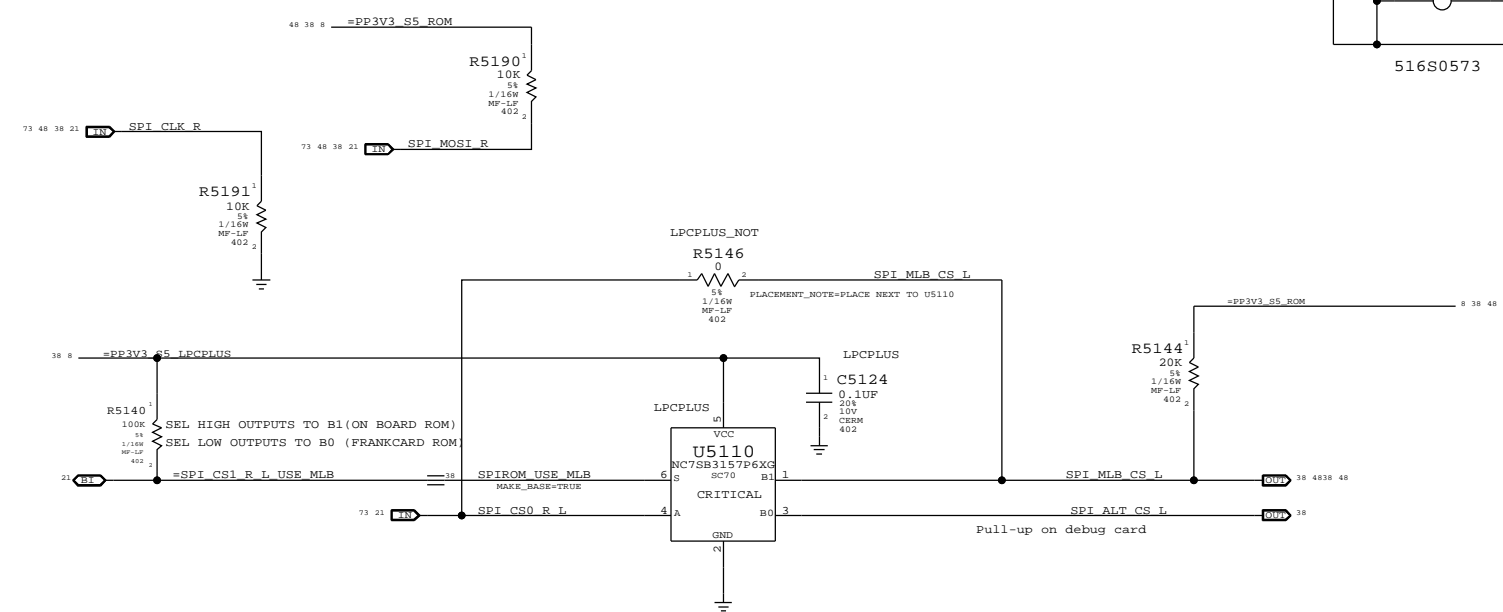
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|---|-----------------------------------|
| <b>SMC Support</b>  |                                   |
| Apple Inc.  | DRAWING NUMBER<br><b>051-7982</b> |
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| REVISION<br><b>C.0.0</b>  | PAGE<br><b>50 OF 109</b>          |

8 7 6 5 4 3 2 1

### LPC+SPI Connector



### Alternate SPI ROM Support

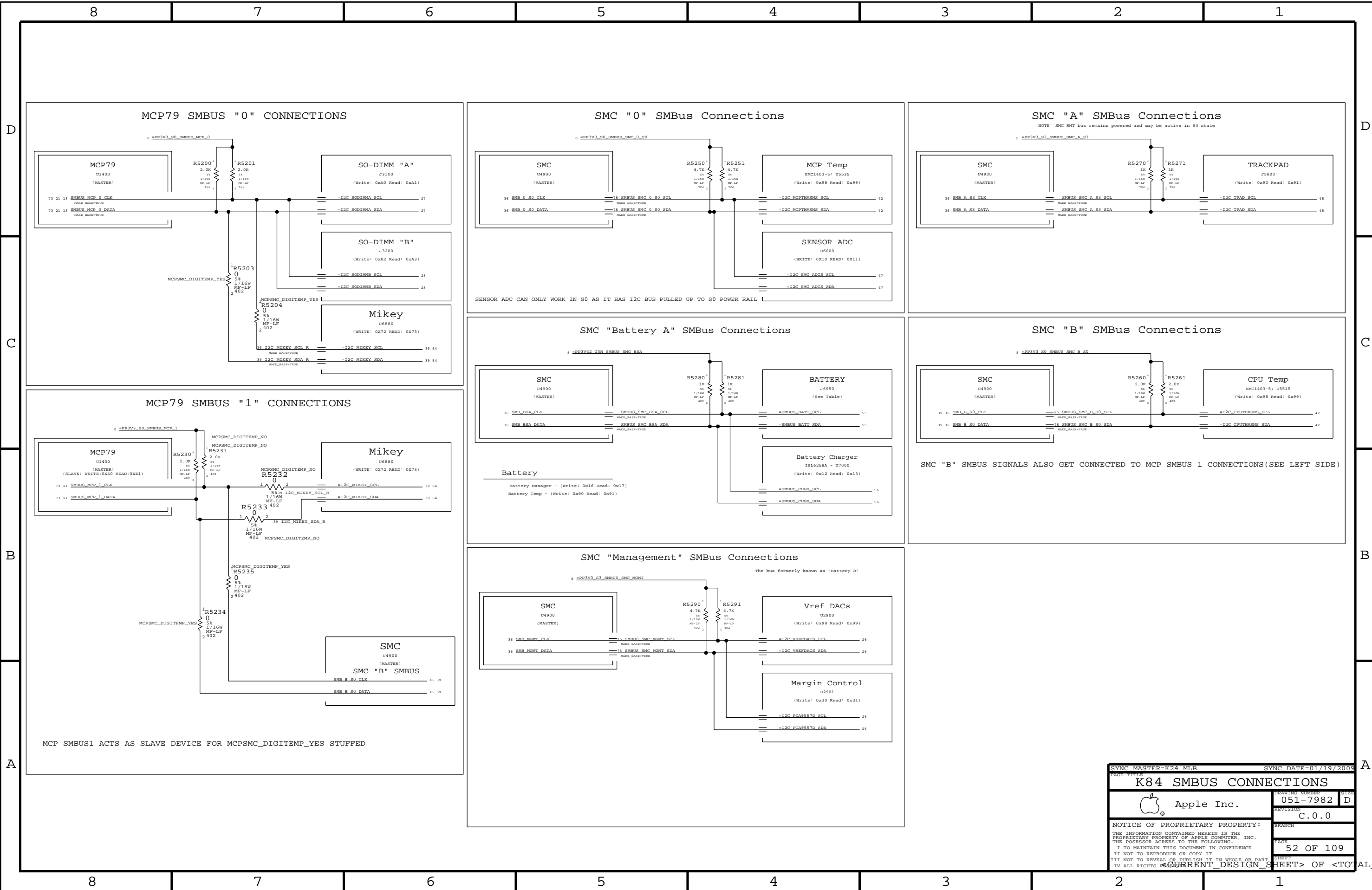


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|---|--|---------------------------|--|
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| PAGE TITLE<br><b>LPC+SPI Debug Connector</b>  |  |                           |  |
| DRAWING NUMBER<br><b>051-7982</b>   |  | REVISION<br><b>D</b>      |  |
| DRAWING NUMBER<br><b>051-7982</b>   |  | REVISION<br><b>C.0.0</b>  |  |
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8 7 6 5 4 3 2 1

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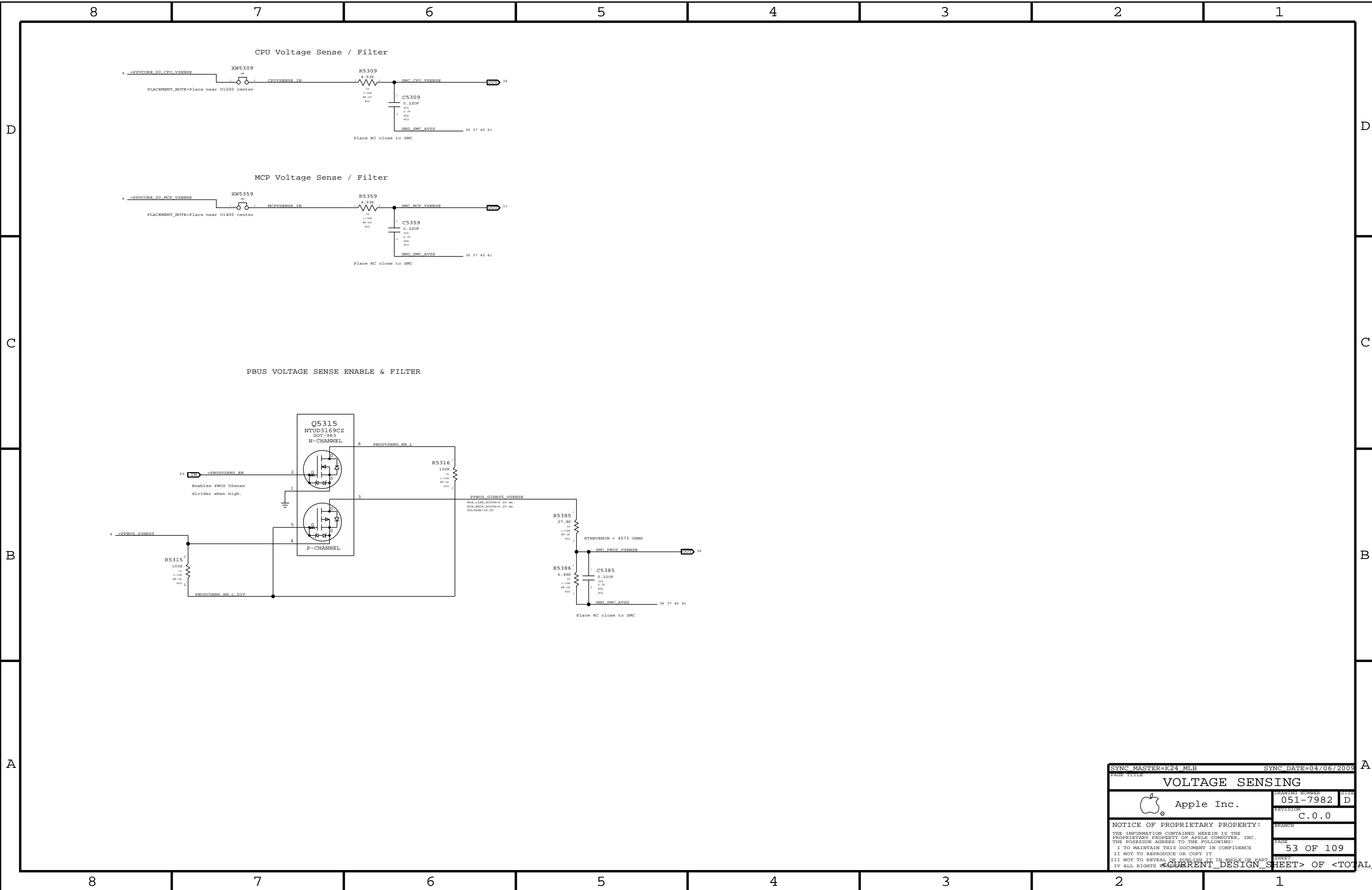
SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

**K84 SMBUS CONNECTIONS**

Apple Inc.  
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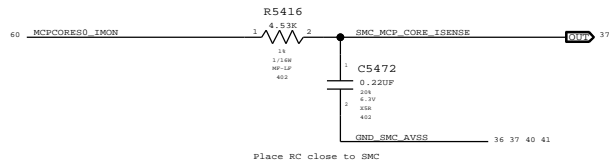
PAGE: 52 OF 109  
 SHEET: 1



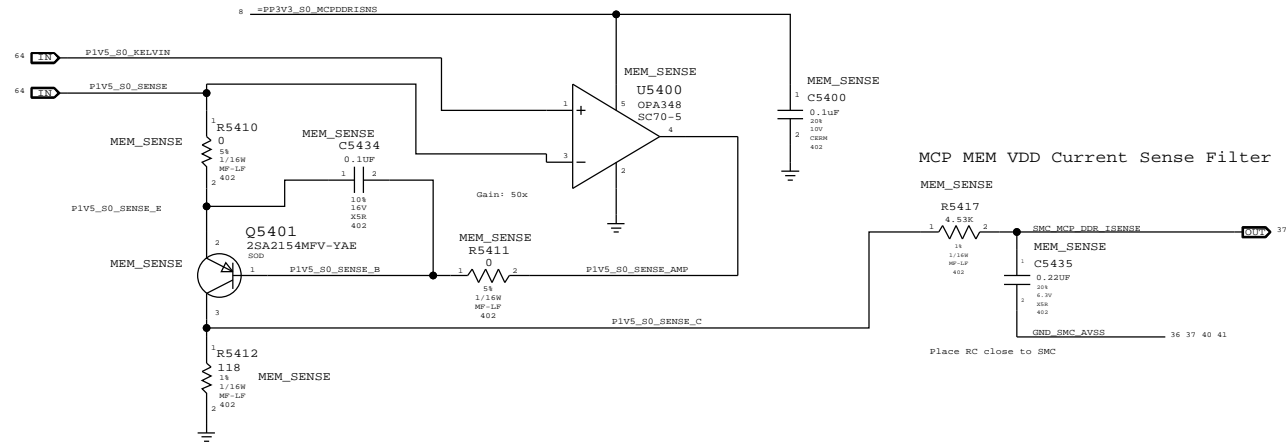
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| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009 |           |
| PAGE TITLE  |  |                      |           |
| <b>VOLTAGE SENSING</b>  |  |                      |           |
|   |  | DESIGN NUMBER        | 051-7982  |
|   |  | REVISION             | D         |
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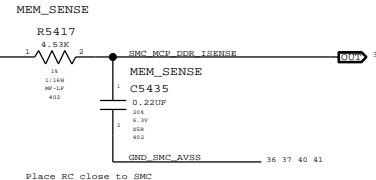
MCP VCore Current Sense Filter



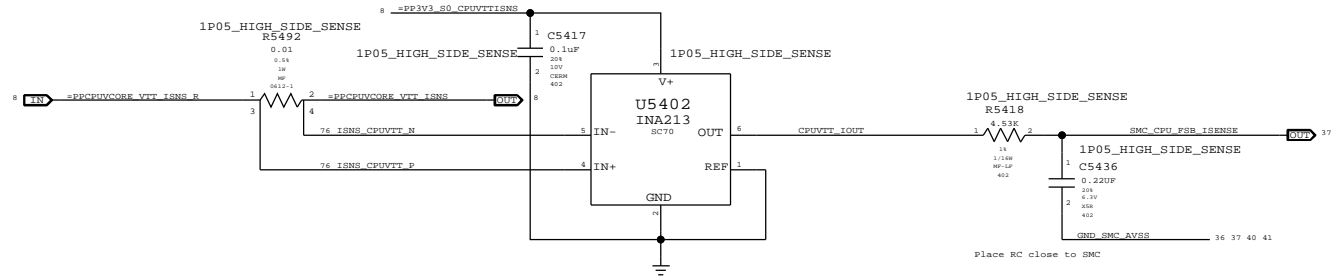
MCP MEM VDD Current Sense



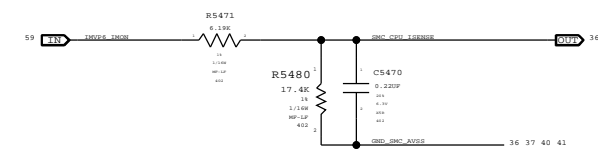
MCP MEM VDD Current Sense Filter



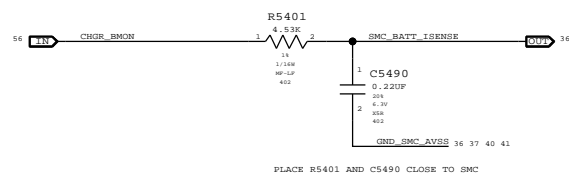
CPU 1.05V AND CPU VCore HIGH SIDE CURRENT SENSE



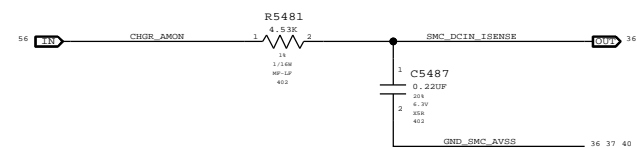
CPU VCore Load Side Current Sense / Filter



DC-IN (BMON) CURRENT SENSE



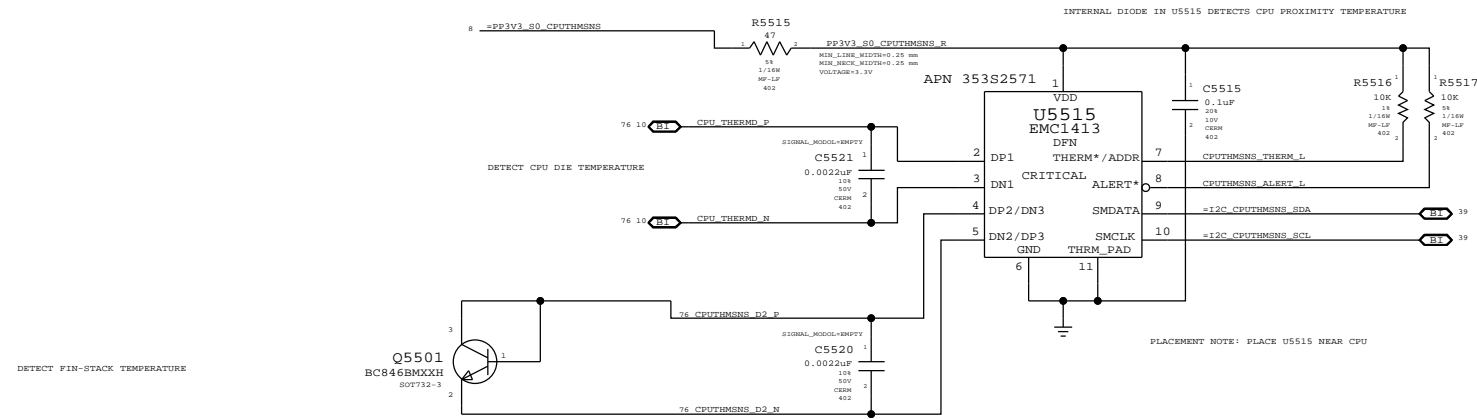
DC-IN (AMON) CURRENT SENSE



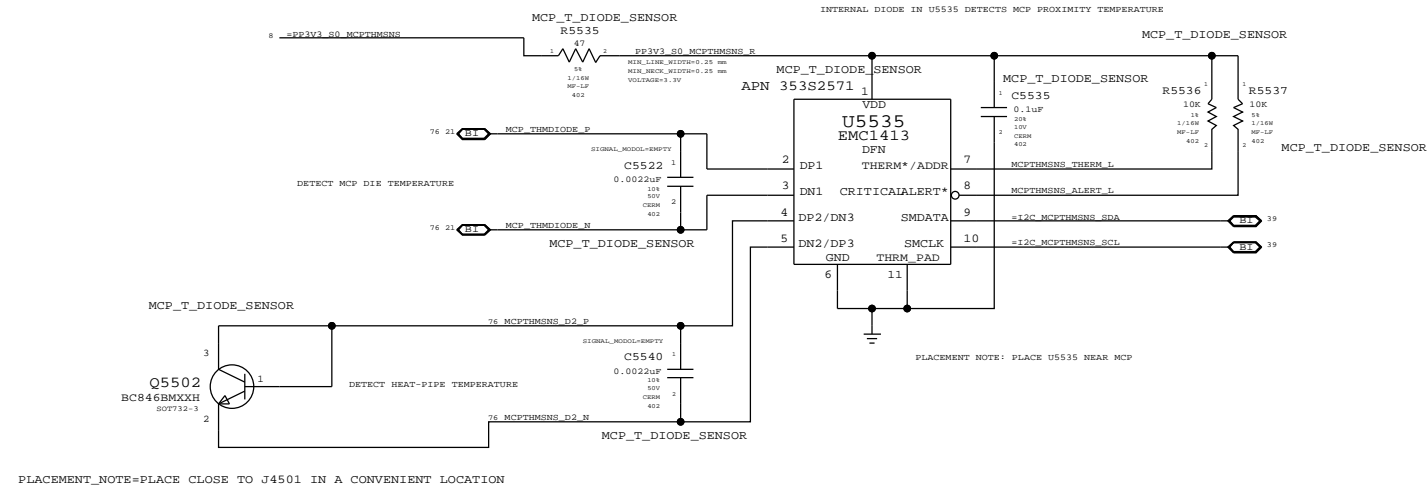
SYNC MASTER=K24 MLB SYNC DATE=01/27/2009

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### CPU T-Diode Thermal Sensor

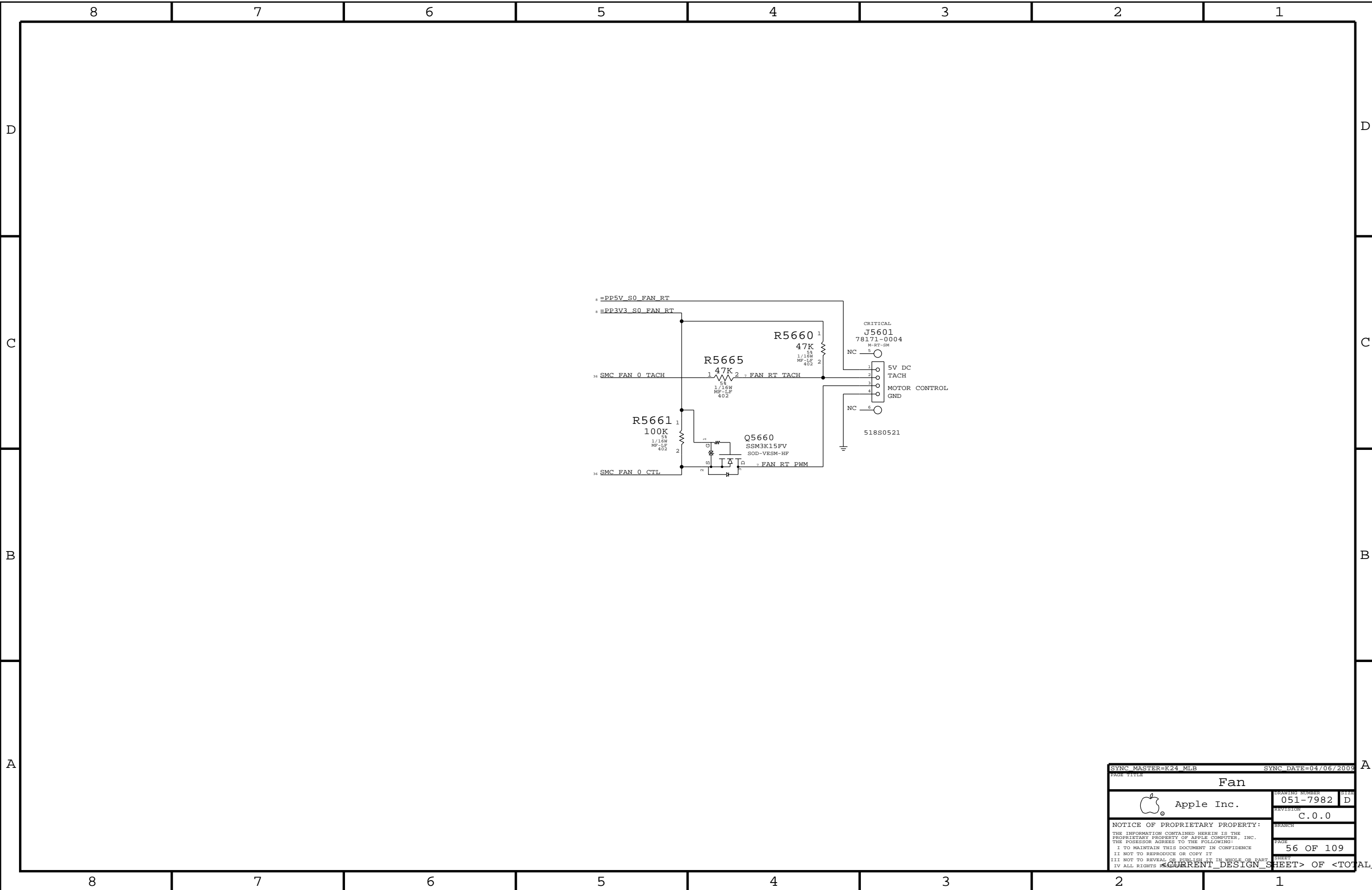


### MCP T-Diode Thermal Sensor



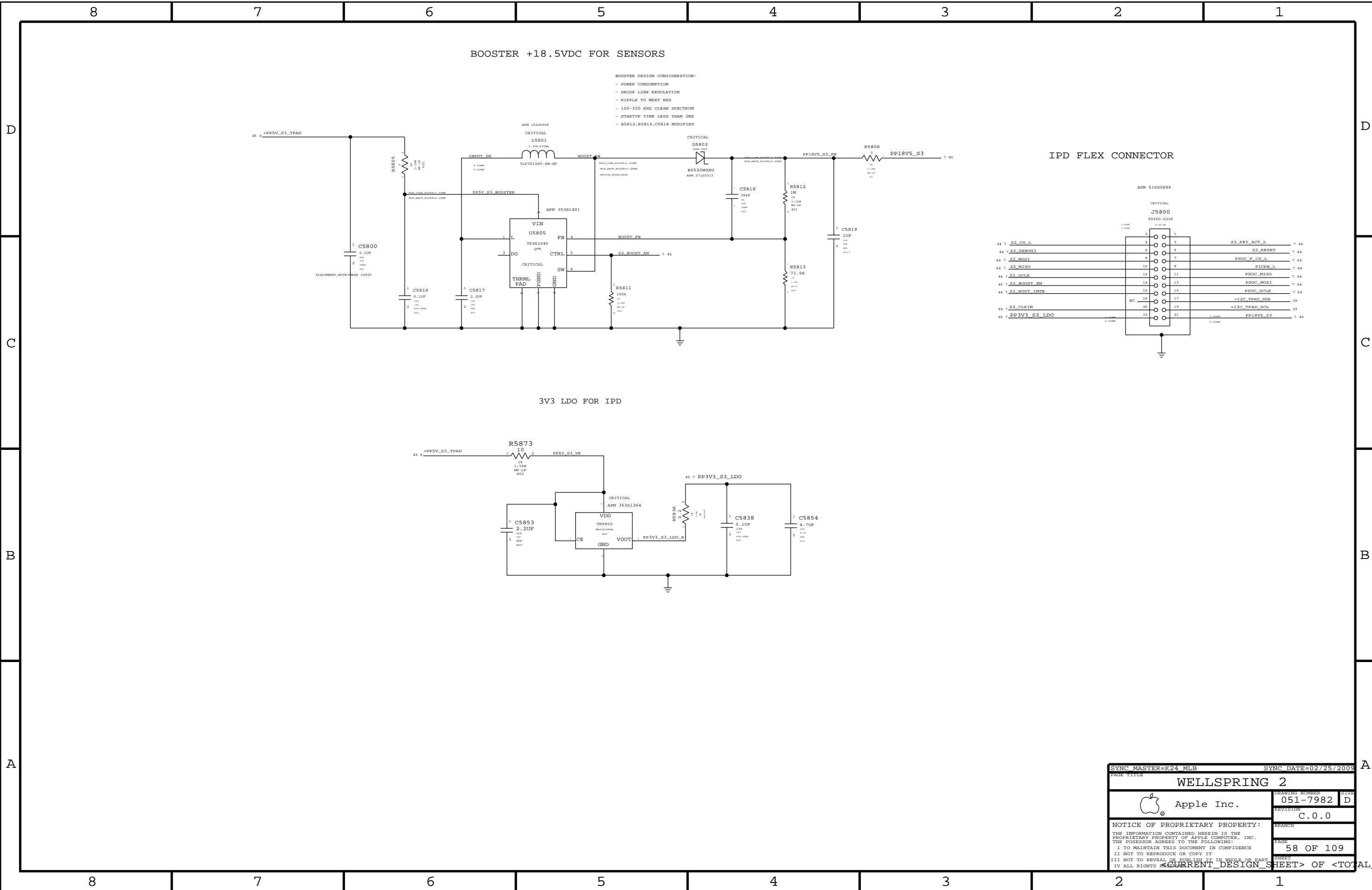
SYNC MASTER=K24 MLB SYNC DATE=02/04/2009

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| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009 |      |
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| Apple Inc.  |  | DRAWING NUMBER       | SIZE |
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|   |  | REVISION             |      |
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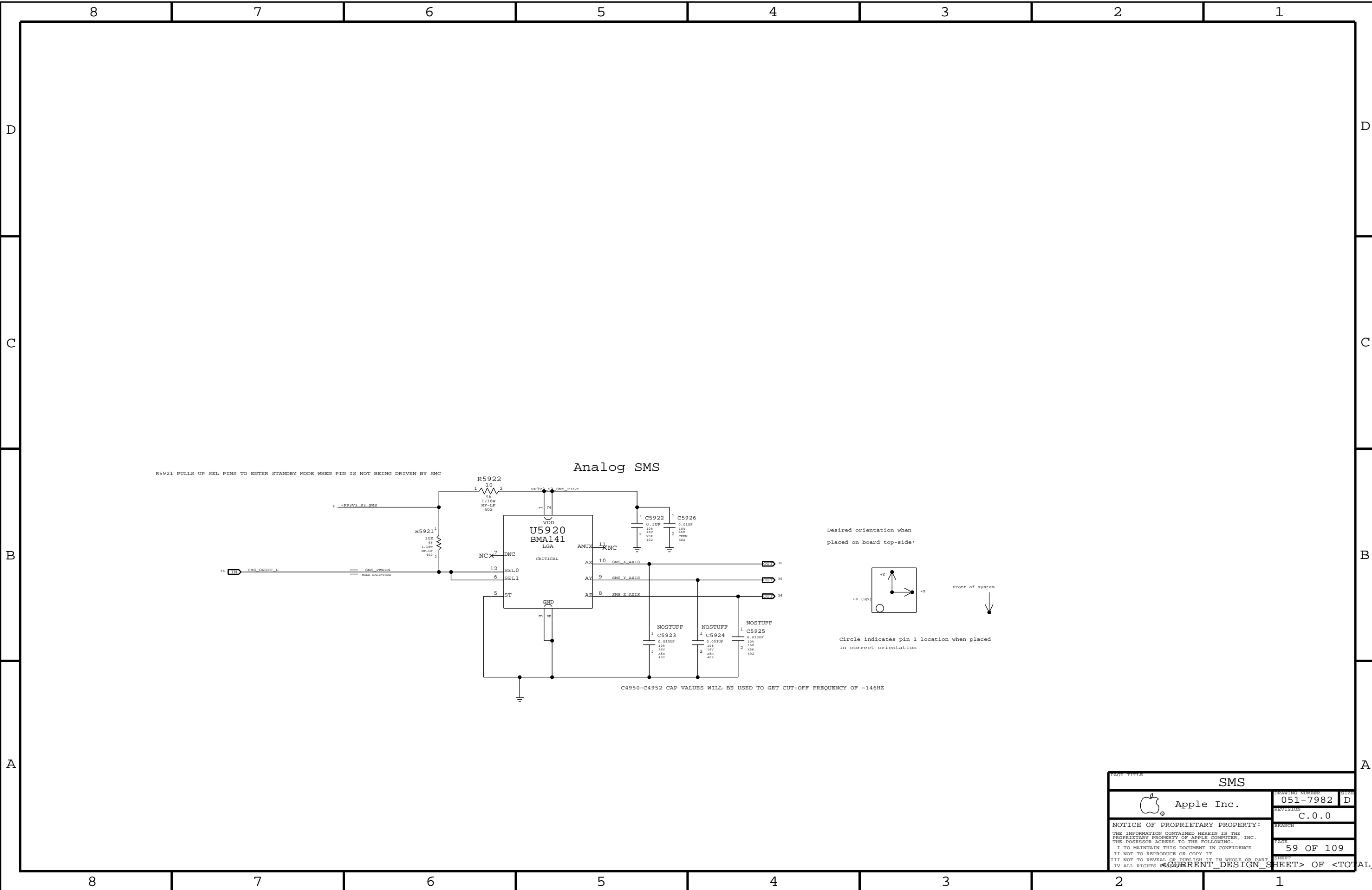
**BOOSTER +18.5VDC FOR SENSORS**

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
  - DROOP LINE REGULATION
  - RIPPLE TO MEET ERS
  - 100-300 KHZ CLEAN SPECTRUM
  - STARTUP TIME LESS THAN 2MS
  - R5812, R5813, C5818 MODIFIED

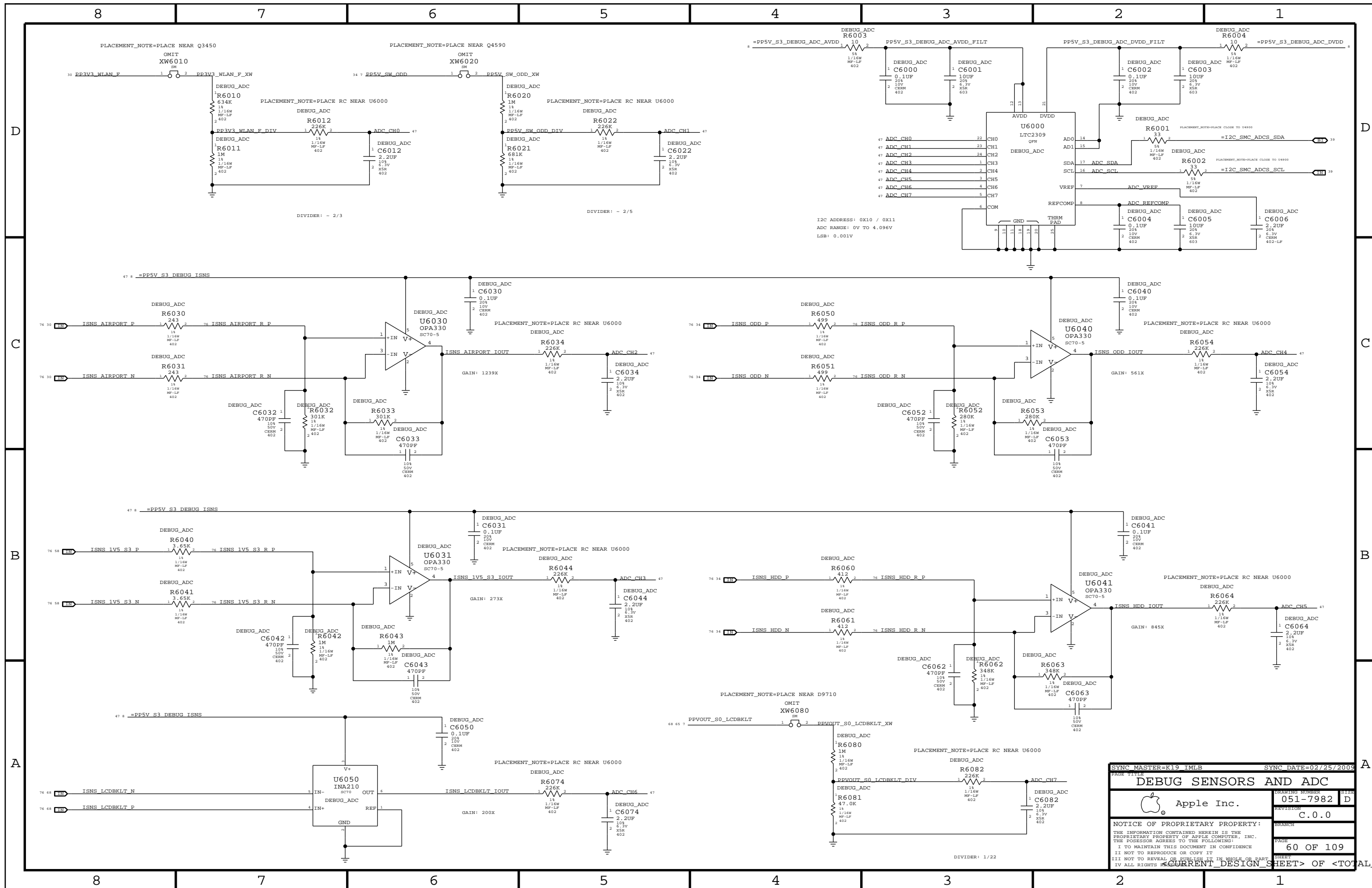
**IPD FLEX CONNECTOR**

**3V3 LDO FOR IPD**

|   |  |                      |            |
|---|--|----------------------|------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=02/25/2009 |            |
| <b>WELLSPRING 2</b>   |  |                      |            |
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SYNC MASTER=K19 IMLB SYNC DATE=02/25/2009

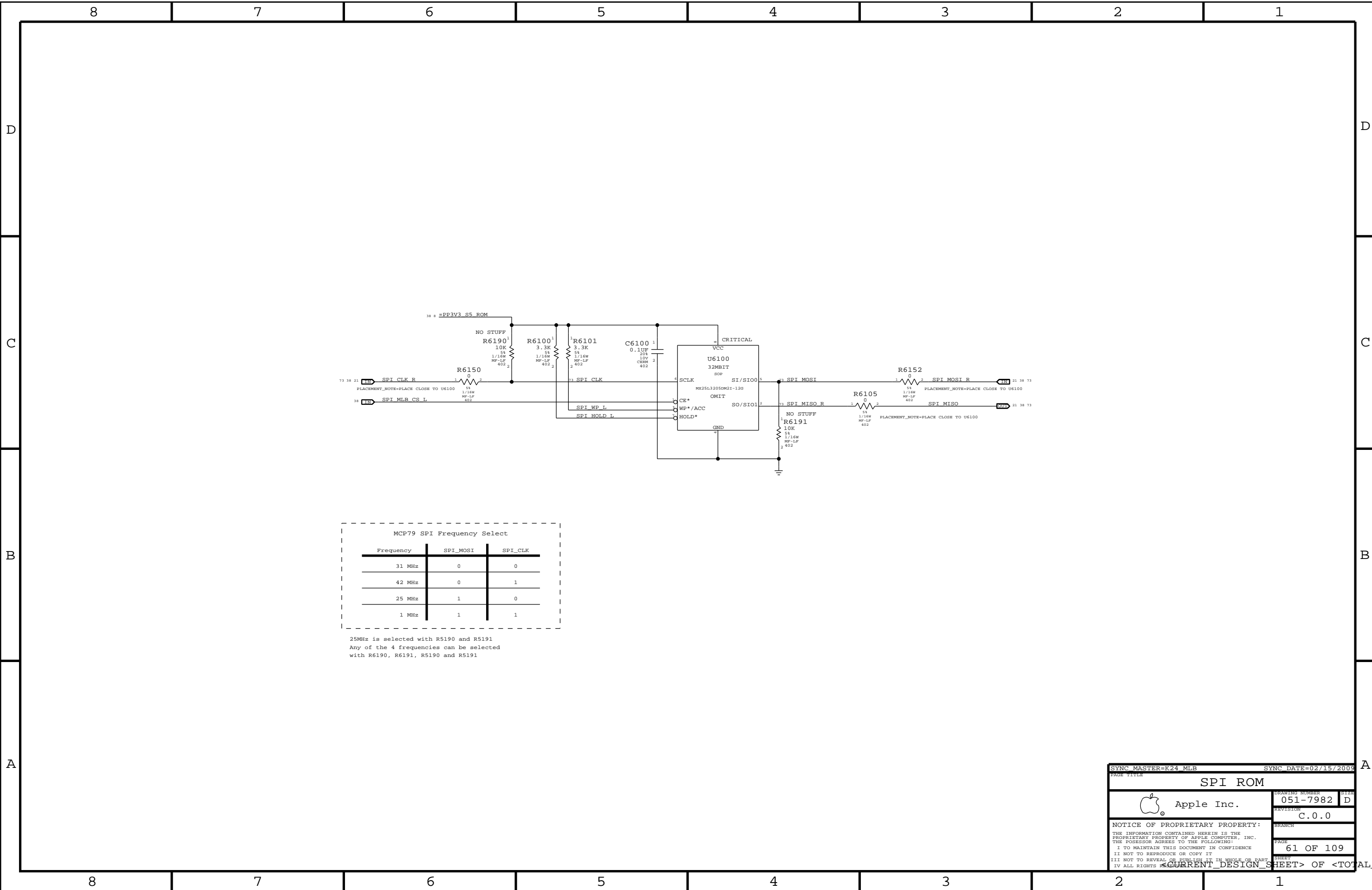
**DEBUG SENSORS AND ADC**

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MCP79 SPI Frequency Select

| Frequency | SPI_MOSI | SPI_CLK |
|-----------|----------|---------|
| 31 MHz    | 0        | 0       |
| 42 MHz    | 0        | 1       |
| 25 MHz    | 1        | 0       |
| 1 MHz     | 1        | 1       |

25MHz is selected with R5190 and R5191  
 Any of the 4 frequencies can be selected  
 with R6190, R6191, R5190 and R5191

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

**SPI ROM**

Apple Inc. DRAWING NUMBER 051-7982 D

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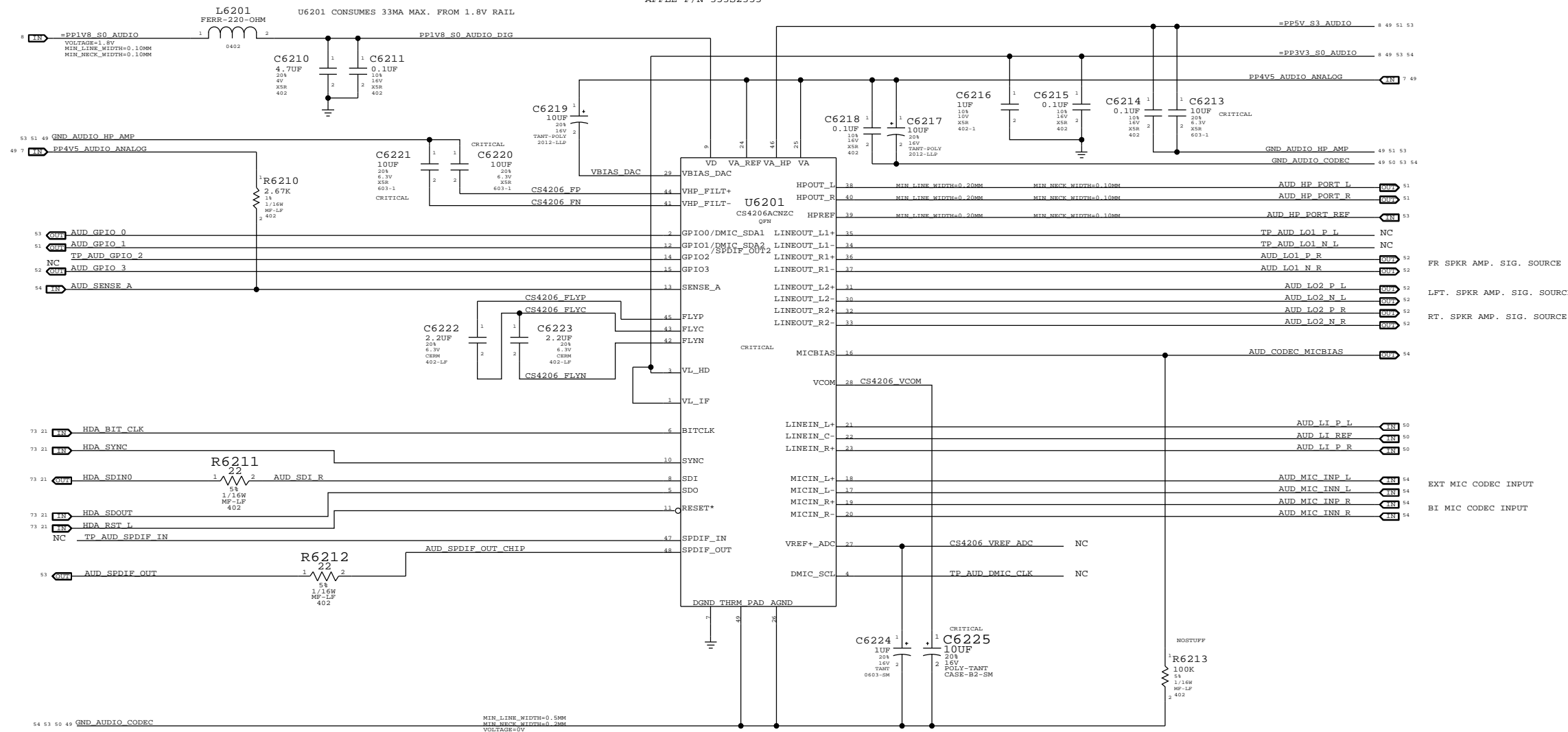
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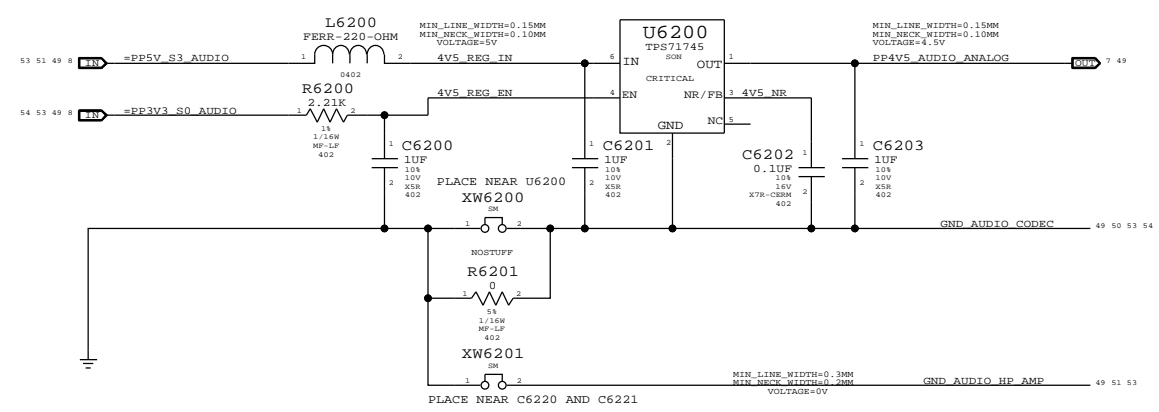
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**AUDIO CODEC**  
APPLE P/N 353S2355



**4.5V POWER SUPPLY FOR CODEC**  
APPLE P/N 353S2456



**NOTES ON CODEC I/O**

- DIFF FSINPUT= 2.45VRMS
- SE FSINPUT= 1.22VRMS
- DAC1 FSOUTPUT= 1.34VRMS
- DAC2/3 FSOUTPUTDIFF= 2.67VRMS
- DAC2/3 FSOUTPUTSE= 1.34VRMS

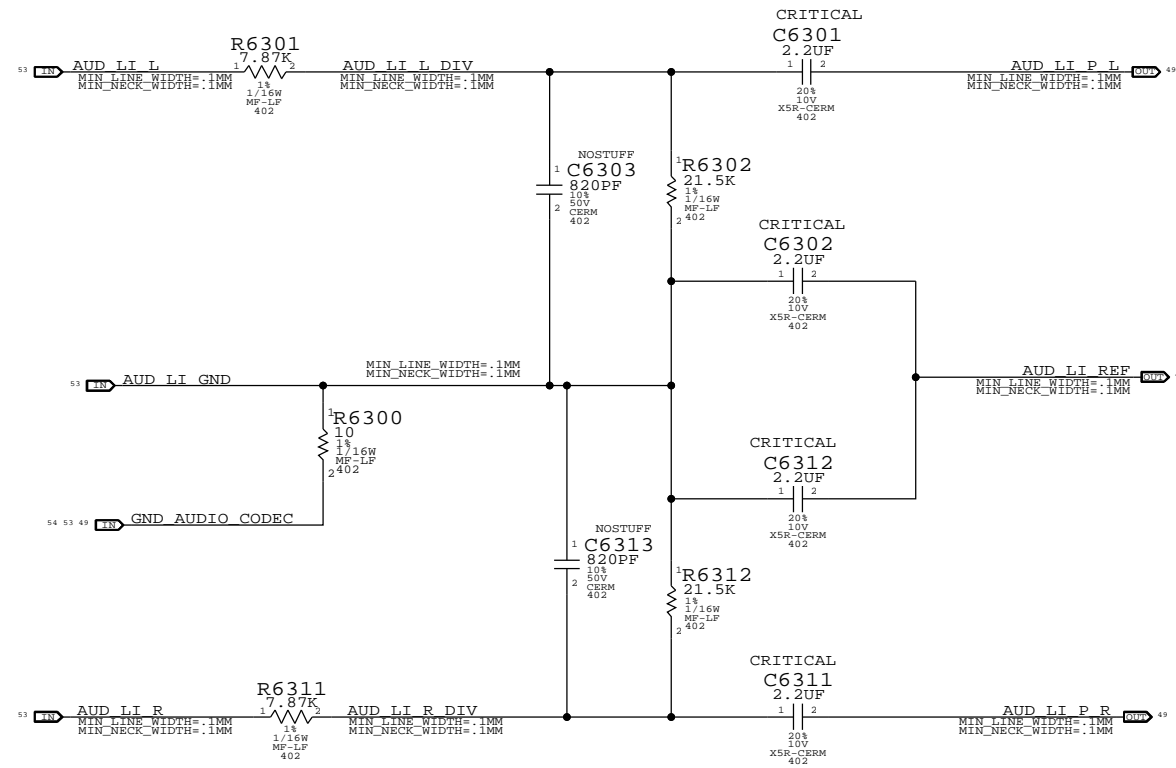
SYNC MASTER=AUDIO SYNC DATE=06/09/2009

|                               |            |
|-------------------------------|------------|
| <b>AUDIO: CODEC/REGULATOR</b> |            |
| Apple Inc.                    | 051-7982 D |
| REVISION                      | C.0.0      |
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LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
 NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)  
 FC\_HP = 3.6 HZ  
 FC\_LP = 43KHZ  
 VIN = 2VRMS, CODEC VIN = 1.14 VRMS



|   |  |                          |            |
|---|--|--------------------------|------------|
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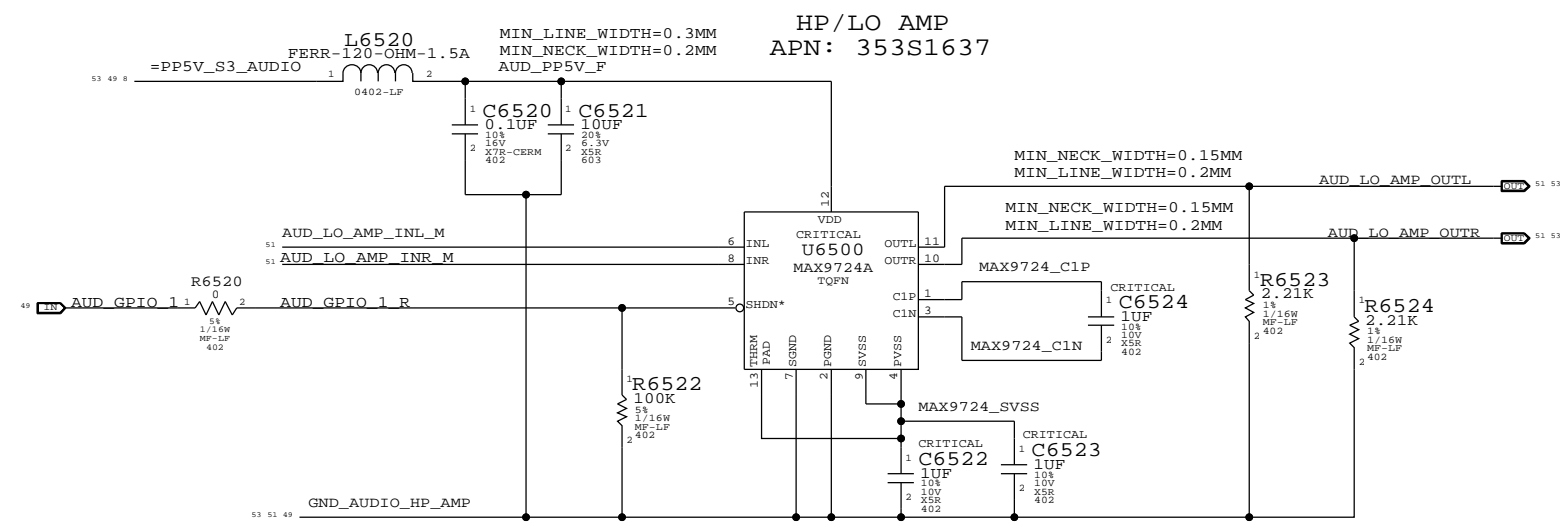
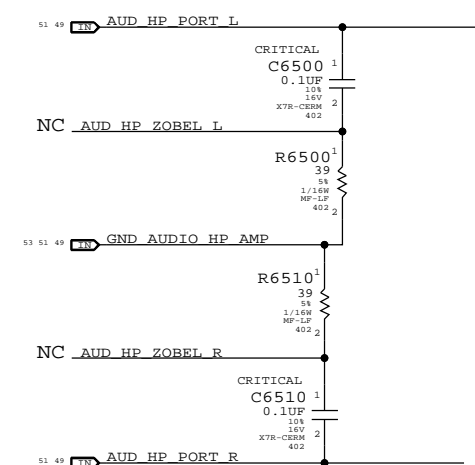
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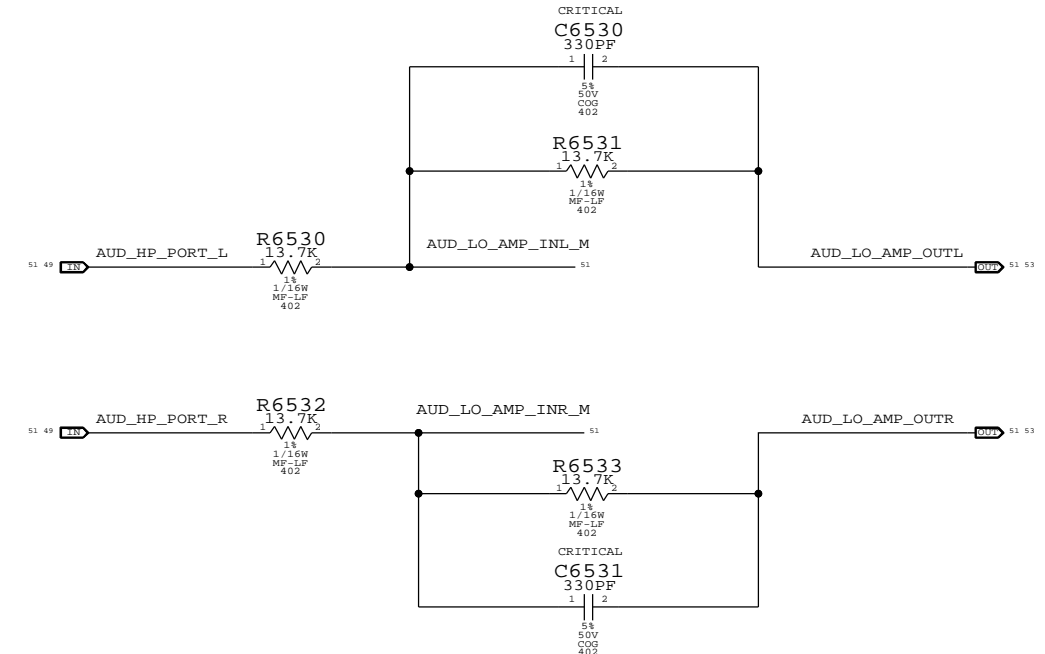
A

### ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



### MAX9724 GAIN/FILTER COMPONENTS

AV\_PB = -1V/V, FC\_LPF = 35.2KHZ



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

### AUDIO: HEADPHONE FILTER

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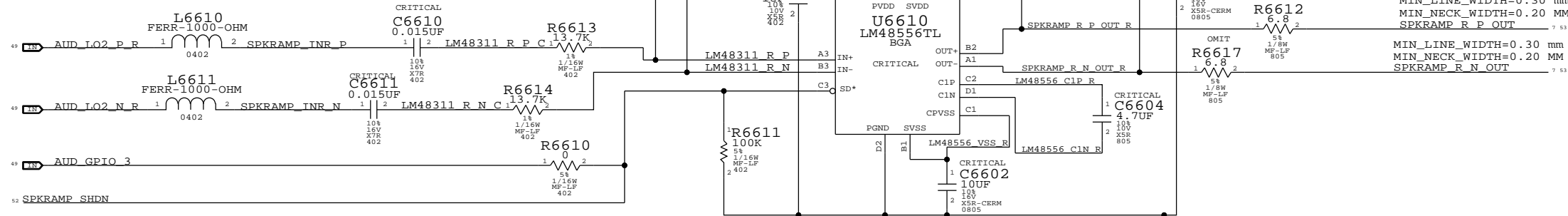
DYNAMIC (SUB) AND PIEZO (SATELLITE) SPKR AMPLIFIERS

SATELLITE HPF FC = 775 HZ  
 SUB 80 HZ < HPF FC < 132 HZ  
 SUB GAIN 6DB (2V/V)  
 SAT GAIN 5.6DB (1.91V/V)

ALIAS OF PP5V\_S3\_REG, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM

52 = PP5V\_S3\_AUDIO\_AMP

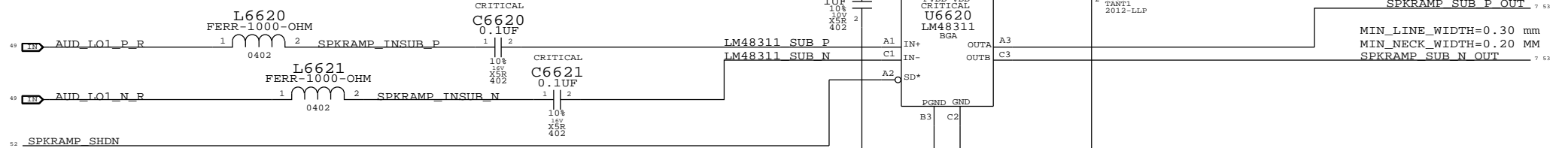
APN: 353S2630



ALIAS OF PP5V\_S3\_REG, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM

52 = PP5V\_S3\_AUDIO\_AMP

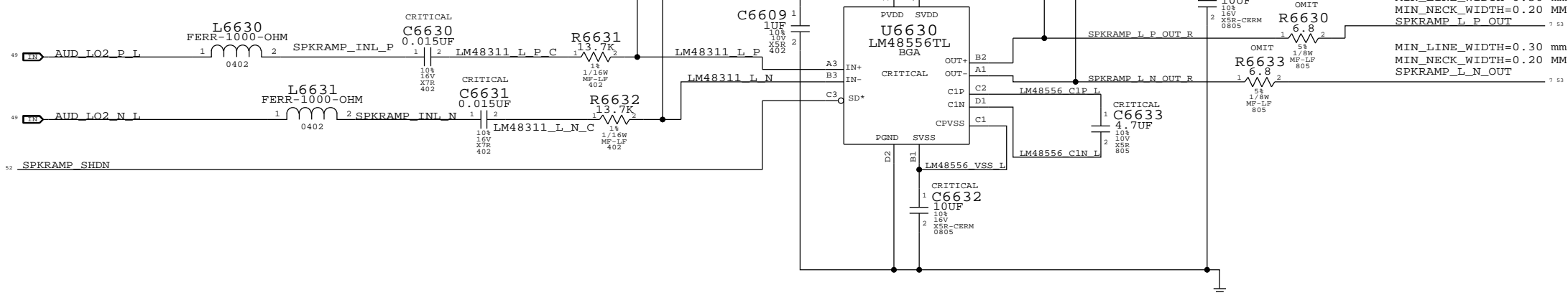
APN: 353S2621



ALIAS OF PP5V\_S3\_REG, MIN\_LINE\_WIDTH=0.60MM, MIN\_NECK\_WIDTH=0.20MM

52 = PP5V\_S3\_AUDIO\_AMP

APN: 353S2630



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

PAGE TITLE

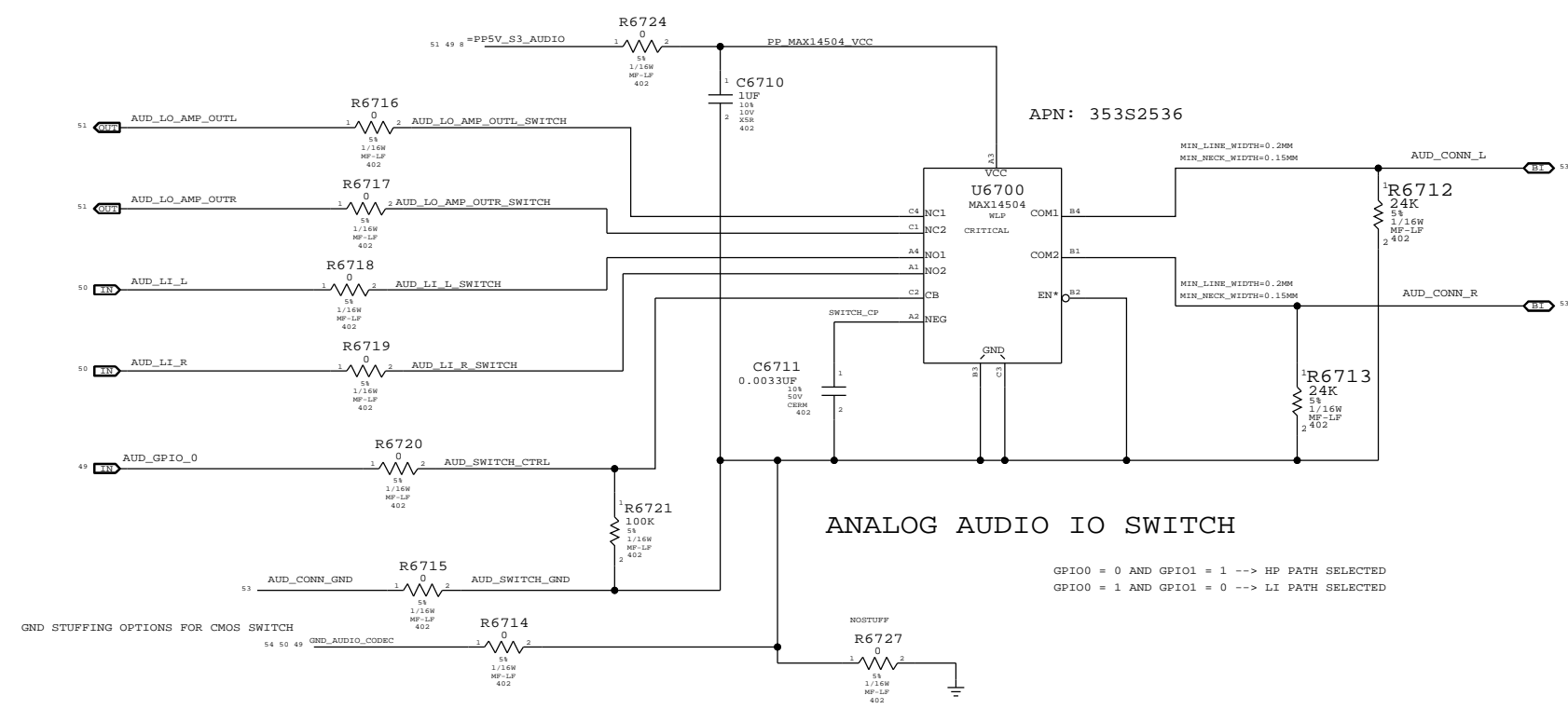
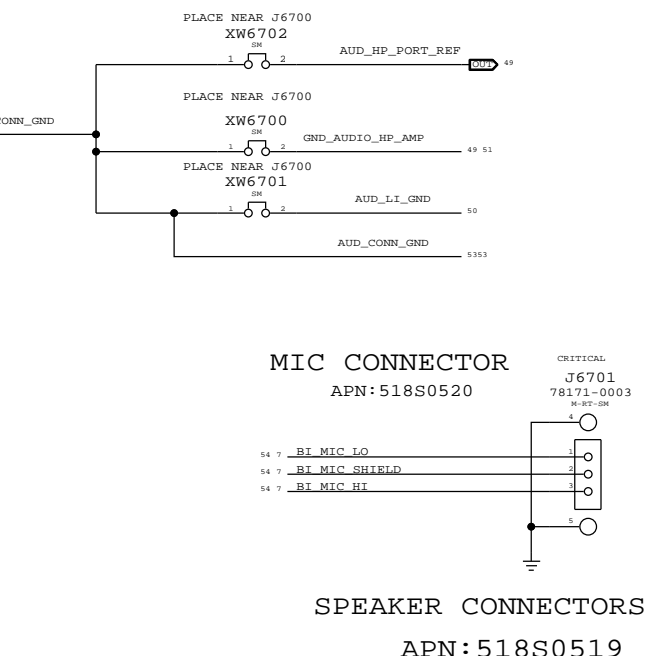
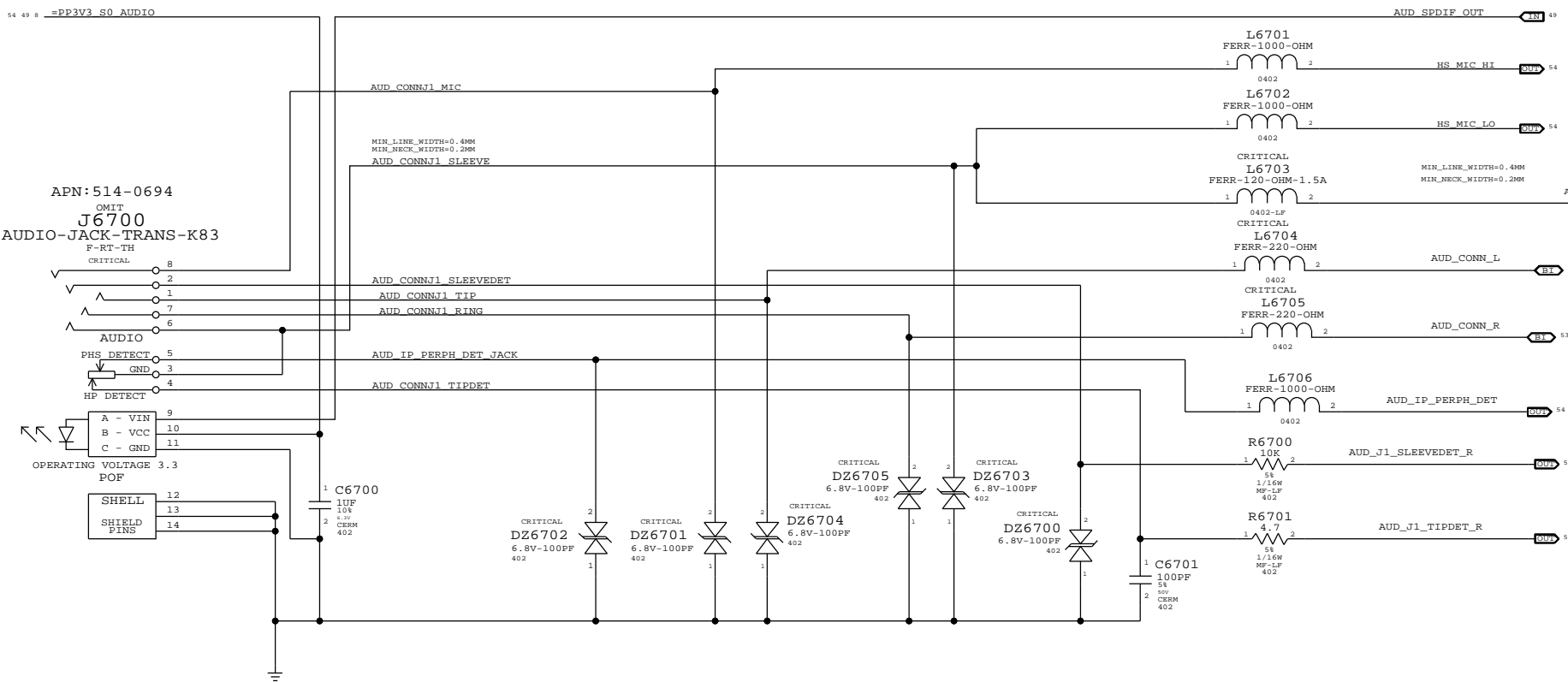
AUDIO: SPEAKER AMP

Apple Inc. 051-7982 D  
 REVISION C.0.0

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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

AUDIO: JACK

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6

5

4

3

2

1

CODEC OUTPUT SIGNAL PATHS

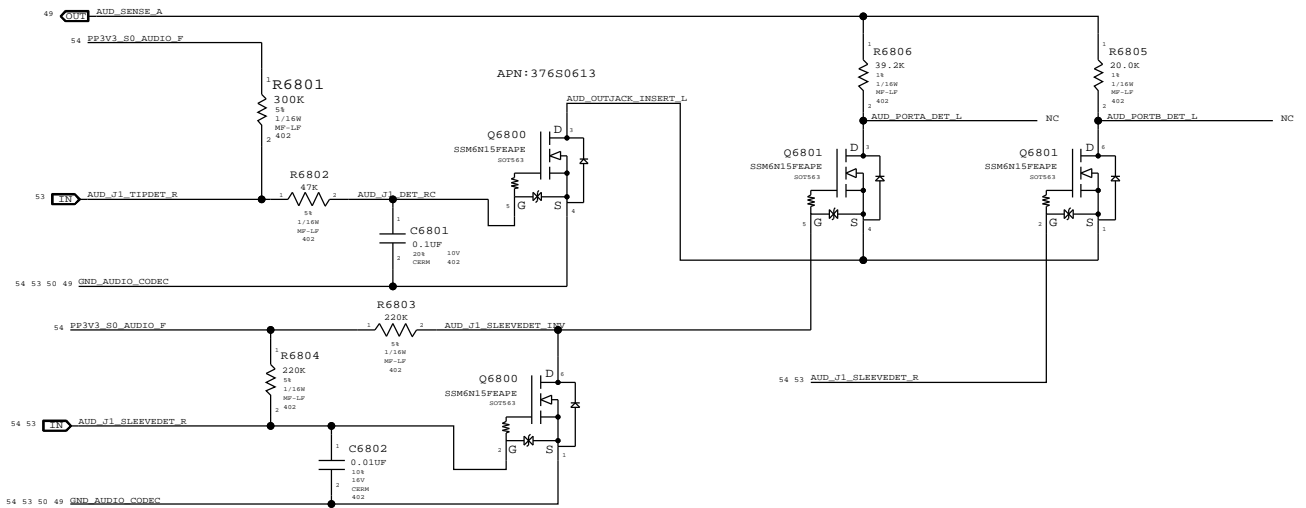
| FUNCTION    | VOLUME   | CONVERTER | PIN COMPLEX | MUTE CONTROL      | DET ASSIGNMENT          |
|-------------|----------|-----------|-------------|-------------------|-------------------------|
| HP/LINE OUT | OX02 (2) | OX02 (2)  | OX09 (9,A)  | GPIO_0 AND GPIO_1 | OX09 (A)                |
| LINE IN     | OX05 (5) | OX05 (5)  | OX0C (12)   | GPIO_0 AND GPIO_1 | OX09 (A) AND UI ELEMENT |
| SATELLITES  | OX04 (4) | OX04 (4)  | OX0B (11)   | GPIO_3            | N/A                     |
| SUB         | OX03 (3) | OX03 (03) | OX0A (10)   | GPIO_3            | N/A                     |
| SPDIF OUT   | N/A      | OX08 (8)  | OX10 (16)   | N/A               | OX0D (B)                |

CODEC INPUT SIGNAL PATHS

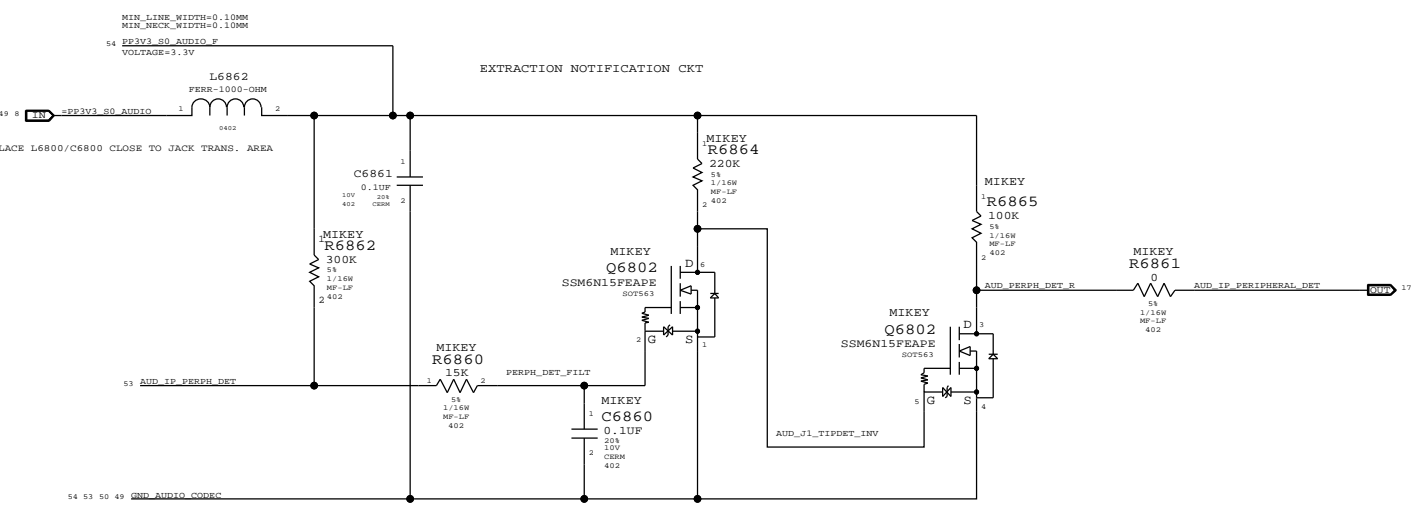
| FUNCTION     | CONVERTER | PIN COMPLEX          | VREP/ENABLE   | DET ASSIGNMENT  |
|--------------|-----------|----------------------|---------------|---|
| BUILT-IN MIC | OX06 (6)  | OX0D (13,B,RIGHT)    | N/A           | N/A   |
| HEADSET MIC  | OX06 (6)  | OX0D (13,V22,B,LEFT) | MCP79 GPIO_38 | MCP79 GPIO_17 (PERIPH DETECT)<br>MCP79 GPIO_4 (LOAD DETECT) |

PORT A DETECT (HEADPHONES)

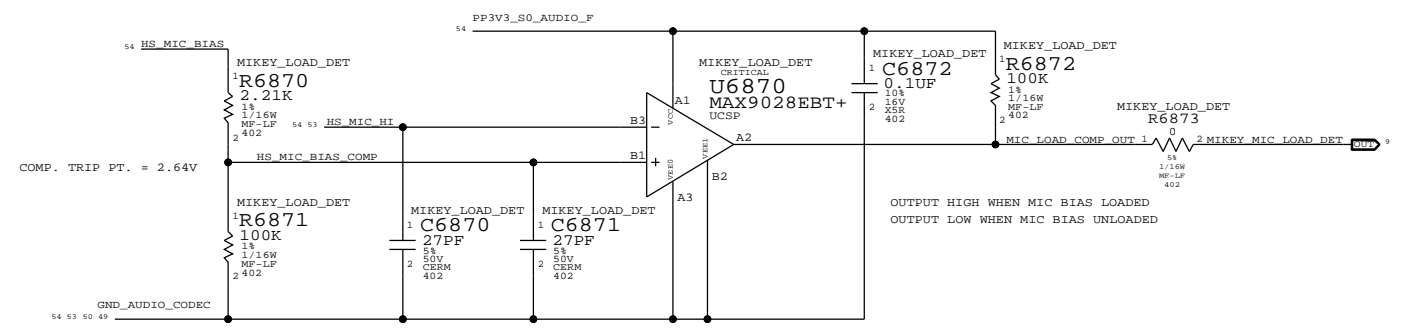
PORT B DETECT (SPDIF DELEGATE)



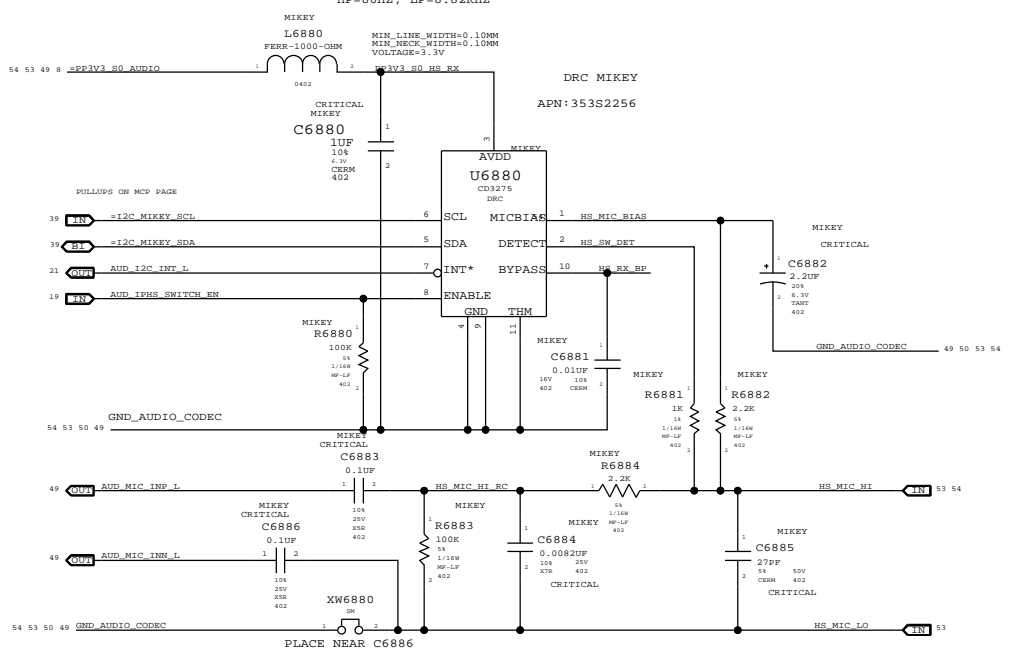
EXTRACTION NOTIFICATION CKT



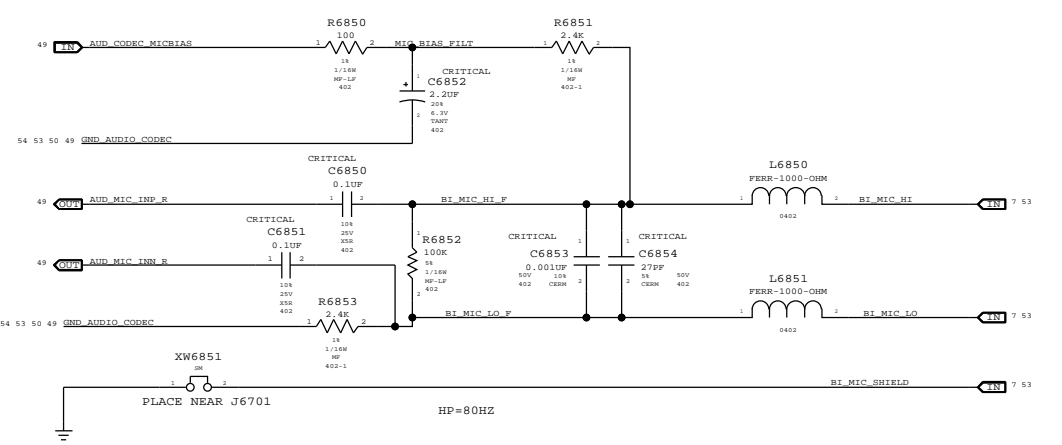
MIKEY MIC LOAD DET CKT



PORT B LEFT (HEADSET MIC)



PORT B RIGHT (BUILT-IN MIC)



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

AUDIO: JACK TRANSLATORS

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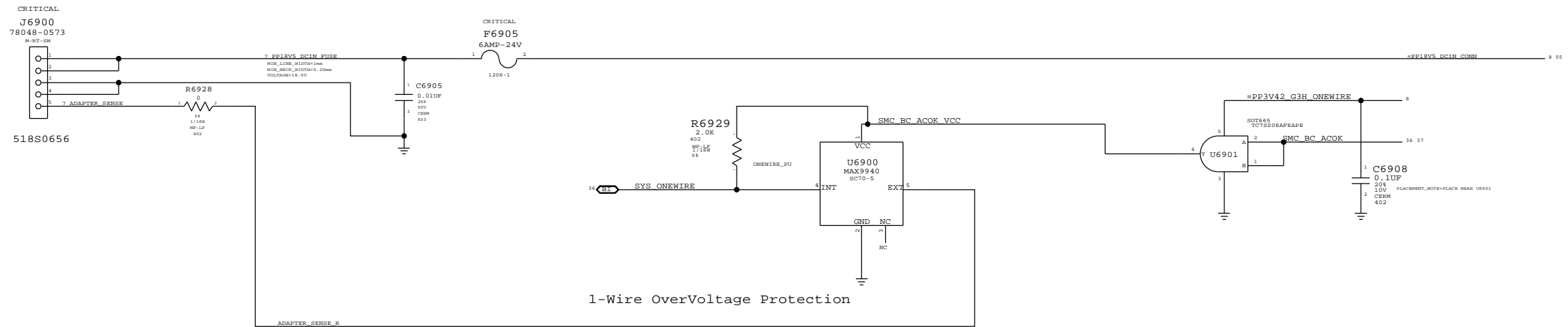
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2

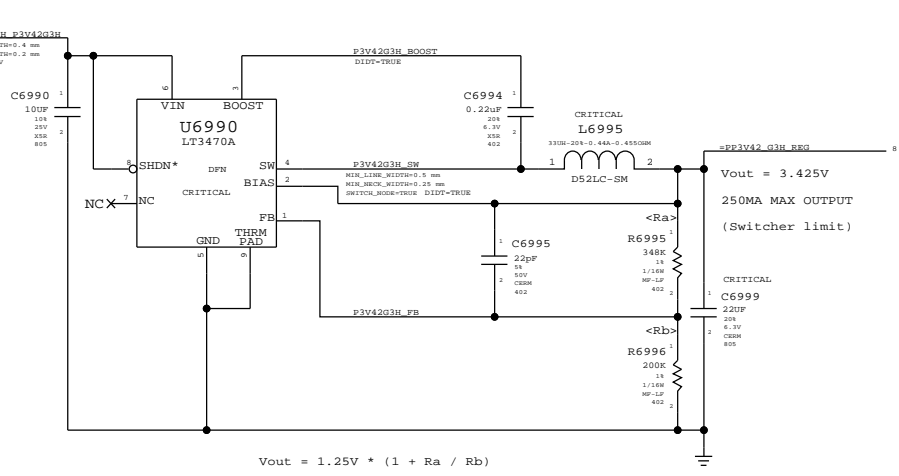
1

MagSafe DC Power Jack

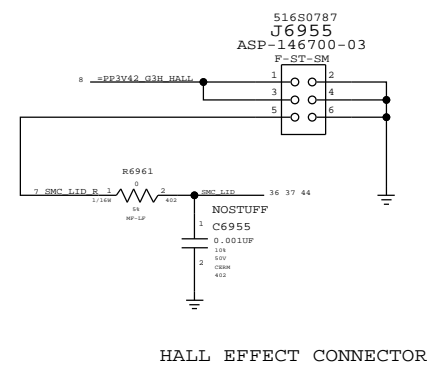
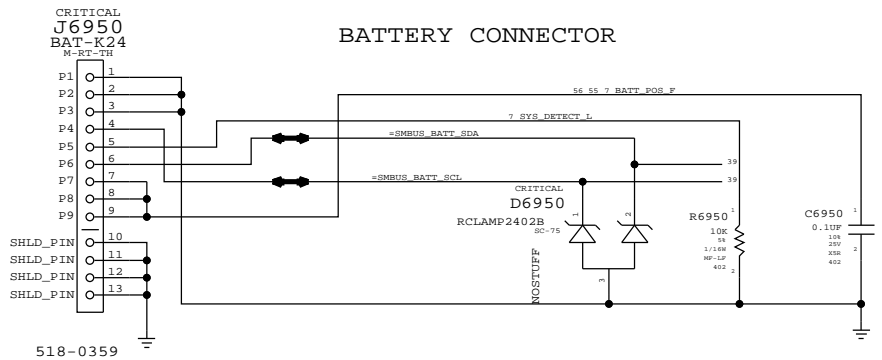


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

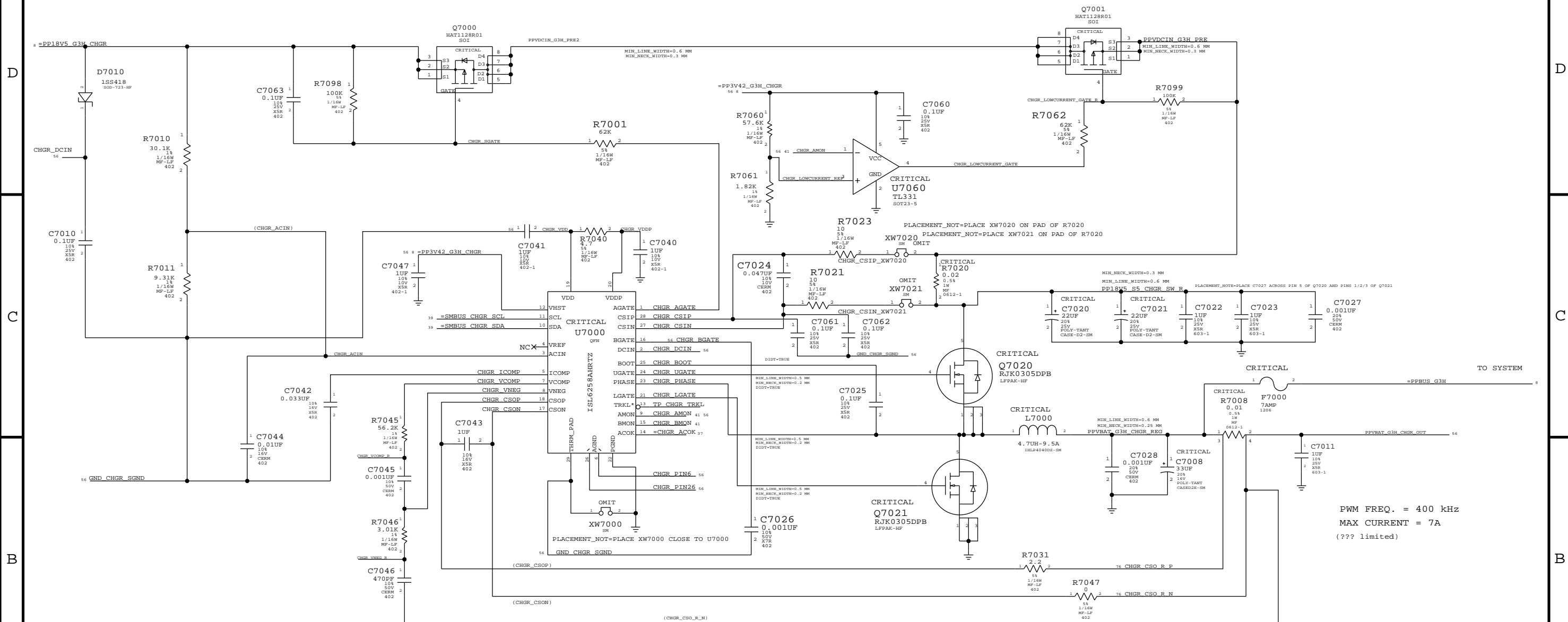


BATTERY CONNECTOR



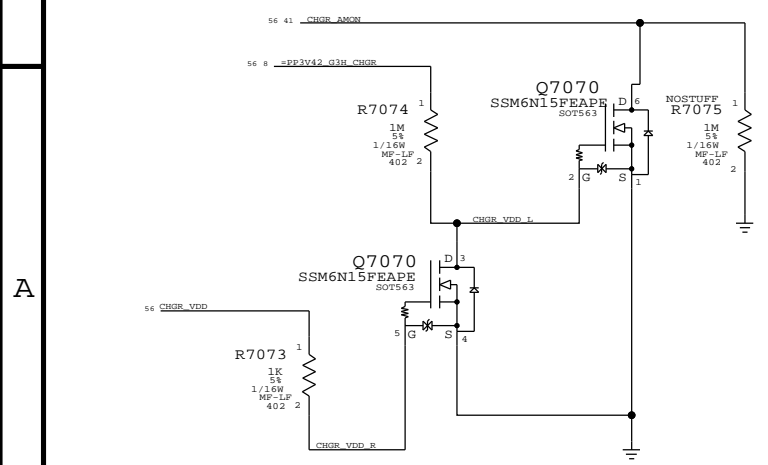
|   |  |                      |  |
|---|--|----------------------|--|
| PAGE TITLE  |  | SYNC DATE=02/05/2009 |  |
| DC-In & Battery Connectors  |  | DRAWING NUMBER       |  |
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# PBUS SUPPLY / BATTERY CHARGER

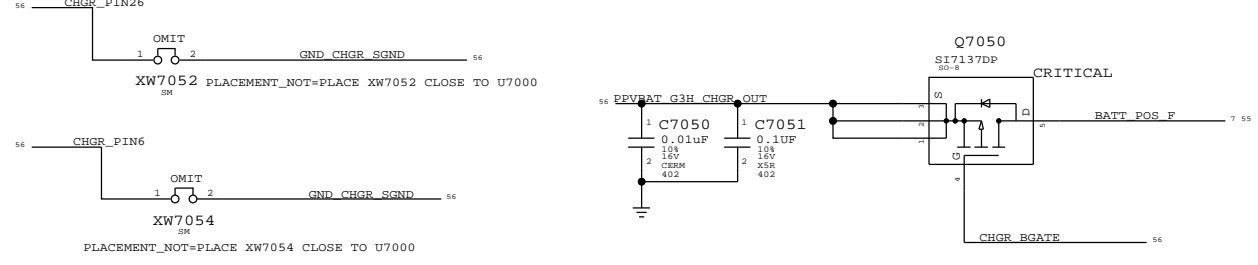


PWM FREQ. = 400 kHz  
 MAX CURRENT = 7A  
 (??? limited)

AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



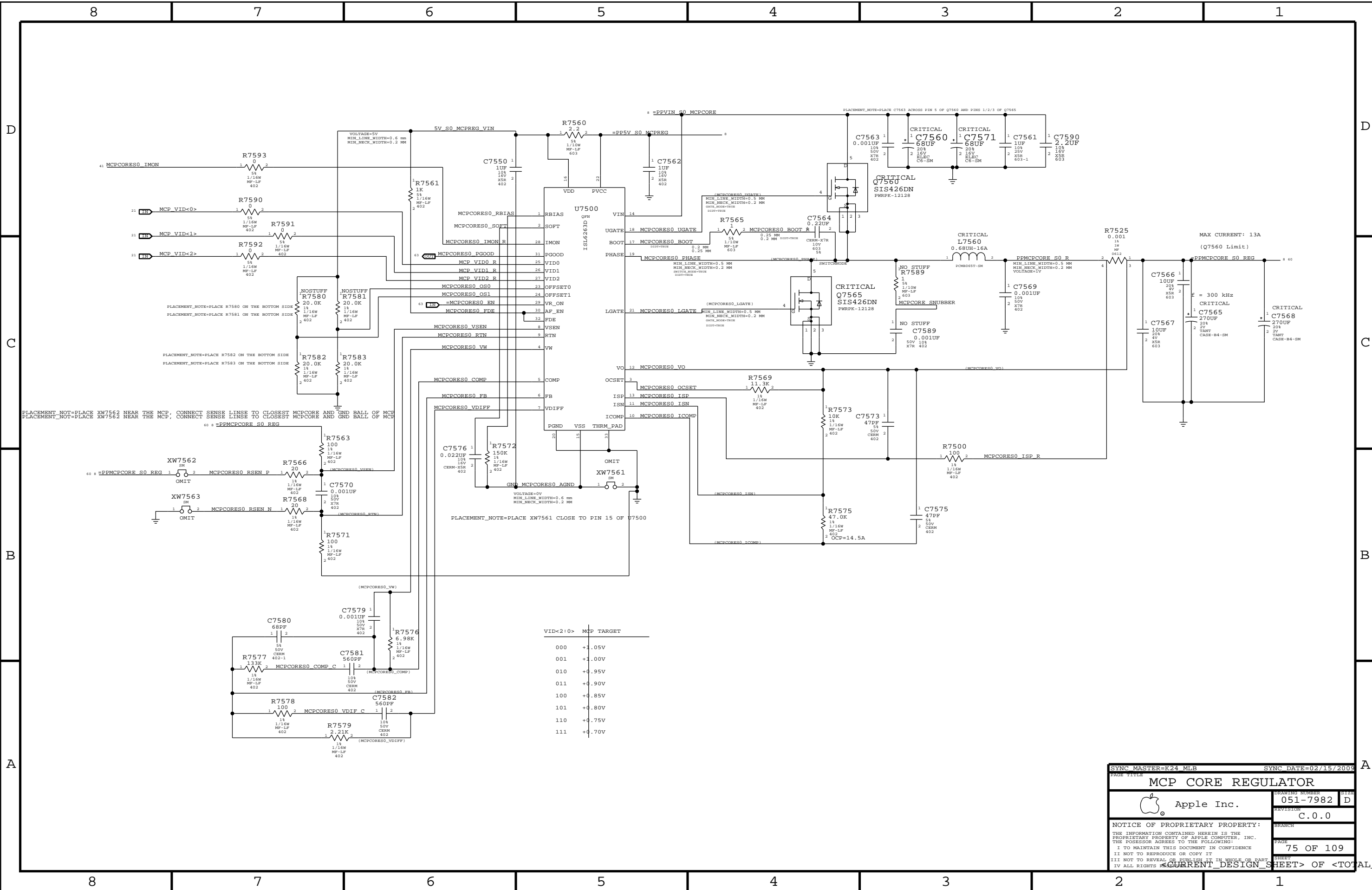
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|---|--|------------------------|--|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=02/05/2009   |  |
| PAGE TITLE<br><b>PBUS Supply/Battery Charger</b>  |  |                        |  |
| CREATOR NUMBER<br>Apple Inc.  |  | REVISION<br>051-7982 D |  |
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| SHEET<br>70 OF 109  |  | PAGE                   |  |











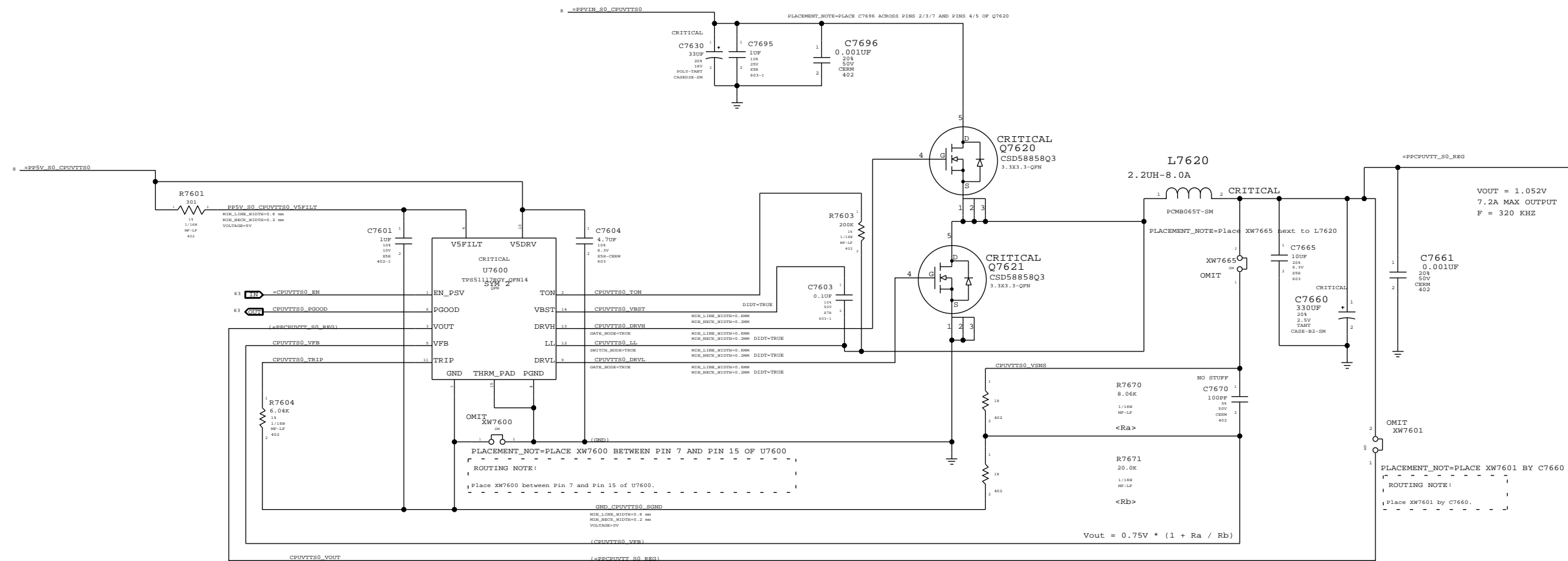
PLACEMENT\_NOTE=PLACE R7580 ON THE BOTTOM SIDE  
 PLACEMENT\_NOTE=PLACE R7581 ON THE BOTTOM SIDE  
 PLACEMENT\_NOTE=PLACE R7582 ON THE BOTTOM SIDE  
 PLACEMENT\_NOTE=PLACE R7583 ON THE BOTTOM SIDE  
 PLACEMENT\_NOT=PLACE XW7562 NEAR THE MCP, CONNECT SENSE LINES TO CLOSEST MCP CORE AND GND BALL OF MCP  
 PLACEMENT\_NOT=PLACE XW7563 NEAR THE MCP, CONNECT SENSE LINES TO CLOSEST MCP CORE AND GND BALL OF MCP

| VID<2:0> | MCP TARGET |
|----------|------------|
| 000      | +1.05V     |
| 001      | +1.00V     |
| 010      | +0.95V     |
| 011      | +0.90V     |
| 100      | +0.85V     |
| 101      | +0.80V     |
| 110      | +0.75V     |
| 111      | +0.70V     |

SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

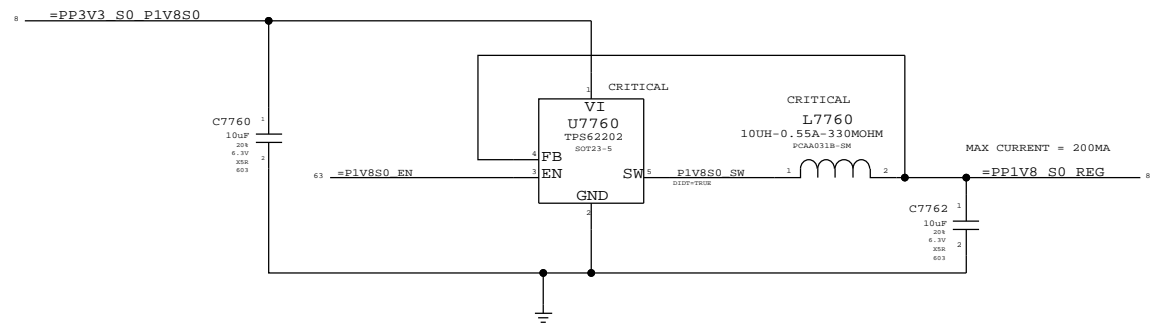
|   |  |                    |            |
|---|--|--------------------|------------|
| PAGE TITLE  |  | MCP CORE REGULATOR |            |
| Apple Inc.  |  | DRAWING NUMBER     | 051-7982 D |
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|   |  | SHEET              |            |

# CPUVTT POWER SUPPLY

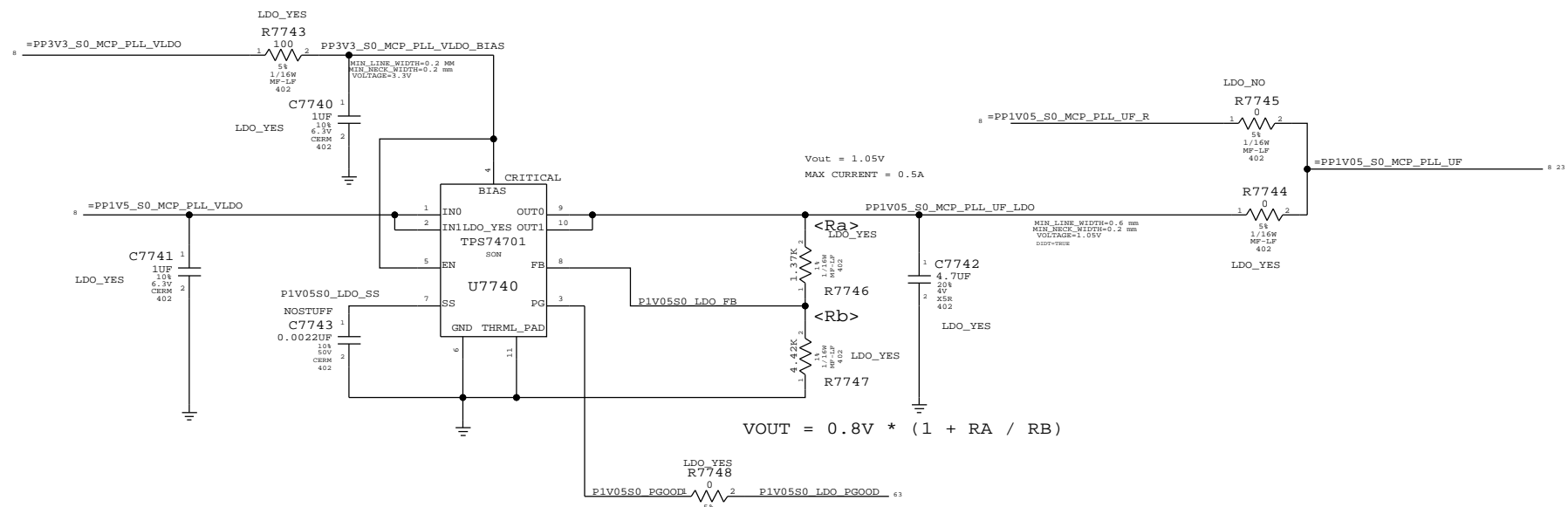


|   |  |                                      |                   |
|---|--|--------------------------------------|-------------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=02/04/2009                 |                   |
| CPU VTT(1.05V) SUPPLY   |  |                                      |                   |
| Apple Inc.  |  | DRAWING NUMBER                       | 051-7982 D        |
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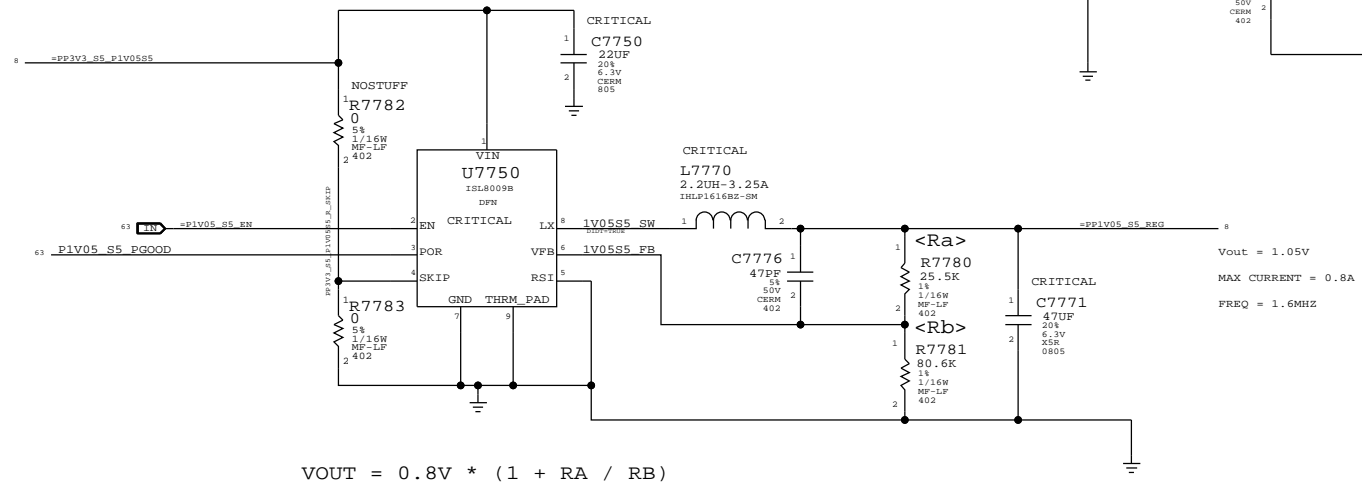
# 1.8V S0 SWITCHER



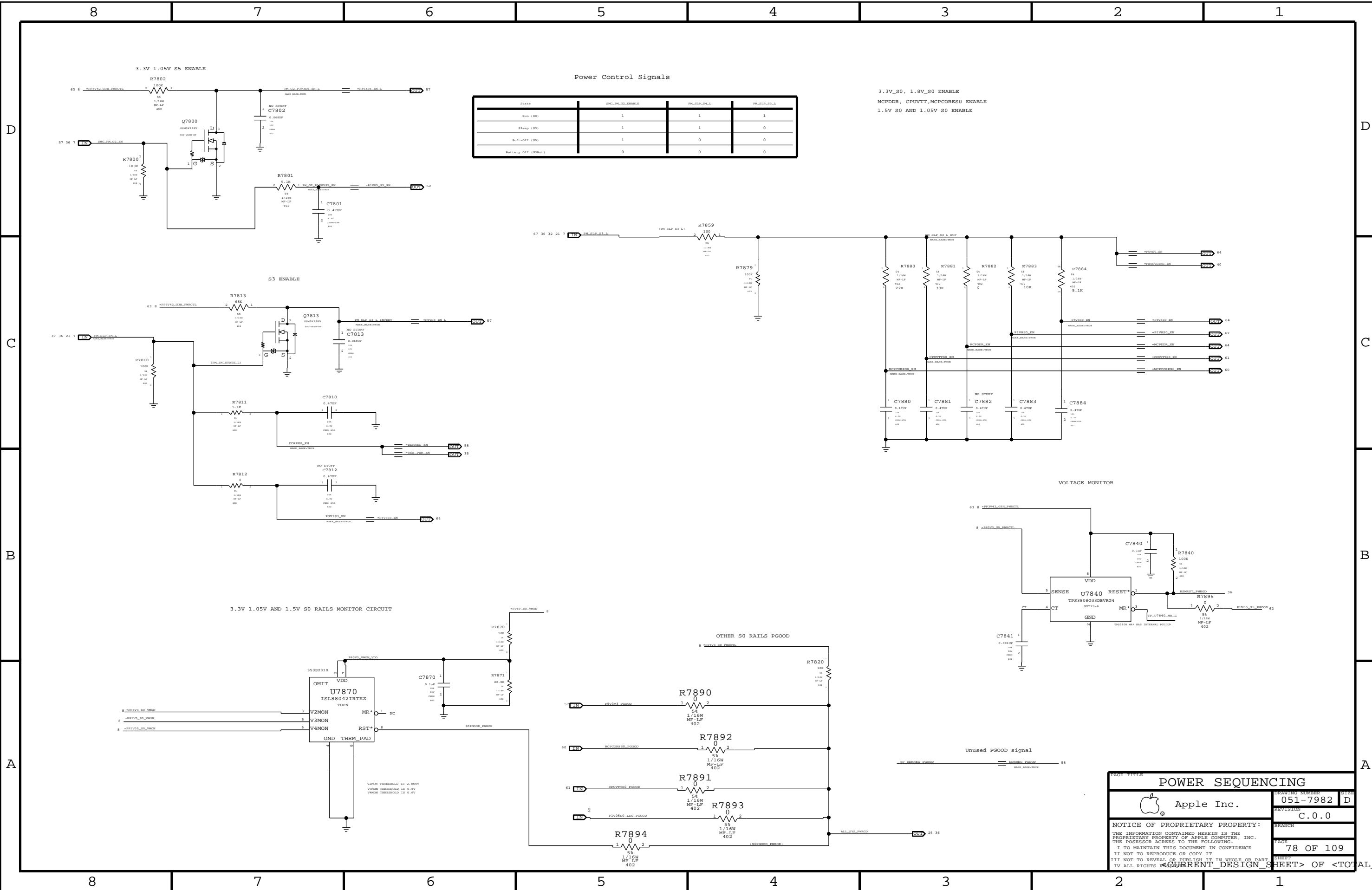
## 1.05V S0 PLL LDO



## MCP 1.05V S5 (AUXC) SUPPLY



|   |  |                      |      |
|---|--|----------------------|------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=03/24/2009 |      |
| PAGE TITLE  |  |                      |      |
| <b>MISC POWER SUPPLIES</b>  |  |                      |      |
| Apple Inc.  |  | DESIGN NUMBER        | SIZE |
|   |  | 051-7982             | D    |
|   |  | REVISION             |      |
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Power Control Signals

| State               | SMC_PM_02_ENABLE | PM_SEP_04_L | PM_SEP_03_L |
|---------------------|------------------|-------------|-------------|
| Run (R0)            | 1                | 1           | 1           |
| Sleep (S3)          | 1                | 1           | 0           |
| Soft-Off (S5)       | 1                | 0           | 0           |
| Battery Off (OSoft) | 0                | 0           | 0           |

**POWER SEQUENCING**

Apple Inc.

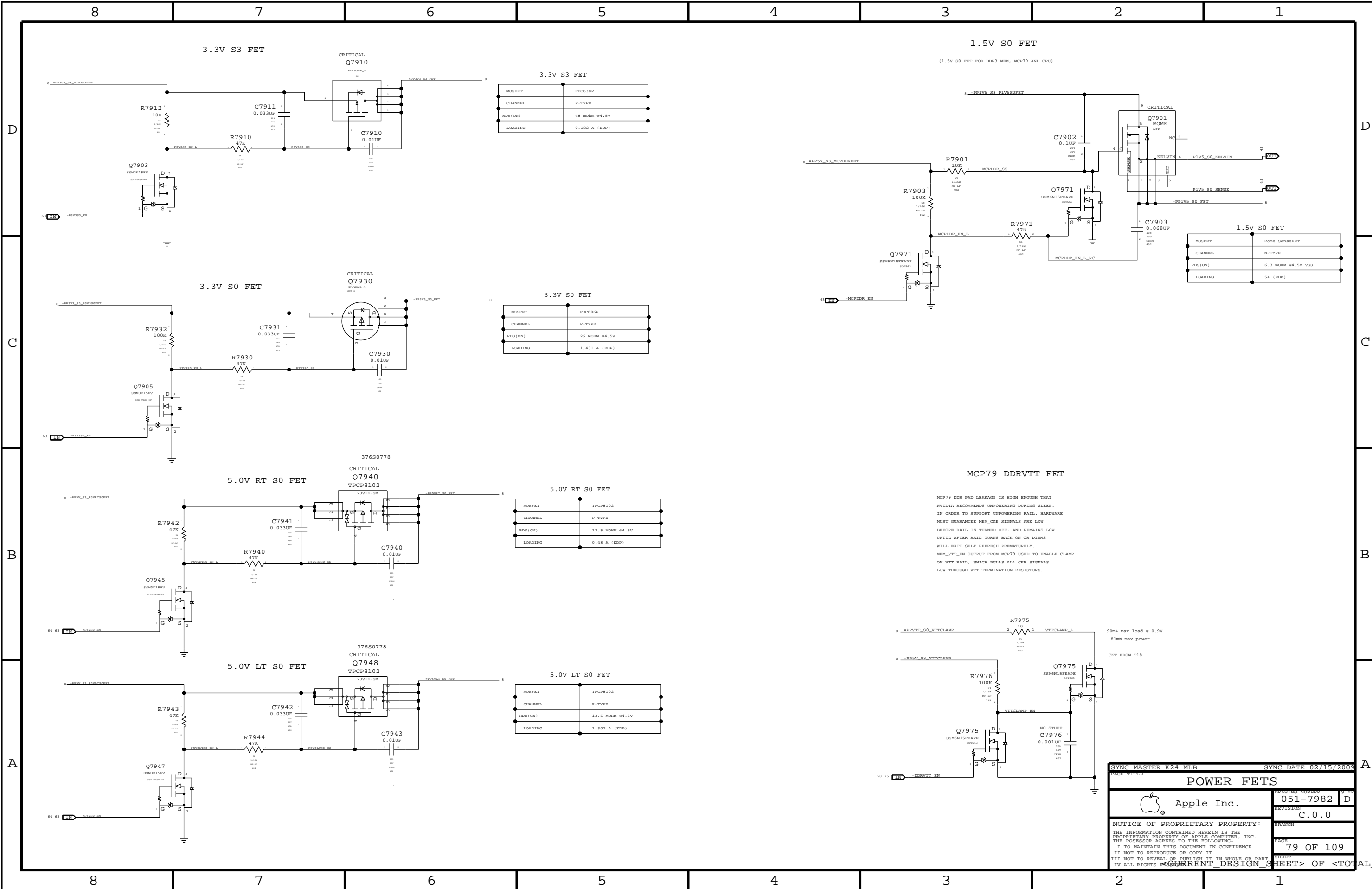
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|-----------------|-----------|-----|---|
| CREATION NUMBER | 051-7982  | REV | D |
| REVISION        | C.0.0     |     |   |
| BATCH           |           |     |   |
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CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

V2MON THRESHOLD IS 2.844V  
 V3MON THRESHOLD IS 0.8V  
 V4MON THRESHOLD IS 0.8V

Unused PGOOD signal

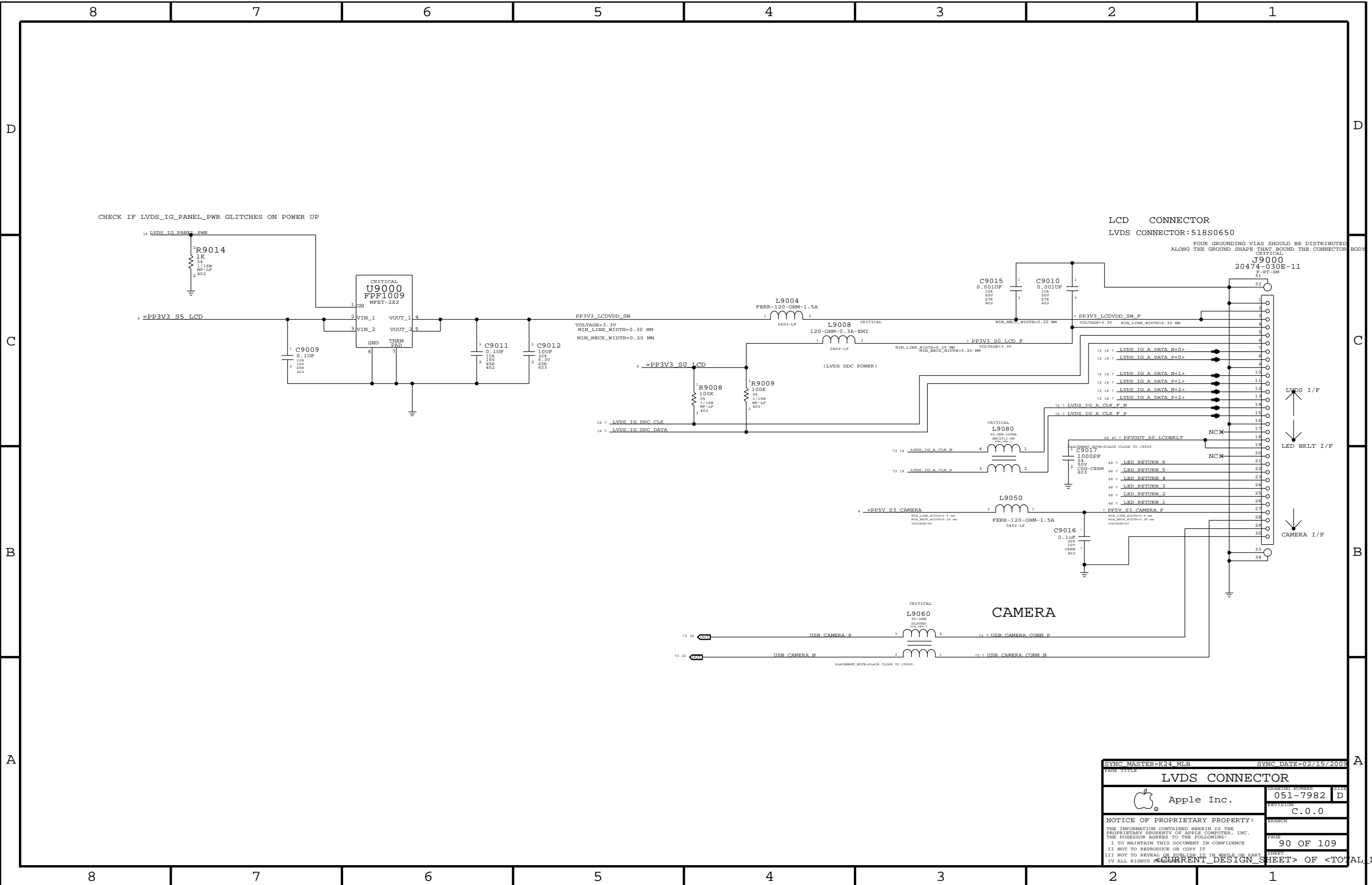


SYNC MASTER=K24 MLB SYNC DATE=02/15/2009

|            |            |
|------------|------------|
| POWER FETS |            |
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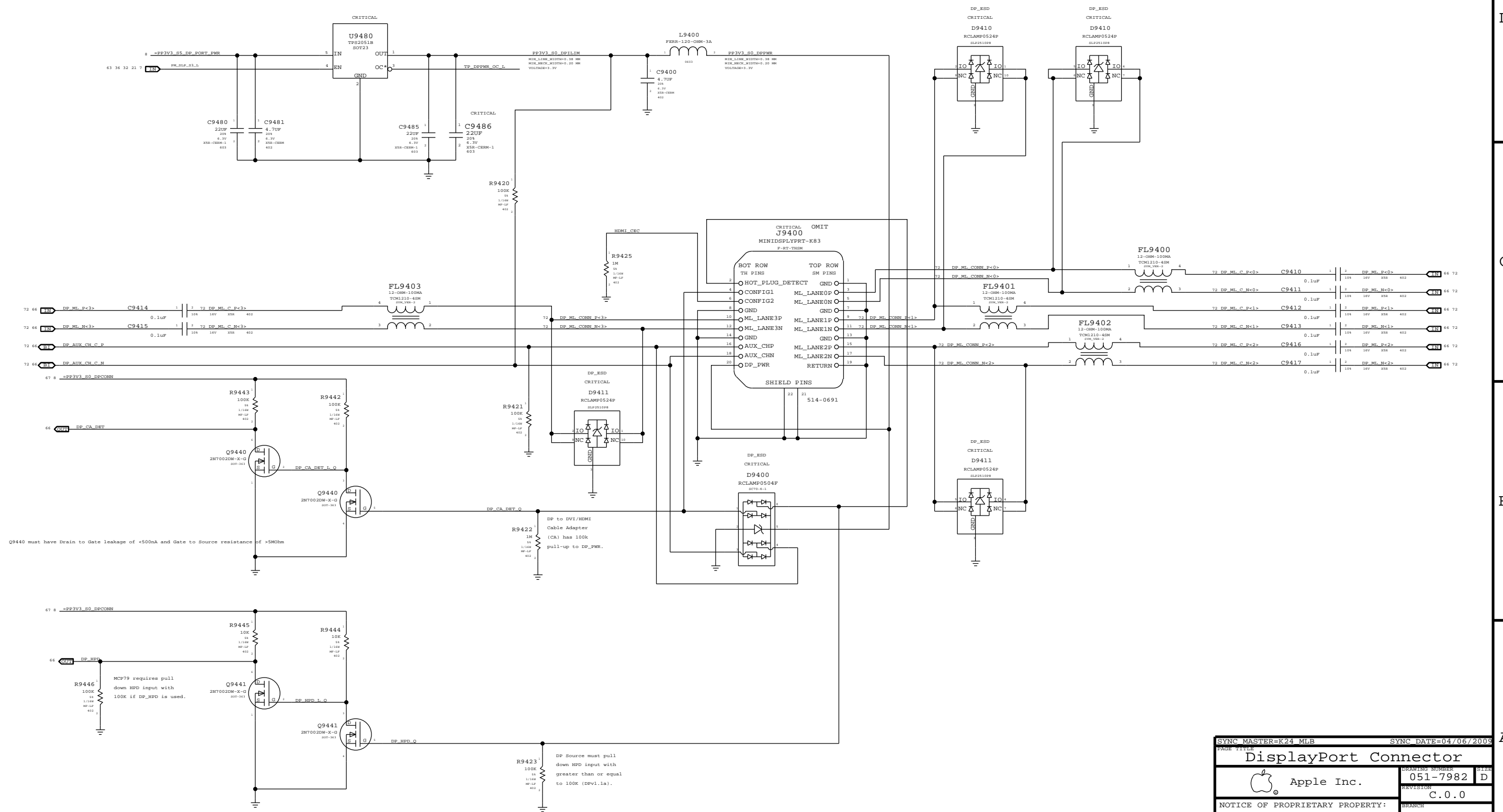


|   |  |                      |            |
|---|--|----------------------|------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=02/15/2009 |            |
| <b>LVDS CONNECTOR</b>   |  |                      |            |
| Apple Inc.  |  | DESIGN NUMBER        | 051-7982 D |
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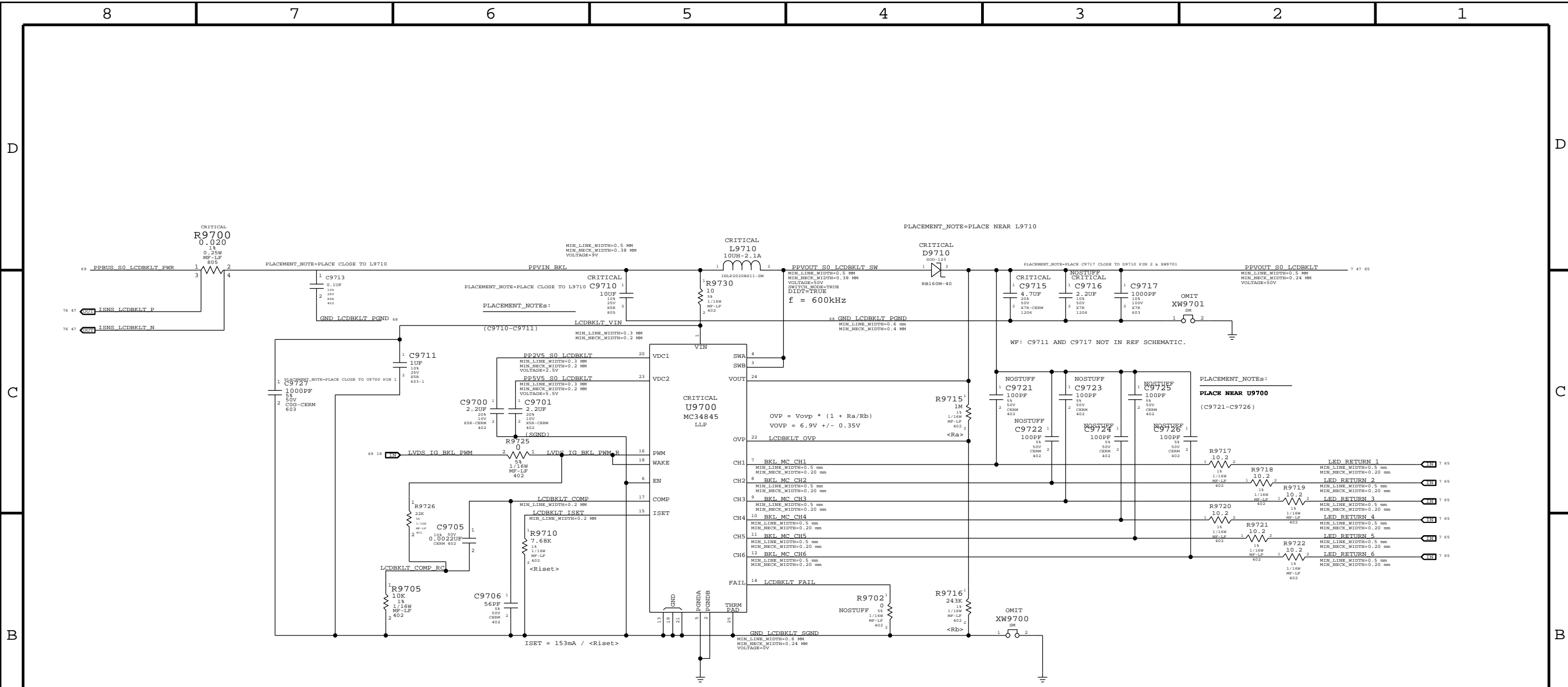


POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS HAVE BEEN USED BEACUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch

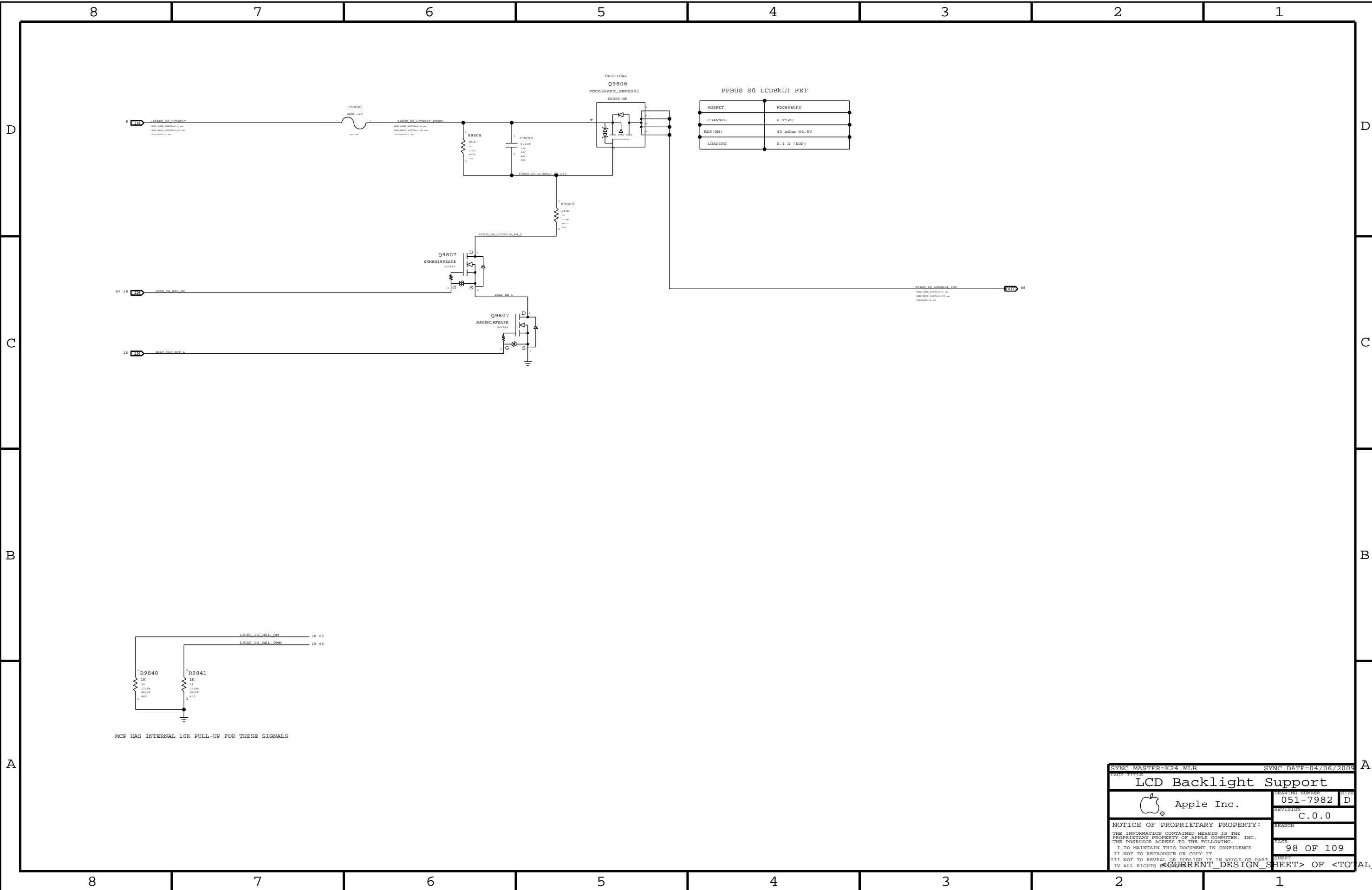


|   |  |                                   |                                    |
|---|--|-----------------------------------|------------------------------------|
| SYNC MASTER=K24 MLB   |  | SYNC DATE=04/06/2009              |                                    |
| <b>DisplayPort Connector</b>  |  |                                   |                                    |
| Apple Inc.  |  | DRAWING NUMBER<br><b>051-7982</b> | SHEET<br><b>D</b>                  |
|   |  | REVISION<br><b>C.0.0</b>          |                                    |
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13.3 Inch Panel (9 LEDs per string)  
 TARGET: ISET = 20mA, OVP = 35V  
 ACTUAL: ISET = 19.9mA, OVP = 35.2V

|   |  |                      |            |
|---|--|----------------------|------------|
| SYNC MASTER=VEMURI K191   |  | SYNC DATE=02/09/2009 |            |
| LCD Backlight Driver (MC34845)  |  |                      |            |
| Apple Inc.  |  | DRAWING NUMBER       | 051-7982 D |
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SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

**LCD Backlight Support**

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FSB (Front-Side Bus) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FSB_50S           | *     | +50_OHM_SE            | +50_OHM_SE         | +50_OHM_SE         | +50_OHM_SE          | +STANDARD            | +STANDARD         |
| FSB_D0TB_50S      | *     | +50_OHM_SE            | +50_OHM_SE         | +50_OHM_SE         | +50_OHM_SE          | +111_DIFFPAIR        | +111_DIFFPAIR     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| FSB_DATA         | *     | +2x_DIELECTRIC       | ?      | FSB_DATA         | TOP_BOTTOM | +4x_DIELECTRIC       | ?      |
| FSB_D0TB         | *     | +3x_DIELECTRIC       | ?      | FSB_D0TB         | TOP_BOTTOM | +8x_DIELECTRIC       | ?      |
| FSB_ADDR         | *     | +STANDARD            | ?      | FSB_ADDR         | TOP_BOTTOM | +3x_DIELECTRIC       | ?      |
| FSB_AD0TB        | *     | +2x_DIELECTRIC       | ?      | FSB_AD0TB        | TOP_BOTTOM | +4x_DIELECTRIC       | ?      |
| FSB_1X           | *     | +STANDARD            | ?      | FSB_1X           | TOP_BOTTOM | +3x_DIELECTRIC       | ?      |

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
D0TBs complementary pairs should be matched within 1 ps of each other. all D0TBs matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA, D0TB signals, with 1x dielectric spacing to the D0TBs.  
D0TB complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. AD0TBs should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to AD0TBs.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock. +0/-1000 mils.  
Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_55S           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |
| CPU_27F4S         | *     | +27F4_OHM_SE          | +27F4_OHM_SE       | +27F4_OHM_SE       | +27F4_OHM_SE        | 7 MIL                | 7 MIL             |

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| CPU_A0TL         | *     | +STANDARD            | ?      | CPU_A0TL         | TOP_BOTTOM | +2x_DIELECTRIC       | ?      |
| CPU_8MIL         | *     | 8 MIL                | ?      |                  |            |                      |        |
| CPU_25MIL        | *     | 25 MIL               | ?      |                  |            |                      |        |
| CPU_25MIL        | *     | 25 MIL               | ?      |                  |            |                      |        |
| CPU_25MIL        | *     | +2x_DIELECTRIC       | ?      |                  |            |                      |        |
| CPU_VCCSENSE     | *     | 25 MIL               | ?      |                  |            |                      |        |

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_55S           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MCP_FSB_COMP     | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_FSB_100S      | *     | +100_OHM_DIFF         | +100_OHM_DIFF      | +100_OHM_DIFF      | +100_OHM_DIFF       | +100_OHM_DIFF        | +100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| CLK_FSB          | *     | +3x_DIELECTRIC       | ?      | CLK_FSB          | TOP_BOTTOM | +4x_DIELECTRIC       | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

| ELECTRICAL CONSTRAINT SET | PHYSICAL | NET_TYPE | PROPERTY         |
|---------------------------|----------|----------|------------------|
| FSB_DATA_00000            | FSB_400  | FSB_DATA | FSB D L<15..0>   |
| FSB_DATA_00001            | FSB_400  | FSB_DATA | FSB D L<15..1>   |
| FSB_DATA_00002            | FSB_400  | FSB_DATA | FSB D L<15..2>   |
| FSB_DATA_00003            | FSB_400  | FSB_DATA | FSB D L<15..3>   |
| FSB_DATA_00004            | FSB_400  | FSB_DATA | FSB D L<15..4>   |
| FSB_DATA_00005            | FSB_400  | FSB_DATA | FSB D L<15..5>   |
| FSB_DATA_00006            | FSB_400  | FSB_DATA | FSB D L<15..6>   |
| FSB_DATA_00007            | FSB_400  | FSB_DATA | FSB D L<15..7>   |
| FSB_DATA_00008            | FSB_400  | FSB_DATA | FSB D L<15..8>   |
| FSB_DATA_00009            | FSB_400  | FSB_DATA | FSB D L<15..9>   |
| FSB_DATA_00010            | FSB_400  | FSB_DATA | FSB D L<15..10>  |
| FSB_DATA_00011            | FSB_400  | FSB_DATA | FSB D L<15..11>  |
| FSB_DATA_00012            | FSB_400  | FSB_DATA | FSB D L<15..12>  |
| FSB_DATA_00013            | FSB_400  | FSB_DATA | FSB D L<15..13>  |
| FSB_DATA_00014            | FSB_400  | FSB_DATA | FSB D L<15..14>  |
| FSB_DATA_00015            | FSB_400  | FSB_DATA | FSB D L<15..15>  |
| FSB_DATA_00016            | FSB_400  | FSB_DATA | FSB D L<15..16>  |
| FSB_DATA_00017            | FSB_400  | FSB_DATA | FSB D L<15..17>  |
| FSB_DATA_00018            | FSB_400  | FSB_DATA | FSB D L<15..18>  |
| FSB_DATA_00019            | FSB_400  | FSB_DATA | FSB D L<15..19>  |
| FSB_DATA_00020            | FSB_400  | FSB_DATA | FSB D L<15..20>  |
| FSB_DATA_00021            | FSB_400  | FSB_DATA | FSB D L<15..21>  |
| FSB_DATA_00022            | FSB_400  | FSB_DATA | FSB D L<15..22>  |
| FSB_DATA_00023            | FSB_400  | FSB_DATA | FSB D L<15..23>  |
| FSB_DATA_00024            | FSB_400  | FSB_DATA | FSB D L<15..24>  |
| FSB_DATA_00025            | FSB_400  | FSB_DATA | FSB D L<15..25>  |
| FSB_DATA_00026            | FSB_400  | FSB_DATA | FSB D L<15..26>  |
| FSB_DATA_00027            | FSB_400  | FSB_DATA | FSB D L<15..27>  |
| FSB_DATA_00028            | FSB_400  | FSB_DATA | FSB D L<15..28>  |
| FSB_DATA_00029            | FSB_400  | FSB_DATA | FSB D L<15..29>  |
| FSB_DATA_00030            | FSB_400  | FSB_DATA | FSB D L<15..30>  |
| FSB_DATA_00031            | FSB_400  | FSB_DATA | FSB D L<15..31>  |
| FSB_DATA_00032            | FSB_400  | FSB_DATA | FSB D L<15..32>  |
| FSB_DATA_00033            | FSB_400  | FSB_DATA | FSB D L<15..33>  |
| FSB_DATA_00034            | FSB_400  | FSB_DATA | FSB D L<15..34>  |
| FSB_DATA_00035            | FSB_400  | FSB_DATA | FSB D L<15..35>  |
| FSB_DATA_00036            | FSB_400  | FSB_DATA | FSB D L<15..36>  |
| FSB_DATA_00037            | FSB_400  | FSB_DATA | FSB D L<15..37>  |
| FSB_DATA_00038            | FSB_400  | FSB_DATA | FSB D L<15..38>  |
| FSB_DATA_00039            | FSB_400  | FSB_DATA | FSB D L<15..39>  |
| FSB_DATA_00040            | FSB_400  | FSB_DATA | FSB D L<15..40>  |
| FSB_DATA_00041            | FSB_400  | FSB_DATA | FSB D L<15..41>  |
| FSB_DATA_00042            | FSB_400  | FSB_DATA | FSB D L<15..42>  |
| FSB_DATA_00043            | FSB_400  | FSB_DATA | FSB D L<15..43>  |
| FSB_DATA_00044            | FSB_400  | FSB_DATA | FSB D L<15..44>  |
| FSB_DATA_00045            | FSB_400  | FSB_DATA | FSB D L<15..45>  |
| FSB_DATA_00046            | FSB_400  | FSB_DATA | FSB D L<15..46>  |
| FSB_DATA_00047            | FSB_400  | FSB_DATA | FSB D L<15..47>  |
| FSB_DATA_00048            | FSB_400  | FSB_DATA | FSB D L<15..48>  |
| FSB_DATA_00049            | FSB_400  | FSB_DATA | FSB D L<15..49>  |
| FSB_DATA_00050            | FSB_400  | FSB_DATA | FSB D L<15..50>  |
| FSB_DATA_00051            | FSB_400  | FSB_DATA | FSB D L<15..51>  |
| FSB_DATA_00052            | FSB_400  | FSB_DATA | FSB D L<15..52>  |
| FSB_DATA_00053            | FSB_400  | FSB_DATA | FSB D L<15..53>  |
| FSB_DATA_00054            | FSB_400  | FSB_DATA | FSB D L<15..54>  |
| FSB_DATA_00055            | FSB_400  | FSB_DATA | FSB D L<15..55>  |
| FSB_DATA_00056            | FSB_400  | FSB_DATA | FSB D L<15..56>  |
| FSB_DATA_00057            | FSB_400  | FSB_DATA | FSB D L<15..57>  |
| FSB_DATA_00058            | FSB_400  | FSB_DATA | FSB D L<15..58>  |
| FSB_DATA_00059            | FSB_400  | FSB_DATA | FSB D L<15..59>  |
| FSB_DATA_00060            | FSB_400  | FSB_DATA | FSB D L<15..60>  |
| FSB_DATA_00061            | FSB_400  | FSB_DATA | FSB D L<15..61>  |
| FSB_DATA_00062            | FSB_400  | FSB_DATA | FSB D L<15..62>  |
| FSB_DATA_00063            | FSB_400  | FSB_DATA | FSB D L<15..63>  |
| FSB_DATA_00064            | FSB_400  | FSB_DATA | FSB D L<15..64>  |
| FSB_DATA_00065            | FSB_400  | FSB_DATA | FSB D L<15..65>  |
| FSB_DATA_00066            | FSB_400  | FSB_DATA | FSB D L<15..66>  |
| FSB_DATA_00067            | FSB_400  | FSB_DATA | FSB D L<15..67>  |
| FSB_DATA_00068            | FSB_400  | FSB_DATA | FSB D L<15..68>  |
| FSB_DATA_00069            | FSB_400  | FSB_DATA | FSB D L<15..69>  |
| FSB_DATA_00070            | FSB_400  | FSB_DATA | FSB D L<15..70>  |
| FSB_DATA_00071            | FSB_400  | FSB_DATA | FSB D L<15..71>  |
| FSB_DATA_00072            | FSB_400  | FSB_DATA | FSB D L<15..72>  |
| FSB_DATA_00073            | FSB_400  | FSB_DATA | FSB D L<15..73>  |
| FSB_DATA_00074            | FSB_400  | FSB_DATA | FSB D L<15..74>  |
| FSB_DATA_00075            | FSB_400  | FSB_DATA | FSB D L<15..75>  |
| FSB_DATA_00076            | FSB_400  | FSB_DATA | FSB D L<15..76>  |
| FSB_DATA_00077            | FSB_400  | FSB_DATA | FSB D L<15..77>  |
| FSB_DATA_00078            | FSB_400  | FSB_DATA | FSB D L<15..78>  |
| FSB_DATA_00079            | FSB_400  | FSB_DATA | FSB D L<15..79>  |
| FSB_DATA_00080            | FSB_400  | FSB_DATA | FSB D L<15..80>  |
| FSB_DATA_00081            | FSB_400  | FSB_DATA | FSB D L<15..81>  |
| FSB_DATA_00082            | FSB_400  | FSB_DATA | FSB D L<15..82>  |
| FSB_DATA_00083            | FSB_400  | FSB_DATA | FSB D L<15..83>  |
| FSB_DATA_00084            | FSB_400  | FSB_DATA | FSB D L<15..84>  |
| FSB_DATA_00085            | FSB_400  | FSB_DATA | FSB D L<15..85>  |
| FSB_DATA_00086            | FSB_400  | FSB_DATA | FSB D L<15..86>  |
| FSB_DATA_00087            | FSB_400  | FSB_DATA | FSB D L<15..87>  |
| FSB_DATA_00088            | FSB_400  | FSB_DATA | FSB D L<15..88>  |
| FSB_DATA_00089            | FSB_400  | FSB_DATA | FSB D L<15..89>  |
| FSB_DATA_00090            | FSB_400  | FSB_DATA | FSB D L<15..90>  |
| FSB_DATA_00091            | FSB_400  | FSB_DATA | FSB D L<15..91>  |
| FSB_DATA_00092            | FSB_400  | FSB_DATA | FSB D L<15..92>  |
| FSB_DATA_00093            | FSB_400  | FSB_DATA | FSB D L<15..93>  |
| FSB_DATA_00094            | FSB_400  | FSB_DATA | FSB D L<15..94>  |
| FSB_DATA_00095            | FSB_400  | FSB_DATA | FSB D L<15..95>  |
| FSB_DATA_00096            | FSB_400  | FSB_DATA | FSB D L<15..96>  |
| FSB_DATA_00097            | FSB_400  | FSB_DATA | FSB D L<15..97>  |
| FSB_DATA_00098            | FSB_400  | FSB_DATA | FSB D L<15..98>  |
| FSB_DATA_00099            | FSB_400  | FSB_DATA | FSB D L<15..99>  |
| FSB_DATA_00100            | FSB_400  | FSB_DATA | FSB D L<15..100> |
| FSB_DATA_00101            | FSB_400  | FSB_DATA | FSB D L<15..101> |
| FSB_DATA_00102            | FSB_400  | FSB_DATA | FSB D L<15..102> |
| FSB_DATA_00103            | FSB_400  | FSB_DATA | FSB D L<15..103> |
| FSB_DATA_00104            | FSB_400  | FSB_DATA | FSB D L<15..104> |
| FSB_DATA_00105            | FSB_400  | FSB_DATA | FSB D L<15..105> |
| FSB_DATA_00106            | FSB_400  | FSB_DATA | FSB D L<15..106> |
| FSB_DATA_00107            | FSB_400  | FSB_DATA | FSB D L<15..107> |
| FSB_DATA_00108            | FSB_400  | FSB_DATA | FSB D L<15..108> |
| FSB_DATA_00109            | FSB_400  | FSB_DATA | FSB D L<15..109> |
| FSB_DATA_00110            | FSB_400  | FSB_DATA | FSB D L<15..110> |
| FSB_DATA_00111            | FSB_400  | FSB_DATA | FSB D L<15..111> |
| FSB_DATA_00112            | FSB_400  | FSB_DATA | FSB D L<15..112> |
| FSB_DATA_00113            | FSB_400  | FSB_DATA | FSB D L<15..113> |
| FSB_DATA_00114            | FSB_400  | FSB_DATA | FSB D L<15..114> |
| FSB_DATA_00115            | FSB_400  | FSB_DATA | FSB D L<15..115> |
| FSB_DATA_00116            | FSB_400  | FSB_DATA | FSB D L<15..116> |
| FSB_DATA_00117            | FSB_400  | FSB_DATA | FSB D L<15..117> |
| FSB_DATA_00118            | FSB_400  | FSB_DATA | FSB D L<15..118> |
| FSB_DATA_00119            | FSB_400  | FSB_DATA | FSB D L<15..119> |
| FSB_DATA_00120            | FSB_400  | FSB_DATA | FSB D L<15..120> |
| FSB_DATA_00121            | FSB_400  | FSB_DATA | FSB D L<15..121> |
| FSB_DATA_00122            | FSB_400  | FSB_DATA | FSB D L<15..122> |
| FSB_DATA_00123            | FSB_400  | FSB_DATA | FSB D L<15..123> |
| FSB_DATA_00124            | FSB_400  | FSB_DATA | FSB D L<15..124> |
| FSB_DATA_00125            | FSB_400  | FSB_DATA | FSB D L<15..125> |
| FSB_DATA_00126            | FSB_400  | FSB_DATA | FSB D L<15..126> |
| FSB_DATA_00127            | FSB_400  | FSB_DATA | FSB D L<15..127> |
| FSB_DATA_00128            | FSB_400  | FSB_DATA | FSB D L<15..128> |
| FSB_DATA_00129            | FSB_400  | FSB_DATA | FSB D L<15..129> |
| FSB_DATA_00130            | FSB_400  | FSB_DATA | FSB D L<15..130> |
| FSB_DATA_00131            | FSB_400  | FSB_DATA | FSB D L<15..131> |
| FSB_DATA_00132            | FSB_400  | FSB_DATA | FSB D L<15..132> |
| FSB_DATA_00133            | FSB_400  | FSB_DATA | FSB D L<15..133> |
| FSB_DATA_00134            | FSB_400  | FSB_DATA | FSB D L<15..134> |
| FSB_DATA_00135            | FSB_400  | FSB_DATA | FSB D L<15..135> |
| FSB_DATA_00136            | FSB_400  | FSB_DATA | FSB D L<15..136> |
| FSB_DATA_00137            | FSB_400  | FSB_DATA | FSB D L<15..137> |
| FSB_DATA_00138            | FSB_400  | FSB_DATA | FSB D L<15..138> |
| FSB_DATA_00139            | FSB_400  | FSB_DATA | FSB D L<15..139> |
| FSB_DATA_00140            | FSB_400  | FSB_DATA | FSB D L<15..140> |
| FSB_DATA_00141            | FSB_400  | FSB_DATA | FSB D L<15..141> |
| FSB_DATA_00142            | FSB_400  | FSB_DATA | FSB D L<15..142> |
| FSB_DATA_00143            | FSB_400  | FSB_DATA | FSB D L<15..143> |
| FSB_DATA_00144            | FSB_400  | FSB_DATA | FSB D L<15..144> |
| FSB_DATA_00145            | FSB_400  | FSB_DATA | FSB D L<15..145> |
| FSB_DATA_00146            | FSB_400  | FSB_DATA | FSB D L<15..146> |
| FSB_DATA_00147            | FSB_400  | FSB_DATA | FSB D L<15..147> |
| FSB_DATA_00148            | FSB_400  | FSB_DATA | FSB D L<15..148> |
| FSB_DATA_00149            | FSB_400  | FSB_DATA | FSB D L<15..149> |
| FSB_DATA_00150            | FSB_400  | FSB_DATA | FSB D L<15..150> |
| FSB_DATA_00151            | FSB_400  | FSB_DATA | FSB D L<15..151> |
| FSB_DATA_00152            | FSB_400  | FSB_DATA | FSB D L<15..152> |
| FSB_DATA_00153            | FSB_400  | FSB_DATA | FSB D L<15..153> |
| FSB_DATA_00154            | FS       |          |                  |

Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_450           | *     | +40_OBM_SE            | +40_OBM_SE         | +40_OBM_SE         | +40_OBM_SE          | +STANDARD            | +STANDARD         |
| MEM_450_VDD       | *     | +40_OBM_SE            | +40_OBM_SE         | +40_OBM_SE         | +40_OBM_SE          | +STANDARD            | +STANDARD         |
| MEM_750           | *     | +70_OBM_DIFF          | +70_OBM_DIFF       | +70_OBM_DIFF       | +70_OBM_DIFF        | +70_OBM_DIFF         | +70_OBM_DIFF      |
| MEM_750_VDD       | *     | +70_OBM_DIFF          | +70_OBM_DIFF       | +70_OBM_DIFF       | +70_OBM_DIFF        | +70_OBM_DIFF         | +70_OBM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MEM_CLK2MEM      | *     | +411_SPACING         | 7      |
| MEM_CTRL2CTRL    | *     | +211_SPACING         | 7      |
| MEM_CTRL2MEM     | *     | +2.511_SPACING       | 7      |
| MEM_CMD2CMD      | *     | +1.511_SPACING       | 7      |
| MEM_CMD2MEM      | *     | +311_SPACING         | 7      |
| MEM_DATA2DATA    | *     | +1.511_SPACING       | 7      |
| MEM_DATA2MEM     | *     | +311_SPACING         | 7      |
| MEM_DQS2MEM      | *     | +311_SPACING         | 7      |
| MEM_2OTHER       | *     | 25 MIL               | 7      |

Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | MEM_CLK           | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_CTRL          | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_CMD           | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_DATA          | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_DQS           | *         | MEM_CLK2MEM      |
| MEM_CMD           | MEM_CMD           | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_CTRL          | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_DATA          | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_DQS           | *         | MEM_CMD2MEM      |
| MEM_DATA          | MEM_DATA          | *         | MEM_DATA2MEM     |
| MEM_DATA          | MEM_CTRL          | *         | MEM_DATA2MEM     |
| MEM_DATA          | MEM_CMD           | *         | MEM_DATA2MEM     |
| MEM_DATA          | MEM_DQS           | *         | MEM_DATA2MEM     |
| MEM_DQS           | MEM_DQS           | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_CTRL          | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_CMD           | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_DATA          | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_DQS           | *         | MEM_DQS2MEM      |

Need to support MEM\_\*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric. DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric. DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_MEM_COMP      | *     | Y                     | 7 MIL              | 7 MIL              | +STANDARD           | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MCP_MEM_COMP     | *     | 8 MIL                | 7      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL     | NET_TYPE         | EFFACTED |
|---------------------------|--------------|------------------|----------|
| MEM_A_CLK_P<5..0>         | MEM_750_VDD  | MEM_CLK          | 15 27    |
| MEM_A_CLK_N<5..0>         | MEM_750_VDD  | MEM_CLK          | 15 27    |
| MEM_A_CKE<3..0>           | MEM_450_VDD  | MEM_CTRL         | 15 27    |
| MEM_A_CS_t<3..0>          | MEM_450_VDD  | MEM_CTRL         | 15 27    |
| MEM_A_ODT<3..0>           | MEM_450_VDD  | MEM_CTRL         | 15 27    |
| MEM_A_A<14..0>            | MEM_450_VDD  | MEM_CMD          | 15 27    |
| MEM_A_BA<2..0>            | MEM_450_VDD  | MEM_CMD          | 15 27    |
| MEM_A_BAS_t               | MEM_450_VDD  | MEM_CMD          | 15 27    |
| MEM_A_CAS_t               | MEM_450_VDD  | MEM_CMD          | 15 27    |
| MEM_A_WE_t                | MEM_450_VDD  | MEM_CMD          | 15 27    |
| MEM_A_DQ<7..0>            | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<15..8>           | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<23..16>          | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<31..24>          | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<39..32>          | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<47..40>          | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<55..48>          | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DQ<63..56>          | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<0>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<1>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<2>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<3>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<4>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<5>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<6>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_A_DM<7>               | MEM_450_VDD  | MEM_DATA         | 15 27    |
| MEM_B_DQS_P<0>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<0>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<1>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<1>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<2>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<2>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<3>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<3>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<4>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<4>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<5>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<5>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<6>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<6>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_P<7>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_DQS_N<7>            | MEM_750_VDD  | MEM_DQS          | 15 27    |
| MEM_B_CLK_P<5..0>         | MEM_750_VDD  | MEM_CLK          | 15 28    |
| MEM_B_CLK_N<5..0>         | MEM_750_VDD  | MEM_CLK          | 15 28    |
| MEM_B_CKE<3..0>           | MEM_450_VDD  | MEM_CTRL         | 15 28    |
| MEM_B_CS_t<3..0>          | MEM_450_VDD  | MEM_CTRL         | 15 28    |
| MEM_B_ODT<3..0>           | MEM_450_VDD  | MEM_CTRL         | 15 28    |
| MEM_B_A<14..0>            | MEM_450_VDD  | MEM_CMD          | 15 28    |
| MEM_B_BA<2..0>            | MEM_450_VDD  | MEM_CMD          | 15 28    |
| MEM_B_BAS_t               | MEM_450_VDD  | MEM_CMD          | 15 28    |
| MEM_B_CAS_t               | MEM_450_VDD  | MEM_CMD          | 15 28    |
| MEM_B_WE_t                | MEM_450_VDD  | MEM_CMD          | 15 28    |
| MEM_B_DQ<7..0>            | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<15..8>           | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<23..16>          | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<31..24>          | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<39..32>          | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<47..40>          | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<55..48>          | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQ<63..56>          | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<0>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<1>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<2>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<3>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<4>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<5>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<6>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DM<7>               | MEM_450_VDD  | MEM_DATA         | 15 28    |
| MEM_B_DQS_P<0>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<0>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<1>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<1>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<2>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<2>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<3>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<3>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<4>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<4>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<5>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<5>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<6>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<6>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_P<7>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MEM_B_DQS_N<7>            | MEM_750_VDD  | MEM_DQS          | 15 28    |
| MCP_MEM_COMP              | MCP_MEM_COMP | MCP_MEM_COMP_VDD | 16       |
| MCP_MEM_COMP              | MCP_MEM_COMP | MCP_MEM_COMP_GND | 16       |

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

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PCI-Express

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_90D          | *     | +100_OHM_DIFF         | +90_OHM_DIFF       | +90_OHM_DIFF       | +90_OHM_DIFF        | +90_OHM_DIFF         | +90_OHM_DIFF      |
| CLK_PCIE_100D     | *     | +100_OHM_DIFF         | +100_OHM_DIFF      | +100_OHM_DIFF      | +100_OHM_DIFF       | +100_OHM_DIFF        | +100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| PCIE             | *     | +3x_DIELECTRIC       | ?      | PCIE             | TOP_BOTTOM | +4x_DIELECTRIC       | ?      |
| CLK_PCIE         | *     | 20 MIL               | ?      |                  |            |                      |        |
| MCP_PEX_COMP     | *     | 8 MIL                | ?      |                  |            |                      |        |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.4

Digital Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DP_100D           | *     | +100_OHM_DIFF         | +100_OHM_DIFF      | +100_OHM_DIFF      | +100_OHM_DIFF       | +100_OHM_DIFF        | +100_OHM_DIFF     |
| LVDS_100D         | *     | +100_OHM_DIFF         | +100_OHM_DIFF      | +100_OHM_DIFF      | +100_OHM_DIFF       | +100_OHM_DIFF        | +100_OHM_DIFF     |
| MCP_PV_COMP       | *     | ?                     | 20 MIL             | 20 MIL             | +STANDARD           | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| DISPLAYPORT      | *     | +3x_DIELECTRIC       | ?      | DISPLAYPORT      | TOP_BOTTOM | +4x_DIELECTRIC       | ?      |
| LVDS             | *     | +3x_DIELECTRIC       | ?      | LVDS             | TOP_BOTTOM | +4x_DIELECTRIC       | ?      |

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
 Displayport/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
 Displayport AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
 Max length of LVDS/Displayport/TMDS traces: 12 inches.  
 SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SATA_100D         | *     | +100_OHM_DIFF         | +100_OHM_DIFF      | +100_OHM_DIFF      | +100_OHM_DIFF       | +100_OHM_DIFF        | +100_OHM_DIFF     |
| SATA_90D_90D      | *     | +90_OHM_DIFF          | +90_OHM_DIFF       | +90_OHM_DIFF       | +90_OHM_DIFF        | +90_OHM_DIFF         | +90_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| SATA             | *     | +4x_DIELECTRIC       | ?      | SATA             | TOP_BOTTOM | +3x_DIELECTRIC       | ?      |
| SATA_TEMP        | *     | 8 MIL                | ?      |                  |            |                      |        |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

| ELECTRICAL CONSTRAINT SET | NET_TYPE         |                  |                       |         |
|---------------------------|------------------|------------------|-----------------------|---------|
|                           | PHYSICAL         | SPACING          |                       |         |
|                           | PCIE_90D         | PCIE_90D         | PCIE MINI_92D_P       | 30      |
|                           | PCIE_90D         | PCIE_90D         | PCIE MINI_92D_N       | 30      |
|                           | PCIE_90D_90D     | PCIE_90D_90D     | PCIE MINI_92D_C_P     | 17 30   |
|                           | PCIE_90D_90D     | PCIE_90D_90D     | PCIE MINI_92D_C_N     | 17 30   |
|                           | PCIE_90D_90D     | PCIE_90D_90D     | PCIE MINI_D2R_P       | 17 30   |
|                           | PCIE_90D_90D     | PCIE_90D_90D     | PCIE MINI_D2R_N       | 17 30   |
|                           | PCIE_90D         | PCIE_90D         | PCIE_PV_92D_P         |         |
|                           | PCIE_90D         | PCIE_90D         | PCIE_PV_92D_N         |         |
|                           | PCIE_PV_90D      | PCIE_PV_90D      | PCIE_PV_92D_C_P       | 9 17    |
|                           | PCIE_PV_90D      | PCIE_PV_90D      | PCIE_PV_92D_C_N       | 9 17    |
|                           | PCIE_PV_90D      | PCIE_PV_90D      | PCIE_PV_D2R_P         | 9 17    |
|                           | PCIE_PV_90D      | PCIE_PV_90D      | PCIE_PV_D2R_N         | 9 17    |
|                           | PCIE_PV_90D      | PCIE_PV_90D      | PCIE_PV_D2R_C_P       | 9 17    |
|                           | PCIE_PV_90D      | PCIE_PV_90D      | PCIE_PV_D2R_C_N       | 9 17    |
|                           | MCP_PEX_CLK_COMP | MCP_PEX_CLK_COMP | MCP_PEX_CLK_COMP      | 17      |
|                           | DP_100D          | DP_100D          | DP_MI_Px3_0x          | 66 67   |
|                           | DP_100D          | DP_100D          | DP_MI_C Px3_0x        | 67      |
|                           | DP_100D          | DP_100D          | DP_MI_Nx3_0x          | 66 67   |
|                           | DP_100D          | DP_100D          | DP_MI_C Nx3_0x        | 67      |
|                           | DP_100D          | DP_100D          | DP_AUX_CH_P           | 18 66   |
|                           | DP_100D          | DP_100D          | DP_AUX_CH_N           | 18 66   |
|                           | DP_100D          | DP_100D          | DP_AUX_CH_SW_P        | 66      |
|                           | DP_100D          | DP_100D          | DP_AUX_CH_SW_N        | 66      |
|                           | DP_100D          | DP_100D          | DP_AUX_CH_C_P         | 66 67   |
|                           | DP_100D          | DP_100D          | DP_AUX_CH_C_N         | 66 67   |
|                           | MCP_IPFAR_RESET  | MCP_IPFAR_RESET  | MCP_IPFAR_RESET       | 18 24   |
|                           | MCP_IPFAR_VPROBE | MCP_IPFAR_VPROBE | MCP_IPFAR_VPROBE      | 18 24   |
|                           | LVDS_100D        | LVDS_100D        | LVDS_IG_A_CLK_P       | 18 65   |
|                           | LVDS_100D        | LVDS_100D        | LVDS_IG_A_CLK_P_P     | 7 65    |
|                           | LVDS_100D        | LVDS_100D        | LVDS_IG_A_CLK_N       | 18 65   |
|                           | LVDS_100D        | LVDS_100D        | LVDS_IG_A_CLK_P_N     | 7 65    |
|                           | LVDS_100D        | LVDS_100D        | LVDS_IG_A_DATA Px2_0x | 7 18 65 |
|                           | LVDS_100D        | LVDS_100D        | LVDS_IG_A_DATA Nx2_0x | 7 18 65 |
|                           | DP_100D          | DP_100D          | DP_MI_CONN Px3_0x     | 67      |
|                           | DP_100D          | DP_100D          | DP_MI_CONN Nx3_0x     | 67      |
|                           | MCP_IPFAR_RESET  | MCP_IPFAR_RESET  | MCP_IPFAR_RESET       | 18 24   |
|                           | MCP_IPFAR_VPROBE | MCP_IPFAR_VPROBE | MCP_IPFAR_VPROBE      | 18 24   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_92D_C_P      | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_92D_C_N      | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_92D_P        | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_92D_N        | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_92D_UP_P     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_92D_UP_N     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_D2R_P        | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_D2R_N        | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_D2R_C_P      | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_D2R_C_N      | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_D2R_UP_P     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_HDD_D2R_UP_N     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_92D_C_P      | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_92D_C_N      | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_92D_P        | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_92D_N        | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_92D_UP_P     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_92D_UP_N     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_D2R_P        | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_D2R_N        | 20 34   |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_D2R_C_P      | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_D2R_C_N      | 7 34    |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_D2R_UP_P     | 34      |
|                           | SATA_90D_90D     | SATA_90D_90D     | SATA_ODD_D2R_UP_N     | 34      |
|                           | MCP_SATA_TEMP    | MCP_SATA_TEMP    | MCP_SATA_TEMP         | 20      |

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MCP Constraints 1

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PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCI_550           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |
| CLK_PCI_550       | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCI              | *     | +STANDARD            | ?      |
| CLK_PCI          | *     | 8 MIL                | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.8.

LPC Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| LPC_550           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |
| CLK_LPC_550       | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| LPC              | *     | 8 MIL                | ?      |
| CLK_LPC          | *     | 8 MIL                | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.9.1.

USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| WDR_USB_201AS     | *     | +STANDARD             | 8 MIL              | 8 MIL              | +STANDARD           | +STANDARD            | +STANDARD         |
| USB_900           | *     | +90_OHM_DIFF          | +90_OHM_DIFF       | +90_OHM_DIFF       | +90_OHM_DIFF        | +90_OHM_DIFF         | +90_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| USB              | *     | +2x_DIELECTRIC       | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.10.1.

SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_550           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB              | *     | +2x_DIELECTRIC       | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.11.1.

HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| HDA_550           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| HDA              | *     | +2x_DIELECTRIC       | ?      |
| MCP_HDA_COMP     | *     | 8 MIL                | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.12.1.

SIO Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_SLOW_550      | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_SLOW         | *     | 8 MIL                | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.13.

SPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SPI_550           | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SPI              | *     | 8 MIL                | ?      |

SOURCE: MCF79 Interface DG (DG-03328-001\_v00), Section 2.14.

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL            | NET_TYPE            | IMPACTED |
|---------------------------|---------------------|---------------------|----------|
| MCP_DBUS0<7..0>           | PCI_550             | PCI                 | 13 19    |
| PCI_AD<23..8>             | PCI_550             | PCI                 |          |
| PCI_AD<24>                | PCI_550             | PCI                 |          |
| PCI_AD<31..25>            | PCI_550             | PCI                 |          |
| PCI_PAR                   | PCI_550             | PCI                 |          |
| PCI_C_BE_4<3..0>          | PCI_550             | PCI                 |          |
| PCI_TRDY_L                | PCI_550             | PCI                 |          |
| PCI_DEVSSEL_L             | PCI_550             | PCI                 |          |
| PCI_PERR_L                | PCI_550             | PCI                 |          |
| PCI_ERRR_L                | PCI_550             | PCI                 |          |
| PCI_STOP_L                | PCI_550             | PCI                 |          |
| PCI_TRDY_H                | PCI_550             | PCI                 |          |
| PCI_FRAME_L               | PCI_550             | PCI                 |          |
| PCI_REQ0_L                | PCI_550             | PCI                 | 19       |
| PCI_CMD0_L                | PCI_550             | PCI                 |          |
| PCI_ERR0_L                | PCI_550             | PCI                 | 19       |
| PCI_CMD1_L                | PCI_550             | PCI                 |          |
| PCI_INT0_L                | PCI_550             | PCI                 |          |
| PCI_INT1_L                | PCI_550             | PCI                 |          |
| PCI_INT2_L                | PCI_550             | PCI                 |          |
| PCI_INT3_L                | PCI_550             | PCI                 |          |
| PCI_INT4_L                | PCI_550             | PCI                 |          |
| PCI_CLK31M_MCP_R          | CLK_PCI_550         | CLK_PCI             | 19       |
| PCI_CLK31M_MCP            | CLK_PCI_550         | CLK_PCI             | 19       |
| LPC_AD<3..0>              | LPC_550             | LPC                 | 19 36 38 |
| LPC_FRAME_L               | LPC_550             | LPC                 | 19 36 38 |
| LPC_RESET_L               | LPC_550             | LPC                 | 19 25    |
| LPC_CLK31M_SMC_R          | CLK_LPC_550         | CLK_LPC             | 19 35    |
| LPC_CLK31M_SMC            | CLK_LPC_550         | CLK_LPC             | 35 36    |
| LPC_CLK31M_LPCPLUS        | CLK_LPC_550         | CLK_LPC             | 25 38    |
| USB_EXTA_P                | USB_900             | USB                 | 20 35    |
| USB_EXTA_N                | USB_900             | USB                 | 20 35    |
| USB_EXTA_MIXED_P          | USB_900             | USB                 | 35       |
| USB_EXTA_MIXED_N          | USB_900             | USB                 | 35       |
| CONN_USB_EXTA_P           | USB_900             | USB                 | 35       |
| CONN_USB_EXTA_N           | USB_900             | USB                 | 35       |
| USB_CAMERA_P              | USB_900             | USB                 | 20 65    |
| USB_CAMERA_N              | USB_900             | USB                 | 20 65    |
| USB_CAMERA_CONN_P         | USB_900             | USB                 | 7 65     |
| USB_CAMERA_CONN_N         | USB_900             | USB                 | 7 65     |
| USB_BT_P                  | USB_900             | USB                 | 20 30    |
| USB_BT_N                  | USB_900             | USB                 | 20 30    |
| CONN_USB2_BT_P            | USB_900             | USB                 | 7 30     |
| CONN_USB2_BT_N            | USB_900             | USB                 | 7 30     |
| USB_TPAD_P                | USB_900             | USB                 | 20 44    |
| USB_TPAD_N                | USB_900             | USB                 | 20 44    |
| USB_TPAD_R_P              | USB_900             | USB                 | 44       |
| USB_TPAD_R_N              | USB_900             | USB                 | 44       |
| USB_IR_P                  | USB_900             | USB                 | 9 20     |
| USB_IR_N                  | USB_900             | USB                 | 9 20     |
| USB_EXTB_P                | USB_900             | USB                 | 20 35    |
| USB_EXTB_N                | USB_900             | USB                 | 20 35    |
| CONN_USB_EXTB_P           | USB_900             | USB                 | 35       |
| CONN_USB_EXTB_N           | USB_900             | USB                 | 35       |
| USB_CARDREADER_P          | USB_900             | USB                 | 9 20     |
| USB_CARDREADER_N          | USB_900             | USB                 | 9 20     |
| MCP_USB_WBIAS_GND         | MCP_USB_WBIAS       | MCP_USB_WBIAS       | 20       |
| SMBUS_MCP_0_CLK           | SMB_550             | SMB                 | 13 21 39 |
| SMBUS_MCP_0_DATA          | SMB_550             | SMB                 | 13 21 39 |
| SMBUS_MCP_1_CLK           | SMB_550             | SMB                 | 21 39    |
| SMBUS_MCP_1_DATA          | SMB_550             | SMB                 | 21 39    |
| HDA_BIT_CLK               | HDA_550             | HDA                 | 21 49    |
| HDA_BIT_CLK_R             | HDA_550             | HDA                 | 21       |
| HDA_SYNC                  | HDA_550             | HDA                 | 21 49    |
| HDA_SYNC_R                | HDA_550             | HDA                 | 21       |
| HDA_RST_E_L               | HDA_550             | HDA                 | 21       |
| HDA_RST_E                 | HDA_550             | HDA                 | 21 49    |
| HDA_RST_N                 | HDA_550             | HDA                 | 21 49    |
| HDA_SDI0                  | HDA_550             | HDA                 | 21 49    |
| HDA_SDI0_CODEC            | HDA_550             | HDA                 | 21 49    |
| HDA_SDO0T                 | HDA_550             | HDA                 | 21 49    |
| HDA_SDO0T_R               | HDA_550             | HDA                 | 21       |
| MCP_HDA_PULLUP_COMP       | MCP_HDA_PULLUP_COMP | MCP_HDA_PULLUP_COMP | 21       |
| RM_CLK31K_SINCLK_R        | RM_CLK31K           | RM_CLK31K           | 21 25    |
| RM_CLK31K_SINCLK          | RM_CLK31K           | RM_CLK31K           | 25 36    |
| SPI_CLK_R                 | SPI_550             | SPI                 | 21 38 48 |
| SPI_CLK                   | SPI_550             | SPI                 | 48       |
| SPI_ALT_CLK               | SPI_550             | SPI                 | 38       |
| SPI_MOSI_R                | SPI_550             | SPI                 | 21 38 48 |
| SPI_MOSI                  | SPI_550             | SPI                 | 48       |
| SPI_ALT_MOSI              | SPI_550             | SPI                 | 38       |
| SPI_MISO                  | SPI_550             | SPI                 | 21 38 48 |
| SPI_MISO_R                | SPI_550             | SPI                 | 48       |
| SPI_ALT_MISO              | SPI_550             | SPI                 | 38       |
| SPI_CSD_E_L               | SPI_550             | SPI                 | 21 38    |
| SPI_CSD_L                 | SPI_550             | SPI                 |          |
| SPI_CSI_E_L               | SPI_550             | SPI                 |          |
| SPI_CSI_E_L_USB_MLB       | SPI_550             | SPI                 |          |

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MCP Constraints 2

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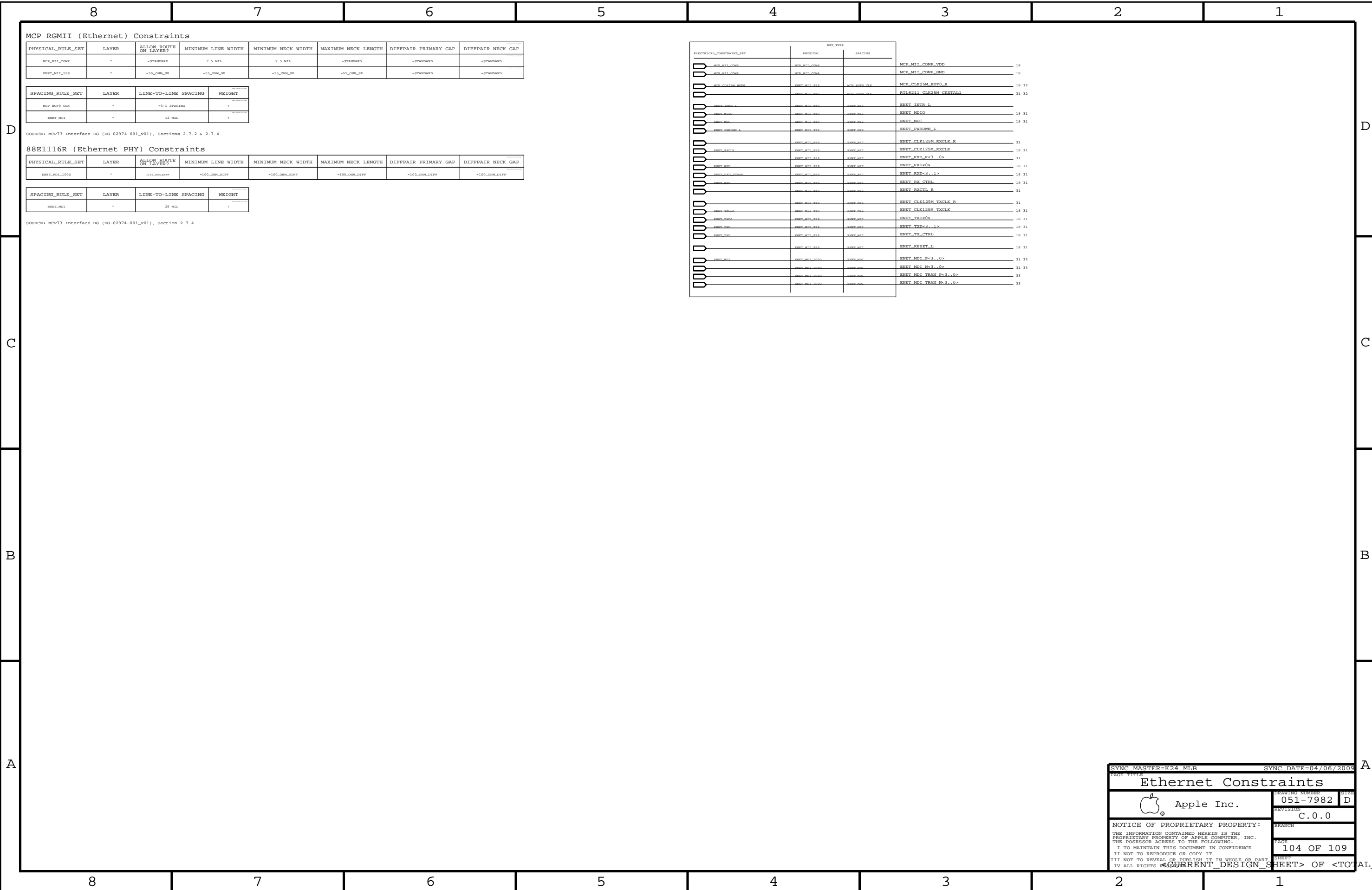
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MCP RGMII (Ethernet) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_MII_COMP      | *     | +STANDARD             | 7.5 MIL            | 7.5 MIL            | +STANDARD           | +STANDARD            | +STANDARD         |
| ENET_MII_55S      | *     | +55_OHM_SE            | +55_OHM_SE         | +55_OHM_SE         | +55_OHM_SE          | +STANDARD            | +STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MCP_BUF0_CLK     | *     | +111_SPACING         | ?      |
| ENET_MII         | *     | 12 MIL               | ?      |

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| ENET_MDI_100D     | *     | +100_OHM_DIFF         | +100_OHM_DIFF      | +100_OHM_DIFF      | +100_OHM_DIFF       | +100_OHM_DIFF        | +100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| ENET_MDI         | *     | 25 MIL               | ?      |

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL      | NET_TYPE                | EFFACTED |
|---------------------------|---------------|-------------------------|----------|
| ENET_MII_COMP_VDD         | MCP_MII_COMP  | MCP_MII_COMP_VDD        | 18       |
| ENET_MII_COMP_GND         | MCP_MII_COMP  | MCP_MII_COMP_GND        | 18       |
| MCP_CLK25M_BUF0_R         | MCP_BUF0_CLK  | MCP_CLK25M_BUF0_R       | 18 31    |
| RTL6211_CLK25M_CRYSTAL1   | MCP_OHM_55    | RTL6211_CLK25M_CRYSTAL1 | 18 31    |
| ENET_INT0_L               | ENET_MII_55S  | ENET_INT0_L             | 18 31    |
| ENET_MDIO                 | ENET_MII_55S  | ENET_MDIO               | 18 31    |
| ENET_MDC                  | ENET_MII_55S  | ENET_MDC                | 18 31    |
| ENET_PRR0VDD_L            | ENET_MII_55S  | ENET_PRR0VDD_L          | 18 31    |
| ENET_CLK125M_RXCLK_R      | ENET_MII_55S  | ENET_CLK125M_RXCLK_R    | 31       |
| ENET_CLK125M_RXCLK        | ENET_MII_55S  | ENET_CLK125M_RXCLK      | 18 31    |
| ENET_RXD<3..0>            | ENET_MII_55S  | ENET_RXD<3..0>          | 31       |
| ENET_RXD<0>               | ENET_MII_55S  | ENET_RXD<0>             | 18 31    |
| ENET_RXD<3..1>            | ENET_MII_55S  | ENET_RXD<3..1>          | 18 31    |
| ENET_RX_CTRL              | ENET_MII_55S  | ENET_RX_CTRL            | 18 31    |
| ENET_RXCTL0_R             | ENET_MII_55S  | ENET_RXCTL0_R           | 31       |
| ENET_CLK125M_TXCLK_R      | ENET_MII_55S  | ENET_CLK125M_TXCLK_R    | 31       |
| ENET_CLK125M_TXCLK        | ENET_MII_55S  | ENET_CLK125M_TXCLK      | 18 31    |
| ENET_TXD<0>               | ENET_MII_55S  | ENET_TXD<0>             | 18 31    |
| ENET_TXD<3..1>            | ENET_MII_55S  | ENET_TXD<3..1>          | 18 31    |
| ENET_TX_CTRL              | ENET_MII_55S  | ENET_TX_CTRL            | 18 31    |
| ENET_RESET_L              | ENET_MII_55S  | ENET_RESET_L            | 18 31    |
| ENET_MDI_P<3..0>          | ENET_MDI_100D | ENET_MDI_P<3..0>        | 31 33    |
| ENET_MDI_N<3..0>          | ENET_MDI_100D | ENET_MDI_N<3..0>        | 31 33    |
| ENET_MDI_TRAN_P<3..0>     | ENET_MDI_100D | ENET_MDI_TRAN_P<3..0>   | 33       |
| ENET_MDI_TRAN_N<3..0>     | ENET_MDI_100D | ENET_MDI_TRAN_N<3..0>   | 33       |

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**Ethernet Constraints**

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| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 1701_DIFFPAIR     | *     | *STANDARD             | *STANDARD          | *STANDARD          | *STANDARD           | 0.1 MM               | 0.1 MM            |

SMC SMBus Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | NET_TYPE            |
|---------------------------|----------|---------|---------------------|
| SMC_SMB_A_S1_SCL          | SMC_A00  | SMC     | SMBUS_SMC_A_S1_SCL  |
| SMC_SMB_A_S1_SDA          | SMC_A00  | SMC     | SMBUS_SMC_A_S1_SDA  |
| SMC_SMB_B_S0_SCL          | SMC_B00  | SMC     | SMBUS_SMC_B_S0_SCL  |
| SMC_SMB_B_S0_SDA          | SMC_B00  | SMC     | SMBUS_SMC_B_S0_SDA  |
| SMC_SMB_C_S0_SCL          | SMC_C00  | SMC     | SMBUS_SMC_C_S0_SCL  |
| SMC_SMB_C_S0_SDA          | SMC_C00  | SMC     | SMBUS_SMC_C_S0_SDA  |
| SMC_SMB_D_S0_SCL          | SMC_D00  | SMC     | SMBUS_SMC_D_S0_SCL  |
| SMC_SMB_D_S0_SDA          | SMC_D00  | SMC     | SMBUS_SMC_D_S0_SDA  |
| SMC_SMB_E0A_SCL           | SMC_E00  | SMC     | SMBUS_SMC_E0A_SCL   |
| SMC_SMB_E0A_SDA           | SMC_E00  | SMC     | SMBUS_SMC_E0A_SDA   |
| SMC_SMB_M0MNT_SCL         | SMC_M00  | SMC     | SMBUS_SMC_M0MNT_SCL |
| SMC_SMB_M0MNT_SDA         | SMC_M00  | SMC     | SMBUS_SMC_M0MNT_SDA |

SMBus Charger Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | NET_TYPE   |
|---------------------------|----------|---------|------------|
| CHGR_C01                  | CHGR_C00 | CHGR    | CHGR_C01_P |
| CHGR_C02                  | CHGR_C00 | CHGR    | CHGR_C02_M |
| CHGR_C03                  | CHGR_C00 | CHGR    | CHGR_C03_P |
| CHGR_C04                  | CHGR_C00 | CHGR    | CHGR_C04_M |

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SMC Constraints





K84 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

| BOARD LAYERS  |  |  |  | BOARD AREAS       |  |  |  | BOARD UNITS (MIL OR MM) | ALLEGRO VERSION |
|---|--|--|--|-------------------|--|--|--|-------------------------|-----------------|
| TOP, 10L2, 10L3, 10L4, 10L5, 10L6, 10L7, 10L8, 10L9, 10L10, 10L11, BOTTOM |  |  |  | NO_TYPE, BGA_P10M |  |  |  | MM                      | 15.5.1          |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DEFAULT           | *     | Y                     | =<BGA_OHM_SE       | 0.100MM            | 30 MM               | 0 MM                 | 0 MM              |
| STANDARD          | *     | Y                     | =DEFAULT           | =DEFAULT           | 12.7 MM             | =DEFAULT             | =DEFAULT          |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 55_OHM_SE         | TOP, BOTTOM | Y                     | 0.090 MM           | 0.090 MM           |                     |                      |                   |
| 55_OHM_SE         | *           | Y                     | 0.076 MM           | 0.076 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 50_OHM_SE         | TOP, BOTTOM | Y                     | 0.115 MM           | 0.115 MM           |                     |                      |                   |
| 50_OHM_SE         | *           | Y                     | 0.076 MM           | 0.076 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 40_OHM_SE         | TOP, BOTTOM | Y                     | 0.145 MM           | 0.100 MM           |                     |                      |                   |
| 40_OHM_SE         | *           | Y                     | 0.126 MM           | 0.100 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 274_OHM_SE        | TOP, BOTTOM | Y                     | 0.310 MM           | 0.310 MM           |                     |                      |                   |
| 274_OHM_SE        | *           | Y                     | 0.222 MM           | 0.222 MM           | =STANDARD           | =STANDARD            | =STANDARD         |

| PHYSICAL_RULE_SET | LAYER                  | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|------------------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 70_OHM_DIFF       | *                      | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 70_OHM_DIFF       | 10L3, 10L4, 10L5, 10L6 | Y                     | 0.151 MM           | 0.100 MM           |                     | 0.224 MM             | 0.224 MM          |
| 70_OHM_DIFF       | TOP, BOTTOM            | Y                     | 0.145 MM           | 0.100 MM           |                     | 0.200 MM             | 0.200 MM          |

| PHYSICAL_RULE_SET | LAYER                  | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|------------------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 90_OHM_DIFF       | *                      | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 90_OHM_DIFF       | 10L3, 10L4, 10L5, 10L6 | Y                     | 0.095 MM           | 0.095 MM           |                     | 0.234 MM             | 0.234 MM          |
| 90_OHM_DIFF       | TOP, BOTTOM            | Y                     | 0.112 MM           | 0.112 MM           |                     | 0.220 MM             | 0.220 MM          |

| PHYSICAL_RULE_SET | LAYER                  | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|------------------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 100_OHM_DIFF      | *                      | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 100_OHM_DIFF      | 10L3, 10L4, 10L5, 10L6 | Y                     | 0.075 MM           | 0.075 MM           |                     | 0.244 MM             | 0.244 MM          |
| 100_OHM_DIFF      | TOP, BOTTOM            | Y                     | 0.091 MM           | 0.091 MM           |                     | 0.230 MM             | 0.230 MM          |

| PHYSICAL_RULE_SET | LAYER                  | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|------------------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 100_OHM_DIFF_HSD  | *                      | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 100_OHM_DIFF_HSD  | 10L3, 10L4, 10L5, 10L6 | Y                     | 0.083 MM           | 0.083 MM           |                     | 0.400 MM             | 0.400 MM          |
| 100_OHM_DIFF_HSD  | TOP, BOTTOM            | Y                     | 0.095 MM           | 0.095 MM           |                     | 0.400 MM             | 0.400 MM          |

| PHYSICAL_RULE_SET | LAYER                  | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|------------------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 110_OHM_DIFF      | *                      | N                     | =STANDARD          | =STANDARD          | =STANDARD           | =STANDARD            | =STANDARD         |
| 110_OHM_DIFF      | 10L3, 10L4, 10L5, 10L6 | Y                     | 0.075 MM           | 0.075 MM           |                     | 0.330 MM             | 0.330 MM          |
| 110_OHM_DIFF      | TOP, BOTTOM            | Y                     | 0.077 MM           | 0.077 MM           |                     | 0.330 MM             | 0.330 MM          |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFPPAIR PRIMARY GAP | DIFPPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 111_DIFPPAIR      | *     | Y                     | =STANDARD          | =STANDARD          | =STANDARD           | 0.1 MM               | 0.1 MM            |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| DEFAULT          | *     | 0.1 MM               | ?      |
| STANDARD         | *     | =DEFAULT             | ?      |
| BGA_P10M         | *     | =DEFAULT             | ?      |
| BGA_P20M         | *     | =DEFAULT             | ?      |
| BGA_P30M         | *     | =DEFAULT             | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| 1.5:1_SPACING    | *     | 0.15 MM              | ?      |
| 2:1_SPACING      | *     | 0.2 MM               | ?      |
| 2.5:1_SPACING    | *     | 0.25 MM              | ?      |
| 3:1_SPACING      | *     | 0.3 MM               | ?      |
| 4:1_SPACING      | *     | 0.4 MM               | ?      |

| SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------------|----------------------|--------|
| 2X_DIELECTRIC    | TOP, BOTTOM | 0.140 MM             | ?      |
| 3X_DIELECTRIC    | TOP, BOTTOM | 0.210 MM             | ?      |
| 4X_DIELECTRIC    | TOP, BOTTOM | 0.280 MM             | ?      |
| 5X_DIELECTRIC    | TOP, BOTTOM | 0.350 MM             | ?      |
| 2X_DIELECTRIC    | *           | 0.126 MM             | ?      |
| 3X_DIELECTRIC    | *           | 0.189 MM             | ?      |
| 4X_DIELECTRIC    | *           | 0.252 MM             | ?      |
| 5X_DIELECTRIC    | *           | 0.315 MM             | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| *                 | *                 | BGA_P10M  | BGA_P10M         |
| MEM_CLK           | *                 | BGA_P10M  | BGA_P10M         |
| CLK_PSB           | *                 | BGA_P10M  | BGA_P10M         |
| CLK_LPC           | *                 | BGA_P10M  | BGA_P10M         |
| CLK_PCI           | *                 | BGA_P10M  | BGA_P10M         |
| CLK_PCIE          | *                 | BGA_P10M  | BGA_P10M         |
| CLK_SLOW          | *                 | BGA_P10M  | BGA_P10M         |
| FSB_D0T6          | FSB_D0T6          | BGA_P10M  | BGA_P10M         |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| MEM_400           | BGA_P10M  | STANDARD          |
| MEM_400_VDD       | BGA_P10M  | STANDARD          |

SYNC MASTER=K24 MLB SYNC DATE=01/19/2009

K84 RULE DEFINITIONS

Apple Inc.  
 DRAWING NUMBER: 051-7982 D  
 REVISION: C.0.0

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