

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2010-03-18

SCHEM, MLB_LDO, K6

PVT, 3/18/10

Page	Contents	Sync	Date
1	Table of Contents	K17_MLB	05/20/2009
2	System Block Diagram	K69_MLB	08/19/2009
3	Power Block Diagram	K69_MLB	08/19/2009
4	BOM Configuration	K24_MLB	07/20/2009
5	Revision History	K24_MLB	07/20/2009
6	FUNC TEST	K24_MLB	07/20/2009
7	Power Aliases	K24_MLB	07/20/2009
8	SIGNAL ALIAS	K24_MLB	07/20/2009
9	CPU FSB	T27_MLB	08/27/2009
10	CPU Power & Ground	T27_MLB	07/20/2009
11	CPU Decoupling	T27_MLB	11/23/2009
12	eXtended Debug Port (mini-XDP)	T27_MLB	07/28/2009
13	MCP CPU Interface	T27_MLB	11/05/2009
14	MCP Memory Interface	T27_MLB	08/06/2009
15	MCP PCIe Interfaces	T27_MLB	11/05/2009
16	MCP Graphics	T27_MLB	11/05/2009
17	MCP SATA, USB & Ethernet	T27_MLB	11/23/2009
18	MCP HDA, LPC & MISC	T27_MLB	11/23/2009
19	MCP Power & Ground	T27_MLB	08/06/2009
20	MCP89 Memory Rail Gating	T27_MLB	11/23/2009
21	MCP89 GFX Core Rail Gating	T27_MLB	11/23/2009
22	MCP Standard Decoupling	T27_MLB	08/15/2009
23	MCP Graphics Support	T27_MLB	08/06/2009
24	SB Misc	T27_MLB	07/28/2009
25	DDR3 SO-DIMM Connector A	T27_MLB	07/28/2009
26	DDR3 SO-DIMM Connector B	T27_MLB	07/28/2009
27	DDR3 BYTE/BIT SWAPS-K6	K18_MLB	06/19/2009
28	FSB/DDR3 Vref Margining	T27_MLB	09/29/2009
29	RIGHT CLUTCH CONNECTOR	T27_MLB	07/28/2009
30	SecureDigital Card Reader	T27_MLB	09/30/2009
31	Ethernet PHY (Caesar II/IV)	T27_MLB	08/20/2009
32	Ethernet Connector	T27_MLB	07/28/2009
33	FireWire LLC/PHY (FW643E)	T27_MLB	07/20/2009
34	FireWire Port & PHY Power	T27_MLB	12/15/2009
35	FireWire Connector	T27_MLB	07/28/2009
36	SATA Connectors	T27_MLB	08/06/2009
37	External USB Connectors	T27_MLB	08/27/2009
38	Internal USB Support	T27_MLB	08/27/2009
39	SMC	T27_MLB	09/02/2009
40	SMC Support	T27_MLB	09/02/2009
41	LPC+SPI Debug Connector	T27_MLB	08/27/2009
42	K6 SMBUS CONNECTIONS	T27_MLB	08/21/2009
43	Voltage Sensing	T27_MLB	08/27/2009
44	Current Sensing	T27_MLB	09/30/2009
45	Thermal Sensors	T27_MLB	08/27/2009

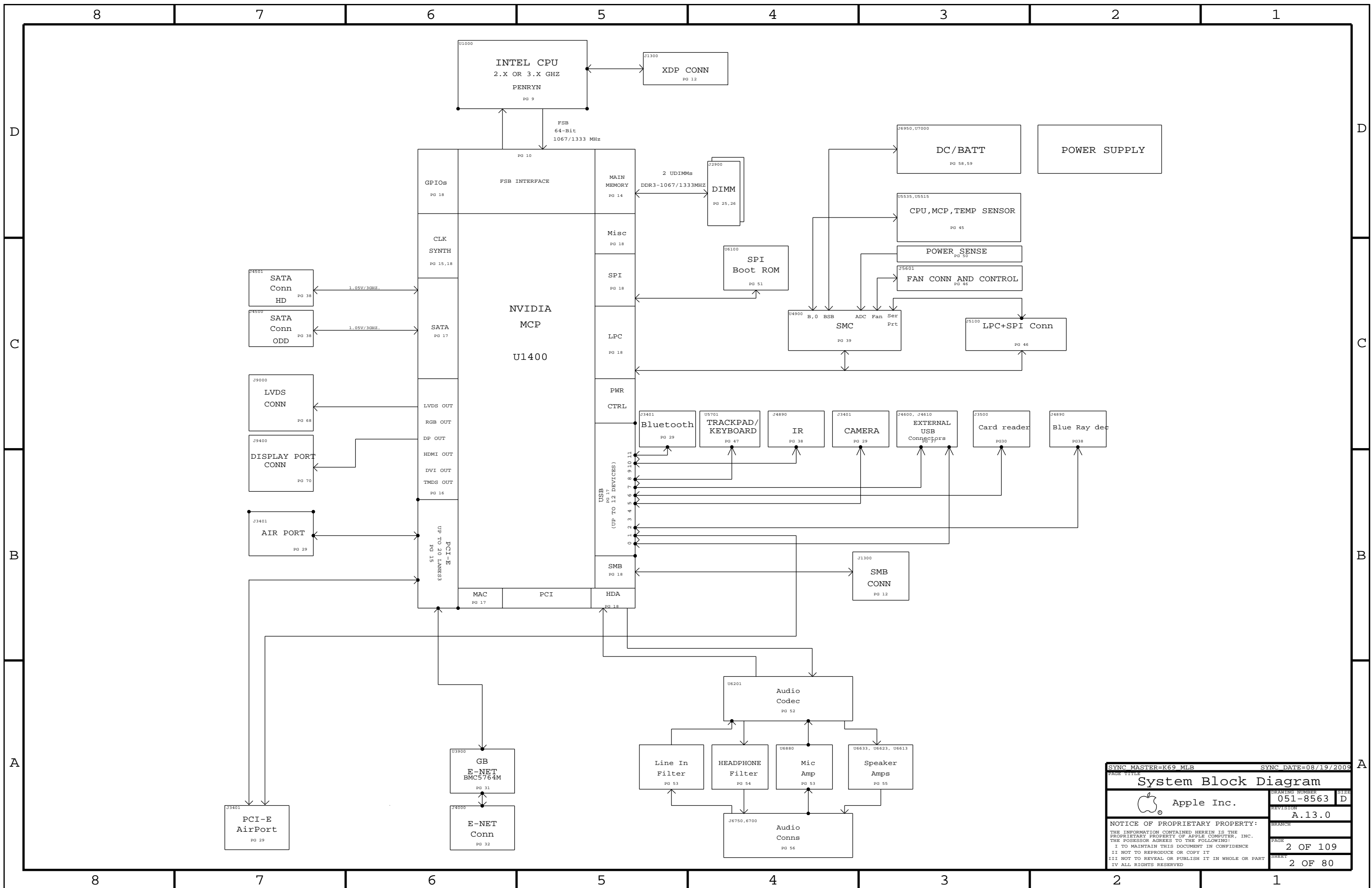
Page	Contents	Sync	Date
46	Fan	K24_MLB	07/20/2009
47	WELLSPRING 1	T27_MLB	08/15/2009
48	WELLSPRING 2	T27_MLB	08/03/2009
49	Sudden Motion Sensor (SMS)	T27_MLB	07/20/2009
50	SPI ROM	T27_MLB	10/21/2009
51	AUDIO: CODEC/REGULATOR	AUDIO	08/31/2009
52	AUDIO: LINE INPUT FILTER	AUDIO	07/17/2009
53	AUDIO: HEADPHONE FILTER	AUDIO	07/17/2009
54	AUDIO: SPEAKER AMP	AUDIO	07/17/2009
55	AUDIO: JACK	AUDIO	08/25/2009
56	AUDIO: JACK TRANSLATORS	AUDIO	08/27/2009
57	DC-In & Battery Connectors	K24_MLB	07/20/2009
58	PBus Supply & Battery Charger	T27_MLB	07/29/2009
59	5V/3.3V SUPPLY	K24_MLB	07/20/2009
60	1.5V/1.35V LVDDR3 Supply	T27_MLB	08/06/2009
61	IMVP6 CPU VCore Regulator	K24_MLB	07/20/2009
62	MCP VCore Regulator	T27_MLB	08/18/2009
63	CPU VTT(1.05V) SUPPLY	K24_MLB	07/20/2009
64	Misc Power Supplies	T27_MLB	09/30/2009
65	Power Sequencing	T27_MLB	11/24/2009
66	Power FETs	T27_MLB	08/27/2009
67	LVDS CONNECTOR	K24_MLB	07/20/2009
68	DISPLAYPORT SUPPORT	K69_MLB	08/12/2009
69	DisplayPort Connector	K24_MLB	07/20/2009
70	LCD Backlight Driver	K69_MLB	08/27/2009
71	LCD Backlight Support	T27_MLB	07/28/2009
72	CPU/FSB Constraints	T27_MLB	08/03/2009
73	Memory Constraints	T27_MLB	08/03/2009
74	MCP Constraints 1	T27_MLB	08/03/2009
75	MCP Constraints 2	T27_MLB	08/27/2009
76	Ethernet Constraints	T27_MLB	11/23/2009
77	FireWire Constraints	T27_MLB	07/20/2009
78	SMC Constraints	T27_MLB	07/28/2009
79	K6/K69 Specific Constraints	T27_MLB	09/08/2009
80	K6/K69 PCB Rule Definitions	T27_MLB	08/06/2009

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8563	1	SCHEM, MLB_LDO, K6	SCH	CRITICAL	
820-2879	1	PCBP, MLB_LDO, K6	PCB	CRITICAL	

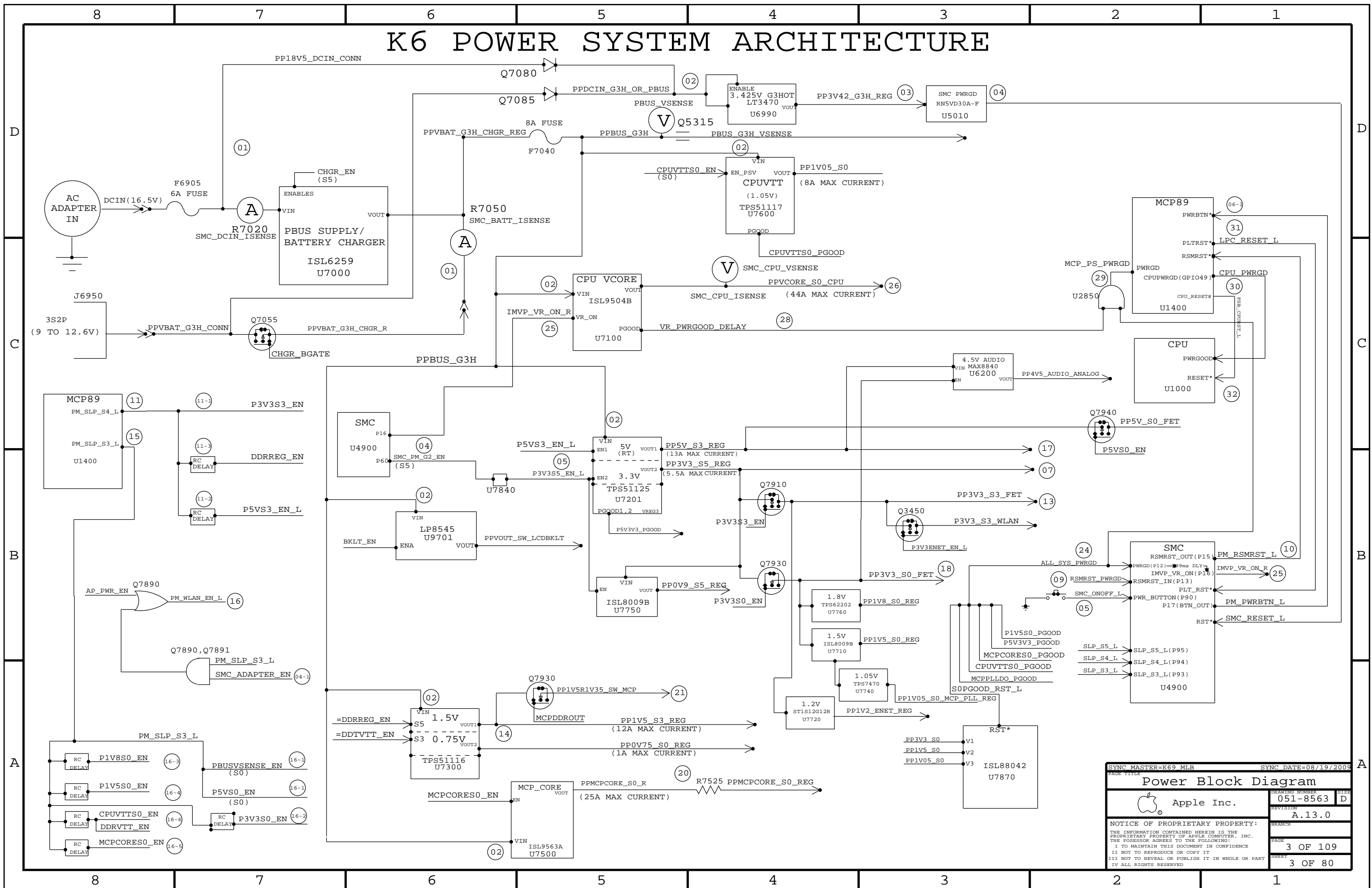
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 ABBREV=DRAWING

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DRAWING NUMBER		051-8563	SIZE D
REVISION		A.13.0	
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SYNC MASTER=K69 MLB		SYNC DATE=08/19/2009	
System Block Diagram			
Apple Inc.		DRAWING NUMBER 051-8563	SIZE D
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K6 POWER SYSTEM ARCHITECTURE



PAGE TITLE		SYNC DATE=08/19/2009	
Power Block Diagram			
Apple Inc.		DRAWING NUMBER	051-8563
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		PAGE	3 OF 109
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1120	PCBA,MLB_LDO,BETTER,K6	K6_COMMON,CPU:2.4GHZ,MCP89M:A02,EEEE:DD24
639-1119	PCBA,MLB_LDO,BEST,K6	K6_COMMON,CPU:2.66GHZ,MCP89M:A02,EEEE:DD23
085-1634	K6_MLB_LDO DEVELOPMENT BOM	K6_DEVEL:PVT

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD23]	CRITICAL	EEEE:DD23
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD24]	CRITICAL	EEEE:DD24

BOM Groups

BOM GROUP	BOM OPTIONS
K6_COMMON	COMMON,ALTERNATE,K6_MISC,K6_DEBUG:PROD,K6_BL,K6_PROGPARTS,RDRV:NO,SPI:25MHZ,CPU_CAP:15
K6_MISC	DP_ESD,MIKEY,BCM5764M,GL137,ENET_ESD,VFRQ:SLPS3,LVDDR3:YES,MCPPLL_R:REG,S0PGOOD_BJT,BOOST_VOL:LOW,HDA:1.5V
K6_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG,IR:PROG,WELLSRING:PROG
K6_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,RDRV:IN_DEVEL
K6_DEVEL:PVT	LPCPLUS,XDP_CONN
K6_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K6_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K6_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO,LPCPLUS,MCPHVDD:P2V5,LDO:FIXED,HTOL_SENSE:YES

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3769	1	PDC,SLQVT,FRQ,2.26,25W,1066,RO,3M,BGA,P7550	U1000	CRITICAL	CPU:2.26GHZ
337S3680	1	PDC,LQDZ,FRQ,2.40,25W,1066,RO,3M,BGA	U1000	CRITICAL	CPU:2.4GHZ
337S3756	1	PDC,SLQPV,FRQ,2.53,25W,1066,RO,3M,BGA	U1000	CRITICAL	CPU:2.53GHZ
337S3761	1	PDC,SLGLA,FRQ,2.66,25W,1066,RO,3M,BGA	U1000	CRITICAL	CPU:2.66GHZ
337S3797	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A01
337S3866	1	IC,MCP89M-A01,31X31MM,BGA1168	U1400	CRITICAL	MCP89M:A02
341S2731	1	IC,1MBIT,SPI FLASH,K17/18	U3990	CRITICAL	BCM5764M
343S0493	1	IC,ASIC,BCM5764M,ENET CONTROLLER, 8x8, 64QFN	U3900	CRITICAL	BCM5764M
338S0753	1	IC,FW643-E2,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
353S2896	1	IC,LP8545,LED BKLT CTRLR,LLP24	U9701	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0563	1	IC,SMC,H58/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0240	1	SMC EXTERNAL,K6	U4900	CRITICAL	SMC:PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0238	1	EFI UNLOCKED,K6/K69	U6100	CRITICAL	BOOTROM:UNLOCKED
341S2589	1	IC,EFI,LOCKED,K6	U6100	CRITICAL	BOOTROM:LOCKED
338S0633	1	IC,CYPRS,CY7C63803-LQXC,4X4MM,USB,24-QFN	U4800	CRITICAL	IR:BLANK
341S2384	1	IC,ENCORE II,CY7C63803-LQXC	U4800	CRITICAL	IR:PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSRING:BLANK
341S2616	1	IC,TP PSOC,K17,K18	U5701	CRITICAL	WELLSRING:PROG

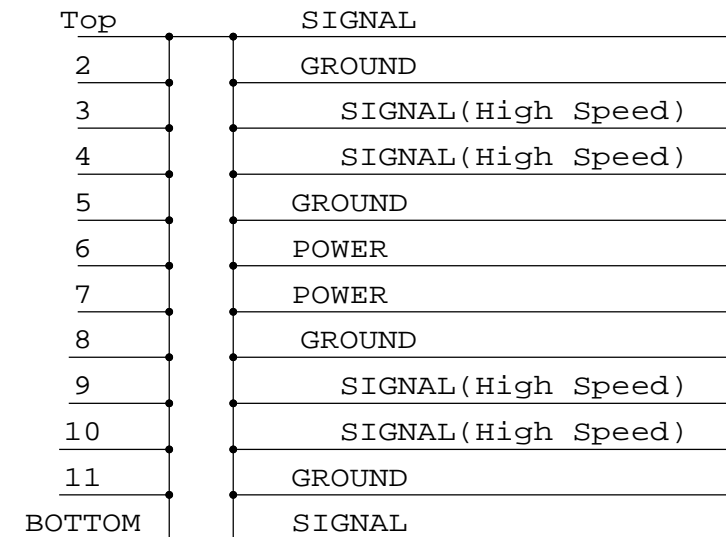
Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	RENEY AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYES AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYES AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
152S1135	152S0586		ALL	TOKO AS ALTERNATE
516-0213	516-0201		ALL	MOLEX AS ALTERNATE
516S0790	516S0706		ALL	MOLEX AS ALTERNATE
376S0699	376S0360		ALL	SEMPEISPE AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1634	1	K6_MLB_LDO DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K6 BOARD STACK-UP



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SYNC MASTER=K24_MLB	
PAGE TITLE	
BOM Configuration	
Apple Inc.	DRAWING NUMBER 051-8563
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Revision History

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B

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Revision History	
 Apple Inc.	DRAWING NUMBER 051-8563
	SIZE D
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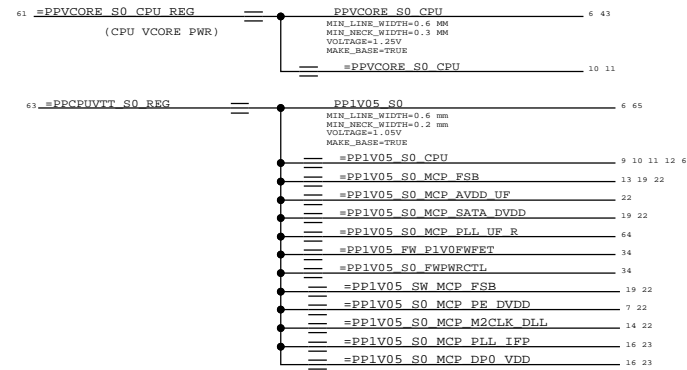
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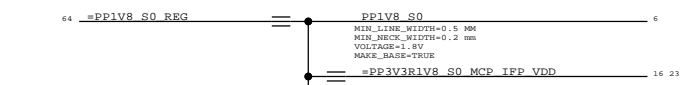
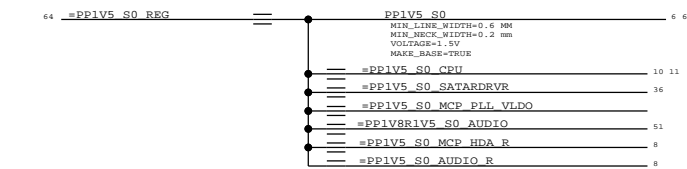
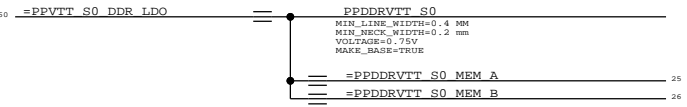
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"S0,SOM" RAILS



LVDDR Vref/VTT (0.75V/0.675V) Rails



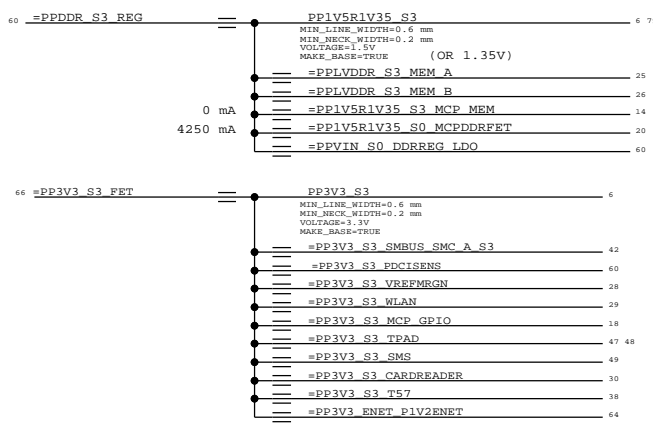
UNUSED MCP PE0[3:0] AVDD/DVDD



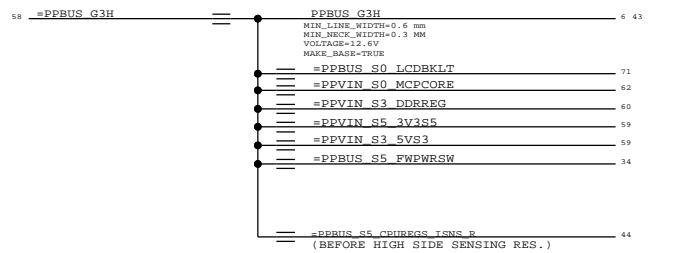
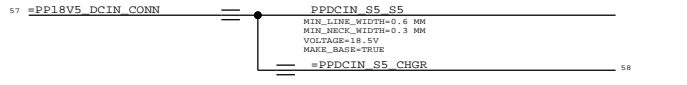
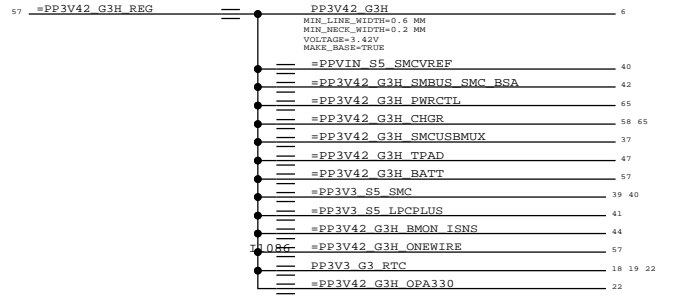
(CONNECTS TO MCP BALLS) 19 =PP1V05_S0 MCP PE DVDD 22 (CONNECTS TO THE DECAPS)
(CONNECTS TO MCP BALLS) 19 =PP1V05_S0 MCP PE AVDD 22 (CONNECTS TO THE DECAPS)

"S3" RAILS

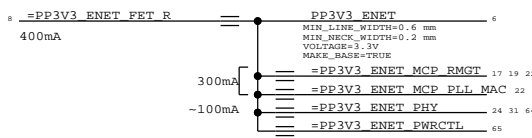
LVDDR (1.5V/1.35V) Rails



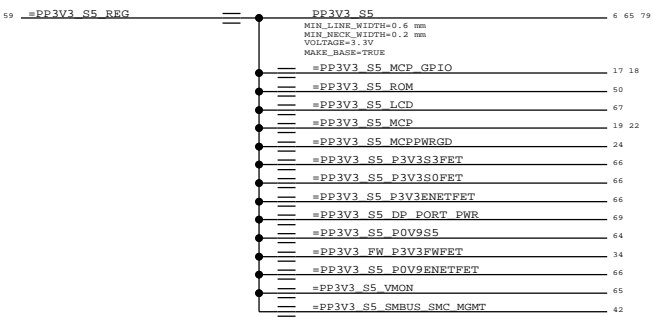
"G3H" RAILS



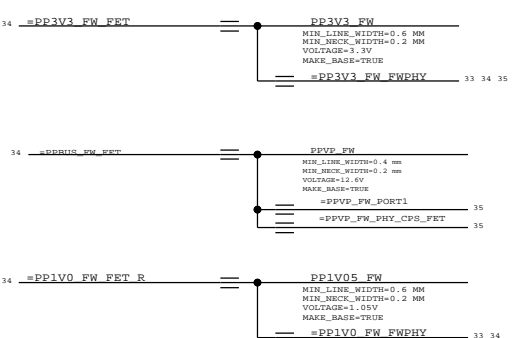
"ENET" RAILS



"S5" RAILS

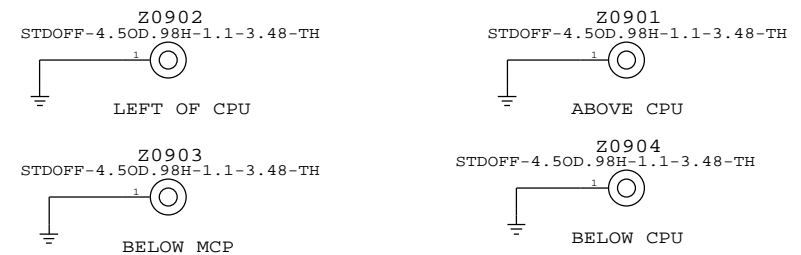


"FIREWIRE" RAILS

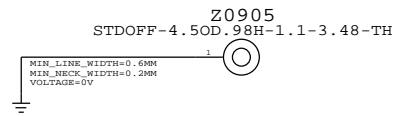


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Power Aliases		DRAWING NUMBER	051-8563
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HEATSINK STANDOFFS



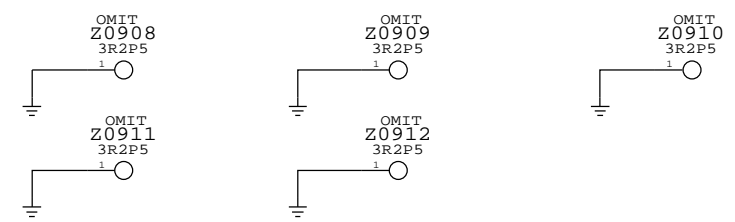
FAN STANDOFF



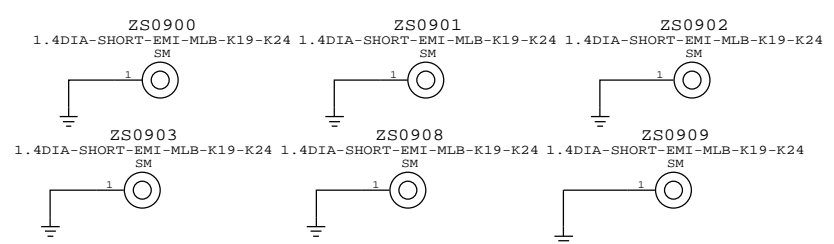
MLB MOUNTING (TO C. BRACKET) SCREW HOLES



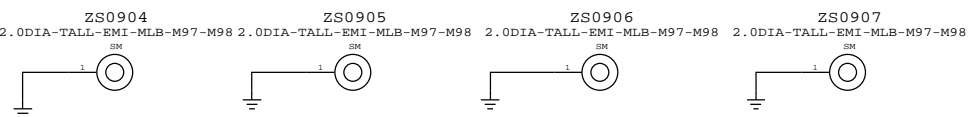
MLB MOUNTING (TO TOPCASE) SCREW HOLES



EMI IO (SHORT) POGO PINS



EMI TALL POGO PINS



PCI-E ALIASES

UNUSED GPU LANES

15	=PEG D2R N<3:0>	==	NC PEG D2R N<3:0>
15	=PEG D2R P<3:0>	==	NC PEG D2R P<3:0>
15	=PEG R2D C N<3:0>	==	NC PEG R2D C N<3:0>
15	=PEG R2D C P<3:0>	==	NC PEG R2D C P<3:0>
74	PEG CLK100M P	==	TP PEG CLK100M P
74	PEG CLK100M N	==	TP PEG CLK100M N
15	PEG CLKREO L	==	TP PEG CLKREO L

USB ALIASES

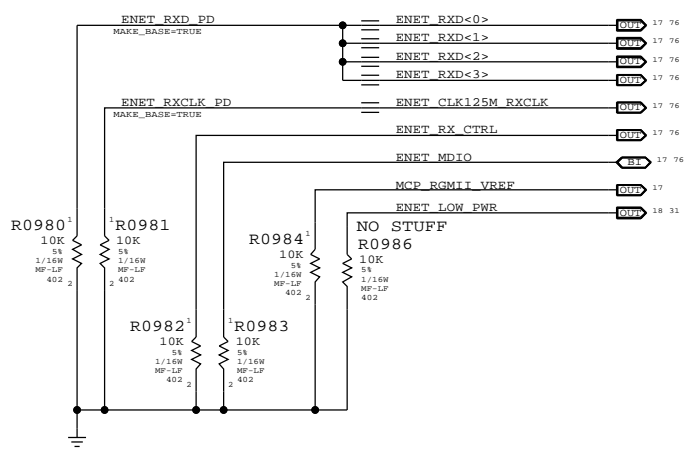
UNUSED USB PORTS

75	17	USB_EXTC_P	==	TP_USB_EXTCP
75	17	USB_EXTC_N	==	TP_USB_EXTCN
75	17	USB_EXTD_P	==	TP_USB_EXTDP
75	17	USB_EXTD_N	==	TP_USB_EXTDN
75	17	USB_WM_P	==	TP_USB_WMP
75	17	USB_WM_N	==	TP_USB_WMN
75	17	USB_MINI_P	==	TP_USB_MINIP
75	17	USB_MINI_N	==	TP_USB_MININ

ETHERNET ALIASES

PLACE_NEAR=U7980.A1:5MM

66	PP3V3_ENET_FET	==	PP3V3_ENET_FET_R
----	----------------	----	------------------



DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

74	MCP_TV_DAC_RSET	==	NC_MCP_TV_DAC_RSET
74	MCP_TV_DAC_VREF	==	NC_MCP_TV_DAC_VREF
	MCP_CLK27M_XTALIN	==	NC_MCP_CLK27M_XTALIN
	MCP_CLK27M_XTALOUT	==	NC_MCP_CLK27M_XTALOUT
74	CRT_IG_R_C_PR	==	NC_CRT_IG_R_C_PR
74	CRT_IG_G_Y_Y	==	NC_CRT_IG_G_Y_Y
74	CRT_IG_B_COMP_PB	==	NC_CRT_IG_B_COMP_PB
74	CRT_IG_HSYNC	==	NC_CRT_IG_HSYNC
74	CRT_IG_VSYNC	==	NC_CRT_IG_VSYNC

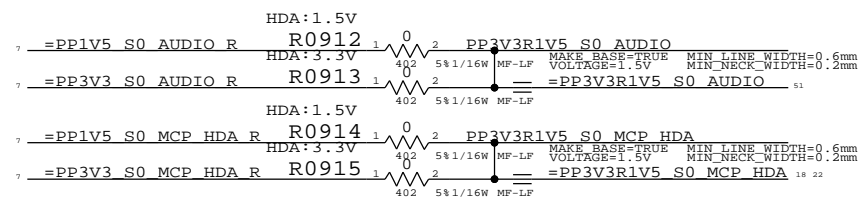
LVDS ALIASES

16	=MCP_IFPA_TXC_P	==	LVDS_IG_A_CLK_P
16	=MCP_IFPA_TXC_N	==	LVDS_IG_A_CLK_N
16	=MCP_IFPA_TXD_P<0..2>	==	LVDS_IG_A_DATA_P<0..2>
16	=MCP_IFPA_TXD_N<0..2>	==	LVDS_IG_A_DATA_N<0..2>
16	=MCP_IFPA_TXD_P<3>	==	NC_LVDS_IG_A_DATAP<3>
16	=MCP_IFPA_TXD_N<3>	==	NC_LVDS_IG_A_DATAN<3>
16	=MCP_IFPB_TXC_P	==	NC_LVDS_IG_B_CLKP
16	=MCP_IFPB_TXC_N	==	NC_LVDS_IG_B_CLKN
16	=MCP_IFPB_TXD_P<0..3>	==	NC_LVDS_IG_B_DATAP<0..3>
16	=MCP_IFPB_TXD_N<0..3>	==	NC_LVDS_IG_B_DATAN<0..3>
16	LCD_IG_BKLT_PWM	==	LCD_BKLT_PWM
16	LCD_IG_BKLT_EN	==	LCD_BKLT_EN
16	=MCP_IFPAB_DDC_CLK	==	LVDS_DDC_CLK
16	=MCP_IFPAB_DDC_DATA	==	LVDS_DDC_DATA

DISPLAY PORT ALIASES

16	DP_IG_ML0_P<0..3>	==	DP_IG_ML_P<0..3>
16	DP_IG_ML0_N<0..3>	==	DP_IG_ML_N<0..3>
16	DP_IG_HPD0	==	DP_EXT_ML_P<0..3>
16	DP_IG_AUX_CH0_P	==	DP_IG_AUX_CH_P
16	DP_IG_AUX_CH0_N	==	DP_IG_AUX_CH_N
68	DP_AUX_CH_C_N	==	DP_EXT_AUX_CH_C_N
68	DP_AUX_CH_C_P	==	DP_EXT_AUX_CH_C_P
68	DP_CA_DET	==	DP_EXT_CA_DET
16	DP_IG_ML1_P<0..3>	==	TP_DP_IG_ML1P<0..3>
16	DP_IG_ML1_N<0..3>	==	TP_DP_IG_ML1N<0..3>
16	DP_IG_AUX_CH1_P	==	TP_DP_IG_AUX_CH1P
16	DP_IG_AUX_CH1_N	==	TP_DP_IG_AUX_CH1N

AUDIO ALIASES



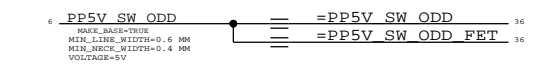
CPU ALIASES

72	CPU_BSEL<0:2>	==	=MCP_BSEL<0:2>
13	CPU_PECT_MCP	==	TP_CPU_PECT_MCP

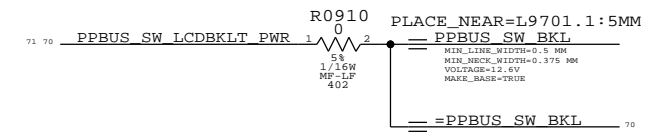
MCP89 ALIASES

16	TP_MCP_RGB_RED	==	NC_MCP_RGB_RED
16	TP_MCP_RGB_GREEN	==	NC_MCP_RGB_GREEN
16	TP_MCP_RGB_BLUE	==	NC_MCP_RGB_BLUE
16	TP_MCP_RGB_HSYNC	==	NC_MCP_RGB_HSYNC
16	TP_MCP_RGB_VSYNC	==	NC_MCP_RGB_VSYNC
16	TP_MCP_RGB_DAC_RSET	==	NC_MCP_RGB_DAC_RSET
16	TP_MCP_RGB_DAC_VREF	==	NC_MCP_RGB_DAC_VREF

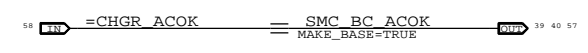
5V ODD ALIASES



BACKLIGHT CONTROLLER ALIASES



CHARGER SIGNAL



MCPCOREISNS SIGNAL

62	MCPCORES0_VO	==	MCPCOREISNS_N
62	MCPCORES0_ISP_R	==	MCPCOREISNS_P

SYNC MASTER=K24_MLB

PAGE TITLE

SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER: 051-8563

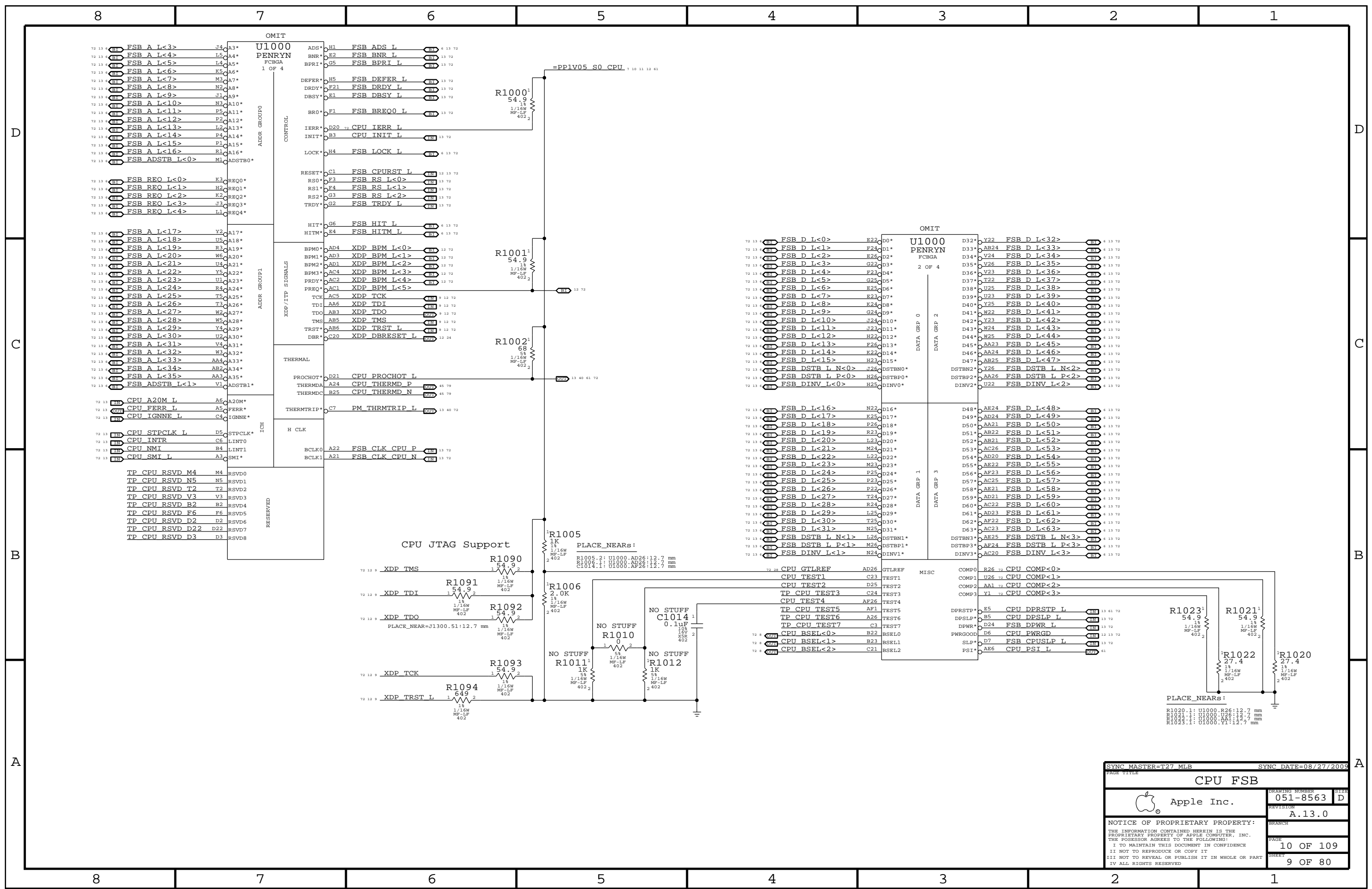
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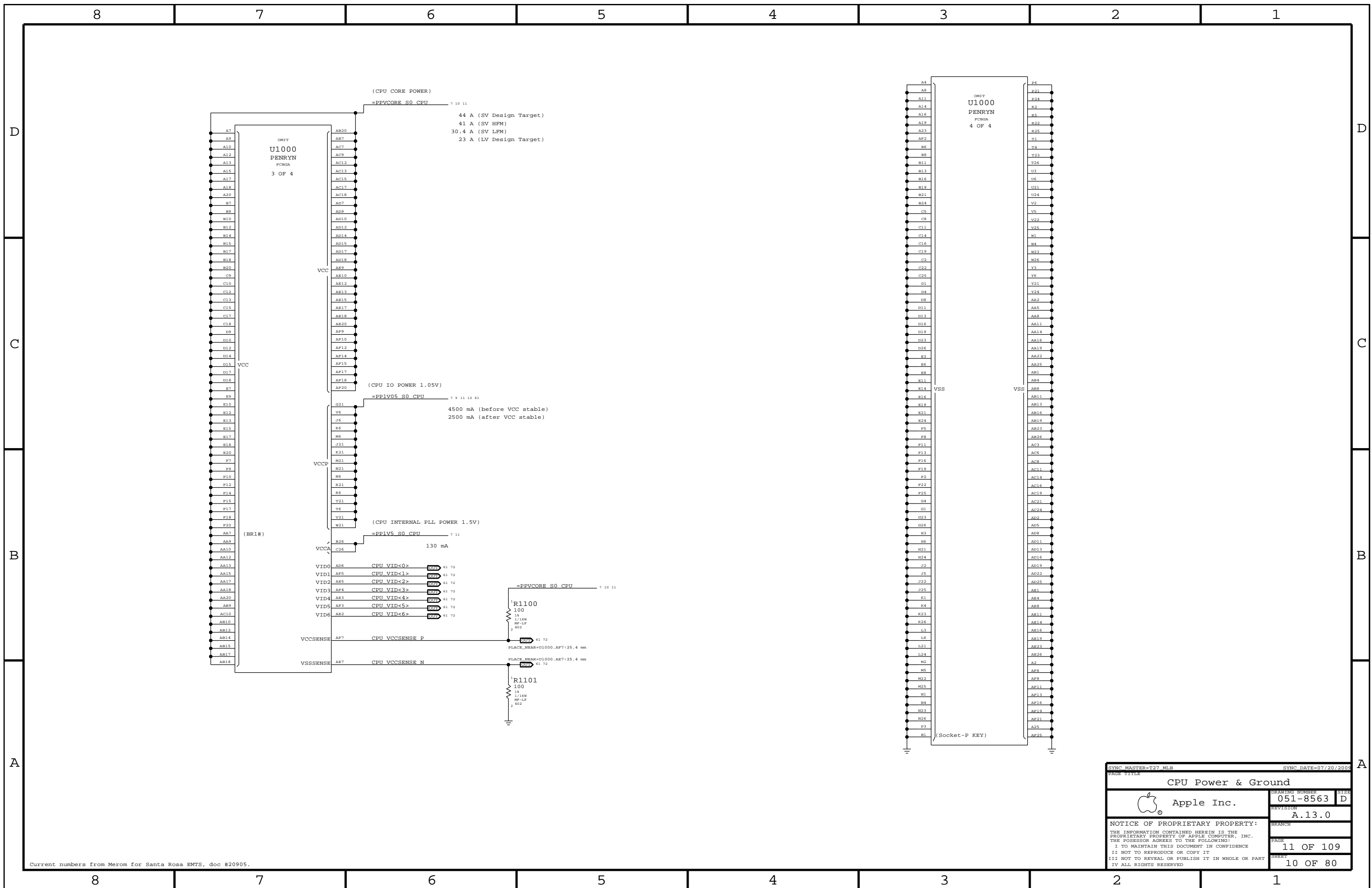
BRANCH: _____

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SHEET: 8 OF 80



PAGE TITLE		SYNC DATE=08/27/2009	
CPU FSB			
Apple Inc.	DRAWING NUMBER	051-8563	SIZE D
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BRANCH		PAGE	10 OF 109
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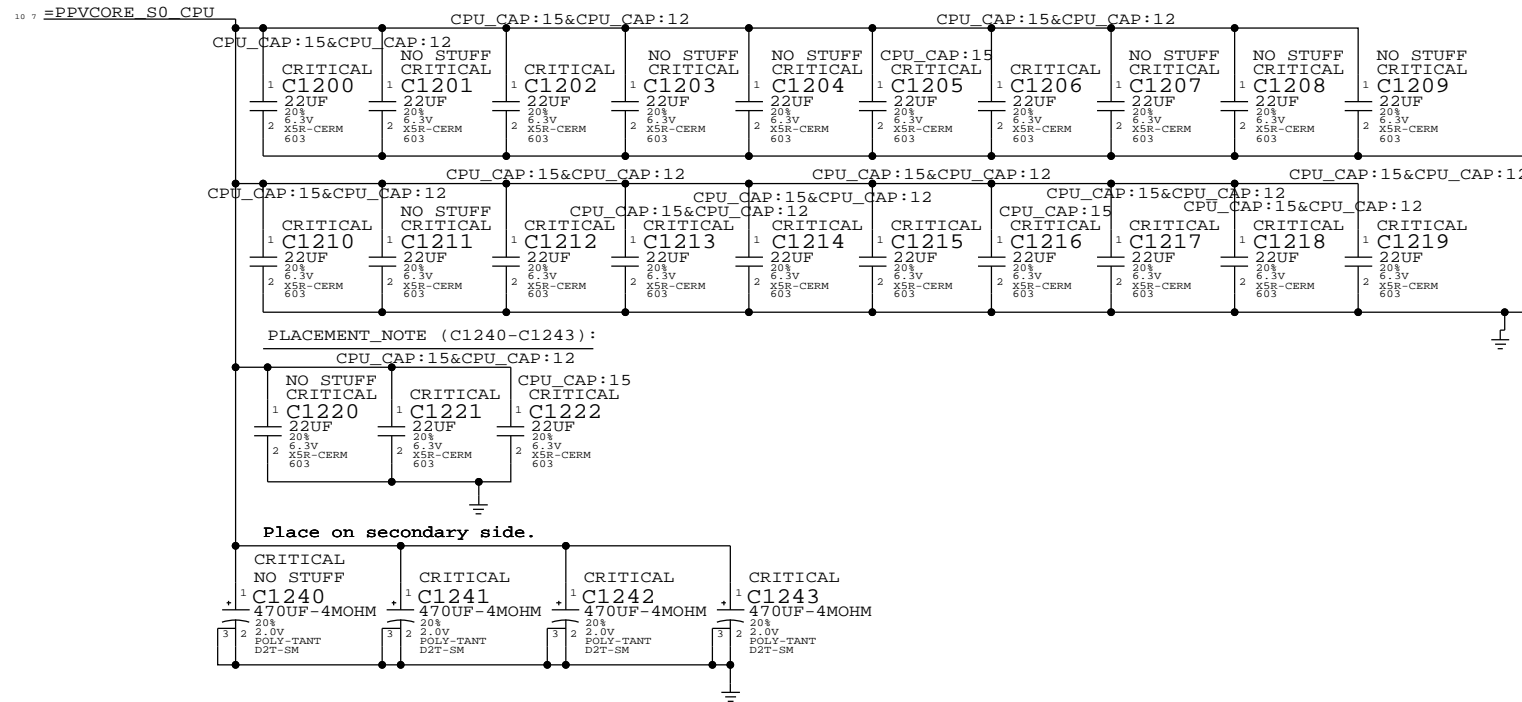
SYNC MASTER=T27_MLB		SYNC DATE=07/20/2005	
PAGE TITLE CPU Power & Ground			
Apple Inc.	DRAWING NUMBER	051-8563	SIZE D
	REVISION	A.13.0	
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		PAGE	11 OF 109
		SHEET	10 OF 80

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU VCore HF and Bulk Decoupling

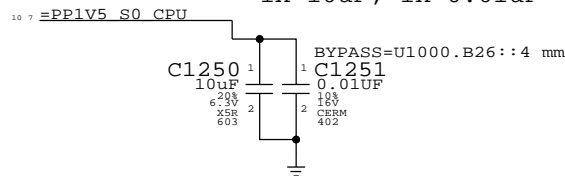
4X 330UF, 20X 22UF 0805

PLACEMENT_NOTE (C1200-C1219):
Place inside socket cavity on secondary side.



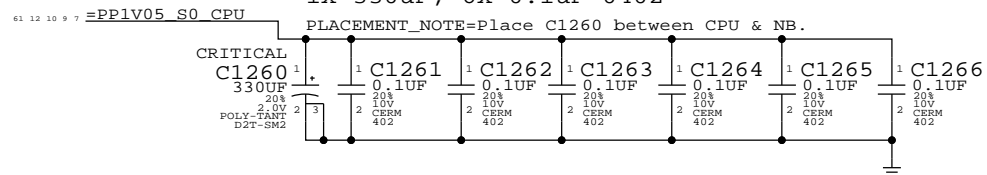
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC MASTER=T27 MLB		SYNC DATE=11/23/2009	
PAGE TITLE CPU Decoupling			
DRAWING NUMBER 051-8563		SIZE D	
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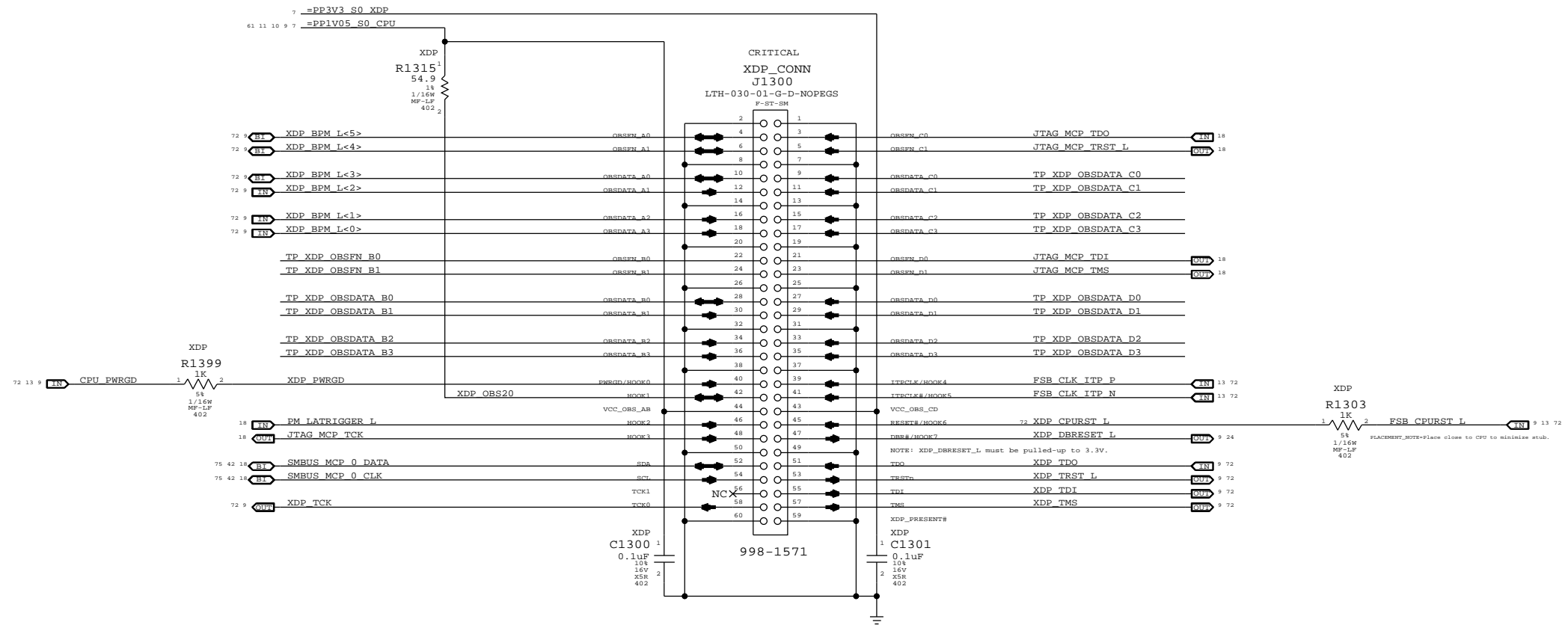
2

1

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP89-specific pinout



← Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
eXtended Debug Port (mini-XDP)			
DRAWING NUMBER		051-8563	SIZE D
REVISION		A.13.0	
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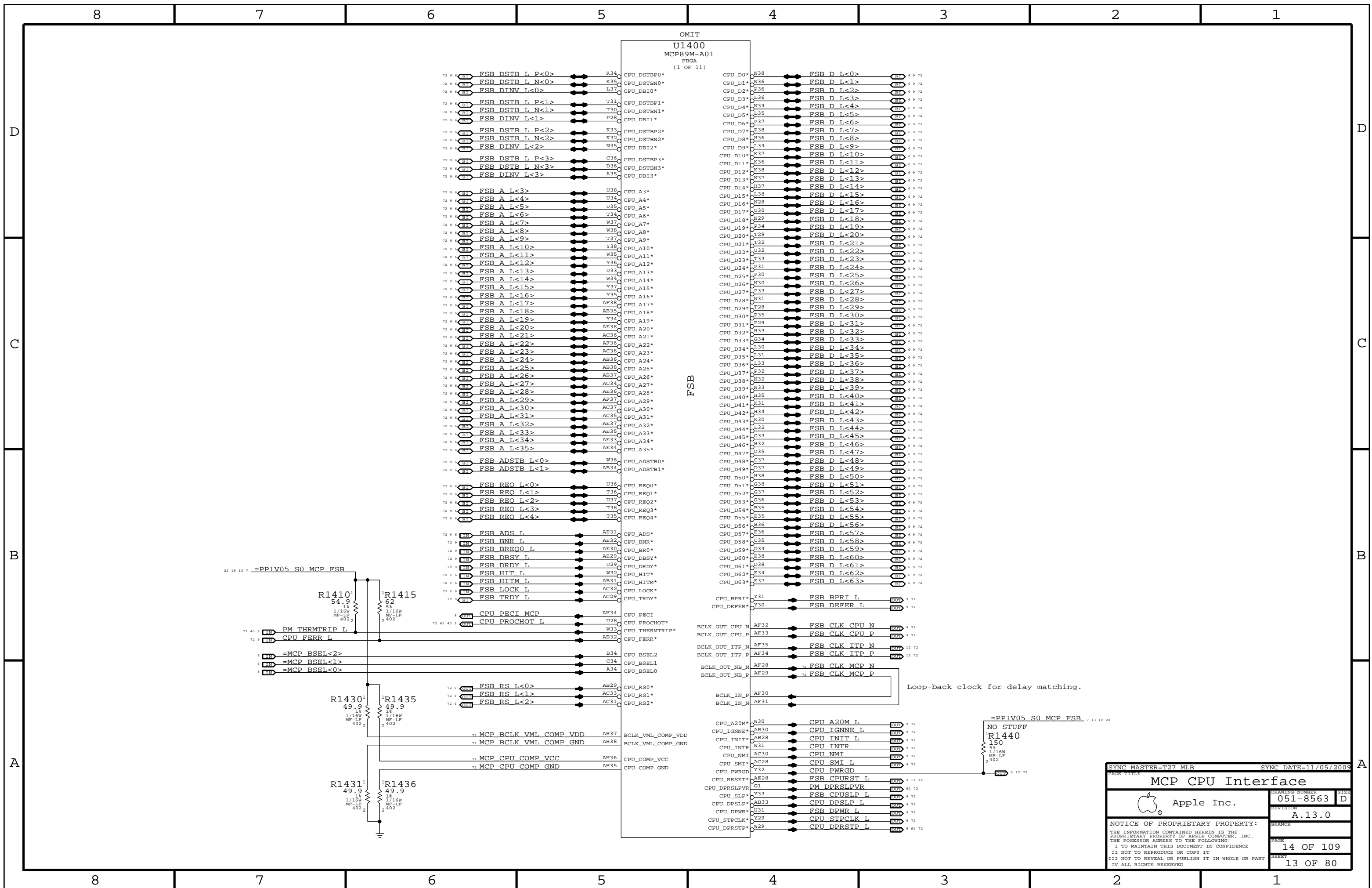
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4

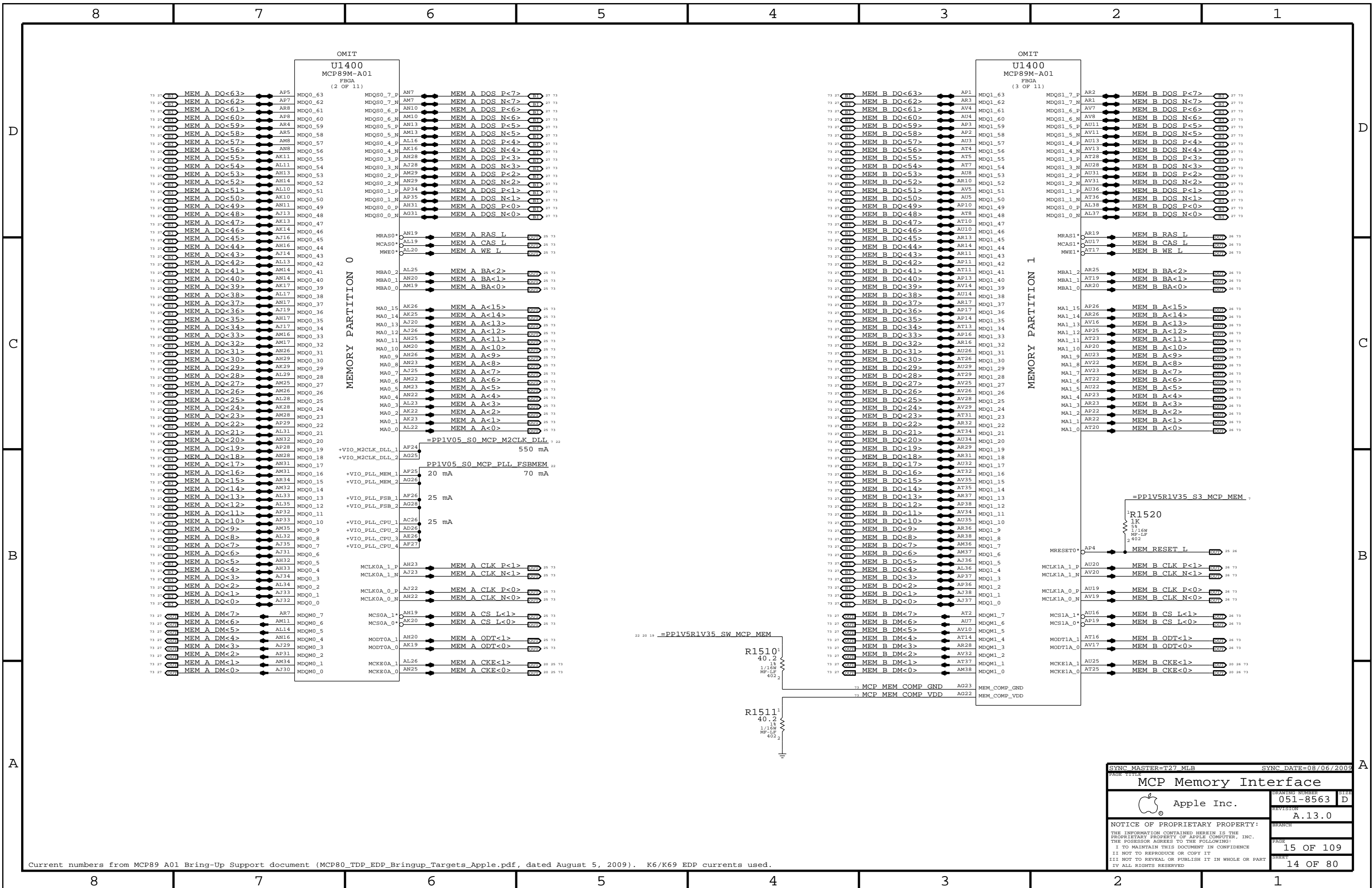
3

2

1

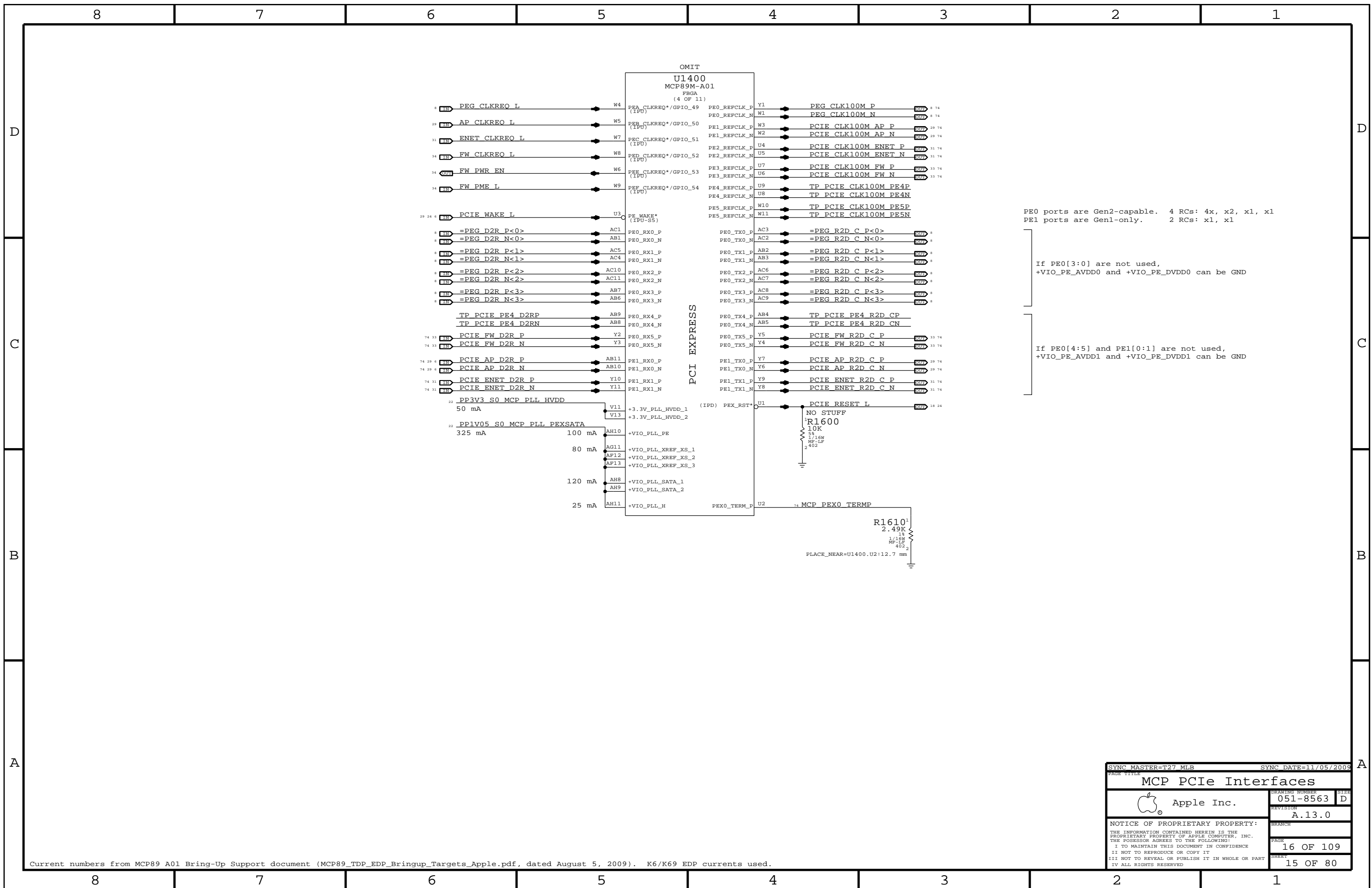


PAGE TITLE		SYNC DATE=11/05/2009	
MCP CPU Interface		DRAWING NUMBER	SIZE
Apple Inc.		051-8563	D
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Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=08/06/2009	
MCP Memory Interface			
Apple Inc.		DRAWING NUMBER	051-8563
		REVISION	A.13.0
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PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
 PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
 +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
 +VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=11/05/2009	
MCP PCIe Interfaces			
Apple Inc.		DRAWING NUMBER 051-8563	SIZE D
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		PAGE 16 OF 109	SHEET 15 OF 80

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C

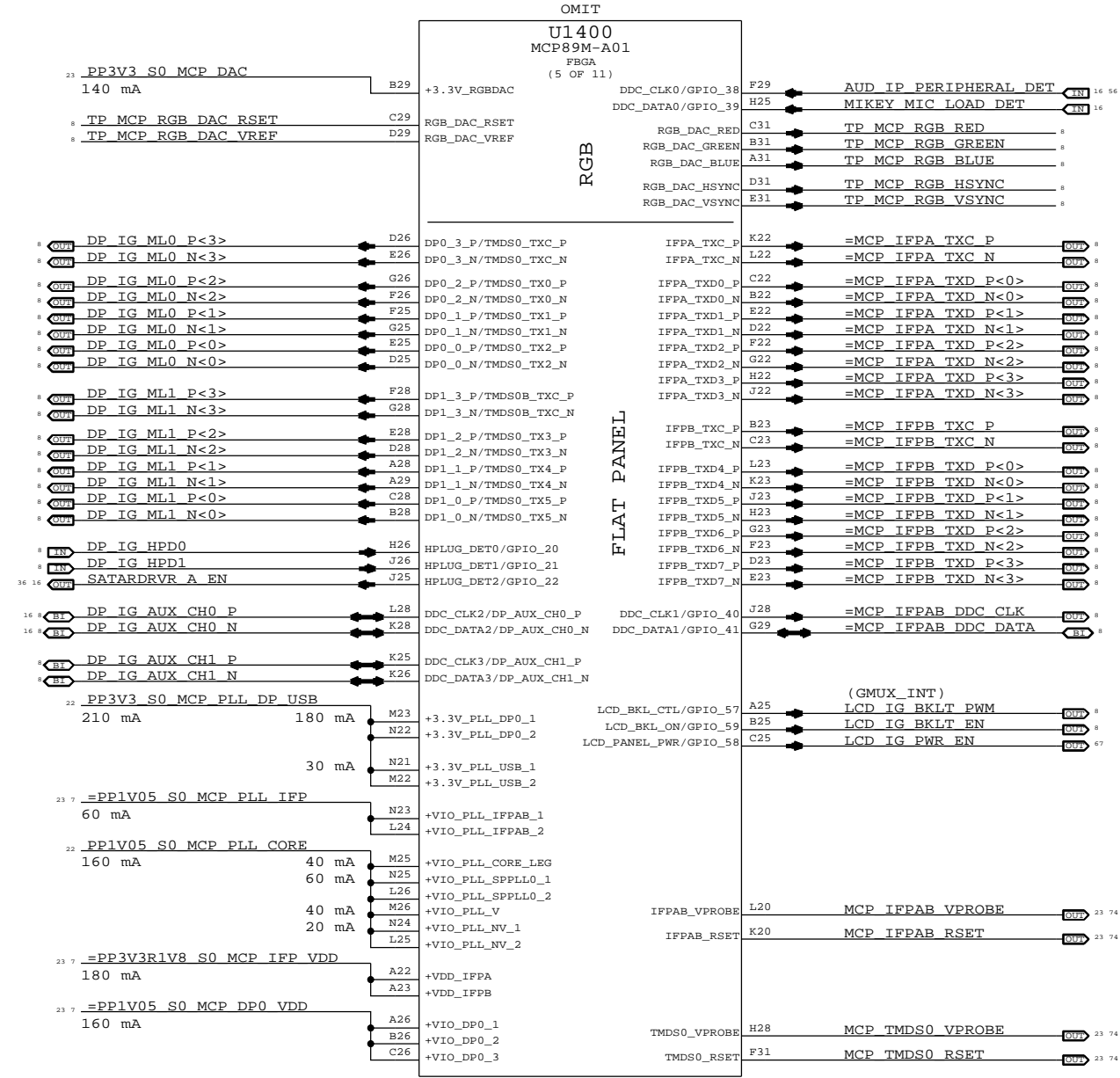
C

B

B

A

A



RGB DAC Disable:
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
 Connect +3.3V_RGBDAC pin to GND.
 NOTE: No Composite/S-Video/Component Video support on MCP89

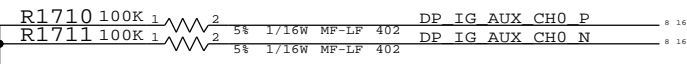
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	TMDS_IG_TXD_P/N<3>	LVDS_IG_A_DATA_P/N<3>
(UNUSED)	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXC_P/N	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<2>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPB_TXD_P/N<3>	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPB_DDC_CLK	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
 TMDS: Power +VDD_IFPx at 3.3V

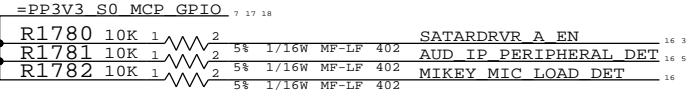
NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

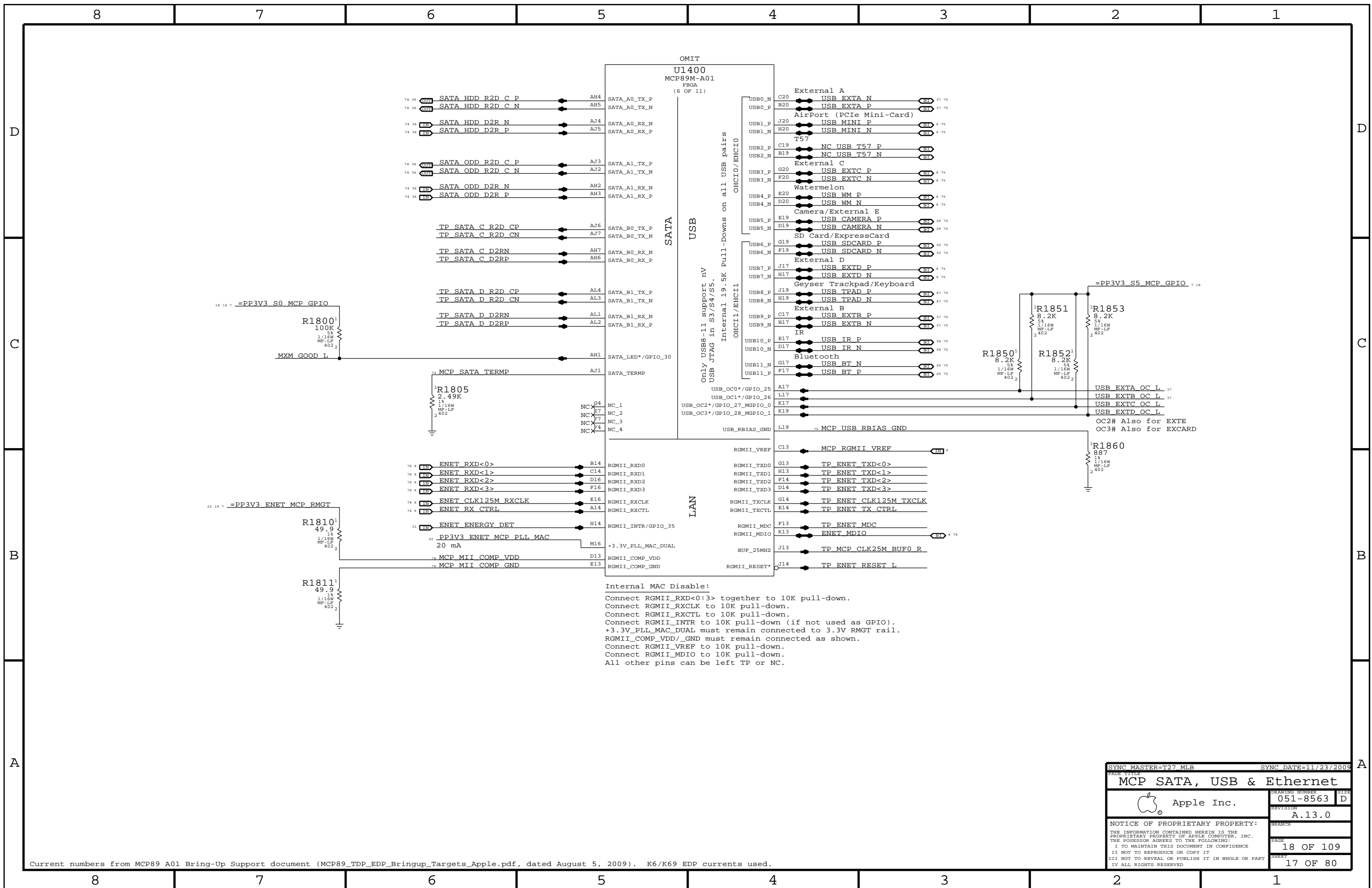


GPIO Pull-Ups



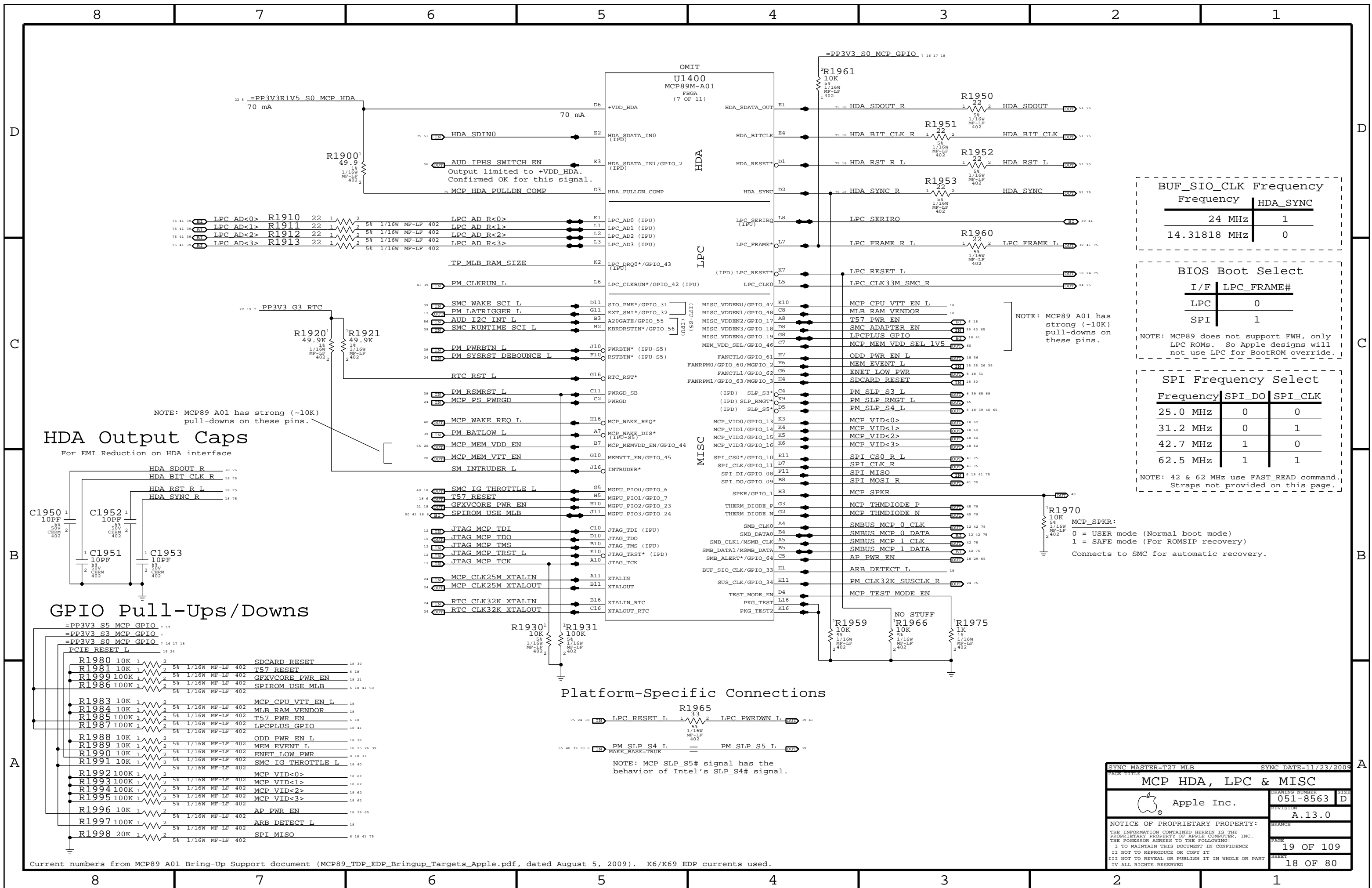
Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

PAGE TITLE		SYNC DATE=11/05/2009	
MCP Graphics			
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Internal MAC Disable:
 Connect RGMII_RXD<0:3> together to 10K pull-down.
 Connect RGMII_RXCLK to 10K pull-down.
 Connect RGMII_RXCTL to 10K pull-down.
 Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
 +3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMTG rail.
 RGMII_COMP_VDD/_GND must remain connected as shown.
 Connect RGMII_VREF to 10K pull-down.
 Connect RGMII_MDIO to 10K pull-down.
 All other pins can be left TP or NC.

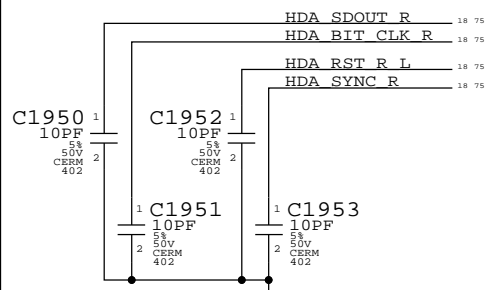
SYNC MASTER=T27 MLB		SYNC DATE=11/23/2009	
PAGE TITLE MCP SATA, USB & Ethernet			
Apple Inc.		DRAWING NUMBER 051-8563	SIZE D
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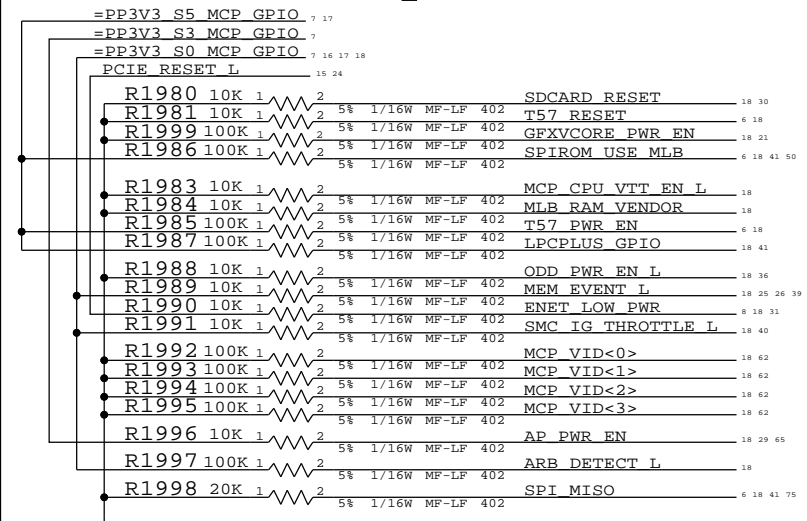
NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

HDA Output Caps

For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select	
I/F	LPC_FRAME#
LPC	0
SPI	1

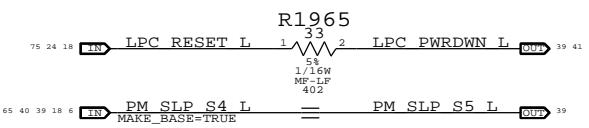
SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

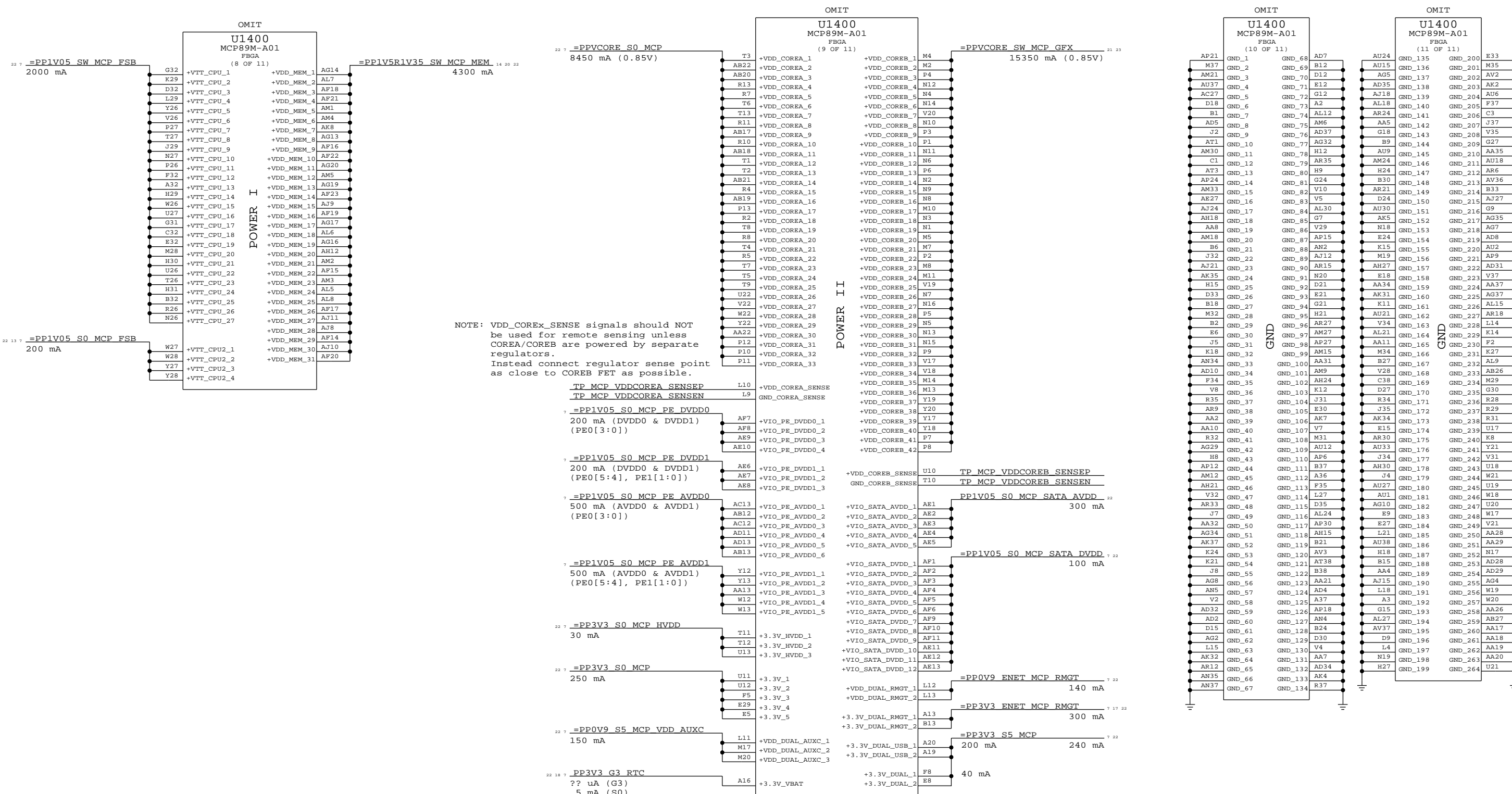
Platform-Specific Connections



NOTE: MCP_SLP_S5# signal has the behavior of Intel's SLP_S4# signal.

PAGE TITLE		SYNC DATE=11/23/2009	
MCP HDA, LPC & MISC		DRAWING NUMBER	051-8563
Apple Inc.		REVISION	A.13.0
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NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.



SYNC MASTER=T27 MLB SYNC DATE=08/06/2009

MCP Power & Ground

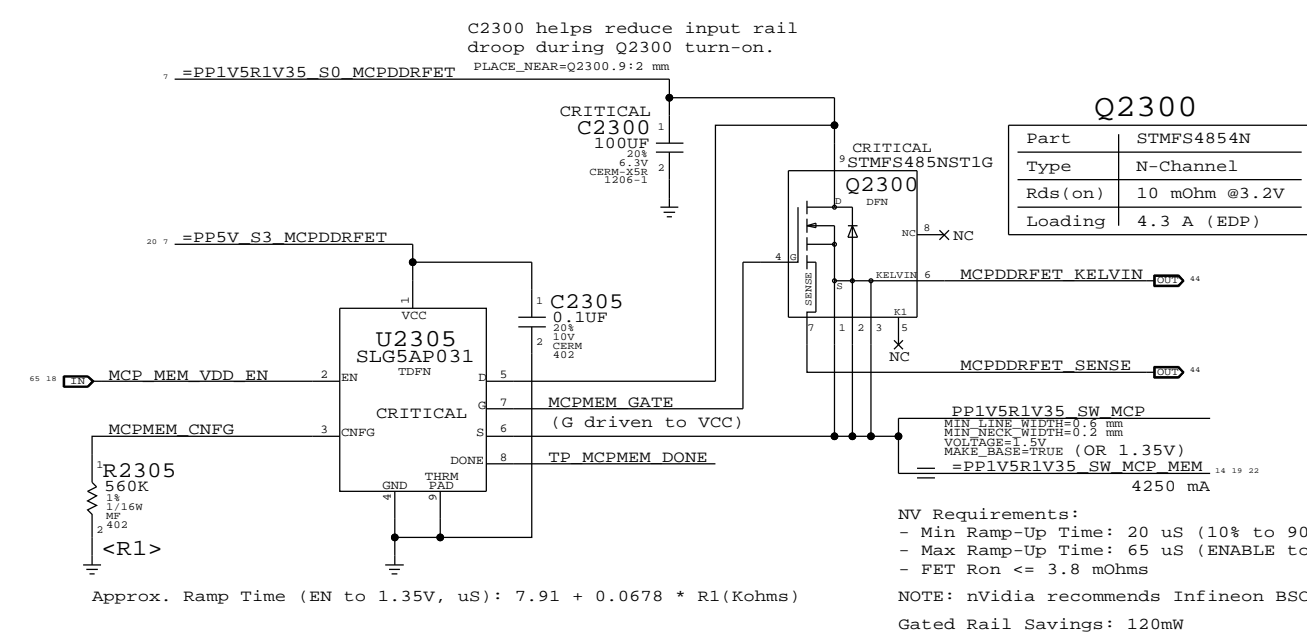
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DRAWING NUMBER 051-8563 SIZE D

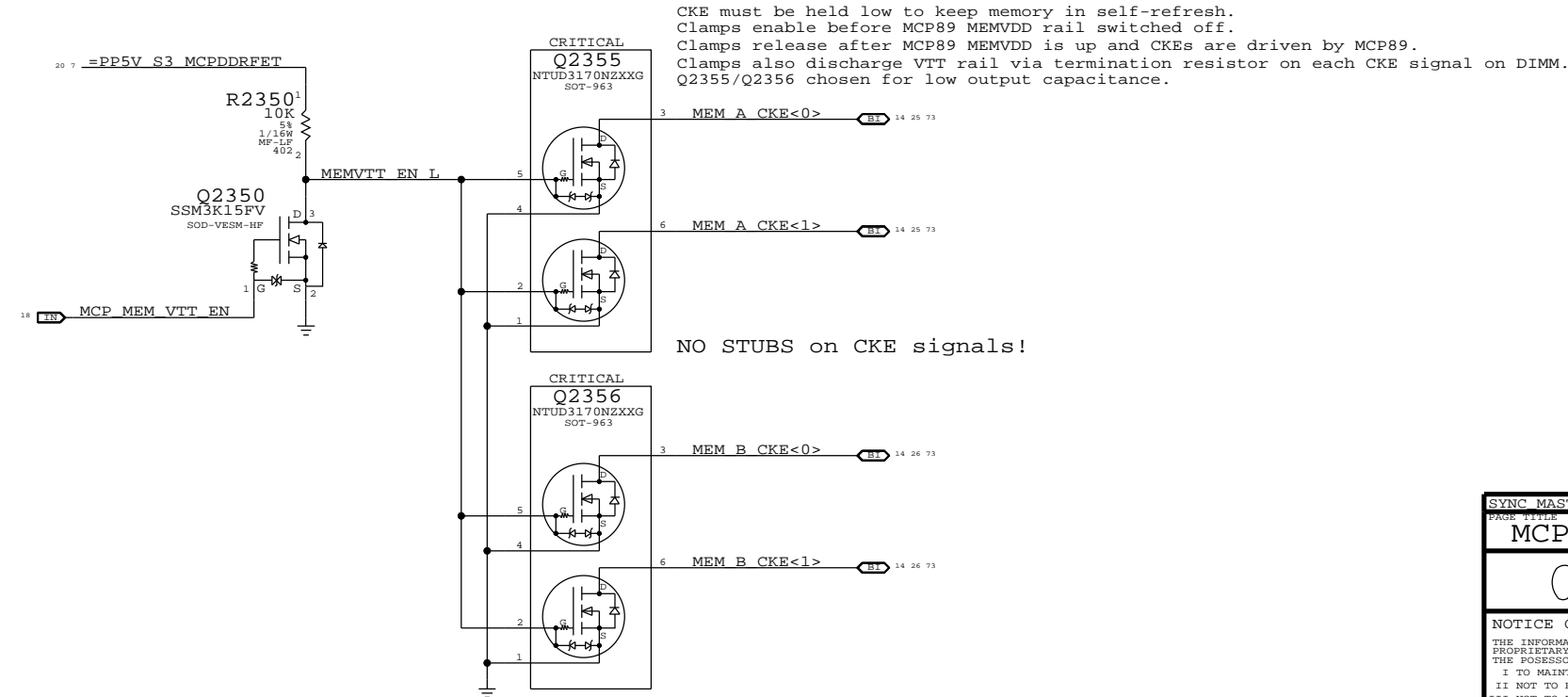
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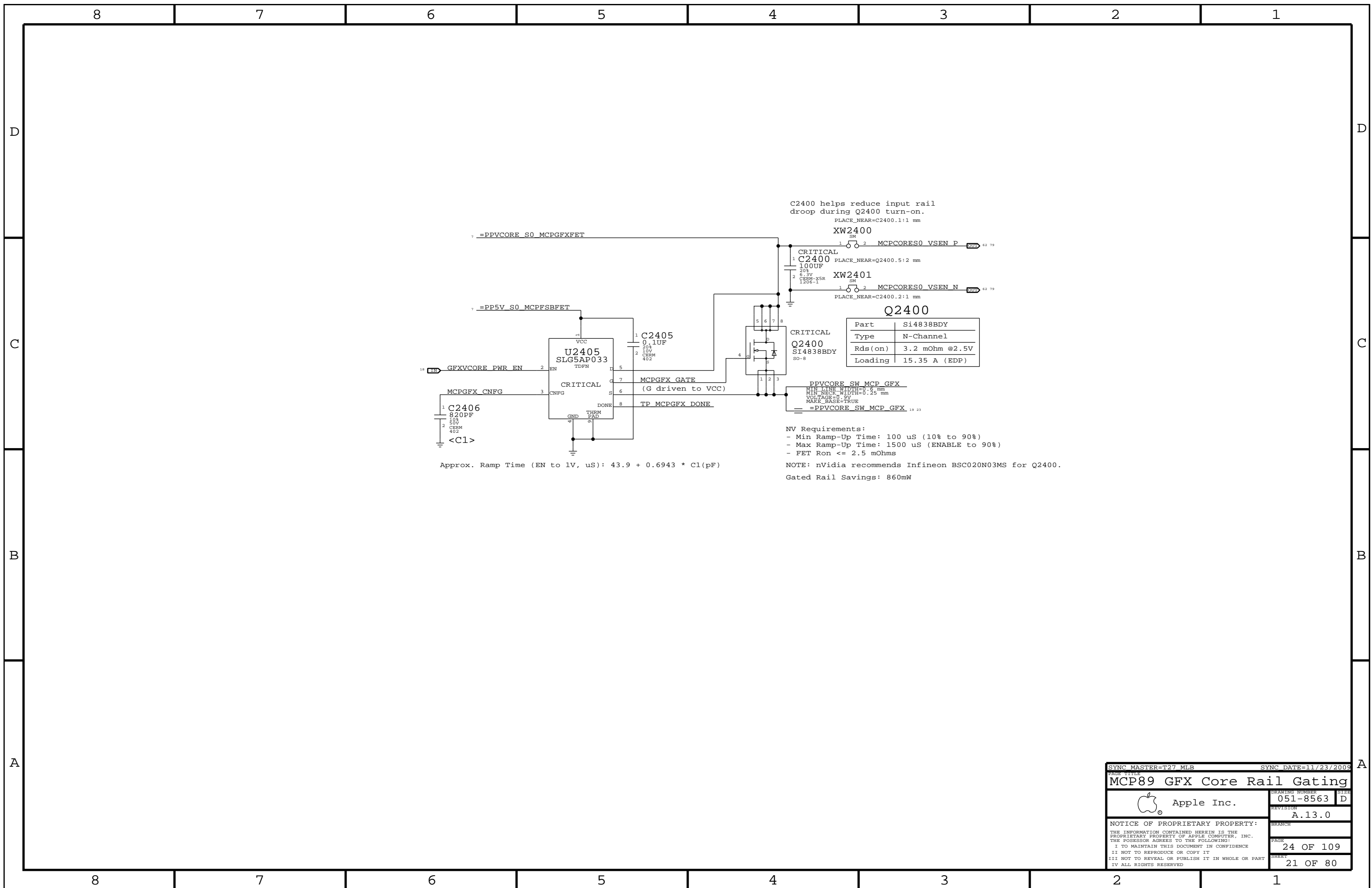
PAGE 20 OF 109 SHEET 19 OF 80



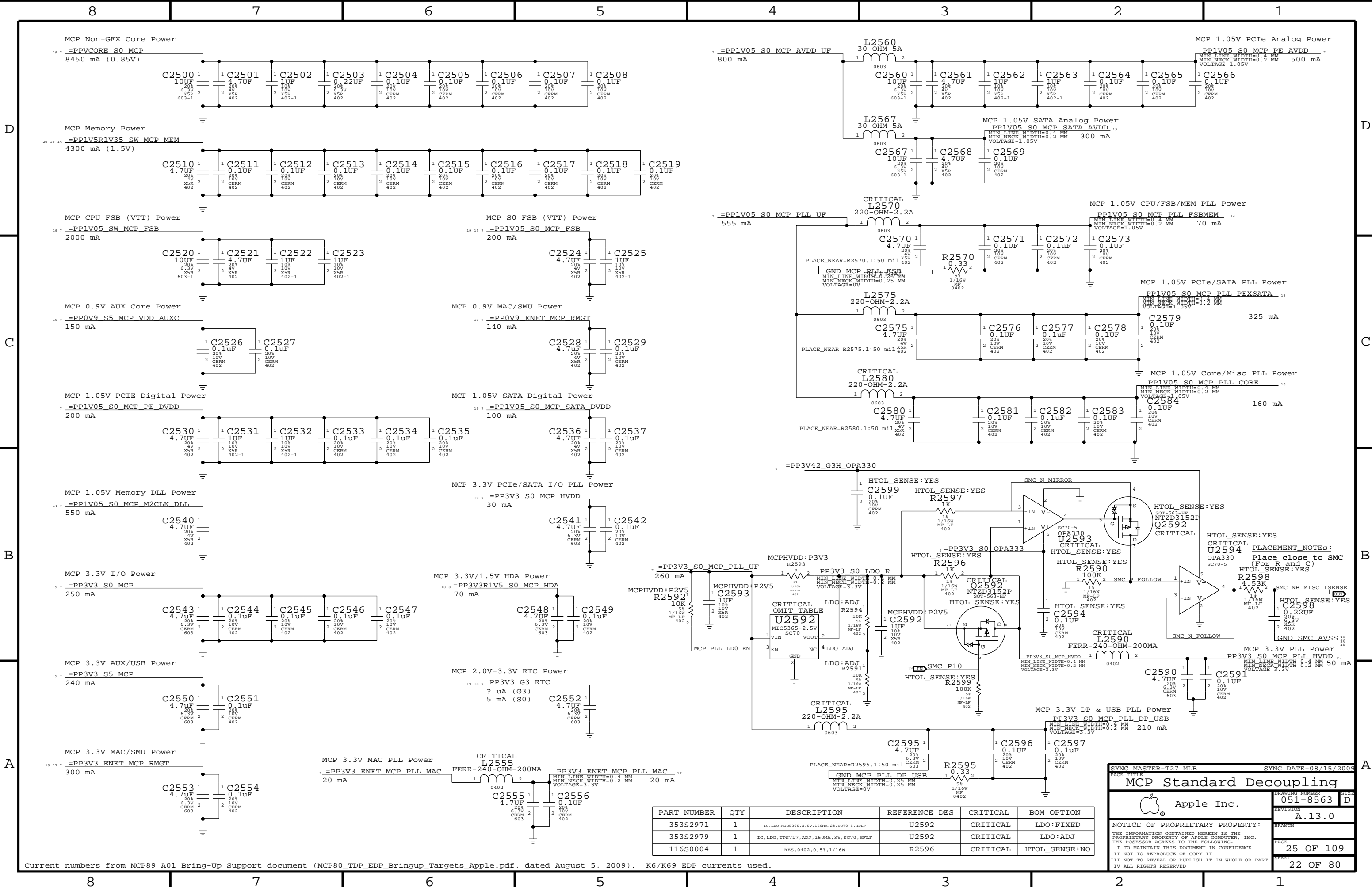
DIMM CKE Clamps



SYNC MASTER=T27 MLB		SYNC DATE=11/23/2009	
PAGE TITLE			
MCP89 Memory Rail Gating			
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SYNC MASTER=T27 MLB		SYNC DATE=11/23/2009	
PAGE TITLE MCP89 GFX Core Rail Gating			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2971	1	IC, LDO, MIC5365, 2.5V, 150mA, 2%, SC70-5, HPLF	U2592	CRITICAL	LDO:FIXED
353S2979	1	IC, LDO, TPS717, ADJ, 150mA, 3%, SC70, HPLF	U2592	CRITICAL	LDO:ADJ
116S0004	1	RES, 0402, 0.5%, 1/16W	R2596	CRITICAL	HTOL_SENSE:NO

SYNC MASTER=T27_MLB SYNC DATE=08/15/2009

MCP Standard Decoupling

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

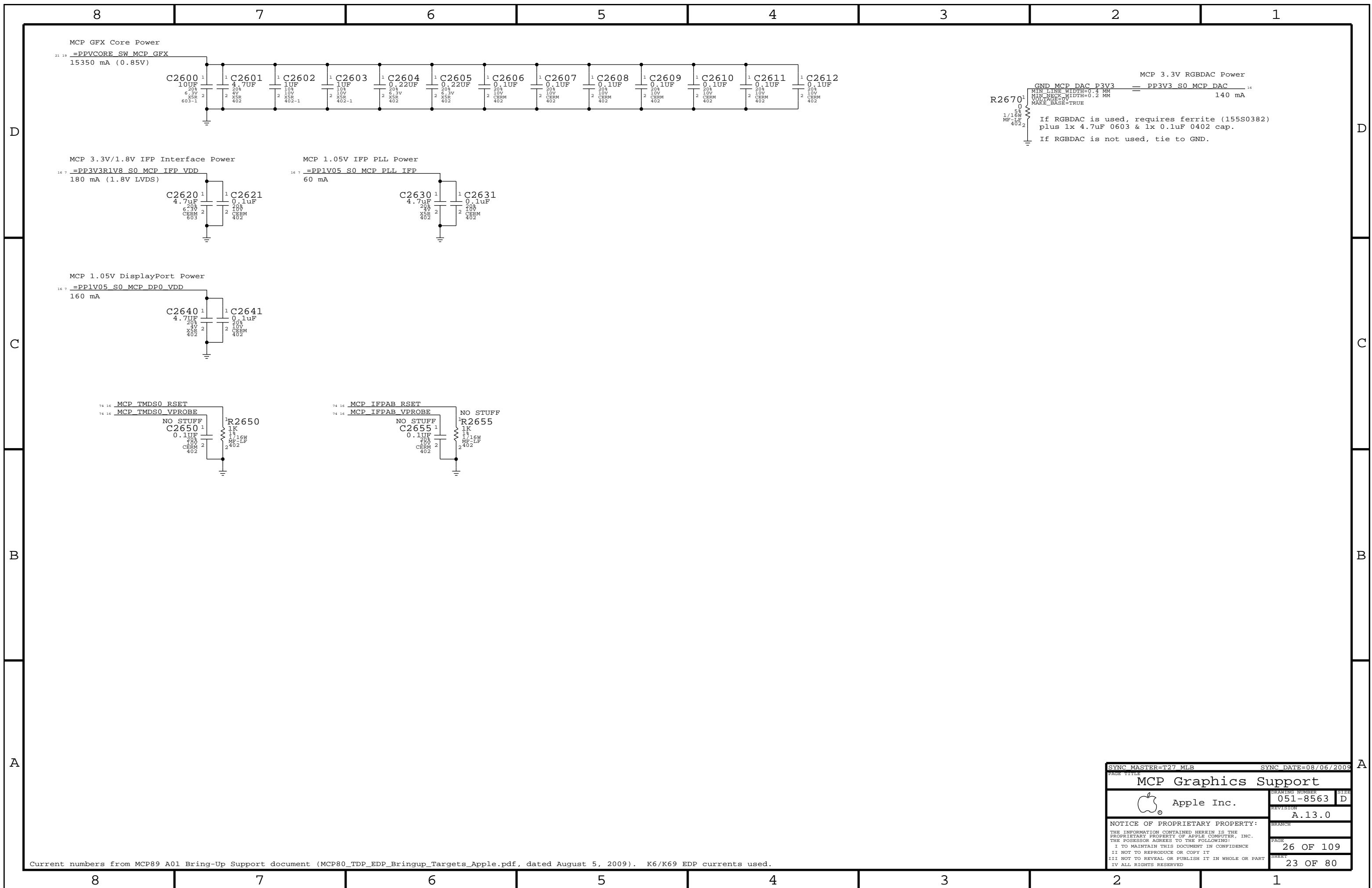
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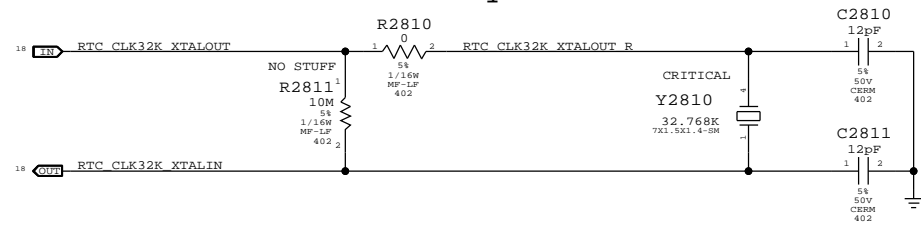
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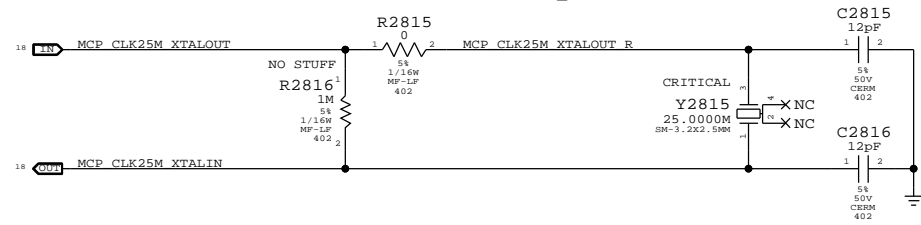
Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27_MLB		SYNC DATE=08/06/2009	
MCP Graphics Support			
	DRAWING NUMBER	051-8563	SIZE
	REVISION	A.13.0	
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		SHEET	23 OF 80

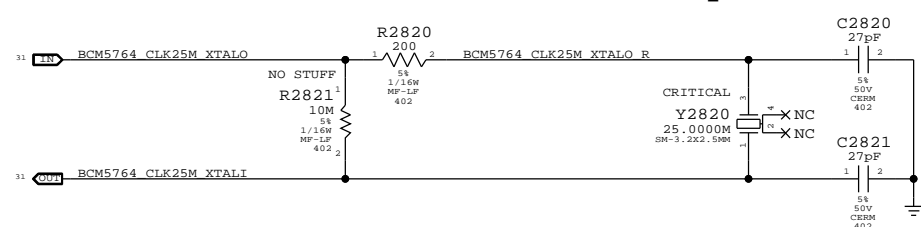
RTC Crystal



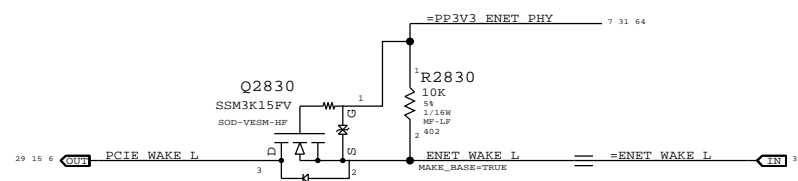
MCP 25MHz Crystal



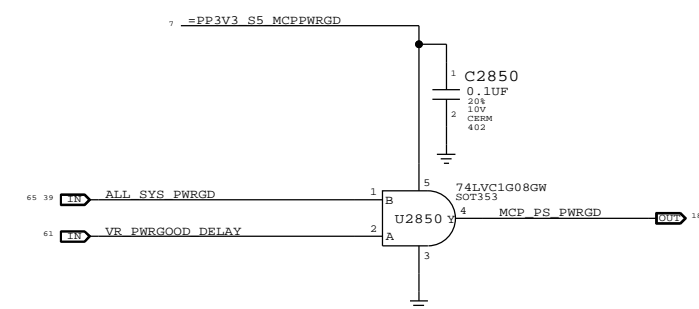
Caesar II (ENET) 25MHz Crystal



Ethernet WAKE# Isolation

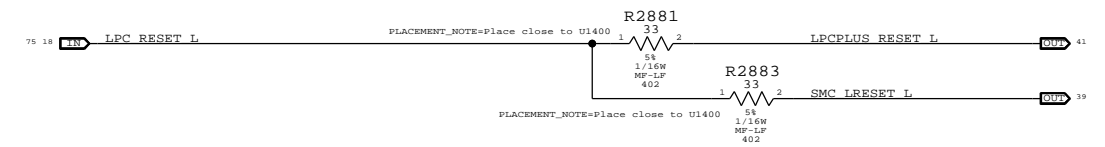


MCP S0 PWRGD & CPU_VLD

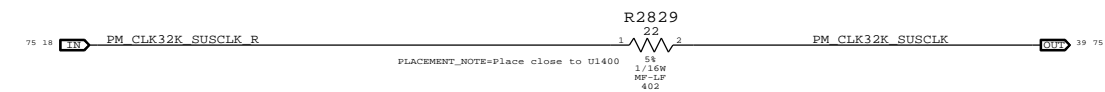
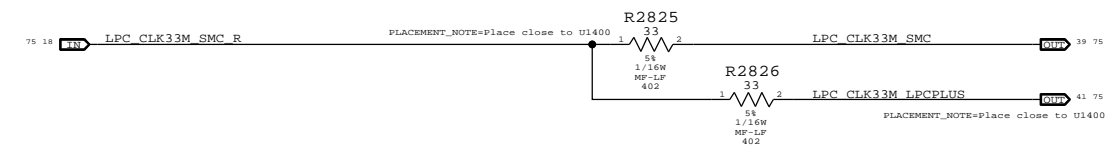
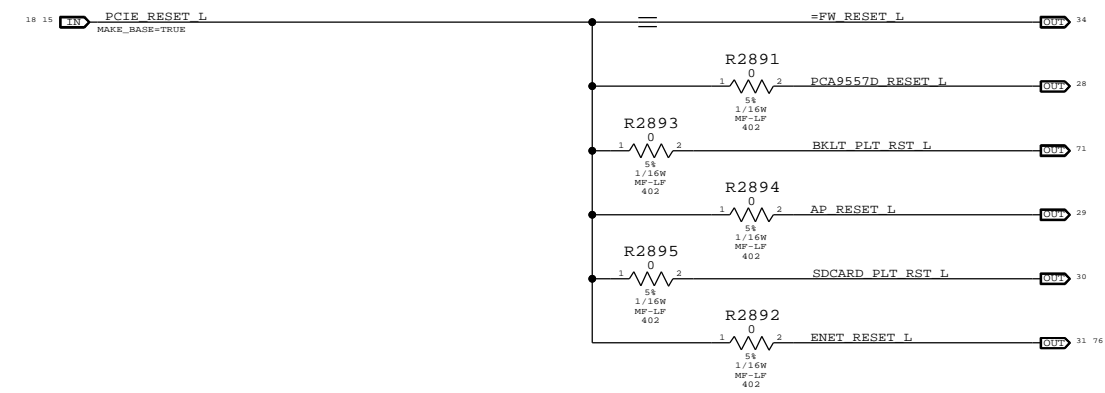


Platform Reset Connections

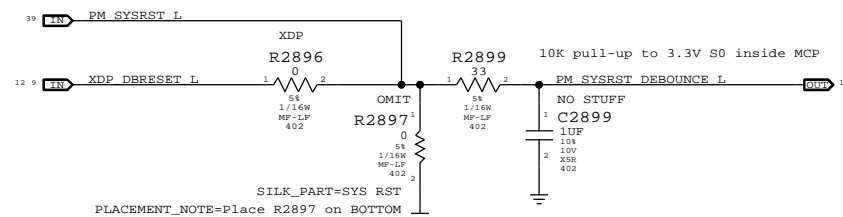
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



System Reset Circuit



SYNC MASTER=T27_MLB		SYNC DATE=07/28/2009	
PAGE TITLE			
SB Misc		DRAWING NUMBER	SIZE
Apple Inc.		051-8563	D
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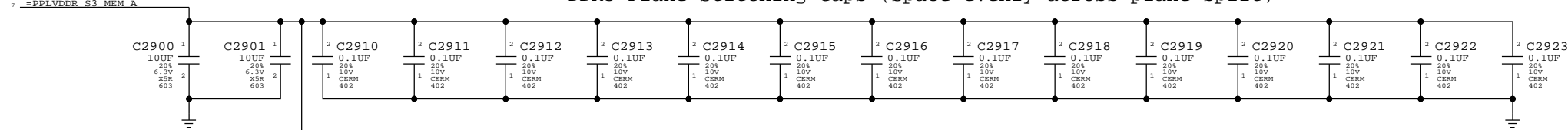
Page Notes

Power aliases required by this page:
 - =PPLVDDR_S3_MEM_A
 - =PPDDRVTT_S0_MEM_A
 - =PPSPD_S0_MEM_A (2.5 - 3.3V)

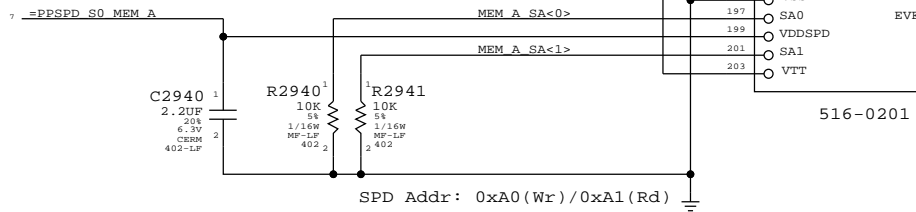
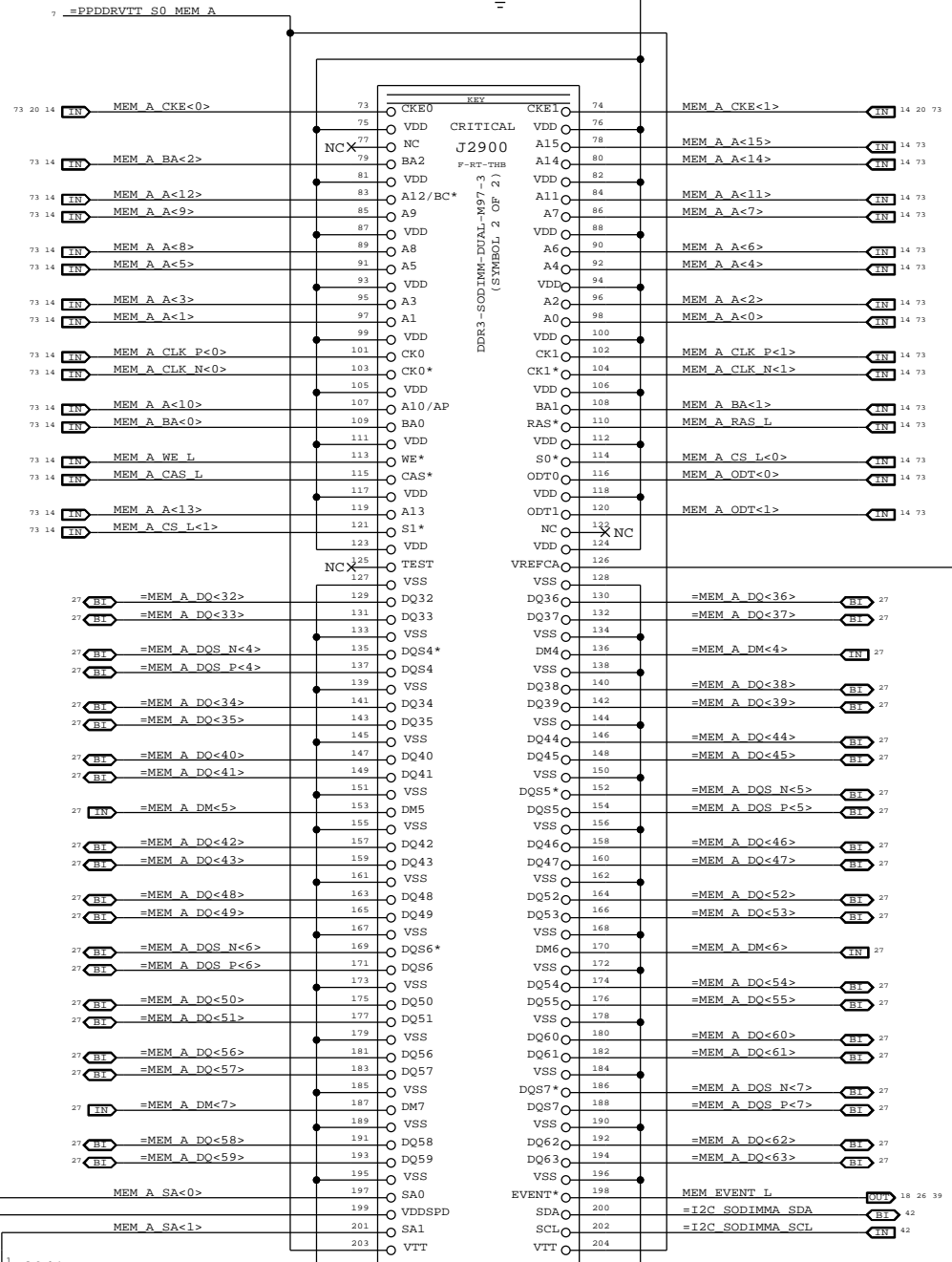
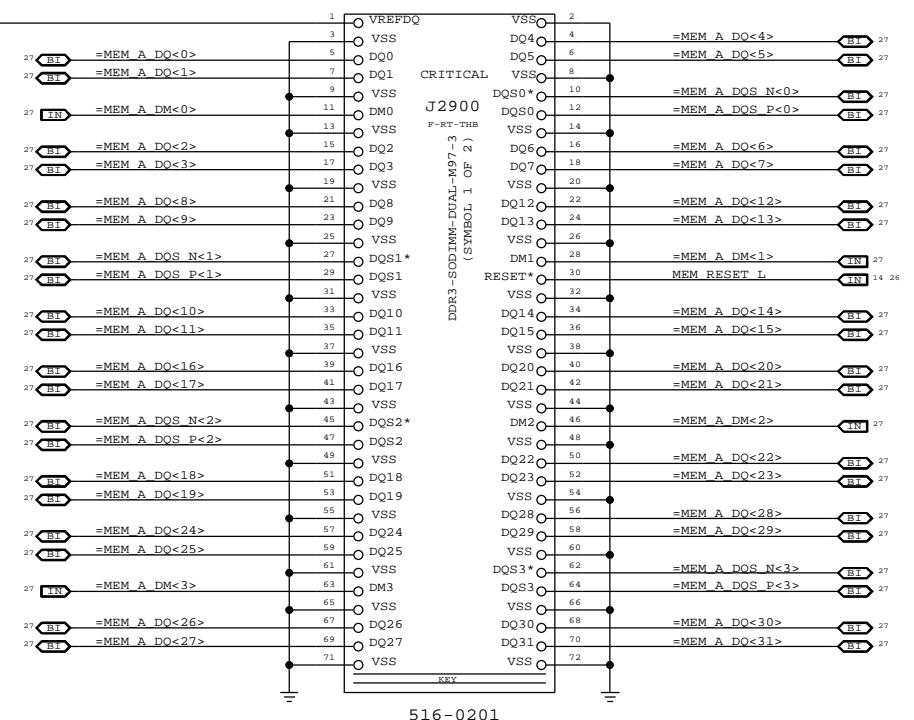
Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

DDR3 Plane Stitching Caps (Space evenly across plane split)



"Factory" (top) slot



SYNC MASTER=T27_MLB		SYNC DATE=07/28/2009	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
Apple Inc.		DRAWING NUMBER	SIZE
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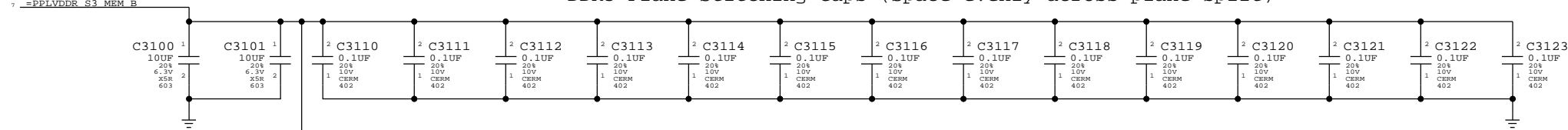
Page Notes

Power aliases required by this page:
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 - =PPDDRVTT_S0_MEM_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)

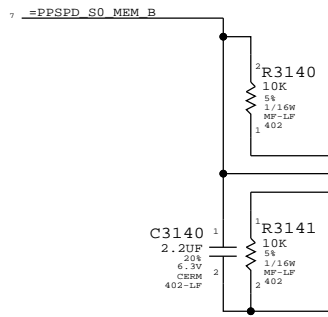
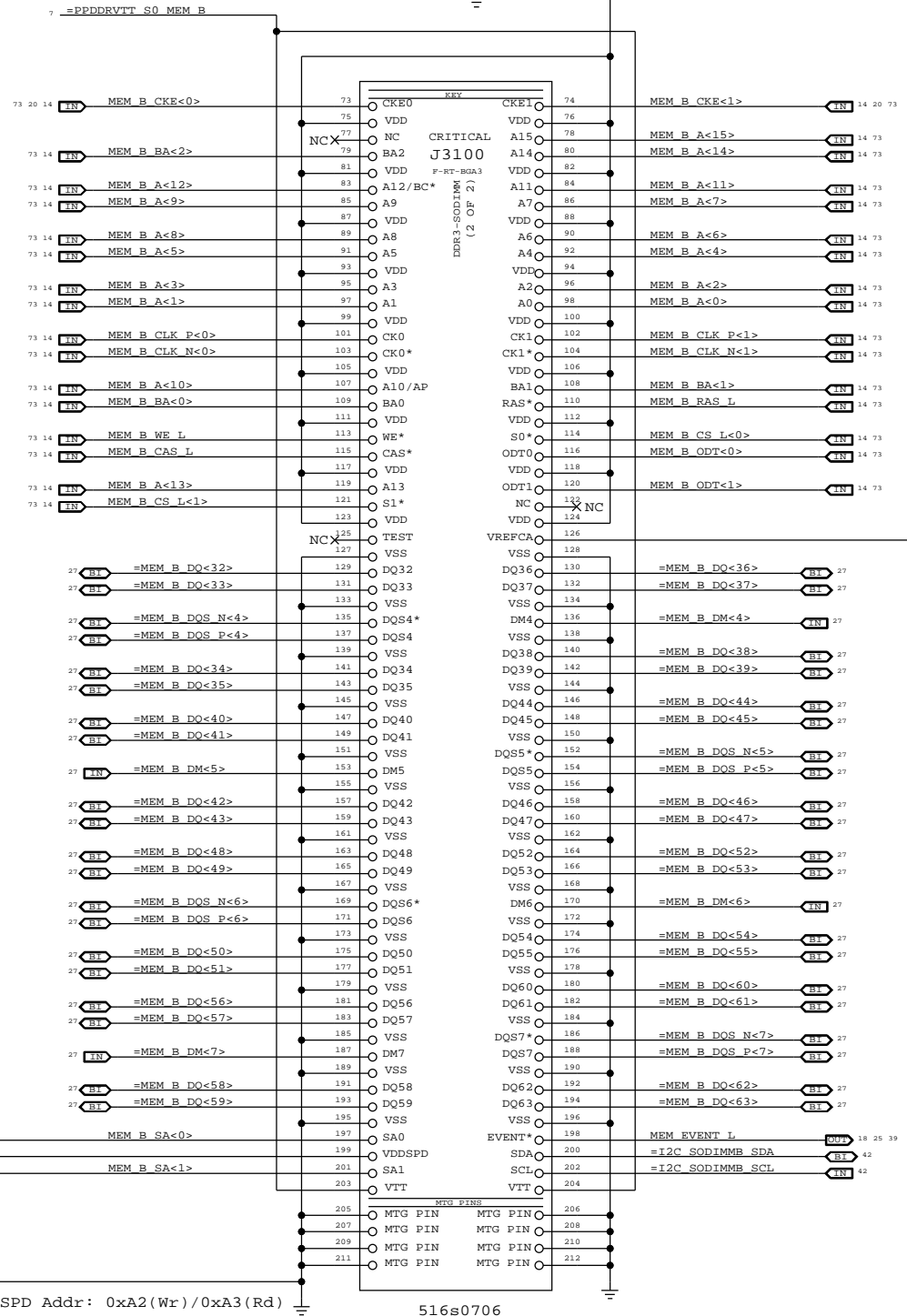
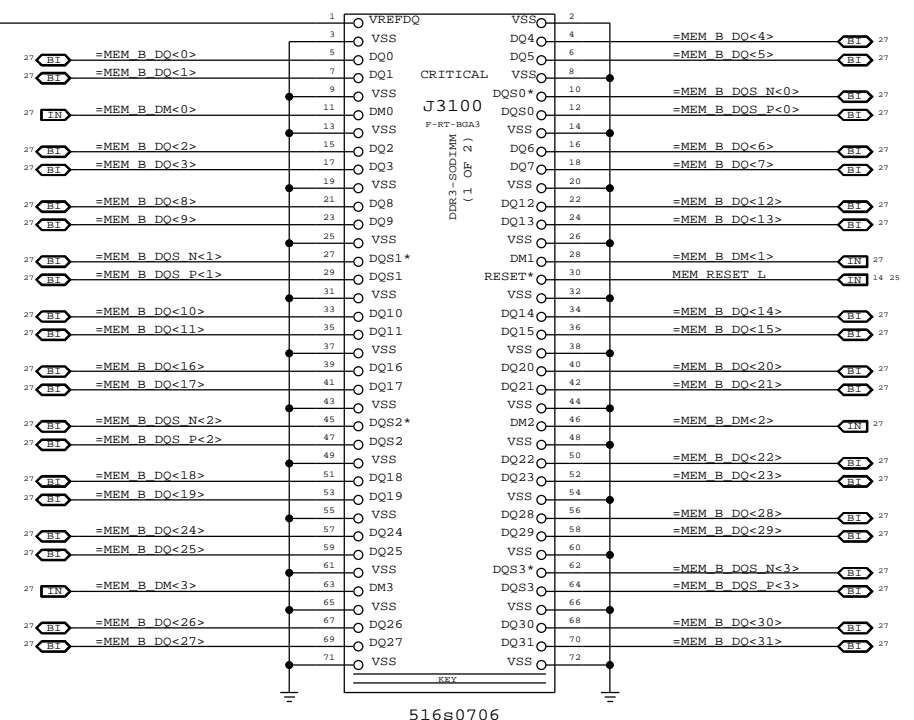
Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

BOM options provided by this page:
 (NONE)

DDR3 Plane Stitching Caps (Space evenly across plane split)



"Expansion" (bottom) slot



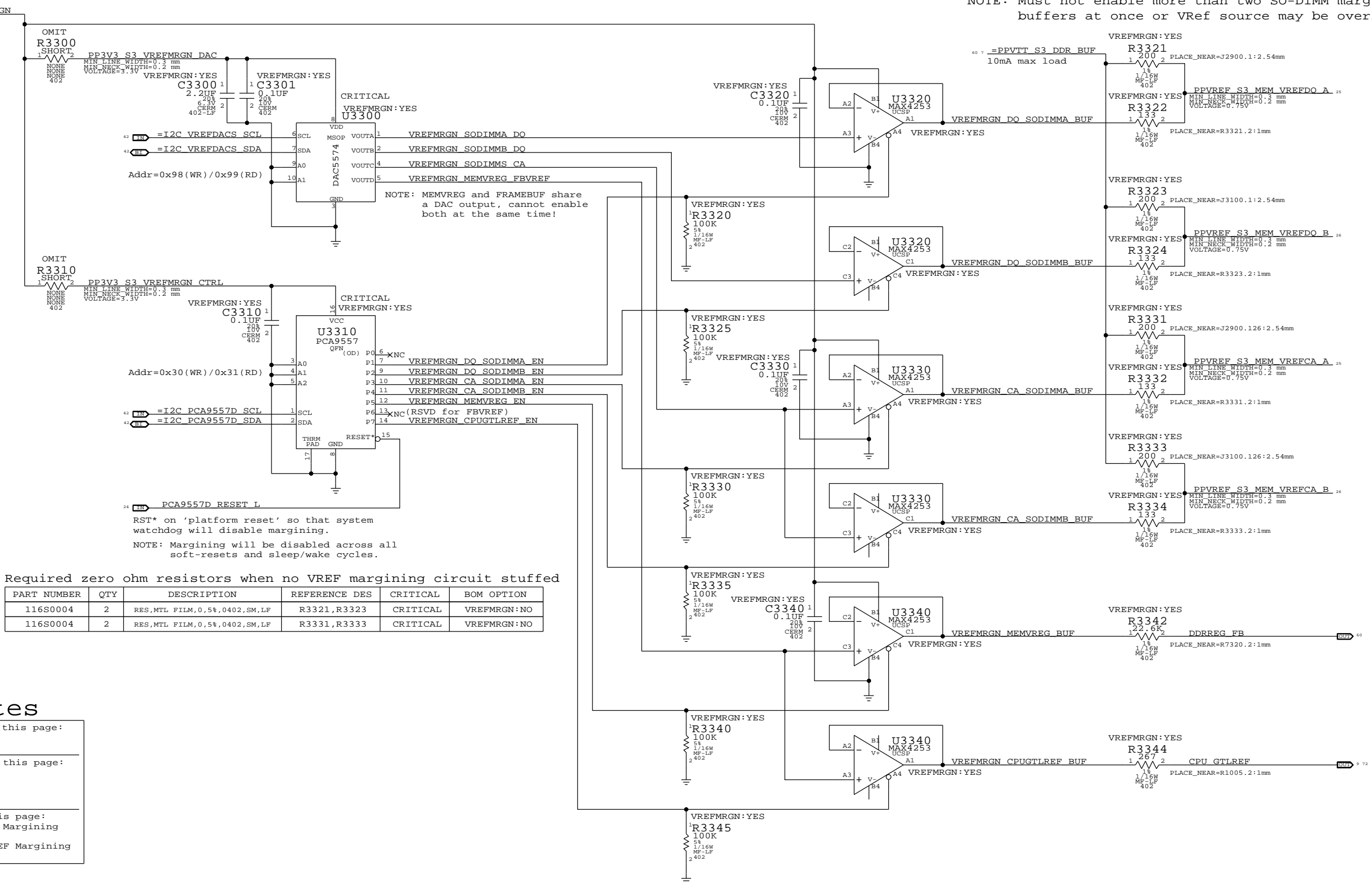
SPD Addr: 0xA2 (Wr) / 0xA3 (Rd) 516s0706

SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
PAGE TITLE			
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Apple Inc.		051-8563	D
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SYNC MASTER=K18_MLB		SYNC DATE=06/19/2009	
PAGE TITLE			
DDR3 BYTE/BIT SWAPS-K6			
DRAWING NUMBER		SIZE	
051-8563		D	
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PAGE		SHEET	
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

RST* on 'platform reset' so that system watchdog will disable margining.
NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES, MTL FILM, 0, 5%, 0402, SM, LF	R3321, R3323	CRITICAL	VREFMRGN: NO
116S0004	2	RES, MTL FILM, 0, 5%, 0402, SM, LF	R3331, R3333	CRITICAL	VREFMRGN: NO

Page Notes

Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN: YES - Stuffs VREF Margining Circuitry.
 VREFMRGN: NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=T27_MLB SYNC DATE=09/29/2009

FSB/DDR3 Vref Margining

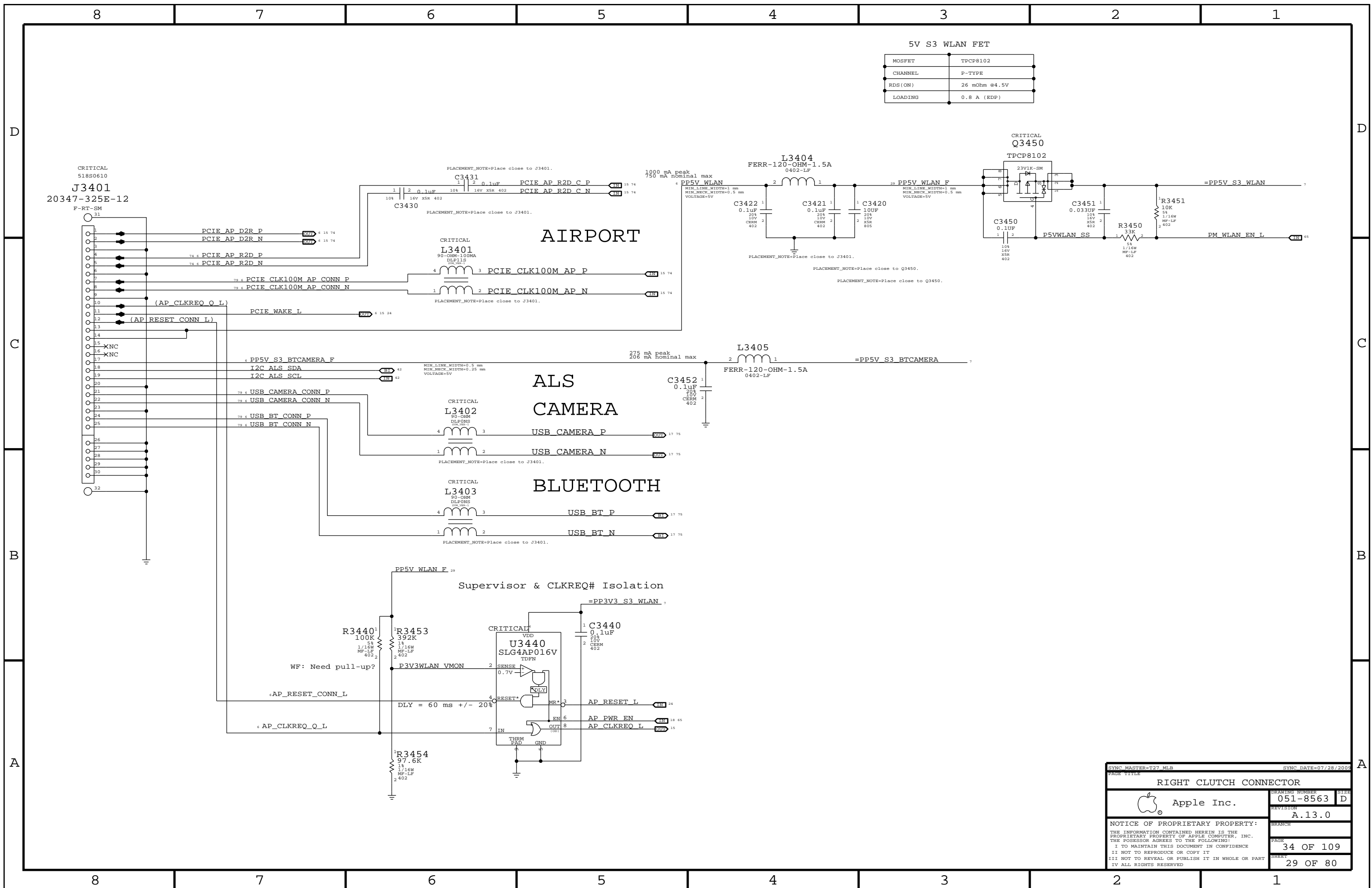
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DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

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PAGE: 33 OF 109 SHEET: 28 OF 80



5V S3 WLAN FET	
MOSFET	TFCP8102
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

CRITICAL
Q3450

TFCP8102

23V1K-SM

C3450

0.1uF

10V

10V

10V

10V

10V

10V

10V

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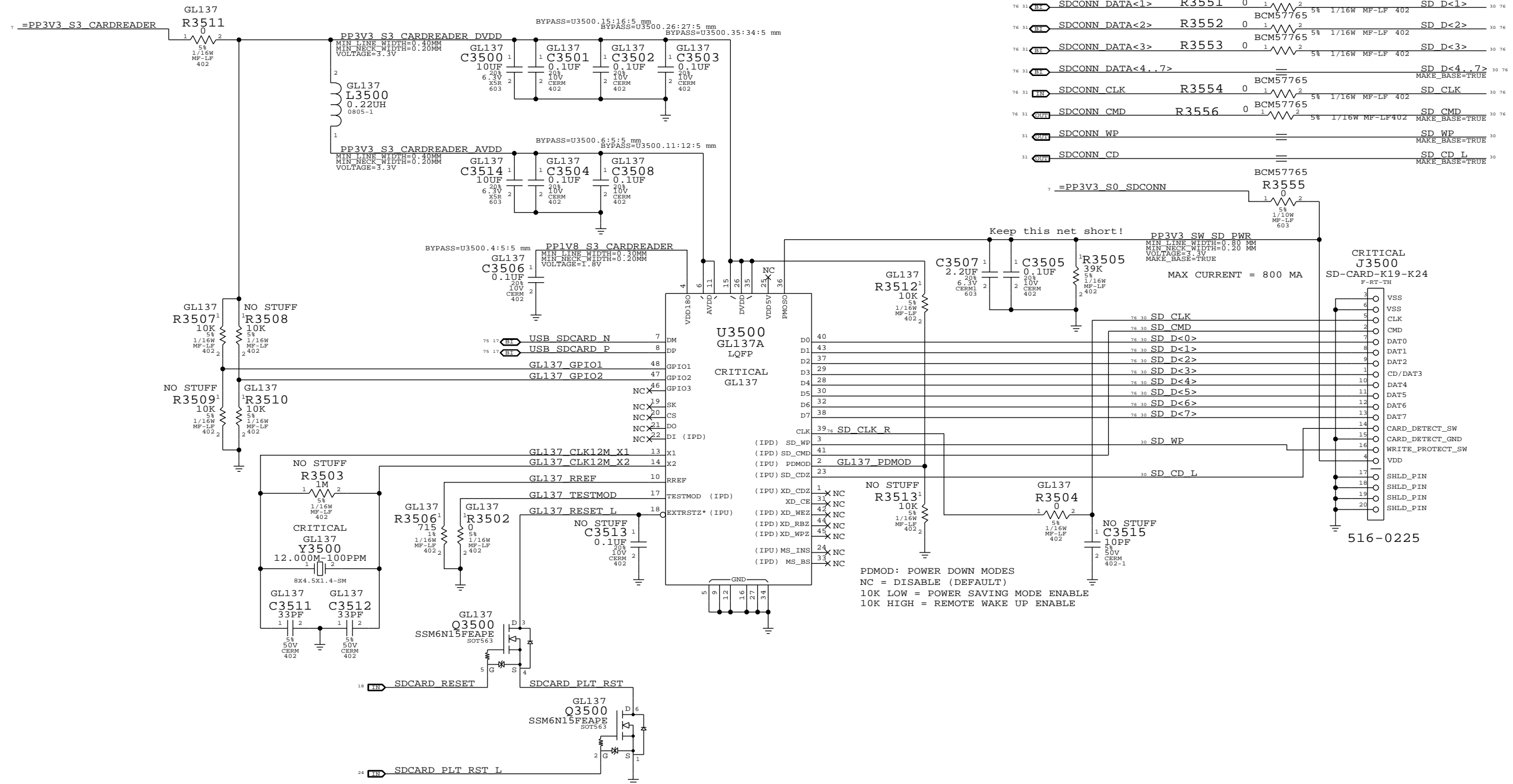
10V

10V

10V

SYNC MASTER=T27_MLB		SYNC DATE=07/28/2009	
PAGE TITLE			
RIGHT CLUTCH CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8563	D
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Caesar IV Support



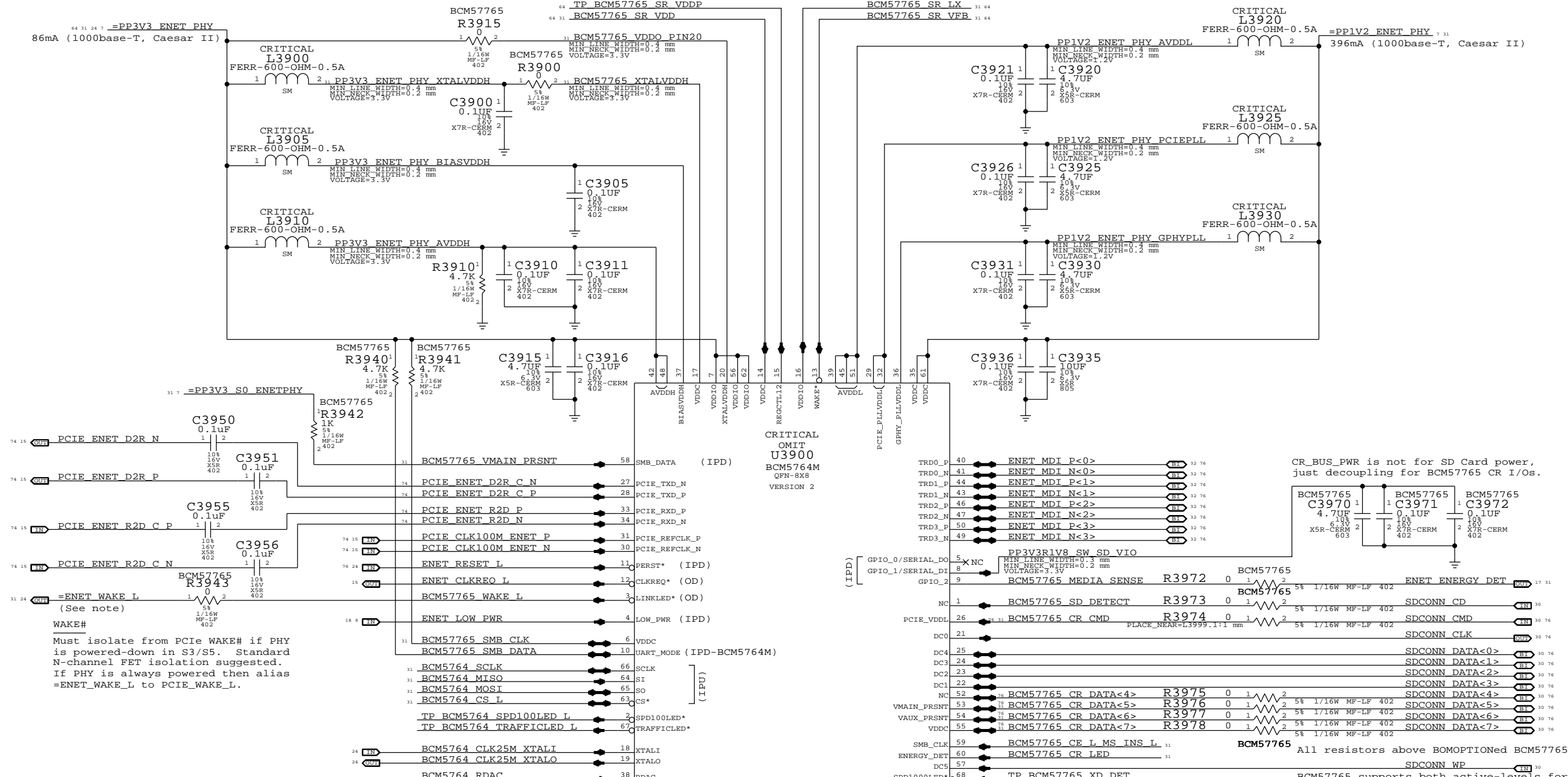
Signal	Resistor	Value	Component	Notes
SDCONN DATA<0>	R3550	0	BCM57765	SD D<0>
SDCONN DATA<1>	R3551	0	BCM57765	SD D<1>
SDCONN DATA<2>	R3552	0	BCM57765	SD D<2>
SDCONN DATA<3>	R3553	0	BCM57765	SD D<3>
SDCONN DATA<4..7>				SD D<4..7> MAKE_BASE=TRUE
SDCONN CLK	R3554	0	BCM57765	SD CLK
SDCONN CMD	R3556	0	BCM57765	SD CMD MAKE_BASE=TRUE
SDCONN WP				SD WP MAKE_BASE=TRUE
SDCONN CD				SD CD L MAKE_BASE=TRUE

PDMOD: POWER DOWN MODES
 NC = DISABLE (DEFAULT)
 10K LOW = POWER SAVING MODE ENABLE
 10K HIGH = REMOTE WAKE UP ENABLE

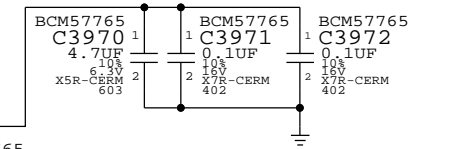
ADDED SERIES RESISTOR TO SD_CMD, MAX CURRENT NUMBER CHANGED TO 800MA

SYNC MASTER=T27 MLB		SYNC DATE=09/30/2009	
SecureDigital Card Reader			
Apple Inc.		DRAWING NUMBER	051-8563
		REVISION	A.13.0
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		PAGE	35 OF 109
		SHEET	30 OF 80

BCM57765 SR pins are internal 1.2V switching regulator.
 If unused: Okay to float all 4 pins. (Broadcom not so sure now)
 If used: VDD/VDDP connect to =PP3V3_ENET_PHY (add bypassing), LX connects to inductor, VFB to =PP1V2_ENET_PHY

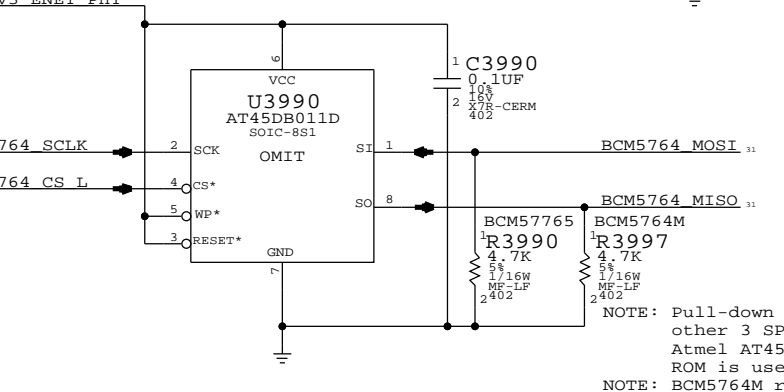


CR_BUS_PWR is not for SD Card power, just decoupling for BCM57765 CR I/Os.



BCM57765 All resistors above BOMOPTIONed BCM57765
 SDCONN WP

PHY Non-Volatile Memory
 ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)



NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
 NOTE: BCM5764M requires SI pull-down instead of SO.

BCM5764M Support

60-ENERGY_DET 31 BCM57765 CR LED R3980 0 1 2 5% 1/16W MF-LF 402 ENET ENERGY DET 17 31

13-WAKE* 64 31 BCM57765 SR VFB R3981 0 1 2 5% 1/16W MF-LF 402 =ENET_WAKE_L (See note) 24 31

53-VMAIN_PRSENT 76 31 BCM57765 CR DATA<5> R3982 1K 1 2 5% 1/16W MF-LF 402 =PP3V3_S0_ENETPHY 7 31

59-SMB_CLK 31 BCM57765 CE L MS INS L R3983 4.7K 1 2 5% 1/16W MF-LF 402 =PP3V3_ENET_PHY 7 24 31 64

58-SMB_DATA 31 BCM57765 VMMAIN_PRSENT R3984 4.7K 1 2 5% 1/16W MF-LF 402 =PP3V3_ENET_PHY 7 24 31 64

54-VAUX_PRSENT 76 31 BCM57765 CR DATA<6> R3985 1K 1 2 5% 1/16W MF-LF 402

16-VDDIO 64 31 BCM57765 SR LX R3986 0 1 2 5% 1/16W MF-LF 402

20-XTALVDDH 31 BCM57765 VDDO_PIN20 R3987 0 1 2 5% 1/16W MF-LF 402 PP3V3_ENET_PHY_XTALVDDH 31

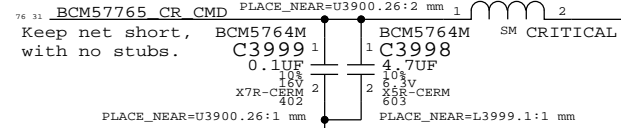
55-VDDC 76 31 BCM57765 CR DATA<7> R3988 0 1 2 5% 1/16W MF-LF 402 =PP1V2_ENET_PHY 7 31

17-VDDC 76 31 BCM57765 XTALVDDH R3989 0 1 2 5% 1/16W MF-LF 402

14-VDDC 64 31 BCM57765 SR VDD R3990 0 1 2 5% 1/16W MF-LF 402

06-VDDC 31 BCM57765 SMB_CLK R3999 0 1 2 5% 1/16W MF-LF 402

26-PCIE_VDDL 76 31 BCM57765 CR_CMD PLACE_NEAR=U3900.26:2 mm 1 2



SYNC MASTER=T27 MLB SYNC DATE=08/20/2009

Ethernet PHY (Caesar II/IV)

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

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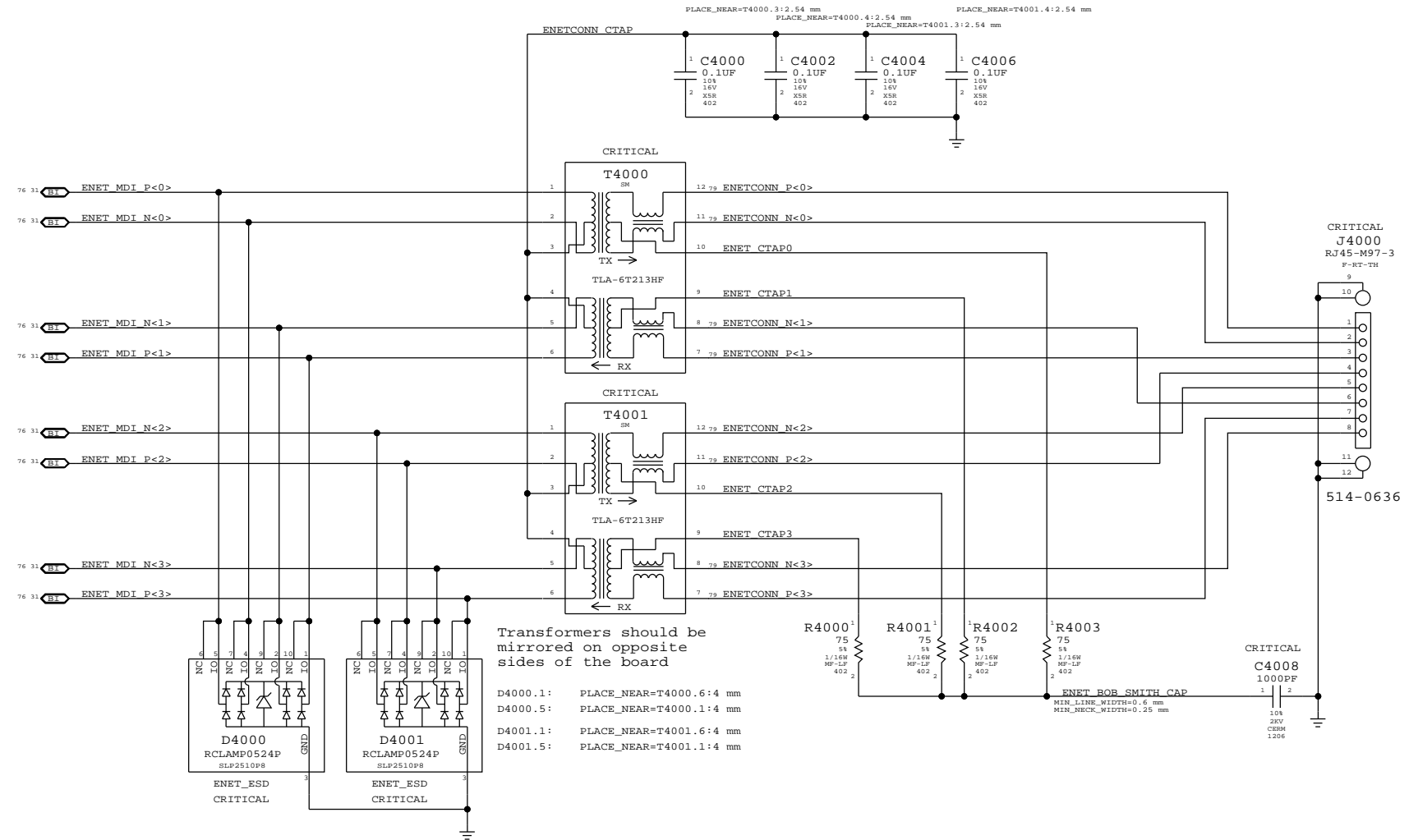
PAGE: 39 OF 109 SHEET: 31 OF 80

Page Notes

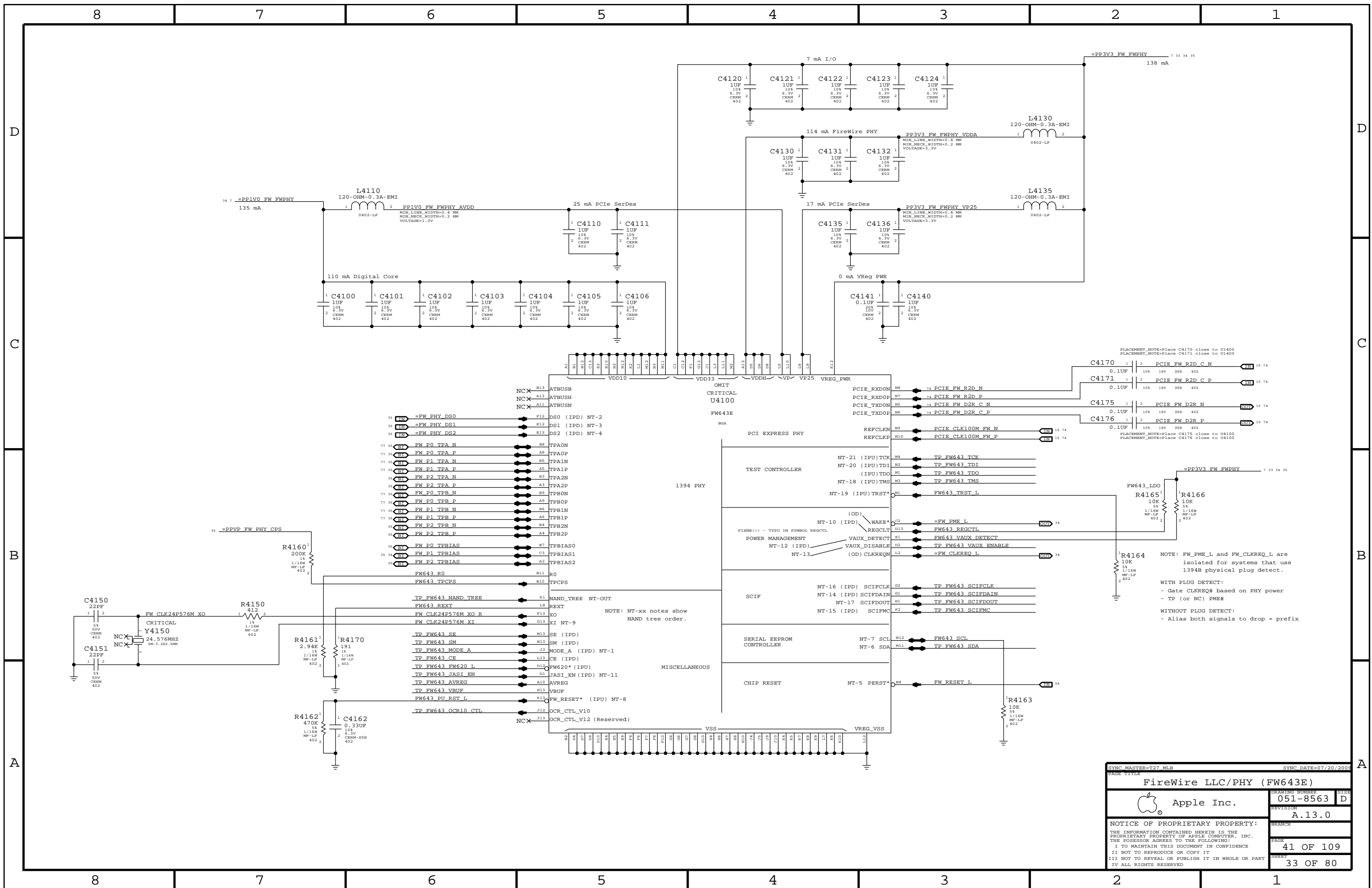
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
PAGE TITLE: Ethernet Connector			
DRAWING NUMBER: 051-8563		SIZE: D	
REVISION: A.13.0		BRANCH:	
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PAGE: 40 OF 109		SHEET: 32 OF 80	



PLACEMENT_NOTE=Place C4170 close to U1400
 PLACEMENT_NOTE=Place C4171 close to U1400

PLACEMENT_NOTE=Place C4175 close to U4100
 PLACEMENT_NOTE=Place C4176 close to U4100

NOTE: FW_PME_L and FW_CLKREQ_L are isolated for systems that use 1394B physical plug detect.

WITH PLUG DETECT:
 - Gate CLKREQ# based on PHY power
 - TP (or NC) PME#

WITHOUT PLUG DETECT:
 - Alias both signals to drop = prefix

NOTE: FW_PME_L and FW_CLKREQ_L are isolated for systems that use 1394B physical plug detect.

WITH PLUG DETECT:
 - Gate CLKREQ# based on PHY power
 - TP (or NC) PME#

WITHOUT PLUG DETECT:
 - Alias both signals to drop = prefix

SYNC MASTER=T27_MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
FireWire LLC/PHY (FW643E)		DRAWING NUMBER	SIZE
Apple Inc.		051-8563	D
		REVISION	
		A.13.0	
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		PAGE	
		41 OF 109	
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		33 OF 80	

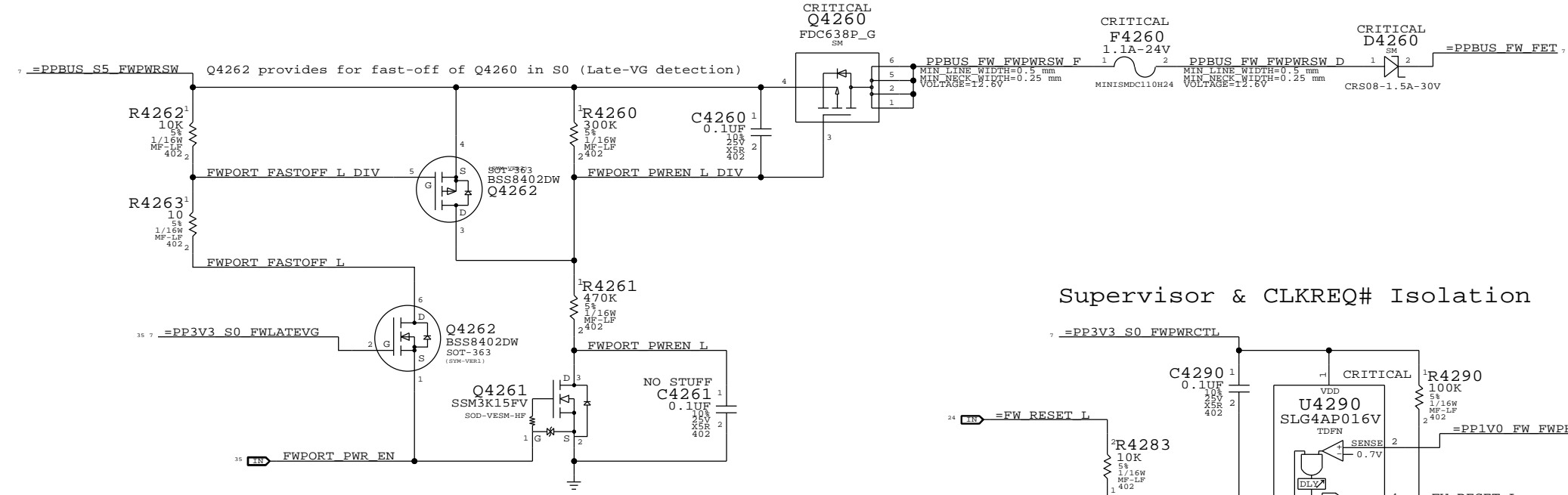
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWRSW (FW VP FET Input)
 - =PPBUS_FW_FET (FW VP FET Output)
 - =PP3V3_FW_P3V3FWFET (3.3V FET Input)
 - =PP3V3_FW_FET (3.3V FET Output)
 - =PP3V3_FW_FWPHY (PHY 3.3V Power)
 - =PP3V3_S0_FWLATEVG
 - =PP3V3_S0_FWPWRCTL
 - =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
 - =PP1V05_FW_P1V0FWFET (1.0V FET Input)
 - =PP1V0_FW_FET_R (1.0V FET Output)
 - =PP1V0_FW_FWPHY (PHY 1.0V)

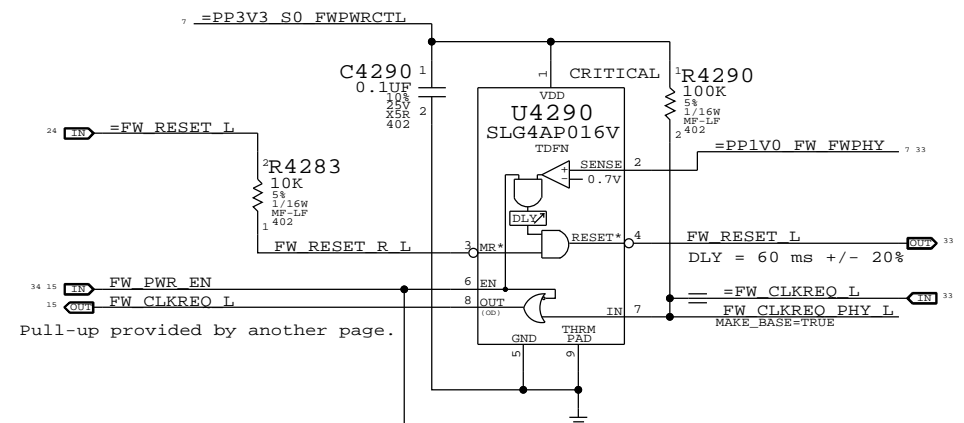
Signal aliases required by this page:
 - =FW_CLKREQ_L
 - =FW_PME_L

BOM options provided by this page:
 (NONE)

FireWire Port Power Switch

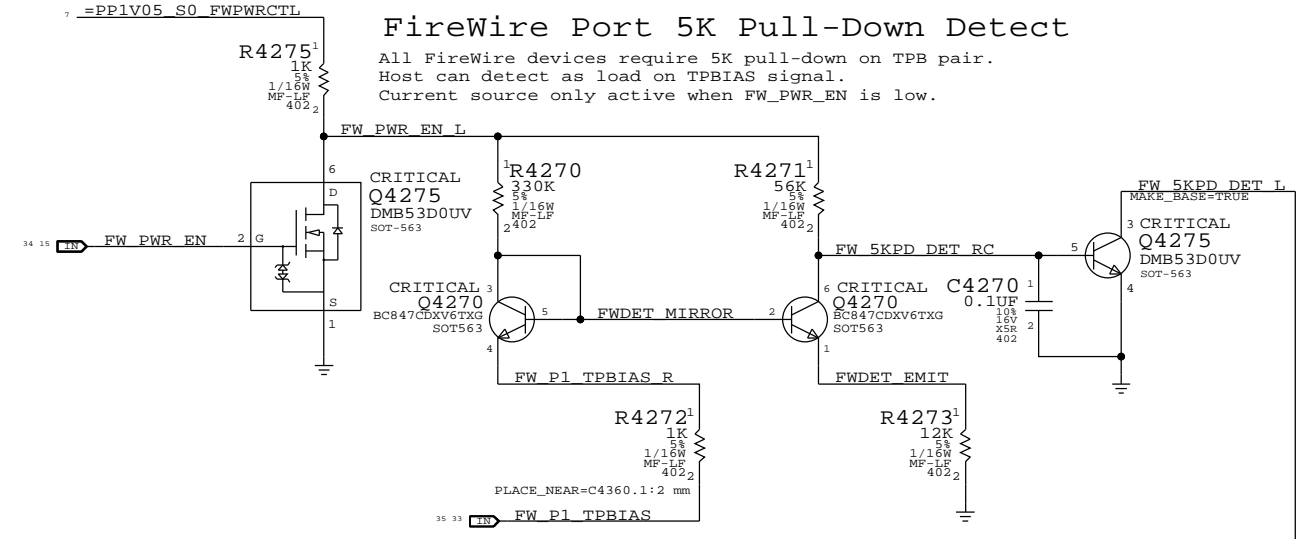


Supervisor & CLKREQ# Isolation



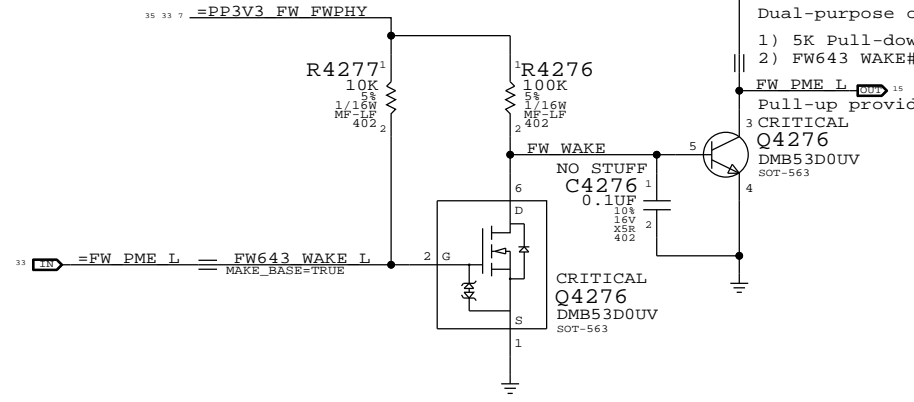
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair. Host can detect as load on TPBIAS signal. Current source only active when FW_PWR_EN is low.



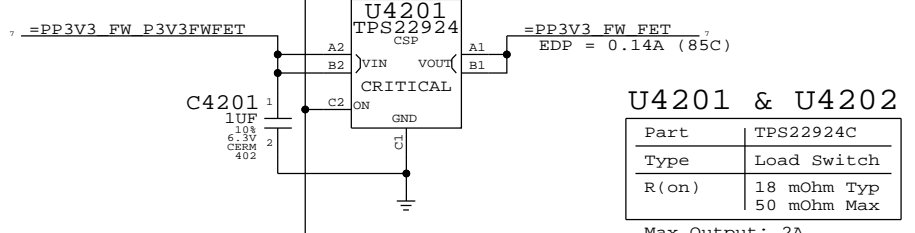
FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



Dual-purpose output:
 1) 5K Pull-down Detect when FW_PWR_EN is low.
 2) FW643 WAKE# (PME#) when PHY is powered.
 Pull-up provided on another page.

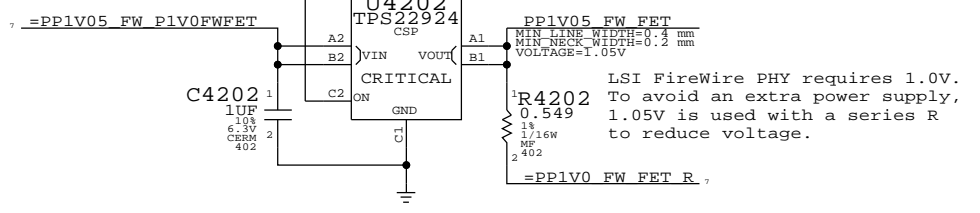
3.3V FW Switch



Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



PAGE TITLE		SYNC DATE=12/15/2009	
FireWire Port & PHY Power		DRAWING NUMBER	051-8563
Apple Inc.		REVISION	A.13.0
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TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT1
 - =PPVP_FW_PHY_CPS_FET (From Port)
 - =PPVP_FW_PHY_CPS (To PHY)
 - =PP3V3_FW_FWPHY
 - =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
 - =FW_PHY_DS0
 - =FW_PHY_DS1
 - =FW_PHY_DS2

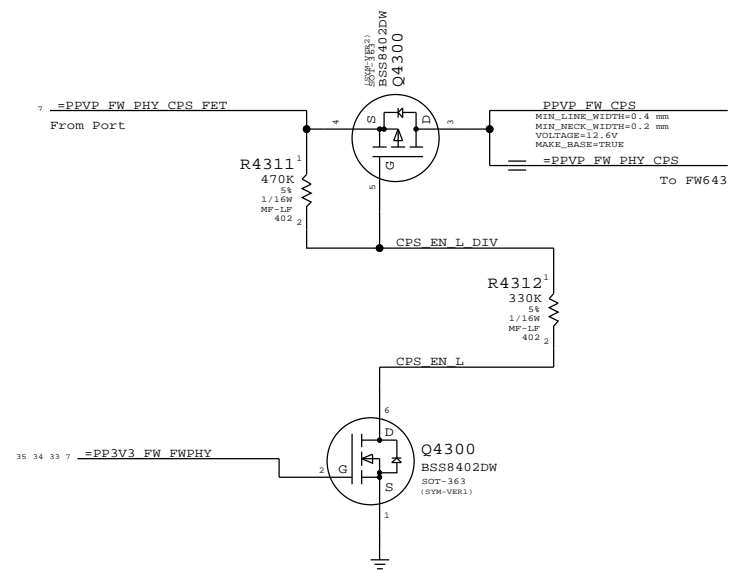
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

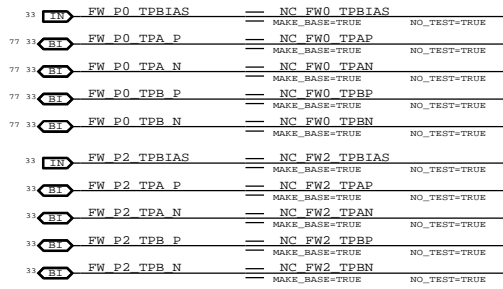
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33. FET blocks current to TPCPS until VDD33 is powered.



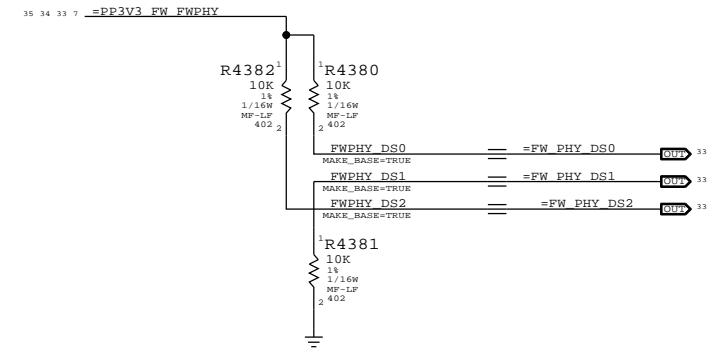
Unused FireWire Ports

Disabled per LSI instructions (All unused port signals TP/NC)



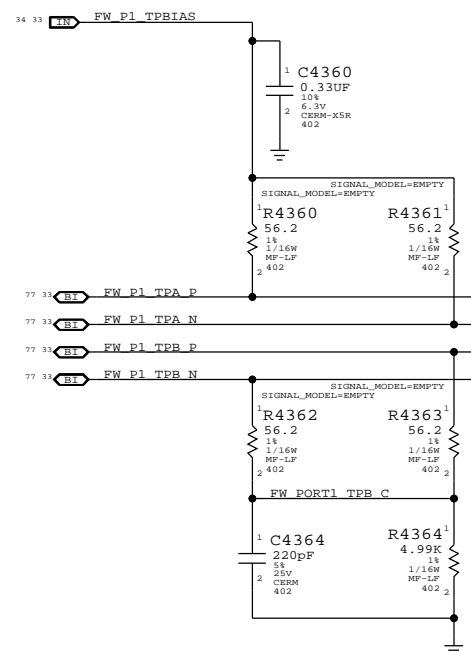
FireWire PHY Config Straps

Configures PHY for:
 - Port "1" Bilingual (1394B)



Termination

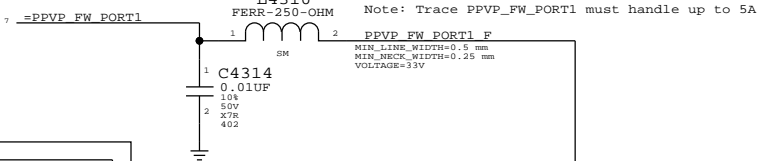
Place close to FireWire PHY



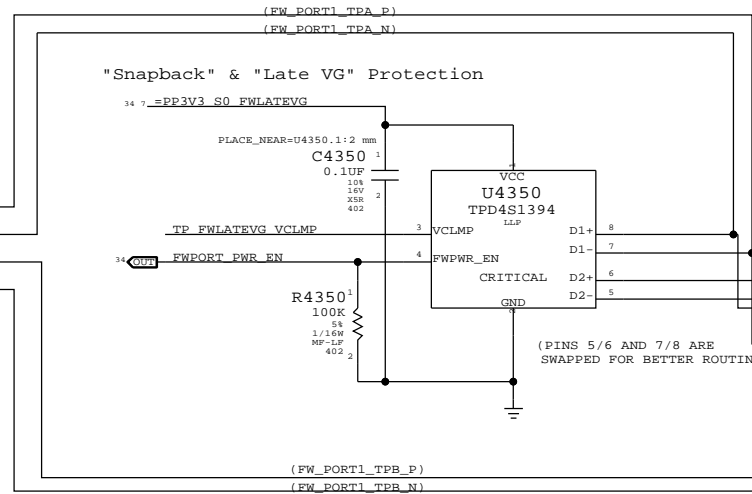
Cable Power

CRITICAL L4310 FERR-250-OHM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

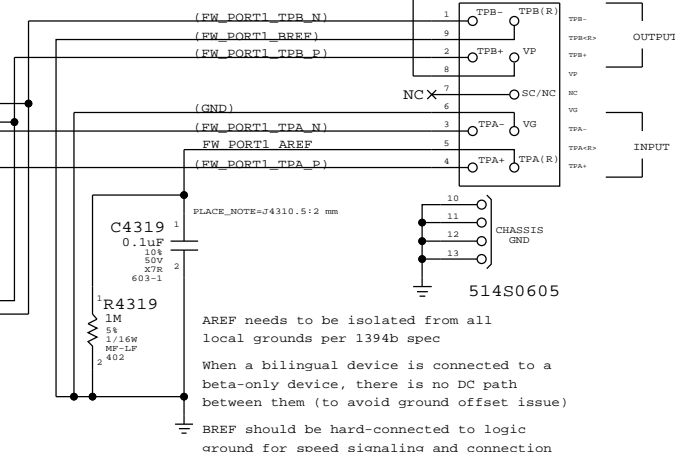


"Snapback" & "Late VG" Protection



PORT 1 BILINGUAL

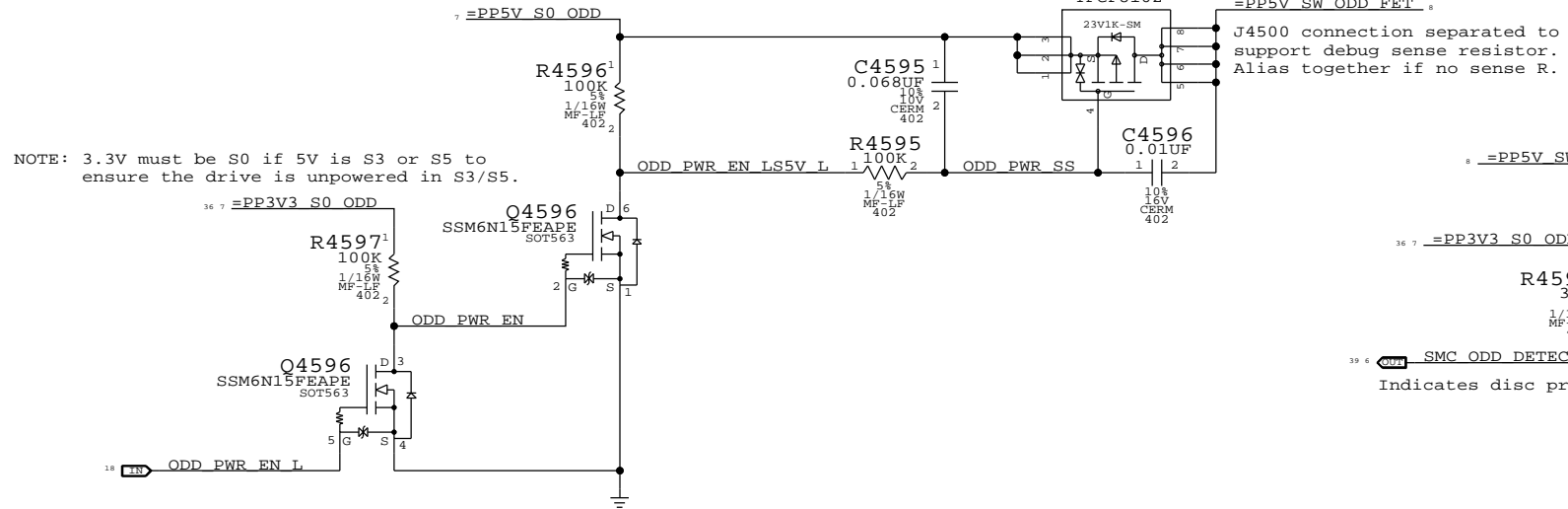
CRITICAL J4310 1394B-M97 F-RT-TH



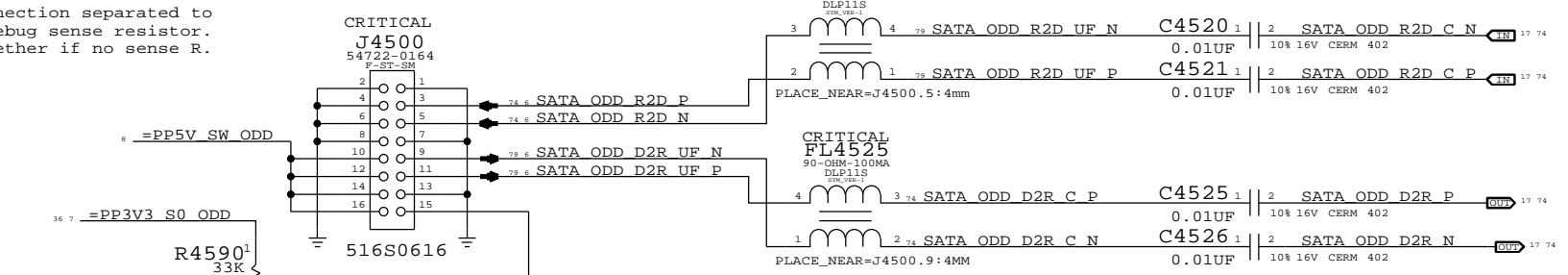
CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
PAGE TITLE: FireWire Connector			
DRAWING NUMBER: 051-8563		SIZE: D	
REVISION: A.13.0		BRANCH:	
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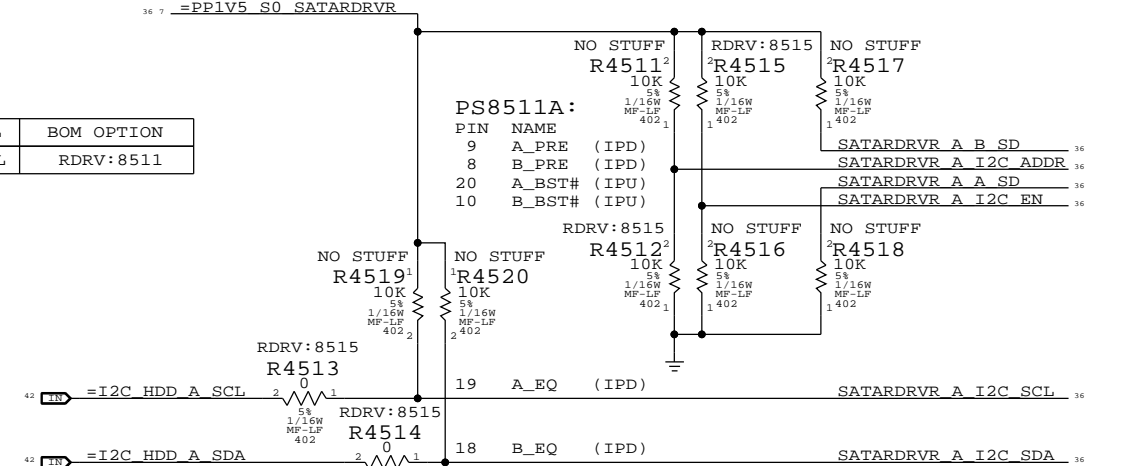
ODD Power Control



SATA ODD Port



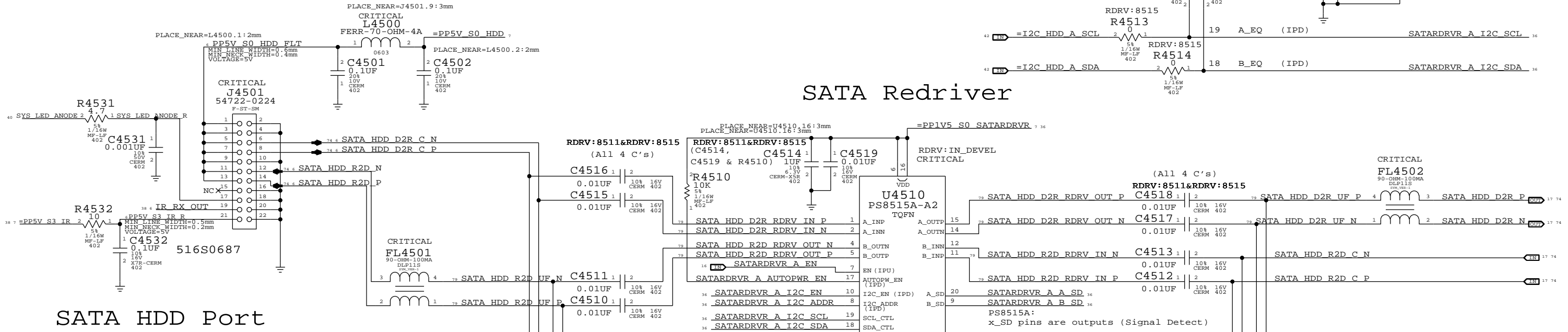
PS8511A / PS8515A Straps



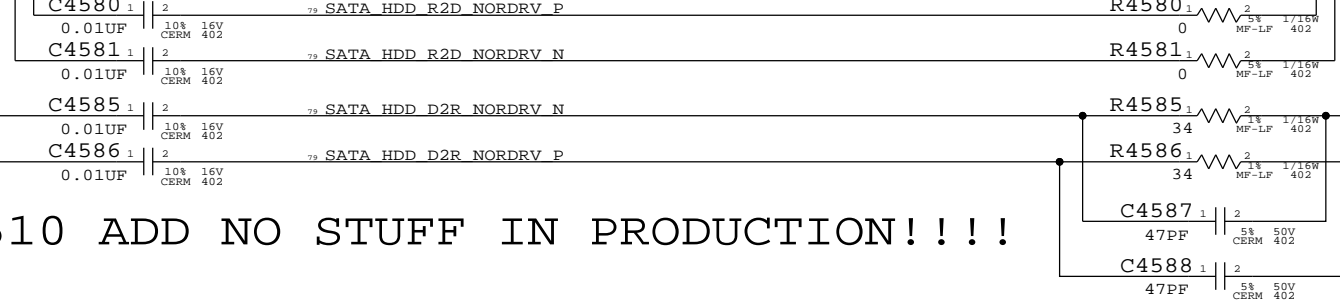
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV:8511

BOMOPTIONS:
 - RDRV:8511 stuffs PS8511A & associated parts (STRAPS TBD!!!)
 - RDRV:8515 stuffs PS8515A & associated parts
 - RDRV:NO stuffs bypass path (neither IC or associated parts stuffed)

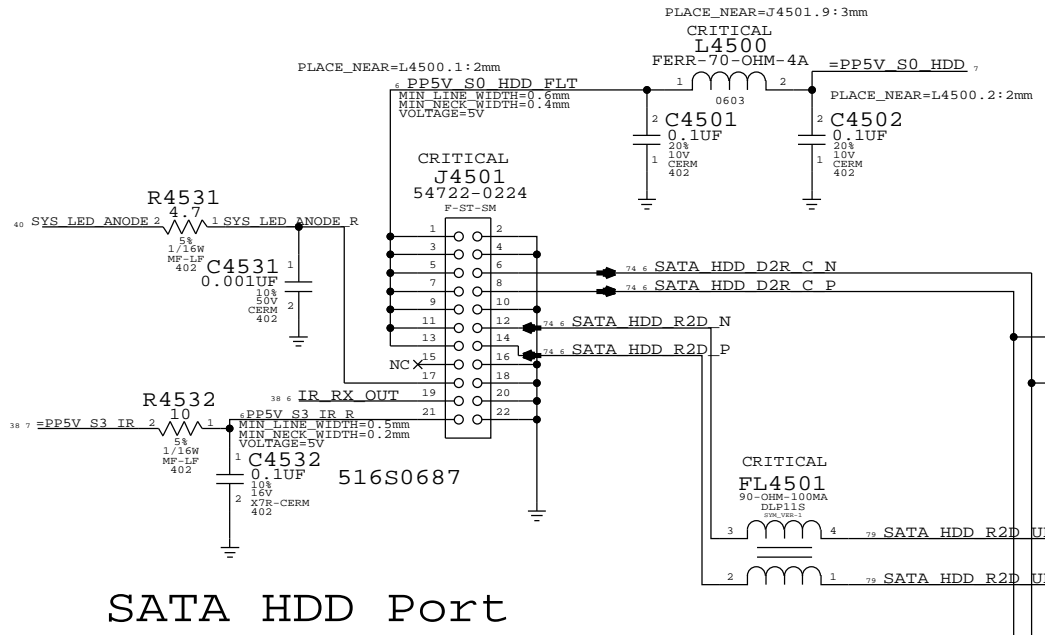
SATA Redriver



Redriver Bypass Path



SATA HDD Port



U4510 ADD NO STUFF IN PRODUCTION!!!

J5401 PINOUTS ARE DIFFERENT FOR K6, DO NOT SYNC THIS PAGE FROM T27 DIRECTLY

SYNC MASTER=T27 MLB SYNC DATE=08/06/2009

SATA Connectors

Apple Inc.

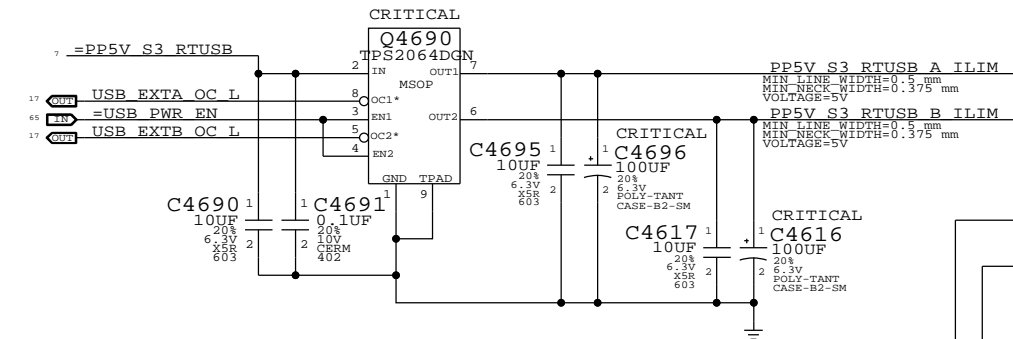
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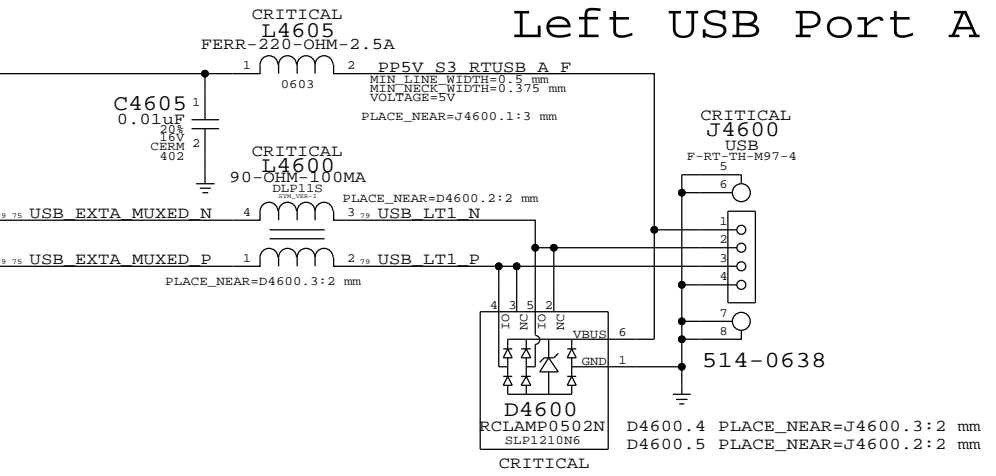
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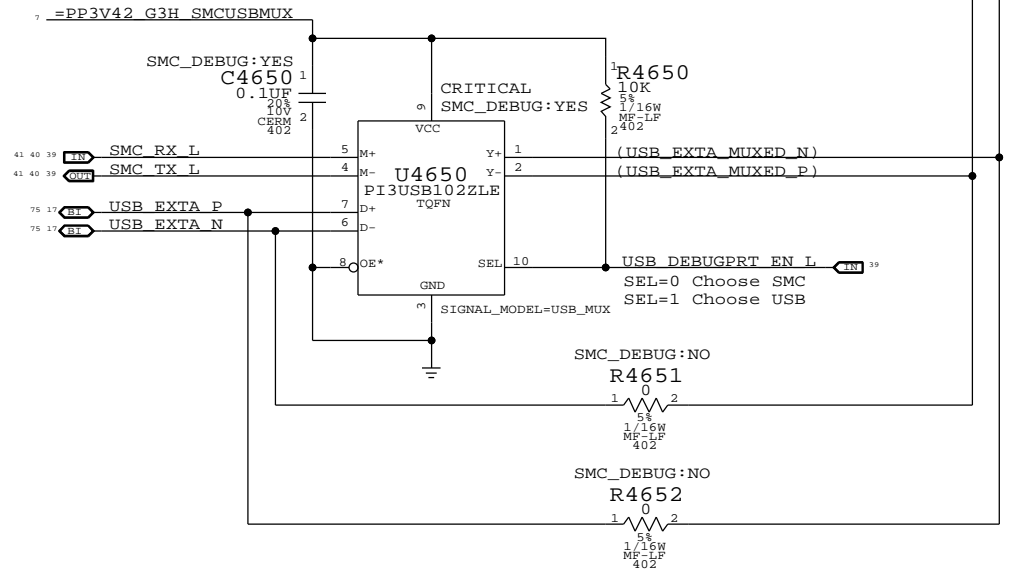
Port Power Switch



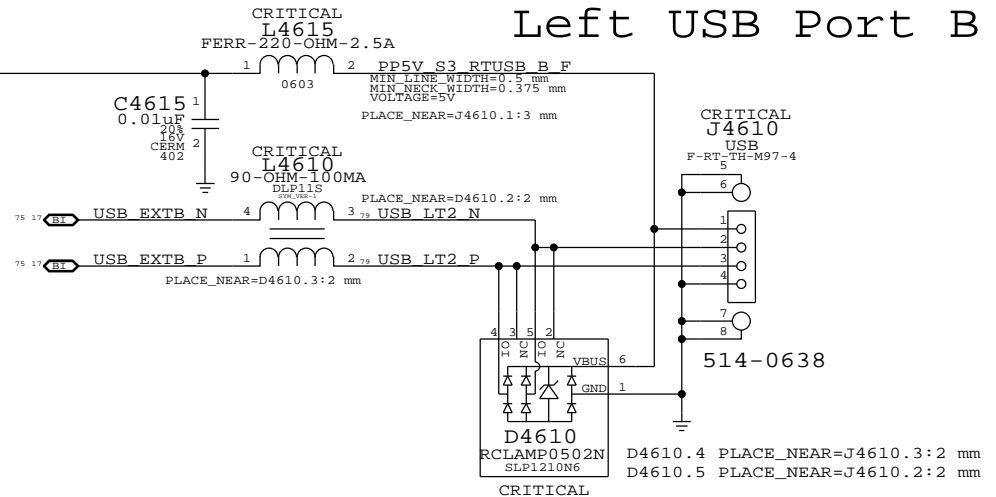
Left USB Port A



USB/SMC Debug Mux

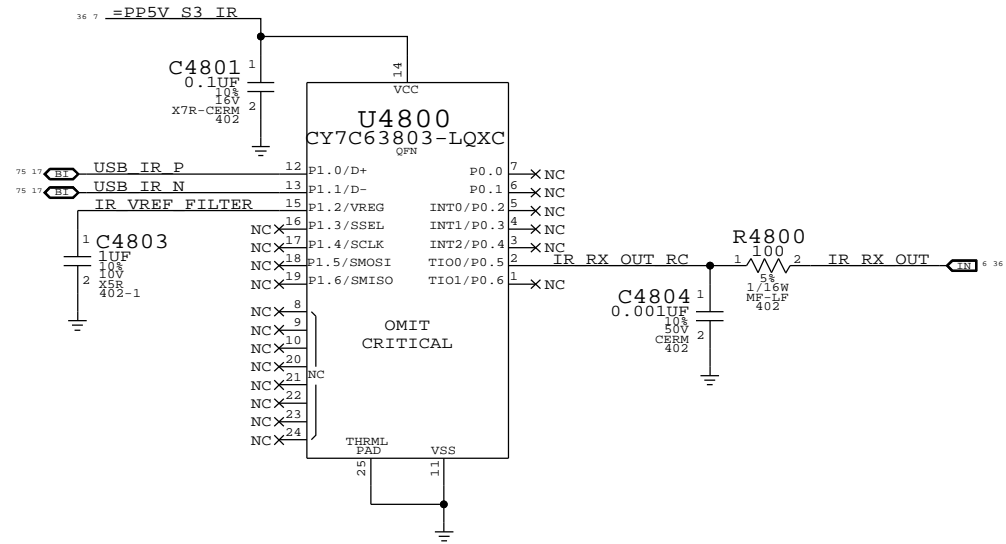


Left USB Port B

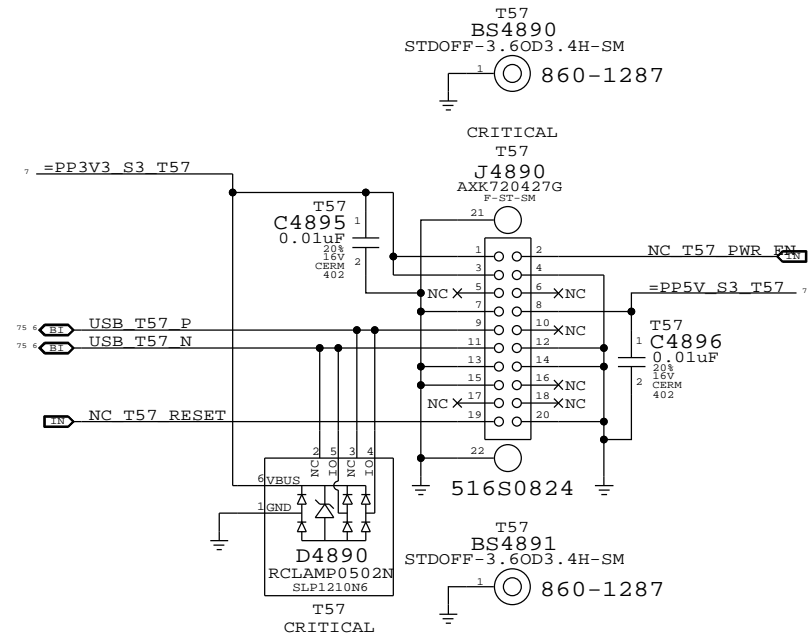


SYNC MASTER=T27 MLB		SYNC DATE=08/27/2009	
External USB Connectors			
Apple Inc.		DRAWING NUMBER	051-8563
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IR Support



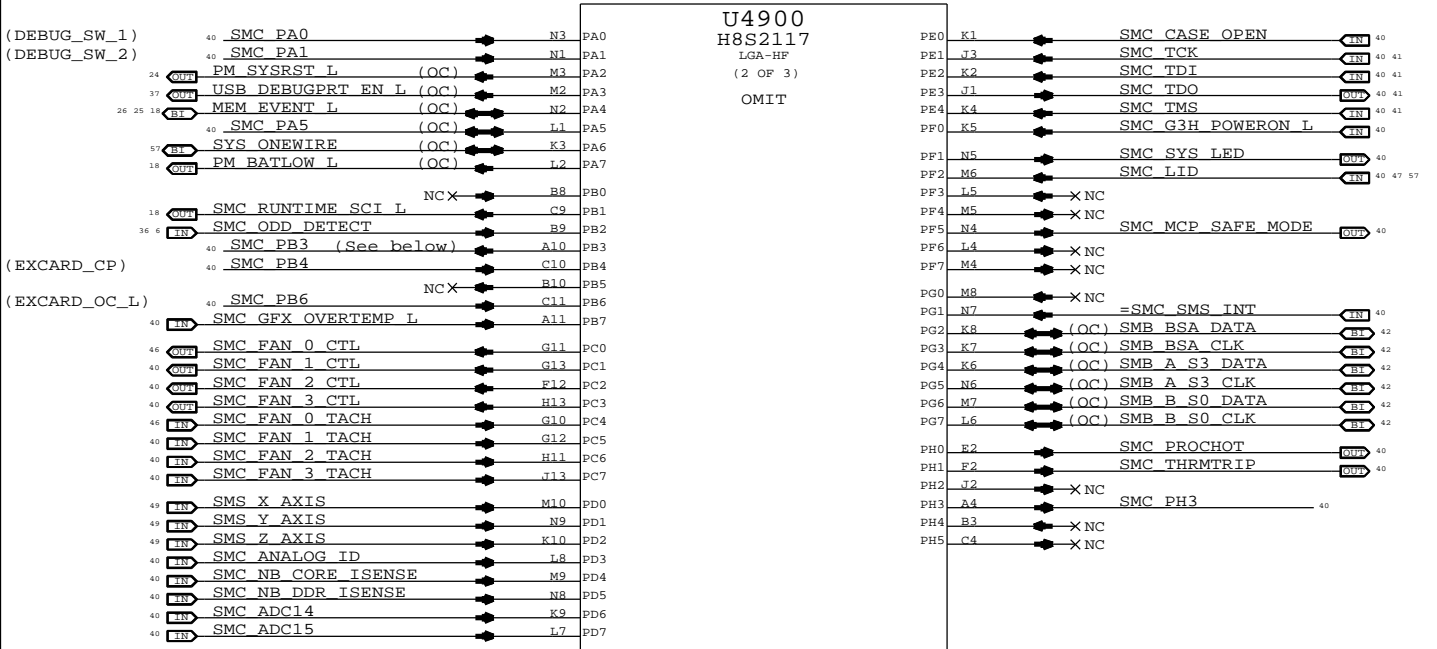
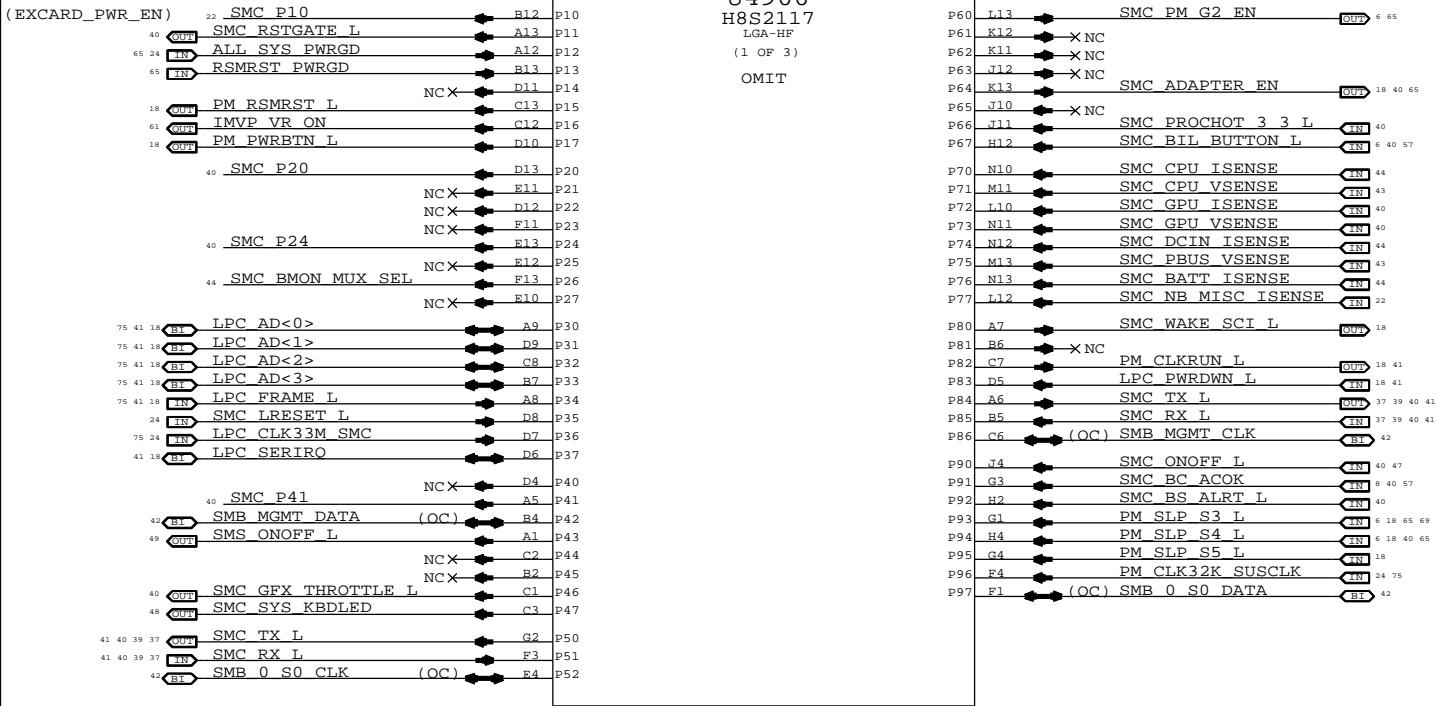
T57 Connector



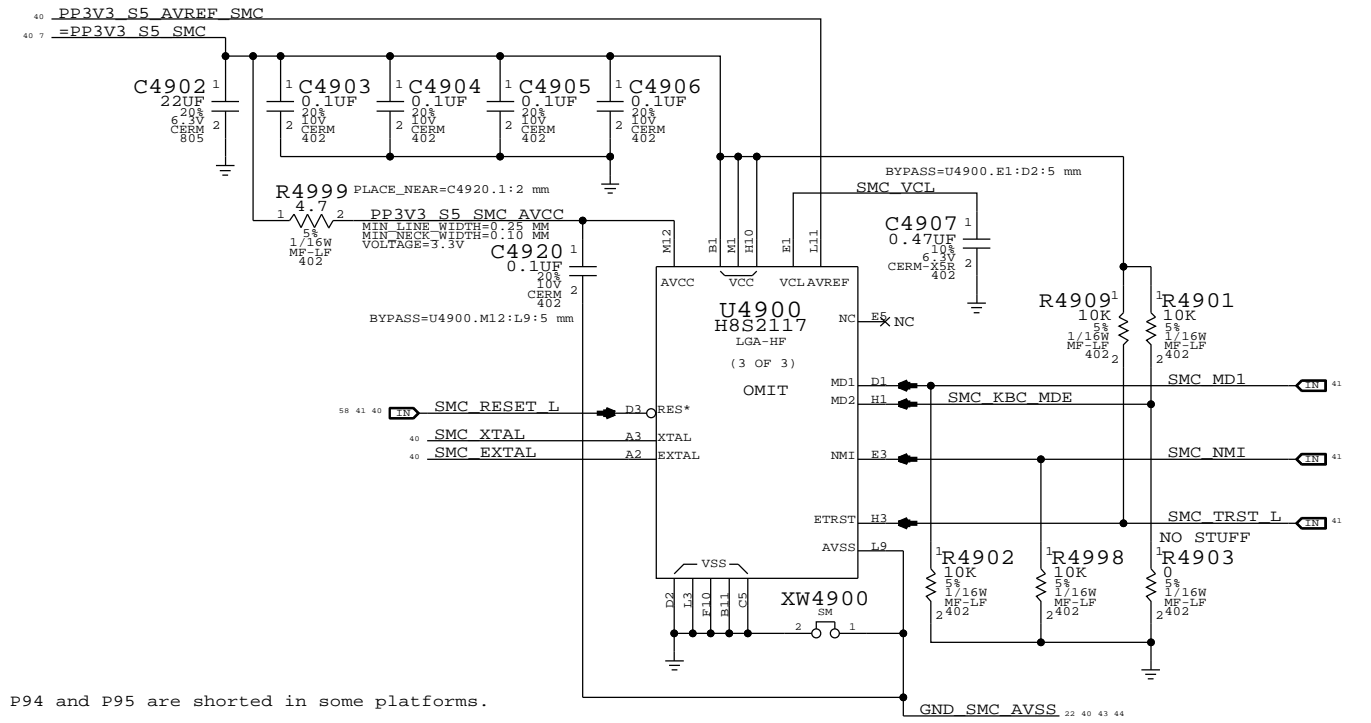
K6 NOTES : D4890 CONNECTION IS DIFFERENT,CANNOT DIRECTLY SYNC FROM T27

SYNC MASTER=T27_MLB		SYNC DATE=08/27/2009	
Internal USB Support			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8563	D
		REVISION	BRANCH
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay.



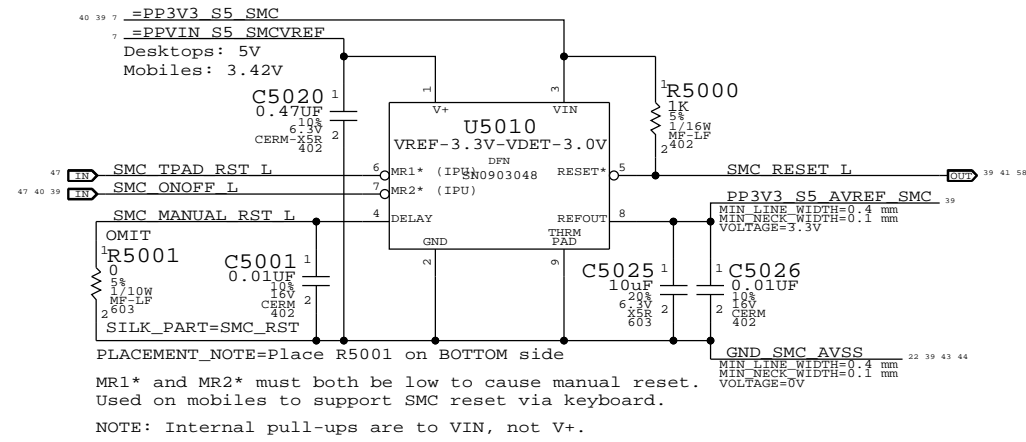
NOTE: P94 and P95 are shorted in some platforms.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

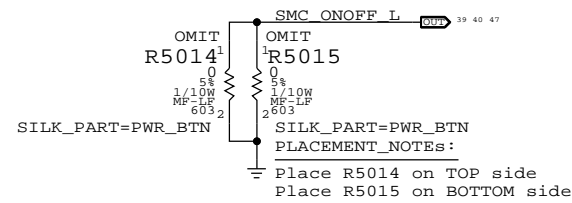
H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC MASTER=T27 MLB		SYNC DATE=09/02/2009	
SMC			
Apple Inc.		DRAWING NUMBER	051-8563
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		PAGE	49 OF 109
		SHEET	39 OF 80

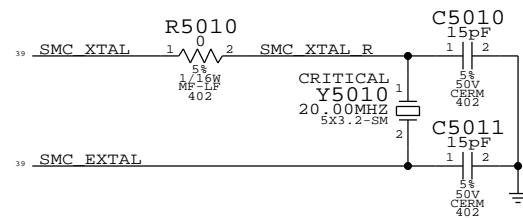
SMC Reset "Button", Supervisor & AVREF Supply



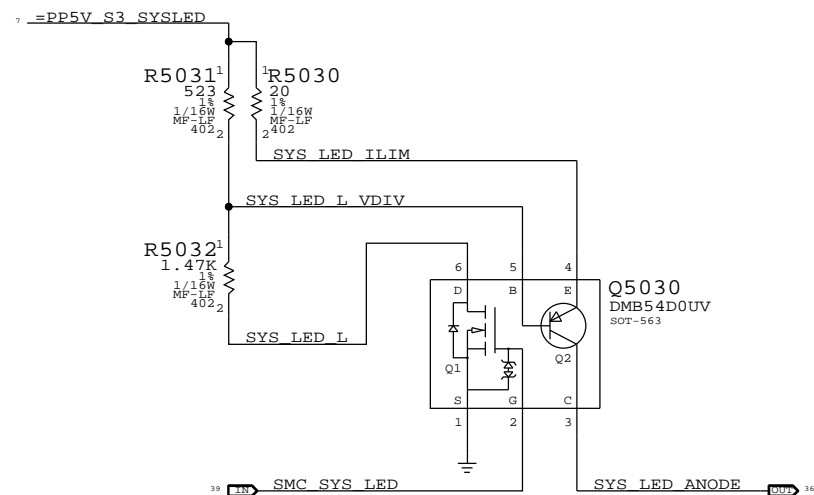
Debug Power "Buttons"



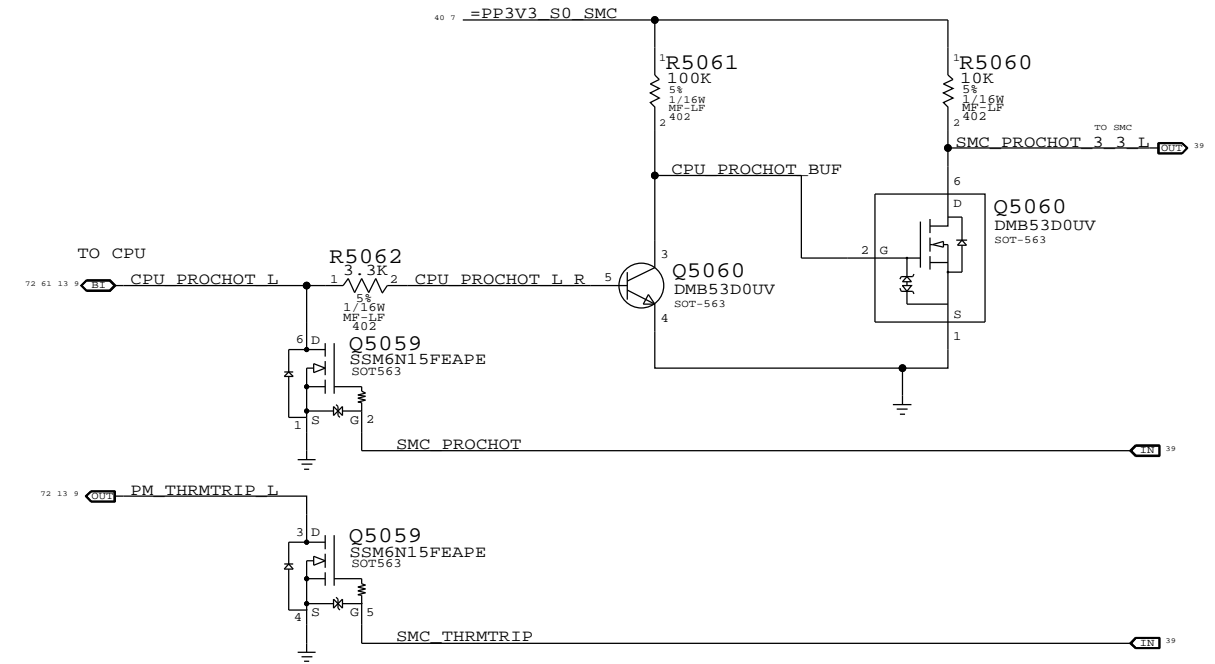
SMC Crystal Circuit



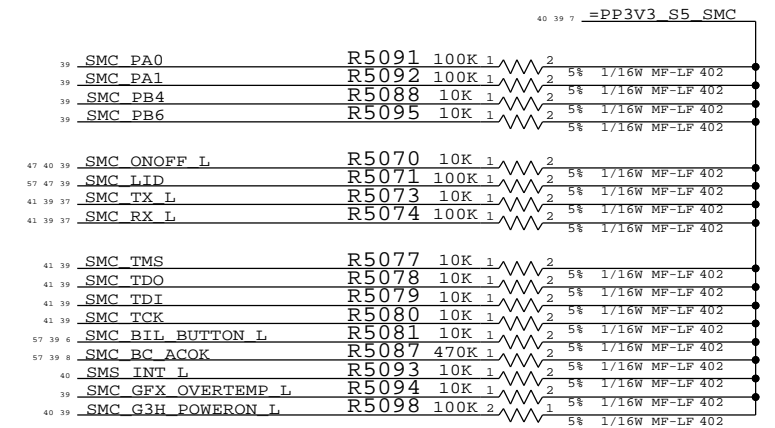
System (Sleep) LED Circuit



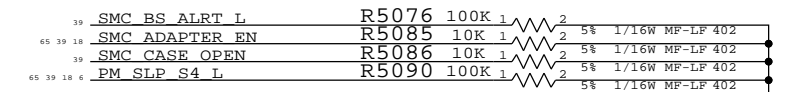
SMC FSB to 3.3V Level Shifting



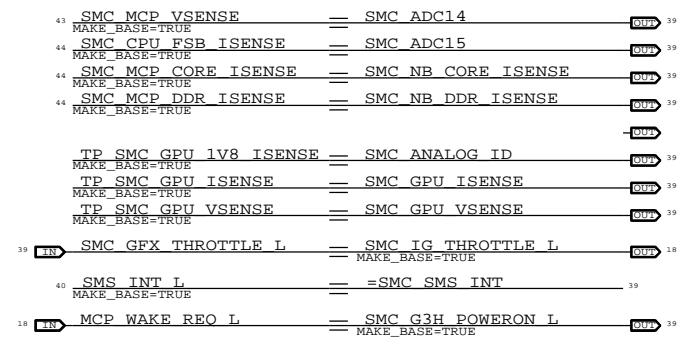
SMC Pull-ups



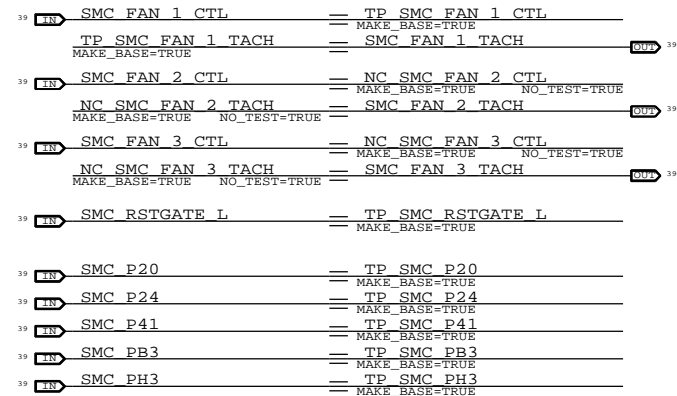
SMC Pull-downs



SMC Aliases



Unused Pins



SYNC MASTER=T27 MLB SYNC DATE=09/02/2009

SMC Support

Apple Inc.

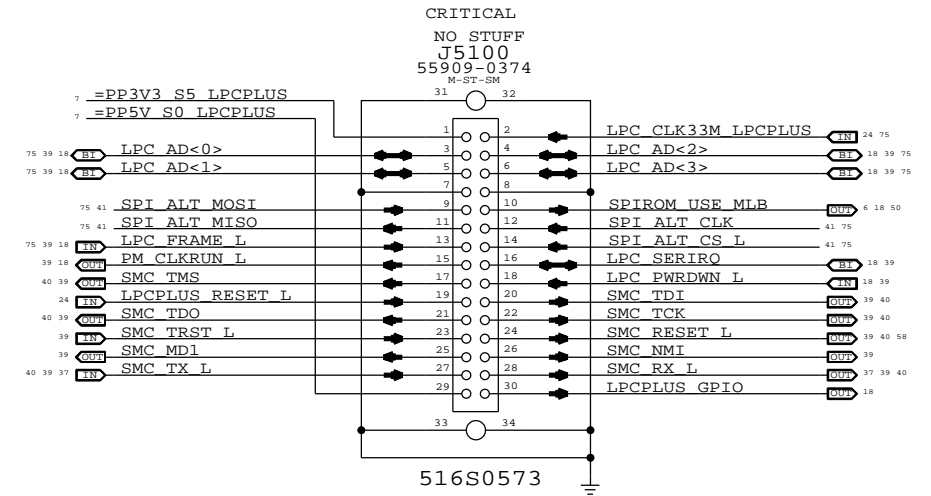
DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

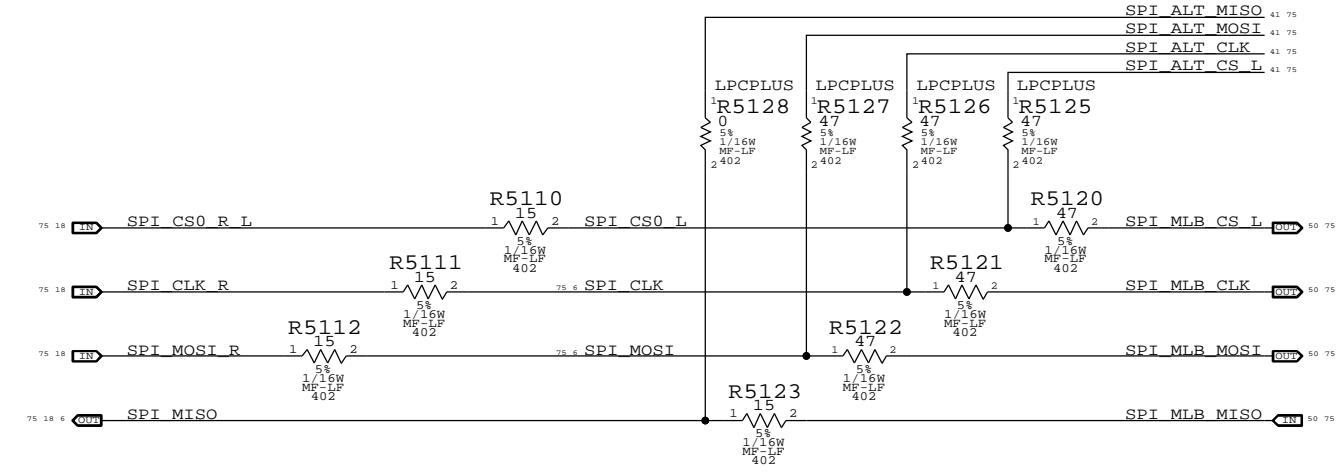
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PAGE: 50 OF 109 SHEET: 40 OF 80

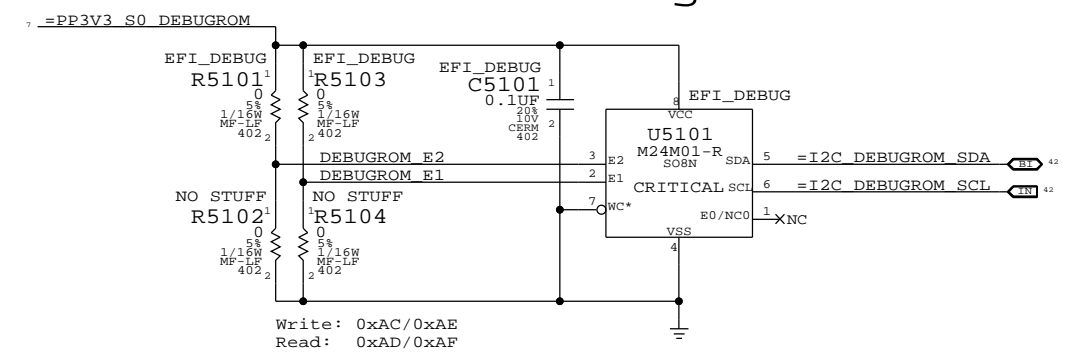
LPC+SPI Connector



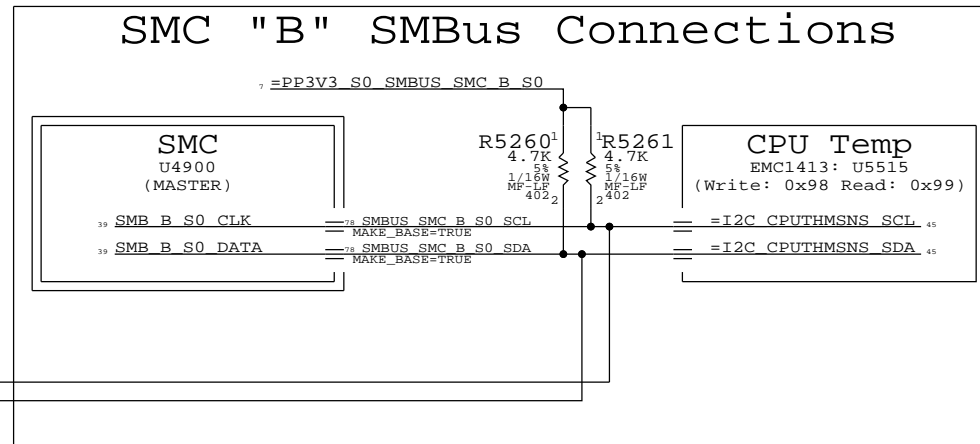
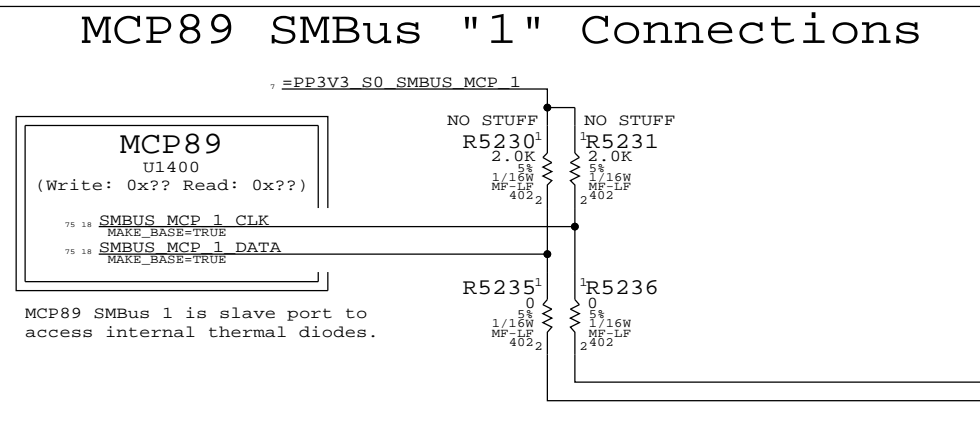
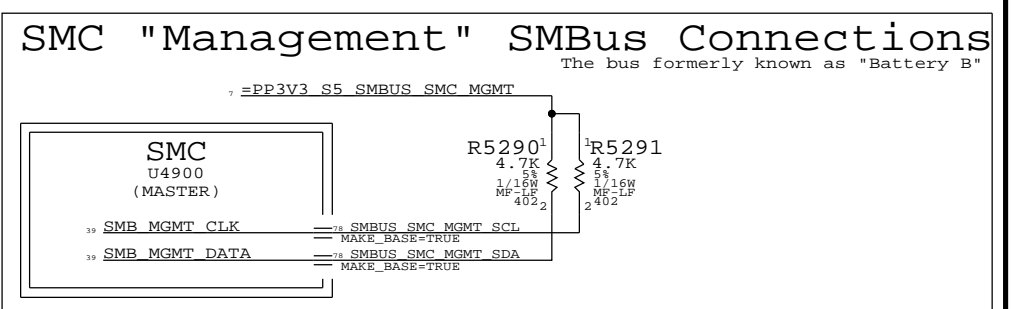
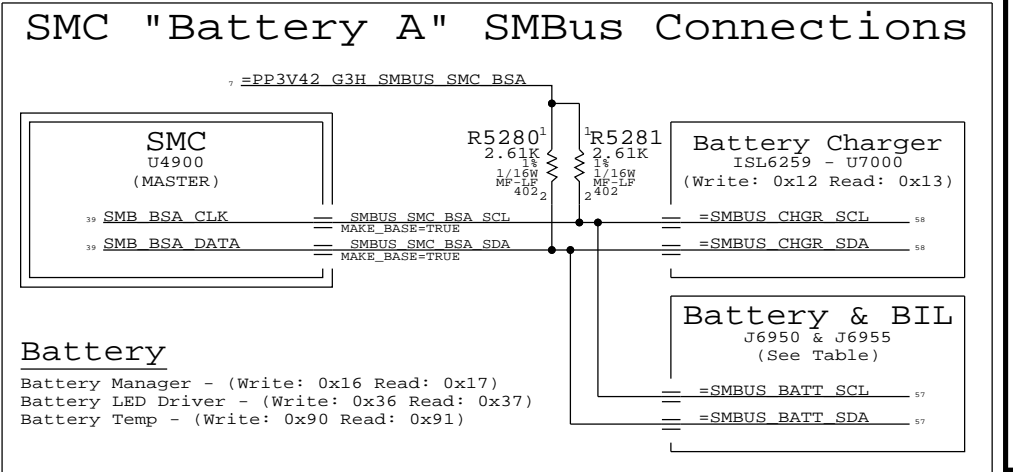
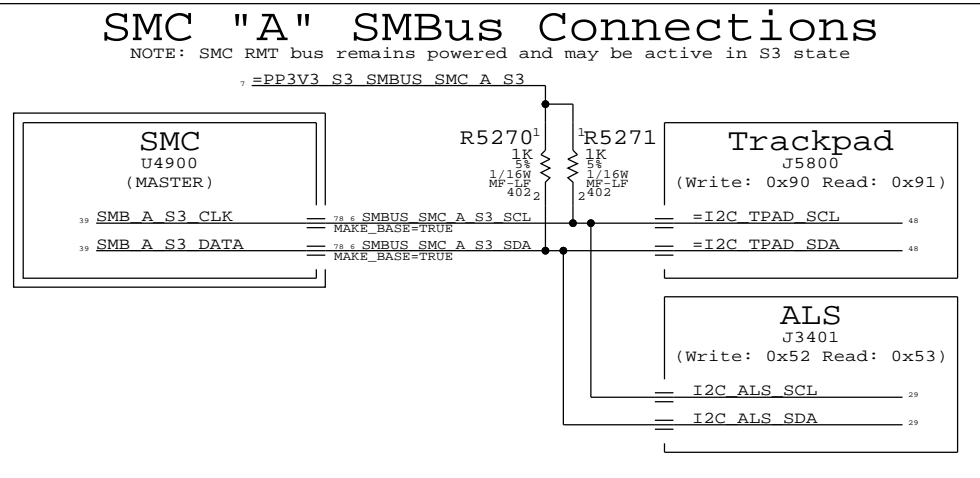
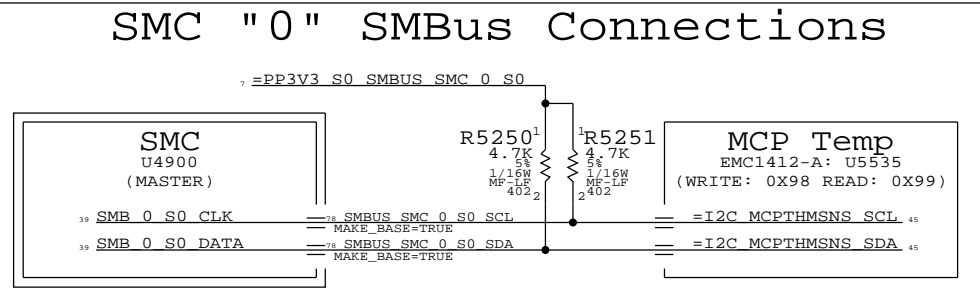
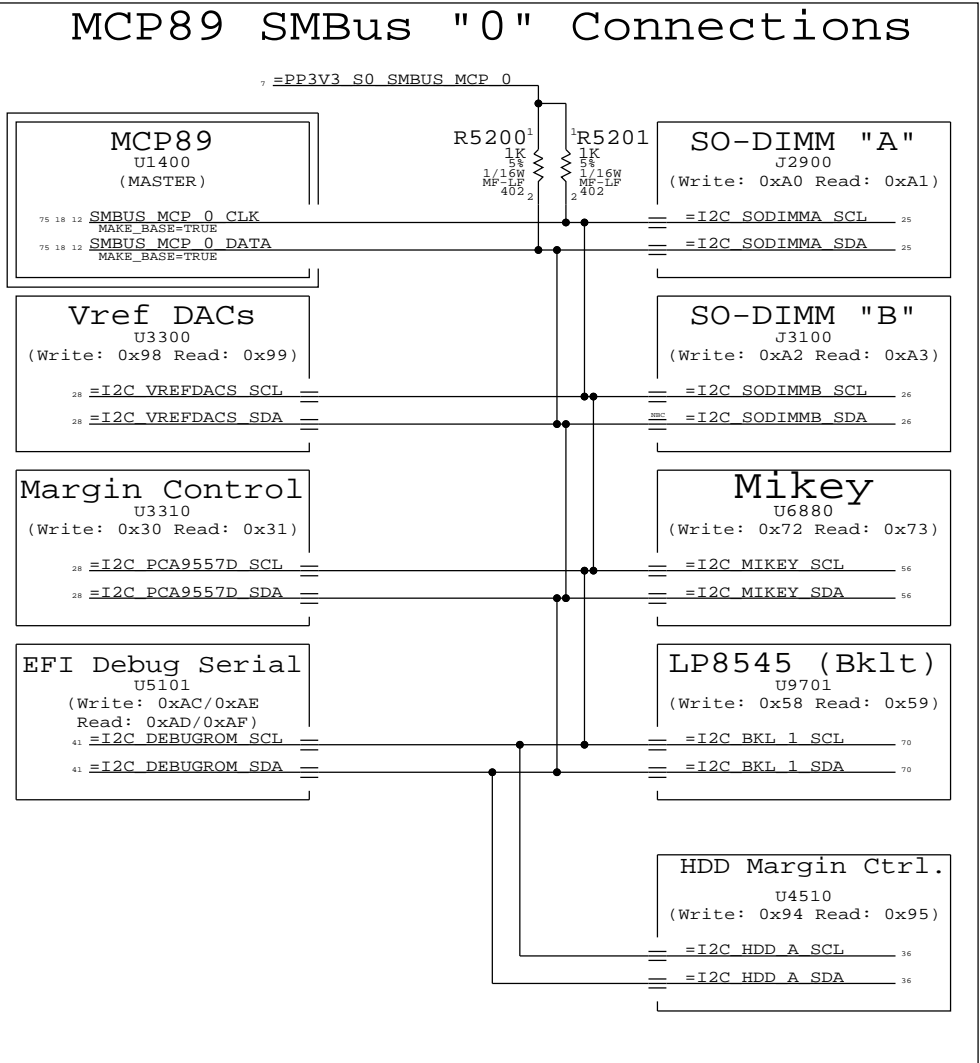
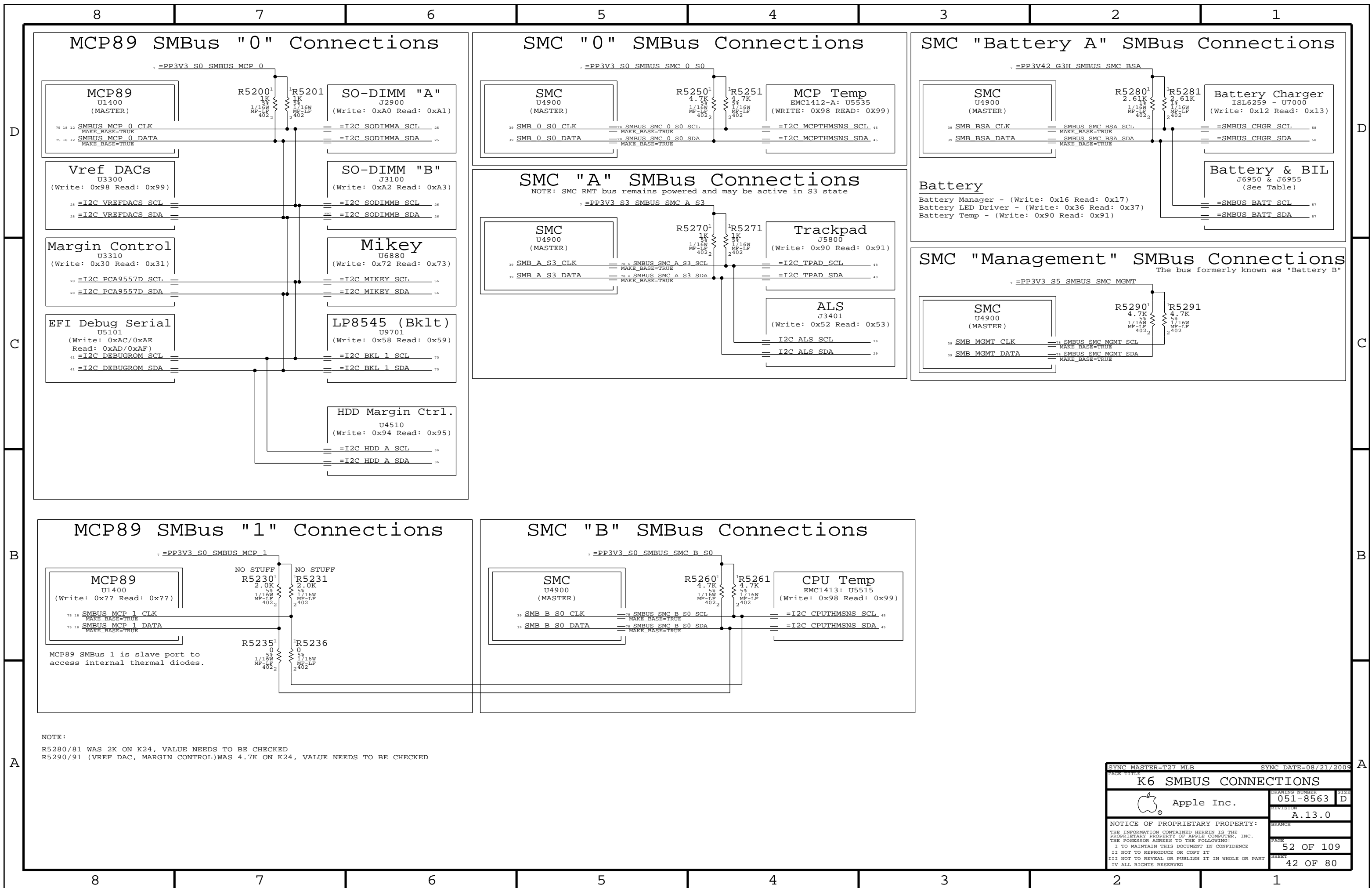
SPI Bus Series Termination



EFI Debug ROM



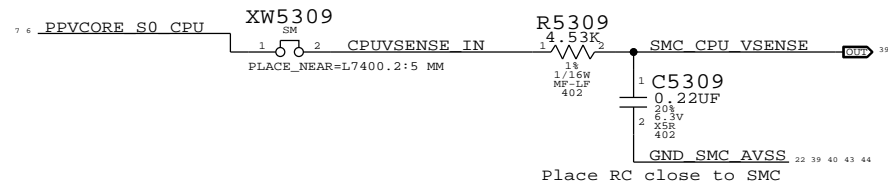
PAGE TITLE		SYNC DATE=08/27/2009	
LPC+SPI Debug Connector			
DRAWING NUMBER		SIZE	
051-8563		D	
REVISION		BRANCH	
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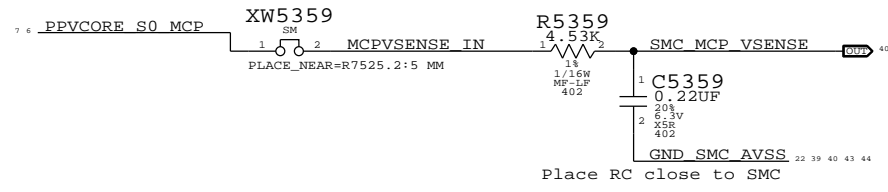
NOTE:
R5280/81 WAS 2K ON K24, VALUE NEEDS TO BE CHECKED
R5290/91 (VREF DAC, MARGIN CONTROL) WAS 4.7K ON K24, VALUE NEEDS TO BE CHECKED

SYNC MASTER=T27 MLB		SYNC DATE=08/21/2009	
PAGE TITLE K6 SMBUS CONNECTIONS			
Apple Inc.		DRAWING NUMBER 051-8563	SIZE D
		REVISION A.13.0	BRANCH
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		PAGE 52 OF 109	SHEET 42 OF 80

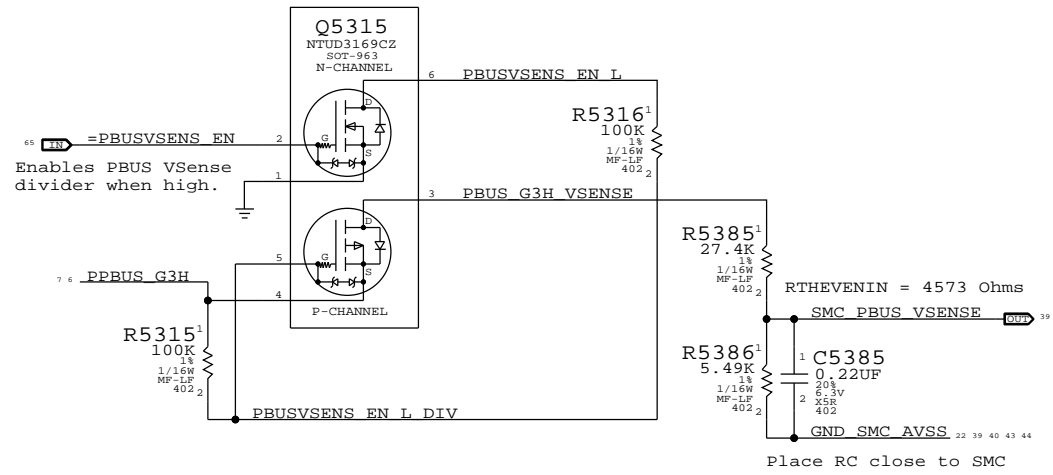
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter

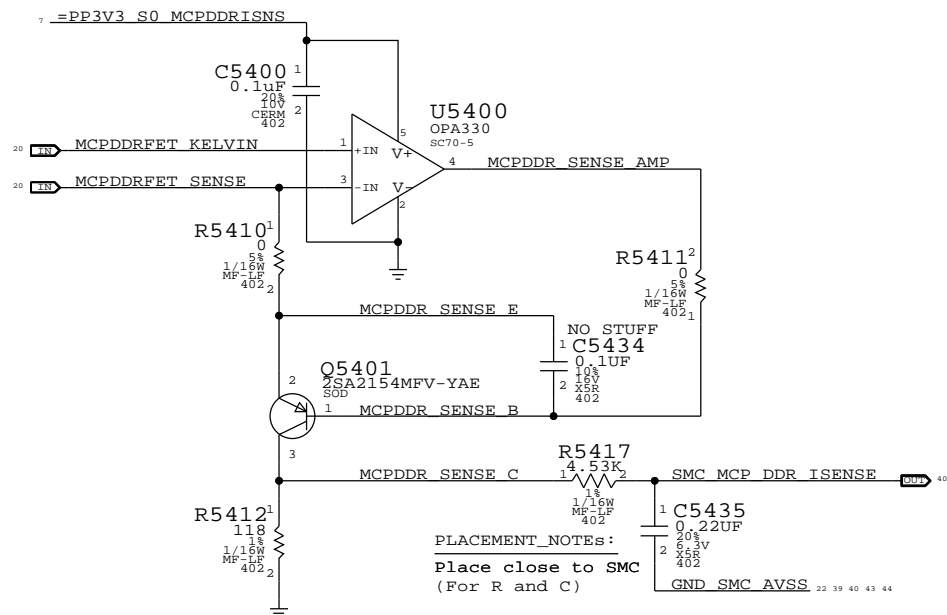


PBUS Voltage Sense Enable & Filter

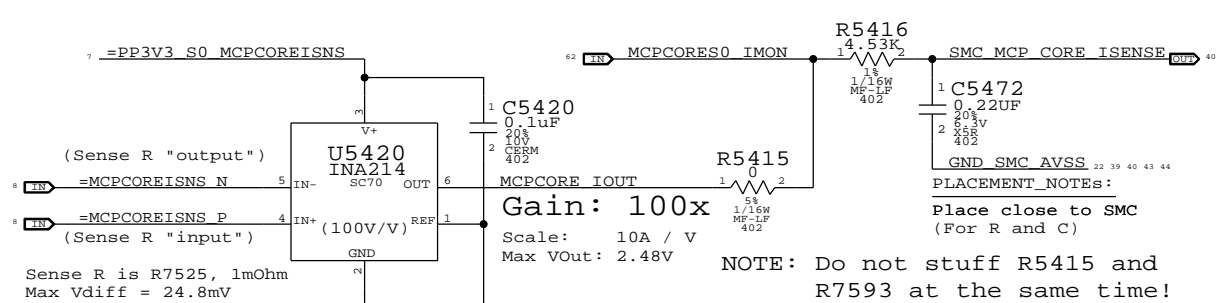


SYNC MASTER=T27 MLB		SYNC DATE=08/27/2009	
Voltage Sensing			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8563	D
		REVISION	
		A.13.0	
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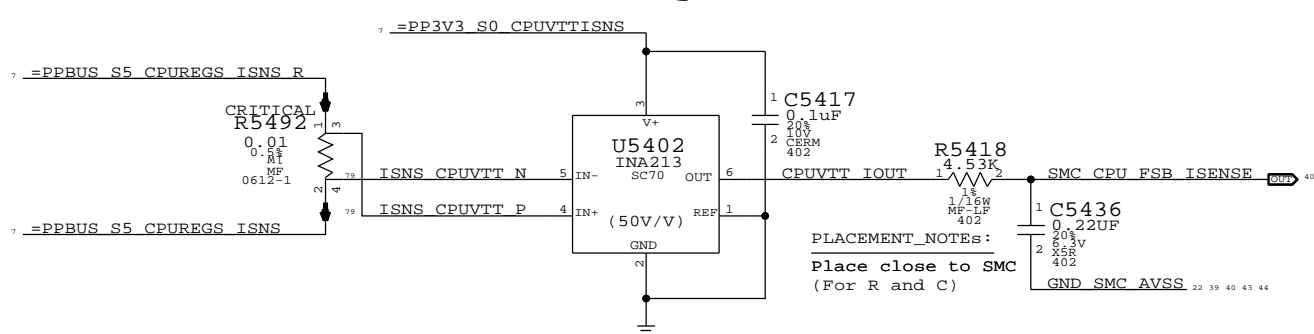
MCP MEM VDD Current Sense / Filter



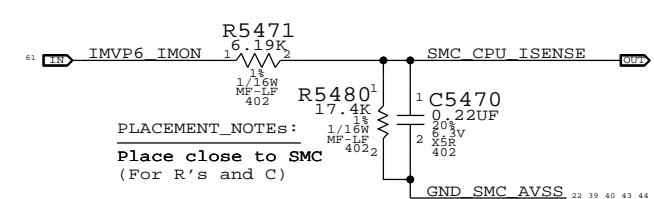
MCP VCore Current Sense Filter



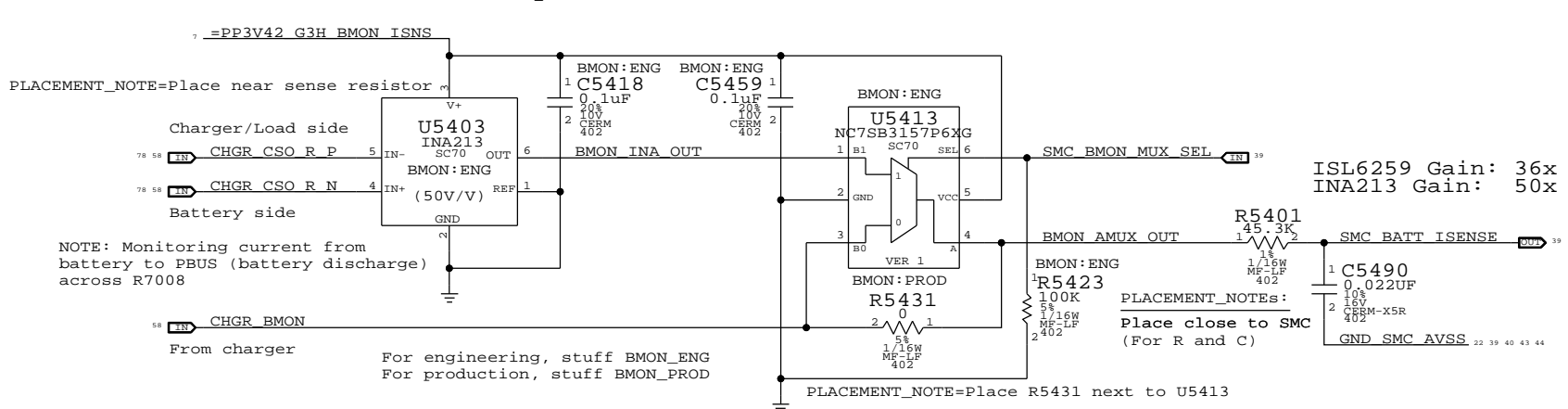
MCP/CPU 1.05V AND CPU VCore High-Side Current Sense / Filter



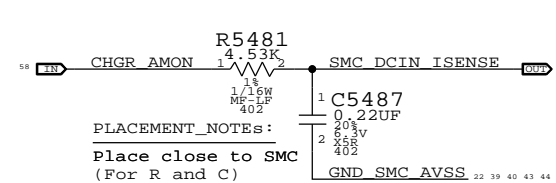
CPU VCore Load Side Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter

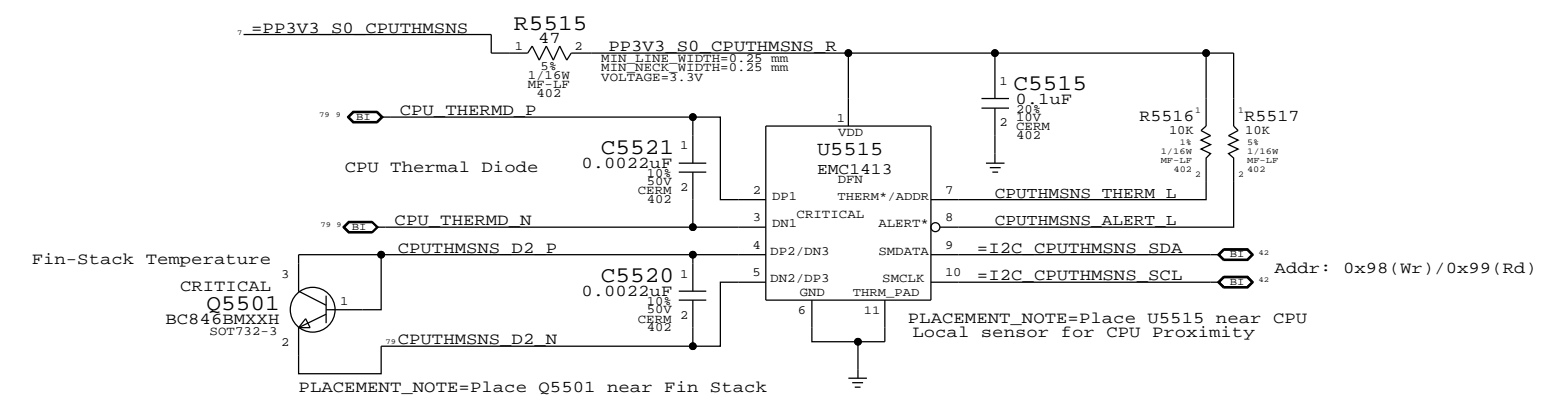


DC-IN (AMON) Current Sense Filter

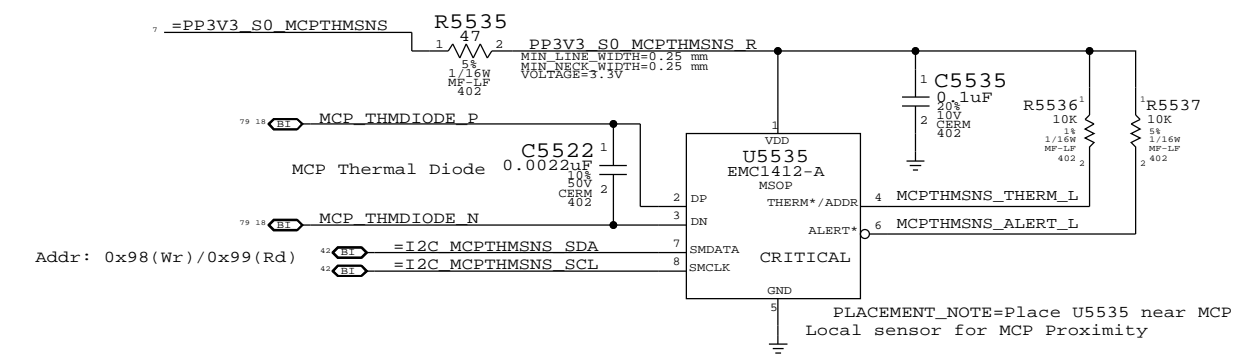


PAGE TITLE		SYNC DATE=09/30/2009	
Current Sensing			
DRAWING NUMBER		SIZE	
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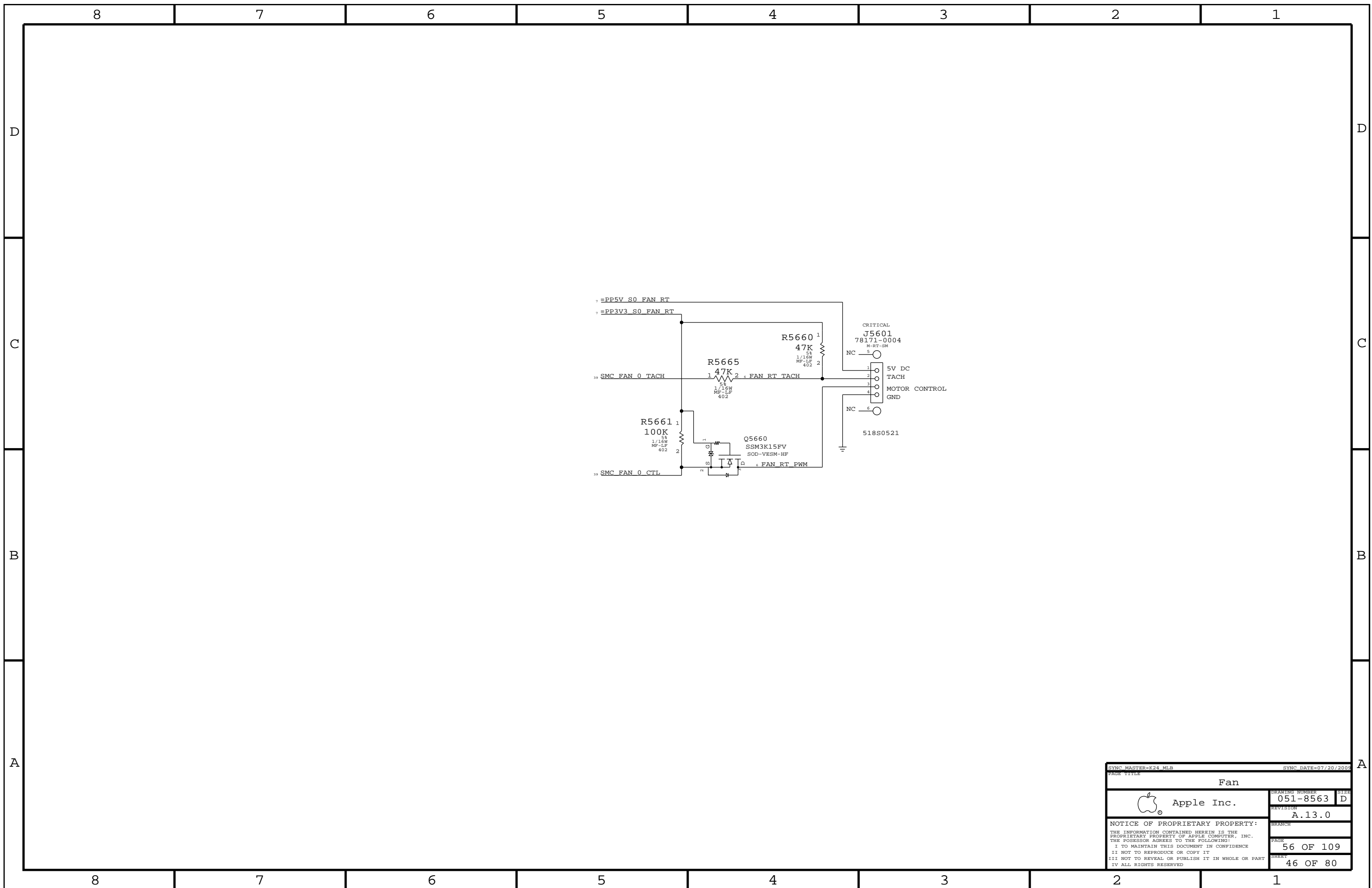
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



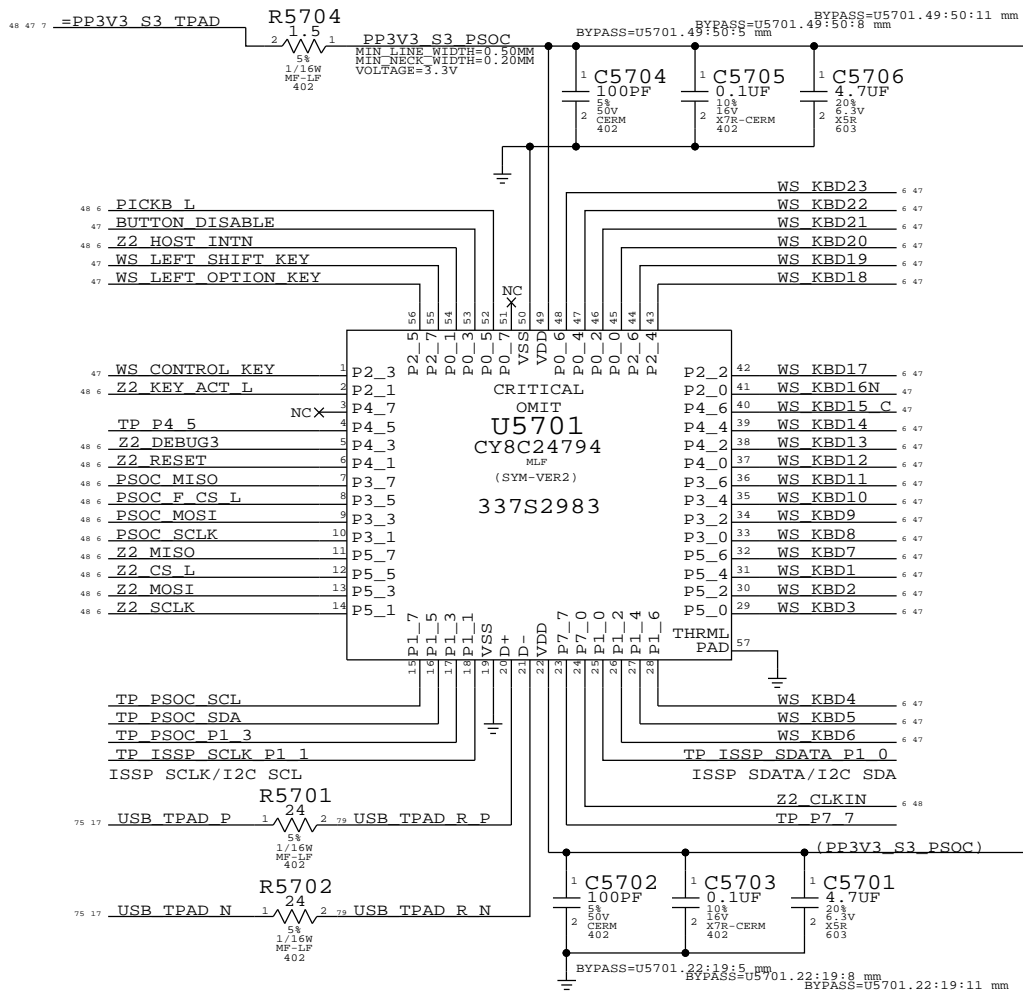
SYNC MASTER=T27 MLB		SYNC DATE=08/27/2009	
Thermal Sensors			
Apple Inc.		DRAWING NUMBER	051-8563
		REVISION	A.13.0
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SYNC MASTER=K24_MLB		SYNC DATE=07/20/2005	
PAGE TITLE Fan			
DRAWING NUMBER 051-8563		SIZE D	
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PAGE 56 OF 109		SHEET 46 OF 80	

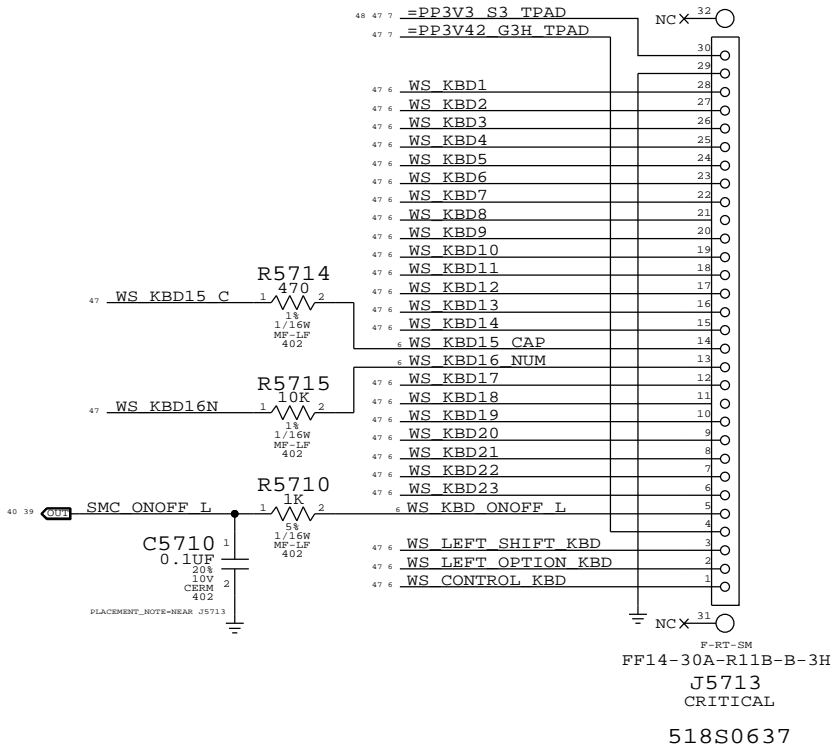
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



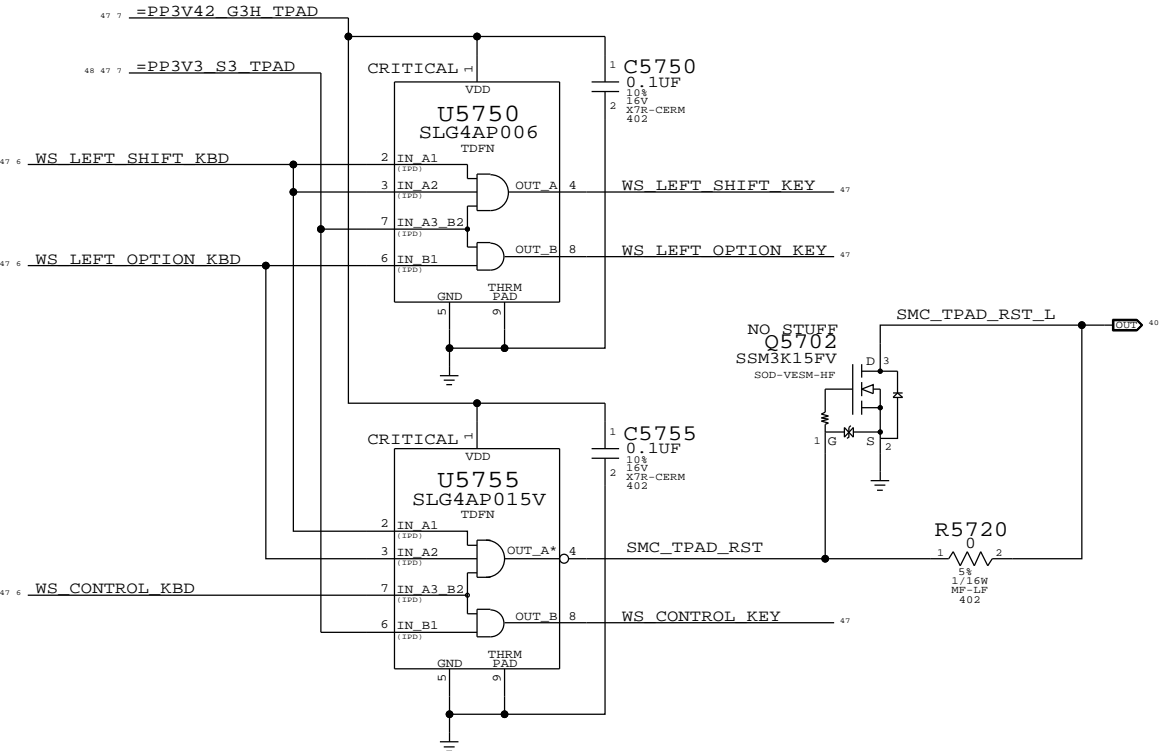
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

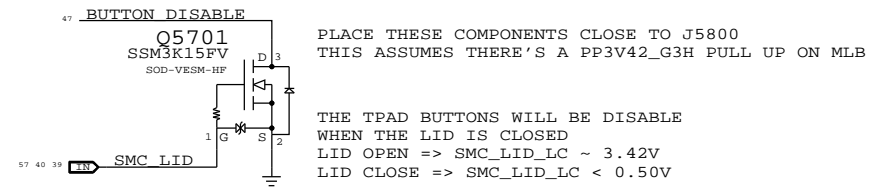


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.



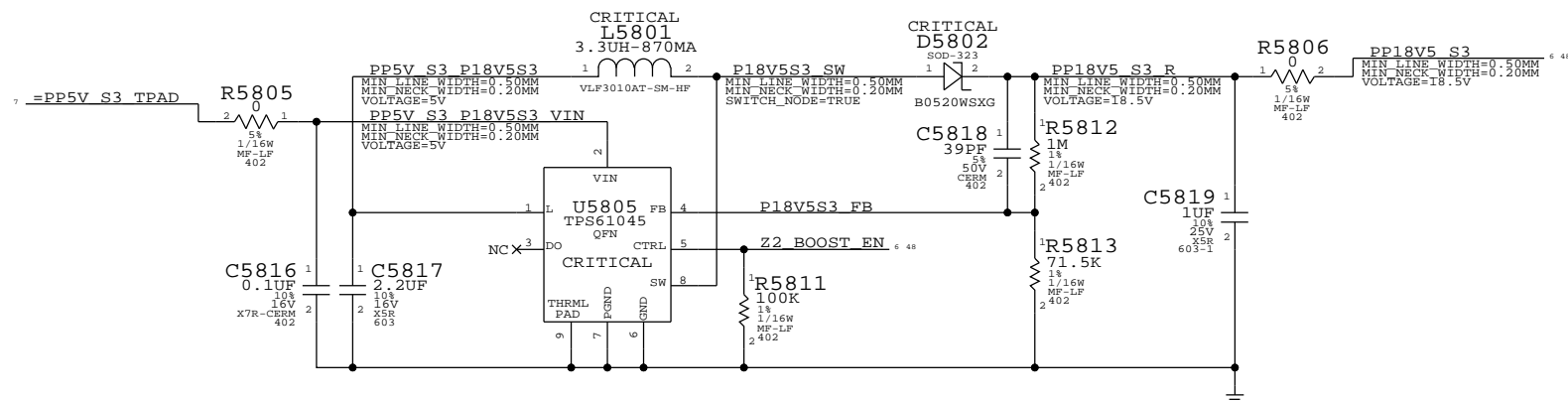
TPAD Buttons Disable



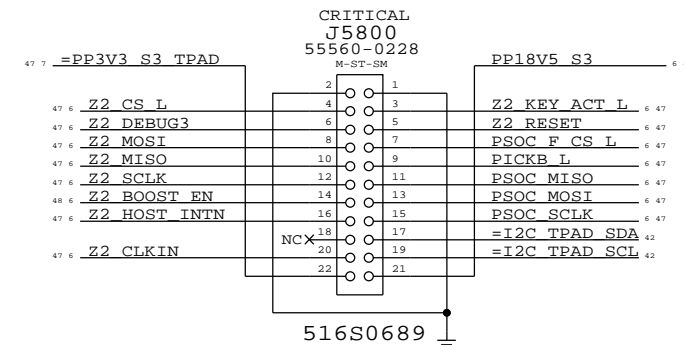
SYNC MASTER=T27 MLB		SYNC DATE=08/15/2009	
PAGE TITLE			
WELLSPRING 1			
Apple Inc.		DRAWING NUMBER	051-8563
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BOOSTER +18.5VDC FOR SENSORS

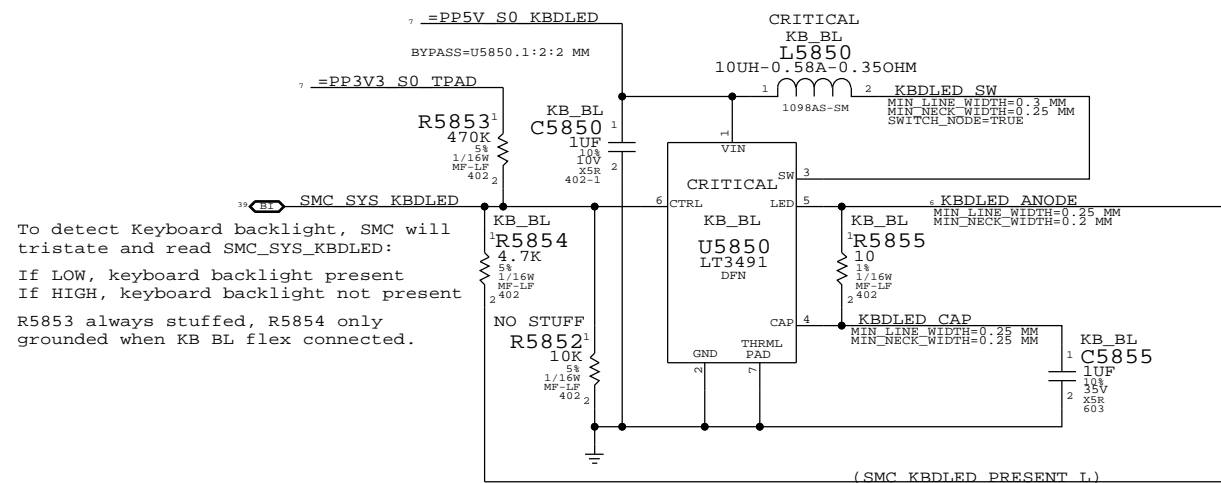
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED



IPD Flex Connector

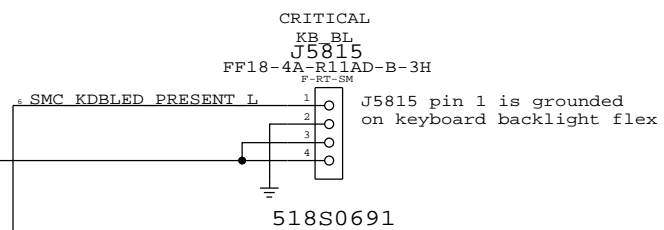


Keyboard Backlight Driver & Detection



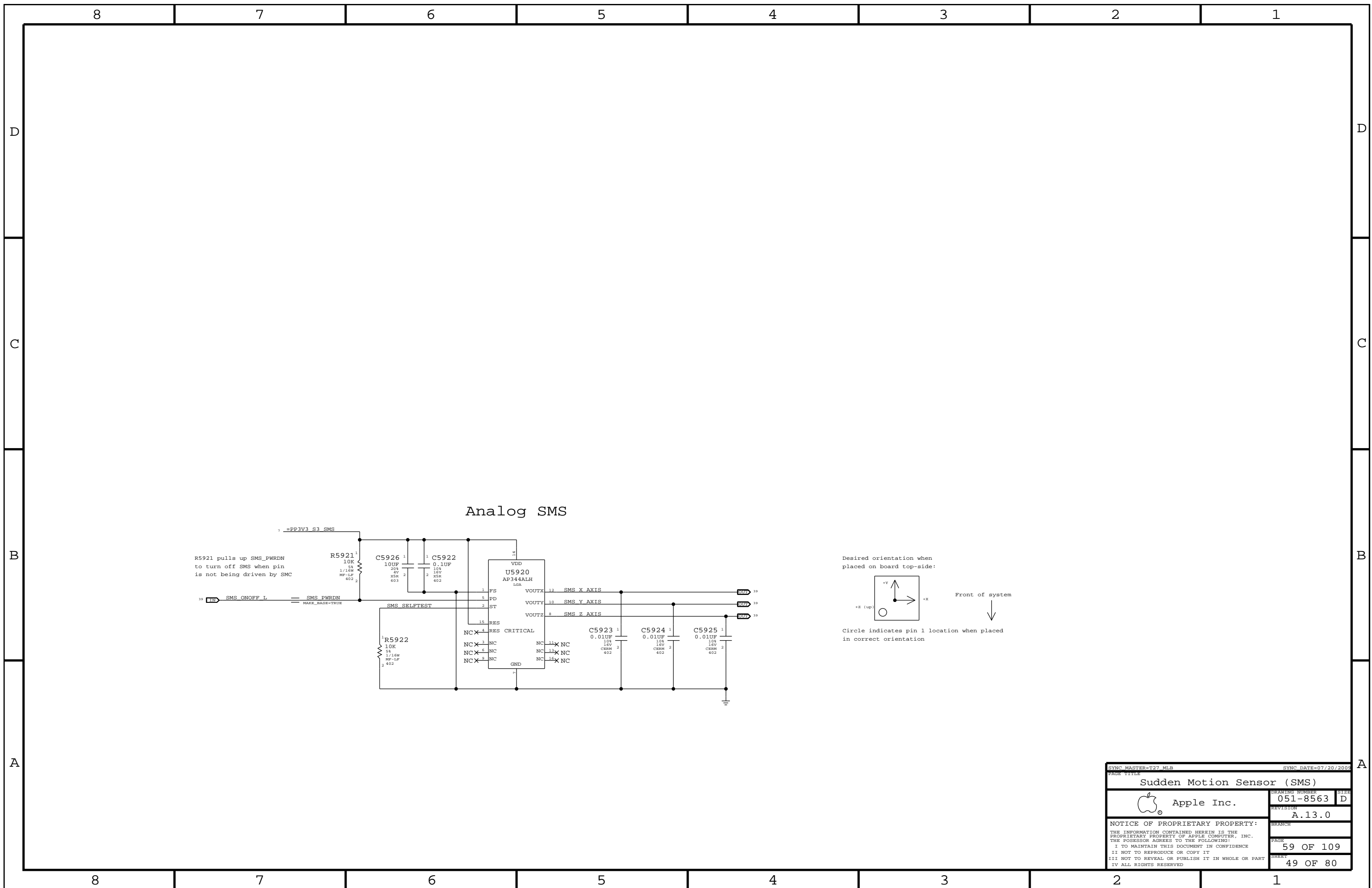
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
 If LOW, keyboard backlight present
 If HIGH, keyboard backlight not present
 R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=T27_MLB		SYNC DATE=08/03/2009	
PAGE TITLE WELLSPRING 2			
DRAWING NUMBER 051-8563		SIZE D	
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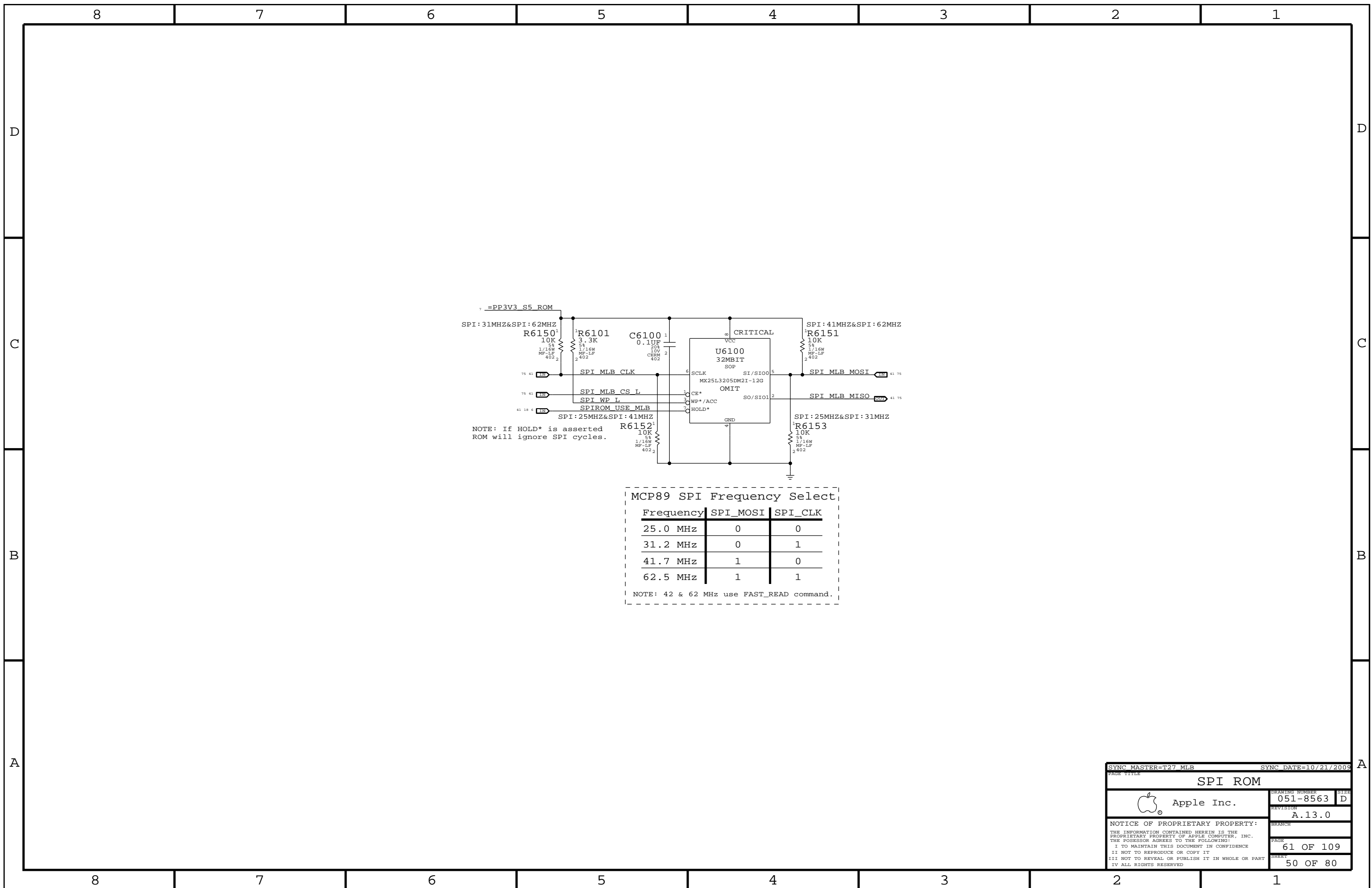
Analog SMS

R5921 pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=T27_MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
Sudden Motion Sensor (SMS)			
DRAWING NUMBER		SIZE	
051-8563		D	
REVISION		PAGE	
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MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=T27_MLB SYNC_DATE=10/21/2009

SPI ROM

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

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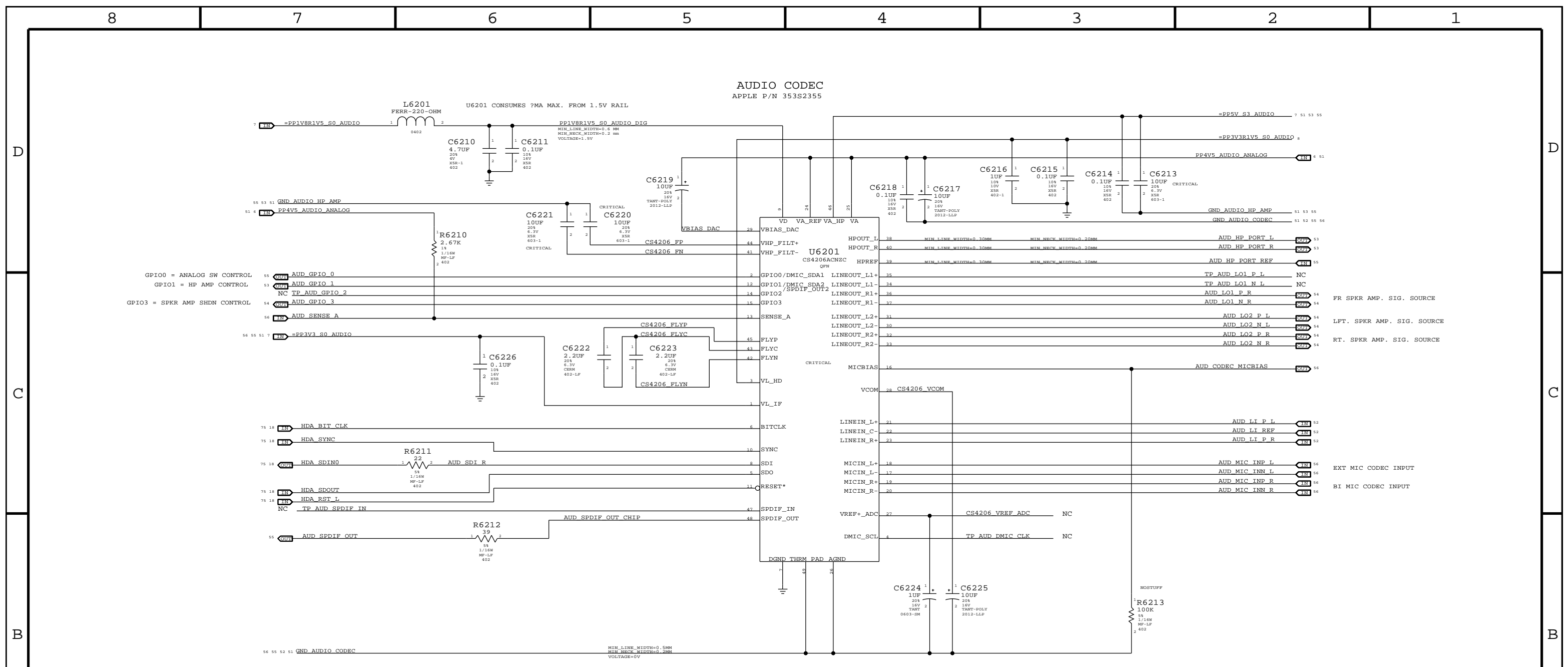
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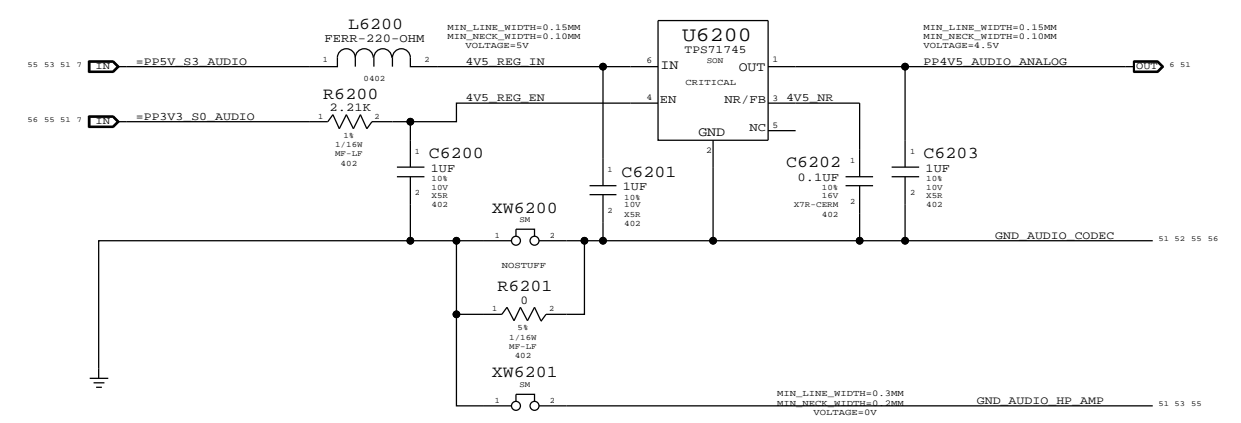
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4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456

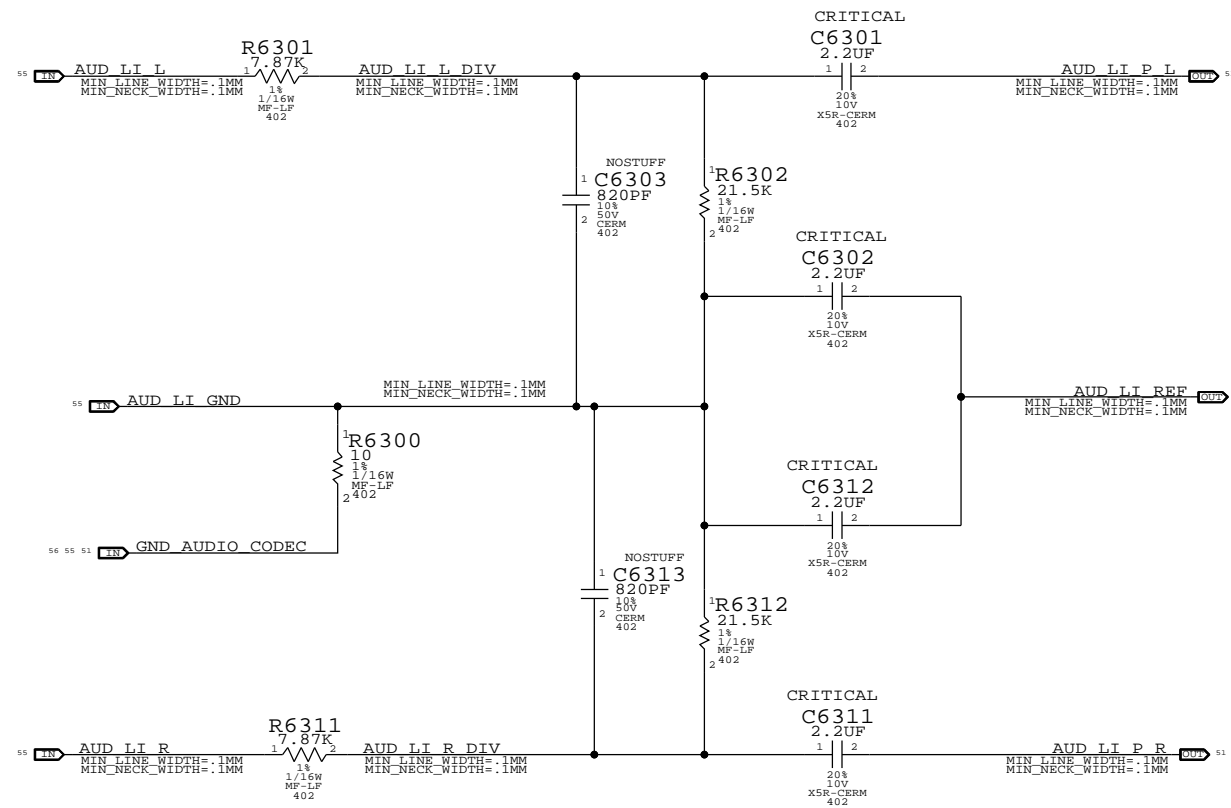



NOTES ON CODEC I/O
 DIFF FSINPUT= 2.45VRMS
 SE FSINPUT= 1.22VRMS
 DAC1 FSOUTPUT= 1.34VRMS
 DAC2/3 FSOUTPUTDIFF= 2.67VRMS
 DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=AUDIO		SYNC DATE=08/31/2005	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
Apple Inc.		DRAWING NUMBER	051-8563
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		PAGE	62 OF 109
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LINE INPUT VOLTAGE DIVIDER

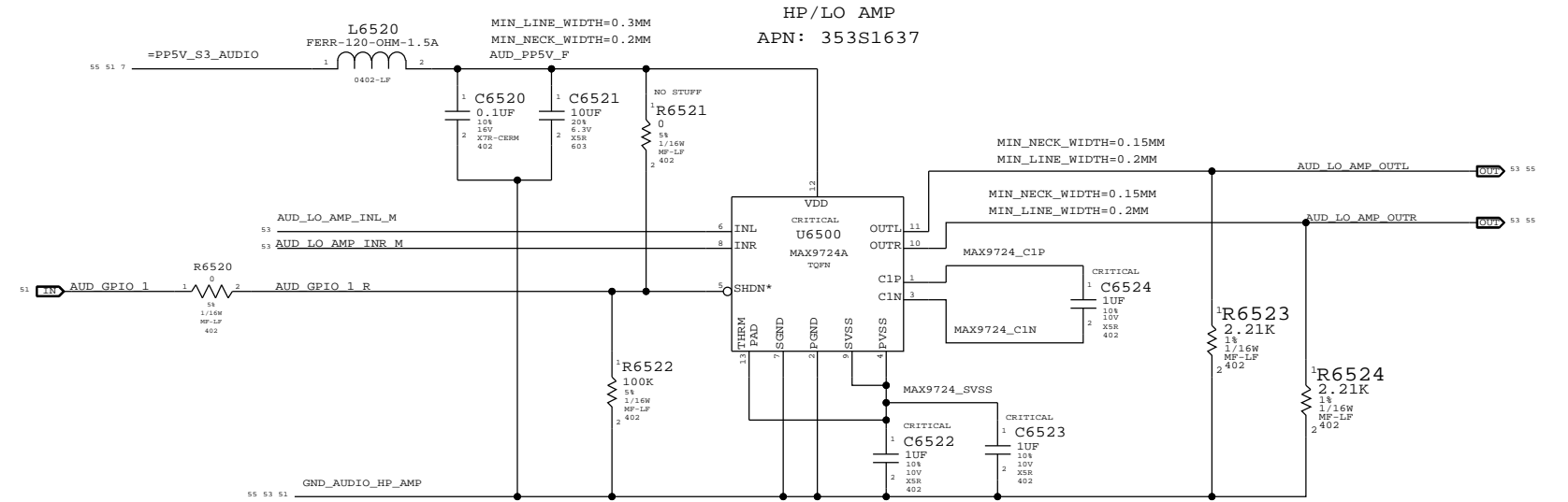
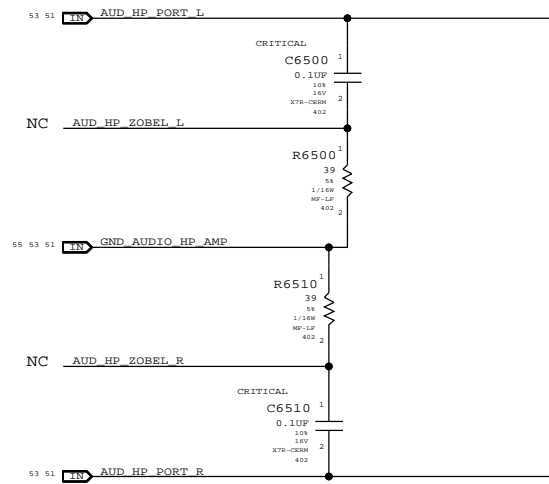
CODEC RIN = 20K OHMS
 NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
 FC_HP = 3.6 HZ
 FC_LP = 43KHZ
 VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE AUDIO: LINE INPUT FILTER		
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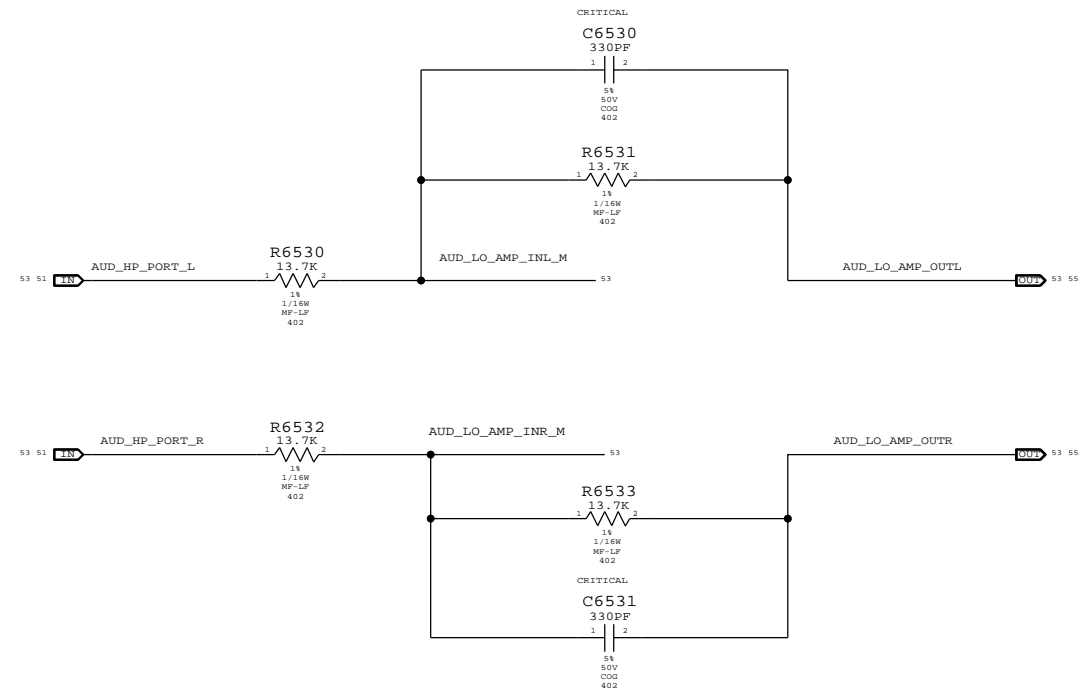
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ

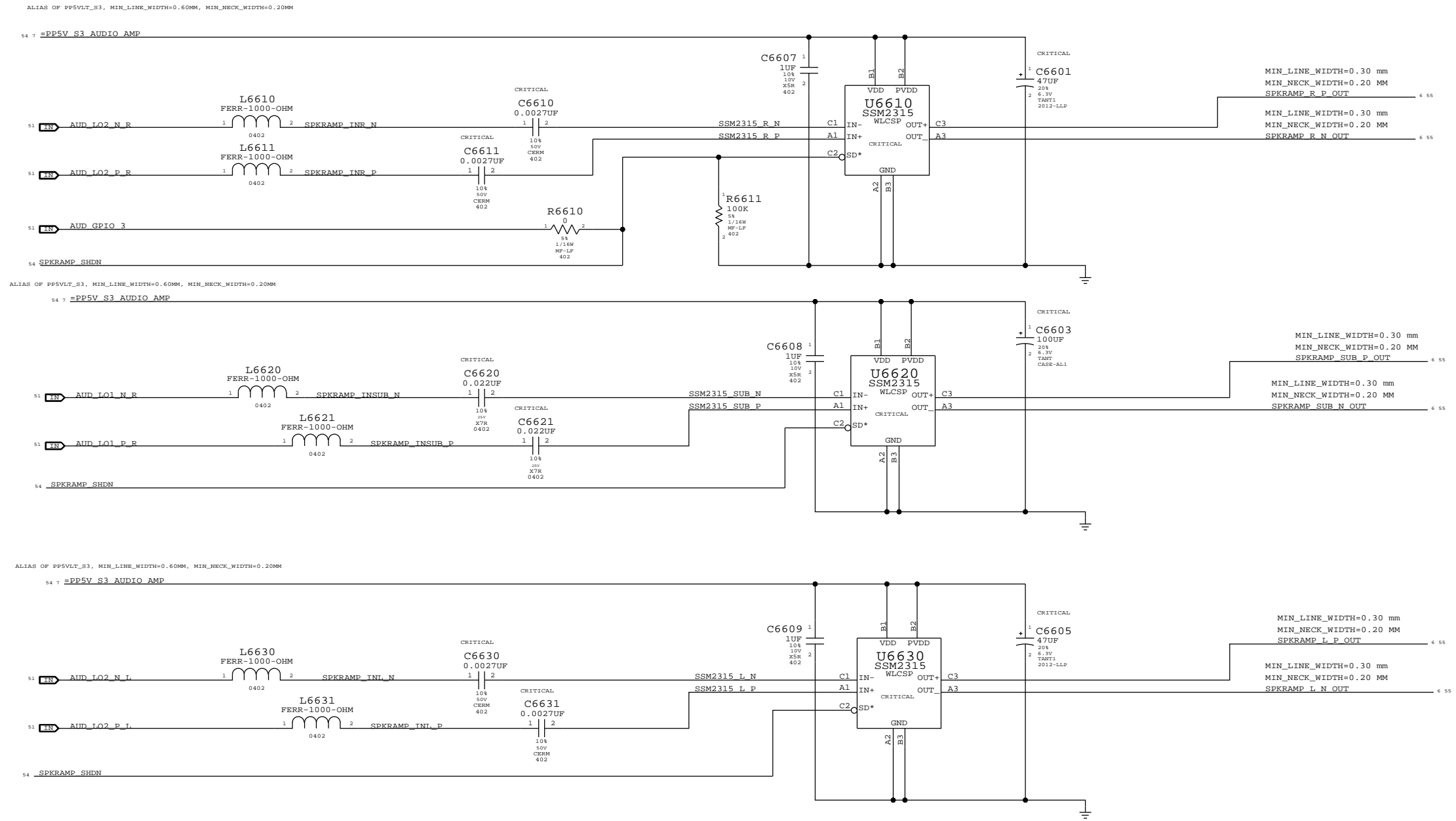



SYNC MASTER=AUDIO		SYNC DATE=07/17/2005	
PAGE TITLE AUDIO: HEADPHONE FILTER			
DRAWING NUMBER 051-8563		SIZE D	
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SATELLITE & SUB TWEETER AMPLIFIER

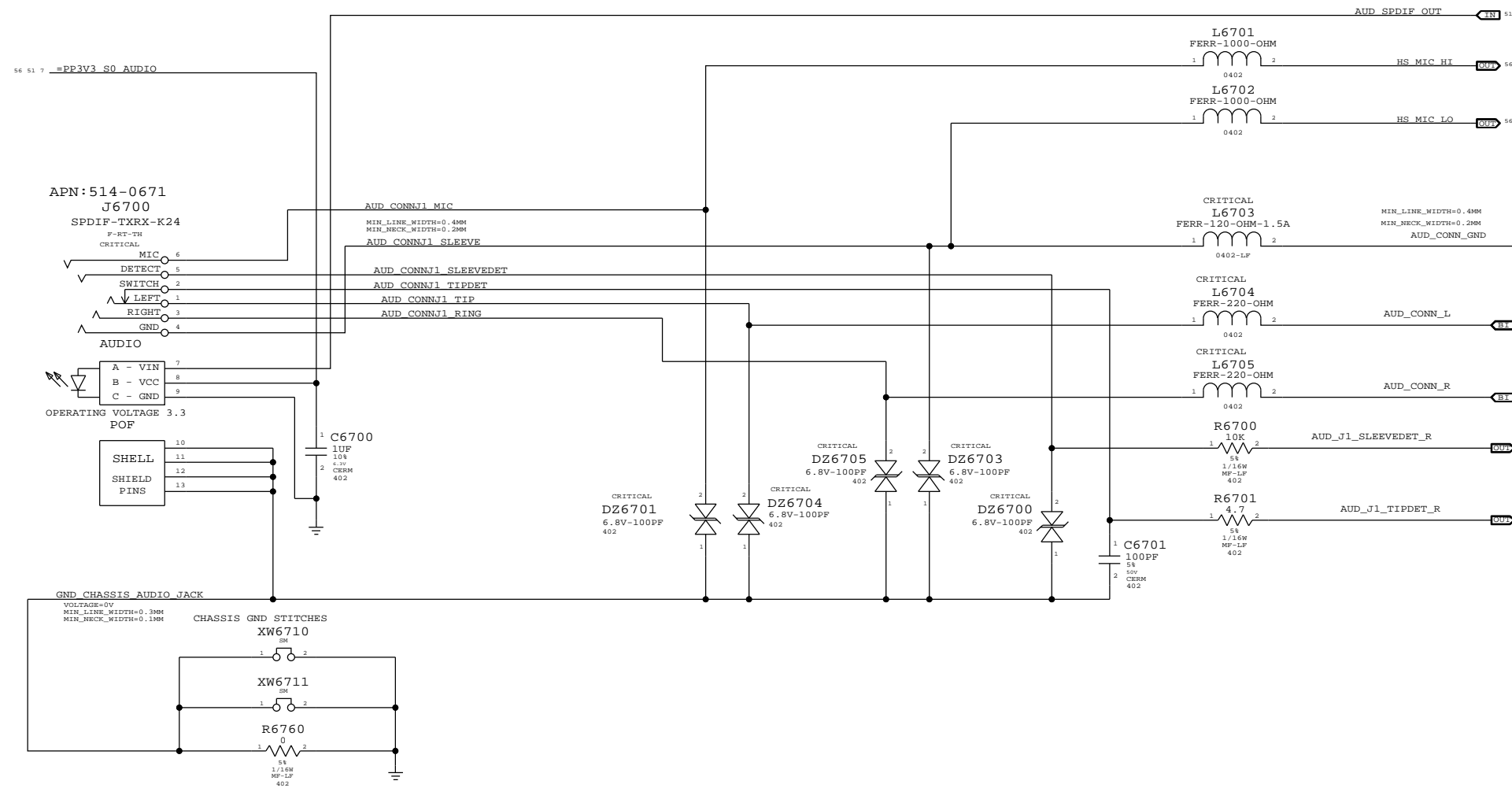
APN:353S2524

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 6DB

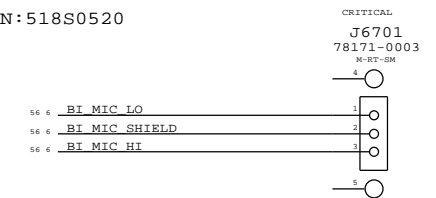


SYNC MASTER=AUDIO		SYNC DATE=07/17/2005	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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	REVISION	A.13.0	
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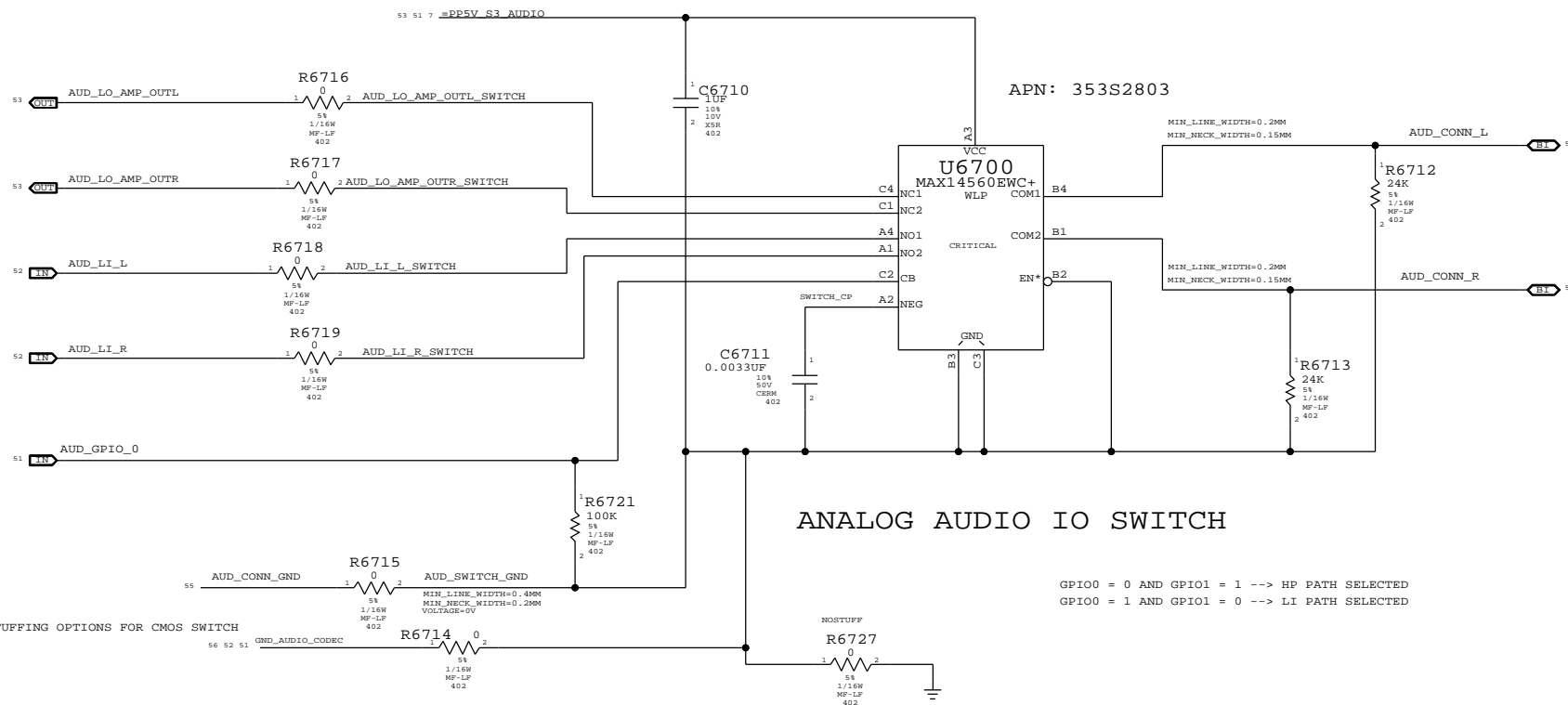
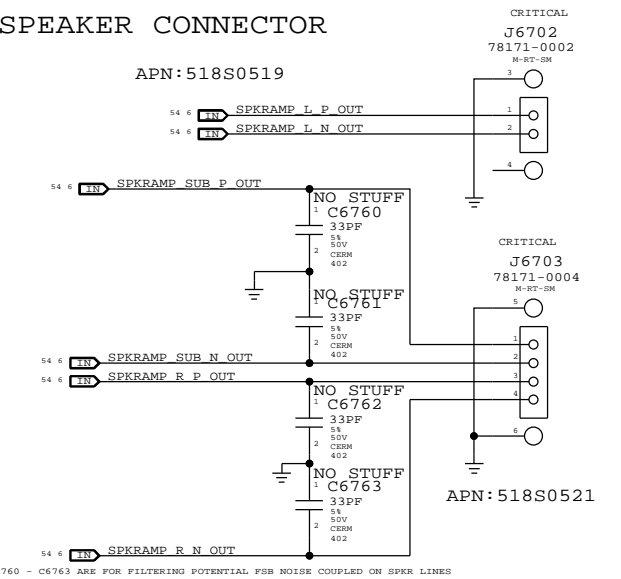
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



MIC CONNECTOR
APN: 518S0520



SPEAKER CONNECTOR



ANALOG AUDIO IO SWITCH

SYNC MASTER=AUDIO		SYNC DATE=08/25/2009	
PAGE TITLE			
AUDIO: JACK		DRAWING NUMBER	SIZE
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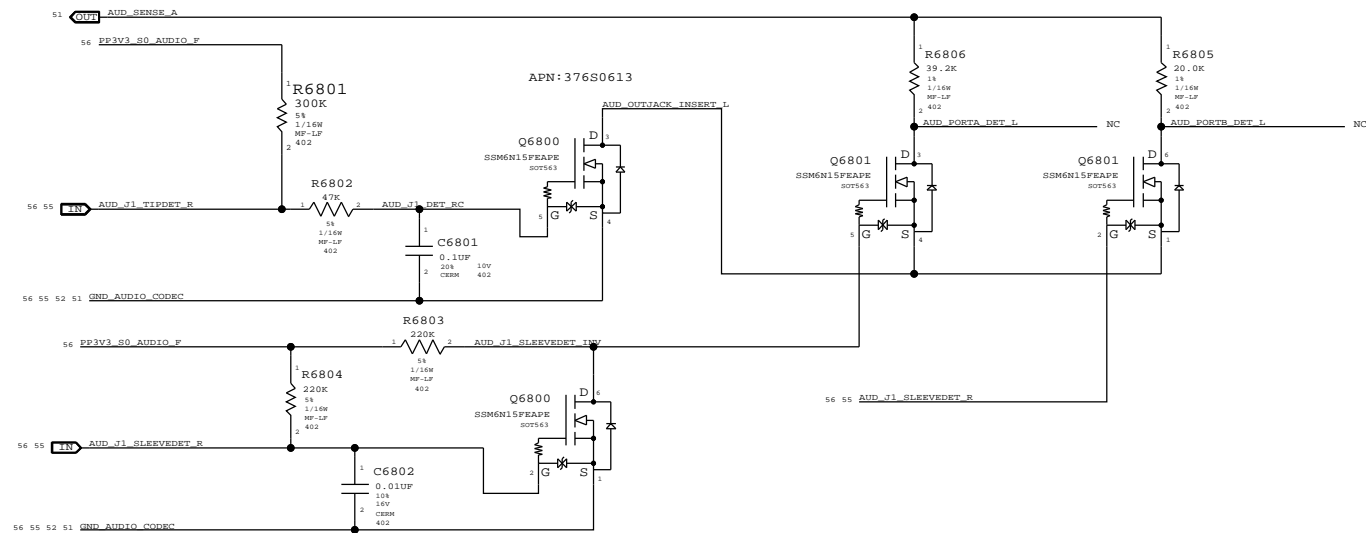
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	OX02 (2)	OX02 (2)	OX09 (9,A)	GPIO_0 AND GPIO_1	OX09 (A)
LINE IN	OX05 (5)	OX05 (5)	OX0C (12)	GPIO_0 AND GPIO_1	OX09 (A) AND UI ELEMENT
SATELLITES	OX04 (4)	OX04 (4)	OX0B (11)	GPIO_3	N/A
SUB	OX03 (3)	OX03 (3)	OX0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	OX08 (8)	OX10 (16)	N/A	OX0D (B)

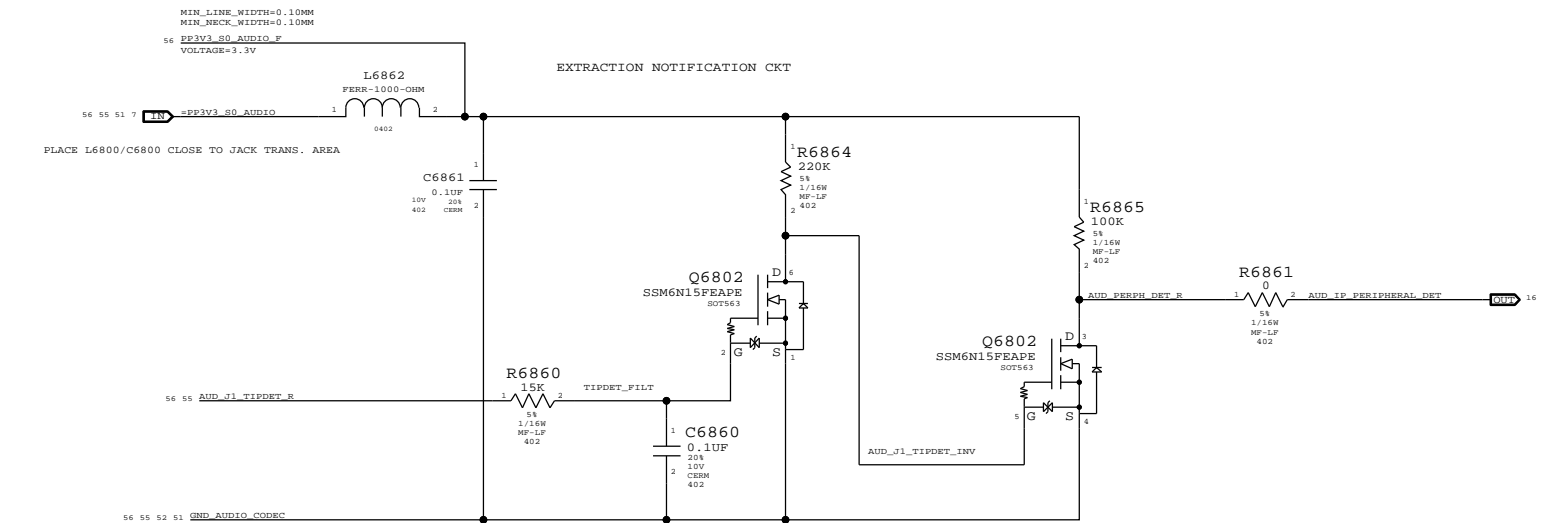
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	OX06 (6)	OX0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	OX06 (6)	OX0D (13,V22,B,LEFT)	MIKEY	MIKEY

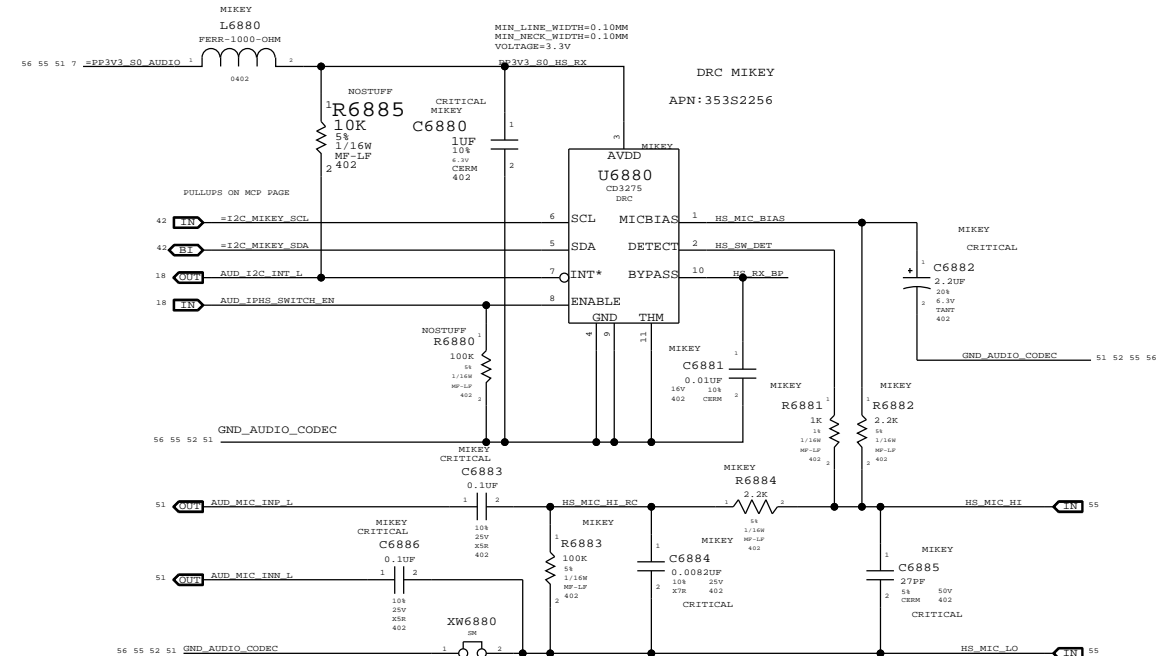
PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)



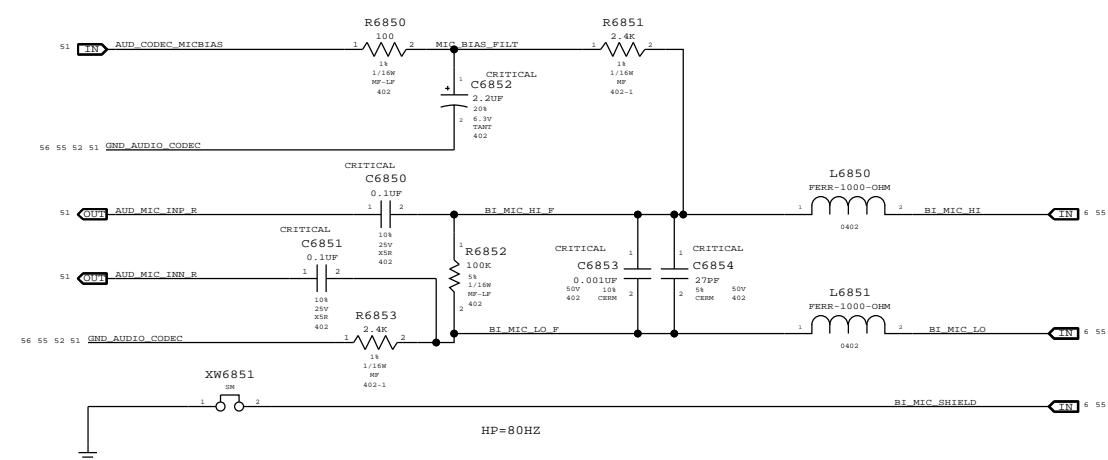
EXTRACTION NOTIFICATION CKT



PORT B LEFT (HEADSET MIC) HP=80HZ, LP=8.82KHZ



PORT B RIGHT (BUILT-IN MIC)



SYNC MASTER=AUDIO SYNC DATE=08/27/2005

PAGE TITLE: AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

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PAGE: 68 OF 109 SHEET: 56 OF 80

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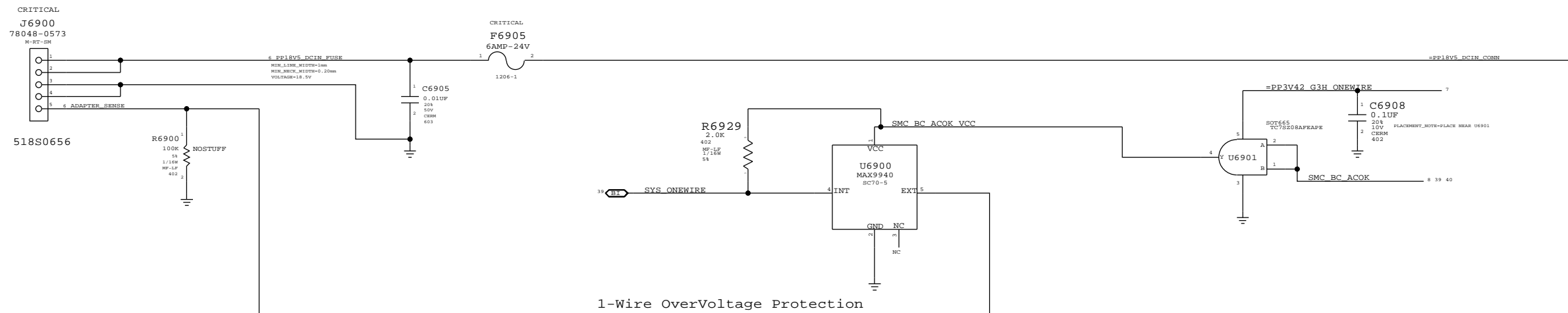
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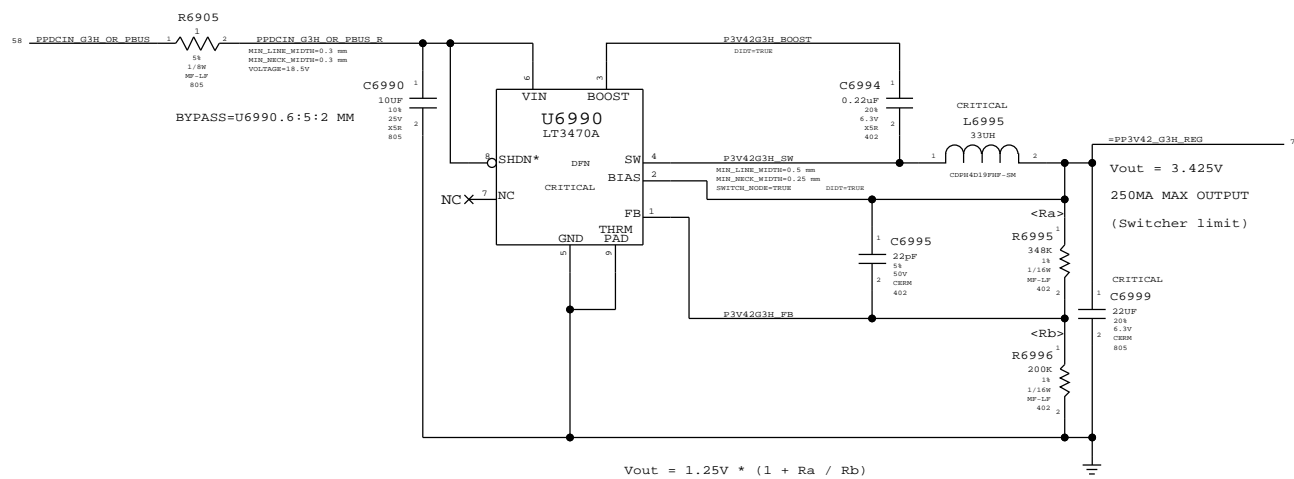
1

MagSafe DC Power Jack

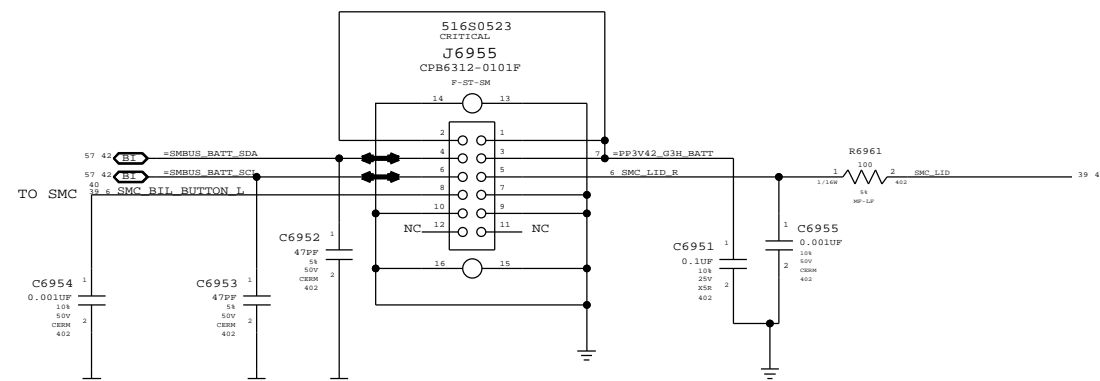


3.425V "G3Hot" Supply

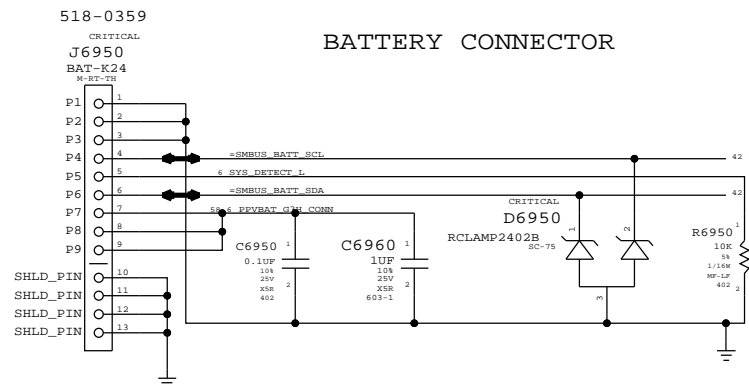
Supply needs to guarantee 3.31V delivered to SMC Vref generator



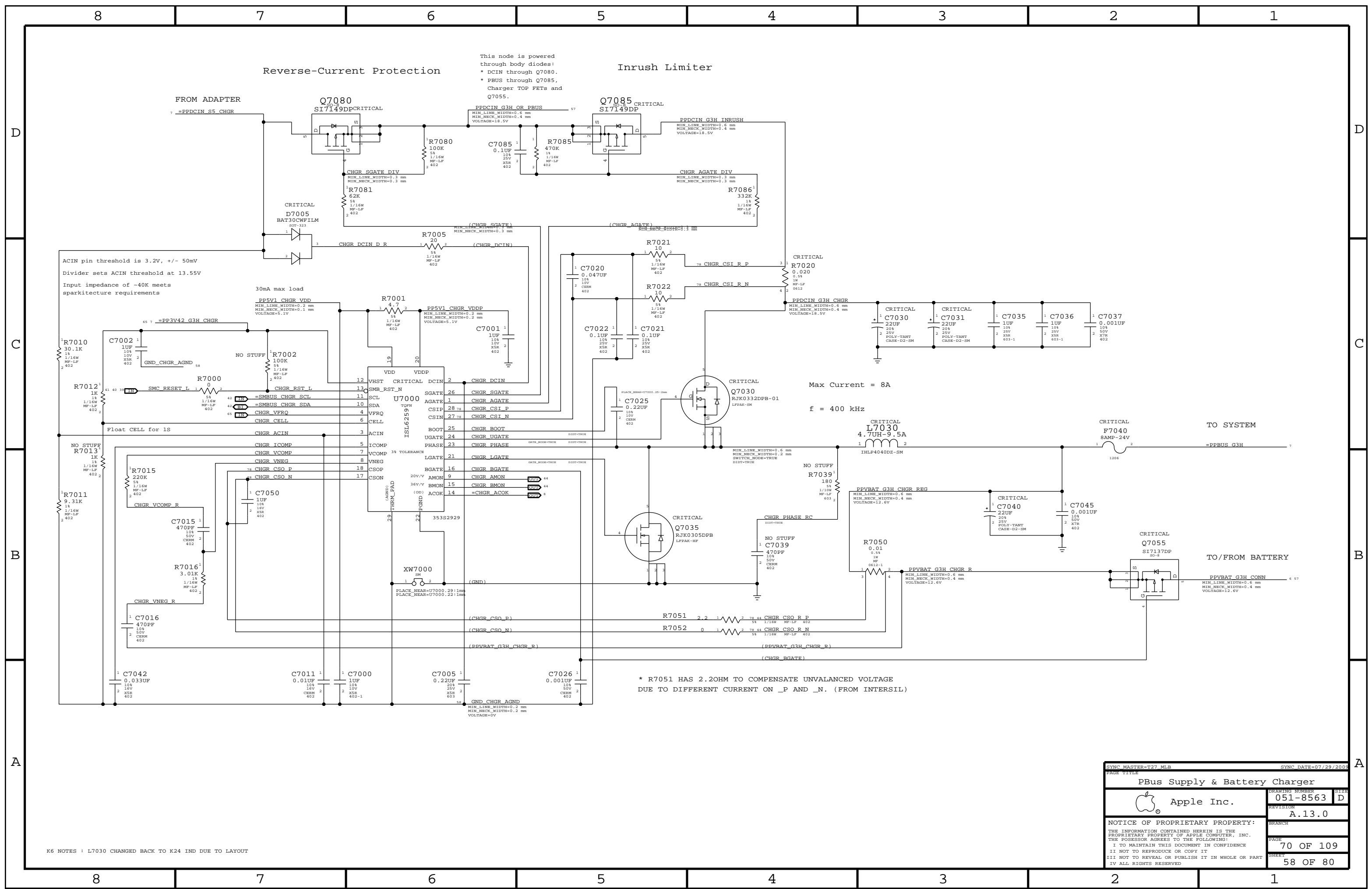
BIL CONNECTOR



BATTERY CONNECTOR



SYNC MASTER=K24_MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
DC-In & Battery Connectors			
DRAWING NUMBER		051-8563	
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This node is powered through body diodes:
 * DCIN through Q7080.
 * PBUS through Q7085, Charger TOP FETs and Q7055.

Reverse-Current Protection

Inrush Limiter

ACIN pin threshold is 3.2V, +/- 50mV
 Divider sets ACIN threshold at 13.55V
 Input impedance of ~40K meets sparkitecture requirements

Max Current = 8A
 f = 400 kHz

* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

U7000

12	VHST	CRITICAL	DCIN	2	CHGR DCIN
13	SMB_RST_N			26	CHGR SGATE
10	SDA		10	AGATE	1
11	SCL		28	CHGR CSI_P	78
4	VFRQ		27	CHGR CSI_N	78
6	CELL		25	CHGR BOOT	
3	ACIN		24	CHGR UGATE	
5	ICOMP		23	CHGR PHASE	
7	VCOMP		21	CHGR LGATE	
8	VNEG		16	CHGR BGATE	
18	CSOP		9	CHGR AMON	44
17	CSON		15	CHGR BMON	44
14	ACOK		14	CHGR ACOK	5

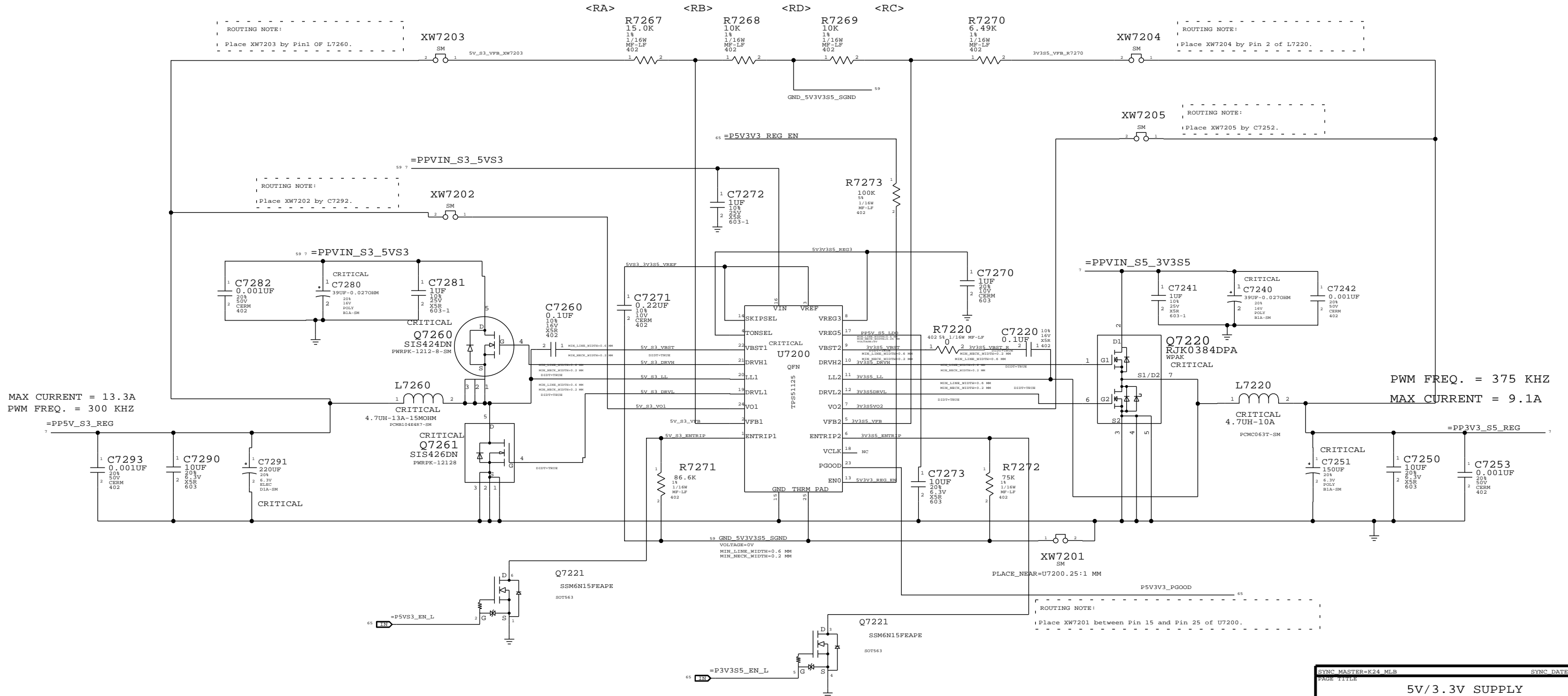
SYNC MASTER=T27_MLB		SYNC DATE=07/29/2005	
PAGE TITLE			
PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	051-8563
		REVISION	A.13.0
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K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



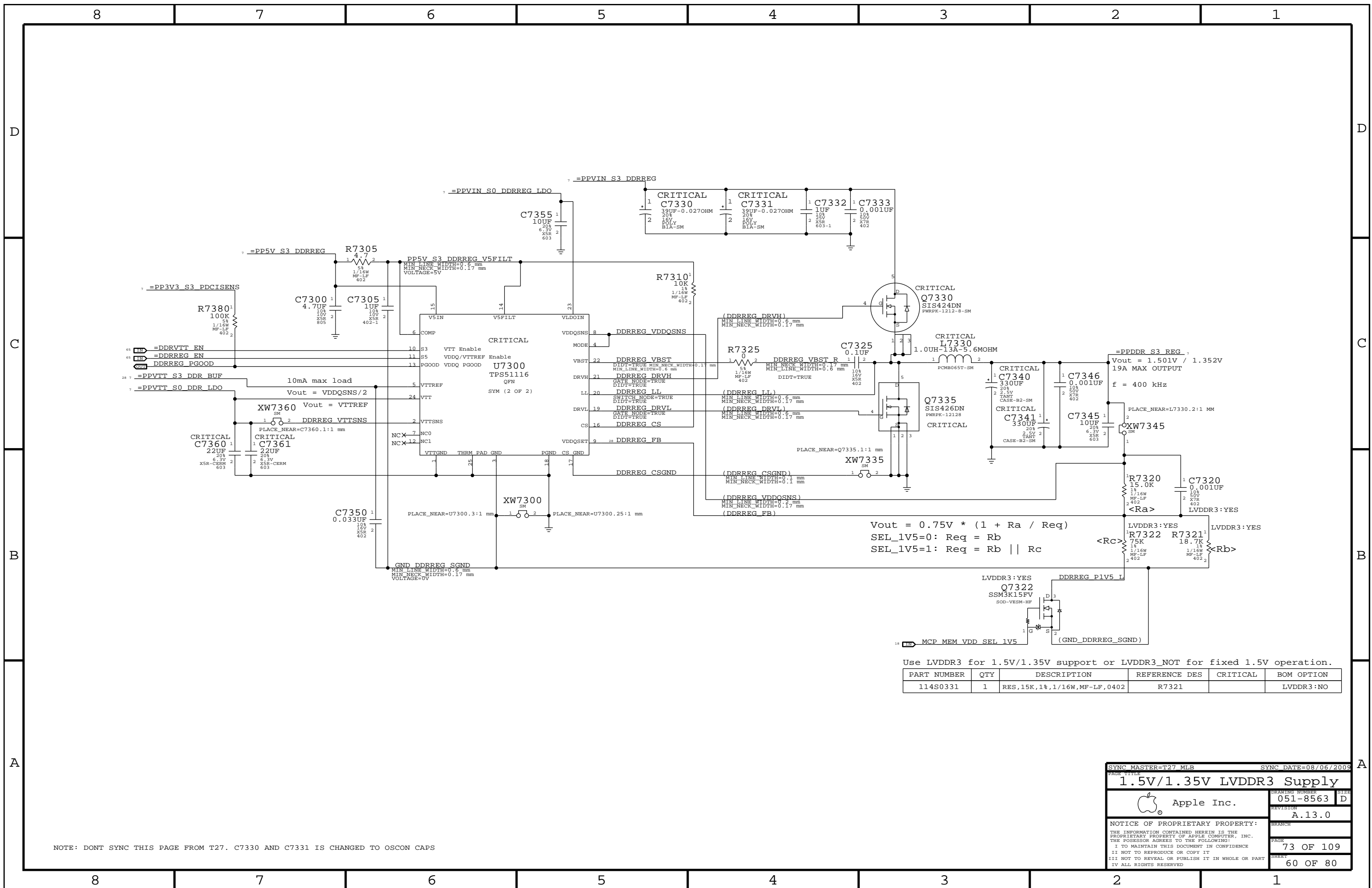
MAX CURRENT = 13.3A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 9.1A

NOTE: DONT SYNC THIS PAGE FROM T27

SYNC MASTER=K24_MLB		SYNC DATE=07/20/2005	
PAGE TITLE 5V/3.3V SUPPLY			
DRAWING NUMBER 051-8563		SIZE D	
REVISION A.13.0		BRANCH	
PAGE 72 OF 109		SHEET 59 OF 80	
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SEPARATED MASTER POOD FOR BOTH 5V AND 3V3.



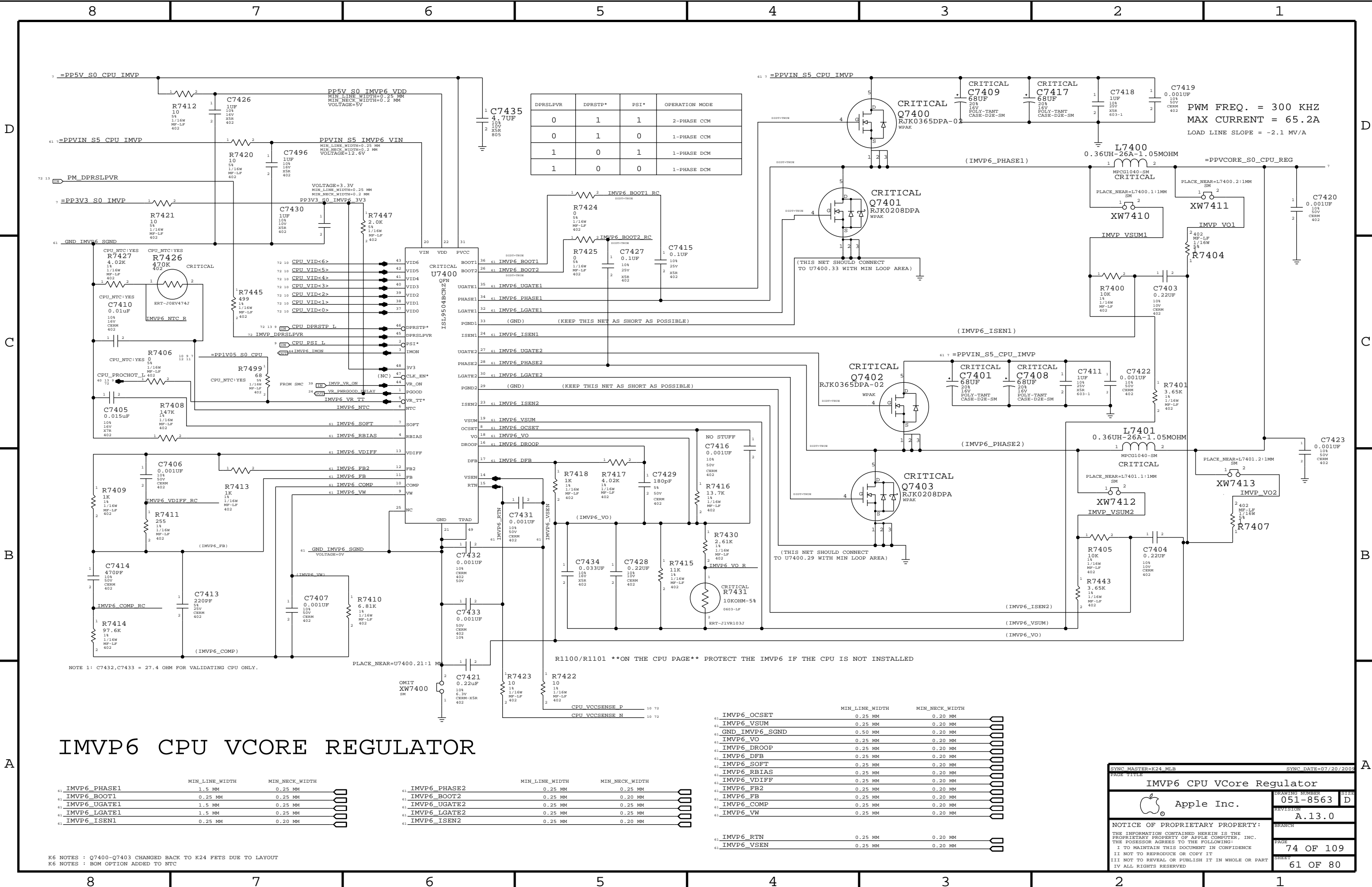
$V_{out} = 0.75V * (1 + R_a / R_{eq})$
 SEL_1V5=0: $R_{eq} = R_b$
 SEL_1V5=1: $R_{eq} = R_b || R_c$

Use LVDDR3 for 1.5V/1.35V support or LVDDR3_NOT for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS

SYNC MASTER=T27 MLB SYNC DATE=08/06/2009
1.5V/1.35V LVDDR3 Supply
 Apple Inc.
 DRAWING NUMBER: 051-8563 SIZE: D
 REVISION: A.13.0
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DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

IMVP6 CPU VCore Regulator

Pin	MIN_LINE_WIDTH	MIN_NECK_WIDTH
61 IMVP6_PHASE1	1.5 MM	0.25 MM
61 IMVP6_BOOT1	0.25 MM	0.25 MM
61 IMVP6_UGATE1	1.5 MM	0.25 MM
61 IMVP6_LGATE1	1.5 MM	0.25 MM
61 IMVP6_ISEN1	0.25 MM	0.20 MM

Pin	MIN_LINE_WIDTH	MIN_NECK_WIDTH
61 IMVP6_PHASE2	0.25 MM	0.25 MM
61 IMVP6_BOOT2	0.25 MM	0.20 MM
61 IMVP6_UGATE2	0.25 MM	0.25 MM
61 IMVP6_LGATE2	0.25 MM	0.25 MM
61 IMVP6_ISEN2	0.25 MM	0.20 MM

Pin	MIN_LINE_WIDTH	MIN_NECK_WIDTH
61 IMVP6_OCSET	0.25 MM	0.20 MM
61 IMVP6_VSUM	0.25 MM	0.20 MM
61 GND_IMVP6_SGND	0.50 MM	0.20 MM
61 IMVP6_VO	0.25 MM	0.20 MM
61 IMVP6_DROOP	0.25 MM	0.20 MM
61 IMVP6_DFB	0.25 MM	0.20 MM
61 IMVP6_SOFT	0.25 MM	0.20 MM
61 IMVP6_RBIA5	0.25 MM	0.20 MM
61 IMVP6_VDIFF	0.25 MM	0.20 MM
61 IMVP6_FB2	0.25 MM	0.20 MM
61 IMVP6_FB	0.25 MM	0.20 MM
61 IMVP6_COMP	0.25 MM	0.20 MM
61 IMVP6_VW	0.25 MM	0.20 MM
61 IMVP6_RTIN	0.25 MM	0.20 MM
61 IMVP6_VSEN	0.25 MM	0.20 MM

K6 NOTES : Q7400-Q7403 CHANGED BACK TO K24 FETS DUE TO LAYOUT
 K6 NOTES : BOM OPTION ADDED TO NTC

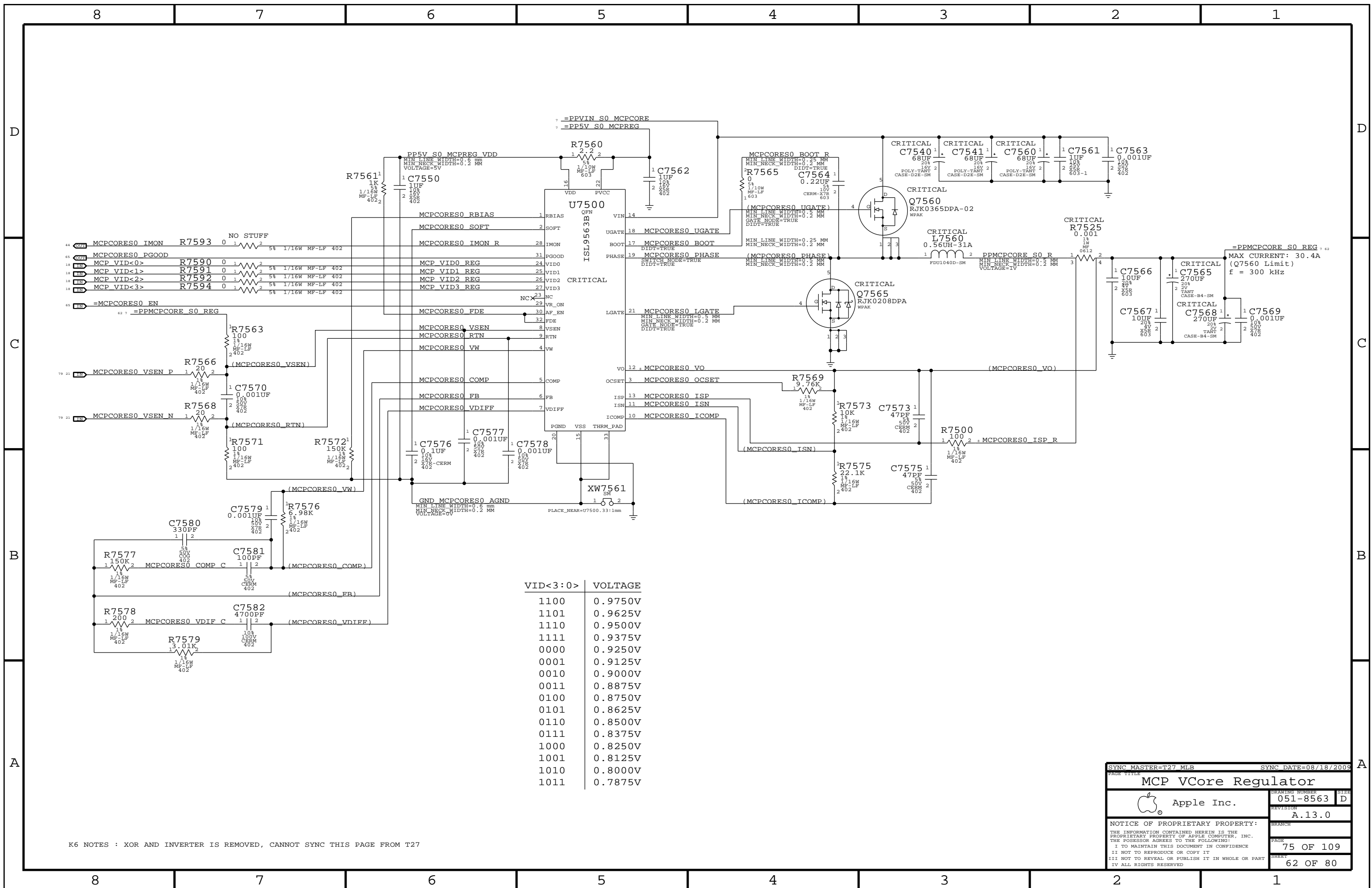
SYNC MASTER=K24_MLB SYNC DATE=07/20/2005
 PAGE 11/11

IMVP6 CPU VCore Regulator

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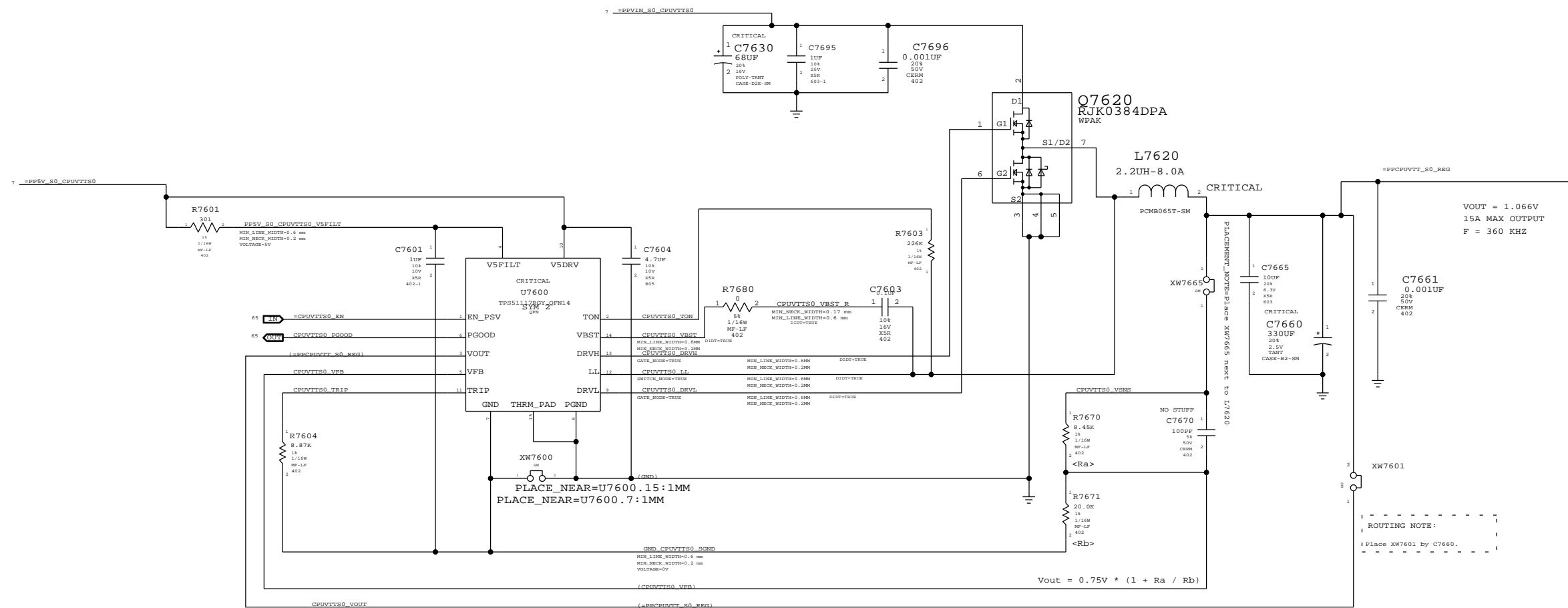
PAGE: 74 OF 109
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K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=T27_MLB		SYNC DATE=08/18/2009	
MCP VCore Regulator			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	75 OF 109
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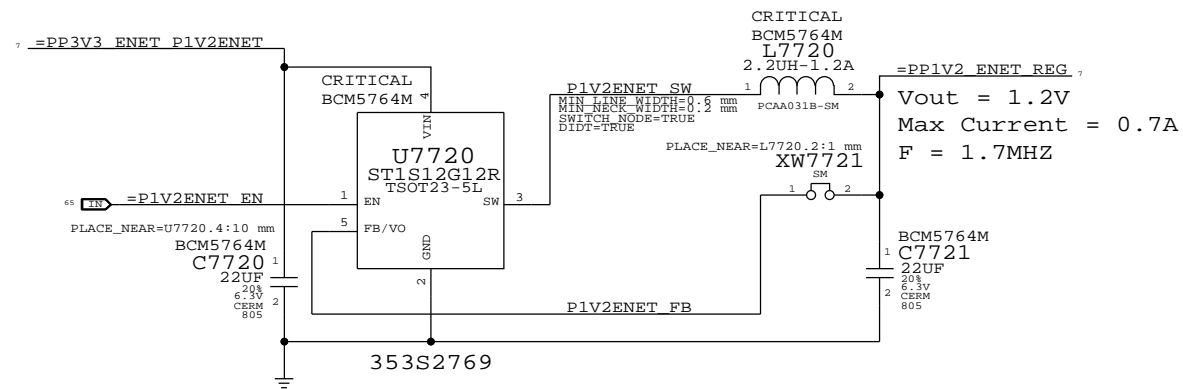
CPUVTT POWER SUPPLY



K6 NOTES : Q7620 CHANGED BACK TO K24 FETS DUE TO LAYOUT

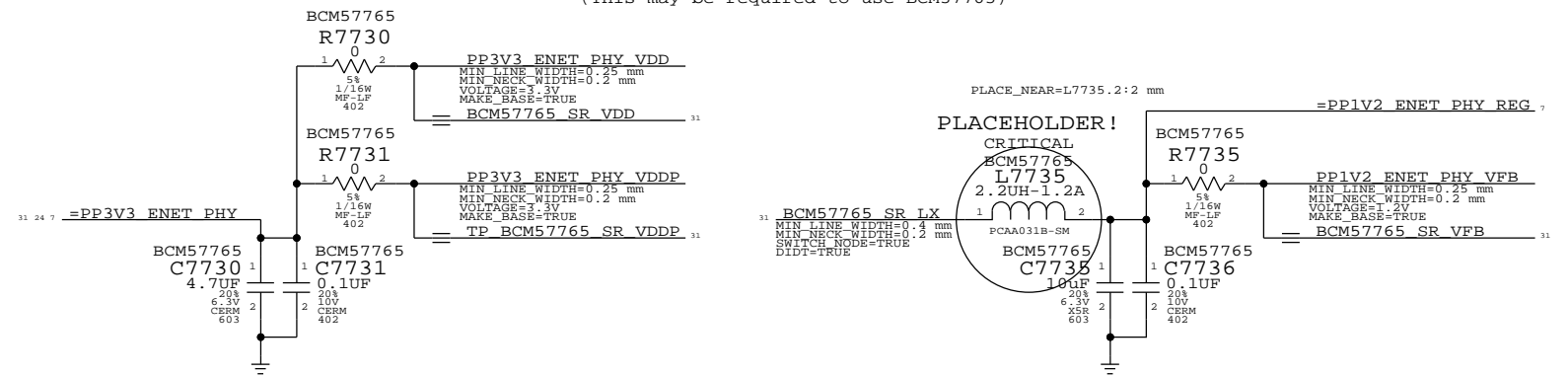
SYNC MASTER=K24_MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
CPU VTT(1.05V) SUPPLY			
DRAWING NUMBER		SIZE	
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1.2V ENET Switcher

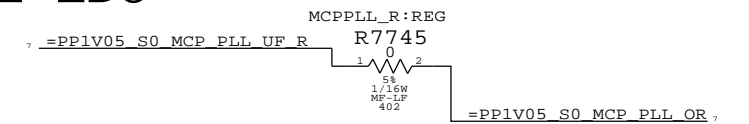


BCM57765 Internal Switcher Support

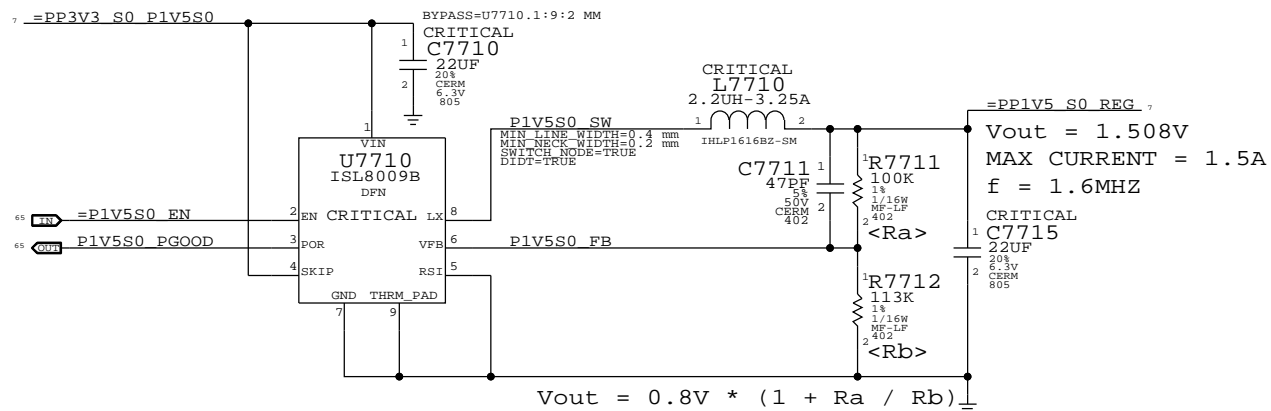
(This may be required to use BCM57765)



1.05V S0 MCP PLL LDO



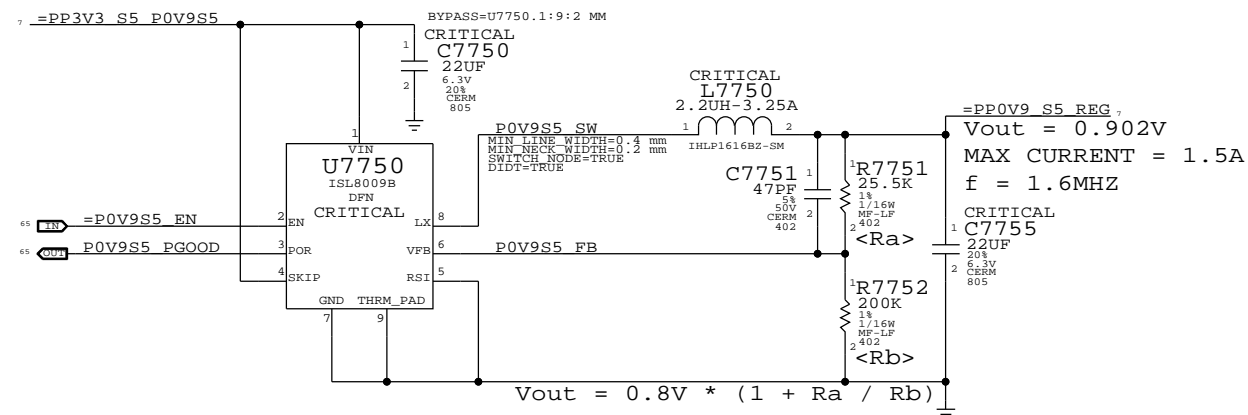
1.5V S0 Regulator



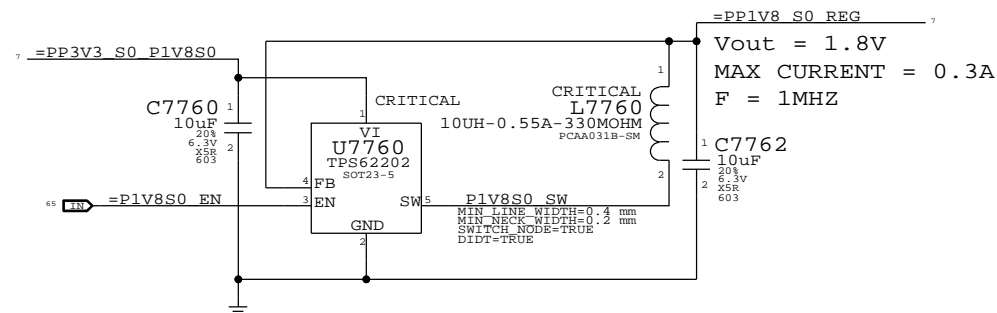
BOMOPTIONS:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
 MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
 TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
 TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



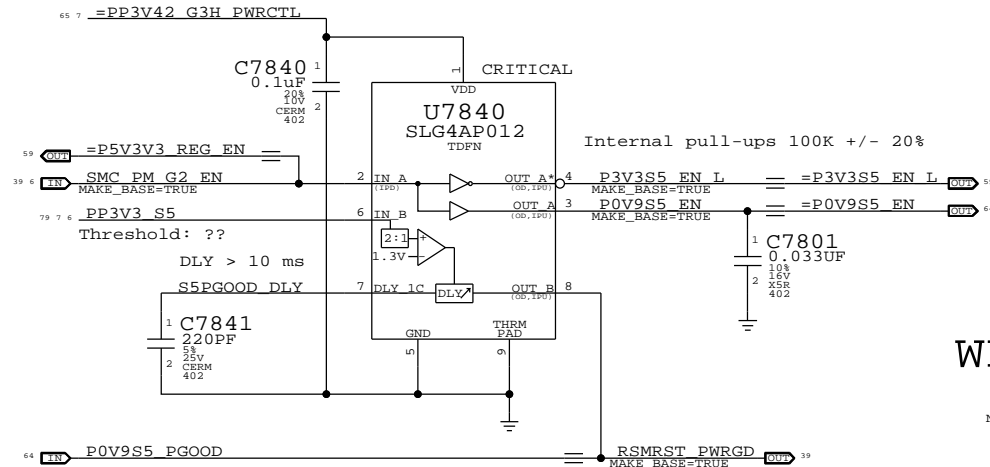
1.8V S0 Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

PAGE TITLE		SYNC DATE=09/30/2009	
Misc Power Supplies			
Apple Inc.		DRAWING NUMBER	051-8563
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		PAGE	77 OF 109
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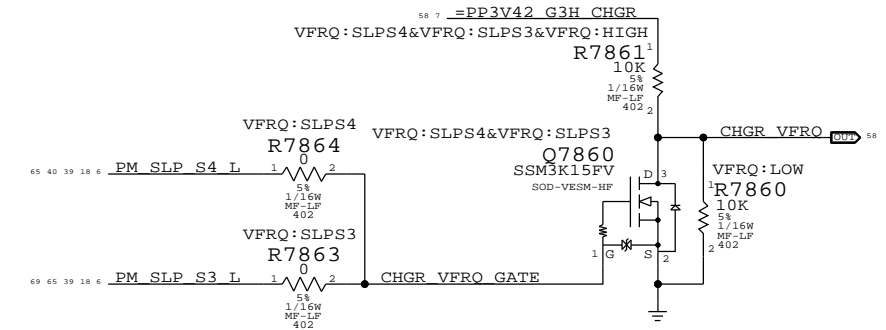
S5 Rail Enables & PGOOD



Power Control Signals

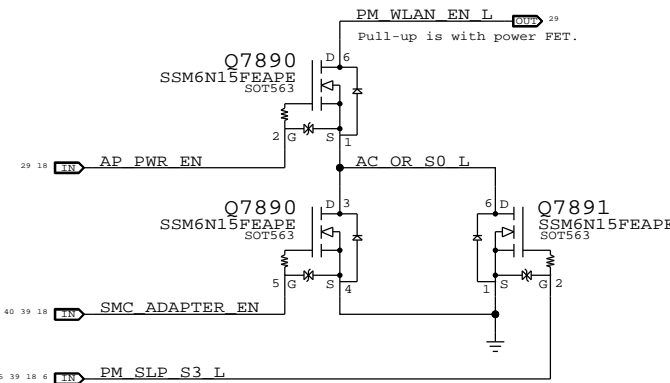
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select

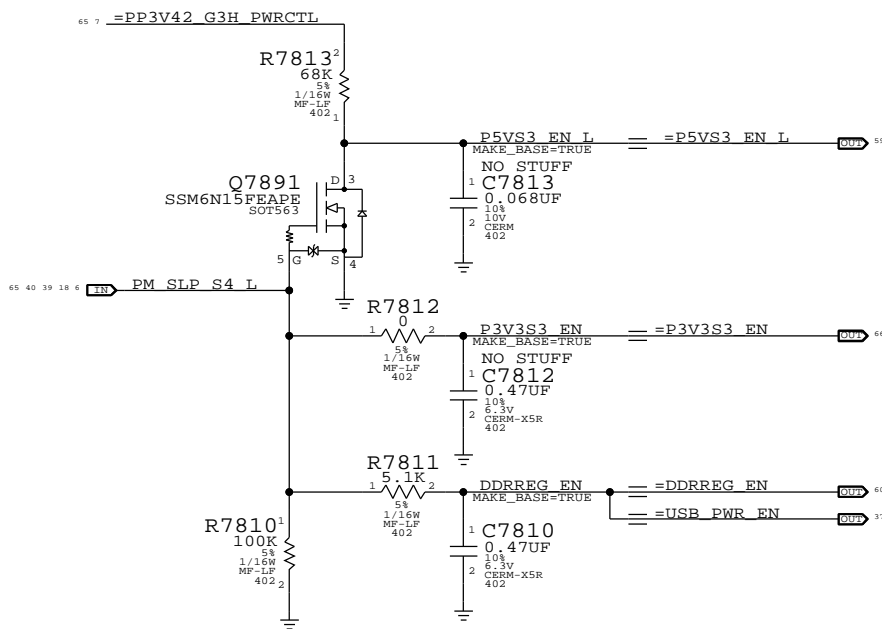


WLAN Enable Generation

WLAN = (*S3* && *AP_PWR_EN* && (*AC* || *S0*))
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

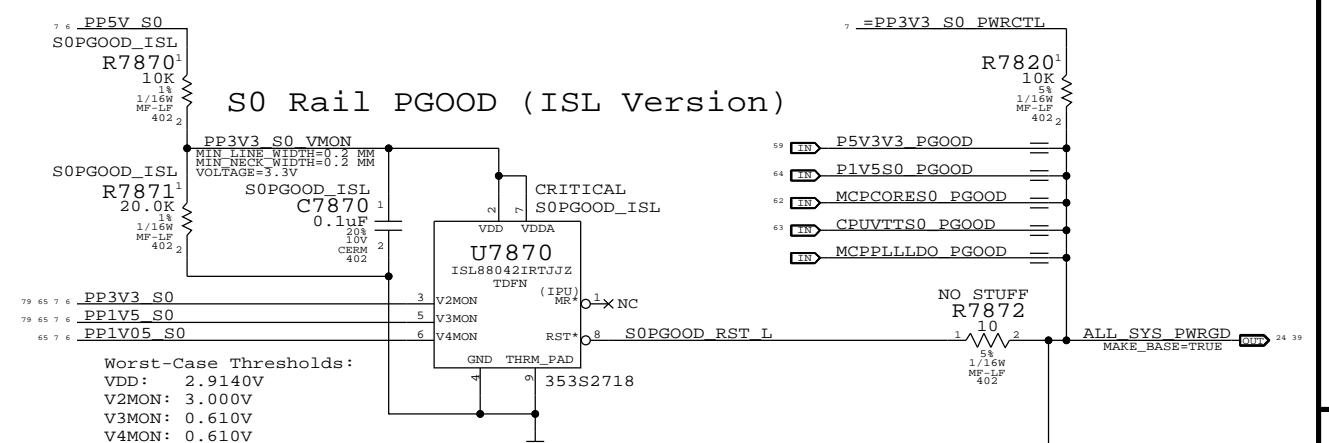


S3 Rail Enables

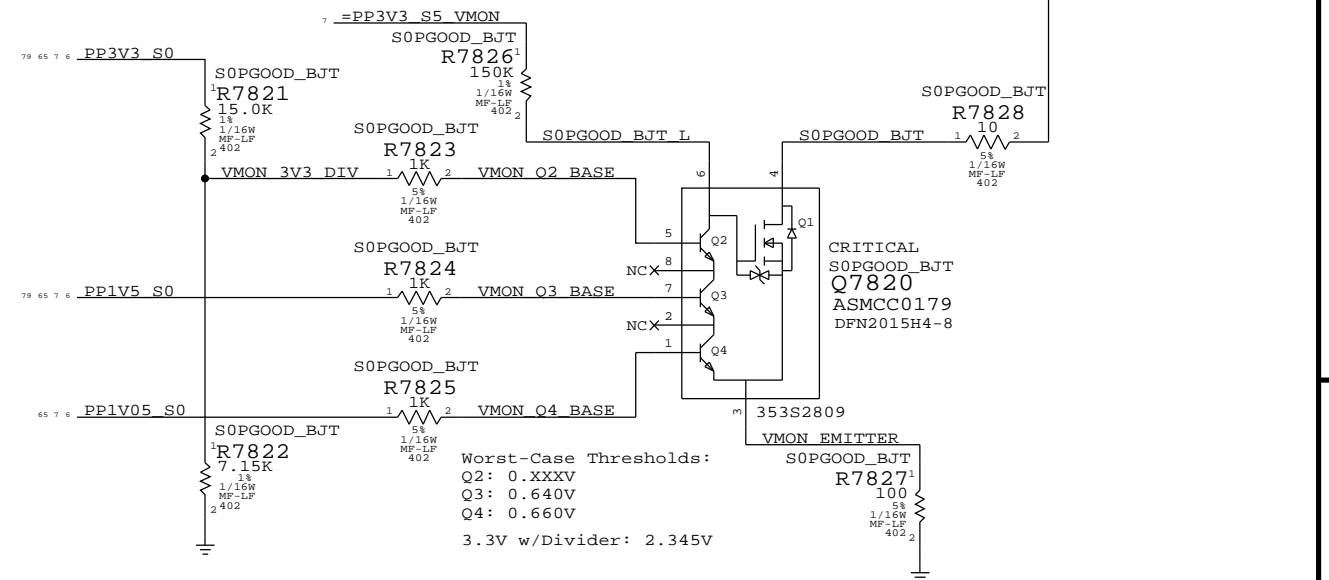


S0 Rail PGOOD Circuitry

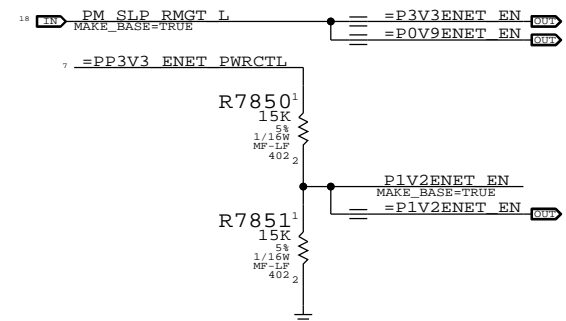
S0 Rail PGOOD (ISL Version)



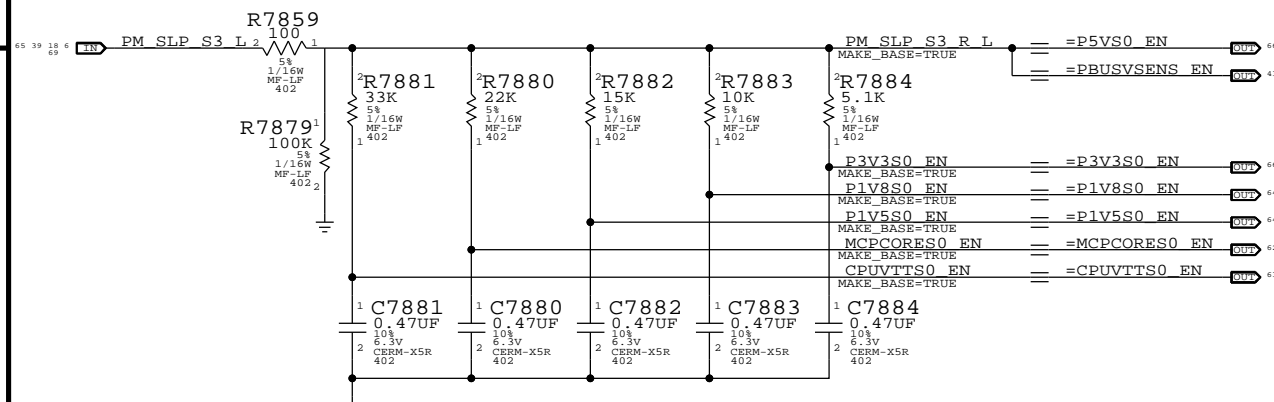
S0 Rail PGOOD (BJT Version)



ENET Rail Enables



S0 Rail Enables



VTT Rail Enable

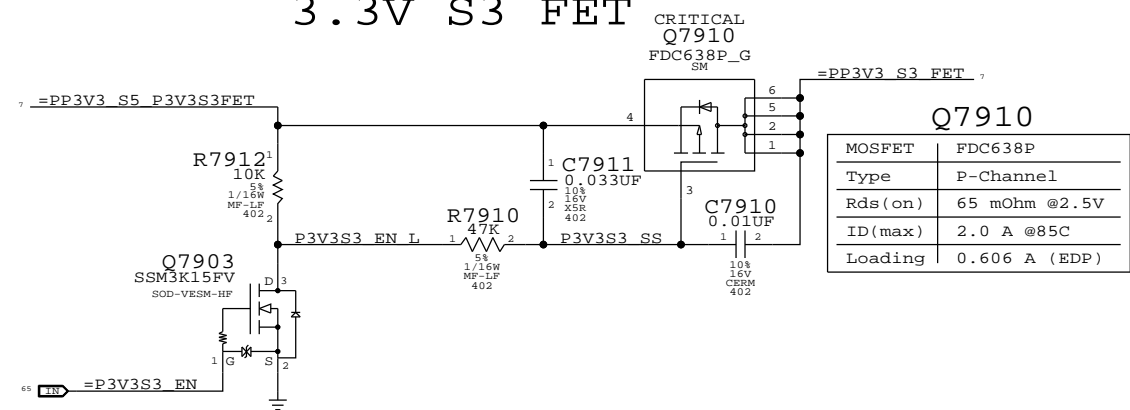
VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).



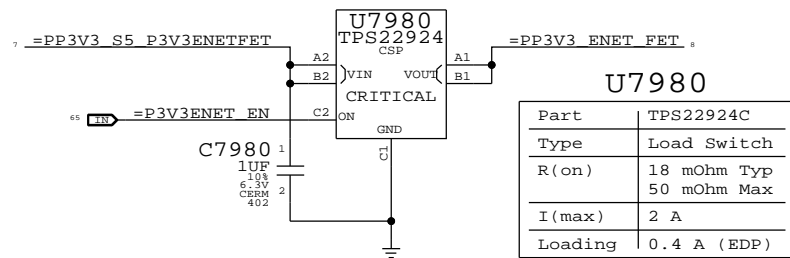
K6 HAS A PULL UP ON DDRREG_PGOOD. REMOVED ALIAS TO TP SIGNAL

SYNC_MASTER=T27_MLB		SYNC_DATE=11/24/2009	
Power Sequencing			
Apple Inc.		DRAWING NUMBER	SIZE
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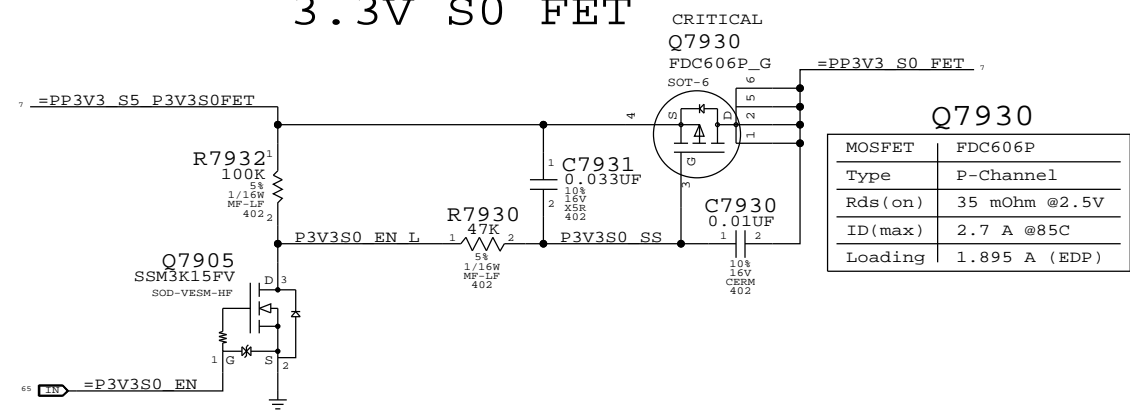
3.3V S3 FET



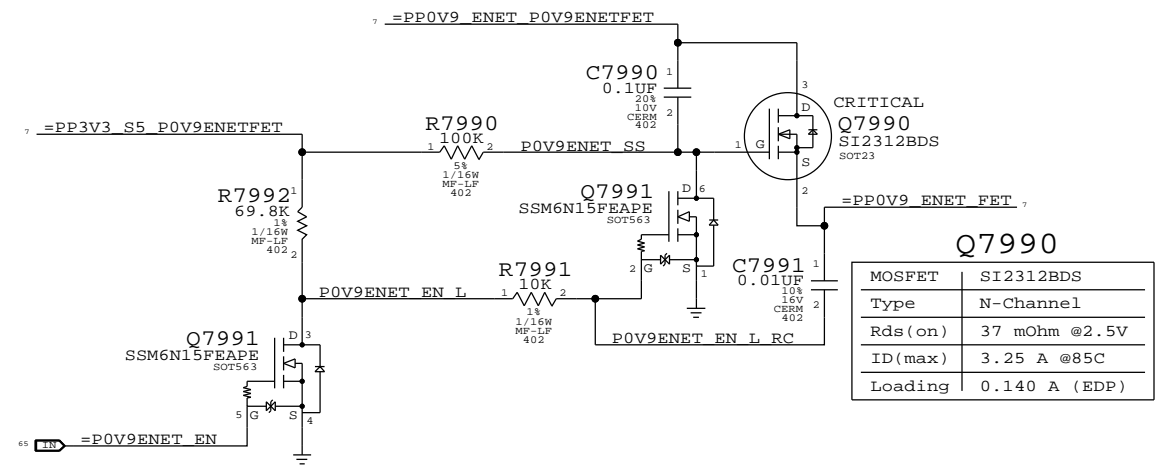
3.3V ENET Switch



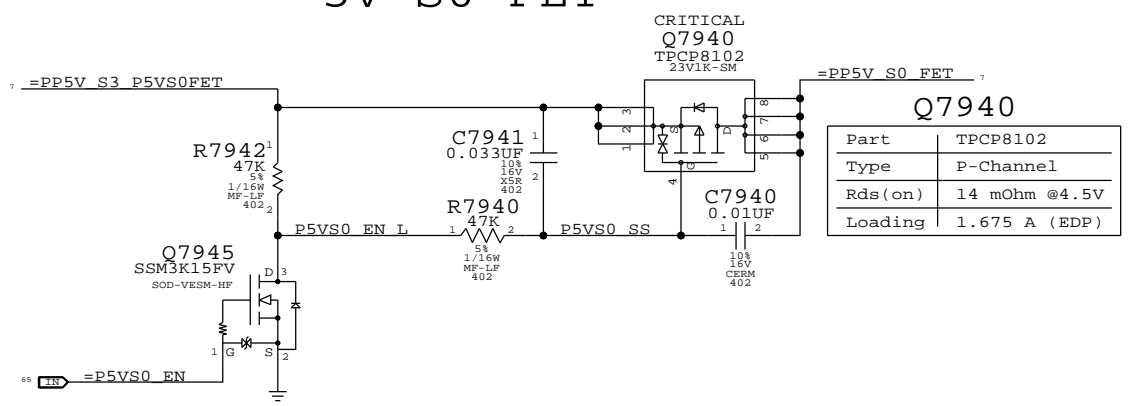
3.3V S0 FET



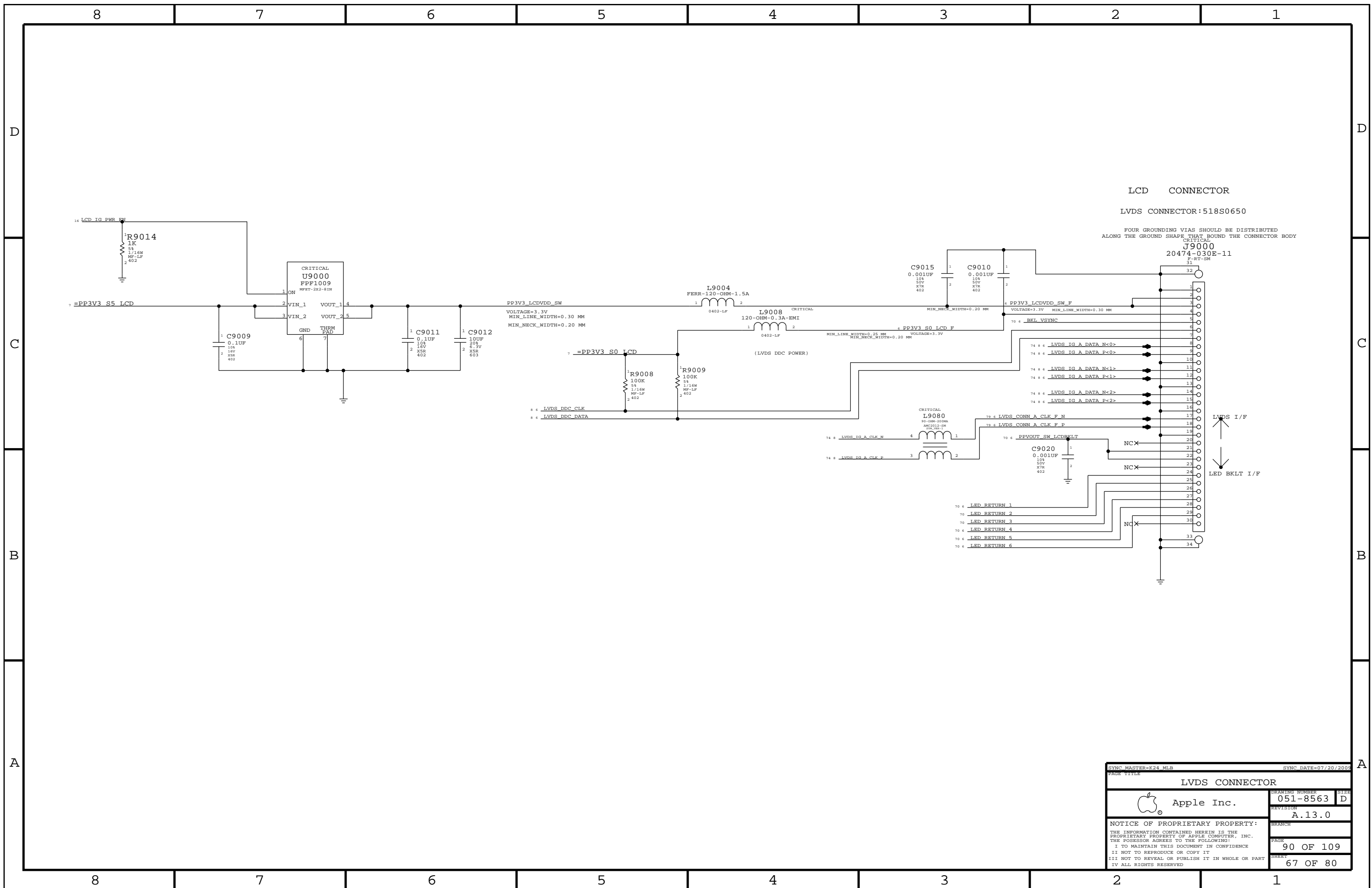
0.9V ENET FET



5V S0 FET



SYNC MASTER=T27 MLB		SYNC DATE=08/27/2009	
PAGE TITLE			
Power FETs			
Apple Inc.	DRAWING NUMBER	051-8563	SIZE
	REVISION	A.13.0	
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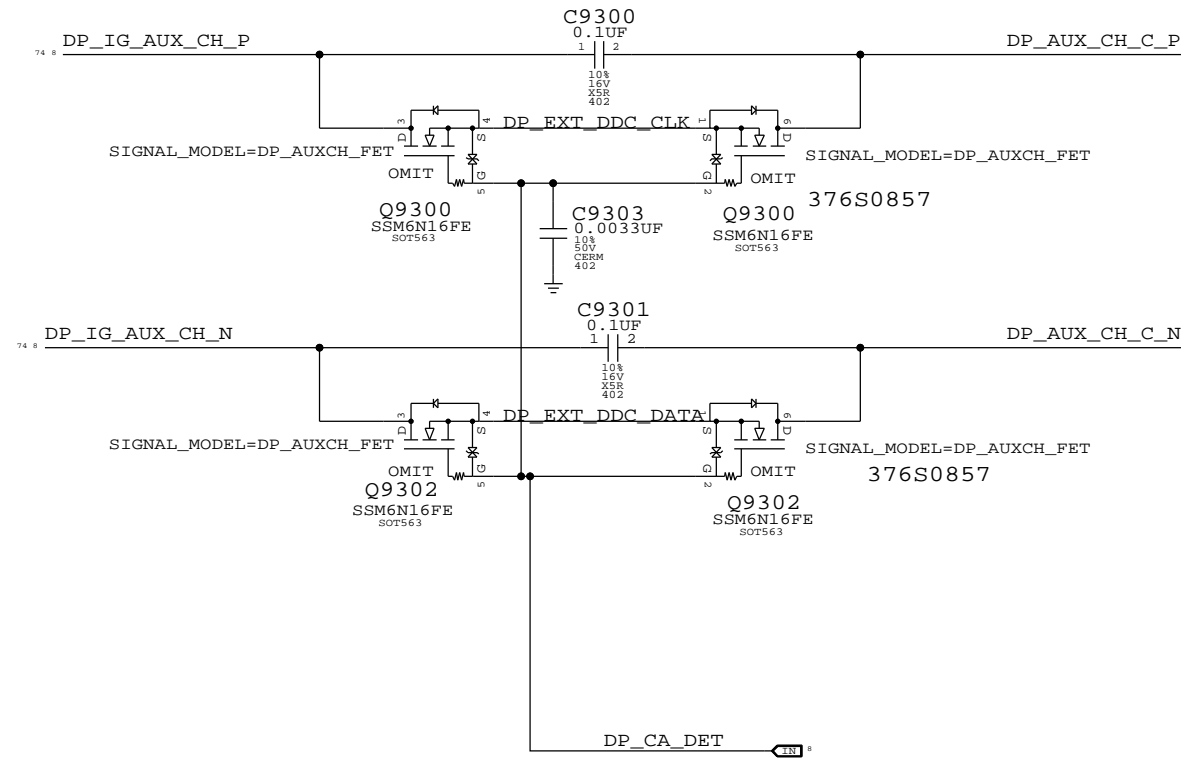
LCD CONNECTOR
LVDS CONNECTOR:518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED
ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

CRITICAL
J9000
20474-030E-11
P-RT-SM

LVDS I/F
LED BKLT I/F

SYNC MASTER=K24 MLB		SYNC DATE=07/20/2005	
PAGE TITLE LVDS CONNECTOR			
DRAWING NUMBER 051-8563		SIZE D	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR, FT, N-CH, DUAL, SOT-563	Q9300, Q9302	CRITICAL	

SYNC MASTER=K69_MLB SYNC DATE=08/12/2009

DISPLAYPORT SUPPORT

Apple Inc.

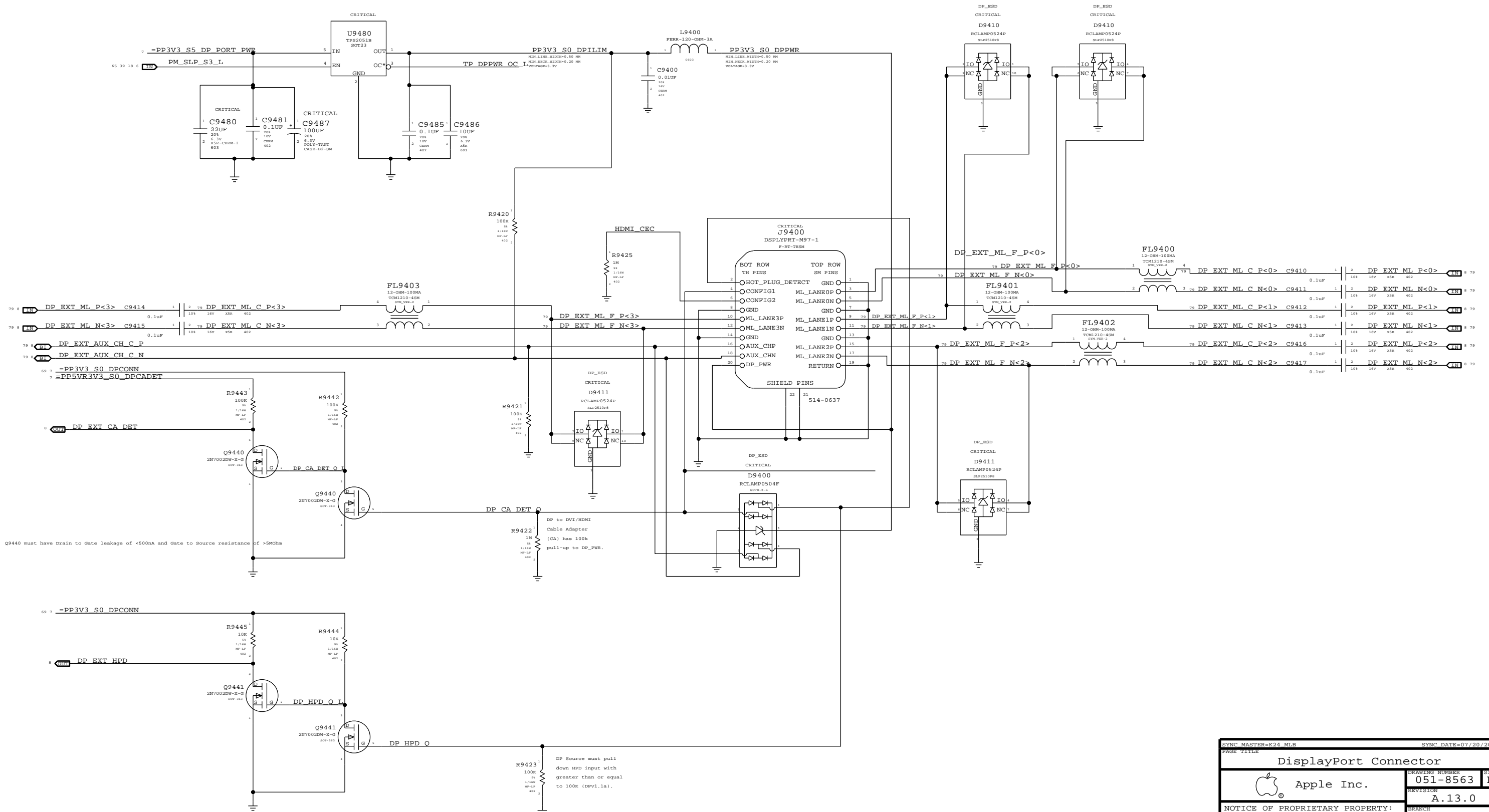
DRAWING NUMBER: 051-8563 SIZE: D

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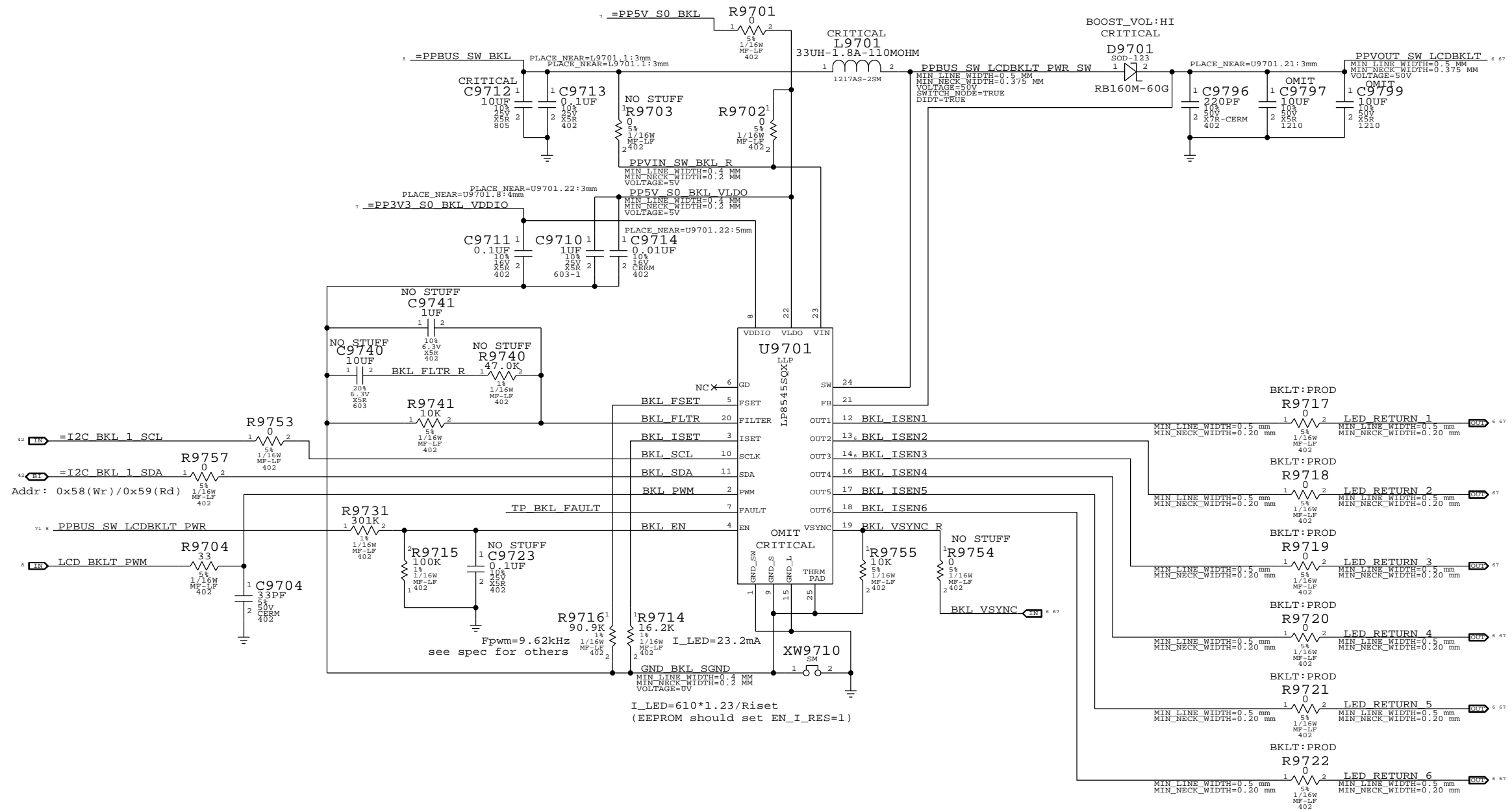
Port Power Switch



R9423 100K
 DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC MASTER=K24_MLB		SYNC DATE=07/20/2009	
PAGE TITLE			
DisplayPort Connector		DRAWING NUMBER	051-8563
Apple Inc.		REVISION	A.13.0
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*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
 *PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
 *LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
 STUFF R9741
 NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FLIM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9720, R9721, R9722		BKLT:ENG
371S0580	1	SCHOTTKY BARRIER DIODE RB160M-40	D9701		BOOST_VOL:LOW
138S0673	2	CAP, 50V, 1210, X5R, 10UF +/-10%	C9797, C9799	CRITICAL	

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K69 MLB SYNC DATE=08/27/2009

LCD Backlight Driver

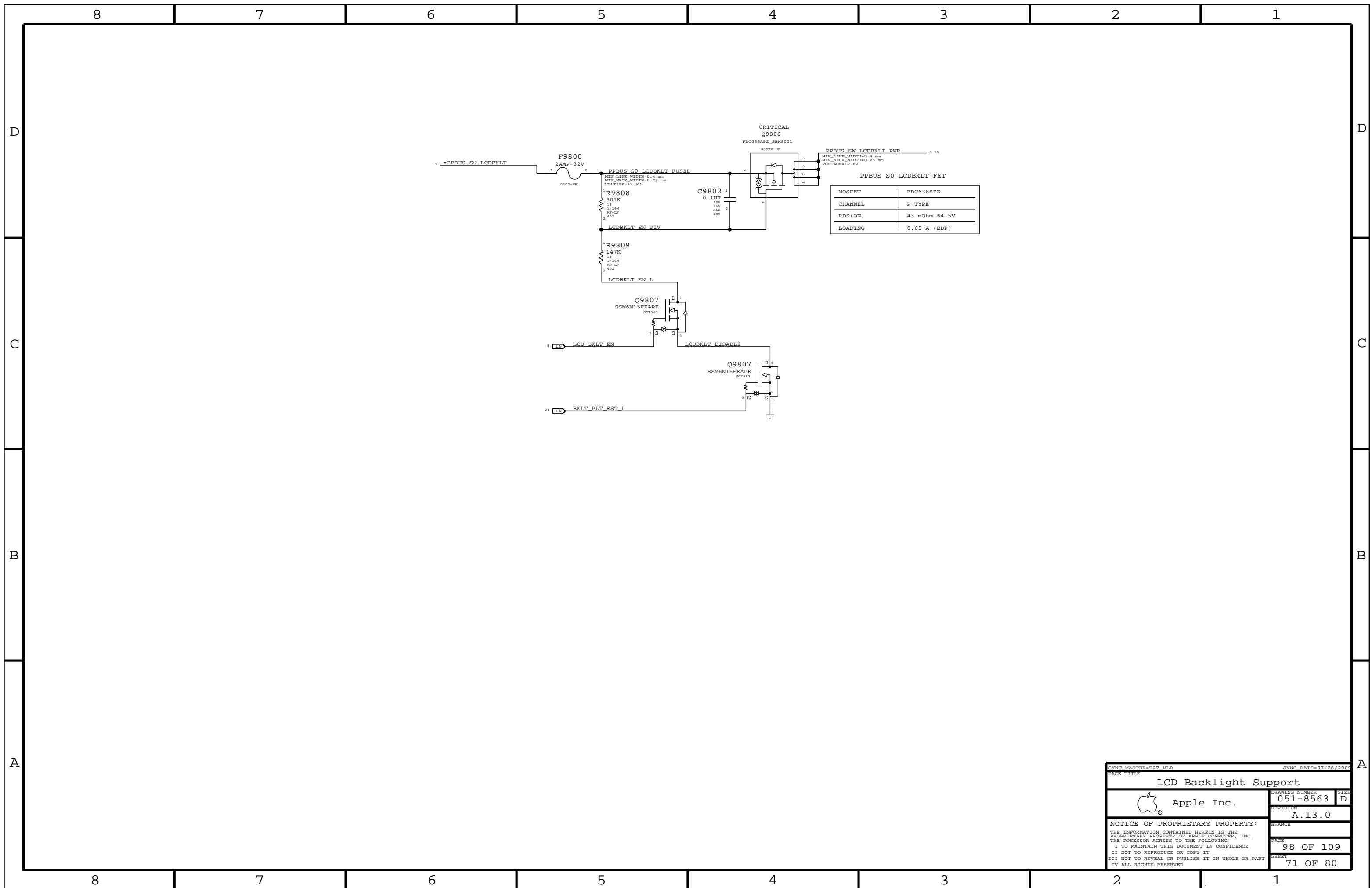
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SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
PAGE TITLE LCD Backlight Support			
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCsense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	9 13
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	9 13
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	9 13
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	9 13
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	9 13
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0 L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	9 13
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	9 13
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	9 13
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 13
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	9 13 40 61
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	9 13 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	9 13
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM THERMTRIP L	9 13 40
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	9 13
CPU_PROM_SB	CPU_50S	CPU_AGTL	CPU DPSLP L	9 13
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9 13 61
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	9 13
FSB_CLK_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	9 13
FSB_CLK_CPUN	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	9 13
FSB_CLK_ITP_P	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	12 13
FSB_CLK_ITP_N	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	12 13
FSB_CLK_MCP_P	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	13
FSB_CLK_MCP_N	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	13
CPU_IERR_L	CPU_50S		CPU IERR L	9
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	13 61
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	61
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	13
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	9 28
CPU_COMP<3>	CPU_50S	CPU_COMP	CPU COMP<3>	9
CPU_COMP<2>	CPU_27P4S	CPU_COMP	CPU COMP<2>	9
CPU_COMP<1>	CPU_50S	CPU_COMP	CPU COMP<1>	9
CPU_COMP<0>	CPU_27P4S	CPU_COMP	CPU COMP<0>	9
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	9 12
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	9 12
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	9 12
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	9 12
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	9 12
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	9 12
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	9 12
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	12
	CPU_50S	CPU_8MIL	CPU VID<6..0>	10 61
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	10 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	10 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	10 61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	10 61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	10 61

SYNC_MASTER=T27_MLB SYNC_DATE=08/03/2009

CPU/FSB Constraints	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NV DG says 3x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 2x inner, 4x outer
 NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 CMD/CTRL signals should be matched within 150 ps.
 All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Need to support MEM_*-style wildcards!

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	14 25
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	14 25
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM A CKE<3..0>	14 20 25
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A CS L<3..0>	14 25
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A ODT<3..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	14 25
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	14 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	14 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	14 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	14 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	14 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	14 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	14 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	14 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	14 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	14 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	14 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	14 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	14 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	14 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	14 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	14 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	14 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	14 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	14 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	14 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	14 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	14 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	14 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	14 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	14 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	14 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	14 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	14 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	14 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	14 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	14 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	14 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	14 26
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	14 26
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM B CKE<3..0>	14 20 26
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B CS L<3..0>	14 26
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B ODT<3..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	14 26
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	14 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	14 27
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	14
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	14

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=T27 MLB		SYNC DATE=08/03/2009	
PAGE TITLE			
Memory Constraints			
Apple Inc.		DRAWING NUMBER	051-8563
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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				
MCP_PEX_COMP	*	8 MIL	?				

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	*	20 MIL	?	CRT	CRT	*	CRT_2CRT
CRT_2CRT	*	15 MIL	?				
CRT_2CLK	*	50 MIL	?				
CRT_2SWITCHER	*	250 MIL	?				
CRT_SYNC	*	=4x_DIELECTRIC	?				
MCP_DAC_COMP	*	=2x_DIELECTRIC	?				

CRT signal single-ended impedance varies by location:
 - 37.5-ohm from MCP to first termination resistor.
 - 50-ohm from first to second termination resistor.
 - 75-ohm from output of three-pole filter to connector (if possible).
 R/G/B signals should be matched as close as possible and < 10 inches.
 SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
 NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max trace length: LVDS 10 inches, DP 8.5 inches.
 SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?	SATA	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?				

SATA intra-pair matching should be 1 ps.
 Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
 SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
MCP_PEG0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
MCP_PEG1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
MCP_PEG2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
MCP_PEG3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP TV DAC VREF
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD P<5..0>
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD N<5..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMP		SATA_TERMP	MCP SATA TERMP

SYNC MASTER=T27 MLB SYNC DATE=08/03/2009

MCP Constraints 1

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAIS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	18 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	18 39 41
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	18 24
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	18 24
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	24 39
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	24 41
USB_EXTN	USB_90D	USB	USB EXTN P	17 37
	USB_90D	USB	USB EXTN N	17 37
	USB_90D	USB	USB EXTN MUXED P	37 79
	USB_90D	USB	USB EXTN MUXED N	37 79
USB_MINI	USB_90D	USB	USB MINI P	8 17
	USB_90D	USB	USB MINI N	8 17
USB_EXTD	USB_90D	USB	USB EXTD P	8 17
	USB_90D	USB	USB EXTD N	8 17
USB_CAMERA	USB_90D	USB	USB CAMERA P	17 29
	USB_90D	USB	USB CAMERA N	17 29
USB_BT	USB_90D	USB	USB BT P	17 29
	USB_90D	USB	USB BT N	17 29
USB_TPAD	USB_90D	USB	USB TPAD P	17 47
	USB_90D	USB	USB TPAD N	17 47
USB_IR	USB_90D	USB	USB IR P	17 38
	USB_90D	USB	USB IR N	17 38
USB_EXTR	USB_90D	USB	USB EXTB P	17 37
	USB_90D	USB	USB EXTB N	17 37
USB_T57	USB_90D	USB	USB T57 P	6 38
	USB_90D	USB	USB T57 N	6 38
USB_EXTC	USB_90D	USB	USB EXTC P	8 17
	USB_90D	USB	USB EXTC N	8 17
USB_SDCARD	USB_90D	USB	USB SDCARD P	17 30
	USB_90D	USB	USB SDCARD N	17 30
USB_WM	USB_90D	USB	USB WM P	8 17
	USB_90D	USB	USB WM N	8 17
MCP_USB_RBIAIS	MCP_USB_RBIAIS		MCP USB RBIAIS GND	17
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	12 18 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	12 18 42
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	18 42
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	18 42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	18 51
	HDA_55S	HDA	HDA BIT CLK R	18 51
HDA_SYNC	HDA_55S	HDA	HDA SYNC	18 51
	HDA_55S	HDA	HDA SYNC R	18 51
HDA_RST_L	HDA_55S	HDA	HDA RST R L	18 51
	HDA_55S	HDA	HDA RST L	18 51
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	18 51
	HDA_55S	HDA	HDA SDIN CODEC	18 51
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	18 51
	HDA_55S	HDA	HDA SDOUT R	18 51
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP HDA PULLDN COMP	18
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	18 24
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	24 39
SPI_CLK	SPT_55S	SPT	SPI CLK R	18 41
	SPT_55S	SPT	SPI CLK	6 41
SPI_MOST	SPT_55S	SPT	SPI MOST R	18 41
	SPT_55S	SPT	SPI MOST	6 41
SPI_MISO	SPT_55S	SPT	SPI MISO	6 18 41
SPI_CS0	SPT_55S	SPT	SPI CS0 R L	18 41
	SPT_55S	SPT	SPI CS0 L	6 41
	SPT_55S	SPT	SPI MLB CLK	41 50
	SPT_55S	SPT	SPI MLB MOSI	41 50
	SPT_55S	SPT	SPI MLB MISO	41 50
	SPT_55S	SPT	SPI MLB CS L	41 50
	SPT_55S	SPT	SPI ALT CLK	41
	SPT_55S	SPT	SPI ALT MOSI	41
	SPT_55S	SPT	SPI ALT MISO	41
	SPT_55S	SPT	SPI ALT CS L	41

SYNC MASTER=T27_MLB SYNC DATE=08/27/2009

MCP Constraints 2

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD	17
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND	17
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R	
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	8 17
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R	
	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK	8 17
	ENET_MII_55S	ENET_MII	ENET_RXD<3..0>	
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	8 17
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	8 17
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	8 17
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
	ENET_MII_55S	ENET_MII	ENET_RESET_L	24 31

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>	31 32
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>	31 32

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SD_DATA	SD_55S	SD_INTERFACE	SD D<4..0>	30
	SD_55S	SD_INTERFACE	SDCONN DATA<4..0>	30 31
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>	31
SD_DATA_B	SD_55S	SD_INTERFACE	SD D<7..5>	30
	SD_55S	SD_INTERFACE	SDCONN DATA<7..5>	30 31
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>	31
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	30
	SD_55S	SD_INTERFACE	SD_CLK R	30
	SD_55S	SD_INTERFACE	SDCONN_CLK	30 31
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	30
	SD_55S	SD_INTERFACE	SDCONN_CMD	30 31
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD	31

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

SYNC MASTER=T27_MLB		SYNC DATE=11/23/2009	
Ethernet Constraints			
		DRAWING NUMBER	051-8563
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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FW_P0_TPA	FW_100D	FW_TP	FW_P0_TPA_P	33 35
FW_P0_TPA	FW_100D	FW_TP	FW_P0_TPA_N	33 35
FW_P0_TPB	FW_100D	FW_TP	FW_P0_TPB_P	33 35
FW_P0_TPB	FW_100D	FW_TP	FW_P0_TPB_N	33 35
FW_P1_TPA	FW_100D	FW_TP	FW_P1_TPA_P	33 35
FW_P1_TPA	FW_100D	FW_TP	FW_P1_TPA_N	33 35
FW_P1_TPB	FW_100D	FW_TP	FW_P1_TPB_P	33 35
FW_P1_TPB	FW_100D	FW_TP	FW_P1_TPB_N	33 35
Port 2 Not Used				

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CANNOT SYNC THIS PAGE FROM T27, FW CONSTRAINTS CHANGED TO 100OHM DIFF

SYNC MASTER=T27_MLB		SYNC DATE=07/20/2005	
PAGE TITLE FireWire Constraints			
 Apple Inc.	DRAWING NUMBER	051-8563	SIZE D
	REVISION	A.13.0	
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 55G	250R	SMBUS_SMC_A_S3_SCL	6 42
SMBUS_SMC_A_S3_SDA	SMB 55G	250R	SMBUS_SMC_A_S3_SDA	6 42
SMBUS_SMC_B_S0_SCL	SMB 55G	250R	SMBUS_SMC_B_S0_SCL	42
SMBUS_SMC_B_S0_SDA	SMB 55G	250R	SMBUS_SMC_B_S0_SDA	42
SMBUS_SMC_O_S0_SCL	SMB 55G	250R	SMBUS_SMC_O_S0_SCL	42
SMBUS_SMC_O_S0_SDA	SMB 55G	250R	SMBUS_SMC_O_S0_SDA	42
SMBUS_SMC_BSA_SCL	SMB 55G	250R	SMBUS_SMC_BSA_SCL	6 42
SMBUS_SMC_BSA_SDA	SMB 55G	250R	SMBUS_SMC_BSA_SDA	6 42
SMBUS_SMC_MGMT_SCL	SMB 55G	250R	SMBUS_SMC_MGMT_SCL	42
SMBUS_SMC_MGMT_SDA	SMB 55G	250R	SMBUS_SMC_MGMT_SDA	42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	58
	1TO1_DIFFPAIR		CHGR_CSI_N	58
	1TO1_DIFFPAIR		CHGR_CSI_R_P	58
	1TO1_DIFFPAIR		CHGR_CSI_R_N	58
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	58
	1TO1_DIFFPAIR		CHGR_CSO_N	58
	1TO1_DIFFPAIR		CHGR_CSO_R_P	44 58
	1TO1_DIFFPAIR		CHGR_CSO_R_N	44 58

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SYNC MASTER=T27_MLB		SYNC DATE=07/28/2009	
SMC Constraints			
 Apple Inc.		DRAWING NUMBER	051-8563
		REVISION	A.13.0
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	TOP	OVERWRITE	OVERWRITE	0.09 MM	5.8 MM	OVERWRITE	OVERWRITE
MCP_DV_COMP_OVERRIDE	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_MEM_COMP_OVERRIDE	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_MII_COMP_OVERRIDE	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_USB_RBIA_OVERRIDE	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_DV_COMP_OVERRIDE	TOP	OVERWRITE	OVERWRITE	0.25 MM	250 MIL	OVERWRITE	OVERWRITE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP CONN P
(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP CONN N
(USB_EXT_A)	USB_90D	USB	USB EXT_A MUXED P
(USB_EXT_A)	USB_90D	USB	USB EXT_A MUXED N
(USB_EXT_A)	USB_90D	USB	USB LT1 P
(USB_EXT_A)	USB_90D	USB	USB LT1 N
(USB_TPAD)	USR_90D	USR	USB TPAD R P
(USB_TPAD)	USR_90D	USR	USB TPAD R N
(USB_CAMERA)	USR_90D	USR	USB CAMERA CONN P
(USB_CAMERA)	USR_90D	USR	USB CAMERA CONN N
(USB_CAMERA)	USR_90D	USR	USB BT CONN P
(USB_CAMERA)	USR_90D	USR	USB BT CONN N
(USB_CAMERA)	USR_90D	USR	USB LT2 P
(USB_CAMERA)	USR_90D	USR	USB LT2 N
(ENET_MDI_100D)	ENETCONN	ENETCONN	ENETCONN P<3..0>
(ENET_MDI_100D)	ENETCONN	ENETCONN	ENETCONN N<3..0>
(SATA_90D)	SATA	SATA	SATA ODD R2D UF P
(SATA_90D)	SATA	SATA	SATA ODD R2D UF N
(SATA_90D)	SATA	SATA	SATA ODD D2R UF P
(SATA_90D)	SATA	SATA	SATA ODD D2R UF N
(SATA_90D)	SATA	SATA	SATA HDD D2R UF P
(SATA_90D)	SATA	SATA	SATA HDD D2R UF N
(SATA_90D)	SATA	SATA	SATA HDD R2D UF P
(SATA_90D)	SATA	SATA	SATA HDD R2D UF N
(SATA_90D)	SATA	SATA	SATA HDD D2R RDRV IN P
(SATA_90D)	SATA	SATA	SATA HDD D2R RDRV IN N
(SATA_90D)	SATA	SATA	SATA HDD R2D RDRV IN P
(SATA_90D)	SATA	SATA	SATA HDD R2D RDRV IN N
(SATA_90D)	SATA	SATA	SATA HDD D2R RDRV OUT P
(SATA_90D)	SATA	SATA	SATA HDD D2R RDRV OUT N
(SATA_90D)	SATA	SATA	SATA HDD R2D RDRV OUT P
(SATA_90D)	SATA	SATA	SATA HDD R2D RDRV OUT N
(SATA_90D)	SATA	SATA	SATA HDD D2R NORDRV P
(SATA_90D)	SATA	SATA	SATA HDD D2R NORDRV N
(SATA_90D)	SATA	SATA	SATA HDD R2D NORDRV P
(SATA_90D)	SATA	SATA	SATA HDD R2D NORDRV N

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(LVDS_100D)	LVDS	LVDS	LVDS CONN A CLK P
(LVDS_100D)	LVDS	LVDS	LVDS CONN A CLK N
(LVDS_100D)	LVDS	LVDS	LVDS CONN A CLK F P
(LVDS_100D)	LVDS	LVDS	LVDS CONN A CLK F N
(LVDS_100D)	LVDS	LVDS	LVDS CONN A DATA P<2..0>
(LVDS_100D)	LVDS	LVDS	LVDS CONN A DATA N<2..0>
(LVDS_100D)	LVDS	LVDS	LVDS CONN B CLK P
(LVDS_100D)	LVDS	LVDS	LVDS CONN B CLK N
(LVDS_100D)	LVDS	LVDS	LVDS CONN B CLK F P
(LVDS_100D)	LVDS	LVDS	LVDS CONN B CLK F N
(LVDS_100D)	LVDS	LVDS	LVDS CONN B DATA P<2..0>
(LVDS_100D)	LVDS	LVDS	LVDS CONN B DATA N<2..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML N<3..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0>
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0>
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C N
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH SW P
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH SW N

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(CPUTHMSNS_D2)	THERM_1T01_55S	THERM	CPUTHMSNS D2 P
(CPUTHMSNS_D2)	THERM_1T01_55S	THERM	CPUTHMSNS D2 N
(CPU_THERMD)	THERM_1T01_55S	THERM	CPU_THERMD P
(CPU_THERMD)	THERM_1T01_55S	THERM	CPU_THERMD N
(MCP_THMSNS_D2)	THERM_1T01_55S	THERM	MCP_THMSNS D2 P
(MCP_THMSNS_D2)	THERM_1T01_55S	THERM	MCP_THMSNS D2 N
(MCP_THMDIODE)	THERM_1T01_55S	THERM	MCP_THMDIODE P
(MCP_THMDIODE)	THERM_1T01_55S	THERM	MCP_THMDIODE N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LV5 S3 P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LV5 S3 N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LV5 S3 R P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LV5 S3 R N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS AIRPORT P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS AIRPORT N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS AIRPORT R P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS AIRPORT R N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS HDD P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS HDD N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS HDD R P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS HDD R N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LCDBKLT P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LCDBKLT N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LCDBKLT R P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS LCDBKLT R N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS ODD P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS ODD N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS ODD R P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS ODD R N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS CPUVTT P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	ISNS CPUVTT N
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN P
(SENSE_DIFFPAIR)	SENSE_1T01_55S	SENSE	MCPCORES0 VSEN N
	MEM_POWER		PP1V5R1V35 S3
	SB_POWER		PP3V3 S5
	SB_POWER		PP3V3 S0
	SB_POWER		PP1V5 S0
	GND		GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(DIFFPAIR)	AUDIO	AUDIO	AUD_SPKRAMP LIN P
(DIFFPAIR)	AUDIO	AUDIO	AUD_SPKRAMP LIN N
(DIFFPAIR)	AUDIO	AUDIO	AUD_SPKRAMP SUBIN P
(DIFFPAIR)	AUDIO	AUDIO	AUD_SPKRAMP SUBIN N
(DIFFPAIR)	AUDIO	AUDIO	AUD_SPKRAMP RIN P
(DIFFPAIR)	AUDIO	AUDIO	AUD_SPKRAMP RIN N
(DIFFPAIR)	AUDIO	AUDIO	SSM2315L P
(DIFFPAIR)	AUDIO	AUDIO	SSM2315L N
(DIFFPAIR)	AUDIO	AUDIO	SSM2315S P
(DIFFPAIR)	AUDIO	AUDIO	SSM2315S N
(DIFFPAIR)	AUDIO	AUDIO	SSM2315R P
(DIFFPAIR)	AUDIO	AUDIO	SSM2315R N
(DIFFPAIR)	AUDIO	AUDIO	SPKRCONN L OUT P
(DIFFPAIR)	AUDIO	AUDIO	SPKRCONN L OUT N
(DIFFPAIR)	AUDIO	AUDIO	SPKRCONN S OUT P
(DIFFPAIR)	AUDIO	AUDIO	SPKRCONN S OUT N
(DIFFPAIR)	AUDIO	AUDIO	SPKRCONN R OUT P
(DIFFPAIR)	AUDIO	AUDIO	SPKRCONN R OUT N
(DIFFPAIR)	AUDIO	AUDIO	BI MIC P
(DIFFPAIR)	AUDIO	AUDIO	BI MIC N
(DIFFPAIR)	AUDIO	AUDIO	HS MIC P
(DIFFPAIR)	AUDIO	AUDIO	HS MIC N

SYNC MASTER=T27_MLB SYNC DATE=09/08/2009

K6/K69 Specific Constraints

Apple Inc.

DRAWING NUMBER: 051-8563 SIZE: D

REVISION: A.13.0

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K6/K69 Board-Specific Physical & Spacing Constraints

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA				MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.080 MM	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.109 MM	=STANDARD	0.224 MM	0.090 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5X_DIELECTRIC	TOP, BOTTOM	0.105 MM	?
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
1.5X_DIELECTRIC	*	0.095 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_LPC	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	STANDARD

SYNC MASTER=T27_MLB		SYNC DATE=08/06/2009	
K6/K69 PCB Rule Definitions			
Apple Inc.		DRAWING NUMBER	051-8563
		REVISION	A.13.0
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