1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
E		396944	PRODUCTION RELEASED	08/26/05	?

SCHEM,MLB,PB15"
08/25/2005

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EMI
GPU_SS	EXT_TMDS (BETTER/BEST)
VGA_BUFFER_RES	INT_TMDS (BEST128)
MMM	SUPERCAP
INT_TMDS (BETTER/BEST)	ADT7460
EXT_TMDS (BEST128)	
BACKUP_BATT	
ADT7467	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6680	1	SCHEM,MLB,PB15	SCH1	
820-1679	1	PCBF,MLB,PB15	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U3Z	LABEL_BST128
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U40	LABEL_BST64
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U41	LABEL_BTR

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6680 REV. E

U51 INTREPID

J23 Ethernet Connector P.28
4 DATA PAIRS
U43 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHZ
J20 FW - B Connector P.30
2 DATA PAIRS @ 400MHZ
U36 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
50MHZ

J13 ODD Connector P.26
EIDE
J12 HDD Connector P.26
UIDE

J15 SW MODEM Connector P.27
J3 LIO/Audio Connector P.27
I2S
I2C
I2C
U53/J1/J18 Fan Circuit P.27

J2 RUX Board Connector P.24
J19 ALS BOARD Connector P.24
J16 BACKUP BATTERY CONNECTOR P.33
C692 SUPERCAP P.33
J26 Battery Connector P.32
Power Supply & Charger P.32-36
J27 DC-In Connector P.32
J8 SLEEP LED P.24
SMBUS
3.3V
U28 PMU P.31
SERIAL
5V
J5 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U8 TI PCI1510 CardBus Controller P.18

U15/U20/U58 MMM P.25
U41 BATTERY CURRENT SENSOR P.25

NOT USED

ETHERNET 10/100/1000 P.13	FIREWIRE 400 MB/S P.13	UATA 100 P.13	EIDE P.13	CARDSLOT P.13	I2S P.14	I2C P.13 P.14

NOT USED USB PORT A P.14
NOT USED USB PORT B P.14
NOT USED USB PORT C P.14
NOT USED USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
MAXBUS P.8

SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12

J28 Serial Debug Connector P.27
U11 BOOT ROM 1M X 8 P.9
J6 AIRPORT Connector P.26
PCI BUS
32BITS
33MHZ
3.3V

J3 BlueTooth (LIO) P.27
J10 SPIDEY P.24

AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47 ATI M11 64MB P.19-22
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
U17 NEC USB2.0 EHCI HC P.17
J3 LEFT USB (VIA LIO) P.27
J17 RIGHT USB (VIA STATLER) P.27

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
U56 APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU

DDR MEMORY P.9
MEMORY BUS
2.5V
167MHZ
64BITS
U16/U18/U28/U27 2:1 DDR MUXES P.10
J25 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.11

J4 Inverter Connector P.23
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
J14 LCD Panel Connector P.23
J21 S-Video Connector P.23
J22 DVI-I Connector P.23

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6680 | REV. E
SCALE NONE | SHT 2 OF 46

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 32

INRUSH LIMITER PG 32

+24V_PBUS

1V20_REF - PG 33
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

RUN/SS
BUCK VCC REGULATOR (LTC1625) PG 33
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO PG 33

+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 34

VCC STBYMD PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 33

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 32

+BATT

3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 32

+PBUS

DC/DC (LTC3411)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 36

+1.8V_MAIN
MAXBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715) PG 36

PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER

+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN

INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK
D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

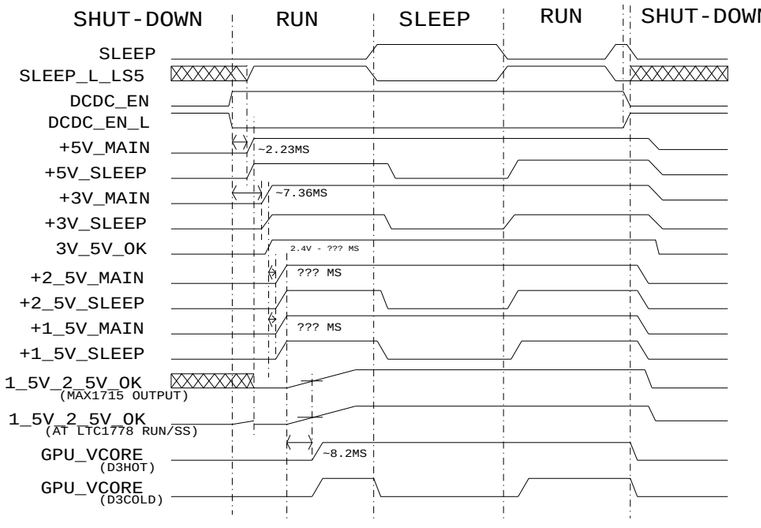
DCDC_EN
SLEEP

MAXBUS SEQUENCING

+5V_MAIN

VCC SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 35

CPU_VCORE (+1.385V)



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT	OF
NONE	3	46

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

1		SIGNAL (1/2 OZ + COPPER PLATING)
2	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
3	PREPREG (3 MIL)	GROUND (1/2 OZ)
4	CORE (3 MIL)	SIGNAL (1/2 OZ)
5	PREPREG (5 MIL)	CUT POWER PLANE (1 OZ)
6	CORE (5 MIL)	CUT POWER PLANE (1 OZ)
7	PREPREG (5 MIL)	SIGNAL (1/2 OZ)
8	CORE (3 MIL)	GROUND (1/2 OZ)
9	PREPREG (3 MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3 MIL)	SIGNAL (1/2 OZ + COPPER PLATING)

BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS
ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA
ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R10 DVI 1394 — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER
SH1 QG-583040 SHLD-SM — CHGND3

MECH. HOLES
ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301 SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302 SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10 SPN NO_TEST=TRUE

GROUND VIAS

ZT76 ZT28 ZT72 ZT69 ZT68 ZT64 ZT61 ZT38 ZT39 ZT40 ZT41 ZT46 ZT71 ZT78 ZT80
ZT50 ZT51 ZT52 ZT53 ZT57 ZT60 ZT82 ZT22 ZT17 ZT35 ZT45 ZT79 ZT81 ZT83 ZT49
ZT48 ZT47 ZT54 ZT55 ZT56 ZT84 ZT5 ZT15 ZT44 ZT4 ZT8 ZT6 ZT32 ZT3 ZT10
ZT11 ZT34 ZT20 ZT43 ZT70 ZT2 ZT9 ZT75 ZT73 ZT63 ZT77 ZT66 ZT62 ZT65 ZT13
ZT25 ZT19 ZT24 ZT67 ZT37 ZT29 ZT31 ZT1 ZT14 ZT12 ZT27 ZT26 ZT30 ZT33 ZT18

(all: HOLE-VIA-20R10)

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 4 OF 46	

CPU_VCORE DECOUPLING NETWORK

CPU_VCORE_SLEEP 5 6 35 40 41

R38 470 5% 1/16W MF 402

C32 10uF 20% 6.3V CERM 805 · C59 10uF 20% 6.3V CERM 805 · C104 10uF 20% 6.3V CERM 805

C33 10uF 20% 6.3V CERM 805 · C58 10uF 20% 6.3V CERM 805 · C107 0.1uF 20% 10V CERM 402

C34 2.2uF 20% 10V CERM 805 · C62 2.2uF 20% 10V CERM 805 · C109 0.1uF 20% 10V CERM 402

C26 C39 C50 C45 C29 C55 C2 C108 0.1uF 20% 10V CERM 402

C30 C49 C31 C47 C27 C53 C103 C110 0.1uF 20% 10V CERM 402

C28 C48 C56 C46 C25 C54 C68 C1 0.1uF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 32)

OMIT
XW34
SM

27 ADT7467_VCORE_MON 1 2

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 5 6 7 8 15 16 35 40

R89 470 5% 1/16W MF 402

C38 C88 C44 C20 C87 C61 0.1uF 20% 10V CERM 402

C18 C89 C72 C10 C69 C81 0.1uF 20% 10V CERM 402

C86 C9 C75 C73 C17 C82 0.1uF 20% 10V CERM 402

40 CPU_AVDD

C810 0.1uF 20% 10V CERM 402 · C811 4.7uF 20% 6.3V CERM 805

+3V_SLEEP

CPU INTERNAL PLL FILTERING

For CPU DFS mode, Must stuff R748
NO STUFF

R453 10 1% 1/16W MF 402 — CPU_VCORE_SLEEP 5 6 35 40 41

R748 10 1% 1/16W MF 402 — 40 CPU_AVDD_VOUT

Vout=0.59*(1+R1/R2)
Place R449 & R452 close to U5 pin 6&5

R302 0 5% 1/16W MF 603

U5 FAN2558 SOT23-6: VIN, PG, EN, GND, VOUT, ADJ

C626 0.001uF 10% 50V CERM 402

R449 118K 1% 1/16W MF 402 — CPU_BST_VCORE128&CPU_BST_VCORE13

R452 100K 1% 1/16W MF 402 — CPU_BST_VCORE128&CPU_BTR_VCORE122&CPU_BST_VCORE126

C102 1uF 10% 6.3V CERM 402

40 CPU_AVDD_VIN

CPU_AVDD_SHDN_L

D17 SN MBR0530

R455 100K 5% 1/16W MF 402

C85 2.2uF 10% 6.3V CERM1 603

C502 0.1uF 20% 10V CERM 402

35 VCORE_SHDN_L

VCORE_SHDN_L_3V

R755 0 5% 1/16W MF 402 — 470OHM FOR BOOT BANGER 41 6 5 JTAG_CPU_TMS

NO STUFF
R775 200K 5% 1/16W MF 402 — 470OHM FOR BOOT BANGER 41 6 5 JTAG_CPU_TDI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0413	1	RES,MF,1/16W,105K OHM,1%,0402,SMD	R449 (R1)		CPU_BTR_VCORE12&CPU_BTR_VCORE122
114S1155	1	RES,MF,1/16W,115K OHM,1%,0402,SMD	R449 (R1)		CPU_BST_VCORE126
114S9764	1	RES,MF,1/16W,97.6K OHM,1%,0402,SMD	R452 (R2)		CPU_BST_VCORE13&CPU_BTR_VCORE122

MPC7447 PULL-UPS

+1_5V_SLEEP — R281 0 5% 1/16W MF 603 — 1_5V_MAXBUS

+1_8V_SLEEP — R283 0 5% 1/16W MF 603 — 1_8V_MAXBUS

40 35 16 15 8 7 6 5 MAXBUS_SLEEP

8 5 CPU_TBEN	R24 10K 5% 1/16W MF 402	
5 CPU_CHKS_L	R4 10K 5% 1/16W MF 402	
5 CPU_SHD0_L	R25 10K 5% 1/16W MF 402	
5 CPU_SHD1_L	R46 10K 5% 1/16W MF 402	
5 CPU_MCP_L	R13 10K 5% 1/16W MF 402	
5 CPU_LSSD_MODE	R26 10K 5% 1/16W MF 402	
5 CPU_L2TSTCLK	R8 10K 5% 1/16W MF 402	
41 5 CPU_CHKSTP_OUT_L	R7 1K 5% 1/16W MF 402	
5 CPU_SRWX_L	R28 10K 5% 1/16W MF 402	
5 CPU_PMONIN_L	R27 10K 5% 1/16W MF 402	
5 CPU_EMODE1_L	R33 10K 5% 1/16W MF 402	
5 CPU_PULLUP	R3 1K 5% 1/16W MF 402	
41 7 6 5 CPU_HRESET_L	R20 10K 5% 1/16W MF 402	
31 5 CPU_SMI_L	R34 10K 5% 1/16W MF 402	
41 6 5 JTAG_CPU_TMS	R32 470 5% 1/16W MF 402	
41 6 5 JTAG_CPU_TDI	R2 470 5% 1/16W MF 402	
14 5 MPIC_CPU_INT_L	R19 10K 5% 1/16W MF 402	
41 5 CPU_SRESET_L	R6 10K 5% 1/16W MF 402	
5 CPU_L1TSTCLK	R37 10K 5% 1/16W MF 402	
5 CPU_EDTI	R36 10K 5% 1/16W MF 402	
41 6 5 JTAG_CPU_TCK	R11 10K 5% 1/16W MF 402	
5 CPU_PULLDOWN	R45 470 5% 1/16W MF 402	

H8 H10 H12 J7 J9 J11 J13 K8 K10 K12 K14 L7 L9 L11 L13 M8 M10 M12 — VDD

B4 C2 C12 D5 F2 H3 J5 K2 L5 M3 N6 P2 P8 P11 R4 R13 R16 T6 T9 U2 U12 U16 V4 V7 V10 V14 — OVDD

E18 G18 — OVDDSENSE

A8 — AVDD

(NAP VOLTAGE=0.98V FOR ALL CONFIG.)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2952	1	IC,A7PM,R1.2.3,1.50GHZ,1.2VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE12_R123
337S2953	1	IC,A7PM,R1.2.3,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE128_R123
337S3069	1	IC,A7PM,R1.2.3,1.67GHZ,1.26VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE126_R123
337S3027	1	IC,A7PM,R1.3,1.50GHZ,1.20VCORE,18W,85C	U56	CRITICAL	NO STUFF
337S3028	1	IC,A7PM,R1.3,1.67GHZ,1.29VCORE,18W,85C	U56	CRITICAL	NO STUFF
337S3105	1	IC,A7PM,R1.2.3,1.67GHZ,1.30VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE13_R123
337S3095	1	IC,A7PM,R1.2.3,1.50GHZ,1.22VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE122_R123
337S3132	1	IC,A7PM,R1.4,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE128_R14
337S3133	1	IC,A7PM,R1.4,1.50GHZ,1.22VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE122_R14
337S3217	1	IC,A7PM,R1.5,1.67GHZ,1.28VCORE,23W,85C	U56	CRITICAL	CPU_BST_VCORE128_R15
337S3218	1	IC,A7PM,R1.5,1.50GHZ,1.22VCORE,18W,85C	U56	CRITICAL	CPU_BTR_VCORE122_R15

OMIT
U56
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)

38 8 CPU_BR_L	D2	BR*
38 8 CPU_BG_L	M1	BG*
38 8 CPU_TS_L	L4	TS*
5 CPU_PULLDOWN	E11	A0
	H1	A1
	C11	A2
	G3	A3
38 8 CPU_ADDR<0>	F10	A4
38 8 CPU_ADDR<1>	L2	A5
38 8 CPU_ADDR<2>	D11	A6
38 8 CPU_ADDR<3>	D1	A7
38 8 CPU_ADDR<4>	C10	A8
38 8 CPU_ADDR<5>	G2	A9
38 8 CPU_ADDR<6>	D12	A10
38 8 CPU_ADDR<7>	L3	A11
38 8 CPU_ADDR<8>	G4	A12
38 8 CPU_ADDR<9>	T2	A13
38 8 CPU_ADDR<10>	F4	A14
38 8 CPU_ADDR<11>	V1	A15
38 8 CPU_ADDR<12>	J4	A16
38 8 CPU_ADDR<13>	R2	A17
38 8 CPU_ADDR<14>	K5	A18
38 8 CPU_ADDR<15>	W2	A19
38 8 CPU_ADDR<16>	J2	A20
38 8 CPU_ADDR<17>	K4	A21
38 8 CPU_ADDR<18>	N4	A22
38 8 CPU_ADDR<19>	J3	A23
38 8 CPU_ADDR<20>	M5	A24
38 8 CPU_ADDR<21>	P5	A25
38 8 CPU_ADDR<22>	N3	A26
38 8 CPU_ADDR<23>	T1	A27
38 8 CPU_ADDR<24>	V2	A28
38 8 CPU_ADDR<25>	U1	A29
38 8 CPU_ADDR<26>	N5	A30
38 8 CPU_ADDR<27>	W1	A31
38 8 CPU_ADDR<28>	B12	A32
38 8 CPU_ADDR<29>	C4	A33
38 8 CPU_ADDR<30>	G10	A34
38 8 CPU_ADDR<31>	B11	A35
NC	C1	AP0
NC	E3	AP1
NC	H6	AP2
NC	F5	AP3
NC	G7	AP4
38 8 CPU_TT<0>	E5	TT0
38 8 CPU_TT<1>	E6	TT1
38 8 CPU_TT<2>	F6	TT2
38 8 CPU_TT<3>	E9	TT3
38 8 CPU_TT<4>	C5	TT4
38 8 CPU_TBST_L	F11	TBST*
38 8 CPU_TSIZ<0>	G8	TSIZ0
38 8 CPU_TSIZ<1>	F7	TSIZ1
38 8 CPU_TSIZ<2>	E7	TSIZ2
38 8 CPU_GBL_L	E2	GBL*
38 8 CPU_WT_L	D3	WT*
38 8 CPU_CI_L	J1	CI*
38 8 CPU_AACK_L	R1	AACK*
38 8 CPU_ARTRY_L	N2	ARTRY*
5 CPU_SHD0_L	E4	SHD0*
5 CPU_SHD1_L	H5	SHD1*
38 8 CPU_HIT_L	B2	HIT*

BVSEL	B7	CPU_BUS_VSEL 7
SYSCLK	A10	SYSCLK_CPU 8 37
CLK_OUT	H2	CPU_CLKOUT_SPN — NO_TEST=TRUE
PLL_CFG0	B8	CPU_PLL_CFG<0> 7
PLL_CFG1	C8	CPU_PLL_CFG<1> 7
PLL_CFG2	C7	CPU_PLL_CFG<2> 7
PLL_CFG3	D7	CPU_PLL_CFG<3> 7
PLL_CFG4	A7	CPU_PLL_CFG<4> 7
DBG*	M2	CPU_DBG_L 8 38
DRDY*	R3	CPU_DRDY_L 8 38
DTI0	G1	CPU_EDTI 5
DTI1	K1	CPU_DTI<0> 8 38
DTI2	P1	CPU_DTI<1> 8 38
DTI3	N1	CPU_DTI<2> 8 38
TDI	B9	JTAG_CPU_TDI 5 6 41
TDO	A4	JTAG_CPU_TDO_TP 41
TMS	F1	JTAG_CPU_TMS 5 6 41
TCK	C6	JTAG_CPU_TCK 5 6 41
TRST*	A5	JTAG_CPU_TRST_L 6 41
LSSD_MODE*	E8	CPU_LSSD_MODE 5
L1_TSTCLK	G8	CPU_L1TSTCLK 5
L2_TSTCLK	B3	CPU_L2TSTCLK 5
TA*	K6	CPU_TA_L 8 38
TEA*	L1	CPU_TEA_L 8 38
TBEN	E1	CPU_TBEN 5 8
QREQ*	P4	CPU_QREQ_L 8 38
QACK*	G5	CPU_QACK_L 8 38
CKSTP_IN*	A3	
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L 5 41
INT*	D4	MPIC_CPU_INT_L 5 14
SMI*	F9	CPU_SMI_L 5 31
MCP*	C9	CPU_MCP_L 5
SRESET*	A2	CPU_SRESET_L 5 41
HRESET*	D8	CPU_HRESET_L 5 6 7 41
PMON_IN*	D9	CPU_PMONIN_L 5
PMON_OUT*	A9	NC
BMODE0*	G9	CPU_EMODE0_L 7
BMODE1*	F8	CPU_EMODE1_L 5
EXT_QUAL	A11	CPU_PULLDOWN 5
CHKS*	A12	CPU_CHKS_L 5
SRW0*	B10	
SRW1*	E10	CPU_SRWX_L 5
IARTRY0*	B6	CPU_PULLUP 5
DX*	D10	CPU_PULLDOWN 5

GND

B5 C3 D6 D13 E17 F3 G17 H4 H7 H9 H11 H13 J6 J8 J10 J12 K7 K3 K9 K11 K13 L6 L8 L10 L12 M4 M7 M9 M11 M13 N7 P3 P9 P12 R5 R14 R17 T7 T10 U3 U13 U17 V5 V8 V11 V15

MPC7447 MAXBUS

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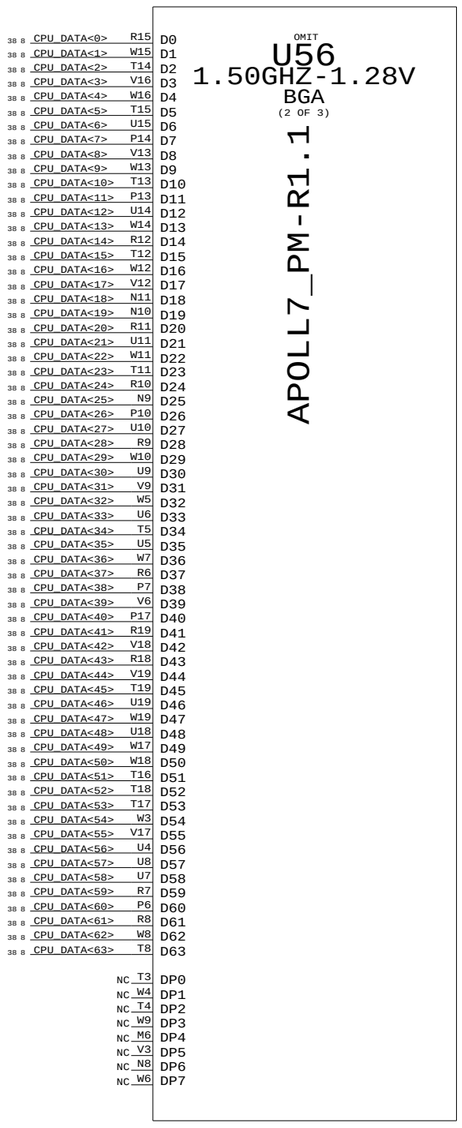
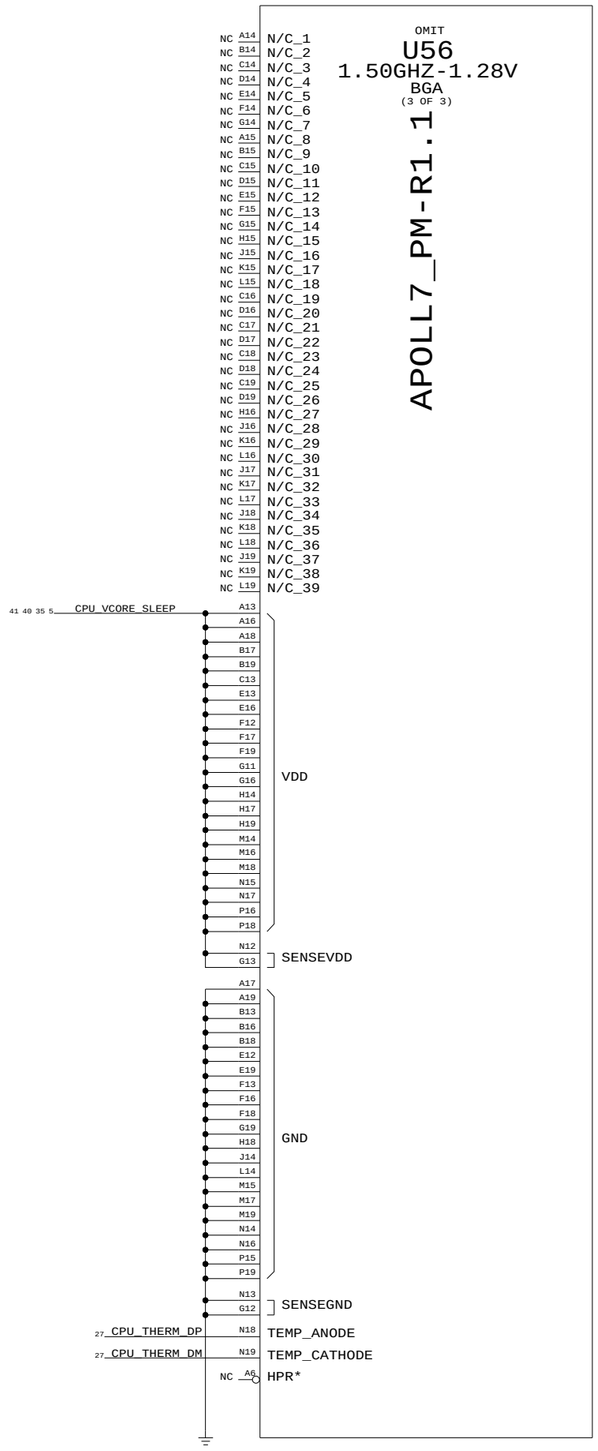
APPLE COMPUTER INC.

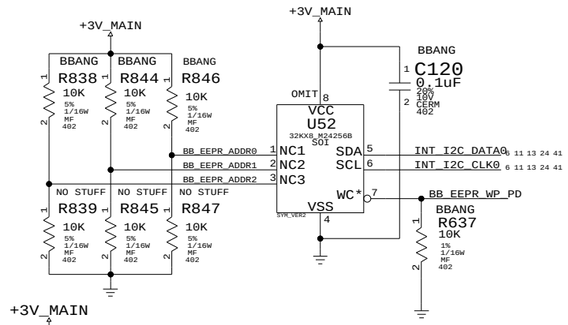
SIZE	DRAWING NUMBER	REV.
D	051-6680	E

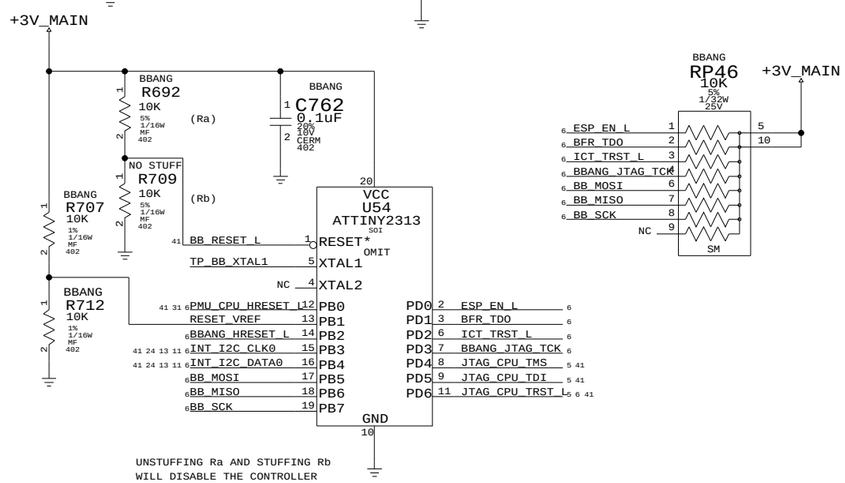
SCALE	SHT	OF
NONE	5	46



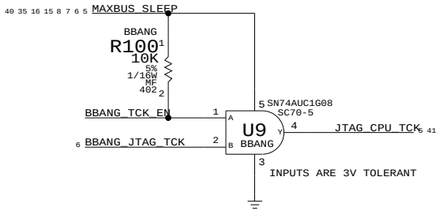


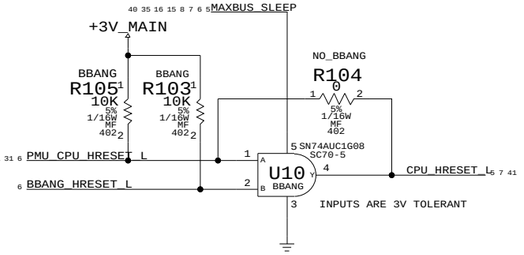
BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

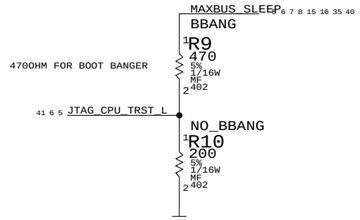




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BBANGER	U54	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BBANGER	U52	BBANG







MPC7447/BBANG

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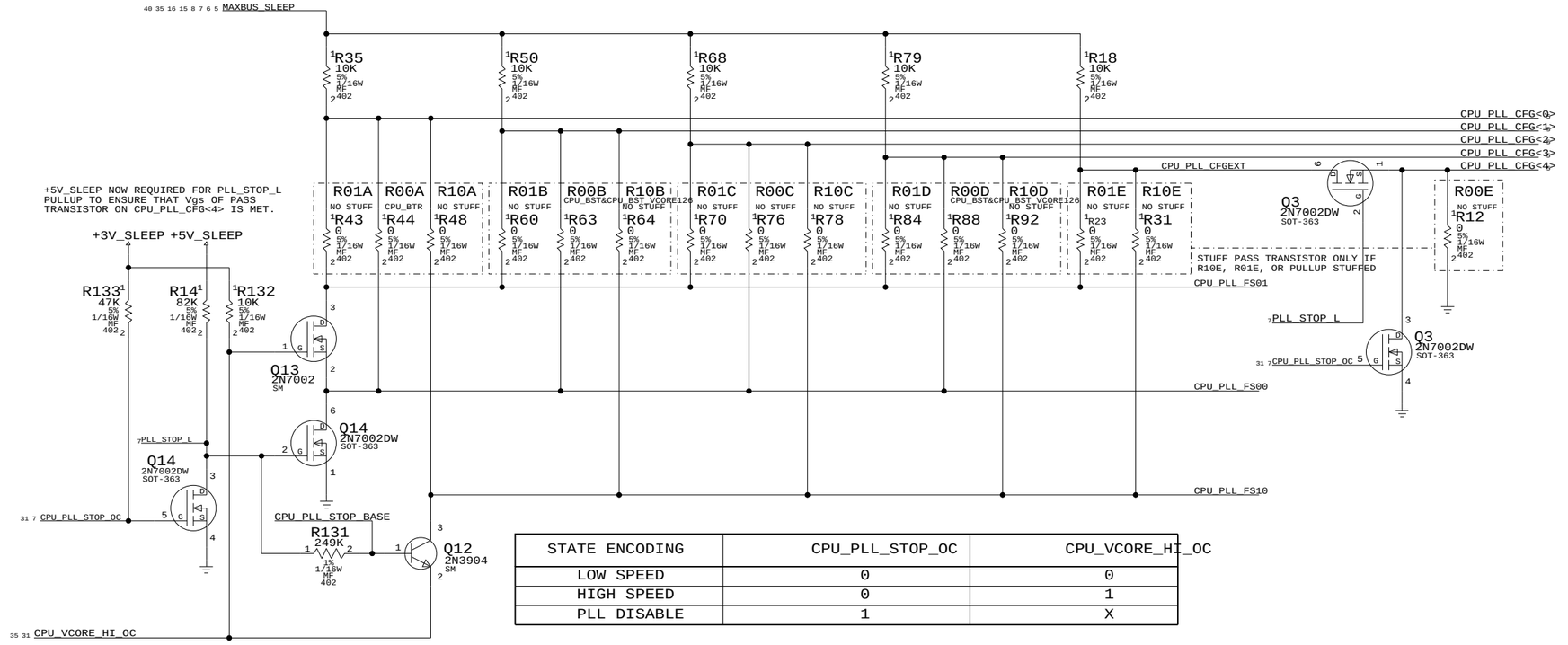
SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 6 OF 46	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

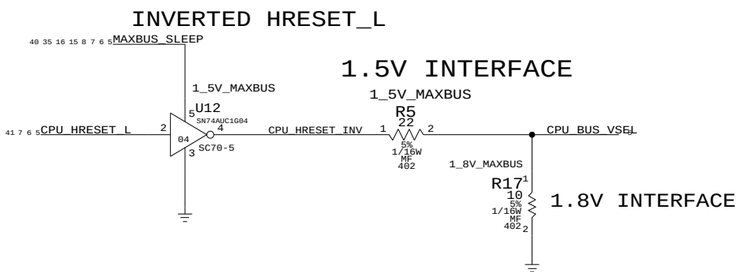
CPU FREQUENCY CONFIGURATION

APOLLO 7PM

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

CPU CONFIGURATION

MAXBUS VSEL



BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT	OF
NONE	7	46

INTREPID BOOT STRAPS

BIT 32 TO 39

40 35 16 15 8 7 6 5 MAXBUS_SLEEP

R640 1 10K 5% 1/16W ME 402 2	R639 1 10K 5% 1/16W ME 402 2	R638 1 10K 5% 1/16W ME 402 2	R666 1 10K 5% 1/16W ME 402 2				
NO STUFF	NO STUFF	NO STUFF					
38 8 6 CPU_DATA<32>	38 8 6 CPU_DATA<33>	38 8 6 CPU_DATA<34>	38 8 6 CPU_DATA<35>	38 8 6 CPU_DATA<36>	38 8 6 CPU_DATA<37>	38 8 6 CPU_DATA<38>	38 8 6 CPU_DATA<39>

R622 1 10K 5% 1/16W ME 402 2	R619 1 10K 5% 1/16W ME 402 2	R618 1 10K 5% 1/16W ME 402 2	R653 1 10K 5% 1/16W ME 402 2	R621 1 10K 5% 1/16W ME 402 2	R620 1 10K 5% 1/16W ME 402 2	R652 1 10K 5% 1/16W ME 402 2	R650 1 10K 5% 1/16W ME 402 2
			NO STUFF				
0: DDR_TRDMODE_Enable_h 1: HDI output	0: Analyzer_Clk_En_h Active	0: DDR_IPDEN Pol 1: Active High	0: Ethernet_SPD_LED Pol 1: Active Low	Spare	Spare	Spare	Spare

BIT 40 TO 47

40 35 16 15 8 7 6 5 MAXBUS_SLEEP

R641 1 10K 5% 1/16W ME 402 2	R665 1 10K 5% 1/16W ME 402 2	R664 1 10K 5% 1/16W ME 402 2	R693 1 10K 5% 1/16W ME 402 2	R694 1 10K 5% 1/16W ME 402 2	R699 1 10K 5% 1/16W ME 402 2		
NO STUFF	SSCG	NO STUFF	NO_SSCG	NO STUFF	NO STUFF		
38 8 6 CPU_DATA<40>	38 8 6 CPU_DATA<41>	38 8 6 CPU_DATA<42>	38 8 6 CPU_DATA<43>	38 8 6 CPU_DATA<44>	38 8 6 CPU_DATA<45>	38 8 6 CPU_DATA<46>	38 8 6 CPU_DATA<47>

R648 1 10K 5% 1/16W ME 402 2	R677 1 10K 5% 1/16W ME 402 2	R623 1 10K 5% 1/16W ME 402 2	R651 1 10K 5% 1/16W ME 402 2	R649 1 10K 5% 1/16W ME 402 2	R678 1 10K 5% 1/16W ME 402 2	R679 1 10K 5% 1/16W ME 402 2	R684 1 10K 5% 1/16W ME 402 2
			NO_SSCG		SSCG		
Spare	Spare	BIT2	BIT1	BIT0	0: Disable (SW CNTL ONLY) 1: Enable (HW CNTL)	0: PCI_PLL4 Source (Clock spread) 1: PCI_PLL4	0: PCI_PLL4 Source (Clock spread) 1: PCI_PLL4

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

40 35 16 15 8 7 6 8 MAXBUS_SLEEP

R696 1 10K 5% 1/16W ME 402 2	R695 1 10K 5% 1/16W ME 402 2	R667 1 10K 5% 1/16W ME 402 2	R668 1 10K 5% 1/16W ME 402 2	R643 1 10K 5% 1/16W ME 402 2	R642 1 10K 5% 1/16W ME 402 2	R698 1 10K 5% 1/16W ME 402 2	
SSCG	SSCG		NO STUFF	NO STUFF	NO STUFF		
38 8 6 CPU_DATA<48>	38 8 6 CPU_DATA<49>	38 8 6 CPU_DATA<50>	38 8 6 CPU_DATA<51>	38 8 6 CPU_DATA<52>	38 8 6 CPU_DATA<53>	38 8 6 CPU_DATA<54>	38 8 6 CPU_DATA<55>

R681 1 10K 5% 1/16W ME 402 2	R680 1 10K 5% 1/16W ME 402 2	R654 1 10K 5% 1/16W ME 402 2	R655 1 10K 5% 1/16W ME 402 2	R625 1 10K 5% 1/16W ME 402 2	R624 1 10K 5% 1/16W ME 402 2	R683 1 10K 5% 1/16W ME 402 2	R626 1 10K 5% 1/16W ME 402 2
NO_SSCG	NO_SSCG	NO STUFF				NO STUFF	
0: Disable PLL4ExtSrc 1: External source	0: PLL5 1: External source	0: BootROM on IDE/CardSlot 1: BootROM on PCI1	OBSOLETE (Should remain high)	0: 133MHz workaround 1: 100MHz workaround	BIT2	BIT1	BIT0

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

0: PCI_REQ_h Active Low
1: PCI_REQ_h Tri-State

0: PCI_GNT_h Active Low
1: PCI_GNT_h Tri-State

0: Enable Analyzer_Clk_En_h
1: Disable Analyzer_Clk_En_h

0: DDR_TRDMODE Enable
1: HDI output

0: Ethernet_SPD_LED Pol Active Low
1: Ethernet_SPD_LED Pol Active High

0: DDR_IPDEN Pol Active Low
1: DDR_IPDEN Pol Active High

0: PCI_GNT_h Active Low
1: PCI_GNT_h Tri-State

0: PCI_REQ_h Active Low
1: PCI_REQ_h Tri-State

R159 4.7 5% 1/16W ME 402
40 14 12 +1_5V_INTREPID_PLL — 1 — 2 — 40 +1_5V_INTREPID_PLL7

C187 0.22uF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

OMIT
U51
INTREPID-REV2.1
BGA

38 8 5 CPU_BR_L	E29	BR	INPUT
38 8 5 CPU_BG_L	E26	BG	NO BUS KEEPER
38 8 5 CPU_TS_L	B27	TS	NO BUS KEEPER

(1 OF 9)
CRITCAL

38 5 CPU_ADDR<0>	D24	A_0
38 5 CPU_ADDR<1>	D25	A_1
38 5 CPU_ADDR<2>	A27	A_2
38 5 CPU_ADDR<3>	E24	A_3
38 5 CPU_ADDR<4>	G23	A_4
38 5 CPU_ADDR<5>	B26	A_5
38 5 CPU_ADDR<6>	A26	A_6
38 5 CPU_ADDR<7>	D23	A_7
38 5 CPU_ADDR<8>	A25	A_8
38 5 CPU_ADDR<9>	E23	A_9
38 5 CPU_ADDR<10>	J22	A_10
38 5 CPU_ADDR<11>	B25	A_11
38 5 CPU_ADDR<12>	H22	A_12
38 5 CPU_ADDR<13>	G22	A_13
38 5 CPU_ADDR<14>	D22	A_14
38 5 CPU_ADDR<15>	B24	A_15
38 5 CPU_ADDR<16>	B23	A_16
38 5 CPU_ADDR<17>	E22	A_17
38 5 CPU_ADDR<18>	J21	A_18
38 5 CPU_ADDR<19>	G21	A_19
38 5 CPU_ADDR<20>	E21	A_20
38 5 CPU_ADDR<21>	A24	A_21
38 5 CPU_ADDR<22>	D21	A_22
38 5 CPU_ADDR<23>	A23	A_23
38 5 CPU_ADDR<24>	H20	A_24
38 5 CPU_ADDR<25>	B22	A_25
38 5 CPU_ADDR<26>	H21	A_26
38 5 CPU_ADDR<27>	A22	A_27
38 5 CPU_ADDR<28>	E20	A_28
38 5 CPU_ADDR<29>	B21	A_29
38 5 CPU_ADDR<30>	D20	A_30
38 5 CPU_ADDR<31>	A21	A_31

MAXBUS INTERFACE

38 5 CPU_CI_L	G26	CI
38 5 CPU_GBL_L	A29	GBL
38 5 CPU_TBST_L	A28	TBST
38 5 CPU_TSIZ<0>	G24	TSIZ_0
38 5 CPU_TSIZ<1>	H24	TSIZ_1
38 5 CPU_TSIZ<2>	D26	TSIZ_2
38 5 CPU_TT<0>	E25	TT_0
38 5 CPU_TT<1>	G25	TT_1
38 5 CPU_TT<2>	B28	TT_2
38 5 CPU_TT<3>	D27	TT_3
38 5 CPU_TT<4>	J25	TT_4
38 5 CPU_WT_L	D28	WT
38 8 5 CPU_AACK_L	B29	AACK — NO BUS KEEPER - PU
38 8 5 CPU_ARTRY_L	H23	ARTRY — NO BUS KEEPER - PU
38 8 5 CPU_HIT_L	B31	HIT — INPUT - PU
38 8 5 CPU_QREQ_L	A32	QREQ — INPUT - PD
38 5 CPU_QACK_L	G27	QACK — NO BUS KEEPER - ?
31 INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
31 INT_SUSPEND_ACK_L	AM8	SUSPENDACK

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

37 8 INT_CPUFB_IN	J24	CPU_FB_IN	
37 8 INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
31 CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
37 5 SYSCLK_CPU — R168 0 5% 1/16W ME 402 — 37 SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
5 CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

	K25	DTI_0	NO BUS KEEPER - ? CPU_DTI<0> 5 38
	D29	DTI_1	NO BUS KEEPER - ? CPU_DTI<1> 5 38
	B30	DTI_2	NO BUS KEEPER - ? CPU_DTI<2> 5 38
	E27	TA	NO BUS KEEPER - PU CPU_TA_L 5 8 38
	E28	TEA	NO BUS KEEPER - PU CPU_TEA_L 5 8 38

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

R169 511 1% 1/16W ME 402 2

R161 1K 1% 1/16W ME 402 2

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

37 8 INT_CPUFB_OUT — R155 0 5% 1/16W ME 402 — 37 INT_CPUFB_OUT_SHORT — R140 0 5% 1/16W ME 402 — 37 INT_CPUFB_OUT_NORM — NO STUFF R128 0 5% 1/16W ME 402 — 37 INT_CPUFB_LONG

37 8 INT_CPUFB_IN — NO STUFF R146 0 5% 1/16W ME 402 — R147 0 5% 1/16W ME 402 — 37 INT_CPUFB_IN_NORM — NO STUFF R141 0 5% 1/16W ME 402 — R136 0 5% 1/16W ME 402

MAXBUS PULL-UPS

MAXBUS_SLEEP 6 7 8 15 16 35 40

38 8 5 CPU_TS_L	RP3 10K 5% 1/16W SM1	2 — 7
38 8 5 CPU_TA_L	RP3 10K 5% 1/16W SM1	1 — 8
38 8 5 CPU_ARTRY_L	RP3 10K 5% 1/16W SM1	4 — 5
38 8 5 CPU_BR_L	RP2 10K 5% 1/16W SM1	1 — 8
38 8 5 CPU_HIT_L	R152 10K 5% 1/16W ME 402	1 — 2
38 8 5 CPU_DRDY_L	RP2 10K 5% 1/16W SM1	3 — 6
38 8 5 CPU_TEA_L	RP2 10K 5% 1/16W SM1	4 — 5
38 8 5 CPU_AACK_L	RP2 10K 5% 1/16W SM1	2 — 7
38 8 5 CPU_DBG_L	R150 10K 5% 1/16W ME 402	1 — 2
38 8 5 CPU_BG_L	RP3 10K 5% 1/16W SM1	3 — 6
38 8 5 CPU_QREQ_L	R151 10K 5% 1/16W ME 402	1 — 2

INTREPID BOOT STRAPS

BIT 56 TO 63

40 35 16 15 8 7 6 5 MAXBUS_SLEEP

R669 1 10K 5% 1/16W ME 402 2	R645 1 10K 5% 1/16W ME 402 2	R697 1 10K 5% 1/16W ME 402 2	R670 1 10K 5% 1/16W ME 402 2	R644 1 10K 5% 1/16W ME 402 2	R646 1 10K 5% 1/16W ME 402 2		
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF			
38 8 6 CPU_DATA<56>	38 8 6 CPU_DATA<57>	38 8 6 CPU_DATA<58>	38 8 6 CPU_DATA<59>	38 8 6 CPU_DATA<60>	38 8 6 CPU_DATA<61>	38 8 6 CPU_DATA<62>	38 8 6 CPU_DATA<63>

R656 1 10K 5% 1/16W ME 402 2	R685 1 10K 5% 1/16W ME 402 2	R657 1 10K 5% 1/16W ME 402 2	R628 1 10K 5% 1/16W ME 402 2	R682 1 10K 5% 1/16W ME 402 2	R658 1 10K 5% 1/16W ME 402 2	R627 1 10K 5% 1/16W ME 402 2	R629 1 10K 5% 1/16W ME 402 2
						NO STUFF	
Spare	Spare	0: OBSOLETE ROM_Overlay_PCI1 1: 0-1 IDE / 2-3 PCI1	0: PCI1_REQ2_L / PCI1_GNT2_L 1: GPIOs	0: PCI1_REQ1_L / PCI1_GNT1_L 1: GPIOs	0: PCI1_REQ0_L / PCI1_GNT0_L 1: GPIOs	0: Firewire PHY interface 1: B-mode interface	0: Processor Bus Mode 1: 64x bus (G4)

Intrepid MaxBus

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SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 8 OF 46	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

OMIT
U51
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR_DATA_0	AK32	MEM_DATA<0>	37 10	
DDR_DATA_1	AK33	MEM_DATA<1>	37 10	
DDR_DATA_2	AK31	MEM_DATA<2>	37 10	
DDR_DATA_3	AK35	MEM_DATA<3>	37 10	
DDR_DATA_4	AK36	MEM_DATA<4>	37 10	
DDR_DATA_5	AJ32	MEM_DATA<5>	37 10	
DDR_DATA_6	AJ35	MEM_DATA<6>	37 10	
DDR_DATA_7	AJ36	MEM_DATA<7>	37 10	
DDR_DATA_8	AG33	MEM_DATA<8>	37 10	
DDR_DATA_9	AG35	MEM_DATA<9>	37 10	
DDR_DATA_10	AH35	MEM_DATA<10>	37 10	
DDR_DATA_11	AG36	MEM_DATA<11>	37 10	
DDR_DATA_12	AH36	MEM_DATA<12>	37 10	
DDR_DATA_13	AH32	MEM_DATA<13>	37 10	
DDR_DATA_14	AG32	MEM_DATA<14>	37 10	
DDR_DATA_15	AG31	MEM_DATA<15>	37 10	
DDR_DATA_16	AE32	MEM_DATA<16>	37 10	
DDR_DATA_17	AF35	MEM_DATA<17>	37 10	
DDR_DATA_18	AF36	MEM_DATA<18>	37 10	
DDR_DATA_19	AE36	MEM_DATA<19>	37 10	
DDR_DATA_20	AE35	MEM_DATA<20>	37 10	
DDR_DATA_21	AE33	MEM_DATA<21>	37 10	
DDR_DATA_22	AD36	MEM_DATA<22>	37 10	
DDR_DATA_23	AD35	MEM_DATA<23>	37 10	
DDR_DATA_24	AA36	MEM_DATA<24>	37 10	
DDR_DATA_25	AA35	MEM_DATA<25>	37 10	
DDR_DATA_26	AA33	MEM_DATA<26>	37 10	
DDR_DATA_27	AB36	MEM_DATA<27>	37 10	
DDR_DATA_28	AB35	MEM_DATA<28>	37 10	
DDR_DATA_29	AC36	MEM_DATA<29>	37 10	
DDR_DATA_30	AA32	MEM_DATA<30>	37 10	
DDR_DATA_31	AB33	MEM_DATA<31>	37 10	
DDR_DATA_32	V36	MEM_DATA<32>	37 10	
DDR_DATA_33	U33	MEM_DATA<33>	37 10	
DDR_DATA_34	U32	MEM_DATA<34>	37 10	
DDR_DATA_35	V35	MEM_DATA<35>	37 10	
DDR_DATA_36	T36	MEM_DATA<36>	37 10	
DDR_DATA_37	U36	MEM_DATA<37>	37 10	
DDR_DATA_38	U35	MEM_DATA<38>	37 10	
DDR_DATA_39	T36	MEM_DATA<39>	37 10	
DDR_DATA_40	P33	MEM_DATA<40>	37 10	
DDR_DATA_41	R36	MEM_DATA<41>	37 10	
DDR_DATA_42	P35	MEM_DATA<42>	37 10	
DDR_DATA_43	P36	MEM_DATA<43>	37 10	
DDR_DATA_44	R36	MEM_DATA<44>	37 10	
DDR_DATA_45	R35	MEM_DATA<45>	37 10	
DDR_DATA_46	R33	MEM_DATA<46>	37 10	
DDR_DATA_47	R32	MEM_DATA<47>	37 10	
DDR_DATA_48	N35	MEM_DATA<48>	37 10	
DDR_DATA_49	M36	MEM_DATA<49>	37 10	
DDR_DATA_50	L35	MEM_DATA<50>	37 10	
DDR_DATA_51	M35	MEM_DATA<51>	37 10	
DDR_DATA_52	M33	MEM_DATA<52>	37 10	
DDR_DATA_53	L36	MEM_DATA<53>	37 10	
DDR_DATA_54	N33	MEM_DATA<54>	37 10	
DDR_DATA_55	M36	MEM_DATA<55>	37 10	
DDR_DATA_56	J32	MEM_DATA<56>	37 10	
DDR_DATA_57	J33	MEM_DATA<57>	37 10	
DDR_DATA_58	J35	MEM_DATA<58>	37 10	
DDR_DATA_59	K32	MEM_DATA<59>	37 10	
DDR_DATA_60	K33	MEM_DATA<60>	37 10	
DDR_DATA_61	J36	MEM_DATA<61>	37 10	
DDR_DATA_62	K36	MEM_DATA<62>	37 10	
DDR_DATA_63	K35	MEM_DATA<63>	37 10	

DDR MEMORY INTERFACE

DDR_A_0	H35	MEM_ADDR<0>	9 37
DDR_A_1	G35	MEM_ADDR<1>	9 37
DDR_A_2	G36	MEM_ADDR<2>	9 37
DDR_A_3	F36	MEM_ADDR<3>	9 37
DDR_A_4	F35	MEM_ADDR<4>	9 37
DDR_A_5	E35	MEM_ADDR<5>	9 37
DDR_A_6	E36	MEM_ADDR<6>	9 37
DDR_A_7	G32	MEM_ADDR<7>	9 37
DDR_A_8	D36	MEM_ADDR<8>	9 37
DDR_A_9	H36	MEM_ADDR<9>	9 37
DDR_A_10	G33	MEM_ADDR<10>	9 37
DDR_A_11	H33	MEM_ADDR<11>	9 37
DDR_A_12	D35	MEM_ADDR<12>	9 37
DDR_BA_0	L30	MEM_BA<0>	9 37
DDR_BA_1	M29	MEM_BA<1>	9 37
DDRCS_0	AN34	MEM_CS_L<0>	9 37
DDRCS_1	AN36	MEM_CS_L<1>	9 37
DDRCS_2	AL35	MEM_CS_L<2>	9 37
DDRCS_3	AL33	MEM_CS_L<3>	9 37
DDR_DQS_0	AJ31	MEM_DQS<0>	10 37
DDR_DQS_1	AH31	MEM_DQS<1>	10 37
DDR_DQS_2	AD32	MEM_DQS<2>	10 37
DDR_DQS_3	AB30	MEM_DQS<3>	10 37
DDR_DQS_4	V30	MEM_DQS<4>	10 37
DDR_DQS_5	P32	MEM_DQS<5>	10 37
DDR_DQS_6	N29	MEM_DQS<6>	10 37
DDR_DQS_7	L32	MEM_DQS<7>	10 37
DDR_DM_0	AJ33	MEM_DQM<0>	10 37
DDR_DM_1	AH33	MEM_DQM<1>	10 37
DDR_DM_2	AD33	MEM_DQM<2>	10 37
DDR_DM_3	AC35	MEM_DQM<3>	10 37
DDR_DM_4	T35	MEM_DQM<4>	10 37
DDR_DM_5	T33	MEM_DQM<5>	10 37
DDR_DM_6	N32	MEM_DQM<6>	10 37
DDR_DM_7	L33	MEM_DQM<7>	10 37
DDRRAS	L29	MEM_RAS_L	9 37
DDRCAS	H32	MEM_CAS_L	9 37
DDRWE	K30	MEM_WE_L	9 37
DDRCKE0	AN35	MEM_CKE<0>	9 37
DDRCKE1	AM35	MEM_CKE<1>	9 37
DDRCKE2	AM36	MEM_CKE<2>	9 37
DDRCKE3	AL36	MEM_CKE<3>	9 37
DDR_SELHI_0	AB32	MEM_MUXSEL_MSB_L_TP	
DDR_SELHI_1	AE29	MEM_MUXSEL_MSB	10 37
DDR_SELLO_0	N30	MEM_MUXSEL_LSB_L_TP	10 37
DDR_SELLO_1	T32	MEM_MUXSEL_LSB	10 37
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 37
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 37
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 37
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 37
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 37
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 37
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 37
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 37
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF	40
DDR_VREF_0	Y22	INT_MEM_VREF	40
DDR_VREF_1	T22		

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

R209 1K 1% 1/16W MF 402

MEM_VREF

+2.5V_INTREPID

R208 10K 1% 1/16W MF 402

R202 10K 1% 1/16W MF 402

C249 0.1uF 10% 10V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP20 4	5	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP20 3	6	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP22 1	8	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP22 7		SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP20 2	7	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP20 8		SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP22 3	6	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP22 5		SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP31 3	6	RAM_CS_L<0>
MEM_CS_L<1>	RP31 2	7	RAM_CS_L<1>
MEM_CS_L<2>	RP29 3	6	RAM_CS_L<2>
MEM_CS_L<3>	RP29 4	5	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP31 1	8	RAM_CKE<0>
MEM_CKE<1>	RP31 4	5	RAM_CKE<1>
MEM_CKE<2>	RP29 1	8	RAM_CKE<2>
MEM_CKE<3>	RP29 2	7	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP14 3	6	RAM_ADDR<0>
MEM_ADDR<1>	RP12 2	7	RAM_ADDR<1>
MEM_ADDR<2>	RP12 1	8	RAM_ADDR<2>
MEM_ADDR<3>	RP12 4	5	RAM_ADDR<3>
MEM_ADDR<4>	RP12 3	6	RAM_ADDR<4>
MEM_ADDR<5>	RP9 2	7	RAM_ADDR<5>
MEM_ADDR<6>	RP9 1	8	RAM_ADDR<6>
MEM_ADDR<7>	RP14 2	7	RAM_ADDR<7>
MEM_ADDR<8>	RP9 4	5	RAM_ADDR<8>
MEM_ADDR<9>	RP14 4	5	RAM_ADDR<9>
MEM_ADDR<10>	RP14 1	8	RAM_ADDR<10>
MEM_ADDR<11>	RP17 4	5	RAM_ADDR<11>
MEM_ADDR<12>	RP9 3	6	RAM_ADDR<12>

BA

MEM_BA<0>	RP17 2	7	RAM_BA<0>
MEM_BA<1>	RP17 1	8	RAM_BA<1>

CNTL

MEM_WE_L	RP17 3	6	RAM_WE_L
MEM_CAS_L	R162 1	2	RAM_CAS_L
MEM_RAS_L	R176 1	2	RAM_RAS_L

1MB BOOT ROM

+3V_MAIN

C125 2.2uF 10% 10V CERM 805

C773 0.1uF 10% 10V CERM 402

C122 0.1uF 10% 10V CERM 402

U11
1MX8-3.3V
TSOP

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		
VPP	11		
OMIT	30		
VCC	31		
GND	23, 39		

PCI_AD<0> … PCI_AD<31> (41 39 26 18 17 12)

ROM_CS_TP_L

R236 0 NO STUFF

R691 10K

R112 10K

ROM_CS_L

R674 1K

R1 0 NO STUFF

ROM_ONBOARD_CS_TP_L

R271 0 NO STUFF

ROM_OE_TP_L

R194 0 NO STUFF

ROM_RW_TP_L

ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1792	1	IC,BOOTROM,4.9.1F3,Q16B	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R247 10K
R257 10K
R260 10K
R265 10K

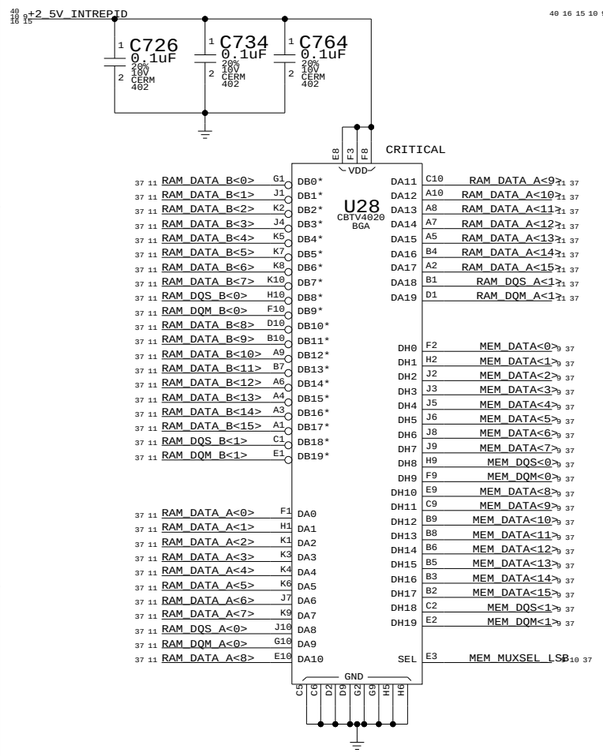
INT_2_5V_COLD

INT - DDR/BOOTROM

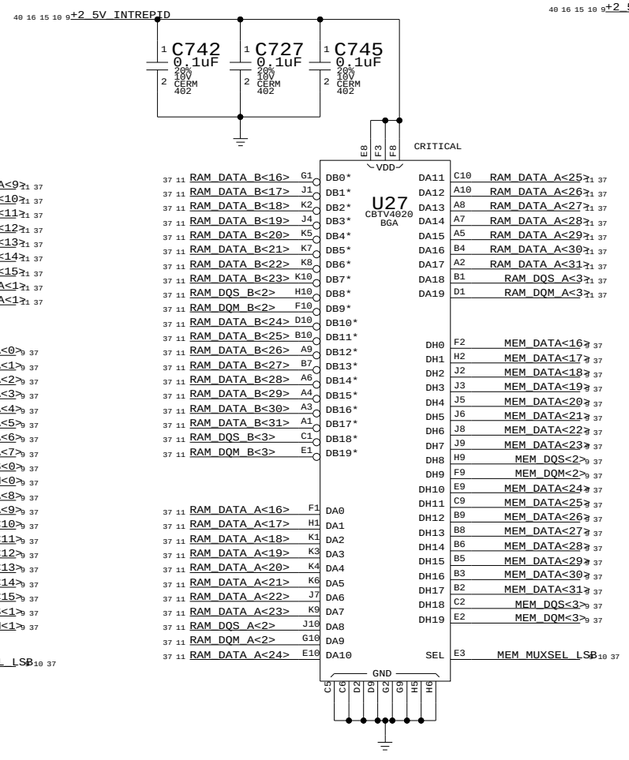
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 9 OF 46	

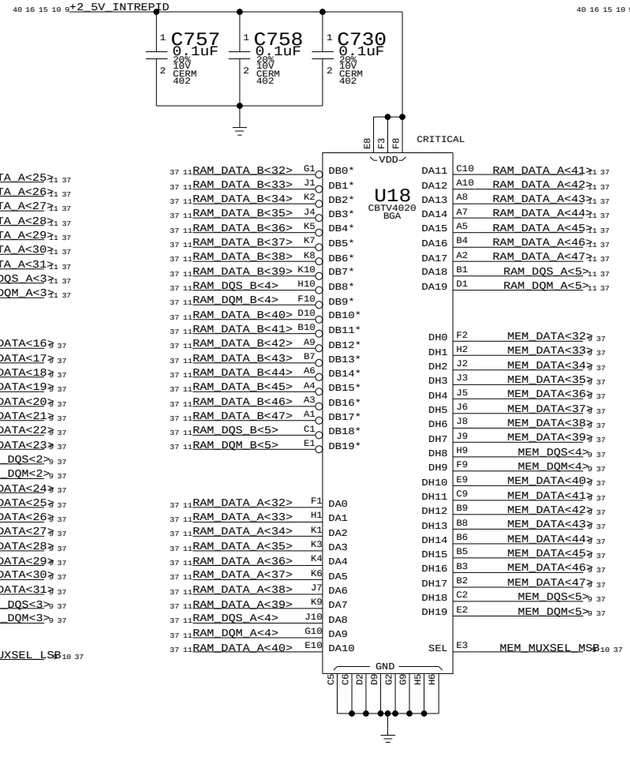
BIT 0..15



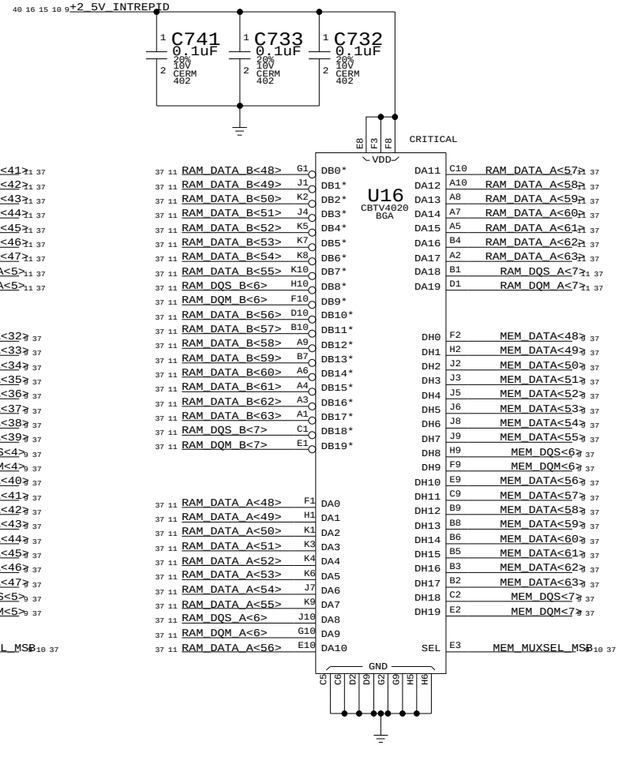
BIT 16..31



BIT 32..47



BIT 48..63



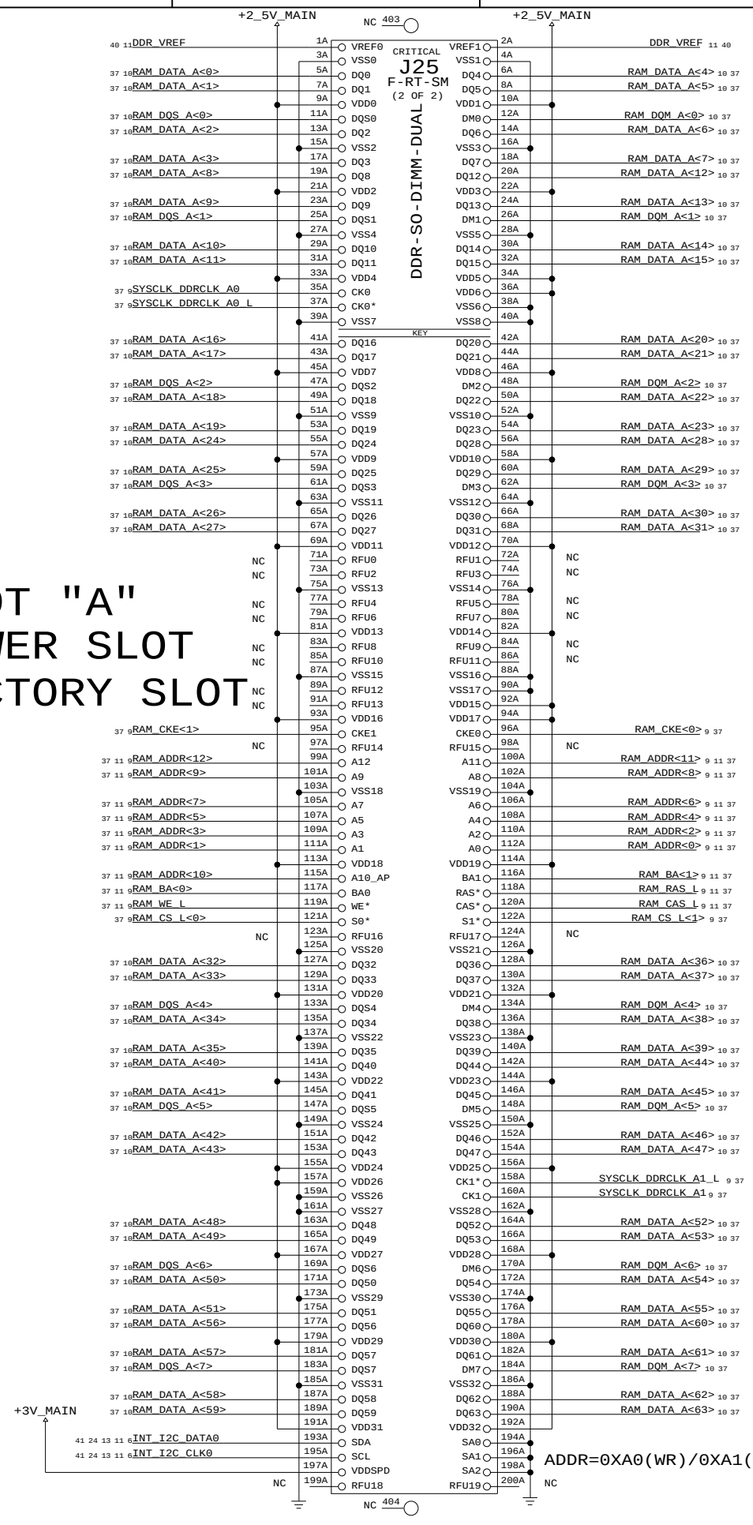
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

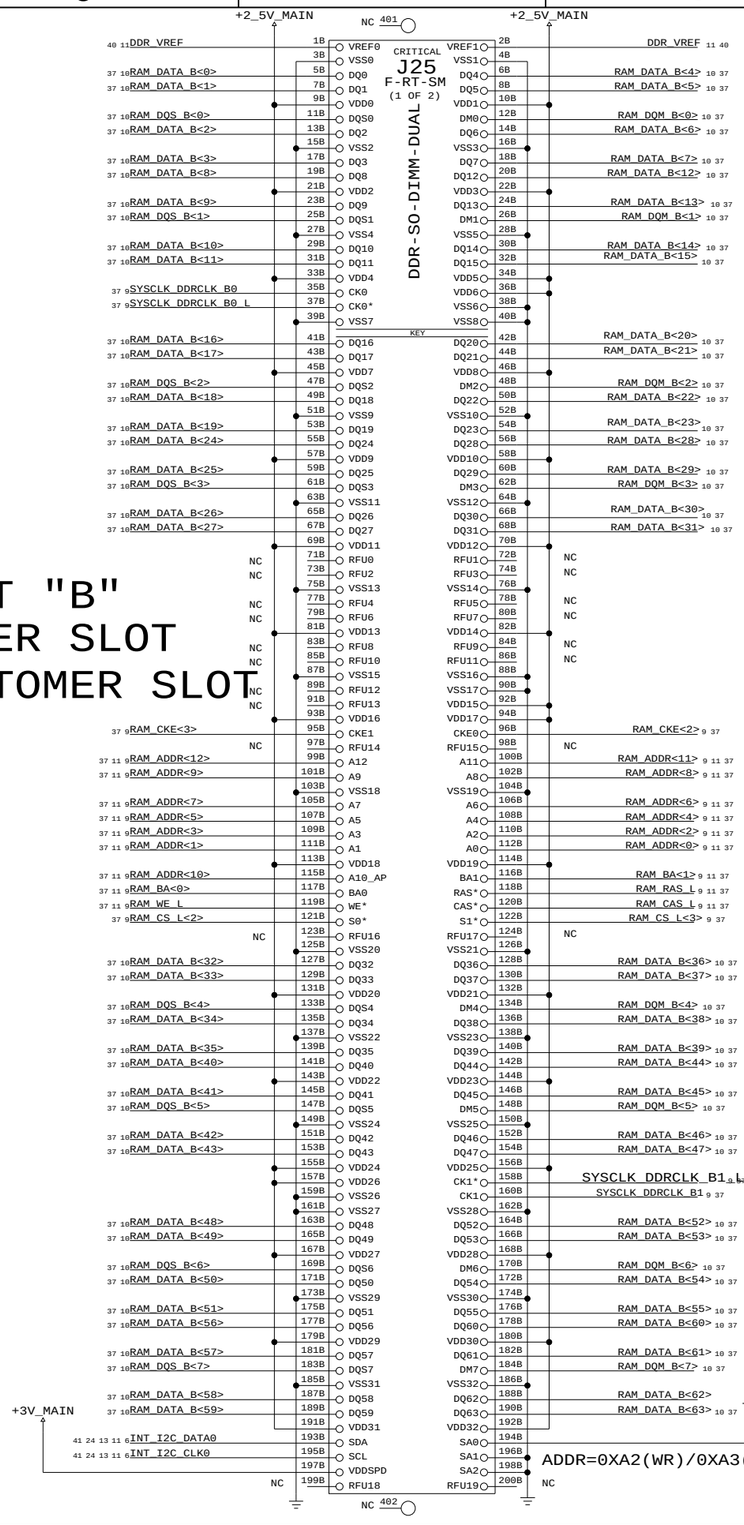
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT OF
NONE	10 46

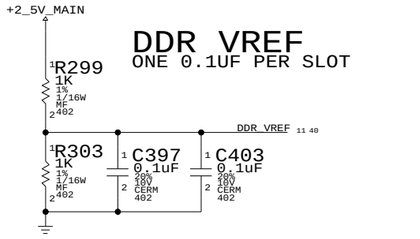


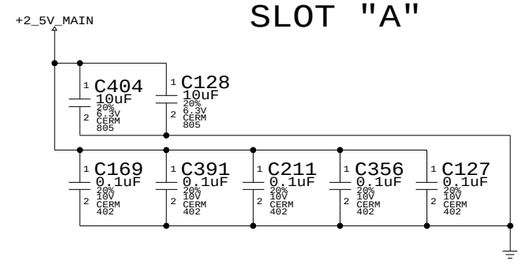
SLOT "A"
LOWER SLOT
FACTORY SLOT

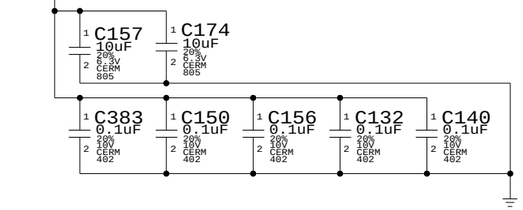


SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting





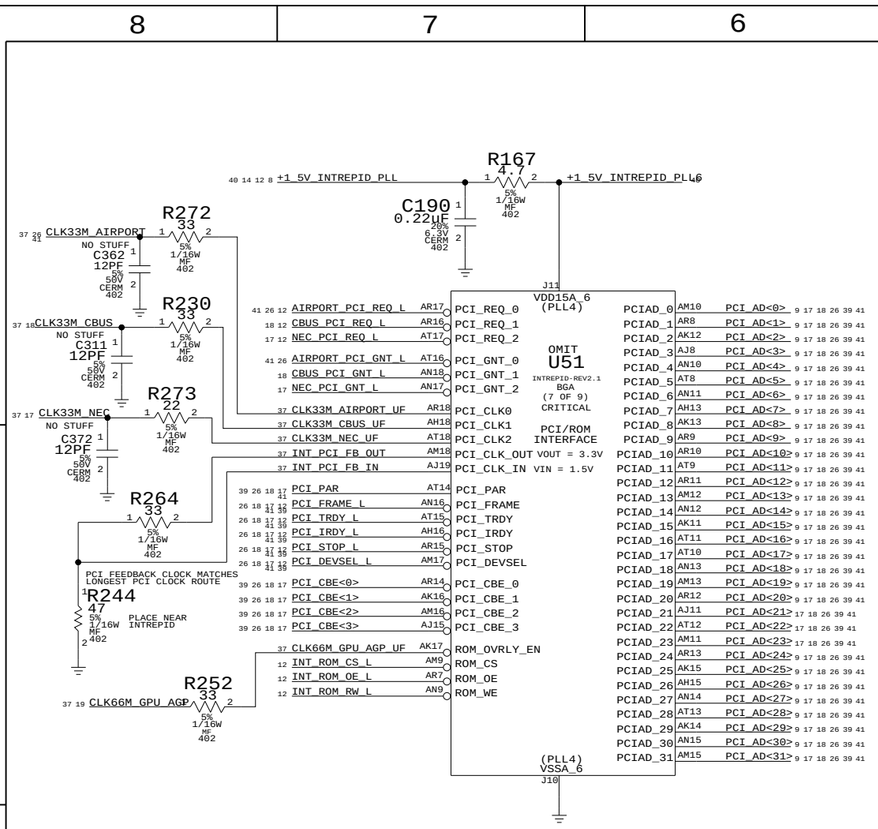


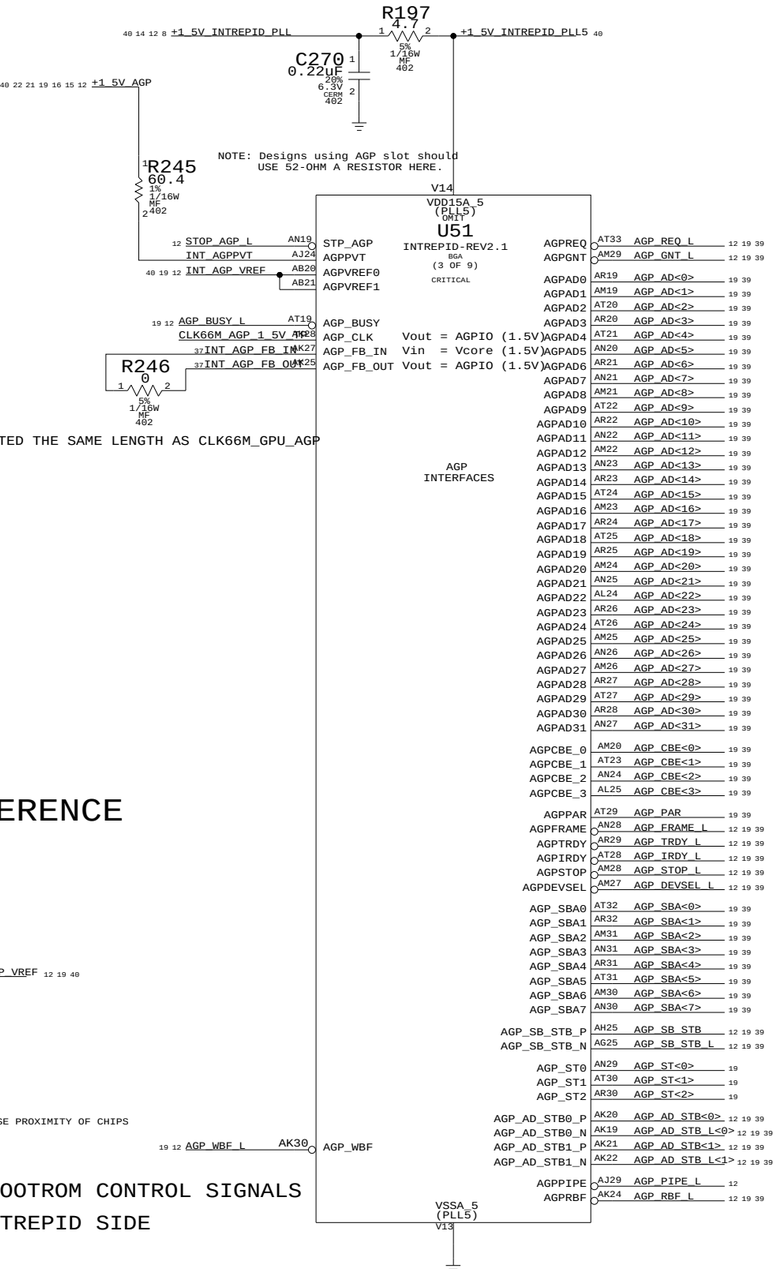
DDR SODIMM CONNS

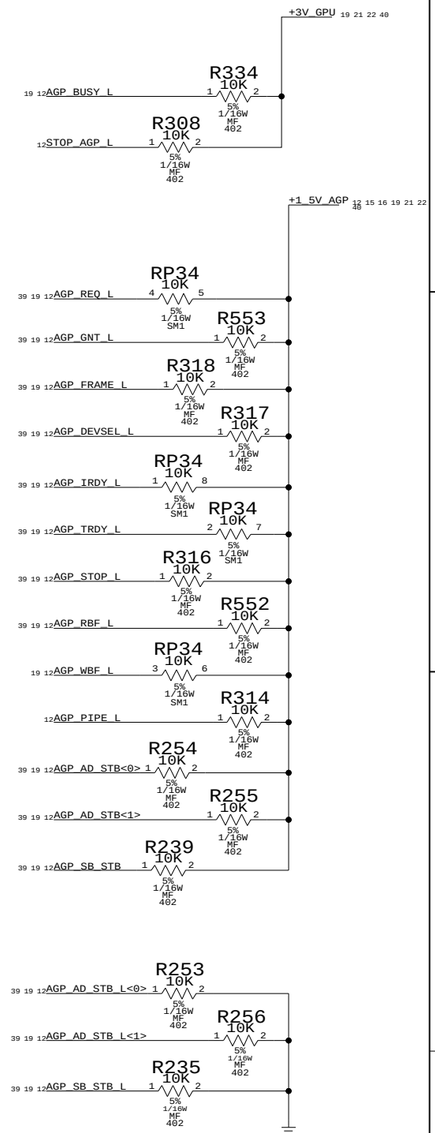
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

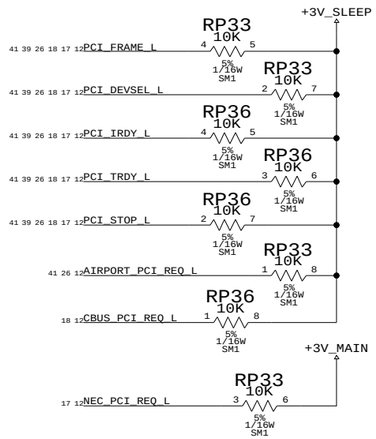
SCALE	SHT	OF
NONE	11	46







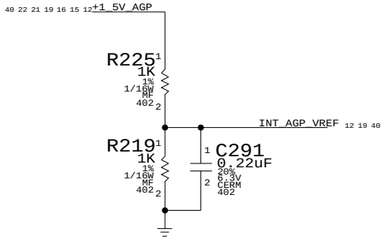
PCI PULL-UPS



NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP

AGP I/O REFERENCE

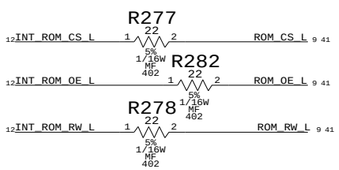
(PLACE CLOSE TO INTREPID AGP BALLS)



SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

PLACE CLOSE TO INTREPID SIDE



AGP PULL-UPS/PULL DOWNS

INTREPID AGP/PCI

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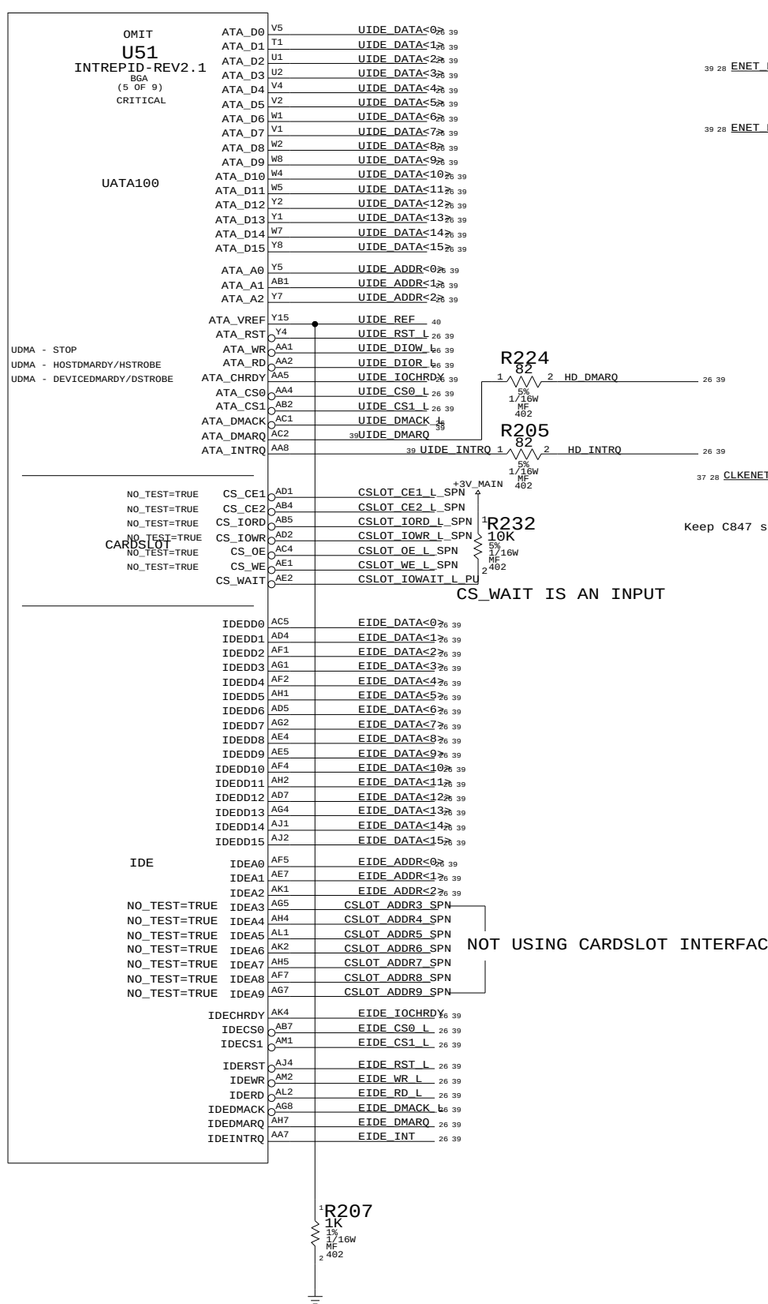
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT	OF
NONE	12	46


OMIT
U51
INTREPID-REV2.1
BGA
(5 OF 9)
CRITICAL
UATA100
ATA_D0 ATA_D1 ATA_D2 ATA_D3 ATA_D4 ATA_D5 ATA_D6 ATA_D7 ATA_D8 ATA_D9 ATA_D10 ATA_D11 ATA_D12 ATA_D13 ATA_D14 ATA_D15
UIDE_DATA<0> UIDE_DATA<1> UIDE_DATA<2> UIDE_DATA<3> UIDE_DATA<4> UIDE_DATA<5> UIDE_DATA<6> UIDE_DATA<7> UIDE_DATA<8> UIDE_DATA<9> UIDE_DATA<10> UIDE_DATA<11> UIDE_DATA<12> UIDE_DATA<13> UIDE_DATA<14> UIDE_DATA<15>
ATA_A0 ATA_A1 ATA_A2
UIDE_ADDR<0> UIDE_ADDR<1> UIDE_ADDR<2>
ATA_VREF
UIDE_REF
ATA_RST
UIDE_RST_L
UDMA - STOP
ATA_WR
UIDE_DIOW_L
UDMA - HOSTDMARDY/HSTROBE
ATA_RD
UIDE_DIOR_L
UDMA - DEVICEDMARDY/DSTROBE
ATA_CHRDY
UIDE_IOCHRDY
ATA_CS0
UIDE_CS0_L
ATA_CS1
UIDE_CS1_L
ATA_DMACK
UIDE_DMACK_L
ATA_DMARQ
UIDE_DMARQ
ATA_INTRQ
UIDE_INTRQ
R224
82
HD_DMARQ
R205
82
HD_INTRQ
NO_TEST=TRUE
CS_CE1 CS_CE2 CS_IORD CS_IOWR CS_OE CS_WE CS_WAIT
CSLOT_CE1_L_SPN CSLOT_CE2_L_SPN CSLOT_IORD_L_SPN CSLOT_IOWR_L_SPN CSLOT_OE_L_SPN CSLOT_WE_L_SPN CSLOT_IOWAIT_L_PU
CARDSLOT
+3V_MAIN
R232
10K
CS_WAIT IS AN INPUT
IDEDD0 IDEDD1 IDEDD2 IDEDD3 IDEDD4 IDEDD5 IDEDD6 IDEDD7 IDEDD8 IDEDD9 IDEDD10 IDEDD11 IDEDD12 IDEDD13 IDEDD14 IDEDD15
EIDE_DATA<0> EIDE_DATA<1> EIDE_DATA<2> EIDE_DATA<3> EIDE_DATA<4> EIDE_DATA<5> EIDE_DATA<6> EIDE_DATA<7> EIDE_DATA<8> EIDE_DATA<9> EIDE_DATA<10> EIDE_DATA<11> EIDE_DATA<12> EIDE_DATA<13> EIDE_DATA<14> EIDE_DATA<15>
IDE
IDEA0 IDEA1 IDEA2 IDEA3 IDEA4 IDEA5 IDEA6 IDEA7 IDEA8 IDEA9
EIDE_ADDR<0> EIDE_ADDR<1> EIDE_ADDR<2> CSLOT_ADDR3_SPN CSLOT_ADDR4_SPN CSLOT_ADDR5_SPN CSLOT_ADDR6_SPN CSLOT_ADDR7_SPN CSLOT_ADDR8_SPN CSLOT_ADDR9_SPN
NOT USING CARDSLOT INTERFACE
IDECHRDY IDECS0 IDECS1 IDERST IDEWR IDERD IDEDMACK IDEDMARQ IDEINTRQ
EIDE_IOCHRDY EIDE_CS0_L EIDE_CS1_L EIDE_RST_L EIDE_WR_L EIDE_RD_L EIDE_DMACK_L EIDE_DMARQ EIDE_INT
R207
1K
CLKENET_LINK_TX
R145
10
ENET_PHY_TX_EN
ENET_LINK_TX_EN
R149
10
ENET_PHY_TX_ER
ENET_LINK_TX_ER
ENET_LINK_TXD<0> ENET_LINK_TXD<1> ENET_LINK_TXD<2> ENET_LINK_TXD<3> ENET_LINK_TXD<4> ENET_LINK_TXD<5> ENET_LINK_TXD<6> ENET_LINK_TXD<7>
CLKENET_LINK_RX
ENET_RX_DV
ENET_RX_ER
ENET_LINK_RXD<0> ENET_LINK_RXD<1> ENET_LINK_RXD<2> ENET_LINK_RXD<3> ENET_LINK_RXD<4> ENET_LINK_RXD<5> ENET_LINK_RXD<6> ENET_LINK_RXD<7>
CLKENET_LINK_GBE_REF
CLKENET_LINK_GTX
ENET_CRS
ENET_COL
ENET_MDIO
ENET_MDC
CLKENET_PHY_GTX
R160
10
Keep C847 stub short
NO STUFF
C847
10pF
JTAG_ASIC_TDI
INT_TDO
JTAG_ASIC_TCK
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L
INT_JTAG_TEI
INT_TST_MONIN_PD
INT_TST_MONOUT_TP
INT_TST_PLLEN_PD
OMIT
U51
INTREPID-REV2.1
BGA
(4 OF 9)
CRITICAL
TX_CLK TX_EN TX_ER
TXD_0 TXD_1 TXD_2 TXD_3 TXD_4 TXD_5 TXD_6 TXD_7
RX_CLK RX_DV RX_ER
RXD_0 RXD_1 RXD_2 RXD_3 RXD_4 RXD_5 RXD_6 RXD_7
GBE_REFCLK GTX_CLK CRS COL MDIO MDC
GB ETHERNET
TDI TDO TCK TMS TRSTN TEI TST_MONIN TST_MONOUT TST_PLLEN
TEST
MISC
RESET PURESET
INT_RESET_L INT_PU_RESET_L
FIREWIRE
PHY_DATA0 PHY_DATA1 PHY_DATA2 PHY_DATA3 PHY_DATA4 PHY_DATA5 PHY_DATA6 PHY_DATA7
FW_LINK_DATA<0> FW_LINK_DATA<1> FW_LINK_DATA<2> FW_LINK_DATA<3> FW_LINK_DATA<4> FW_LINK_DATA<5> FW_LINK_DATA<6> FW_LINK_DATA<7>
PHY_LPS PHY_CTL0 PHY_CTL1 PHY_LREQ FWR_PCLK
FW_PHY_LPS FW_LINK_CNTL<0> FW_LINK_CNTL<1> FW_LINK_LREQ CLKFW_LINK_PCLK
FWR_LCLK FW_LINKON FW_PINT
CLKFW_LINK_LCLK FW_LKON FW_PINT
R186
22
FW_PHY_LREQ
R195
22
CLKFW_PHY_LCLK
IICCLK_0 IICDATA_0 IICCLK_1 IICDATA_1
INT_I2C_CLK0 INT_I2C_DATA0 INT_I2C_CLK1 INT_I2C_DATA1
TEST PULL-UPS/DOWNS
+3V_MAIN
RP35
10K
JTAG_ASIC_TDI
JTAG_ASIC_TMS
INT_TDO
HW_PLL<BIT 0>
R269
10K
NO STUFF
R630
10K
INT_TST_PLLEN_PD
R270
10K
JTAG_ASIC_TCK
R263
1K
JTAG_ASIC_TRST_L
INT_JTAG_TEI
INT_TST_MONIN_PD
R259
1K
I2C PULL-UPS
+3V_MAIN
RP32
2.2K
INT_I2C_CLK0
INT_I2C_DATA0
INT_I2C_CLK1
INT_I2C_DATA1
ENET_PHY_TXD<0> ENET_PHY_TXD<1> ENET_PHY_TXD<2> ENET_PHY_TXD<3> ENET_PHY_TXD<4> ENET_PHY_TXD<5> ENET_PHY_TXD<6> ENET_PHY_TXD<7>
RP16
RP10
22
ENET_LINK_TXD<0> ENET_LINK_TXD<1> ENET_LINK_TXD<2> ENET_LINK_TXD<3> ENET_LINK_TXD<4> ENET_LINK_TXD<5> ENET_LINK_TXD<6> ENET_LINK_TXD<7>
ENET_TXD SERIES TERMINATION
BUS / ADDR
I2C-0 (MAIN)
I2C-1 (MAIN)
I2C-2 (SLEEP)
PMU (SLEEP)
A0-WR A1-RD
RAM - LOWER J25 - PG 11
N/A
A2-WR A3-RD
RAM - UPPER J25 - PG 11
AC-WR AD-RD
SOFT MODEM J14 - PG 26
AE-WR AF-RD
BOOTBANG EEPROM U51 - PG 6
84-WR 85-RD
LMU J3000 - PG 24 (LMU on RUX Brd.)
5C-WR 5D-RD
FAN CONTROLLER U52 - PG 26
6A-WR 6B-RD
SNAPPER SOUND J2 - PG 26
D2-WR D3-RD
CLOCK SLEW SSCG U30 - PG 14
B0-WR B1-RD
MMM U15 - PG 42
ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES
JTG_RSTN_L
TST_TEI_H
JTG_TDO_H (I/O)
JTG_TDI_H (I/O)
TST_PLLEN_H
ANALYZER_CLK
DESCRIPTION
1 X X X X X JTAG MODE
0 0 EXTPLL SHUTDOWN (OUTPUT) DDR_ TPDENABLE (OUTPUT) 0 (OUTPUT) NORMAL OPERATION
0 0 (OUTPUT) 0(I) 1 SELECTED PLL OUTPUTS VIEW PLLS (SOFTWARE)
0 0 HWPLL_ TESTSEL5 (INPUT) 1(I) 1 SELECTED PLL OUTPUTS VIEW PLLS (HARDWARE)
0 1 0(I) 0(I) MEMWE SYNC/MEM DATA BYPASS ATPG NORMAL
0 1 0(I) 1(I) 0 X(I) ATPG IDDQ
0 1 0(I) 1(I) 1 X(I) TEST TRI-STATE
0 1 1(I) 0(I) 0 X(I) FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0 1 1(I) 0(I) 1 X(I) FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0 1 1(I) 1(I) X X(I) FUNCTIONAL TEST IDDQ
INT - ENET/FW/UATA EIDE/I2C
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6680
REV. E
SCALE NONE
SHT 13 OF 46

USB PORT ASSIGNMENTS

PORT A B C D/UNUSED

R181 10K — USB_DAM
R183 10K — USB_DAP
R123 10K — USB_DBP
R121 10K — USB_DBM
R164 10K — USB_DCM
R165 10K — USB_DCP
R182 10K — USB_DDM
R180 10K — USB_DDP

PORT E/BLUETOOTH

R174 22 — USB_DEP — BT_USB_DP
R179 22 — USB_DEM — BT_USB_DM
R178 15K — R175 15K

PORT F/TRACKPAD

R635 22 — USB_DFP — USB_TPAD_P
R603 22 — USB_DFM — USB_TPAD_N
R129 15K — R125 15K

+2_5V_MAIN — NO STUFF R568 0 — +1_8V_MAIN — R565 0

U49 LTC1962-ADJ MSOP
IN, NC, NC, SHDN, OUT, ADJ, BYP, GND
LTC1962_INT_VIN, LTC1962_INT_ADJ, LTC1962_INT_BYP
C721 1uF 10V CERM 603
C392 0.01uF 20% 16V CERM 402
R574 18.7K 1% 1/16W MF 402
R567 68.1K 1% 1/16W MF 402
C723 10uF 20% 6.3V CERM 805
+1_5V_INTREPID_PLL -> 1.55V OUTPUT

+3V_SLEEP
R148 10K — CBUS_INT_L
R746 10K — AIRPORT_PCI_INT_L
+3V_MAIN — R158 10K — NEC_PCI_INT_L
PCI INTERRUPTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

+3V_MAIN — GPIO/EXTINT PULLUPS
R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP6 10K — INT_EXTINT10_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
USB_MODEM RP15 10K — INT_MOD_DTO_UF
USB_MODEM RP15 10K — INT_MOD_CLKOUT_UF
RP5 10K — NC EXTINT11
RP4 10K — NC EXTINT12
USB_MODEM RP15 10K — INT_MOD_DTI
USB_MODEM RP15 10K — INT_MOD_SYNC_UF
USB_MODEM R206 10K — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

+3V_MAIN — SSCG L15 400-OHM-EMI SM-1
+2_5V_MAIN — SSCG L14 400-OHM-EMI SM-1
+3V_CG_PLL_MAIN
SSCG C402 1uF 20% 10V CERM 603
SSCG C399 0.1uF 20% 10V CERM 402
SSCG C400 0.1uF 20% 10V CERM 402
+2_5V_CG_MAIN
SSCG C394 0.1uF 20% 10V CERM 402
MAIN_RESET_L
NO STUFF R286 0
SSCG R287 10K
SSCG R288 10K
NO STUFF R295 10K

SSCG U31 CY28512D TSSOP OMIT — CRITICAL
CLKIN 20 — FSEL 3 — SCLK 9 — SDATA 8 — ADDRSEL 14 — RESET* 17 — PD* 13 — LOCK 2 — ODSEL 4
VDD0 1, VDD1 10, VDDA 12, VDDC 5, VDD2 18
VSS0 7, VSS1 19, VSSA 11, VSSC 6, VSSQ 15
CPU0 16 CG_CLKOUT
INTERNAL 250K PULL-UP; OUTPUT IMPEDANCE ~18-20 OHMS; INTERNAL 250K PULL-DOWN

INT_REF_CLK_OUT — CG_FSEL — INT_I2C_CLK1 — INT_I2C_DATA1 — CG_ADDRSEL — CG_RESET_L — CG_SYSCLK_EN — CG_LOCK
SSCG R293 33 — INT_REF_CLK_IN
SSCG R292 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
SSCG R284 0 — VCORE_VGATE
NO STUFF R296 10K

NO STUFF R467 0 — SYSTEM_CLK_EN
R457 0 — INT_TDO — CG_SYSCLK_EN
NO STUFF J9 U.FL-R-SMT F-ST-SM — CLK18M_INT_EXT
NO STUFF R134 0
NO STUFF R113 51
NO STUFF R144 10M
R143 0
CRITICAL Y2 OMIT 18.432M 8X4.5MM-SM
CLK18M_XTAL_IN
C152 22pF 5% 50V CERM 402
C151 22pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 16PF
R218 0 — INT_REF_CLK_OUT
+3V_MAIN — R802 10K — MMM_SIRQ_L — R801 10K — MMM_FFIRQ_L

HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

R240 4.7 — +1_5V_INTREPID_PLL
C337 0.22uF 20% 6.3V CERM 402
R280 4.7 — +1_5V_INTREPID_PLL
C389 0.22uF 20% 6.3V CERM 402
R279 4.7 — +1_5V_INTREPID_PLL
C388 0.22uF 20% 6.3V CERM 402
R243 4.7 — +1_5V_INTREPID_PLL
C386 0.22uF 20% 6.3V CERM 402
R201 4.7 — +1_5V_INTREPID_PLL
C387 0.22uF 20% 6.3V CERM 402

+3V_MAIN — L13 FERR-EMI-100-OHM SM
+3V_INTREPID_USB
C235 0.01uF 16V CERM 402
C246 0.1uF 10V CERM 402
C256 10uF 20% 6.3V CERM 805

SSCG R450 0

U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9) — OMIT

GPIO0 — VCORE A/B SEL
GPIO1 — GENERAL PURPOSE I/O'S
GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO9, GPIO11, GPIO12, GPIO15, GPIO16
CG_FSEL_1 — CG_FSEL_INT — INT_GPIO1_PU — COMM_RESET_L — FW_PHY_PD — SND_HP_MUTE_L — SND_AMP_MUTE_L — INT_GPIO9_PU — SND_HW_RESET_L — INT_GPIO12_PU — INT_GPIO15_PU — INT_ENET_RST_L

EXTINT0, EXTINT1, EXTINT2, EXTINT3, EXTINT4, EXTINT5, EXTINT6, EXTINT7, EXTINT8, EXTINT9, EXTINT10, EXTINT11, EXTINT12, EXTINT13, EXTINT14, EXTINT15, EXTINT16, EXTINT17, CPU_INT — INTERRUPTS
POWERBOOK SPARE
CBUS_REG_L, CBUS_IREQ_L
COMM_RING_DET_L, PMU_INT_L, AGP_ATI_INT_L, INT_EXTINT3_PU, SND_LIN_SENSE_L, ENET_ENERGY_DET, AIRPORT_PCI_INT_L, CBUS_INT_L, INT_EXTINT8_PU, PMU_INT_NMI, INT_EXTINT10_PU, MMM_FFIRQ_L, MMM_SIRQ_L, INT_EXTINT13_PU, INT_EXTINT14_PU, SND_HP_SENSE_L, INT_EXTINT16_PU, NEC_PCI_INT_L, MPIC_CPU_INT_L, PMU_PME_L, INT_PROC_SLEEP_REQ_L, INT_PEND_PROC_INT

PCIPME, PROCSLEEPREQ, PENDPROCINT

XTAL_IN, XTAL_OUT, STOPXTAL, WATCHDOG, BUF_REF_CLK_OUT, SS_REF_CLK_IN — CLOCKS
CLK18M_INT_XIN, CLK18M_INT_XOUT, SYSTEM_CLK_EN, INT_WATCHDOG_L, INT_REF_CLK_OUT_UF, INT_REF_CLK_IN

PCI VDD15A_1 (PLL1) AA16 — PCI VDD15A_2 (PLL2) AJ12 — PCI VDD15A_3 (PLL3) AJ17 — PCI VDD15A_4 (PLL7) AJ18 — PCI VDD15A_8 (PLL9) AG29
VDDU33_1 T8 — VDDU33_2 U8
VSSA1 (PLL1) AA15 — VSSA2 (PLL2) AJ13 — VSSA3 (PLL3) AJ16 — VSSA4 (PLL7) AK18 — VSSA_8 (PLL9) AH29 — VSSU_1 R9 — VSSU_2 R8

SCCTXDA AF9 COMM_TXD_L — SCCRTSA AN3 COMM_RTS_L — SCCDTRA AF10 COMM_DTR_L — SCCRXDA AG11 COMM_RXD — SCCGPIOA AG9 COMM_GPIO_L — SCCTRXCA AT4 COMM_TRXC
VIA
MISO SCCTXDB AR4 PMU_FROM_INT — REQ* SCCRTSB AL5 PMU_REQ_L — MOSI SCCRXDB AG10 PMU_TO_INT — ACK* SCCGPIOB AP4 PMU_ACK_L — SCK SCCTRXCB AM5 PMU_CLK

USB_VD0_P L8 USB_DAP — USB_VD0_N L7 USB_DAM
USB_VD1_P G2 USB_DBP — USB_VD1_N G1 USB_DBM
USB_PRTPWR0 J4 USB_PWREN_AB_L — USB_PWRFLT0 K4 USB_OC_AB_L
USB_VD2_P H2 USB_DCP — USB_VD2_N H1 USB_DCM
USB_VD3_P M7 USB_DDP — USB_VD3_N M8 USB_DDM
USB_PRTPWR1 J2 USB_PWREN_CD_L — USB_PWRFLT1 J1 USB_OC_CD_L
USB_VD4_P K5 USB_DEP — USB_VD4_N L5 USB_DEM
USB_VD5_P P8 USB_DFP — USB_VD5_N N8 USB_DFM
USB_PRTPWR2 M5 USB_PWREN_EF_L — USB_PWRFLT2 N7 USB_OC_EF_L
USB

AUD_DTO R4 INT_I2S0_SND_TO_DAC_UF — AUD_DTI R7 INT_I2S0_SND_FROM_ADC — AUD_SYNC T5 INT_I2S0_SND_LRCLK_UF — AUD_BITCLK P2 INT_I2S0_SND_SCLK_UF — AUD_CLKOUT R5 INT_I2S0_SND_MCLK_UF
AUDIO/I2S
MOD_DTO R2 INT_MOD_DTO_UF — (SIGNAL FROM MODEM) MOD_DTI T4 INT_MOD_DTI — MOD_SYNC R1 INT_MOD_SYNC_UF — MOD_BITCLK V8 INT_MOD_BITCLK_UF — MOD_CLKOUT P1 INT_MOD_CLKOUT_UF

IICCLK_2 AL4 — IICDATA_2 AH8
IIC
+3V_SLEEP — R258 1K — R241 1K — INT_I2C_CLK2 — INT_I2C_DATA2

RP13 47 — INT_I2S0_SND_TO_DAC
RP13 47 — INT_I2S0_SND_LRCLK
RP13 47 — INT_I2S0_SND_SCLK
RP13 47 — INT_I2S0_SND_MCLK
SOFT_MODEM RP47 0K — INT_MOD_DTO
SOFT_MODEM RP47 0K — INT_MOD_SYNC
SOFT_MODEM RP47 0K — INT_MOD_BITCLK
SOFT_MODEM RP47 0K — INT_MOD_CLKOUT

INT - USB/GPIOS/I2S

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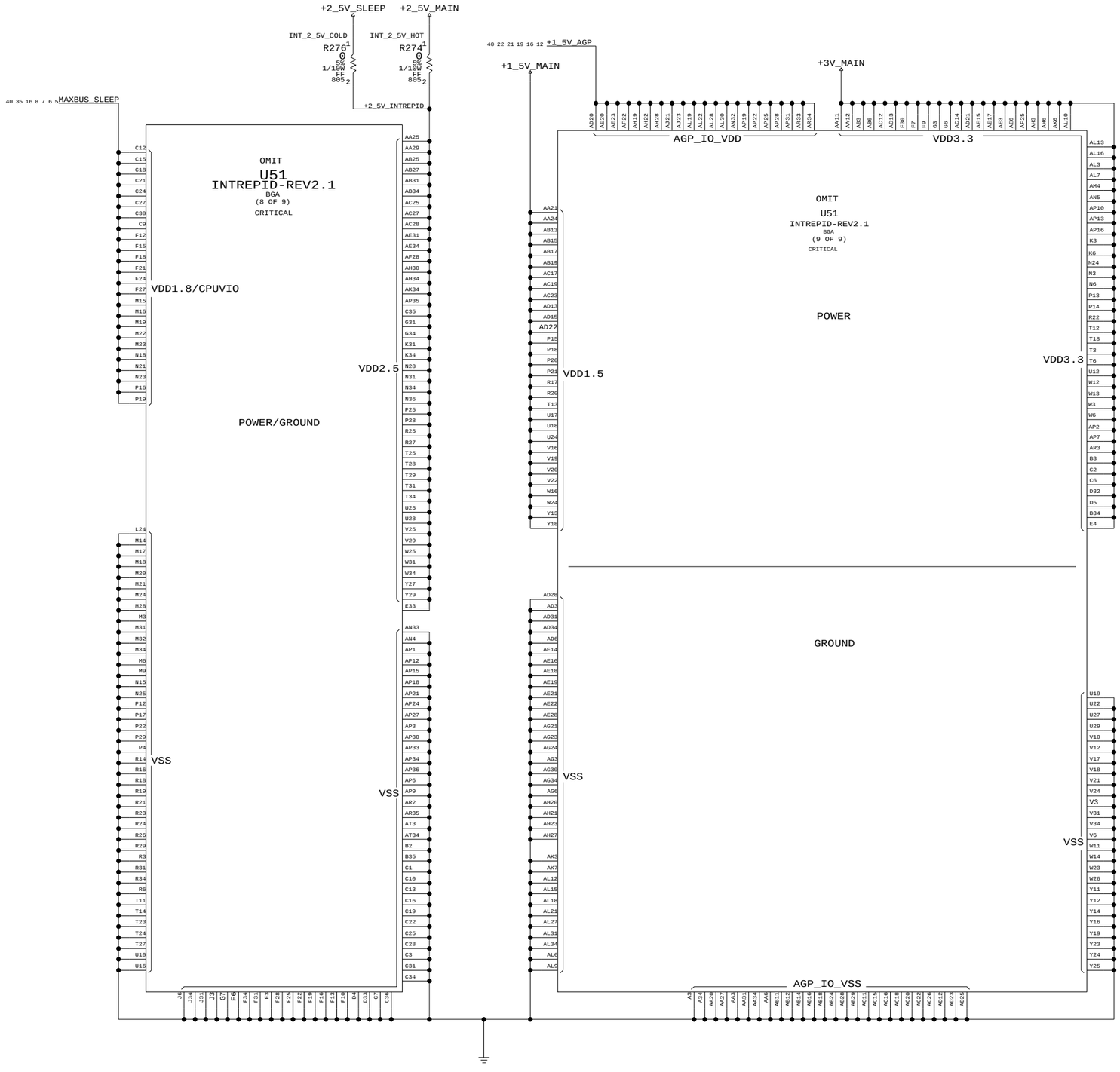
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y2	CRITICAL	?

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 14 OF 46	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE: NONE

SHT 15 OF 46

INTREPID MAXBUS DECOUPLING

35 15 8 7 6 5 MAXBUS_SLEEP 40

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

C148 10uF, C142 10uF, C144 10uF, C146 10uF
C182 0.22uF, C178 0.22uF, C141 0.22uF, C145 0.22uF, C214 0.22uF, C163 0.22uF, C164 0.22uF, C225 0.22uF, C160 0.22uF, C159 0.22uF
C204 0.22uF, C166 0.22uF, C205 0.22uF, C223 0.22uF, C229 0.22uF, C181 0.22uF, C207 0.22uF, C208 0.22uF, C183 0.22uF, C180 0.22uF
C165 0.22uF, C206 0.22uF, C147 0.22uF, C149 0.22uF, C179 0.22uF, C162 0.22uF, C161 0.22uF, C213 0.22uF

INTREPID CORE DECOUPLING

+1_5V_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C324 10uF, C325 10uF, C201 10uF, C200 10uF
C299 0.22uF, C279 0.22uF, C262 0.22uF, C292 0.22uF, C248 0.22uF, C302 0.22uF, C300 0.22uF, C290 0.22uF, C272 0.22uF, C259 0.22uF
C301 0.22uF, C278 0.22uF, C226 0.22uF, C238 0.22uF, C250 0.22uF, C263 0.22uF, C224 0.22uF, C222 0.22uF, C261 0.22uF, C227 0.22uF
C271 0.22uF, C310 0.22uF, C288 0.22uF, C260 0.22uF, C303 0.22uF, C287 0.22uF, C258 0.22uF, C236 0.22uF, C289 0.22uF

INTREPID AGP I/O DECOUPLING

40 22 21 19 15 12 +1_5V_AGP

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

C381 10uF, C380 10uF, C382 10uF, C379 10uF
C367 0.22uF, C319 0.22uF, C330 0.22uF, C363 0.22uF, C366 0.22uF, C332 0.22uF, C361 0.22uF, C320 0.22uF, C328 0.22uF, C364 0.22uF
C365 0.22uF, C329 0.22uF, C345 0.22uF, C346 0.22uF, C373 0.22uF, C344 0.22uF, C331 0.22uF, C312 0.22uF, C354 0.22uF, C347 0.22uF
C321 0.22uF

INTREPID 3.3V DECOUPLING

+3V_MAIN

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

C378 10uF, C376 10uF, C377 10uF, C375 10uF
C170 0.22uF, C358 0.22uF, C268 0.22uF, C327 0.22uF, C342 0.22uF, C215 0.22uF, C352 0.22uF, C171 0.22uF, C158 0.22uF, C309 0.22uF
C175 0.22uF, C357 0.22uF, C351 0.22uF, C350 0.22uF, C286 0.22uF, C176 0.22uF, C189 0.22uF, C167 0.22uF, C371 0.22uF, C359 0.22uF
C285 0.22uF, C283 0.22uF, C269 0.22uF, C221 0.22uF, C234 0.22uF, C247 0.22uF, C257 0.22uF, C343 0.22uF, C313 0.22uF, C228 0.22uF
C360 0.22uF, C308 0.22uF, C318 0.22uF, C237 0.22uF, C317 0.22uF, C341 0.22uF, C177 0.22uF, C212 0.22uF, C349 0.22uF, C184 0.22uF

INTREPID DDR DECOUPLING

40 15 10 9 +2_5V_INTREPID

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

C314 10uF, C322 10uF, C191 10uF, C202 10uF
C304 0.22uF, C266 0.22uF, C172 0.22uF, C281 0.22uF, C243 0.22uF, C253 0.22uF, C334 0.22uF, C241 0.22uF, C348 0.22uF, C192 0.22uF
C306 0.22uF, C252 0.22uF, C275 0.22uF, C297 0.22uF, C240 0.22uF, C218 0.22uF, C274 0.22uF, C369 0.22uF, C368 0.22uF, C168 0.22uF
C265 0.22uF, C251 0.22uF, C216 0.22uF, C254 0.22uF, C305 0.22uF, C186 0.22uF, C219 0.22uF, C315 0.22uF, C264 0.22uF, C294 0.22uF
C323 0.22uF, C273 0.22uF, C242 0.22uF, C203 0.22uF, C333 0.22uF, C217 0.22uF, C230 0.22uF, C293 0.22uF, C231 0.22uF, C296 0.22uF
C239 0.22uF, C316 0.22uF, C185 0.22uF, C282 0.22uF, C295 0.22uF, C280 0.22uF

INTREPID/MAIN 2.5V DECOUPLING

+2_5V_MAIN

10 X 0.22UF (0402)

C770 0.22uF, C139 0.22uF, C335 0.22uF, C735 0.22uF, C245 0.22uF, C736 0.22uF, C739 0.22uF, C395 0.22uF, C374 0.22uF, C385 0.22uF

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT	OF
NONE	16	46

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

+3V_NEC_VDD 17 40

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN

L7 FERR-EMI-100-OHM SM

R172 0 5% 1/16W MF 603

C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805

40 NEC_AVDD

40 17 +3V_NEC_VDD

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
N10 M12 — AVDD

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

41 39 26 18 12 9 PCI_AD<0>	M5	AD0	
41 39 26 18 12 9 PCI_AD<1>	P5	AD1	
41 39 26 18 12 9 PCI_AD<2>	N5	AD2	
41 39 26 18 12 9 PCI_AD<3>	P4	AD3	
41 39 26 18 12 9 PCI_AD<4>	N4	AD4	
41 39 26 18 12 9 PCI_AD<5>	M3	AD5	
41 39 26 18 12 9 PCI_AD<6>	N3	AD6	
41 39 26 18 12 9 PCI_AD<7>	M1	AD7	
41 39 26 18 12 9 PCI_AD<8>	L2	AD8	
41 39 26 18 12 9 PCI_AD<9>	L1	AD9	
41 39 26 18 12 9 PCI_AD<10>	K2	AD10	
41 39 26 18 12 9 PCI_AD<11>	L3	AD11	
41 39 26 18 12 9 PCI_AD<12>	K1	AD12	
41 39 26 18 12 9 PCI_AD<13>	K3	AD13	
41 39 26 18 12 9 PCI_AD<14>	J2	AD14	
41 39 26 18 12 9 PCI_AD<15>	J1	AD15	
41 39 26 18 12 9 PCI_AD<16>	F2	AD16	
41 39 26 18 12 9 PCI_AD<17>	E3	AD17	
41 39 26 18 12 9 PCI_AD<18>	E1	AD18	
41 39 26 18 12 9 PCI_AD<19>	D3	AD19	
41 39 26 18 12 9 PCI_AD<20>	D1	AD20	
41 39 26 18 12 PCI_AD<21>	D2	AD21	
41 39 26 18 12 PCI_AD<22>	C2	AD22	
41 39 26 18 12 PCI_AD<23>	C1	AD23	
41 39 26 18 12 9 PCI_AD<24>	B4	AD24	
41 39 26 18 12 9 PCI_AD<25>	A4	AD25	
41 39 26 18 12 9 PCI_AD<26>	B5	AD26	
(PCI_AD<27>)	C4	AD27	
41 39 26 18 12 9 PCI_AD<28>	A5	AD28	
41 39 26 18 12 9 PCI_AD<29>	C5	AD29	
41 39 26 18 12 9 PCI_AD<30>	B6	AD30	
41 39 26 18 12 9 PCI_AD<31>	A6	AD31	
39 26 18 12 PCI_CBE<0>	M2	CBE0	
39 26 18 12 PCI_CBE<1>	J3	CBE1	
39 26 18 12 PCI_CBE<2>	F1	CBE2	
39 26 18 12 PCI_CBE<3>	C3	CBE3	
41 39 26 18 12 PCI_PAR	J4	PAR	
41 39 26 18 12 PCI_FRAME_L	F3	FRAME	
41 39 26 18 12 PCI_IRDY_L	F4	IRDY	
41 39 26 18 12 PCI_TRDY_L	G1	TRDY	
41 39 26 18 12 PCI_STOP_L	G3	STOP	
NEC_IDSEL	B3	IDSEL	
41 39 26 18 12 PCI_DEVSEL_L	G2	DEVSEL	
12 NEC_PCI_REQ_L	C6	REQ	
12 NEC_PCI_GNT_L	D6	GNT	
18 PCI_PERR_L	H2	PERR	
18 PCI_SERR_L	H1	SERR	OD
NEC_PCI_INTA_L	C7	INTA	OD
NEC_PCI_INTB_L	B7	INTB	OD
NEC_PCI_INTC_L	A7	INTC	OD
37 12 CLK33M_NEC	A8	PCLK	
17 NEC_IO_RESET_L	B8	VBRSRT	
NEC_CRUN_L	N6	CRUN	
17 NEC_PME_L	D8	PME	OD
17 NEC_MAIN_RESET_L	C8	VCCRST	
NEC_SMI_L_TP	L6	SMI	OD
17 NEC_LEGC	L7	LEGC	

R636 22 5% 1/16W MF 402

Series Rpaks required to facilitate NAND-tree testing

RP45 47 5% 1/16W SM1
NC 1 — 8 NC
14 NEC_PCI_INT 2 — 7 NEC_PCI_INTA_L
3 — 6 NEC_PCI_INTB_L
4 — 5 NEC_PCI_INTC_L

R617 4.7k 5% 1/16W MF 402

RP44 47 5% 1/16W SM1
31 28 25 24 IO_RESET_L 1 — 8 NEC_IO_RESET_L 17
41 31 26 14 PMU_PME_L 2 — 7 NEC_PME_L 17
41 31 26 20 19 18 14 MAIN_RESET_L 3 — 6 NEC_MAIN_RESET_L 17
17 NEC_LEGC 4 — 5

VSS
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 D12 G4 J11 F11 D8

Y1's LOAD CAPACITANCE = 16 pF
OMIT
CRITICAL
Y1 30.0000M 8X4.5MM-SM
NEC_XT2_R

C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

XT1/SCLK L9 NEC_XT1
XT2 P8 NEC_XT2

R613 43.2 1% 1/16W MF 402 — NEC_USB_DAM 27 39 41
R612 43.2 1% 1/16W MF 402 — NEC_USB_DAP 27 39 41
R609 43.2 1% 1/16W MF 402 — NEC_USB_DBM 27 39 41
R610 43.2 1% 1/16W MF 402 — NEC_USB_DBP 27 39 41

Low/Full/High Speed (External)
Low/Full/High Speed (External)

RSDM1 M14 NEC_USB_RSDM1
DM1 M13 (NEC_USB_DAM)
DP1 L14 (NEC_USB_DAP)
RSDP1 K13 NEC_USB_RSDP1
RSDM2 K14 NEC_USB_RSDM2
DM2 K12 (NEC_USB_DBM)
DP2 J14 (NEC_USB_DBP)
RSDP2 J12 NEC_USB_RSDP2
RSDM3 H11 NC
DM3 G11
DP3 G13
RSDP3 G14 NC
RSDM4 F12 NC
DM4 F14
DP4 E12
RSDP4 E14 NC
RSDM5 E13 NC
DM5 D14
DP5 C13
RSDP5 C14 NC

RREF P11 NEC_RREF — R614 9.09K 1% 1/16W MF 402 — NEC_AVSS_F 17
Tie to GND (NEC_AVSS_F) at ball N11

OCI1 B12 NEC_LUSB_OCI
OCI2 B11 NEC_RUSB_OCI
OCI3 B10 NEC_OCI<3>
OCI4 A10 NEC_OCI<4>
OCI5 B9 NEC_OCI<5>

RP43 10K 5% 1/16W SM1 (3 — 6)
RP43 10K 5% 1/16W SM1 (4 — 5)
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402

PPON1 C12 OUT NEC_LUSB_PPON 41
PPON2 A11 OUT NEC_RUSB_PPON 41
PPON3 C11 OUT NEC_PPON3_TP
PPON4 C10 OUT NEC_PPON4_TP
PPON5 A9 OUT NEC_PPON5_TP
NC1 P6 NEC_NC<1>
NC2 M6 NEC_NC<2>

+3V_NEC_VDD 17 40

NEC documentation indicates that NCs must be tied high.

NTEST1 M8 IPD NC
SMC M7 IPD NC
TEB N7 IPD NC
AMC P7 IPD NEC_AMC_TP
TEST L8 IPD NC

NANDTEST M10 NEC_NANDTESTEN_TP
SRCLK M9 NC
SRDTA N9 NEC_NANDTESTOUT_TP
SRMOD P9 IPD NC
AVSS(R) N11 P13 M12 AVSS
NEC_AVSS_F 1 — R798 0 5% 1/16W MF 603 — 2

+3V_MAIN

RP43 10K 5% 1/16W SM1 (7 — 2)
RP43 10K 5% 1/16W SM1 (8 — 1)

R607 0 5% 1/16W MF 402
17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 27 41

R608 0 5% 1/16W MF 402
17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 27 41

NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. E
SCALE NONE | SHT 17 OF 46

PCI1510 PULL-UPS

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

INTEGRATED PULL-UP

PC CARD/CARDBUS CONNECTOR

CRITICAL
J5
QT500806-L111
M-ST-SM1

CRITICAL
U8
PCI1510GGU
BGA
CLAMP FOR PC-CARD
CLAMP FOR PCI

U4
TPS2211
SSOI

CRITICAL

CARDBUS

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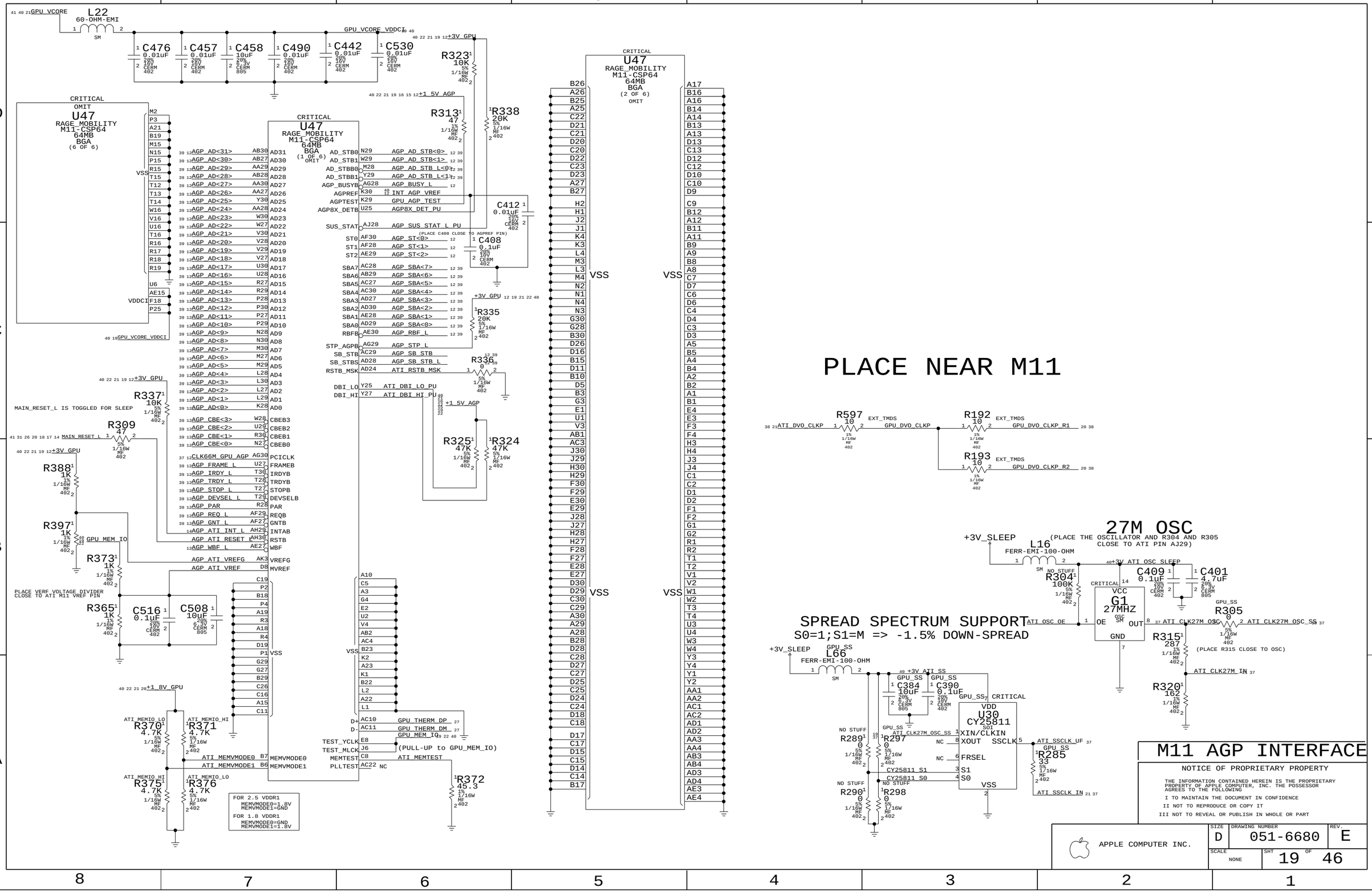
SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 18 OF 46	


GPU_VCORE
L22
60-OHM-EMI
SM
C476 0.01uF
C457 0.01uF
C458 10uF
C490 0.01uF
C442 0.01uF
C530 0.01uF
GPU_VCORE_VDDCI
+3V_GPU
R323 10K
+1.5V_AGP
R313 47
R338 20K
CRITICAL
OMIT
U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(6 OF 6)
(1 OF 6)
(2 OF 6)
VSS
VDDCI
AGP_AD<31>
AGP_AD<30>
AGP_AD<29>
AGP_AD<28>
AGP_AD<27>
AGP_AD<26>
AGP_AD<25>
AGP_AD<24>
AGP_AD<23>
AGP_AD<22>
AGP_AD<21>
AGP_AD<20>
AGP_AD<19>
AGP_AD<18>
AGP_AD<17>
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AGP_AD<14>
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AGP_AD<12>
AGP_AD<11>
AGP_AD<10>
AGP_AD<9>
AGP_AD<8>
AGP_AD<7>
AGP_AD<6>
AGP_AD<5>
AGP_AD<4>
AGP_AD<3>
AGP_AD<2>
AGP_AD<1>
AGP_AD<0>
AD_STB0
AD_STB1
AD_STBB0
AD_STBB1
AGP_BUSYB
AGPREF
AGPTEST
AGP8X_DETB
SUS_STAT
ST0
ST1
ST2
SBA7
SBA6
SBA5
SBA4
SBA3
SBA2
SBA1
SBA0
RBFB
STP_AGPB
SB_STB
SB_STBS
RSTB_MSK
DBI_LO
DBI_HI
AGP_AD_STB<0>
AGP_AD_STB<1>
AGP_AD_STB_L<0>
AGP_AD_STB_L<1>
AGP_BUSY_L
INT_AGP_VREF
GPU_AGP_TEST
AGP8X_DET_PU
AGP_SUS_STAT_L_PU
AGP_ST<0>
AGP_ST<1>
AGP_ST<2>
AGP_SBA<7>
AGP_SBA<6>
AGP_SBA<5>
AGP_SBA<4>
AGP_SBA<3>
AGP_SBA<2>
AGP_SBA<1>
AGP_SBA<0>
AGP_RBF_L
AGP_STP_L
AGP_SB_STB
AGP_SB_STB_L
ATI_RSTB_MSK
ATI_DBI_LO_PU
ATI_DBI_HI_PU
C412 0.01uF
C408 0.1uF
(PLACE C408 CLOSE TO AGPREF PIN)
R335 20K
R336 0
R325 47K
R324 47K
CBEB3
CBEB2
CBEB1
CBEB0
PCICLK
FRAMEB
IRDYB
TRDYB
STOPB
DEVSELB
PAR
REQB
GNTB
INTAB
RSTB
WBF
VREFG
MVREF
CLK66M_GPU_AGP
AGP_FRAME_L
AGP_IRDY_L
AGP_TRDY_L
AGP_STOP_L
AGP_DEVSEL_L
AGP_PAR
AGP_REQ_L
AGP_GNT_L
AGP_ATI_INT_L
AGP_ATI_RESET_L
AGP_WBF_L
AGP_ATI_VREFG
AGP_ATI_VREF
MAIN_RESET_L
MAIN_RESET_L IS TOGGLED FOR SLEEP
R309 47
R337 10K
R388 1K
R397 1K
R373 1K
R365 1K
C516 0.1uF
C508 10uF
PLACE VERF VOLTAGE DIVIDER
CLOSE TO ATI M11 VREF PIN
GPU_MEM_IO
+1.8V_GPU
ATI_MEMIO_LO
ATI_MEMIO_HI
R370 4.7K
R371 4.7K
R375 4.7K
R376 4.7K
ATI_MEMVMODE0
ATI_MEMVMODE1
MEMVMODE0
MEMVMODE1
FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V
A10
A23
K1
B22
L2
A22
L1
AC10
AC11
GPU_THERM_DP
GPU_THERM_DM
GPU_MEM_IO
E8
J6
C8
AC22
TEST_YCLK
TEST_MLCK
MEMTEST
PLLTEST
ATI_MEMTEST
(PULL-UP to GPU_MEM_IO)
R372 45.3
PLACE NEAR M11
R597 10
R192 10
R193 10
EXT_TMDS
ATI_DVO_CLKP
GPU_DVO_CLKP
GPU_DVO_CLKP_R1
GPU_DVO_CLKP_R2
27M OSC
+3V_SLEEP
(PLACE THE OSCILLATOR AND R304 AND R305
CLOSE TO ATI PIN AJ29)
L16
FERR-EMI-100-OHM
+3V_ATI_OSC_SLEEP
R304 100K
NO STUFF
C409 0.1uF
C401 4.7uF
G1
27MHZ
VCC
OSC
OE
OUT
GND
ATI_OSC_OE
ATI_CLK27M_OSC
ATI_CLK27M_OSC_SS
R305 0
R315 287
(PLACE R315 CLOSE TO OSC)
R320 162
ATI_CLK27M_IN
SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD
L66
+3V_ATI_SS
C384 10uF
C390 0.1uF
U30
CY25811
SOI
VDD
XIN/CLKIN
XOUT
SSCLK
NC
FRSEL
S1
S0
CY25811_S1
CY25811_S0
R289 0
R297 0
R290 0
R298 0
R285 33
ATI_SSCLK_UF
ATI_SSCLK_IN
M11 AGP INTERFACE
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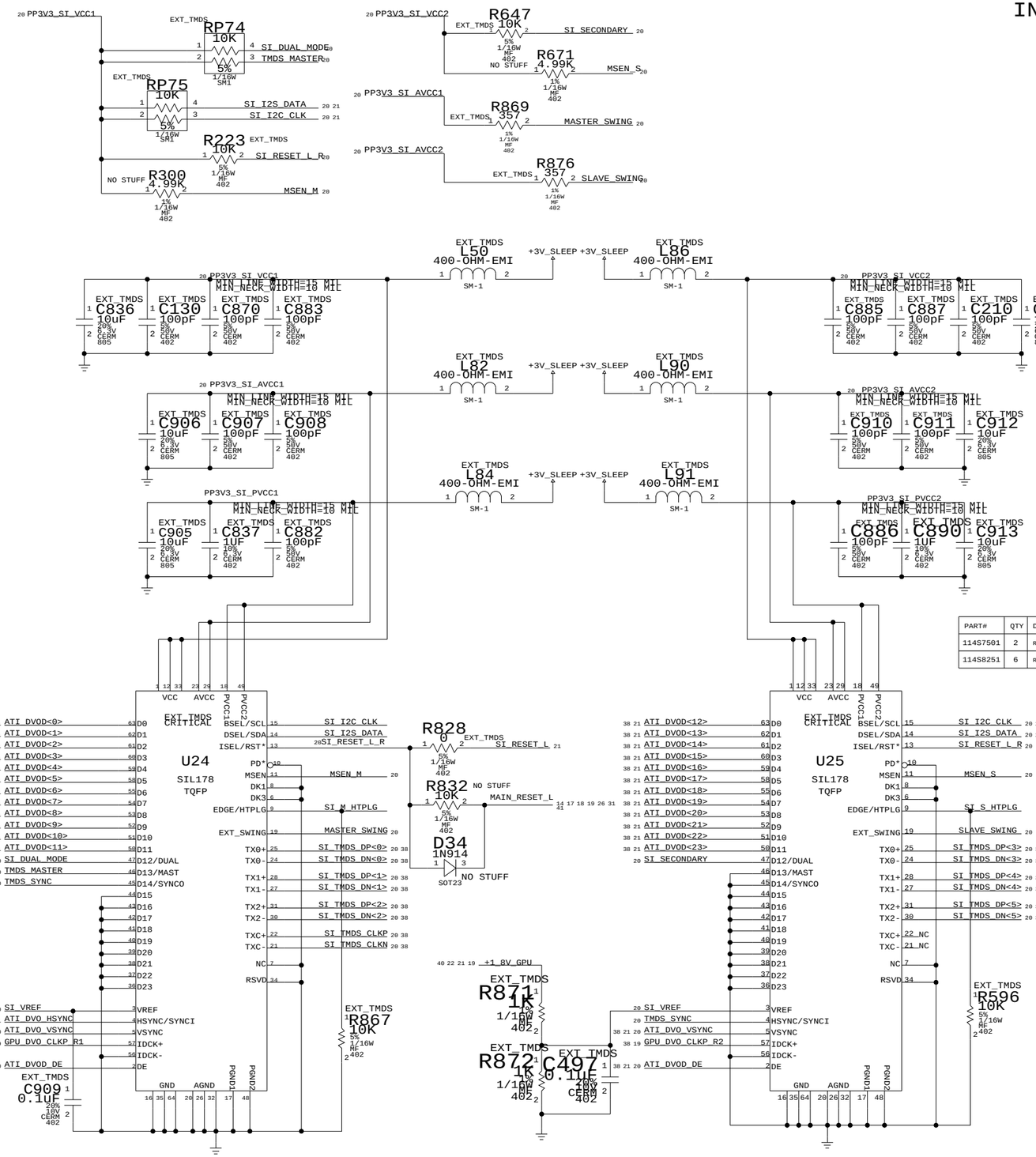
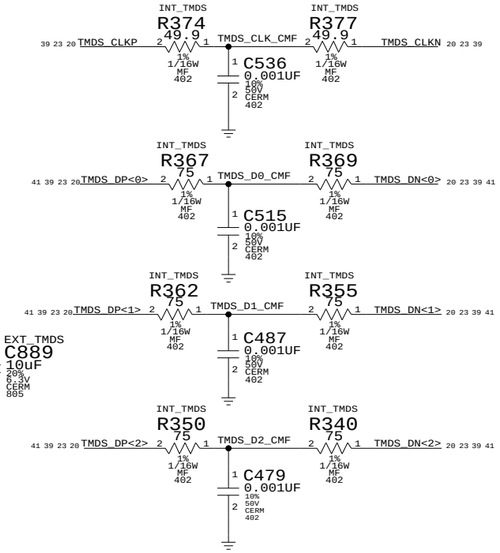
SIZE D
DRAWING NUMBER 051-6680
REV. E
SCALE NONE
SHT 19 OF 46

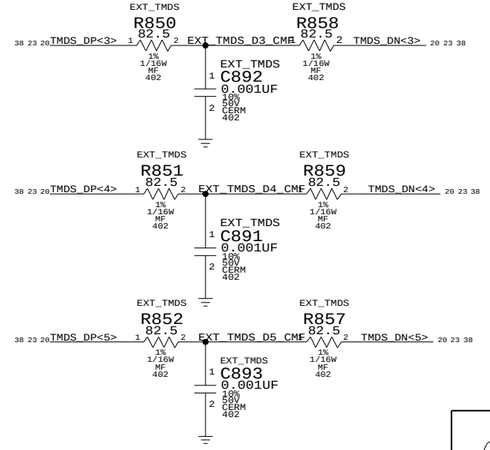


INT/EXT TMDS D<0:2> TERMINATION

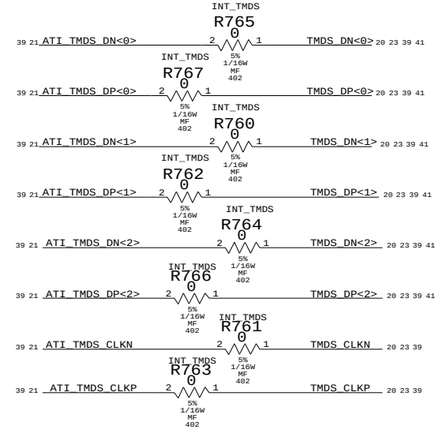


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S7501	2	RES, MF, 1/16W, 75 OHM, 1%, 0402, SMD	R374,R377		EXT_TMDS
114S8251	6	RES, MF, 1/16W, 82.5 OHM, 1%, 0402, SMD	R340,R350,R355,R362,R367,R369		EXT_TMDS

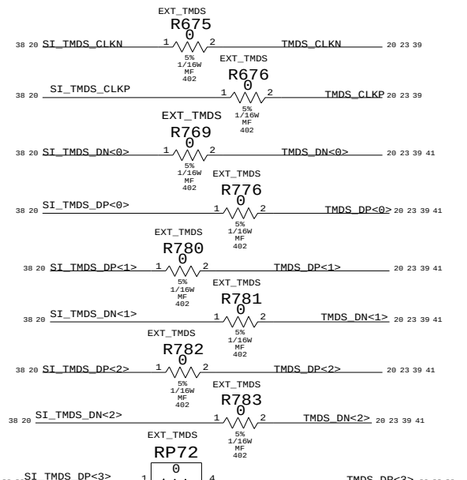
EXT TMDS D<3:5> TERMINATION



ATI INTERNAL TMDS SERIES TERMINATION



SILICON IMAGE TMDS SERIES TERMINATION



INT/EXT TMDS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 20 OF 46	

GPU VCORE - 1.2V

(PUT ALL CAPS BELOW ATI ASIC)

GPU VCORE SUPPLY

M10 Power Shut down Sequencing

PLACE ALL TMDS 0 OHMS close to GPU

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

M11 CORE PWR/LVDS/TMDS

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SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE: NONE

SHT 21 OF 46

GPU PLL - 1.8V

+2_5V_SLEEP → U34 MM1571J SOT-25A (CRITICAL) (150mA MAX)
VIN, VOUT, CONT, NOISE, GND
GPU_CORE_OK
ATI_PVDD_BYP
C830 1uF 20% 10V CERM 603
C553 0.01uF 20% 10V CERM 402
1_8V_PVDD_STD
+1_8V_ATI_PVDD → L20 FERR-220-OHM 0402 → +1_8V_GPU_PLL
R787 0 5% 1/16W MF 402
+1_8V_GPU
C552 10uF 20% 6.3V CERM 805
C418 10uF 20% 6.3V CERM 805
C414 0.1uF 20% 10V CERM 402
C413 0.01uF 20% 10V CERM 402 (21mA)

+2_5V_SLEEP → L23 FERR-220-OHM 0402 → +2_5V_GPU_A2VDD (140mA)
C459 10uF 20% 6.3V CERM 805
C460 0.01uF 20% 10V CERM 402
C461 0.01uF 20% 10V CERM 402

+1_8V_GPU → L21 FERR-220-OHM 0402 → +1_8V_GPU_AVDDQ (2mA)
C464 10uF 20% 6.3V CERM 805
C463 0.01uF 20% 10V CERM 402

+1_8V_GPU → L24 FERR-220-OHM 0402 → +1_8V_GPU_VDDDI (AVDD+VDDDI=75mA)
C478 10uF 20% 6.3V CERM 805
C462 0.01uF 20% 10V CERM 402
C454 0.01uF 20% 10V CERM 402

+2_5V_SLEEP → L28 FERR-220-OHM 0402 → +2_5V_GPU_MCLK
C511 10uF 20% 6.3V CERM 805
C527 0.01uF 20% 10V CERM 402
C472 0.01uF 20% 10V CERM 402

+1_8V_GPU → L19 FERR-220-OHM 0402 → +1_8V_GPU_AVDD (AVDD+VDDDI=75mA)
C427 10uF 20% 6.3V CERM 805
C453 0.01uF 20% 10V CERM 402
C450 0.01uF 20% 10V CERM 402

AK29 PVDD
AF23 AVDD0
AF24 AVDD1
A2VDD0 ← +2_5V_GPU_A2VDD
A2VDD1
A2VDDQ ← +1_8V_GPU_AVDDQ
VDD1DI ← +1_8V_GPU_VDDDI
AF20 VDD2DI
VDDRH0 ← +2_5V_GPU_MCLK
VDDRH1

PVSS AK30
AVSSQ AF22
A2VSSQ AJ22
AVSSN0 AE22
AVSSN1 AE23
A2VSSN0 AE19
A2VSSN1 AE20
VSS1DI AG23
VSS2DI AF19
VSSRH0 F20
VSSRH1 M6

AGP 4X I/O - 1.5V

+1_5V_AGP → L18 FERR-10-OHM-500MA SM
C438 0.1uF 20% 10V CERM 402
C444 0.1uF 20% 10V CERM 402
C423 0.1uF 20% 10V CERM 402
C424 0.1uF 20% 10V CERM 402
C422 10uF 20% 6.3V CERM 805 (20mA)
C439 0.01uF 20% 10V CERM 402
C447 0.01uF 20% 10V CERM 402
C425 0.01uF 20% 10V CERM 402
C417 0.01uF 20% 10V CERM 402

K25
L25
T25
Y28
K27
AA25
K26
L26
M26
N26
P26
R26 VDDP
T26
U26
V26
Y26
AA26
AB26
AC26

MEMORY CORE - 2.5V

+2_5V_SLEEP → L25 FERR-220-OHM 0805 → +2_5V_GPU_MEMCORE (1800mA)
C470 0.1uF 20% 10V CERM 402
C539 0.1uF 20% 10V CERM 402
C475 0.1uF 20% 10V CERM 402
C419 0.1uF 20% 10V CERM 402
C483 10uF 20% 6.3V CERM 805
C471 0.01uF 20% 10V CERM 402
C538 0.01uF 20% 10V CERM 402
C504 0.01uF 20% 10V CERM 402
C420 0.01uF 20% 10V CERM 402

E5
E6
E12
E13
E18 VDDM
E19
E20
E26
F26

OMIT
CRITICAL
U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(4 OF 6)

F5
G5
H5
J5
K5
L5
M5
N5
P5
R5
T5
U5
V5
W5
Y5
AA5 VDDR1
AB5
AC5
AD5
G26
K6
R6
Y6
AA6
F8
F9
F15
F16
F21
F22
H25
J25
J26

LVDS PLL - 1.8V

+1_8V_ATI_PVDD → L32 FERR-220-OHM 0402 → +1_8V_GPU_PNLPLL (40mA)
C493 10uF 20% 6.3V CERM 805
C468 0.01uF 20% 10V CERM 402
GPU_MEM_IO

E7
H26
E9
E10
E11
E14
E15
E16 VDDR1
E17
E21
E22
E23
E24
E25

MEMORY PLL - 1.8V

+1_8V_ATI_PVDD → L30 FERR-220-OHM 0402 → +1_8V_GPU_MEMPLL
C537 10uF 20% 6.3V CERM 805
C523 0.01uF 20% 10V CERM 402
+1_8V_GPU_TP_PLL
C831 10uF 20% 6.3V CERM 805
C832 0.01uF 20% 10V CERM 402

AK21 LPVDD
AK11 TPVDD
A7 MPVDD

LVDS - 2.5V

+2_5V_SLEEP → L26 FERR-10-OHM-500MA SM → +2_5V_GPU_PNLIO (350mA)
C499 10uF 20% 6.3V CERM 805
C500 0.01uF 20% 10V CERM 402
C473 0.01uF 20% 10V CERM 402

AE16 LVDDR_18
AF16 LVDDR_18
AG16 LVDDR_25
AF17 LVDDR_25

AG12 TXVDDR0
AG13 TXVDDR1
AG14 TXVDDR2
AG15 TXVDDR3

LPVSS AJ21
TPVSS AJ11
MPVSS A6

LVSSR0 AH16
LVSSR1 AG17
LVSSR2 AH17
LVSSR3 AF18

DVOVMODE AH12
TXVSSR1 AH13
TXVSSR2 AH14
TXVSSR3 AH15

LVDS/TMDS - 1.8V

+1_8V_GPU → L29 FERR-220-OHM 0402 → +1_8V_GPU_PNLIO (180mA)
C514 10uF 20% 6.3V CERM 805
C492 0.1uF 20% 10V CERM 402
C496 0.1uF 20% 10V CERM 402
C489 0.1uF 20% 10V CERM 402
C491 0.1uF 20% 10V CERM 402
C501 0.01uF 20% 10V CERM 402
C506 0.01uF 20% 10V CERM 402

VDDR4: AF6 AE7 AF7 AE8
VDDR3: AF8 AE9 AF9 AF10 AD25 AE25 AE26 AF26

MEMORY I/O

+2_5V_SLEEP → U60 MM1571J SOT-25A (CRITICAL) (150mA MAX)
VIN, VOUT, CONT, NOISE, GND
GPU_CORE_OK
ATI_TPVDD_BYP
C833 1uF 20% 10V CERM 603
C834 0.01uF 20% 10V CERM 402
+1_8V_ATI_TPVDD → L75 FERR-220-OHM 0402 → +1_8V_GPU_TP_PLL
R788 0 5% 1/16W MF 402
1_8V_TPVDD_STD
C835 10uF 20% 6.3V CERM 805
GPU_MEM_IO
L31 FERR-220-OHM 0805

(1200mA) GPU_MEM_IO_FLT
C551 10uF 20% 6.3V CERM 805
C421 0.1uF 20% 10V CERM 402
C456 0.1uF 20% 10V CERM 402
C488 0.1uF 20% 10V CERM 402
C517 0.1uF 20% 10V CERM 402
C546 0.1uF 20% 10V CERM 402
C545 0.1uF 20% 10V CERM 402
C544 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C541 0.1uF 20% 10V CERM 402
C436 0.1uF 20% 10V CERM 402
C437 0.1uF 20% 10V CERM 402
C540 0.1uF 20% 10V CERM 402
C547 0.1uF 20% 10V CERM 402
C542 0.01uF 20% 10V CERM 402

1.8V DVO POWER (EXT.TMDS)

+1_8V_GPU → EXT_TMDS L81 FERR-10-OHM-500MA SM → +1_8V_GPU_DVO
C535 10uF 20% 6.3V CERM 805
C519 0.1uF 20% 10V CERM 402
C534 0.1uF 20% 10V CERM 402
C521 0.1uF 20% 10V CERM 402
INT_TMDS R843 0 5% 1/16W MF 603
+3V_GPU → L33 FERR-10-OHM-500MA SM → +3V_GPU_FLT
C550 10uF 20% 6.3V CERM 805
C518 0.1uF 20% 10V CERM 402
C520 0.1uF 20% 10V CERM 402
C430 0.1uF 20% 10V CERM 402
C880 0.1uF 20% 10V CERM 402
C881 0.1uF 20% 10V CERM 402
C426 0.1uF 20% 10V CERM 402
EXT_TMDS R842 0 5% 1/16W MF 402 ← +1_8V_GPU
INT_TMDS R841 0 5% 1/10W MF 402 ← ATI_DVOVMODE

1.5V

+1_5V_SLEEP → R275 0 5% 1/10W FF 805 → +1_5V_AGP

1.8V

+1_8V_SLEEP → R363 0 5% 1/10W FF 805 → +1_8V_GPU

2.5V

+1_8V_SLEEP, +2_5V_SLEEP → R312 0 5% 1/10W FF 805 (ATI_MEMIO_LO), R319 0 5% 1/10W FF 805 (ATI_MEMIO_HI) → GPU_MEM_IO

3.3V

+3V_SLEEP → R379 0 5% 1/10W FF 805 → +3V_GPU

3.3V IO SUPPLY

(Max Current varies, depends on usage)

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA,HYNIX GC	U47	CRITICAL	ATI_128MB
338S0207	1	IC,ATI,M11-CSP64,GRAPHICTLR,667BGA,HYNIX MEM	U47	CRITICAL	ATI_64MB

M11 POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 22 OF 46	

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN
74AHC1G32 U40 (SM, 32) — OMIT L38 FERR-60-OHM-0.1A 0402
21 ATI_VSYNC → ATI_VSYNC_BUF → 2 VGA_VSYNC 23 41
PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR
+3V_MAIN
74AHC1G32 U39 (SM, 32) — OMIT L36 FERR-60-OHM-0.1A 0402
21 ATI_HSYNC → ATI_HSYNC_BUF → 2 VGA_HSYNC 23 41

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L37 370-OHM SM SYM_VER-1
39 20 TMDS_CLKP ↔ TMDS_CONN_CLKP 23 38 41
39 20 TMDS_CLKN ↔ TMDS_CONN_CLKN 23 38 41

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

FL1 LCFILTER SM-220MHZ CRITICAL — 38 21 GPU_B → VGA_B 23 41
FL2 LCFILTER SM-220MHZ CRITICAL — 38 21 GPU_G → VGA_G 23 41
FL3 LCFILTER SM-220MHZ CRITICAL — 38 21 GPU_R → VGA_R 23 41
C641 3.3pF 0.25pF 50V CERM 402
C634 3.3pF 0.25pF 50V CERM 402
C631 3.3pF 0.25pF 50V CERM 402
R462 75 1% 1/16W MF 402 NO STUFF
R458 75 1% 1/16W MF 402 NO STUFF
R456 75 1% 1/16W MF 402 NO STUFF

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F2 0.5AMP-13.2V CRITICAL SM → +5V_DDC_SLEEP_UF → L42 400-OHM-EMI SM-1 → +5V_DDC_SLEEP 40 41

DVI CONNECTOR

J22 QHI112 F-RT-TH CRITICAL — CHGND1 / CHGND2
L45 90-OHM-300mA 2012H CRITICAL SYM_VER-1
41 39 20 TMDS_DN<0> ↔ TMDS_CONN_DN<0> 23 38
41 39 20 TMDS_DP<0> ↔ TMDS_CONN_DP<0> 23 38
38 23 TMDS_CONN_DN<5>
38 23 TMDS_CONN_DP<5>
TMDS_CONN_DN<2> 23 38
TMDS_CONN_DN<1> 23 38
TMDS_CONN_DP<2> 23 38
TMDS_CONN_DP<1> 23 38
TMDS_CONN_DN<4> 23 38
TMDS_CONN_DN<3> 23 38
TMDS_CONN_DP<4> 23 38
TMDS_CONN_DP<3> 23 38
41 23 DVI_DDC_CLK_UF
(+5V_DDC SLEEP)
41 23 DVI_DDC_DATA_UF
41 38 23 TMDS_CONN_CLKP
41 38 23 TMDS_CONN_CLKN
VGA_VSYNC 23 41
41 23 DVI_HPD_UF
41 23 VGA_B
41 23 VGA_HSYNC
VGA_R 23 41
VGA_G 23 41
C5B
C5A

PLACE NEAR C5A & C5B
R464 0 5% 1/16W MF 402
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19
CHGND1

C667 0.01UF 20% 50V CERM 603
C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C653 100pF 5% 25V CERM 201

DVI DDC ISOLATION

Isolation required for DVI power switch

D19 MBR0530 SM — DDC_CLK_ISO
R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402 — DVI_DDC_CLK
R477 100 5% 1/16W MF 402 — 2 DVI_DDC_DATA
R469 100 5% 1/16W MF 402 — DVI_HPD

3V LEVEL SHIFTERS

+3V_SLEEP
Q39 2N7002DW SOT-363 — DVI_DDC_CLK ↔ GPU_DVI_DDC_CLK 41
Q39 2N7002DW SOT-363 — 2 DVI_DDC_DATA ↔ GPU_DVI_DDC_DATA 41
Q40 2N7002DW SOT-363 — DVI_HPD ↔ GPU_HPD 21
R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON low. As host rails rise, TP0610 will turn off, and DDC CLK remote device path will be disabled as well.

Q38 TP0610 SM — 41 23 DVI_DDC_CLK_DF ↔ DVI_TURN_ON
41 40 23 +5V_DDC_SLEEP
R473 680 5% 1/16W MF 402
R459 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
R460 10K 5% 1/16W MF 402 — DVI_TURN_ON_TLM
Q35 MMDT3904 SOT-363 — DVI_TURN_ON_BASE
SOFT_PWR_ON_L 24 31 35 41

+3V_SLEEP
Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP
R485 68.1K 1% 1/16W MF 402
C668 0.1UF 20% 10V CERM 402
GPIO.
HPD_4V_REF
U42 LMC7211 SM — V+ / V-
R472 10K 1% 1/16W MF 402 — 41 23 DVI_HPD_UF ↔ DVI_HPD_DIV
R482 10K 1% 1/16W MF 402
R484 100K 1% 1/16W MF 402
R475 10K 5% 1/16W MF 402 — HPD_PWR_SW_BASE
Q35 MMDT3904 SOT-363
HPD_PWR_SW
R470 330 5% 1/16W MF 402
HPD_REF_EN_L
Q40 2N7002DW SOT-363
21 HPD_PWR_SNS_EN
R483 470K 5% 1/16W MF 402

CRITICAL L47 90-OHM-300mA 2012H SYM_VER-1 — EXT_TMDS
38 23 TMDS_CONN_DN<2> ↔ TMDS_DN<2> 20 39 41
38 23 TMDS_CONN_DP<2> ↔ TMDS_DP<2> 20 39 41
CRITICAL L46 90-OHM-300mA 2012H SYM_VER-1
38 23 TMDS_CONN_DN<1> ↔ TMDS_DN<1> 20 39 41
38 23 TMDS_CONN_DP<1> ↔ TMDS_DP<1> 20 39 41
CRITICAL L44 90-OHM-300mA 2012H SYM_VER-1 — EXT_TMDS
38 20 TMDS_DN<3> ↔ TMDS_CONN_DN<3> 23 38
38 20 TMDS_DP<3> ↔ TMDS_CONN_DP<3> 23 38
CRITICAL L49 90-OHM-300mA 2012H SYM_VER-1 — EXT_TMDS
38 20 TMDS_DN<4> ↔ TMDS_CONN_DN<4> 23 38
38 20 TMDS_DP<4> ↔ TMDS_CONN_DP<4> 23 38
CRITICAL L85 90-OHM-300mA 2012H SYM_VER-1 — EXT_TMDS
38 20 TMDS_DN<5> ↔ TMDS_CONN_DN<5> 23 38
38 20 TMDS_DP<5> ↔ TMDS_CONN_DP<5> 23 38

LCD INTERFACE

LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN
R347 100K 5% 1/16W MF 402
C474 2200pF 10% 50V CERM 603
R354 100K 5% 1/16W MF 402 — LCD_PWREN_L
LCD_DIGON_L
Q28 2N7002 SM — 23 21 FP_PWR_EN
Q29 SI3443DV TSOP — +3V_LCD_SW → L27 FERR-250-OHM SM → +3V_LCD 41 40 (LVDS DDC POWER)
+3V_SLEEP
C548 0.001UF 10% 50V CERM 402 — CHGND4
C503 0.001UF 10% 50V CERM 402 — CHGND4
C701 0.001UF 10% 50V CERM 402
C702 0.001UF 10% 50V CERM 402 — NO STUFF
C549 0.001UF 10% 50V CERM 402 — CHGND4
R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402

CRITICAL J14 G-501973 F-RT-SM
NC
23 21 41 LVDS_DDC_CLK
23 21 41 LVDS_DDC_DATA
39 21 41 LVDS_L0N
39 21 41 LVDS_L0P
39 21 41 LVDS_L1N
39 21 41 LVDS_L1P
41 39 21 LVDS_L2N
41 39 21 LVDS_L2P
41 39 21 CLKLVDS_LN
41 39 21 CLKLVDS_LP
LVDS_DDC_CLK 23 41
LVDS_DDC_DATA 23 41

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM — 1 +14V_INV
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW
L74 400-OHM-EMI SM-1
R750 100K 5% 1/16W MF 402 — FP_PWR_EN_L
C812 0.001UF 20% 50V CERM 402
C813 10UF 20% 6.3V CERM 805
CRITICAL J4 SM-2MT
Q76 FDG6324L SC70-6 — 23 21 FP_PWR_EN
C815 0.001UF 20% 50V CERM 402
41 40 +5V_INV_SW
L72 400-OHM-EMI SM-1 — 2 41 BRIGHT_PWM
+3V_MAIN
C816 0.001UF 10% 50V CERM 402
C19 0.001UF 20% 50V CERM 402
41 INV_GND
L1 FERR-250-OHM SM
C22 0.1UF 10% 16V CERM 402
21 INV_ON_PWM
U2 NC7S32 SC70
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
CHGND3

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM — GPU_TV_GND1 → L54 FERR-10-OHM-500MA SM → TV_GND1 40 41
C657 0.01UF 20% 50V CERM 603
GPU_Y → L53 3.3UH 0603
C663 560PF 10% 50V CERM 402
C656 560PF 10% 50V CERM 402
GPU_C → L57 3.3UH 0603
C661 560PF 10% 50V CERM 402
C660 560PF 10% 50V CERM 402
GPU_COMP → L55 3.3UH 0603
C664 560PF 10% 50V CERM 402
C658 560PF 10% 50V CERM 402
CRITICAL J21 MINIDIN RT-TH MH11773-WMR8A
TV_C 41
TV_Y 41
TV_COMP 41
CHGND1
XW14 SM — GPU_TV_GND2 40 → L56 FERR-10-OHM-500MA SM → TV_GND2 40 41
C659 0.01UF 20% 50V CERM 603
Place GND shorts at graphics controller
CHGND1

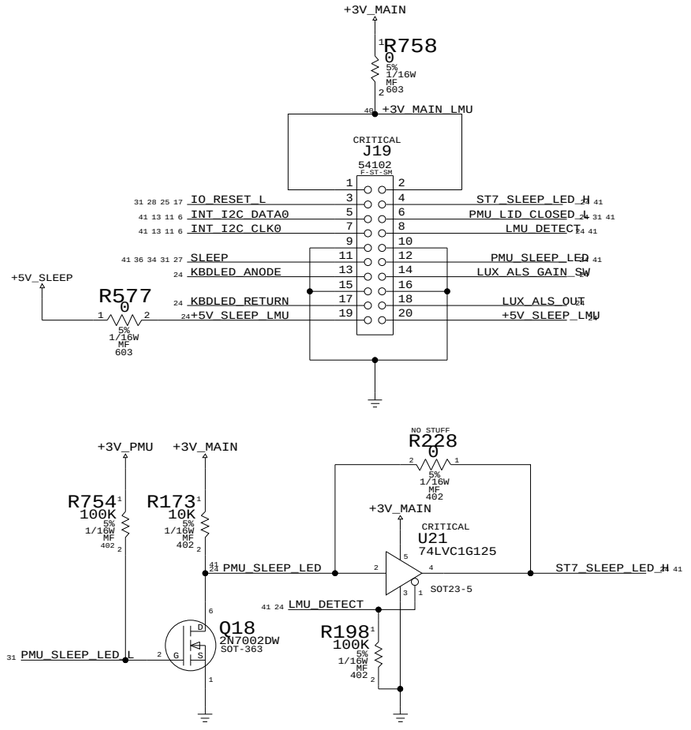
R753 0 5% 1/16W MF 402
C819 0.01UF 20% 50V CERM 603
CHGND3

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

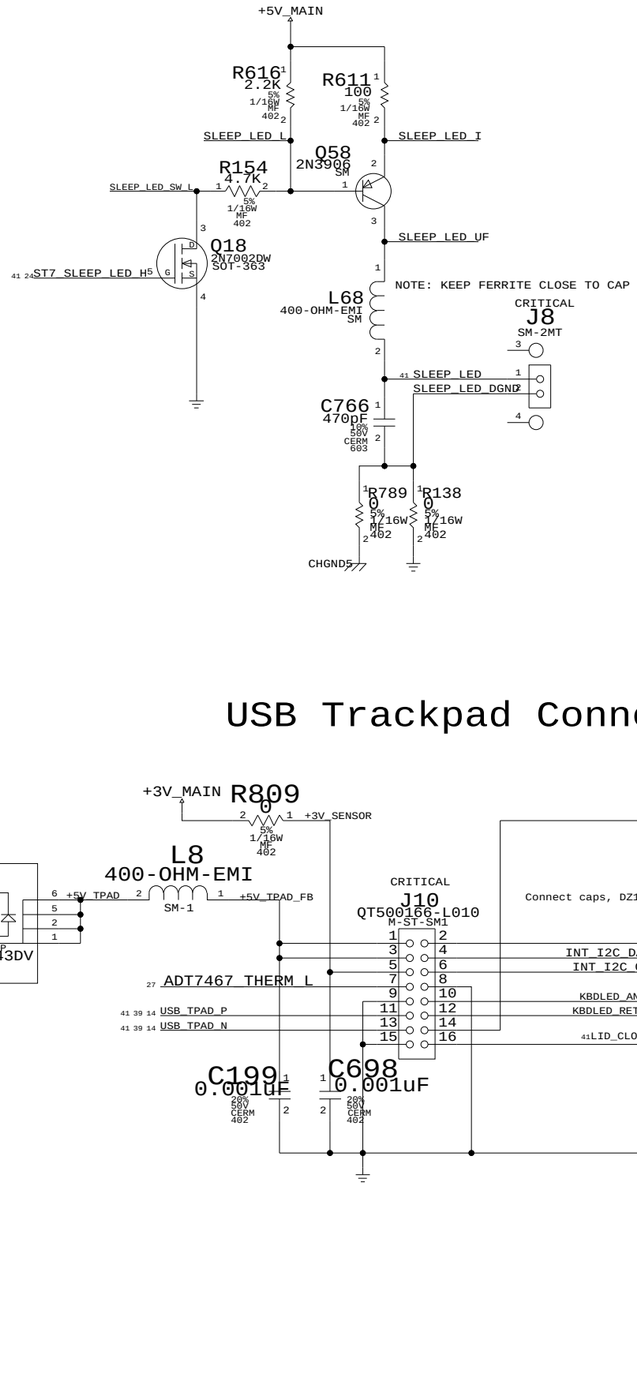
VIDEO CONNECTORS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6680 | REV. E
SCALE NONE | SHT 23 OF 46

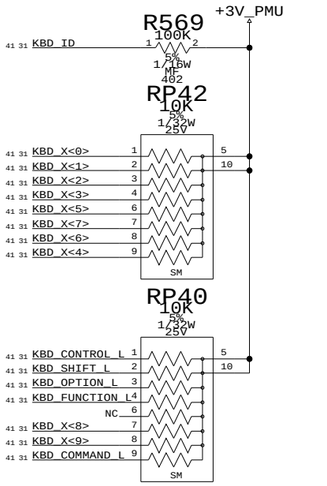
LMU/RIGHT SENSOR CONNECTOR



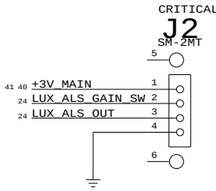
SLEEP LED

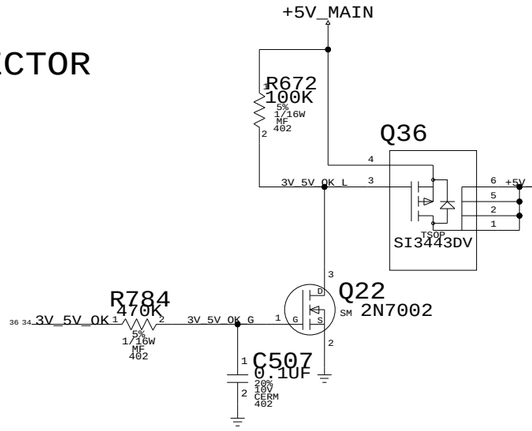


KEYBOARD PULLUPS

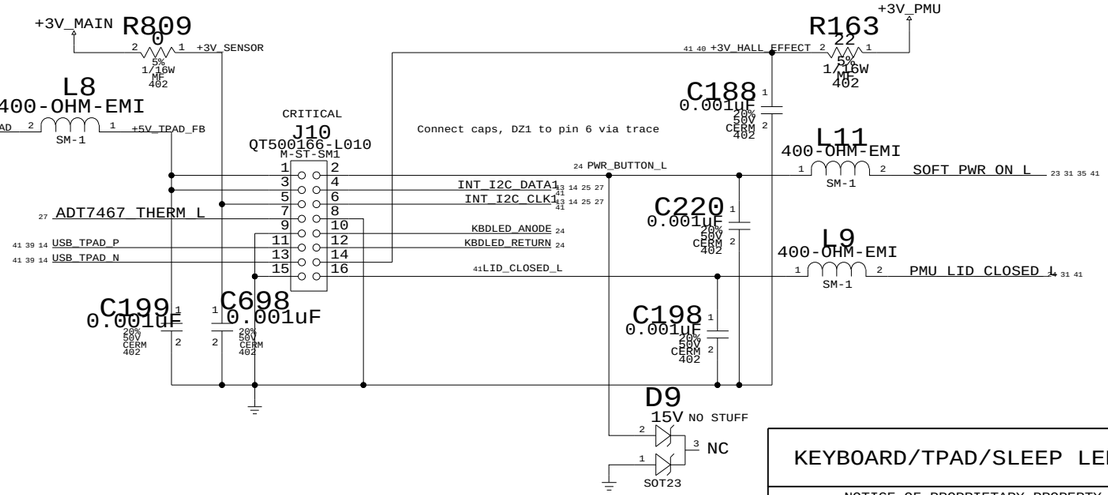


LEFT LIGHT SENSOR CONNECTOR

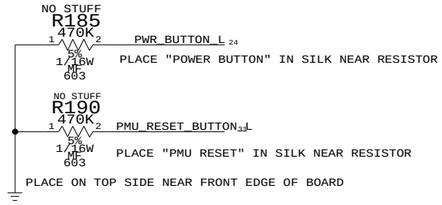




USB Trackpad Connector



DEBUG HELPERS



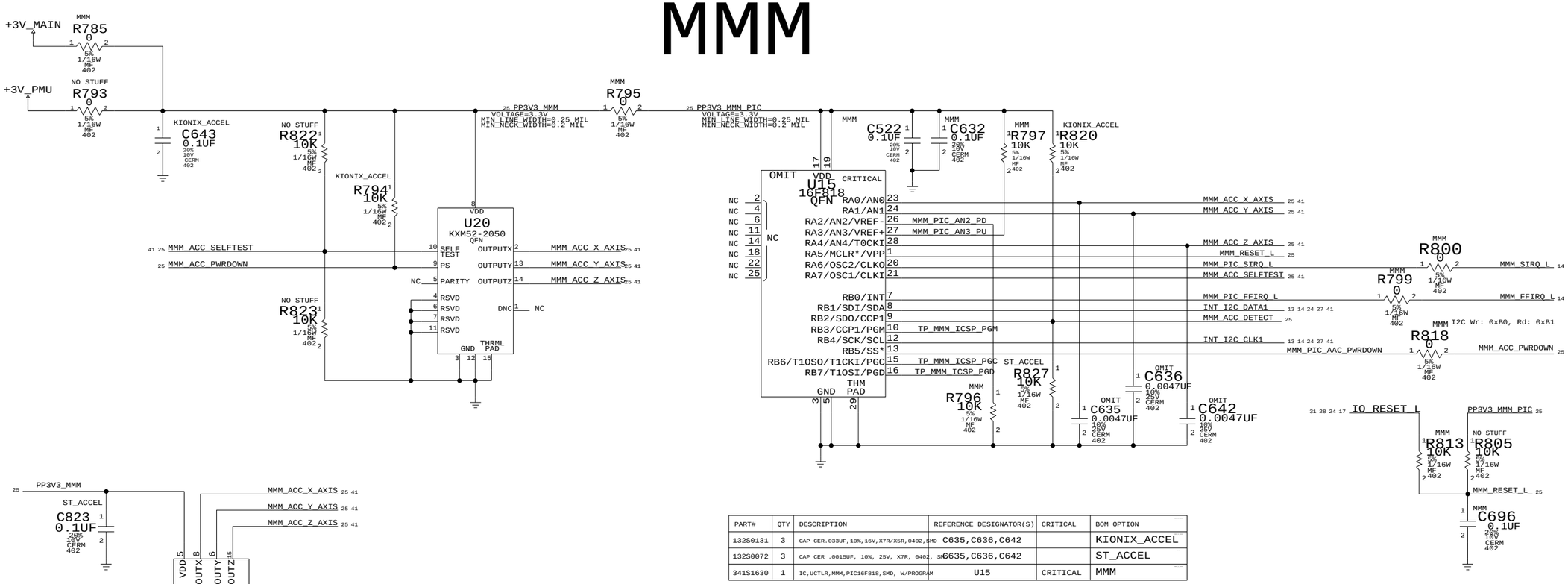
KEYBOARD/TPAD/SLEEP LED

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

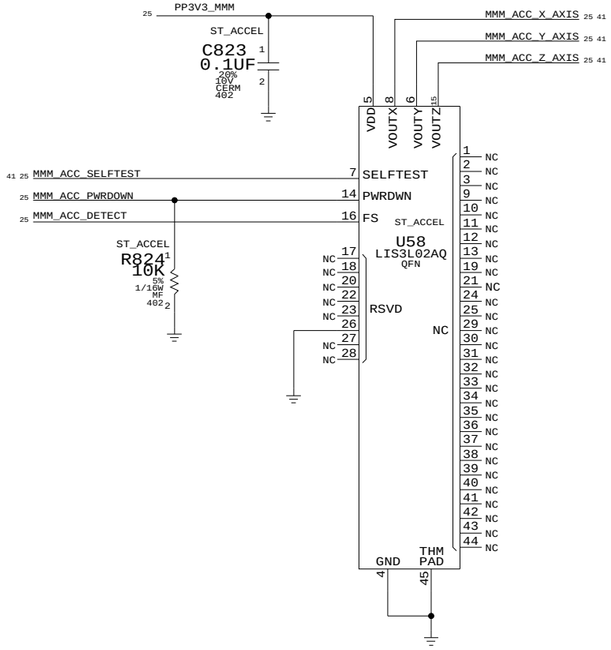
SCALE	SHT	OF
NONE	24	46

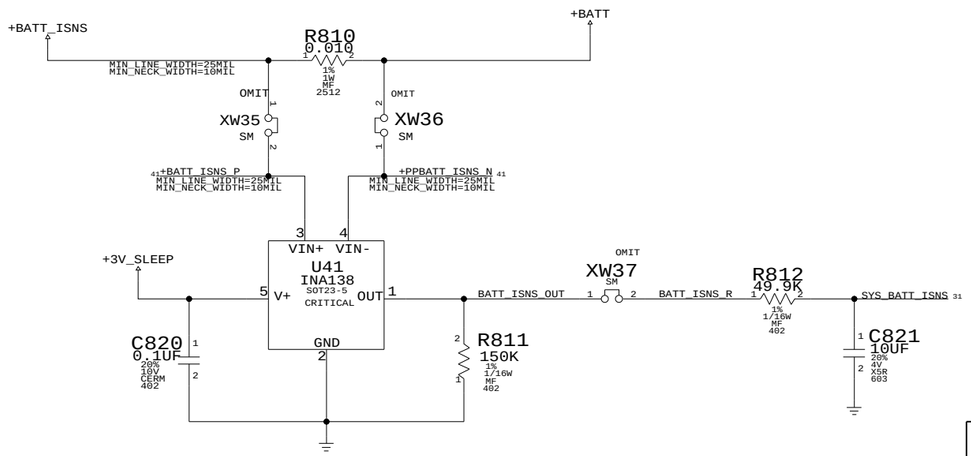
MMM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	CAP CER.033UF,10%,16V,X7R/X5R,0402,SMD	C635,C636,C642		KIONIX_ACCEL
132S0072	3	CAP CER .0015UF, 10%, 25V, X7R, 0402, SM	C635,C636,C642		ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD, W/PROGRAM	U15	CRITICAL	MMM

BATTERY CURRENT SENSE





MMM & BATTERY CURRENT SENSOR

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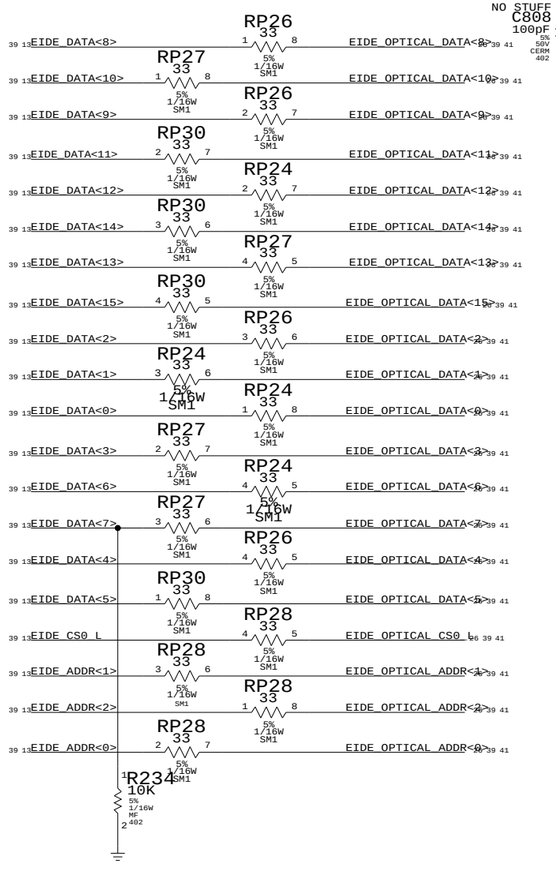
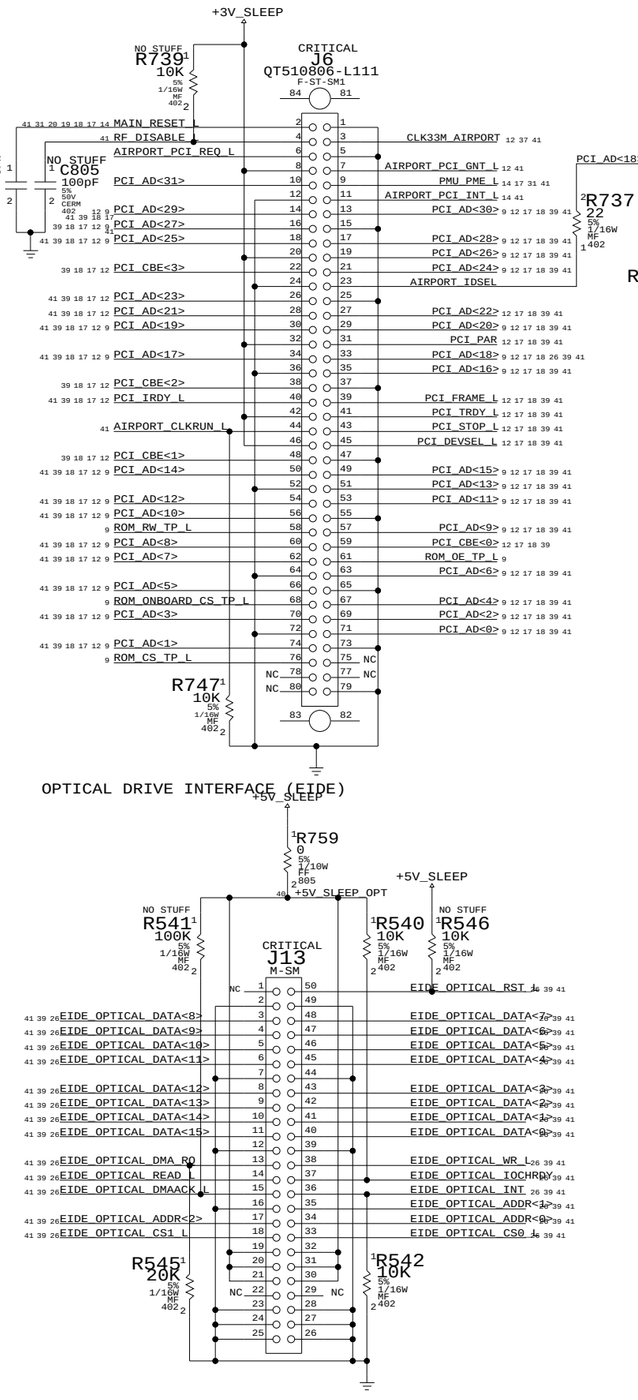
D	051-6680	E
SCALE: NONE	SHT 25 OF 46	

WIRELESS INTERFACE

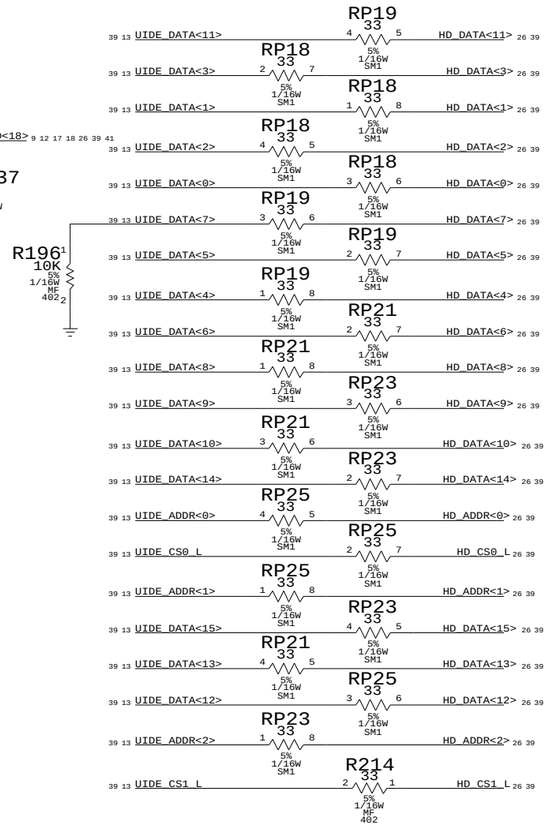
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID



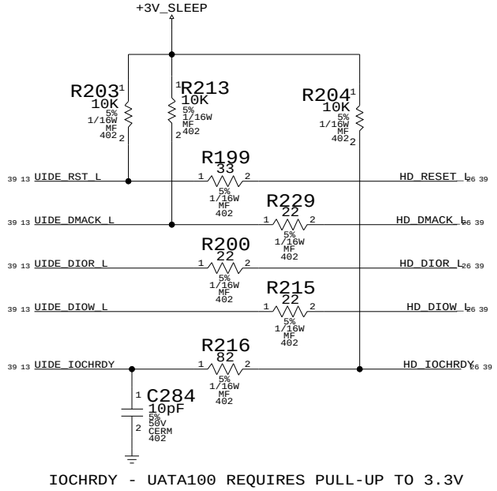
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID

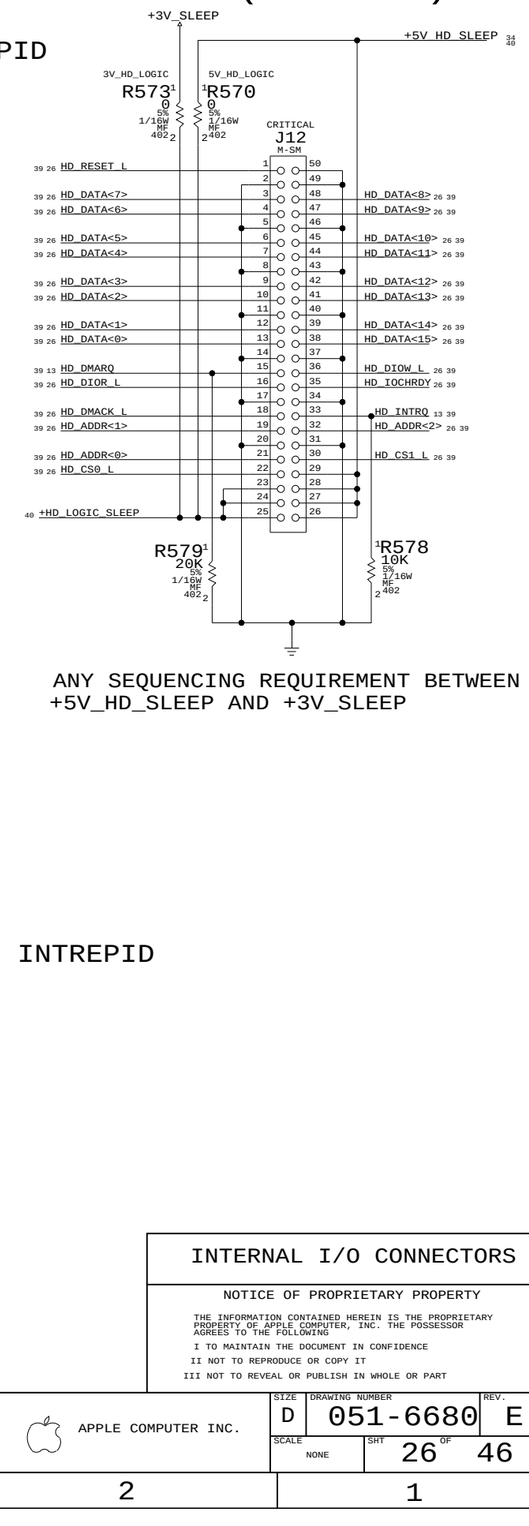


PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

INTERNAL I/O CONNECTORS

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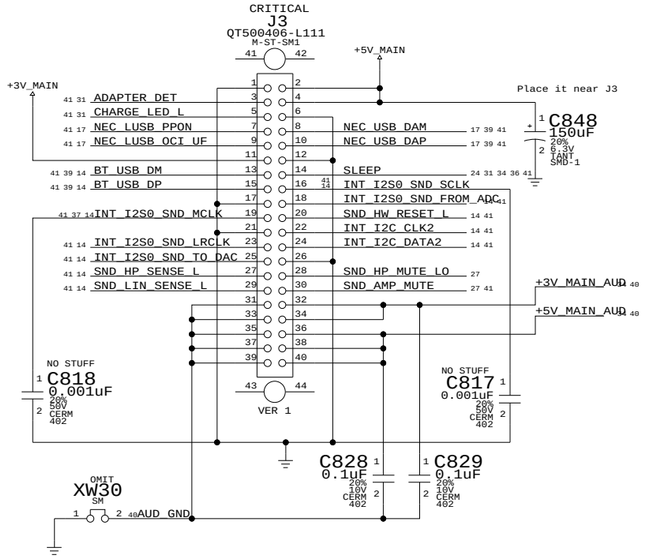
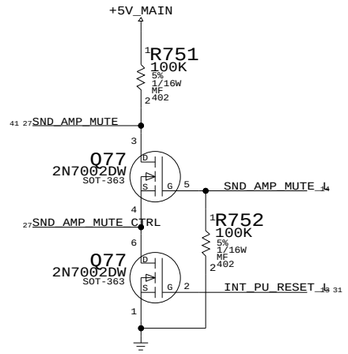
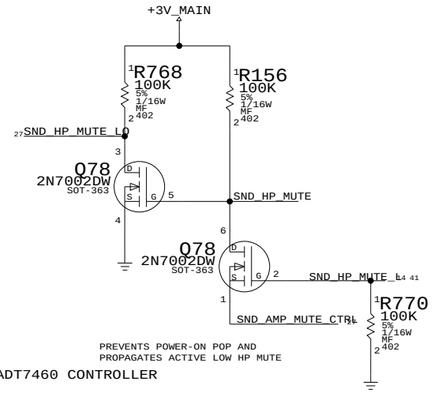
D	051-6680	E
SCALE: NONE	SHT 26 OF 46	

LEFT I/O & AUDIO BOARD (LIO)



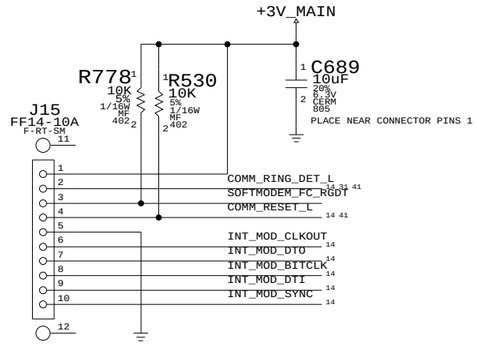


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

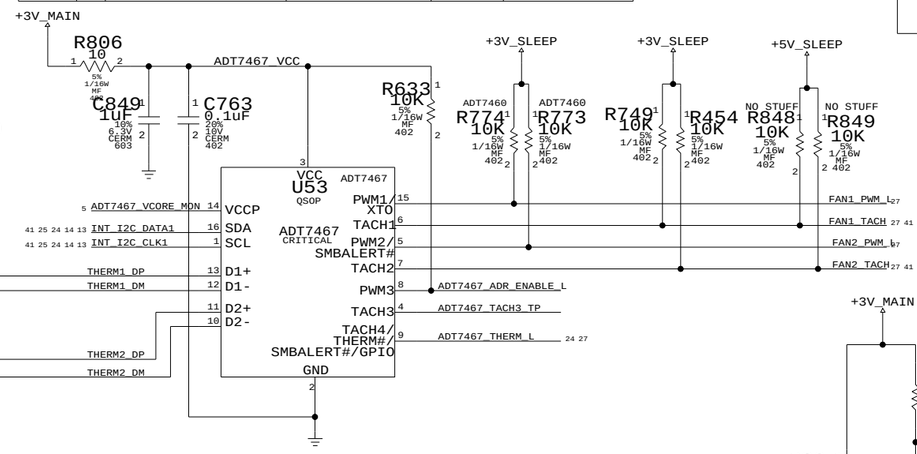
SOFT MODEM CONN



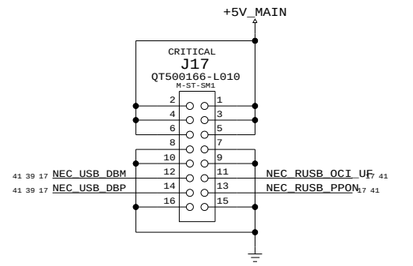
FAN INTERFACE

FAN CONTROLLER

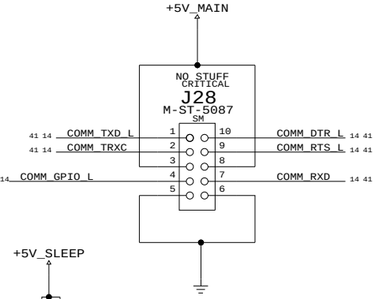
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S0608	1	IC,ADT7460,FAN CTLR,16P QSOP	U53	CRITICAL	ADT7460



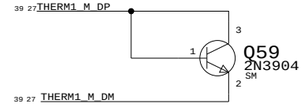
RIGHT USB BOARD



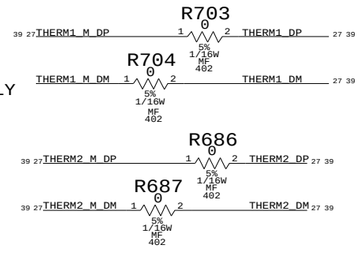
SERIAL DEBUG INTERFACE



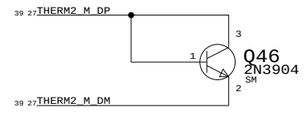
PLACE CLOSE TO CPU
MAIN1



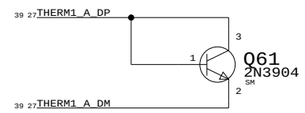
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



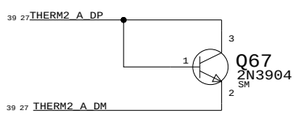
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



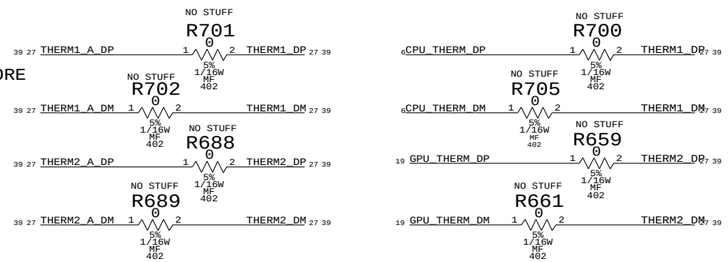
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



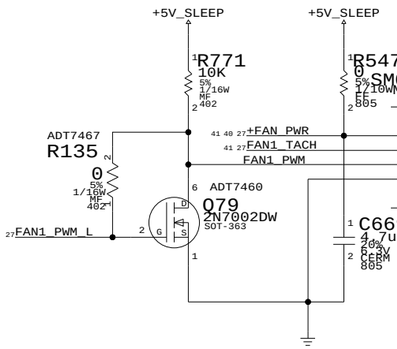
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



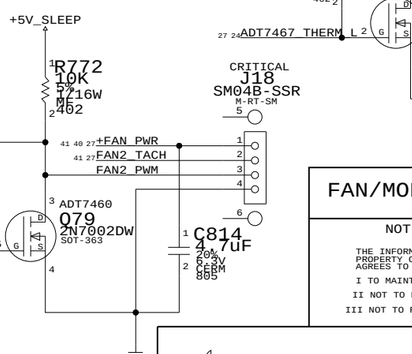
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

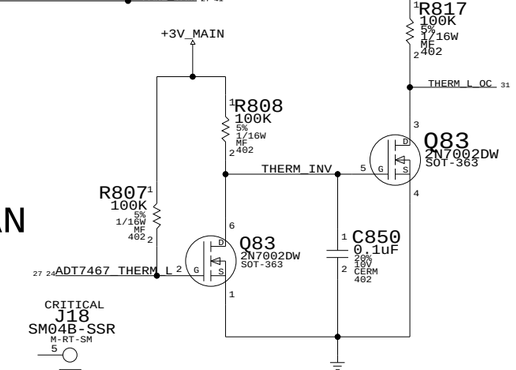


CPU FAN



GPU FAN





FAN/MODEM/SOUND/BACKUP BATT.

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 27 OF 46	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0079	338S0223		U43	ALT FOR 88E1111 B1

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/16W MF 402

3405_MODE

R507 0 5% 1/16W MF 402

U45 LTC3405 SOT23-6 CRITICAL

VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L60 3.3uH SM1

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

C674 10uF 20% 6.3V CERM 805

3405_VFB

R503 182K 1% 1/16W MF 402 R1

+1_0V_MARVELL

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — CLKENET_LINK_TX — CLKENET_PHY_TX

R421 0 5% 1/16W MF 402 — CLKENET_LINK_RX — CLKENET_PHY_RX

R445 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF — CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402 — C852 10pF 5% 50V CERM 402

Keep C851 & C852 Stubs short

U43 88E1111-BDE BCC

TX_CLK, RX_CLK, 125CLK (CRITICAL), CTRL10, NC

DVDD: C594 0.1uF, C601 0.01uF, C608 0.1uF, C619 0.01uF, C603 0.1uF, C599 0.01uF

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

+2_5V_MAIN

R442 0 5% 1/16W FF 805

VDDO: C597 0.1uF, C612 0.01uF, C623 0.1uF, C600 0.01uF, C598 0.1uF, C595 10uF

+2_5V_MARVELL

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C646 0.1uF, C648 0.1uF, C645 0.1uF, C647 0.1uF

PLACE CAPS AT CONNECTOR PINS 5 & 6

VDDOH

VDDOX

L35 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

AVDD: C614 0.1uF, C616 0.1uF, C618 0.1uF, C602 0.01uF, C592 10uF

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

R814 0 5% 1/16W FF 805

+2_5V_MARVELL_CONN

J23 MJ-R0076 F-RT-TH

PRIMARY

ENET_CTAP, ENET_CTAP, MDI_0+, MDI_0-, MDI_1+, MDI_1-, MDI_2+, MDI_2-, MDI_3+, MDI_3-

1CT:1CT, 75 OHM

SECONDARY J1 J2 J3 J4 J5 J6 J7 J8

RJ45 CABLE SIDE

RJ45 CHIP SIDE

CHGND1

SHIELD 1000PF, 2000V

+2_5V_MARVELL

R431 10K 5% 1/16W MF 402

R430 10K 5% 1/16W MF 402

R432 1.5K 5% 1/16W MF 402

R422 1K 5% 1/16W MF 402 — INT_ENET_RST_L

D15 1N914 SOT23 — IO_RESET_L — ENET_RST_L

ENET_COMA

Q32 2N7002DW SOT-363 — AC_IN

Q32 2N7002DW SOT-363 — SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

C611 2.2uF 10% 10V CERM 805

ENET_HSDACP, ENET_HSDACM

CLK25M_ENET_XIN, CLK25M_ENET_XOUT

ENET_VSSC

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R425 20K 5% 1/16W MF 402

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M

CLK25M_XTAL_IN

C604 27pF 5% 50V CERM 402 — C624 27pF 5% 50V CERM 402

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402 — NO STUFF R429 49.9 1% 1/16W MF 402 — R428 10K 5% 1/16W MF 402

R427 4.99K 1% 1/16W MF 402

TX_EN, TX_ER, GTX_CLK

RXD0–RXD7, RX_DV, RX_ER

CRS, COL, MDC, MDIO

INT-/INT+, RESET, COMA

S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-

HSDAC+, HSDAC-

XTAL1, XTAL2, VSSC

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX

CONFIG0–CONFIG6

SEE CONFIG TABLES (BELOW)

TDI, TDO, TCK, TMS, TRST

RSET, SEL_OSC, SEL_2.5V, GND

R433 49.9 1% 1/16W MF 402 — R434 49.9 1% 1/16W MF 402 — MDI0_PD

R435 49.9 1% 1/16W MF 402 — R436 49.9 1% 1/16W MF 402 — MDI1_PD

R437 49.9 1% 1/16W MF 402 — R438 49.9 1% 1/16W MF 402 — MDI2_PD

R439 49.9 1% 1/16W MF 402 — R440 49.9 1% 1/16W MF 402 — MDI3_PD

C622 0.01uF, C613 0.01uF, C615 0.01uF, C617 0.01uF

PLACE RESISTORS CLOSE TO PHY

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

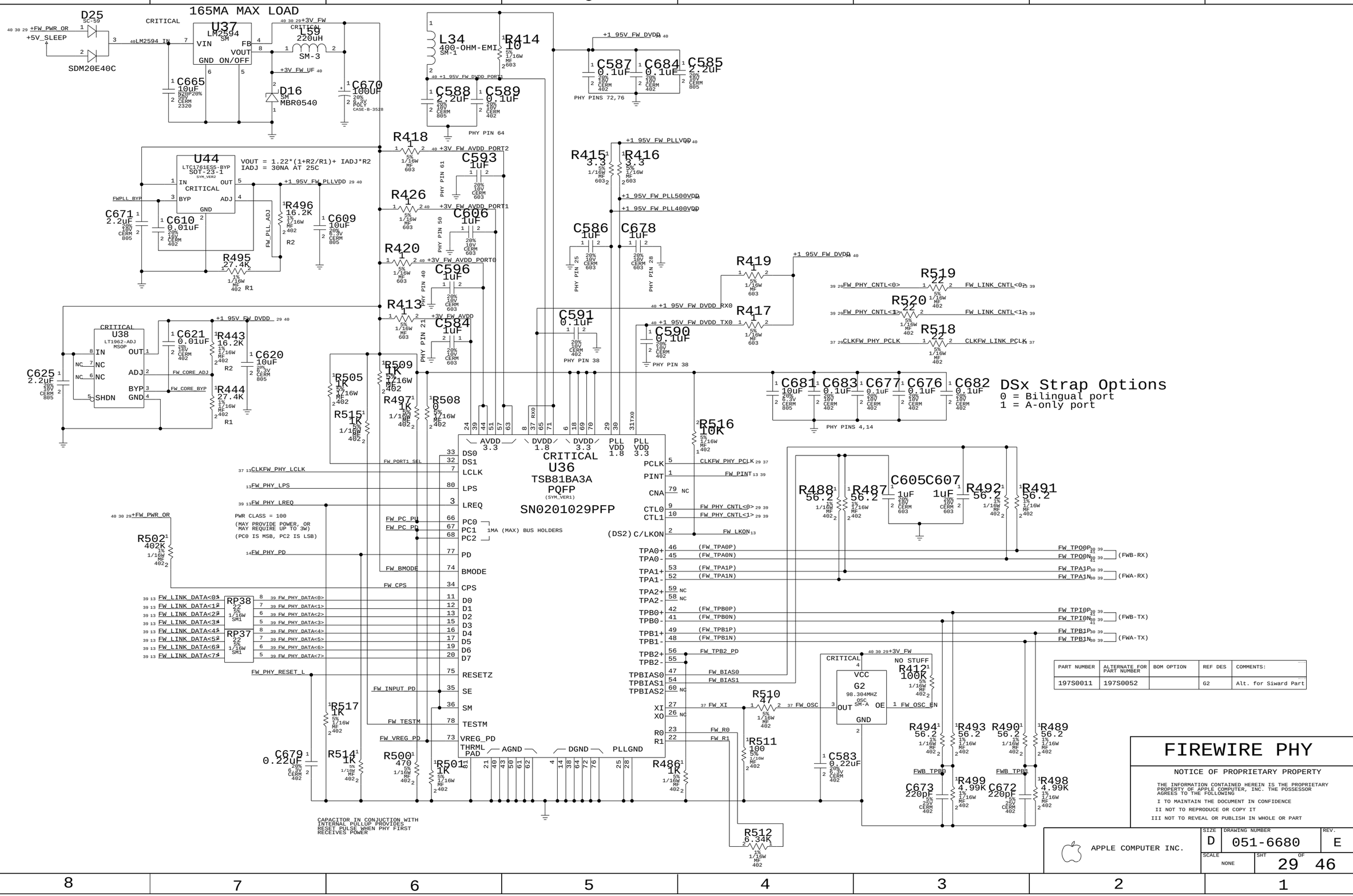
CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 28 OF 46	


165MA MAX LOAD
CRITICAL
D25
SC-59
SDM20E40C
+FW_PWR_OR
+5V_SLEEP
U37
LM2594
SM
VIN
FB
VOUT
GND ON/OFF
LM2594_IN
L59
220uH
SM-3
+3V_FW
+3V_FW_UF
D16
SM
MBR0540
C665
10uF
C670
100uF
6.3V
POLY
CASE-B-3528
L34
400-OHM-EMI
SM-1
R414
10
C588
2.2uF
C589
0.1uF
PHY PIN 64
+1.95V_FW_DVDD
C587
0.1uF
C684
0.1uF
C585
2.2uF
PHY PINS 72,76
R418
+3V_FW_AVDD_PORT2
PHY PIN 61
C593
1uF
R426
+3V_FW_AVDD_PORT1
PHY PIN 50
C606
1uF
R420
+3V_FW_AVDD_PORT0
PHY PIN 40
C596
1uF
R413
+3V_FW_AVDD
PHY PIN 21
C584
1uF
U44
LTC1761ESS-BYP
SOT-23-1
SYM_VER2
VOUT = 1.22*(1+R2/R1)+ IADJ*R2
IADJ = 30NA AT 25C
IN
OUT
BYP
ADJ
GND
FWPLL_BYP
+1.95V_FW_PLLVDD
C671
2.2uF
C610
0.01uF
R496
16.2K
R2
C609
10uF
6.3V
R495
27.4K
R1
FW_PLL_ADJ
R415
3.3
R416
3.3
+1.95V_FW_PLL500VDD
+1.95V_FW_PLL400VDD
C586
1uF
C678
1uF
PHY PIN 25
PHY PIN 28
R419
+1.95V_FW_DVDD
R417
+1.95V_FW_DVDD_RX0
+1.95V_FW_DVDD_TX0
C591
0.1uF
C590
0.1uF
PHY PIN 38
R519
22
FW_PHY_CNTL<0>
FW_LINK_CNTL<0>
R520
22
FW_PHY_CNTL<1>
FW_LINK_CNTL<1>
R518
22
CLKFW_PHY_PCLK
CLKFW_LINK_PCLK
CRITICAL
U38
LT1962-ADJ
MSOP
IN
OUT
NC
NC
ADJ
BYP
SHDN
GND
C621
0.01uF
R443
16.2K
R2
C620
10uF
6.3V
C625
2.2uF
FW_CORE_ADJ
FW_CORE_BYP
R444
27.4K
R1
C681
10uF
C683
0.1uF
C677
0.1uF
C676
0.1uF
C682
0.1uF
PHY PINS 4,14
DSx Strap Options
0 = Bilingual port
1 = A-only port
R505
1K
R509
1K
R497
1K
R508
0
R515
1K
R516
10K
CLKFW_PHY_PCLK
R517
1K
R514
1K
R500
470
R501
1K
R486
1K
R510
47
R511
100
R512
6.34K
C679
0.22uF
C583
0.22uF
CRITICAL
U36
TSB81BA3A
PQFP
(SYM_VER1)
SN0201029PFP
AVDD 3.3
DVDD 1.8
DVDD 3.3
PLL VDD 1.8
PLL VDD 3.3
DS0
DS1
LCLK
LPS
LREQ
PC0
PC1
PC2
PD
BMODE
CPS
D0
D1
D2
D3
D4
D5
D6
D7
RESETZ
SE
SM
TESTM
VREG_PD
THRML PAD
AGND
DGND
PLLGND
PCLK
PINT
CNA
CTL0
CTL1
C/LKON
TPA0+
TPA0-
TPA1+
TPA1-
TPA2+
TPA2-
TPB0+
TPB0-
TPB1+
TPB1-
TPB2+
TPB2-
TPBIAS0
TPBIAS1
TPBIAS2
XI
XO
R0
R1
TX0
RX0
1TX0
FW_PORT1_SEL
CLKFW_PHY_LCLK
FW_PHY_LPS
FW_PHY_LREQ
PWR CLASS = 100
(MAY PROVIDE POWER, OR
MAY REQUIRE UP TO 5W)
(PC0 IS MSB, PC2 IS LSB)
FW_PC_PU
FW_PC_PD
1MA (MAX) BUS HOLDERS
FW_PHY_PD
FW_BMODE
FW_CPS
FW_PHY_RESET_L
FW_INPUT_PD
FW_TESTM
FW_VREG_PD
FW_PINT
FW_LKON
FW_PHY_CNTL<0>
FW_PHY_CNTL<1>
FW_TPA0P
FW_TPA0N
FW_TPA1P
FW_TPA1N
FW_TPB0P
FW_TPB0N
FW_TPB1P
FW_TPB1N
FW_TPB2_PD
FW_BIAS0
FW_BIAS1
FW_R0
FW_R1
FW_XI
FW_OSC
R502
402K
RP38
22
RP37
22
FW_LINK_DATA<0>
FW_LINK_DATA<1>
FW_LINK_DATA<2>
FW_LINK_DATA<3>
FW_LINK_DATA<4>
FW_LINK_DATA<5>
FW_LINK_DATA<6>
FW_LINK_DATA<7>
FW_PHY_DATA<0>
FW_PHY_DATA<1>
FW_PHY_DATA<2>
FW_PHY_DATA<3>
FW_PHY_DATA<4>
FW_PHY_DATA<5>
FW_PHY_DATA<6>
FW_PHY_DATA<7>
CAPACITOR IN CONJUCTION WITH
INTERNAL PULLUP PROVIDES
RESET PULSE WHEN PHY FIRST
RECEIVES POWER
R487
56.2
C605C607
1uF
R492
56.2
R491
56.2
R488
56.2
FW_TPO0P
FW_TPO0N
(FWB-RX)
FW_TPA1P
FW_TPA1N
(FWA-RX)
FW_TPI0P
FW_TPI0N
(FWB-TX)
FW_TPB1P
FW_TPB1N
(FWA-TX)
CRITICAL
VCC
G2
98.304MHZ
OSC
SM-A
OUT
OE
GND
+3V_FW
NO STUFF
R412
100K
FW_OSC_EN
R494
56.2
R493
56.2
R490
56.2
R489
56.2
FWB_TPB0
FWB_TPB1
C673
220pF
C672
220pF
R499
4.99K
R498
4.99K
PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:
197S0011 | 197S0052 | | G2 | Alt. for Siward Part
FIREWIRE PHY
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6680
REV. E
SCALE NONE
SHT 29 OF 46

PORT POWER SWITCH

+PBUS
F3 1.5A-24V MINISMDC
+FW_PBUS
CRITICAL Q34 NDS9407 SOI
+FW_SW
CRITICAL D24 SMB B340B
+FW_PWR_OR
R448 470K 5% 1/16W MF 402
C639 0.01UF 20% 16V CERM 402
FW_GATE_EN
+3V_PMU
R447 100K 5% 1/16W MF 402
DP6 BAS16TW SOT-363
POWER_UP
Q33 2N7002DW SOT-363
PMU_POWER_UP_L
R461 330K 5% 1/16W MF 402
FW_GATE_EN_RC
Q33 2N7002DW SOT-363
FW_POWER_UP
R803 0 5% 1/16W MF 402
DCDC_EN
DCDC_EN_CTRL
DP6 BAS16TW SOT-363
R446 10K 5% 1/16W MF 402
AC_IN
AC_IN_FW_CNTL
DP6 BAS16TW SOT-363
R777 470K 5% 1/16W MF 402

ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

+3V_FW
R451 10K 5% 1/16W MF 402
+3V_FW_ESD_ITM
L39 400-OHM-EMI SM-1
NO STUFF C822 0.1UF 20% 10V CERM 402
C630 0.1UF 20% 10V CERM 402
C637 0.001UF 20% 50V CERM 402
D21 1N5227B SOT23
C638 0.01UF 20% 16V CERM 402
+3V_FW_ESD
D20 BAV99DW SOT-363
D23 BAV99DW SOT-363
D20 BAV99DW SOT-363
D23 BAV99DW SOT-363
C633 0.01UF 20% 16V CERM 402

L76 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
FW_TPO0P
FW_TPO0N
L77 CRITICAL 90-OHM-300mA 2012H SYM_VER-1
FW_TPI0P
FW_TPI0N

PORT 0
1394a/b
(BILINGUAL)
514S0058

CRITICAL J20 1394B F-RT-SM
INT-SHIELD
TPA
TPA(R)
TPA*
VG
SC
VP
TPB
TPB(R)
TPB*
INT-SHIELD
FW_TPA0P
(AREF)
FW_TPA0N
FW_VGND0
NC
FW_VP0
FW_TPB0P
(BREF)
FW_TPB0N
(TPI0R)
C650 0.01UF 20% 16V CERM 402
CHGND1

R465 1M 5% 1/16W MF 402
C649 0.1uF 20% 50V CERM 805
NO STUFF C652 0.01UF 20% 16V CERM 402
R466 0 5% 1/10W MF 805
NO STUFF C651 0.01UF 20% 16V CERM 402
CHGND1

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE IS
PLUGGED TO A BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN THEM
(TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33

L51 FERR-250-OHM SM

R837 0 5% 1/16W MF 603
+FW_PWR_OR_F
PLACE NEAR D24
Q37 NO STUFF SI2319DS SOT23
NO STUFF R829 470K 5% 1/16W MF 402
+FW_PWR_OR_GATE
NO STUFF R830 470K 5% 1/16W MF 402
+FW_PWR_OR_GATE_L
NO STUFF R831 649K 1% 1/16W MF 402
NO STUFF Q73 2N7002 SM
+FW_PWR_CTRL
NO STUFF D35 SM MBR0540
+2_5V_REG_F
NO STUFF C824 1UF 20% 10V CERM 603

+3V_FW
NO STUFF C825 0.1UF 20% 10V CERM 402
NO STUFF U59 LMC7211 SM
+3V_FW_ESD_R
NO STUFF R834 10K 5% 1/16W MF 402
+3V_FW_ESD
+2_5V_REG
2.5V REG
NO STUFF C826 0.01UF 20% 16V CERM 402
NO STUFF R835 102K 1% 1/16W MF 402
NO STUFF R836 332K 1% 1/16W MF 402
PLACE NEAR D23
NO STUFF R833 604K 1% 1/16W MF 402

2.5V REG: 2.50V - 2.15V
200MS - 500MS

F1 1.5AMP-33V SM
+FW_PWR1
L58 FERR-250-OHM SM

+3V_FW_ESD
D22 BAV99DW SOT-363
D18 BAV99DW SOT-363
C640 0.01UF 20% 16V CERM 402
D22 BAV99DW SOT-363
D18 BAV99DW SOT-363
C644 0.01UF 20% 16V CERM 402

PORT 1
1394a ONLY
514-0057

L52 260-OHM-330MA SM1 SYM_VER-2
FW_TPA1P
FW_TPA1N
L48 260-OHM-330MA SM1 SYM_VER-2
FW_TPB1P
FW_TPB1N
CRITICAL J24 1394A F-RT-TH
FW_TPO1P
FW_TPO1N
FW_TPI1P
FW_TPI1N
FW_VP1
FW_VGND1
TPO
TPO#
TPI
TPI#
VP
VGND

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

R471 0 5% 1/10W MF 805
C662C666 0.01uF 0.01UF 20% 16V CERM 402
CHGND1

R816 0 5% 1/16W MF 402 EMI
CHGND1

FIREWIRE PORTS

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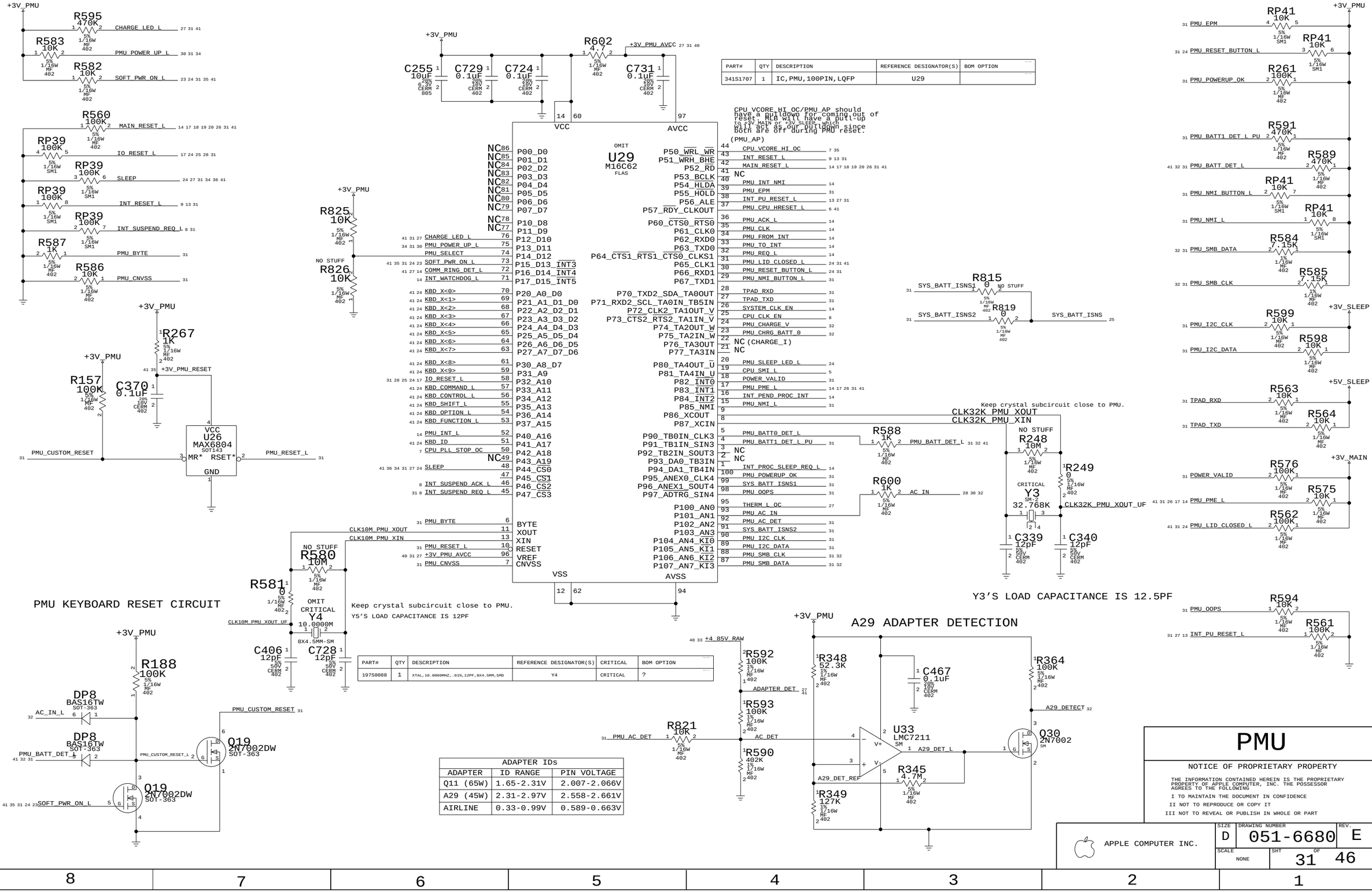
SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 30 OF 46	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1707	1	IC,PMU,100PIN,LQFP	U29	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0088	1	XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD	Y4	CRITICAL	?

PMU

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SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 31 OF 46	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 50V X7R 603-1

DC INRUSH LIMITER

Q68 SI4435DY SOI

R21 330K 5% 1/16W MF 402

C11 0.1uF 20% 50V CERM 805

AC ENABLE GATE

R51 20K 1% 1/16W MF 402

+3V_PMU

R40 97.6K 1% 1/16W MF 402

R16 100K 1% 1/16W MF 402

C801 0.01uF 20% 16V CERM 402

R15 10K 5% 1/16W MF 402

U1 LMC7211 SM

1V20_REF

AC_DIV

AC_IN

AC_IN_L

R41 1M 5% 1/16W MF 402

R42 10K 1% 1/16W MF 402

R30 57.6K 1% 1/16W MF 402

Q1 2N7002DW SOT-363

R22 470K 5% 1/16W MF 402

GREATER THAN 13.1V DETECT

R29 470K 5% 1/16W MF 402

AC_ENABLE_L

Q1 2N7002DW SOT-363

BACKFEED PROTECTION

+ADAPTER_SW

Q69 SI4435DY SOI

+ADAPTER_SENSE

R732 47K 5% 1/16W MF 402

BKFD_PROT_GATE

C803 0.01UF 20% 16V CERM 603

R734 68K 1% 1/16W MF 402

BKFD_PROT_EN_L

Q9 2N7002DW SOT-363

AC_IN

C36 0.01uF 20% 50V CERM 603

+24V_PBUS

U3 MAX4172 TSSOP

RS+ RS- PG OUT GND V+

NC NC1 NC2

MAX4172_OUT

R77 2.21K 0.1% 1/16W MF 603

Place close to RS-

C233 0.1uF 10% 50V X7R 603-1

PLACE U24 NEXT TO R382

R61 0.025 1% 1W MF 2512

1772_CSSP

1772_CSSN

R82 4.7 5% 1/16W MF 402

R87 4.7 5% 1/16W MF 402

R57 100K 1% 1/16W MF 402

D4 1N914 SOT23

C67 1uF 20% 50V CERM 1210

R49 12.7K 1% 1/16W MF 402

C71 0.47uF 10% 16V CERM 1206

C95 0.47UF 10% 16V CERM 1206

CSSP CSSN

U6 MAX1772 QSOP

DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CLS GND CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT

1772_DCIN 1772_ACIN 1772_ACOK_L (+3V_PMU) 1772_VCTL 1772_ICTL 1772_ICHG 1772_IINP 1772_CCV 1772_CCI 1772_CCS 1772_CELLS 1772_DLOV 1772_BST 1772_DHI 1772_LX 1772_DLO (GND) 1772_CSIP 1772_CSIN

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402

C798 0.1uF 20% 16V CERM 402

+3V_PMU

C794 0.1uF 20% 16V CERM 402

R745 47.2K 0.1% 1/16W TF 603

IAC_RC_COMP

IAC_FB

U55 LMC7111 SOT23-5

PLACE R383 CLOSE TO LTC1625

ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

R727 10K 1% 1/16W MF 402

DP1 BAS16TW SOT-363

R119 150 1% 1/16W MF 402

1625_COMP

ADAPTER_I_REG

CURRENT_THRESHOLD

R736 42.2K 0.1% 1/16W TF 603

R738 82.5K 0.1% 1/16W TF 603

R742 51.1K 0.1% 1/16W TF 603

A29_CURRENT_ADJ

OVER_18V_ADJ

R744 100K 5% 1/16W MF 402

Q2 2N7002DW SOT-363

A29_DETECT

AC_GTR_18V

Q74 2N7002DW SOT-363

1772_ACOK_L

C809 1uF 20% 16V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+BATT

+24V_PBUS

F5 5AMP-125V SM-2

+PBUS

F4 5AMP-125V SM-2

+BATT_24V_FUSE

+BATT_14V_FUSE

Q6 SI4435DY SOI

Q7 SUD45P03 TO-252

R716 47K 5% 1/16W MF 402

R710 47K 5% 1/16W MF 402

BATT_24V_GATE

BATT_14V_GATE

R717 10K 5% 1/16W MF 402

R711 10K 5% 1/16W MF 402

DP1 BAS16TW SOT-363

BATT_24PBUS_EN

BATT_14PBUS_EN

AC_IN_L

DP1 BAS16TW SOT-363

R102 158K 1% 1/16W MF 402

Q9 2N7002DW SOT-363

AC_IN_L_RC

C118 10uF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF

WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON

RC TIME IS 480K*10uF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU

R73 27.4K 1% 1/16W MF 402

R62 10K 1% 1/16W MF 402

R58 10K 1% 1/16W MF 402

R74 4.12K 1% 1/16W MF 402

R733 20K 1% 1/16W MF 402

BATTV_HIGH

R59 100K 5% 1/16W MF 402

Q4 2N7002DW SOT-363

R75 5.23K 1% 1/16W MF 402

BATTV_LOW

PMU_CHARGE

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R731 1K 1% 1/16W MF 402

BATT_LOW_L

Q71 2N7002DW SOT-363

Q71 2N7002DW SOT-363

R56 1K 1% 1/16W MF 402

R55 1K 1% 1/16W MF 402

C43 0.01uF 20% 16V CERM 402

C42 0.01uF 20% 16V CERM 402

1772_CCV_RC

1772_REF

R54 10K 1% 1/16W MF 402

R53 4.12K 1% 1/16W MF 402

1772_CLS

R83 1K 1% 1/16W MF 402

C24 0.1uF 20% 16V CERM 402

C23 1uF 20% 10V CERM 603

1772_GND

C41 1uF 20% 10V CERM 603

C98 0.1uF 20% 25V CERM 603

C99 0.1uF 20% 25V CERM 603

R94 100K 5% 1/16W MF 402

XW1 SM

C853 1000pF 20% 25V X7R 402

NO STUFF

Q64 IRF7811W SO-8

D36 SM MBRS140T3

CRITICAL L70 10uH SM1

+BATT_RSNS

R715 0.05 1% 1W MF 2512

+BATT_24V_FUSE

C780 4.7uF 20% 25V CERM 1206

C795 4.7uF 20% 25V CERM 1206

C790 4.7uF 20% 25V CERM 1206

C779 33uF 20% 25V SPEC SM1

C777 4.7uF 20% 25V CERM 1206

C792 4.7uF 20% 25V CERM 1206

C785 4.7uF 20% 25V CERM 1206

R720 1 5% 1/16W MF 603

R713 1 5% 1/16W MF 603

SWITCHER VOLTAGE CONTROL

+3V_PMU

R741 100K 5% 1/16W MF 402

Q72 2N7002DW SOT-363

CHARGE_DISABLE

Q72 2N7002DW SOT-363

PMU_CHRG_BATT_0

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

+3V_PMU

C799 0.1uF 20% 16V CERM 402

U57 LMC7211 SM

BATT_LOW

R729 100K 1% 1/16W MF 402

R740 499K 1% 1/16W MF 402

BATT_DIV

1V65_REF

R730 100K 1% 1/16W MF 402

R735 100K 1% 1/16W MF 402

C807 0.047uF 10% 16V CERM 402

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

+BATT_VSNS

R47 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

Q2 2N7002DW SOT-363

A29_DETECT

+BATT_POS

(BATT_IN_PD)

BATT_CLK

BATT_DATA

PMU_BATT_DET_L

BATT_NEG

L5 FERR-EMI-100-OHM SM

L2 FERR-50-OHM SM

+BATT_ISNS

L6 FERR-50-OHM SM

L4 FERR-EMI-100-OHM SM

PMU_SMB_CLK

L3 FERR-EMI-100-OHM SM

PMU_SMB_DATA

D6 1N914 SOT23

1772_BST_ESR

R725 33 5% 1/8W FF 1206

R52 100K 5% 1/16W MF 402

C97 0.1uF 20% 25V CERM 603

R96 4.7 5% 1/16W MF 603

+24V_PBUS

C96 0.1uF 20% 50V CERM 805

CRITICAL Q70 IRF7805 SM

C112 2.2UF 10% 50V X7R 1206

C117 2.2UF 10% 50V X7R 1206

C113 2.2UF 10% 50V X7R 1206

C115 2.2UF 10% 50V X7R 1206

C116 2.2UF 10% 50V X7R 1206

BATTERY CHARGER

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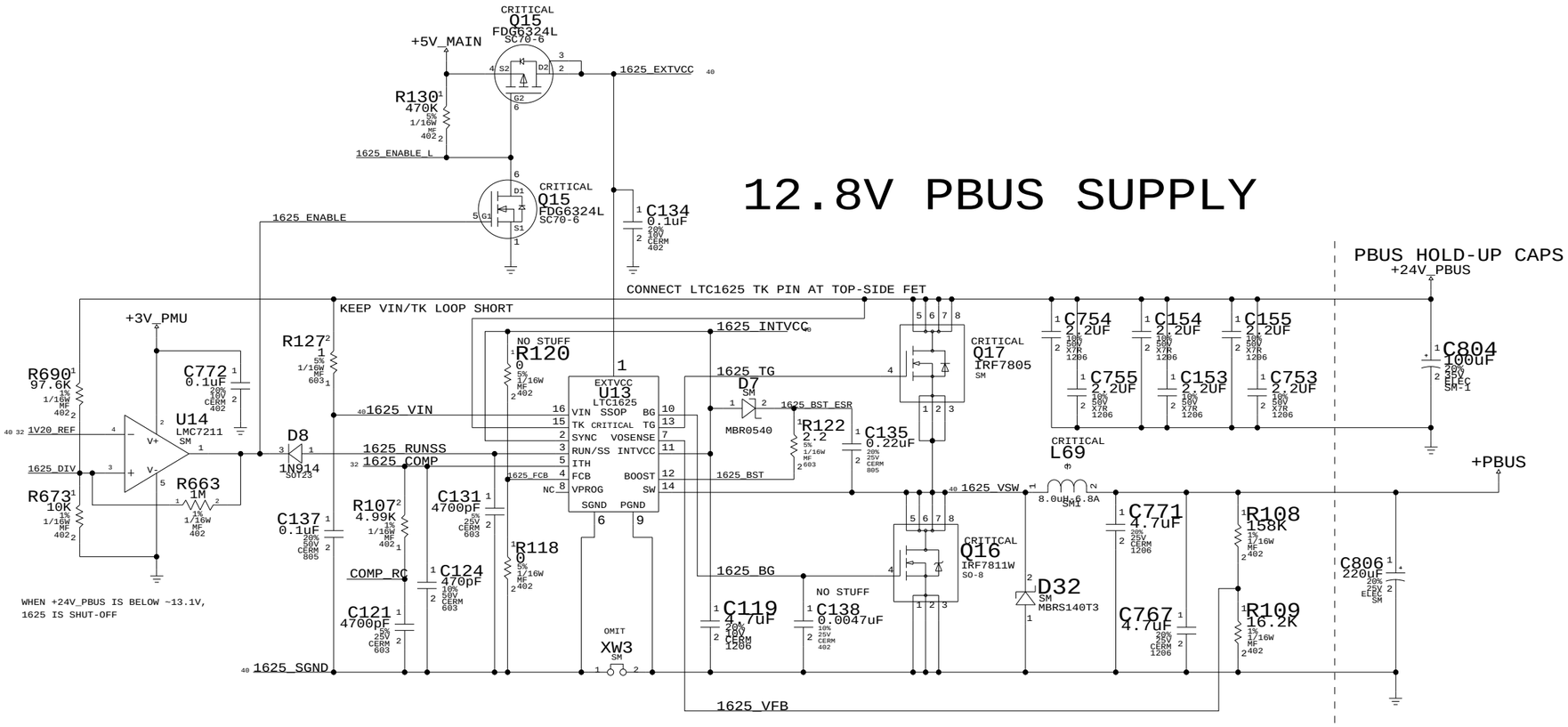
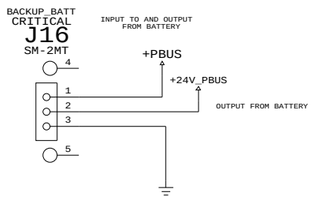
SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE	SHT	OF
NONE	32	46

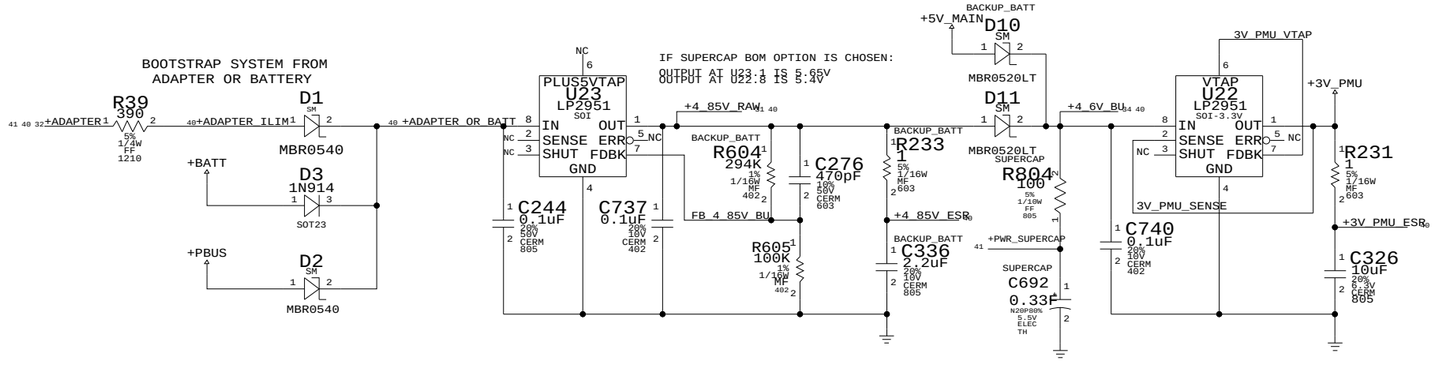
12.8V PBUS SUPPLY



BACKUP BATTERY



PMU SUPPLY



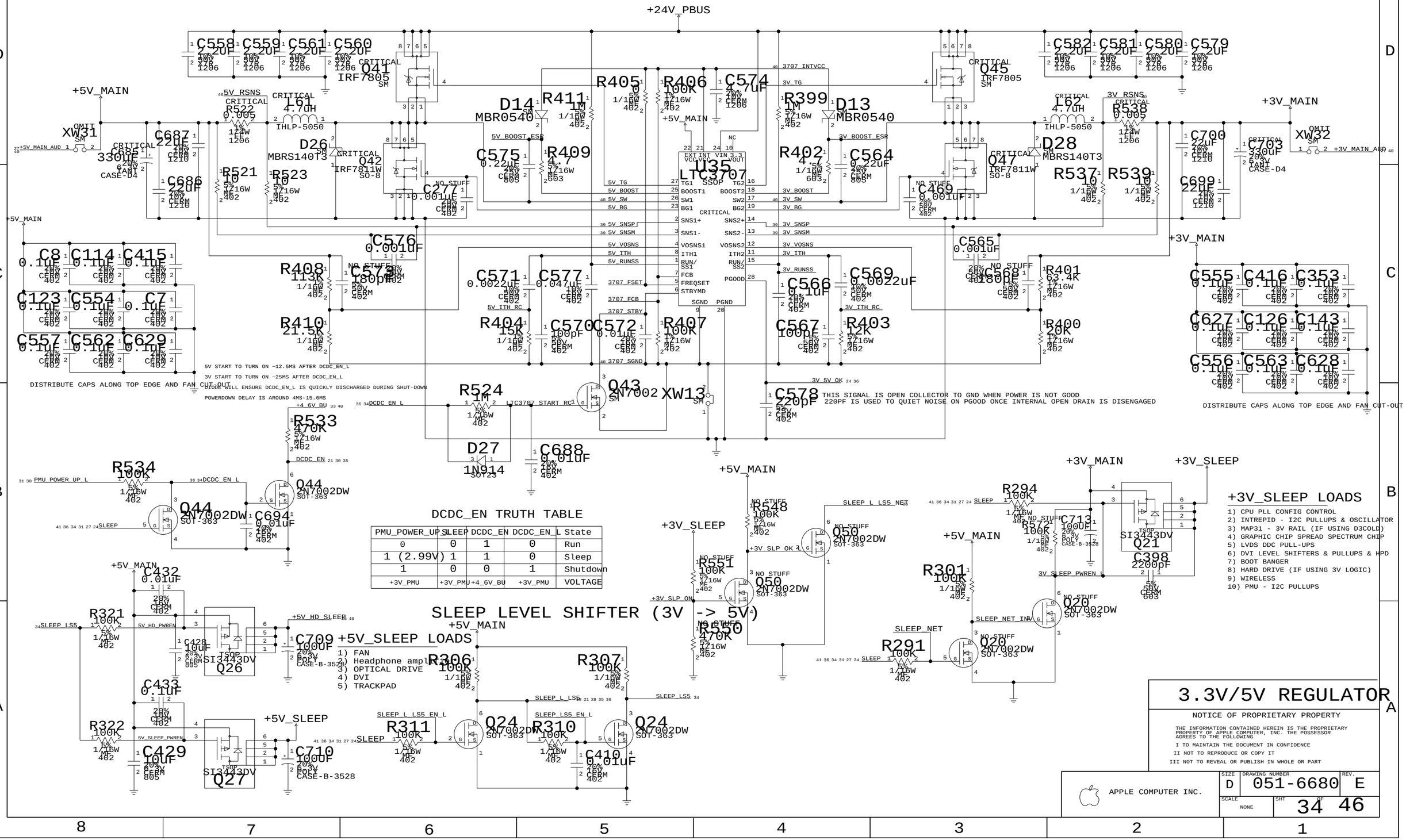
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W,357K OHM,1%,0402,SMD	R604	?	SUPERCAP

12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 33 OF 46	

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 34 OF 46	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.67GHZ (1.28VCORE) 1.300V->0.975V

1.50GHZ 1.200V->0.975V

1.67GHZ (1.26VCORE) 1.300V->0.975V

(VALUE WITHOUT OFFSET)

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of Vcore

(R93 CPU_BTR BOM OPTION SEE BOM TABLE)

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

	A/B_ =	
D<4..0>	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, V = VA. B

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

Connect MAX1717 GND pin 13 to GND at bottom-side FET

(CPU Vcore value with offset)

1.67GHZ 1.320V->0.990V (CPU SPEC: 1.280V -> 0.980V)

1.50GHZ 1.240V->0.990V (CPU SPEC: 1.200V -> 0.980V)

1.67GHZ(1.26VCORE) 1.300V->0.990V (CPU SPEC: 1.260V -> 0.980V)

ROUTE AS DIFFERENTIAL PAIR

Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Keep trace fat and short!!

Fmax Test Connections

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L71	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2493	1	RES,MF,1/16W,2.49K OHM,1%,0402,SMD	R93	?	CPU_BTR_VCORE12
114S4023	1	RES,MF,1/16W,4.02K OHM,1%,0402,SMD	R97	?	CPU_BTR_VCORE12
116S1000	1	RES,MF,1/16W,0 OHM,5%,0402,SMD	R93	?	CPU_BST_VCORE126
114S1503	1	RES,MF,1/16W,1.5K OHM,1%,0402,SMD	R97	?	CPU_BST_VCORE126
114S2433	1	RES,MF,1/16W,2.43K OHM,1%,0402,SMD	R93	?	CPU_BST_VCORE13
114S4023	1	RES,MF,1/16W,4.02K OHM,1%,0402,SMD	R97	?	CPU_BST_VCORE13
114S2003	1	RES,MF,1/16W,2K OHM,1%,0402,SMD	R93	?	CPU_BTR_VCORE122
114S6043	1	RES,MF,1/16W,6.04K OHM,1%,0402,SMD	R97	?	CPU_BTR_VCORE122

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

VCORE SUPPLY

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SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE: NONE | SHT 35 OF 46

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M11 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. E

SCALE NONE | SHT 36 OF 46

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M11 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. E

SCALE NONE | SHT 37 OF 46

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS0	CPU_AACK_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200	MIL7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800	MIL7		(250)			
	CPU_OACK_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_OREQ_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000	MIL7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700	MIL7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100	MIL7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

TMDS/DVO SIGNAL CONSTRAINTS

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL		100 OHM SPACING FOR TMDS
SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL		100 OHM SPACING FOR TMDS
SI_TMDS_DN<0>	SI_TMDS_D0			100 OHM SPACING FOR TMDS
SI_TMDS_DP<0>	SI_TMDS_D0			100 OHM SPACING FOR TMDS
SI_TMDS_DN<1>	SI_TMDS_D1			100 OHM SPACING FOR TMDS
SI_TMDS_DP<1>	SI_TMDS_D1			100 OHM SPACING FOR TMDS
SI_TMDS_DN<2>	SI_TMDS_D2			100 OHM SPACING FOR TMDS
SI_TMDS_DP<2>	SI_TMDS_D2			100 OHM SPACING FOR TMDS
SI_TMDS_DN<3>	SI_TMDS_D3			100 OHM SPACING FOR TMDS
SI_TMDS_DP<3>	SI_TMDS_D3			100 OHM SPACING FOR TMDS
SI_TMDS_DN<4>	SI_TMDS_D4			100 OHM SPACING FOR TMDS
SI_TMDS_DP<4>	SI_TMDS_D4			100 OHM SPACING FOR TMDS
SI_TMDS_DN<5>	SI_TMDS_D5			100 OHM SPACING FOR TMDS
SI_TMDS_DP<5>	SI_TMDS_D5			100 OHM SPACING FOR TMDS

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

ATI_DVOD<23..0>	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610		
ATI_DVOD_DE	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_HSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_VSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		
ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:500 MIL	6	610.0000	165.0 MHz:::	
GPU_DVO_CLKP_R1	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	
GPU_DVO_CLKP_R2	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	

TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<3>	TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<3>	TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<4>	TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<4>	TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<5>	TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<5>	TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DN<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS
TMDS_CONN_DP<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS

GPU_R	GPU_R	500.0000	100 OHM SPACING
GPU_G	GPU_G	500.0000	100 OHM SPACING
GPU_B	GPU_B	500.0000	100 OHM SPACING

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E

SCALE: NONE

SHT 38 OF 46

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ
	AGP_SB_STB	L:S:1050 MIL:1450 MIL	4		(350)	8 MIL SPACING		66.00 MHZ
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL	4		(350)	8 MIL SPACING		66.00 MHZ
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_STOP_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_PAR	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_REQ_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_GNT_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
	AGP_RBF_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL			(200)			100.0 MHZ
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL	4		(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHZ
	HD_DIOW_L	L:S:3000 MIL:5200 MIL	4		(200)			100.0 MHZ
	HD_DIOR_L	L:S:6100 MIL:6150 MIL	4	10 MIL SPACING	(200)			100.0 MHZ
	HD_DMACK_L	L:S:4500 MIL:6000 MIL	4		(200)			100.0 MHZ
	HD_CS0_L	L:S:3000 MIL:6000 MIL	4		(200)			100.0 MHZ
	HD_CS1_L	L:S:3000 MIL:6000 MIL	4		(200)			100.0 MHZ
	HD_DMARQ	L:S:4500 MIL:6000 MIL	4		(200)			100.0 MHZ
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL	4	10 MIL SPACING	(200)			100.0 MHZ
	HD_INTRQ	L:S:3000 MIL:5000 MIL	4					100.0 MHZ
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ
	EIDE_INT	L:S::500 MIL						33.00 MHZ
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_LINK_TXD<7..0>	L:S::600						
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL	4					
	ENET_LINK_TX_ER	L:S::400 MIL						
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL	4					
	ENET_LINK_TX_EN	L:S::400 MIL						
	ENET_MDIO	L:S:8000 MIL:9000 MIL						
	ENET_MDC	L:S:8000 MIL:9000 MIL						
	ENET_COL	L:S:8000 MIL:9000 MIL						
	ENET_CRS	L:S:8000 MIL:9000 MIL						
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		
	FW_LINK_CNTL<1..0>	L:S:9000:10000						
	FW_PHY_CNTL<1..0>	L:S::300						
	FW_LINK_LREQ	L:S::300 MIL						
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						
	FW_PINT	L:S:8500 MIL:9500 MIL						

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_TPAD_N	USB_TPAD_N	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_TPAD_P	USB_TPAD_P	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	REMOVE CONSTRAIN TO AVOID DRC OCCUR					
	1772_CSSN					
	1772_CSSP					
	1772_CSIN					
	1772_CSIP					
	3V_SNSM					
	3V_SNSP					
	5V_SNSM					
	5V_SNSP					
	THERM1_M_DM					
	THERM1_M_DP					
	THERM2_M_DM					
	THERM2_M_DP					
	THERM1_A_DM					
	THERM1_A_DP					
	THERM2_A_DM					
	THERM2_A_DP					

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	E
SCALE: NONE	SHT 39 OF 46	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+BATT	VOLTAGE=12.8V	MIN_LINE_WIDTH=10MIL	MIN_NECK_WIDTH=25MIL	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 41
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	41
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	41
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 33 41
	I496 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 40
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 40
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 41
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 41
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		27 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		41
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		24 41
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 41
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 41
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23 41
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	23 41
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		23
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		23
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		23 41
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		23 41
AUDIO	I435 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 34
	I435 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 34
	I435 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		27
FAN	I438 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 41
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41

I/O AREA
INVERTER
TRACKPAD
LVDS

CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN
CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 35 41
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 35
	I386 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	I386 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	I387 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
CARDBUS	I386 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 21 41
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 21 22
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	22
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 22
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21 22
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 21 22
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	22
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21 22
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	22
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	22
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	I346 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	I347 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		21
	I348 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		36
	I349 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
	I350 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
	I351 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		21
	I352 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
	I353 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		36
	I354 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		36
	I355 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		36
	I356 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	22
	I361 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	I318 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	I317 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	I432 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	29
	I414 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	I345 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29 30
	I416 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30 41
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30 41
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	I415 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	I386 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	32 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	34
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		36
	2_5V_ILIM		MIN_LINE_WIDTH=8		36
	MAX1715_TON		MIN_LINE_WIDTH=8		36
	MAX1715_SKIP		MIN_LINE_WIDTH=8		36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	35
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_ILIM		MIN_LINE_WIDTH=8		35
	VCORE_REF		MIN_LINE_WIDTH=8		35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		35
	VCORE_CC		MIN_LINE_WIDTH=8		35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		35 41
	VCORE_TIME		MIN_LINE_WIDTH=8		35
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		35
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		35
	I437 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	21
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	21
	1778_ION		MIN_LINE_WIDTH=8		21
	1778_ITH		MIN_LINE_WIDTH=8		21
	1778_ITH_RC		MIN_LINE_WIDTH=8		21
	1778_VFB		MIN_LINE_WIDTH=8		21 41
	1778_FCB		MIN_LINE_WIDTH=8		21
	1778_VRNG		MIN_LINE_WIDTH=8		21
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_VFB		MIN_LINE_WIDTH=8		36
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		36
	LTC3411_ITH		MIN_LINE_WIDTH=8		36
	LTC3411_SYNC		MIN_LINE_WIDTH=8		36
	LTC3411_SHDN		MIN_LINE_WIDTH=8		36
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
CY28512D LMU CONN	I436 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	I436 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
OPT DRIVER	I436 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. E

SCALE NONE | SHT 40 OF 46

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	I2	JTAG_ASIC_TMS	TRUE			13 28
	I3	JTAG_ASIC_TDI	TRUE			13
	I1	JTAG_ASIC_TDO_TP	TRUE			28
	I4	JTAG_ASIC_TCK	TRUE			13 28
	I6	JTAG_ASIC_TRST_L	TRUE			13 28
	I5	CPU_CHKSTP_OUT_L	TRUE			5
	I7	CPU_SRESET_L	TRUE			5
	I9	CPU_HRESET_L	TRUE			5 6 7
	I8	JTAG_CPU_TMS	TRUE			5 6
	I10	JTAG_CPU_TDI	TRUE			5 6
	I12	JTAG_CPU_TDO_TP	TRUE			5
	I11	JTAG_CPU_TCK	TRUE			5 6
	I13	JTAG_CPU_TRST_L	TRUE			5 6
	I18	INT_JTAG_TEI	TRUE			13
	I20	INT_TST_MONIN_PD	TRUE			13
	I19	INT_TST_MONOUT_TP	TRUE			13
	I21	INT_TST_PLLEN_PD	TRUE			13
INT I2C	I15	INT_I2C_CLK0	TRUE			6 11 13 24
	I14	INT_I2C_DATA0	TRUE			6 11 13 24
	I16	INT_I2C_CLK1	TRUE			13 14 24 25 27
	I17	INT_I2C_DATA1	TRUE			13 14 24 25 27
PWR/GND	I21	+PBUS	TRUE			40
	I216	+24V_PBUS	TRUE			40
	I25	GPU_VCORE	TRUE			19 21 40
	I24	1778_VFB	TRUE			21 40
	I27	CPU_VCORE_SLEEP	TRUE			5 6 35 40
	I26	VCORE_FB	TRUE			35 40
	I23	+1_8V_MAIN	TRUE			40
	I218	+2_5V_MAIN	TRUE			40
	I219	+5V_MAIN	TRUE	2		40 41
	I220	+5V_SLEEP	TRUE	2		40 41
	I222	+3V_MAIN	TRUE	4		24 40
			TRUE		1000	IN
	I222	+3V_PMU	TRUE			40
CARDBUS	I36	CBUS_DET_1_L	TRUE		2000	18
	I35	CBUS_DET_2_L	TRUE		2000	18
DVI	I40	TMDS_CONN_CLKN	TRUE		1000	23 38
	I39	TMDS_CONN_CLKP	TRUE		1000	23 38
	I42	VGA_R	TRUE		1000	23
	I41	VGA_G	TRUE		1000	23
	I44	VGA_B	TRUE		1000	23
	I43	VGA_HSYNC	TRUE		1000	23
	I46	VGA_VSYNC	TRUE		1000	23
	I45	DVI_DDC_CLK_UF	TRUE		1000	23
	I47	DVI_DDC_DATA_UF	TRUE		1000	23
	I48	DVI_HPD_UF	TRUE		1000	23
	I49	+5V_DDC_SLEEP	TRUE		2000	23 40
			TRUE	2	2000	IN
			TRUE	6	1000	IN
CHGND1						
LVDS	I52	LVDS_L0N			1000	21 23 39
	I51	LVDS_L0P			1000	21 23 39
	I53	LVDS_L1N			1000	21 23 39
	I55	LVDS_L1P			1000	21 23 39
	I54	LVDS_L2N			1000	21 23 39
	I57	LVDS_L2P			1000	21 23 39
	I56	CLKLVDS_LN	TRUE		1000	21 23 39
	I58	CLKLVDS_LP	TRUE		1000	21 23 39
	I59	LVDS_DDC_CLK	TRUE		1000	21 23
	I60	LVDS_DDC_DATA	TRUE		1000	21 23
	I62	+3V_LCD	TRUE	2	2000	23 40
	I223	+3V_SLEEP	TRUE		2000	40 41
			TRUE	2	2000	IN
			TRUE	6	1000	IN
CHGND4						
INVERTER	I67	+14V_INV	TRUE		2000	23 40
	I66	+5V_INV_SW	TRUE		2000	23 40
	I68	BRIGHT_PWM	TRUE		2000	23
	I249	INV_GND	TRUE		2000	23
			TRUE		1000	IN
S-VIDEO	I70	TV_C	TRUE		2000	23
	I72	TV_Y	TRUE		2000	23
	I71	TV_COMP	TRUE		2000	23
	I73	TV_GND1	TRUE		2000	23 40
	I74	TV_GND2	TRUE		2000	23 40
LIO	I76	INT_I2S0_SND_TO_DAC	TRUE		1000	14 27
	I75	INT_I2S0_SND_LRCLK	TRUE		1000	14 27
	I78	INT_I2S0_SND_MCLK	TRUE		1000	14 27 37
	I83	INT_I2S0_SND_SCLK	TRUE		1000	14 27
	I82	INT_I2S0_SND_FROM_ADC	TRUE		1000	14 27
	I77	SND_HP_MUTE_L	TRUE		1000	14 27
	I79	SND_AMP_MUTE	TRUE		1000	27
	I84	SND_HW_RESET_L	TRUE		1000	14 27
	I85	SND_HP_SENSE_L	TRUE		1000	14 27
	I86	SND_LIN_SENSE_L	TRUE		1000	14 27
	I81	INT_I2C_CLK2	TRUE		1000	14 27
	I80	INT_I2C_DATA2	TRUE		1000	14 27
	I87	ADAPTER_DET	TRUE		1000	27 31
	I88	CHARGE_LED_L	TRUE		1000	27 31
	I89	NEC_LUSB_OCI_UF	TRUE		1000	17 27
	I90	NEC_LUSB_PPON	TRUE		1000	17 27
	I222	+5V_MAIN	TRUE	2	2000	40 41
	I223	+5V_SLEEP	TRUE	2	3000	40 41
	I221	+3V_SLEEP	TRUE		2000	40 41

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	I194	NEC_USB_DAM	TRUE			17 27 39
	I195	NEC_USB_DAP	TRUE			17 27 39
	I196	NEC_USB_DBM	TRUE			17 27 39
	I197	NEC_USB_DBP	TRUE			17 27 39
	I198	BT_USB_DM	TRUE			14 27 39
	I199	BT_USB_DP	TRUE			14 27 39
	I167	USB_TPAD_N	TRUE			14 24 39
	I168	USB_TPAD_P	TRUE			14 24 39
RT. USB	I192	NEC_RUSB_PPON	TRUE			17 27
	I191	NEC_RUSB_OCI_UF	TRUE			17 27
WIRELESS	I165	PCI_AD<0..31>	TRUE		1000	9 12 17 18 26 39
	I166	PCI_FRAME_L	TRUE		1000	12 17 18 26 39
	I169	PCI_TRDY_L	TRUE		1000	12 17 18 26 39
	I170	PCI_IRDY_L	TRUE		1000	12 17 18 26 39
	I171	PCI_DEVSEL_L	TRUE		1000	12 17 18 26 39
	I172	PCI_STOP_L	TRUE		1000	12 17 18 26 39
	I173	PCI_PAR	TRUE		1000	12 17 18 26 39
	I174	AIRPORT_PCI_REQ_L	TRUE		1000	12 26
	I175	AIRPORT_PCI_GNT_L	TRUE		1000	12 26
	I176	AIRPORT_PCI_INT_L	TRUE		1000	14 26
	I177	MAIN_RESET_L	TRUE		1000	14 17 18 19 20 26 31
	I178	CLK33M_AIRPORT	TRUE		1000	12 26 37
	I179	PMU_PME_L	TRUE		1000	14 17 26 31
	I180	ROM_ONBOARD_CS_L	TRUE		1000	9
	I181	ROM_OE_L	TRUE		1000	9 12
	I182	ROM_CS_L	TRUE		1000	9 12
	I183	ROM_RW_L	TRUE		1000	9 12
	I220	RF_DISABLE_L	TRUE		1000	26
	I230	AIRPORT_CLKRUN_L	TRUE		1000	26
	I124	+3V_AIRPORT	TRUE	4	2000	40
			TRUE	6	1000	IN
OPTICAL	I126	EIDE_OPTICAL_DATA<0..15>	TRUE		2000	26 39
	I127	EIDE_OPTICAL_DMA_RQ	TRUE		2000	26 39
	I128	EIDE_OPTICAL_READ_L	TRUE		2000	26 39
	I129	EIDE_OPTICAL_DMAACK_L	TRUE		2000	26 39
	I130	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	26 39
	I131	EIDE_OPTICAL_CS0_L	TRUE		2000	26 39
	I132	EIDE_OPTICAL_CS1_L	TRUE		2000	26 39
	I133	EIDE_OPTICAL_RST_L	TRUE		2000	26 39
	I134	EIDE_OPTICAL_WR_L	TRUE		2000	26 39
	I135	EIDE_OPTICAL_IOCHRDY	TRUE		2000	26 39
	I136	EIDE_OPTICAL_INT	TRUE		2000	26 39
TRACKPAD	I137	+5V_TPAD_SLEEP	TRUE		3000	40
	I138	TPAD_F_TXD	TRUE		3000	
	I139	TPAD_F_RXD	TRUE		3000	
	I140	SOFT_PWR_ON_L	TRUE		3000	23 24 31 35
MODEM/ SERIAL	I141	COMM_RESET_L	TRUE		4000	14 27
	I142	COMM_SHUTDOWN	TRUE		4000	
	I143	COMM_RING_DET_L	TRUE		4000	14 27 31
	I144	COMM_TXD_L	TRUE		4000	14 27
	I145	COMM_TRXC	TRUE		4000	14 27
	I146	COMM_GPIO_L	TRUE		4000	14 27
	I147	COMM_DTR_L	TRUE		4000	14 27
	I148	COMM_RTS_L	TRUE		4000	14 27
	I149	COMM_RXD	TRUE		4000	14 27
KEYBOARD	I149	KBD_ID	TRUE		3000	24 31
	I155	KBD_INTL	TRUE		3000	
	I156	KBD_JIS	TRUE		3000	
	I152	KBD_CAPSLOCK_LED	TRUE		3000	
	I153	KBD_NUMLOCK_LED	TRUE		3000	
	I154	KBD_FUNCTION_L			3000	24 31
	I150	KBD_COMMAND_L			3000	24 31
	I157	KBD_OPTION_L			3000	24 31
	I158	KBD_CONTROL_L			3000	24 31
	I159	KBD_SHIFT_L			3000	24 31
	I160	KBD_X<0..9>			3000	24 31
	I161	KBD_Y<0..7>			3000	
BATTERY	I163	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	I162	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	I164	BATT_CLK	TRUE		1000	32
	I165	BATT_DATA	TRUE		1000	32
	I161	PMU_BATT_DET_L	TRUE		1000	31 32
FANS	I167	+FAN_PWR	TRUE		3000	27 40
	I168	FAN1_TACH	TRUE		3000	27
	I169	FAN2_TACH	TRUE		3000	27
	I170	FAN1_GND	TRUE		3000	40
	I171	FAN2_GND	TRUE		3000	40
ETHERNET	I172	MDI_P<0..3>	TRUE		1000	28 39
	I173	MDI_M<0..3>	TRUE		1000	28 39
FIREWIRE	I197	FW_TPO0P	TRUE		1000	29 30 39
	I176	FW_TPO0N	TRUE		1000	29 30 39
	I175	FW_TPO0R	TRUE		1000	30
	I177	FW_TPI0P	TRUE		1000	29 30 39
	I178	FW_TPI0N	TRUE		1000	29 30 39
	I179	+FW_VP0	TRUE		1000	30 40
	I180	FW_VGND	TRUE		1000	41

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	I181	FW_TPO1P	TRUE		1000	30 39
	I182	FW_TPO1N	TRUE		1000	30 39
	I183	FW_TPI1P	TRUE		1000	30 39
	I184	FW_TPI1N	TRUE		1000	30 39
	I185	+FW_VP1	TRUE		1000	30 40
	I186	FW_VGND	TRUE		1000	41
DC PWR IN	I188	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	32 33 40
LMU/ALS	I250	ST7_SLEEP_LED_H	TRUE			24
	I250	PMU_SLEEP_LED	TRUE			24
	I250	PMU_LID_CLOSED_L	TRUE			24 31
	I250	LMU_DETECT	TRUE			24
			TRUE	6	1000	IN
MISC.				(100 MIL PROBE PREFERRED)		
	I190	SLEEP_LED	TRUE			24
	I191	PMU_KB_RESET_L	TRUE			
	I189	SLEEP	TRUE			24 27 31 34 36
	I193	PMU_CPU_HRESET_L	TRUE			6 31
	I192	BB_RESET_L	TRUE			6
	I224	+3V_PMU_RESET	TRUE			31 35
	I250	MMM_ACC_X_AXIS	TRUE			25
	I250	MMM_ACC_Y_AXIS	TRUE			25
	I250	MMM_ACC_Z_AXIS	TRUE			25
	I250	MMM_ACC_SELFTEST	TRUE			25
	I250	+BATT_ISNS_P	TRUE			25
	I250	+PPBATT_ISNS_N	TRUE			25
	I250	+PWR_SUPERCAP	TRUE			33
		REMOVE CONSTRAIN FOR UNUSED FUNCTIONAL TP				
	I248	+3V_HALL_EFFECT				24 40
	I248	LID_CLOSED_L				24
	I248	TMDS_DN<0..2>				20 23 39
	I248	TMDS_DP<0..2>				20 23 39

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REVISION HISTORY

EVT2 RELEASE

08/13/04 - 1. CHANGE EXT TMDS SWING RESISTORS TO 510 OHM (R869, R876), REMOVE SI_RESET PULL HIGH
2. CHANGE RGB SIGNAL INPEDENCE (R341, R342, R346, R456, R458, R462)
3. ADD 2 RESISTORS (NO STUFF) BETWEEN FAN_PWM AND FAN_PWM_L OF FAN1 AND FAN2
4. CHANGE 2 CAPS (C233, C803) TO IMPROVE FEEDBACK PROTECTION AND PBUS CURRENT LIMIT CIRCUIT
5. MODIFY CPU_VCORE VID AND CPU_VCORE SETTING

08/16/04 - 1. MODIFY CPU_AVDD SETTING
08/20/04 - 1. ADD TRACKPAD POWER +5V_TPAD CONTROL CIRCUIT
09/01/04 - 1. CHANGE ALL FONTS INTO SMALL ONES
09/02/04 - 1. MODIFT CPU_VCORE VID AND CPU_VCORE SEETING AGAIN
2. MODIFY CPU_AVDD SEETING AGAIN
3. CHANGE INT TMDS DAMPING RESISTERS (R760-R767) TO 0 OHM
09/03/04 - 1. ADD MMM CIRCUIT, ARRANGE 2 INTREPID GPIOS FOR MM_FFIRQ_L, MM_SIRQ_L AND PULL UP RESISTORS R801, R802
2. ADD R803 BETWEEN DP6 AND DCDC_IN
3. ADD R804 AND SUPERCAP C692 ON +4_6V_BU
4. CHANGE TRACKPAD CONNECTOR J10 AND PIN OUT

09/06/04 - 1. ADD EMI SOLUTION L12
09/07/04 - 1. CHANGE TRACKPAD CONNECTOR PIN OUT
09/08/04 - 1. ADD BATTERY CURRENT SENSOR CIRCUIT
09/09/04 - 1. ADD EMI SOLUTION R816; ADD MMM RESET CIRCUIT
09/10/04 - 1. MODIFY FIREWIRE PORT0 POWER CIRCUIT
2. ADD NET FROM BATTERY CURRENT SENSOR CIRCUIT TO PMU
09/13/04 - 1. ADD CURRENT LIMITER R821 BETWEEN PMU(U29) AND U33
2. ADD PULL UP AND PULL DOWN RESISTORS FOR MMM SENSOR

DVT RELEASE

09/27/04 - 1. ADD ST MMM SENSOR CIRCUIT
10/14/04 - 2. ADD FIREWIRE POWER PROTECT CIRCUIT
10/15/04 - 3. CHANGE EXT_TMDS TERMINAL RESISTERS AND V SWINING RESISTOR
10/22/04 - 4. CHANGE FAN CONTROLLER FROM ADT7460 TO ADT7467
11/02/04 - 5. CHANGE BBANG IC TO ATTINY2313

PVT RELEASE

12/17/04 - 1. REMOVE ALL OPEN JUMPER
12/17/04 - 2. SCHEMATIC RELEASE FOR PRODUCTION

PVT RELEASE (REV C)

02/11/05 - 1. CHANGE FW F3 TO 740S0018

PRODUCTION RELEASE (REV D)

04/12/05 - 1. ADD MPU R1.4
2. CHANGE 88E1111 B1(338S0223) TO PRIMARY AND B0 (338S0079) TO SECONDARY

PRODUCTION RELEASE (REV E)

08/24/05 - 1. ADD MPU R1.5 (337S3217 AND 337S3218)
08/25/05 - 1. ADD 341S1792 (BOOTROM,4.9.1F3)

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL      28D2< 40B3>
+1_5V_AGP          12B5< 12D1< 12D4< 15D6< 16C8<
                 19C6< 19D6< 21A8< 21B4<> 21D5<>
                 22B8< 22D6< 40C3>
+1_5V_AGP_GPU      22C5< 40C3>
+1_5V_AGP_NECK     21B4<> 40B3>
+1_5V_GPU_VDD15    21D3< 40C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 40D3>
+1_5V_INTREPID_PLL1  14C3< 40D3>
+1_5V_INTREPID_PLL2  14D3< 40D3>
+1_5V_INTREPID_PLL3  14D3< 40D3>
+1_5V_INTREPID_PLL4  14D3< 40D3>
+1_5V_INTREPID_PLL5  12D3< 40D3>
+1_5V_INTREPID_PLL6  12D6< 40D3>
+1_5V_INTREPID_PLL7  8D5< 40D3>
+1_5V_INTREPID_PLL8  14D3< 40C3>
+1_5V_LDO          40D6>
+1_5V_MAIN         40D6>
+1_5V_SLEEP        40D6>
+1_5V_SLEEP_NECK   36D2<> 40B3>
+1_5V_SLEEP_VIN    40D6>
+1_8V_ATI_PVDD     21C5<> 22B6< 22B6< 22D6<> 40C3>
+1_8V_ATI_TPVDD    22D2<> 40B3>
+1_8V_GPU          19A8< 20A6< 21D7< 22A2< 22A6<
                 22B1< 22B6< 22C8< 22D6< 22D8< 40C3>
+1_8V_GPU_AVDD     22D5< 40B3>
+1_8V_GPU_AVDDQ    22D4< 22D7< 40B3>
+1_8V_GPU_DVO      22B2<
+1_8V_GPU_MEMPLL   22B5< 40B3>
+1_8V_GPU_PLL      22D5< 40C3>
+1_8V_GPU_PNLIO    22A5< 40B3>
+1_8V_GPU_PNLPLL   22B5< 40B3>
+1_8V_GPU_TP_PLL   22B5< 22D1< 40B3>
+1_8V_GPU_VDDDI    22C7< 22D4< 40C3>
+1_8V_MAIN         40D6> 41C6>
+1_8V_PVDD_NECK    21B5<> 40B3>
+1_8V_SLEEP        40D6>
+1_8V_SLEEP_NECK   36D2<> 40B3>
+1_95V_FW_DVDD     29C4< 29C7<> 29D5< 40A3>
+1_95V_FW_DVDD_PORT1  29D6< 40A3>
+1_95V_FW_DVDD_RX0  29C5< 40A3>
+1_95V_FW_DVDD_TX0  29C5< 40A3>
+1_95V_FW_PLL400VDD  29C4< 40A3>
+1_95V_FW_PLL500VDD  29D4< 40A3>
+1_95V_FW_PLLVDD   29D4< 29D6<> 40A3>
+2_5V_CG_MAIN      14C6<
+2_5V_GPU          22A7<> 40C3>
+2_5V_GPU_A2VDD    22D4< 22D7< 40B3>
+2_5V_GPU_MCLK     22C7< 22D4< 40B3>
+2_5V_GPU_MEMCORE  22C5< 40C3>
+2_5V_GPU_PNLIO    22A5< 40C3>
+2_5V_INTREPID     9A7< 10D3< 10D5< 10D6< 10D8< 15D6<
                 16B8< 40D3>
+2_5V_MAIN         40D6> 41C6>
+2_5V_MARVELL      28B8< 28C4< 40B3>
+2_5V_MARVELL_AVDD  28C4< 40B3>
+2_5V_MARVELL_CONN  28B3<>
+2_5V_REG          30A6<
+2_5V_REG_F        30A7<>
+2_5V_SLEEP        40D6>
+2_5V_SLEEP_NECK1  21C4<> 40B3>
+2_5V_SLEEP_NECK2  36D2<> 40B3>
+3V_AIRPORT        40C3> 41C3>
+3V_ATI_OSC_SLEEP  19B2< 40B3>
+3V_ATI_SS         19A3< 40B3>
+3V_CG_PLL_MAIN    14C6<
+3V_FW             29A3< 29D7<> 30B7<> 30D5< 40A3>
+3V_FW_AVDD        29C6< 40A3>
+3V_FW_AVDD_PORT0  29C6< 40A3>
+3V_FW_AVDD_PORT1  29C6< 40A3>
+3V_FW_AVDD_PORT2  29D6< 40A3>
+3V_FW_ESD         30A5< 30B4<> 30D3<>
+3V_FW_ESD_ILIM    30D4<
+3V_FW_ESD_R       30A6<
+3V_FW_UF          29D7<> 40A3>
+3V_GPU            12D1< 19B8< 19C6< 19C8< 19D6<
                 21C4< 21C5< 21C7< 21D7< 22A6< 22B1<
                 40C3>
+3V_GPU_FLT        22B2< 40C3>
+3V_HALL_EFFECT    24B2<> 40B6> 41C1>
+3V_INTREPID_USB   14C3< 40D3>
+3V_LCD            23B4<> 40B6> 41B6>
+3V_LCD_SW         23B4<> 40B6>
+3V_MAIN           24B8<> 40D6> 41C6>
+3V_MAIN_AUD       27C6<> 34C1<> 40B6>
+3V_MAIN_JUMPER    34D2<> 40D1>
+3V_MAIN_LMU       24D7<> 40A1>
+3V_MAIN_SSCG      40A1>
+3V_NEC_VDD        17B3< 17D7< 17D7< 40A3>
+3V_PMU            40D6> 41C6>
+3V_PMU_AVCC       27B1< 31B6< 31D5<> 40C6>
+3V_PMU_ESR        33A2< 40C6>
+3V_PMU_RESET      31C7< 35A4<> 41C1>
+3V_SENSOR         24B4<>
+3V_SLEEP          40D6> 41A6> 41B6>
+3V_SLEEP_NECK     36D1<> 40B3>
+3V_SLEEP_PCCARD   18D7< 40C3>
+3V_SLP_OK_L       34B4<>
+3V_SLP_ON         34A5<>
+4_6V_BU           33B3<> 34B7< 40C6>
+4_85V_ESR         33A4< 40C6>
+4_85V_RAW         31A4< 33B4<> 40C6>
+5V_DDC_SLEEP      23D3<> 23D5<> 40B6> 41B6>
+5V_DDC_SLEEP_UF   23D6< 40B6>
+5V_HDD            26D1<>
+5V_HD_SLEEP       26D1<> 34A7<> 40C6>
+5V_INV_SW         23B2<> 40B6> 41A6>
+5V_INV_UF_SW      23B2<> 40B6>
+5V_MAIN           40D6> 41A6> 41C6>
+5V_MAIN_AUD       27C6<> 34C8<> 40B6>
+5V_MAIN_JUMPER    34D8<> 40D1>
+5V_SLEEP          40D6> 41A6> 41C6>
+5V_SLEEP_LMU      24C6<> 24C7<>
+5V_SLEEP_OPT      26B5<> 40A1>
+5V_TPAD           24B5<>
+5V_TPAD_FB        24B4<>
+5V_TPAD_SLEEP     40B6> 41B3>
+14V_INV           23B2<> 40B6> 41B6>
+24V_PBUS          40D6> 41C6>
+ADAPTER           32D8<> 33A7< 40C6> 41D1>
+ADAPTER_ILIM      33A6<> 40C6>
+ADAPTER_OR_BATT   33A5<> 40C6>
+ADAPTER_SENSE     32D4<> 40C6>
+ADAPTER_SW        32D5<> 40C6> 40C6>
+BATT              40D6>
+BATT_14V_FUSE     32D1<> 40C6>
+BATT_24V_FUSE     32B1< 32D2<> 40C6>
+BATT_ISNS_P       25A5<> 41C1>
+BATT_POS          32A4<> 40C6> 41A3>
+BATT_RSNS         32B2< 40C6>
+BATT_VSNS         32A4< 40C6>
+FAN_PWR           27A3< 27A4< 40B6> 41A3>
+FW_AMP_SENSE      40A3>
+FW_PBUS           30D7<> 40A3>
+FW_PWR1           30B5< 40A3>
+FW_PWR_CTRL       30A7<>
+FW_PWR_OR         29B8< 29D8<> 30D5<> 40A3>
+FW_PWR_OR_F       30B7<>
+FW_PWR_OR_GATE    30B8<>
+FW_PWR_OR_GATE_L  30A8<
+FW_SW             30D5<> 40A3>
+FW_VP0            30C1<> 40A3> 41A3>
+FW_VP1            30A3<> 40A3> 41D1>
+GPU_VDD15_NECK    21B5<> 40B3>
+GPU_VDD15_UF      21B5<> 21D4<> 40B3>
+HD_LOGIC_SLEEP    26C2<> 40C6>
+PBUS              40D6> 41C6>
+PBUS_JUMPER       33C3<> 40D1>
+PPBATT_ISNS_N     25A4<> 41C1>
+PWR_SUPERCAP      33A4< 41C1>
+VCC_CBUS_SW       18B1< 18B2< 18D2<> 40C3>
+VPP_CBUS_SW       18B1< 18B2< 18D2<> 40C3>
1V20_REF           32C7< 33C8< 40D1>
1V65_REF           32A5<
1_5V_BOOST         36C6<> 40C1>
1_5V_BST           36C5<> 40C1>
1_5V_DH            36C5<> 40C1>
1_5V_DL            36B5<> 40C1>
1_5V_FB            36B5< 36B7< 40C1>
1_5V_ILIM          36C5<> 40C1>
1_5V_LX            36B5<> 40C1>
1_5V_LX_F          36B7<> 36C5<> 40C1>
1_5V_SLEEP_EN_L    36C7<> 36D7<>
1_8V_PVDD_STD      22D6<
1_8V_SLEEP_PWREN_L  36A3<>
1_8V_SW            36A5<> 40A1>
1_8V_SW_F          36A4<> 40A1>
1_8V_TPVDD_STD     22D1<
1_8V_VFB           36A5<> 40A1>
2_5V_BOOST         36C4<> 40D1>
2_5V_BST           36C4<> 40D1>
2_5V_DH            36C3<> 40D1>
2_5V_DL            36B3<> 40C1>
2_5V_FB            36B4<
2_5V_ILIM          36C5<> 40C1>
2_5V_LX            36B3<> 40D1>
2_5V_LX_F          36B2<> 36C4<> 40D1>
2_5V_SLEEP_PWREN_L  36C2<>
3V_5V_OK           24A6<> 34B4<> 36A8< 36D6<
3V_5V_OK_G         24A6<
3V_5V_OK_L         24B5<>
3V_BG              34C4<>
3V_BOOST           34C4<>
3V_BOOST_ESR       34D3<>
3V_ITH             34C4<>
3V_ITH_RC          34C3<
3V_PMU_VTAP        33B3<
3V_RSNS            34D2<> 40D1>
3V_RUNSS           34C4<
3V_SLEEP_PWREN_L   34B3<>
3V_SNSM            34C4< 39A2>
3V_SNSP            34C4< 39A2>
3V_SW              34C4<> 40D1>
3V_TG              34D4<>
3V_VOSNS           34C4<>
5V_BG              34C5<>
5V_BOOST           34C5<>
5V_BOOST_ESR       34D6<>
5V_HD_PWREN        34A8<>
5V_ITH             34C5<>
5V_ITH_RC          34C6<
5V_RSNS            34D7<> 40D1>
5V_RUNSS           34C5<
5V_SLEEP_PWREN     34A8<>
5V_SNSM            34C5< 39A2>
5V_SNSP            34C5< 39A2>
5V_SW              34C5<> 40D1>
5V_TG              34C5<>
5V_VOSNS           34C5<>
1625_BG            33C5<>
1625_BST           33C5<
1625_BST_ESR       33C5<>
1625_COMP          32D2< 33C6<
1625_DIV           33C8<
1625_ENABLE        33D7<>
1625_ENABLE_L      33D6<>
1625_EXTVCC        33D5<> 40D1>
1625_FCB           33C6<
1625_INTVCC        33C5<> 40D1>
1625_RUNSS         33C6<
1625_SGND          33B7<> 40D1>
1625_TG            33C5<>
1625_VFB           33B5<>
1625_VIN           33C6< 40D1>
1625_VSW           33C4<> 40D1>
1772_ACIN          32B5<
1772_ACOK_L        32B5<> 32C4<>
1772_BST           32B4<>
1772_BST_ESR       32C3<
1772_CCI           32B5<>
1772_CCS           32B5<
1772_CCV           32B5<>
1772_CCV_RC        32B5<
1772_CELLS         32B4<
1772_CLS           32A4<
1772_CSIN          32B4<> 39A2>
1772_CSIP          32B4<> 39A2>
1772_CSSN          32C5< 39A2>
1772_CSSP          32C5< 39A2>
1772_DCIN          32B5< 40C6>
1772_DHI           32B4<>
1772_DLO           32B4<>
1772_DLOV          32B4<> 40C6>
1772_GND           32A5<> 40C6>
1772_ICHG          32B5<>
1772_ICTL          32B5<>
1772_IINP          32B5<
1772_LDO           32C4<> 40C6>
1772_LX            32B4<> 40C6>
1772_REF           32B5<>
1772_VCTL          32B5<
1778_BG            21A5<> 40B1>
1778_BST           21A5<> 40B1>
1778_BST_RC        21A5< 40B1>
1778_FCB           21A6< 40B1>
1778_GND           21A6< 21A7<> 40B1>
1778_ION           21A5< 40B1>
1778_ITH           21A6<> 40B1>
1778_ITH_RC        21A7< 40B1>
1778_SHDN_L        21A6<>
1778_TG            21A5<> 40B1>
1778_VCC           21A5< 40B1>
1778_VFB           21A2< 21A5< 40B1> 41C6>
1778_VIN           21A5< 40B1>
1778_VRNG          21A6< 40B1>
3405_MODE          28D5<
3405_VFB           28D4<>
3707_FCB           34C5<
3707_FSET          34C5<
3707_INTVCC        34D4<> 40D1>
3707_SGND          34B5<> 40D1>
3707_STBY          34C5<>
A29_CLS_ADJ        32A5<>
A29_CURRENT_ADJ    32C4<>
A29_DETECT         31A2< 32A5<> 32C4<>
A29_DET_L          31A3<
A29_DET_REF        31A4<
AC_DET             31A4<
AC_DIV             32C7<
AC_ENABLE_GATE     32D6<>
AC_ENABLE_L        32C5<>
AC_GTR_18V         32C3<>
AC_IN              28B8<> 30C8< 31B3< 32C5<> 32C6<>
AC_IN_FW_CNTL      30C7<>
AC_IN_L            31A8<> 32C2<> 32C6<>
AC_IN_L_RC         32C2<
ADAPTER_DET        27D8<> 31A4< 41A6>
ADAPTER_I_REG      32D3<>
ADT7467_ADR_ENABLE_L  27B3<>
ADT7467_TACH3_TP   27B3<
ADT7467_THERM_L    24B4<> 27A2<> 27B3<
ADT7467_VCC        27C4<
ADT7467_VCORE_MON  5C8<> 27B4<
AGP8X_DET_PU       19C6<>
AGP_AD<0>          12D2<> 19C7<>
AGP_AD<15..0>      39D5>
AGP_AD<1>          12C2<> 19C7<>
AGP_AD<2>          12C2<> 19C7<>
AGP_AD<3>          12C2<> 19C7<>
AGP_AD<4>          12C2<> 19C7<>
AGP_AD<5>          12C2<> 19C7<>
AGP_AD<6>          12C2<> 19C7<>
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AGP_AD<12>         12C2<> 19C7<>
AGP_AD<13>         12C2<> 19C7<>
AGP_AD<14>         12C2<> 19C7<>
AGP_AD<15>         12C2<> 19C7<>
AGP_AD<16>         12C2<> 19C7<>
AGP_AD<31..16>     39D5>
AGP_AD<17>         12C2<> 19C7<>
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AGP_AD<19>         12C2<> 19C7<>
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AGP_AD<21>         12C2<> 19C7<>
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AGP_AD<25>         12C2<> 19C7<>
AGP_AD<26>         12C2<> 19D7<>
AGP_AD<27>         12B2<> 19D7<>
AGP_AD<28>         12B2<> 19D7<>
AGP_AD<29>         12B2<> 19D7<>
AGP_AD<30>         12B2<> 19D7<>
AGP_AD<31>         12B2<> 19D7<>
AGP_AD_STB<0>      12A2<> 12B2< 19D6<> 39D5>
AGP_AD_STB<1>      12A2<> 12B2< 19D6<> 39D5>
AGP_AD_STB_L<0>    12A2<> 12B2< 19D6<> 39D5>
AGP_AD_STB_L<1>    12A2<> 12A2< 19D6<> 39D5>
AGP_ATI_INT_L      14B5<> 19B7<>
AGP_ATI_RESET_L    19B7<
AGP_ATI_VREF       19B7<
AGP_ATI_VREFG      19B7<
AGP_BUSY_L         12C4<> 12D2< 19D6>
AGP_CBE<0>         12B2<> 19B7<>
AGP_CBE<1..0>      39D5>
AGP_CBE<1>         12B2<> 19B7<>
AGP_CBE<2>         12B2<> 19B7<>
AGP_CBE<3..2>      39D5>
AGP_CBE<3>         12B2<> 19B7<>
AGP_DEVSEL_L       12B2<> 12C2< 19B7<> 39D5>
AGP_FRAME_L        12B2<> 12C2< 19B7<> 39D5>
AGP_GNT_L          12C2< 12D2<> 19B7< 39D5>
AGP_IRDY_L         12B2<> 12C2< 19B7<> 39D5>
AGP_PAR            12B2<> 19B7> 39D5>
AGP_PIPE_L         12A2<> 12B2<
AGP_RBF_L          12A2<> 12C2< 19C6> 39C5>
AGP_REQ_L          12C2< 12D2<> 19B7<> 39D5>
AGP_SBA<0>         12B2< 19C6>
AGP_SBA<7..0>      39D5>
AGP_SBA<1>         12B2<> 19C6>
AGP_SBA<2>         12B2<> 19C6>
AGP_SBA<3>         12B2<> 19C6>
AGP_SBA<4>         12B2<> 19C6>
AGP_SBA<5>         12B2<> 19C6>
AGP_SBA<6>         12B2<> 19C6>
AGP_SBA<7>         12B2<> 19C6<>
AGP_SB_STB         12B2<> 12B2< 19C6<> 39D5>
AGP_SB_STB_L       12A2< 12A2<> 19C6<> 39D5>
AGP_ST<0>          12A2<> 19C6<
AGP_ST<1>          12A2<> 19C6<
AGP_ST<2>          12A2<> 19C6<
AGP_STOP_L         12B2<> 12C2< 19B7<> 39D5>
AGP_STP_L          19C6<
AGP_SUS_STAT_L_PU  19C6<
AGP_TRDY_L         12B2<> 12C2< 19B7<> 39D5>
AGP_WBF_L          12A4<> 12B2< 19B7>
AIRPORT_CLKRUN_L   26C6<> 41C3>
AIRPORT_IDSEL      26C5<>
AIRPORT_PCI_GNT_L  12D7<> 26D5<> 41C3>
AIRPORT_PCI_INT_L  14B5<> 14D7< 26D5<> 41C3>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 26D6<> 41C3>
ATI_AGP_FBSKEW<0>  21C2< 21C7<>
ATI_AGP_FBSKEW<1>  21C2< 21C7<>
ATI_BUS_CFG<0>     21B2< 21C7<>
ATI_BUS_CFG<1>     21B2< 21C7<>
ATI_BUS_CFG<2>     21B2< 21C7<>
ATI_CLK27M_IN      19A1< 21B7<> 37B1>
ATI_CLK27M_OSC     19B2< 37B1>
ATI_CLK27M_OSC_SS  19A3< 19B1< 37B1>
ATI_DBI_HI_PU      19C6<>
ATI_DBI_LO_PU      19C6<>
ATI_DVOD<0>        20B8< 21D7<>
ATI_DVOD<23..0>    38C1>
ATI_DVOD<1>        20B8< 21D7<>
ATI_DVOD<2>        20B8< 21D7<>
ATI_DVOD<3>        20B8< 21D7<>
ATI_DVOD<4>        20B8< 21D7<>
ATI_DVOD<5>        20B8< 21D7<>
ATI_DVOD<6>        20B8< 21D7<>
ATI_DVOD<7>        20B8< 21D7<>
ATI_DVOD<8>        20B8< 21D7<>
ATI_DVOD<9>        20B8< 21D7<>
ATI_DVOD<10>       20B8< 21D7<>
ATI_DVOD<11>       20A8< 21D7<>
ATI_DVOD<12>       20B6< 21D7<>
ATI_DVOD<13>       20B6< 21D7<>
ATI_DVOD<14>       20B6< 21D7<>
ATI_DVOD<15>       20B6< 21D7<>
ATI_DVOD<16>       20B6< 21D7<>
ATI_DVOD<17>       20B6< 21D7<>
ATI_DVOD<18>       20B6< 21C7<>
ATI_DVOD<19>       20B6< 21C7<>
ATI_DVOD<20>       20B6< 21C7<>
ATI_DVOD<21>       20B6< 21C7<>
ATI_DVOD<22>       20B6< 21C7<>
ATI_DVOD<23>       20A6< 21C7<>
ATI_DVOD_DE        20A6< 20A8< 21C7<> 38C1>
ATI_DVOVMODE       22A3<
ATI_DVO_CLKP       19B4< 21C7<> 38C1>
ATI_DVO_HSYNC      20A8< 21C7<> 38C1>
ATI_DVO_VSYNC      20A6< 20A8< 21C7<> 38C1>
ATI_GPIO8_PD       21C7<>
ATI_GPIO9_SPN      21C7<>
ATI_GPIO10_SPN     21C7<>
ATI_GPIO11_SPN     21C7<>
ATI_GPIO12_SPN     21C7<>
ATI_GPIO13_SPN     21C7<>
ATI_HSYNC          21D5<> 23D8<
ATI_HSYNC_BUF      23D8<>
ATI_MEMTEST        19A6<>
ATI_MEMVMODE0      19A7<
ATI_MEMVMODE1      19A7<
ATI_OSC_OE         19B3<
ATI_PVDD_BYP       22D6<>
ATI_R2SET          21D6<>
ATI_RSET           21D6<>
ATI_RSTB_MSK       19C6<>
ATI_SSCLK_IN       19A2< 21B7<> 37B1>
ATI_SSCLK_UF       19A2<> 37B1>
ATI_TESTEN         21B7<
ATI_TMDS_CLKN      20C2< 21B7> 39B2>
ATI_TMDS_CLKP      20C2< 21B7> 39B2>
ATI_TMDS_DN<0>     20D2< 21B7> 39B2>
ATI_TMDS_DN<1>     20D2< 21B7> 39B2>
ATI_TMDS_DN<2>     20C2< 21B7> 39B2>
ATI_TMDS_DP<0>     20D2< 21B7> 39B2>
ATI_TMDS_DP<1>     20D2< 21B7> 39B2>
ATI_TMDS_DP<2>     20C2< 21B7> 39B2>
ATI_TPVDD_BYP      22D1<>
ATI_VSYNC          21D5<> 23D8<
ATI_VSYNC_BUF      23D8<>
ATI_X1CLK_SKEW<0>  21C2< 21C7<>
ATI_X1CLK_SKEW<1>  21B2< 21C7<>
AUD_GND            27C8<> 40B6>
AUXWIN_PU          21C6<>
BATTV_HIGH         32B7<>
BATTV_LOW          32B8<>
BATT_14PBUS_EN     32C1<>
BATT_14V_GATE      32C1<>
BATT_24PBUS_EN     32C2<>
BATT_24V_GATE      32C1<>
BATT_CLK           32A4<> 41A3>
BATT_DATA          32A4<> 41A3>
BATT_DIV           32A5<
BATT_ISNS_OUT      25A4<>
BATT_ISNS_R        25A3<>
BATT_LOW           32A6<>
BATT_LOW_L         32B6<>
BATT_NEG           32A4<> 40C6> 41A3>
BBANG_HRESET_L     6A2< 6B3<>
BBANG_JTAG_TCK     6A4<> 6B2<> 6C2<
BBANG_TCK_EN       6A4<
BB_EEPR_ADDR0      6D3<
BB_EEPR_ADDR1      6D3<
BB_EEPR_ADDR2      6D3<
BB_EEPR_WP_PD      6D2<>
BB_MISO            6B3<> 6C2<
BB_MOSI            6B3<> 6C2<
BB_RESET_L         6C3< 41C1>
BB_SCK             6B3<> 6C2<
BFR_TDO            6C2< 6C2<>
BKFD_PROT_EN_L     32C5<>
BKFD_PROT_GATE     32D5<>
BRIGHT_PWM         23A2<> 41A6>
BRIGHT_PWM_UF      23A2<>
BT_USB_DM          14C1< 27D8<> 39B2> 41D3>
BT_USB_DP          14C1< 27D8<> 39B2> 41D3>
CBUS_ADDR<0>       18B1< 18B4>
CBUS_ADDR<1>       18B1< 18B4>
CBUS_ADDR<2>       18B1< 18B4>
CBUS_ADDR<3>       18B1< 18B4>
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CBUS_ADDR<5>       18B1< 18B4>
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CBUS_ADDR<7>       18B1< 18B4>
CBUS_ADDR<8>       18B1< 18B4>
CBUS_ADDR<9>       18B1< 18B4>
CBUS_ADDR<10>      18B4> 18C1<
CBUS_ADDR<11>      18B1< 18B4>
CBUS_ADDR<12>      18B1< 18B4>
CBUS_ADDR<13>      18B1< 18B4>
CBUS_ADDR<14>      18B1< 18B4>
CBUS_ADDR<15>      18B1< 18B4>
CBUS_ADDR<16>      18B1< 18B4<
CBUS_ADDR<17>      18B2< 18B4>
CBUS_ADDR<18>      18B2< 18B4>
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CBUS_ADDR<20>      18B2< 18B4>
CBUS_ADDR<21>      18B2< 18B4>
CBUS_ADDR<22>      18A4> 18B2<
CBUS_ADDR<23>      18A4> 18B2<
CBUS_ADDR<24>      18A4> 18B2<
CBUS_ADDR<25>      18A4> 18B2<
CBUS_ADDR_16_UF    18B5<>
CBUS_BVD1_L        18A2< 18C4<
CBUS_BVD2_L        18B2< 18C4<
CBUS_CE1_L         18C1< 18C4>
CBUS_CE2_L         18B2< 18B4>
CBUS_DATA<0>       18A1< 18A4<>
CBUS_DATA<1>       18A1< 18A4<>
CBUS_DATA<2>       18A1< 18A4<>
CBUS_DATA<3>       18A4<> 18C1<
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CBUS_DATA<5>       18A4<> 18C1<
CBUS_DATA<6>       18A4<> 18C1<
CBUS_DATA<7>       18A4<> 18C1<
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CBUS_DATA<9>       18A2< 18A4<>
CBUS_DATA<10>      18A2< 18A4<>
CBUS_DATA<11>      18A4<> 18C2<
CBUS_DATA<12>      18A4<> 18C2<
CBUS_DATA<13>      18A4<> 18C2<
CBUS_DATA<14>      18A4<> 18C2<
CBUS_DATA<15>      18A4<> 18C2<
CBUS_DET_1_L       18C2< 18C4< 41C6>
CBUS_DET_2_L       18A2< 18C4< 41C6>
CBUS_INPACK_L      18B2< 18B4<
CBUS_INT_L         14B5<> 14D7< 18A7<>
CBUS_IORD_L        18B2< 18C4>
CBUS_IOWR_L        18B2< 18C4>
CBUS_MFUNC1_PD     18A7< 18A7<>
CBUS_MFUNC2_PD     18A7< 18A7<>
CBUS_MFUNC3_PD     18A7< 18A7<>
CBUS_MFUNC4_PD     18A7< 18A7<>
CBUS_MFUNC5_PD     18A7< 18A7<>
CBUS_MFUNC6_PD     18A7< 18A7<>
CBUS_OE_L          18B1< 18C4>
CBUS_PCI_GNT_L     12D7<> 18A7<
CBUS_PCI_IDSEL     18B7<
CBUS_PCI_REQ_L     12A7< 12D7<> 18A7>
CBUS_PCI_RESET_L   18A7<
CBUS_READY         18B1< 18C4<
CBUS_REG_L         18B2< 18C4>
CBUS_RESET_L       18B2< 18C4>
CBUS_SUSPEND_PU    18A7< 18D7<
CBUS_VCCD0_L       18C4<>
CBUS_VCCD1_L       18C4<>
CBUS_VPPD0         18C4<>
CBUS_VPPD1         18C5<>
CBUS_VS1           18B2< 18C4<>
CBUS_VS2           18B2< 18C4<>
CBUS_WAIT_L        18B2< 18B4<
CBUS_WE_L          18B1< 18C4>
CBUS_WP_L          18A1< 18B4<
CG_ADDRSEL         14B7<
CG_CLKOUT          14B6<>
CG_FSEL            14B7< 14C5<
CG_FSEL_INT        14C5<>
CG_LOCK            14B7<>
CG_RESET_L         14B7<
CG_SYSCLK_EN       14B5< 14B7<
CHARGE_DISABLE     32A7<>
CHARGE_LED_L       27D8<> 31C6<> 31D7< 41A6>
CLK10M_PMU_XIN     31B6<
CLK10M_PMU_XOUT    31B6<
CLK10M_PMU_XOUT_UF  31B7<
CLK18M_INT_EXT     14B6<> 37B1>
CLK18M_INT_XIN     14A5< 37B1>
CLK18M_INT_XOUT    14A5<> 37B1>
CLK18M_XTAL_IN     14A5< 37B1>
CLK25M_ENET_XIN    28A7<>
CLK25M_ENET_XOUT   28A7<>
CLK25M_XTAL_IN     28A7<>
CLK32K_PMU_XIN     31B3<>
CLK32K_PMU_XOUT    31B3<>
CLK32K_PMU_XOUT_UF  31B2<>
CLK33M_AIRPORT     12D8< 26D5<> 37C1> 41C3>
CLK33M_AIRPORT_UF  12C7<> 37C1>
CLK33M_CBUS        12D8< 18A7< 37C1>
CLK33M_CBUS_UF     12C7<> 37C1>
CLK33M_NEC         12C8< 17B7< 37C1>
CLK33M_NEC_UF      12C7<> 37C1>
CLK66M_AGP_1_5V_TP  12C4>
CLK66M_GPU_AGP     12C8< 19B7<> 37C1>
CLK66M_GPU_AGP_UF  12C7<> 37C1>
CLKENET_LINK_GBE_REF  13C5< 28C8< 37B1>
CLKENET_LINK_GTX   13C5<> 37A1>
CLKENET_LINK_RX    13D5< 28C8< 37B1>
CLKENET_LINK_TX    13D5< 28D8< 37A1>
CLKENET_PHY_GBE_REF  28C7<> 37B1>
CLKENET_PHY_GTX    13C6< 28C7<> 37A1>
CLKENET_PHY_RX     28C7<> 37B1>
CLKENET_PHY_TX     28D7<> 37A1>
CLKFW_LINK_LCLK    13C3<> 37A1>
CLKFW_LINK_PCLK    13C3<> 29C3< 37A1>
CLKFW_PHY_LCLK     13C2< 29B7< 37A1>
CLKFW_PHY_PCLK     29B4> 29C4< 37A1>
CLKLVDS_LN         21B5> 23A4<> 39C2> 41B6>
CLKLVDS_LP         21B5> 23A4<> 39C2> 41B6>
CLKLVDS_UN         39C2>
CLKLVDS_UP         39C2>
COMM_DTR_L         14C2> 27C1<> 41B3>
COMM_GPIO_L        14C2<> 27C2<> 41B3>
COMM_RESET_L       14C5<> 27D3< 41B3>
COMM_RING_DET_L    14B5<> 14C7< 27D3< 31C6<> 41B3>
COMM_RTS_L         14C2> 27C1<> 41B3>
COMM_RXD           14C2<> 27C1<> 41B3>
COMM_SHUTDOWN      41B3>
COMM_TRXC          14C2<> 27C2<> 41B3>
COMM_TXD_L         14C2<> 27C2<> 41B3>
COMP_RC            33C6<
CPU_AACK_L         5A7< 8B5<> 8C2< 38D5>
CPU_ADDR<0>        5C7<> 8D5<>
CPU_ADDR<0..31>    38D5>
CPU_ADDR<1>        5C7<> 8D5<>
CPU_ADDR<2>        5C7<> 8D5<>
CPU_ADDR<3>        5C7<> 8D5<>
CPU_ADDR<4>        5C7<> 8D5<>
CPU_ADDR<5>        5C7<> 8C5<>
CPU_ADDR<6>        5C7<> 8C5<>
CPU_ADDR<7>        5C7<> 8C5<>
CPU_ADDR<8>        5C7<> 8C5<>
CPU_ADDR<9>        5C7<> 8C5<>
CPU_ADDR<10>       5B7<> 8C5<>
CPU_ADDR<11>       5B7<> 8C5<>
CPU_ADDR<12>       5B7<> 8C5<>
CPU_ADDR<13>       5B7<> 8C5<>
CPU_ADDR<14>       5B7<> 8C5<>
CPU_ADDR<15>       5B7<> 8C5<>
CPU_ADDR<16>       5B7<> 8C5<>
CPU_ADDR<17>       5B7<> 8C5<>
CPU_ADDR<18>       5B7<> 8C5<>
CPU_ADDR<19>       5B7<> 8C5<>
CPU_ADDR<20>       5B7<> 8C5<>
CPU_ADDR<21>       5B7<> 8C5<>
CPU_ADDR<22>       5B7<> 8C5<>
CPU_ADDR<23>       5B7<> 8C5<>
CPU_ADDR<24>       5B7<> 8C5<>
CPU_ADDR<25>       5B7<> 8C5<>
CPU_ADDR<26>       5B7<> 8C5<>
CPU_ADDR<27>       5B7<> 8C5<>
CPU_ADDR<28>       5B7<> 8C5<>
CPU_ADDR<29>       5B7<> 8C5<>
CPU_ADDR<30>       5B7<> 8C5<>
CPU_ADDR<31>       5B7<> 8C5<>
CPU_ARTRY_L        5A7<> 8B5<> 8D2< 38D5>
CPU_AVDD           5C3< 40D3>
CPU_AVDD_ADJ       5C2<
CPU_AVDD_SHDN_L    5C3<>
CPU_AVDD_VIN       5C3< 40D3>
CPU_AVDD_VOUT      5C2<> 40D3>
CPU_BG_L           5C7< 8C2< 8D5<> 38D5>
CPU_BR_L           5C7> 8D2< 8D5< 38D5>
CPU_BUS_VSEL       5C3< 7A6<
CPU_CHKSTP_OUT_L   5B3<> 5C2< 41D6>
CPU_CHKS_L         5A3< 5D2<
CPU_CI_L           5A7> 8B5<> 38D5>
CPU_CLKOUT_SPN     5C3>
CPU_CLK_EN         8A5< 31C4<>
CPU_DATA<0>        6D8<> 8D3<>
CPU_DATA<0..31>    38D5>
CPU_DATA<1>        6D8<> 8D3<>
CPU_DATA<2>        6D8<> 8D3<>
CPU_DATA<3>        6D8<> 8D3<>
CPU_DATA<4>        6D8<> 8D3<>
CPU_DATA<5>        6D8<> 8D3<>
CPU_DATA<6>        6D8<> 8D3<>
CPU_DATA<7>        6D8<> 8D3<>
CPU_DATA<8>        6D8<> 8D3<>
CPU_DATA<9>        6C8<> 8D3<>
CPU_DATA<10>       6C8<> 8D3<>
CPU_DATA<11>       6C8<> 8D3<>
CPU_DATA<12>       6C8<> 8C3<>
CPU_DATA<13>       6C8<> 8C3<>
CPU_DATA<14>       6C8<> 8C3<>
CPU_DATA<15>       6C8<> 8C3<>
CPU_DATA<16>       6C8<> 8C3<>
CPU_DATA<17>       6C8<> 8C3<>
CPU_DATA<18>       6C8<> 8C3<>
CPU_DATA<19>       6C8<> 8C3<>
CPU_DATA<20>       6C8<> 8C3<>
CPU_DATA<21>       6C8<> 8C3<>
CPU_DATA<22>       6C8<> 8C3<>
CPU_DATA<23>       6C8<> 8C3<>
CPU_DATA<24>       6C8<> 8C3<>
CPU_DATA<25>       6C8<> 8C3<>
CPU_DATA<26>       6C8<> 8C3<>
CPU_DATA<27>       6C8<> 8C3<>
CPU_DATA<28>       6C8<> 8C3<>
CPU_DATA<29>       6C8<> 8C3<>
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CPU_DATA<31>       6C8<> 8C3<>
CPU_DATA<32>       6C8<> 8C3<> 8D8<
CPU_DATA<32..63>   38D5>
CPU_DATA<33>       6C8<> 8C3<> 8D8<
CPU_DATA<34>       6C8<> 8C3<> 8D8<
CPU_DATA<35>       6C8<> 8C3<> 8D8<
CPU_DATA<36>       6B8<> 8C3<> 8D8<
CPU_DATA<37>       6B8<> 8C3<> 8D8<
CPU_DATA<38>       6B8<> 8C3<> 8D8<
CPU_DATA<39>       6B8<> 8B3<> 8D8<
CPU_DATA<40>       6B8<> 8B3<> 8C8<
CPU_DATA<41>       6B8<> 8B3<> 8C8<
CPU_DATA<42>       6B8<> 8B3<> 8C8<
CPU_DATA<43>       6B8<> 8B3<> 8C8<
CPU_DATA<44>       6B8<> 8B3<> 8C8<
CPU_DATA<45>       6B8<> 8B3<> 8C8<
CPU_DATA<46>       6B8<> 8B3<> 8B8<
CPU_DATA<47>       6B8<> 8B3<> 8B8<
CPU_DATA<48>       6B8<> 8A8< 8B3<>
CPU_DATA<49>       6B8<> 8A8< 8B3<>
CPU_DATA<50>       6B8<> 8A8< 8B3<>
CPU_DATA<51>       6B8<> 8A8< 8B3<>
CPU_DATA<52>       6B8<> 8A8< 8B3<>
CPU_DATA<53>       6B8<> 8A8< 8B3<>
CPU_DATA<54>       6B8<> 8A8< 8B3<>
CPU_DATA<55>       6B8<> 8A8< 8B3<>
CPU_DATA<56>       6B8<> 8B3< 8B3<>
CPU_DATA<57>       6B8<> 8B3< 8B3<>
CPU_DATA<58>       6B8<> 8B3< 8B3<>
CPU_DATA<59>       6B8<> 8B3< 8B3<>
CPU_DATA<60>       6B8<> 8B3< 8B3<>
CPU_DATA<61>       6B8<> 8B3< 8B3<>
CPU_DATA<62>       6A8<> 8B3< 8B3<>
CPU_DATA<63>       6A8<> 8B3< 8B3<>
CPU_DBG_L          5C3< 8A3<> 8C2< 38D5>
CPU_DRDY_L         5C3> 8A3< 8C2< 38D5>
CPU_DTI<0>         5C3< 8A3<>
CPU_DTI<0..2>      38D5>
CPU_DTI<1>         5C3< 8A3<>
CPU_DTI<2>         5C3< 8A3<>
CPU_EDTI           5A2< 5C3<
CPU_EMODE0_L       5A3< 7A4<
CPU_EMODE1_L       5A3< 5C2<
CPU_GBL_L          5A7<> 8B5<> 38D5>
CPU_HIT_L          5A7> 8B5< 8D2< 38D5>
CPU_HRESET_INV     7A7<>
CPU_HRESET_L       5B3< 5C2< 6A1<> 7A5< 7A8< 41D6>
CPU_L1TSTCLK       5B2< 5B3<
CPU_L2TSTCLK       5B3< 5C2<
CPU_LSSD_MODE      5B3< 5C2<
CPU_MCP_L          5B3< 5D2<
CPU_PLL_CFG<0>     5C3< 7D3<
CPU_PLL_CFG<1>     5C3< 7D3<
CPU_PLL_CFG<2>     5C3< 7D3<
CPU_PLL_CFG<3>     5C3< 7D3<
CPU_PLL_CFG<4>     5C3< 7D3<>
CPU_PLL_CFGEXT     7D4<>
CPU_PLL_FS00       7C4<>
CPU_PLL_FS01       7C4<
CPU_PLL_FS10       7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC    7C4<> 7C8<> 31B6<>
CPU_PMONIN_L       5A3< 5C2<
CPU_PULLDOWN       5A2< 5A3< 5A3< 5C7<>
CPU_PULLUP         5A3< 5C2<
CPU_QACK_L         5B3<> 8B5<> 38D5>
CPU_QREQ_L         5B3> 8B5< 8C2< 38D5>
CPU_SHD0_L         5A7<> 5D2<
CPU_SHD1_L         5A7<> 5D2<
CPU_SMI_L          5B3< 5C2< 31C4<>
CPU_SRESET_L       5B2< 5B3< 41D6>
CPU_SRWX_L         5A3< 5C2<
CPU_TA_L           5B3< 8A3<> 8D2< 38D5>
CPU_TBEN           5B3< 5D2< 8A5<>
CPU_TBST_L         5A7> 8B5<> 38D5>
CPU_TEA_L          5B3< 8A3<> 8C2< 38D5>
CPU_THERM_DM       6A6<> 27A6<
CPU_THERM_DP       6A6<> 27A6<
CPU_TSIZ<0>        5A7> 8B5<>
CPU_TSIZ<0..2>     38D5>
CPU_TSIZ<1>        5A7> 8B5<>
CPU_TSIZ<2>        5A7> 8B5<>
CPU_TS_L           5C7<> 8D2< 8D5<> 38D5>
CPU_TT<0>          5A7<> 8B5<>
CPU_TT<0..4>       38D5>
CPU_TT<1>          5A7<> 8B5<>
CPU_TT<2>          5A7<> 8B5<>
CPU_TT<3>          5A7<> 8B5<>
CPU_TT<4>          5A7<> 8B5<>
CPU_VCORE_HI_OC    7B8<> 31D4<> 35C8<
CPU_VCORE_PWR_SEQ  35D8<>
CPU_VCORE_SEQ      35D8<
CPU_VCORE_SEQ_L    35D8<
CPU_VCORE_SLEEP    5D2< 5D8<> 6C6<> 35C1< 35D2< 40D3>
                 41C6>
CPU_VCORE_SNUB     35B3<
CPU_WT_L           5A7> 8B5<> 38C5>
CSLOT_ADDR3_SPN    13B7>
CSLOT_ADDR4_SPN    13B7>
CSLOT_ADDR5_SPN    13B7>
CSLOT_ADDR6_SPN    13B7>
CSLOT_ADDR7_SPN    13B7>
CSLOT_ADDR8_SPN    13B7>
CSLOT_ADDR9_SPN    13B7>
CSLOT_CE1_L_SPN    13C7>
CSLOT_CE2_L_SPN    13C7>
CSLOT_IORD_L_SPN   13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN   13C7>
CSLOT_OE_L_SPN     13C7>
CSLOT_WE_L_SPN     13C7>
CURRENT_THRESHOLD  32C3<
CY25811_S0         19A3<
CY25811_S1         19A3<
DCDC_EN            21A7<> 30C8< 34B7<> 35C7<>
DCDC_EN_CTRL       30C7<>
DCDC_EN_L          34B6< 34B7<> 36C7<>
DDC_CLK_ISO        23D4<>
DDR_VREF           11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                 40D3>
DVI_DDC_CLK        23D4<>
DVI_DDC_CLK_UF     23C5<> 23D3<> 41B6>
DVI_DDC_DATA       23C4<>
DVI_DDC_DATA_UF    23C5<> 41B6>
DVI_HPD            23C4<>
DVI_HPD_DIV        23C2<
DVI_HPD_UF         23C3< 23C5<> 41B6>
DVI_TURN_ON        23D3<>
DVI_TURN_ON_BASE   23D2<>
DVI_TURN_ON_ILIM   23D2<
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EIDE_ADDR<2..0>    39B5>
EIDE_ADDR<1>       13B7> 26B8<
EIDE_ADDR<2>       13B7> 26B8<
EIDE_CS0_L         13B7> 26B8< 39B5>
EIDE_CS1_L         13B7> 26A8< 39B5>
EIDE_DATA<0>       13C7<> 26C8<
EIDE_DATA<15..0>   39B5>
EIDE_DATA<1>       13C7<> 26C8<
EIDE_DATA<2>       13C7<> 26C8<
EIDE_DATA<3>       13C7<> 26C8<
EIDE_DATA<4>       13C7<> 26B8<
EIDE_DATA<5>       13B7<> 26B8<
EIDE_DATA<6>       13B7<> 26B8<
EIDE_DATA<7>       13B7<> 26B8<
EIDE_DATA<8>       13B7<> 26D8<
EIDE_DATA<9>       13B7<> 26C8<
EIDE_DATA<10>      13B7<> 26D8<
EIDE_DATA<11>      13B7<> 26C8<
EIDE_DATA<12>      13B7<> 26C8<
EIDE_DATA<13>      13B7<> 26C8<
EIDE_DATA<14>      13B7<> 26C8<
EIDE_DATA<15>      13B7<> 26C8<
EIDE_DMACK_L       13A7<> 26A8< 39B5>
EIDE_DMARQ         13A7< 26A8< 39B5>
EIDE_INT           13A7< 26A8< 39B5>
EIDE_IOCHRDY       13B7< 26A8< 39B5>
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EIDE_OPTICAL_ADDR<2..0>  39B5> 41C3>
EIDE_OPTICAL_ADDR<1>  26A5<> 26B7<
EIDE_OPTICAL_ADDR<2>  26A6<> 26B7<
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EIDE_OPTICAL_CS1_L  26A6<> 26A7< 39B5> 41C3>
EIDE_OPTICAL_DATA<0>  26A5<> 26C7<
EIDE_OPTICAL_DATA<15..0>  39B5> 41C3>
EIDE_OPTICAL_DATA<1>  26A5<> 26C7<
EIDE_OPTICAL_DATA<2>  26A5<> 26C7<
EIDE_OPTICAL_DATA<3>  26A5<> 26C7<
EIDE_OPTICAL_DATA<4>  26A5<> 26B7<
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EIDE_OPTICAL_DATA<13>  26A6<> 26C7<
EIDE_OPTICAL_DATA<14>  26A6<> 26C7<
EIDE_OPTICAL_DATA<15>  26A6<> 26C7<
EIDE_OPTICAL_DMAACK_L  26A6<> 26A7< 39A5> 41C3>
EIDE_OPTICAL_DMA_RQ  26A6<> 26A7< 39A5> 41C3>
EIDE_OPTICAL_INT  26A5<> 26A7< 39A5> 41B3>
EIDE_OPTICAL_IOCHRDY  26A5<> 26A7< 39A5> 41B3>
EIDE_OPTICAL_READ_L  26A6<> 26A7< 39B5> 41C3>
EIDE_OPTICAL_RST_L  26A7< 26B5<> 39A5> 41C3>
EIDE_OPTICAL_WR_L  26A5<> 26A7< 39B5> 41B3>
EIDE_RD_L          13A7> 26A8< 39B5>
EIDE_RST_L         13B7> 26A8< 39B5>
EIDE_WR_L          13A7> 26A8< 39B5>
ENET_COL           13C5< 28B7> 39A5>
ENET_COMA          28B7<>
ENET_CRS           13C5< 28B7> 39A5>
ENET_CTAP_CHGND    40A6>
ENET_ENERGY_DET    14B5<> 28B7<>
ENET_HSDACM        28A7<>
ENET_HSDACP        28A7<>
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ENET_LINK_RXD<7..0>  39A5>
ENET_LINK_RXD<1>   13C5< 28C7>
ENET_LINK_RXD<2>   13C5< 28C7>
ENET_LINK_RXD<3>   13C5< 28B7>
ENET_LINK_RXD<4>   13C5< 28B7>
ENET_LINK_RXD<5>   13C5< 28B7>
ENET_LINK_RXD<6>   13C5< 28B7>
ENET_LINK_RXD<7>   13C5< 28B7>
ENET_LINK_TXD<0>   13B4< 13D5>
ENET_LINK_TXD<7..0>  39A5>
ENET_LINK_TXD<1>   13B4< 13D5>
ENET_LINK_TXD<2>   13B4< 13D5>
ENET_LINK_TXD<3>   13B4< 13D5>
ENET_LINK_TXD<4>   13B4< 13D5>
ENET_LINK_TXD<5>   13B4< 13D5>
ENET_LINK_TXD<6>   13A4< 13D5>
ENET_LINK_TXD<7>   13A4< 13D5>
ENET_LINK_TX_EN    13D5<> 39A5>
ENET_LINK_TX_ER    13D5<> 39A5>
ENET_MDC           13C5> 28B7< 39A5>
ENET_MDIO          13C5<> 28B7<> 39A5>
ENET_PHY_TXD<0>    13B5< 28C7<
ENET_PHY_TXD<7..0>  39A5>
ENET_PHY_TXD<1>    13B5< 28C7<
ENET_PHY_TXD<2>    13B5< 28C7<
ENET_PHY_TXD<3>    13B5< 28C7<
ENET_PHY_TXD<4>    13B5< 28C7<
ENET_PHY_TXD<5>    13B5< 28C7<
ENET_PHY_TXD<6>    13A5< 28C7<
ENET_PHY_TXD<7>    13A5< 28C7<
ENET_PHY_TX_EN     13D6< 28C7< 39A5>
ENET_PHY_TX_ER     13D6< 28C7< 39A5>
ENET_RSET          28A5<
ENET_RST_L         28B7<
ENET_RX_DV         13D5< 28B7> 39A5>
ENET_RX_ER         13C5< 28B7> 39A5>
ENET_VSSC          28A7<>
ESP_EN_L           6C2<> 6C2<
EXT_TMDS_D3_CMF    20B3<
EXT_TMDS_D4_CMF    20A3<
EXT_TMDS_D5_CMF    20A3<
FAN1_GND           40B6> 41A3>
FAN1_PWM           27A4<>
FAN1_PWM_L         27A5<> 27B2<>
FAN1_TACH          27A4< 27B2< 41A3>
FAN2_GND           40B6> 41A3>
FAN2_PWM           27A3<>
FAN2_PWM_L         27A3<> 27B2<>
FAN2_TACH          27A3< 27B2< 41A3>
FB_4_85V_BU        33A5<
FP_PWR_EN          21C6<> 23A5< 23B3<>
FP_PWR_EN_L        23B3<>
FWB_TPB0           29A3<
FWB_TPB1           29A3<
FWPLL_BYP          29D8<>
FW_BIAS0           29A4<>
FW_BIAS1           29A4<>
FW_BMODE           29B6<
FW_CORE_ADJ        29C7<
FW_CORE_BYP        29C7<>
FW_CPS             29B6<
FW_GATE_EN         30D6<>
FW_GATE_EN_RC      30C6<>
FW_INPUT_PD        29A6<
FW_LINK_CNTL<0>    13C3<> 29C3<
FW_LINK_CNTL<1..0>  39A5>
FW_LINK_CNTL<1>    13C3<> 29C3<
FW_LINK_DATA<0>    13D3<> 29B7<
FW_LINK_DATA<7..0>  39A5>
FW_LINK_DATA<1>    13D3<> 29B7<
FW_LINK_DATA<2>    13D3<> 29B7<
FW_LINK_DATA<3>    13D3<> 29B7<
FW_LINK_DATA<4>    13C3<> 29B7<
FW_LINK_DATA<5>    13C3<> 29A7<
FW_LINK_DATA<6>    13C3<> 29A7<
FW_LINK_DATA<7>    13C3<> 29A7<
FW_LINK_LREQ       13C3<> 39A5>
FW_LKON            13C3<> 29B4<>
FW_OSC             29A4< 37A1>
FW_OSC_EN          29A3<
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FW_PC_PU           29B6<
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FW_PHY_CNTL<1..0>  39A5>
FW_PHY_CNTL<1>     29B4<> 29C4<
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FW_PHY_DATA<7..0>  39A5>
FW_PHY_DATA<1>     29B7<>
FW_PHY_DATA<2>     29B7<>
FW_PHY_DATA<3>     29B7<>
FW_PHY_DATA<4>     29B7<>
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FW_PHY_DATA<7>     29A7<>
FW_PHY_LPS         13C3<> 29B7<
FW_PHY_LREQ        13C2< 29B7<> 39A5>
FW_PHY_PD          14C5<> 29B7<
FW_PHY_RESET_L     29A7<
FW_PINT            13C3<> 29B4> 39A5>
FW_PLL_ADJ         29C7<
FW_PORT1_SEL       29B6<
FW_POWER_UP        30C7<>
FW_R0              29A4<>
FW_R1              29A4<>
FW_TESTM           29A6<
FW_TPA1N           29B2<> 30A4<> 39D2>
FW_TPA1P           29B2<> 30A4<> 39D2>
FW_TPAO0N          30C2<> 39D2>
FW_TPAO0P          30C2<> 39D2>
FW_TPB1N           29A2<> 30A4<> 39D2>
FW_TPB1P           29B2<> 30A4<> 39D2>
FW_TPB2_PD         29A4<>
FW_TPBI0N          30C2<> 39D2>
FW_TPBI0P          30C2<> 39D2>
FW_TPI0N           29B2<> 30C3<> 39D2> 41A3>
FW_TPI0P           29B2<> 30C3<> 39D2> 41A3>
FW_TPI1N           30A3<> 39D2> 41D1>
FW_TPI1P           30A3<> 39D2> 41D1>
FW_TPO0N           29B2<> 30C3<> 39D2> 41A3>
FW_TPO0P           29B2<> 30C3<> 39D2> 41A3>
FW_TPO0R           30C1<> 41A3>
FW_TPO1N           30A3<> 39D2> 41D1>
FW_TPO1P           30A3<> 39D2> 41D1>
FW_VDD_ON          40A3>
FW_VGND            41A3> 41D1>
FW_VGND0           30C1<> 40A3>
FW_VGND1           30A3<> 40A3>
FW_VREG_PD         29A6<
FW_XI              29A4<> 37A1>
GPU_AGP_TEST       19C6<
GPU_B              21D6<> 23C8<> 38A1>
GPU_C              21D6<> 23A8<
GPU_COMP           21D6<> 23A8<
GPU_CORE_OK        21A6<> 21D4<> 22D2<> 22D7<>
GPU_DVI_DDC_CLK    21C5<> 23D3<>
GPU_DVI_DDC_DATA   21C5<> 23C3<>
GPU_DVO_CLKP       19B3<
GPU_DVO_CLKP_R1    19B2< 20A8<> 38C1>
GPU_DVO_CLKP_R2    19B2< 20A6<> 38C1>
GPU_G              21D6<> 23C8<> 38B1>
GPU_HPD            21C5<> 23C3<>
GPU_MEM_IO         19A6<> 19B8< 22A7< 22B4< 22D2<
                 40C3>
GPU_MEM_IO_FLT     22C2< 40C3>
GPU_R              21D6<> 23B8<> 38B1>
GPU_THERM_DM       19A6<> 27A6<
GPU_THERM_DP       19A6<> 27A6<
GPU_TV_GND1        23B8<> 40B6>
GPU_TV_GND2        23A8<> 40B6>
GPU_VCORE          19D8<> 21B3<> 21B5<> 21D4< 40C3>
                 41C6>
GPU_VCORE_CNTL     21A3<>
GPU_VCORE_CNTL_L   21A4<> 21B7<>
GPU_VCORE_CNTL_RC  21A3<>
GPU_VCORE_NECK     21B5<> 40B3>
GPU_VCORE_PWR_SEQ  21A8<>
GPU_VCORE_SEQ      21A8<
GPU_VCORE_SEQ_L    21A8<
GPU_VCORE_SW       21A4<> 40B1>
GPU_VCORE_SW_F     21A3<> 40B1>
GPU_VCORE_VDDCI    19C8< 19D6< 40B3>
GPU_Y              21D6<> 23B8<
HD_ADDR<0>         26C2<> 26C3<
HD_ADDR<2..0>      39C5>
HD_ADDR<1>         26C2<> 26C3<
HD_ADDR<2>         26B3< 26C1<>
HD_CS0_L           26C2<> 26C3< 39B5>
HD_CS1_L           26B3< 26C1<> 39B5>
HD_DATA<0>         26C2<> 26D3<
HD_DATA<15..0>     39C5>
HD_DATA<1>         26C2<> 26D3<
HD_DATA<2>         26D2<> 26D3<
HD_DATA<3>         26D2<> 26D3<
HD_DATA<4>         26C3< 26D2<>
HD_DATA<5>         26C3< 26D2<>
HD_DATA<6>         26C3< 26D2<>
HD_DATA<7>         26C3< 26D2<>
HD_DATA<8>         26C3< 26D1<>
HD_DATA<9>         26C3< 26D1<>
HD_DATA<10>        26C3< 26D1<>
HD_DATA<11>        26D1<> 26D3<
HD_DATA<12>        26B3< 26D1<>
HD_DATA<13>        26B3< 26D1<>
HD_DATA<14>        26C1<> 26C3<
HD_DATA<15>        26B3< 26C1<>
HD_DIOR_L          26A3< 26C2<> 39B5>
HD_DIOW_L          26A3< 26C1<> 39B5>
HD_DMACK_L         26A3< 26C2<> 39B5>
HD_DMARQ           13C6< 26C2<> 39B5>
HD_INTRQ           13C6< 26C1<> 39B5>
HD_IOCHRDY         26A3< 26C1<> 39B5>
HD_RESET_L         26A3< 26D2<> 39C5>
HIGH_VCORE         21A2<>
HIGH_VCORE_DIVD    21A3<
HPD_4V_REF         23C2<
HPD_PWR_SNS_EN     21C7<> 23C3<>
HPD_PWR_SW         23C1<
HPD_PWR_SW_BASE    23C2<>
HPD_REF_EN_L       23C2<>
IAC_FB             32D4<
IAC_RC_COMP        32D3<
ICT_TRST_L         6B2<> 6C2<
INTREPID_ACS_REF   8A5<
INT_AGPPVT         12D4<>
INT_AGP_FB_IN      12C4< 37C1>
INT_AGP_FB_OUT     12C4<> 37C1>
INT_AGP_VREF       12B5< 12D4<> 19D6< 40C3>
INT_CPUFB_IN       8A5< 8B5< 37D1>
INT_CPUFB_IN_NORM  8A4< 37D1>
INT_CPUFB_LONG     8A3< 37D1>
INT_CPUFB_OUT      8A5<> 8A5< 37D1>
INT_CPUFB_OUT_NORM  8A4< 37D1>
INT_CPUFB_OUT_SHORT  8A5< 37D1>
INT_DDRCLK2_N_TP   9B6<>
INT_DDRCLK2_P_TP   9B6<>
INT_DDRCLK5_N_TP   9B6<>
INT_DDRCLK5_P_TP   9B6<>
INT_ENET_RST_L     14B5<> 28B8<
INT_EXTINT3_PU     14A7< 14B5<>
INT_EXTINT8_PU     14B5<> 14C7<
INT_EXTINT10_PU    14B5<> 14B7<
INT_EXTINT13_PU    14B5<> 14B7<
INT_EXTINT14_PU    14B5<> 14C7<
INT_EXTINT16_PU    14B5<> 14B7<
INT_GPIO1_PU       14B7< 14C5<> 35C8<
INT_GPIO9_PU       14B5<> 14B7<
INT_GPIO12_PU      14B5<> 14B7<
INT_GPIO15_PU      14B5<> 14B7<
INT_I2C_CLK0       6B3<> 6D2<> 11A5<> 11A8<> 13C2<
                 13C3<> 24D7<> 41C6>
INT_I2C_CLK1       13C2< 13C3<> 14B7< 24B3<> 25C2<>
                 27B4<> 41C6>
INT_I2C_CLK2       14A2<> 27D7<> 41A6>
INT_I2C_DATA0      6B3<> 6D2<> 11A5<> 11A8<> 13C2<
                 13C3<> 24D7<> 41C6>
INT_I2C_DATA1      13B2< 13C3<> 14B7< 24B3<> 25C2<>
                 27B4<> 41C6>
INT_I2C_DATA2      14A2<> 27D7<> 41A6>
INT_I2S0_SND_FROM_ADC  14B2< 27D7<> 41A6>
INT_I2S0_SND_LRCLK  14B1< 27D8<> 41A6>
INT_I2S0_SND_LRCLK_UF  14A3<>
INT_I2S0_SND_MCLK  14B1< 27D8<> 37B1> 41A6>
INT_I2S0_SND_MCLK_UF  14A3<>
INT_I2S0_SND_SCLK  14B1< 27D7<> 41A6>
INT_I2S0_SND_SCLK_UF  14A3<>
INT_I2S0_SND_TO_DAC  14B1< 27D8<> 41A6>
INT_I2S0_SND_TO_DAC_UF  14B3<>
INT_JTAG_TEI       13C2< 13C5< 41D6>
INT_MEM_REF_H      9B6< 40C3>
INT_MEM_VREF       9A7< 9B6<> 40C3>
INT_MOD_BITCLK     14A1< 27C3<
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT     14A1< 27C3<
INT_MOD_CLKOUT_UF  14A3<> 14A7<
INT_MOD_DTI        14A2< 14A7< 27C3<
INT_MOD_DTO        14B1< 27C3<
INT_MOD_DTO_UF     14A3<> 14A7<
INT_MOD_SYNC       14A1< 27C3<
INT_MOD_SYNC_UF    14A3<> 14A7<
INT_PCI_FB_IN      12C7< 37C1>
INT_PCI_FB_OUT     12C7<> 37C1>
INT_PEND_PROC_INT  14A5< 31C4<>
INT_PROC_SLEEP_REQ_L  14A5< 31B4<>
INT_PU_RESET_L     13D3< 27D5<> 31A2< 31C4<>
INT_REF_CLK_IN     14A5< 14B5< 37C1>
INT_REF_CLK_OUT    14A5< 14B7< 37C1>
INT_REF_CLK_OUT_UF  14A5<> 37C1>
INT_RESET_L        9B3< 13D3< 31C7< 31D4<>
INT_ROM_CS_L       12A5< 12C7>
INT_ROM_OE_L       12A5< 12C7>
INT_ROM_RW_L       12A5< 12C7>
INT_SUSPEND_ACK_L  8B5> 31B6<>
INT_SUSPEND_REQ_L  8B5< 31B6<> 31C7<
INT_TDO            13C5> 13D2< 14A6< 28A5<
INT_TST_MONIN_PD   13C2< 13C5< 41C6>
INT_TST_MONOUT_TP  13C5> 41C6>
INT_TST_PLLEN_PD   13C5< 13D2< 41C6>
INT_WATCHDOG_L     14A5> 31C6<>
INV_GND            23A1<> 41A6>
INV_ON_PWM         21C6<> 23A3<
IO_RESET_L         17A8< 24D7<> 25C2< 28B8< 31C6<>
                 31D7<
JTAG_ASIC_TCK      13C5< 13D2< 28A5< 41D6>
JTAG_ASIC_TDI      13C5< 13D2< 41D6>
JTAG_ASIC_TDO_TP   28A5> 41D6>
JTAG_ASIC_TMS      13C5< 13D2< 28A5< 41D6>
JTAG_ASIC_TRST_L   13C2< 13C5< 28A5< 41D6>
JTAG_CPU_TCK       5A2< 5B3< 6A3> 41D6>
JTAG_CPU_TDI       5B2< 5C3< 6B2<> 41D6>
JTAG_CPU_TDO_TP    5C3> 41D6>
JTAG_CPU_TMS       5B2< 5B3< 6B2<> 41D6>
JTAG_CPU_TRST_L    5B3< 6A4< 6B2<> 41D6>
KBDLED_ANODE       24B3<> 24D7<>
KBDLED_RETURN      24B3<> 24D7<>
KBD_CAPSLOCK_LED   41B3>
KBD_COMMAND_L      24C2< 31C6<> 41B3>
KBD_CONTROL_L      24C2< 31C6<> 41A3>
KBD_FUNCTION_L     24C2< 31B6<> 41B3>
KBD_ID             24D2< 31B6<> 41B3>
KBD_INTL           41B3>
KBD_JIS            41B3>
KBD_NUMLOCK_LED    41B3>
KBD_OPTION_L       24C2< 31B6<> 41B3>
KBD_SHIFT_L        24C2< 31C6<> 41A3>
KBD_X<0>           24D2< 31C6<>
KBD_X<0..9>        41A3>
KBD_X<1>           24D2< 31C6<>
KBD_X<2>           24C2< 31C6<>
KBD_X<3>           24C2< 31C6<>
KBD_X<4>           24C2< 31C6<>
KBD_X<5>           24C2< 31C6<>
KBD_X<6>           24C2< 31C6<>
KBD_X<7>           24C2< 31C6<>
KBD_X<8>           24C2< 31C6<>
KBD_X<9>           24C2< 31C6<>
KBD_Y<0..7>        41A3>
LCD_DIGON_L        23B6<
LCD_PWREN_L        23B5<>
LED_LINK10         28B5<>
LED_LINK100        28B5<>
LED_RX_SPN         28B5>
LID_CLOSED_L       24A3<> 41C1>
LM2594_IN          29D8<> 40A3>
LMU_DETECT         24C7<> 24D6<> 41D1>
LT1962_INT_ADJ     14D7<
LT1962_INT_BYP     14D7<>
LTC1625_ITH        32D2<>
LTC1962_INT_VIN    14D8<> 40A1>
LTC3405_SW         28D4<> 40A3>
LTC3411_EN_L       36A7<
LTC3411_GND        36A5<> 40A1>
LTC3411_ITH        36A5<> 40A1>
LTC3411_ITH_RC     36A5<> 40A1>
LTC3411_SHDN       36A6<> 40A1>
LTC3411_SYNC       36A6<> 40A1>
LTC3411_VCC        36A6< 36A7<> 40B1>
LTC3707_START_RC   34B6<
LUX_ALS_GAIN_SW    24B8<> 24D6<>
LUX_ALS_OUT        24B8<> 24D6<>
LVDS_DDC_CLK       21C5<> 23A4< 23B4<> 41B6>
LVDS_DDC_DATA      21C5<> 23A4< 23B4<> 41B6>
LVDS_L0N           21B5> 23B4<> 39C2> 41B6>
LVDS_L0P           21B5> 23B4<> 39C2> 41B6>
LVDS_L1N           21B5> 23B4<> 39C2> 41B6>
LVDS_L1P           21B5> 23B4<> 39C2> 41B6>
LVDS_L2N           21B5> 23A4<> 39C2> 41B6>
LVDS_L2P           21B5> 23A4<> 39C2> 41B6>
LVDS_L3N_TP        21B5>
LVDS_L3P_TP        21B5>
LVDS_U0N           39C2>
LVDS_U0P           39C2>
LVDS_U1N           39C2>
LVDS_U1P           39C2>
LVDS_U2N           39C2>
LVDS_U2P           39C2>
MAIN_RESET_L       14C7< 17A8< 18A7< 19B8< 20B6<
                 26D6<> 31D4<> 31D7< 41C3>
MASTER_SWING       20B7< 20D6<
MAX1715_GND        36B5<> 36C5<> 40C1>
MAX1715_ON_RC      36C7<>
MAX1715_REF        36B5<> 40C1>
MAX1715_SKIP       36C4< 40C1>
MAX1715_TON        36C5< 40C1>
MAX1715_VCC        36D5< 40C1>
MAX4172_OUT        32D4<>
MAXBUS_SLEEP       5D2< 5D5< 6A3< 6B2< 6B4< 7B7< 7D8<
                 8B3< 8B8< 8C8< 8D1< 8D8< 15D8< 16D8<
                 35D8< 40D3>
MDI0_PD            28B4<
MDI1_PD            28B4<
MDI2_PD            28B4<
MDI3_PD            28B3<
MDI_M<0>           28B5<> 39D2>
MDI_M<0..3>        41A3>
MDI_M<1>           28B5<> 39D2>
MDI_M<2>           28B5<> 39C2>
MDI_M<3>           28B5<> 39C2>
MDI_P<0>           28B5<> 39D2>
MDI_P<0..3>        41A3>
MDI_P<1>           28B5<> 39D2>
MDI_P<2>           28B5<> 39C2>
MDI_P<3>           28B5<> 39C2>
MEM_ADDR<0>        9B5< 9D6<>
MEM_ADDR<12..0>    37A5>
MEM_ADDR<1>        9B5< 9D6<>
MEM_ADDR<2>        9B5< 9D6<>
MEM_ADDR<3>        9B5< 9D6<>
MEM_ADDR<4>        9B5< 9D6<>
MEM_ADDR<5>        9B5< 9D6<>
MEM_ADDR<6>        9B5< 9D6<>
MEM_ADDR<7>        9B5< 9D6<>
MEM_ADDR<8>        9B5< 9D6<>
MEM_ADDR<9>        9A5< 9D6<>
MEM_ADDR<10>       9A5< 9D6<>
MEM_ADDR<11>       9A5< 9D6<>
MEM_ADDR<12>       9A5< 9D6<>
MEM_BA<0>          9A5< 9D6<>
MEM_BA<1..0>       37A5>
MEM_BA<1>          9A5< 9C6<>
MEM_CAS_L          9A5< 9C6<> 37A5>
MEM_CKE<0>         9B6<> 9C5<
MEM_CKE<3..0>      37A5>
MEM_CKE<1>         9B6<> 9C5<
MEM_CKE<2>         9B6<> 9C5<
MEM_CKE<3>         9B6<> 9C5<
MEM_CS_L<0>        9C5< 9C6<>
MEM_CS_L<3..0>     37A5>
MEM_CS_L<1>        9C5< 9C6<>
MEM_CS_L<2>        9C5< 9C6<>
MEM_CS_L<3>        9C5< 9C6<>
MEM_DATA<0>        9D8<> 10C7<>
MEM_DATA<7..0>     37D5>
MEM_DATA<1>        9D8<> 10C7<>
MEM_DATA<2>        9D8<> 10C7<>
MEM_DATA<3>        9D8<> 10C7<>
MEM_DATA<4>        9D8<> 10C7<>
MEM_DATA<5>        9D8<> 10C7<>
MEM_DATA<6>        9D8<> 10C7<>
MEM_DATA<7>        9D8<> 10C7<>
MEM_DATA<8>        9D8<> 10C7<>
MEM_DATA<15..8>    37D5>
MEM_DATA<9>        9D8<> 10C7<>
MEM_DATA<10>       9D8<> 10C7<>
MEM_DATA<11>       9D8<> 10C7<>
MEM_DATA<12>       9D8<> 10B7<>
MEM_DATA<13>       9C8<> 10B7<>
MEM_DATA<14>       9C8<> 10B7<>
MEM_DATA<15>       9C8<> 10B7<>
MEM_DATA<16>       9C8<> 10C5<>
MEM_DATA<23..16>   37C5>
MEM_DATA<17>       9C8<> 10C5<>
MEM_DATA<18>       9C8<> 10C5<>
MEM_DATA<19>       9C8<> 10C5<>
MEM_DATA<20>       9C8<> 10C5<>
MEM_DATA<21>       9C8<> 10C5<>
MEM_DATA<22>       9C8<> 10C5<>
MEM_DATA<23>       9C8<> 10C5<>
MEM_DATA<24>       9C8<> 10C5<>
MEM_DATA<31..24>   37C5>
MEM_DATA<25>       9C8<> 10C5<>
MEM_DATA<26>       9C8<> 10C5<>
MEM_DATA<27>       9C8<> 10C5<>
MEM_DATA<28>       9C8<> 10C5<>
MEM_DATA<29>       9C8<> 10B5<>
MEM_DATA<30>       9C8<> 10B5<>
MEM_DATA<31>       9C8<> 10B5<>
MEM_DATA<32>       9C8<> 10C3<>
MEM_DATA<39..32>   37C5>
MEM_DATA<33>       9C8<> 10C3<>
MEM_DATA<34>       9C8<> 10C3<>
MEM_DATA<35>       9C8<> 10C3<>
MEM_DATA<36>       9C8<> 10C3<>
MEM_DATA<37>       9C8<> 10C3<>
MEM_DATA<38>       9C8<> 10C3<>
MEM_DATA<39>       9B8<> 10C3<>
MEM_DATA<40>       9B8<> 10C3<>
MEM_DATA<47..40>   37B5>
MEM_DATA<41>       9B8<> 10C3<>
MEM_DATA<42>       9B8<> 10C3<>
MEM_DATA<43>       9B8<> 10C3<>
MEM_DATA<44>       9B8<> 10C3<>
MEM_DATA<45>       9B8<> 10B3<>
MEM_DATA<46>       9B8<> 10B3<>
MEM_DATA<47>       9B8<> 10B3<>
MEM_DATA<48>       9B8<> 10C1<>
MEM_DATA<55..48>   37B5>
MEM_DATA<49>       9B8<> 10C1<>
MEM_DATA<50>       9B8<> 10C1<>
MEM_DATA<51>       9B8<> 10C1<>
MEM_DATA<52>       9B8<> 10C1<>
MEM_DATA<53>       9B8<> 10C1<>
MEM_DATA<54>       9B8<> 10C1<>
MEM_DATA<55>       9B8<> 10C1<>
MEM_DATA<56>       9B8<> 10C1<>
MEM_DATA<63..56>   37A5>
MEM_DATA<57>       9B8<> 10C1<>
MEM_DATA<58>       9B8<> 10C1<>
MEM_DATA<59>       9B8<> 10C1<>
MEM_DATA<60>       9B8<> 10C1<>
MEM_DATA<61>       9B8<> 10B1<>
MEM_DATA<62>       9B8<> 10B1<>
MEM_DATA<63>       9B8<> 10B1<>
MEM_DQM<0>         9C6<> 10C7<> 37D5>
MEM_DQM<1>         9C6<> 10B7<> 37D5>
MEM_DQM<2>         9C6<> 10C5<> 37C5>
MEM_DQM<3>         9C6<> 10B5<> 37C5>
MEM_DQM<4>         9C6<> 10C3<> 37B5>
MEM_DQM<5>         9C6<> 10B3<> 37B5>
MEM_DQM<6>         9C6<> 10C1<> 37B5>
MEM_DQM<7>         9C6<> 10B1<> 37A5>
MEM_DQS<0>         9C6<> 10C7<> 37D5>
MEM_DQS<1>         9C6<> 10B7<> 37D5>
MEM_DQS<2>         9C6<> 10C5<> 37C5>
MEM_DQS<3>         9C6<> 10B5<> 37C5>
MEM_DQS<4>         9C6<> 10C3<> 37B5>
MEM_DQS<5>         9C6<> 10B3<> 37B5>
MEM_DQS<6>         9C6<> 10C1<> 37B5>
MEM_DQS<7>         9C6<> 10B1<> 37A5>
MEM_MUXSEL_LSB     9B6<> 10B5<> 10B7<> 37A5>
MEM_MUXSEL_LSB_L_TP  9B6<>
MEM_MUXSEL_MSB     9B6<> 10B1<> 10B3<> 37A5>
MEM_MUXSEL_MSB_L_TP  9B6<>
MEM_RAS_L          9A5< 9C6<> 37A5>
MEM_WE_L           9A5< 9C6<> 37A5>
MMM_ACC_DETECT     25B8<> 25C2<>
MMM_ACC_PWRDOWN    25B8<> 25C1< 25C7<>
MMM_ACC_SELFTEST   25B8<> 25C2<> 25C7<> 41C1>
MMM_ACC_X_AXIS     25C5> 25C6< 25D2<> 41C1>
MMM_ACC_Y_AXIS     25B6< 25C2<> 25C5> 41C1>
MMM_ACC_Z_AXIS     25B6< 25C2<> 25C5> 41C1>
MMM_FFIRQ_L        14A6< 14B5<> 25C1<
MMM_PIC_AAC_PWRDOWN  25C2<>
MMM_PIC_AN2_PD     25C4<>
MMM_PIC_AN3_PU     25C4<>
MMM_PIC_FFIRQ_L    25C2<>
MMM_PIC_SIRQ_L     25C2<>
MMM_RESET_L        25C1<> 25C2<>
MMM_SIRQ_L         14A6< 14B5<> 25C1<
MPIC_CPU_INT_L     5B2< 5B3< 14B5>
MSEN_M             20B7> 20D7<
MSEN_S             20B4> 20D6<
NEC_AMC_TP         17A5<
NEC_AVDD           17D6< 40A3>
NEC_AVSS_F         17A5< 17B4<
NEC_CRUN_L         17A7<>
NEC_IDSEL          17B7<
NEC_IO_RESET_L     17A7< 17B7<
NEC_LEGC           17A7< 17A8<
NEC_LUSB_OCI       17B3< 17B5<
NEC_LUSB_OCI_UF    17B1< 27D8<> 41A6>
NEC_LUSB_PPON      17B5> 27D8<> 41A6>
NEC_MAIN_RESET_L   17A7< 17A7<
NEC_NANDTESTEN_TP  17A4<
NEC_NANDTESTOUT_TP  17A4<>
NEC_NC<1>          17B5<>
NEC_NC<2>          17B5<>
NEC_OCI<3>         17B5<
NEC_OCI<4>         17B5<
NEC_OCI<5>         17B5<
NEC_PCI_GNT_L      12C7<> 17B7<
NEC_PCI_INTA_L     17B7<>
NEC_PCI_INTB_L     17B7<>
NEC_PCI_INTC_L     17B7<>
NEC_PCI_INT_L      14B5<> 14D7< 17B8<
NEC_PCI_REQ_L      12A7< 12D7<> 17B7>
NEC_PME_L          17A7< 17A7<
NEC_PPON3_TP       17B5>
NEC_PPON4_TP       17B5>
NEC_PPON5_TP       17B5>
NEC_RREF           17B5<>
NEC_RUSB_OCI       17B3< 17B5<
NEC_RUSB_OCI_UF    17B1< 27D1<> 41D3>
NEC_RUSB_PPON      17B5> 27D1<> 41D3>
NEC_SMI_L_TP       17A7>
NEC_USB_DAM        17D2<> 27D7<> 39B2> 41D3>
NEC_USB_DAP        17D2<> 27D7<> 39B2> 41D3>
NEC_USB_DBM        17C2<> 27D2<> 39B2> 41D3>
NEC_USB_DBP        17C2<> 27D2<> 39B2> 41D3>
NEC_USB_RSDM1      17C5<>
NEC_USB_RSDM2      17C5<>
NEC_USB_RSDP1      17C5<>
NEC_USB_RSDP2      17C5<>
NEC_XT1            17D5<
NEC_XT2            17D5<>
NEC_XT2_R          17D4<
OVER_18V_ADJ       32C3<>
PCI1510_VR_EN_L    18C7<
PCI_AD<0>          9C3< 12D6<> 17D7<> 18C7<> 26B5<>
PCI_AD<31..0>      39C5> 41D3>
PCI_AD<1>          9C3< 12D6<> 17D7<> 18C7<> 26B6<>
PCI_AD<2>          9C3< 12D6<> 17D7<> 18C7<> 26C5<>
PCI_AD<3>          9C3< 12D6<> 17C7<> 18C7<> 26C6<>
PCI_AD<4>          9C3< 12D6<> 17C7<> 18C7<> 26C5<>
PCI_AD<5>          9C3< 12D6<> 17C7<> 18C7<> 26C6<>
PCI_AD<6>          9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<7>          9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<8>          9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<9>          9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<10>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<11>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<12>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<13>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<14>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<15>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<16>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<17>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<18>         9C3< 12C6<> 17C7<> 18B7<> 26C5<>
                 26D4<
PCI_AD<19>         9B3< 12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<20>         9B3< 12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<21>         12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<22>         12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<23>         12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<24>         9C1< 12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<25>         9C1< 12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<26>         9C1< 12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<27>         9C1< 12C6<> 17C8<> 18B7<> 26D6<>
PCI_AD<28>         9C1< 12C6<> 17C7<> 18B7<> 26C5<>
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PCI_AD<31>         9C1< 12C6<> 17B7<> 18B7<> 26D6<>
PCI_CBE<0>         12C7<> 17B7<> 18B7<> 26C5<>
PCI_CBE<3..0>      39C5>
PCI_CBE<1>         12C7<> 17B7<> 18B7<> 26C6<>
PCI_CBE<2>         12C7<> 17B7<> 18B7<> 26C6<>
PCI_CBE<3>         12C7<> 17B7<> 18B7<> 26C6<>
PCI_DEVSEL_L       12B7< 12C7<> 17B7<> 18A7<> 26C5<>
                 39C5> 41C3>
PCI_FRAME_L        12B7< 12C7<> 17B7<> 18B7<> 26C5<>
                 39C5> 41D3>
PCI_IRDY_L         12B7< 12C7<> 17B7<> 18B7<> 26C6<>
                 39C5> 41D3>
PCI_PAR            12C7<> 17B7<> 18B7<> 26C5<> 39C5>
                 41C3>
PCI_PERR_L         17B7<> 18B7<> 18D7<
PCI_SERR_L         17B7> 18B7> 18D7<
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PCI_STOP_L       12A7< 12C7<> 17B7<> 18B7<> 26C5<>
                 39C5> 41C3>
PCI_TRDY_L       12B7< 12C7<> 17B7<> 18A7<> 26C5<>
                 39C5> 41D3>
PLL_STOP_L        7C4<> 7C8<>
PMU_ACK_L        14C2< 31C4<>
PMU_AC_DET       31A5< 31B4<>
PMU_AC_IN        31B4<>
PMU_BATT0_DET_L  31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L   31A8<> 31B3< 31D2< 32A4<> 41A3>
PMU_BYTE         31B6< 31C7<
PMU_CHARGE_V     31C4<> 32B8<>
PMU_CHRG_BATT_B  31C4<> 32A8<>
PMU_CLK          14C2<> 31C4<>
PMU_CNVSS        31B6< 31C7<
PMU_CPU_HRESET_L  6A2< 6C3<> 31C4<> 41C1>
PMU_CUSTOM_RESET  31A7<> 31B8<
PMU_CUSTOM_RESET_L  31A8<>
PMU_EPM          31C4<> 31D2<
PMU_FROM_INT     14C2<> 31C4<>
PMU_I2C_CLK      31B4<> 31C2<
PMU_I2C_DATA     31B4<> 31C2<
PMU_INT_L        14B5<> 14B7< 31B6<>
PMU_INT_NMI      14B5<> 14B7< 31D4<>
PMU_KB_RESET_L   41C1>
PMU_LID_CLOSED_L  24A1< 24D6<> 31B2< 31C4<> 41D1>
PMU_NMI_BUTTON_L  31C2< 31C4<>
PMU_NMI_L        31C2< 31C4<>
PMU_OOPS         31B2< 31B4<>
PMU_PME_L        14A5<> 17A8< 26D5<> 31B2< 31C4<>
                 41C3>
PMU_POWERUP_OK   31B4<> 31D2<
PMU_POWER_UP_L   30C8<> 31C6<> 31D7< 34B8<
PMU_RFQ_L        14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  24A7> 31C4<> 31D2<
PMU_RESET_L      31B6< 31B7>
PMU_SELECT       31C6>
PMU_SLEEP_LED    24C7<> 24D6<> 41D1>
PMU_SLEEP_LED_L  24C8<> 31C4<>
PMU_SMB_CLK      31B4<> 31C2< 32A3<
PMU_SMB_DATA     31B4<> 31C2< 32A2<
PMU_TO_INT       14C2<> 31C4<>
POWER_UP         30D7<>
POWER_VALID      31B2< 31C4<>
PP3V3_MMM        25C8< 25D5<
PP3V3_MMM_PIC    25C1< 25D5<
PP3V3_SI_AVCC1   20C7< 20D7<
PP3V3_SI_AVCC2   20C5< 20D7<
PP3V3_SI_PVCC1   20C7<
PP3V3_SI_PVCC2   20C5<
PP3V3_SI_VCC1    20C7< 20D8<
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PWR_BUTTON_L     24A7< 24B3<>
RAM_ADDR<0>      9B4< 11B3<> 11B6<>
RAM_ADDR<12..0>  37A5>
RAM_ADDR<1>      9B4< 11B5<> 11B8<>
RAM_ADDR<2>      9B4< 11B3<> 11B6<>
RAM_ADDR<3>      9B4< 11B5<> 11B8<>
RAM_ADDR<4>      9B4< 11B3<> 11B6<>
RAM_ADDR<5>      9B4< 11B5<> 11B8<>
RAM_ADDR<6>      9B4< 11B3<> 11B6<>
RAM_ADDR<7>      9B4< 11B5<> 11B8<>
RAM_ADDR<8>      9B4< 11B3<> 11B6<>
RAM_ADDR<9>      9A4< 11B5<> 11B8<>
RAM_ADDR<10>     9A4< 11B5<> 11B8<>
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RAM_BA<1..0>     37A5>
RAM_BA<1>        9A4< 11B3<> 11B6<>
RAM_CAS_L        9A4< 11B3<> 11B6<> 37A5>
RAM_CKE<0>       9A4< 9C4< 11C6<>
RAM_CKE<3..0>    37A5>
RAM_CKE<1>       9A4< 9C4< 11C8<>
RAM_CKE<2>       9A4< 9C4< 11C3<>
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RAM_CS_L<3..0>   37A5>
RAM_CS_L<1>      9C4< 11B6<>
RAM_CS_L<2>      9C4< 11B5<>
RAM_CS_L<3>      9C4< 11B3<>
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RAM_DATA_A<7..0>  37D5>
RAM_DATA_A<1>    10C8<> 11D6<>
RAM_DATA_A<2>    10C8<> 11D4<>
RAM_DATA_A<3>    10B8<> 11D6<>
RAM_DATA_A<4>    10B8<> 11D8<>
RAM_DATA_A<5>    10B8<> 11D6<>
RAM_DATA_A<6>    10B8<> 11D4<>
RAM_DATA_A<7>    10B8<> 11D8<>
RAM_DATA_A<8>    10B8<> 11D3<>
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RAM_DATA_A<9>    10C7<> 11D8<>
RAM_DATA_A<10>   10C7<> 11D6<>
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RAM_DATA_A<23>   10B6<> 11C6<>
RAM_DATA_A<24>   10B6<> 11C8<>
RAM_DATA_A<31..24>  37C5>
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RAM_DATA_A<26>   10C5<> 11C8<>
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RAM_DATA_A<28>   10C5<> 11C6<>
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RAM_DATA_A<30>   10C5<> 11C6<>
RAM_DATA_A<31>   10C5<> 11C6<>
RAM_DATA_A<32>   10B4<> 11B8<>
RAM_DATA_A<39..32>  37B5>
RAM_DATA_A<33>   10C4<> 11B8<>
RAM_DATA_A<34>   10C4<> 11B8<>
RAM_DATA_A<35>   10C4<> 11B8<>
RAM_DATA_A<36>   10B4<> 11B6<>
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RAM_DATA_A<61>   10C1<> 11A6<>
RAM_DATA_A<62>   10C1<> 11A6<>
RAM_DATA_A<63>   10C1<> 11A6<>
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RAM_DATA_B<1>    10C8<> 11D5<>
RAM_DATA_B<2>    10C8<> 11D5<>
RAM_DATA_B<3>    10C8<> 11D5<>
RAM_DATA_B<4>    10C8<> 11D3<>
RAM_DATA_B<5>    10C8<> 11D3<>
RAM_DATA_B<6>    10C8<> 11D3<>
RAM_DATA_B<7>    10C8<> 11D3<>
RAM_DATA_B<8>    10C8<> 11D5<>
RAM_DATA_B<15..8>  37C5>
RAM_DATA_B<9>    10C8<> 11D5<>
RAM_DATA_B<10>   10C8<> 11D5<>
RAM_DATA_B<11>   10C8<> 11D5<>
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RAM_DATA_B<15>   10C8<> 11D3<>
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RAM_DATA_B<23..16>  37C5>
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RAM_DATA_B<19>   10C6<> 11C5<>
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RAM_DATA_B<21>   10C6<> 11C3<>
RAM_DATA_B<22>   10C6<> 11C3<>
RAM_DATA_B<23>   10C6<> 11C3<>
RAM_DATA_B<32>   10D4<> 11B5<>
RAM_DATA_B<25..24>  37C5>
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RAM_DQM_A<7>     10C1<> 11A6<> 37A5>
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RAM_DQM_B<7>     10C2<> 11A3<> 37A5>
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RAM_DQS_A<4>     10B4<> 11B8<> 37B5>
RAM_DQS_A<5>     10C3<> 11B8<> 37B5>
RAM_DQS_A<6>     10B2<> 11A6<> 37B5>
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RAM_DQS_B<2>     10C6<> 11C5<> 37C5>
RAM_DQS_B<3>     10C6<> 11C5<> 37C5>
RAM_DQS_B<4>     10C4<> 11B5<> 37B5>
RAM_DQS_B<5>     10C4<> 11B5<> 37B5>
RAM_DQS_B<6>     10C2<> 11A5<> 37B5>
RAM_DQS_B<7>     10C2<> 11A5<> 37A5>
RAM_RAS_L        9A4< 11B3<> 11B6<> 37A5>
RAM_WE_L         9A4< 11B5<> 11B8<> 37A5>
RESET_VREF       6C3<>
RF_DISABLE_L     26D6<> 41C3>
ROM_CS_L         9B3< 12A4< 41C3>
ROM_CS_TP_L      9C4< 26E6<>
ROM_OE_L         9B3< 12A4< 41C3>
ROM_OE_TP_L      9B3< 26C5<>
ROM_ONBOARD_CS_L  9B3< 41C3>
ROM_ONBOARD_CS_TP_L  9B3< 26C6<>
ROM_RW_L         9B3< 12A4< 41C3>
ROM_RW_TP_L      9B3< 26C6<>
ROM_WP_L         9B3<
SI_DUAL_MODE     20A8< 20D7<
SI_I2C_CLK       20B4< 20B7< 20D7< 21C5<>
SI_I2S_DATA      20B4<> 20B7<> 20D7< 21C5<>
SI_M_HTPLG       20B7<
SI_RESET_L       20B6< 21C7<>
SI_RESET_L_R     20B4< 20B7< 20D7<
SI_SECONDARY     20A8< 20D5<>
SI_S_HTPLG       20B4<
SI_TMDS_CLKN     20A7< 20C2< 38D1>
SI_TMDS_CLKP     20A7< 20C2< 38D1>
SI_TMDS_DN<0>    20A7< 20B2< 38D1>
SI_TMDS_DN<1>    20A7< 20B2< 38D1>
SI_TMDS_DN<2>    20A7< 20B2< 38D1>
SI_TMDS_DN<3>    20A4< 20B2< 38D1>
SI_TMDS_DN<4>    20A4< 20B2< 38D1>
SI_TMDS_DN<5>    20A2< 20A4< 38D1>
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SI_TMDS_DP<1>    20A7< 20B2< 38D1>
SI_TMDS_DP<2>    20A7< 20B2< 38D1>
SI_TMDS_DP<3>    20A4< 20B2< 38D1>
SI_TMDS_DP<4>    20A2< 20A4< 38D1>
SI_TMDS_DP<5>    20A2< 20A4< 38C1>
SI_VREF          20A6< 20A8<
SLAVE_SWING      20B4< 20D6<
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SLEEP_LED_I      24D3<
SLEEP_LED_L      24D4<
SLEEP_LED_SW_L   24D4<>
SLEEP_LED_UF     24D3<
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SLEEP_L_LS5      18D5< 21A7<> 28A8<> 34A5<> 35C7<>
                 36C8<
SLEEP_L_LS5_EN_L  34A6<>
SLEEP_L_LS5_INV  36A3< 36C2< 36C8<>
SLEEP_L_LS5_NET  34B3<> 36C8<>
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SLEEP_NET_INV    34A3<>
SND_AMP_MUTE     27C7<> 27D6<> 41A6>
SND_AMP_MUTE_CTRL  27B5<> 27D6<>
SND_AMP_MUTE_L   14B5<> 27D5<>
SND_HP_MUTE      27C5<>
SND_HP_MUTE_L    14C5<> 27C5<> 41A6>
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SND_HW_RESET_L   14A8< 14B5<> 27D7<> 41A6>
SND_LIN_SENSE_L  14B5<> 27C8<> 41A6>
SOFTMODEM_FC_RGDT  27D3<
SOFT_PWR_ON_L    23D1<> 24B1< 31A8<> 31C6<> 31D7<
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ST7_SLEEP_LED_H  24C5<> 24C6<> 24D6<> 41D1>
STOP_AGP_L       12D2< 12D4<>
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SYSCLK_CPU_UF    8A5<> 37D1>
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SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 37C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37C1>
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SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 37D1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 37D1>
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SYSTEM_CLK_EN    14A5< 14B6< 31C4<>
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SYS_BATT_ISNS1   31B4<> 31C3<
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THERM1_A_DP      27A7< 27A8< 39A2>
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THERM1_DP        27A5< 27A6< 27B5<> 27B6< 39A2>
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THERM1_M_DP      27B7< 27B8< 39A2>
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THERM2_A_DP      27A7< 27A8< 39A2>
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THERM2_DP        27A5< 27A6< 27B5<> 27B6< 39A2>
THERM2_M_DM      27B7< 27B8< 39A2>
THERM2_M_DP      27B7< 27B8< 39B5<>
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THERM_L_OC       27B1<> 31B4<>
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TMDS_CLKP        20C1< 20C1< 20D4< 23C8<> 39C2>
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TMDS_CONN_CLKP   23C6<> 23C7<> 38C1> 41C6>
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TMDS_CONN_DN<1>  23C4<> 23D5<> 38C1>
TMDS_CONN_DN<2>  23C4<> 23D5<> 38C1>
TMDS_CONN_DN<3>  23B3<> 23C5<> 38B1>
TMDS_CONN_DN<4>  23C1<> 23C5<> 38B1>
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TMDS_CONN_DP<0>  23D6<> 38C1>
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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6680 | REV. E

SCALE NONE | SHT 44 OF 46

*** Part Cross-Reference for the entire design ***

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J8	CON_2RTSM_125	24
J9	CON_F1ST_S2MT_SM	14
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J14	CON_F30RT_S2MT_SM	23
J15	CON_F10RT_S2MT_SM	27
J16	CON_3RTSM_125	33
J17	CON_M16ST_D_SMA	27
J18	CON_M4RT_S2MT_SM	27
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J20	CON_F9RT_1394B_S6MT_SMA	30
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J24	CON_F6RT_S4MT_TH1	30
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J27	CON_M4RT_S_SM	32
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U12	SN74AUC1G04	7
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U14	COMPARATOR_LMC7211	33
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