1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB

DVT Build - 12/02/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
12		412764	ENGINEERING RELEASE		12/03/05

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH	CRITICAL	
820-1881	1	PCBF,MULLET,M1	PCB	CRITICAL	PCB_THICK
920-0342	1	PCBF,MULLET_THIN,M1	PCB	CRITICAL	PCB_THIN

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Fri Dec 2 23:03:42 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 12

SHT 1 OF 104

System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	2	104

J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q8300
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q8305
PP5V_S0
5.0V
PM_SLP_S3_LS5V
IMVP_VR_ON
IMVP_PWRGD_IN
U7500
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
?V
VR_PWRGOOD_DELAY
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
PP1V8_S3
1.8V
NC
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
PPVCORE_S0_GPU
1.2V - 1.0V
NC
Q8310
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
PP2V5_S3
2.5V
NC
Q8320
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
NC
Q8330
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
Q8315
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q8325
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 3 OF 104	

"Better" BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7401	PCBA,MULLET_BTR,HY128,M1	075-0139,075-0140,075-0154,EEE_UNH
630-7403	PCBA,MULLET_BTR,SAM128,M1	075-0139,075-0140,075-0156,EEE_UNK

"Best" BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7429	PCBA,MULLET_BST,SAM128,M1	075-0139,075-0171,075-0156,EEE_UR8
630-7430	PCBA,MULLET_BST,HY128,M1	075-0139,075-0171,075-0154,EEE_UR9
630-7254	PCBA,MULLET_BST,SAM256,M1	075-0139,075-0171,075-0138,EEE_TYY
630-7402	PCBA,MULLET_BST,HY256,M1	075-0139,075-0171,075-0155,EEE_UNJ

Phantom BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
075-0139	PROJ_PTS,MULLET,M1	COMMON,M1_COMMON,M1_DEBUG,PROJ_PROTOEVTDVT
075-0140	LE_MENU,MULLET_BTR,M1	CPU_BTR,LEMENU_PROTOEVTDVT
075-0171	LE_MENU,MULLET_BST,M1	CPU_BST,LEMENU_PROTOEVTDVT
075-0156	128SAM,MULLET,M1	VRAM_128_SAMSUNG
075-0154	128HY,MULLET,M1	GPU_MEM_HYNIX,VRAM_128_HYNIX
075-0138	256SAM,MULLET,M1	GPU_MEM_256M,VRAM_256_SAMSUNG
075-0155	256HY,MULLET,M1	GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M1_COMMON	M1_COMMON1,M1_COMMON2,M1_COMMON3
M1_COMMON1	ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS,INVERTER_BUF
M1_COMMON2	KBDLED_HAS,LVDS_PD,MEMVREF_S3,MEMVTT_EN_PU,PCB_THICK
M1_COMMON3	RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU,USB_G_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0138	1	256SAM,B13,MULLET,M1	BOM3	CRITICAL	075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM1	CRITICAL	075-0139
075-0140	1	LE MENU,MULLET BTR,M1	BOM2	CRITICAL	075-0140
075-0154	1	128HY,MULLET,M1	BOM3	CRITICAL	075-0154
075-0155	1	256HY,MULLET,M1	BOM3	CRITICAL	075-0155
075-0156	1	128SAM,MULLET,M1	BOM3	CRITICAL	075-0156
075-0171	1	LE MENU,MULLET BST,M1	BOM2	CRITICAL	075-0171

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TYY]	CRITICAL	EEE_TYY	M1,BST,SAM256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNH]	CRITICAL	EEE_UNH	M1,BTR,HY128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNJ]	CRITICAL	EEE_UNJ	M1,BST,HY256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNK]	CRITICAL	EEE_UNK	M1,BTR,SAM128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UR8]	CRITICAL	EEE_UR8	M1,BST,SAM128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UR9]	CRITICAL	EEE_UR9	M1,BST,HY128

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX

"LeMenu Stage #1" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	LEMENU_STAGE1
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	LEMENU_STAGE1
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	LEMENU_STAGE1
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU_STAGE1
341S1812	1	IC,EFI,BOOTROM DEVELOPMENT,M1	U6301	CRITICAL	BOOTROM_DEVEL
341S1813	1	IC,EFI,BOOTROM FINAL,M1	U6301	CRITICAL	BOOTROM_FINAL
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	LEMENU_STAGE1
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	LEMENU_STAGE1

"LeMenu Stage #2" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	LEMENU_STAGE2

"LeMenu Stage #3" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3267	1	IC,M1 BTR,479 BGA	U0700	CRITICAL	CPU_BTR
337S3268	1	IC,M1 BST,479 BGA	U0700	CRITICAL	CPU_BST
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	LEMENU_STAGE3
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	LEMENU_STAGE3

LeMenu Stage Mappings

BOM GROUP	BOM OPTIONS
LEMENU_LOCALPROTO	BOOTROM_DEVEL,LEMENU_STAGE1,LEMENU_STAGE2,LEMENU_STAGE3
LEMENU_PROTOEVTDVT	LEMENU_STAGE2,LEMENU_STAGE3
PROJ_PROTOEVTDVT	BOOTROM_DEVEL,LEMENU_STAGE1
LEMENU_PVTRAMP	LEMENU_STAGE3
PROJ_PVTRAMP	BOOTROM_FINAL,LEMENU_STAGE1,LEMENU_STAGE2

The number of parts managed as Le Menu decreases as a project progresses.
The above stages and build settings are per 8/25 strategy statement.

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 12

SCALE NONE | SHT 4 OF 104

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	57
TRUE		IMVP6_COMP	57
TRUE		P5VS5_RUNSS	58 62
TRUE		P1V5S0_RUNSS	58 62
TRUE		P2V5S3_MODE	59
TRUE		P2V5S3_SHDNRT	59
TRUE		P1V2S3_RT	59
TRUE		P1V2S3_RUNSS	39 59
TRUE		P1V8S3_COMP	60
TRUE		P1V8S3_FSET	60
TRUE		P3V3S5_COMP	61
TRUE		P3V3S5_FSET	61
TRUE		P1V05S0_COMP	61
TRUE		P1V05S0_FSET	61
TRUE		P3V42G3H_FB	62
TRUE		GPUVCORE_COMP	66
TRUE		GPUVCORE_FSET	66
TRUE		GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 79
TRUE		FSB_ADS_L	7 12 79
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 79
TRUE		FSB_BNR_L	7 12 79
TRUE		FSB_BREQ0_L	7 12 79
TRUE		FSB_D_L<63..0>	7 12 79
TRUE		FSB_DBSY_L	7 12 79
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 79
TRUE		FSB_DRDY_L	7 12 79
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 79
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 79
TRUE		FSB_HIT_L	7 12 79
TRUE		FSB_HITM_L	7 12 79
TRUE		FSB_LOCK_L	7 12 79
TRUE		FSB_REQ_L<4..0>	7 12 79

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST		
	=PP5V_S0_FAN_LT	54 63
	FAN_LT_PWM	54
	FAN_LT_TACH	54
	FAN_RT_PWM	54
	FAN_RT_TACH	54

LPC+ Debug Connector

FUNC_TEST		
TRUE	=PP3V3_S5_LPCPLUS	49 63
TRUE	=PP5V_S0_LPCPLUS	49 63
TRUE	LPC_AD<0>	21 47 49 56
TRUE	LPC_AD<1>	21 47 49 56
TRUE	LPC_FRAME_L	21 47 49 56
TRUE	PM_CLKRUN_L	23 40 47 49 56
TRUE	BOOT_LPC_SPI_L	22 47 49
TRUE	SMC_TMS	47 48 49
TRUE	DEBUG_RST_L	26 49
TRUE	SMC_TRST_L	47 49
TRUE	SMC_TDO	47 48 49
TRUE	SMC_MD1	47 49
TRUE	SMC_TX_L	47 48 49
TRUE	FWH_INIT_L	21 48 49
TRUE	PCI_CLK_PORT80_LPC	34 49
TRUE	LPC_AD<2>	21 47 49 56
TRUE	LPC_AD<3>	21 47 49 56
TRUE	INT_SERIRQ	23 47 49 56
TRUE	PM_SUS_STAT_L	23 47 48 49 56
TRUE	SMC_TDI	47 48 49
TRUE	SMC_TCK	47 48 49
TRUE	SMC_RST_L	47 48 49
TRUE	SMC_NMI	47 49
TRUE	SMC_RX_L	47 48 49
TRUE	SV_SET_UP	23 49

Left ALS Connector

FUNC_TEST		
TRUE	=PP3V3_S3_LTALS	63 76
TRUE	ALS_GAIN	6 47 76
TRUE	LTALS_OUT	53 76
TRUE	GND\g	

Camera Connector

FUNC_TEST		
TRUE	=PP5V_S3_CAMERA	43 63
TRUE	=USB2_CAMERA_N	6 43
TRUE	=USB2_CAMERA_P	6 43
TRUE	=SMBUS_ATS_SDA	27 43
TRUE	=SMBUS_ATS_SCL	27 43
TRUE	GND\g	

Thermal Diode Connectors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	50
TRUE	HSTHMSNS_DX_N	50
TRUE	RSFSTHMSNS_D_P	50
TRUE	RSFSTHMSNS_D_N	50

Other Func Test Points

FUNC_TEST		
TRUE	=PP1V05_S0_REG	51 61 63
TRUE	PM_SYSRST_L	23 26 47
TRUE	SMC_ONOFF_L	43 47 48 51

Current Sense Calibration

FUNC_TEST		
TRUE	ISENSE_CAL_EN	
TRUE	=PP5V_S0_ISENSECAL	
TRUE	PP1V8_S3_REG	63
TRUE	PP1V5_S0_REG	63
TRUE	PPVCORE_S0_GPU	63
TRUE	PPVCORE_S0_CPU	63
TRUE	GND\g	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST		
TRUE	SMC_BS_ALRT_L	47 48 64
TRUE	=SMBUS_BATT_SCL	27 64
TRUE	=SMBUS_BATT_SDA	27 64
TRUE	GND_BATT	64

Left I/O Data Connector

FUNC_TEST		
TRUE	=PP1V5_S0_LIO	45 63
TRUE	=PPDCIN_G3H_LIO	45 63
TRUE	=PP5V_S5_LIO	45 63
TRUE	=PP3V42_G3H_LIO	45 63
TRUE	PP5V_S0_AUDIO_PWR	45
TRUE	PP5V_S0_AUDIO	45
TRUE	GND_AUDIO_PWR	45
TRUE	GND_AUDIO	45
TRUE	ACZ_SDATAIN<0>	21 45 79
TRUE	ACZ_SDATAOUT	21 45 79
TRUE	ACZ_BITCLK	21 45 79
TRUE	ACZ_RST_L	21 45 79
TRUE	EXCARD_OC_L	6 45 48
TRUE	LTUSB_OC_L	6 45
TRUE	LIO_BATT_ISENSE	45 51
TRUE	SMC_SYS_ISET	45 47
TRUE	SMC_BATT_ISET	45 47
TRUE	SMC_BATT_CHG_EN	45 47 48
TRUE	SMC_BC_ACOK	45 47 48
TRUE	SMC_ADAPTER_EN	41 45 47 48
TRUE	LIO_P3V3S0_EN_L	45 62
TRUE	LIO_DCIN_ISENSE	45 51
TRUE	LIO_P3V3S3_EN	45 62
TRUE	SMC_BATT_TRICKLE_EN_L	45 47 48
TRUE	SYS_ONEWIRE	45 47 48
TRUE	MINI_CLKREQ_L	34 45
TRUE	SMC_EXCARD_CP	45 47 48
TRUE	EXCARD_CLKREQ_L	34 45
TRUE	SMC_EXCARD_PWR_EN	45 47
TRUE	LIO_PLT_RESET_L	26 45
TRUE	ACZ_SYNC	21 45 79
TRUE	=USB2_LT_N	6 45
TRUE	=USB2_LT_P	6 45
TRUE	=USB2_EXCARD_N	6 45
TRUE	=USB2_EXCARD_P	6 45
TRUE	=PCIE_EXCARD_R2D_N	45 46
TRUE	=PCIE_EXCARD_R2D_P	45 46
TRUE	=PCIE_EXCARD_D2R_N	45 46
TRUE	=PCIE_EXCARD_D2R_P	45 46
TRUE	PCIE_CLK100M_EXCARD_P	34 45
TRUE	PCIE_CLK100M_EXCARD_N	34 45
TRUE	=PCIE_MINI_R2D_N	45 46
TRUE	=PCIE_MINI_R2D_P	45 46
TRUE	=PCIE_MINI_D2R_N	45 46
TRUE	=PCIE_MINI_D2R_P	45 46
TRUE	PCIE_CLK100M_MINI_P	34 45
TRUE	PCIE_CLK100M_MINI_N	34 45
TRUE	=SMBUS_LIO_SMC_SCL	27 45
TRUE	=SMBUS_LIO_SMC_SDA	27 45
TRUE	=SMBUS_LIO_SB_SCL	27 45
TRUE	=SMBUS_LIO_SB_SDA	27 45
TRUE	PCIE_WAKE_L	23 37 45

Left I/O Power Connector

FUNC_TEST		
TRUE	=PPBUS_G3H_LIO_CONN	63 64
TRUE	GND\g	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	5	104

NC_CPU_A32_L = TP_CPU_A32_L (7)
NC_CPU_A33_L = TP_CPU_A33_L (7)
NC_CPU_A34_L = TP_CPU_A34_L (7)
NC_CPU_A35_L = TP_CPU_A35_L (7)
NC_CPU_A36_L = TP_CPU_A36_L (7)
NC_CPU_A37_L = TP_CPU_A37_L (7)
NC_CPU_A38_L = TP_CPU_A38_L (7)
NC_CPU_A39_L = TP_CPU_A39_L (7)
NC_CPU_APM0_L = TP_CPU_APM0_L (7)
NC_CPU_APM1_L = TP_CPU_APM1_L (7)
NC_CPU_EXTBREF = TP_CPU_EXTBREF (7)
NC_CPU_HFPLL = TP_CPU_HFPLL (7)
NC_CPU_SPARE0 = TP_CPU_SPARE0 (7)
NC_CPU_SPARE1 = TP_CPU_SPARE1 (7)
NC_CPU_SPARE2 = TP_CPU_SPARE2 (7)
NC_CPU_SPARE4 = TP_CPU_SPARE4 (7)

NC_MEM_A_A<15..14> = MEM_A_A<15..14> (28)
NC_MEM_B_A<15..14> = MEM_B_A<15..14> (29)
TP_NB_CFG<4..3> = NB_CFG<4..3> (14)
TP_NB_CFG<6> = NB_CFG<6> (14)
TP_NB_CFG<8> = NB_CFG<8> (14)
TP_NB_CFG<11..10> = NB_CFG<11..10> (14)
TP_NB_CFG<15..14> = NB_CFG<15..14> (14)
TP_NB_CFG<17> = NB_CFG<17> (14)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> = NB_CFG<13..12> (14)

TP_SB_SUS_CLK = SUS_CLK_SB (23)

NC_SB_XOR_T5 = TP_SB_XOR_T5 (21)
NC_SB_XOR_U5 = TP_SB_XOR_U5 (21)
NC_SB_XOR_V3 = TP_SB_XOR_V3 (21)
NC_SB_XOR_V4 = TP_SB_XOR_V4 (21)
NC_SB_XOR_W3 = TP_SB_XOR_W3 (21)

TP_SMC_RSTGATE_L = SMC_RSTGATE_L (47)
ALS_GAIN (76 47 5) = =RTALS_GAIN (53)

NC_ENET_CTRL12 = ENET_CTRL12 (37)
NC_ENET_CTRL25 = ENET_CTRL25 (37)

Ethernet Power Management Support

ENET_LOM_DISABLE
R0600
0
5%
1/16W
MF-LF
402

SB_GPIO30 (22, IN) — 1 — 2 — ENET_LOM_DIS_L (OUT 37)

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (44) = USB2_RT_P = USB_A_P (22)
=USB2_RT_N (44) = USB2_RT_N = USB_A_N (22)
=RTUSB_OC_L (44) = RTUSB_OC_L = USB_A_OC_L (22)

USB Port "B" = Trackpad (Geyser)

=USB_TRACKPAD_P (43) = USB_TRACKPAD_P = USB_B_P (22)
=USB_TRACKPAD_N (43) = USB_TRACKPAD_N = USB_B_N (22)
UNUSED_USB_B_OC_L = USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (45 5) = USB2_LT_P = USB_C_P (22)
=USB2_LT_N (45 5) = USB2_LT_N = USB_C_N (22)
LTUSB_OC_L = USB_C_OC_L (22)

USB Port "D" = Camera

=USB2_CAMERA_P (43 5) = USB2_CAMERA_P = USB_D_P (22)
=USB2_CAMERA_N (43 5) = USB2_CAMERA_N = USB_D_N (22)
UNUSED_USB_D_OC_L = USB_D_OC_L (22)

USB Port "E" = ExpressCard

=USB2_EXCARD_P (45 5) = USB2_EXCARD_P = USB_E_P (22)
=USB2_EXCARD_N (45 5) = USB2_EXCARD_N = USB_E_N (22)
EXCARD_OC_L (48 45 5) = USB_E_OC_L (22)

USB Port "F" = IR Receiver

=USB_IR_P (76) = USB_IR_P = USB_F_P (22)
=USB_IR_N (76) = USB_IR_N = USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

=USB_BT_P (76) = USB_BT_P = USB_G_P (22)
=USB_BT_N (76) = USB_BT_N = USB_G_N (22)

USB Port "H" = Reserved (PCI-E Mini Card)

TP_USB2_HP = USB_H_P (22)
TP_USB2_HN = USB_H_N (22)

Trace deleted to make room for other diffpairs over RAM connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1
GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI2 (75)
=GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1
GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI1 (75)
=GND_CHASSIS_DVI3 (75)
=GND_CHASSIS_DVI5 (75)
=GND_CHASSIS_ENET (38)
=GND_CHASSIS_FW_EMI (42)
=GND_CHASSIS_FW_PORT1 (42)
=GND_CHASSIS_RTUSB (44)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1
GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_LCD1 (74)
=GND_CHASSIS_LCD2 (74)
=GND_CHASSIS_LCD3 (74)
=GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1
2
3
GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_INVERTER (74)

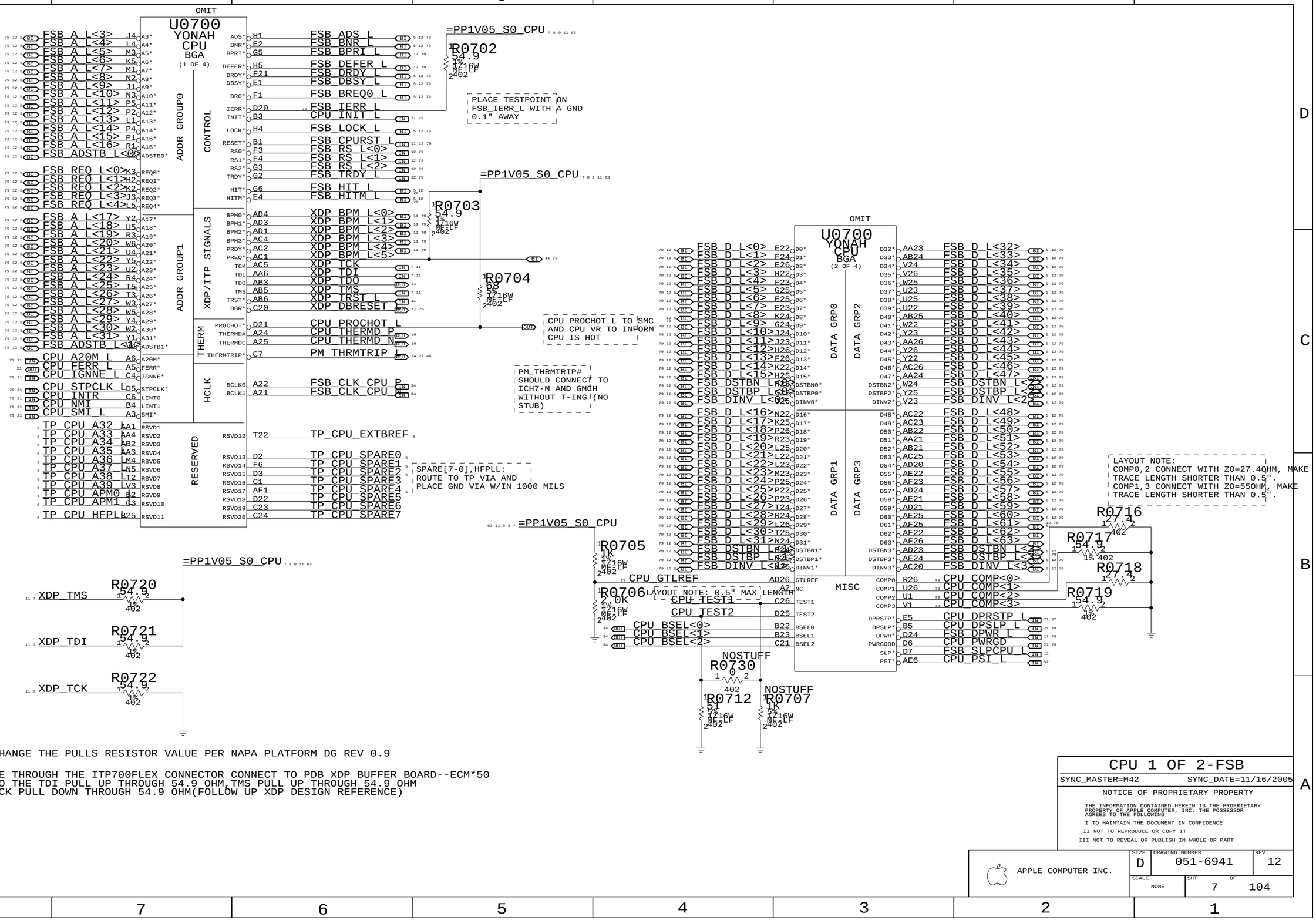
Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 12

SCALE NONE | SHT 6 OF 104



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

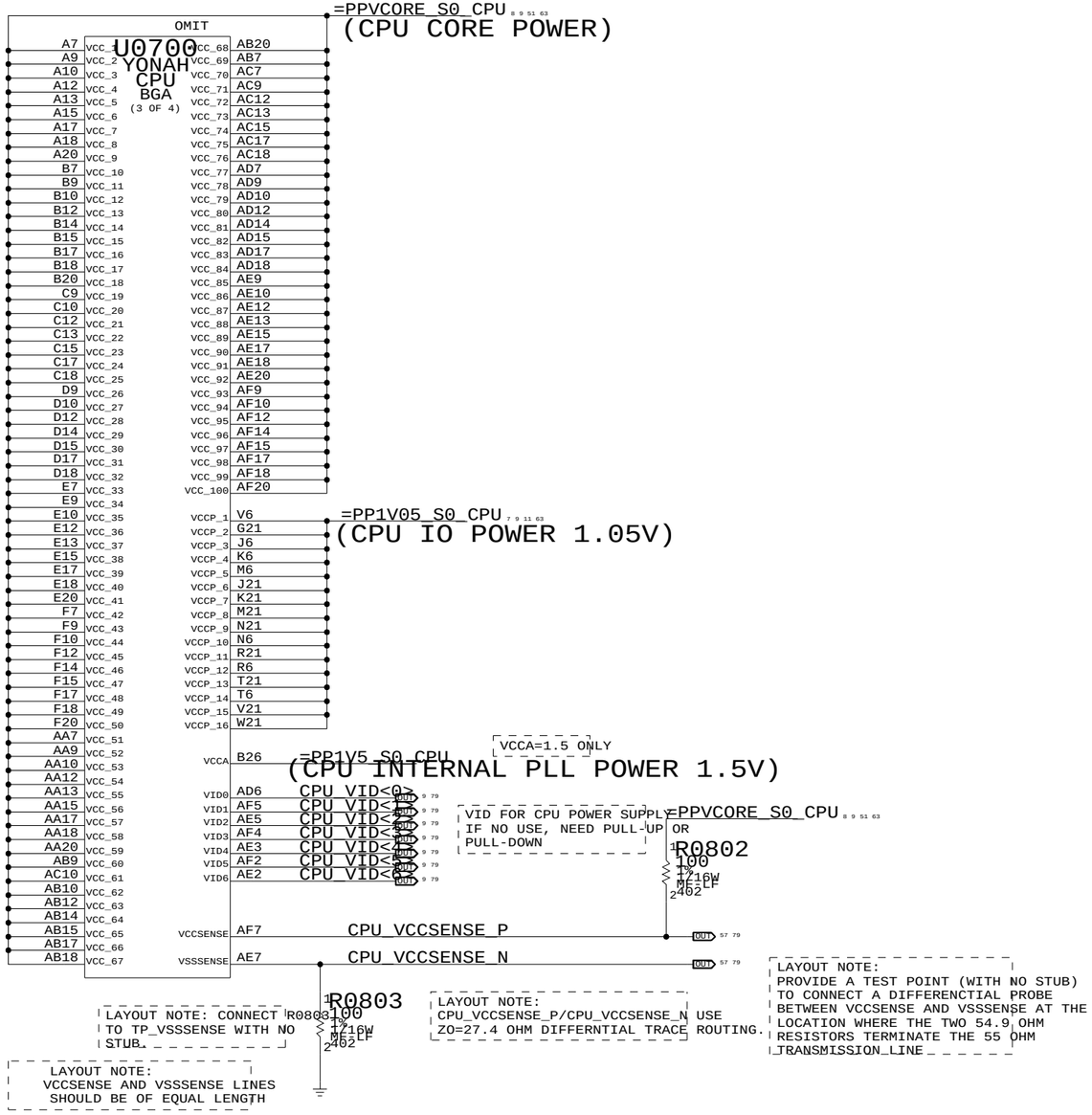
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

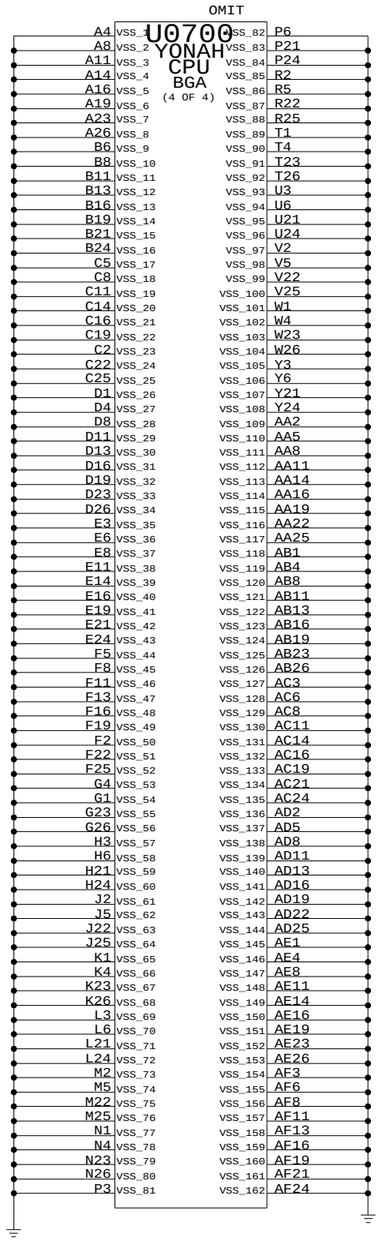
CPU 1 OF 2-FSB

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 7 OF 104	





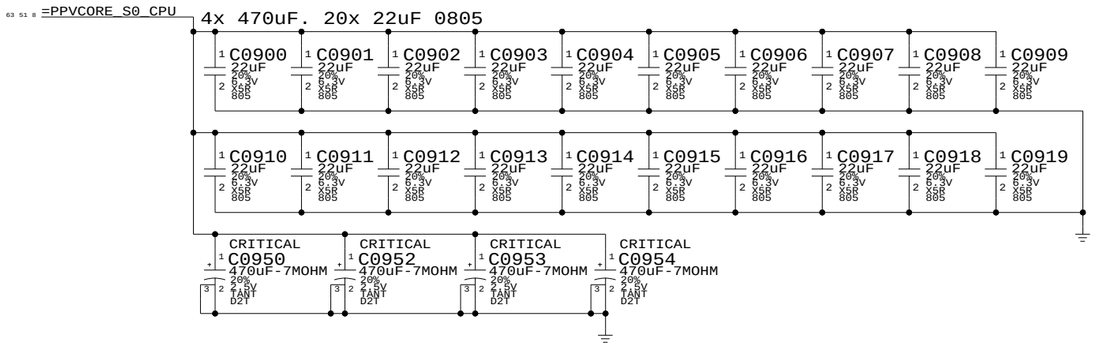
CPU 2 OF 2-PWR/GND

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

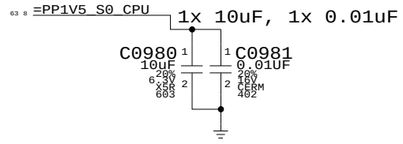
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT: 8 OF: 104	

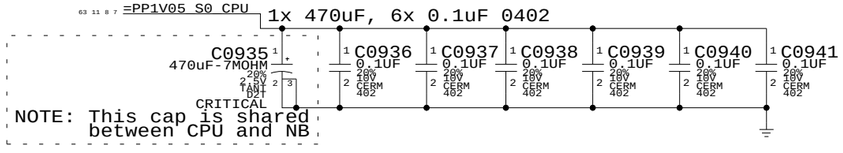
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

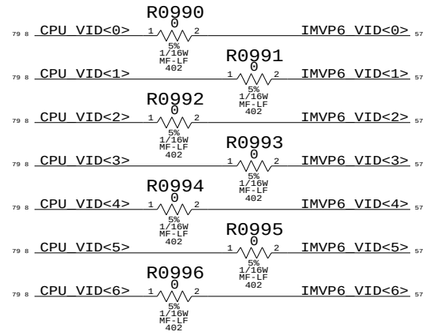


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



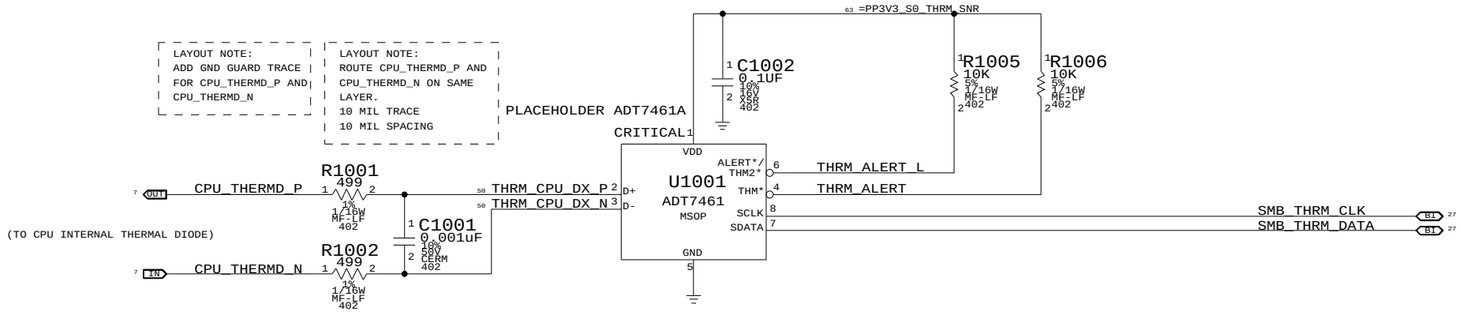
CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT: 9 OF: 104	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

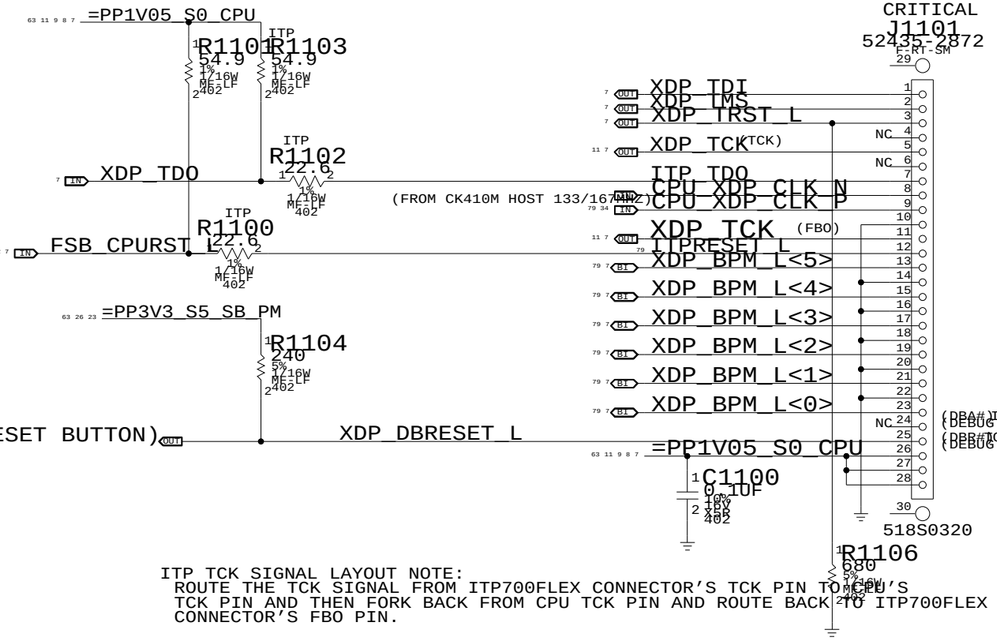
SYNC_MASTER=M42 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	10	104

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

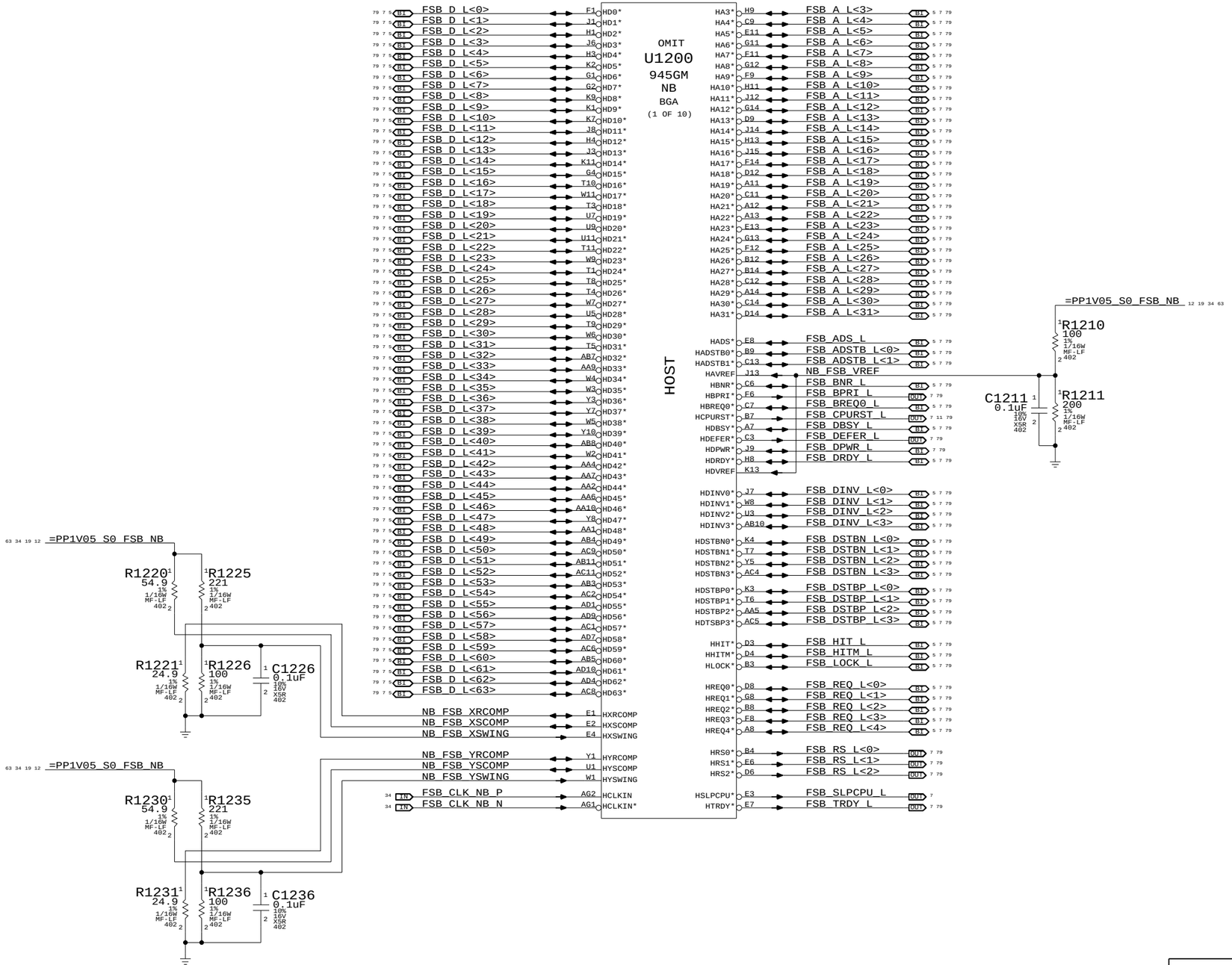
CPU ITP700FLEX DEBUG

SYNC_MASTER=MSX SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	11	104



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	12	104

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

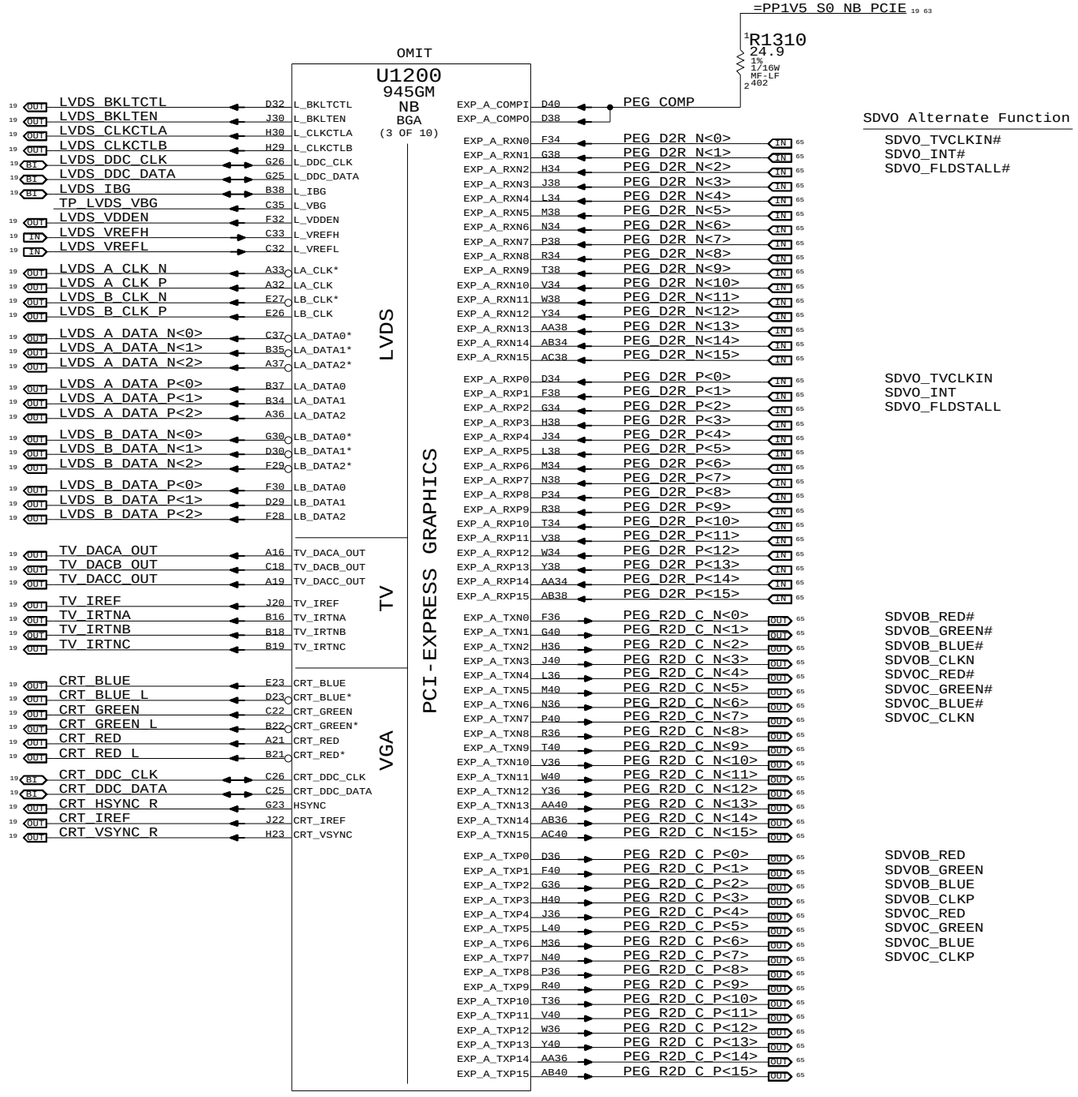
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



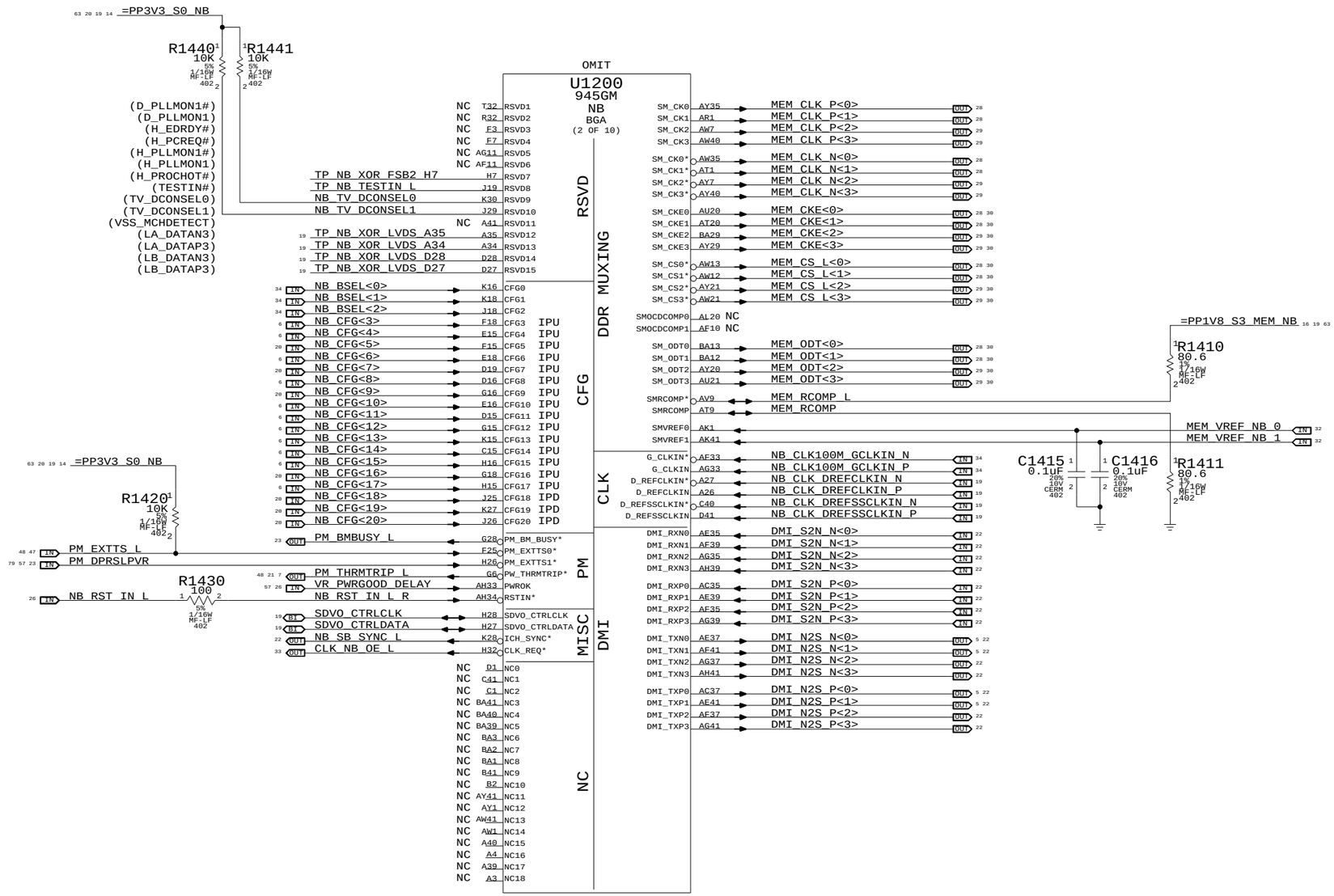
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	13	104



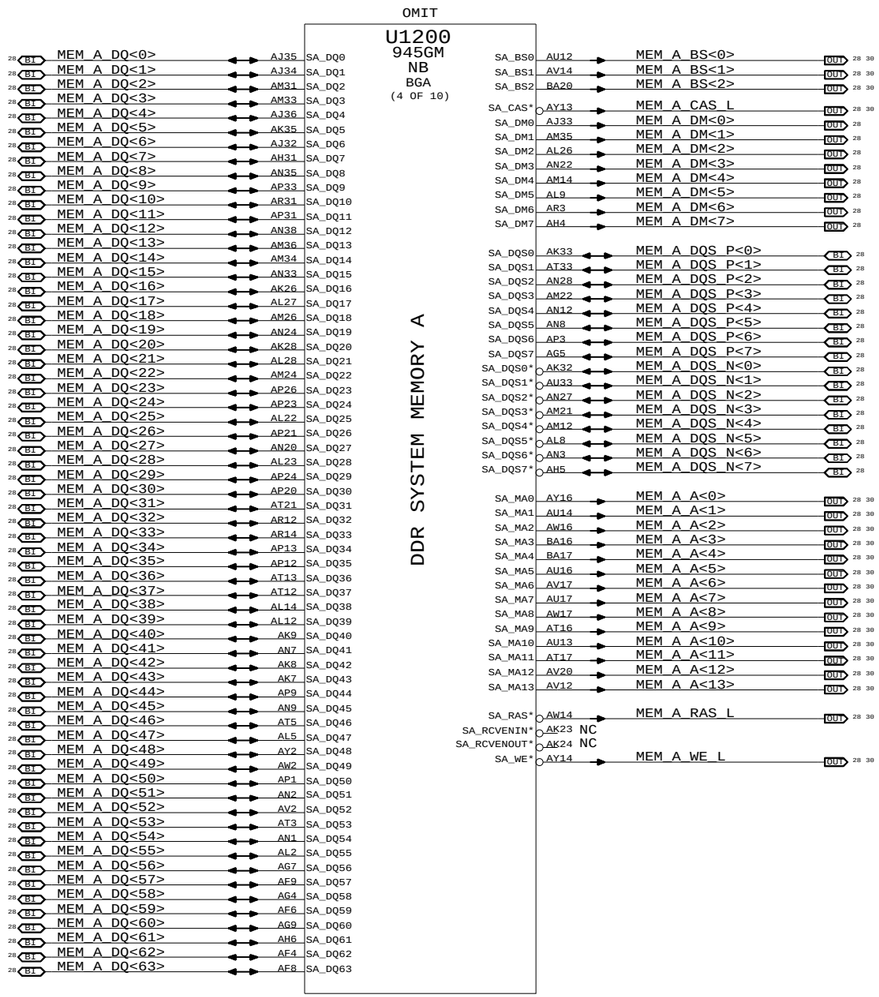
NB Misc Interfaces

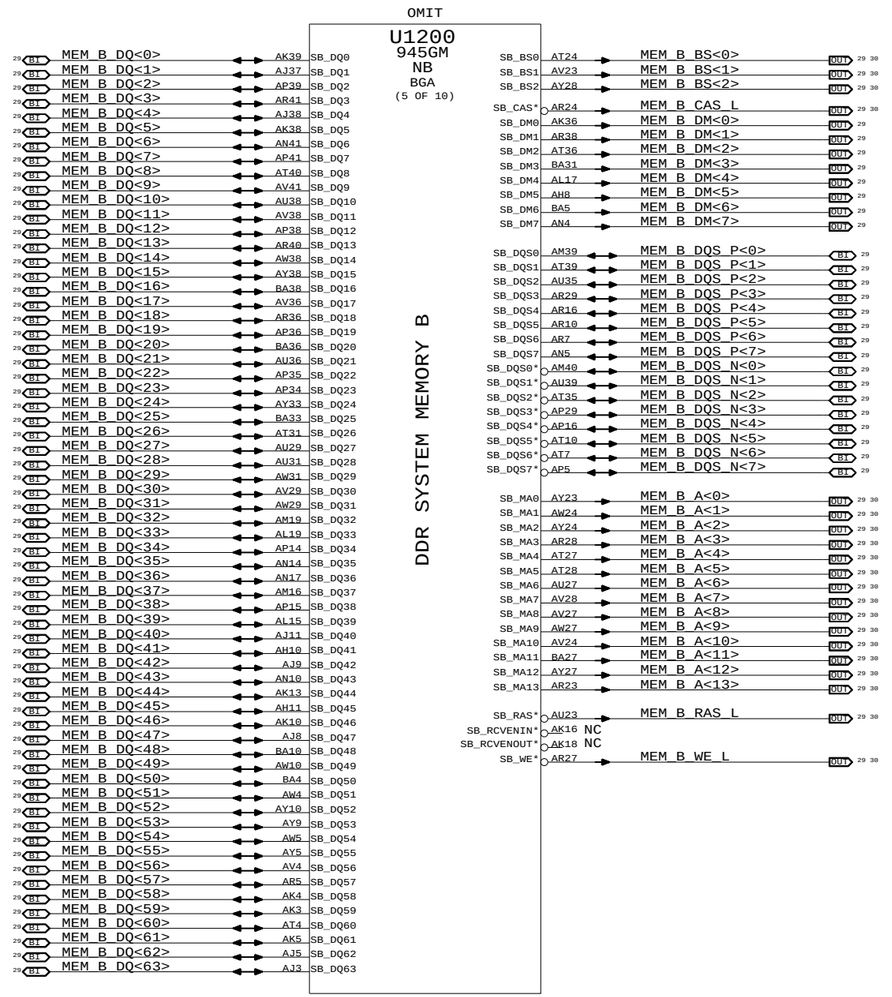
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	14	104





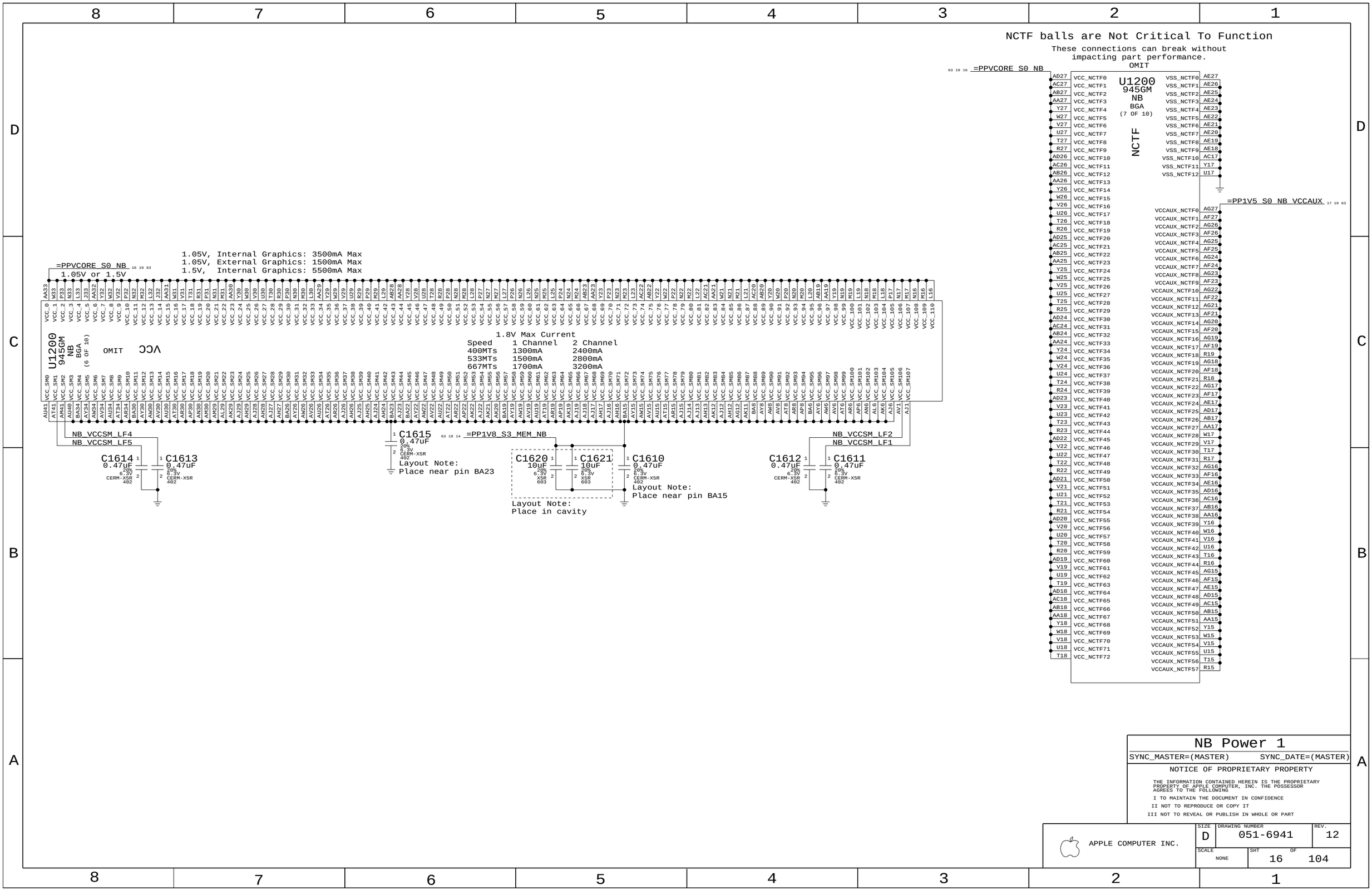
NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	15	104



NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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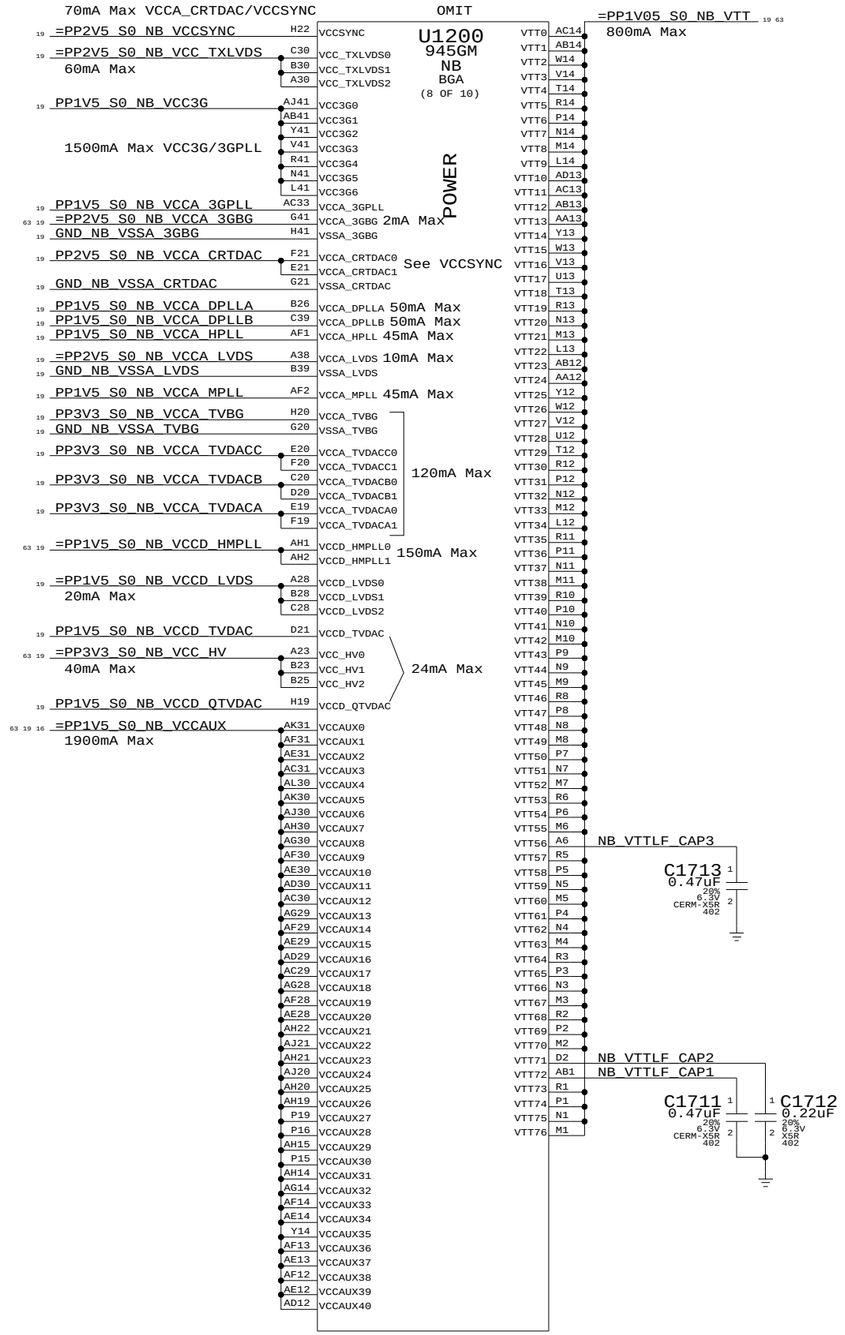
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	16	104



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	17	104

OMIT

U1200
945GM
NB
BGA
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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	18	104

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	1500mA Max
	=PP1V05_S0_FSB_NB	10mA Max?
	=PP1V05_S0_NB_VTT	800mA Max
	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	=PP1V5_S0_NB	?mA Max
	=PP1V5_S0_NB_3G	1500mA Max
	=PP1V5_S0_NB_3GPLL	
	=PP1V5_S0_NB_PCIE	?mA Max
	=PP1V5_S0_NB_PLL	100mA Max
	=PP1V5_S0_NB_TVDAC	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
	=PP3V3_S0_NB	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	40mA Max

=PP1V05_S0_NB_CRT
- CRT_RED
- CRT_GREEN
- CRT_BLUE
- CRT_RED_L
- CRT_GREEN_L
- CRT_BLUE_L
- CRT_IREF
- CRT_HSYNC_R
- CRT_VSYNC_R

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA

=PP1V5_S0_NB_TVDAC
- TV_DACA_OUT
- TV_DACB_OUT
- TV_DACC_OUT
- TV_IREF
- TV_IRTNA
- TV_IRTNB
- TV_IRTNC

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0>
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0>
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0>
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0>
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA

(MCH LVDS DATA/CLK TX 2.5V PWR)
=PP2V5_S0_NB_VCC_TXLVDS

(MCH LVDS DIGITAL 1.5V PWR)
=PP1V5_S0_NB_VCCD_LVDS

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS

=PPVCORE_S0_NB
- PP2V5_S0_NB_VCCA_CRTDAC (MCH CRTDAC ANALOG 2.5V PWR)
- GND_NB_VSSA_CRTDAC

(MCH H/V SYNC 2.5V PWR)
=PP2V5_S0_NB_VCCSYNC

=PP1V5_S0_NB_TVDAC
- PP1V5_S0_NB_VCCD_TVDAC (MCH TVDAC DEDICATED PWR 1.5V)

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC

(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA

(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB

(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC

(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG

GND_NB_VSSA_TVBG

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA

(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB

- NB_CLK_DREFCLKIN_P
- NB_CLK_DREFCLKIN_N
- NB_CLK_DREFSSCLKIN_P
- NB_CLK_DREFSSCLKIN_N

=PPVCORE_S0_NB, 1500mA Max — GMCH CORE PWR 1.05V BYPASS

CRITICAL
C1900 470uF-7MOHM 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

=PP1V05_S0_NB_VTT, 800mA Max — MCH VTT BYPASS (MCH FSB 1.05V PWR)

C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity

(SHARE C0940 470UF)
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

=PP3V3_S0_NB_VCC_HV, 40mA Max — MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG, 2mA Max — MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX, 1900mA Max — GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

C1918 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_PLL, 100mA Max — GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)

L1934 FERR-120-OHM-0.2A 0603
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_HPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) 45mA Max

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

L1936 FERR-120-OHM-0.2A 0603
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_MPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) 45mA Max

1500mA Max

=PP1V5_S0_NB_3G, 1500mA Max — L1970 91nH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY SMB2
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V)

=PP1V5_S0_NB_3GPLL, 1500mA Max — L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V)
R1975 0.51 1% 1/16W MF-LF 402
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
Layout Note: 3GPLL 10uF cap should be placed in cavity
GND_NB_VSSA_3GBG
Layout Note: Route to caps, then GND

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V)

1500mA Max

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 19 OF 104	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075 2.2K 5% 1/16W MF-LF 402 2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 63
NBCFG_VCC_1V5
1 R2058 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 63
NBCFG_DMI_REVERSE
1 R2059 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 63
NBCFG_SDVO_AND_PCIE
1 R2060 2.2K 5% 1/16W MF-LF 402 2

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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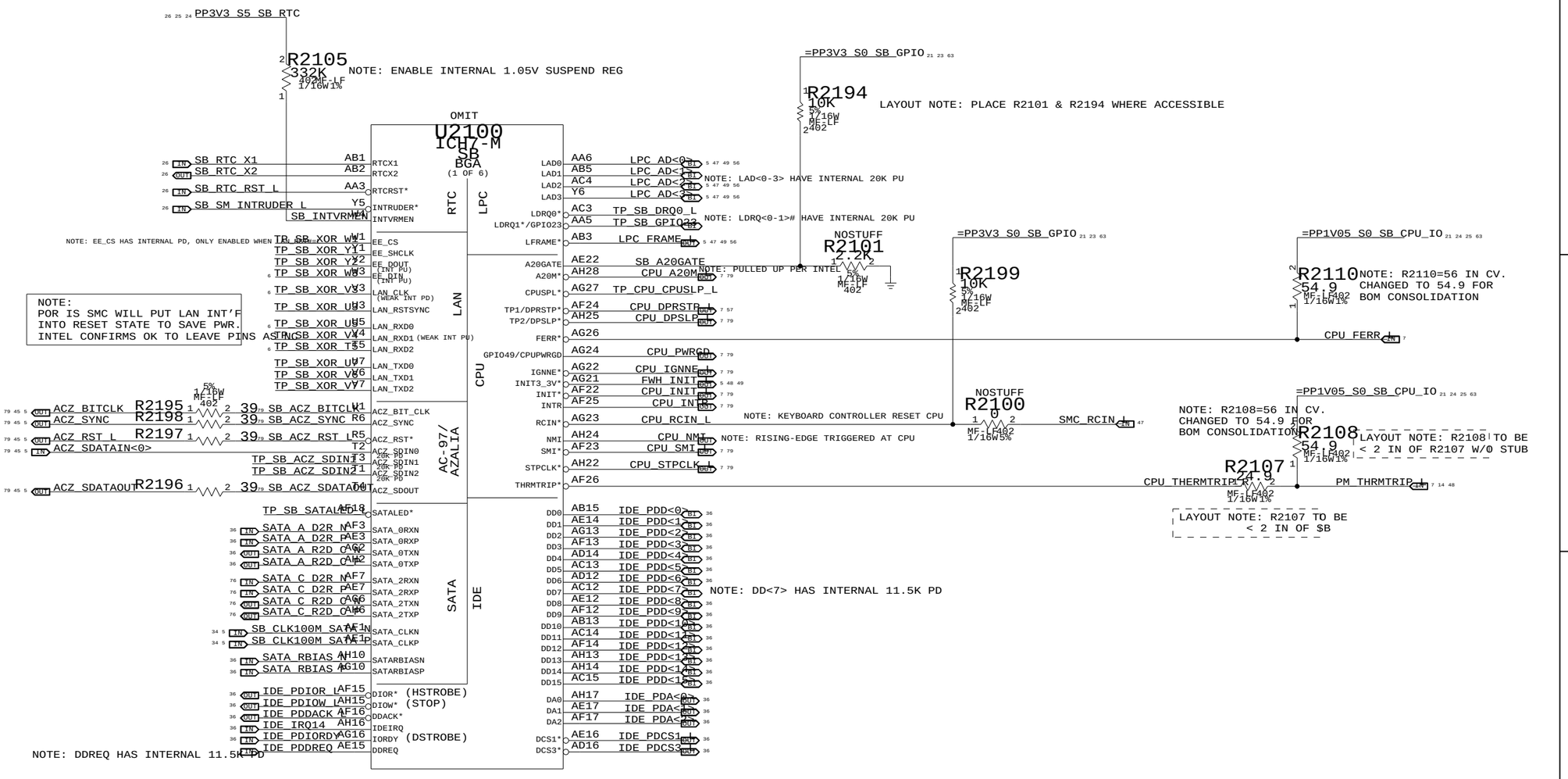
SIZE D | DRAWING NUMBER 051-6941 | REV. 12

SCALE NONE | SHT 20 OF 104



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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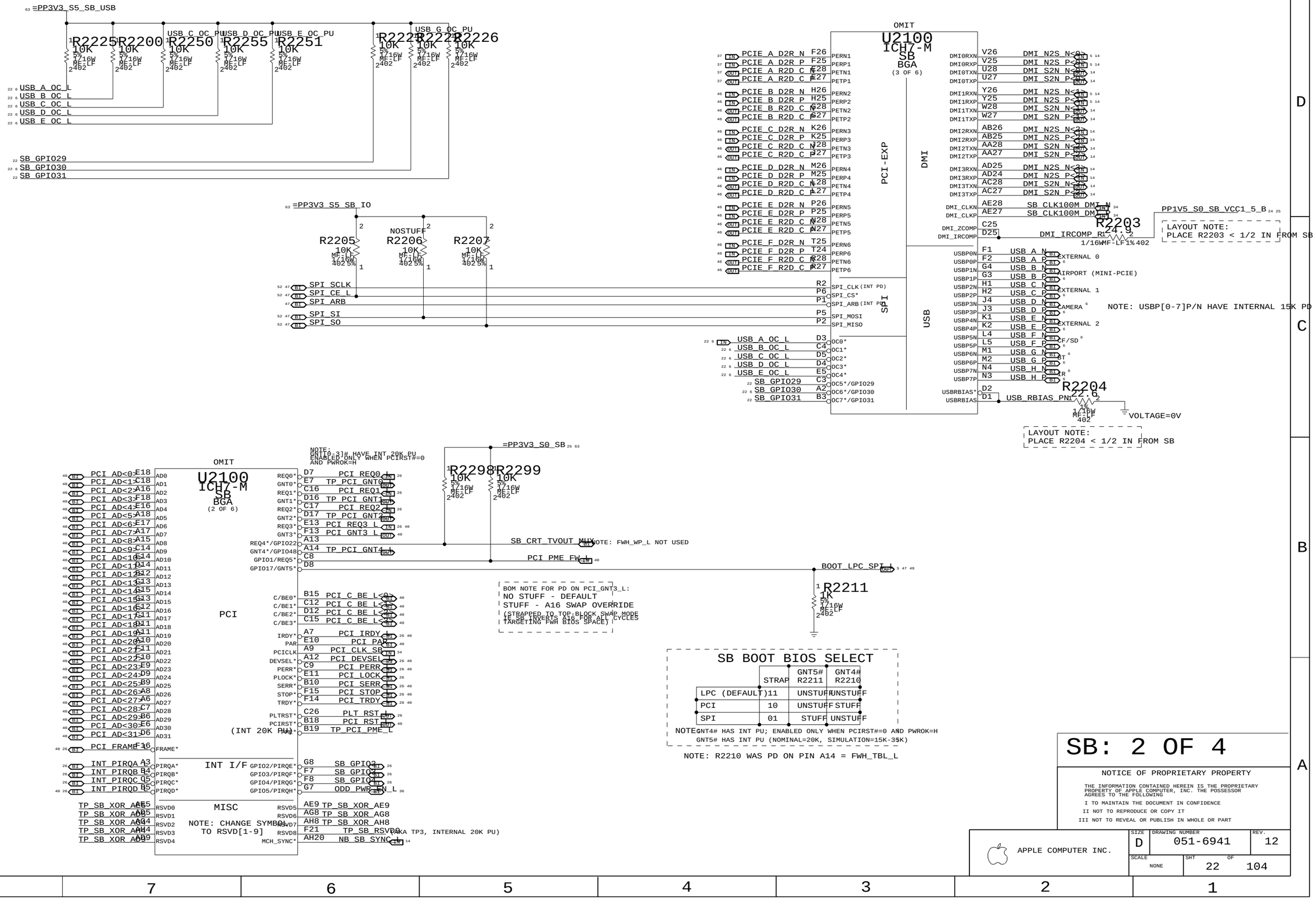
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT: 21 OF: 104	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2227 10K 5% 1/16W MF-LF 402
R2228 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
USB_G_OC_PU
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K 1/16W MF-LF 402 5%
NOSTUFF
R2206 10K 1/16W MF-LF 402 5%
R2207 10K 1/16W MF-LF 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N G28
PCIE_A_R2D_C_P G27
PCIE_B_D2R_N H26
PCIE_B_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_C_D2R_N K26
PCIE_C_D2R_P K25
PCIE_C_R2D_C_N K28
PCIE_C_R2D_C_P K27
PCIE_D_D2R_N M26
PCIE_D_D2R_P M25
PCIE_D_R2D_C_N L28
PCIE_D_R2D_C_P L27
PCIE_E_D2R_N P26
PCIE_E_D2R_P P25
PCIE_E_R2D_C_N N28
PCIE_E_R2D_C_P N27
PCIE_F_D2R_N T25
PCIE_F_D2R_P T24
PCIE_F_R2D_C_N R28
PCIE_F_R2D_C_P R27
PCI-EXP
SPI_CLK (INT PD) R2
SPI_CS* P6
SPI_ARB (INT PU) P1
SPI_MOSI P5
SPI_MISO P2
SPI
USB_A_OC_L D3
USB_B_OC_L C4
USB_C_OC_L D5
USB_D_OC_L D4
USB_E_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
SB_GPIO31 B3
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
DMI
DMI0RXN V26
DMI0RXP V25
DMI0TXN U28
DMI0TXP U27
DMI1RXN Y26
DMI1RXP Y25
DMI1TXN W28
DMI1TXP W27
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA28
DMI2TXP AA27
DMI3RXN AD25
DMI3RXP AD24
DMI3TXN AC28
DMI3TXP AC27
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_CLKN AE28
DMI_CLKP AE27
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_ZCOMP C25
DMI_IRCOMP D25
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N F1
USBP0P F2
USBP1N G4
USBP1P G3
USBP2N H1
USBP2P H2
USBP3N J4
USBP3P J3
USBP4N K1
USBP4P K2
USBP5N L4
USBP5P L5
USBP6N M1
USBP6P M2
USBP7N N4
USBP7P N3
USB_A_N
USB_A_P
USB_B_N
USB_B_P
USB_C_N
USB_C_P
USB_D_N
USB_D_P
USB_E_N
USB_E_P
USB_F_N
USB_F_P
USB_G_N
USB_G_P
USB_H_N
USB_H_P
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
USBRBIAS* D2
USBRBIAS D1
USB_RBIAS_PN
R2204 22.6 1/16W MF-LF 1% 402
VOLTAGE=0V
LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB
NOTE: CHANGE SYMBOL TO RSVD[1-9]
PCI_AD<0> E18
PCI_AD<1> C18
PCI_AD<2> A16
PCI_AD<3> F18
PCI_AD<4> E16
PCI_AD<5> A18
PCI_AD<6> E17
PCI_AD<7> A17
PCI_AD<8> A15
PCI_AD<9> C14
PCI_AD<10> E14
PCI_AD<11> D14
PCI_AD<12> B12
PCI_AD<13> C13
PCI_AD<14> A13
PCI_AD<15> C12
PCI_AD<16> E12
PCI_AD<17> C11
PCI_AD<18> D11
PCI_AD<19> A11
PCI_AD<20> A10
PCI_AD<21> F11
PCI_AD<22> F10
PCI_AD<23> E9
PCI_AD<24> D9
PCI_AD<25> B9
PCI_AD<26> A8
PCI_AD<27> A6
PCI_AD<28> C7
PCI_AD<29> B6
PCI_AD<30> E6
PCI_AD<31> D6
PCI_FRAME_L F16
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
FRAME*
PCI
INT_PIRQA_L A3
INT_PIRQB_L B4
INT_PIRQC_L C5
INT_PIRQD_L B5
PIRQA*
PIRQB*
PIRQC*
PIRQD*
INT I/F
TP_SB_XOR_AE5 AE5
TP_SB_XOR_AB5 AB5
TP_SB_XOR_AG4 AG4
TP_SB_XOR_AH4 AH4
TP_SB_XOR_AD9 AD9
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
MISC
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
NOTE: GNT1:3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 TP_PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 PCI_GNT3_L
REQ4*/GPIO22 A13
GNT4*/GPIO48 A14 TP_PCI_GNT4_L
GPIO1/REQ5* C8
GPIO17/GNT5* D8
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL
PERR* C9 PCI_PERR
PLOCK* E11 PCI_LOCK
SERR* B10 PCI_SERR
STOP* F15 PCI_STOP
TRDY* F14 PCI_TRDY
PLTRST* C26 PLT_RST
PCIRST* B18 PCI_RST
(INT 20K PU) PME* B19 TP_PCI_PME_L
GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 ODD_PWR_EN_L
RSVD5 AE9 TP_SB_XOR_AE9
RSVD6 AG8 TP_SB_XOR_AG8
RSVD7 AH8 TP_SB_XOR_AH8
RSVD8 F21 TP_SB_RSVD8 (AKA TP3, INTERNAL 20K PU)
MCH_SYNC* AH20 NB_SB_SYNC_L
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
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DRAWING NUMBER 051-6941
REV. 12
SCALE NONE
SHT 22 OF 104

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 63

=PP3V3_S5_SB 23 25 63

NO_REBOOT_MODE

RP2300 10K 5% 1/16W 5M-LF

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%

63 25 23 =PP3V3_S5_SB

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

OMIT
U2100
ICH7-M SB
BGA
(4 OF 6)

SMB_CLK 27 BI → C22 SMBCLK
SMB_DATA 27 BI → B22 SMBDATA
SMB_LINK_ALERT_L → A16 SMLINKALERT*
SMLINK<0> → B25 SMLINK0
SMLINK<1> → A25 SMLINK1
NOT USED
PM_RI_L → A28 RI*
SB_SPKR → A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L 56 49 48 47 5 OUT → A27 SUS_STAT*
PM_SYSRST_L 47 26 5 IN → A22 SYS_RST*
PM_BMBUSY_L 14 IN → AB18 GPIO0/BM_BUSY*
SMB_ALERT_L → B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 OUT → AC20 GPIO18/STPPCI*
PM_STPCPU_L 33 OUT → AF21 GPIO20/STPCPU*
SB_GPIO26 → A21 GPIO26
BIOS_REC 23 → B21 GPIO27
FWH_MFG_MODE 23 → E23 GPIO28
PM_CLKRUN_L 56 49 47 40 5 BI → AG18 GPIO32/CLKRUN*
TP_AZ_DOCK_EN → AC19 GPIO33/AZ_DOCK_EN*
RESERVED FOR MOBILE AZALIA DOCKING INTF
AZ_DOCK_RST → U2 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L 45 37 5 IN → F20 WAKE*
INT_SERIRQ 56 49 47 5 BI → AH21 SERIRQ
PM_THRM_L 47 IN → AF20 THRM*
VR_PWRGD_CK410 26 IN → AD22 VRMPWRGD
TP_SB_GPIO6 BI → AD21 GPIO6
SMC_RUNTIME_SCI_L 47 IN → AC18 GPIO7
SMC_EXTSMI_L 47 IN → E21 GPIO8

SMB
CLKS
SYS GPIO
PWR MNGT
GPIO

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

AF19 SB_GPIO21 → R2302 100 → 1 2
AH18 SB_GPIO19 → R2303 100 → 1 2
AH19
AE19 SB_GPIO37 → R2305 100 → 1 2
SATA_C_DET_L IN 36

CLK14 AC1 SB_CLK14P3M_TIMER IN 34
CLK48 B2 SB_CLK48M_USBCHB IN 34
SUSCLK C20 SUS_CLK_SB OUT 6

SLP_S3* B24 PM_SLP_S3 OUT 41 47 62
SLP_S4* D23 PM_SLP_S4 OUT 39 47 62
SLP_S5* F22 PM_SLP_S5 OUT 47 48
PWROK AA4 PM_SB_PWROK OUT 26
DPRSLPVR AC22 PM_DPRSLPVR OUT 14 57 79
NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
TP0/BATLOW* C21 PM_BATLOW_L IN 47
PWRBTN* C23 PM_PWRBTN_L IN 47
LAN_RST* C19 PM_LAN_ENABLE
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4 PM_RSMRST_L IN 47

GPIO9 E20 SMS_INT_L IN 47 48
GPIO10 A20 SMC_SB_NMI_L IN 47
GPIO12 F19 PATA_PWR_EN OUT 23
GPIO13 E19
GPIO14 R4 IDE_RESET_L OUT 36
GPIO15 E22 SV_SET_UP 5 23 49
GPIO24 R3 CRB_SV_DET 23
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 SB_CLK100M_SATA_OE_L 33
GPIO38 AD20 TP_SB_GPIO38 BI
GPIO39 AE20 SATA_C_PWR_EN_L OUT 23

DEF=GPI
DEF=GPI
DEF=GPO

=PP3V3_S5_SB_PM 11 26 63

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

R2399 100K 5% 1/16W 402 2MF-LF

SMC_WAKE_SCI_L IN 47

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

63 25 23 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%

SV_SET_UP 5 23 49
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 2MF-LF 5%

63 25 23 =PP3V3_S5_SB

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

R2314 NOSTUFF 0 1/16W 402 2MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 23 25 63

R2390 10K 5% 1/16W 2MF-LF 402

23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 21 23 63

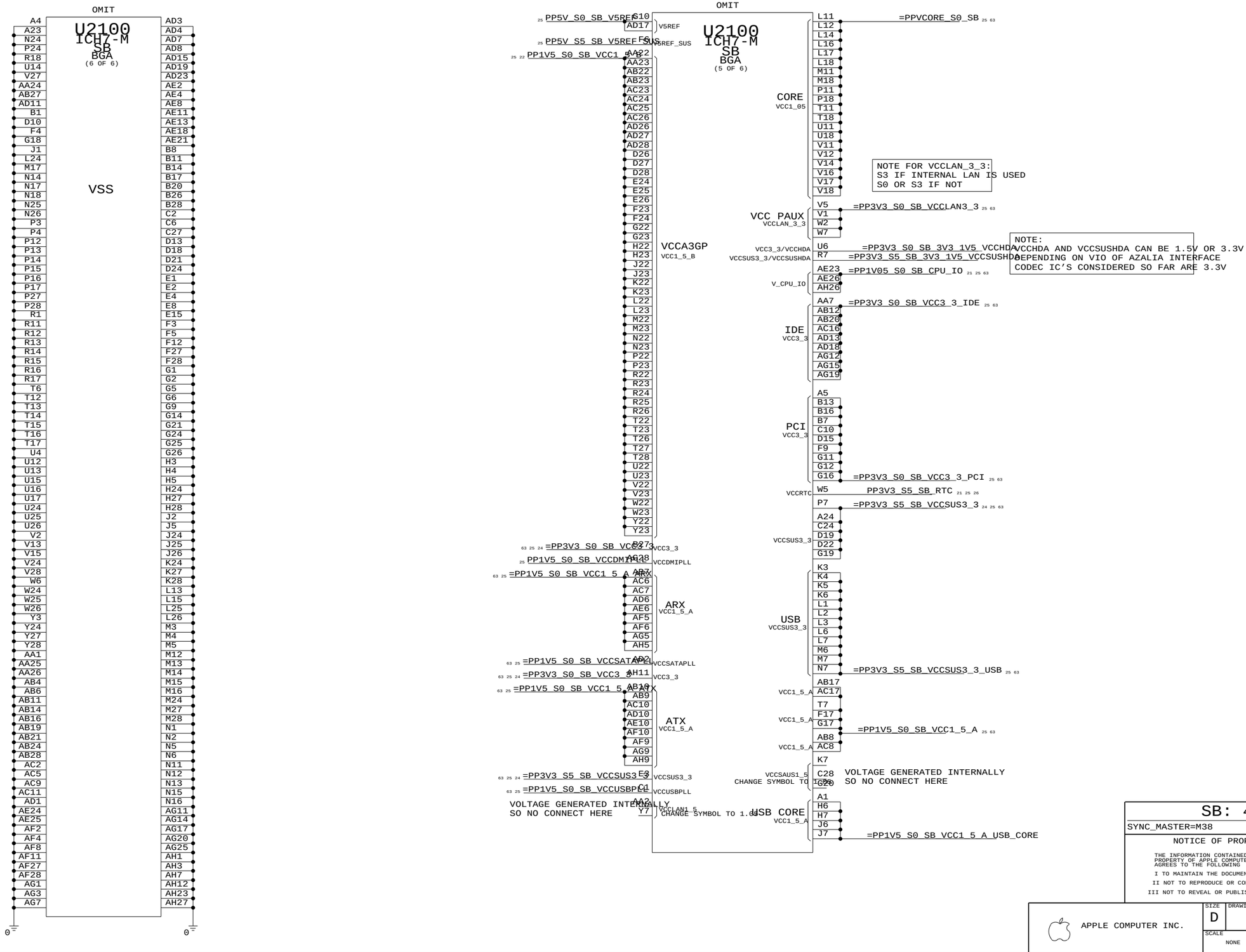
R2388 10K 5% 1/16W 2MF-LF 402

23 SATA_C_PWR_EN_L

SB: 3 OF 4
SYNC_MASTER=M38 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 23 OF 104	


OMIT
U2100
ICH7-M
SB
BGA
(6 OF 6)
VSS
OMIT
U2100
ICH7-M
SB
BGA
(5 OF 6)
V5REF
V5REF_SUS
VCCA3GP
VCC1_5_B
CORE
VCC1_05
VCC_PAUX
VCCLAN_3_3
VCC3_3/VCCHDA
VCCSUS3_3/VCCSUSHDA
V_CPU_IO
IDE
VCC3_3
PCI
VCC3_3
VCCRTC
USB
VCCSUS3_3
VCC1_5_A
ARX
VCC1_5_A
ATX
VCC1_5_A
VCCSUS3_3
VCCUSBPLL
VCCLAN1_5
USB CORE
VCC1_5_A
VCCSAUS1_5
VCCDMIPLL
VCCSATAPLL
VCC3_3
PP5V_S0_SB_V5REF
PP5V_S5_SB_V5REF_SUS
PP1V5_S0_SB_VCC1_5_A
=PPVCORE_S0_SB
=PP3V3_S0_SB_VCCLAN3_3
=PP3V3_S0_SB_3V3_1V5_VCCHDA
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
=PP1V05_S0_SB_CPU_IO
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_VCC3_3_PCI
PP3V3_S5_SB_RTC
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S0_SB_VCC3_3
=PP1V5_S0_SB_VCCDMIPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCCSATAPLL
=PP3V3_S0_SB_VCC3_3
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP3V3_S5_SB_VCCSUS3_3
=PP1V5_S0_SB_VCCUSBPLL
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT
NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V
VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE
CHANGE SYMBOL TO 1.0u
VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE
CHANGE SYMBOL TO 1.0u
SB: 4 OF 4
SYNC_MASTER=M38
SYNC_DATE=11/16/2005
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SIZE
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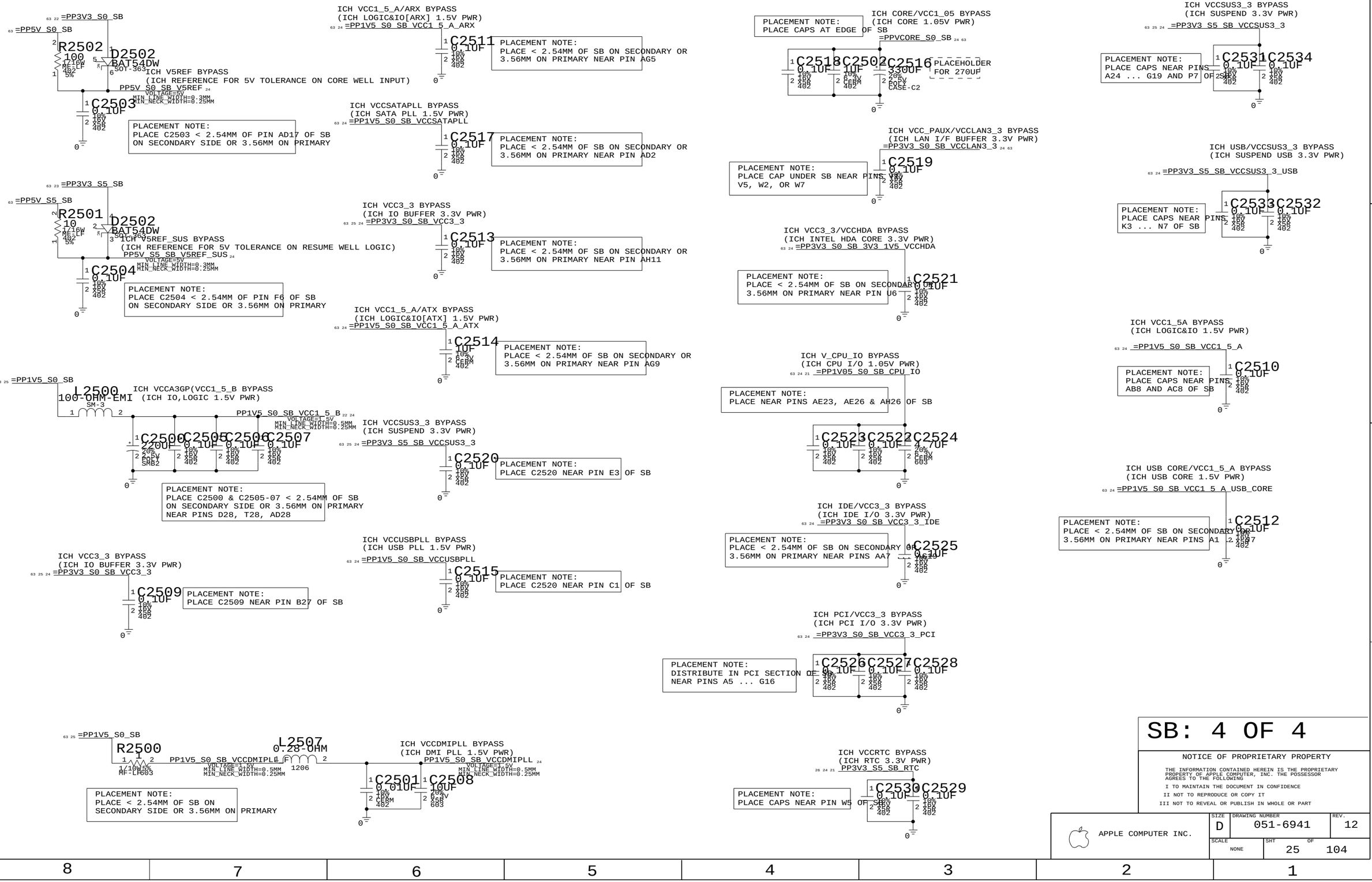
DRAWING NUMBER
051-6941
REV.
12
SCALE
NONE
SHT
24
OF
104


ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
100-OHM-EMI
PP1V5_S0_SB_VCC1_5_B
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V5, W2, OR W7
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1
SB: 4 OF 4
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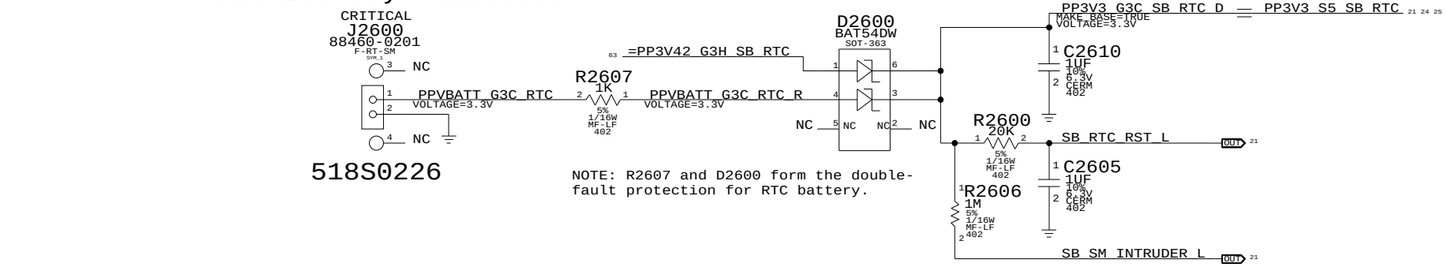
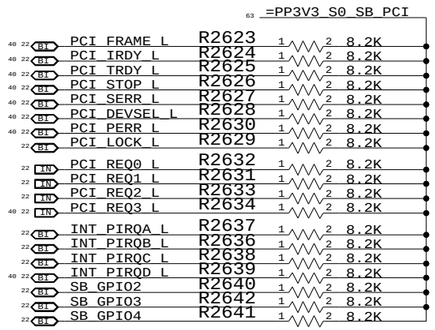
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 12
SCALE NONE
SHT 25 OF 104

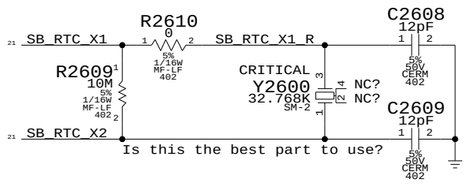
RTC Battery Connector



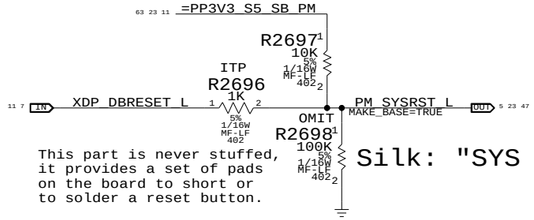
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



Is this the best part to use?

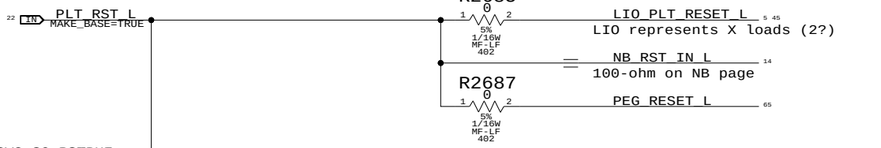


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

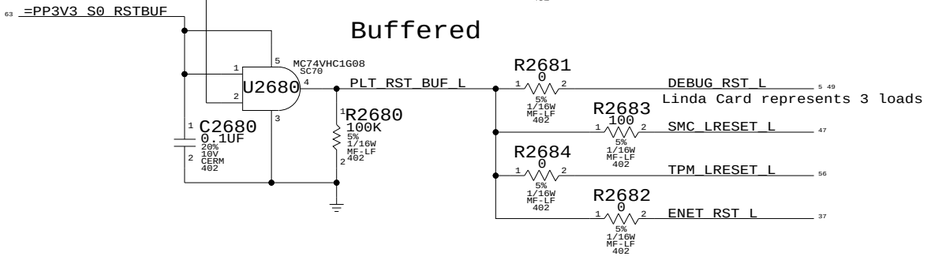
Silk: "SYS RST"

Platform Reset Connections

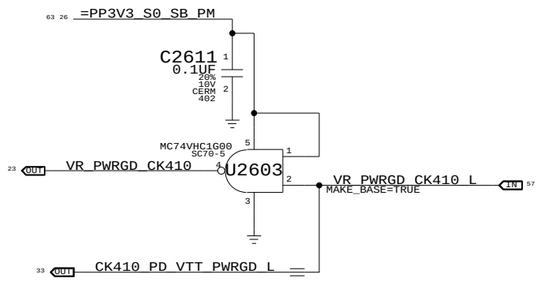
Unbuffered



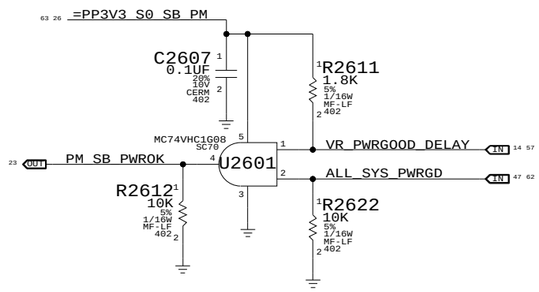
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



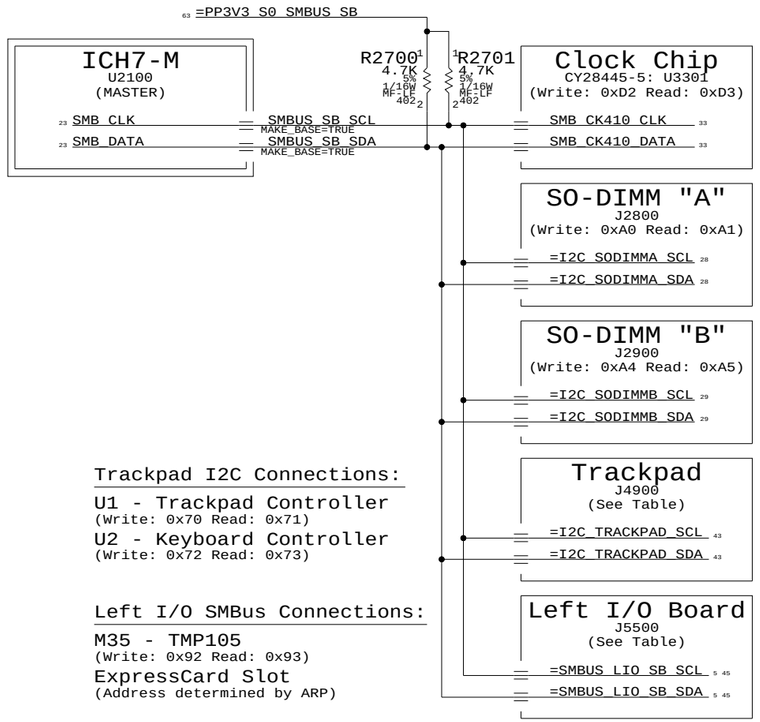
SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 26 OF 104	

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

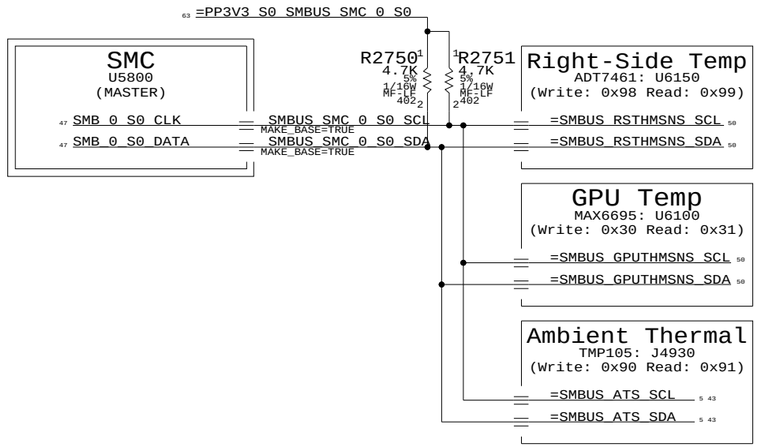
U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

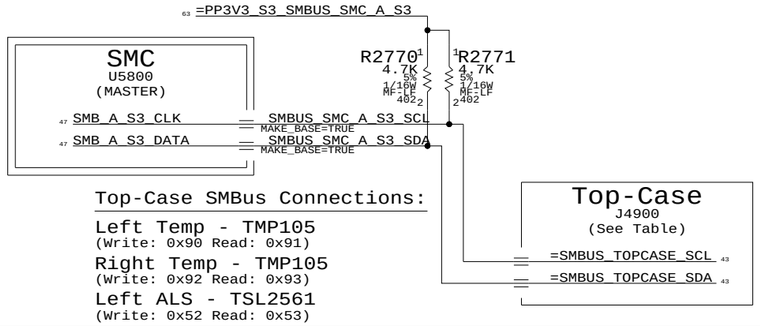
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



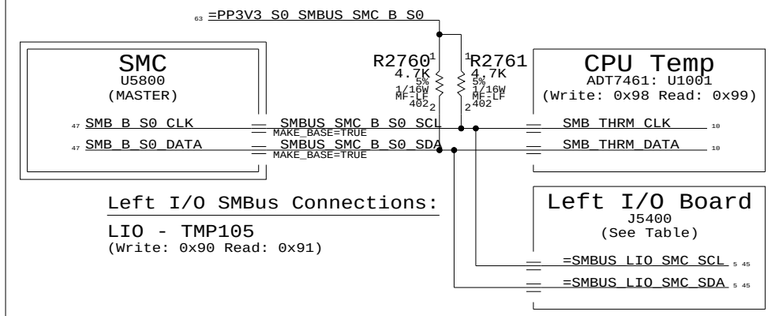
Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

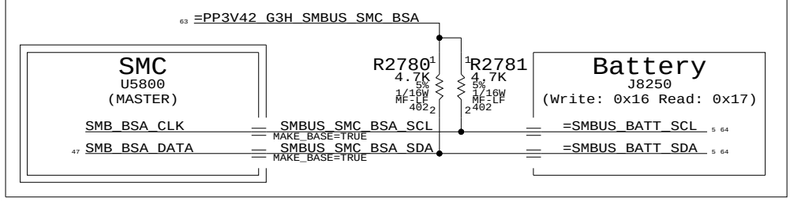
SMC "B" SMBus Connections



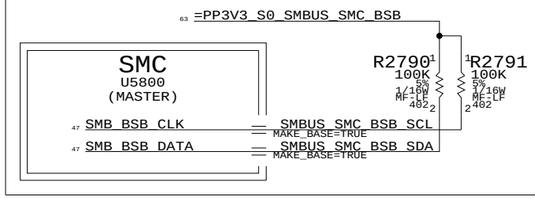
Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	27	104

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot

32 29 MEM_VREF

C2801 2.2uF 20% 6.3V CERM 603

C2800 0.1uF 20% 10V CERM 402

63 29 28 =PP1V8_S3_MEM

203 NC

201 NC

CRITICAL
J2800
F-RT-SM
DDR2-SODIMM-DUAL

	1A	VREF	VSS0	2A			
	3A	VSS1	DQ4	4A	MEM_A_DQ<8>		15
15 MEM_A_DQ<14>	5A	DQ0	DQ5	6A	MEM_A_DQ<12>		15
15 MEM_A_DQ<13>	7A	DQ1	VSS2	8A			
	9A	VSS4	DM0	10A	MEM_A_DM<1>		15
15 MEM_A_DQS_N<1>	11A	DQS0*	VSS5	12A			
15 MEM_A_DQS_P<1>	13A	DQS0	DQ6	14A	MEM_A_DQ<15>		15
	15A	VSS6	DQ7	16A	MEM_A_DQ<9>		15
15 MEM_A_DQ<10>	17A	DQ2	VSS7	18A			
15 MEM_A_DQ<11>	19A	DQ3	DQ12	20A	MEM_A_DQ<2>		15
	21A	VSS8	DQ13	22A	MEM_A_DQ<3>		15
15 MEM_A_DQ<5>	23A	DQ8	VSS9	24A			
15 MEM_A_DQ<4>	25A	DQ9	DM1	26A	MEM_A_DM<0>		15
	27A	VSS10	VSS11	28A			
15 MEM_A_DQS_N<0>	29A	DQS1*	CK0	30A	MEM_CLK_P<0>		14
15 MEM_A_DQS_P<0>	31A	DQS1	CK0*	32A	MEM_CLK_N<0>		14
	33A	VSS12	VSS13	34A			
15 MEM_A_DQ<6>	35A	DQ10	DQ14	36A	MEM_A_DQ<1>		15
15 MEM_A_DQ<7>	37A	DQ11	DQ15	38A	MEM_A_DQ<0>		15
	39A	VSS14	VSS15	40A			
			KEY				
	41A	VSS16	VSS17	42A			
15 MEM_A_DQ<19>	43A	DQ16	DQ20	44A	MEM_A_DQ<23>		15
15 MEM_A_DQ<18>	45A	DQ17	DQ21	46A	MEM_A_DQ<22>		15
	47A	VSS18	VSS19	48A			
15 MEM_A_DQS_N<2>	49A	DQS2*	NC0	50A	DIMM_OVERTEMP_L		29 48
15 MEM_A_DQS_P<2>	51A	DQS2	DM2	52A	MEM_A_DM<2>		15
	53A	VSS21	VSS22	54A			
15 MEM_A_DQ<20>	55A	DQ18	DQ22	56A	MEM_A_DQ<21>		15
15 MEM_A_DQ<16>	57A	DQ19	DQ23	58A	MEM_A_DQ<17>		15
	59A	VSS23	VSS24	60A			
15 MEM_A_DQ<28>	61A	DQ24	DQ28	62A	MEM_A_DQ<29>		15
15 MEM_A_DQ<25>	63A	DQ25	DQ29	64A	MEM_A_DQ<24>		15
	65A	VSS25	VSS26	66A			
15 MEM_A_DM<3>	67A	DM3	DQS3*	68A	MEM_A_DQS_N<3>		15
NC	69A	NC1	DQS3	70A	MEM_A_DQS_P<3>		15
	71A	VSS27	VSS28	72A			
15 MEM_A_DQ<27>	73A	DQ26	DQ30	74A	MEM_A_DQ<26>		15
15 MEM_A_DQ<30>	75A	DQ27	DQ31	76A	MEM_A_DQ<31>		15
	77A	VSS29	VSS30	78A			
30 14 MEM_CKE<0>	79A	CKE0	NC/CKE1	80A	MEM_CKE<1>		14 30
	81A	VDD0	VDD1	82A			
NC	83A	NC2	NC/A15	84A	MEM_A_A<15>		6
30 15 MEM_A_BS<2>	85A	BA2	NC/A14	86A	MEM_A_A<14>		6
	87A	VDD2	VDD3	88A			
30 15 MEM_A_A<12>	89A	A12	A11	90A	MEM_A_A<11>		15 30
30 15 MEM_A_A<9>	91A	A9	A7	92A	MEM_A_A<7>		15 30
30 15 MEM_A_A<8>	93A	A8	A6	94A	MEM_A_A<6>		15 30
	95A	VDD4	VDD5	96A			
30 15 MEM_A_A<5>	97A	A5	A4	98A	MEM_A_A<4>		15 30
30 15 MEM_A_A<3>	99A	A3	A2	100A	MEM_A_A<2>		15 30
30 15 MEM_A_A<1>	101A	A1	A0	102A	MEM_A_A<0>		15 30
	103A	VDD6	VDD7	104A			
30 15 MEM_A_A<10>	105A	A10/AP	BA1	106A	MEM_A_BS<1>		15 30
30 15 MEM_A_BS<0>	107A	BA0	RAS*	108A	MEM_A_RAS_L		15 30
30 15 MEM_A_WE_L	109A	WE*	S0*	110A	MEM_CS_L<0>		14 30
	111A	VDD8	VDD9	112A			
30 15 MEM_A_CAS_L	113A	CAS*	ODT0	114A	MEM_ODT<0>		14 30
30 14 MEM_CS_L<1>	115A	NC/S1*	NC/A13	116A	MEM_A_A<13>		15 30
	117A	VDD10	VDD11	118A			
30 14 MEM_ODT<1>	119A	NC/ODT1	NC3	120A	NC		
	121A	VSS31	VSS32	122A			
15 MEM_A_DQ<35>	123A	DQ32	DQ36	124A	MEM_A_DQ<38>		15
15 MEM_A_DQ<39>	125A	DQ33	DQ37	126A	MEM_A_DQ<34>		15
	127A	VSS33	VSS34	128A			
15 MEM_A_DQS_N<4>	129A	DQS4*	DM4	130A	MEM_A_DM<4>		15
15 MEM_A_DQS_P<4>	131A	DQS4	VSS35	132A			
	133A	VSS36	DQ38	134A	MEM_A_DQ<32>		15
15 MEM_A_DQ<37>	135A	DQ34	DQ39	136A	MEM_A_DQ<36>		15
15 MEM_A_DQ<33>	137A	DQ35	VSS37	138A			
	139A	VSS38	DQ44	140A	MEM_A_DQ<57>		15
15 MEM_A_DQ<60>	141A	DQ40	DQ45	142A	MEM_A_DQ<63>		15
15 MEM_A_DQ<59>	143A	DQ41	VSS39	144A			
	145A	VSS40	DQS5*	146A	MEM_A_DQS_N<7>		15
15 MEM_A_DM<7>	147A	DM5	DQS5	148A	MEM_A_DQS_P<7>		15
	149A	VSS41	VSS42	150A			
15 MEM_A_DQ<58>	151A	DQ42	DQ46	152A	MEM_A_DQ<56>		15
15 MEM_A_DQ<61>	153A	DQ43	DQ47	154A	MEM_A_DQ<62>		15
	155A	VSS43	VSS44	156A			
15 MEM_A_DQ<43>	157A	DQ48	DQ52	158A	MEM_A_DQ<40>		15
15 MEM_A_DQ<45>	159A	DQ49	DQ53	160A	MEM_A_DQ<42>		15
	161A	VSS45	VSS46	162A			
NC	163A	NC_TEST	CK1	164A	MEM_CLK_P<1>		14
	165A	VSS47	CK1*	166A	MEM_CLK_N<1>		14
15 MEM_A_DQS_N<5>	167A	DQS6*	VSS48	168A			
15 MEM_A_DQS_P<5>	169A	DQS6	DM6	170A	MEM_A_DM<5>		15
	171A	VSS49	VSS50	172A			
15 MEM_A_DQ<41>	173A	DQ50	DQ54	174A	MEM_A_DQ<47>		15
15 MEM_A_DQ<46>	175A	DQ51	DQ55	176A	MEM_A_DQ<44>		15
	177A	VSS51	VSS52	178A			
15 MEM_A_DQ<51>	179A	DQ56	DQ60	180A	MEM_A_DQ<54>		15
15 MEM_A_DQ<50>	181A	DQ57	DQ61	182A	MEM_A_DQ<55>		15
	183A	VSS53	VSS54	184A			
15 MEM_A_DM<6>	185A	DM7	DQS7*	186A	MEM_A_DQS_N<6>		15
	187A	VSS55	DQS7	188A	MEM_A_DQS_P<6>		15
15 MEM_A_DQ<53>	189A	DQ58	VSS56	190A			
15 MEM_A_DQ<48>	191A	DQ59	DQ62	192A	MEM_A_DQ<52>		15
63 29 =PPSPD_S0_MEM	193A	VSS57	DQ63	194A	MEM_A_DQ<49>		15
27 =I2C_SODIMMA_SDA	195A	SDA	VSS58	196A			
27 =I2C_SODIMMA_SCL	197A	SCL	SA0	198A			
	199A	VDDSPD	SA1	200A	ADDR=0xA0(WR)/0xA1(RD)		

202 NC

204 NC

516S0382

DDR2 Bypass Caps

(For return current)

63 29 28 =PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603

C2809 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402

C2811 0.1uF 20% 10V CERM 402

C2812 0.1uF 20% 10V CERM 402

C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402

C2815 0.1uF 20% 10V CERM 402

C2816 0.1uF 20% 10V CERM 402

C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402

C2819 0.1uF 20% 10V CERM 402

C2820 0.1uF 20% 10V CERM 402

C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	28	104

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (thru-hole) slot

32 28 MEM_VREF

C2901 2.2uF 20% 6.3V CERM 603

C2900 0.1uF 20% 10V CERM 402

63 29 28 =PP1V8_S3_MEM

20 NC

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		2B	VSS0		
	3B	VSS1		4B	DQ4	15	MEM_B_DQ<9>
15	MEM_B_DQ<15>	5B	DQ0	6B	DQ5	15	MEM_B_DQ<11>
15	MEM_B_DQ<14>	7B	DQ1	8B	VSS2		
	9B	VSS4	DM0	10B		15	MEM_B_DM<1>
15	MEM_B_DQS_N<1>	11B	DQS0*	12B	VSS5		
15	MEM_B_DQS_P<1>	13B	DQS0	14B	DQ6	15	MEM_B_DQ<12>
	15B	VSS6	DQ7	16B		15	MEM_B_DQ<8>
15	MEM_B_DQ<10>	17B	DQ2	18B	VSS7		
15	MEM_B_DQ<13>	19B	DQ3	20B	DQ12	15	MEM_B_DQ<3>
	21B	VSS8	DQ13	22B		15	MEM_B_DQ<6>
15	MEM_B_DQ<7>	23B	DQ8	24B	VSS9		
15	MEM_B_DQ<2>	25B	DQ9	26B	DM1	15	MEM_B_DM<0>
	27B	VSS10	VSS11	28B			
15	MEM_B_DQS_N<0>	29B	DQS1*	30B	CK0	14	MEM_CLK_P<3>
15	MEM_B_DQS_P<0>	31B	DQS1	32B	CK0*	14	MEM_CLK_N<3>
	33B	VSS12	VSS13	34B			
15	MEM_B_DQ<1>	35B	DQ10	36B	DQ14	15	MEM_B_DQ<0>
15	MEM_B_DQ<4>	37B	DQ11	38B	DQ15	15	MEM_B_DQ<5>
	39B	VSS14	VSS15	40B			
			KEY				
	41B	VSS16	VSS17	42B			
15	MEM_B_DQ<21>	43B	DQ16	44B	DQ20	15	MEM_B_DQ<22>
15	MEM_B_DQ<19>	45B	DQ17	46B	DQ21	15	MEM_B_DQ<18>
	47B	VSS18	VSS19	48B			
15	MEM_B_DQS_N<2>	49B	DQS2*	50B	NC0	28 48	DIMM_OVERTEMP_L
15	MEM_B_DQS_P<2>	51B	DQS2	52B	DM2	15	MEM_B_DM<2>
	53B	VSS21	VSS22	54B			
15	MEM_B_DQ<20>	55B	DQ18	56B	DQ22	15	MEM_B_DQ<17>
15	MEM_B_DQ<23>	57B	DQ19	58B	DQ23	15	MEM_B_DQ<16>
	59B	VSS23	VSS24	60B			
15	MEM_B_DQ<29>	61B	DQ24	62B	DQ28	15	MEM_B_DQ<26>
15	MEM_B_DQ<24>	63B	DQ25	64B	DQ29	15	MEM_B_DQ<28>
	65B	VSS25	VSS26	66B			
15	MEM_B_DM<3>	67B	DM3	68B	DQS3*	15	MEM_B_DQS_N<3>
NC	69B	NC1	DQS3	70B		15	MEM_B_DQS_P<3>
	71B	VSS27	VSS28	72B			
15	MEM_B_DQ<27>	73B	DQ26	74B	DQ30	15	MEM_B_DQ<31>
15	MEM_B_DQ<25>	75B	DQ27	76B	DQ31	15	MEM_B_DQ<30>
	77B	VSS29	VSS30	78B			
30 14	MEM_CKE<2>	79B	CKE0	80B	NC/CKE1	14 30	MEM_CKE<3>
	81B	VDD0	VDD1	82B			
NC	83B	NC2	NC/A15	84B		6	MEM_B_A<15>
30 15	MEM_B_BS<2>	85B	BA2	86B	NC/A14	6	MEM_B_A<14>
	87B	VDD2	VDD3	88B			
30 15	MEM_B_A<12>	89B	A12	90B	A11	15 30	MEM_B_A<11>
30 15	MEM_B_A<9>	91B	A9	92B	A7	15 30	MEM_B_A<7>
30 15	MEM_B_A<8>	93B	A8	94B	A6	15 30	MEM_B_A<6>
	95B	VDD4	VDD5	96B			
30 15	MEM_B_A<5>	97B	A5	98B	A4	15 30	MEM_B_A<4>
30 15	MEM_B_A<3>	99B	A3	100B	A2	15 30	MEM_B_A<2>
30 15	MEM_B_A<1>	101B	A1	102B	A0	15 30	MEM_B_A<0>
	103B	VDD6	VDD7	104B			
30 15	MEM_B_A<10>	105B	A10/AP	106B	BA1	15 30	MEM_B_BS<1>
30 15	MEM_B_BS<0>	107B	BA0	108B	RAS*	15 30	MEM_B_RAS_L
30 15	MEM_B_WE_L	109B	WE*	110B	S0*	14 30	MEM_CS_L<2>
	111B	VDD8	VDD9	112B			
30 15	MEM_B_CAS_L	113B	CAS*	114B	ODT0	14 30	MEM_ODT<2>
30 14	MEM_CS_L<3>	115B	NC/S1*	116B	NC/A13	15 30	MEM_B_A<13>
	117B	VDD10	VDD11	118B			
30 14	MEM_ODT<3>	119B	NC/ODT1	120B	NC3		NC
	121B	VSS31	VSS32	122B			
15	MEM_B_DQ<36>	123B	DQ32	124B	DQ36	15	MEM_B_DQ<32>
15	MEM_B_DQ<33>	125B	DQ33	126B	DQ37	15	MEM_B_DQ<37>
	127B	VSS33	VSS34	128B			
15	MEM_B_DQS_N<4>	129B	DQS4*	130B	DM4	15	MEM_B_DM<4>
15	MEM_B_DQS_P<4>	131B	DQS4	132B	VSS35		
	133B	VSS36	DQ38	134B		15	MEM_B_DQ<38>
15	MEM_B_DQ<34>	135B	DQ34	136B	DQ39	15	MEM_B_DQ<39>
15	MEM_B_DQ<35>	137B	DQ35	138B	VSS37		
	139B	VSS38	DQ44	140B		15	MEM_B_DQ<44>
15	MEM_B_DQ<40>	141B	DQ40	142B	DQ45	15	MEM_B_DQ<45>
15	MEM_B_DQ<41>	143B	DQ41	144B	VSS39		
	145B	VSS40	DQS5*	146B		15	MEM_B_DQS_N<5>
15	MEM_B_DM<5>	147B	DM5	148B	DQS5	15	MEM_B_DQS_P<5>
	149B	VSS41	VSS42	150B			
15	MEM_B_DQ<42>	151B	DQ42	152B	DQ46	15	MEM_B_DQ<46>
15	MEM_B_DQ<43>	153B	DQ43	154B	DQ47	15	MEM_B_DQ<47>
	155B	VSS43	VSS44	156B			
15	MEM_B_DQ<62>	157B	DQ48	158B	DQ52	15	MEM_B_DQ<58>
15	MEM_B_DQ<59>	159B	DQ49	160B	DQ53	15	MEM_B_DQ<63>
	161B	VSS45	VSS46	162B			
NC	163B	NC_TEST	CK1	164B		14	MEM_CLK_P<2>
	165B	VSS47	CK1*	166B		14	MEM_CLK_N<2>
15	MEM_B_DQS_N<7>	167B	DQS6*	168B	VSS48		
15	MEM_B_DQS_P<7>	169B	DQS6	170B	DM6	15	MEM_B_DM<7>
	171B	VSS49	VSS50	172B			
15	MEM_B_DQ<60>	173B	DQ50	174B	DQ54	15	MEM_B_DQ<56>
15	MEM_B_DQ<61>	175B	DQ51	176B	DQ55	15	MEM_B_DQ<57>
	177B	VSS51	VSS52	178B			
15	MEM_B_DQ<54>	179B	DQ56	180B	DQ60	15	MEM_B_DQ<55>
15	MEM_B_DQ<51>	181B	DQ57	182B	DQ61	15	MEM_B_DQ<50>
	183B	VSS53	VSS54	184B			
15	MEM_B_DM<6>	185B	DM7	186B	DQS7*	15	MEM_B_DQS_N<6>
	187B	VSS55	DQS7	188B		15	MEM_B_DQS_P<6>
15	MEM_B_DQ<52>	189B	DQ58	190B	VSS56		
15	MEM_B_DQ<49>	191B	DQ59	192B	DQ62	15	MEM_B_DQ<53>
63 29 28	=PPSPD_S0_MEM	193B	VSS57	194B	DQ63	15	MEM_B_DQ<48>
27	=I2C_SODIMMB_SDA	195B	SDA	196B	VSS58		Resistor prevents pwr-gnd short
27	=I2C_SODIMMB_SCL	197B	SCL	198B	SA0		
	199B	VDDSPD	SA1	200B			SODIMM_A_SA1
							ADDR=0xA4(WR)/0xA5(RD)

516-0140 202 NC

=PPSPD_S0_MEM 28 29 63

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

63 29 28 =PP1V8_S3_MEM

C2908 10UF 20% 6.3V X5R 603

C2909 10UF 20% 6.3V X5R 603

C2910 0.1uF 20% 10V CERM 402

C2911 0.1uF 20% 10V CERM 402

C2912 0.1uF 20% 10V CERM 402

C2913 0.1uF 20% 10V CERM 402

C2914 0.1uF 20% 10V CERM 402

C2915 0.1uF 20% 10V CERM 402

C2916 0.1uF 20% 10V CERM 402

C2917 0.1uF 20% 10V CERM 402

C2918 0.1uF 20% 10V CERM 402

C2919 0.1uF 20% 10V CERM 402

C2920 0.1uF 20% 10V CERM 402

C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

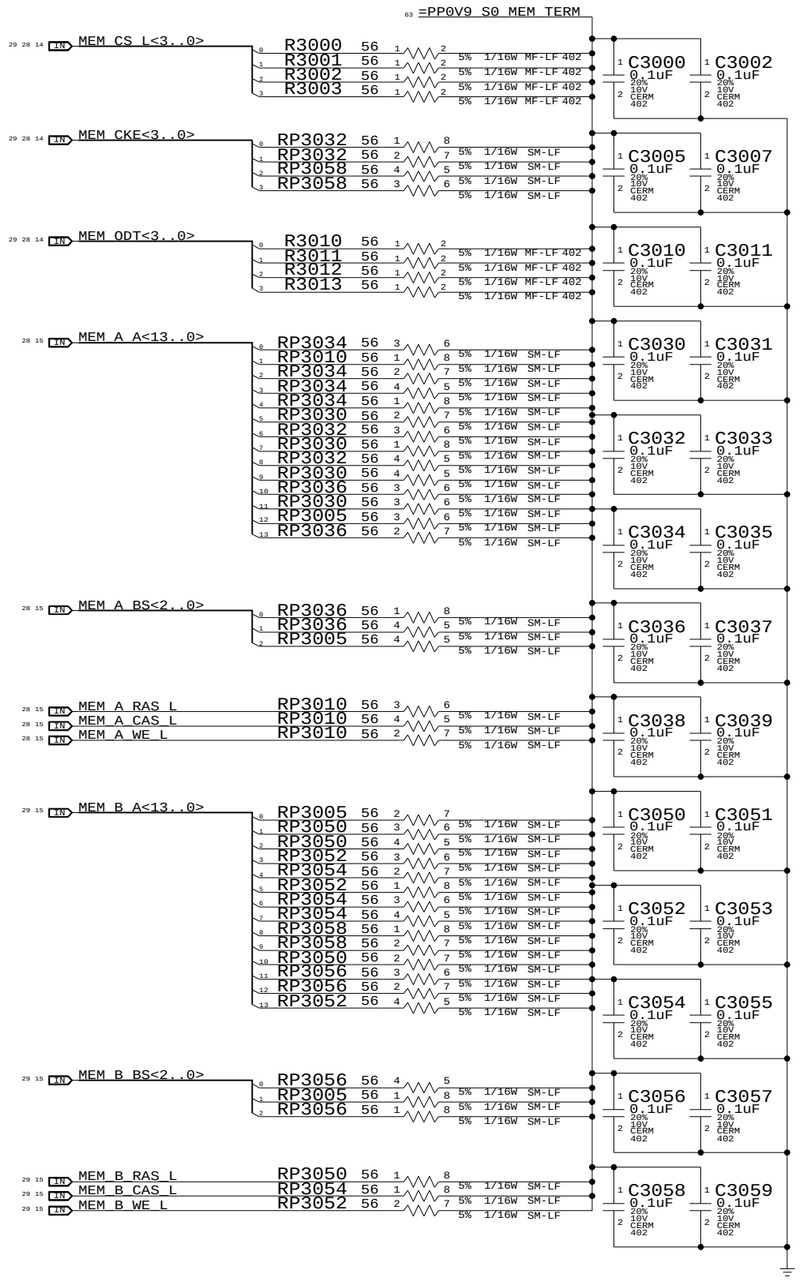
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	29	104

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	30	104

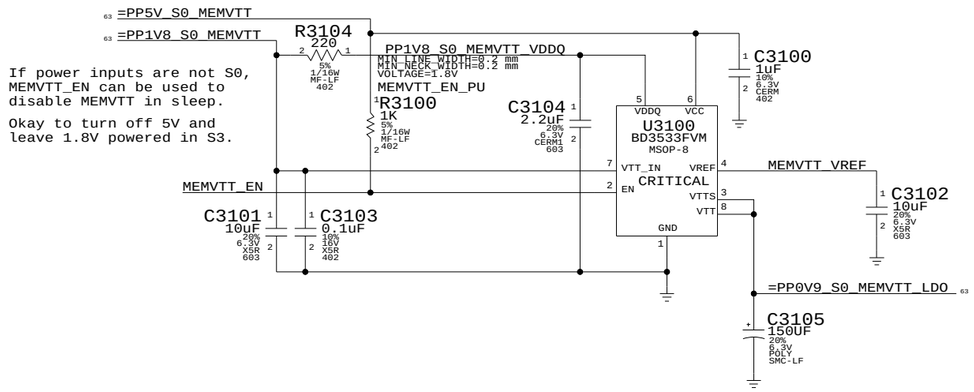
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

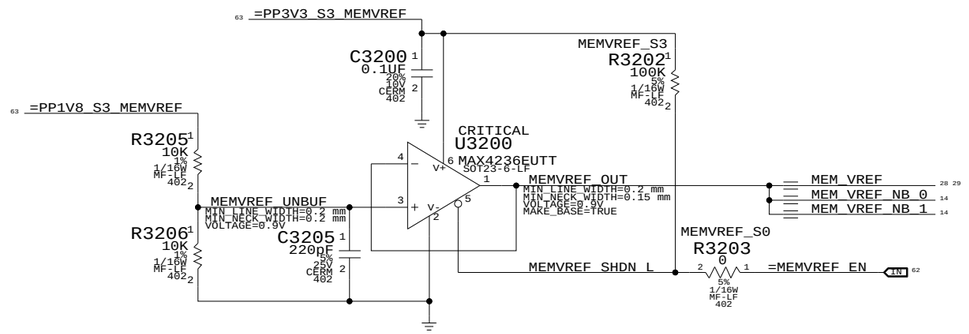
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	31	104



DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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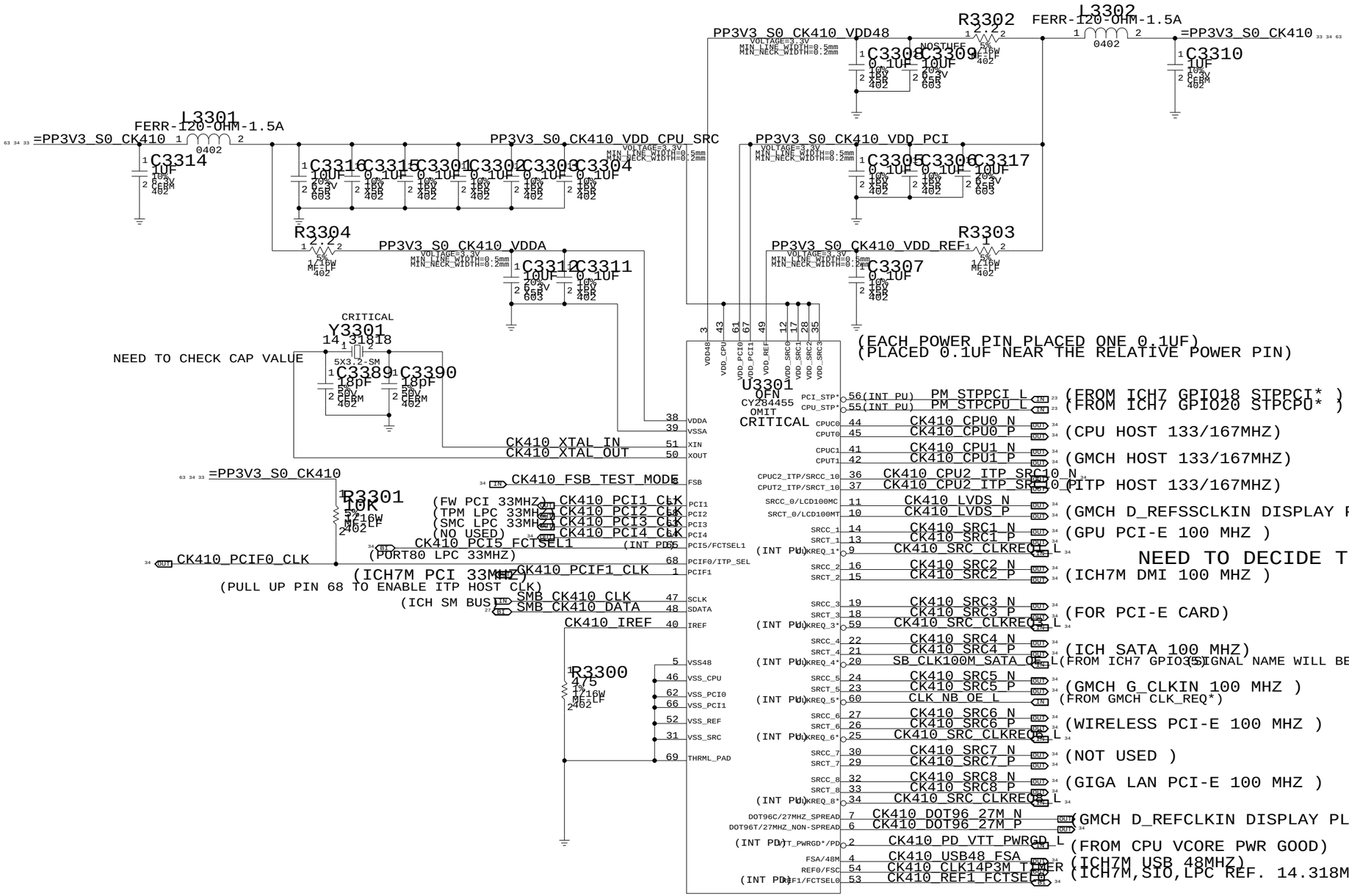
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	32	104



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SS	T100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	BD	SRCT0	SRCC0

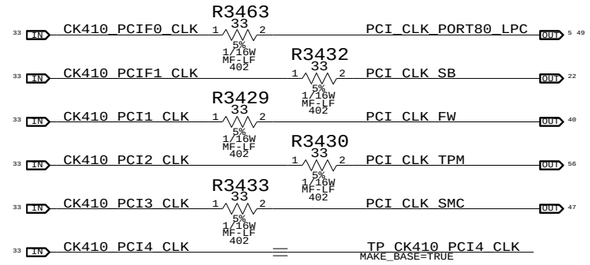
CLOCKS

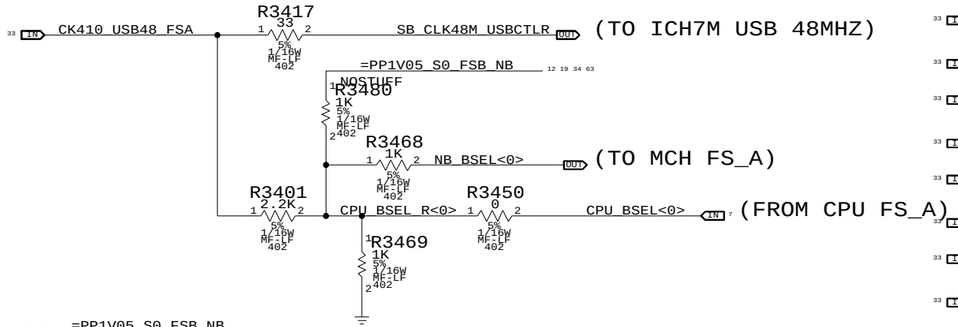
SYNC_MASTER=M82 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	33	104

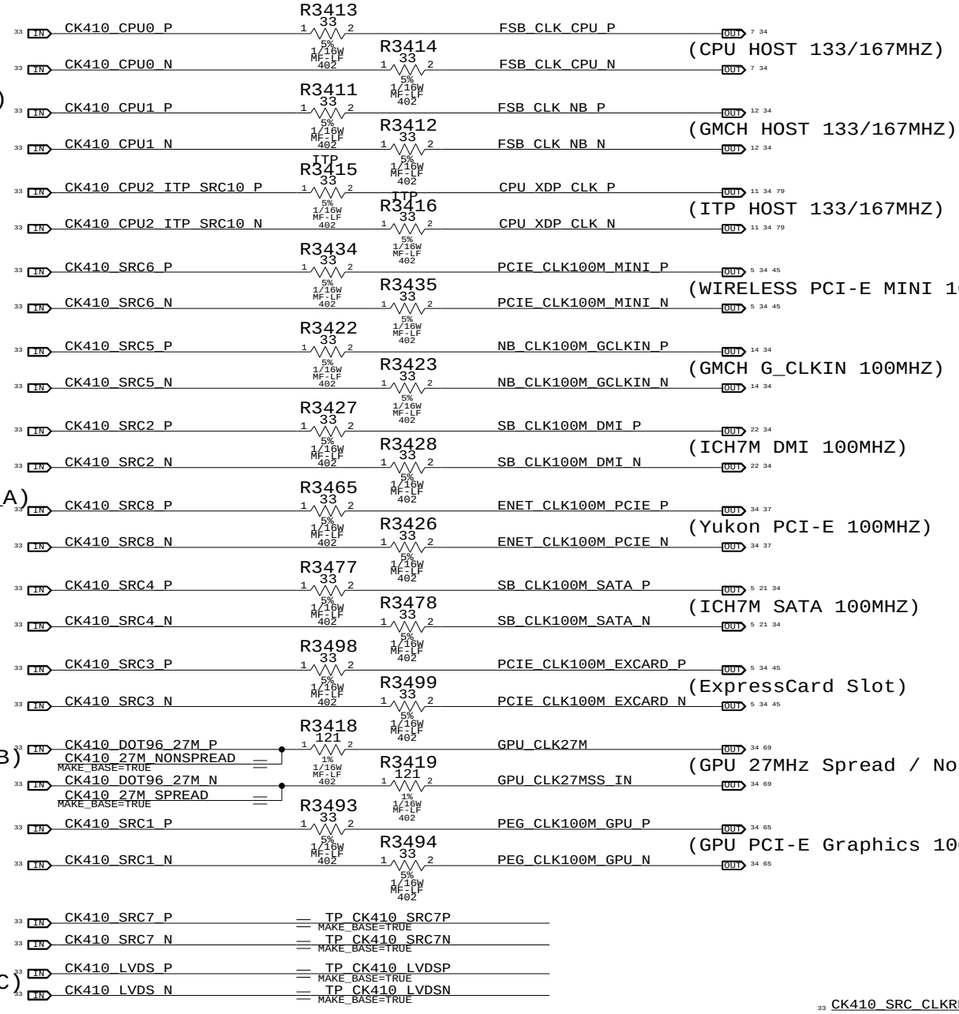


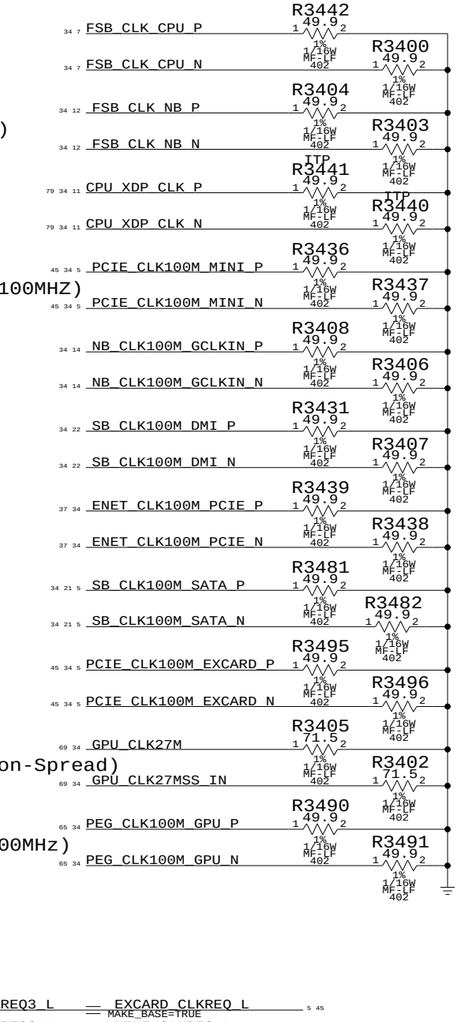


NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

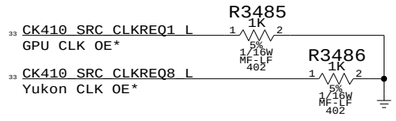
FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED





CK410_SRC_CLKREQ3_L — EXCARD_CLKREQ_L (MAKE_BASE=TRUE)
CK410_SRC_CLKREQ6_L — MINI_CLKREQ_L (MAKE_BASE=TRUE)



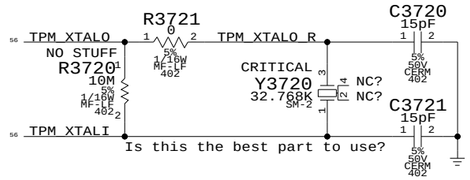
Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

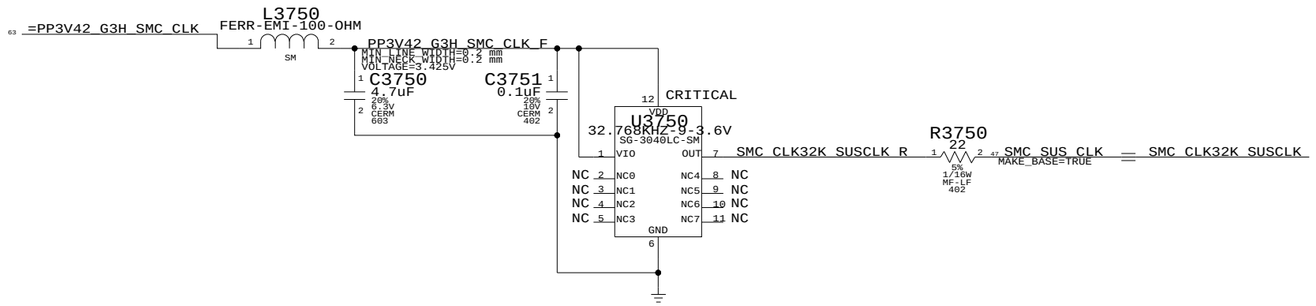
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT: 34	OF: 104

TPM Crystal Circuit



SMC G3Hot Oscillator



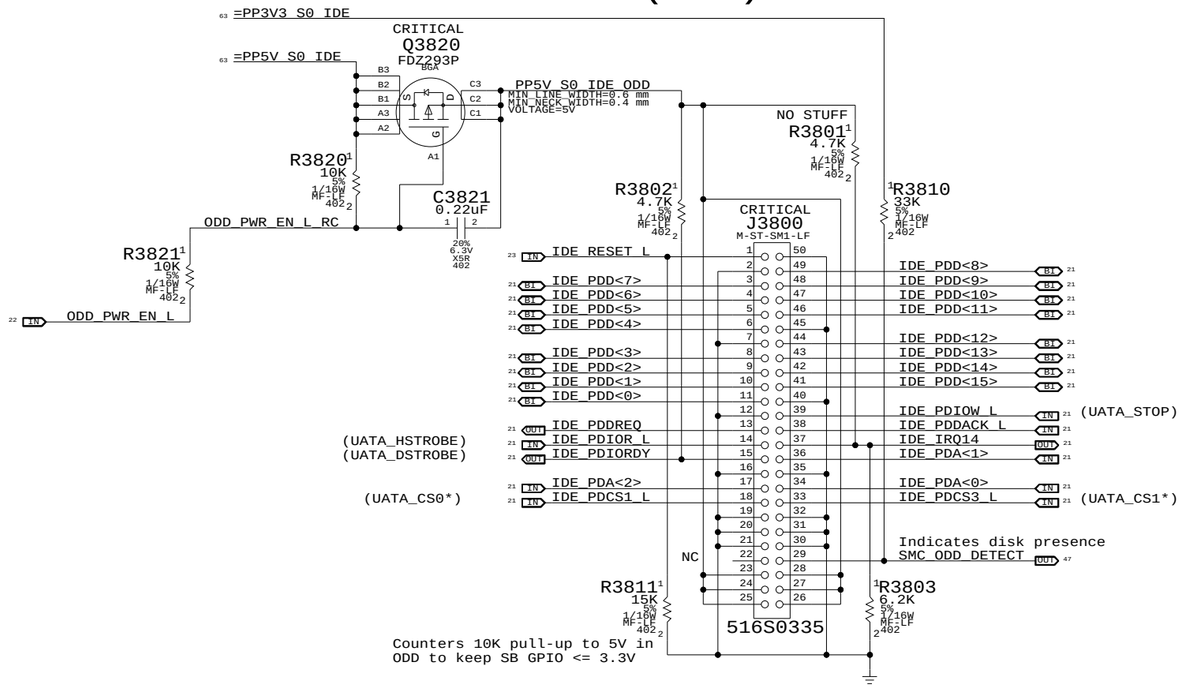
Mobile Clocking

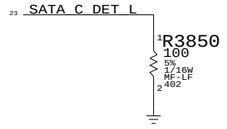
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

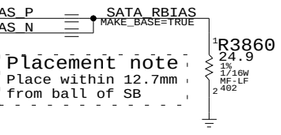
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 37 OF 104	

IDE (ODD) Connector





21 SATA_A_R2D_C_P — TP_SATA_A_R2DP (MAKE_BASE=TRUE)
21 SATA_A_R2D_C_N — TP_SATA_A_R2DN (MAKE_BASE=TRUE)
21 SATA_A_D2R_P — TP_SATA_A_D2RP (MAKE_BASE=TRUE)
21 SATA_A_D2R_N — TP_SATA_A_D2RN (MAKE_BASE=TRUE)



PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 38 OF 104	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01 MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

=PP2V5_S3_ENET AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402 =PP2V5_S3_ENET

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET
R4101 4.7K 5% 1/16W MF-LF 402

=PP1V2_S3_ENET
=PP3V3_S3_ENET

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

C4113 0.1UF 10% 16V X5R 402

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

ENET_LOM_DIS_L
=ENET_VMAIN_AVLBL
ENET_CTRL25
ENET_CTRL12
ENET_RSET

R4102 4.87K 1% 1/16W MF-LF 402

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

OMIT
CRITICAL
U4101
88E8053
QFN

ANALOG
PCI EXPRESS
MEDIA
LED
TEST
TWSI
SPI
MAIN CLK

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053

INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

THRML_PAD

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0
ENET_MDI1
ENET_MDI2
ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET
R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

=PP3V3_S3_ENET
PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

ENET_VPD_DATA
ENET_VPD_CLK

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP1V2_S3_ENET
C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP3V3_S3_ENET
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE	SHT	OF
NONE	41	104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

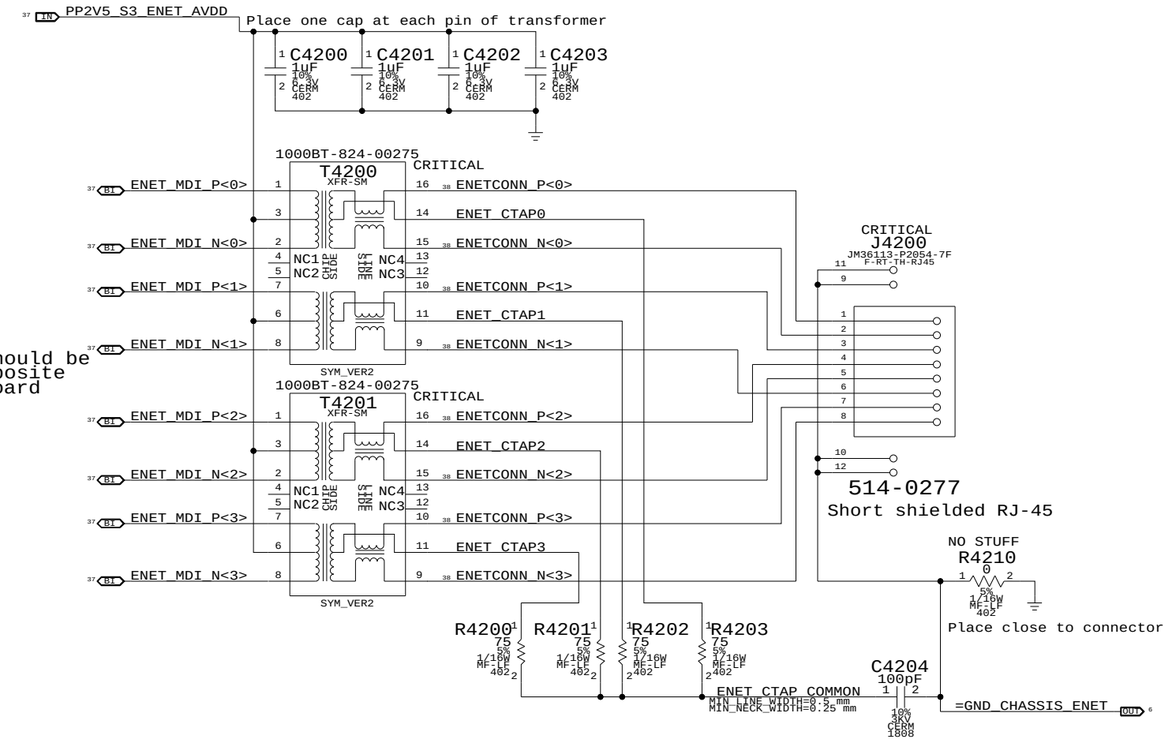
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

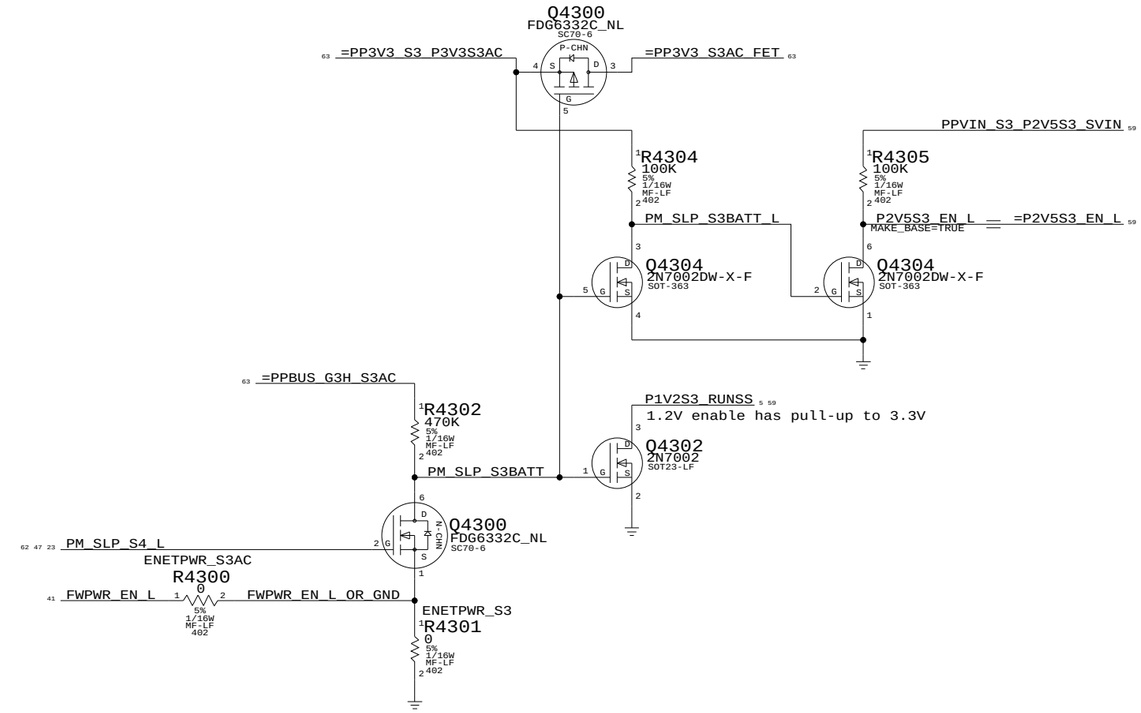
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 42 OF 104	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	43	104

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23256 ADDED
6/21/2005 - CHANGED INT*_IO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IO TO ADI3 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT IO_REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST# AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW_DIFF_PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

0.001A DURING SLEEP

63 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 20% 16V CERM 402
C4422 0.1UF 20% 16V CERM 402
C4426 0.1UF 20% 16V CERM 402
C4428 0.1UF 20% 16V CERM 402
C4430 0.1UF 20% 16V CERM 402
C4432 0.1UF 20% 16V CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

GND_FW_VSSA 40
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

63 =PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

CRITICAL
U4400
FW32306
BGA
OMIT

VDD0 G4, VDD1 N1, VDD2 N2, VDD3 K5, VDD4 K6, VDD5 K7, VDD6 L13, VDD7 H13, VDD9 A2
VDDA0 D10, VDDA1 A13, VDDA2 B13, VDDA3 A7, VDDA4 A8, VDDA5 D6
VIOS F13

PCI_AD<0> F10 PCI_AD0
PCI_AD<1> G10 PCI_AD1
PCI_AD<2> H10 PCI_AD2
PCI_AD<3> H12 PCI_AD3
PCI_AD<4> J13 PCI_AD4
PCI_AD<5> J12 PCI_AD5
PCI_AD<6> K13 PCI_AD6
PCI_AD<7> K10 PCI_AD7
PCI_AD<8> L12 PCI_AD8
PCI_AD<9> M13 PCI_AD9
PCI_AD<10> L11 PCI_AD10
PCI_AD<11> M12 PCI_AD11
PCI_AD<12> M11 PCI_AD12
PCI_AD<13> N12 PCI_AD13
PCI_AD<14> M10 PCI_AD14
PCI_AD<15> N11 PCI_AD15
PCI_AD<16> M4 PCI_AD16
PCI_AD<17> N5 PCI_AD17
PCI_AD<18> N4 PCI_AD18
M3 PCI_AD19
PCI_AD<19>
PCI_AD<20> M2 PCI_AD20
PCI_AD<21> N3 PCI_AD21
PCI_AD<22> K4 PCI_AD22
PCI_AD<23> M1 PCI_AD23
PCI_AD<24> K2 PCI_AD24
PCI_AD<25> J4 PCI_AD25
PCI_AD<26> K1 PCI_AD26
PCI_AD<27> J2 PCI_AD27
PCI_AD<28> J1 PCI_AD28
PCI_AD<29> H2 PCI_AD29
PCI_AD<30> H4 PCI_AD30
PCI_AD<31> H1 PCI_AD31

PCI_C_BE_L<0> K12 PCI_CBE0*
PCI_C_BE_L<1> M9 PCI_CBE1*
PCI_C_BE_L<2> L3 PCI_CBE2*
PCI_C_BE_L<3> L1 PCI_CBE3*

PCI_PAR N10 PCI_PAR
PCI_FRAME_L N6 PCI_FRAME*
PCI_IRDY_L M6 PCI_IRDY*
PCI_TRDY_L N7 PCI_TRDY*
PCI_DEVSEL_L N8 PCI_DEVSEL*
PCI_STOP_L M7 PCI_STOP*
FW_PCI_IDSEL L2 PCI_IDSEL

R4431 22 5% 1/16W MF-LF 402

PCI_REQ3_L E2 PCI_REQ*
PCI_GNT3_L E1 PCI_GNT*
PCI_PERR_L M8 PCI_PERR*
PCI_SERR_L N9 PCI_SERR*

PCI_CLK_FW G2 PCI_CLK
PM_CLKRUN_L D1 PCI_CLKRUN*

R4432 100 5% 1/16W MF-LF 402

THIS IS FROM ICH-7M
PCI_RST_L
FW_PCI_RST_L F1 PCI_RST*
INT_PIRQD_L D2 PCI_INTA*
PCI_PME_FW_L F2 PCI_PME*

VSS0 A1, VSS1 B2, VSS2 C3, VSS3 D4, VSS4 E4, VSS5 E5, VSS6 F4, VSS7 F6, VSS8 F7, VSS9 F8, VSS10 G1, VSS11 G6, VSS12 G7, VSS13 G8, VSS14 H6, VSS15 H7, VSS16 H8, VSS17 J5, VSS18 J9, VSS19 J10, VSS20 K8, VSS21 K9, VSS22 N13
VSSA0 E13, VSSA1 E9, VSSA2 D9, VSSA3 D7, VSSA4 D5

XW4400 SM

GND_FW_VSSA 40

197S0178 3.2MMX2.5MM CRITICAL
Y4403 SM-3.2X2.5MM 24.576MHZ
R4400 300 5% 1/16W MF-LF 402
FW_XO_R
C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402
NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI A5 FW_XI
XO B5 FW_XO
RESET* B4 FW_PWRON_RST_L
R1 A6 FW_R1
R0 B7 FW_R0

SPEC RECOMMENDS 2.49K

R4452 2.49K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

TPBIAS0 B8 FW_A_TPBIAS
TPA0_P A9 FW_A_TPA_P
TPA0_N B9 FW_A_TPA_N
TPB0_P B10 FW_A_TPB_P
TPB0_N A10 FW_A_TPB_N
TPBIAS1 D8 FW_B_TPBIAS
TPA1_P A11 FW_B_TPA_P
TPA1_N B11 FW_B_TPA_N
TPB1_P B12 FW_B_TPB_P
TPB1_N A12 FW_B_TPB_N
TPBIAS2 C13 FW_C_TPBIAS
TPA2_P C11 FW_C_TPA_P
TPA2_N C12 FW_C_TPA_N
TPB2_P D13 FW_C_TPB_P
TPB2_N D12 FW_C_TPB_N

(all BI, 42)

MODE_420 M5
MODE_A B6
MODE FOR EXTERNAL LINK

PC0 E12 FW_PC0 BI
DUAL PORT DEVICES ARE POWER CLASS 4 (’100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (’000’)
PC1 F13
PC2 F12
CONTENDER G12 LOW = NOT BUS MANAGER
CARDBUSN B1 LOW = PCI OPERATION
MPCI_ACTN_323 E10

MANUFACTURING TEST PINS
TEST0 C2
TEST1 C1
TEST2 A4
SE A3
SM B3

FIREWIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 44 OF 104	

Page Notes

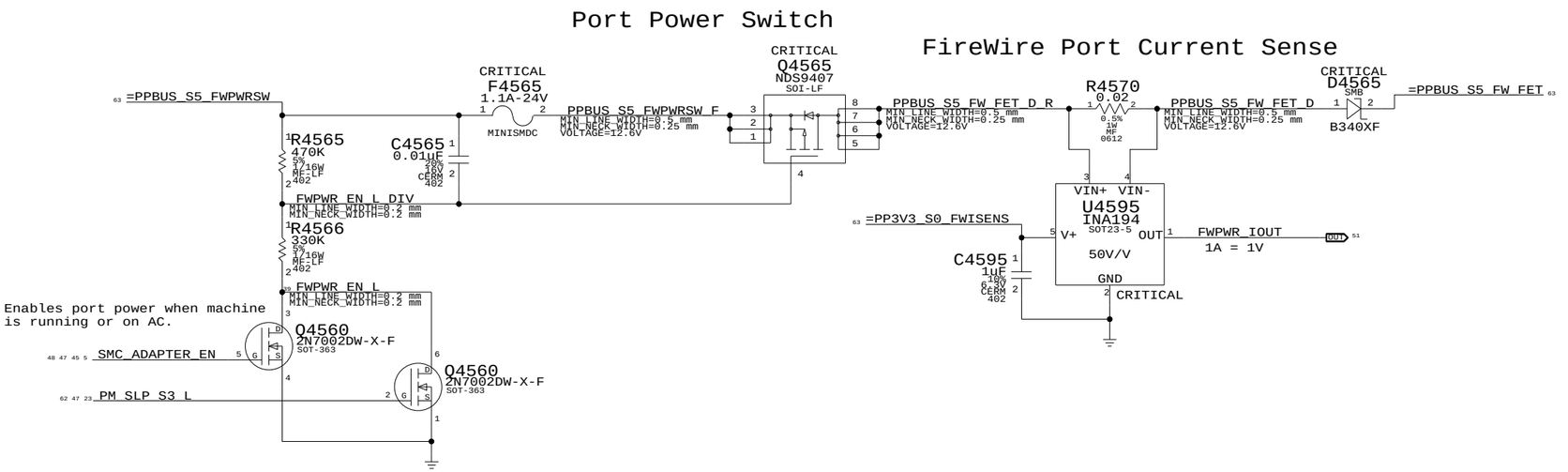
Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	45	104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 42
	FW	FW_110D	FW_PORT1_TPA_FL_N 42
	FW	FW_110D	FW_PORT1_TPB_FL_P 42
	FW	FW_110D	FW_PORT1_TPB_FL_N 42

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

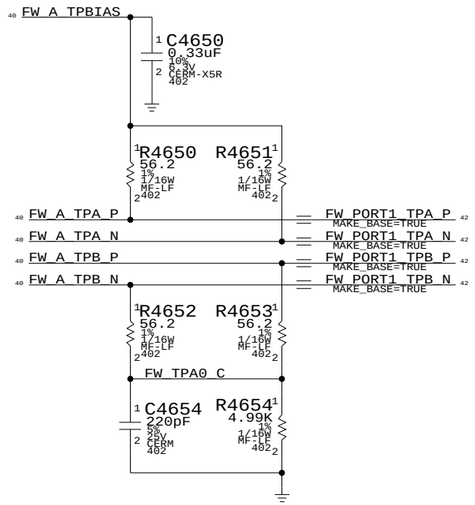
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

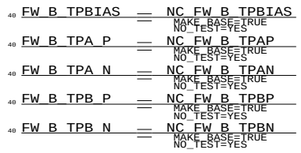
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

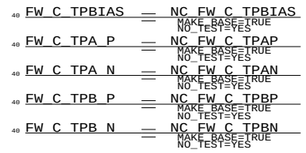
Place close to FireWire PHY



2nd TPA/TPB pair unused

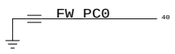


3rd TPA/TPB pair unused

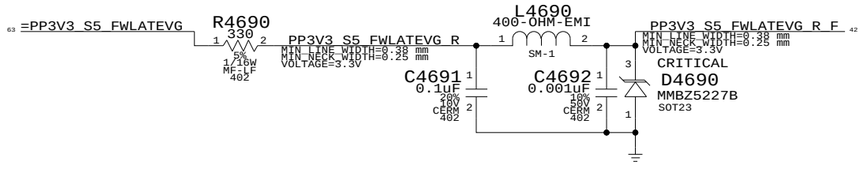


FW Power Class Strap

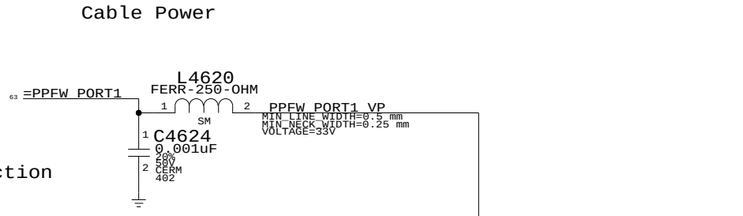
Single-port system sets PC=0



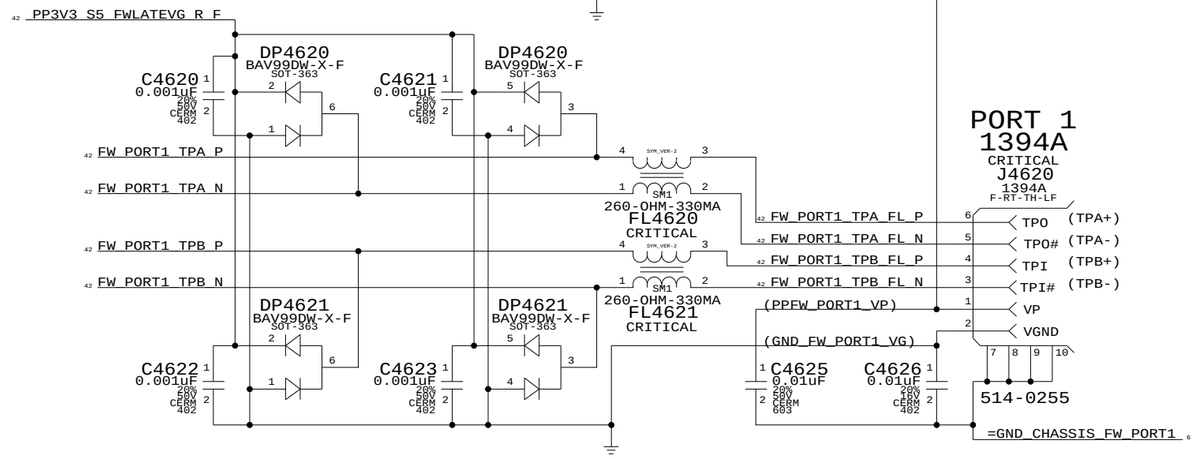
Late-VG Protection Power

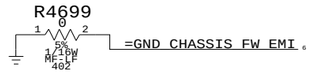


Cable Power



"Snapback" & "Late VG" Protection





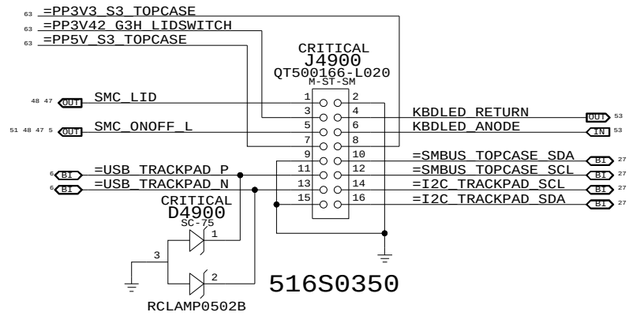
FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

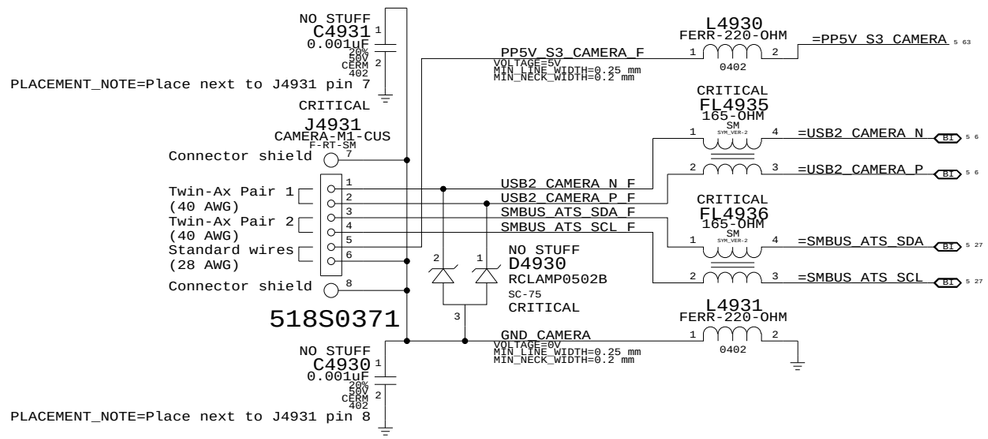
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT: 46 OF: 104	

Top-Case Connector



Camera Connector



Internal USB Connections

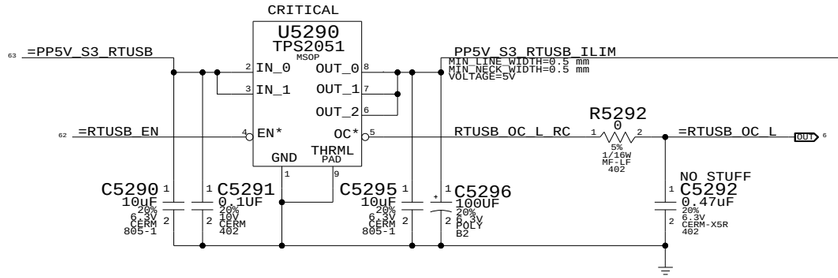
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

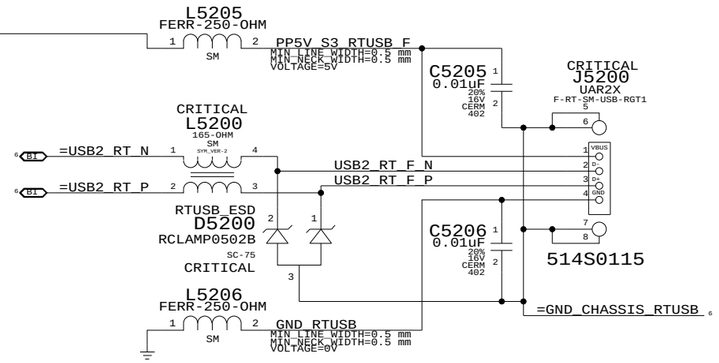
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	49	104

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

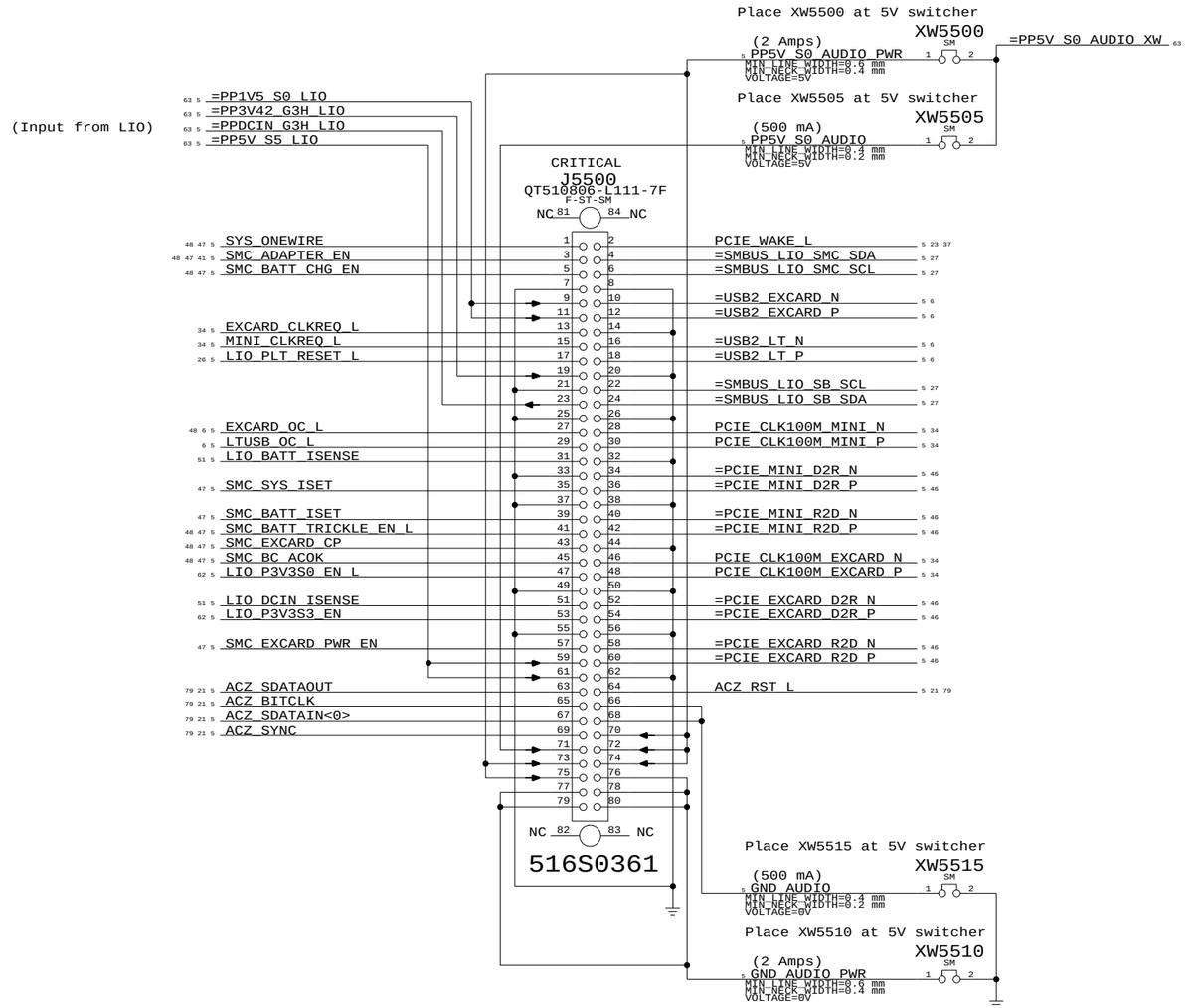
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	52	104

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	55	104

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

45 5	=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P (MAKE_BASE=TRUE)	PCIE_B_R2D_C_P	22
45 5	=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N (MAKE_BASE=TRUE)	PCIE_B_R2D_C_N	22
45 5	=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P (MAKE_BASE=TRUE)	PCIE_B_D2R_P	22
45 5	=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N (MAKE_BASE=TRUE)	PCIE_B_D2R_N	22

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

45 5	=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE)	PCIE_C_R2D_C_P	22
45 5	=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE)	PCIE_C_R2D_C_N	22
45 5	=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE)	PCIE_C_D2R_P	22
45 5	=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE)	PCIE_C_D2R_N	22

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP (MAKE_BASE=TRUE)	PCIE_D_R2D_C_P	22
TP_PCIE_D_R2DN (MAKE_BASE=TRUE)	PCIE_D_R2D_C_N	22
TP_PCIE_D_D2RP (MAKE_BASE=TRUE)	PCIE_D_D2R_P	22
TP_PCIE_D_D2RN (MAKE_BASE=TRUE)	PCIE_D_D2R_N	22

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP (MAKE_BASE=TRUE)	PCIE_E_R2D_C_P	22
TP_PCIE_E_R2DN (MAKE_BASE=TRUE)	PCIE_E_R2D_C_N	22
TP_PCIE_E_D2RP (MAKE_BASE=TRUE)	PCIE_E_D2R_P	22
TP_PCIE_E_D2RN (MAKE_BASE=TRUE)	PCIE_E_D2R_N	22

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP (MAKE_BASE=TRUE)	PCIE_F_R2D_C_P	22
TP_PCIE_F_R2DN (MAKE_BASE=TRUE)	PCIE_F_R2D_C_N	22
TP_PCIE_F_D2RP (MAKE_BASE=TRUE)	PCIE_F_D2R_P	22
TP_PCIE_F_D2RN (MAKE_BASE=TRUE)	PCIE_F_D2R_N	22

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	57	104

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
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PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	SMC_PM_G2_EN		
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	SMC_ADAPTER_EN		
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	SPI_ARB		
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	SPI_SCLK		
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	SPI_SI		
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	SPI_SO		
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L		
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT_3_3_L		
SMC_P20	D13	P20	P70/AN0	N12	SMC_CPU_ISENSE		
SMC_P21	D14	P21	P71/AN1	R13	SMC_CPU_VSENSE		
SMC_P22	D15	P22	P72/AN2	P13	SMC_GPU_ISENSE		
SMC_P23	E12	P23	P73/AN3	R14	SMC_GPU_VSENSE		
SMC_BATT_TRICKLE_EN	E14	P24	P74/AN4	P14	SMC_DCIN_ISENSE		
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	SMC_PBUS_VSENSE		
SMC_P26	E13	P26	P76/AN6	N13	SMC_BATT_ISENSE		
SMC_P27	F14	P27	P77/AN7	P15	SMC_FWIRE_ISENSE		
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	SMC_WAKE_SCI_L		
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	SMC_TPM_GPIO		
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	PM_CLKRUN_L		
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	PM_SUS_STAT_L		
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	SC_TX_L		
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	SC_RX_L		
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK		
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	SMC_ONOFF_L		
SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2	SMC_BC_ACOK		
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	SMC_BS_ALRT_L		
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	PM_SLP_S3_L		
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	PM_SLP_S4_L		
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	PM_SLP_S5_L		
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	SMC_SUS_CLK		
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	SMB_0_S0_DATA		
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1					
SMC_TX_L	G1	P50					
SMC_RX_L	G4	P51					
SMB_0_S0_CLK	F2	P52/SCL0					

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SMC_H8S2116
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SMC_RCIN_L	R3	PA0/KIN8*/PA2PC	PE0	M3	SMC_CASE_OPEN		
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	SMC_TCK		
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC_TDI		
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC_TDO		
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC_TMS		
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0		
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1		
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	SMC_LID		
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L		
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	SMC_BATT_ISET		
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	SMC_BATT_VSET		
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	SMC_SYS_ISET		
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	SMC_SYS_VSET		
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	SPI_CE_L		
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3		
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	SMB_BSA_DATA		
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	SMB_BSA_CLK		
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	SMB_A_S3_DATA		
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	SMB_A_S3_CLK		
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	SMB_B_S0_DATA		
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	SMB_B_S0_CLK		
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	SMC_PROCHOT		
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	SMC_THRMTRIP		
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	SMC_FWE		
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	ALS_GAIN		
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	SMS_INT_L		
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	SMS_ONOFF_L		
SMC_ANALOG_ID	N11	PD3/AN11					
SMC_NB_ISENSE	P10	PD4/AN12					
SMC_MEM_ISENSE	R10	PD5/AN13					
ALS_LEFT	N10	PD6/AN14					
ALS_RIGHT	M10	PD7/AN15					

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SMC_H8S2116
BGA
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G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

=PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL

C5807 0.47UF 20% 6.3V CERM-X5R 402

VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

=PP3V3_S5_SMC

R5899 4.7 5% 1/10W MF-LF 402

PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25
MIN_NECK_WIDTH=0.20

C5820 0.1UF 20% 10V CERM 402

PP3V3_AVREF_SMC

=PP3V3_S5_SMC

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402

GND_SMC_AVSS

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BGA
(3 OF 4)

SMC_RST_L
SMC_XTAL
SMC_EXTAL

KBC_MDE

SMC_MD1
SMC_NMI
SMC_TRST_L

R5898 10K 5% 1/16W MF-LF 402
R5803 10K 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
NOSTUFF

XW5800
SM

GND_SMC_AVSS

SMC

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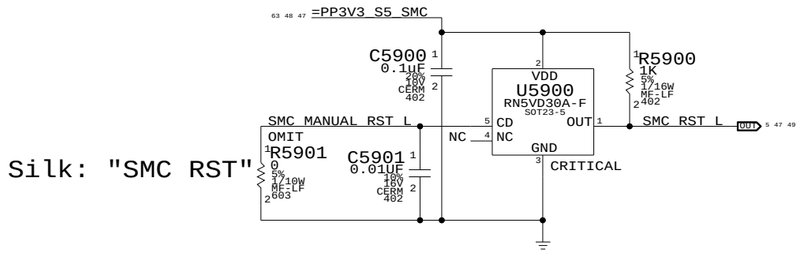
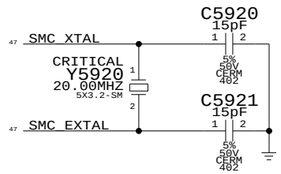
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 58 OF 104	

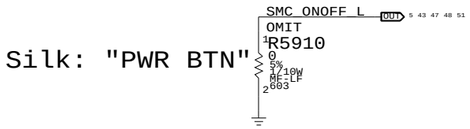
SMC Reset Button / Brownout Detect



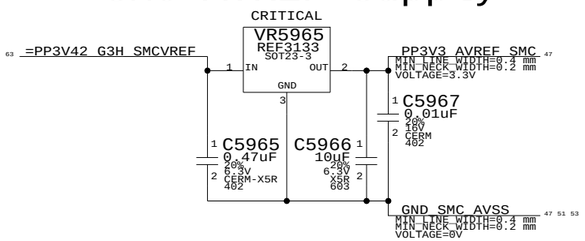
SMC Crystal Circuit



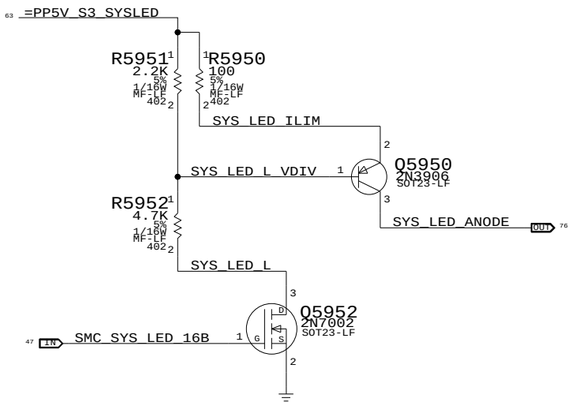
Debug Power Button



SMC AVREF Supply



System (Sleep) LED Circuit



SMC_CPU_INIT_3_3_L

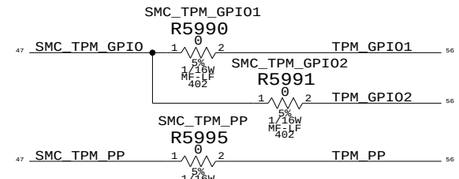
SMC_CPU_INIT_3_3_L — FWH_INIT_L (5 21 49)
MAKE_BASE=TRUE

SMC_NB_ISENSE (47) — SMC_P1V05S0_ISENSE (51)
SMC_MEM_ISENSE (47) — SMC_P1V8S3_ISENSE (51)
PM_EXTTS_L (47 14) — DIMM_OVERTEMP_L (28 29)

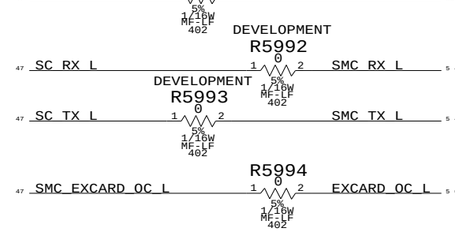
SMC_SYS_LED — TP_SMC_SYS_LED
SMC_ANALOG_ID — TP_SMC_ANALOG_ID
SMC_BATT_VSET — TP_SMC_BATT_VSET
SMC_SYS_VSET — TP_SMC_SYS_VSET
SMC_FAN_2_CTL — TP_SMC_FAN_2_CTL
SMC_FAN_2_TACH — TP_SMC_FAN_2_TACH
SMC_FAN_3_CTL — TP_SMC_FAN_3_CTL
SMC_FAN_3_TACH — TP_SMC_FAN_3_TACH
SMC_XDP_TCK — TP_SMC_XDP_TCK
SMC_XDP_TDO_L — TP_SMC_XDP_TDO_L
SMC_XDP_TMS — TP_SMC_XDP_TMS
SMC_XDP_TRST_L — TP_SMC_XDP_TRST_L
SMC_P20 — TP_SMC_P20
SMC_P21 — TP_SMC_P21
SMC_P22 — TP_SMC_P22
SMC_P23 — TP_SMC_P23
SMC_P26 — TP_SMC_P26
SMC_P27 — TP_SMC_P27
SMC_PF0 — TP_SMC_PF0
SMC_PF1 — TP_SMC_PF1

(all MAKE_BASE=TRUE)

SMC_TPM_GPIO1

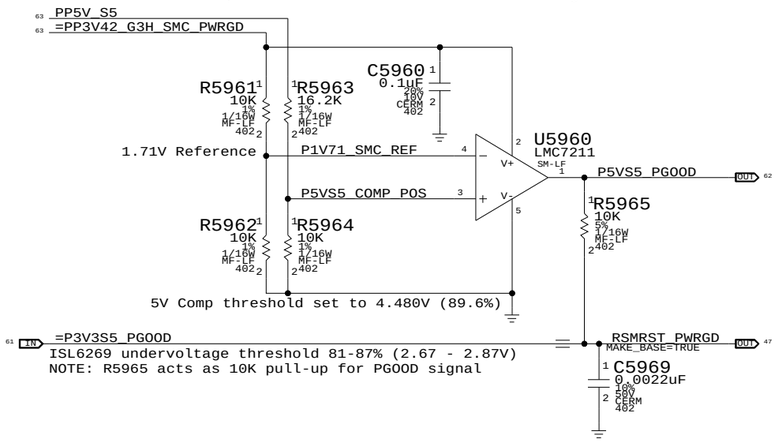


SMC_TPM_PP

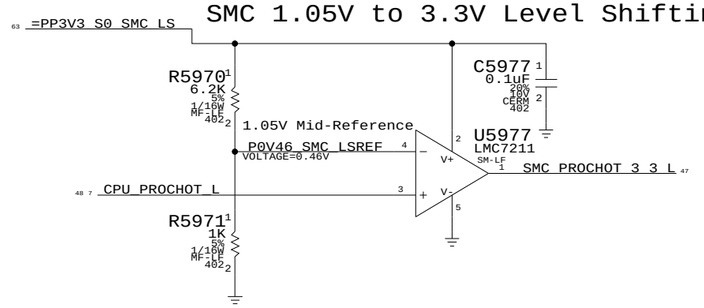


SMC PWRGD Circuit

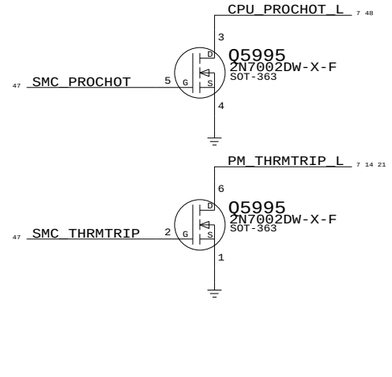
Reports when 5V S5 and 3.3V S5 are in regulation



SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



SMC_XXX_3_3 Pull-ups

63 48 47 =PP3V3_S5_SMC
63 56 =PP3V3_S3_TPM
63 55 =PP3V3_S3_SMS

47 23 SMS_INT_L	R5930	10K	5% 1/16W MF-LF 402
56 47 SMC_TPM_RESET_L	R5931	10K	5% 1/16W MF-LF 402
51 48 47 43 5 SMC_ONOFF_L	R5932	10K	5% 1/16W MF-LF 402
47 43 SMC_LID	R5933	100K	5% 1/16W MF-LF 402
47 SMC_FWE	R5934	10K	5% 1/16W MF-LF 402
49 48 47 5 SMC_TX_L	R5935	10K	5% 1/16W MF-LF 402
49 48 47 5 SMC_RX_L	R5936	100K	5% 1/16W MF-LF 402
47 45 5 SYS_ONEWIRE	R5937	2.0K	5% 1/16W MF-LF 402
64 47 5 SMC_BS_ALRT_L	R5938	100K	5% 1/16W MF-LF 402
49 47 5 SMC_TMS	R5939	10K	5% 1/16W MF-LF 402
49 47 5 SMC_TDO	R5940	10K	5% 1/16W MF-LF 402
49 47 5 SMC_TDI	R5941	10K	5% 1/16W MF-LF 402
49 47 5 SMC_TCK	R5942	10K	5% 1/16W MF-LF 402
47 SMC_CPU_RESET_3_3_L	R5980	10K	5% 1/16W MF-LF 402
47 SMC_XDP_TCK_3_3	R5981	10K	5% 1/16W MF-LF 402
47 SMC_XDP_TDO_3_3	R5982	10K	5% 1/16W MF-LF 402
47 45 5 SMC_BATT_TRICKLE_EN_L	R5943	10K	5% 1/16W MF-LF 402
47 45 5 SMC_BATT_CHG_EN	R5944	10K	5% 1/16W MF-LF 402
47 45 41 5 SMC_ADAPTER_EN	R5945	10K	5% 1/16W MF-LF 402
47 SMC_CASE_OPEN	R5946	10K	5% 1/16W MF-LF 402
47 45 5 SMC_BC_ACOK	R5947	470K	5% 1/16W MF-LF 402
47 45 5 SMC_EXCARD_CP	R5948	10K	5% 1/16W MF-LF 402
56 49 47 23 5 PM_SUS_STAT_L	R5983	100K	5% 1/16W MF-LF 402
47 23 PM_SLP_S5_L	R5984	100K	5% 1/16W MF-LF 402

SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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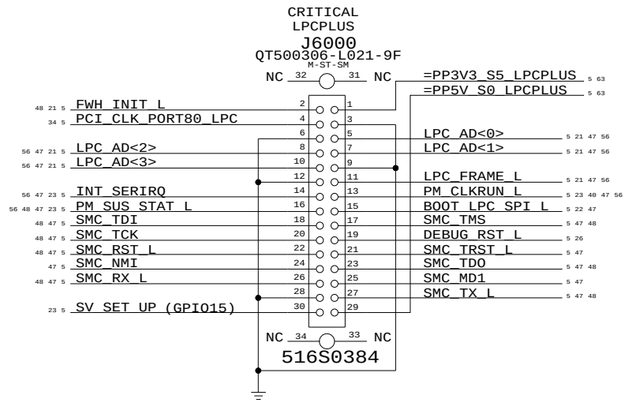
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 59 OF 104	



LPC+ Debug Connector

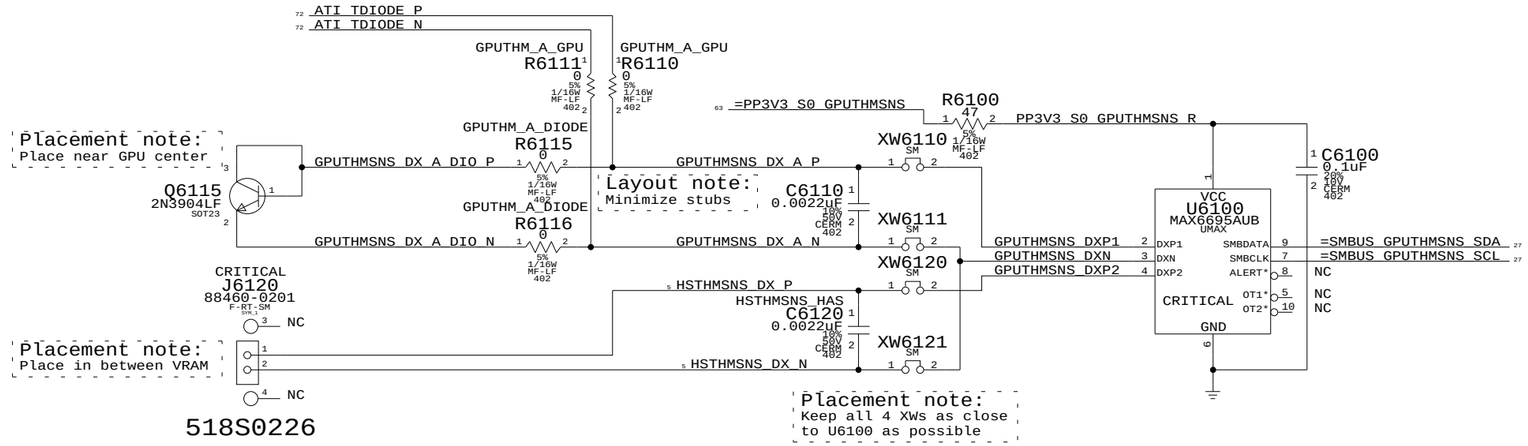
SYNC_MASTER=M42 SYNC_DATE=07/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

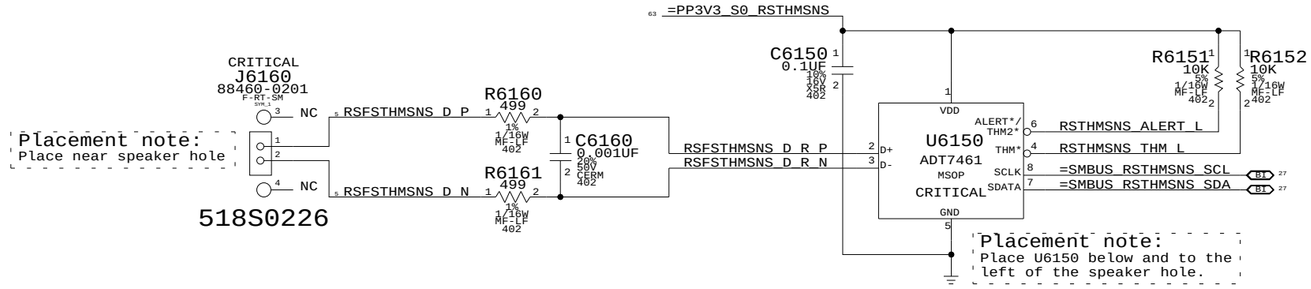
SCALE	SHT	OF
NONE	60	104

GPU / Heat Pipe Thermal Sensor

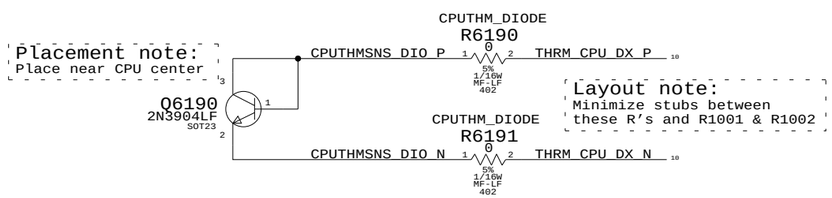


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

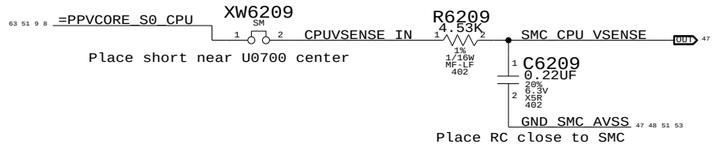
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

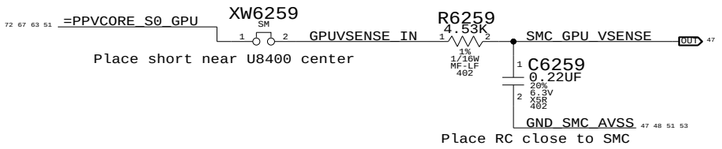
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	61	104

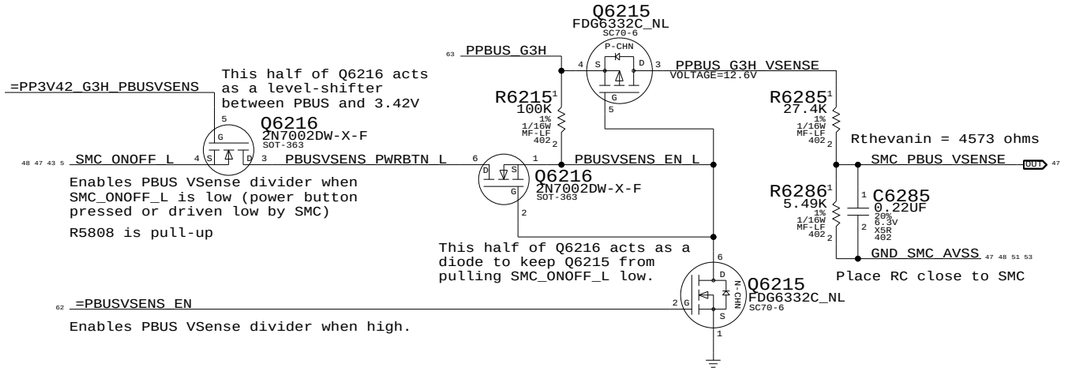
CPU Voltage Sense / Filter



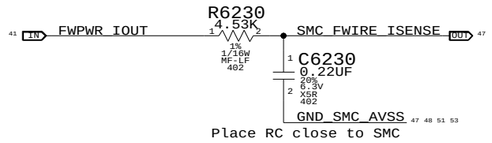
GPU Voltage Sense / Filter



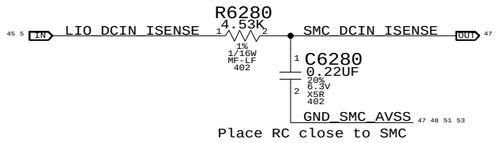
PBUS Voltage Sense Enable & Filter



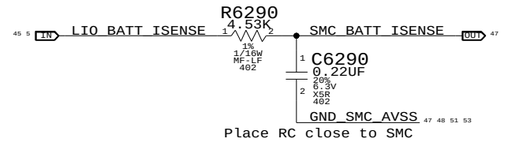
FireWire Current Sense Filter



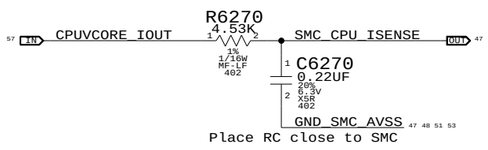
DCIN Current Sense Filter



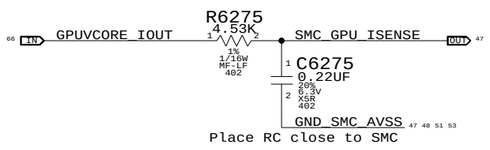
Battery Current Sense Filter



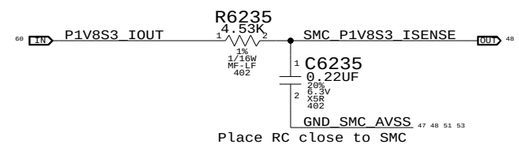
CPU Current Sense Filter



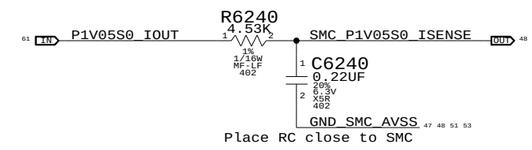
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

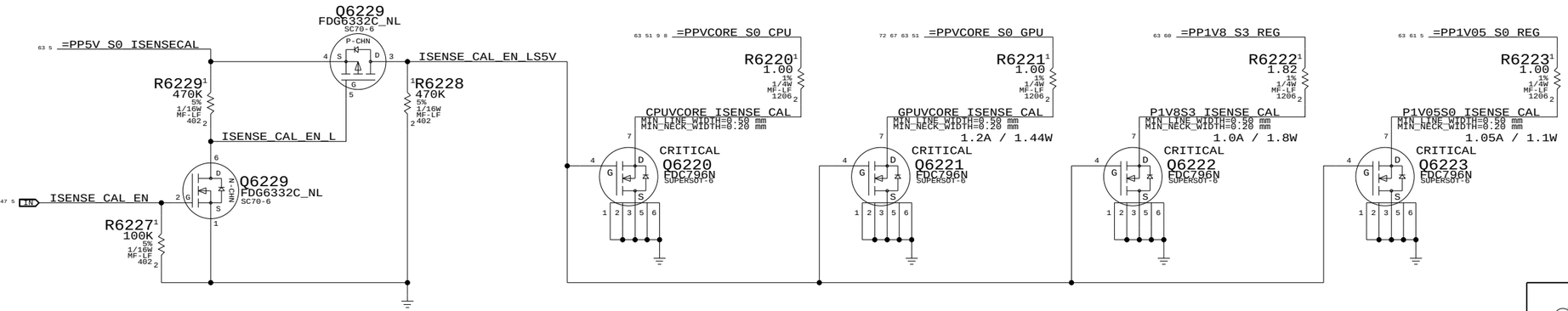


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
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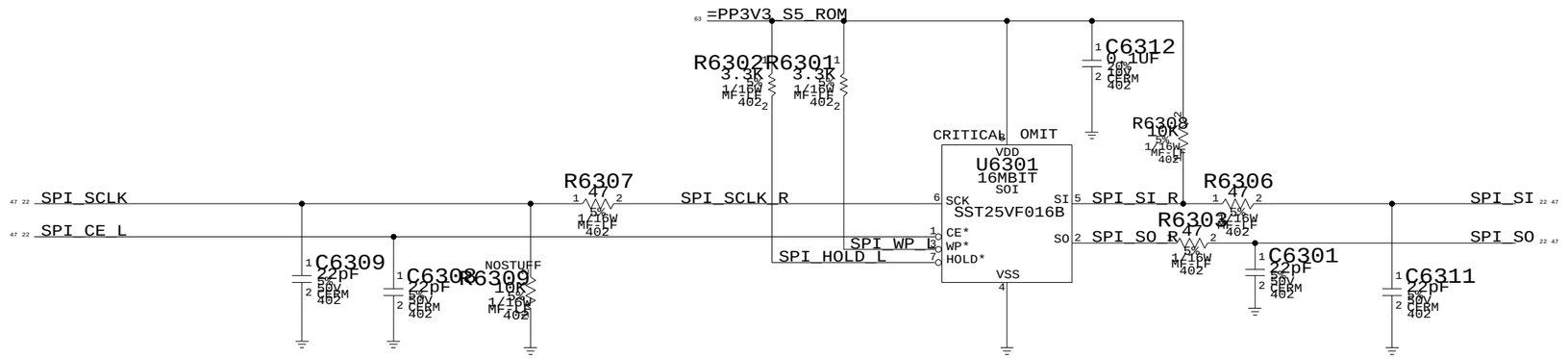
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 12
	SCALE NONE	SHT 62 OF 104	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

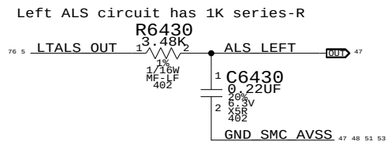
SYNC_MASTER=MAY SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

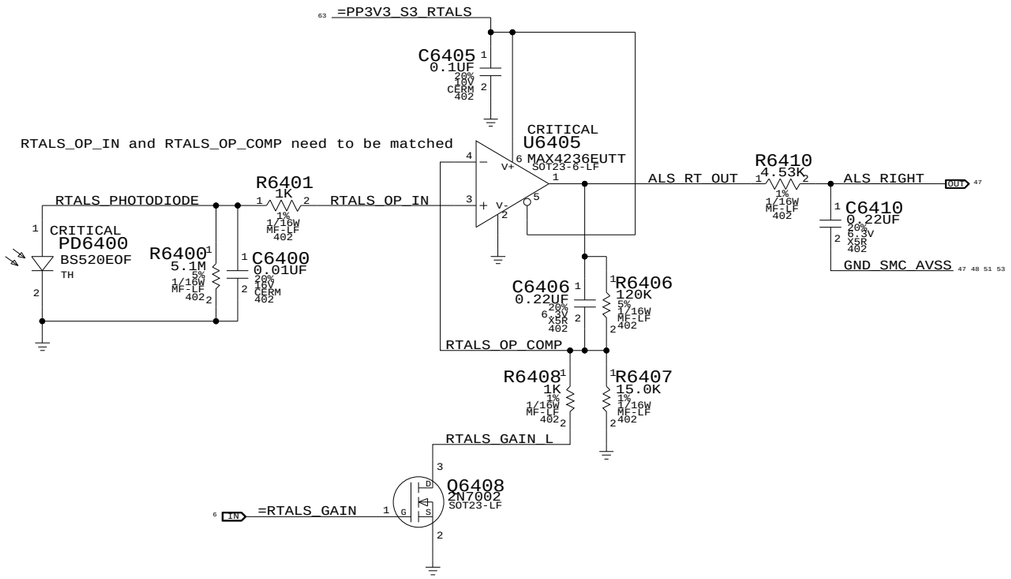
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	63	104

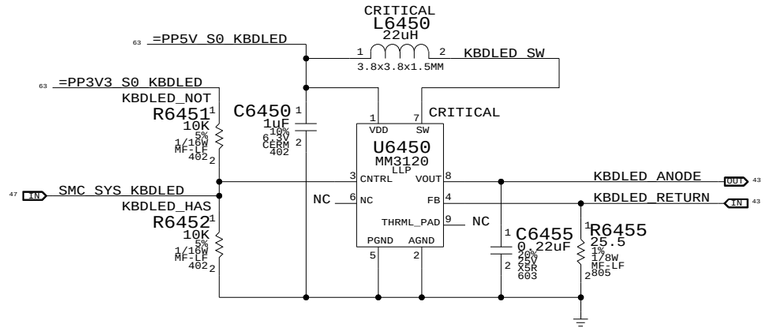
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



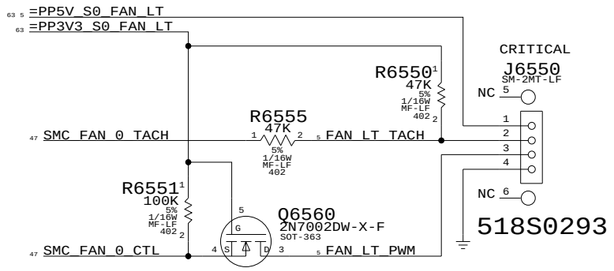
ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

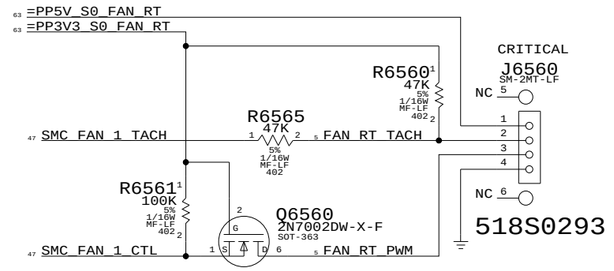
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 64 OF 104	

Left Fan



Right Fan



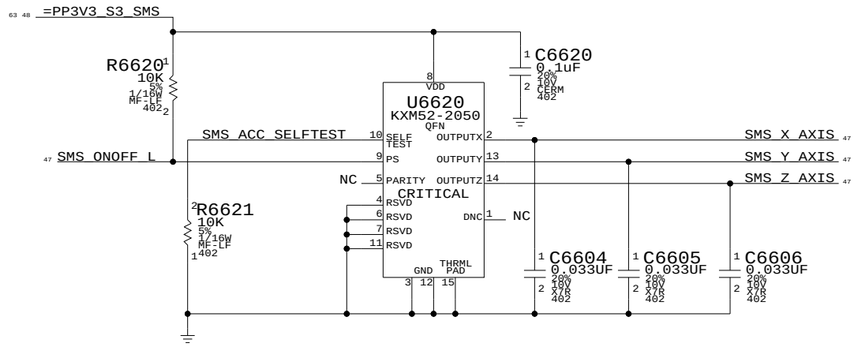
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

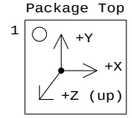
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	65	104



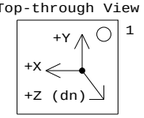
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

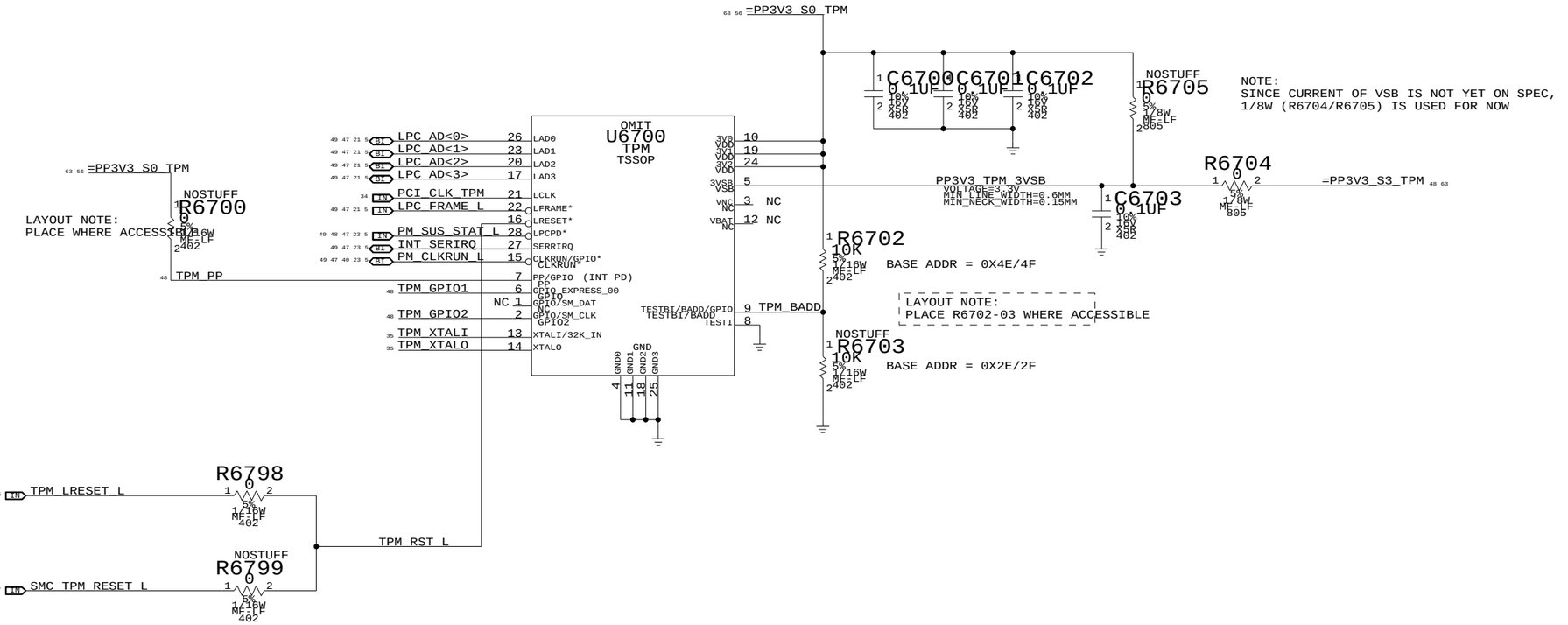
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE: NONE

SHT 66 OF 104



TPM

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	67	104

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

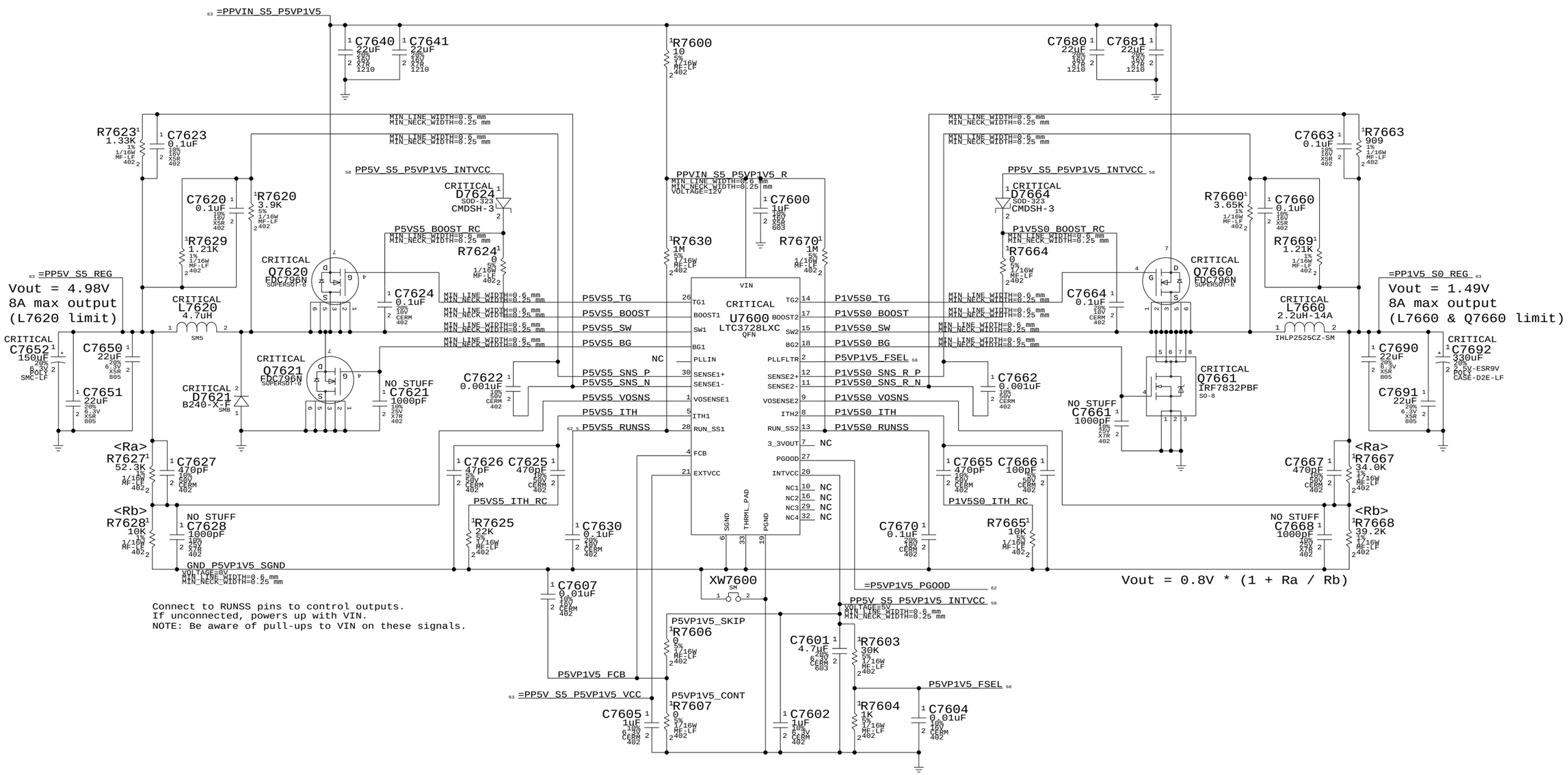
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 75 OF 104	



5V / 1.5V Power Supply

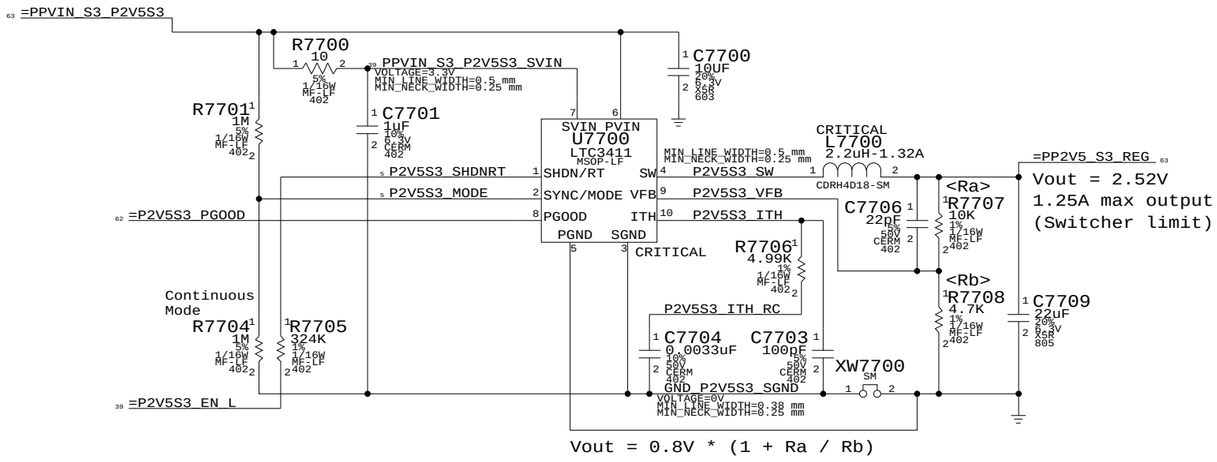
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

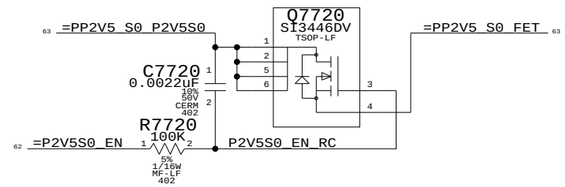
SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	76	104

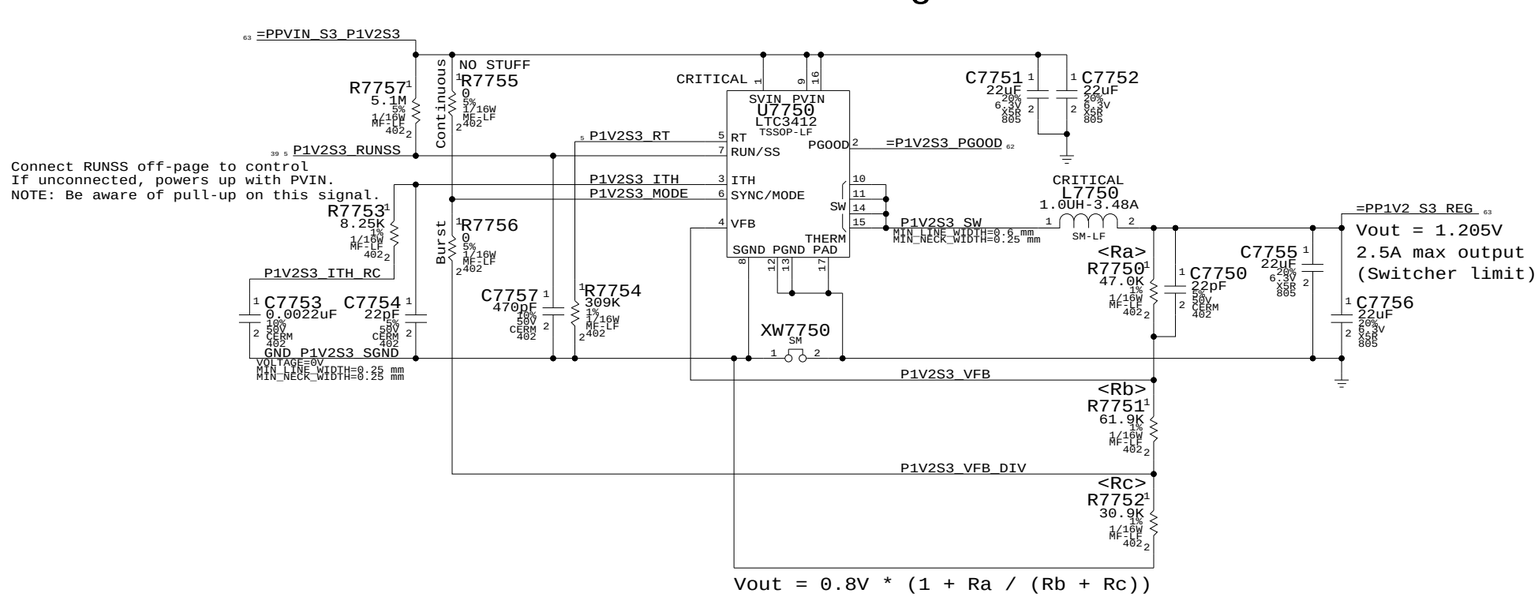
2.5V S3 Regulator



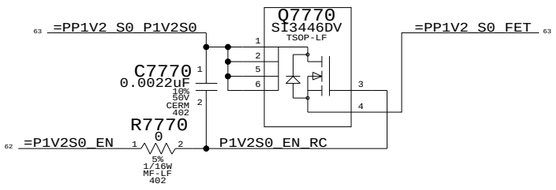
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



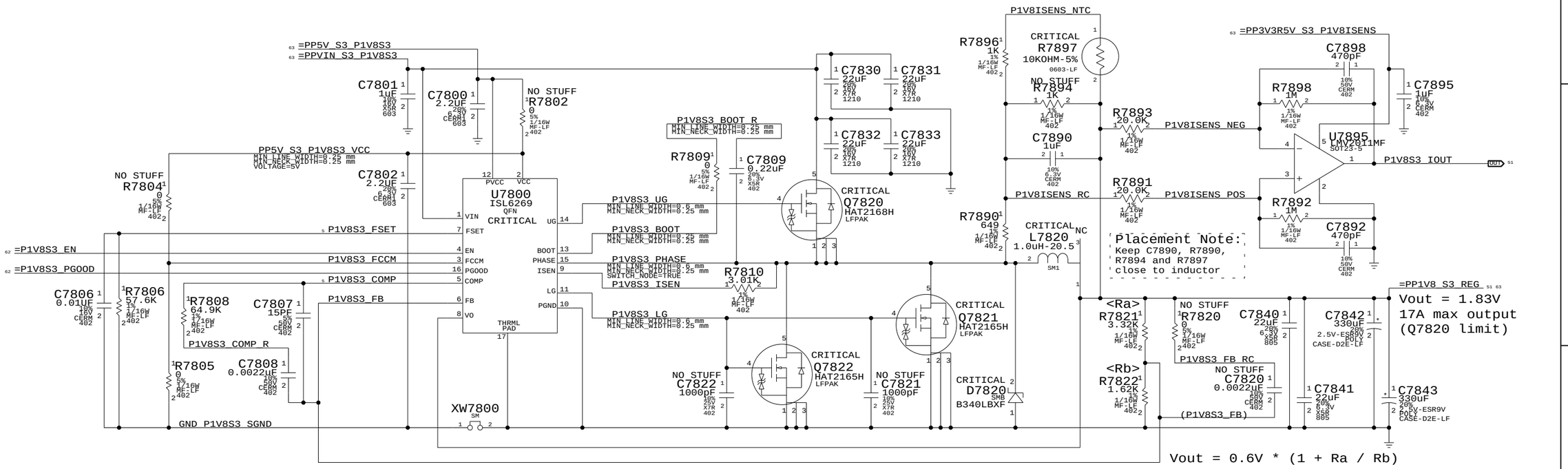
2.5V & 1.2V Regulators

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

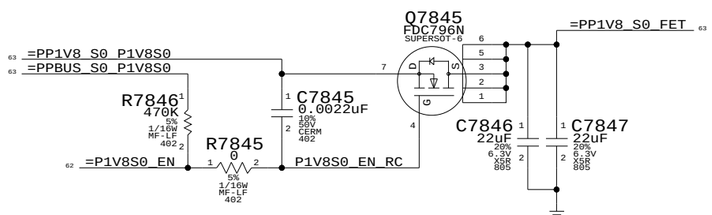
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 77 OF 104	

1.8V S3 Current Sense



1.8V S0 FET



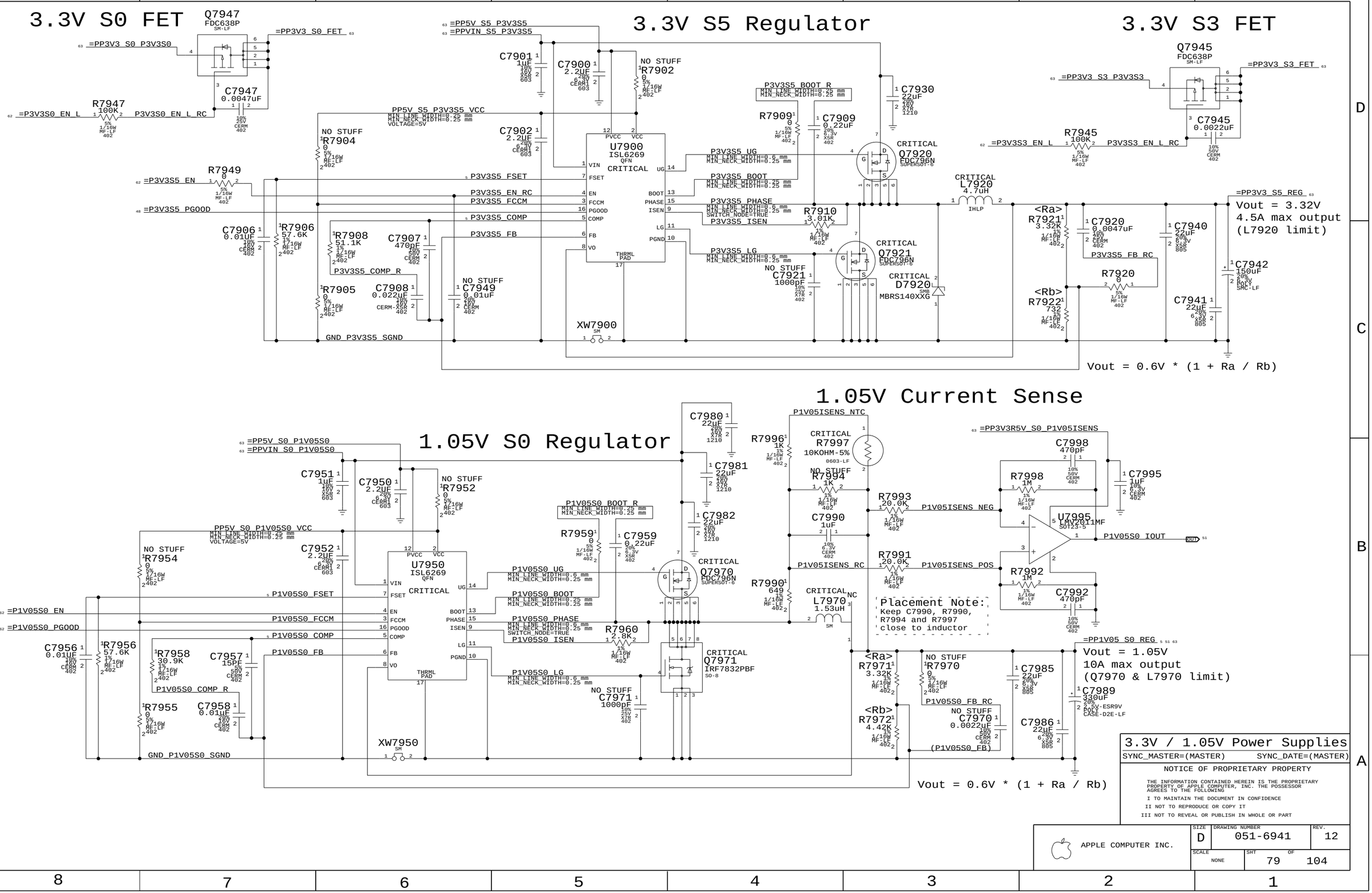
1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	78	104


3.3V S0 FET
Q7947
FDC638P
SM-LF
=PP3V3_S0_FET
=PP3V3_S0_P3V3S0
C7947
0.0047uF
R7947
100K
=P3V3S0_EN_L
P3V3S0_EN_L_RC
3.3V S5 Regulator
=PP5V_S5_P3V3S5
=PPVIN_S5_P3V3S5
C7901
1uF
C7900
2.2uF
NO STUFF
R7902
0
P3V3S5_BOOT_R
R7909
0
C7909
0.22uF
C7930
22uF
PP5V_S5_P3V3S5_VCC
C7902
2.2uF
NO STUFF
R7904
0
U7900
ISL6269
QFN
CRITICAL
P3V3S5_UG
P3V3S5_BOOT
P3V3S5_PHASE
P3V3S5_ISEN
P3V3S5_LG
CRITICAL
Q7920
FDC796N
SUPERSOT-6
CRITICAL
L7920
4.7uH
IHLP
R7949
0
=P3V3S5_EN
=P3V3S5_PGOOD
P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
P3V3S5_COMP
P3V3S5_FB
C7906
0.01UF
R7906
57.6K
R7908
51.1K
C7907
470pF
P3V3S5_COMP_R
R7905
0
C7908
0.022uF
NO STUFF
C7949
0.01uF
GND_P3V3S5_SGND
XW7900
SM
R7910
3.01K
NO STUFF
C7921
1000pF
CRITICAL
Q7921
FDC796N
SUPERSOT-6
CRITICAL
D7920
SMB
MBRS140XXG
=PP3V3_S5_REG
Vout = 3.32V
4.5A max output
(L7920 limit)
<Ra>
R7921
3.32K
C7920
0.0047uF
P3V3S5_FB_RC
R7920
0
<Rb>
R7922
732
C7940
22uF
C7941
22uF
C7942
150uF
Vout = 0.6V * (1 + Ra / Rb)
3.3V S3 FET
Q7945
FDC638P
SM-LF
=PP3V3_S3_FET
=PP3V3_S3_P3V3S3
C7945
0.0022uF
R7945
100K
=P3V3S3_EN_L
P3V3S3_EN_L_RC
1.05V Current Sense
P1V05ISENS_NTC
R7996
1K
CRITICAL
R7997
10KOHM-5%
0603-LF
NO STUFF
R7994
1K
R7993
20.0K
P1V05ISENS_NEG
C7990
1uF
R7991
20.0K
P1V05ISENS_RC
P1V05ISENS_POS
R7990
649
CRITICAL
L7970
1.53uH
NC
Placement Note:
Keep C7990, R7990,
R7994 and R7997
close to inductor
=PP3V3R5V_S0_P1V05ISENS
C7998
470pF
R7998
1M
C7995
1uF
U7995
LMV211MF
SOT23-5
P1V05S0_IOUT
R7992
1M
C7992
470pF
1.05V S0 Regulator
=PP5V_S0_P1V05S0
=PPVIN_S0_P1V05S0
C7951
1uF
C7950
2.2uF
NO STUFF
R7952
0
C7980
22uF
C7981
22uF
C7982
22uF
P1V05S0_BOOT_R
R7959
0
C7959
0.22uF
PP5V_S0_P1V05S0_VCC
C7952
2.2uF
NO STUFF
R7954
0
U7950
ISL6269
QFN
CRITICAL
P1V05S0_UG
P1V05S0_BOOT
P1V05S0_PHASE
P1V05S0_ISEN
P1V05S0_LG
CRITICAL
Q7970
FDC796N
SUPERSOT-6
R7960
2.8K
CRITICAL
Q7971
IRF7832PBF
SO-8
NO STUFF
C7971
1000pF
=P1V05S0_EN
=P1V05S0_PGOOD
P1V05S0_FSET
P1V05S0_FCCM
P1V05S0_COMP
P1V05S0_FB
C7956
0.01UF
R7956
57.6K
R7958
30.9K
C7957
15PF
P1V05S0_COMP_R
R7955
0
C7958
0.01uF
GND_P1V05S0_SGND
XW7950
SM
<Ra>
R7971
3.32K
NO STUFF
R7970
0
P1V05S0_FB_RC
<Rb>
R7972
4.42K
NO STUFF
C7970
0.0022uF
(P1V05S0_FB)
C7985
22uF
C7986
22uF
=PP1V05_S0_REG
Vout = 1.05V
10A max output
(Q7970 & L7970 limit)
C7989
330uF
Vout = 0.6V * (1 + Ra / Rb)
3.3V / 1.05V Power Supplies
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
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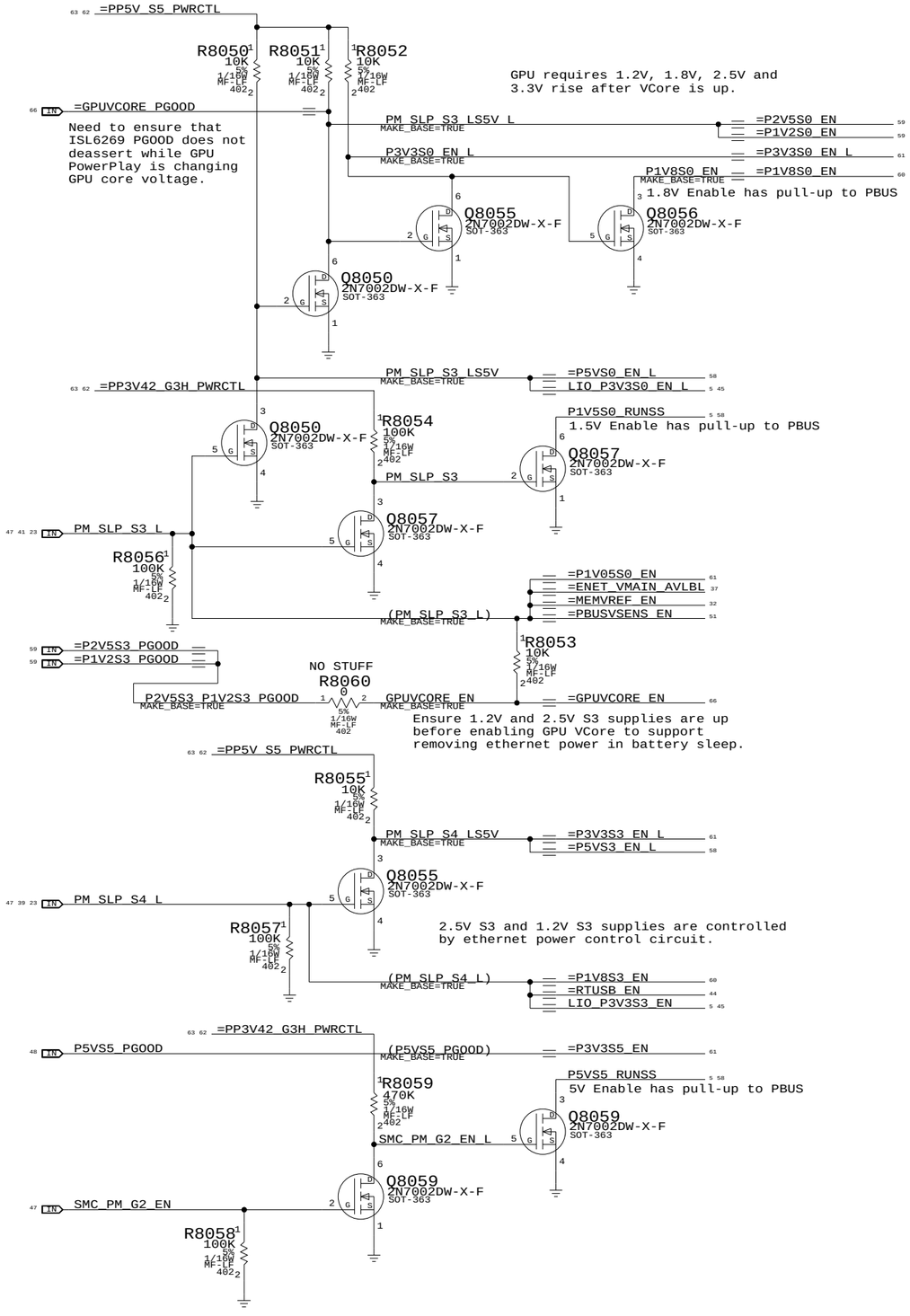
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 12
SCALE NONE
SHT 79 OF 104

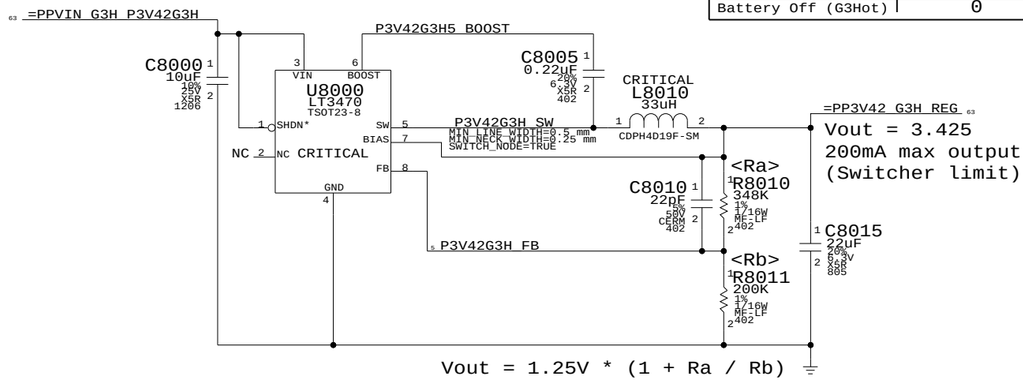
Power Control Signals



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.425V "G3Hot" Supply

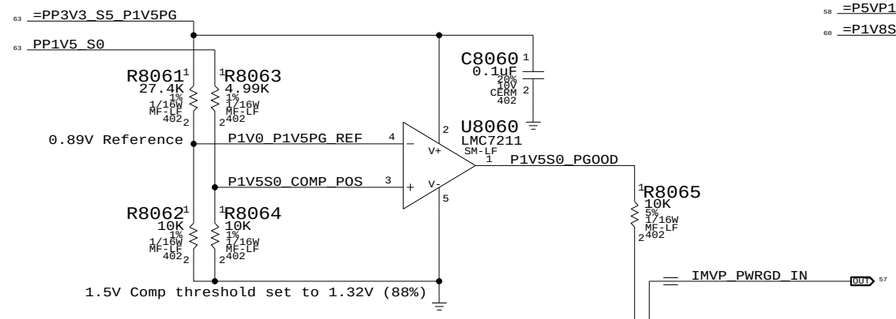
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



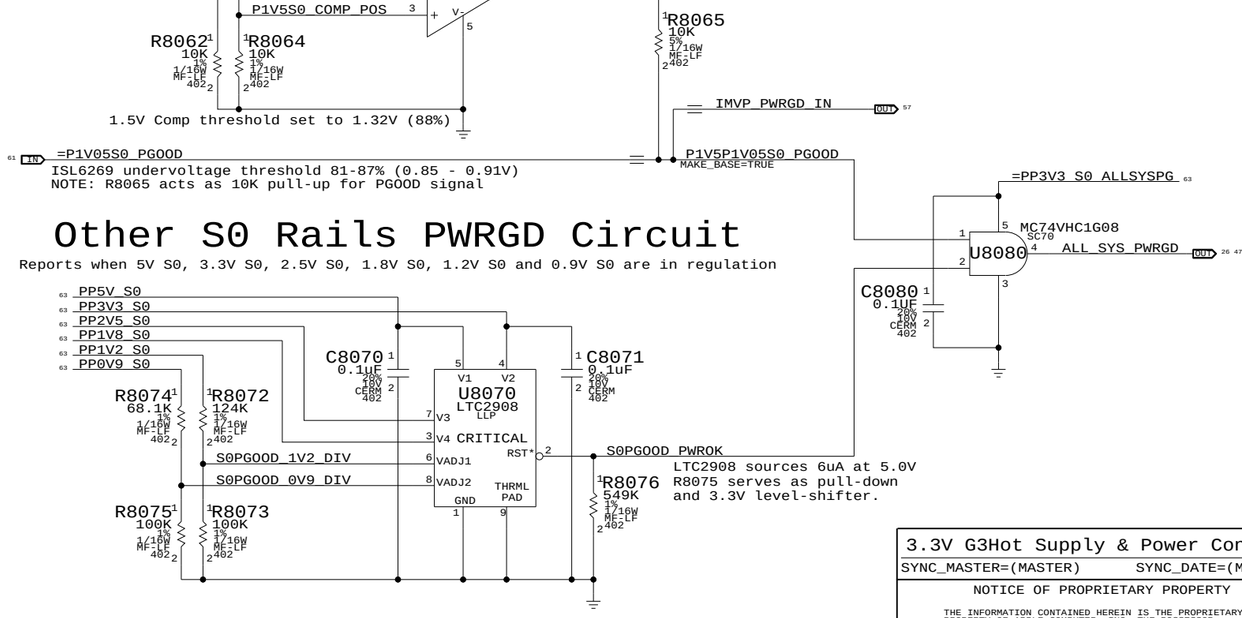
Unused PGOOD Signals

=P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

=P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

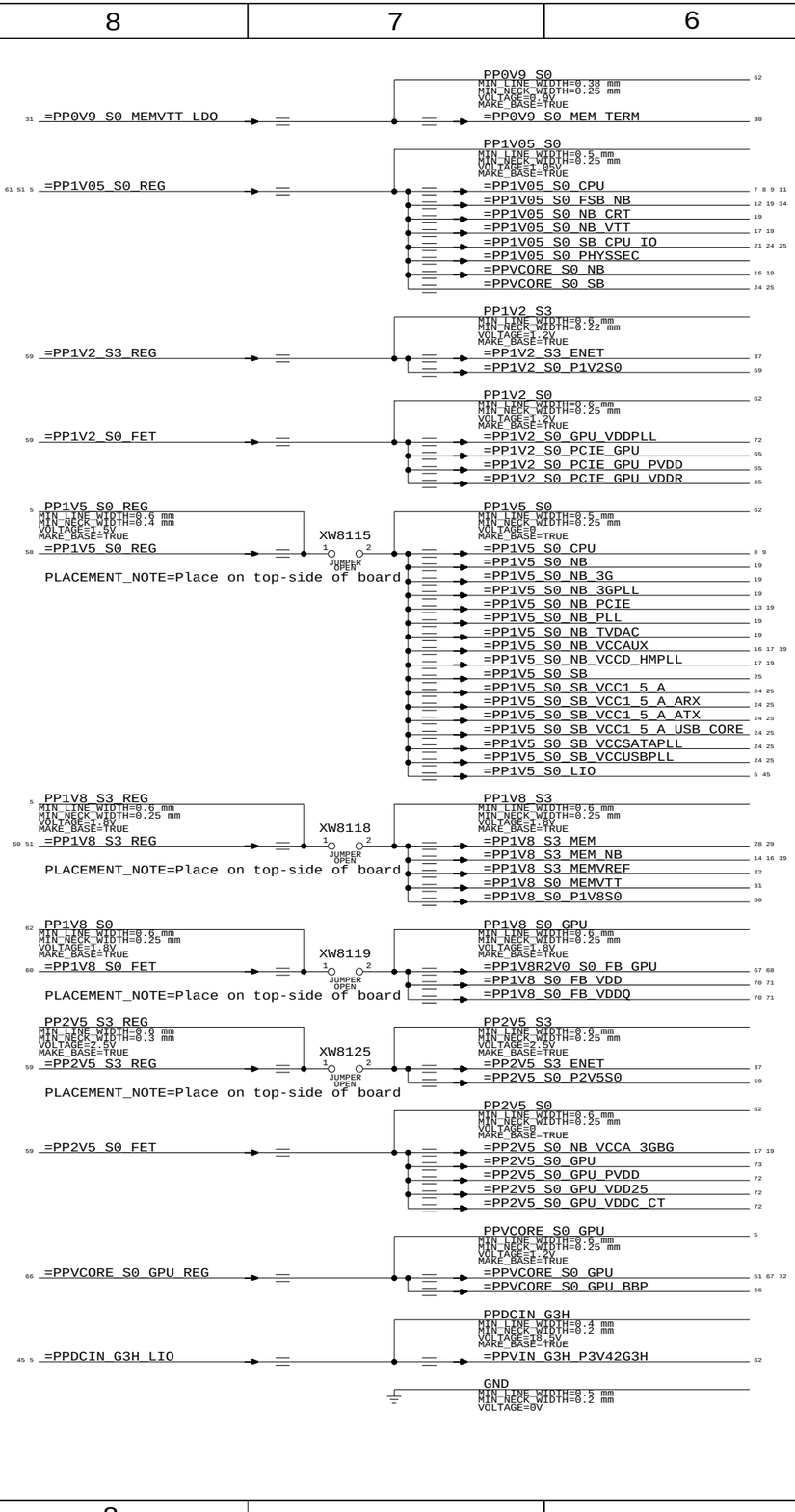
3.3V G3Hot Supply & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	80	104



Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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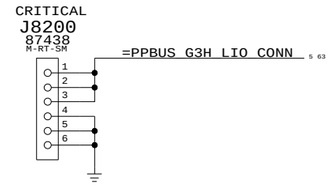
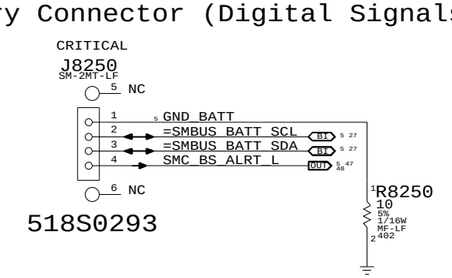
Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)



518S0293

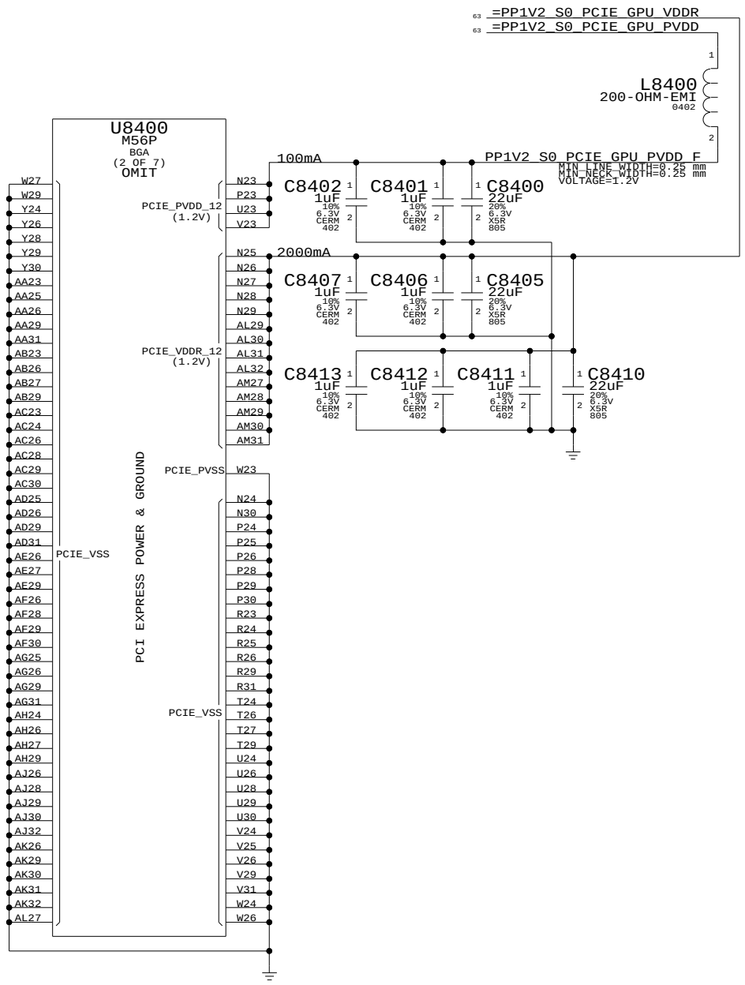
PBus-In & Battery Connectors

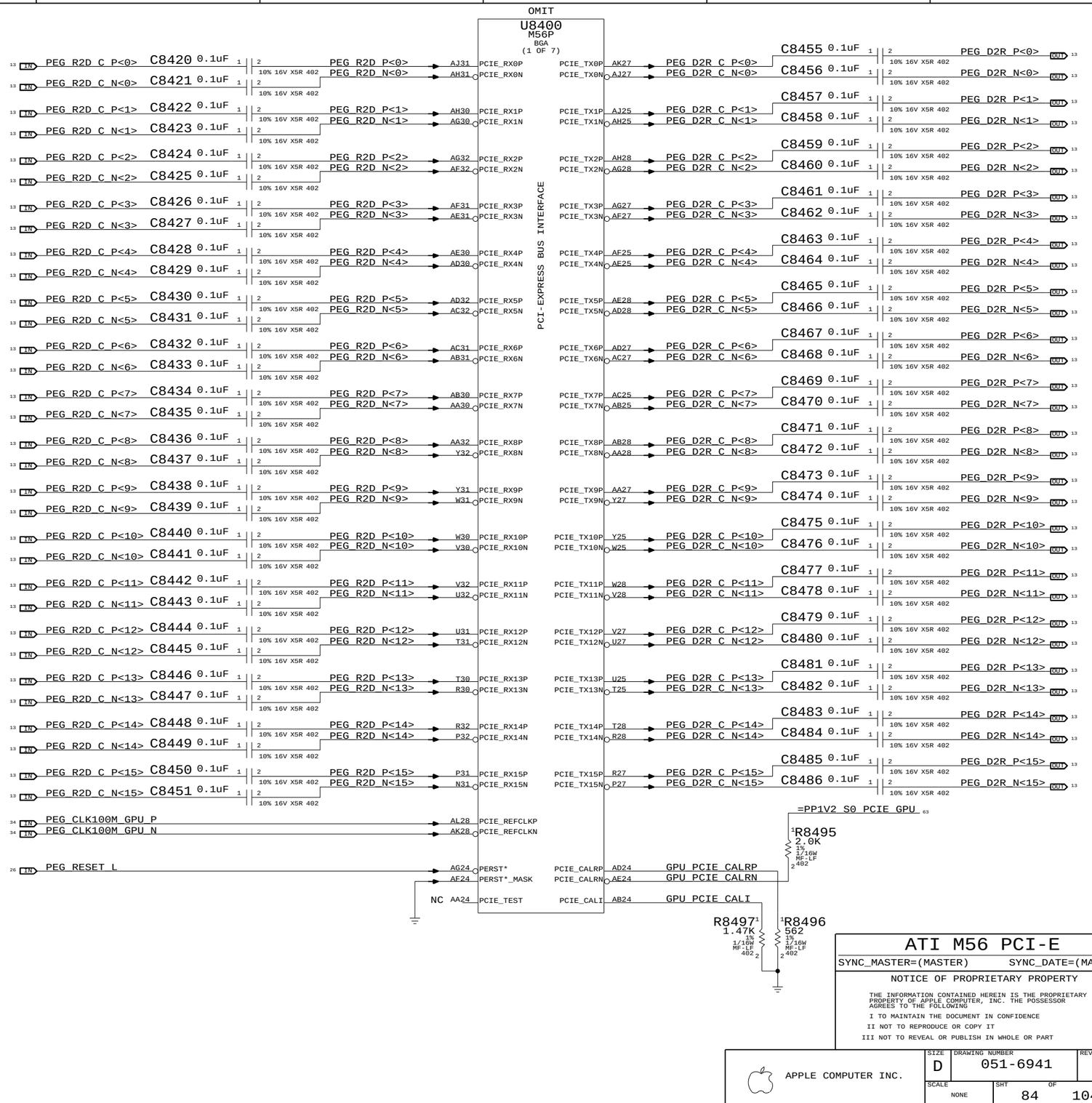
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	82	104





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 84 OF 104	

GPU VCore Supply

=PP5V_S0_GPUVCORE
=PPVIN_S0_GPUVCORE
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM1 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C8502 2.2UF 20% 6.3V CERM1 603
R8504 0 5% 1/16W MF-LF 402
=GPUVCORE_EN
=GPUVCORE_PGOOD
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
R8508 150K 1% 1/16W MF-LF 402
C8507 15pF 5% 50V CERM 402
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
GPUVCORE_COMP_R
NO STUFF R8505 0 5% 1/16W MF-LF 402
C8508 470pF 10% 50V CERM 402
GND_GPUVCORE_SGND
XW8500 SM
U8500 ISL6269 QFN
CRITICAL
THRML PAD
VIN, FSET, EN, FCCM, PGOOD, COMP, FB, VO, PVCC, VCC, UG, BOOT, PHASE, ISEN, LG, PGND
GPUVCORE_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
GPUVCORE_BOOT
GPUVCORE_PHASE
SWITCH_NODE=TRUE
GPUVCORE_ISEN
GPUVCORE_LG
GPUVCORE_BOOT_R
R8509 0 5% 1/16W MF-LF 402
C8509 0.22UF 20% 6.3V X5R 402
R8510 3.01K 1% 1/16W MF-LF 402
C8530 22uF 20% 16V X7R 1210
C8531 22uF 20% 16V X7R 1210
C8532 22uF 20% 16V X7R 1210
CRITICAL Q8520 HAT2168H LFPAK
CRITICAL Q8521 HAT2165H LFPAK
CRITICAL Q8522 HAT2165H LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
C8521 1000pF 10% 25V X7R 402
CRITICAL D8520 SMB B340LBXF
GPUISENS_NTC
R8596 1K 1% 1/16W MF-LF 402
CRITICAL R8597 10KOHM-5% 0603-LF
NO STUFF R8594 1K 1% 1/16W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
GPUISENS_RC
R8590 649 1% 1/16W MF-LF 402
CRITICAL L8520 1.0uH-20.5 SM1
NC
R8593 20.0K 1% 1/16W MF-LF 402
GPUISENS_NEG
R8591 20.0K 1% 1/16W MF-LF 402
GPUISENS_POS
=PP3V3R5V_S0_GPUISENS
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
GPUVCORE_IOUT
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402
Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor
=PPVCORE_S0_GPU_REG
B24: Vout = 1.10V / 0.95V
B13: Vout = 1.08V / 1.00V
17A max output
(Q8520 limit)
<Ra> R8521 3.01K 1% 1/16W MF-LF 402
<Rb> R8522 5.11K 1% 1/16W MF-LF 402
NO STUFF R8520 0 5% 1/16W MF-LF 402
GPUVCORE_FB_RC
NO STUFF C8520 0.0022uF 10% CERM 402
(GPUVCORE_FB)
C8540 22uF 20% 6.3V X5R 805
C8542 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C8541 22uF 20% 6.3V X5R 805
C8543 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
<Rc> R8523 12.4K 1% 1/16W MF-LF 402
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

=PP3V3_S0_GPU
R8526 100K 5% 1/16W MF-LF 402
R8525 0 5% 1/16W MF-LF 402
GPU_VCORE_HIGH
GPU_VCORE_HIGH_RC
Q8523 2N7002DW-X-F SOT-363
C8523 0.1uF 10% 16V X5R 402
GPU_VCORE_LOW
R8524 10K 5% 1/16W MF-LF 402

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

Q8575 SI3446DV TSOP-LF
=PPVCORE_S0_GPU_BBP
GPUBB_EN_L
CRITICAL U8550 FAN2558 SOT23-6-LF
VIN, PG, EN, GND, VOUT, ADJ
=PP3V3_S0_GPUBBP
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM1 603
=PPVOUT_S0_GPUBBP_LDO
Vout = (1.58V /) 1.50V
180mA max output
(LDO limit)
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22uF 20% 6.3V X5R 805
GPUBBP_ADJ
NO STUFF R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
<Rc>
C8557 22uF 20% 6.3V X5R 805
GPUBBP_ADJ_LOW
NO STUFF Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

=PP5V_S0_GPUBBCTL
Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V
For proper M56 power sequence, this pull-up must be powered before VCore
R8570 100K 5% 1/16W MF-LF 402
GPUBB_EN_L
GPU_BB_CTL
R8561 0 5% 1/16W MF-LF 402
GPU_GENERICD
GPUBB_EN
Q8570 2N7002 SOT23-LF
C8570 0.01uF 10% 16V CERM 402
R8560 10K 5% 1/16W MF-LF 402

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active.
When inactive, provides VSS to BBN pins.

=PP3V3_S0_GPUBBN
C8580 10uF 20% 6.3V X5R 603
GPUBB_EN
GPUBBN_CAPP
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
C8581 2.2uF 20% 6.3V CERM1 603
GPUBBN_CAPN
U8580 MAX1673 SOI
CRITICAL
SHDN_L, IN, CAP+, CAP-, LIN/SKIP_L, GND, FB, OUT
<Ra> R8587 66.5K 1% 1/16W MF-LF 402
GPUBBN_FB
<Rb> R8588 10K 1% 1/16W MF-LF 402
C8589 22uF 20% 6.3V X5R 805
=PNVOUT_S0_GPUBBN_REG
Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA
Vout = -0.50V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
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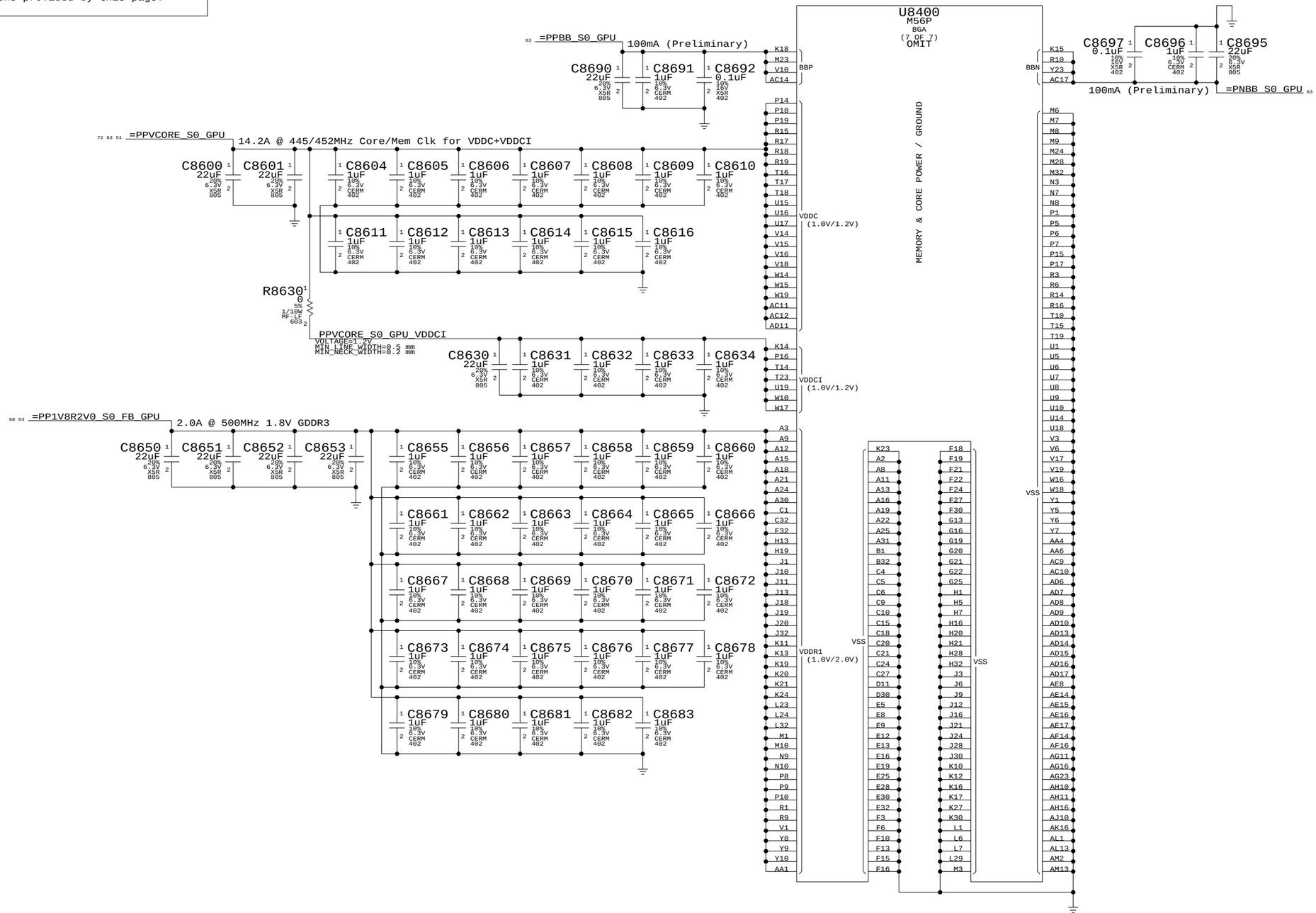
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

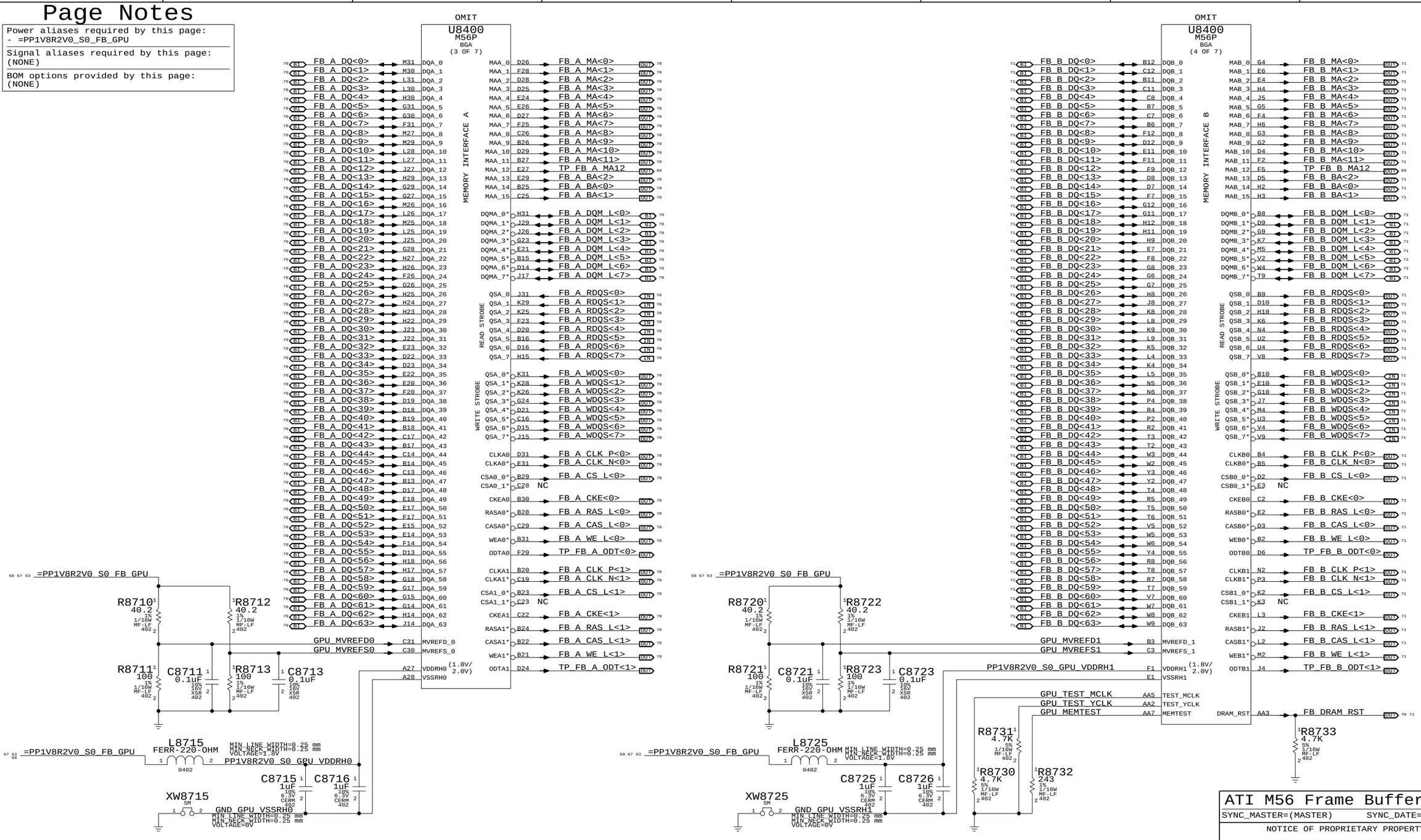
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 86 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 87 OF 104	

	Serial ROM	TestBus	Misc	Straps
GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved
GPU_GPIO_3		TESTIN[3]		Reserved
GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
GPU_GPIO_5		TESTIN[5]		Reserved
GPU_GPIO_6		TESTIN[6]		Reserved
GPU_GPIO_7	ENA_BL	TESTIN[7]		
GPU_GPIO_8	ROMSO	TESTWR		Reserved
GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]
GPU_GPIO_10	ROMSCK	TESTOUT[8]		
GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]
GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]
GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]
GPU_GPIO_14		TESTIN[8]		
GPU_GPIO_15		TESTIN[9]	PWRCNTL	
GPU_GPIO_16			SS_IN	
GPU_GPIO_17			Thm Mon Int	

GPU_GPIO_0 — MAKE_BASE=TRUE — NC_GPU_GPIO_0
GPU_GPIO_1 — MAKE_BASE=TRUE — NC_GPU_GPIO_1
GPU_GPIO_2 — MAKE_BASE=TRUE — NC_GPU_GPIO_2
GPU_GPIO_3 — MAKE_BASE=TRUE — NC_GPU_GPIO_3
GPU_GPIO_4 — MAKE_BASE=TRUE — NC_GPU_GPIO_4
GPU_GPIO_5 — MAKE_BASE=TRUE — NC_GPU_GPIO_5
GPU_GPIO_6 — MAKE_BASE=TRUE — NC_GPU_GPIO_6
GPU_GPIO_7 — MAKE_BASE=TRUE — GPU_BLON
GPU_GPIO_8 — MAKE_BASE=TRUE — NC_GPU_GPIO_8
GPU_GPIO_9 — MAKE_BASE=TRUE — NC_GPU_GPIO_9
GPU_GPIO_10 — MAKE_BASE=TRUE — TP_GPU_GPIO_10
GPU_GPIO_11 — MAKE_BASE=TRUE — NC_GPU_GPIO_11
GPU_GPIO_12 — MAKE_BASE=TRUE — NC_GPU_GPIO_12
GPU_GPIO_13 — MAKE_BASE=TRUE — NC_GPU_GPIO_13
GPU_GPIO_14 — MAKE_BASE=TRUE — NC_GPU_GPIO_14 NO_TEST=TRUE
GPU_GPIO_15 — MAKE_BASE=TRUE — GPU_VCORE_LOW
GPU_GPIO_16 — MAKE_BASE=TRUE — GPU_CLK27MSS_IN
GPU_GPIO_17 — MAKE_BASE=TRUE — NC_GPU_GPIO_17 NO_TEST=TRUE
GPU_GPIO_18 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_18
GPU_GPIO_19 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_19
GPU_GPIO_20 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_20
GPU_GPIO_21 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_21
GPU_GPIO_22 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_22
GPU_GPIO_23 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_23
GPU_GPIO_24 — MAKE_BASE=TRUE — GPU_MEM_256M
GPU_GPIO_25 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_25
GPU_GPIO_26 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_26
GPU_GPIO_27 — MAKE_BASE=TRUE — GPU_MEMID
GPU_GPIO_28 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_28
GPU_GPIO_29 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_29
GPU_GPIO_30 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_30
GPU_GPIO_31 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_31
GPU_GPIO_32 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_32
GPU_GPIO_33 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_33
GPU_GPIO_34 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_34

=PP3V3_S0_GPU_GPIOS

R8800 10K 5% 1/16W MF-LF 402
NO STUFF R8802 10K 5% 1/16W MF-LF 402
NO STUFF R8804 10K 5% 1/16W MF-LF 402
NO STUFF R8806 10K 5% 1/16W MF-LF 402
NO STUFF R8809 10K 5% 1/16W MF-LF 402
GPU_MEM_256M R8812 10K 5% 1/16W MF-LF 402
GPU_MEM_256M R8824 10K 5% 1/16W MF-LF 402

GPU_DEEPMH_EN R8801 10K 5% 1/16W MF-LF 402
NO STUFF R8803 10K 5% 1/16W MF-LF 402
R8805 10K 5% 1/16W MF-LF 402
NO STUFF R8808 10K 5% 1/16W MF-LF 402
GPU_MEM_64M R8813 10K 5% 1/16W MF-LF 402
NO STUFF R8811 10K 5% 1/16W MF-LF 402
GPU_MEM_HYNIX R8827 10K 5% 1/16W MF-LF 402

ROMCFGID[3..0]
0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

Required for debug access
Required for debug access
Required for debug access
Required for debug access

Renamed signals

GPU_CLK27M — MAKE_BASE=TRUE — GPU_XTALIN

Unused signals

NC_GPU_XTALOUT — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_XTALOUT
NC_ATI_ROMCS_L — MAKE_BASE=TRUE NO_TEST=TRUE — TP_ATI_ROMCS_L
NC_FB_A_MA12 — MAKE_BASE=TRUE NO_TEST=TRUE — TP_FB_A_MA12
NC_FB_B_MA12 — MAKE_BASE=TRUE NO_TEST=TRUE — TP_FB_B_MA12
NC_GPU_GENERICA — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_GENERICA
NC_GPU_GENERICB — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_GENERICB
NC_GPU_GENERICC — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_GENERICC
NC_GPU_VGA_R — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_VGA_R
NC_GPU_VGA_G — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_VGA_G
NC_GPU_VGA_B — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_VGA_B
TP_GPU_VGA_HSYNC — MAKE_BASE=TRUE — GPU_VGA_HSYNC
TP_GPU_VGA_VSYNC — MAKE_BASE=TRUE — GPU_VGA_VSYNC
NC_GPU_TV_Y — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_TV_Y
NC_GPU_TV_C — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_TV_C
NC_GPU_TV_COMP — MAKE_BASE=TRUE NO_TEST=TRUE — GPU_TV_COMP
NC_LVDS_U_DATAP<3> — MAKE_BASE=TRUE NO_TEST=TRUE — LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3> — MAKE_BASE=TRUE NO_TEST=TRUE — LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3> — MAKE_BASE=TRUE NO_TEST=TRUE — LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3> — MAKE_BASE=TRUE NO_TEST=TRUE — LVDS_L_DATA_N<3>
NC_ATI_DVPCLK — MAKE_BASE=TRUE NO_TEST=TRUE — ATI_DVPCLK
NC_ATI_DVPCNTL<2..0> — MAKE_BASE=TRUE NO_TEST=TRUE — ATI_DVPCNTL<2..0>
NC_ATI_DVPDATA<15..0> — MAKE_BASE=TRUE NO_TEST=TRUE — ATI_DVPDATA<15..0>

Required for debug access

TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

=PP3V3_S0_GPU

R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402

GPU_DDC_B_CLK
GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 12
SCALE NONE | SHT 88 OF 104

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_S0_FB_VDD

=PP1V8_S0_FB_VDDQ

C8900 C8901 C8902 C8903 C8904 — 22uF 20% 6.3V X5R 805; 0.1uF 10% 16V X5R 402

L8910 FERR-220-OHM 0402 — PP1V8_S0_FB_A0_VDDA0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

L8915 FERR-220-OHM 0402 — PP1V8_S0_FB_A0_VDDA1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

C8910 C8915 — 0.1uF 10% 16V X5R 402 — U8900.J1 U8900.J12

C8920 — 22uF 20% 6.3V X5R 805

C8921 C8922 C8923 C8924 C8925 C8926 — 0.1uF 10% 16V X5R 402

R8930 R8932 — 2.37K 1% 1/10W MF-LF 402

FB_A0_VREF0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A0_VREF1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R8931 R8933 — 5.49K 1% 1/10W MF-LF 402

C8931 C8933 — 0.1uF 10% 16V X5R 402

R8940 R8942 R8944 — 121 1% 1/10W MF-LF 402

R8946 — 60.4 1% 1/10W MF-LF 402

R8941 — 0 5% 1/10W MF-LF 402

R8943 — 121 1% 1/10W MF-LF 402

R8945 — 60.4 1% 1/10W MF-LF 402

R8947 — 121 1% 1/10W MF-LF 402

R8948 — 243 1% 1/10W MF-LF 402

R8949 — 0 5% 1/10W MF-LF 402

U8900 — FBGA (2 OF 2) — CRITICAL OMIT — 16MX32-GDDR3-500MHZ K4J52324QC-BC20

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

C8950 C8951 C8952 C8953 C8954 — 22uF 20% 6.3V X5R 805; 0.1uF 10% 16V X5R 402

L8960 FERR-220-OHM 0402 — PP1V8_S0_FB_A1_VDDA0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

L8965 FERR-220-OHM 0402 — PP1V8_S0_FB_A1_VDDA1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

C8960 C8965 — 0.1uF 10% 16V X5R 402 — U8900.J1 U8900.J12

C8970 — 22uF 20% 6.3V X5R 805

C8971 C8972 C8973 C8974 C8975 C8976 — 0.1uF 10% 16V X5R 402

R8980 R8982 — 2.37K 1% 1/10W MF-LF 402

FB_A1_VREF0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A1_VREF1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R8981 R8983 — 5.49K 1% 1/10W MF-LF 402

C8981 C8983 — 0.1uF 10% 16V X5R 402

R8990 R8992 R8994 — 121 1% 1/10W MF-LF 402

R8996 — 60.4 1% 1/10W MF-LF 402

R8991 — 0 5% 1/10W MF-LF 402

R8993 — 121 1% 1/10W MF-LF 402

R8995 — 60.4 1% 1/10W MF-LF 402

R8997 — 121 1% 1/10W MF-LF 402

R8998 — 243 1% 1/10W MF-LF 402

R8999 — 0 5% 1/10W MF-LF 402

U8950 — FBGA (1 OF 2) — CRITICAL OMIT — 16MX32-GDDR3-500MHZ K4J52324QC-BC20

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<0> FB_A_CLK_P<0> FB_A_CLK_N<0> FB_A_CS_L<0> FB_A_WE_L<0> FB_A_CAS_L<0> FB_A_RAS_L<0>

FB_A0_ZQ FB_A0_MF FB_A0_SEN

FB_DRAM_RST

FB_A_RDQS<0> FB_A_RDQS<1> FB_A_RDQS<2> FB_A_RDQS<3>

FB_A_WDQS<0> FB_A_WDQS<1> FB_A_WDQS<2> FB_A_WDQS<3>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

FB_A_DQM_L<0> FB_A_DQM_L<1> FB_A_DQM_L<2> FB_A_DQM_L<3>

FB_A_DQ<0> FB_A_DQ<1> FB_A_DQ<2> FB_A_DQ<3> FB_A_DQ<4> FB_A_DQ<5> FB_A_DQ<6> FB_A_DQ<7> FB_A_DQ<8> FB_A_DQ<9> FB_A_DQ<10> FB_A_DQ<11> FB_A_DQ<15> FB_A_DQ<14> FB_A_DQ<12> FB_A_DQ<13> FB_A_DQ<19> FB_A_DQ<16> FB_A_DQ<18> FB_A_DQ<17> FB_A_DQ<23> FB_A_DQ<21> FB_A_DQ<20> FB_A_DQ<22> FB_A_DQ<24> FB_A_DQ<25> FB_A_DQ<26> FB_A_DQ<27> FB_A_DQ<29> FB_A_DQ<30> FB_A_DQ<28> FB_A_DQ<31>

NC NC

FB_A1_ZQ FB_A1_MF FB_A1_SEN

FB_A_RDQS<4> FB_A_RDQS<5> FB_A_RDQS<6> FB_A_RDQS<7>

FB_A_WDQS<4> FB_A_WDQS<5> FB_A_WDQS<6> FB_A_WDQS<7>

FB_A_DQM_L<4> FB_A_DQM_L<5> FB_A_DQM_L<6> FB_A_DQM_L<7>

FB_A_DQ<32> FB_A_DQ<34> FB_A_DQ<33> FB_A_DQ<35> FB_A_DQ<36> FB_A_DQ<37> FB_A_DQ<38> FB_A_DQ<39> FB_A_DQ<40> FB_A_DQ<41> FB_A_DQ<42> FB_A_DQ<43> FB_A_DQ<46> FB_A_DQ<44> FB_A_DQ<47> FB_A_DQ<45> FB_A_DQ<48> FB_A_DQ<49> FB_A_DQ<50> FB_A_DQ<51> FB_A_DQ<52> FB_A_DQ<55> FB_A_DQ<54> FB_A_DQ<53> FB_A_DQ<60> FB_A_DQ<59> FB_A_DQ<61> FB_A_DQ<57> FB_A_DQ<62> FB_A_DQ<56> FB_A_DQ<63> FB_A_DQ<58>

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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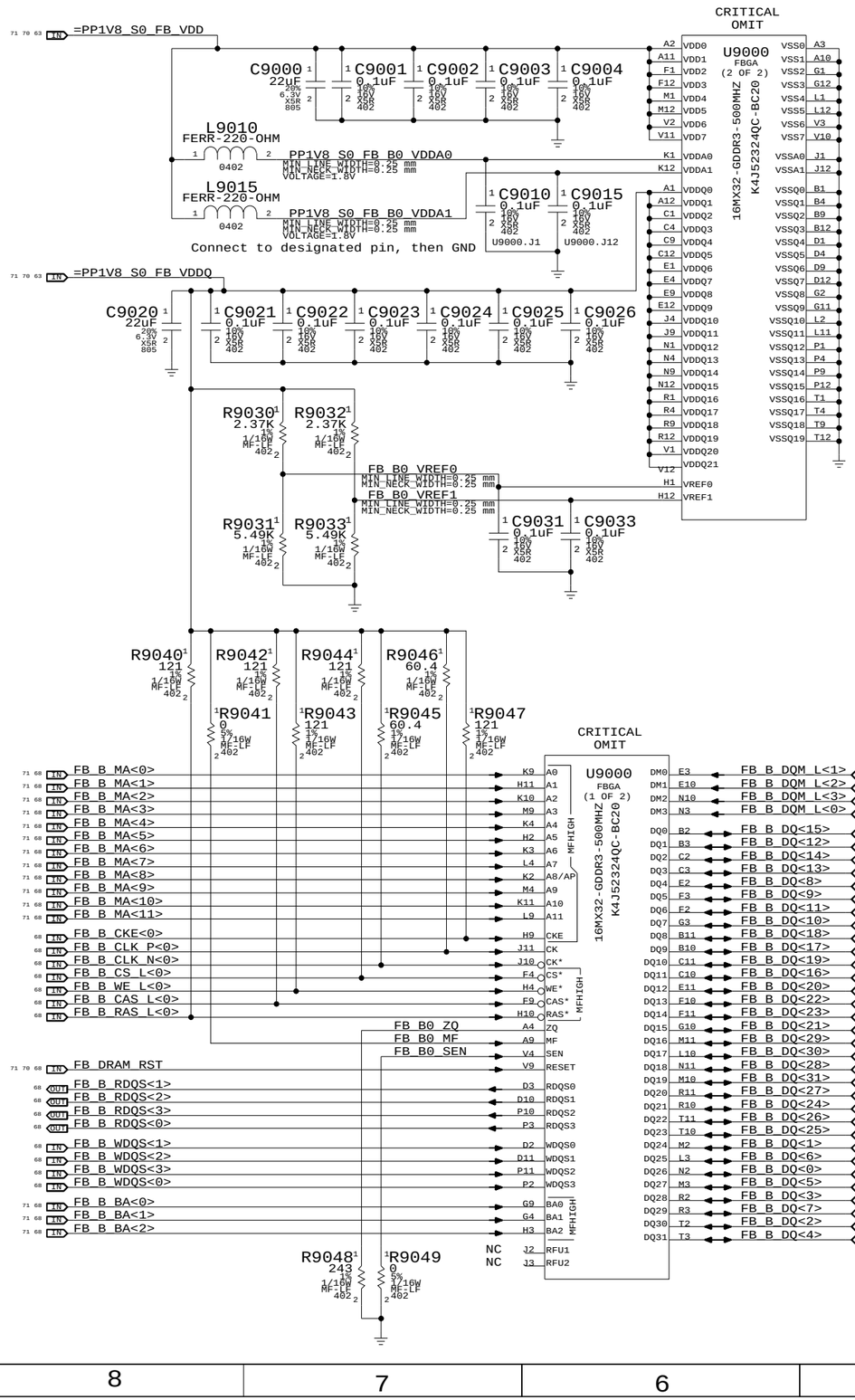
SCALE NONE | SHT 89 OF 104

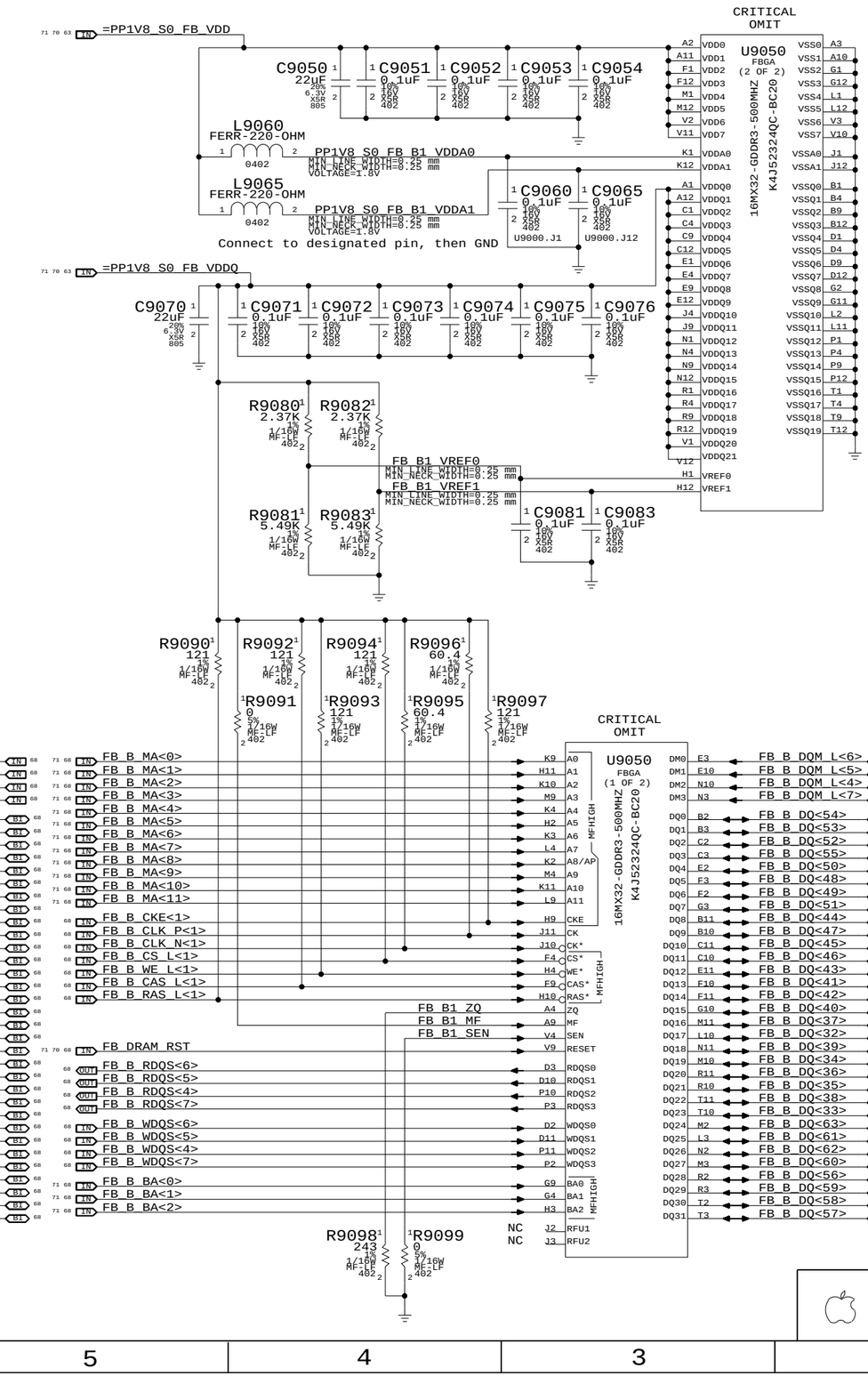
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

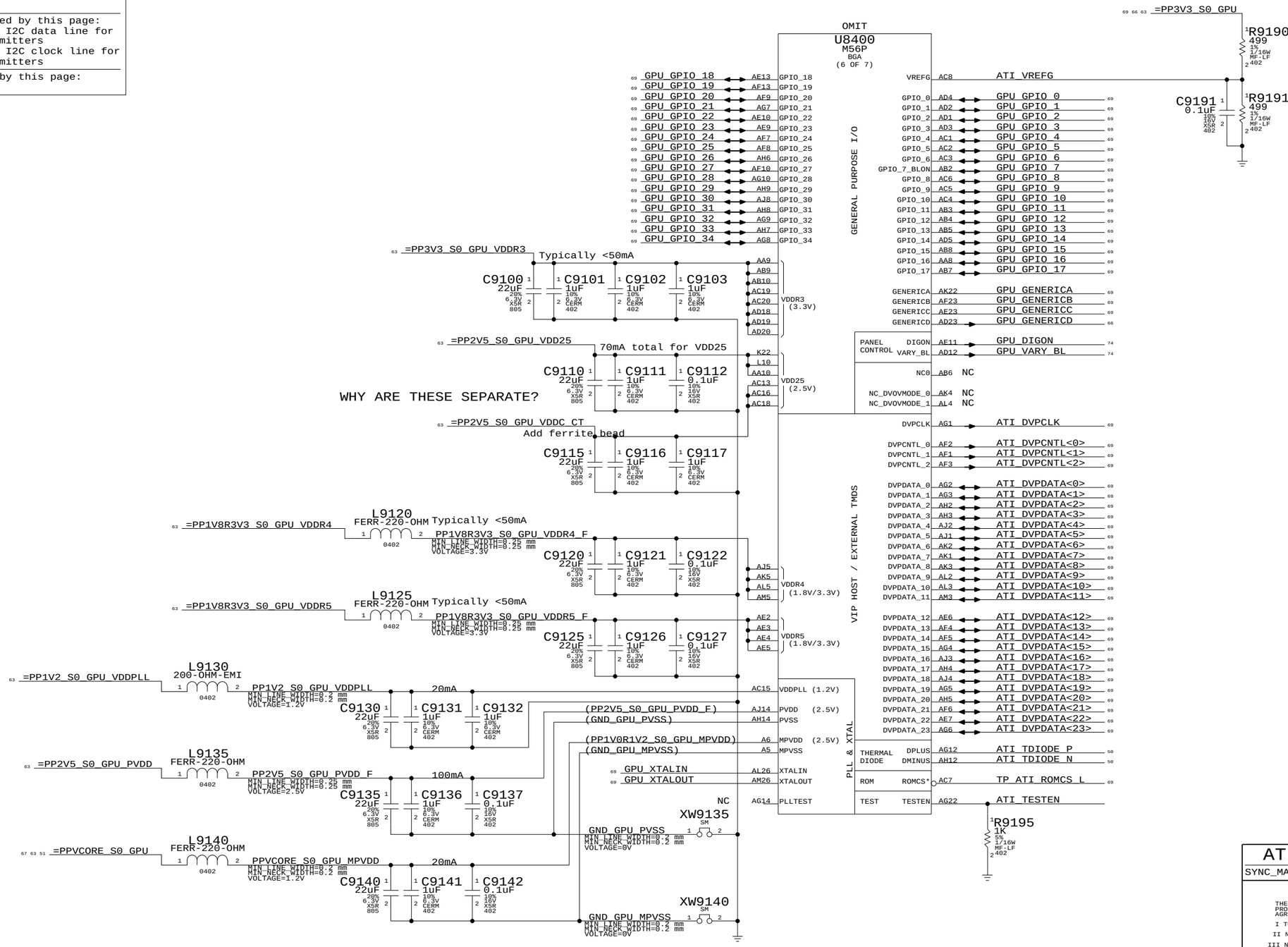
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 90 OF 104	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-6941	12
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Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

63 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9300 22uF 20% 6.3V X5R 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9305 22uF 20% 6.3V X5R 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9310 22uF 20% 6.3V X5R 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22uF 20% 6.3V X5R 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9320 22uF 20% 6.3V X5R 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9325 22uF 20% 6.3V X5R 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9330 22uF 20% 6.3V X5R 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9340 22uF 20% 6.3V X5R 805; C9345 22uF 20% 6.3V X5R 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
AM8 TPVDD (2.5V)
AL8 TPVSS
AJ6 AK6 AL6 AM6 TXVDDR (2.5V)
AJ7 AK7 AK8 AL7 AM7 TXVSSR
AL25 AM25 AVDD (2.5V)
AJ24 AK25 AVSS
AK23 AVSSQ

DAC (CRT)
AM23 VDD1DI (2.5V)
AL23 VSS1DI
73 ATI RSET → AL22 RSET

DAC2 (TV/CRT2)
AL16 AM16 A2VDD (2.5V)
AL17 AM17 A2VSS
NC AL14 NC_A2VDDQ
AK13 A2VSSQ
AJ16 VDD2DI (2.5V)
AJ17 VSS2DI
73 ATI R2SET → AK14 R2SET

LVDS
AE19 LVPVD (2.5V)
AE18 LVPVSS
AC21 AC22 AD21 AD22 AE20 AE21 AE22 AF19 AF20 LVDDR (2.5V)
AF17 AF18 AF21 AF22 AG17 AG19 AH17 AH19 AJ19 AK17 LVSSR

MONITOR IDENTIFICATION
75 HPD → AF11 HPD1

TXCP	AM9	TMDS_CLK_P	OUT 74 75 79
TXCM	AL9	TMDS_CLK_N	OUT 74 75 79
TX0P	AL10	TMDS_DATA_P<0>	OUT 74 75 79
TX0M	AK10	TMDS_DATA_N<0>	OUT 74 75 79
TX1P	AM11	TMDS_DATA_P<1>	OUT 74 75 79
TX1M	AL11	TMDS_DATA_N<1>	OUT 74 75 79
TX2P	AM12	TMDS_DATA_P<2>	OUT 74 75 79
TX2M	AL12	TMDS_DATA_N<2>	OUT 74 75 79
TX3P	AJ9	TMDS_DATA_P<3>	OUT 74 75 79
TX3M	AK9	TMDS_DATA_N<3>	OUT 74 75 79
TX4P	AJ11	TMDS_DATA_P<4>	OUT 74 75 79
TX4M	AK11	TMDS_DATA_N<4>	OUT 74 75 79
TX5P	AJ12	TMDS_DATA_P<5>	OUT 74 75 79
TX5M	AK12	TMDS_DATA_N<5>	OUT 74 75 79
R	AK24	GPU_VGA_R	OUT 69
G	AM24	GPU_VGA_G	OUT 69
B	AL24	GPU_VGA_B	OUT 69
HSYNC	AJ23	GPU_VGA_HSYNC	OUT 69
VSYNC	AJ22	GPU_VGA_VSYNC	OUT 69
R2	AK15	GPU_R2	OUT 74 75
G2	AM15	GPU_G2	OUT 74 75
B2	AL15	GPU_B2	OUT 74 75
H2SYNC	AF15	GPU_H2SYNC	OUT 75
V2SYNC	AG15	GPU_V2SYNC	OUT 75
Y	AJ15	GPU_TV_Y	OUT 69
C	AJ13	GPU_TV_C	OUT 69
COMP	AH15	GPU_TV_COMP	OUT 69
TXCLK_UP	AJ21	LVDS_U_CLK_P	OUT 74 77
TXCLK_UN	AK21	LVDS_U_CLK_N	OUT 74 77
TXOUT_U0P	AG18	LVDS_U_DATA_P<0>	OUT 74 77
TXOUT_U0N	AH18	LVDS_U_DATA_N<0>	OUT 74 77
TXOUT_U1P	AK20	LVDS_U_DATA_P<1>	OUT 74 77
TXOUT_U1N	AJ20	LVDS_U_DATA_N<1>	OUT 74 77
TXOUT_U2P	AG20	LVDS_U_DATA_P<2>	OUT 74 77
TXOUT_U2N	AH20	LVDS_U_DATA_N<2>	OUT 74 77
TXOUT_U3P	AH21	LVDS_U_DATA_P<3>	OUT 69
TXOUT_U3N	AG21	LVDS_U_DATA_N<3>	OUT 69
TXCLK_LP	AM18	LVDS_L_CLK_P	OUT 74 77
TXCLK_LN	AL18	LVDS_L_CLK_N	OUT 74 77
TXOUT_L0P	AL19	LVDS_L_DATA_P<0>	OUT 74 77
TXOUT_L0N	AK19	LVDS_L_DATA_N<0>	OUT 74 77
TXOUT_L1P	AM20	LVDS_L_DATA_P<1>	OUT 74 77
TXOUT_L1N	AL20	LVDS_L_DATA_N<1>	OUT 74 77
TXOUT_L2P	AM21	LVDS_L_DATA_P<2>	OUT 74 77
TXOUT_L2N	AL21	LVDS_L_DATA_N<2>	OUT 74 77
TXOUT_L3P	AJ18	LVDS_L_DATA_P<3>	OUT 69
TXOUT_L3N	AK18	LVDS_L_DATA_N<3>	OUT 69
DDC1CLK	AH23	GPU_DDC_A_CLK	BI 75
DDC1DATA	AH22	GPU_DDC_A_DATA	BI 75
DDC2CLK	AG13	GPU_DDC_B_CLK	BI 69
DDC2DATA	AH13	GPU_DDC_B_DATA	BI 69
DDC3CLK	AF12	GPU_DDC_C_CLK	BI 74
DDC3DATA	AE12	GPU_DDC_C_DATA	BI 74

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI_RSET 73
ATI_R2SET 73
R9350 499 1% 1/10W MF-LF 402
R9351 715 1% 1/10W MF-LF 402

GPU_HPD 75 IN

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
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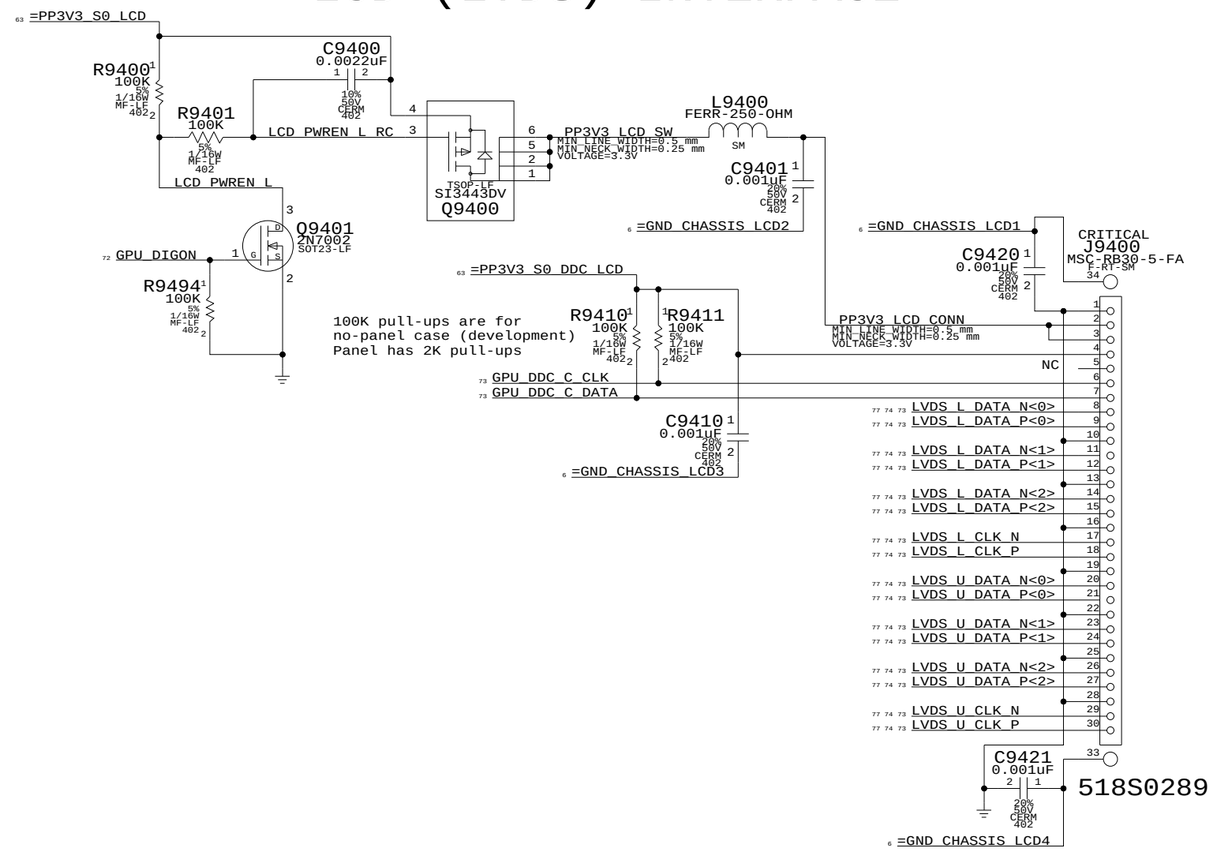
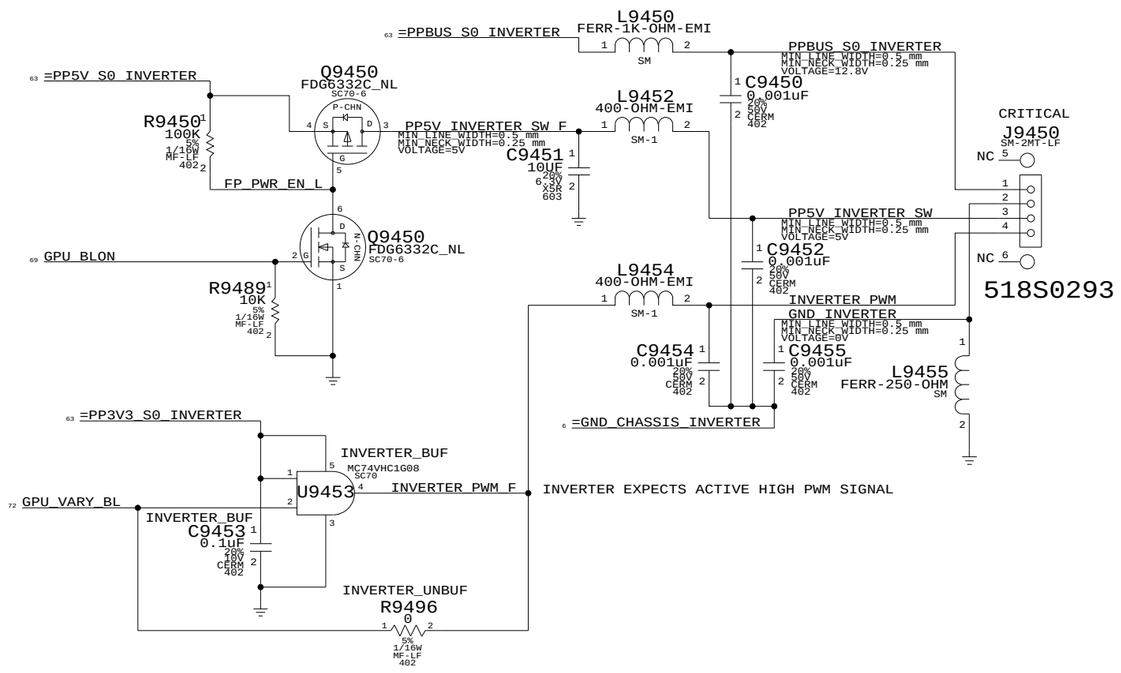
LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 74 77
	LVDS	LVDS	LVDS_U_CLK_N	73 74 77
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 74 77
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 74 77
	LVDS	LVDS	LVDS_L_CLK_P	73 74 77
	LVDS	LVDS	LVDS_L_CLK_N	73 74 77
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 74 77
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 74 77
	TMDS	TMDS	TMDS_CLK_P	73 75 79
	TMDS	TMDS	TMDS_CLK_N	73 75 79
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 79



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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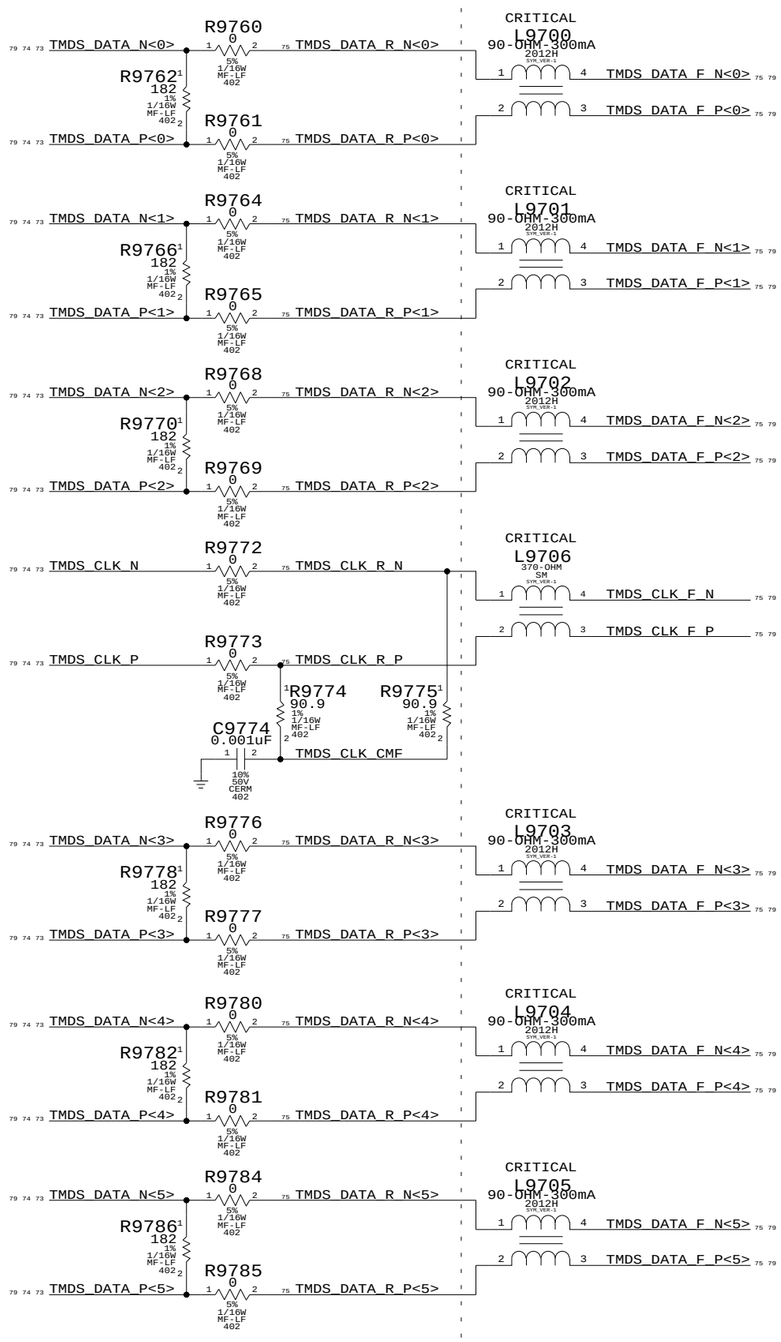
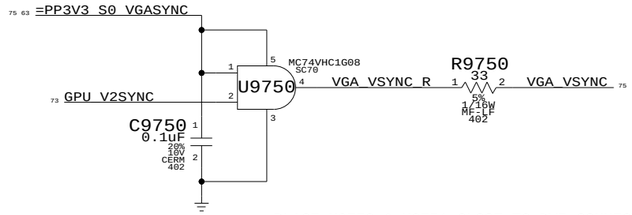
D	051-6941	12
SCALE: NONE	SHT: 94	OF: 104

TMDS Filtering

Place series R's and common-mode filtering close to GPU, common mode chokes near connector.

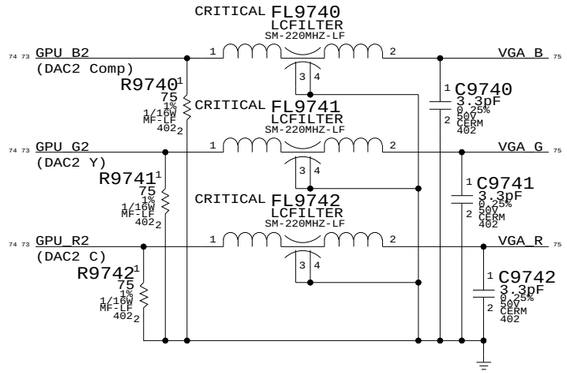


VGA SYNC BUFFERS



PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

Isolation required for DVI power switch

3V LEVEL SHIFTERS

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
	TMDS	TMDS
	TMDSCONN	TMDSCONN
	TMDSCONN	TMDSCONN
	TMDSCONN	TMDSCONN
	TMDSCONN	TMDSCONN

TMDS_CLK_R_P
TMDS_CLK_R_N
TMDS_DATA_R_P<5..0>
TMDS_DATA_R_N<5..0>
TMDS_CLK_F_P
TMDS_CLK_F_N
TMDS_DATA_F_P<5..0>
TMDS_DATA_F_N<5..0>

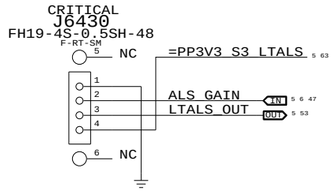
External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

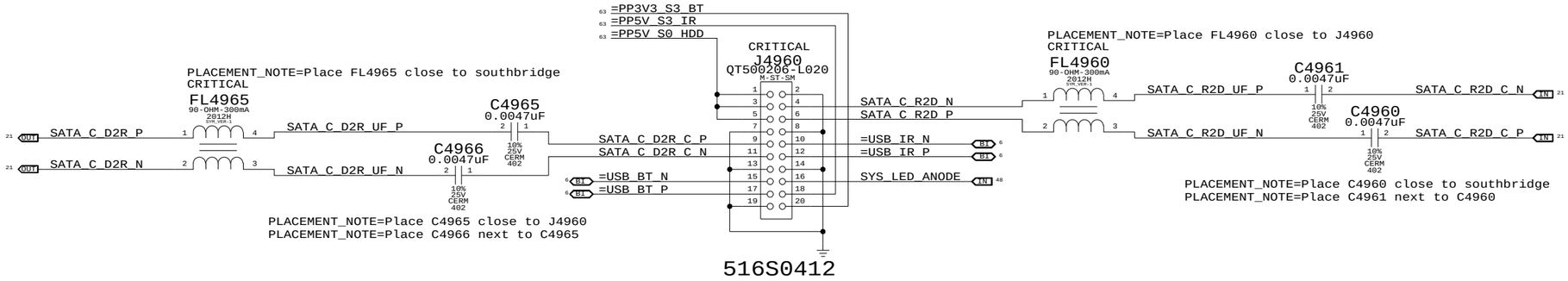
SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 97 OF 104	

Left ALS Connector



518S0395

Bluetooth (M13P) & SATA HDD Flex Connector



516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M1 Specific Connectors

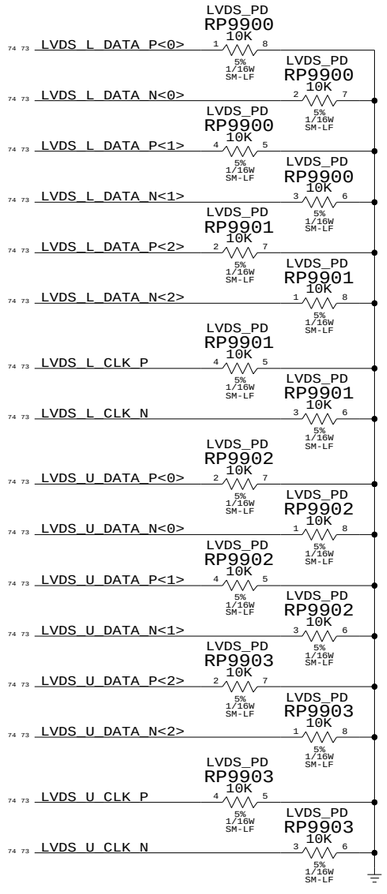
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12
SCALE: NONE	SHT 98 OF 104	

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	99	104

Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42.
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.
2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

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DMS Checkin #07001

2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.
2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.
2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.
2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.
2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.
2005/09/30 - 4248911 - Sync with M38 & M42.
2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.
2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.

DMS Checkin #07002

2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.
2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.
2005/10/06 - 4227330 - Added ESD protection on top-case USB port.
2005/10/07 - 4286888 - BOM restructuring per EVT build plan.
2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.
2005/10/07 - 4248911 - Sync with M38 & M42.

DMS Checkin #07003

2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.
2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).
2005/10/08 - 4286729 - Changed value of TPM Xtal caps.
2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.
2005/10/09 - 4235898 - Part moves & refdes changes to support sync with M9.
2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.
2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.

DMS Checkin #07004

2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.
2005/10/10 - 4247941 - Net property updates found via back-annotation.

DMS Checkin #07005

2005/10/10 - 4229560 - Removed Physical Security circuitry.
2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.
2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.
2005/10/10 - 4248911 - Sync with M38 & M42.
2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.

DMS Checkin #07006

2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.
2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.
2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.
2005/10/12 - 4248911 - Sync with M38 & M42.
2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.
2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.
2005/10/12 - 4223808 - Power supply changes per vendor feedback.
2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).
2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.
2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.
2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.
2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.
2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.
2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.

DMS Checkin #07007

2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.

DMS Checkin #07008

2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.

DMS Checkin #07009

2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.
2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.
2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.
2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.
2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.

DMS Release #08000-11000 (EVT releases)

2005/10/20 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/10/21 - 4310267 - Synced 3 pages from mlb_evt branch back to trunk.
2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.
2005/10/26 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/11/03 - 4310267 - Synced 6 pages from mlb_evt branch back to trunk.
2005/11/15 - 4310267 - Synced 5 pages from mlb_evt branch back to trunk.
2005/11/15 - 4298899 - Removed unused platform reset gate.
2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.
2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.
2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.
2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.
2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.
2005/11/16 - 4345921 - FUNC_TEST updates per test team request.
2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.
2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.
2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.

DMS Checkin #11001

2005/11/16 - 4235898 - Sync with M38 & M42.
(11.1.0) 2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.
(11.2.0) 2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.
2005/11/18 - 4235898 - Changed R4210 package size per M9 request.
(11.3.0) 2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.
2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.
2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.
2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.
2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.
2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.
2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.
(11.4.0) 2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).

Date - Radar # - Description

DMS Checkin #11002

2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.
2005/11/21 - 4343202 - Changed RC value and net name for USB OC.
2005/11/22 - 4350840 - Swapped TMDS termination components for placement.
2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.
2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.
2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.
2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.
2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.
2005/11/30 - 4351181 - Changed ITP connector BOM option.
2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.
2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.
2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.
2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.
2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.
2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.

DMS Checkin #11003

2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.
2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.
2005/12/02 - 4363870 - Removed M1a support from BOM.
2005/12/02 - 4217524 - Updated part number for J6430.

DMS Release #12000

12

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE: NONE SHT: 100 OF: 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 57
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	57
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 79
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 79
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	57

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 45
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 45

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	12

SCALE	SHT	OF
NONE	104	104