

Mullet

M1 MLB
09/26/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

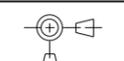
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4	4	BOM Configuration	N/A	N/A
5	5	Functional / ICT Test	N/A	N/A
6	6	Signal Aliases	N/A	N/A
7	7	CPU 1 OF 2-FSB	M42	09/08/2005
8	8	CPU 2 OF 2-PWR/GND	M42	09/08/2005
9	9	CPU Decoupling & VID	(MASTER)	(MASTER)
10	10	CPU MISCl-TEMP SENSOR	M42	09/08/2005
11	11	CPU ITP700FLEX DEBUG	M42	09/08/2005
12	12	NB CPU Interface	(MASTER)	(MASTER)
13	13	NB PEG / Video Interfaces	(MASTER)	(MASTER)
14	14	NB Misc Interfaces	(MASTER)	(MASTER)
15	15	NB DDR2 Interfaces	(MASTER)	(MASTER)
16	16	NB Power 1	(MASTER)	(MASTER)
17	17	NB Power 2	(MASTER)	(MASTER)
18	18	NB Grounds	(MASTER)	(MASTER)
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)
20	20	NB Config Straps	(MASTER)	(MASTER)
21	21		M38	09/08/2005
22	22		M38	09/08/2005
23	23		M38	09/08/2005
24	24		M38	09/08/2005
25	25		M42	09/08/2005
26	26	SB Misc	(MASTER)	(MASTER)
27	27	M1 SMBus Connections	(MASTER)	(MASTER)
28	28	DDR2 SO-DIMM Connector A	(MASTER)	(MASTER)
29	29	DDR2 SO-DIMM Connector B	(MASTER)	(MASTER)
30	30	Memory Active Termination	(MASTER)	(MASTER)
31	31	Memory Vtt Supply	(MASTER)	(MASTER)
32	32	DDR2 VRef	(MASTER)	(MASTER)
33	33	CLOCKS	M42	09/08/2005
34	34	Clock Termination	(MASTER)	(MASTER)
35	37	Mobile Clocking	(MASTER)	(MASTER)
36	38	PATA Connector	(MASTER)	(MASTER)
37	41	ETHERNET CONTROLLER	M42	09/08/2005
38	42	Ethernet Connector	(MASTER)	(MASTER)
39	44	FIREWIRE CONTROLLER	M42	08/29/2005
40	45	FireWire Port Power	(MASTER)	(MASTER)

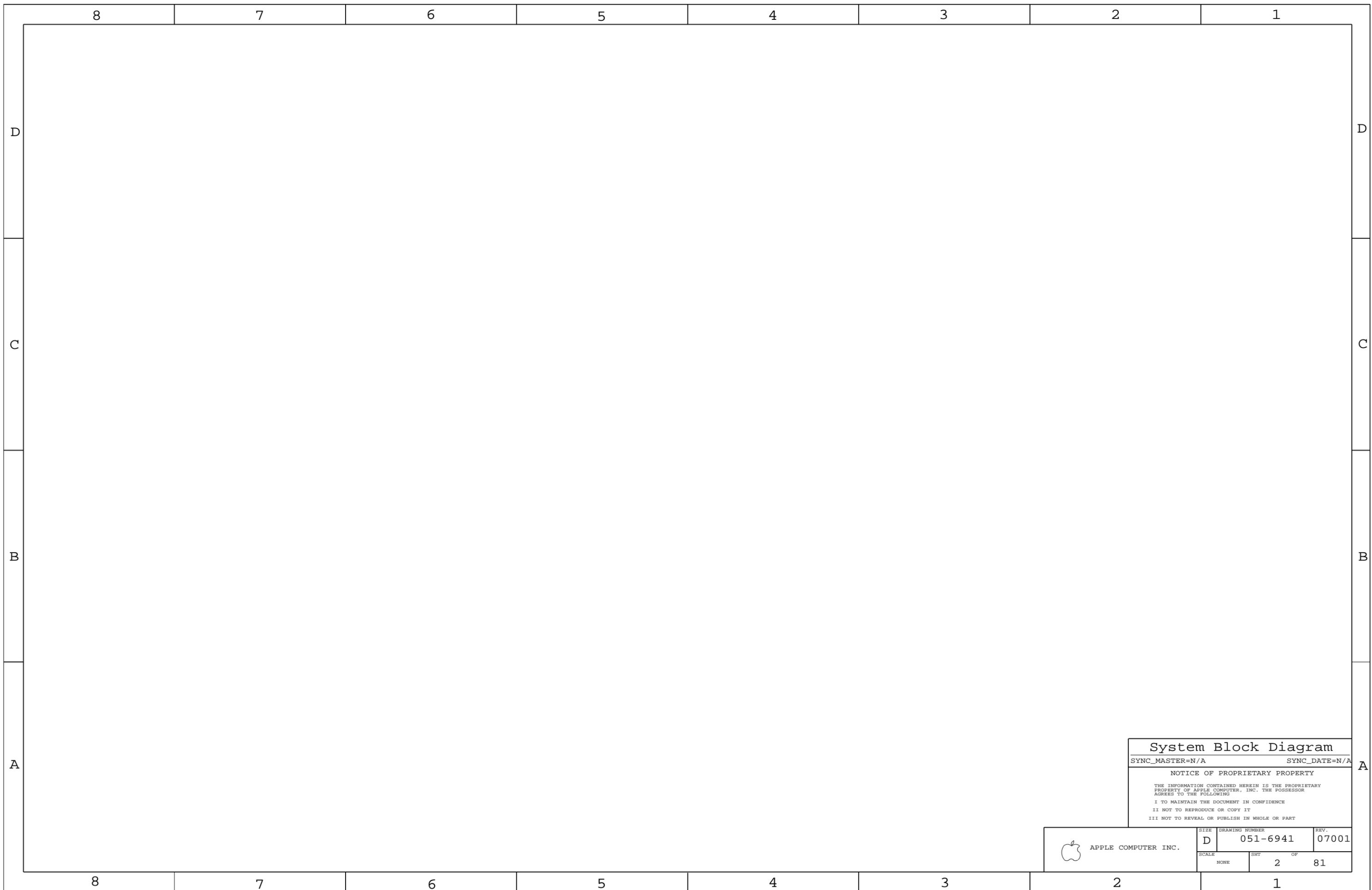
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44	55	Left I/O Board Connector	(MASTER)	(MASTER)
45	57	PCI-E Connections	(MASTER)	(MASTER)
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65	84	ATI M56 PCI-E	(MASTER)	(MASTER)
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67	86	ATI M56 Core Power	(MASTER)	(MASTER)
68	87	ATI M56 Frame Buffer I/F	(MASTER)	(MASTER)
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70	89	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
71	90	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
72	91	ATI M56 GPIO/DVO/Misc	(MASTER)	(MASTER)
73	93	ATI M56 Video Interfaces	(MASTER)	(MASTER)
74	94	Internal Display Connectors	(MASTER)	(MASTER)
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77	100	Revision History	N/A	N/A
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80	103	M1 Spacing & Physical Constraints	(MASTER)	(MASTER)
81	104	M1 Net Properties	(MASTER)	(MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM, MULLET, M1	SCH		
820-1881	1	PCBF, MULLET, M1	PCB		
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:TSQ]	CRITICAL	VRAM_128
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:TYT]	CRITICAL	VRAM_256

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Mon Sep 26 13:38:08 2005

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X.XXX :	_____	ENG APPD	MFG APPD		
ANGLES :	_____	QA APPD	DESIGNER		
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 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				051-6941	REV. 07001
				SHT 1 OF 81	



System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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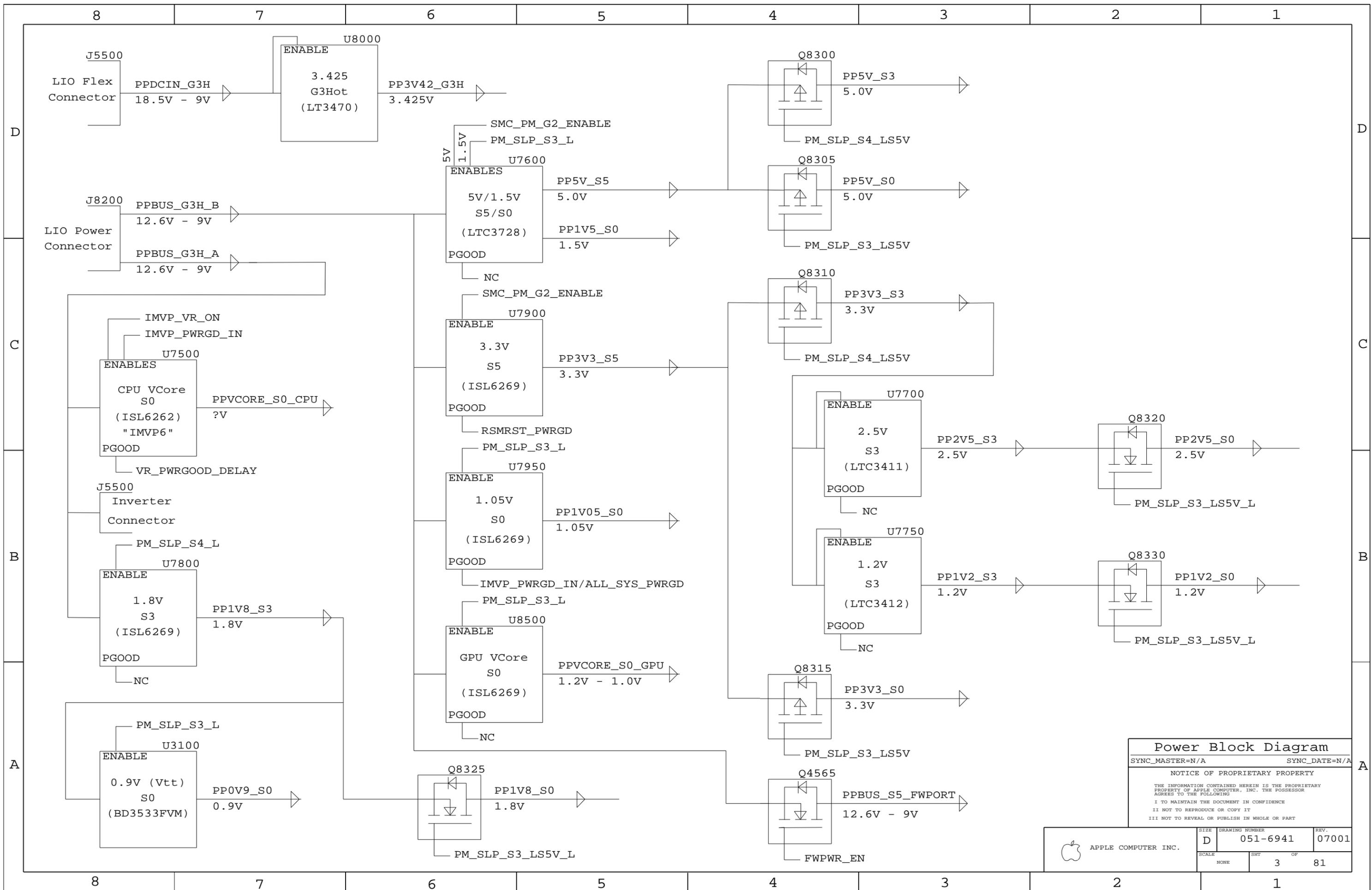
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	SCALE NONE	SH# 2	OF 81



Power Block Diagram
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT	OF	
NONE	3	81	

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<h3>Phantom BOM #'s</h3> <table border="1"> <thead> <tr> <th>PART NUMBER</th> <th>QTY</th> <th>DESCRIPTION</th> <th>REFERENCE DES</th> <th>CRITICAL</th> <th>BOM OPTION</th> </tr> </thead> <tbody> <tr> <td>075-0137</td> <td>1</td> <td>128, MULLET, M1</td> <td>BOM1</td> <td></td> <td>075-0137</td> </tr> <tr> <td>075-0138</td> <td>1</td> <td>256, MULLET, M1</td> <td>BOM2</td> <td></td> <td>075-0138</td> </tr> <tr> <td>075-0139</td> <td>1</td> <td>PROJ_PTS, MULLET, M1</td> <td>BOM3</td> <td></td> <td>075-0139</td> </tr> <tr> <td>075-0140</td> <td>1</td> <td>LEMENU_PTS, MULLET, M1</td> <td>BOM4</td> <td></td> <td>075-0140</td> </tr> </tbody> </table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	075-0137	1	128, MULLET, M1	BOM1		075-0137	075-0138	1	256, MULLET, M1	BOM2		075-0138	075-0139	1	PROJ_PTS, MULLET, M1	BOM3		075-0139	075-0140	1	LEMENU_PTS, MULLET, M1	BOM4		075-0140																								
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<h3>"LeMenu Stage #1" Parts</h3> <table border="1"> <thead> <tr> <th>PART NUMBER</th> <th>QTY</th> <th>DESCRIPTION</th> <th>REFERENCE DES</th> <th>CRITICAL</th> <th>BOM OPTION</th> </tr> </thead> <tbody> <tr> <td>338S0266</td> <td>1</td> <td>IC, ATI, M56P, GRPHSCTRL, 880BGA, LF</td> <td>U8400</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>338S0268</td> <td>1</td> <td>IC, FW32306, 1394A LINK, BGA, 129P</td> <td>U4400</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>338S0270</td> <td>1</td> <td>IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO</td> <td>U4101</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>338S0274</td> <td>1</td> <td>IC, SMC, HS8/2116</td> <td>U5800</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>341S1797</td> <td>1</td> <td>IC, EEPROM, SERIAL IIC, 8KBIT, SO8</td> <td>U4102</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>341S1812</td> <td>1</td> <td>IC, EFI, BOOTROM DEVELOPMENT, M1</td> <td>U6301</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>353S1235</td> <td>1</td> <td>IC, CPU VOLTAGE REGULATOR, IMPV, TWO PHASE</td> <td>U7530</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> <tr> <td>359S0101</td> <td>1</td> <td>IC, CY28445-5, CLOCK GEN, 68PIN QFN</td> <td>U3301</td> <td>CRITICAL</td> <td>LEMENU_STAGE1</td> </tr> </tbody> </table> <p>341S1813 is production BootROM</p>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	338S0266	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF	U8400	CRITICAL	LEMENU_STAGE1	338S0268	1	IC, FW32306, 1394A LINK, BGA, 129P	U4400	CRITICAL	LEMENU_STAGE1	338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1	338S0274	1	IC, SMC, HS8/2116	U5800	CRITICAL	LEMENU_STAGE1	341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL	LEMENU_STAGE1	341S1812	1	IC, EFI, BOOTROM DEVELOPMENT, M1	U6301	CRITICAL	LEMENU_STAGE1	353S1235	1	IC, CPU VOLTAGE REGULATOR, IMPV, TWO PHASE	U7530	CRITICAL	LEMENU_STAGE1	359S0101	1	IC, CY28445-5, CLOCK GEN, 68PIN QFN	U3301	CRITICAL	LEMENU_STAGE1
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338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1																																																								
338S0274	1	IC, SMC, HS8/2116	U5800	CRITICAL	LEMENU_STAGE1																																																								
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341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	LEMENU_STAGE2																																																								
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338S0269	1	IC, 945GM, SOUTHBRIDGE	U1200	CRITICAL	LEMENU_STAGE3																																																								
343S0385	1	IC, SB, 652BGA	U2100	CRITICAL	LEMENU_STAGE3																																																								
<table border="1"> <tr> <td colspan="3" style="text-align: center;">BOM Configuration</td> </tr> <tr> <td colspan="2">SYNC_MASTER=N/A</td> <td>SYNC_DATE=N/A</td> </tr> <tr> <td colspan="3" style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</td> </tr> <tr> <td colspan="3"> <small>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</small> </td> </tr> <tr> <td colspan="3"> <small>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</small> </td> </tr> <tr> <td colspan="3"> <small>II NOT TO REPRODUCE OR COPY IT</small> </td> </tr> <tr> <td colspan="3"> <small>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</small> </td> </tr> <tr> <td rowspan="2" style="text-align: center;">  APPLE COMPUTER INC. </td> <td>SIZE</td> <td>DRAWING NUMBER</td> </tr> <tr> <td>D</td> <td>051-6941</td> </tr> <tr> <td>SCALE</td> <td>SHT</td> <td>REV.</td> </tr> <tr> <td>NONE</td> <td>4 OF</td> <td>07001</td> </tr> <tr> <td></td> <td></td> <td>81</td> </tr> </table>								BOM Configuration			SYNC_MASTER=N/A		SYNC_DATE=N/A	NOTICE OF PROPRIETARY PROPERTY			<small>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</small>			<small>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</small>			<small>II NOT TO REPRODUCE OR COPY IT</small>			<small>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</small>			 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	D	051-6941	SCALE	SHT	REV.	NONE	4 OF	07001			81																			
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		81																																																											
8	7	6	5	4	3	2	1																																																						

Functional Test Points

Power Supply NO_TESTS

NO_TEST	Value	Pin
TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5V5S_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V0S0_COMP	60
TRUE	P1V0S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTS

NO_TEST	Value	Pin
TRUE	FSB_A_L<31..3>	7 12 81
TRUE	FSB_ADS_L	7 12 81
TRUE	FSB_ADSTB_L<1..0>	7 12 81
TRUE	FSB_BNR_L	7 12 81
TRUE	FSB_BREQ0_L	7 12 81
TRUE	FSB_D_L<63..0>	7 12 81
TRUE	FSB_DBSY_L	7 12 81
TRUE	FSB_DINV_L<3..0>	7 12 81
TRUE	FSB_DRDY_L	7 12 81
TRUE	FSB_DSTBN_L<3..0>	7 12 81
TRUE	FSB_DSTBP_L<3..0>	7 12 81
TRUE	FSB_HIT_L	7 12 81
TRUE	FSB_HITM_L	7 12 81
TRUE	FSB_LOCK_L	7 12 81
TRUE	FSB_REO_L<4..0>	7 12 81

Fan Connectors

FUNC_TEST	Pin
=PP5V_S0_FAN_LT	53 62
FAN_LT_PWM	53
FAN_LT_TACH	53
FAN_RT_PWM	53
FAN_RT_TACH	53

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Battery Digital Connector

FUNC_TEST	Pin	
TRUE	SMC_BS_ALERT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

LPC+ Debug Connector

FUNC_TEST	Pin	
TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 46 48 76
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORTB0_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST	Pin	
TRUE	=PP1V05_S0_REG	50 60 62

Left I/O Data Connector

FUNC_TEST	Pin	
TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S5_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 81
TRUE	ACZ_SDATAOUT	21 44 81
TRUE	ACZ_BITCLK	21 44 81
TRUE	ACZ_RST_L	21 44 81
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_ADAPTER_EN	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIEN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 81
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST	Pin	
TRUE	=PPBUS_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

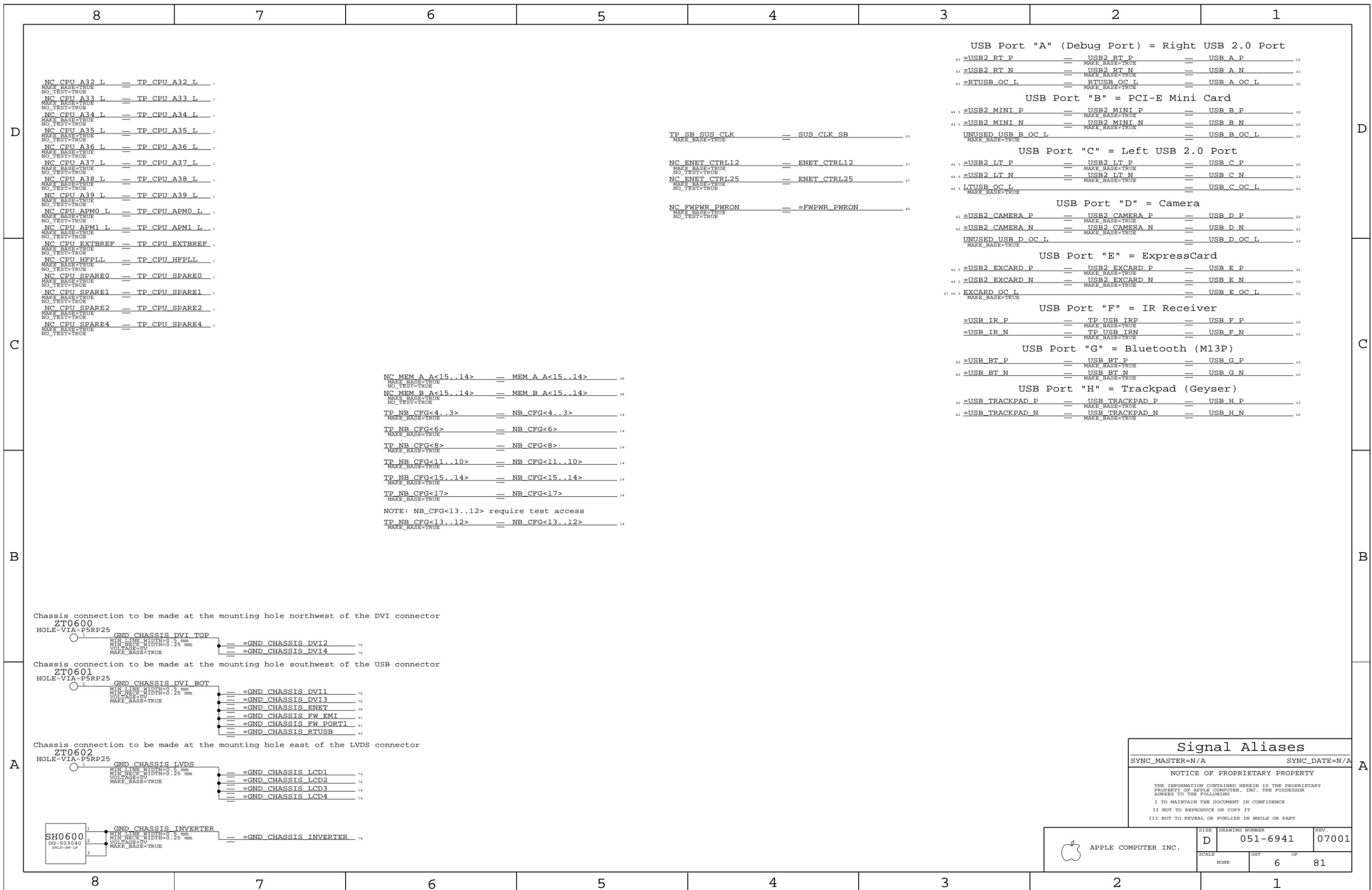
Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

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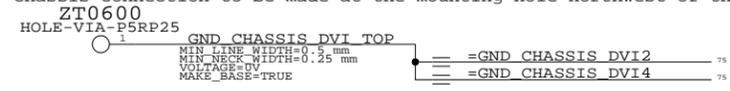
NC CPU A32 L == TP CPU A32 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A33 L == TP CPU A33 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A34 L == TP CPU A34 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A35 L == TP CPU A35 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A36 L == TP CPU A36 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A37 L == TP CPU A37 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A38 L == TP CPU A38 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU A39 L == TP CPU A39 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU APM0 L == TP CPU APM0 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU APM1 L == TP CPU APM1 L
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU EXTREF == TP CPU EXTREF
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU HFPLL == TP CPU HFPLL
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU SPARE0 == TP CPU SPARE0
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU SPARE1 == TP CPU SPARE1
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU SPARE2 == TP CPU SPARE2
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC CPU SPARE4 == TP CPU SPARE4
 MAKE_BASE=TRUE
 NO_TEST=TRUE

TP_SB_SUS_CLK == SUS_CLK_SB
 MAKE_BASE=TRUE
 NC_ENET_CTRL12 == ENET_CTRL12
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC_ENET_CTRL25 == ENET_CTRL25
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC_FWPWR_PWRON == FWPWR_PWRON
 MAKE_BASE=TRUE
 NO_TEST=TRUE

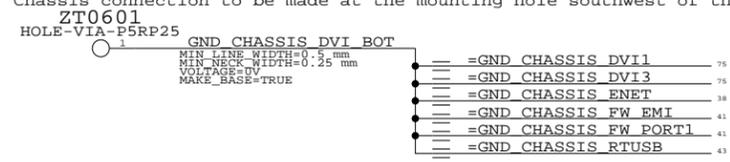
NC_MEM_A_A<15..14> == MEM_A_A<15..14>
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 NC_MEM_B_A<15..14> == MEM_B_A<15..14>
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP_NB_CFG<4..3> == NB_CFG<4..3>
 MAKE_BASE=TRUE
 TP_NB_CFG<6> == NB_CFG<6>
 MAKE_BASE=TRUE
 TP_NB_CFG<8> == NB_CFG<8>
 MAKE_BASE=TRUE
 TP_NB_CFG<11..10> == NB_CFG<11..10>
 MAKE_BASE=TRUE
 TP_NB_CFG<15..14> == NB_CFG<15..14>
 MAKE_BASE=TRUE
 TP_NB_CFG<17> == NB_CFG<17>
 MAKE_BASE=TRUE
 NOTE: NB_CFG<13..12> require test access
 TP_NB_CFG<13..12> == NB_CFG<13..12>
 MAKE_BASE=TRUE

USB Port "A" (Debug Port) = Right USB 2.0 Port
 =USB2_RT_P == USB2_RT_P == USB_A_P
 MAKE_BASE=TRUE
 =USB2_RT_N == USB2_RT_N == USB_A_N
 MAKE_BASE=TRUE
 =RTUSB_OC_L == RTUSB_OC_L == USB_A_OC_L
 MAKE_BASE=TRUE
 USB Port "B" = PCI-E Mini Card
 =USB2_MINI_P == USB2_MINI_P == USB_B_P
 MAKE_BASE=TRUE
 =USB2_MINI_N == USB2_MINI_N == USB_B_N
 MAKE_BASE=TRUE
 UNUSED_USB_B_OC_L == USB_B_OC_L
 MAKE_BASE=TRUE
 USB Port "C" = Left USB 2.0 Port
 =USB2_LT_P == USB2_LT_P == USB_C_P
 MAKE_BASE=TRUE
 =USB2_LT_N == USB2_LT_N == USB_C_N
 MAKE_BASE=TRUE
 LTUSB_OC_L == USB_C_OC_L
 MAKE_BASE=TRUE
 USB Port "D" = Camera
 =USB2_CAMERA_P == USB2_CAMERA_P == USB_D_P
 MAKE_BASE=TRUE
 =USB2_CAMERA_N == USB2_CAMERA_N == USB_D_N
 MAKE_BASE=TRUE
 UNUSED_USB_D_OC_L == USB_D_OC_L
 MAKE_BASE=TRUE
 USB Port "E" = ExpressCard
 =USB2_EXCARD_P == USB2_EXCARD_P == USB_E_P
 MAKE_BASE=TRUE
 =USB2_EXCARD_N == USB2_EXCARD_N == USB_E_N
 MAKE_BASE=TRUE
 EXCARD_OC_L == USB_E_OC_L
 MAKE_BASE=TRUE
 USB Port "F" = IR Receiver
 =USB_IR_P == TP_USB_IRP == USB_F_P
 MAKE_BASE=TRUE
 =USB_IR_N == TP_USB_IRN == USB_F_N
 MAKE_BASE=TRUE
 USB Port "G" = Bluetooth (M13P)
 =USB_BT_P == USB_BT_P == USB_G_P
 MAKE_BASE=TRUE
 =USB_BT_N == USB_BT_N == USB_G_N
 MAKE_BASE=TRUE
 USB Port "H" = Trackpad (Geyser)
 =USB_TRACKPAD_P == USB_TRACKPAD_P == USB_H_P
 MAKE_BASE=TRUE
 =USB_TRACKPAD_N == USB_TRACKPAD_N == USB_H_N
 MAKE_BASE=TRUE

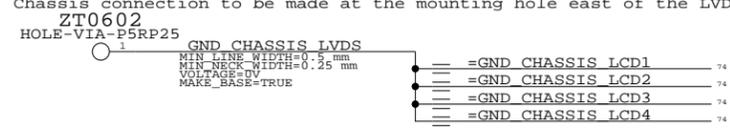
Chassis connection to be made at the mounting hole northwest of the DVI connector



Chassis connection to be made at the mounting hole southwest of the USB connector

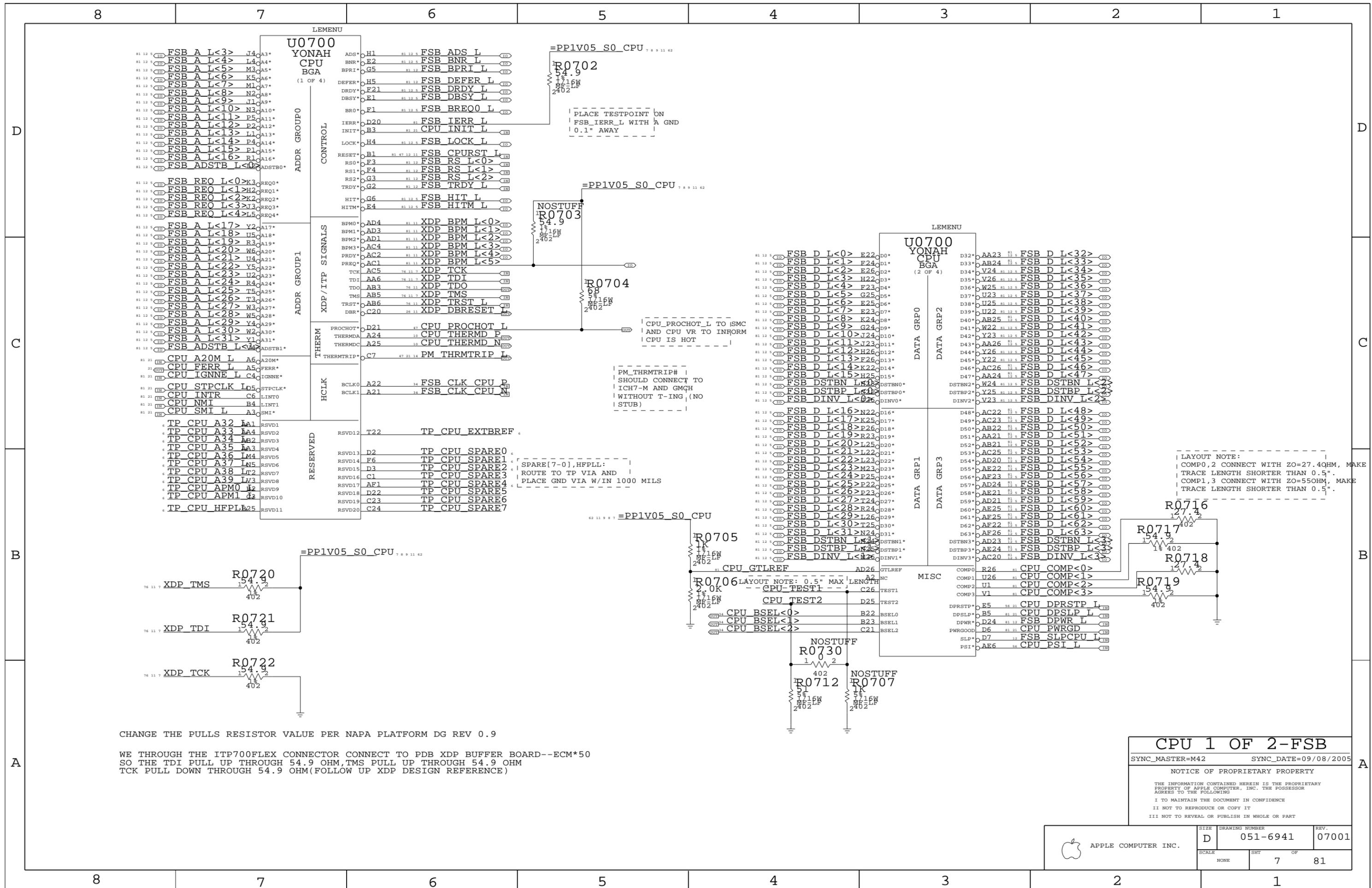


Chassis connection to be made at the mounting hole east of the LVDS connector



Signal Aliases	
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CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
 SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM
 TCK PULL DOWN THROUGH 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

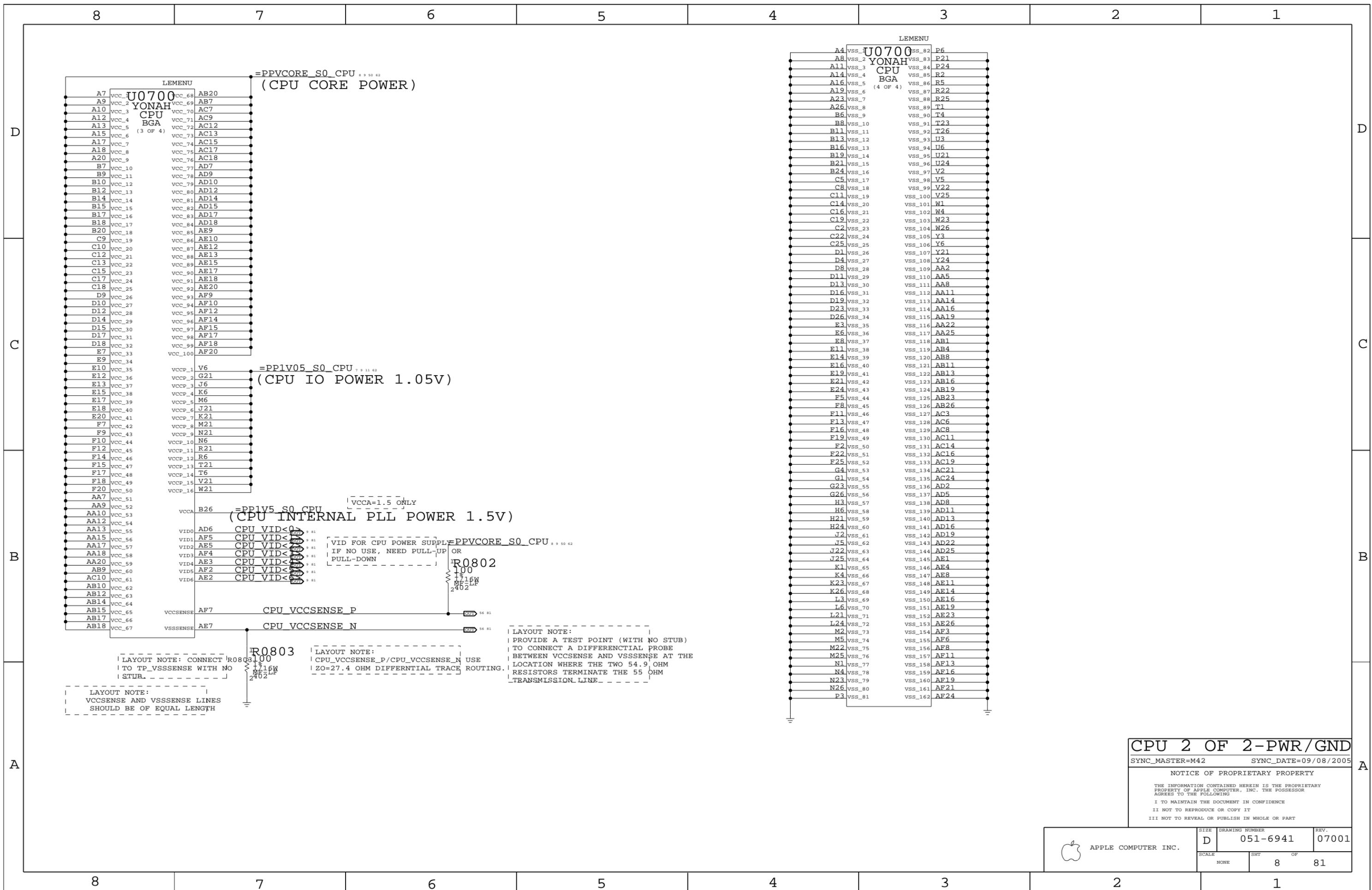
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=PPVCORE_S0_CPU (CPU CORE POWER)

=PP1V05_S0_CPU (CPU IO POWER 1.05V)

=PP1V5_S0_CPU (CPU INTERNAL PLL POWER 1.5V)

VID FOR CPU POWER SUPPLY =PPVCORE_S0_CPU
 IF NO USE, NEED PULL-UP OR PULL-DOWN

LAYOUT NOTE:
 PROVIDE A TEST POINT (WITH NO STUB)
 TO CONNECT A DIFFERENTIAL PROBE
 BETWEEN VCCSENSE AND VSSSENSE AT THE
 LOCATION WHERE THE TWO 54.9 OHM
 RESISTORS TERMINATE THE 55 OHM
 TRANSMISSION LINE

LAYOUT NOTE: CONNECT R0803 TO TP_VSSSENSE WITH NO STUB

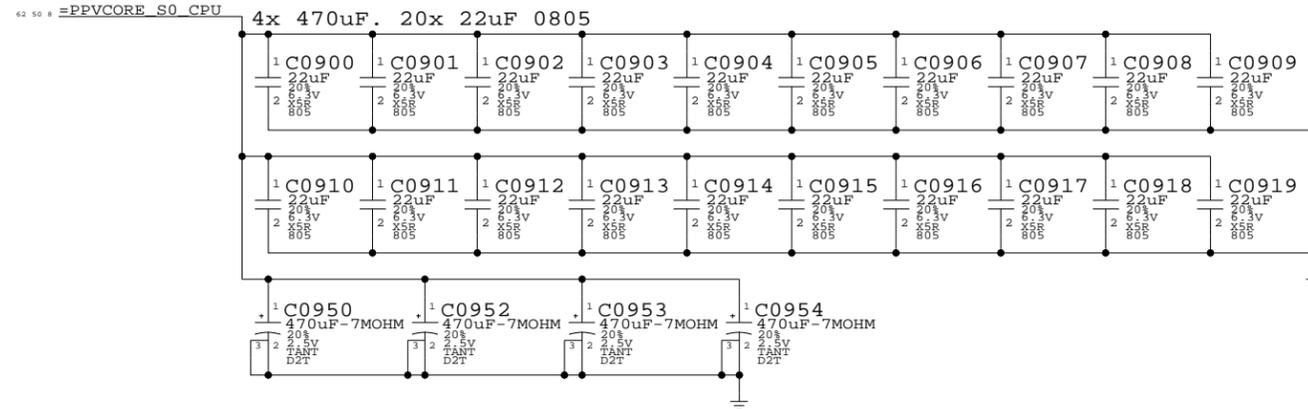
LAYOUT NOTE: VCCSENSE AND VSSSENSE LINES SHOULD BE OF EQUAL LENGTH

CPU 2 OF 2-PWR/GND
 SYNC_MASTER=M42 SYNC_DATE=09/08/2005

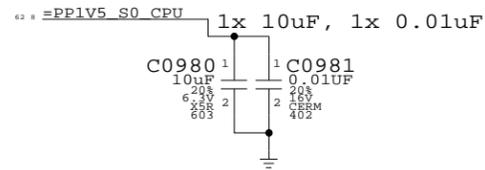
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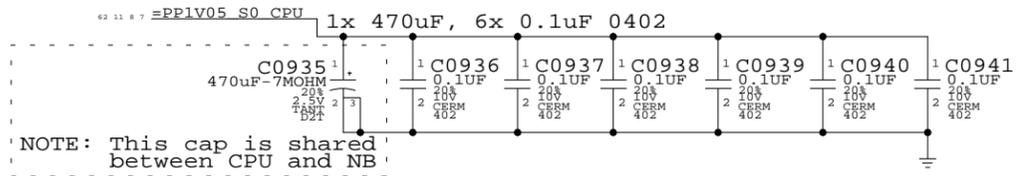
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

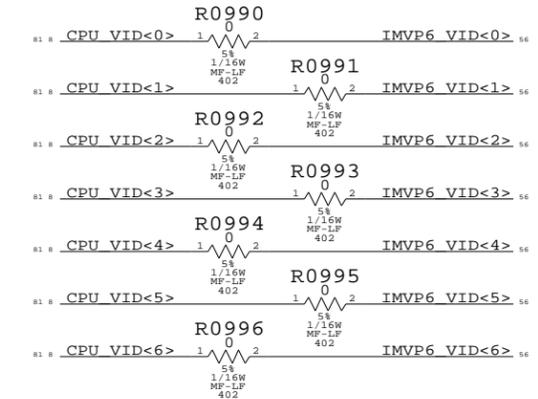


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
 Will probably be removed before production



CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D

C

C

B

B

A

A

8

7

6

5

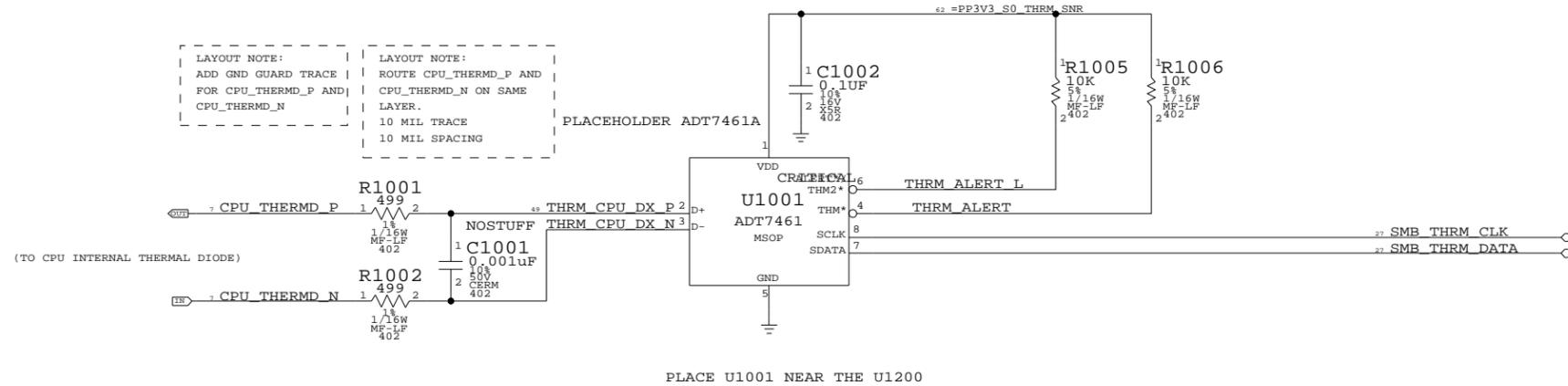
4

3

2

1

CPU ZONE THERMAL SENSOR



CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42 SYNC_DATE=09/08/2005

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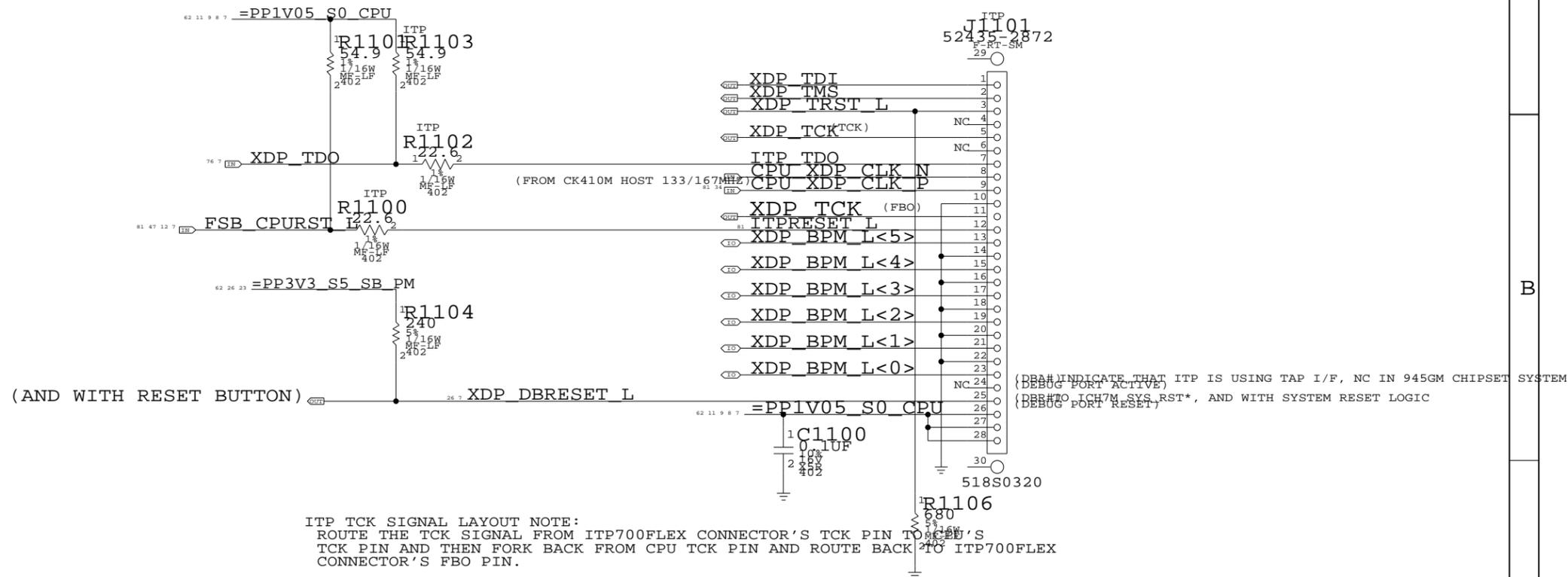
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CPU ITP700FLEX DEBUG SUPPORT

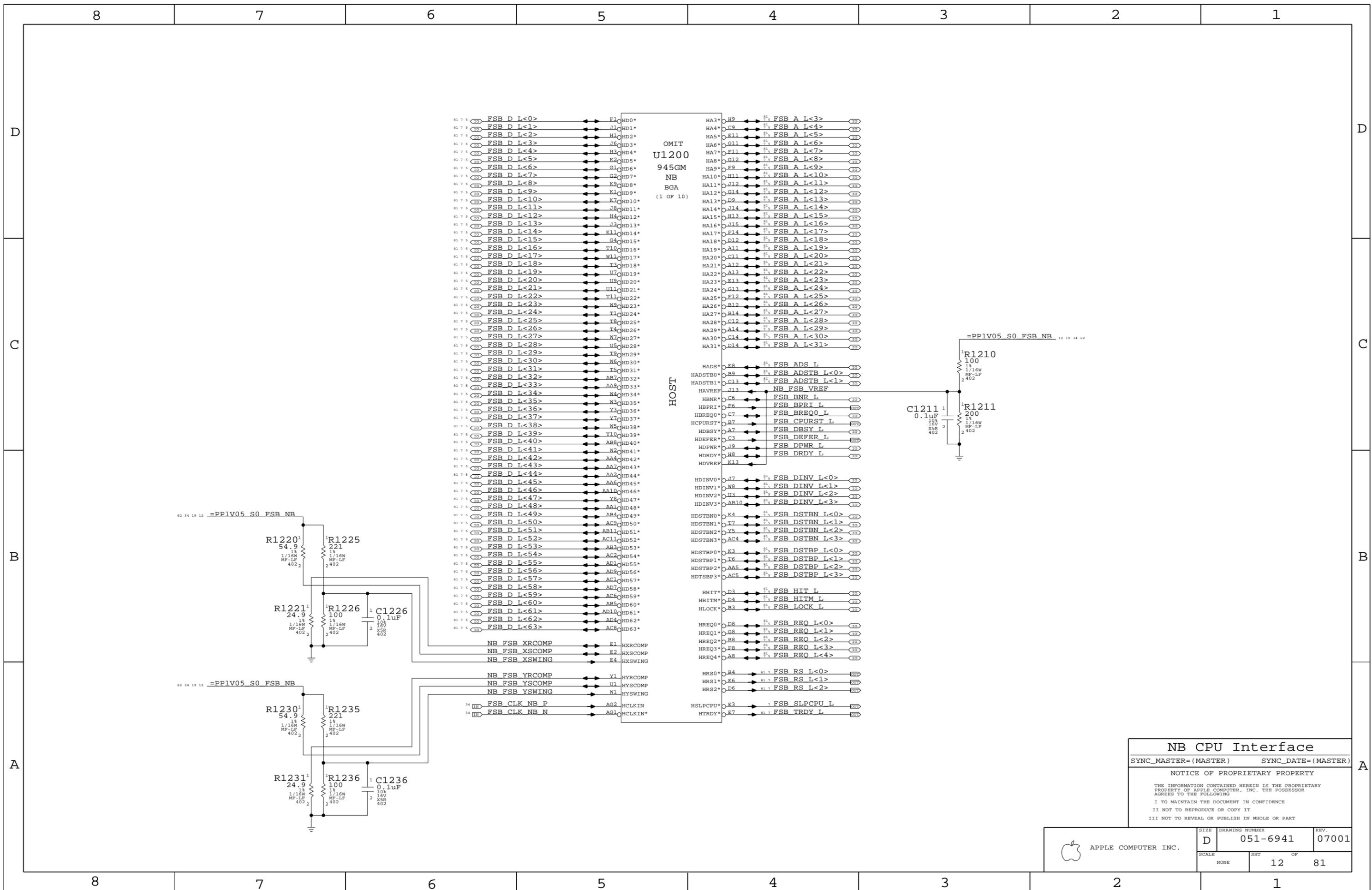


CPU ITP700FLEX DEBUG

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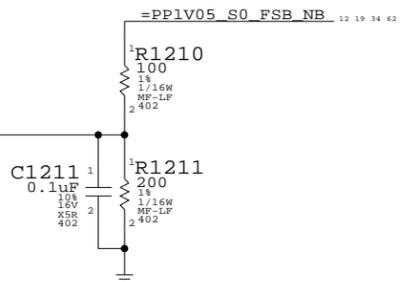
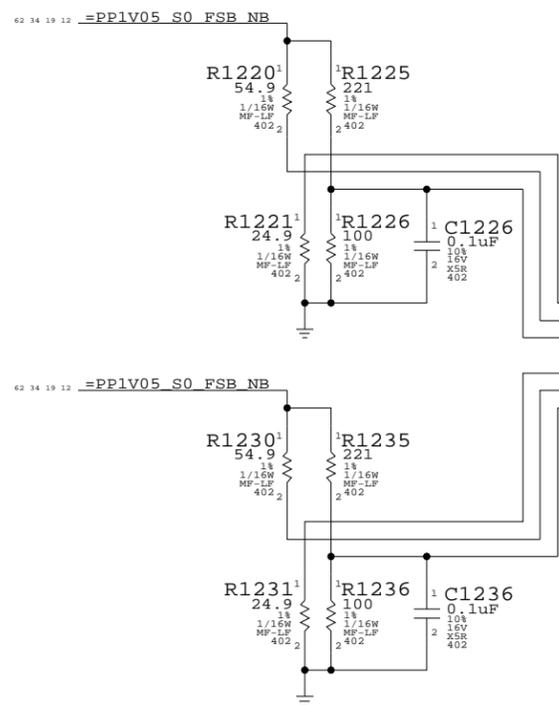
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		11	81



OMIT
U1200
945GM
NB
BGA
(1 OF 10)

HOST

81 7 5	FSB D L<0>	F1	HD0*	HA3*	H9	FSB A L<3>	EA
81 7 6	FSB D L<1>	J1	HD1*	HA4*	C9	FSB A L<4>	EA
81 7 7	FSB D L<2>	H1	HD2*	HA5*	E11	FSB A L<5>	EA
81 7 8	FSB D L<3>	J5	HD3*	HA6*	G11	FSB A L<6>	EA
81 7 9	FSB D L<4>	H1	HD4*	HA7*	F11	FSB A L<7>	EA
81 7 10	FSB D L<5>	K2	HD5*	HA8*	G12	FSB A L<8>	EA
81 7 11	FSB D L<6>	G1	HD6*	HA9*	F9	FSB A L<9>	EA
81 7 12	FSB D L<7>	G2	HD7*	HA10*	H11	FSB A L<10>	EA
81 7 13	FSB D L<8>	K9	HD8*	HA11*	J12	FSB A L<11>	EA
81 7 14	FSB D L<9>	K1	HD9*	HA12*	G14	FSB A L<12>	EA
81 7 15	FSB D L<10>	K7	HD10*	HA13*	D9	FSB A L<13>	EA
81 7 16	FSB D L<11>	J8	HD11*	HA14*	J14	FSB A L<14>	EA
81 7 17	FSB D L<12>	H4	HD12*	HA15*	H13	FSB A L<15>	EA
81 7 18	FSB D L<13>	J1	HD13*	HA16*	J15	FSB A L<16>	EA
81 7 19	FSB D L<14>	K11	HD14*	HA17*	F14	FSB A L<17>	EA
81 7 20	FSB D L<15>	G4	HD15*	HA18*	D12	FSB A L<18>	EA
81 7 21	FSB D L<16>	T10	HD16*	HA19*	A11	FSB A L<19>	EA
81 7 22	FSB D L<17>	W11	HD17*	HA20*	C11	FSB A L<20>	EA
81 7 23	FSB D L<18>	T3	HD18*	HA21*	A12	FSB A L<21>	EA
81 7 24	FSB D L<19>	U7	HD19*	HA22*	A13	FSB A L<22>	EA
81 7 25	FSB D L<20>	U9	HD20*	HA23*	E13	FSB A L<23>	EA
81 7 26	FSB D L<21>	U11	HD21*	HA24*	G13	FSB A L<24>	EA
81 7 27	FSB D L<22>	T11	HD22*	HA25*	F12	FSB A L<25>	EA
81 7 28	FSB D L<23>	W9	HD23*	HA26*	B12	FSB A L<26>	EA
81 7 29	FSB D L<24>	T1	HD24*	HA27*	B14	FSB A L<27>	EA
81 7 30	FSB D L<25>	T8	HD25*	HA28*	C12	FSB A L<28>	EA
81 7 31	FSB D L<26>	T4	HD26*	HA29*	A14	FSB A L<29>	EA
81 7 32	FSB D L<27>	W7	HD27*	HA30*	C14	FSB A L<30>	EA
81 7 33	FSB D L<28>	U5	HD28*	HA31*	D14	FSB A L<31>	EA
81 7 34	FSB D L<29>	T9	HD29*				
81 7 35	FSB D L<30>	W6	HD30*	HADS*	E8	FSB ADS L	EA
81 7 36	FSB D L<31>	T5	HD31*	HADSTB0*	B9	FSB ADSTB L<0>	EA
81 7 37	FSB D L<32>	AB7	HD32*	HADSTB1*	C13	FSB ADSTB L<1>	EA
81 7 38	FSB D L<33>	AA9	HD33*	HAVREF	J13	NB FSB VREF	EA
81 7 39	FSB D L<34>	WA	HD34*	HBNR*	C6	FSB BNR L	EA
81 7 40	FSB D L<35>	W1	HD35*	HBPR1*	E6	FSB BPRI L	EA
81 7 41	FSB D L<36>	Y1	HD36*	HBREQ0*	C7	FSB BREQ0 L	EA
81 7 42	FSB D L<37>	Y7	HD37*	HCPURST*	B7	FSB CPURST L	EA
81 7 43	FSB D L<38>	W8	HD38*	HDBSY*	A7	FSB DBSY L	EA
81 7 44	FSB D L<39>	Y10	HD39*	HDEFER*	C3	FSB DEFER L	EA
81 7 45	FSB D L<40>	AB8	HD40*	HDPWR*	J9	FSB DPWR L	EA
81 7 46	FSB D L<41>	W2	HD41*	HDRDY*	H8	FSB DRDY L	EA
81 7 47	FSB D L<42>	AA4	HD42*	HDRVREF	K13		EA
81 7 48	FSB D L<43>	AA7	HD43*				
81 7 49	FSB D L<44>	AA2	HD44*				
81 7 50	FSB D L<45>	AA6	HD45*	HDINV0*	J7	FSB DINV L<0>	EA
81 7 51	FSB D L<46>	AA11	HD46*	HDINV1*	W8	FSB DINV L<1>	EA
81 7 52	FSB D L<47>	Y8	HD47*	HDINV2*	U3	FSB DINV L<2>	EA
81 7 53	FSB D L<48>	AA1	HD48*	HDINV3*	AB10	FSB DINV L<3>	EA
81 7 54	FSB D L<49>	AB4	HD49*	HDSTBN0*	K4	FSB DSTBN L<0>	EA
81 7 55	FSB D L<50>	AC9	HD50*	HDSTBN1*	T7	FSB DSTBN L<1>	EA
81 7 56	FSB D L<51>	AB11	HD51*	HDSTBN2*	Y5	FSB DSTBN L<2>	EA
81 7 57	FSB D L<52>	AC11	HD52*	HDSTBN3*	AC4	FSB DSTBN L<3>	EA
81 7 58	FSB D L<53>	AB3	HD53*	HDSTBP0*	K3	FSB DSTBP L<0>	EA
81 7 59	FSB D L<54>	AC2	HD54*	HDSTBP1*	T6	FSB DSTBP L<1>	EA
81 7 60	FSB D L<55>	AD1	HD55*	HDSTBP2*	AA5	FSB DSTBP L<2>	EA
81 7 61	FSB D L<56>	AD2	HD56*	HDTSBP3*	AC5	FSB DSTBP L<3>	EA
81 7 62	FSB D L<57>	AC1	HD57*				
81 7 63	FSB D L<58>	AD7	HD58*	HHIT*	D3	FSB HIT L	EA
81 7 64	FSB D L<59>	AC6	HD59*	HHITM*	D4	FSB HITM L	EA
81 7 65	FSB D L<60>	AB5	HD60*	HLOCK*	B3	FSB LOCK L	EA
81 7 66	FSB D L<61>	AD10	HD61*				
81 7 67	FSB D L<62>	AD4	HD62*	HREQ0*	D8	FSB REQ L<0>	EA
81 7 68	FSB D L<63>	AC8	HD63*	HREQ1*	G8	FSB REQ L<1>	EA
				HREQ2*	B8	FSB REQ L<2>	EA
				HREQ3*	F8	FSB REQ L<3>	EA
				HREQ4*	A8	FSB REQ L<4>	EA
				HRS0*	B4	FSB RS L<0>	EA
				HRS1*	E6	FSB RS L<1>	EA
				HRS2*	D6	FSB RS L<2>	EA
				HSLPCPU*	E3	FSB SLPCPU L	EA
				HTRDY*	E7	FSB TRDY L	EA



NB CPU Interface
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		SHT: 12	OF: 81

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

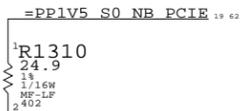
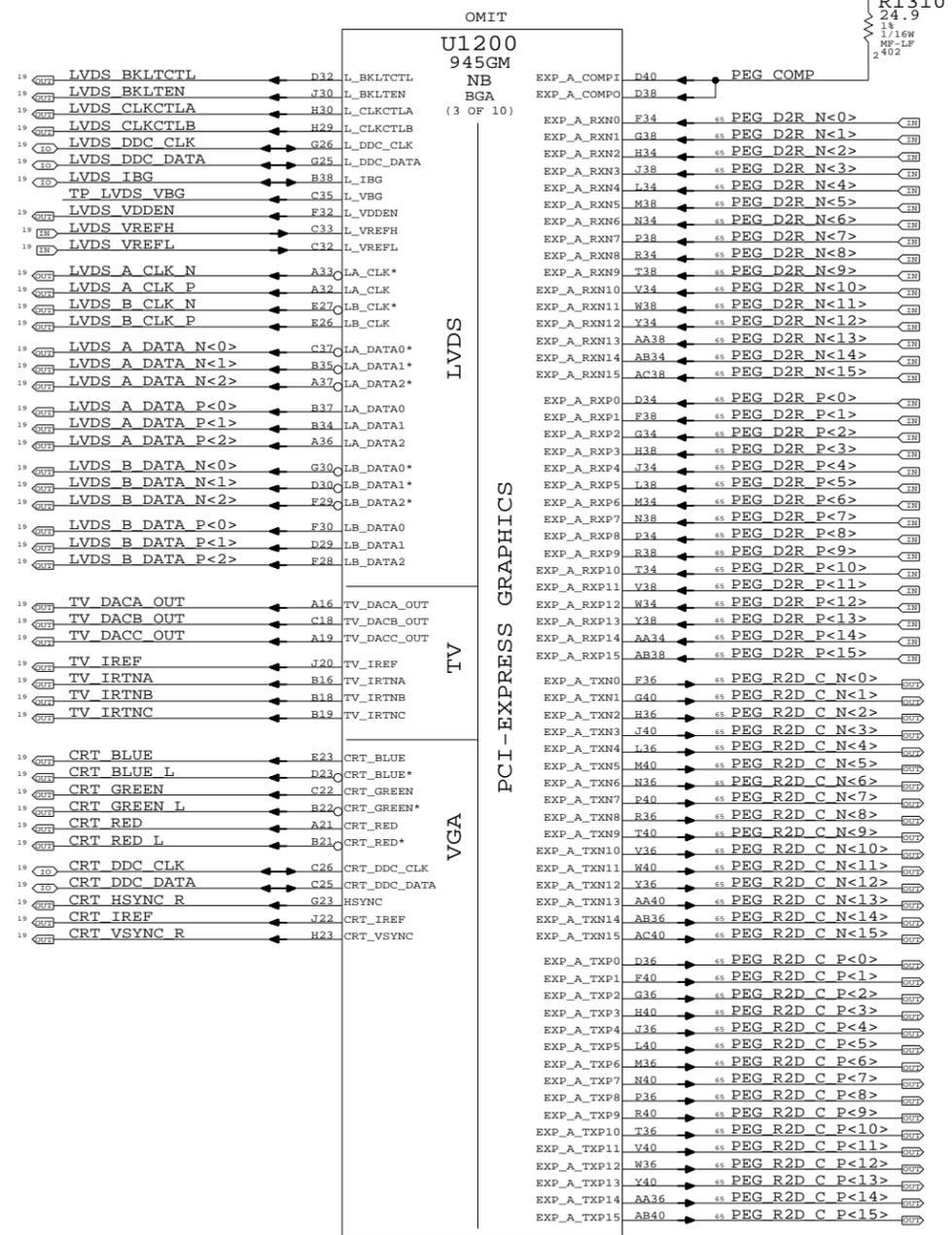
Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

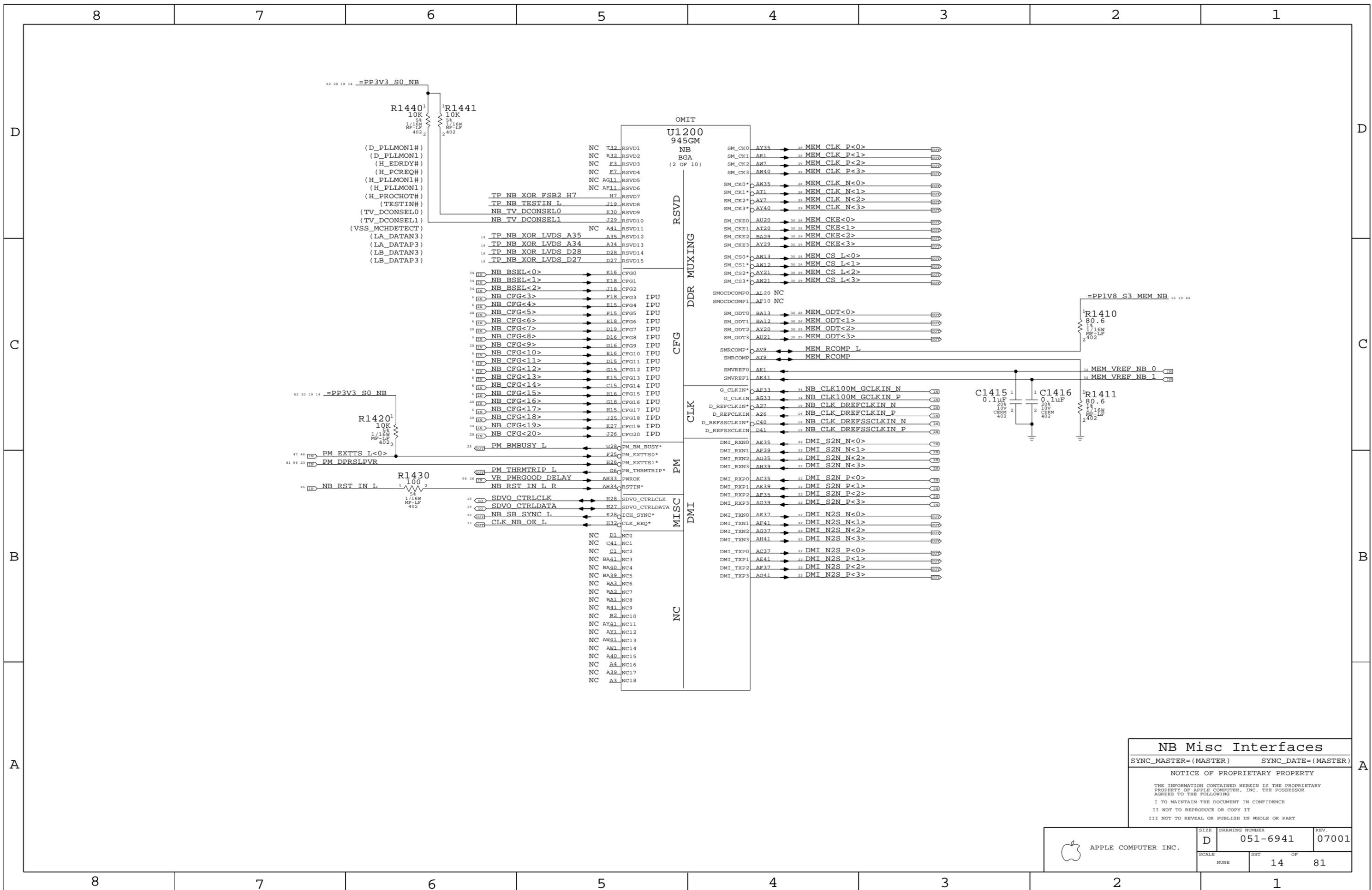
SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces
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		13	81



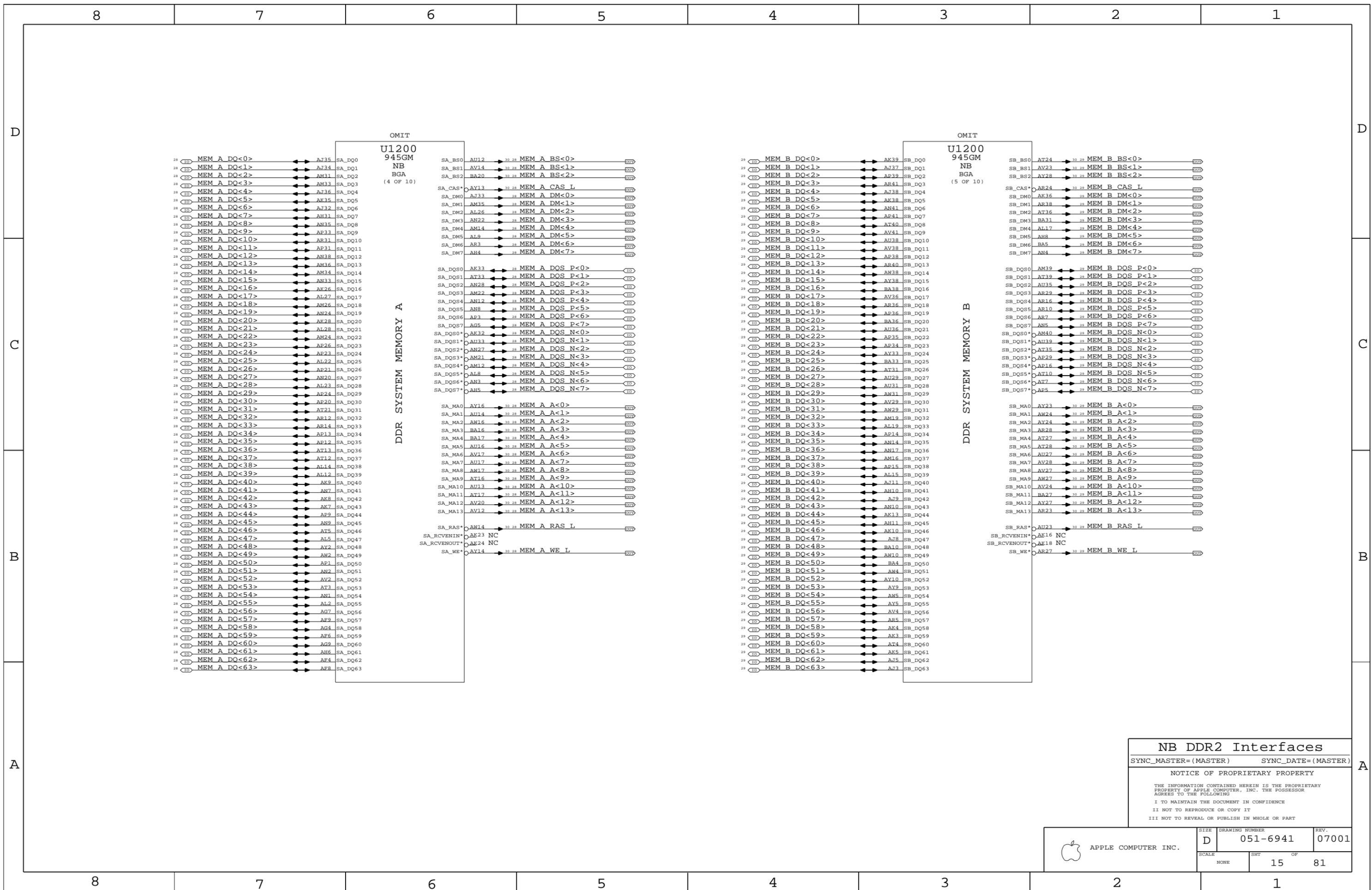
NB Misc Interfaces
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NONE	14	81	



NB DDR2 Interfaces
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NCTF balls are Not Critical To Function

These connections can break without impacting part performance. OMIT

62 19 16 =PPVCORE S0 NB

U1200 945GM NB BGA (7 OF 10)

NCTF

VCC_NCTF0 AE27
VCC_NCTF1 AE26
VCC_NCTF2 AE25
VCC_NCTF3 AE24
VCC_NCTF4 AE23
VCC_NCTF5 AE22
VCC_NCTF6 AE21
VCC_NCTF7 AE20
VCC_NCTF8 AE19
VCC_NCTF9 AE18
VCC_NCTF10 AC17
VCC_NCTF11 Y17
VCC_NCTF12 U17

VSS_NCTF0 AE27
VSS_NCTF1 AE26
VSS_NCTF2 AE25
VSS_NCTF3 AE24
VSS_NCTF4 AE23
VSS_NCTF5 AE22
VSS_NCTF6 AE21
VSS_NCTF7 AE20
VSS_NCTF8 AE19
VSS_NCTF9 AE18
VSS_NCTF10 AC17
VSS_NCTF11 Y17
VSS_NCTF12 U17

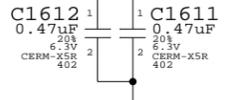
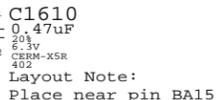
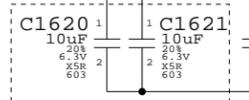
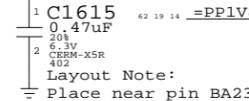
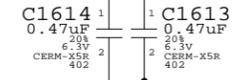
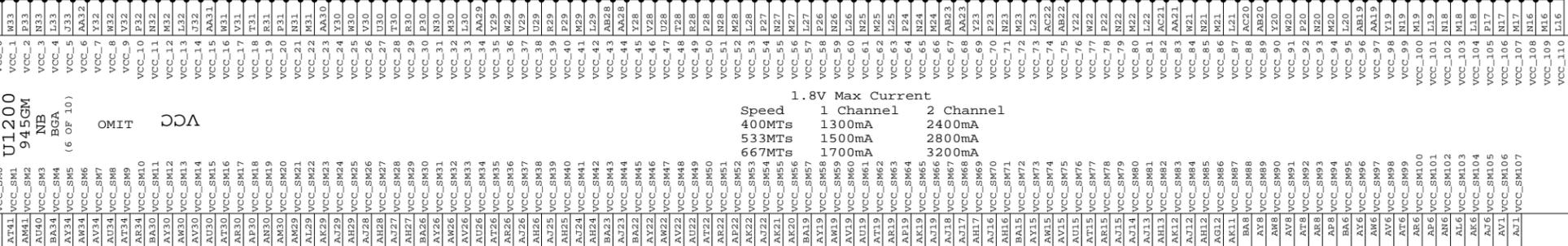
VCCAUX_NCTF0 AG27
VCCAUX_NCTF1 AF27
VCCAUX_NCTF2 AG26
VCCAUX_NCTF3 AF26
VCCAUX_NCTF4 AG25
VCCAUX_NCTF5 AF25
VCCAUX_NCTF6 AG24
VCCAUX_NCTF7 AF24
VCCAUX_NCTF8 AG23
VCCAUX_NCTF9 AF23
VCCAUX_NCTF10 AG22
VCCAUX_NCTF11 AF22
VCCAUX_NCTF12 AG21
VCCAUX_NCTF13 AF21
VCCAUX_NCTF14 AG20
VCCAUX_NCTF15 AF20
VCCAUX_NCTF16 AG19
VCCAUX_NCTF17 AF19
VCCAUX_NCTF18 R19
VCCAUX_NCTF19 AG18
VCCAUX_NCTF20 AF18
VCCAUX_NCTF21 R18
VCCAUX_NCTF22 AG17
VCCAUX_NCTF23 AF17
VCCAUX_NCTF24 AE17
VCCAUX_NCTF25 AD17
VCCAUX_NCTF26 AB17
VCCAUX_NCTF27 AA17
VCCAUX_NCTF28 W17
VCCAUX_NCTF29 V17
VCCAUX_NCTF30 T17
VCCAUX_NCTF31 R17
VCCAUX_NCTF32 AG16
VCCAUX_NCTF33 AF16
VCCAUX_NCTF34 AE16
VCCAUX_NCTF35 AD16
VCCAUX_NCTF36 AC16
VCCAUX_NCTF37 AB16
VCCAUX_NCTF38 AA16
VCCAUX_NCTF39 Y16
VCCAUX_NCTF40 W16
VCCAUX_NCTF41 V16
VCCAUX_NCTF42 U16
VCCAUX_NCTF43 T16
VCCAUX_NCTF44 R16
VCCAUX_NCTF45 AG15
VCCAUX_NCTF46 AF15
VCCAUX_NCTF47 AE15
VCCAUX_NCTF48 AD15
VCCAUX_NCTF49 AC15
VCCAUX_NCTF50 AB15
VCCAUX_NCTF51 AA15
VCCAUX_NCTF52 Y15
VCCAUX_NCTF53 W15
VCCAUX_NCTF54 V15
VCCAUX_NCTF55 U15
VCCAUX_NCTF56 T15
VCCAUX_NCTF57 R15

=PP1V5 S0 NB VCCAUX 17 19 62

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

=PPVCORE S0 NB 16 19 62
1.05V or 1.5V

1.8V Max Current
Speed 1 Channel 2 Channel
400MTs 1300mA 2400mA
533MTs 1500mA 2800mA
667MTs 1700mA 3200mA



Layout Note:
Place near pin BA23

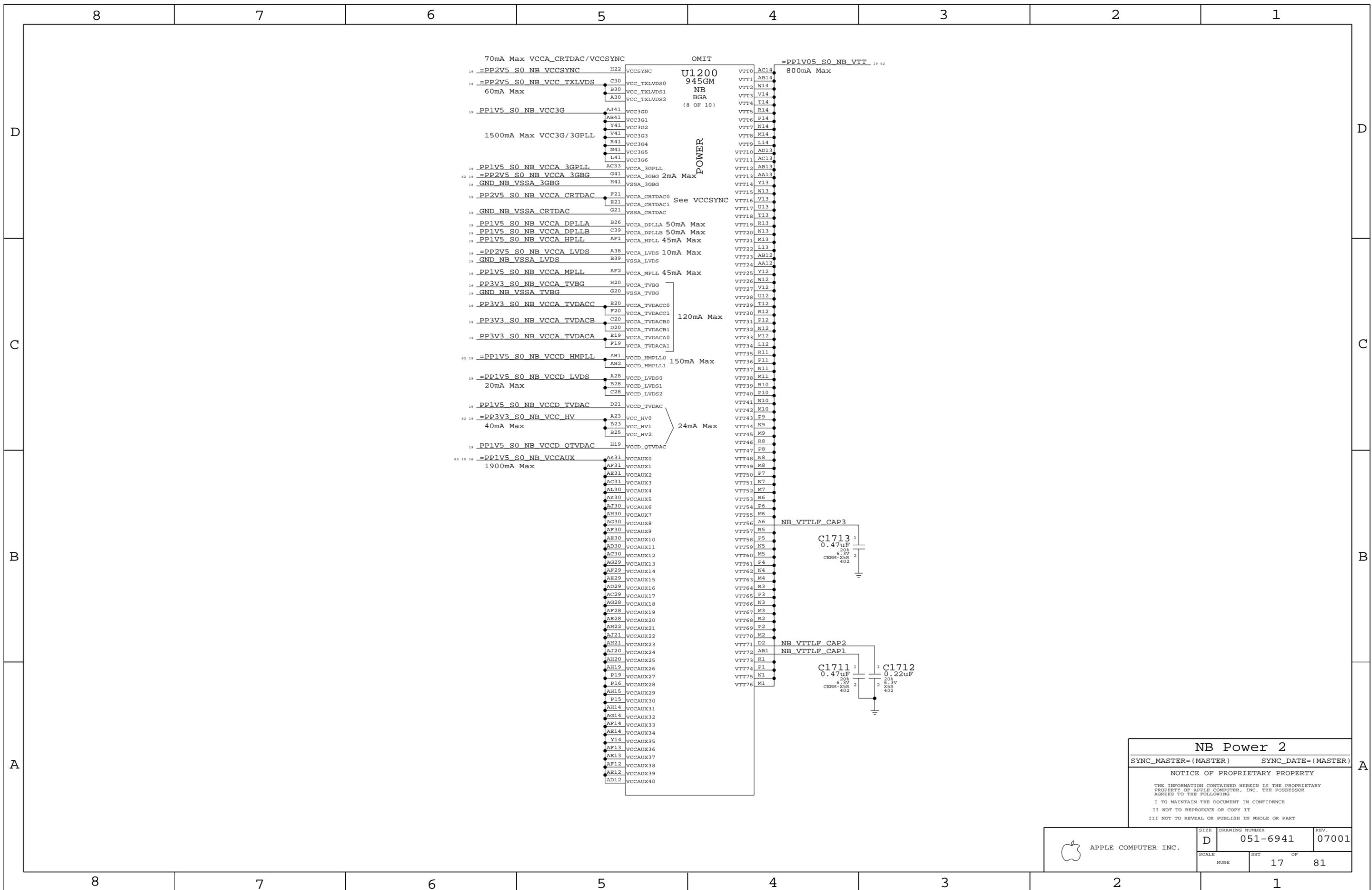
Layout Note:
Place in cavity

Layout Note:
Place near pin BA15

NB Power 1
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	16	81	



NB Power 2

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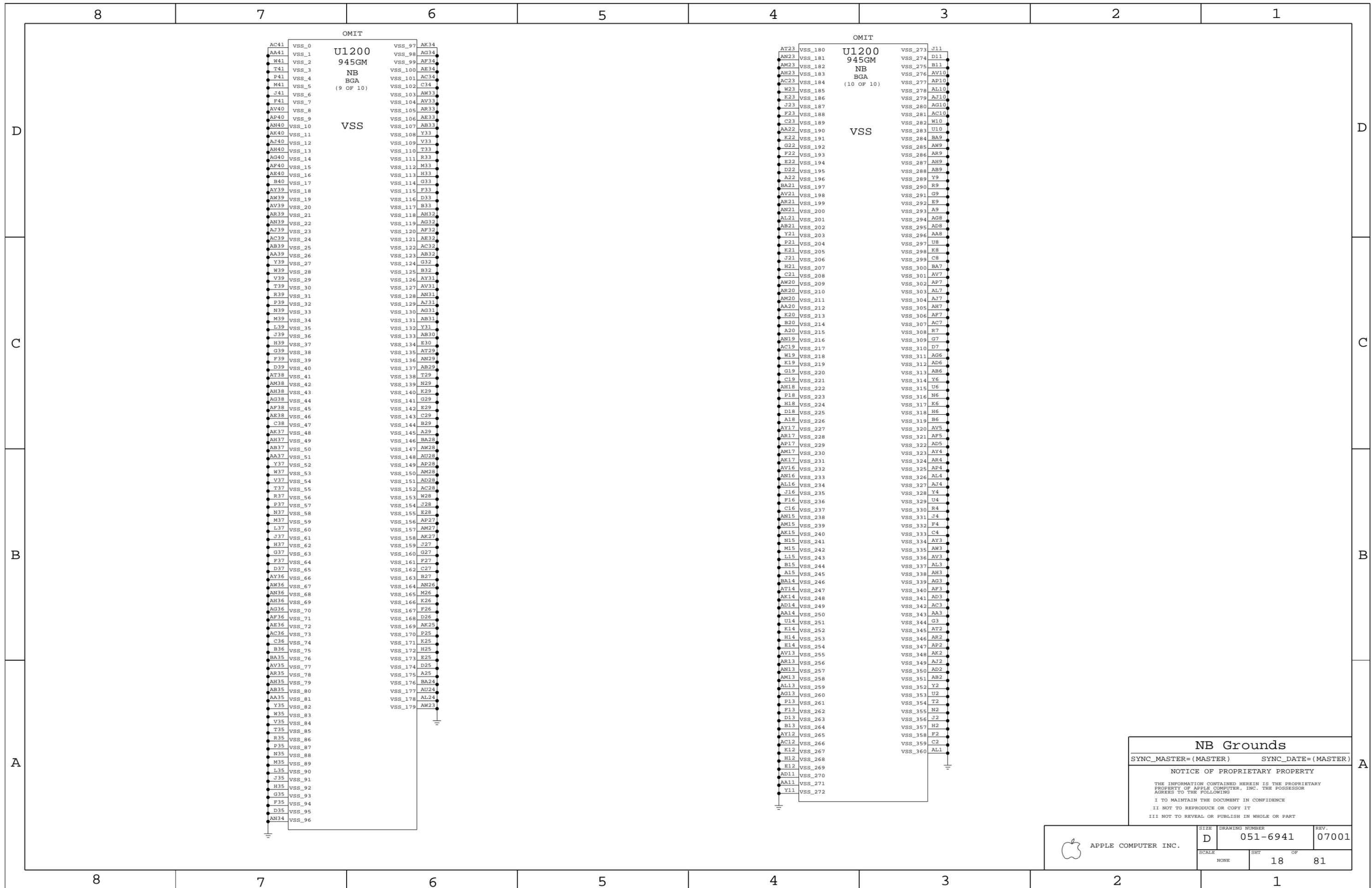
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	SCALE NONE	SHT OF 17	OF 81



NB Grounds
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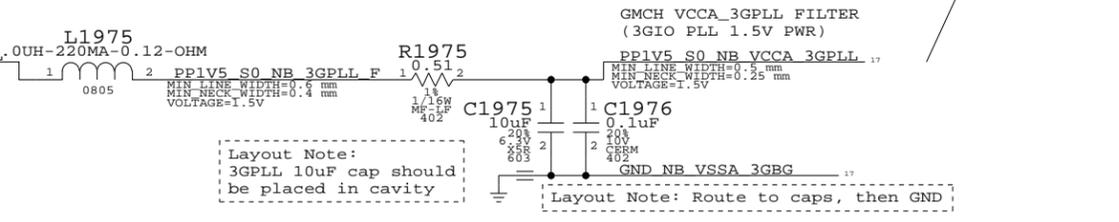
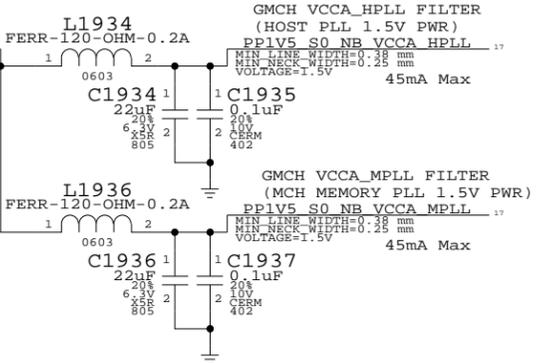
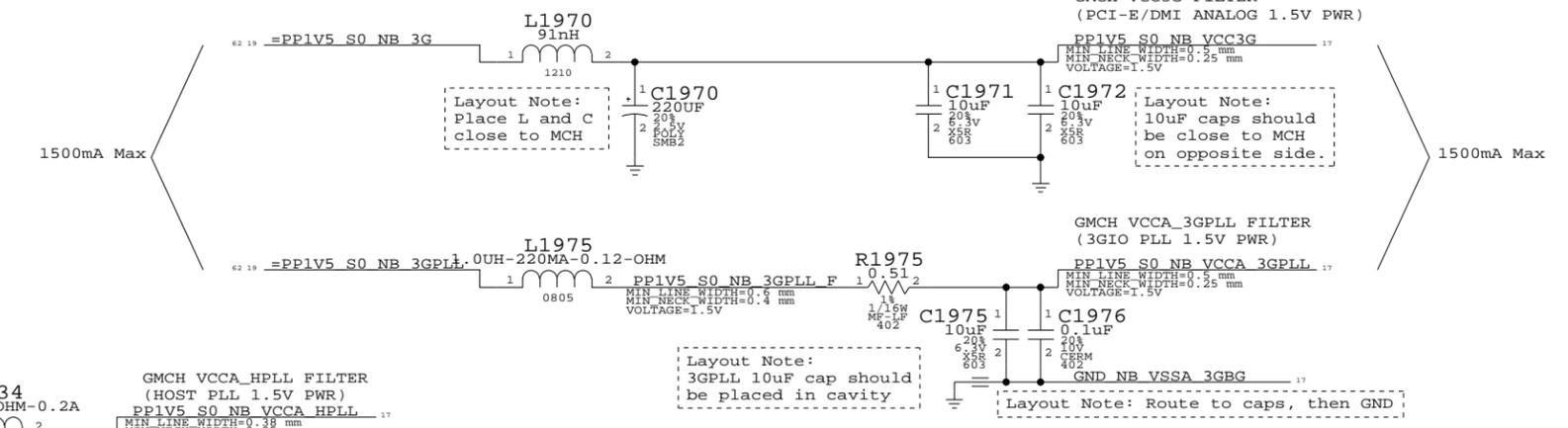
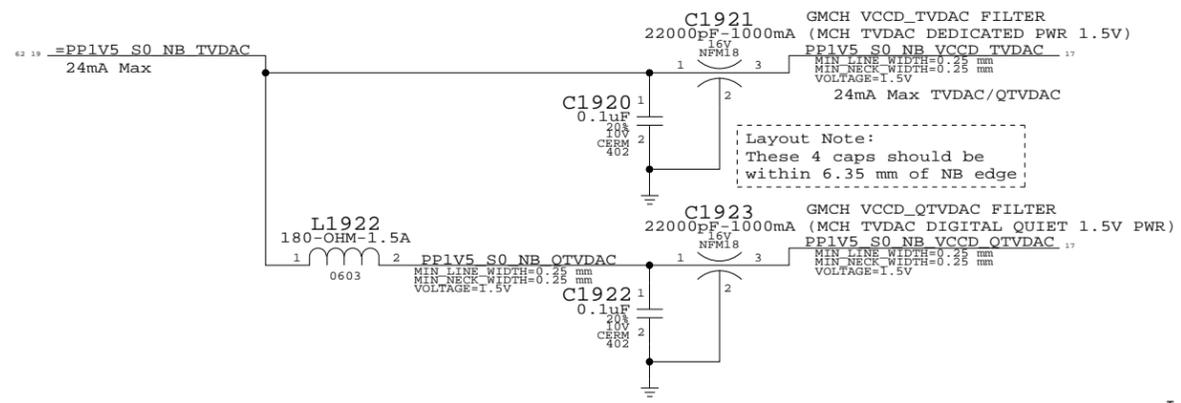
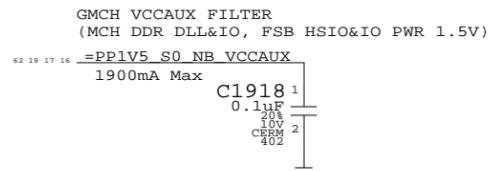
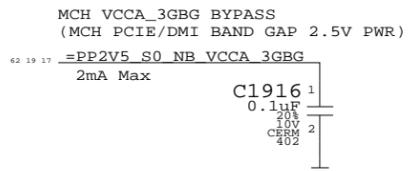
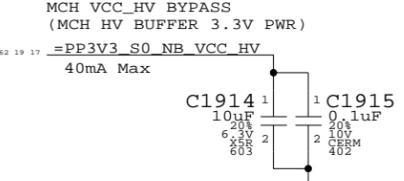
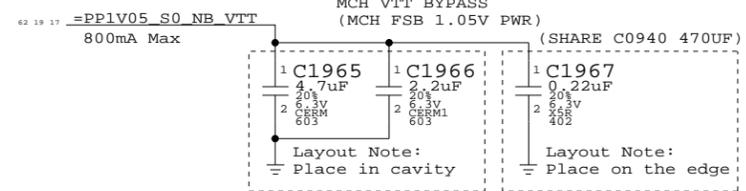
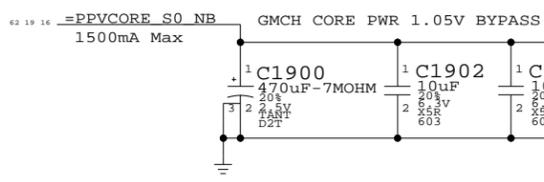
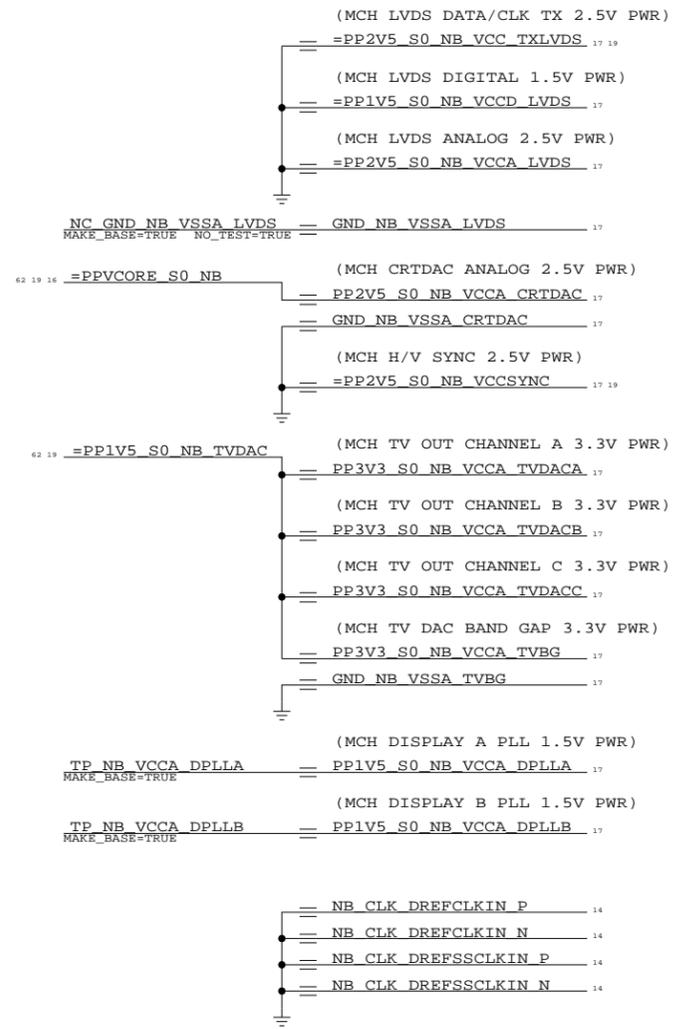
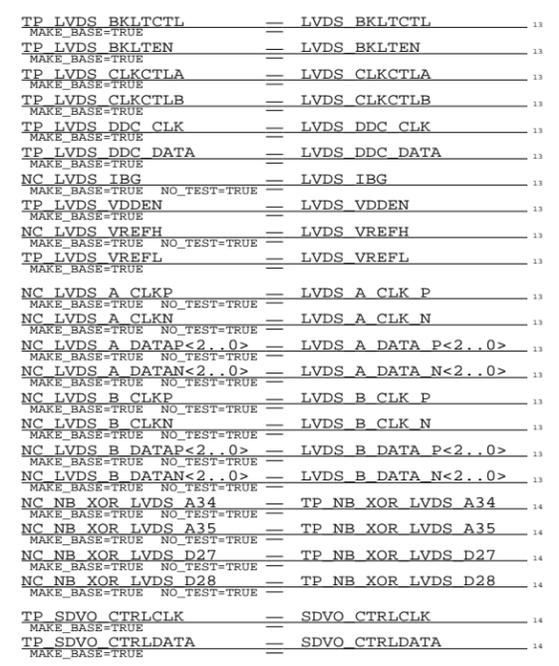
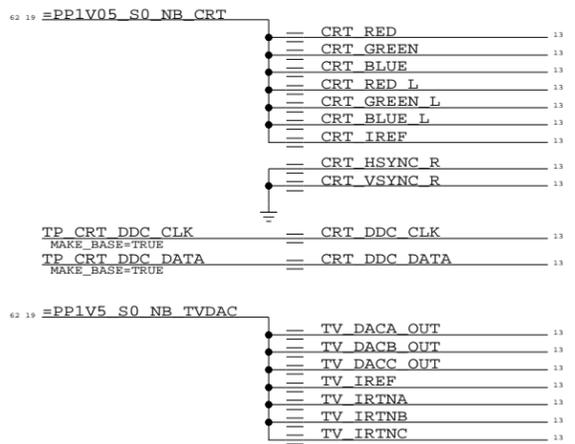
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SCALE	SHT	OF	
NONE	18		81

Power Interface

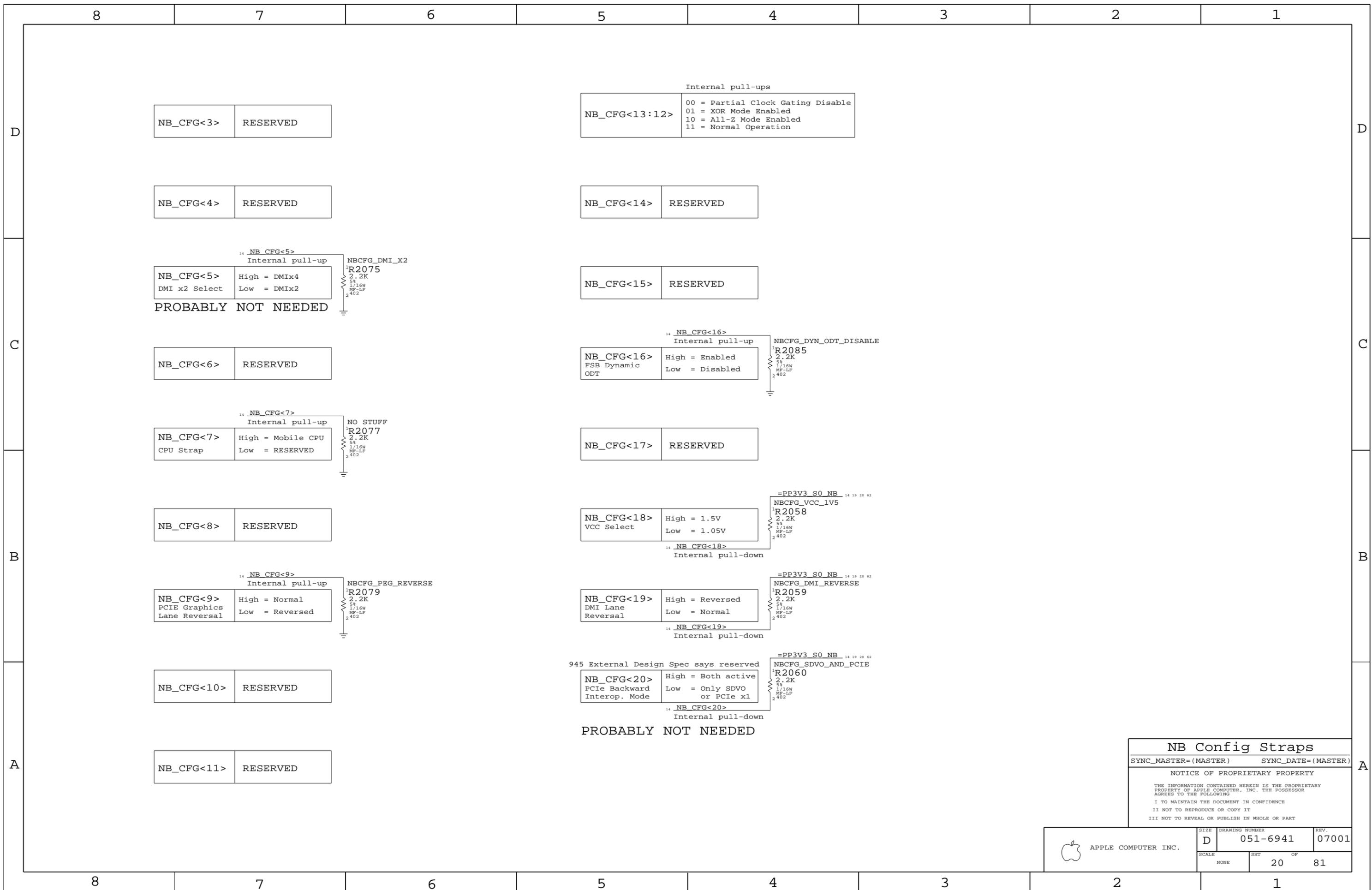
These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	1500mA Max
	=PP1V05_S0_FSB_NB	10mA Max?
	=PP1V05_S0_NB_VTT	800mA Max
	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	=PP1V5_S0_NB	?mA Max
	=PP1V5_S0_NB_3G	>1500mA Max
	=PP1V5_S0_NB_3GPLL	
	=PP1V5_S0_NB_PCIE	?mA Max
	=PP1V5_S0_NB_PLL	100mA Max
	=PP1V5_S0_NB_TVDAC	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	3200mA Max
132mA Max	=PP2V5_S0_NB_VCCSYN	70mA Max
	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
40mA Max?	=PP3V3_S0_NB	?mA Max
	=PP3V3_S0_NB_VCC_HV	40mA Max

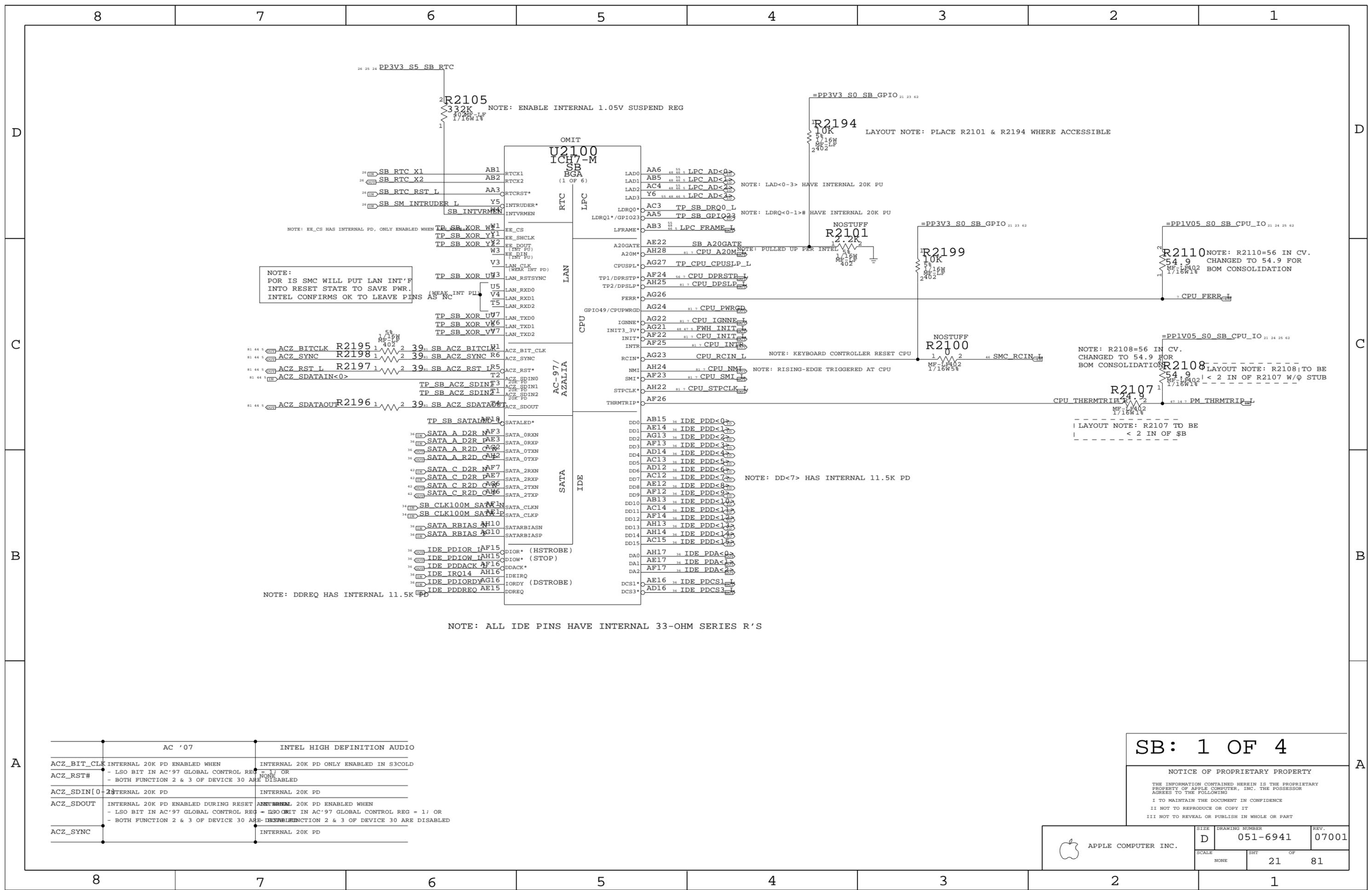


NB (GM) Decoupling
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NB Config Straps
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NONE	20		81



NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

NOTE: LAD<0-3> HAVE INTERNAL 20K PU

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: PULLED UP PER INTEL

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: RISING-EDGE TRIGGERED AT CPU

NOTE: DD<7> HAS INTERNAL 11.5K PD

LAYOUT NOTE: PLACE R2101 & R2194 WHERE ACCESSIBLE

NOTE: R2110=56 IN CV.
CHANGED TO 54.9 FOR
BOM CONSOLIDATION

NOTE: R2108=56 IN CV.
CHANGED TO 54.9 FOR
BOM CONSOLIDATION

LAYOUT NOTE: R2108 TO BE
CHANGED TO 54.9 FOR
BOM CONSOLIDATION

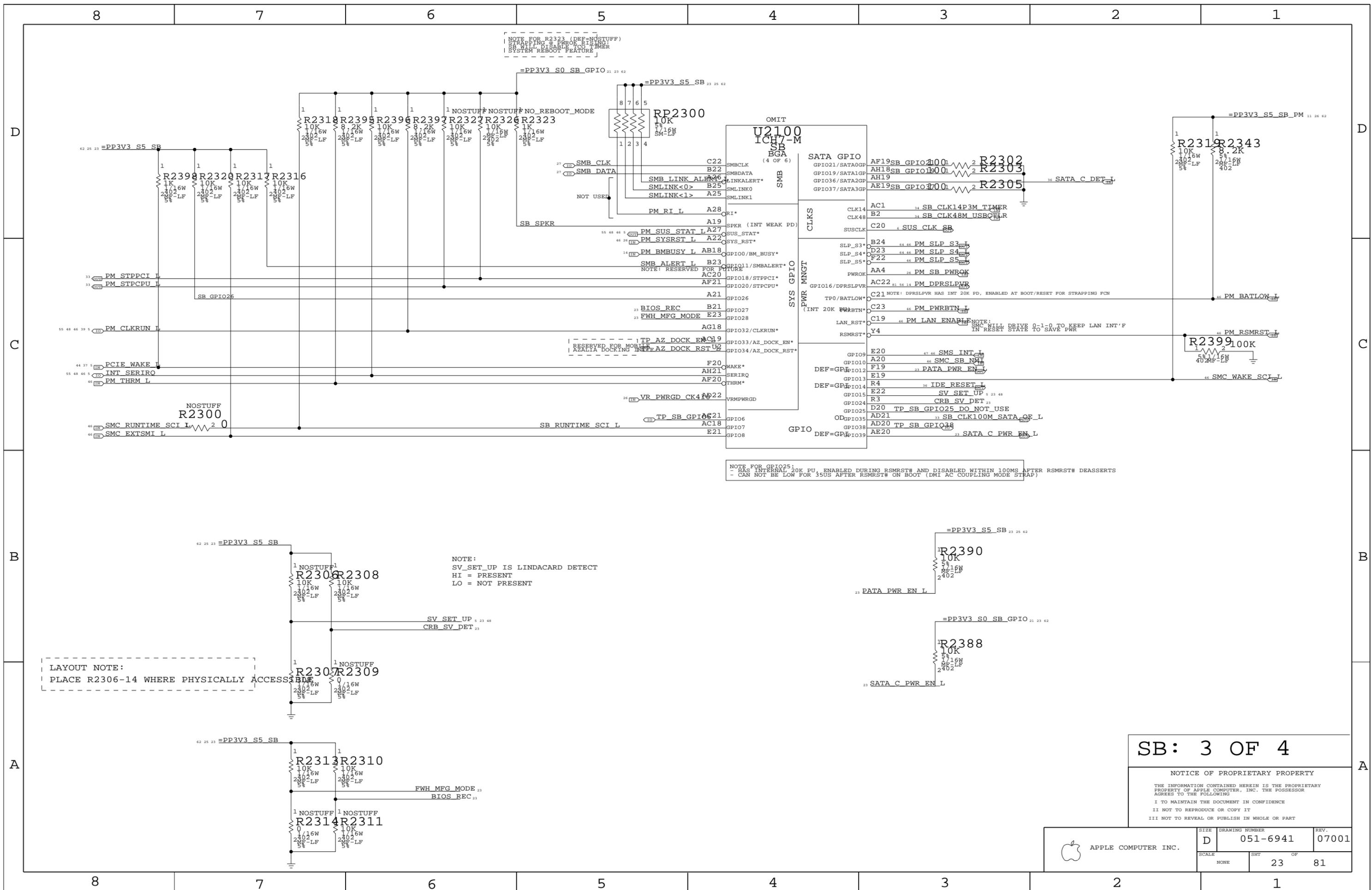
LAYOUT NOTE: R2107 TO BE
CHANGED TO 54.9 FOR
BOM CONSOLIDATION

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

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	D	051-6941	07001
SCALE	NONE	SHT	OF
		21	81



NOTE FOR R2323 (DEF=NOSTUFF)
 STRAPPING @ PWRK RISING:
 SE WILL DISABLE TCO TIMER
 SYSTEM REBOOT FEATURE]

NOTE FOR GPIO25:
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

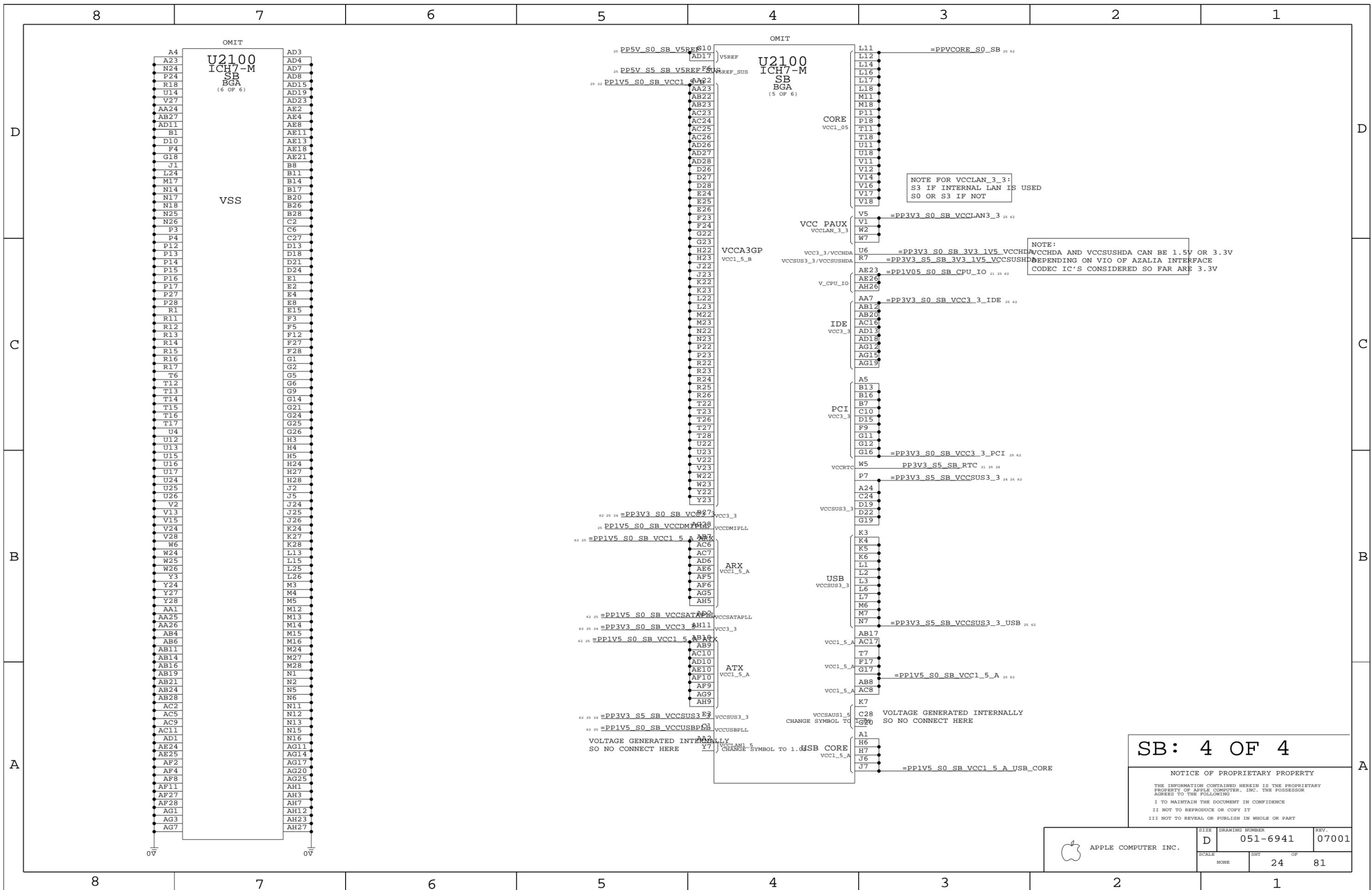
NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

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	D	051-6941	07001
SCALE	SHT OF		
NONE	23		81



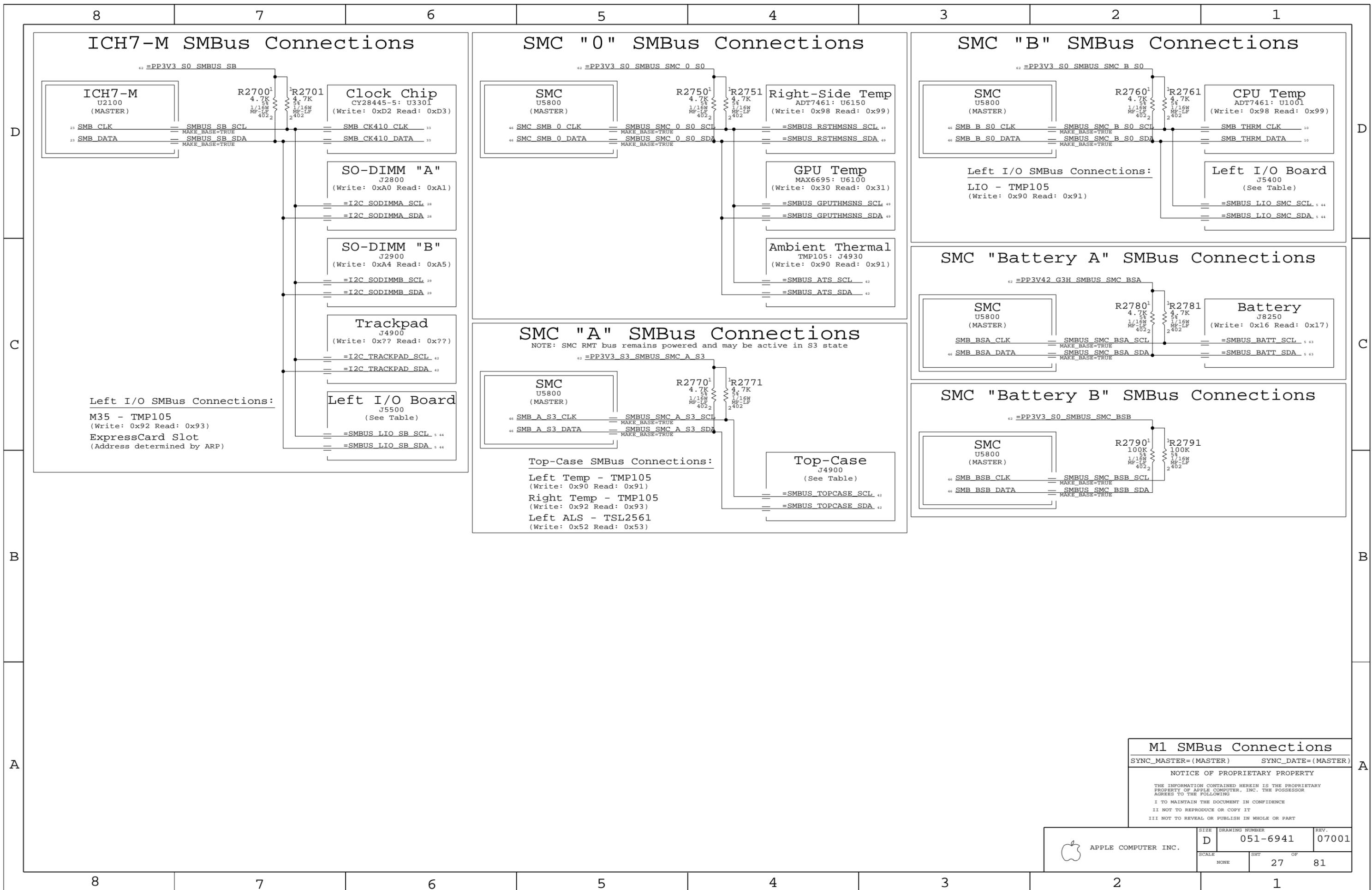
NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

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	D	051-6941	07001
SCALE	SHT OF		
NONE	24		81



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT	OF	
NONE	27	81	

Page Notes

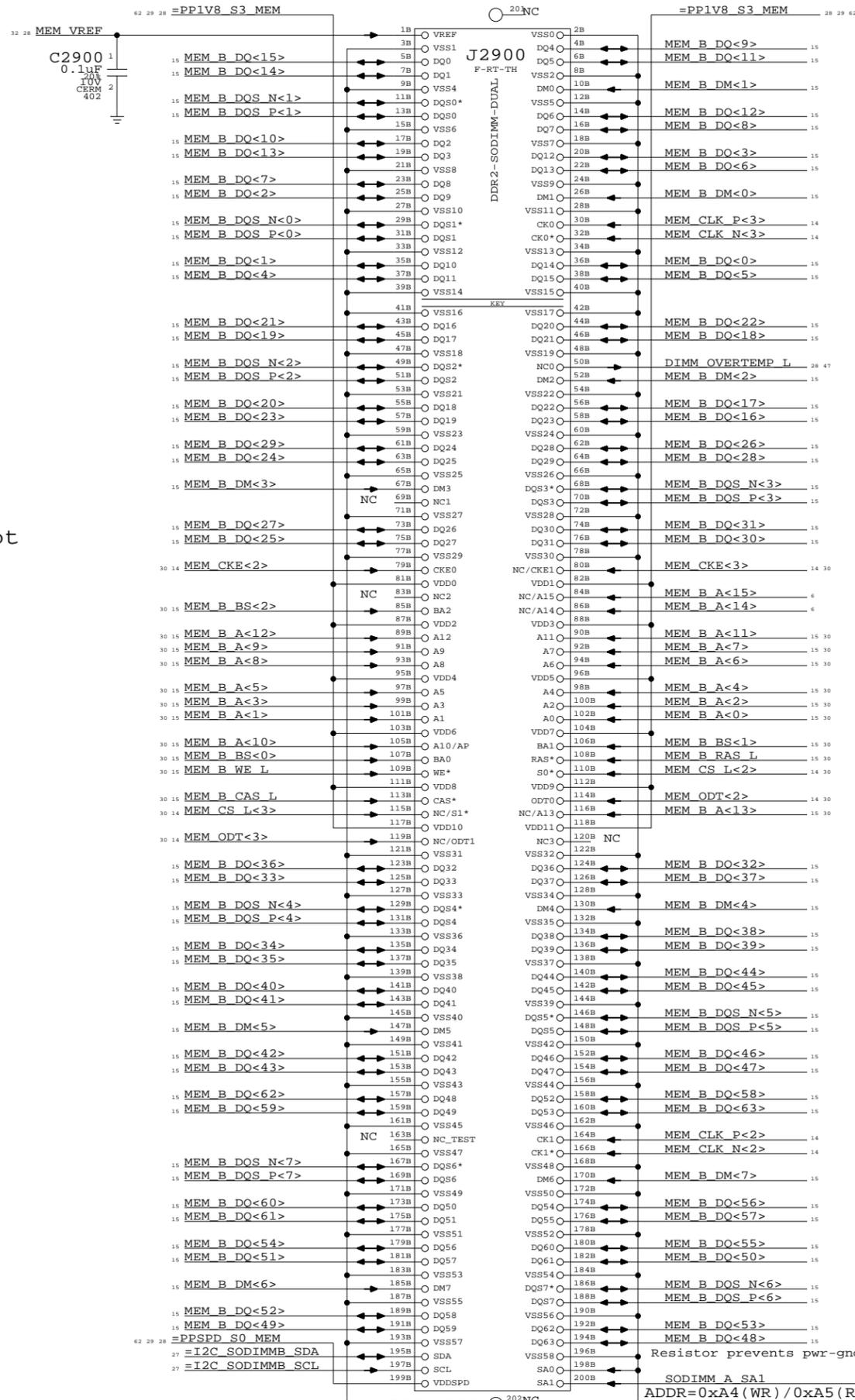
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

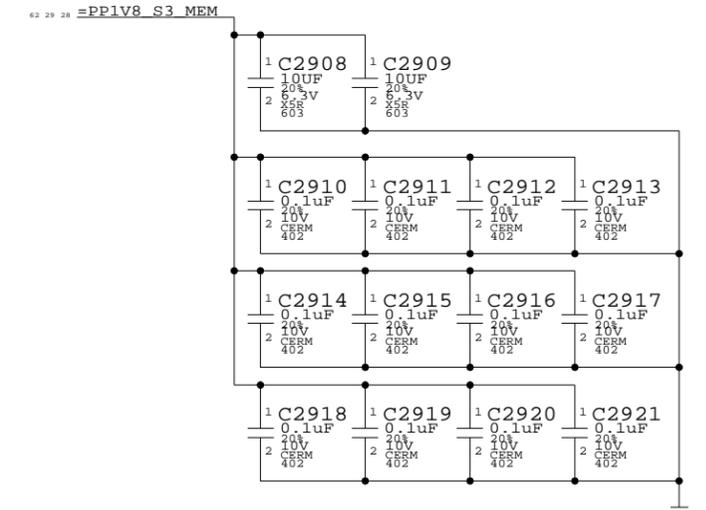
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.

"Lower" (thru-hole) slot



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 07001
	SCALE NONE	SHEET 29	OF 81

8

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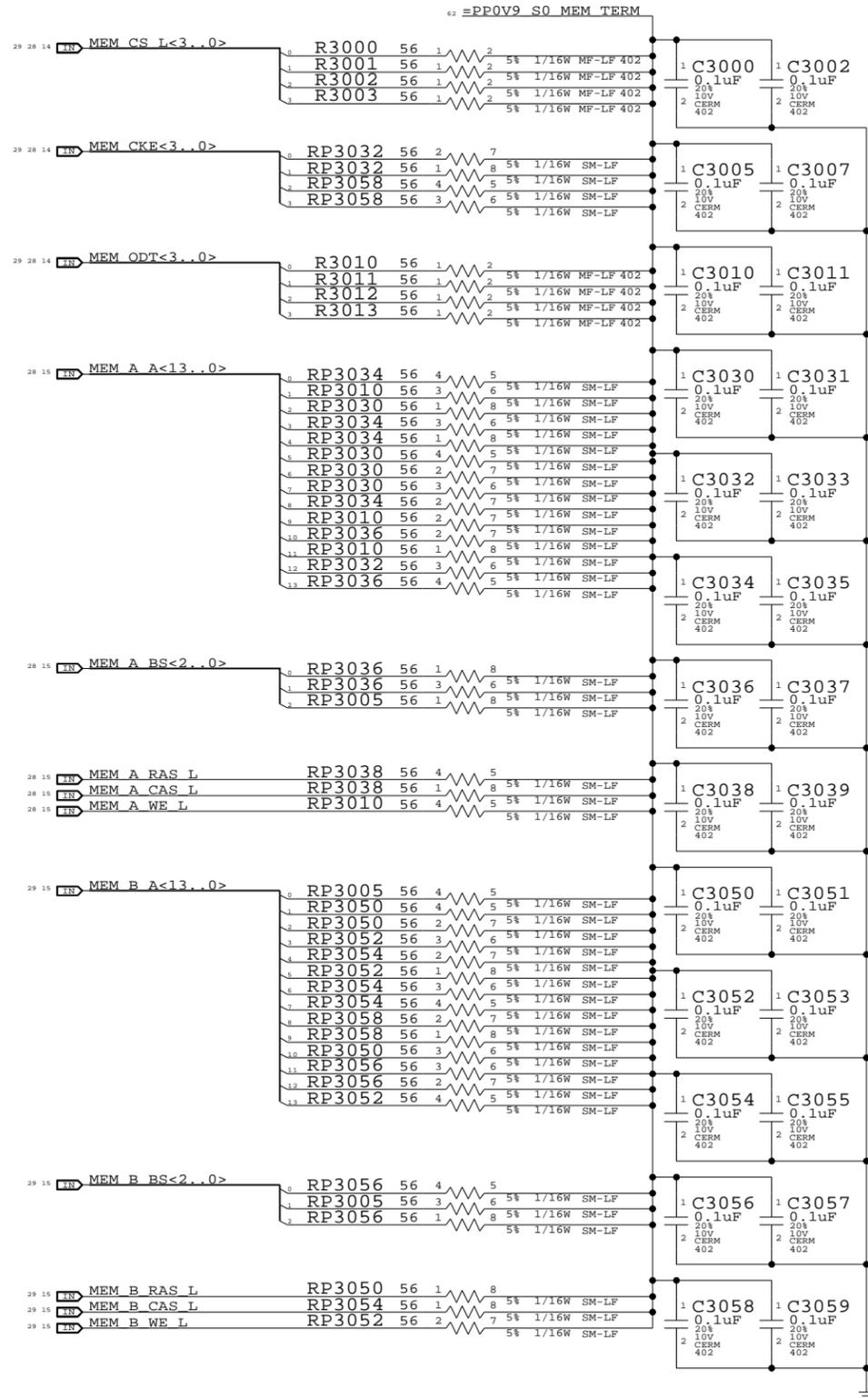
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
 Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE	SHT	OF
NONE	30	81

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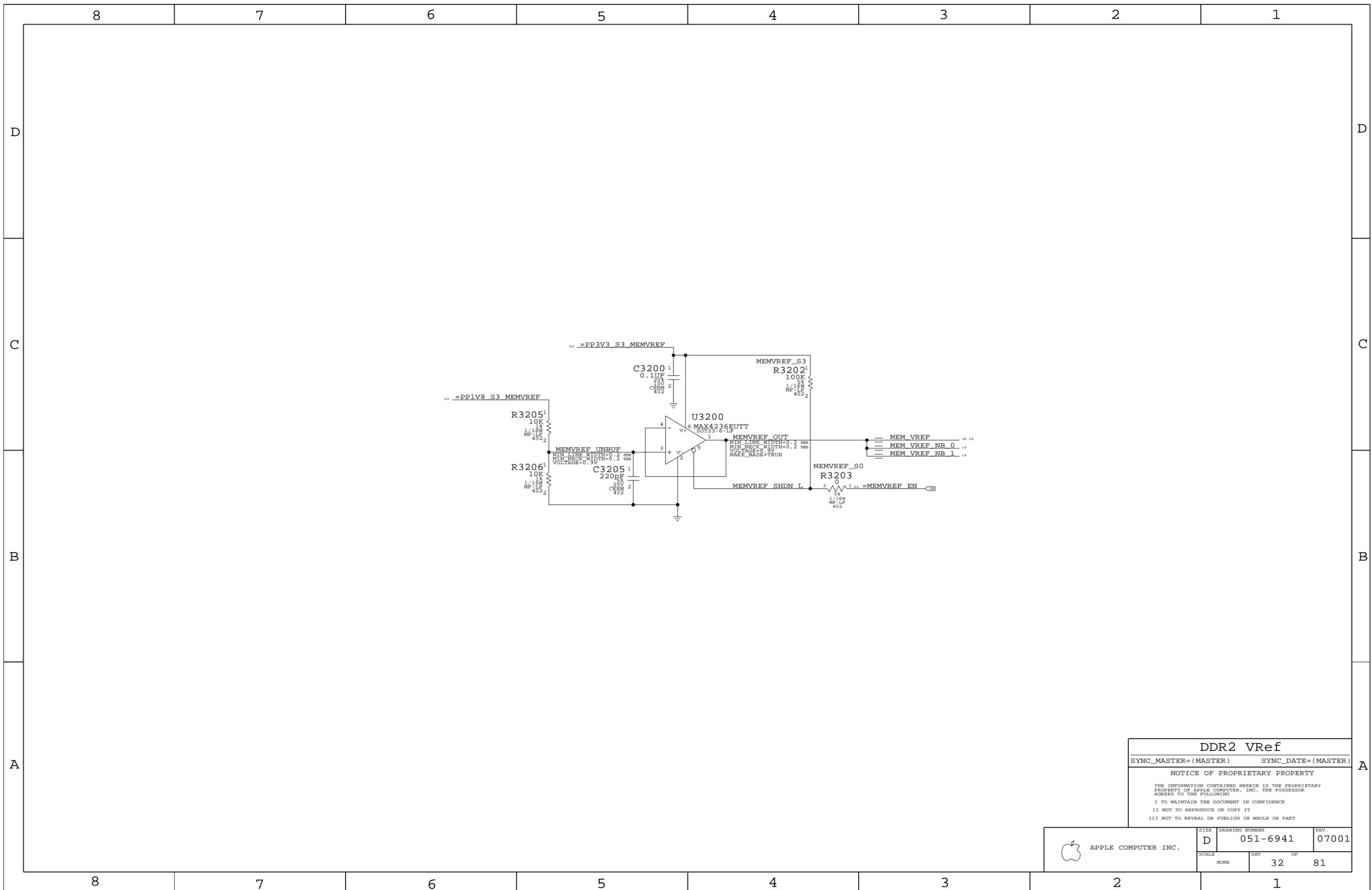
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1



DDR2 Vref

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

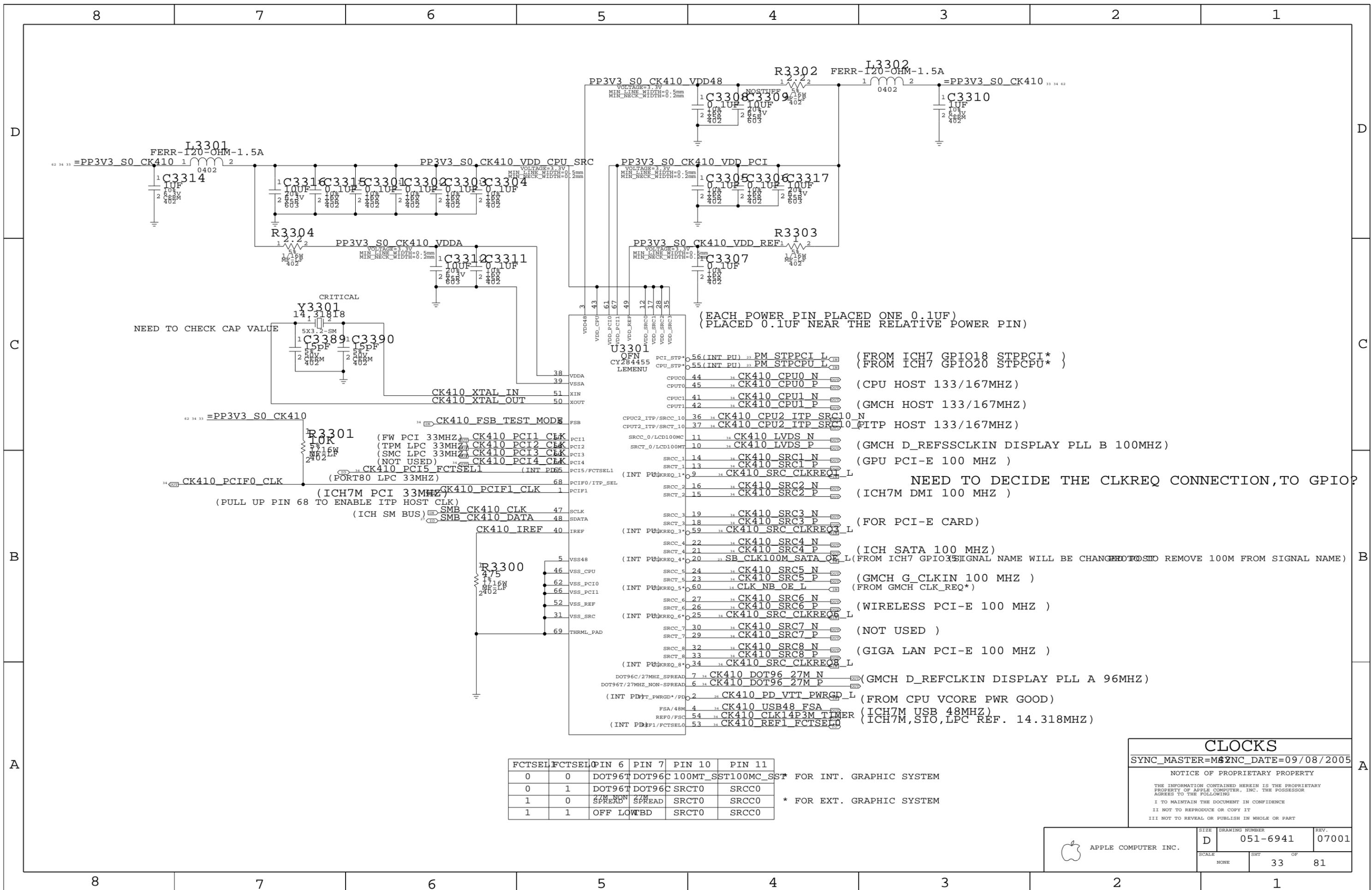
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	SCALE NONE	SHT 32	OF 81



CRITICAL
NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(FROM ICH7 GPIO35 SIGNAL NAME WILL BE CHANGED TO SIO REMOVE 100M FROM SIGNAL NAME)

(ICH SATA 100 MHZ)

(GMCH G_CLKIN 100 MHZ)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M, SIO, LPC REF. 14.318MHZ)

FCTSEL	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST100MC_SST*	FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0
1	1	OFF	LOW	SRCT0	SRCC0

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

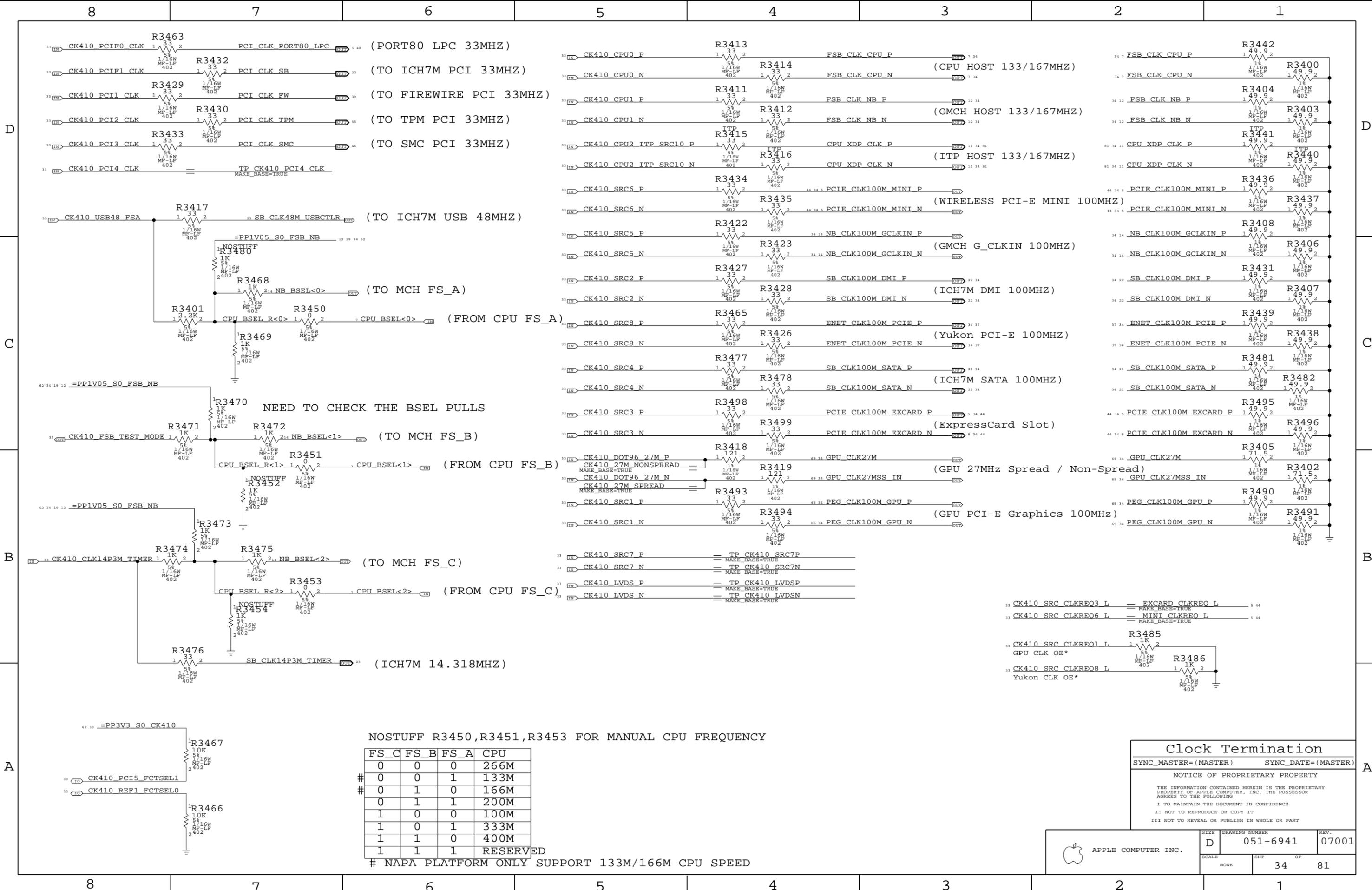
SYNC_MASTER=MSYNC_DATE=09/08/2005

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	33		81



NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
0	0	0	0	266M
0	0	1	1	133M
0	1	0	0	166M
0	1	1	1	200M
1	0	0	0	100M
1	0	1	1	333M
1	1	0	0	400M
1	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE	SHT	OF
NONE	34	81

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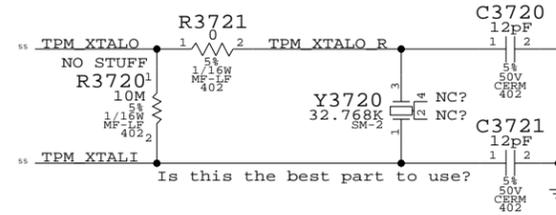
2

1

D

D

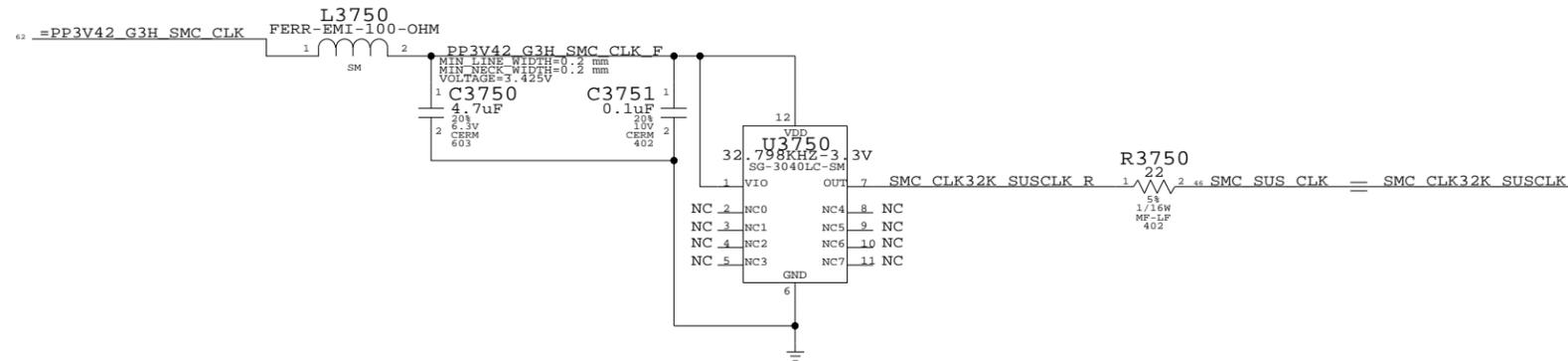
TPM Crystal Circuit



C

C

SMC G3Hot Oscillator



B

B

A

A

Mobile Clocking
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	NONE	SHT OF	81

8

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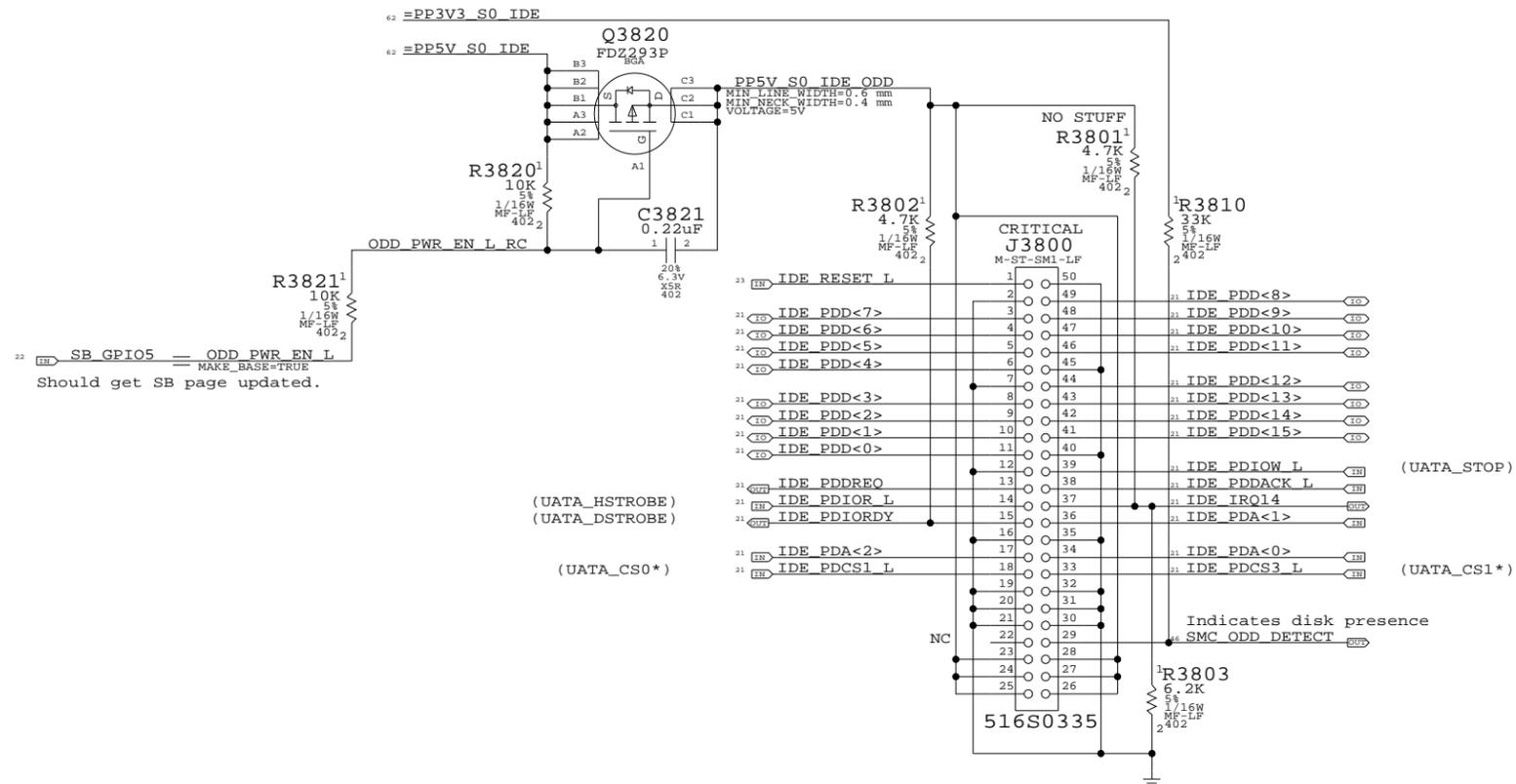
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3

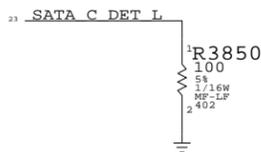
2

1

IDE (ODD) Connector



SB GPIO5 = ODD PWR_EN L
MAKE_BASE=TRUE
Should get SB page updated.



- 21 SATA A R2D C P == TP SATA A R2DP
MAKE_BASE=TRUE
- 21 SATA A R2D C N == TP SATA A R2DN
MAKE_BASE=TRUE
- 21 SATA A D2R P == TP SATA A D2RP
MAKE_BASE=TRUE
- 21 SATA A D2R N == TP SATA A D2RN
MAKE_BASE=TRUE

- 21 SATA RBIAS P == SATA RBIAS
MAKE_BASE=TRUE
- 21 SATA RBIAS N == SATA RBIAS
MAKE_BASE=TRUE

Placement note
Place within 12.7mm
from ball of SB

PATA Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-6941	07001
SCALE	SHT OF		
NONE	36		81

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
BY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
ETHERNET	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
PHY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
	ENETCONN	ENET_100D

Page Notes

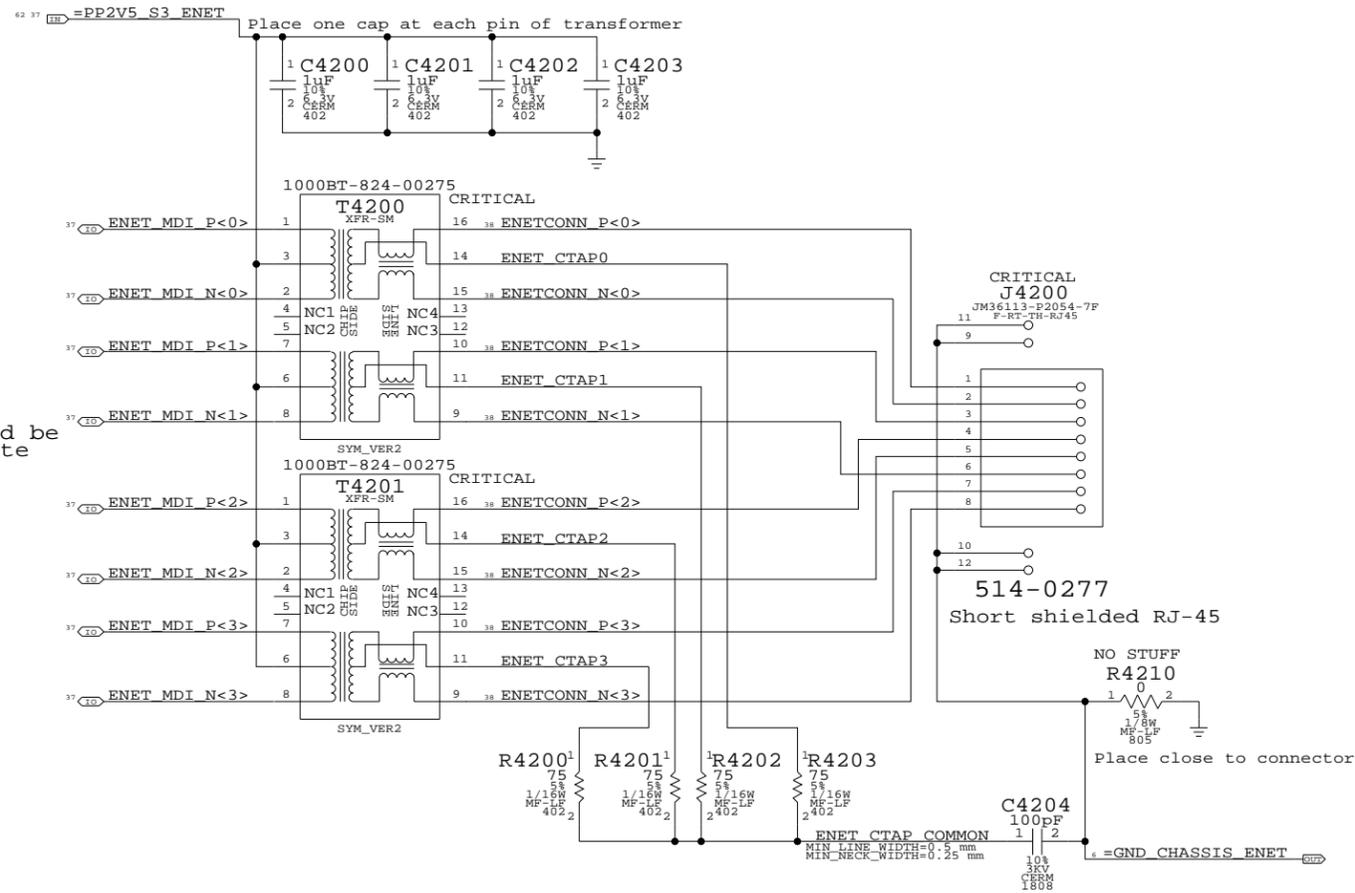
Power aliases required by this page:

- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-6941	07001
SCALE	SHT	OF	
NONE	38	81	

PAGE NOTES

INPUT
 =PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
 =PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
 PCI_GNT3_L - PCI GRANT FROM SB
 PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
 PCI_RST_L - PCI RESET FROM SB
 FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

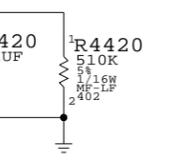
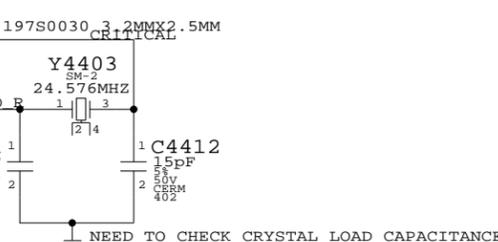
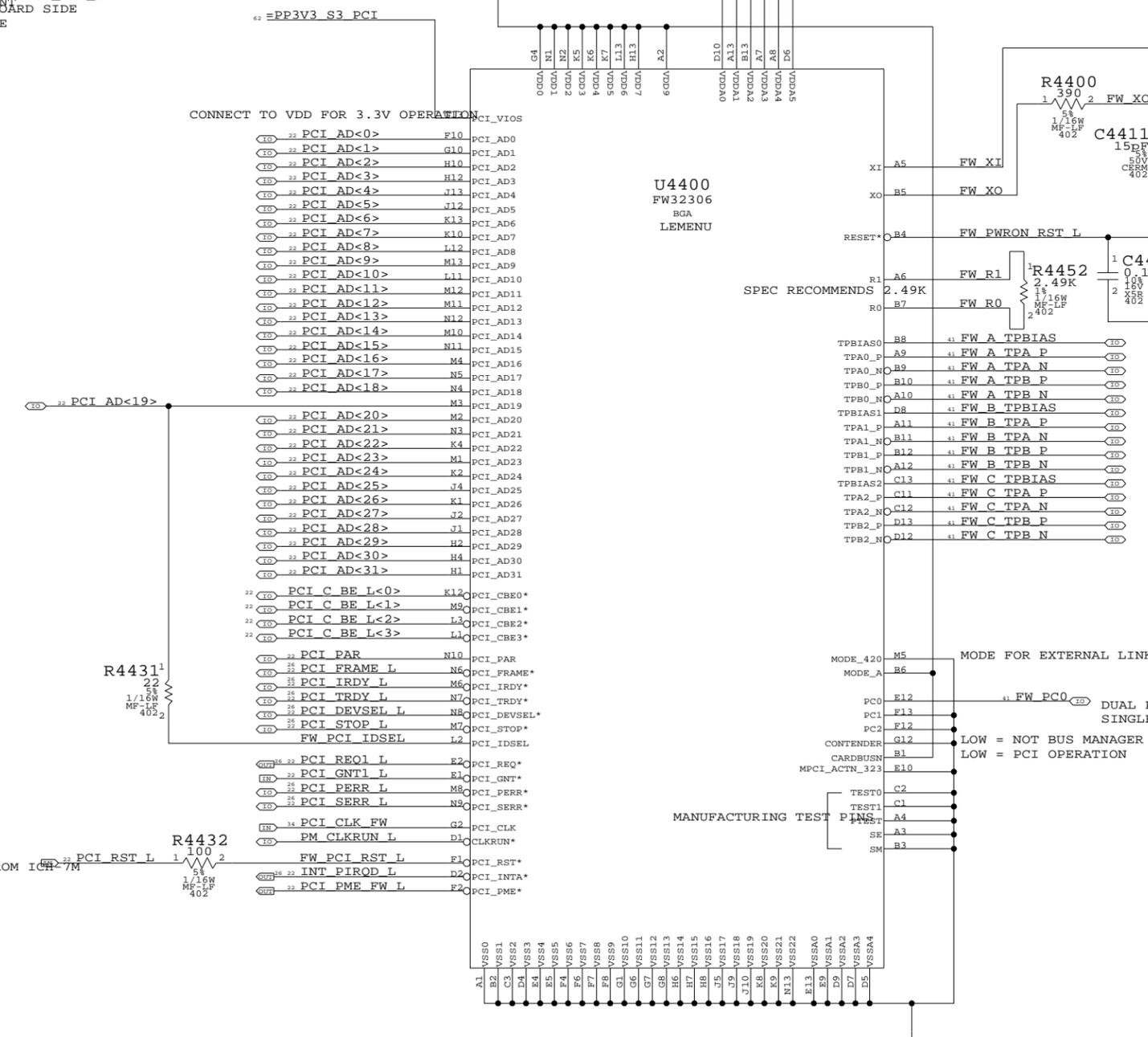
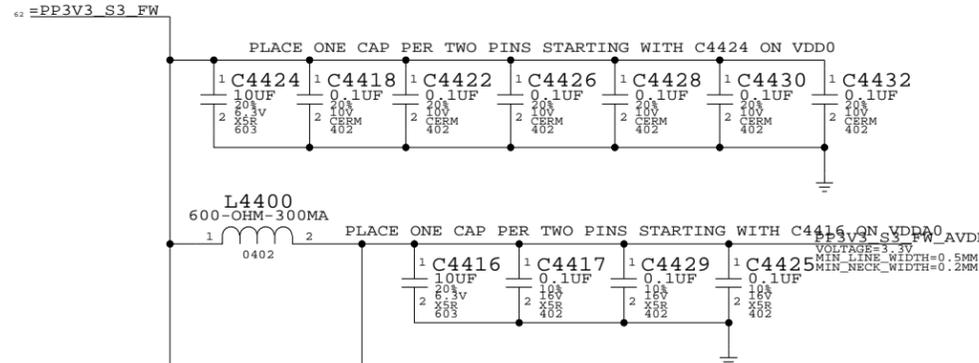
INPUT/OUTPUT
 PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
 PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
 FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
 FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
 FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
 PCI_REQ3_L - PCI REQUEST TO SB
 PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
 INT_PIROD_L - INTERRUPT TO SB
 PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/18/2005 - FIRST REVISION OF PAGE
 6/22/2005 - BGA VERSION OF FW32306 ADDED
 6/22/2005 - CHANGED PIN 1 TO INT_PIROD (PER ARCHITECTURAL DEFINITION)
 6/22/2005 - CHANGED PIN 11 TO PCI_PERR (PER ARCHITECTURAL DEFINITION)
 6/22/2005 - ADDED INT_PIROD TO REQ3/REQ4 (PER ARCHITECTURAL DEFINITION)
 6/22/2005 - ADDED CLK_RUN_DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
 6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
 6/22/2005 - CHANGED C4421 - REDUNDANT
 6/22/2005 - REMOVED C4421 - REDUNDANT
 7/26/2005 - BEING OUT PCI CONNECTION TO BE CONNECTED ON PORT PAGE
 CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
 0.001A DURING SLEEP



FIREWIRE CONTROLLER
 SYNC_MASTER=MSYNC_DATE=08/29/2005

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SCALE	SHT	OF	
NONE	39	81	

Page Notes

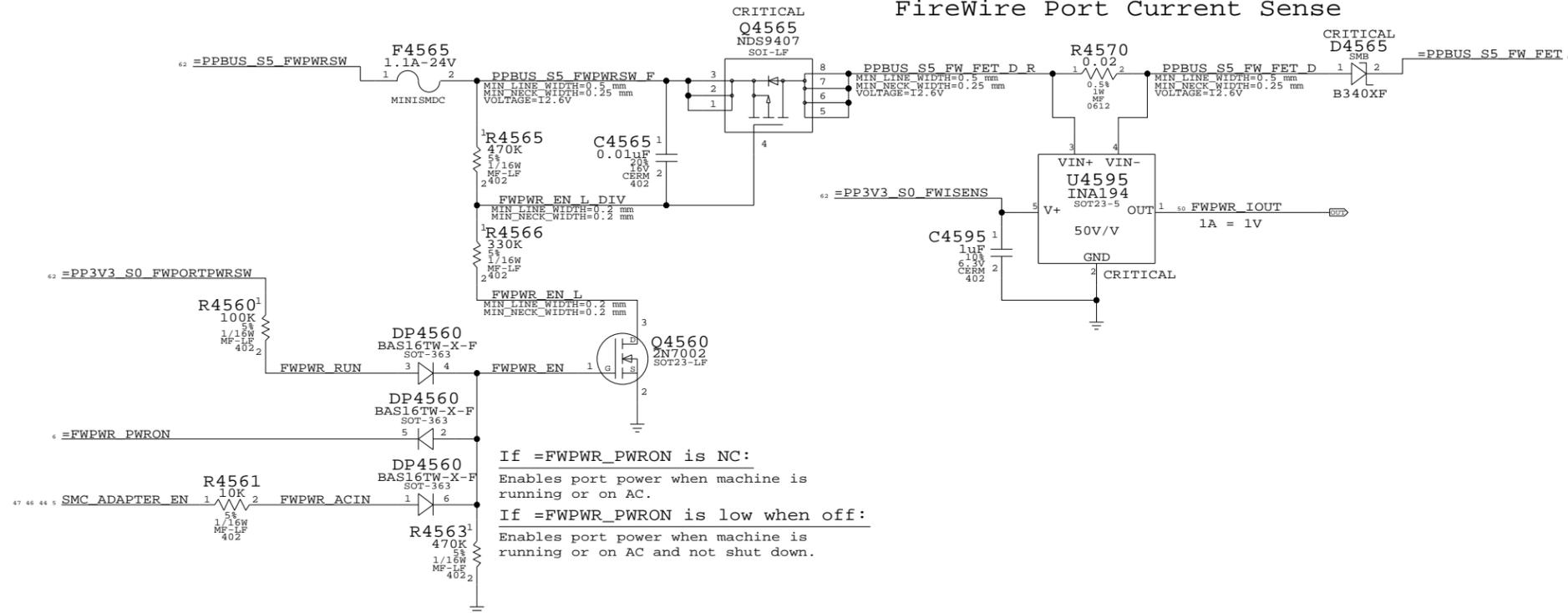
Power aliases required by this page:
 - =PPBUS_S0_FWPWRSW (system supply for bus power)
 - =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
 - =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
 (NONE)

Port Power Switch

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	40	81	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	FW	FW_110D
BY	FW	FW_110D
PHY	FW	FW_110D
PAGE	FW	FW_110D

Page Notes

Power aliases required by this page:
 - =PPFW_PORT1
 - =PP3V3_S5_FWLATEVG
 - =GND_CHASSIS_FW_PORT1

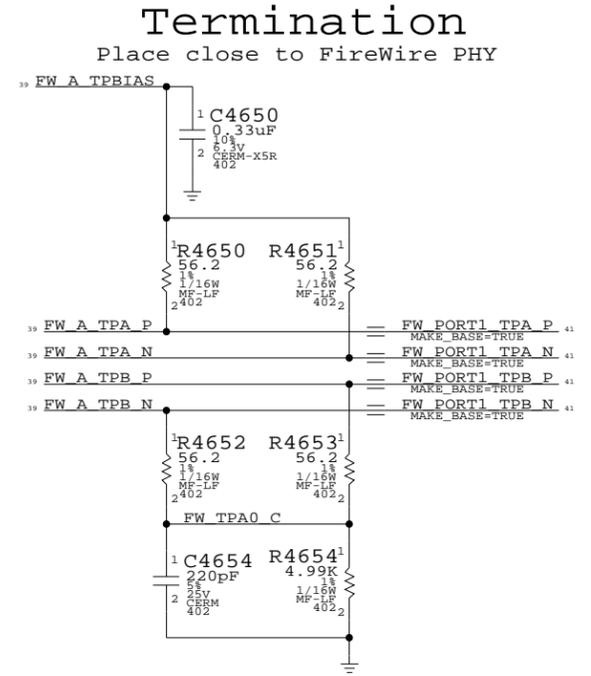
Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

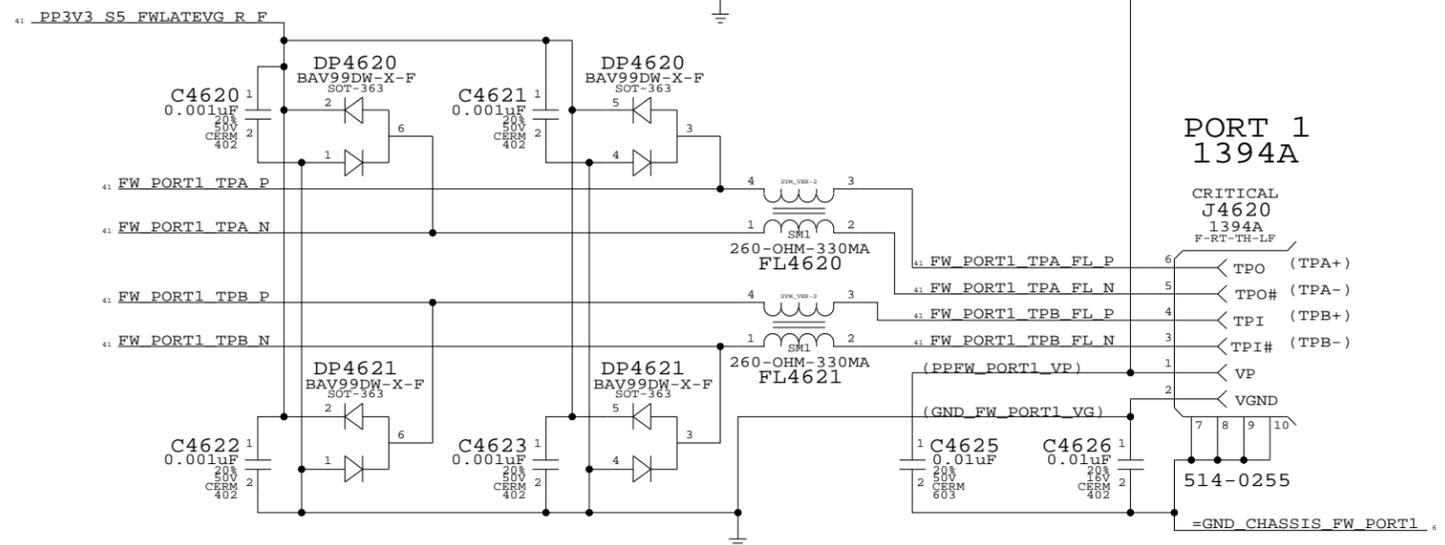
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



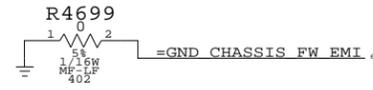
"Snapback" & "Late VG" Protection



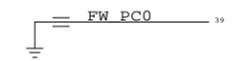
2nd TPA/TPB pair unused

3rd TPA/TPB pair unused

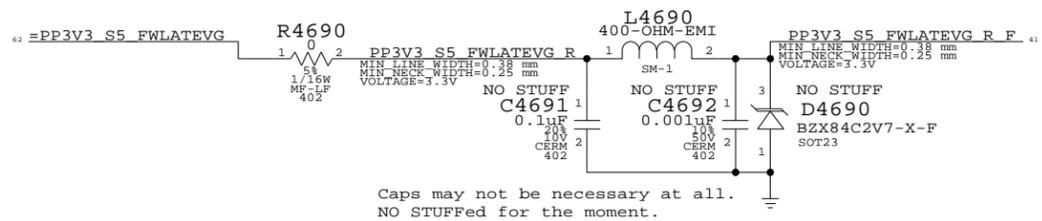
- | | |
|--|--|
| FW B TPBIAS == NC FW B TPBIAS
MAKE_BASE=TRUE
NO_TEST=YES | FW C TPBIAS == NC FW C TPBIAS
MAKE_BASE=TRUE
NO_TEST=YES |
| FW B TPA P == NC FW B TPAP
MAKE_BASE=TRUE
NO_TEST=YES | FW C TPA P == NC FW C TPAP
MAKE_BASE=TRUE
NO_TEST=YES |
| FW B TPA N == NC FW B TPAN
MAKE_BASE=TRUE
NO_TEST=YES | FW C TPA N == NC FW C TPAN
MAKE_BASE=TRUE
NO_TEST=YES |
| FW B TPB P == NC FW B TPBP
MAKE_BASE=TRUE
NO_TEST=YES | FW C TPB P == NC FW C TPBP
MAKE_BASE=TRUE
NO_TEST=YES |
| FW B TPB N == NC FW B TPBN
MAKE_BASE=TRUE
NO_TEST=YES | FW C TPB N == NC FW C TPBN
MAKE_BASE=TRUE
NO_TEST=YES |



FW Power Class Strap
 Single-port system sets PC=0



Late-VG Protection Power



FireWire Ports
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	41	81	

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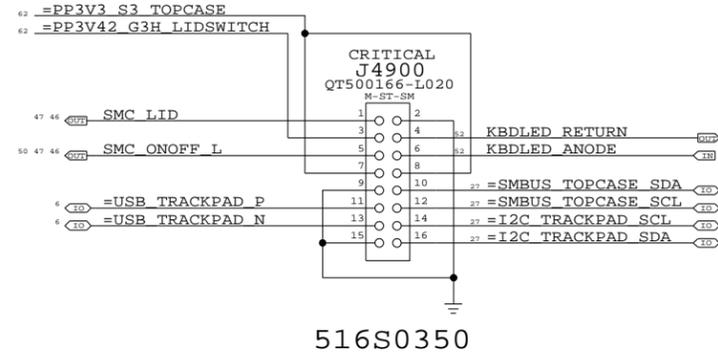
2

1

D

D

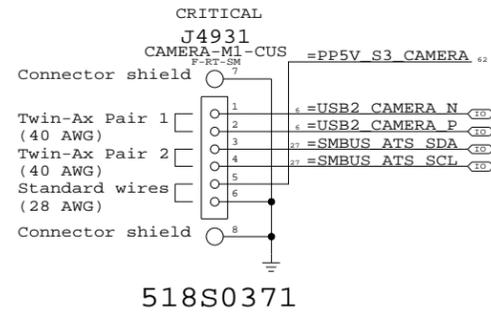
Top-Case Connector



C

C

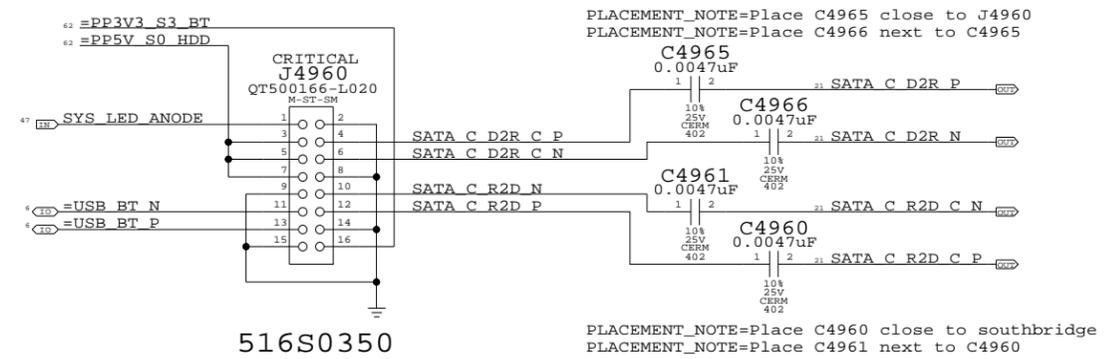
Camera Connector



B

B

Bluetooth (M13P) & SATA HDD Flex Connector



A

A

Internal USB Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT OF		
NONE	42 OF		81

8

7

6

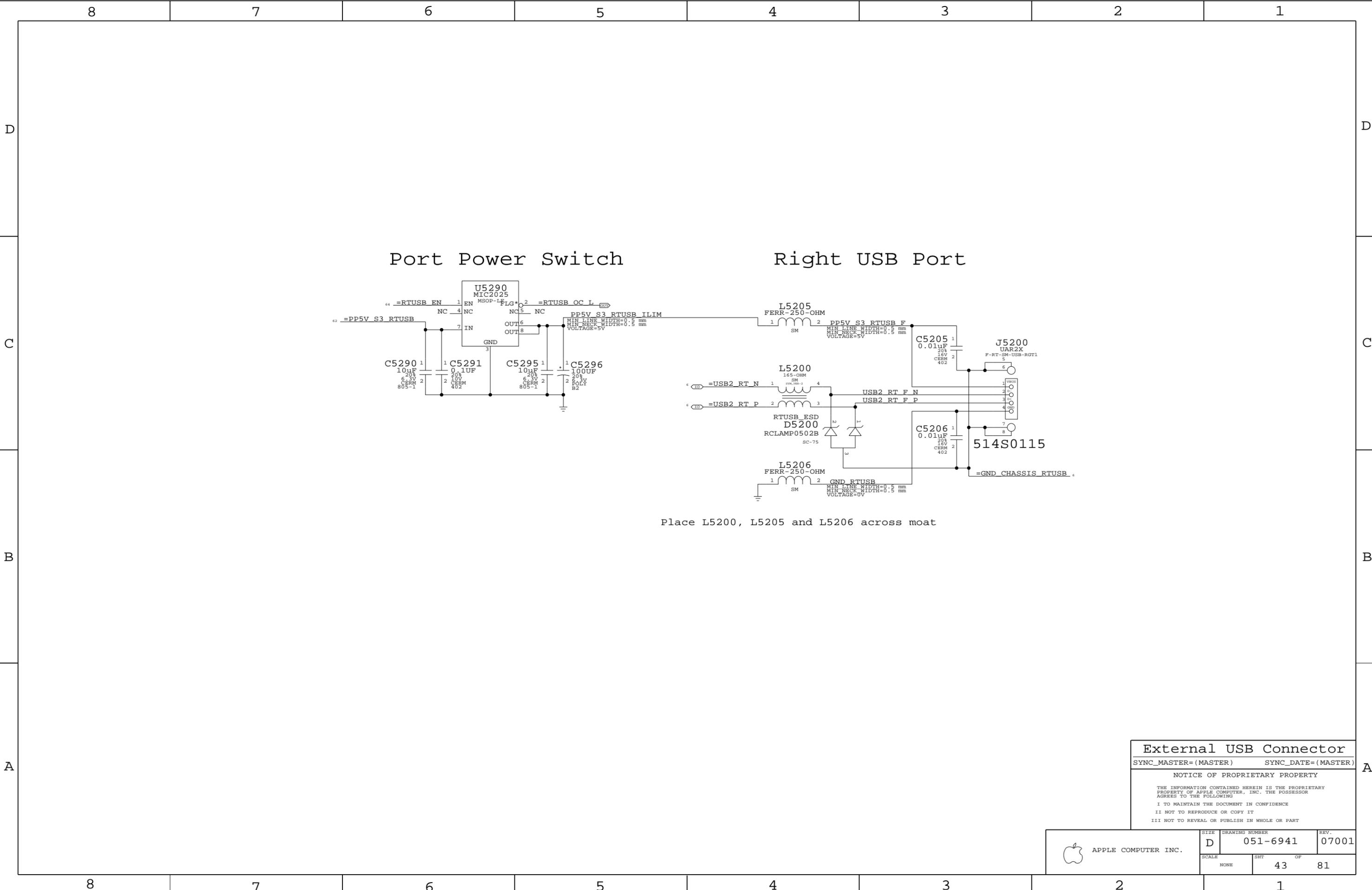
5

4

3

2

1



Port Power Switch

Right USB Port

Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

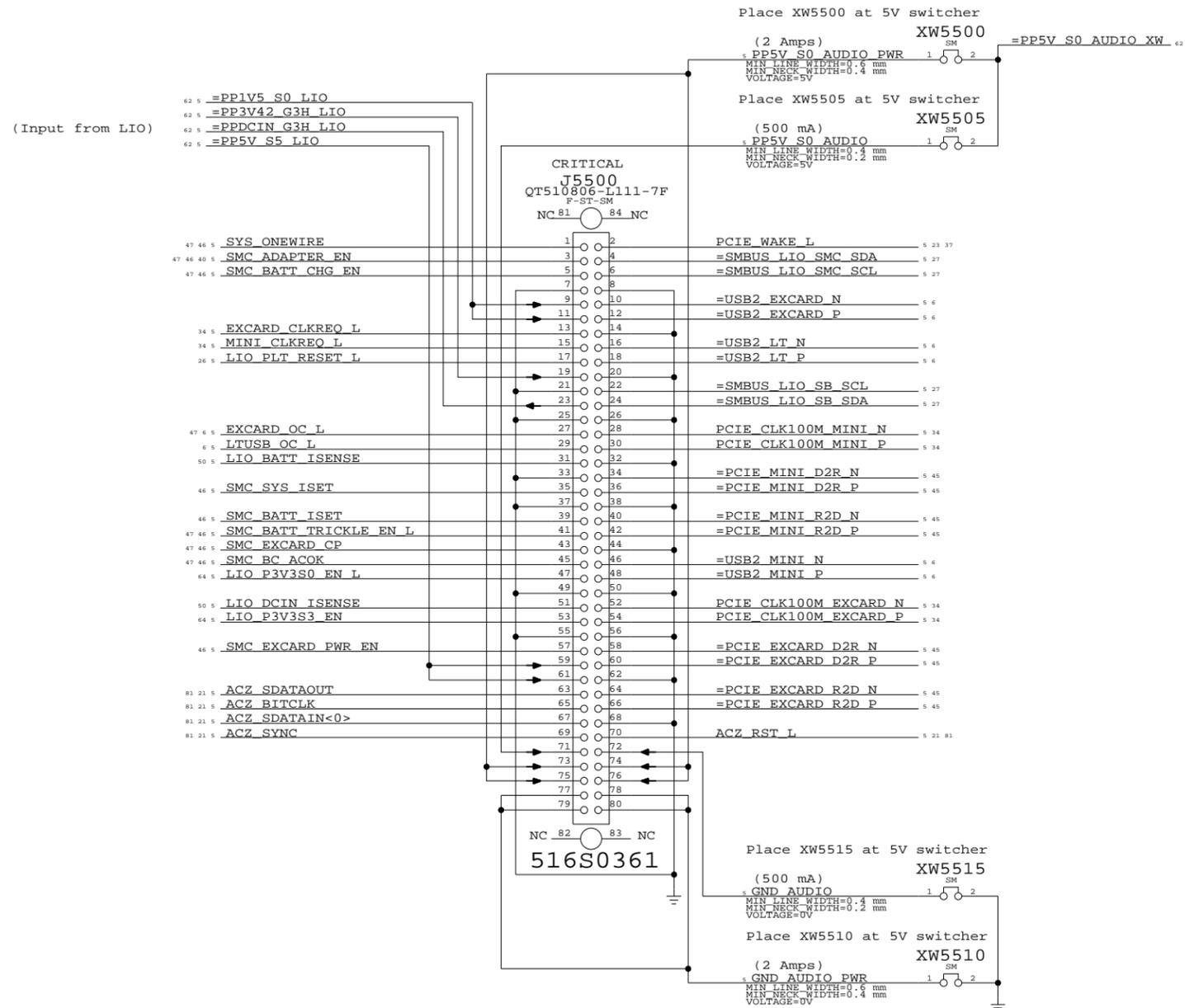
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Left I/O Board Connector



Left I/O Board Connector
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SCALE	SHT OF		
NONE	44 OF		81

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D

D

C

C

B

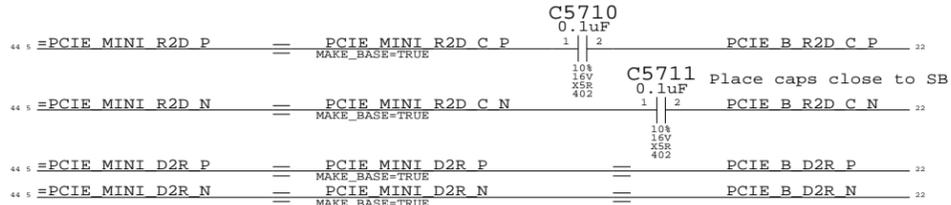
B

A

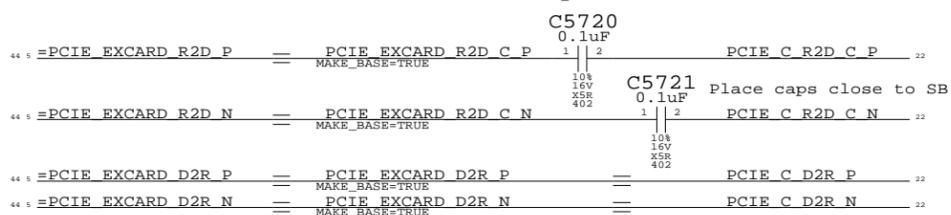
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PCI-E x1 Port "A" = Ethernet (Yukon)

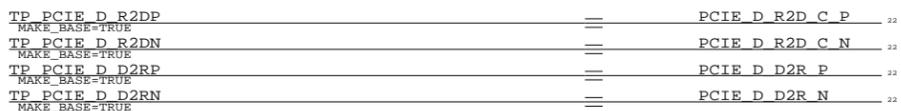
PCI-E x1 Port "B" = PCI-E Mini Card



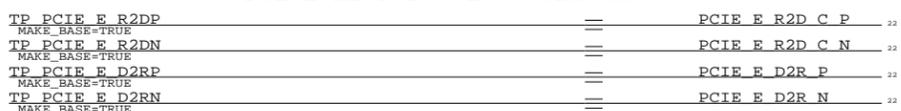
PCI-E x1 Port "C" = ExpressCard



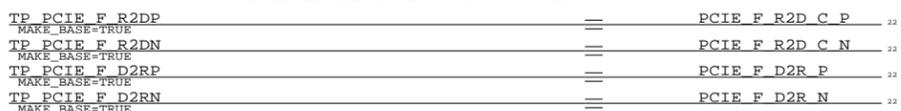
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections

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SCALE	SHT	OF	
NONE	45	81	

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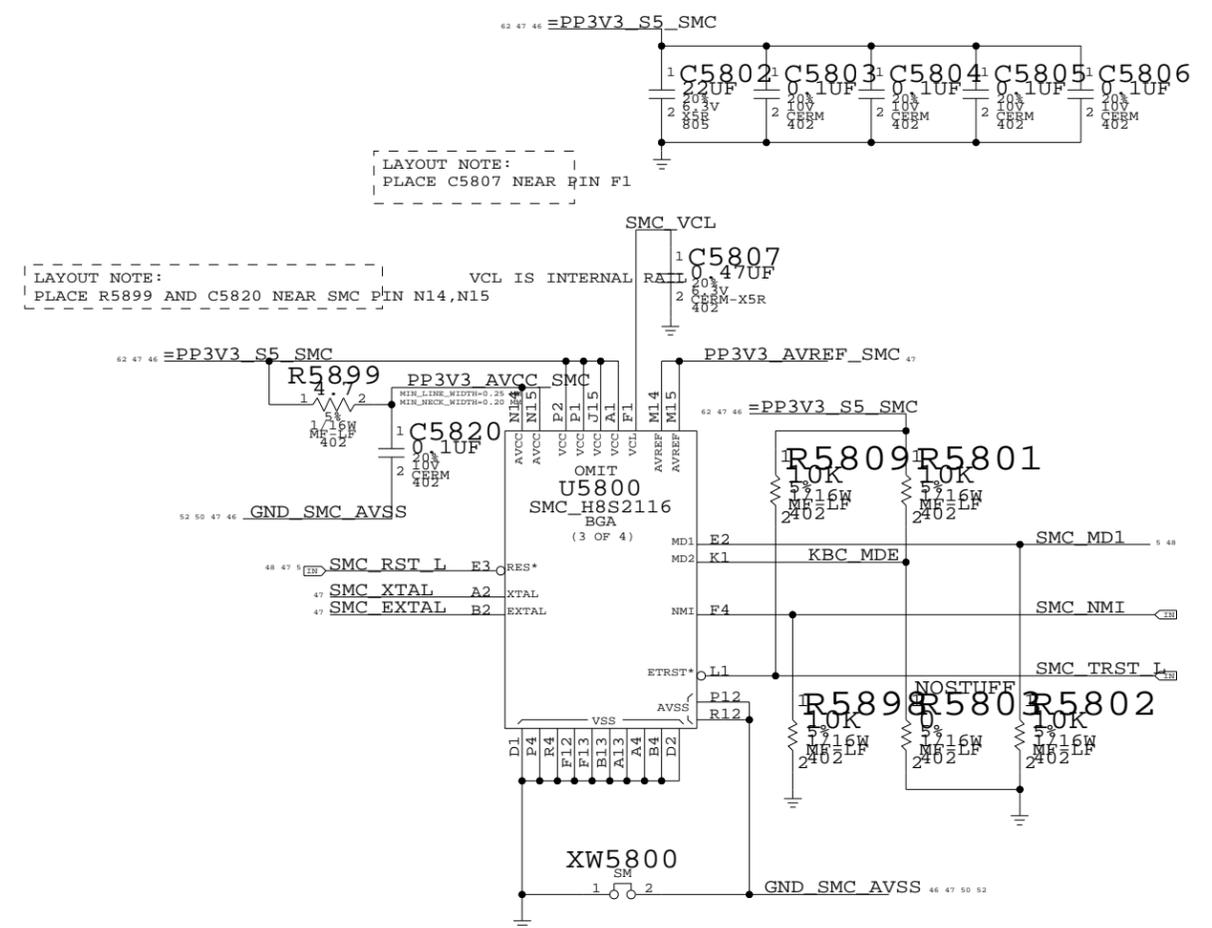
1

UNUSED PINS HAVE THE FORMAT
 THEY ARE WHERE BY SOFTWARE THEY
 CAN BE LEFT NO CONNECTED.

8		7		6		5		4		3		2		1	
UNUSED PINS HAVE THE FORMAT THEY ARE WHERE BY SOFTWARE THEY CAN BE LEFT NO CONNECTED.															
OMIT U5800 SMC_H8S2116 BGA (1 OF 4)															
23	PM LAN ENABLE	B12	P10			P60/KIN0*	L13	64	SMC PM G2 EN	OUT					
26	SMC_RSTGATE L	C13	P11			P61/KIN1*	L14	47 44 45 5	SMC ADAPTER EN	OUT					
64 26	ALL_SYS_PWRGD	A15	P12			P62/KIN2*	L15	76 22	SPI_ARB	IN					
47	RSMRST_PWRGD	B14	P13			P63/KIN3*	K12	51 22	SPI_SCLK	IN					
23	SMC_SB_NMI	B15	P14			P64/KIN4*	K13	76 51 22	SPI_SI	IN					
23	PM_RSMRST L	C14	P15			P65/KIN5*	K14	76 51 22	SPI_SO	IN					
76 56	IMVP_VR_ON	D12	P16			P66/IRQ6*/KIN6*	J12	47	SMC PROCHOT 3 3	L					
23	PM_PWRBTN L	C15	P17			P67/IRQ7*/KIN7*	J13	47	SMC CPU INIT 3	L					
47	SMC_P20	D13	P20			P70/AN0	N12	50	SMC CPU ISENSE	IN					
47	SMC_P21	D14	P21			P71/AN1	R13	50	SMC CPU VSENSE	IN					
47	SMC_P22	D15	P22			P72/AN2	P13	50	SMC GPU ISENSE	IN					
47	SMC_P23	E12	P23			P73/AN3	R14	50	SMC GPU VSENSE	IN					
47 44 5	SMC_BATT_TRICKLE_EN	E14	P24			P74/AN4	P14	50	SMC DCIN ISENSE	IN					
47 44 5	SMC_BATT_CHG_EN	E15	P25			P75/AN5	R15	50	SMC PBUS VSENSE	IN					
47	SMC_P26	E13	P26			P76/AN6	N13	50	SMC BATT ISENSE	IN					
47	SMC_P27	F14	P27			P77/AN7	P15	50	SMC FWIRE ISENSE	IN					
55 48 21 5	LPC_AD<0>	D9	P30/LAD0			P80/PME*	C7	23	SMC WAKE SCI L	IN					
55 48 21 5	LPC_AD<1>	C9	P31/LAD1			P81/GA20	A7	47	SMC TPM GPIO	IN					
55 48 21 5	LPC_AD<2>	A9	P32/LAD2			P82/CLKRUN*	B7 55 48 39 21 1		PM_CLKRUN L	OUT					
55 48 21 5	LPC_AD<3>	B9	P33/LAD3			P83/LPCRUN*	D6 55 48 23 1		PM_SUS_STAT L	IN					
55 48 21 5	LPC_FRAME L	D8	P34/LFRAME*			P84/IRQ3*/TXD1	C6	47	SC_TX L	OUT					
26	SMC_LRESET L	C8	P35/LRESET*			P85/IRQ4*/RXD1	A6	47	SC_RX L	OUT					
38	PCI_CLK_SMC	A8	P36/LCLK			P86/IRQ5*/SCL1/SCL1	B6	27	SMB_BSB_CLK	IN					
55 48 23 5	INT_SERIRQ	D7	P37/SERIRQ			P90/IRQ2*	K4	50 47 42	SMC_ONOFF L	IN					
76	SMC_XDP_TMS L	A5	P40/TMIO			P91/IRQ1*	J2	47 44 5	SMC_BC_ACOK	IN					
76	SMC_XDP_TDI L	B5	P41/TMO0			P92/IRQ0*	J1	63 47 5	SMC_BS_ALERT L	IN					
27	SMB_BSB_DATA	D5	P42/SDA1			P93/IRQ12*	J3	64 23	PM_SLP_S3 L	IN					
47	SMC_TPM_PP	C3	P43/TM11/EXSCK1			P94/IRQ13*	J4	64 23	PM_SLP_S4 L	IN					
76	SMC_XDP_TRST L	B1	P44/TMO1			P95/IRQ14*	H2	23	PM_SLP_S5 L	IN					
76	SMC_XDP_TCK	C2	P45			P96/EXCL	H1	35	SMC_SUS_CLK	IN					
47	SMC_SYS_LED	D3	P46/PWX0/PWM0			P97/IRQ15*/SDA0	G2	27	SMC_SMB_0_DATA	IN					
52	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1												
48 47 5	SMC_TX L	G1	P50												
48 47 5	SMC_RX L	G4	P51												
27	SMC_SMB_0_CLK	F2	P52/SCL0												

8		7		6		5		4		3		2		1	
OMIT U5800 SMC_H8S2116 BGA (2 OF 4)															
21	SMC_RCIN L	R3	PA0/KIN8*/PA2CC			PE0	M3	47	SMC_CASE_OPEN	IN					
76 48 22 5	BOOT_LPC_SPI L	P3	PA1/KIN9*/PA2BD			PE1*/ETCK	M2	48 47 5	SMC_TCK	IN					
26 23	PM_SYSRST L	R2	PA2/KIN10*/PS2AC			PE2*/ETDI	M1	48 47 5	SMC_TDI	IN					
55 47	SMC_TPM_RESET L	N3	PA3/KIN11*/PS2AC			PE3*/ETDO	L4	48 47 5	SMC_TDO	OUT					
47 14	PM_EXTTLS L<0>	R1	PA4/KIN12*/PS2BC			PE4*/ETMS	L2	48 47 5	SMC_TMS	IN					
23	PM_THRM L	N2	PA5/KIN13*/PS2BD			PF0/IRQ8*/PWM2	M7		SMC_PF0	47					
47 44 5	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC			PF1/IRQ9*/PWM3	P6		SMC_PF1	47					
23	PM_BATLOW L	N1	PA7/KIN15*/PS2CD			PF2/IRQ10*/TMOY	R6	47 42	SMC_LID	IN					
23	SMC_EXTSMI L	B10	PB0/LSMI*			PF3/IRQ11*/TMOX	N6	47	SMC_CPU_RESET 3	L					
23	SMC_RUNTIME_SCI L	A10	PB1/LSCI			PF4/PWM4	M6	44 5	SMC_BATT_ISET	IN					
36	SMC_ODD_DETECT	D10	PB2			PF5/PWM5	R5	47	SMC_BATT_VSET	IN					
50	ISENSE_CAL_EN	A11	PB3			PF6/PWM6	P5	44 5	SMC_SYS_ISET	IN					
47 44 5	SMC_EXCARD_CP	B11	PB4			PF7/PWM7	N5	47	SMC_SYS_VSET	IN					
44 5	SMC_EXCARD_PWR_EN	C11	PB5			PG0/EXIRQ8*/TMIX	P9	76 51 22	SPI_CE L	IN					
47	SMC_EXCARD_PWR_OC L	A12	PB6			PG1/EXIRQ9*/TMIX	R9	76	SMC_XDP_TCK 3 3	IN					
76	SMC_XDP_TDO 3 3 L	D11	PB7			PG2/EXIRQ10*/SDA2	N9	27	SMB_BSA_DATA	IN					
53	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*			PG3/EXIRQ11*/SCL2	P8	27	SMB_BSA_CLK	IN					
53	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*			PG4/EXIRQ12*/EXSDAA	R8	27	SMB_A_S3_DATA	IN					
47	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*			PG5/EXIRQ13*/EXSCLA	M8	27	SMB_A_S3_CLK	IN					
47	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*			PG6/EXIRQ14*/EXSDAB	P7	27	SMB_B_S0_DATA	IN					
53	SMC_FAN_0 TACH	H14	PC4/TIOCA1/WUE12*			PG7/EXIRQ15*/EXSCLB	R7	27	SMB_B_S0_CLK	IN					
47	SMC_FAN_1 TACH	H15	PC5/TIOCB1/TCLKC/WUE13*			PH0/EXIRQ6*	E1	47	SMC_PROCHOT	OUT					
47	SMC_FAN_2 TACH	H13	PC6/TIOCA2/WUE14*			PH1/EXIRQ7*	F3	47	SMC_THRMTRIP	OUT					
47	SMC_FAN_3 TACH	H12	PC7/TIOCB2/TCLKD/WUE15*			PH2/FWE	K2	47	SMC_FWE	OUT					
54	SMS_X_AXIS	M11	PD0/AN8			PH3/EXEXCL	C4	52	ALS_GAIN	OUT					
54	SMS_Y_AXIS	P11	PD1/AN9												
54	SMS_Z_AXIS	R11	PD2/AN10												
47	SMC_ANALOG_ID	N11	PD3/AN11												
47	SMC_NB_ISENSE	P10	PD4/AN12												
47	SMC_MEM_ISENSE	R10	PD5/AN13												
52	ALS_LEFT	N10	PD6/AN14												
52	ALS_RIGHT	M10	PD7/AN15												

8		7		6		5		4		3		2		1	
OMIT U5800 SMC_H8S2116 BGA (4 OF 4)															
G3	NC0	NC12	E15												
H3	NC1	NC13	A14												
K3	NC2	NC14	C12												
L3	NC3	NC15	C10												
N4	NC4	NC16	C5												
M5	NC5	NC17	A3												
N7	NC6	NC18	B8												
M12	NC7	NC19	E4												
M13	NC8	NC20	H4												
L12	NC9	NC21	M9												
K15	NC10	NC22	N8												
J14	NC11														



SMC

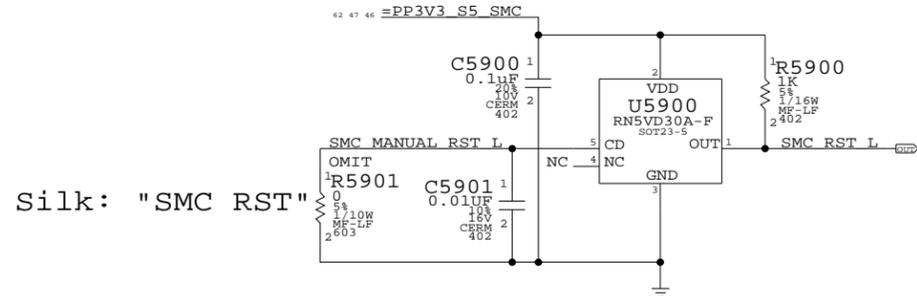
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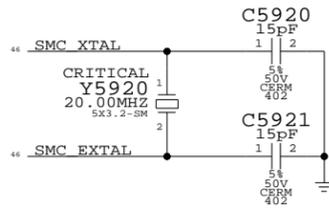
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT	OF	
NONE	46	81	

SMC Reset Button / Brownout Detect



Silk: "SMC RST"

SMC Crystal Circuit

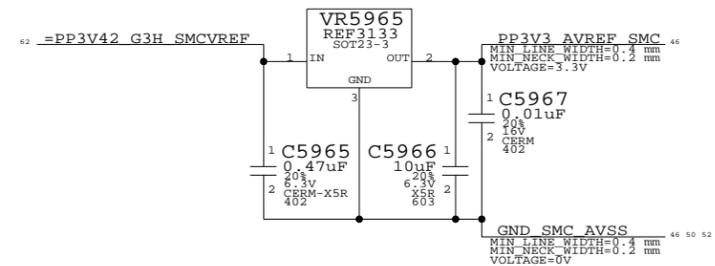


Debug Power Button

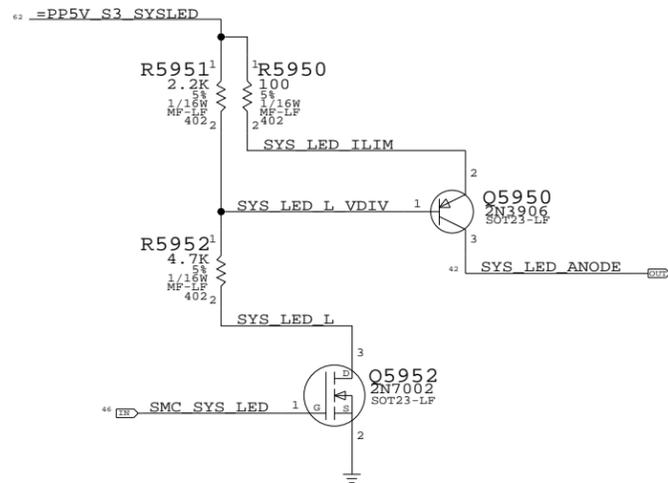


Silk: "PWR BTN"

SMC AVREF Supply

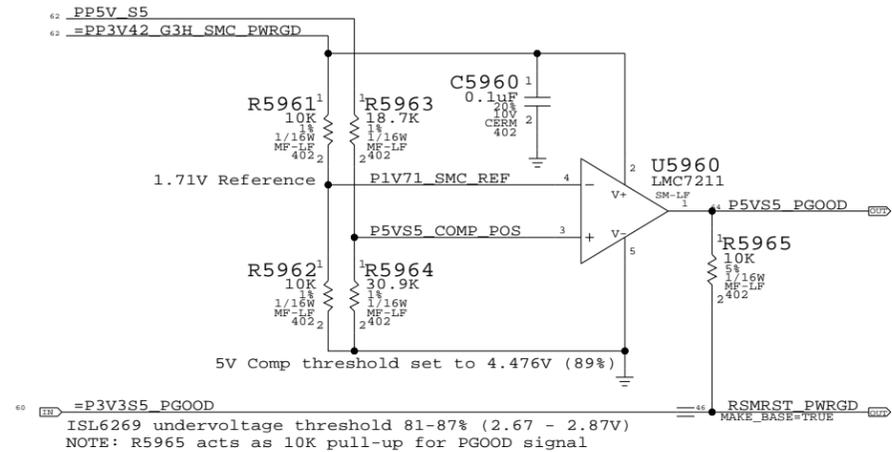


System (Sleep) LED Circuit

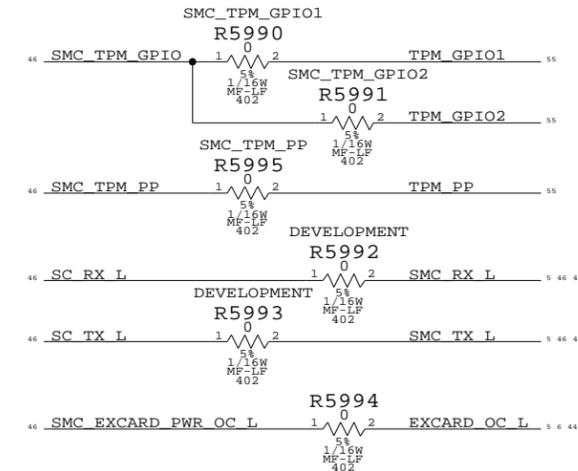
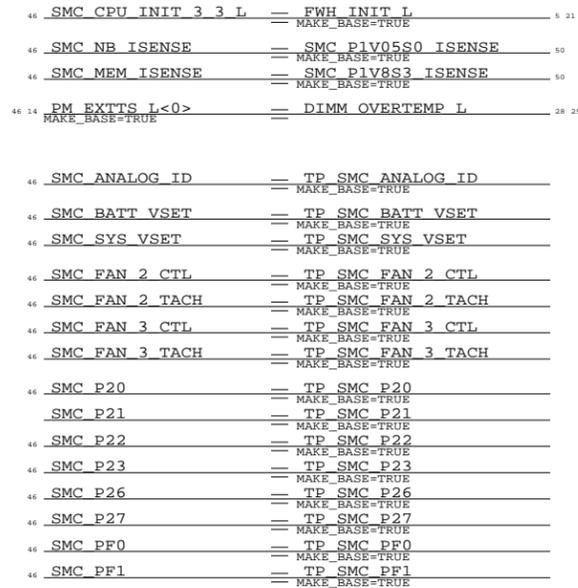


SMC PWRGD Circuit

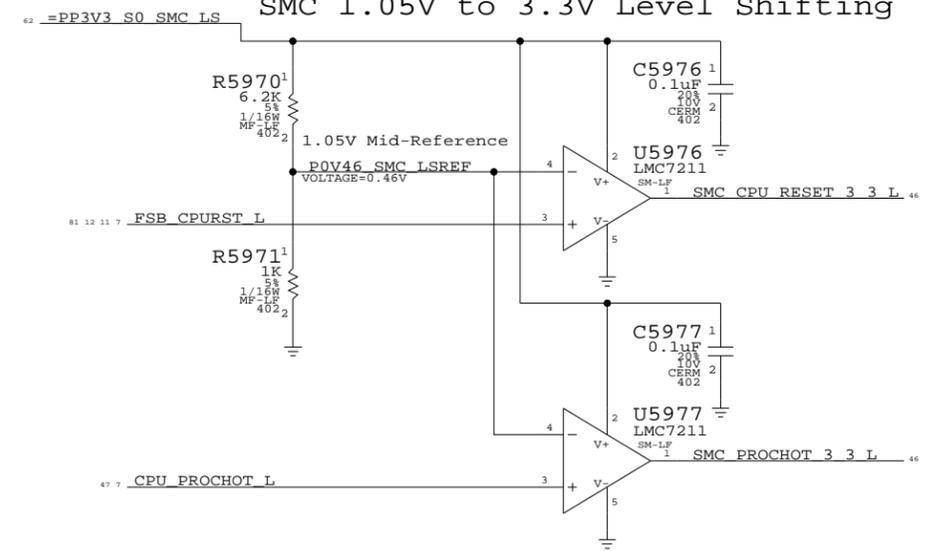
Reports when 5V S5 and 3.3V S5 are in regulation



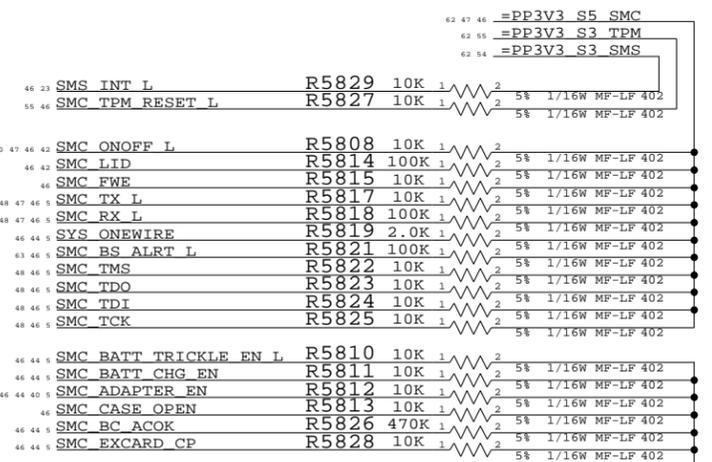
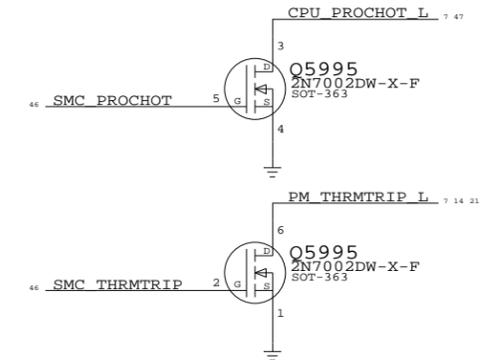
5V Comp threshold set to 4.476V (89%)
ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal



SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



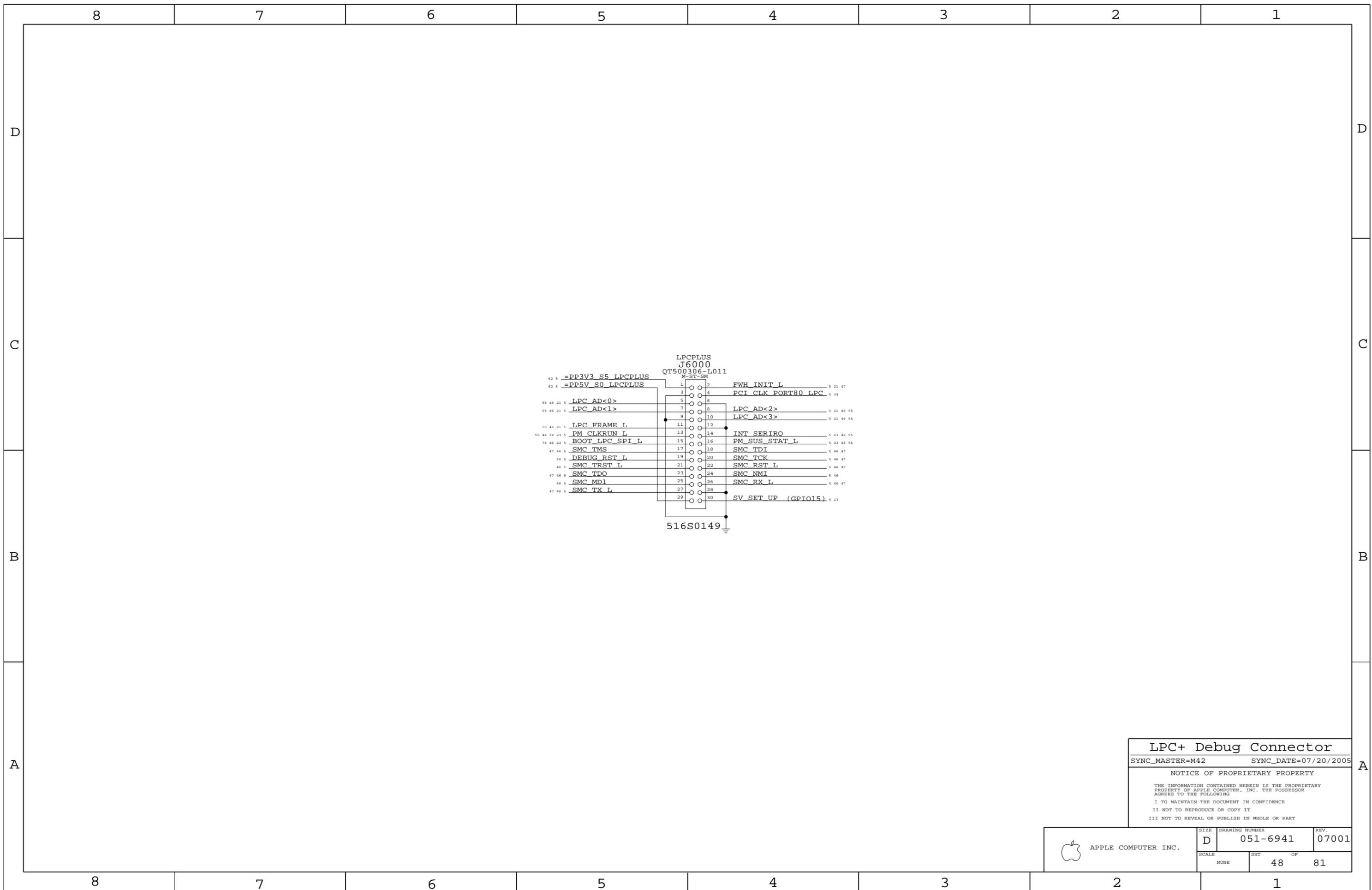
SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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		47	81



LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

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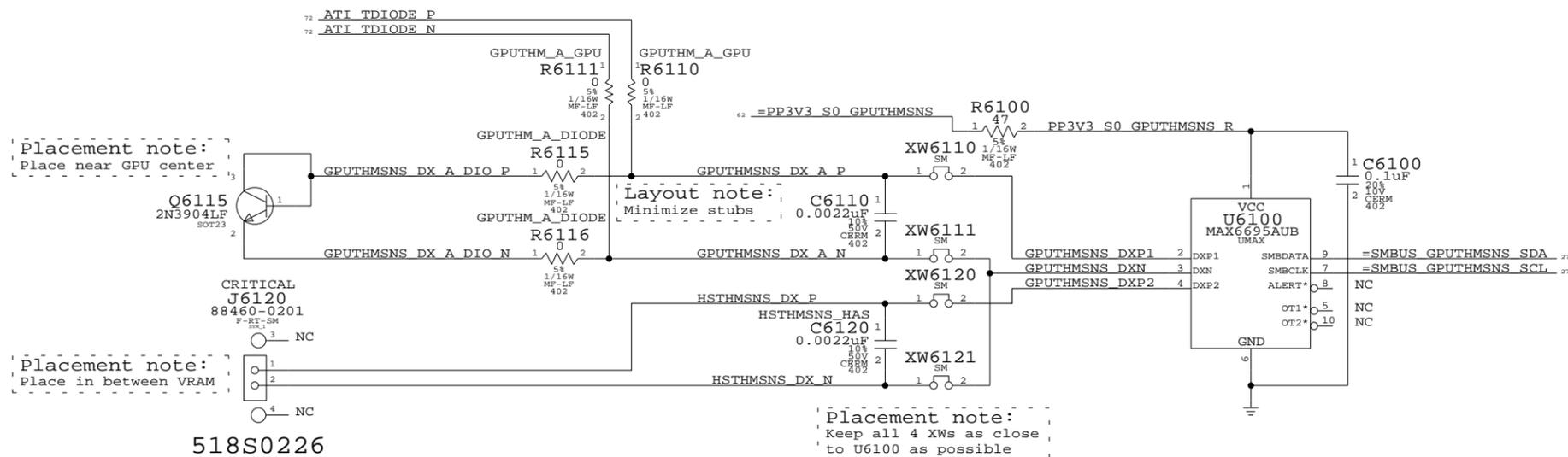
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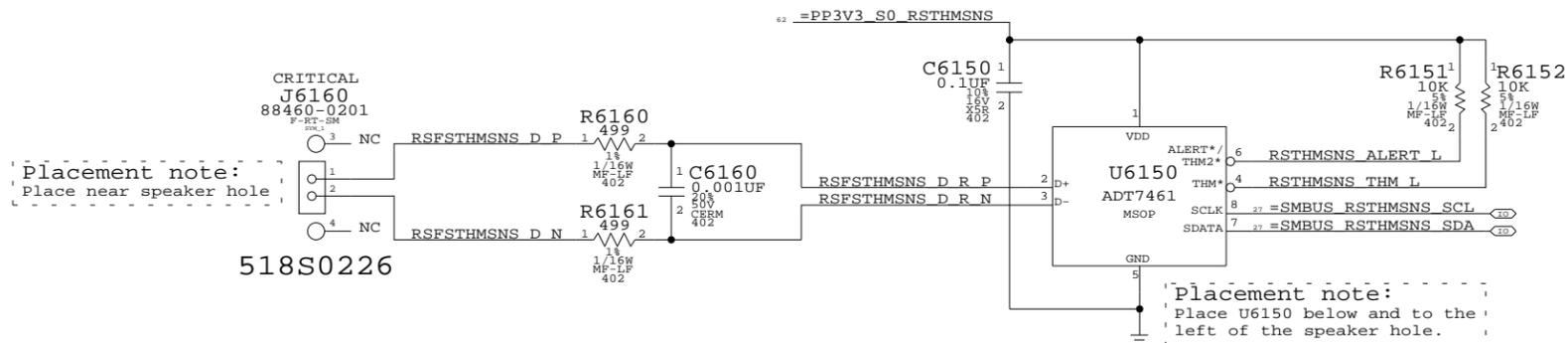
 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 07001
	SCALE NONE	SHEET 48	OF 81

GPU / Heat Pipe Thermal Sensor

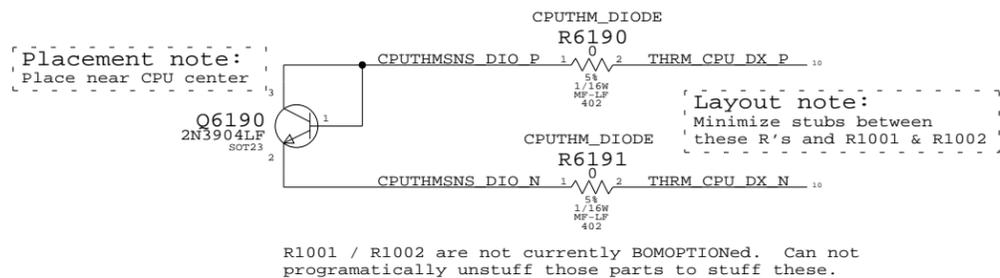


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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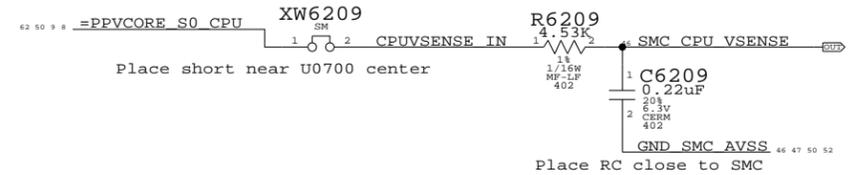
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II NOT TO REPRODUCE OR COPY IT

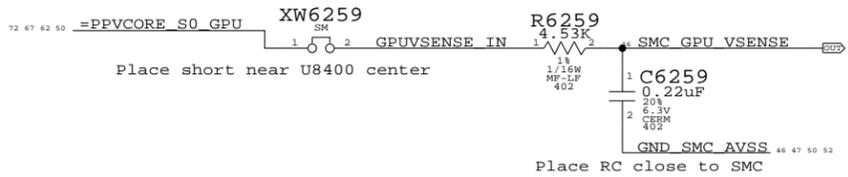
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT OF		
NONE	49 OF		81

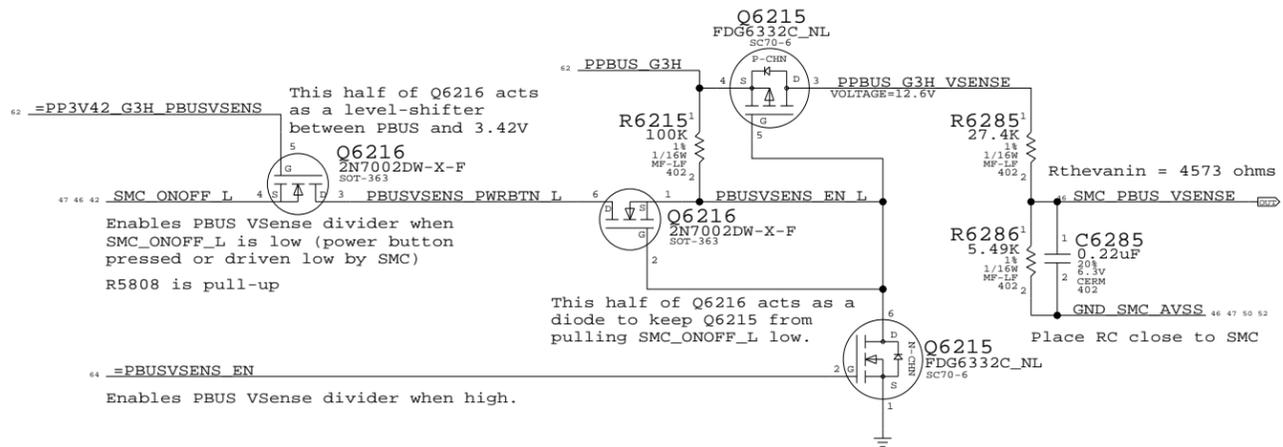
CPU Voltage Sense / Filter



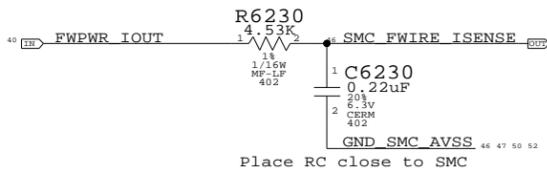
GPU Voltage Sense / Filter



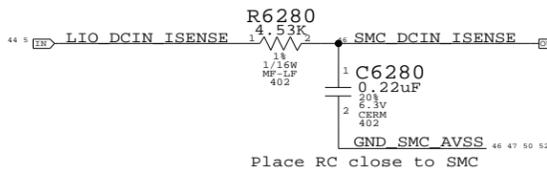
PBUS Voltage Sense Enable & Filter



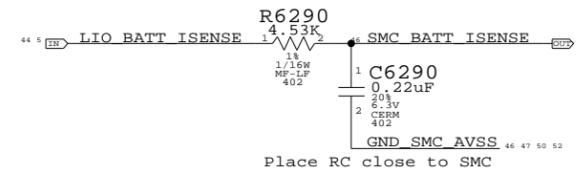
FireWire Current Sense Filter



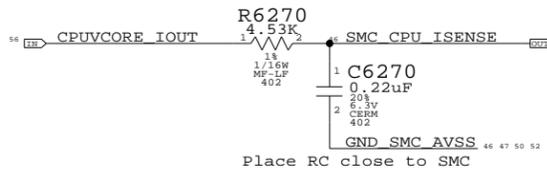
DCIN Current Sense Filter



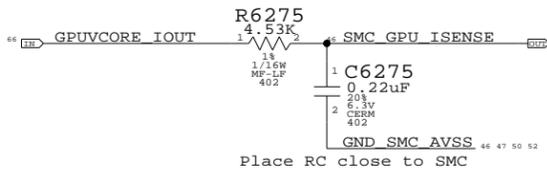
Battery Current Sense Filter



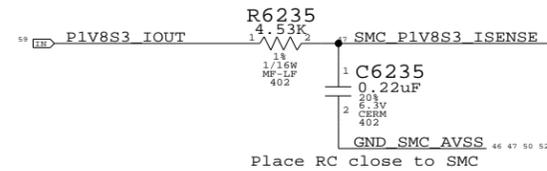
CPU Current Sense Filter



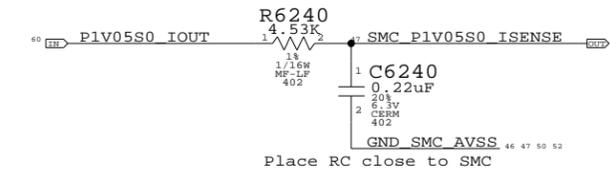
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

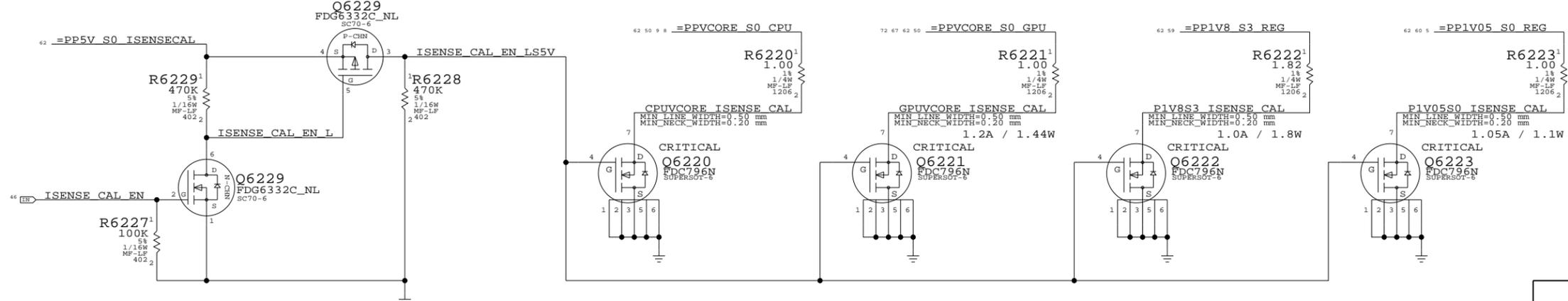


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

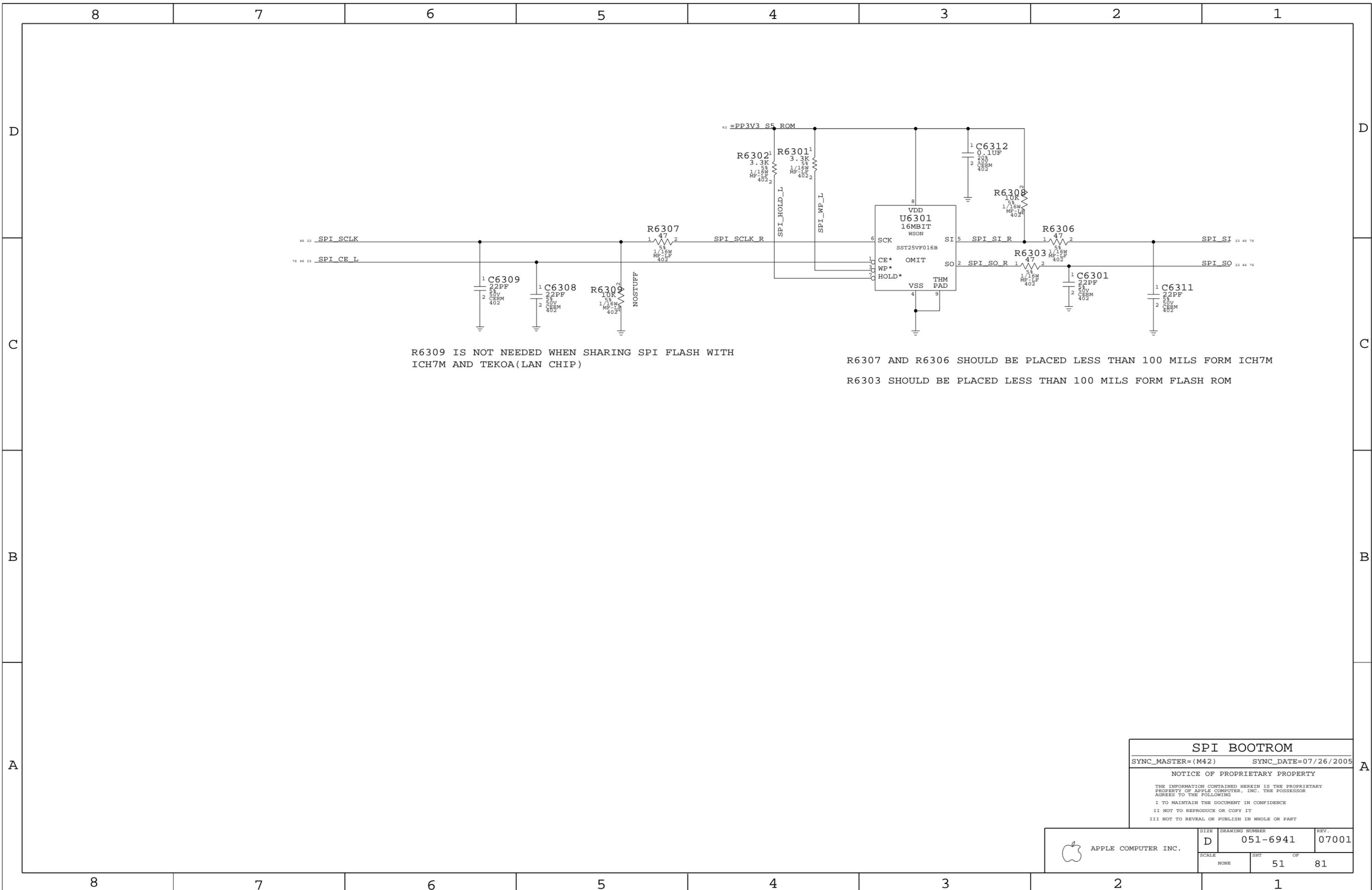
Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	50	81	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

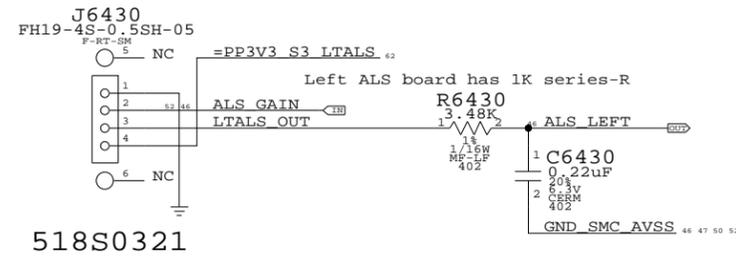
R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
 R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM
 SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

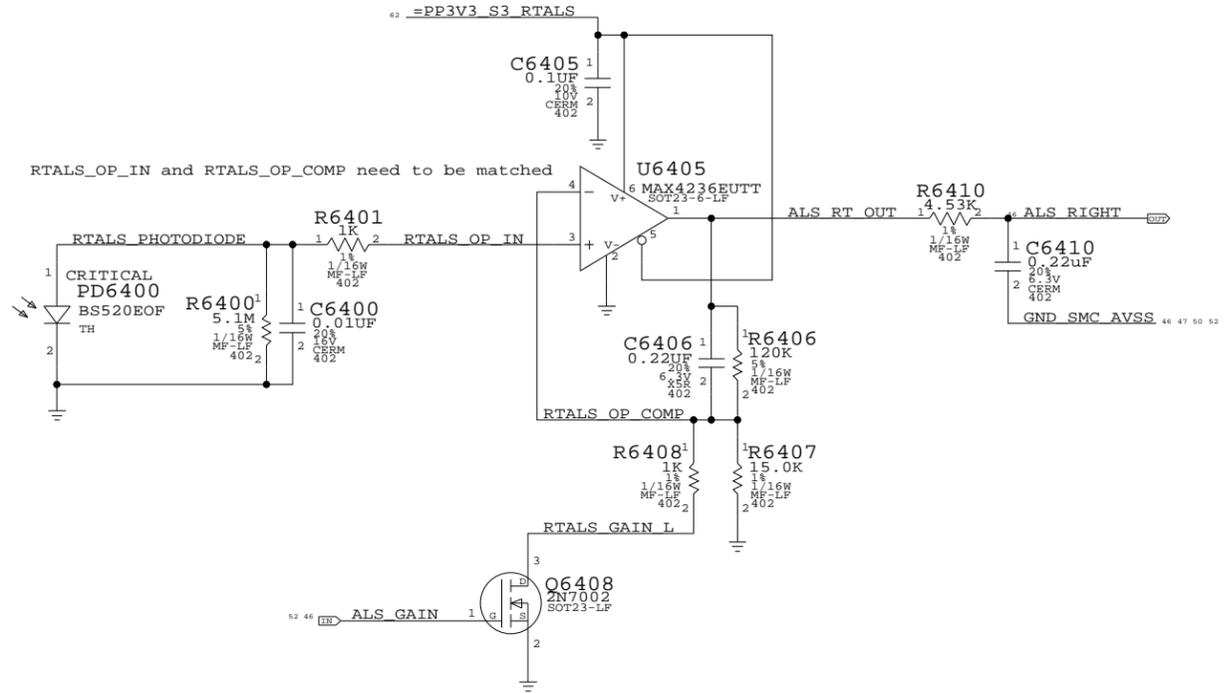
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SCALE	SHT OF		
NONE	51 OF		81

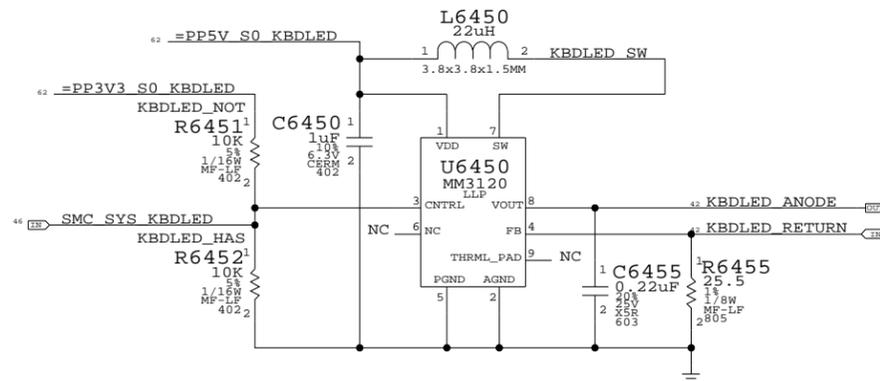
Left ALS "Connector"



Right ALS Circuit

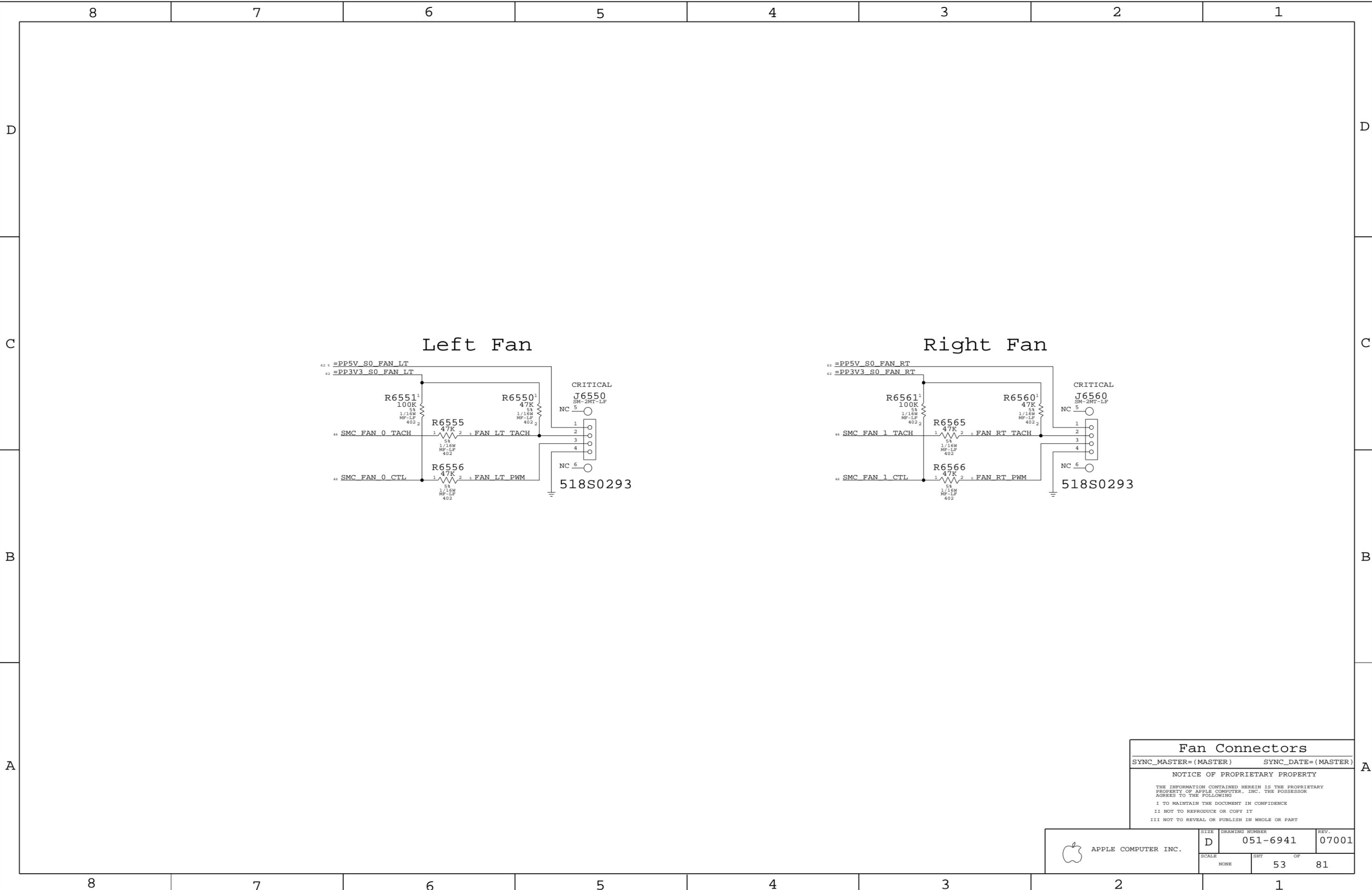


Keyboard LED Driver



ALS Support
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SCALE	SHT	OF	
NONE	52	81	



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE		SHT	OF
NONE		53	81

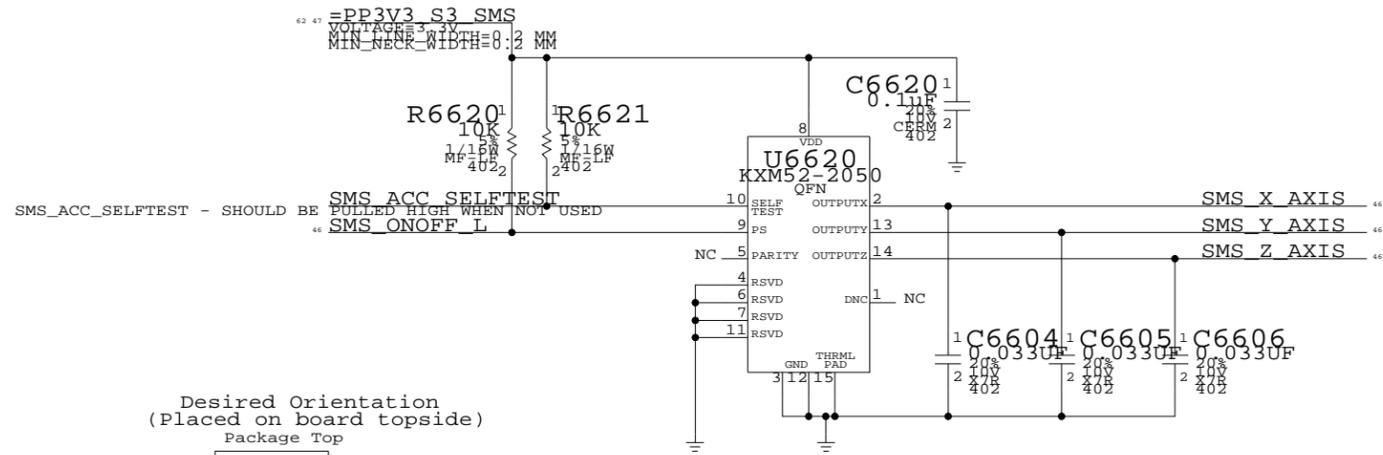
PAGE NOTES

INPUT
 =PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
 SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

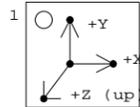
OUTPUT
 SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
 7/28/2005 - REMOVED BOU TABLE AND UPDATED SYMBOL TO KXM52-2050
 7/28/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L



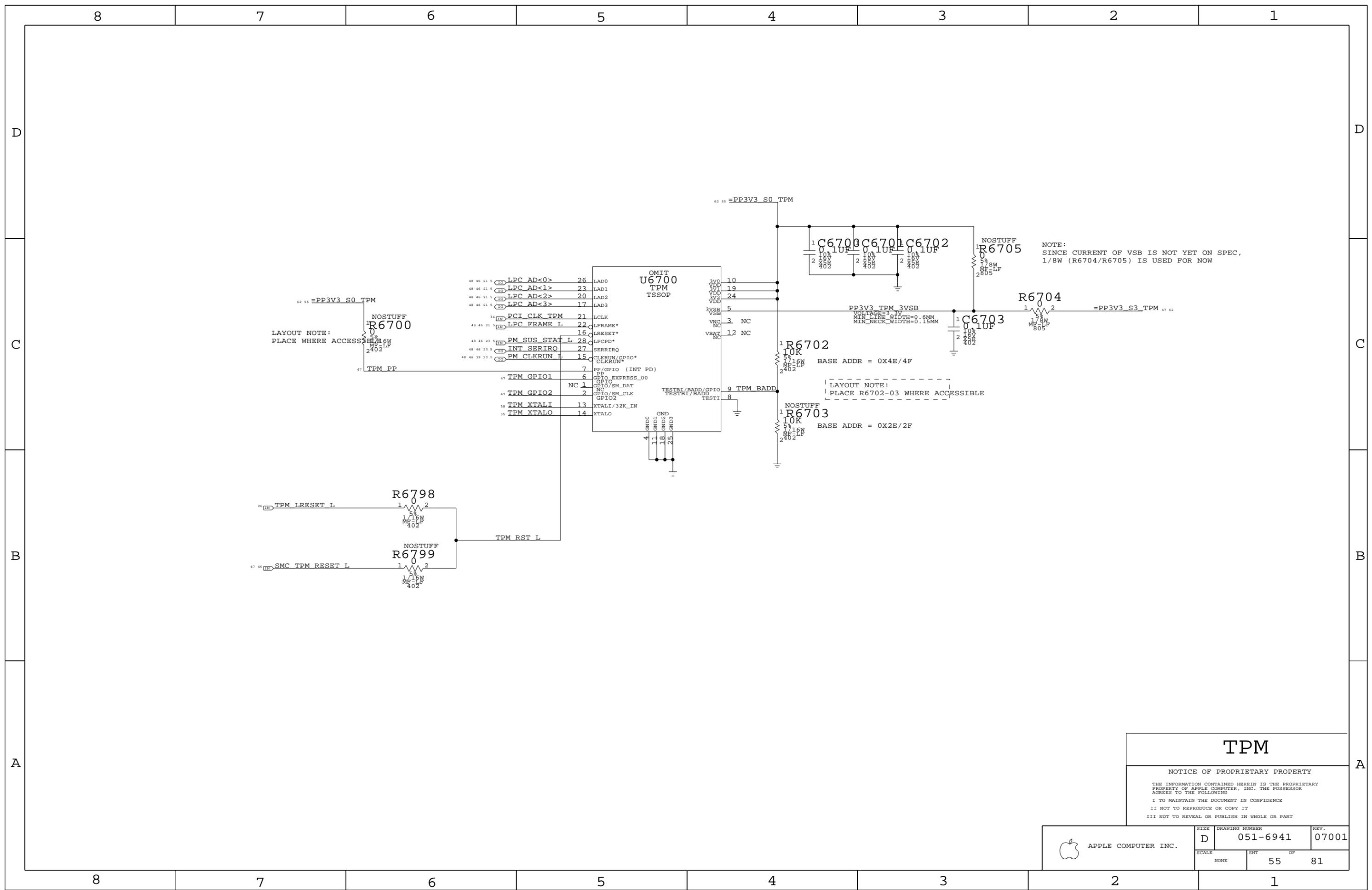
Desired Orientation
 (Placed on board topside)
 Package Top



SMS
 SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

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SCALE	SHT	OF	
NONE	54	81	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

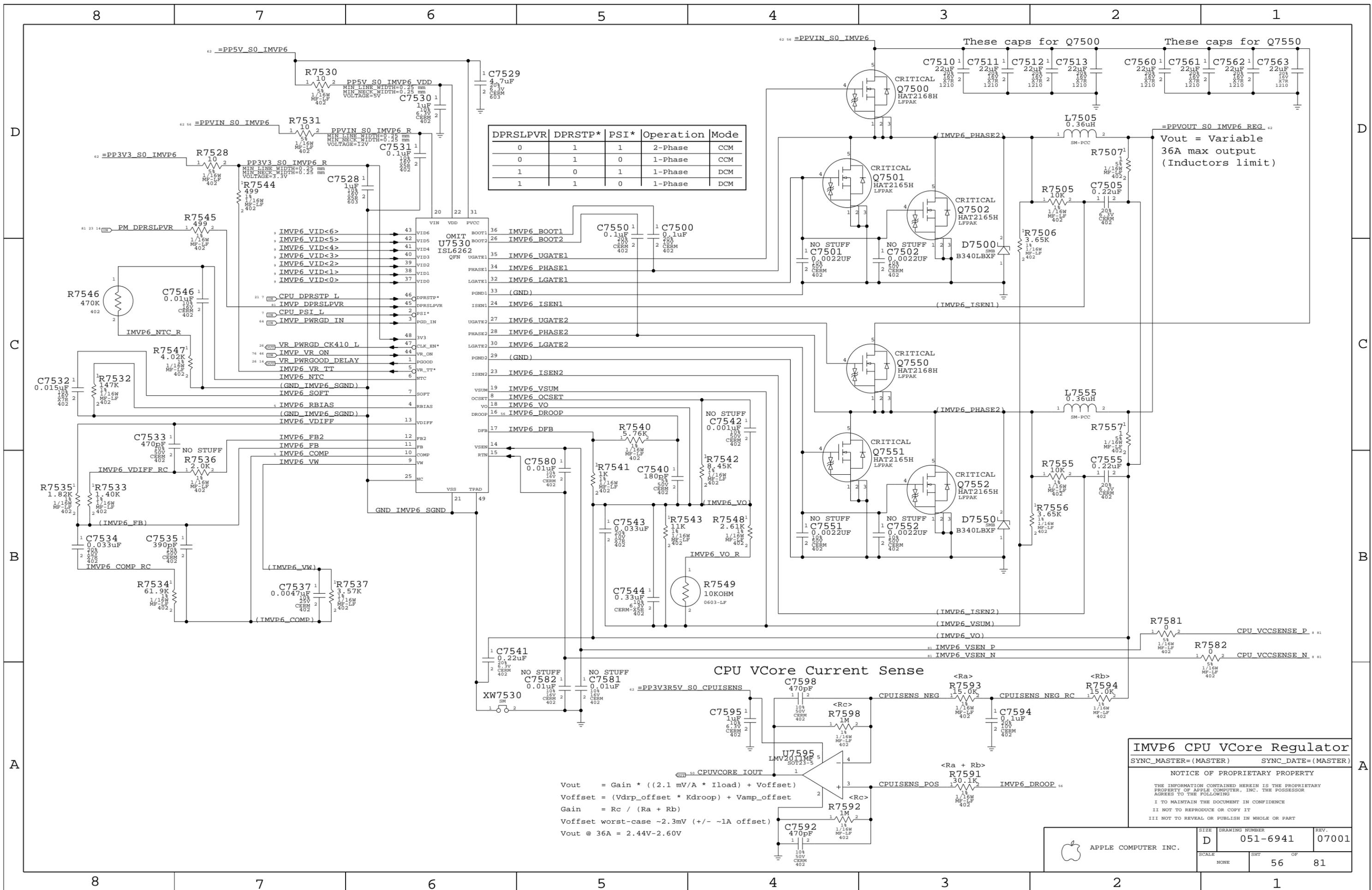
TPM

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SCALE	SHT	OF	
NONE	55	81	



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

$$V_{out} = Gain * ((2.1 \text{ mV/A} * I_{load}) + V_{offset})$$

$$V_{offset} = (V_{drp_offset} * K_{droop}) + V_{amp_offset}$$

$$Gain = R_c / (R_a + R_b)$$

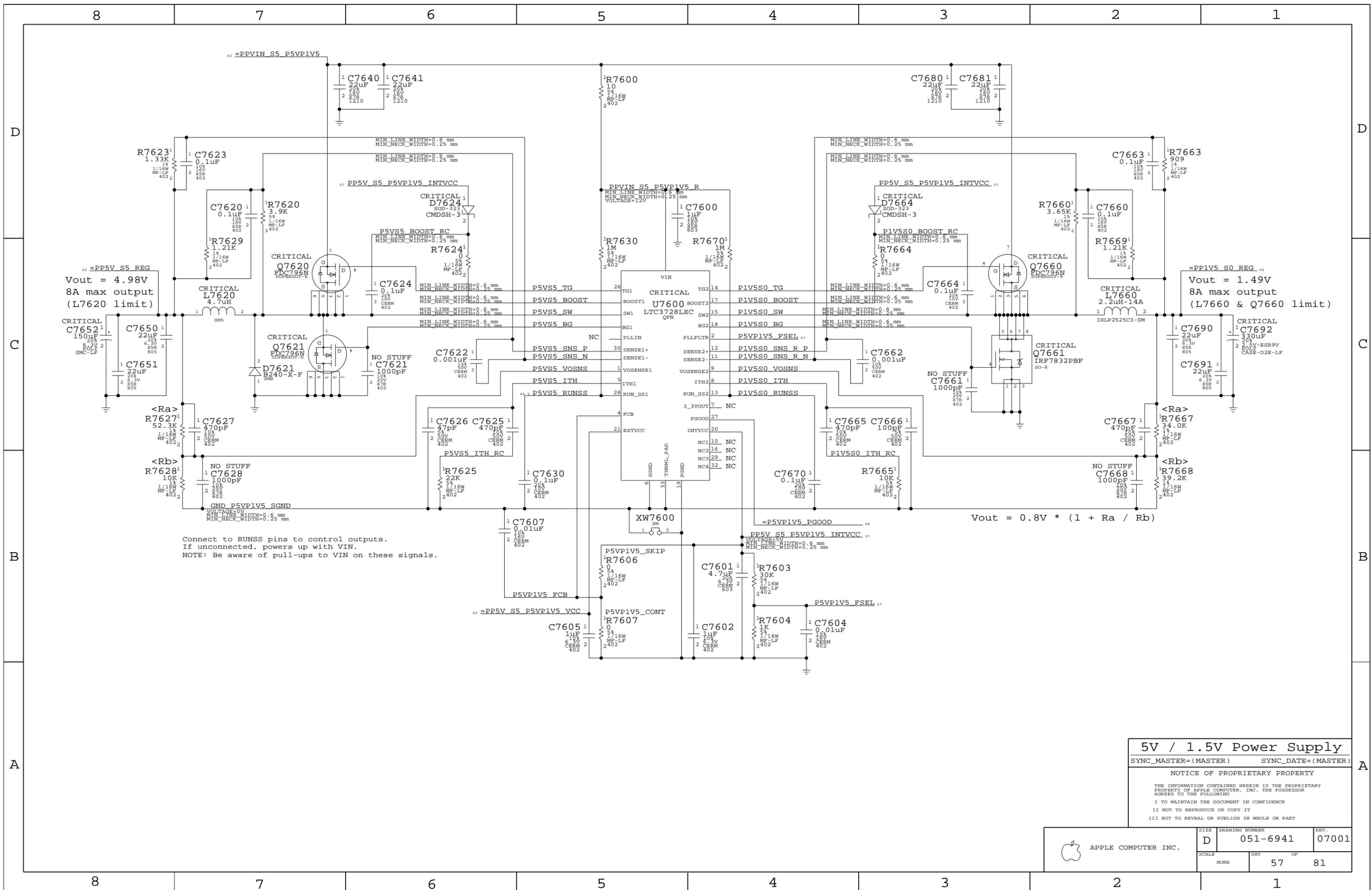
$$V_{offset \text{ worst-case}} \sim 2.3\text{mV} (+/- \sim 1\text{A offset})$$

$$V_{out @ 36\text{A}} = 2.44\text{V} - 2.60\text{V}$$

IMVP6 CPU VCore Regulator
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	56	81	



5V / 1.5V Power Supply

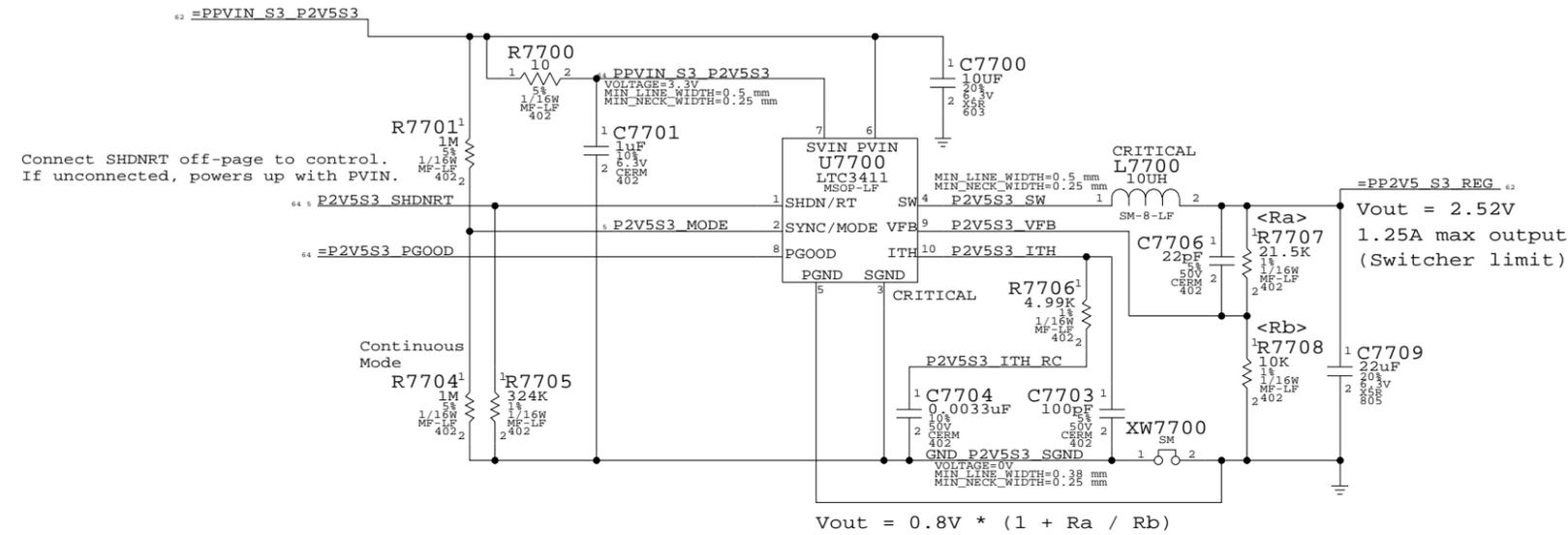
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

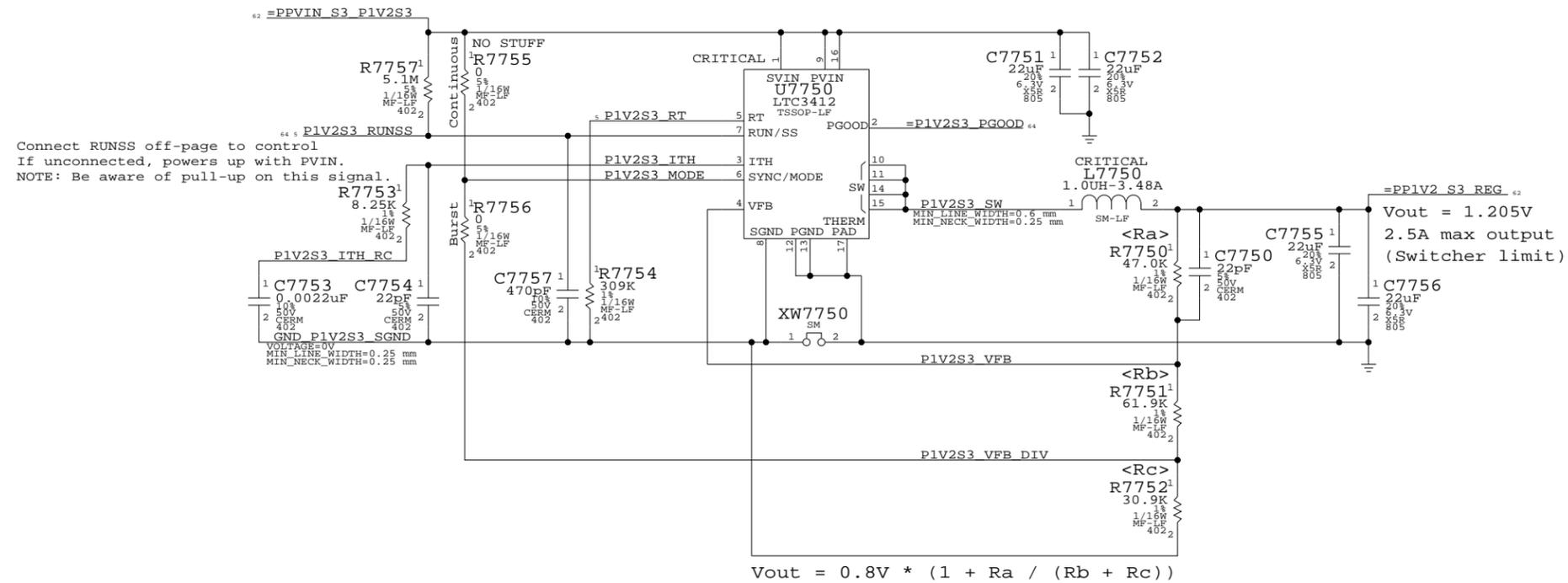
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	D	051-6941	07001
SCALE	SHT	OF	
NONE	57	81	

2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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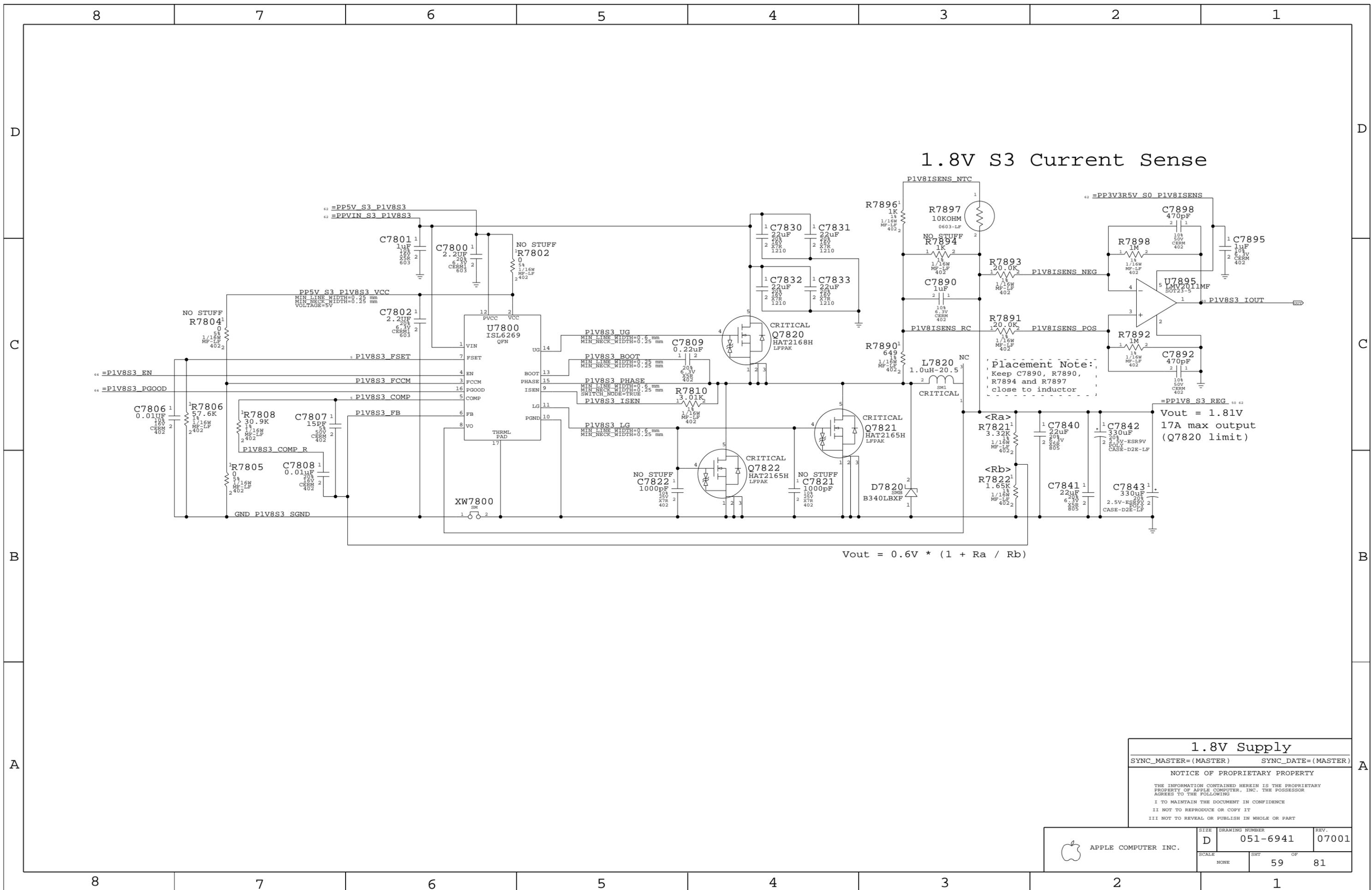
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	58	81



1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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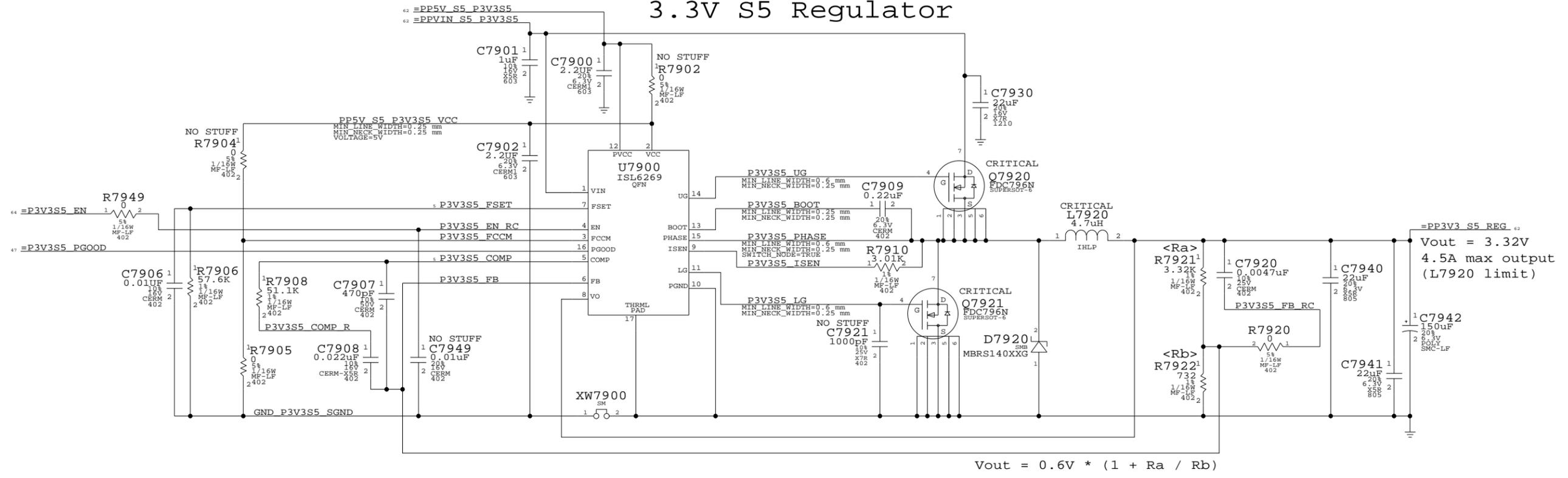
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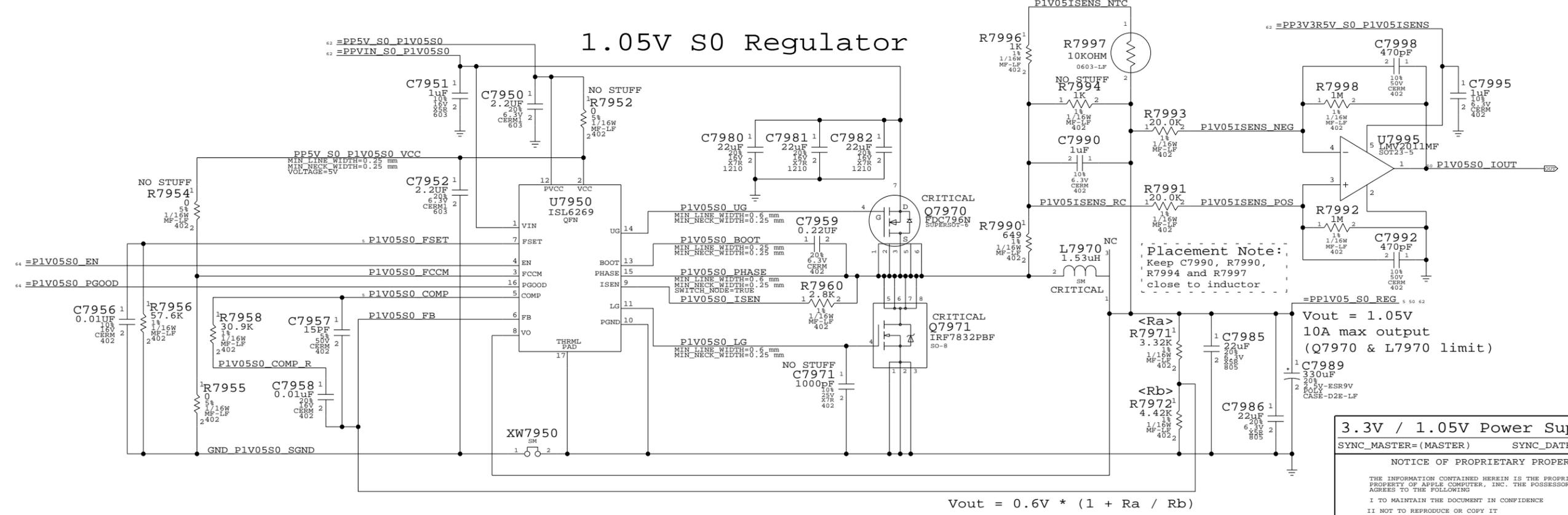
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT	OF	
NONE	59	81	

3.3V S5 Regulator



1.05V Current Sense

1.05V S0 Regulator



3.3V / 1.05V Power Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	60	81	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

4

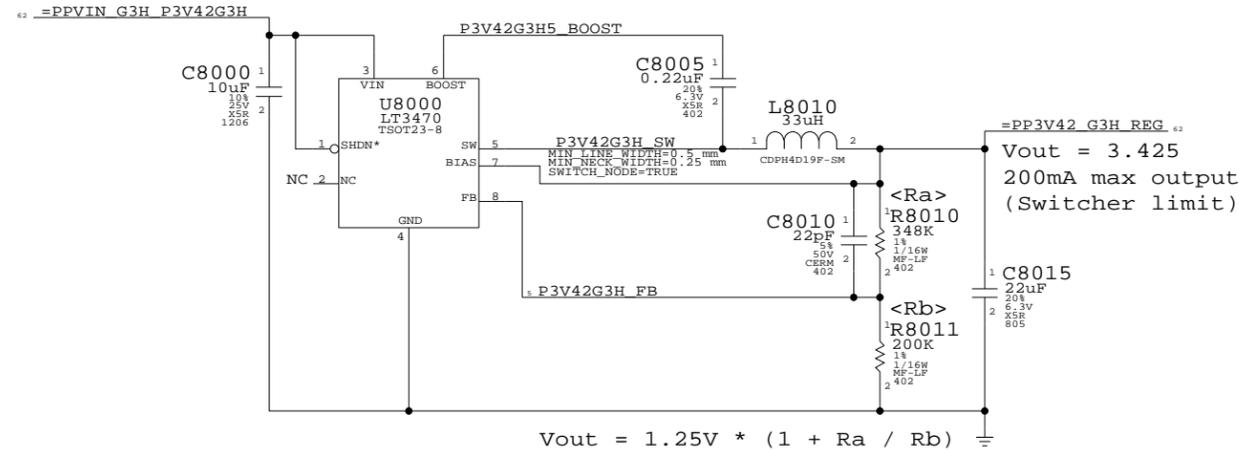
3

2

1

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



3.3V G3Hot Supply

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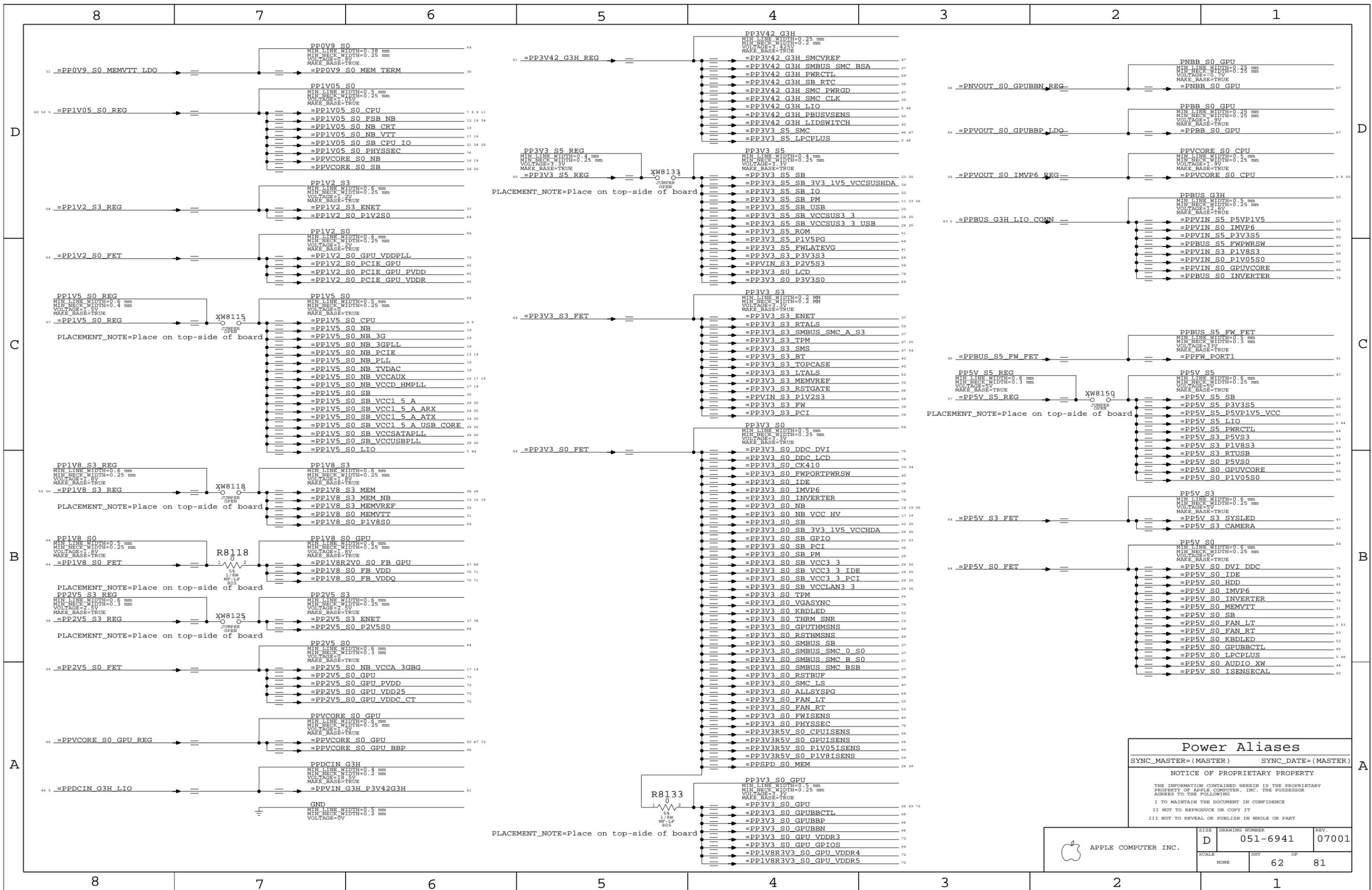
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NONE	61	81



Power Aliases

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	D	051-6941	07001
SCALE	SHEET	OF	
NONE	62	81	

8

7

6

5

4

3

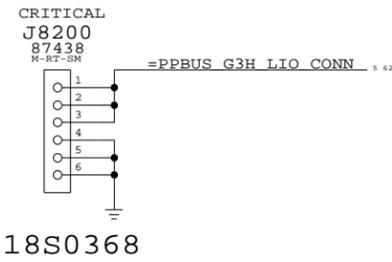
2

1

D

D

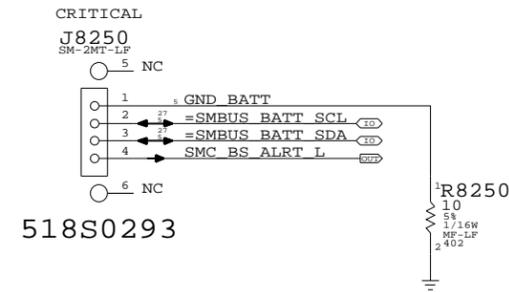
Left I/O Power Connector



C

C

Battery Connector (Digital Signals)



B

B

A

A

PBus-In & Battery Connectors
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	07001
SCALE	SHT OF		
NONE	63 OF		81

8

7

6

5

4

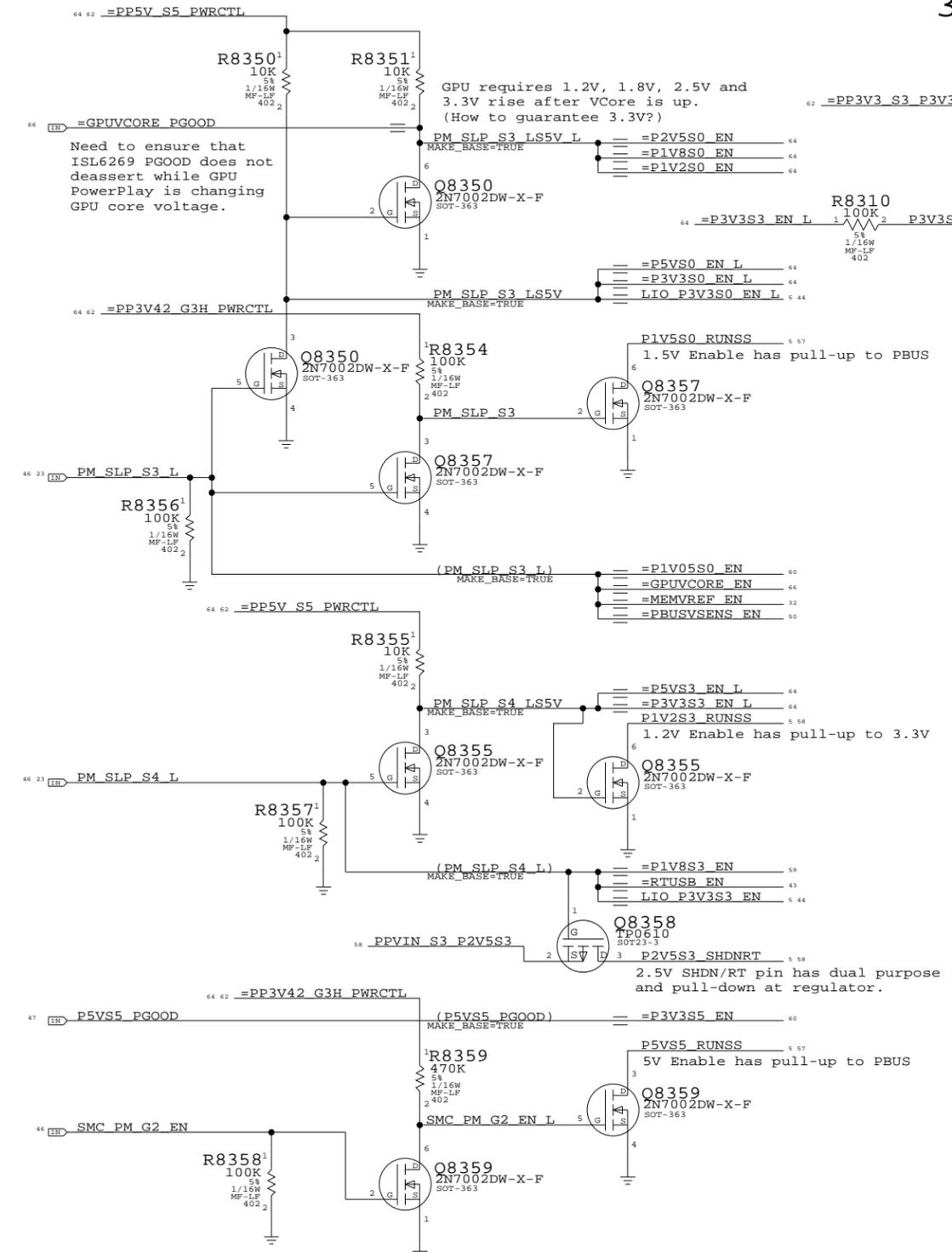
3

2

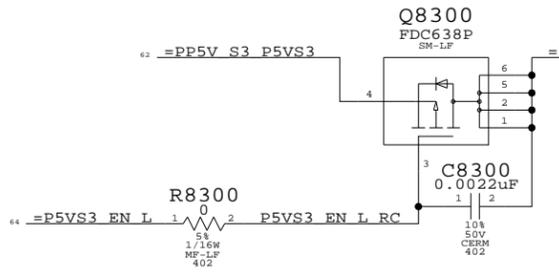
1

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

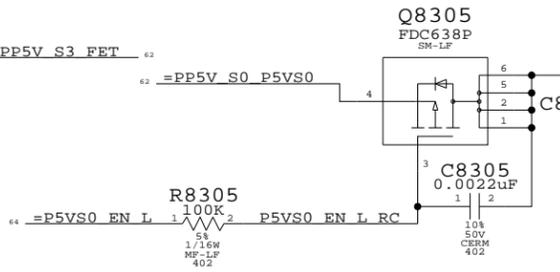
Power Control Signals



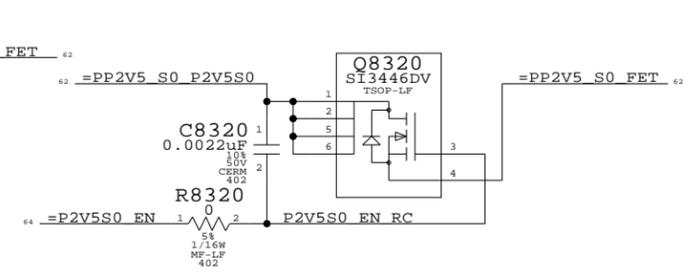
5V S3 FET



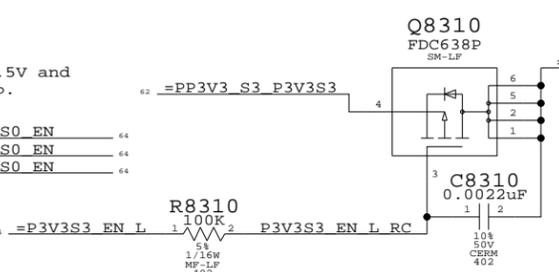
5V S0 FET



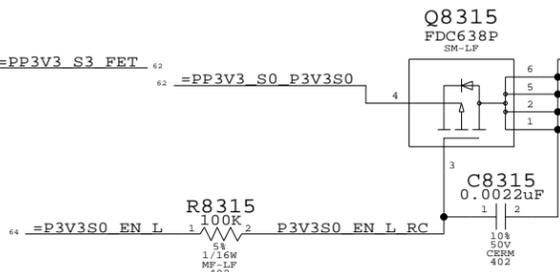
2.5V S0 FET



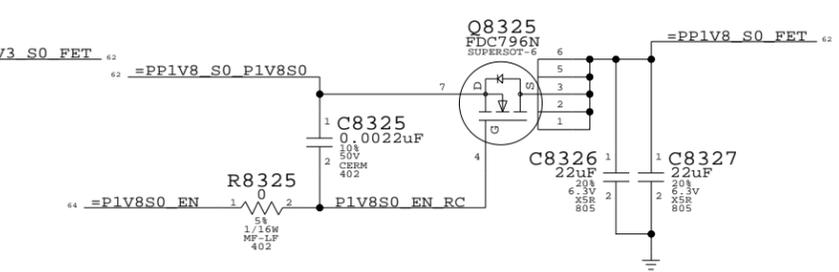
3.3V S3 FET



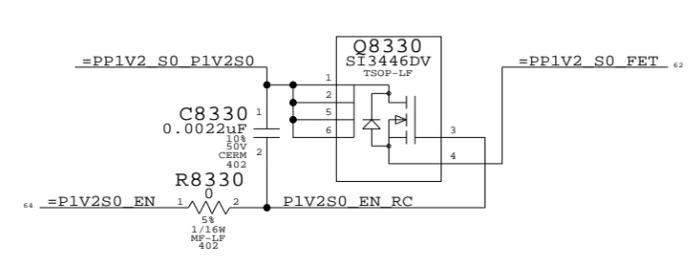
3.3V S0 FET



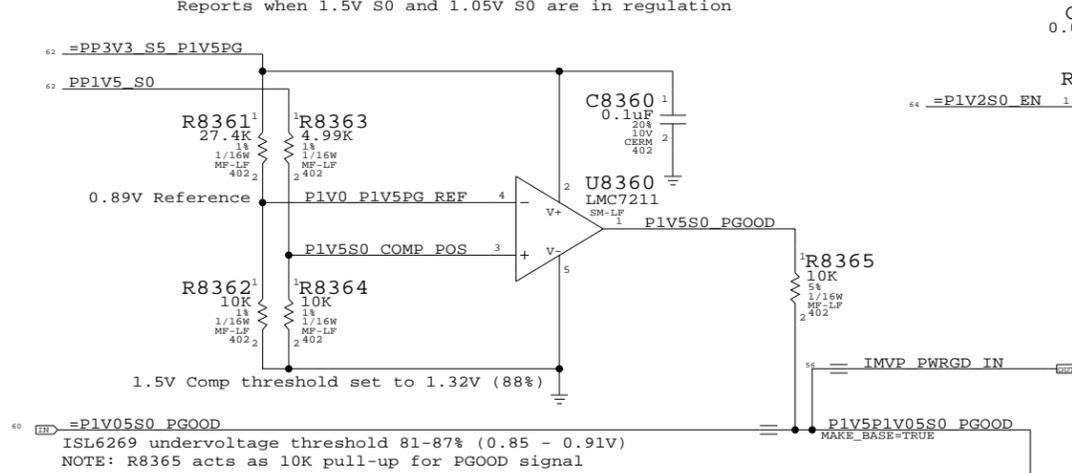
1.8V S0 FET



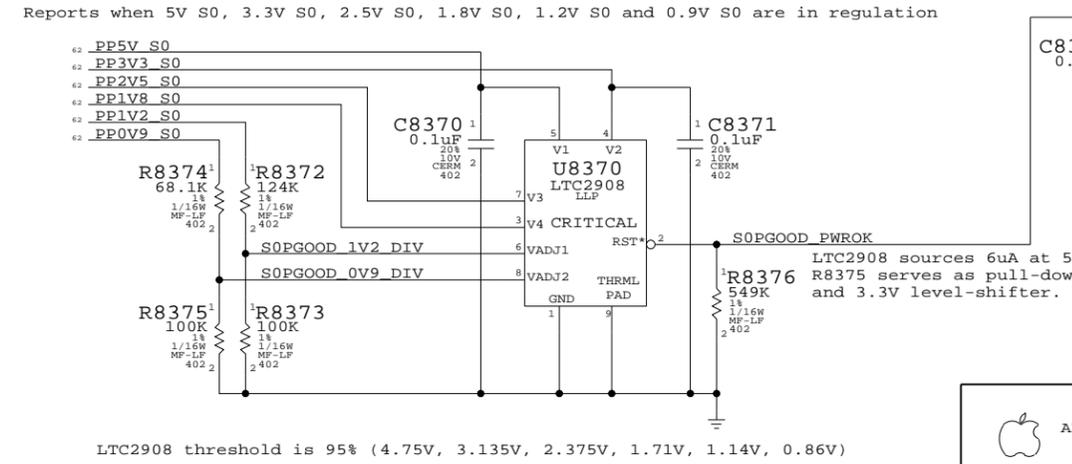
1.2V S0 FET



1.5V / 1.05V PWRGD Circuit



Other S0 Rails PWRGD Circuit



Unused PGOOD Signals

=P5VP1V5_PGOOD	=TP_P5V_P1V5_PGOOD
=P2V5S3_PGOOD	=TP_P2V5S3_PGOOD
=P1V8S3_PGOOD	=TP_P1V8S3_PGOOD
=P1V2S3_PGOOD	=TP_P1V2S3_PGOOD

These rails are monitored by LTC2908

S3/S0 FETs & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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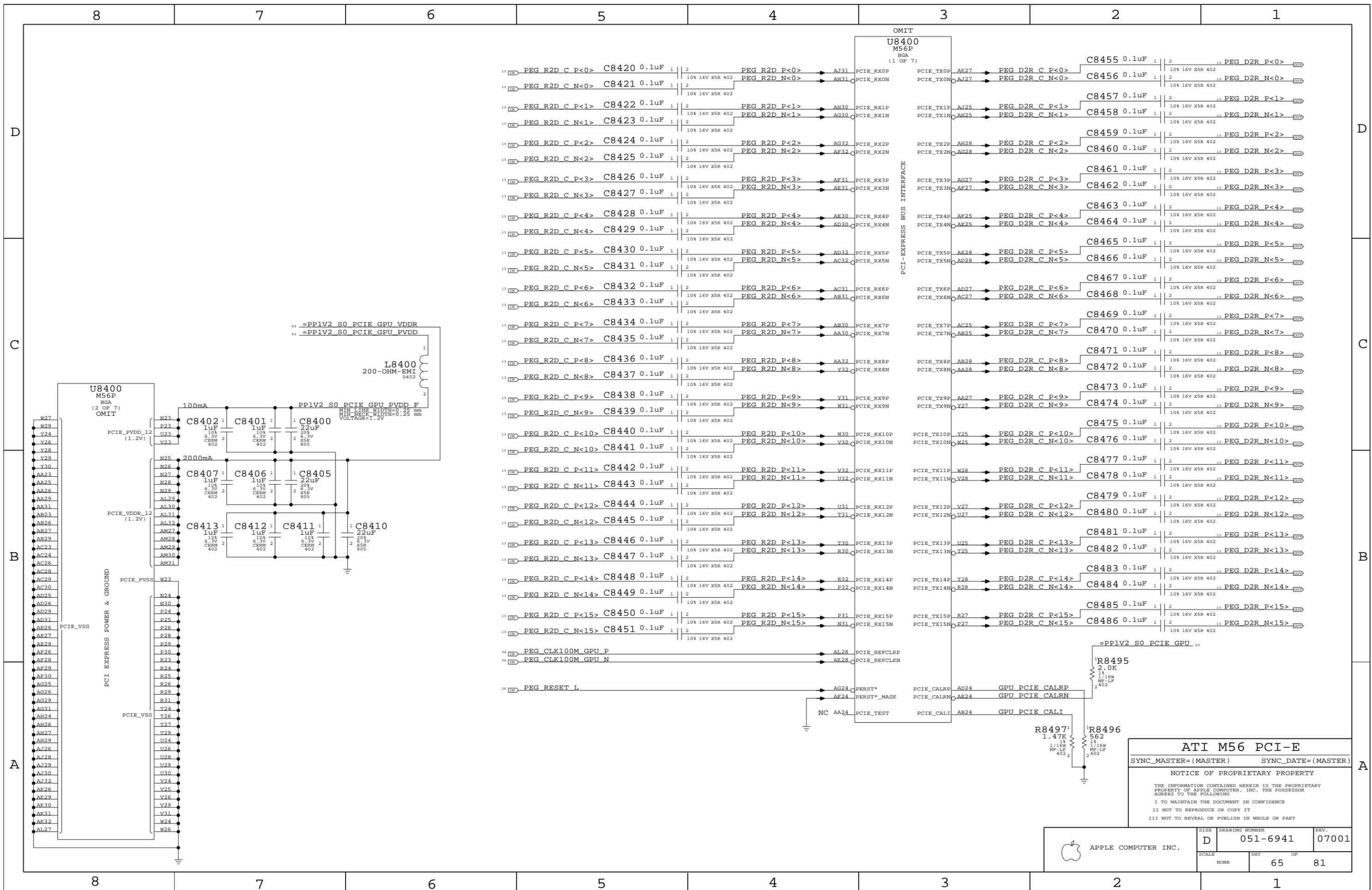
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ATI M56 PCI-E
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	D	051-6941	07001
SCALE	NONE	SHT	OF
		65	81

Page Notes

Power aliases required by this page:

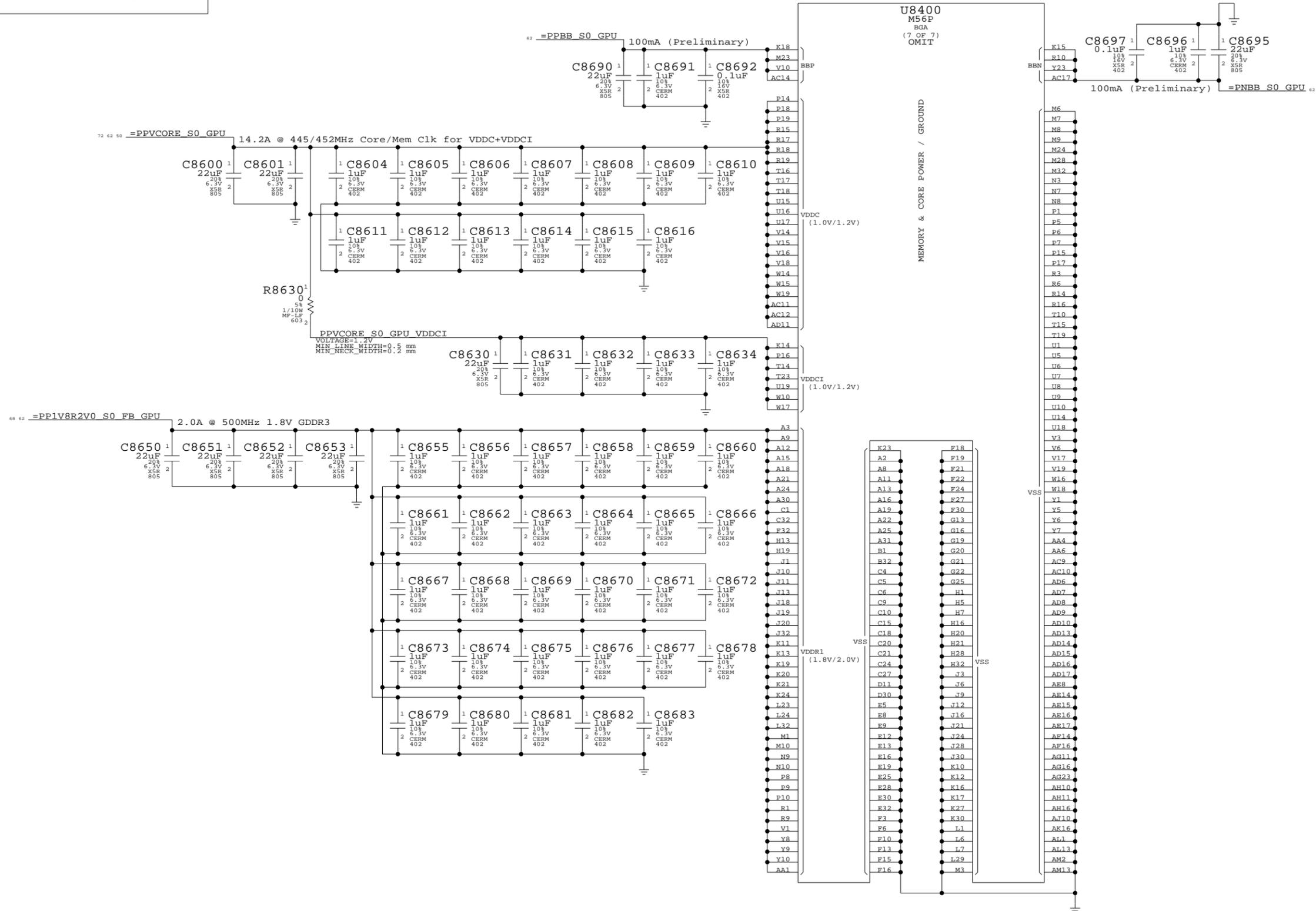
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



ATI M56 Core Power
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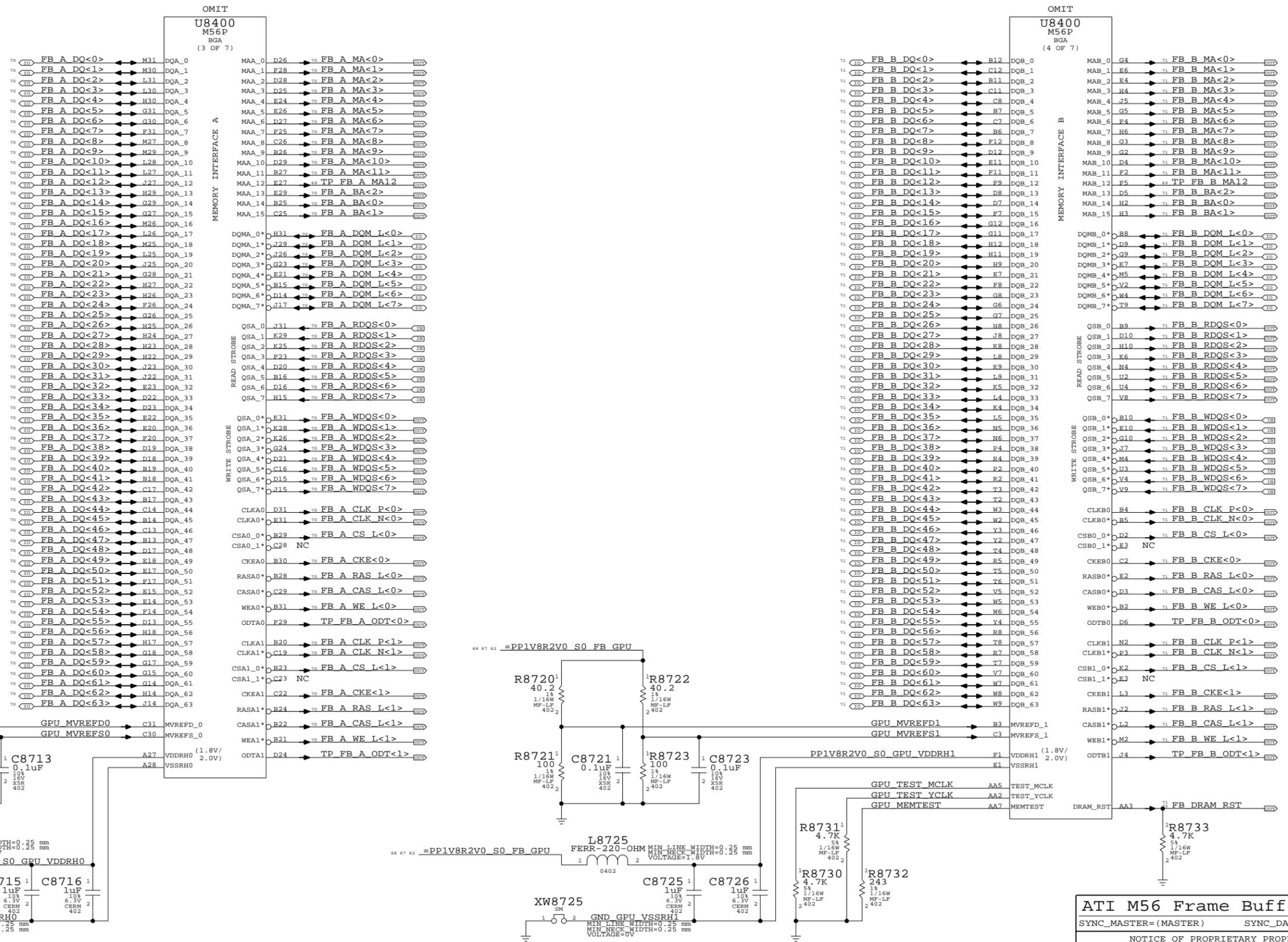
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	NONE	SHT	OF
		67	81

Page Notes

Power aliases required by this page:
 - =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
 (NONE)

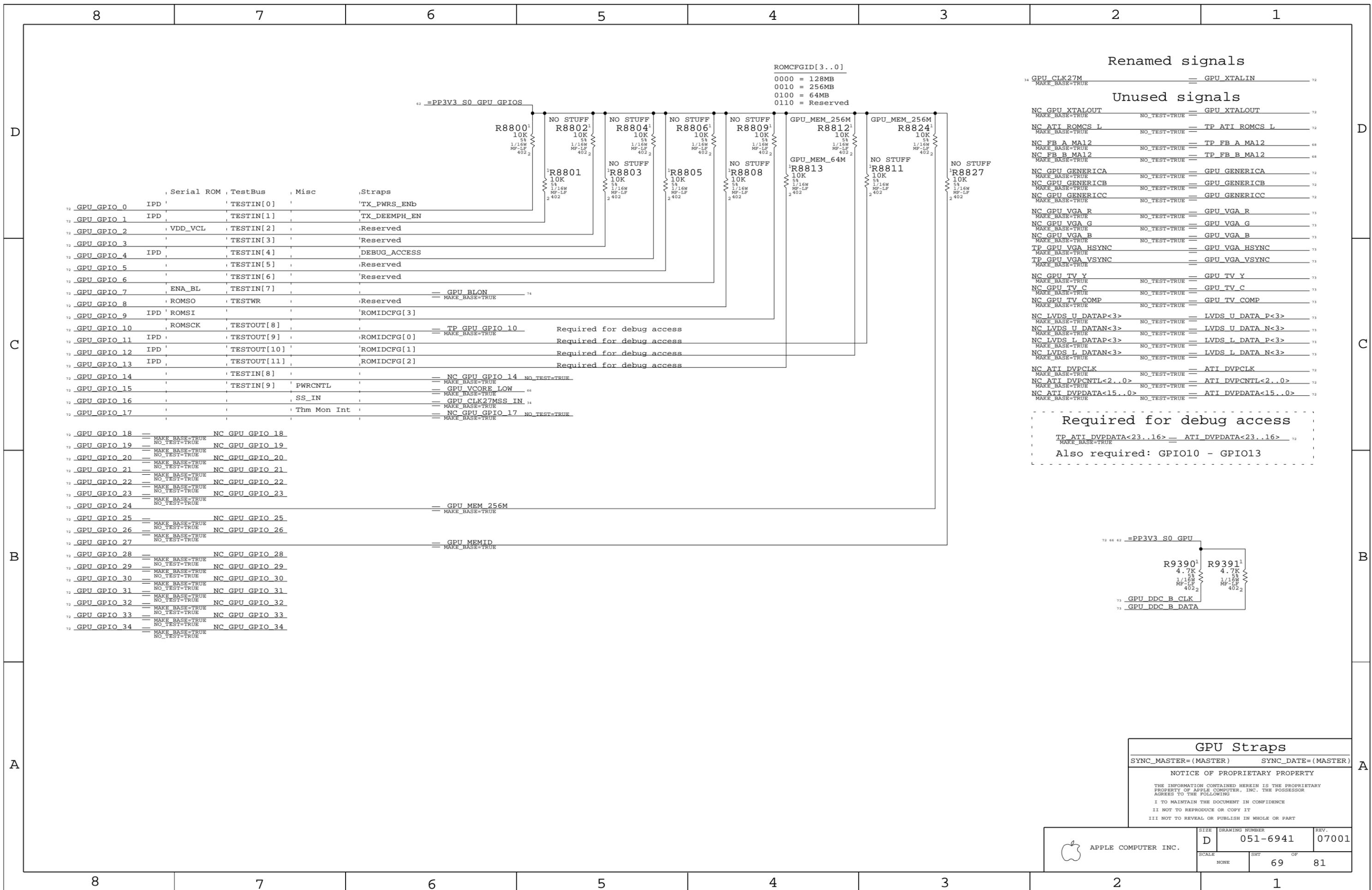
BOM options provided by this page:
 (NONE)



ATI M56 Frame Buffer I/F
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	68	81	



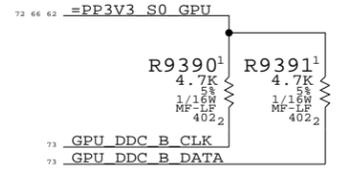
ROMCFGID[3..0]
 0000 = 128MB
 0010 = 256MB
 0100 = 64MB
 0110 = Reserved

Renamed signals

- GPU_CLK27M == GPU_XTALIN
- NC_GPU_XTALOUT == GPU_XTALOUT
- NC_ATI_ROMCS_L == TP_ATI_ROMCS_L
- NC_FB_A_MAI2 == TP_FB_A_MAI2
- NC_FB_B_MAI2 == TP_FB_B_MAI2
- NC_GPU_GENERICA == GPU_GENERICA
- NC_GPU_GENERICB == GPU_GENERICB
- NC_GPU_GENERICC == GPU_GENERICC
- NC_GPU_VGA_R == GPU_VGA_R
- NC_GPU_VGA_G == GPU_VGA_G
- NC_GPU_VGA_B == GPU_VGA_B
- TP_GPU_VGA_HSYNC == GPU_VGA_HSYNC
- TP_GPU_VGA_VSYNC == GPU_VGA_VSYNC
- NC_GPU_TV_Y == GPU_TV_Y
- NC_GPU_TV_C == GPU_TV_C
- NC_GPU_TV_COMP == GPU_TV_COMP
- NC_LVDS_U_DATAP<3> == LVDS_U_DATA_P<3>
- NC_LVDS_U_DATAN<3> == LVDS_U_DATA_N<3>
- NC_LVDS_L_DATAP<3> == LVDS_L_DATA_P<3>
- NC_LVDS_L_DATAN<3> == LVDS_L_DATA_N<3>
- NC_ATI_DVPCLK == ATI_DVPCLK
- NC_ATI_DVPCNTL<2..0> == ATI_DVPCNTL<2..0>
- NC_ATI_DVPDATA<15..0> == ATI_DVPDATA<15..0>

Required for debug access

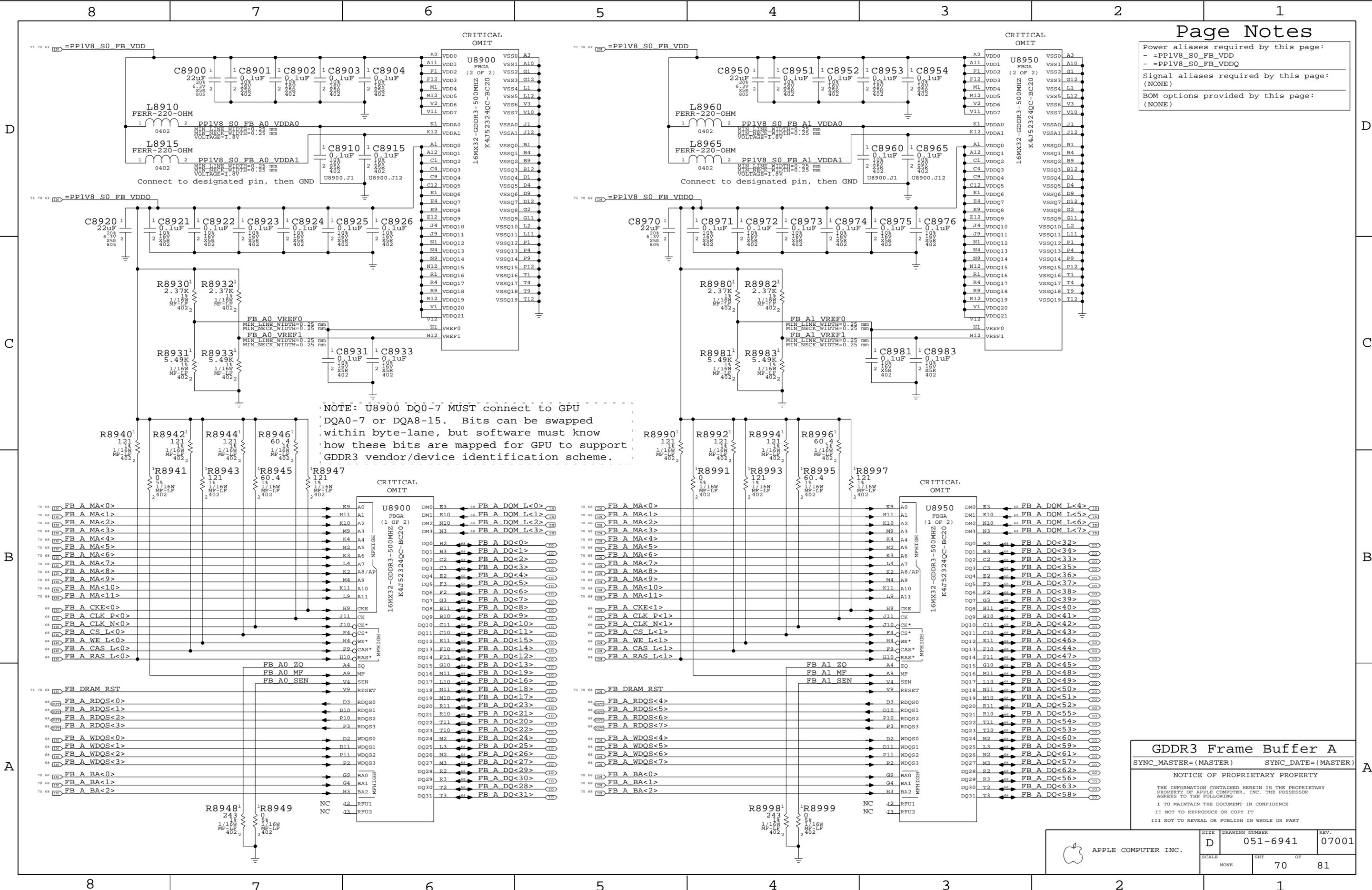
TP_ATI_DVPDATA<23..16> == ATI_DVPDATA<23..16>
 Also required: GPIO10 - GPIO13



GPU Straps
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	NONE	SHT	OF
		69	81

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

GDDR3 Frame Buffer A

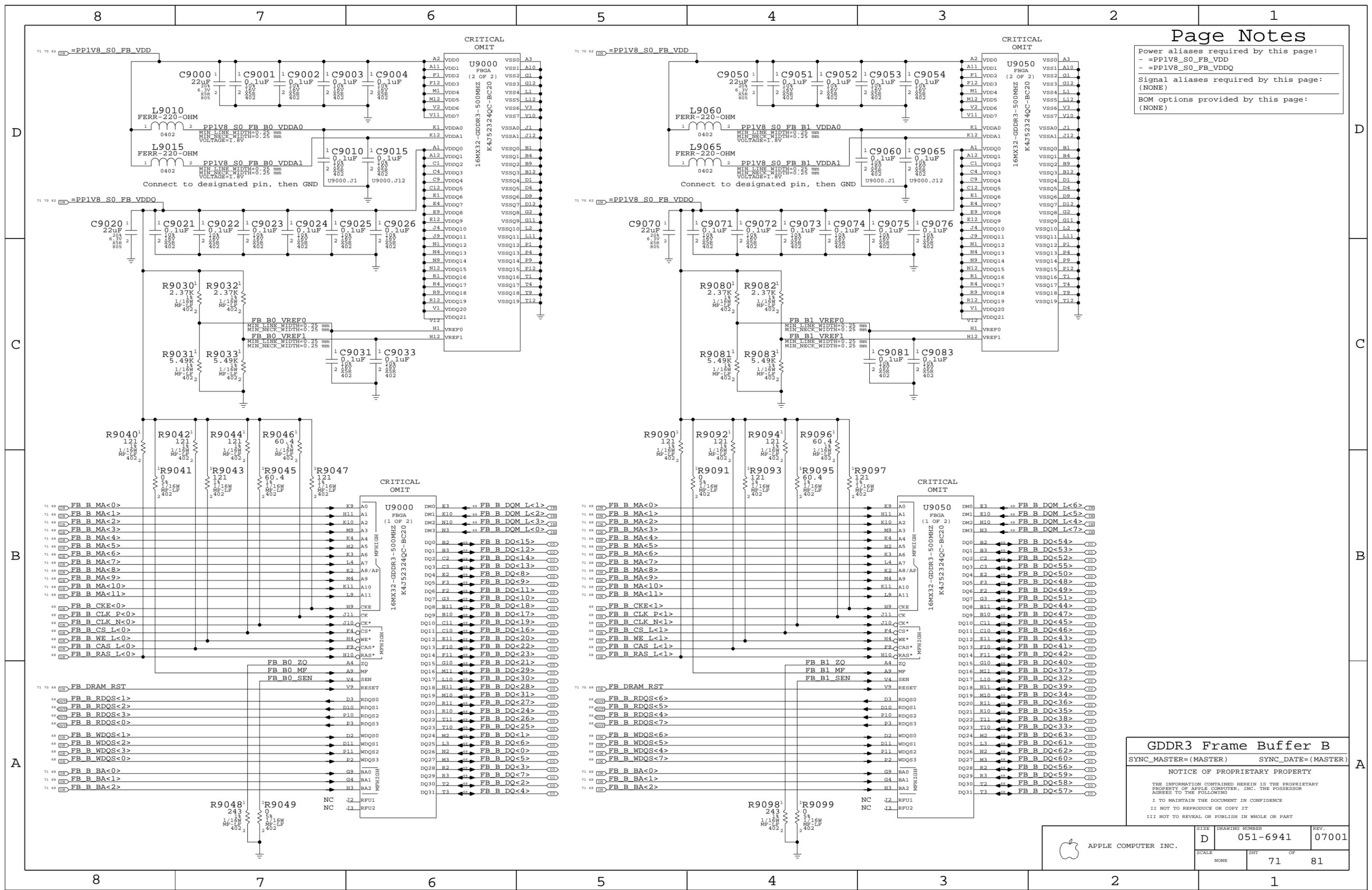
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHEET	OF	
NONE	70	81	

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



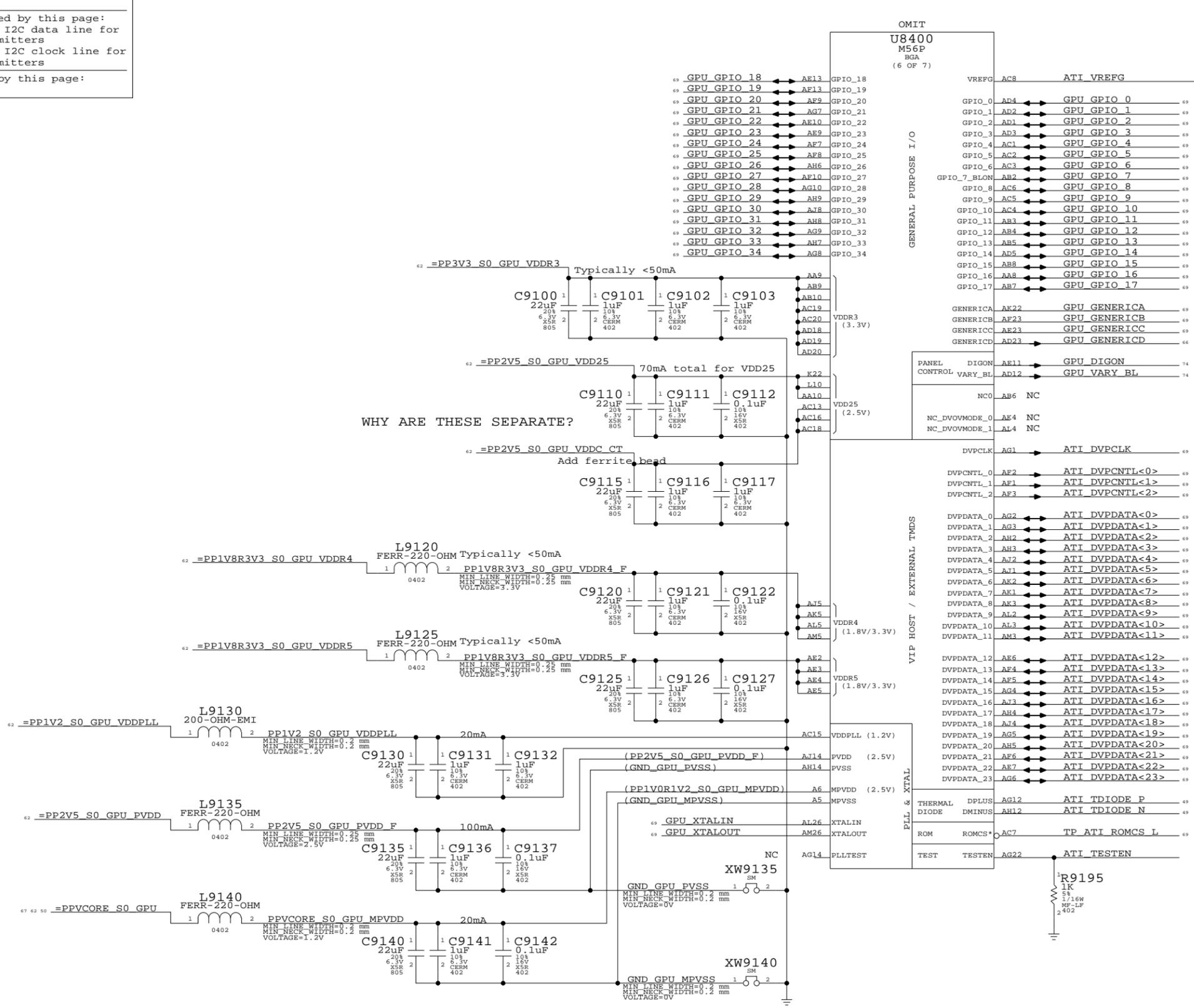
GDDR3 Frame Buffer B
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)



ATI M56 GPIO/DVO/Misc
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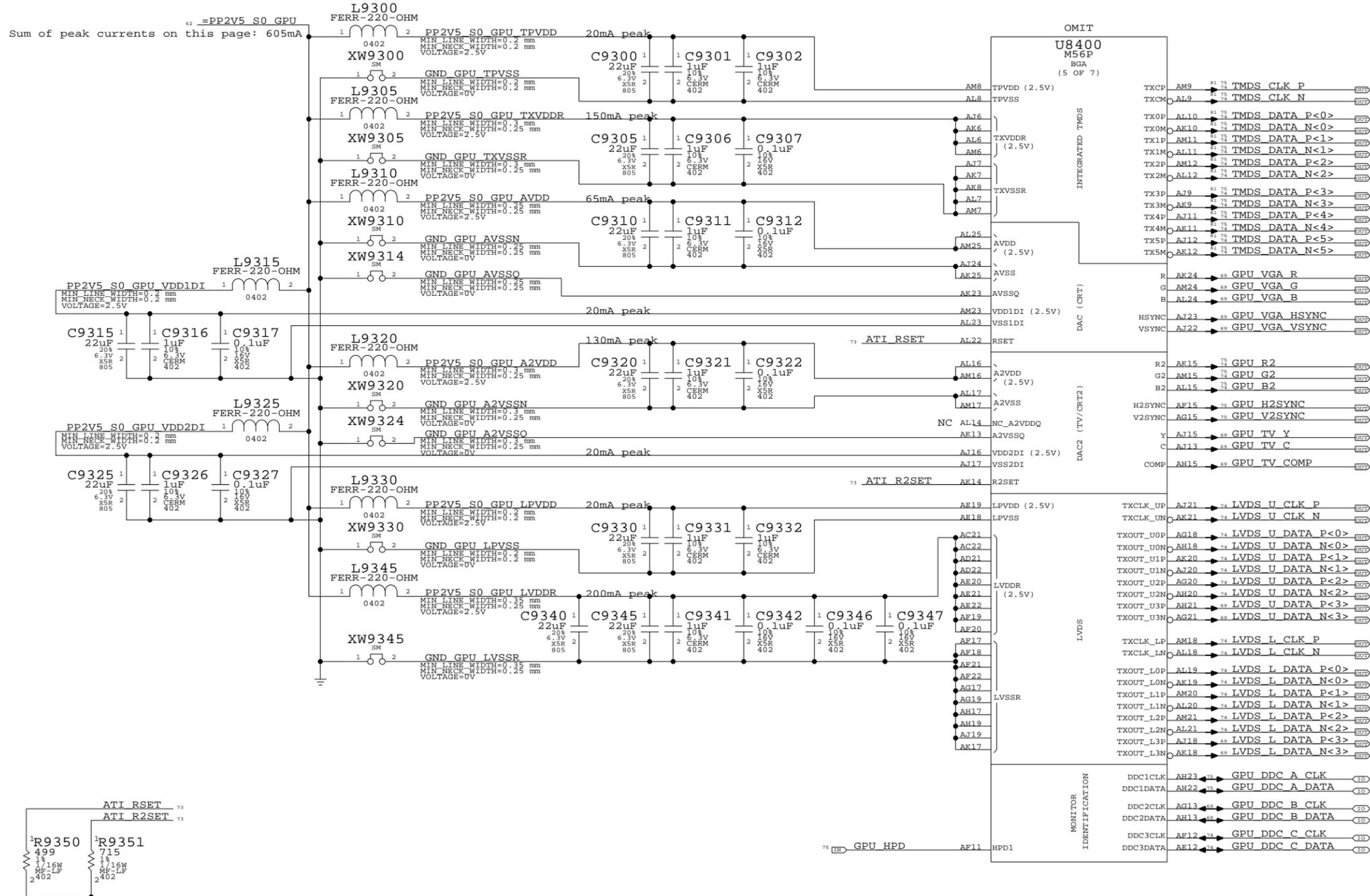
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT	OF	
NONE	72	81	

Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

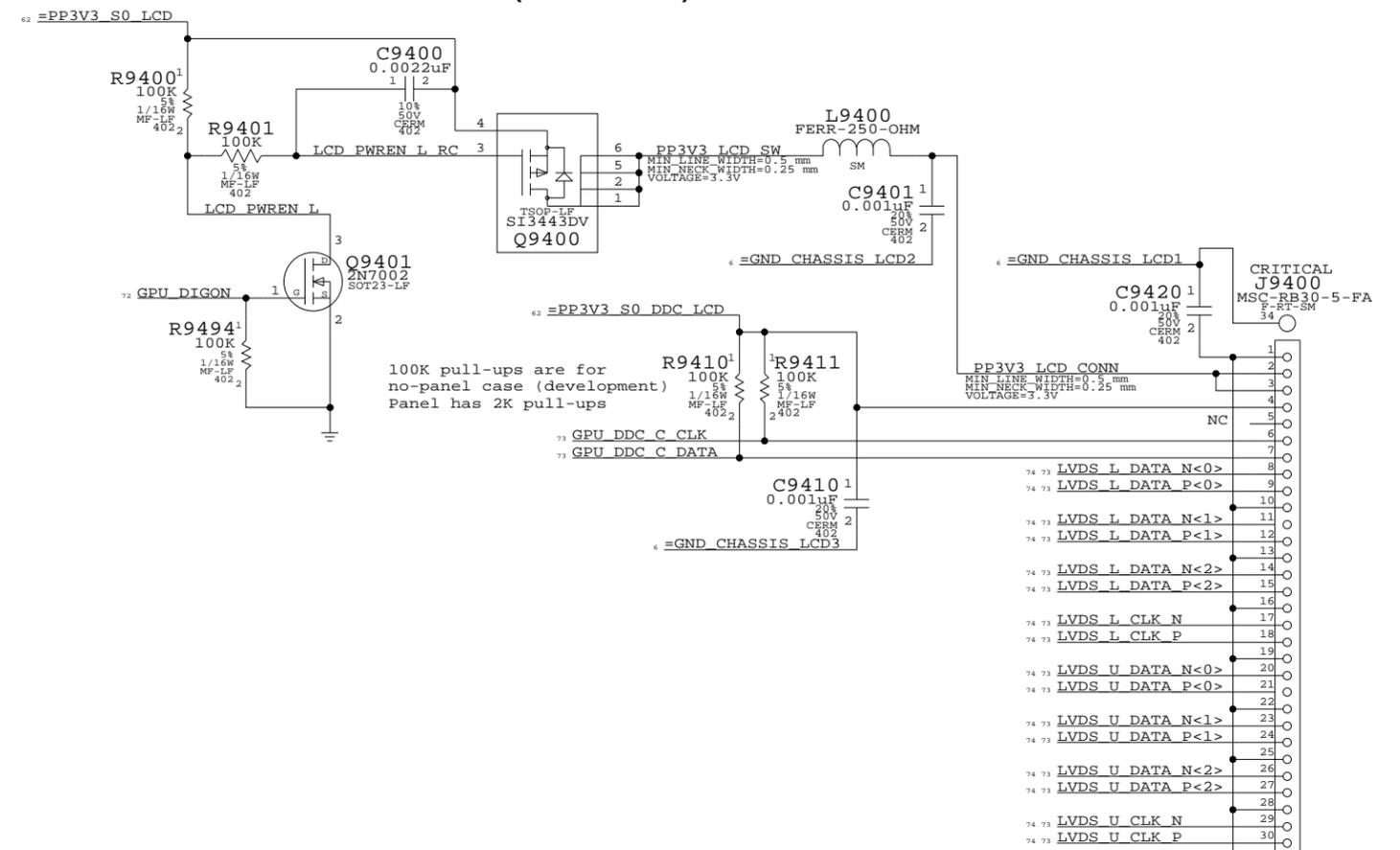
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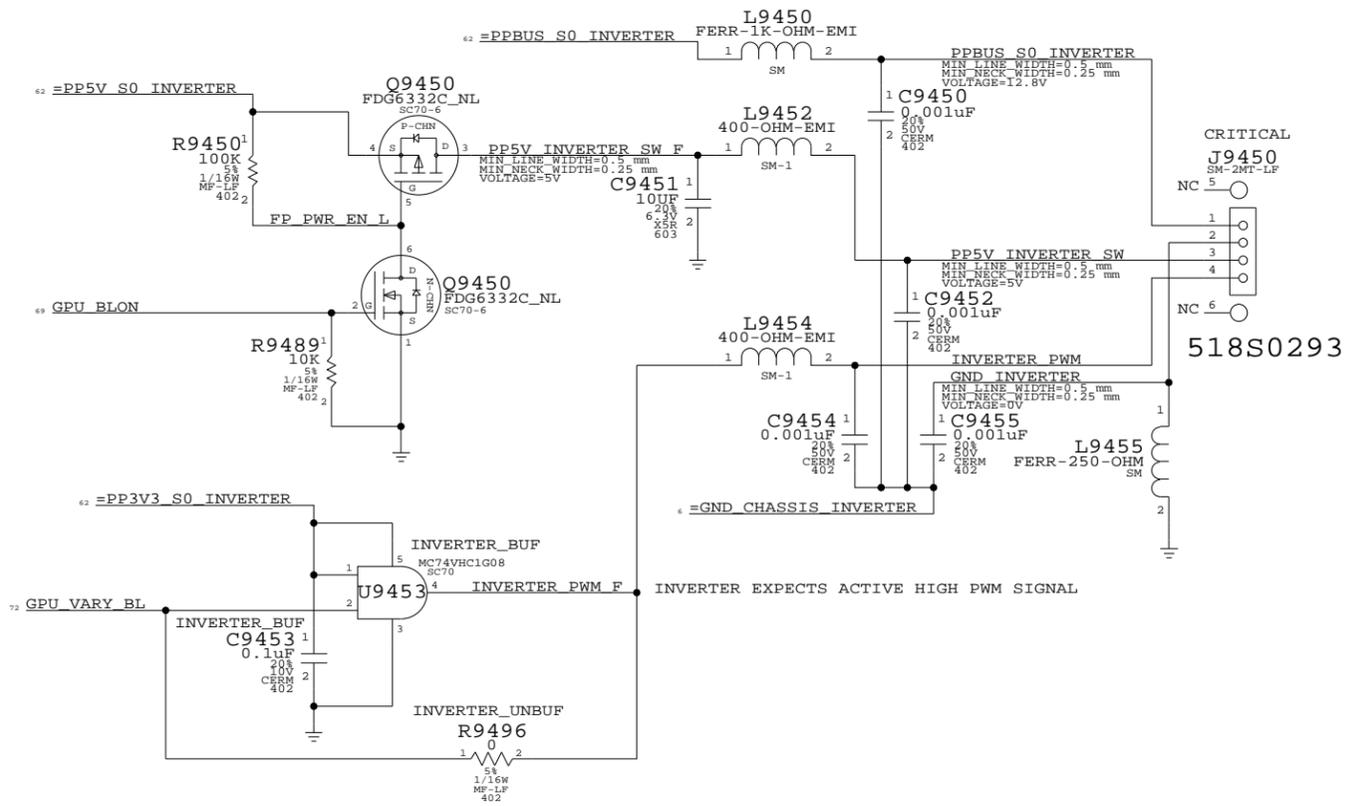
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
SCALE	SHT	OF	
NONE	73	81	

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 74
	LVDS	LVDS	LVDS_U_CLK_N	73 74
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 74
	LVDS	LVDS	LVDS_L_CLK_P	73 74
	LVDS	LVDS	LVDS_L_CLK_N	73 74
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 74
	TMDS	TMDS	TMDS_CLK_P	73 75 81
	TMDS	TMDS	TMDS_CLK_N	73 75 81
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 81
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 81
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 81
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 81



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	74	81	

Secure Signal List

Nets must be buried with no exposed vias between parts listed in SECURE_NET property. No test points allowed between the secure devices, test points are allowed past the secure devices except on nets marked as NO_TEST=TRUE, no test points are allowed on those nets.

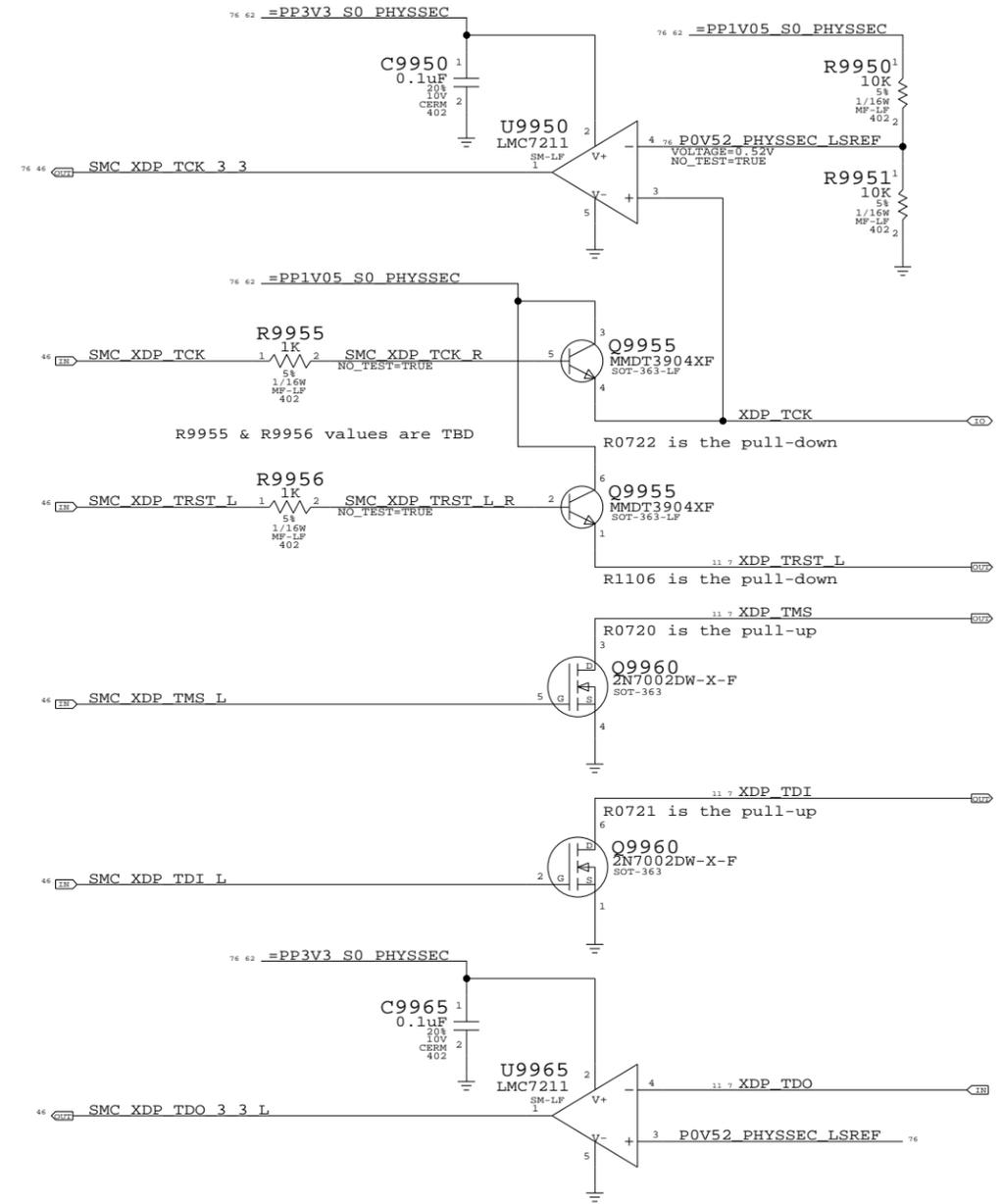
SECURE_NET=U2100:U5800	SPI CE L	22 46 51
SECURE_NET=U2100:U5800	SPI SO	22 46 51
SECURE_NET=U2100:U5800	SPI SI	22 46 51
SECURE_NET=U2100:U5800	SPI ARB	22 46
SECURE_NET=U5800:U7530	BOOT LPC SPI L	5 22 46 48
SECURE_NET=U5800:U7530	IMVP VR ON	46 56
SECURE_NET=U0700:U9950:Q9955	XDP TCK	7 11 76
SECURE_NET=U9950:U5800	SMC XDP TCK 3 3	46 76
SECURE_NET=U5800:R9955	SMC XDP TCK L	
SECURE_NET=U9955:Q9955	SMC XDP TCK L R	

NEED TO TURN PCI_GNT3_L INTO A NC NET!

SMC <-> CPU JTAG Level-Shifting

ALL OF THESE PARTS WILL BE COVERED IN EPOXY

Place these parts on one side and as close together as possible, and keep enough room from other parts to leave room for epoxy covering. Nets that are local to this circuit do not need test points as they will not be accessible.



Physical Security

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	NONE	SHT	OF
		76	81

	8	7	6	5	4	3	2	1
	<p>Date - Radar # - Description</p> <p><u>DMS Release #03000 (RFA #394758)</u></p> <p>2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part. 2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.</p> <p><u>Changes from Proto Branch (DMS Release #04000):</u></p> <p>2005/08/27 - 4230219 - Changed Y3301 to non-obsolete part. 2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply. 2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs. 2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.</p> <p>2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only. 2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only. 2005/08/27 - 4225433 - Changed PBUS voltage sense circuit. 2005/08/28 - 4217535 - Added Left ALS FFC connector. 2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2. 2005/08/28 - 4235203 - Changed BOM settings to stuff R2251. 2005/08/28 - 4217524 - Added LEFT ALS connector (J6430). 2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts. 2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#). 2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5. 2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit. 2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3. 2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin. 2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B. 2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194. 2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on. 2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach. 2005/08/28 - 4227323 - Repinned Top-Case Flex connector.</p> <p><u>DMS Checkin #04001</u></p> <p>2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part. 2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs. 2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K. 2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5. 2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD. 2005/08/29 - 4227336 - Changed Y5920 to 197S0169. 2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21). 2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22). 2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23). 2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states. 2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58). 2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.</p> <p><u>DMS Checkin #04002</u></p> <p>2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit. 2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector. 2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint. 2005/08/31 - 4227328 - Added ESD protection diode on right USB port. 2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds. 2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K. 2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.</p> <p><u>DMS Checkin #04003</u></p> <p>2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex. 2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500. 2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets. 2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps. 2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO. 2005/08/31 - 4240486 - Power line width & neck reductions at PCB request. 2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.</p> <p><u>DMS Checkin #04004</u></p> <p>2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.</p> <p><u>DMS Checkin #04005</u></p> <p>2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB. 2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values. 2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU. 2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.</p> <p><u>DMS Checkin #04006</u></p> <p>2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page. 2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot. 2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence. 2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K. 2005/09/03 - 4232534 - Added notes for power supplies and connectors.</p> <p><u>DMS Checkin #04007</u></p> <p>2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC. 2005/09/06 - 4246683 - Removed NO_STUFF option from R8805 per ATI request. 2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.</p> <p><u>DMS Release #05000-07000 (Proto 2 releases)</u></p> <p>2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests. 2005/09/08 - 4248911 - Sync with M38 & M42 2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package. 2005/09/08 - 4229560 - First implementation of Physical Security Guidelines. 2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS. 2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security. 2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library). 2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library). 2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch. 2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.</p>							
D								D
C								C
B								B
A								A
	8	7	6	5	4	3	2	1

Revision History		
SYNC_MASTER=N/A	SYNC_DATE=N/A	
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	SCALE NONE	SHT 77	OF 81

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR	*	=3:1_SPACING	FSB_DATA	*	=3:1_SPACING
FSB_ADDR2ADDR	*	=2:1_SPACING	FSB_DATA2DATA	*	=2:1_SPACING
FSB_ADSTB	*	=3:1_SPACING	FSB_DSTB	*	=3:1_SPACING
FSB_ADDR2ADSTB	*	=3:1_SPACING	FSB_DATA2DSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_COMMON	*	=2:1_SPACING

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CPU_2T01	*	=2:1_SPACING
CPU_COMP	*	25 MIL
CPU_GTLREF	*	25 MIL
CPU_ITP	*	=2:1_SPACING
CPU_VCCSENSE	*	25 MIL

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_CLK2MEM	*	=4:1_SPACING
MEM_CTRL2CTRL	*	=2:1_SPACING
MEM_CTRL2MEM	*	=3:1_SPACING
MEM_CMD2CMD	*	=1.5:1_SPACING
MEM_CMD2MEM	*	=3:1_SPACING
MEM_DATA2DATA	*	=1.5:1_SPACING
MEM_DATA2MEM	*	=3:1_SPACING
MEM_DQS2MEM	*	=3:1_SPACING
MEM_2OTHER	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCIE	*	20 MIL
DMI	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
IDE	*	=1.8:1_SPACING
SATA	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
AUDIO	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
USB2	*	=4:1_SPACING
USB2_2CLK	*	25 MIL

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
SMB	*	=3:1_SPACING
SPI	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	*	25 MIL
CLK_PCIE	*	20 MIL
CLK_MED	*	20 MIL
CLK_SLOW	*	10 MIL

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-6941	07001
SCALE	SHT	OF	
NONE	78		81

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FB_ADCTRL	*	=2.5:1_SPACING
FB_CLK	*	=2.5:1_SPACING
FB_DATA	*	=2.5:1_SPACING

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedance.
DQ/DQM/DQS lines are 40-ohm single-ended impedance.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS	*	=3:1_SPACING
TMDS	*	=3:1_SPACING
VGA	*	15 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS_PAIR2PAIR	*	25 MIL
TMDS_PAIR2PAIR	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedance.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedance as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
ENET	*	=3:1_SPACING
FW	*	=3:1_SPACING

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCI	*	=2:1_SPACING

More System Constraints

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SCALE	SHT	OF	
NONE	79	81	

M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.076 MM	0.076 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
DEFAULT	*	0.1 MM
STANDARD	*	=DEFAULT
BGA_P1MM	*	=DEFAULT
BGA_P2MM	*	=DEFAULT
BGA_P3MM	*	=DEFAULT

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	*	0.15 MM
1.8:1_SPACING	*	0.18 MM
2:1_SPACING	*	0.2 MM
2.5:1_SPACING	*	0.25 MM
3:1_SPACING	*	0.3 MM
4:1_SPACING	*	0.4 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	ISL2, ISL11	0.1 MM
1.8:1_SPACING	ISL2, ISL11	0.1 MM
2:1_SPACING	ISL2, ISL11	0.1 MM
2.5:1_SPACING	ISL2, ISL11	0.1 MM
3:1_SPACING	ISL2, ISL11	0.1 MM
4:1_SPACING	ISL2, ISL11	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	ISL2, ISL11	0.1 MM
CLK_PCIE	ISL2, ISL11	0.1 MM
CLK_MED	ISL2, ISL11	0.1 MM
CLK_SLOW	ISL2, ISL11	0.1 MM
CPU_COMP	ISL2, ISL11	0.1 MM
CPU_GTLREF	ISL2, ISL11	0.1 MM
CPU_VCCSENSE	ISL2, ISL11	0.1 MM
DMI	ISL2, ISL11	0.1 MM
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM
MEM_2OTHER	ISL2, ISL11	0.1 MM
PCIE	ISL2, ISL11	0.1 MM
SATA	ISL2, ISL11	0.1 MM
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM
VGA	ISL2, ISL11	0.1 MM

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADDR	* OVERRIDE	=STANDARD OVERRIDE
FSB_ADSTB	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADSTB	* OVERRIDE	=2:1_SPACING OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DATA	* OVERRIDE	=STANDARD OVERRIDE
FSB_DSTB	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DSTB	* OVERRIDE	=2:1_SPACING OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_2OTHER	* OVERRIDE	0.5 MM OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI
PCI_55S

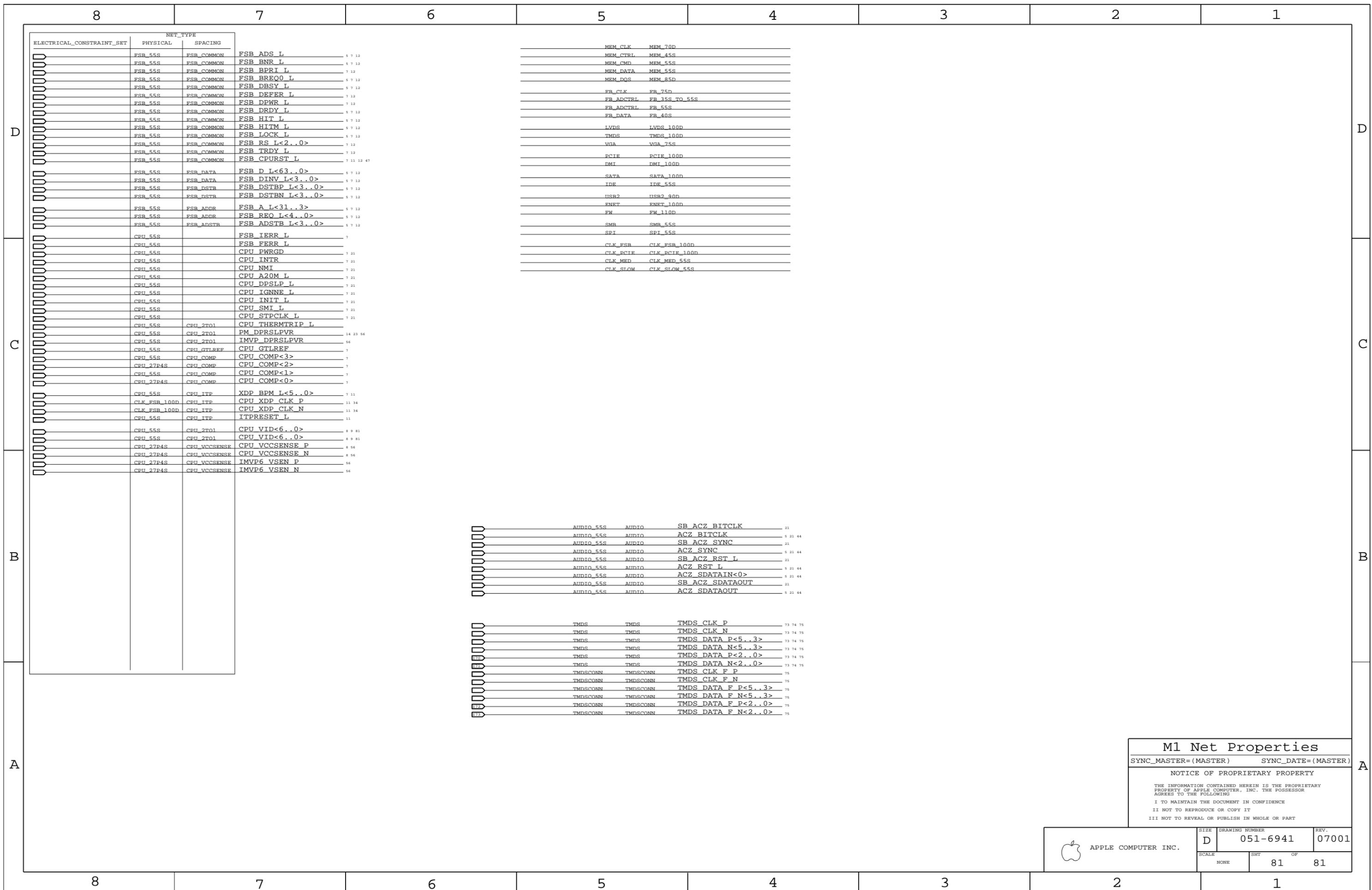
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints

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NONE	80		81



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
FSB_55S	FSB_COMMON	FSB ADS L
FSB_55S	FSB_COMMON	FSB BNR L
FSB_55S	FSB_COMMON	FSB BPRI L
FSB_55S	FSB_COMMON	FSB BREQ0 L
FSB_55S	FSB_COMMON	FSB DBSY L
FSB_55S	FSB_COMMON	FSB DEFER L
FSB_55S	FSB_COMMON	FSB DPWR L
FSB_55S	FSB_COMMON	FSB DRDY L
FSB_55S	FSB_COMMON	FSB HIT L
FSB_55S	FSB_COMMON	FSB HITM L
FSB_55S	FSB_COMMON	FSB LOCK L
FSB_55S	FSB_COMMON	FSB RS L<2..0>
FSB_55S	FSB_COMMON	FSB TRDY L
FSB_55S	FSB_COMMON	FSB CPURST L
FSB_55S	FSB_DATA	FSB D L<63..0>
FSB_55S	FSB_DATA	FSB DINV L<3..0>
FSB_55S	FSB_DSTR	FSB DSTBP L<3..0>
FSB_55S	FSB_DSTR	FSB DSTBN L<3..0>
FSB_55S	FSB_ADDR	FSB A L<31..3>
FSB_55S	FSB_ADDR	FSB REQ L<4..0>
FSB_55S	FSB_ADSTR	FSB ADSTB L<3..0>
CPU_55S		FSB IERR L
CPU_55S		FSB FERR L
CPU_55S		CPU PWRGD
CPU_55S		CPU INTR
CPU_55S		CPU NMI
CPU_55S		CPU A20M L
CPU_55S		CPU DPSLP L
CPU_55S		CPU IGNE L
CPU_55S		CPU INIT L
CPU_55S		CPU SMI L
CPU_55S		CPU STPCLK L
CPU_55S	CPU_2T01	CPU THERMTRIP L
CPU_55S	CPU_2T01	PM DPRSLPVR
CPU_55S	CPU_2T01	IMVP DPRSLPVR
CPU_55S	CPU_GTLREF	CPU GTLREF
CPU_55S	CPU_COMP	CPU COMP<3>
CPU_27P4S	CPU_COMP	CPU COMP<2>
CPU_55S	CPU_COMP	CPU COMP<1>
CPU_27P4S	CPU_COMP	CPU COMP<0>
CPU_55S	CPU_ITP	XDP BPM L<5..0>
CLK_FSB_100D	CPU_ITP	CPU XDP CLK P
CLK_FSB_100D	CPU_ITP	CPU XDP CLK N
CPU_55S	CPU_ITP	ITPRESET L
CPU_55S	CPU_2T01	CPU VID<6..0>
CPU_55S	CPU_2T01	CPU VID<6..0>
CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P
CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N
CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P
CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N

MEM_CLK	MEM_70D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIe	PCIe_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

AUDIO_55S	AUDIO	SB ACZ BITCLK	21
AUDIO_55S	AUDIO	ACZ BITCLK	5 21 44
AUDIO_55S	AUDIO	SB ACZ SYNC	21
AUDIO_55S	AUDIO	ACZ SYNC	5 21 44
AUDIO_55S	AUDIO	SB ACZ_RST L	21
AUDIO_55S	AUDIO	ACZ_RST L	5 21 44
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
AUDIO_55S	AUDIO	SB ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44
TMDS	TMDS	TMDS_CLK_P	73 74 75
TMDS	TMDS	TMDS_CLK_N	73 74 75
TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties
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	D	051-6941	07001
SCALE	NONE	SHT	OF
		81	81