

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M9 MLB

4/12/2006

PVT

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

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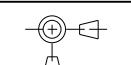
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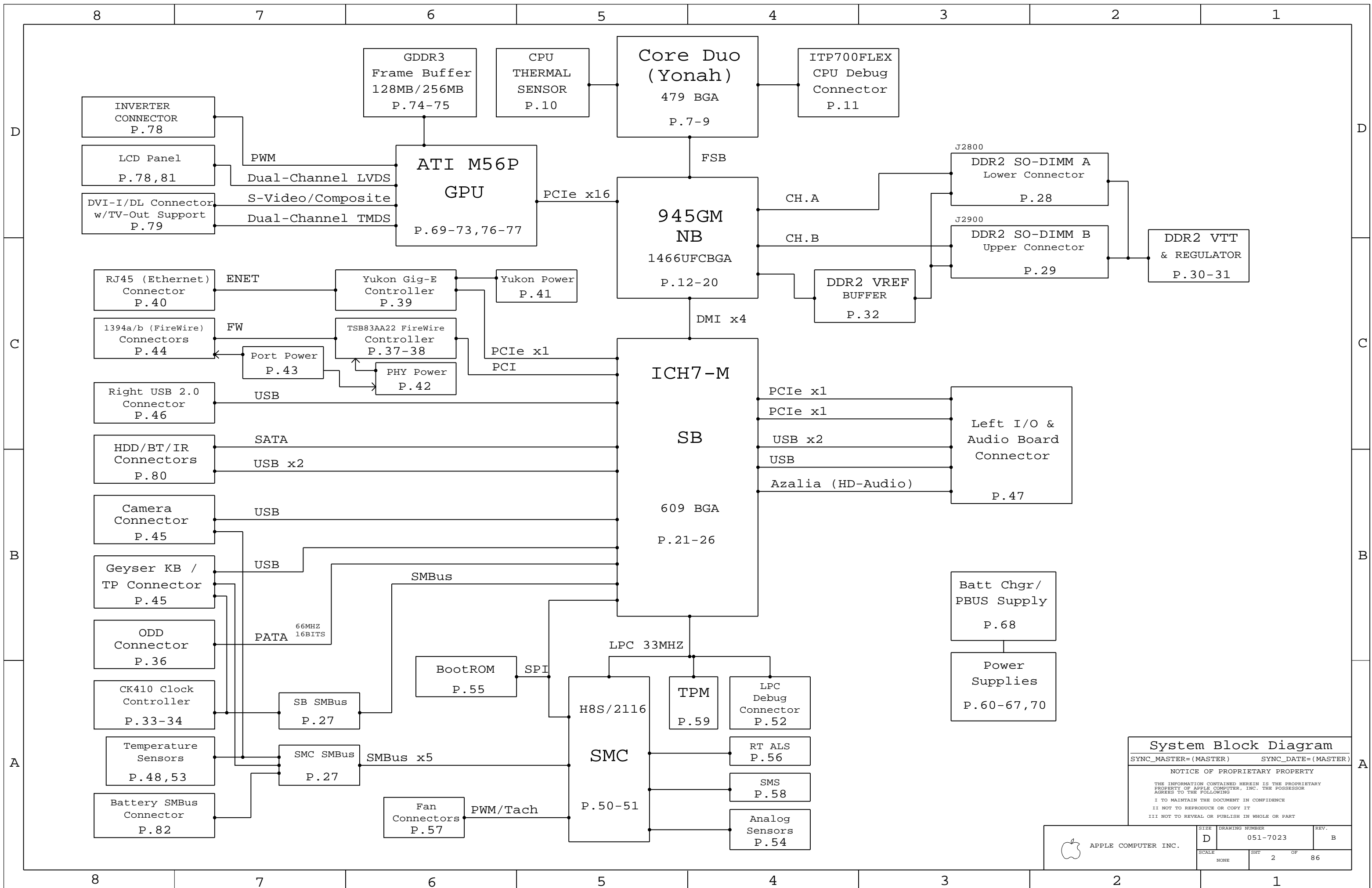
ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7023	1	SCHEM, MLB, M9	SCH	CRITICAL	
820-2023	1	PCBF, MLB, M9	PCB	CRITICAL	

DRAWING
TITLE=SULLY
ABBREV=DRAWING
LAST_MODIFIED=Wed Apr 12 12:10:18 2006

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7023	REV. B
				SHT	1 OF 86

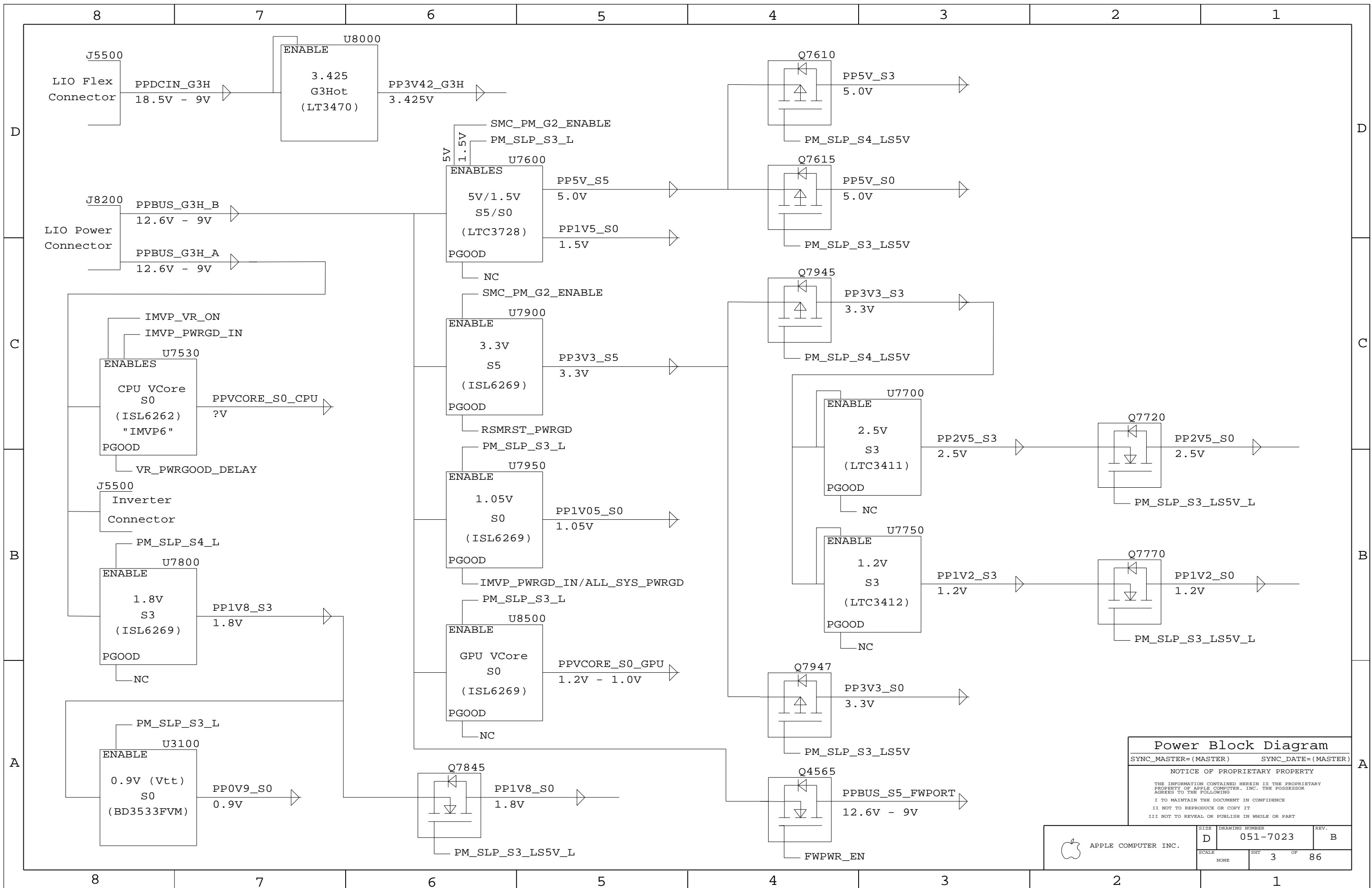


System Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT 2 OF 86		
NONE			



Power Block Diagram
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Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA
TRUE	IMVP6_RBIAS
TRUE	P5VS5_RUNSS
TRUE	P1V5S0_RUNSS
TRUE	P2V5S3_MODE
TRUE	P2V5S3_SHDNRT
TRUE	P1V2S3_RT
TRUE	P1V2S3_RUNSS
TRUE	P1V8S3_COMP
TRUE	P1V8S3_FSET
TRUE	P3V3S5_COMP
TRUE	P3V3S5_FSET
TRUE	P1V0S0_COMP
TRUE	P1V0S0_FSET
TRUE	P3V42G3H_FB
TRUE	GPUVCORE_COMP
TRUE	GPUVCORE_FSET
TRUE	GPUBBP_ADJ

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA
TRUE	FSB_A_L<31..3>
TRUE	FSB_ADS_L
TRUE	FSB_ADSTB_L<1..0>
TRUE	FSB_BNR_L
TRUE	FSB_BREQ0_L
TRUE	FSB_D_L<63..0>
TRUE	FSB_DBSY_L
TRUE	FSB_DINV_L<3..0>
TRUE	FSB_DRDY_L
TRUE	FSB_DSTBN_L<3..0>
TRUE	FSB_DSTBP_L<3..0>
TRUE	FSB_HIT_L
TRUE	FSB_HITM_L
TRUE	FSB_LOCK_L
TRUE	FSB_REQ_L<4..0>

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA	
TRUE	DMI_N2S_P<1..0>
TRUE	DMI_N2S_N<1..0>
TRUE	SB_CLK100M_SATA_P
TRUE	SB_CLK100M_SATA_N

Power Nets

FUNC_TEST	TP
TRUE	PP0V9_S0
TRUE	PP1V05_S0
TRUE	PP1V2_S0
TRUE	PP1V2_S3
TRUE	PP1V5_S0
TRUE	PP1V8_S0
TRUE	PP1V8_S3
TRUE	PP2V5_S0
TRUE	PP2V5_S3
TRUE	PP3V3_S0
TRUE	PP3V3_S3
TRUE	PP3V3_S5
TRUE	PP5V_S0
TRUE	PP5V_S5
TRUE	PPBUS_G3H
TRUE	GND

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST	TP
TRUE	IMVP_VR_ON
TRUE	IMVP_DPRSLEVR
TRUE	PM_SLP_S3_L
TRUE	PM_SLP_S3BATT
TRUE	PM_SLP_S4_L
TRUE	PM_SLP_S5_L
TRUE	P1V5P1V05S0_PGOOD
TRUE	CPU_DPRSTP_L
TRUE	IMVP6_VID<6..0>
TRUE	FSB_CLK_CPU_N
TRUE	FSB_CLK_CPU_P
TRUE	PLT_RST_L
TRUE	PLT_RST_L
TRUE	PEG_RESET_L
TRUE	SMC_LRESET_L
TRUE	TPM_LRESET_L
TRUE	CPU_STPCLK_L
TRUE	FSB_CLK_NB_P
TRUE	FSB_CLK_NB_N
TRUE	CLK_NB_OE_L
TRUE	NB_CLK100M_GCLKIN_P
TRUE	NB_CLK100M_GCLKIN_N
TRUE	GND
TRUE	GND
TRUE	GND
TRUE	CPU_THERMTRIP_R
TRUE	TP_SB_SUS_CLK

MAC-1 TPs

FUNC_TEST	TP
TRUE	CPU_PWRGD
TRUE	TP_CPU_CPUSLP_L
TRUE	PM_DPRSLEVR
TRUE	CPU_DPSLP_L
TRUE	PM_LAN_ENABLE
TRUE	PCI_RST_L
TRUE	PM_RSMRST_L
TRUE	PM_SB_PWROK
TRUE	SB_RTC_RST_L
TRUE	PM_STPCPU_L
TRUE	PM_STPPCI_L
TRUE	VR_PWRGD_CK410
TRUE	VR_PWRGD_GOOD_DELAY
TRUE	FSB_CPURST_L
TRUE	FSB_SLP_CPU_L
TRUE	FSB_DPWR_L
TRUE	NB_SB_SYNC_L
TRUE	PP2V5_S0_GPU_TPVD
TRUE	PP2V5_S0_GPU_TXVDDR
TRUE	PP2V5_S0_GPU_AVDD
TRUE	PP2V5_S0_GPU_A2VDD
TRUE	PP2V5_S0_GPU_LPVD
TRUE	PP2V5_S0_GPU_LVDDR
TRUE	PP3V3_S0
TRUE	PP3V3_S0_CK410_VDD48
TRUE	PP3V3_S0_CK410_VDD_PCI
TRUE	PP3V3_S0_CK410_VDD_REF
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC
TRUE	PP3V3_S0_CK410_VDDA
TRUE	PP3V3_FWPHY
TRUE	PP3V3_FWPHY_AVDD
TRUE	PP3V3_FWPHY_PLLVDD
TRUE	PP1V95_FWPHY
TRUE	PP1V95_FWPHY_PLLVDD
TRUE	PP1V2_S3
TRUE	PP3V3_S3AC
TRUE	PP2V5_S3
TRUE	PP2V5_S3_ENET_AVDD

Fan Connectors

FUNC_TEST	TP
TRUE	PP5V_S0
TRUE	FAN_LT_PWM
TRUE	FAN_LT_TACH
TRUE	FAN_RT_PWM
TRUE	FAN_RT_TACH

LPC+ Debug Connector

FUNC_TEST	TP
TRUE	PP3V42_G3H
TRUE	PP5V_S0
TRUE	LPC_AD<0>
TRUE	LPC_AD<1>
TRUE	LPC_FRAME_L
TRUE	PM_CLKRUN_L
TRUE	BOOT_LPC_SPI_L
TRUE	SMC_TMS
TRUE	DEBUG_RST_L
TRUE	SMC_TRST_L
TRUE	SMC_TDO
TRUE	SMC_MDI
TRUE	SMC_TX_L
TRUE	FWH_INIT_L
TRUE	PCI_CLK_PORT80_LPC
TRUE	LPC_AD<2>
TRUE	LPC_AD<3>
TRUE	INT_SERIRO
TRUE	PM_SUS_STAT_L
TRUE	SMC_SDI
TRUE	SMC_TCK
TRUE	SMC_RST_L
TRUE	SMC_NMI
TRUE	SMC_RX_L
TRUE	SV_SET_UP

Resistor Calibration

FUNC_TEST	TP
TRUE	PP5V_S0
TRUE	PP1V8_S3
TRUE	PP1V05_S0
TRUE	PPVCORE_S0_CPU
TRUE	PPVCORE_S0_GPU
TRUE	ISENSE_CAL_EN
TRUE	GND

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST	TP
TRUE	PP5V_S3
TRUE	USB2_CAMERA_N
TRUE	USB2_CAMERA_P
TRUE	SMBUS_SMC_0_S0_SDA
TRUE	SMBUS_SMC_0_S0_SCL

Thermal Sensors

FUNC_TEST	TP
TRUE	HSTHMSNS_DX_P
TRUE	HSTHMSNS_DX_N
TRUE	RSFSTHMSNS_D_P
TRUE	RSFSTHMSNS_D_N

SMC TPs

FUNC_TEST	TP
TRUE	PM_SYSRST_L
TRUE	SMC_ONOFF_L

Battery Connector

FUNC_TEST	TP
TRUE	BATT_POS
TRUE	BATT_NEG
TRUE	SMC_BS_ALERT_L
TRUE	SMBUS_SMC_BSA_SCL
TRUE	SMBUS_SMC_BSA_SDA

Left I/O Data Connector

FUNC_TEST	TP
TRUE	PP1V5_S0
TRUE	PPBUS_G3H
TRUE	PP3V42_G3H
TRUE	PP5V_S0_AUDIO
TRUE	GND_AUDIO
TRUE	ALS_GAIN
TRUE	LTALS_OUT
TRUE	ACZ_SDATAIN<0>
TRUE	ACZ_SDATAOUT
TRUE	ACZ_BITCLK
TRUE	ACZ_RST_L
TRUE	EXCARD_OC_L
TRUE	LTUSB_OC_L
TRUE	LT2USB_OC_L
TRUE	PM_SLP_S3_LS5V
TRUE	PM_SLP_S4_L
TRUE	SYS_ONEWIRE
TRUE	MINI_CLKREO_L
TRUE	SMC_EXCARD_CP
TRUE	EXCARD_CLKREO_L
TRUE	SMC_EXCARD_PWR_EN
TRUE	LIO_PLT_RESET_L
TRUE	ACZ_SYNC
TRUE	USB2_LT_N
TRUE	USB2_LT_P
TRUE	USB2_EXCARD_N
TRUE	USB2_EXCARD_P
TRUE	PCIE_EXCARD_R2D_C_N
TRUE	PCIE_EXCARD_R2D_C_P
TRUE	PCIE_EXCARD_D2R_P
TRUE	PCIE_CLK100M_EXCARD_P
TRUE	PCIE_CLK100M_EXCARD_N
TRUE	USB2_LT2_N
TRUE	USB2_LT2_P
TRUE	PCIE_MINI_R2D_C_N
TRUE	PCIE_MINI_R2D_C_P
TRUE	PCIE_MINI_D2R_N
TRUE	PCIE_MINI_D2R_P
TRUE	PCIE_CLK100M_MINI_P
TRUE	PCIE_CLK100M_MINI_N
TRUE	SMBUS_SB_SCL
TRUE	SMBUS_SB_SDA
TRUE	PCIE_WAKE_L
TRUE	SMC_BC_ACOK

Left I/O Power Connector

FUNC_TEST	TP
TRUE	PP18V5_DCIN
TRUE	PP5V_S5
TRUE	PP5V_S0_AUDIO_PWR
TRUE	GND_AUDIO_PWR
TRUE	GND

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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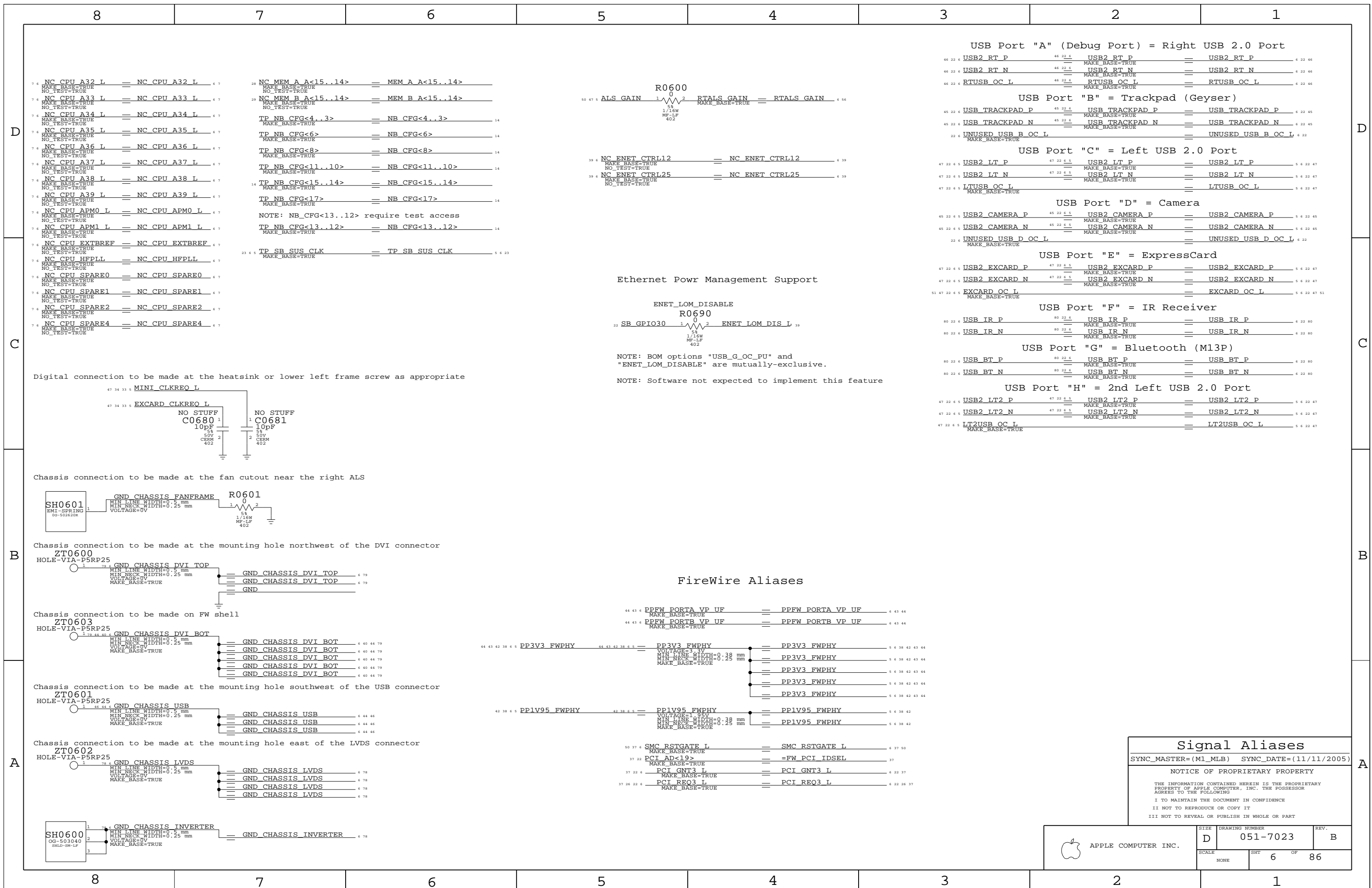
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SCALE	SHT	OF	
NONE	5	86	



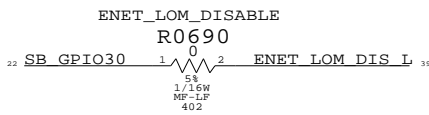
7 4 NC CPU A32 L == NC CPU A32 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A33 L == NC CPU A33 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A34 L == NC CPU A34 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A35 L == NC CPU A35 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A36 L == NC CPU A36 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A37 L == NC CPU A37 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A38 L == NC CPU A38 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU A39 L == NC CPU A39 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU APM0 L == NC CPU APM0 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU APM1 L == NC CPU APM1 L 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU SPARE0 == NC CPU SPARE0 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU SPARE1 == NC CPU SPARE1 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU SPARE2 == NC CPU SPARE2 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 7 4 NC CPU SPARE4 == NC CPU SPARE4 4 7
 MAKE_BASE=TRUE
 NO_TEST=TRUE

28 NC MEM A A<15..14> == MEM A A<15..14>
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 29 NC MEM B A<15..14> == MEM B A<15..14>
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 TP NB CFG<4..3> == NB CFG<4..3> 14
 MAKE_BASE=TRUE
 TP NB CFG<6> == NB CFG<6> 14
 MAKE_BASE=TRUE
 TP NB CFG<8> == NB CFG<8> 14
 MAKE_BASE=TRUE
 TP NB CFG<11..10> == NB CFG<11..10> 14
 MAKE_BASE=TRUE
 TP NB CFG<15..14> == NB CFG<15..14> 14
 MAKE_BASE=TRUE
 TP NB CFG<17> == NB CFG<17> 14
 MAKE_BASE=TRUE
 NOTE: NB_CFG<13..12> require test access
 TP NB CFG<13..12> == NB CFG<13..12> 14
 MAKE_BASE=TRUE
 23 5 TP SB SUS CLK == TP SB SUS CLK 5 4 23
 MAKE_BASE=TRUE



39 6 NC ENET CTRL12 == NC ENET CTRL12 6 39
 MAKE_BASE=TRUE
 NO_TEST=TRUE
 39 6 NC ENET CTRL25 == NC ENET CTRL25 6 39
 MAKE_BASE=TRUE
 NO_TEST=TRUE

Ethernet Powr Management Support



NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.
 NOTE: Software not expected to implement this feature

USB Port "A" (Debug Port) = Right USB 2.0 Port

46 22 6 USB2_RT_P == USB2_RT_P == USB2_RT_P 6 22 46
 MAKE_BASE=TRUE
 46 22 6 USB2_RT_N == USB2_RT_N == USB2_RT_N 6 22 46
 MAKE_BASE=TRUE
 46 22 6 RTUSB_OC_L == RTUSB_OC_L == RTUSB_OC_L 6 22 46
 MAKE_BASE=TRUE

USB Port "B" = Trackpad (Geyser)

45 22 6 USB_TRACKPAD_P == USB_TRACKPAD_P == USB_TRACKPAD_P 6 22 45
 MAKE_BASE=TRUE
 45 22 6 USB_TRACKPAD_N == USB_TRACKPAD_N == USB_TRACKPAD_N 6 22 45
 MAKE_BASE=TRUE
 22 6 UNUSED_USB_B_OC_L == UNUSED_USB_B_OC_L 6 22
 MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

47 22 6 USB2_LT_P == USB2_LT_P == USB2_LT_P 5 6 22 47
 MAKE_BASE=TRUE
 47 22 6 USB2_LT_N == USB2_LT_N == USB2_LT_N 5 6 22 47
 MAKE_BASE=TRUE
 47 22 6 LTUSB_OC_L == LTUSB_OC_L 5 6 22 47
 MAKE_BASE=TRUE

USB Port "D" = Camera

45 22 6 USB2_CAMERA_P == USB2_CAMERA_P == USB2_CAMERA_P 5 6 22 45
 MAKE_BASE=TRUE
 45 22 6 USB2_CAMERA_N == USB2_CAMERA_N == USB2_CAMERA_N 5 6 22 45
 MAKE_BASE=TRUE
 22 6 UNUSED_USB_D_OC_L == UNUSED_USB_D_OC_L 6 22
 MAKE_BASE=TRUE

USB Port "E" = ExpressCard

47 22 6 USB2_EXCARD_P == USB2_EXCARD_P == USB2_EXCARD_P 5 6 22 47
 MAKE_BASE=TRUE
 47 22 6 USB2_EXCARD_N == USB2_EXCARD_N == USB2_EXCARD_N 5 6 22 47
 MAKE_BASE=TRUE
 51 22 6 EXCARD_OC_L == EXCARD_OC_L 5 6 22 47 51
 MAKE_BASE=TRUE

USB Port "F" = IR Receiver

80 22 6 USB_IR_P == USB_IR_P == USB_IR_P 6 22 80
 MAKE_BASE=TRUE
 80 22 6 USB_IR_N == USB_IR_N == USB_IR_N 6 22 80
 MAKE_BASE=TRUE

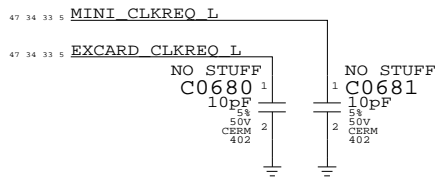
USB Port "G" = Bluetooth (M13P)

80 22 6 USB_BT_P == USB_BT_P == USB_BT_P 6 22 80
 MAKE_BASE=TRUE
 80 22 6 USB_BT_N == USB_BT_N == USB_BT_N 6 22 80
 MAKE_BASE=TRUE

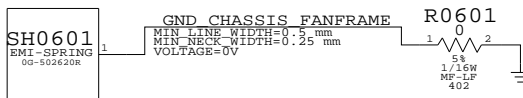
USB Port "H" = 2nd Left USB 2.0 Port

47 22 6 USB2_LT2_P == USB2_LT2_P == USB2_LT2_P 5 6 22 47
 MAKE_BASE=TRUE
 47 22 6 USB2_LT2_N == USB2_LT2_N == USB2_LT2_N 5 6 22 47
 MAKE_BASE=TRUE
 47 22 6 LT2USB_OC_L == LT2USB_OC_L 5 6 22 47
 MAKE_BASE=TRUE

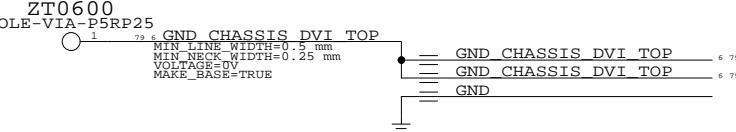
Digital connection to be made at the heatsink or lower left frame screw as appropriate



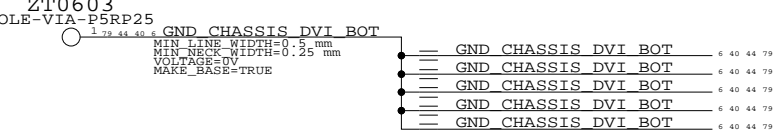
Chassis connection to be made at the fan cutout near the right ALS



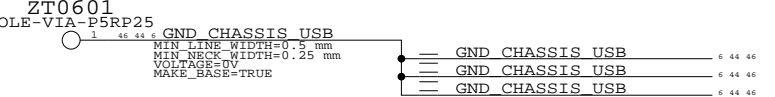
Chassis connection to be made at the mounting hole northwest of the DVI connector



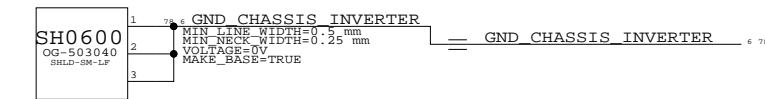
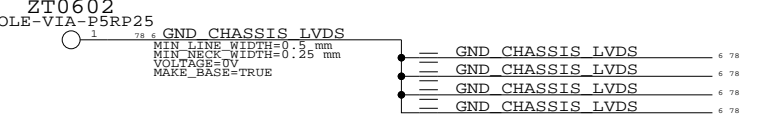
Chassis connection to be made on FW shell



Chassis connection to be made at the mounting hole southwest of the USB connector



Chassis connection to be made at the mounting hole east of the LVDS connector



FireWire Aliases

44 43 6 PPFW_PORTA_VP_UF == PPFW_PORTA_VP_UF 6 43 44
 MAKE_BASE=TRUE
 44 43 6 PPFW_PORTB_VP_UF == PPFW_PORTB_VP_UF 6 43 44
 MAKE_BASE=TRUE

44 43 42 38 6 5 PP3V3_FWPHY == PP3V3_FWPHY 5 6 38 42 43 44
 VOLTAGE=3.3V
 MIN_LINE_WIDTH=0.38 mm
 MIN_NECK_WIDTH=0.25 mm
 MAKE_BASE=TRUE

42 38 6 5 PP1V95_FWPHY == PP1V95_FWPHY 5 6 38 42
 VOLTAGE=1.95V
 MIN_LINE_WIDTH=0.38 mm
 MIN_NECK_WIDTH=0.25 mm
 MAKE_BASE=TRUE

50 37 6 SMC_RSTGATE_L == SMC_RSTGATE_L 6 37 50
 MAKE_BASE=TRUE
 37 22 6 PCI_AD<19> == =FW_PCI_IDSEL 37
 MAKE_BASE=TRUE
 37 22 6 PCI_GNT3_L == PCI_GNT3_L 6 22 37
 MAKE_BASE=TRUE
 37 28 22 6 PCI_REQ3_L == PCI_REQ3_L 6 22 26 37
 MAKE_BASE=TRUE

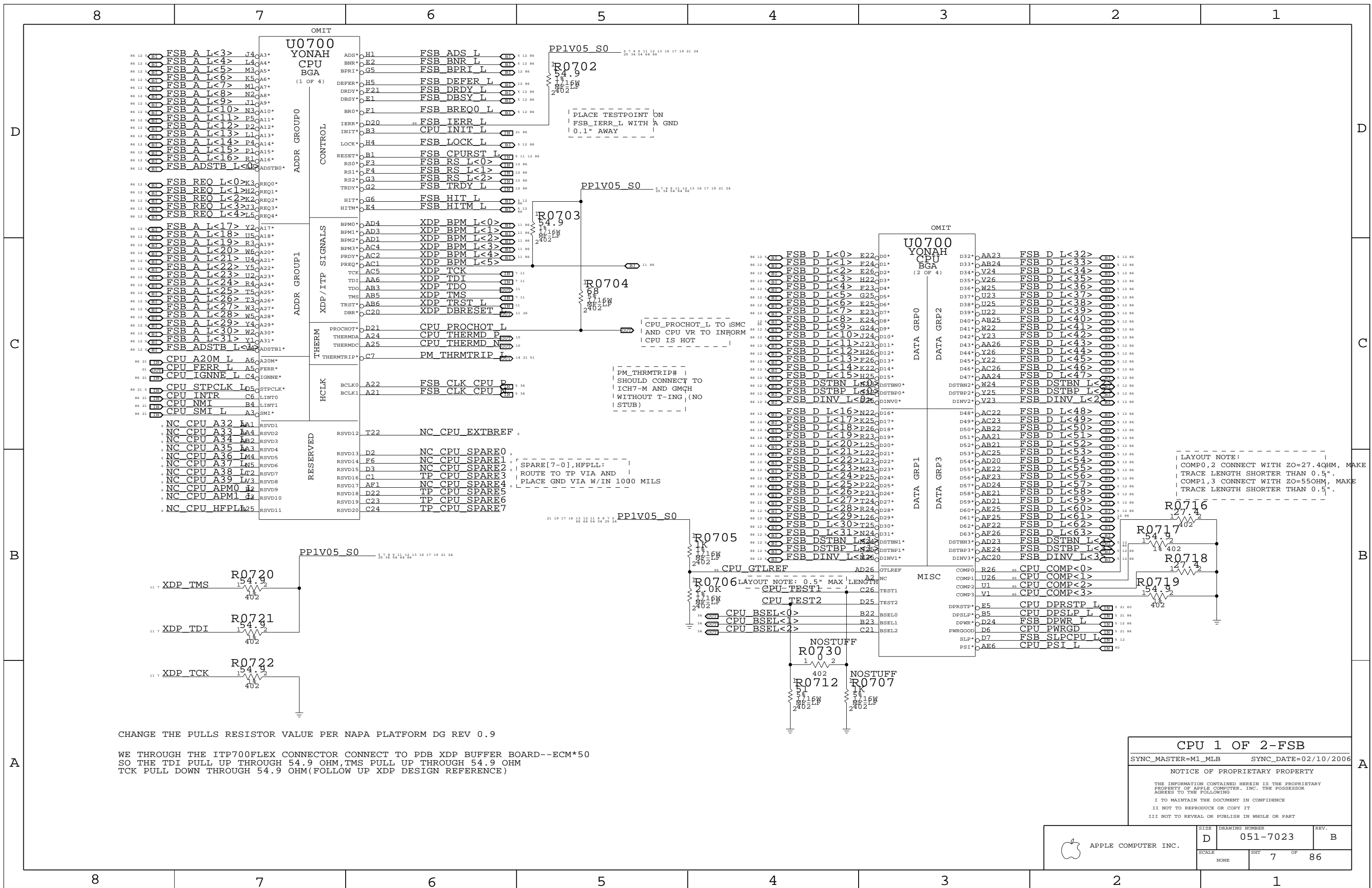
Signal Aliases

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/11/2005)

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NONE	6		



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM#50
 SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM
 TCK PULL DOWN THROUGH 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

LAYOUT NOTE:
 COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE
 TRACE LENGTH SHORTER THAN 0.5".
 COMP1,3 CONNECT WITH ZO=55OHM, MAKE
 TRACE LENGTH SHORTER THAN 0.5".

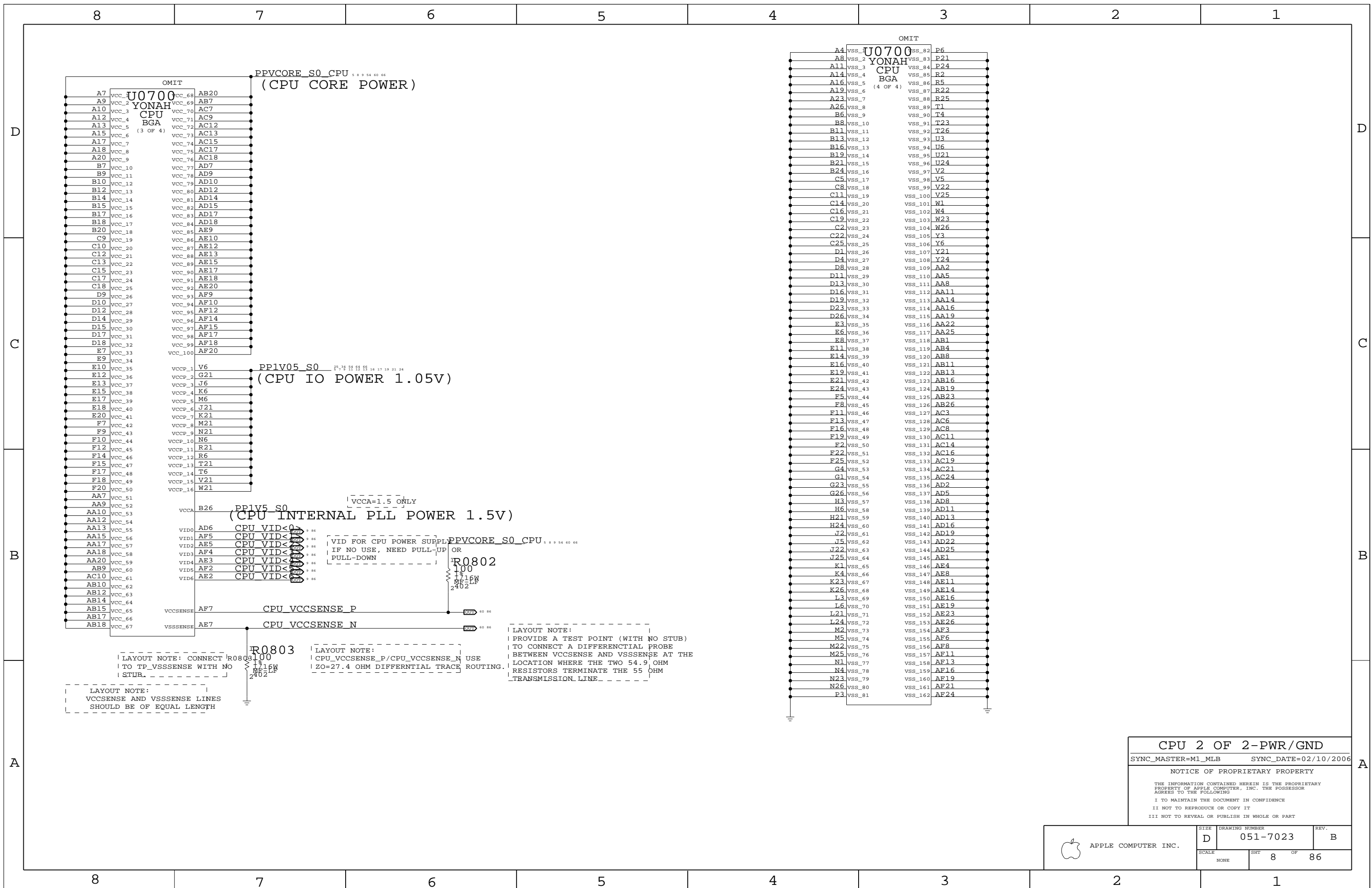
CPU 1 OF 2-FSB
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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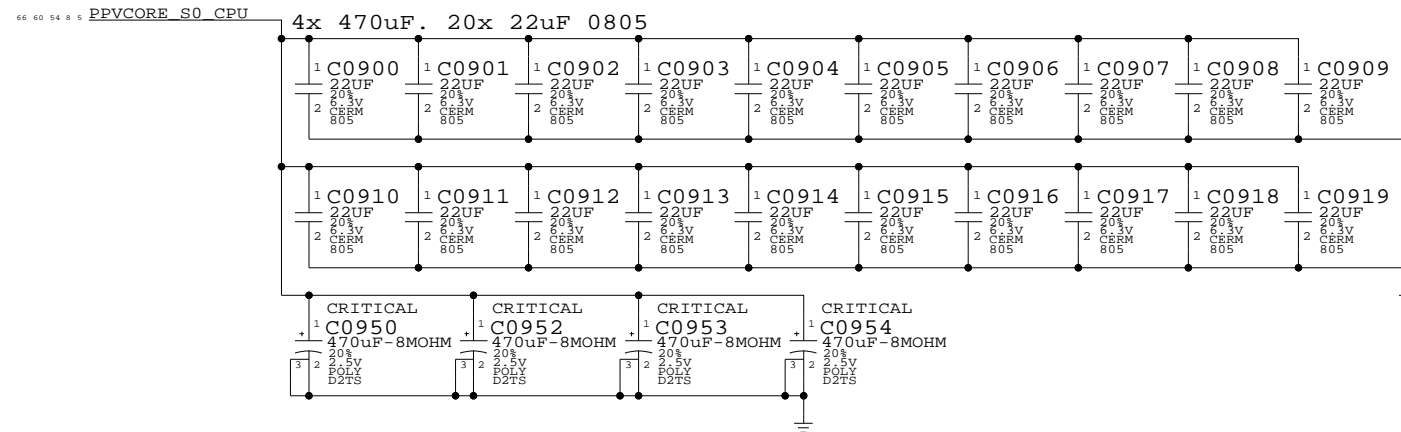


CPU 2 OF 2-PWR/GND
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

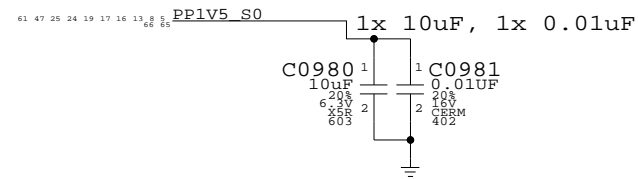
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NONE			

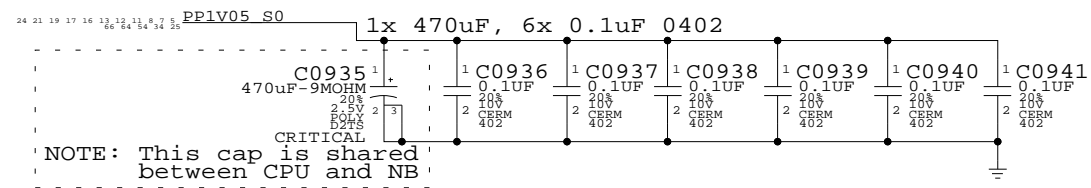
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

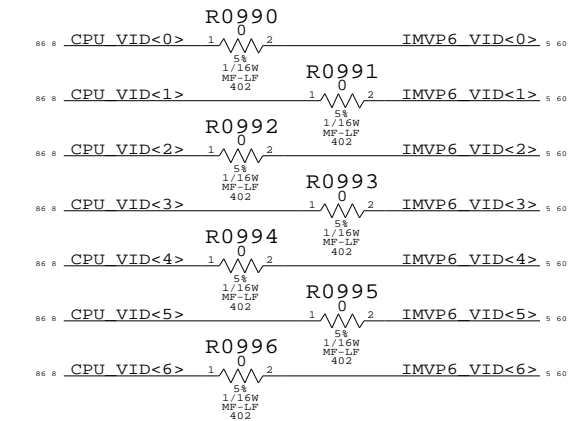


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



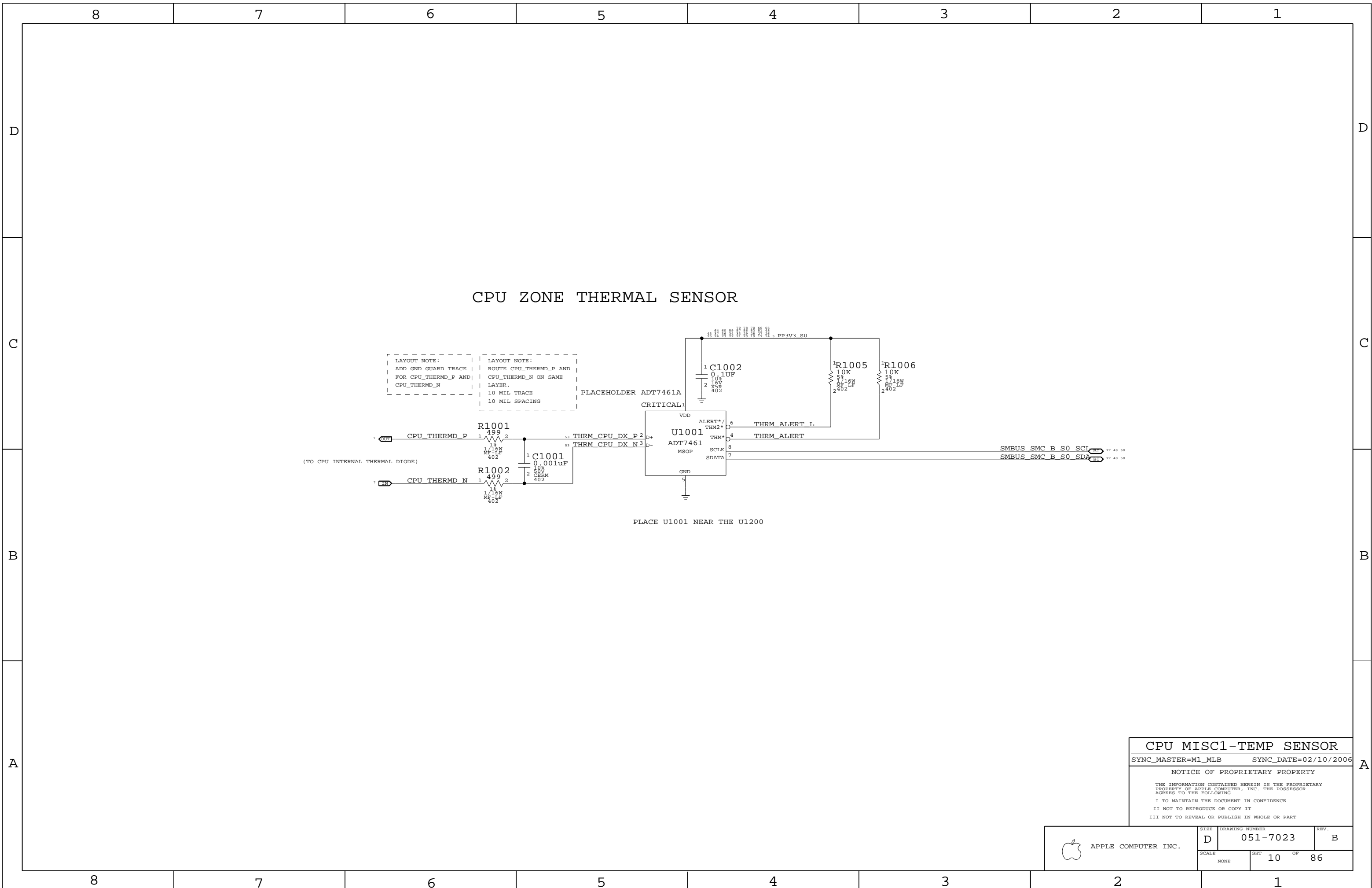
CPU Decoupling & VID

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

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CPU MISC1-TEMP SENSOR

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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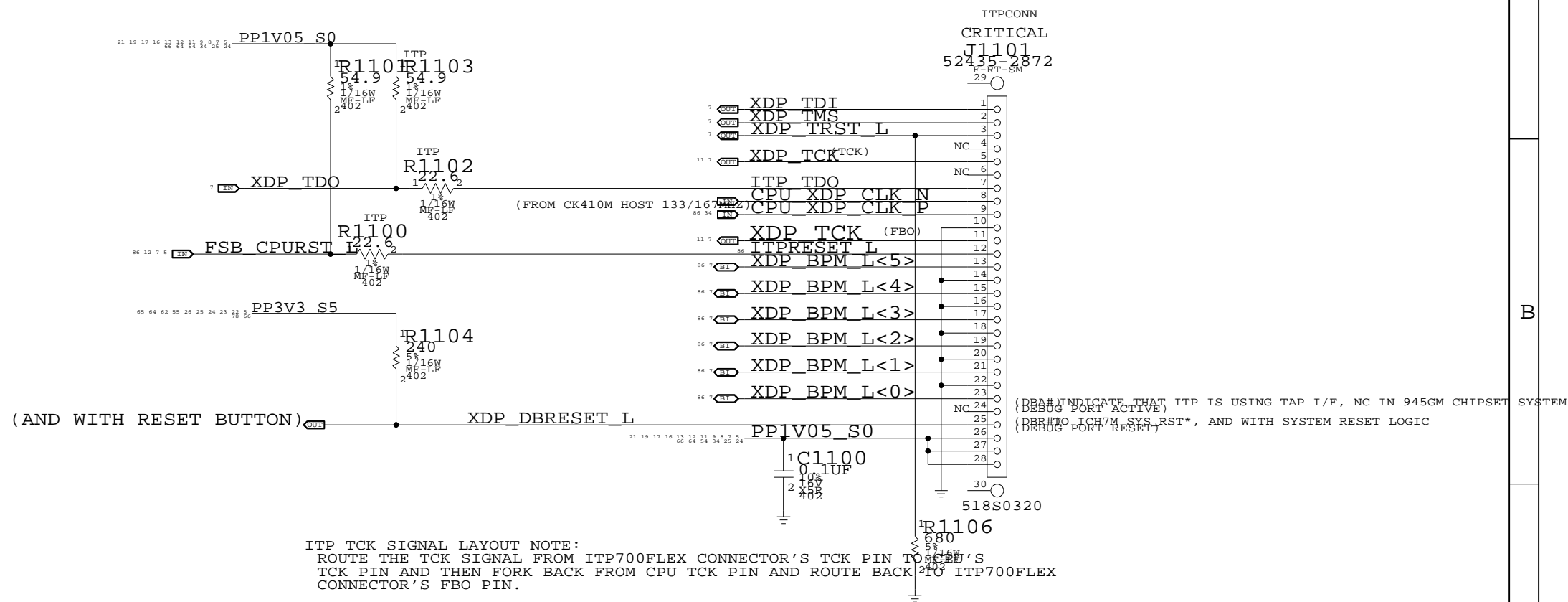
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CPU ITP700FLEX DEBUG SUPPORT

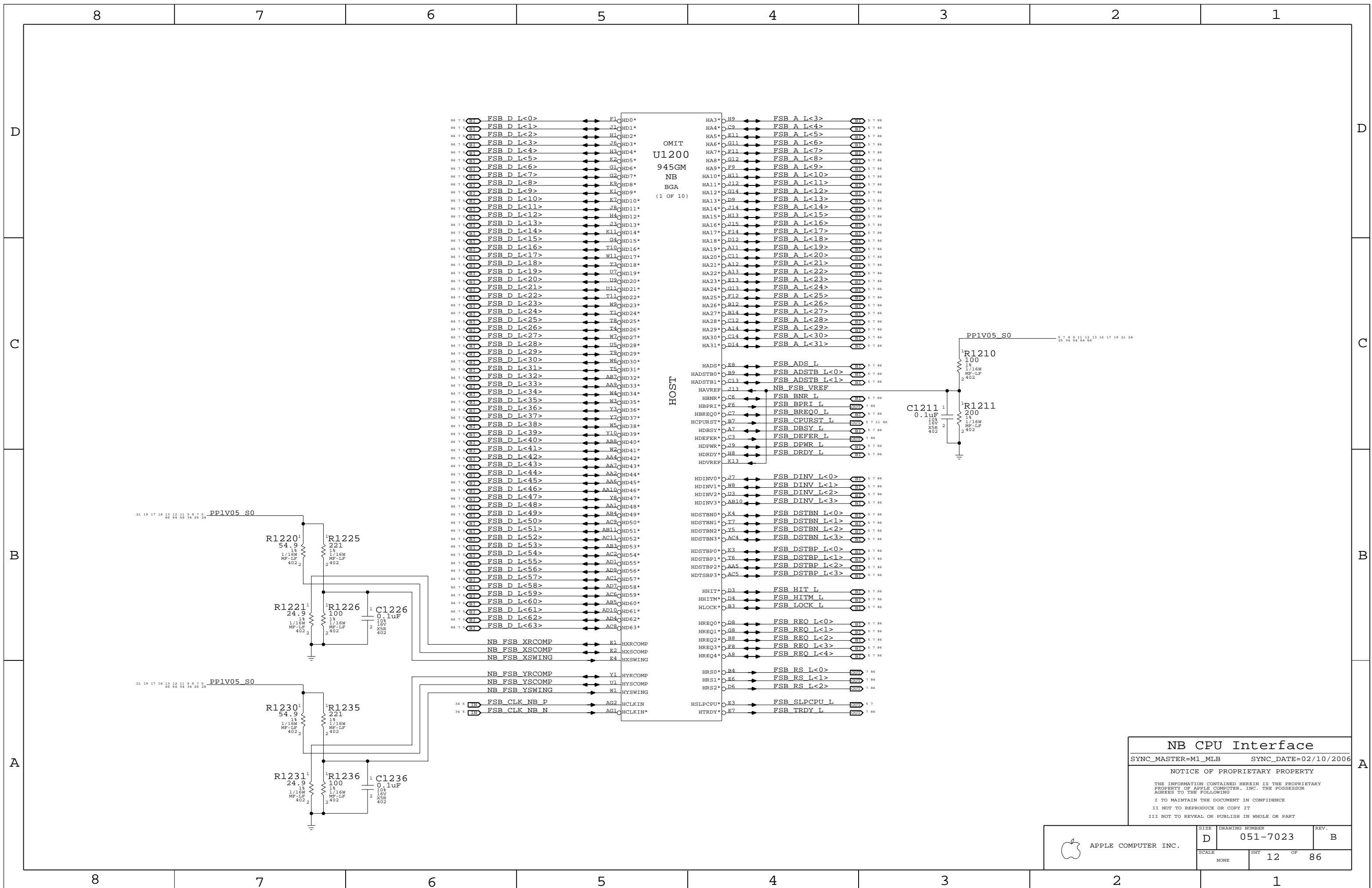


ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO
 CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG
 SYNC_MASTER=MSYNCBDATE=02/10/2006

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OMIT
U1200
945GM
NB
BGA
(1 OF 10)

HOST

NB CPU Interface
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NONE			

LVDS Disable

Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

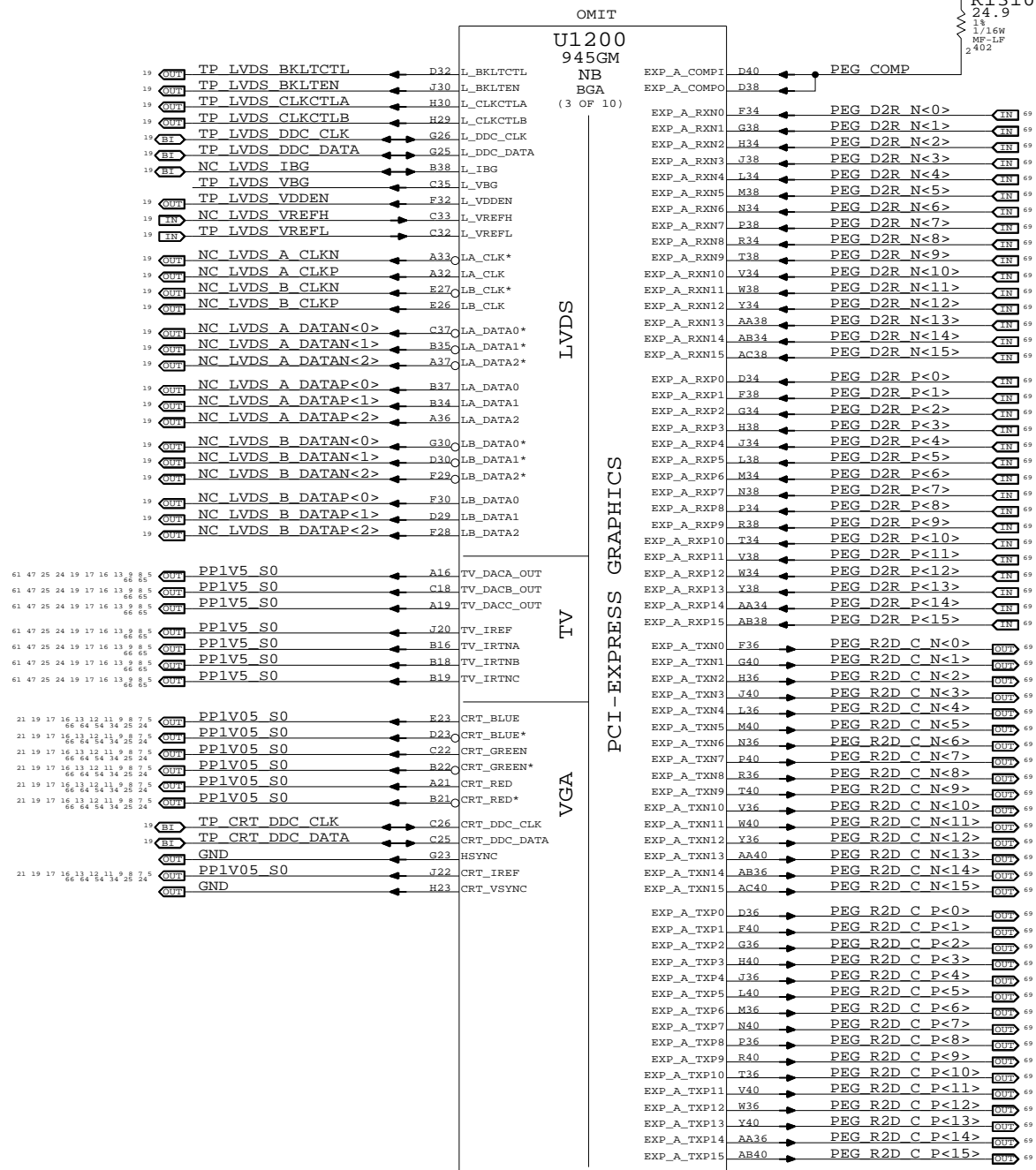
Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

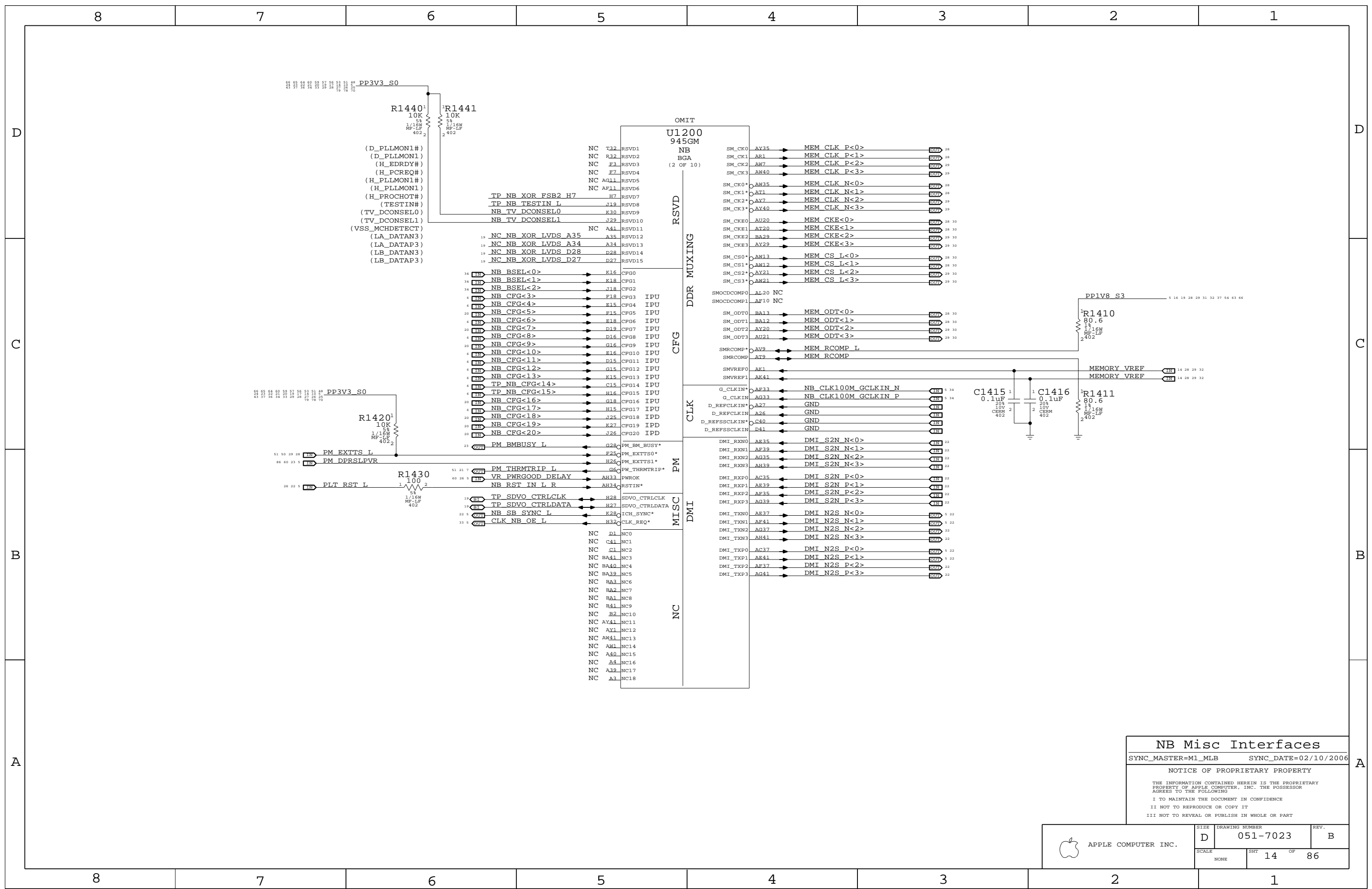
SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
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NONE			



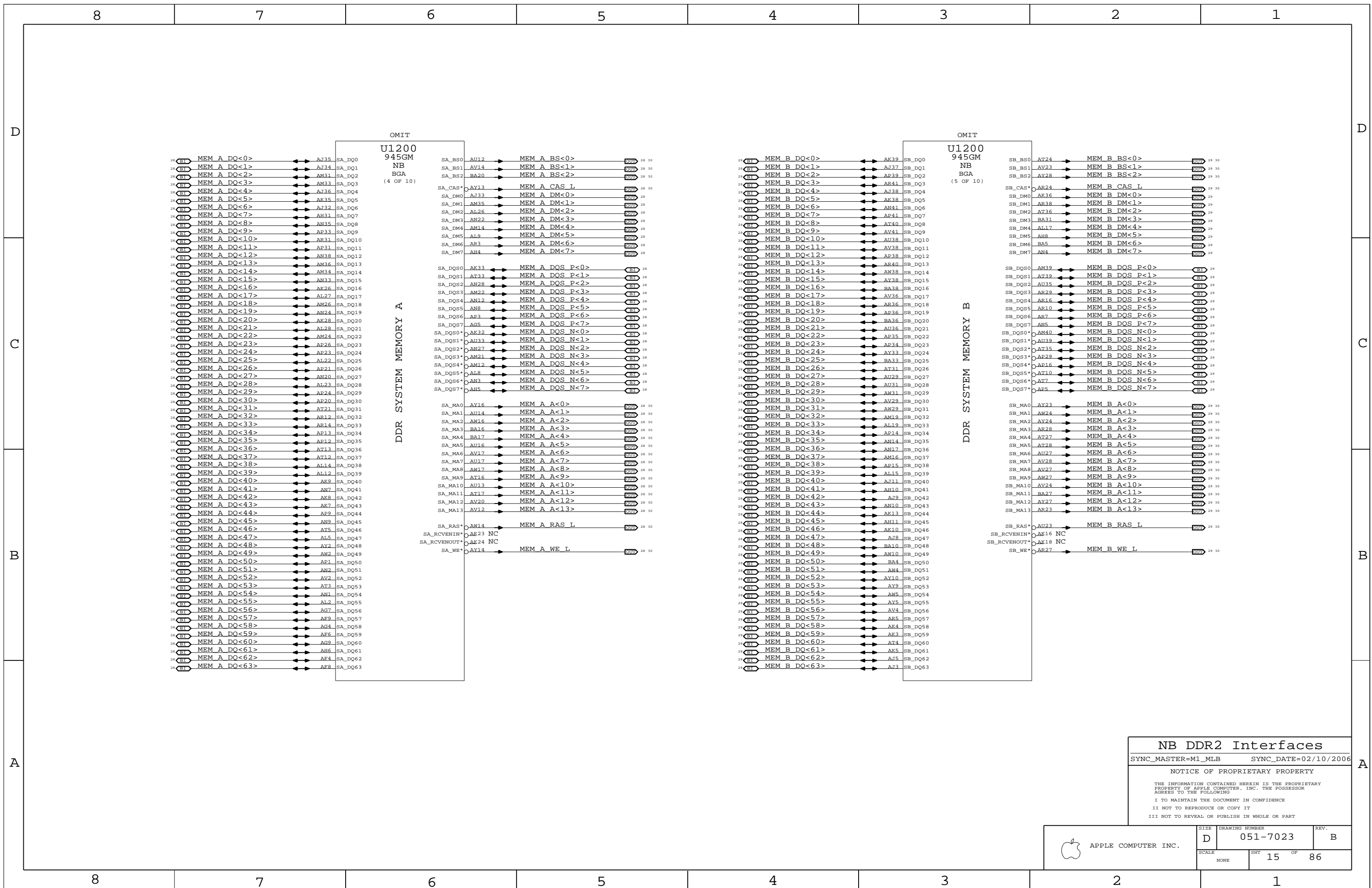
NB Misc Interfaces

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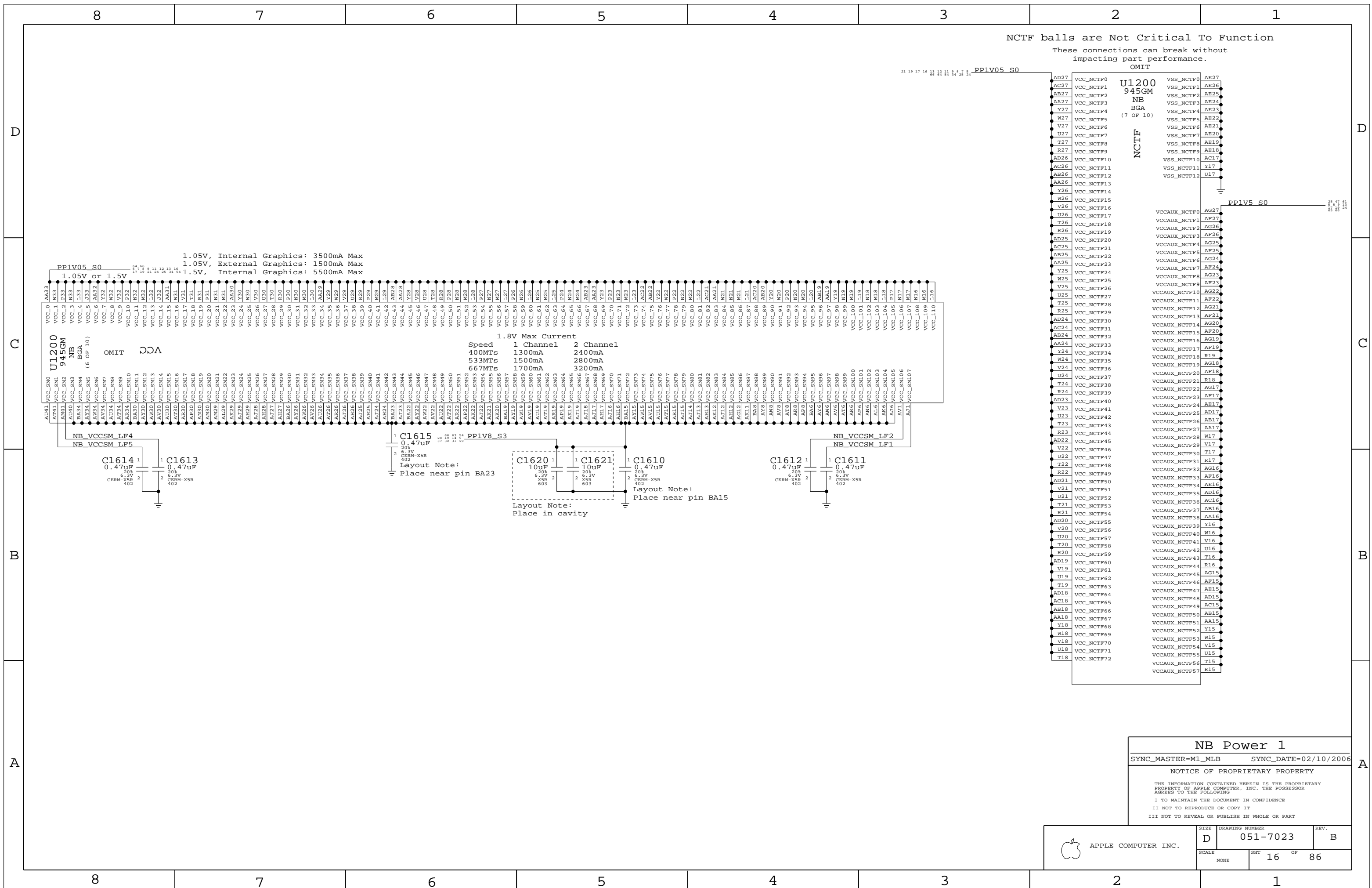
NB DDR2 Interfaces
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NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

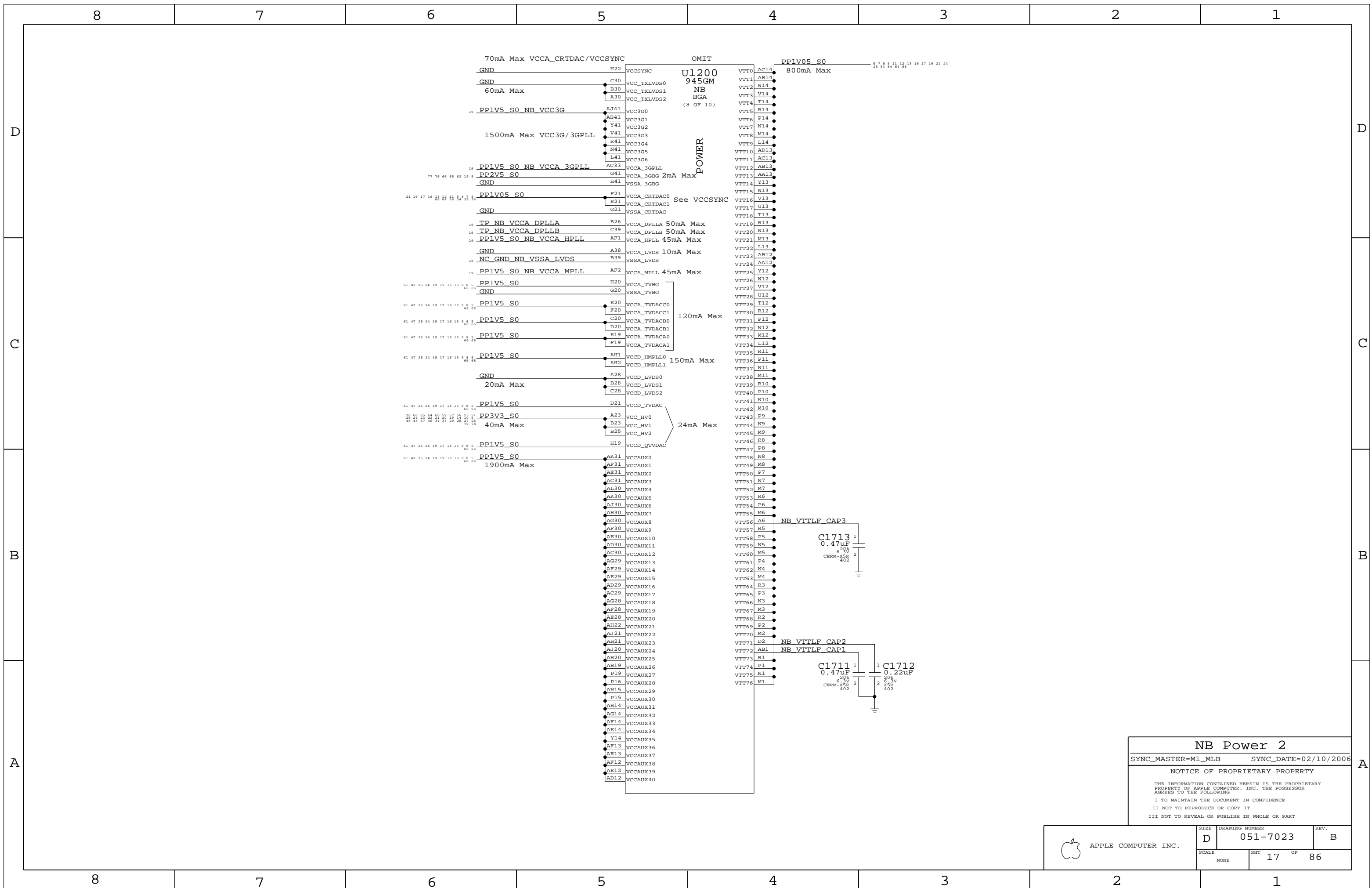
VSS_NCTF0 AE27
 VSS_NCTF1 AE26
 VSS_NCTF2 AE25
 VSS_NCTF3 AE24
 VSS_NCTF4 AE23
 VSS_NCTF5 AE22
 VSS_NCTF6 AE21
 VSS_NCTF7 AE20
 VSS_NCTF8 AE19
 VSS_NCTF9 AE18
 VSS_NCTF10 AC17
 VSS_NCTF11 Y17
 VSS_NCTF12 U17

VCCAUX_NCTF0 AG27
 VCCAUX_NCTF1 AF27
 VCCAUX_NCTF2 AG26
 VCCAUX_NCTF3 AF26
 VCCAUX_NCTF4 AG25
 VCCAUX_NCTF5 AF25
 VCCAUX_NCTF6 AG24
 VCCAUX_NCTF7 AF24
 VCCAUX_NCTF8 AG23
 VCCAUX_NCTF9 AF23
 VCCAUX_NCTF10 AG22
 VCCAUX_NCTF11 AF22
 VCCAUX_NCTF12 AG21
 VCCAUX_NCTF13 AF21
 VCCAUX_NCTF14 AG20
 VCCAUX_NCTF15 AF20
 VCCAUX_NCTF16 AG19
 VCCAUX_NCTF17 AF19
 VCCAUX_NCTF18 R19
 VCCAUX_NCTF19 AG18
 VCCAUX_NCTF20 AF18
 VCCAUX_NCTF21 R18
 VCCAUX_NCTF22 AG17
 VCCAUX_NCTF23 AF17
 VCCAUX_NCTF24 AE17
 VCCAUX_NCTF25 AD17
 VCCAUX_NCTF26 AB17
 VCCAUX_NCTF27 AA17
 VCCAUX_NCTF28 W17
 VCCAUX_NCTF29 V17
 VCCAUX_NCTF30 T17
 VCCAUX_NCTF31 R17
 VCCAUX_NCTF32 AG16
 VCCAUX_NCTF33 AF16
 VCCAUX_NCTF34 AE16
 VCCAUX_NCTF35 AD16
 VCCAUX_NCTF36 AC16
 VCCAUX_NCTF37 AB16
 VCCAUX_NCTF38 AA16
 VCCAUX_NCTF39 Y16
 VCCAUX_NCTF40 W16
 VCCAUX_NCTF41 V16
 VCCAUX_NCTF42 U16
 VCCAUX_NCTF43 T16
 VCCAUX_NCTF44 R16
 VCCAUX_NCTF45 AG15
 VCCAUX_NCTF46 AF15
 VCCAUX_NCTF47 AE15
 VCCAUX_NCTF48 AD15
 VCCAUX_NCTF49 AC15
 VCCAUX_NCTF50 AB15
 VCCAUX_NCTF51 AA15
 VCCAUX_NCTF52 Y15
 VCCAUX_NCTF53 W15
 VCCAUX_NCTF54 V15
 VCCAUX_NCTF55 U15
 VCCAUX_NCTF56 T15
 VCCAUX_NCTF57 R15

NB Power 1
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NONE			



NB Power 2

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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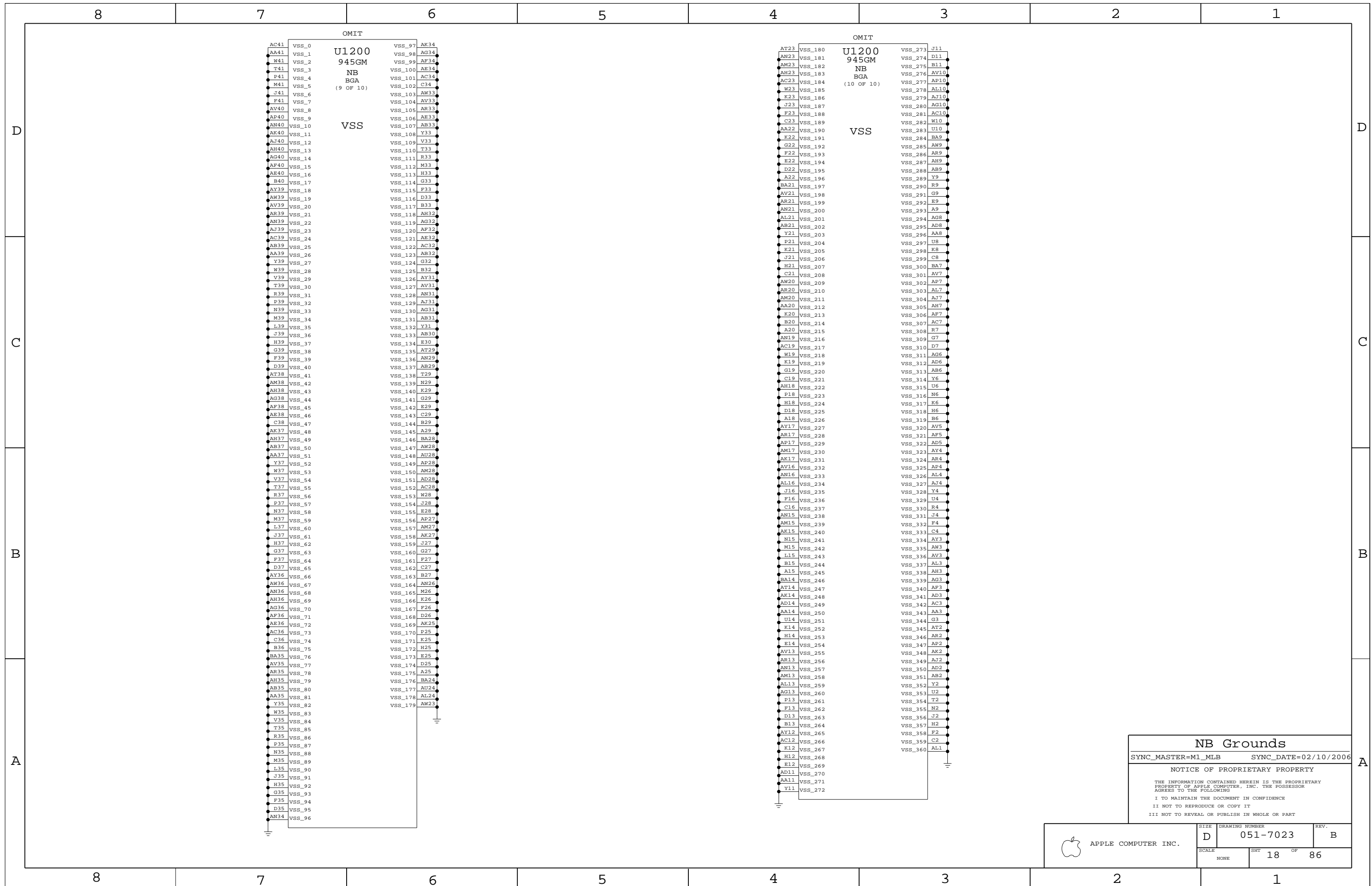
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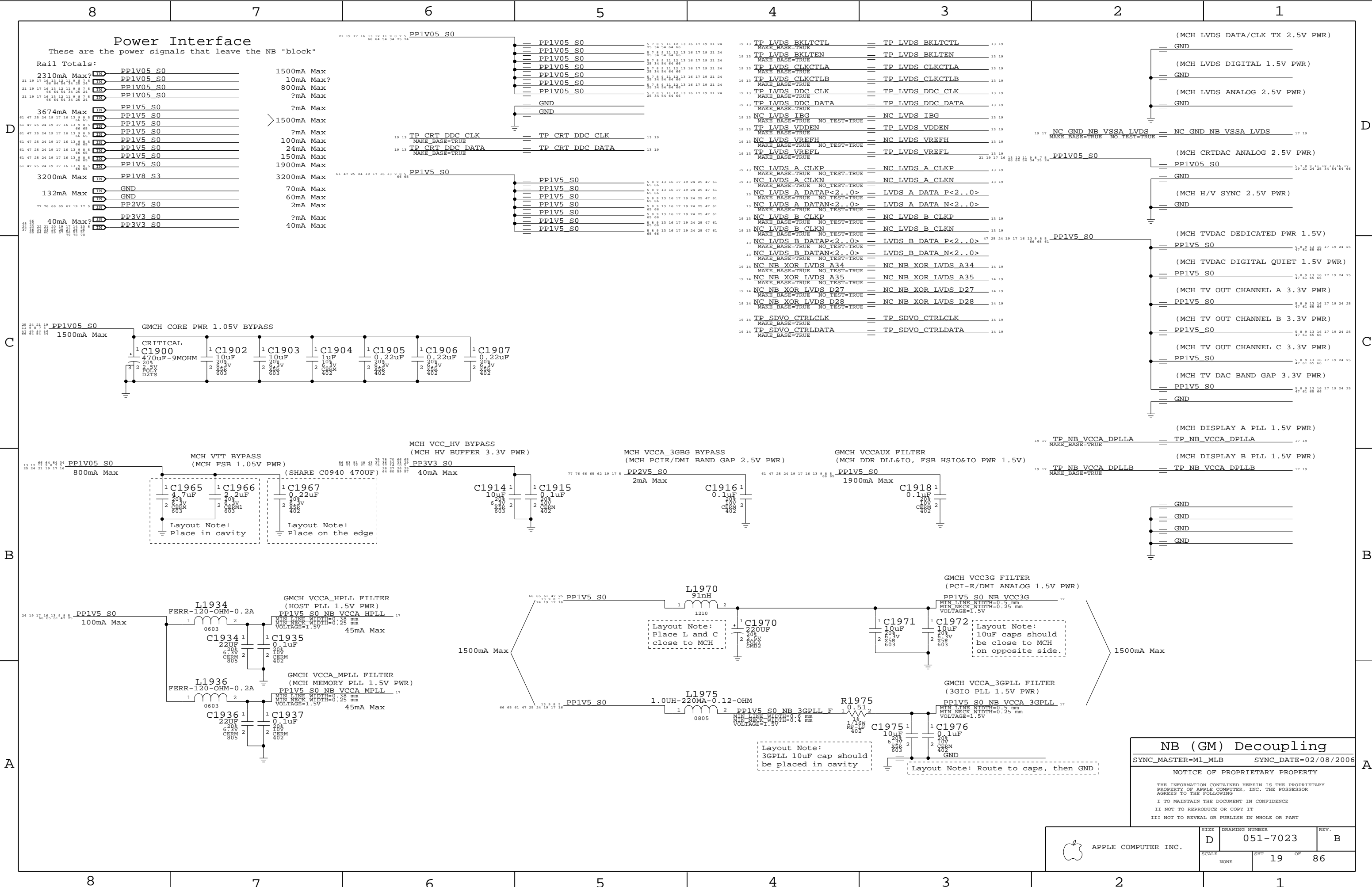
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NB Grounds
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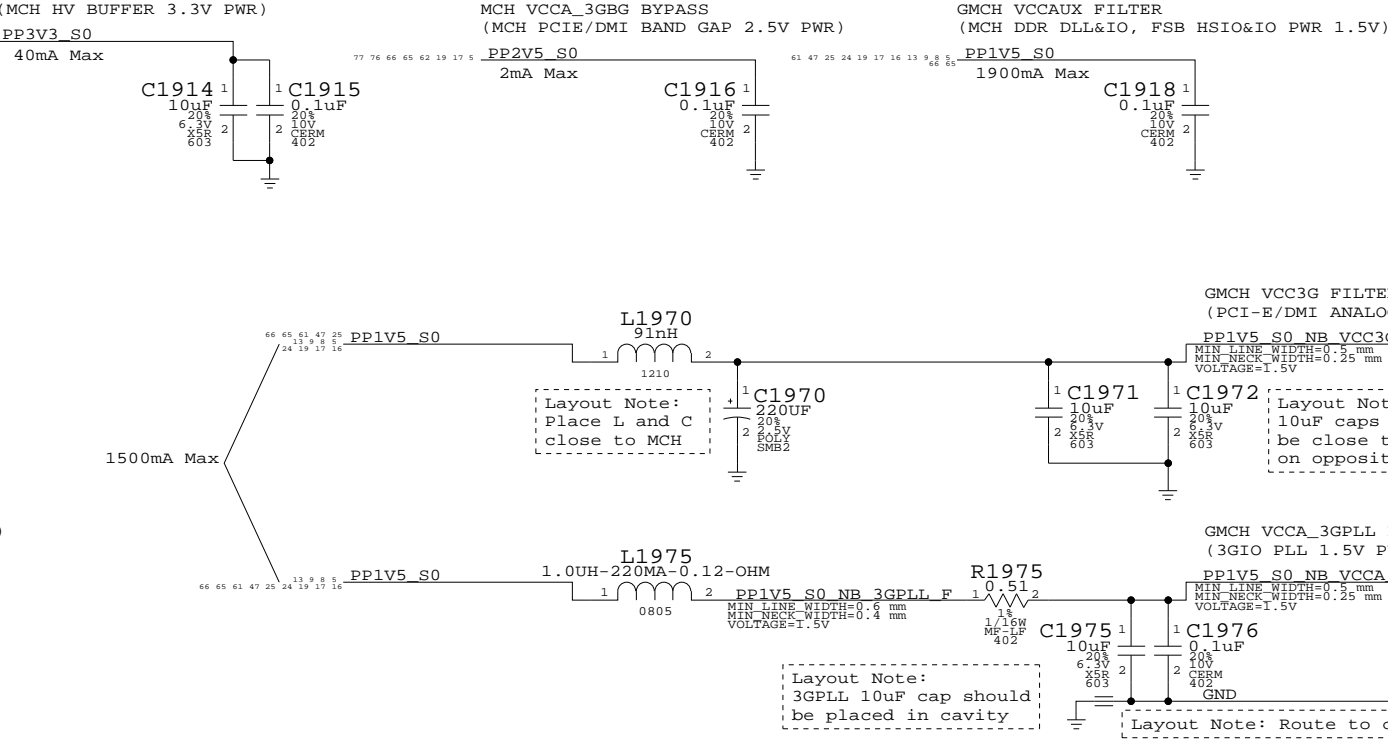
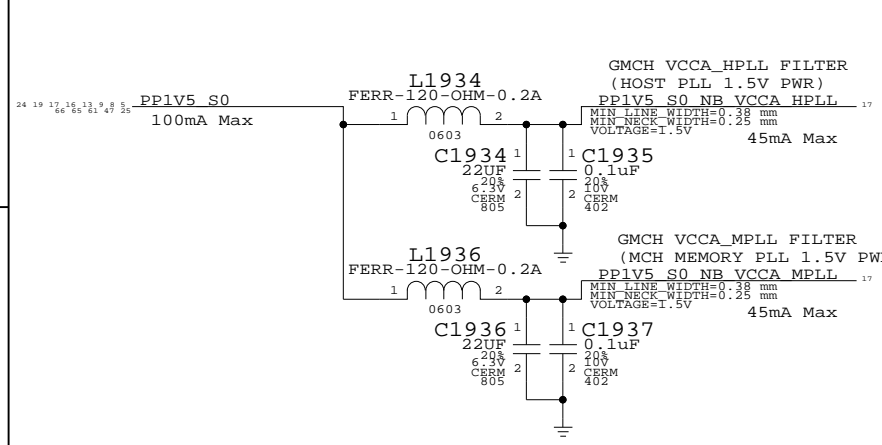
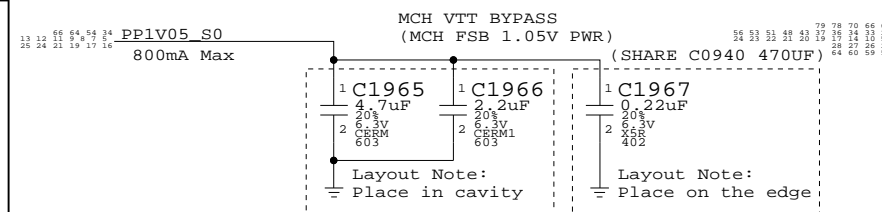
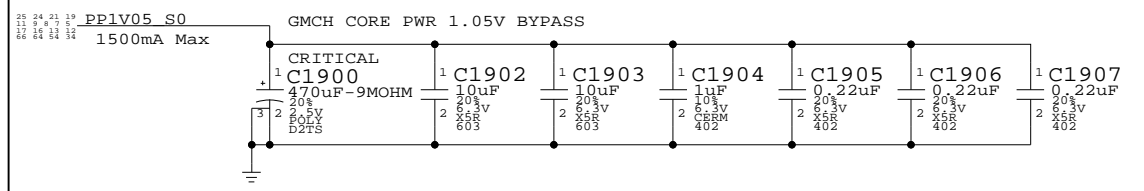
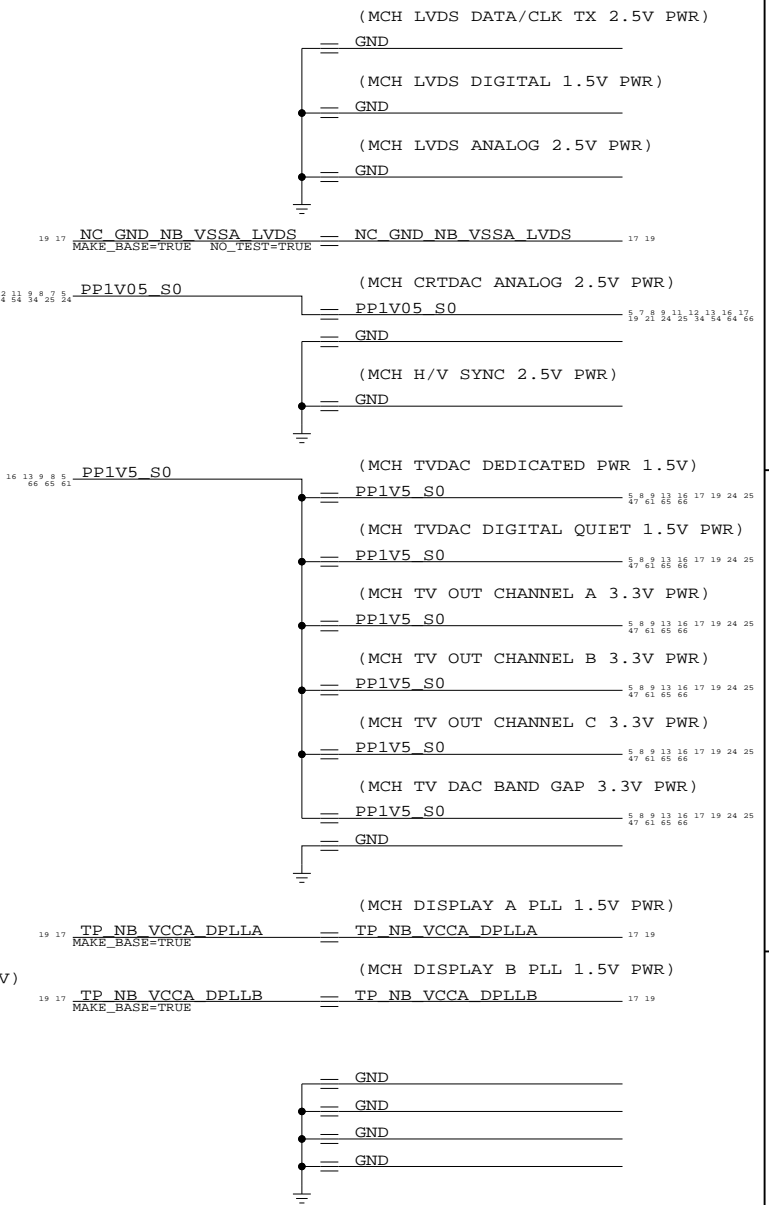
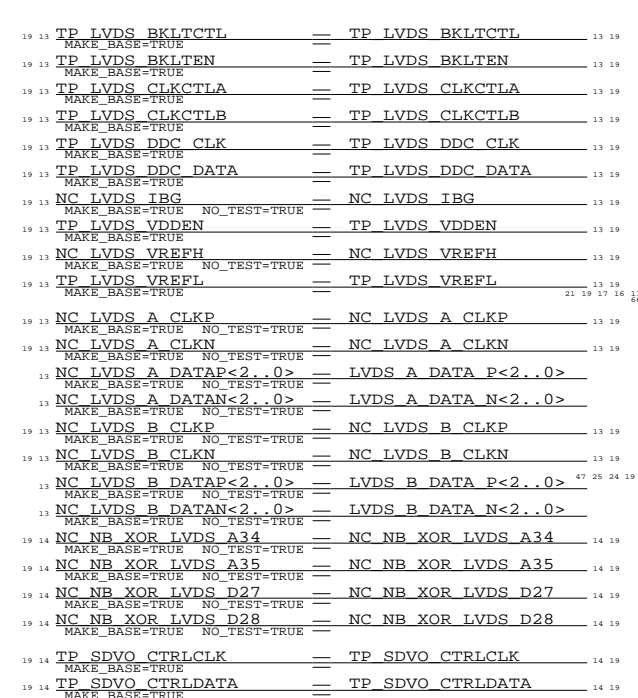
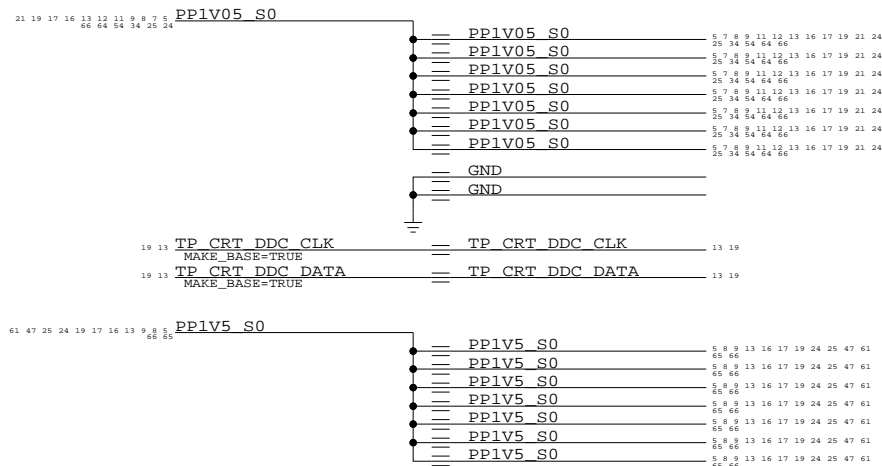


Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	PP1V05_S0	1500mA Max
10mA Max?	PP1V05_S0	10mA Max?
800mA Max	PP1V05_S0	800mA Max
?mA Max	PP1V05_S0	?mA Max
3674mA Max	PP1V5_S0	?mA Max
1500mA Max	PP1V5_S0	>1500mA Max
?mA Max	PP1V5_S0	?mA Max
100mA Max	PP1V5_S0	100mA Max
24mA Max	PP1V5_S0	24mA Max
150mA Max	PP1V5_S0	150mA Max
1900mA Max	PP1V5_S0	1900mA Max
3200mA Max	PP1V8_S3	3200mA Max
70mA Max	GND	70mA Max
60mA Max	GND	60mA Max
2mA Max	PP2V5_S0	2mA Max
?mA Max	PP3V3_S0	?mA Max
40mA Max?	PP3V3_S0	40mA Max



NB (GM) Decoupling

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

NOTICE OF PROPRIETARY PROPERTY

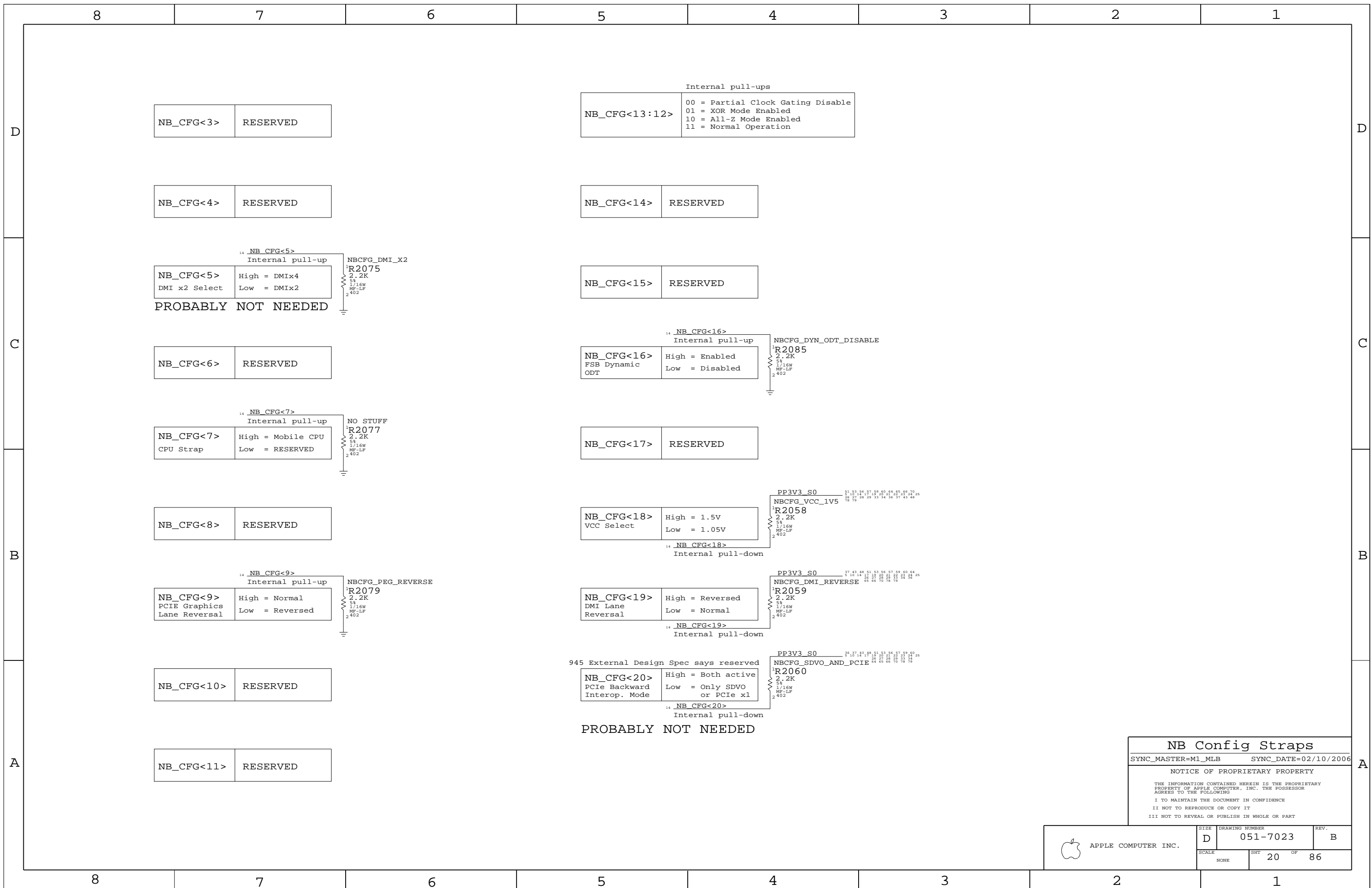
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	D	051-7023	B
SCALE	SHT	OF	
NONE	19	OF	86



NB_CFG<3> RESERVED

Internal pull-ups
 NB_CFG<13:12> 00 = Partial Clock Gating Disable
 01 = XOR Mode Enabled
 10 = All-Z Mode Enabled
 11 = Normal Operation

NB_CFG<4> RESERVED

NB_CFG<14> RESERVED

¹⁴ NB_CFG<5>
 Internal pull-up
 NBCFG_DMI_X2
¹R2075
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<5> High = DMIx4
 DMI x2 Select Low = DMIx2
 PROBABLY NOT NEEDED

NB_CFG<15> RESERVED

NB_CFG<6> RESERVED

¹⁴ NB_CFG<16>
 Internal pull-up
 NBCFG_DYN_ODT_DISABLE
¹R2085
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<16> High = Enabled
 FSB Dynamic ODT Low = Disabled

¹⁴ NB_CFG<7>
 Internal pull-up
 NO STUFF
¹R2077
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<7> High = Mobile CPU
 CPU Strap Low = RESERVED

NB_CFG<17> RESERVED

NB_CFG<8> RESERVED

PP3V3_S0
 NBCFG_VCC_1V5
¹R2058
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<18> High = 1.5V
 VCC Select Low = 1.05V
¹⁴ NB_CFG<18>
 Internal pull-down

¹⁴ NB_CFG<9>
 Internal pull-up
 NBCFG_PEG_REVERSE
¹R2079
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<9> High = Normal
 PCIe Graphics Lane Reversal Low = Reversed

PP3V3_S0
 NBCFG_DMI_REVERSE
¹R2059
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<19> High = Reversed
 DMI Lane Reversal Low = Normal
¹⁴ NB_CFG<19>
 Internal pull-down

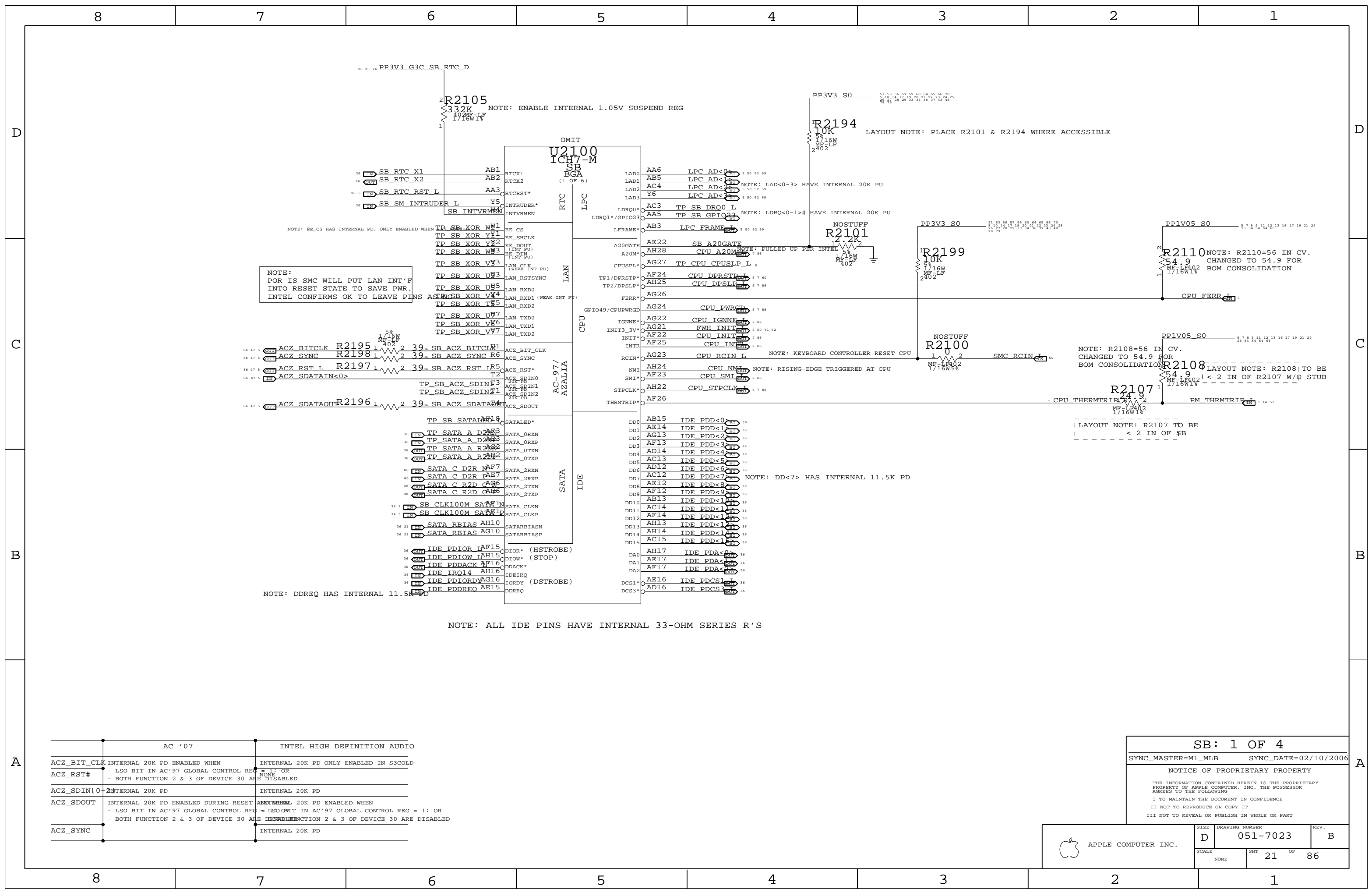
NB_CFG<10> RESERVED

945 External Design Spec says reserved
 PP3V3_S0
 NBCFG_SDVO_AND_PCIE
¹R2060
 2.2K
 5V
 1/16W MF-LP
 2 402
 NB_CFG<20> High = Both active
 PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
¹⁴ NB_CFG<20>
 Internal pull-down
 PROBABLY NOT NEEDED

NB_CFG<11> RESERVED

NB Config Straps
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.
 SIZE D DRAWING NUMBER 051-7023 REV. B
 SCALE NONE SHT 20 OF 86



NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS

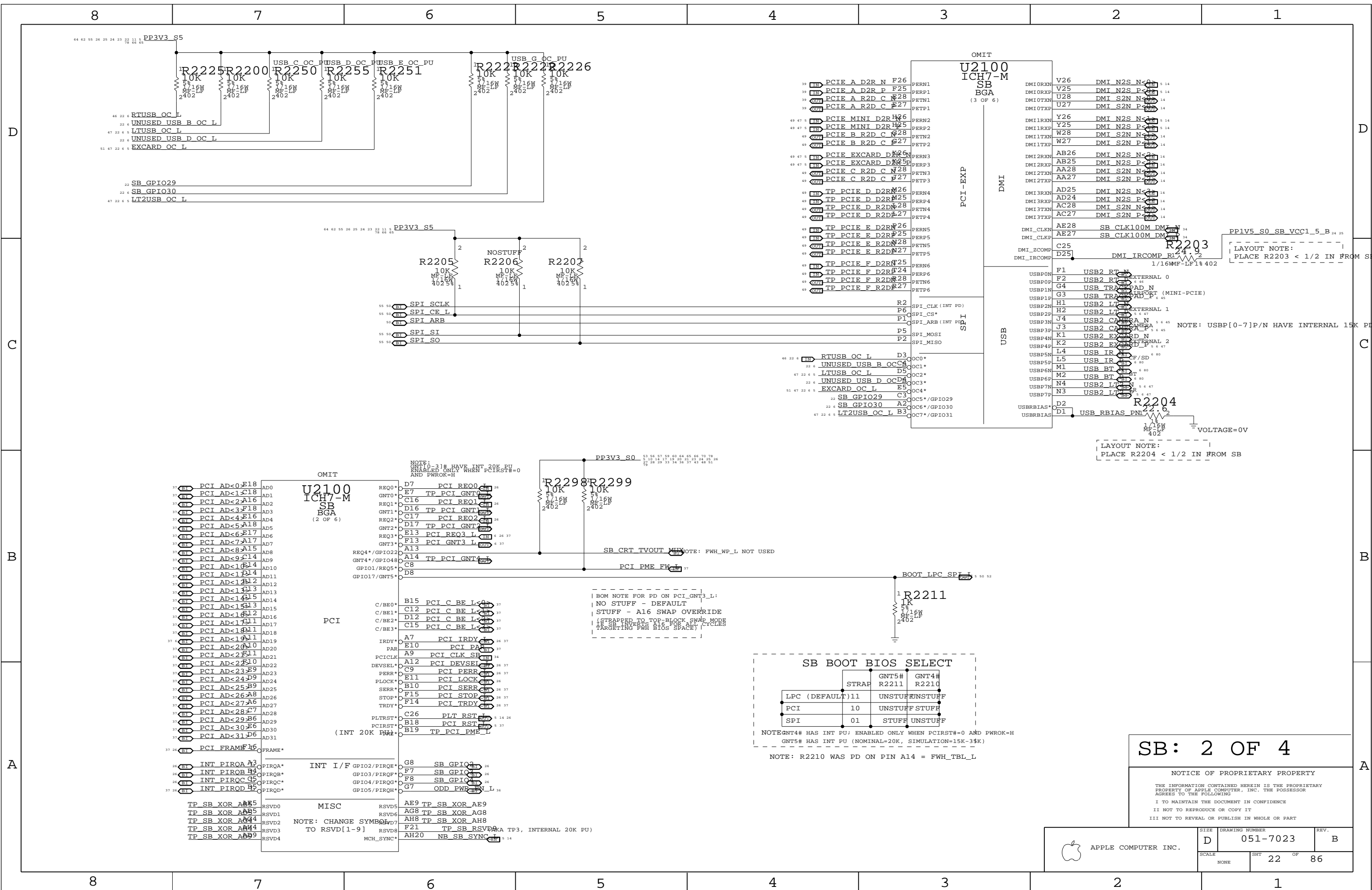
NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_RST#	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_SDIN[0:2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND INTERNAL 20K PD ENABLED WHEN LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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	D	051-7023	B
SCALE	NONE	SHT	21 OF 86



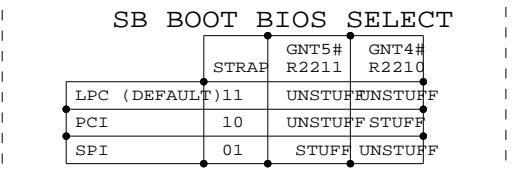
SB: 2 OF 4

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SCALE NONE	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SHT 22 OF 86		



APPLE COMPUTER INC.



NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST# = 0 AND PWROK = H
 GNT5# HAS INT PU (NOMINAL = 20K, SIMULATION = 15K-35K)
 NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

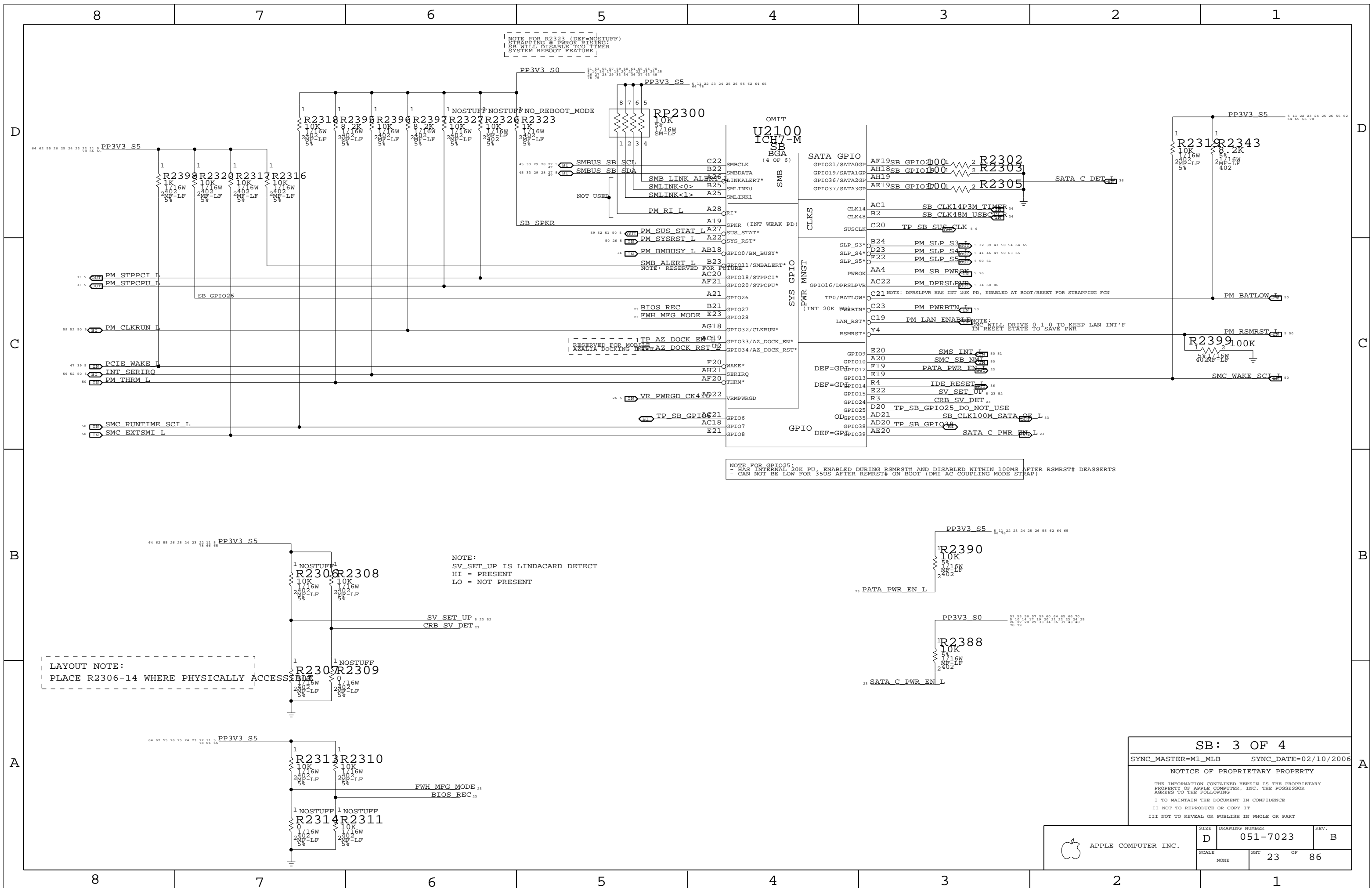
BOM NOTE FOR PD ON PCI_GNT3_L:
 NO STUFF - DEFAULT
 STUFF - A16 SWAP OVERRIDE
 (STRAPPED TO TOP-BLOCK SWAP MODE
 TO TARGETING FWH BIOS SPACE)

NOTE: CHANGE SYMBOL TO RSVD[1-9] TO RSVD8 (INTERNAL 20K PU)
 MCH_SYNC#

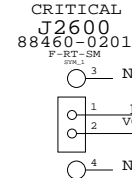
LAYOUT NOTE:
 PLACE R2203 < 1/2 IN FROM SB

LAYOUT NOTE:
 PLACE R2204 < 1/2 IN FROM SB

NOTE: USBP[0-7] P/N HAVE INTERNAL 15K PU

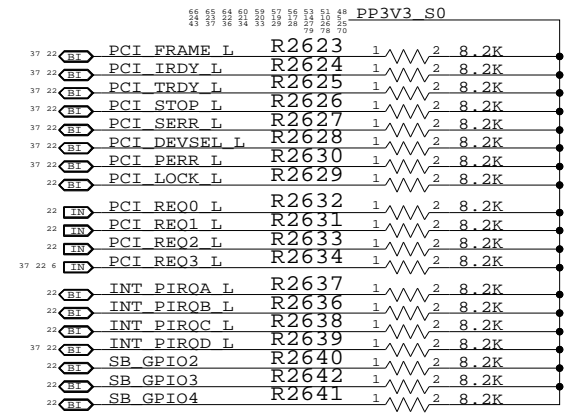
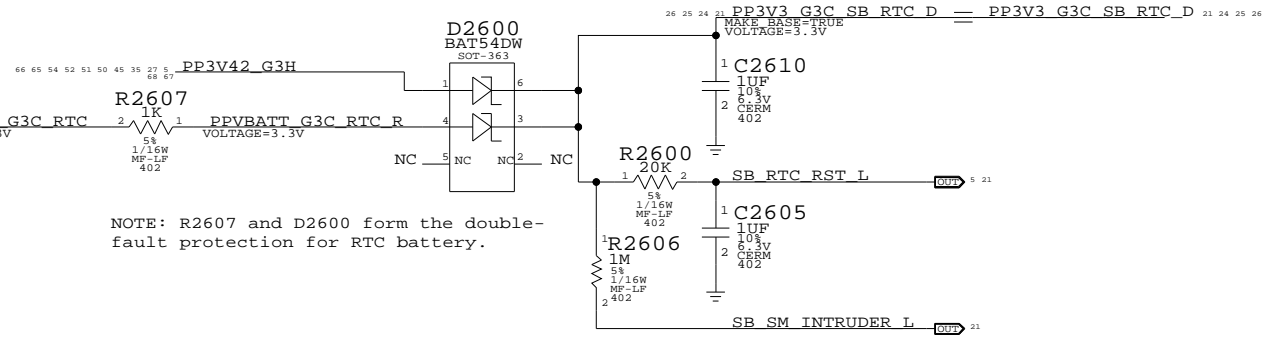


RTC Battery Connector

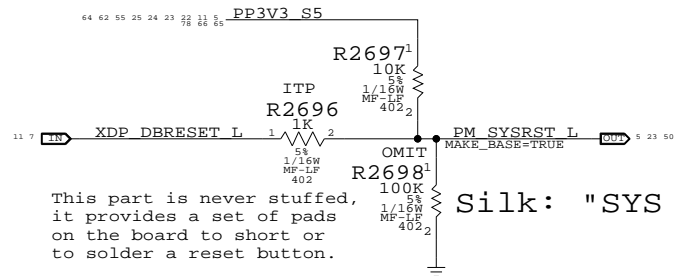
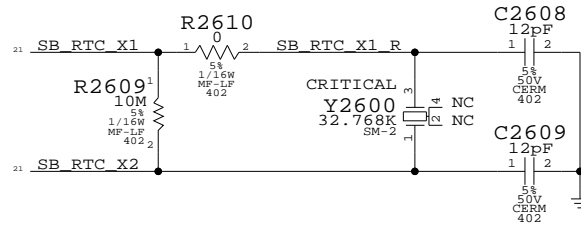


518S0226

NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit

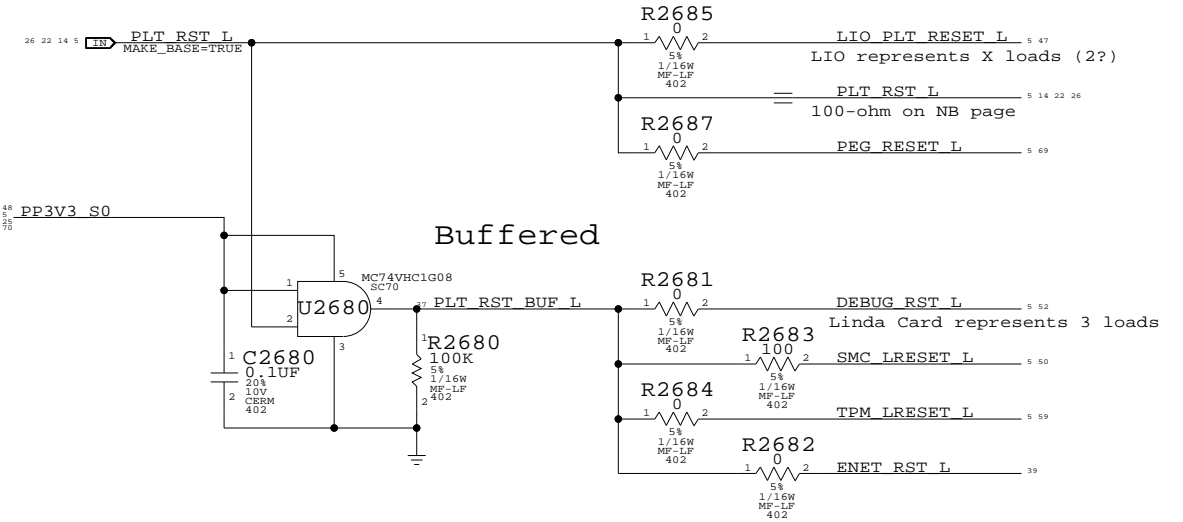


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

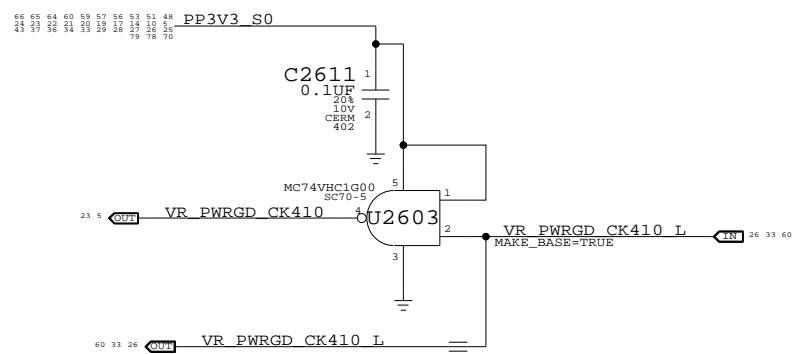
Silk: "SYS RST"

Platform Reset Connections

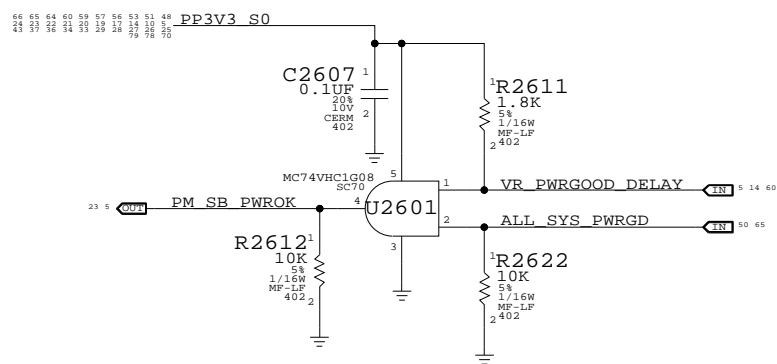
Unbuffered



Initial resistor values are based on CRB, but may change after characterization.

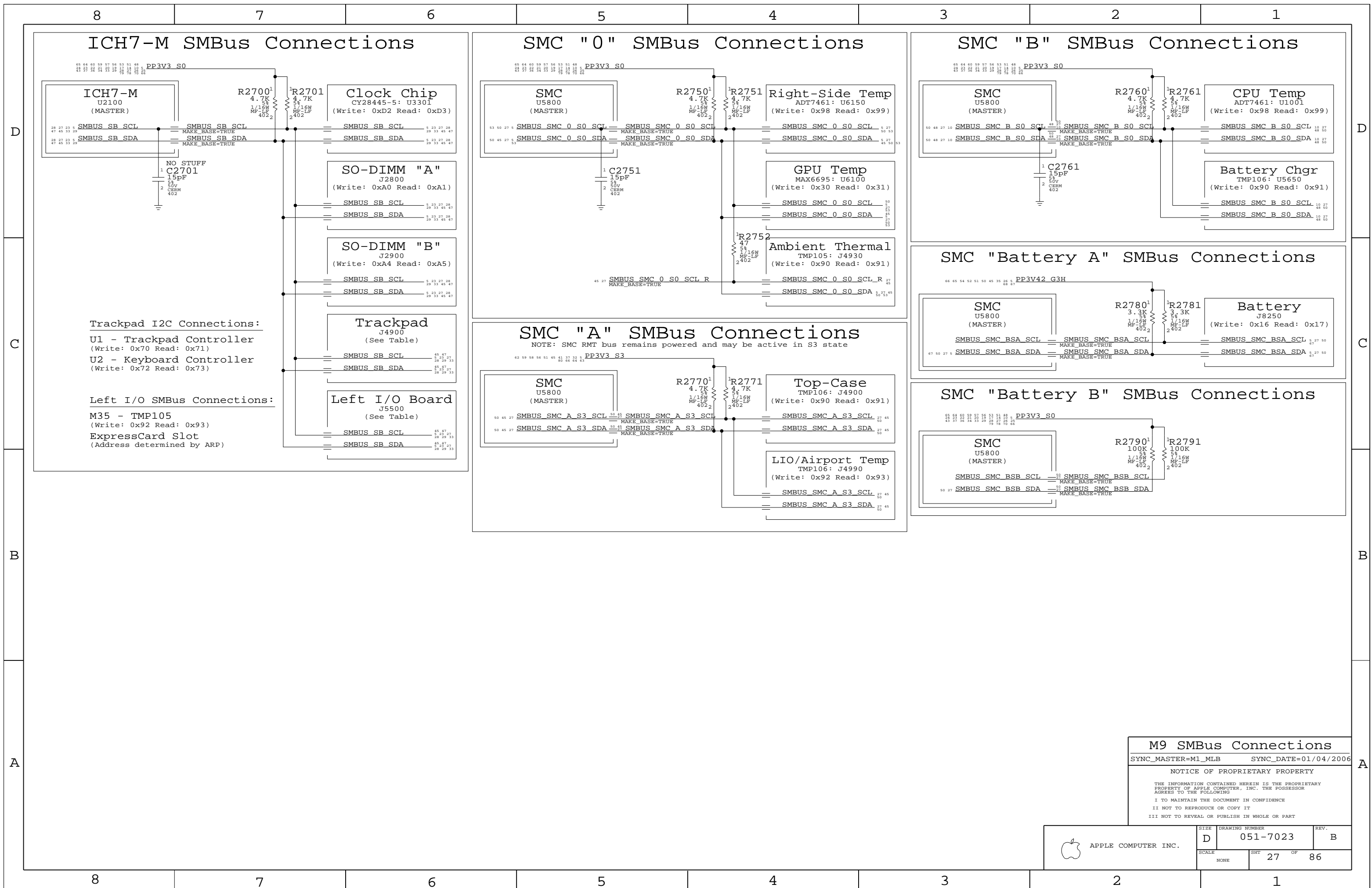


1G00 used as small & cheap inverter

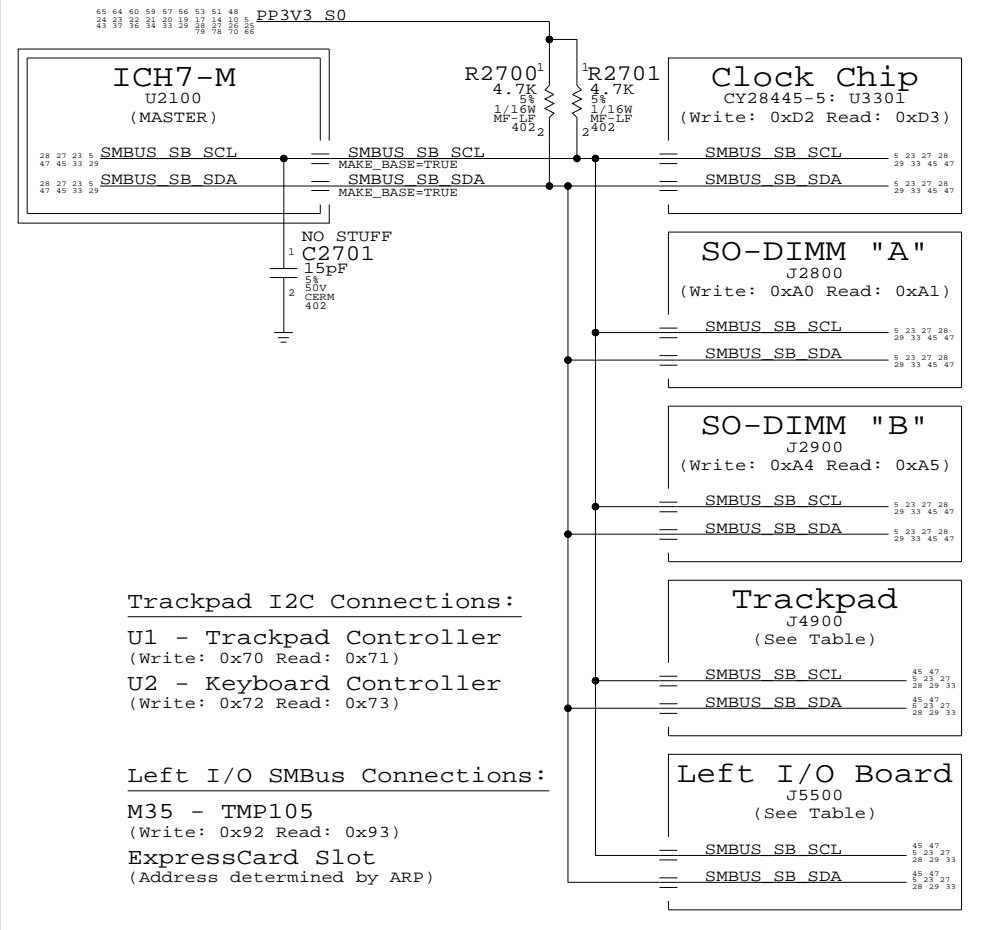


SB Misc		
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006	
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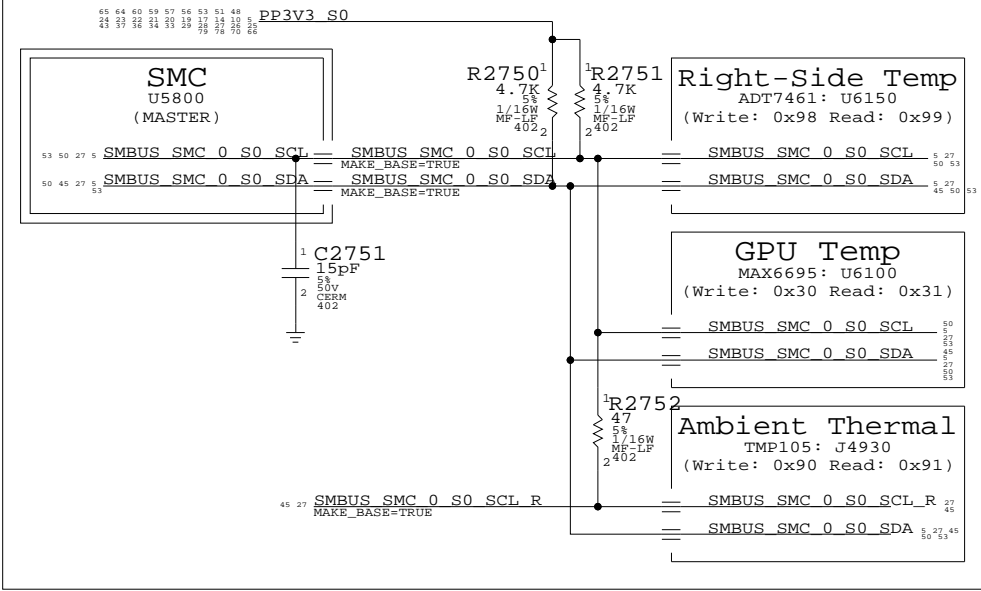
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	26	86	



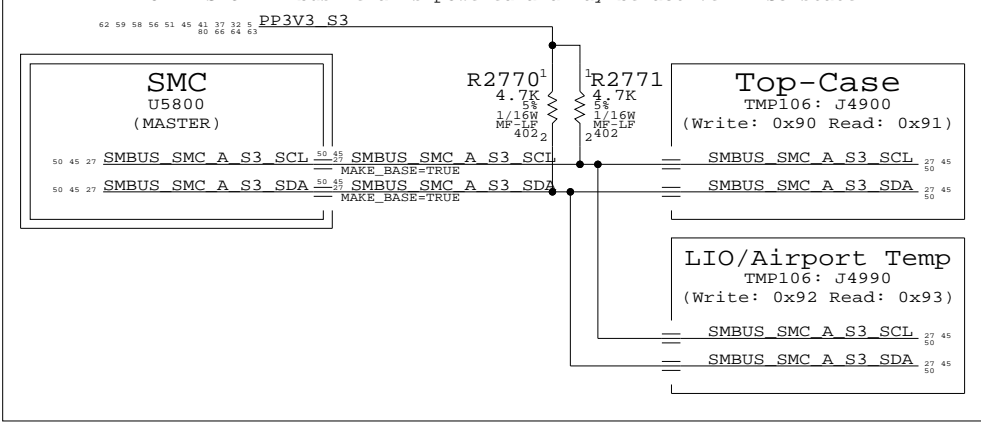
ICH7-M SMBus Connections



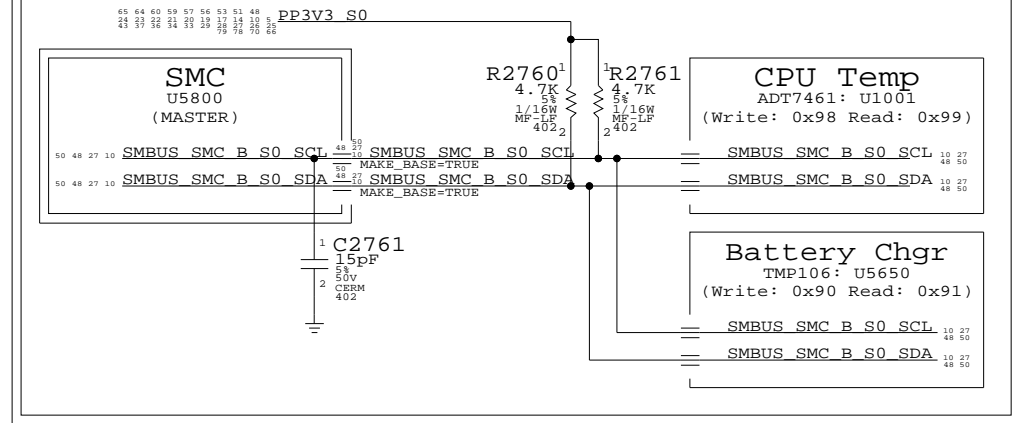
SMC "0" SMBus Connections



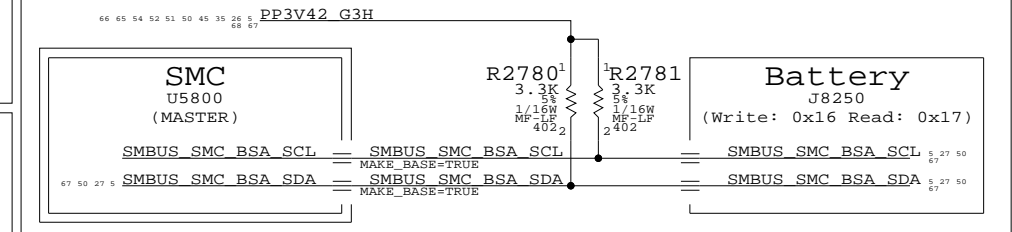
SMC "A" SMBus Connections



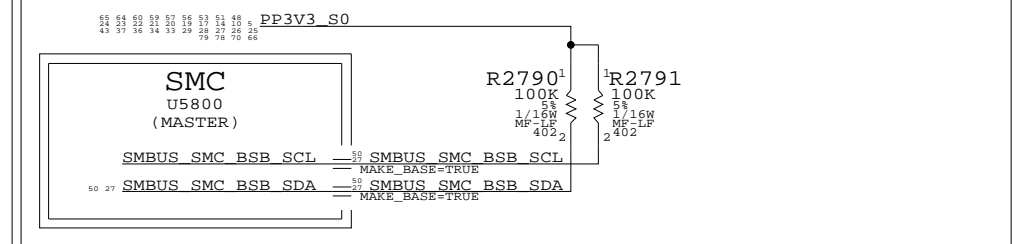
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M9 SMBus Connections

SYNC_MASTER=M1_MLB SYNC_DATE=01/04/2006

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	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	27	86	

Page Notes

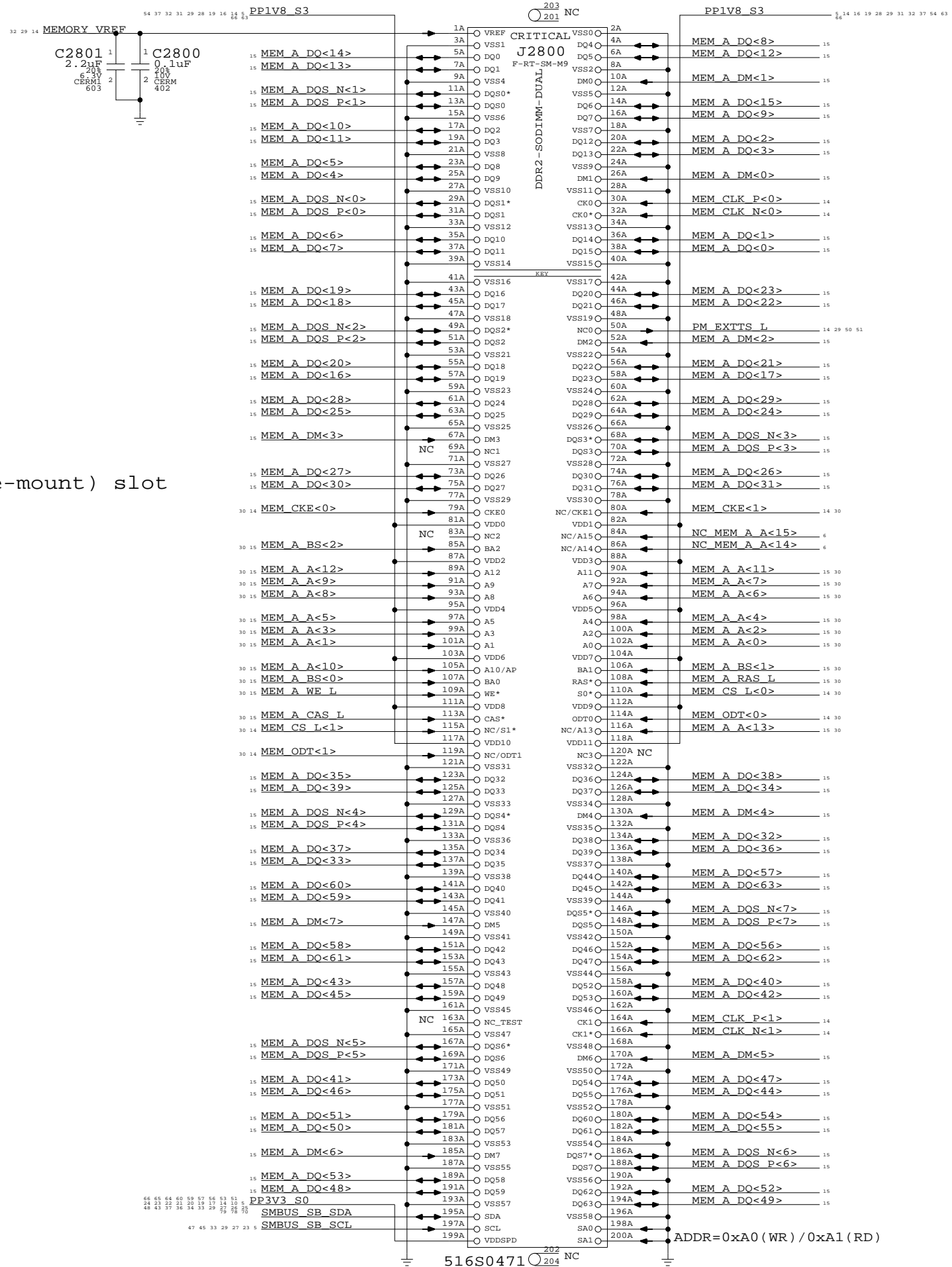
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

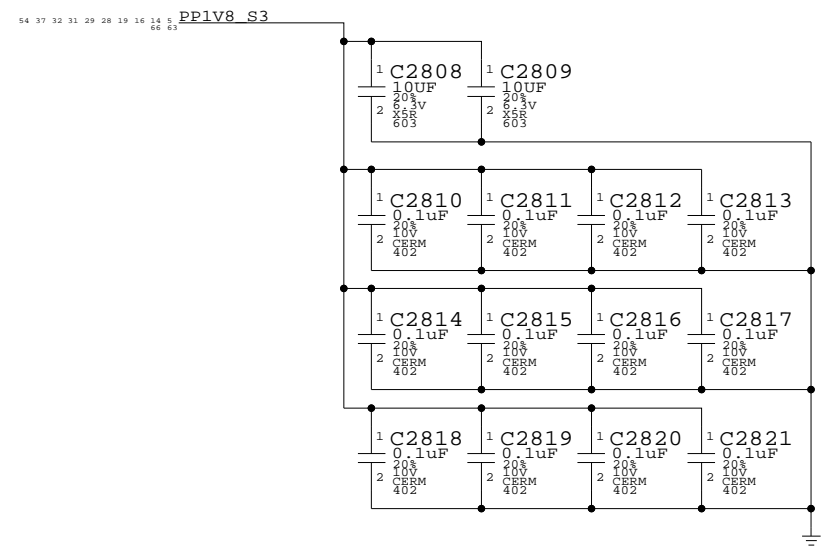
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.

"Lower" (surface-mount) slot



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector A
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	
NONE	28	86	

Page Notes

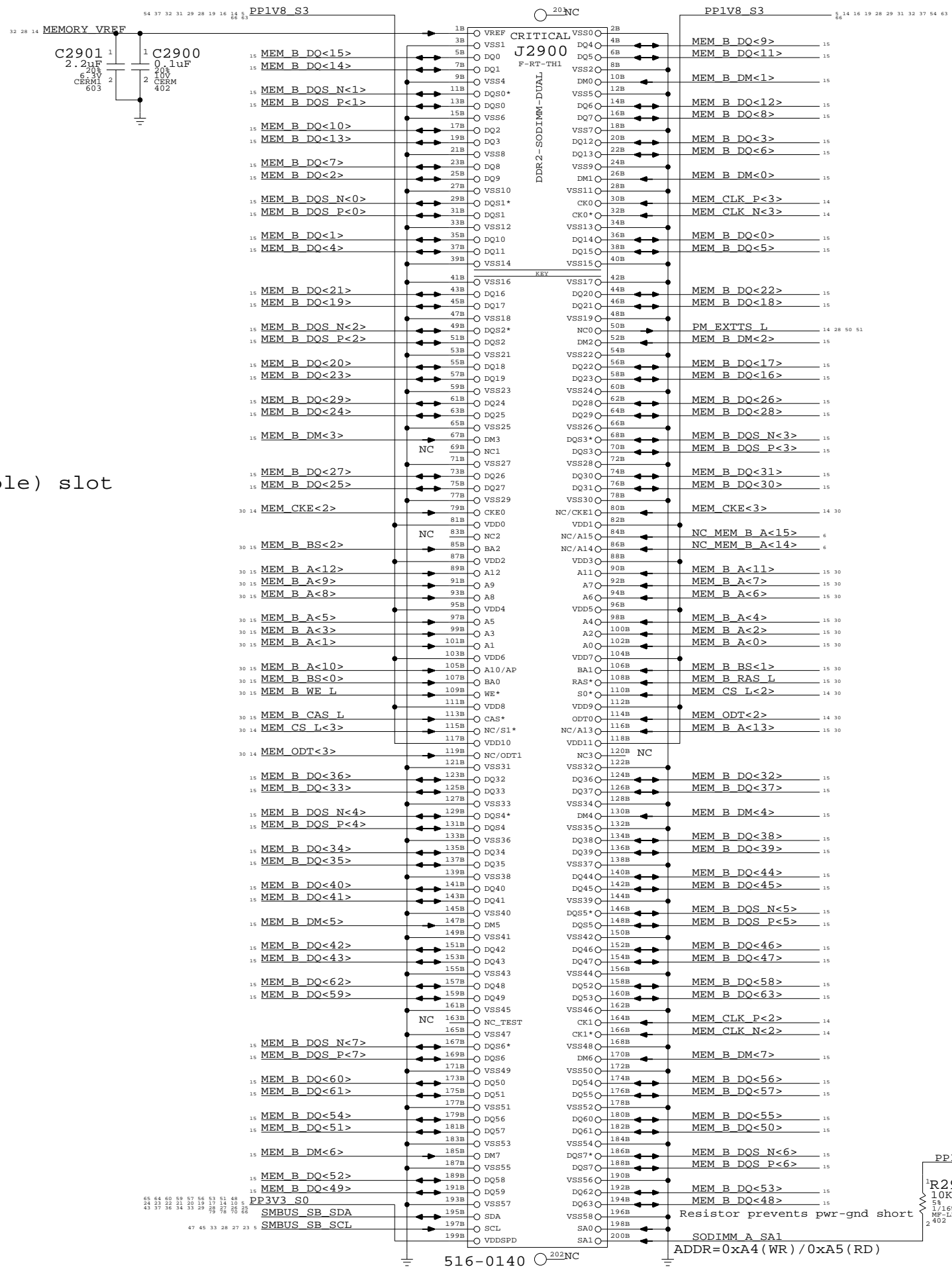
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

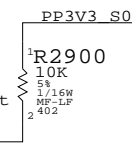
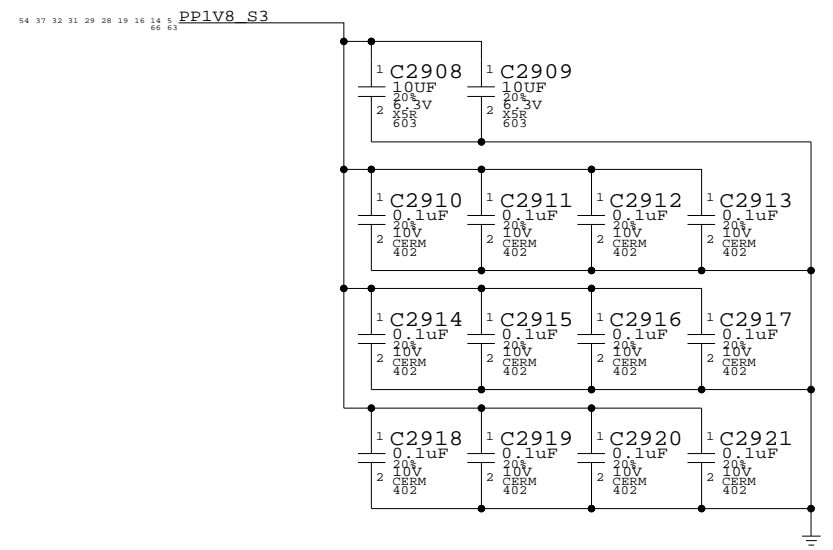
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.

"Upper" (thru-hole) slot



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

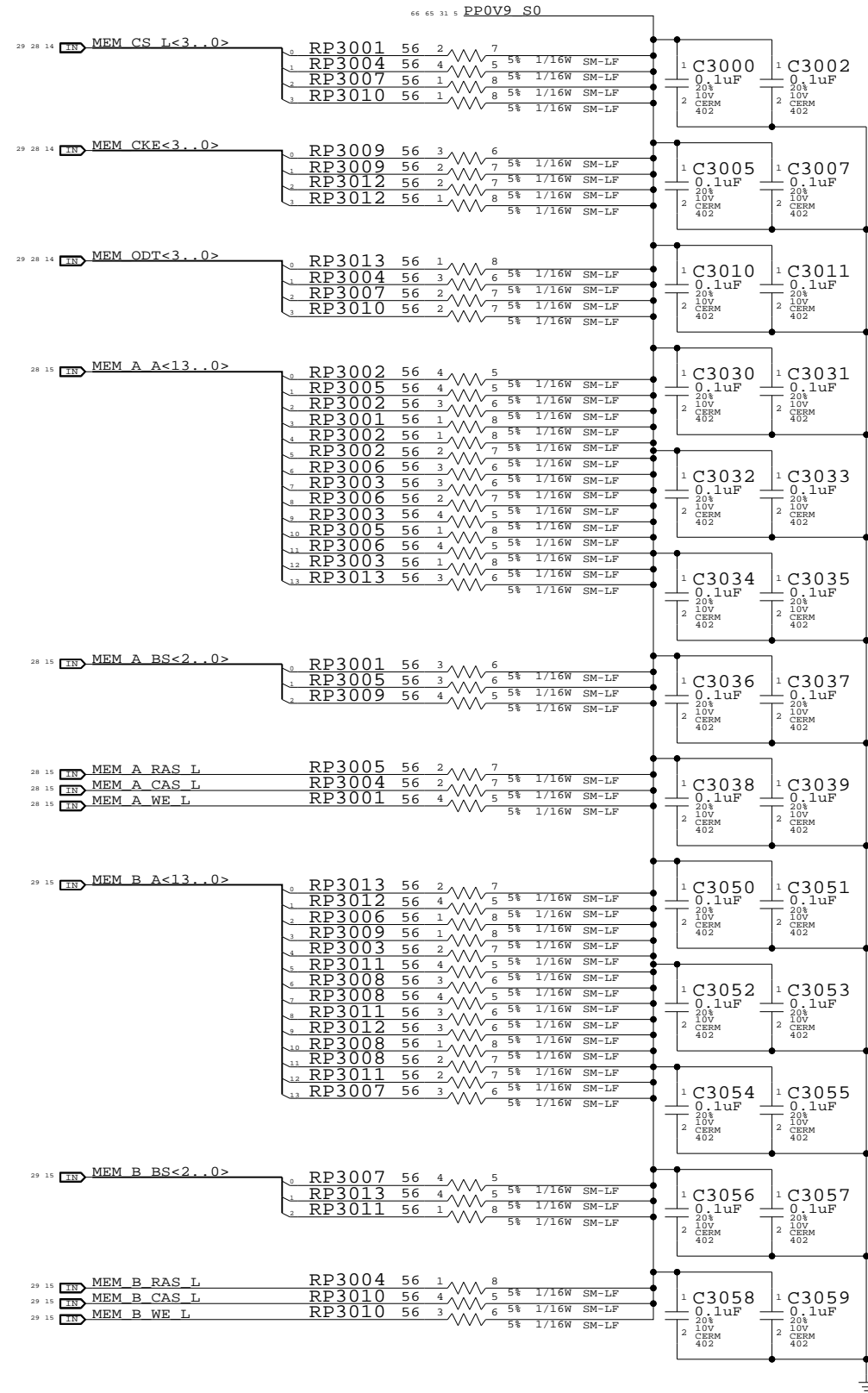
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	B
SCALE	SHT	OF	
NONE	29	86	

One cap for each side of every RPAK, one cap for every two discrete resistors
 Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/07/2006)

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	D	051-7023	B
SCALE	SHT		OF
NONE	30		86

Page Notes

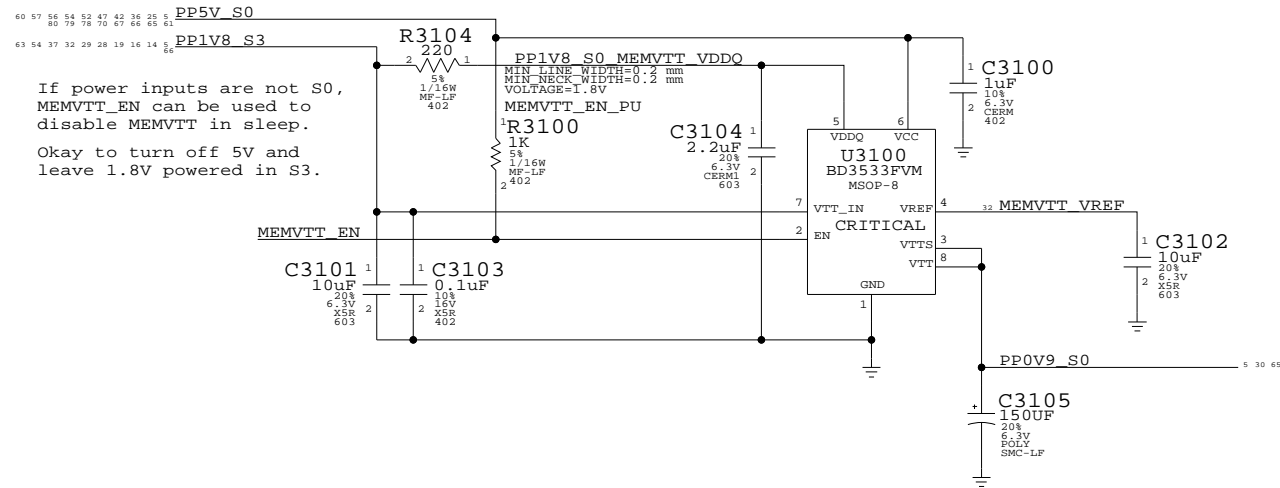
Power aliases required by this page:

- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

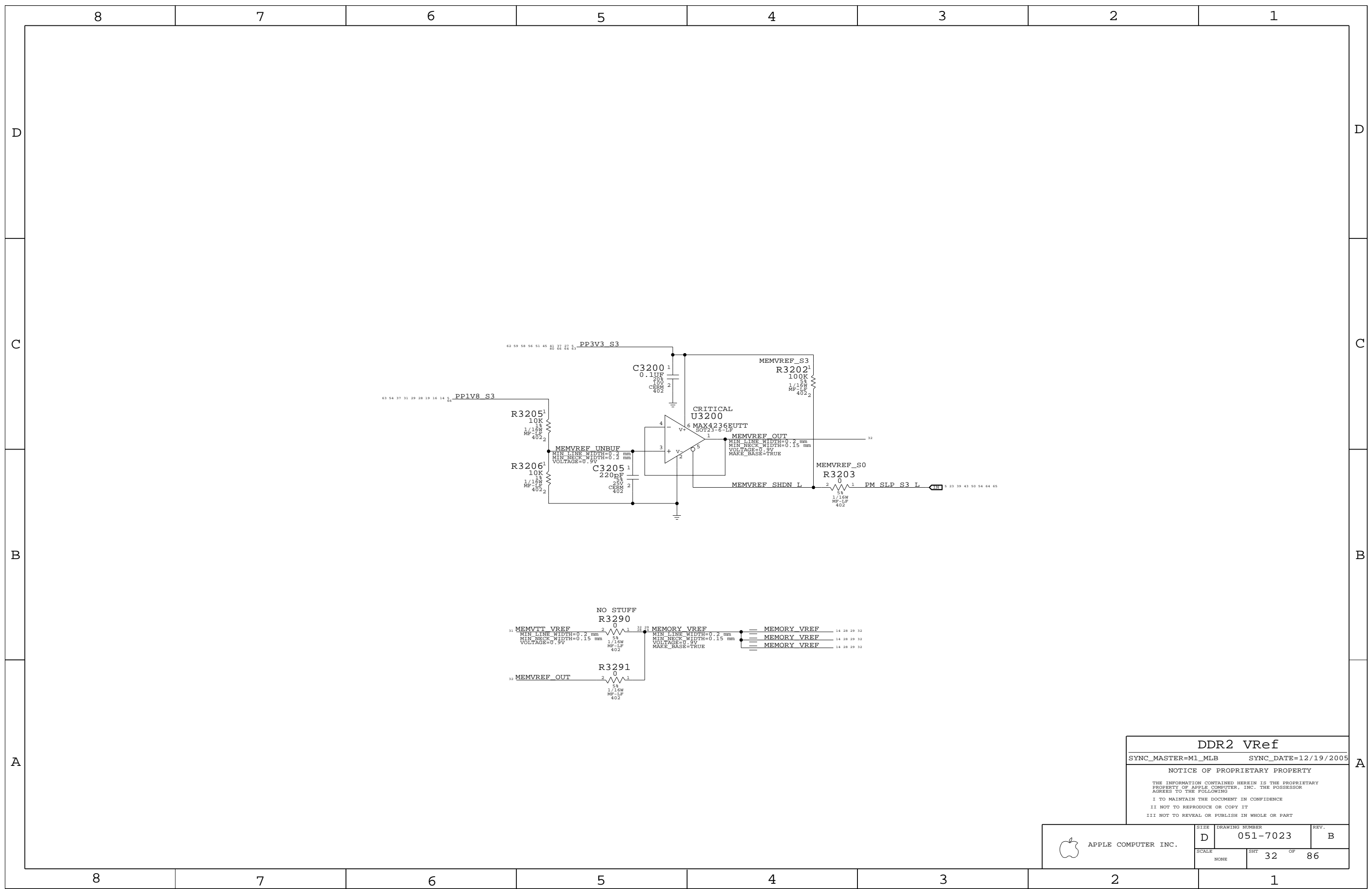
DDR2 Vtt Regulator



If power inputs are not S0,
MEMVTT_EN can be used to
disable MEMVTT in sleep.
Okay to turn off 5V and
leave 1.8V powered in S3.

Memory Vtt Supply
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	31	86	



DDR2 Vref

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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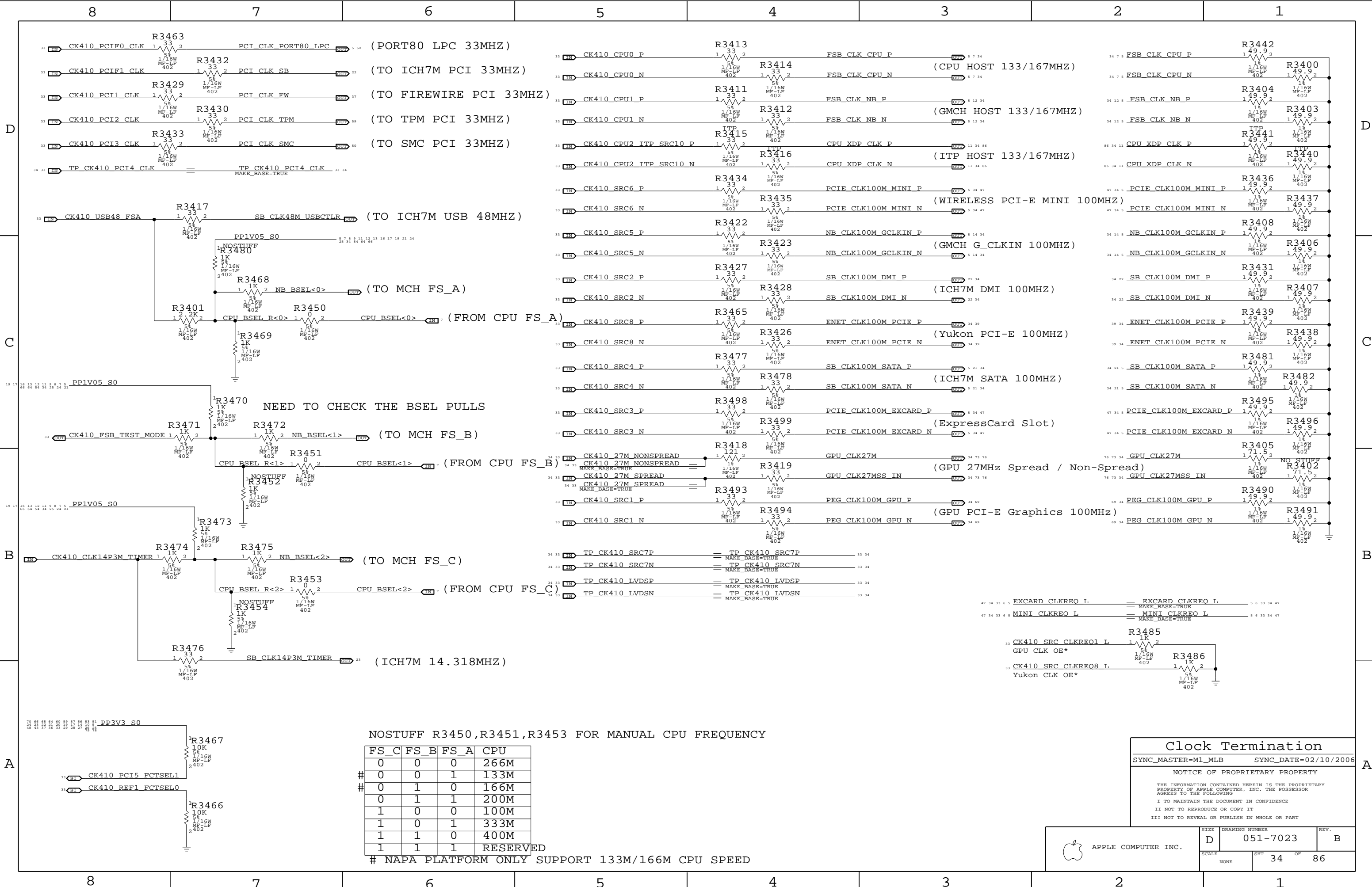
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHT 32	OF 86



NOSTUFF R3450, R3451, R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
#	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
#	0	1	1	200M
#	1	0	0	100M
#	1	0	1	333M
#	1	1	0	400M
#	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	
NONE	34	86	

8

7

6

5

4

3

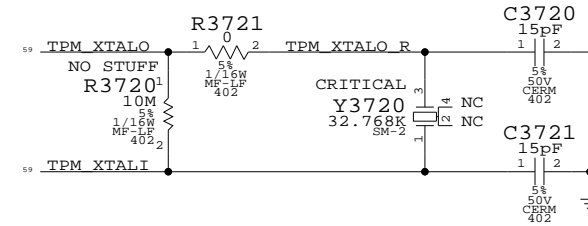
2

1

D

D

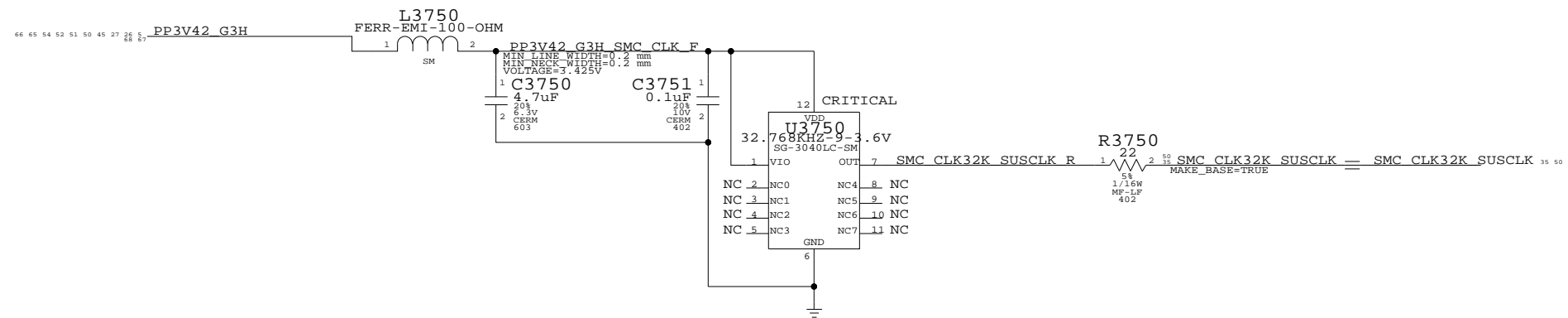
TPM Crystal Circuit



C

C

SMC G3Hot Oscillator



B

B

A

A

8

7

6

5

4

3

2

1

Mobile Clocking

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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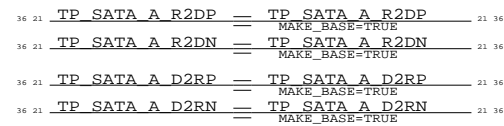
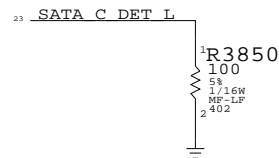
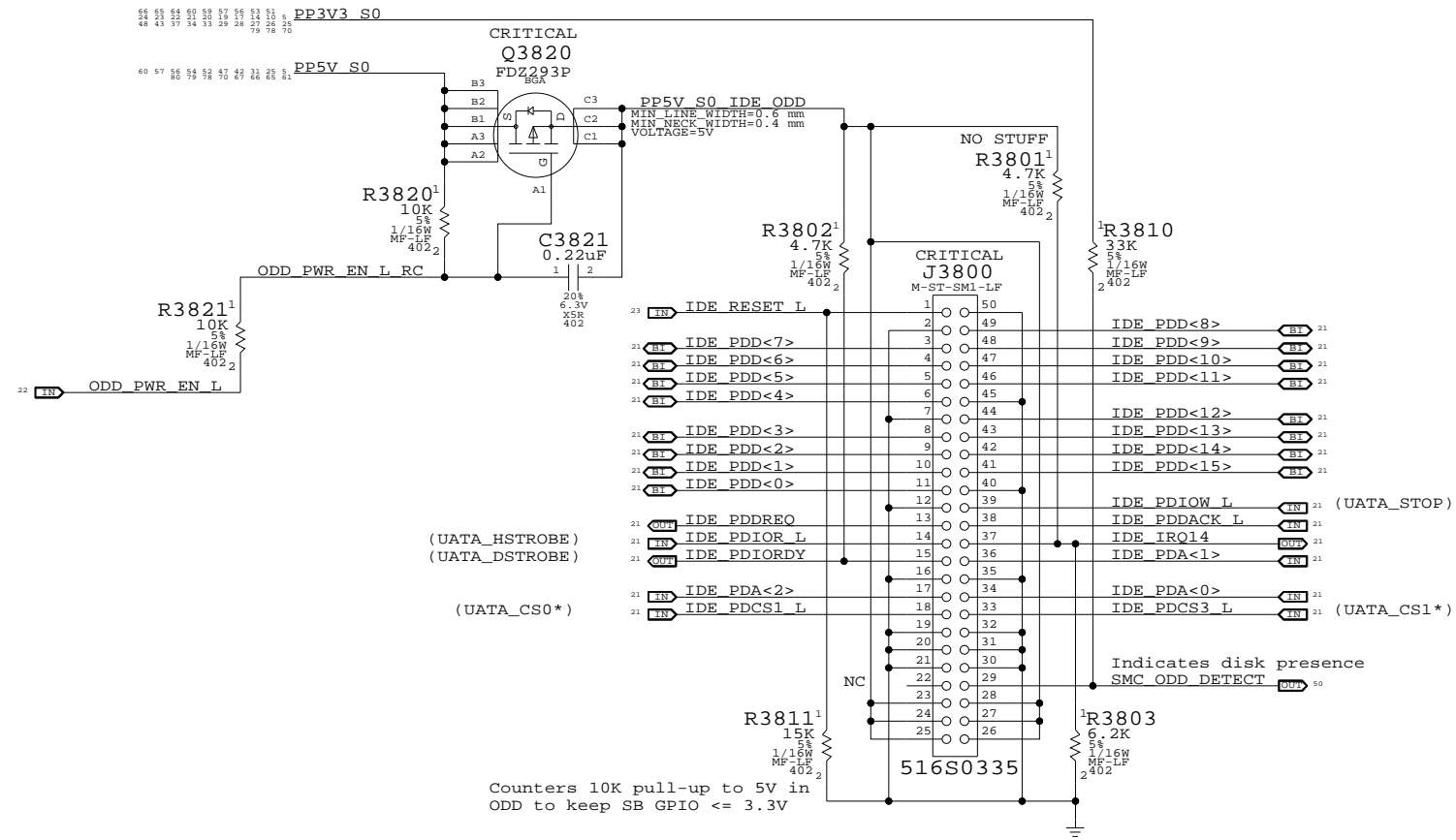
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	35	86	

IDE (ODD) Connector

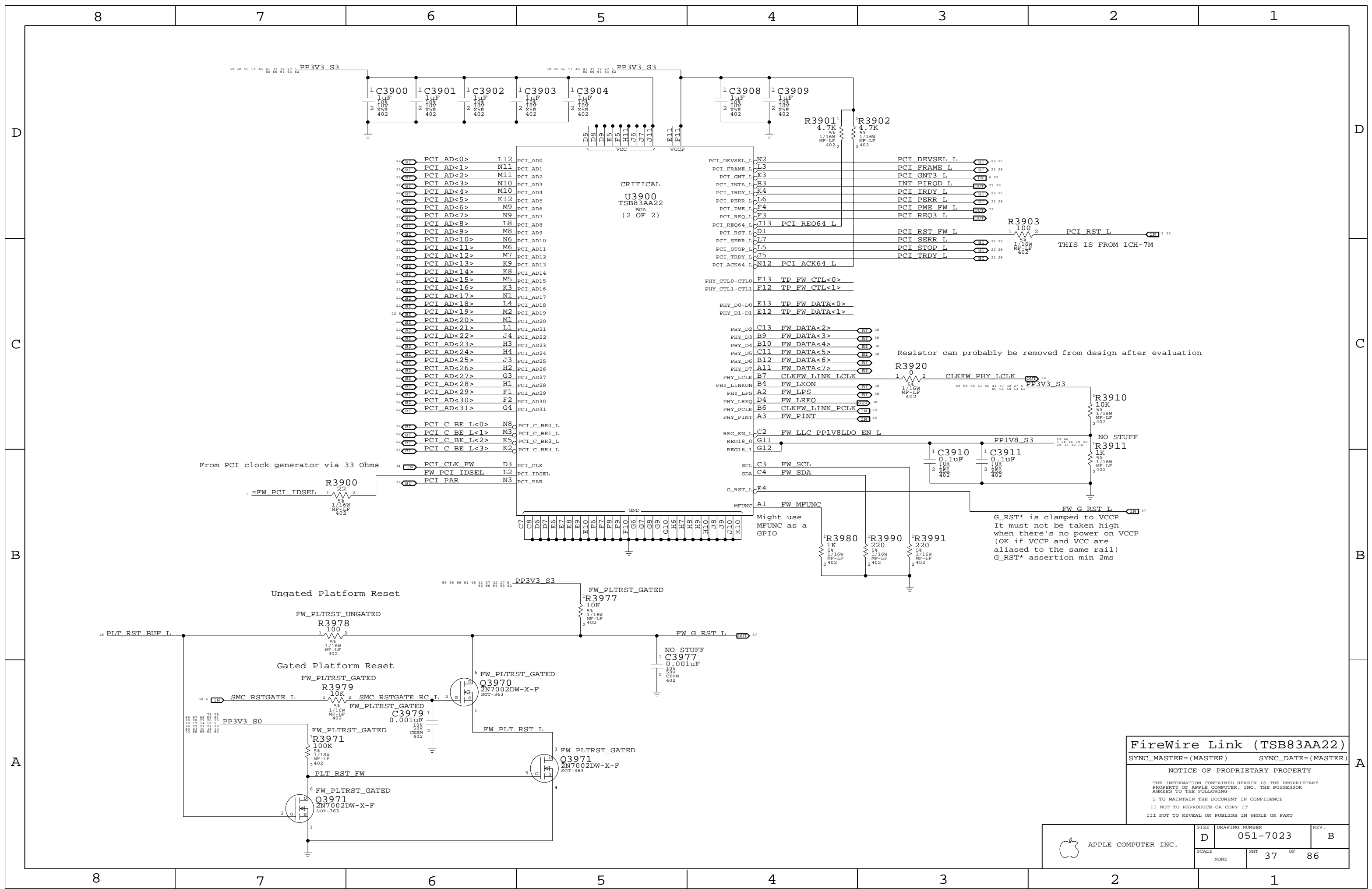


Placement note
Place within 12.7mm
from ball of SB

PATA Connector
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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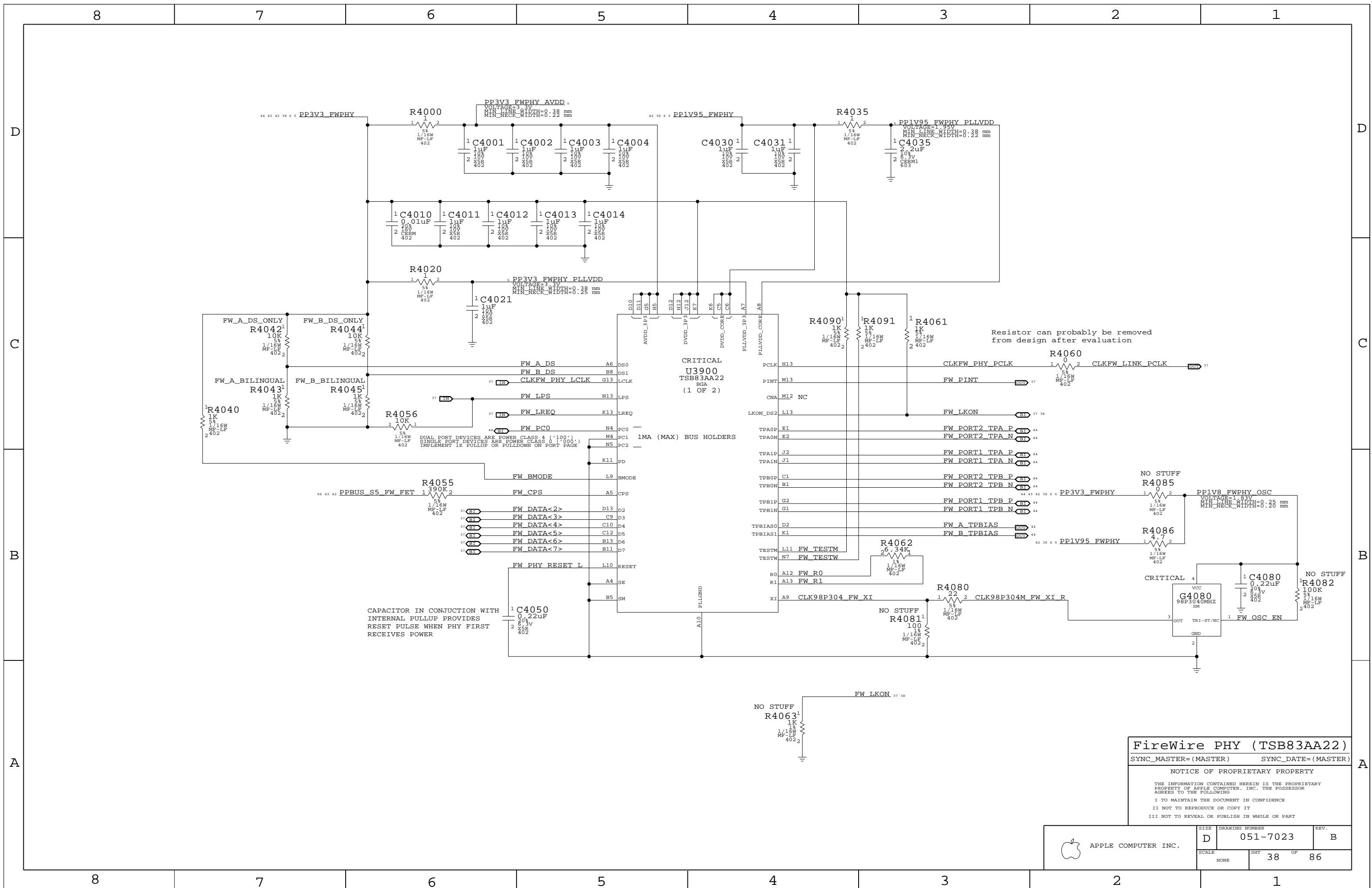
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	36	86	



FireWire Link (TSB83AA22)
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	37	86	



FireWire PHY (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHEET 38	OF 86

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
BY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
ETHERNET	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
PHY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D

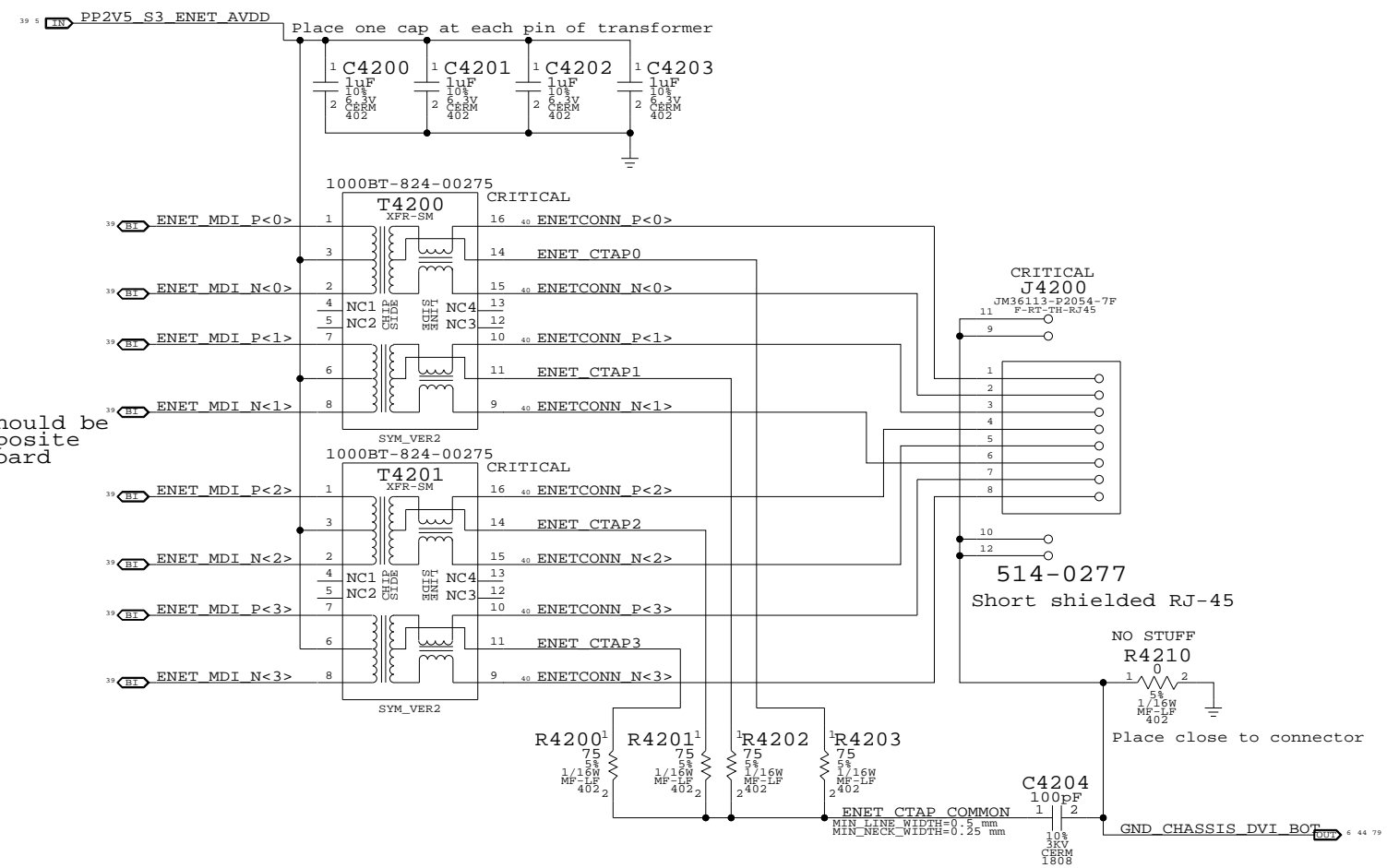
Page Notes

Power aliases required by this page:
 - =PP2V5_ENET
 - =GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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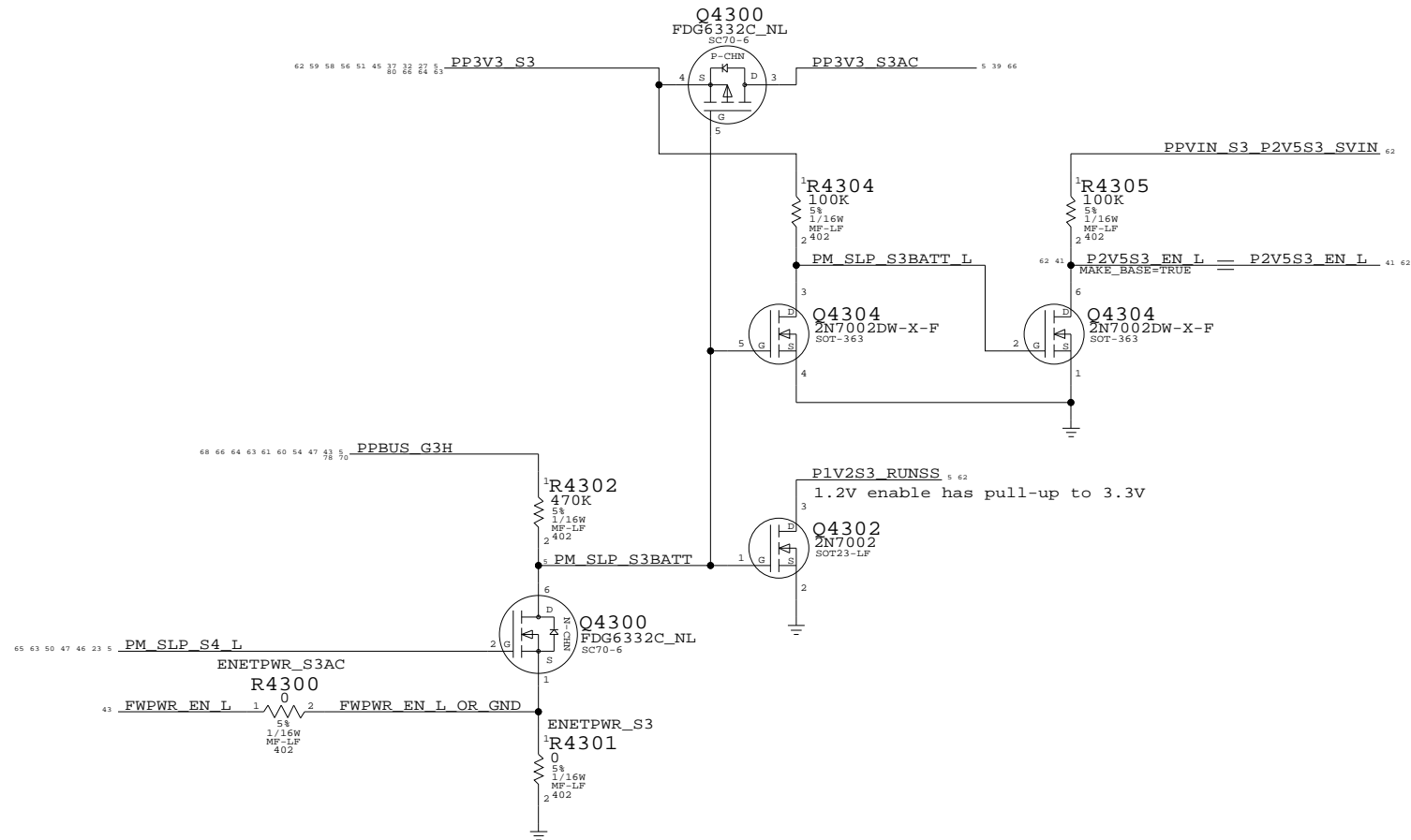
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	40	86	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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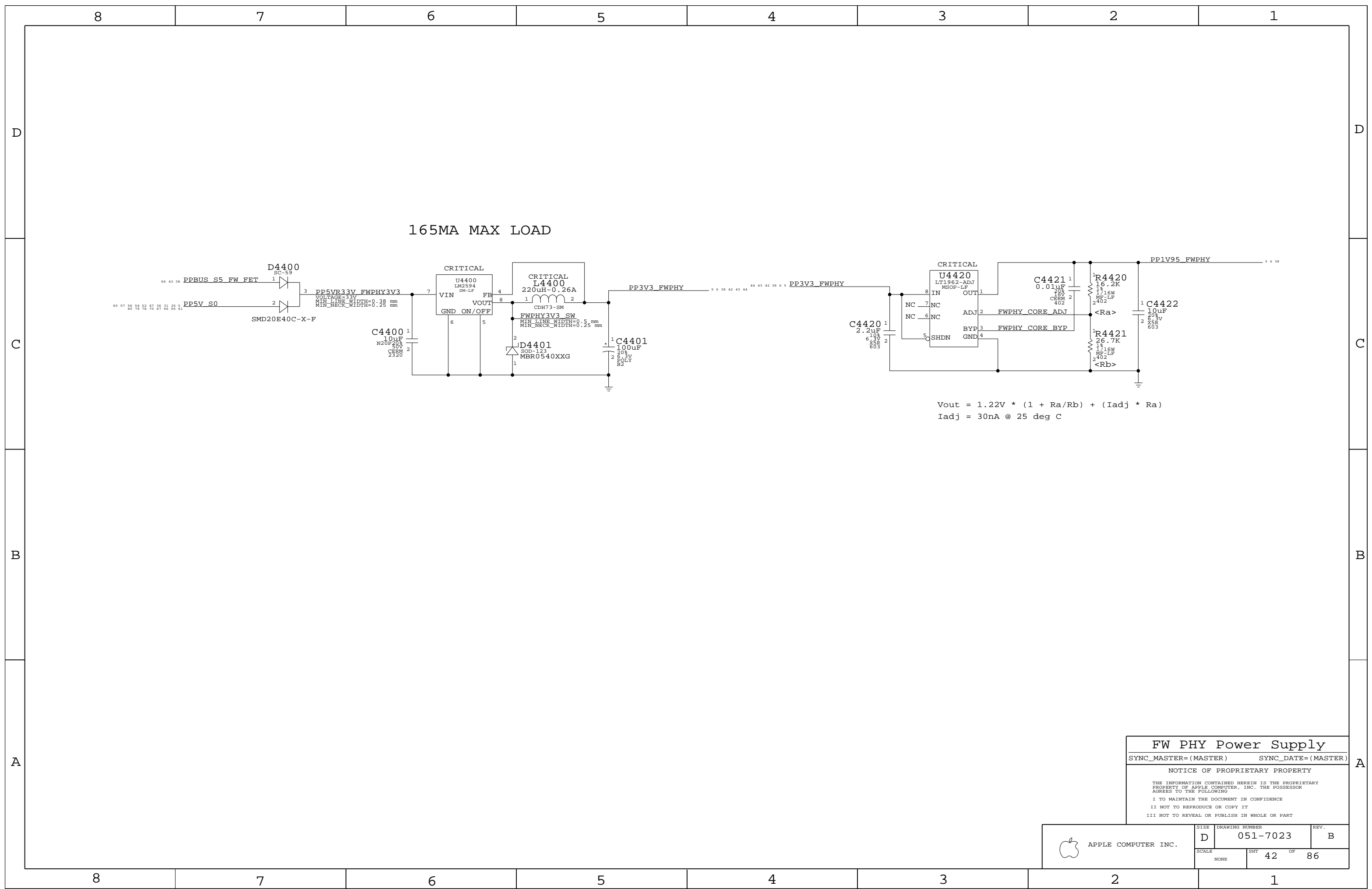
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	D	051-7023	B
SCALE	SHT	OF	
NONE	41	86	



165MA MAX LOAD

$$V_{out} = 1.22V * (1 + R_a/R_b) + (I_{adj} * R_a)$$

$$I_{adj} = 30nA @ 25 \text{ deg C}$$

FW PHY Power Supply
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	
NONE	42	86	

Page Notes

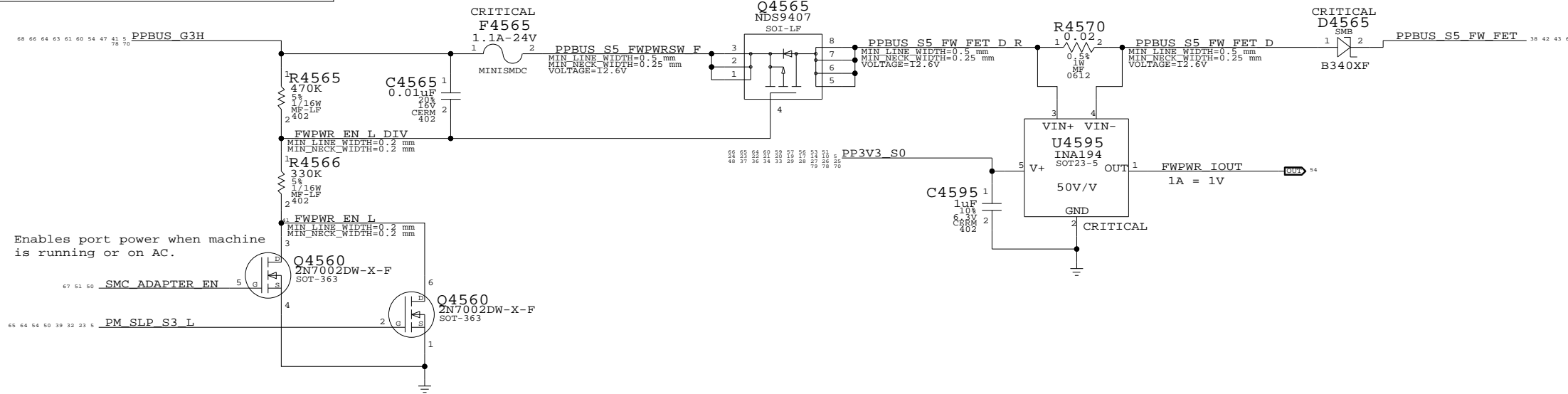
Power aliases required by this page:
 - =PPBUS_S0_FWPWRSW (system supply for bus power)
 - =PP3V3_S0_FWPORPTPWRSW

Signal aliases required by this page:
 - =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
 (NONE)

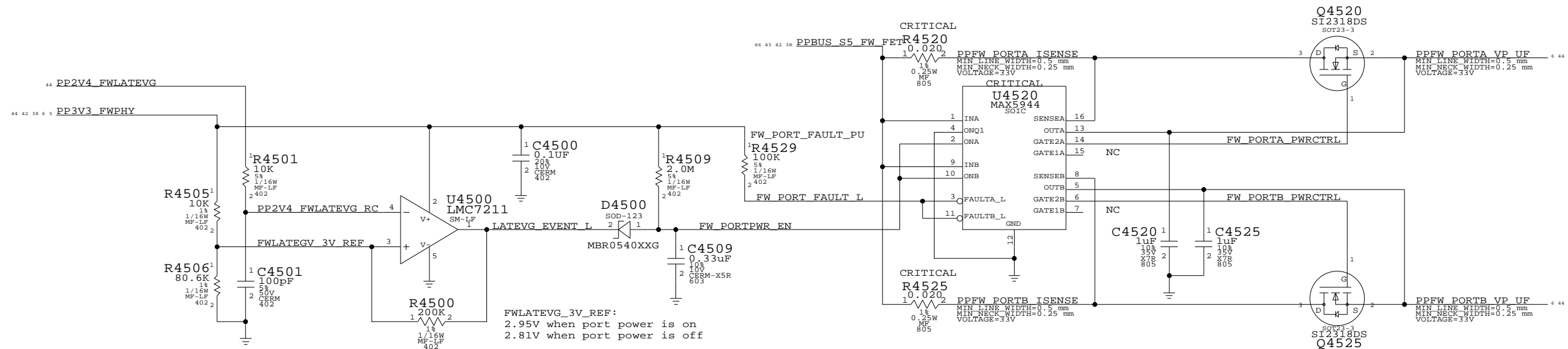
Port Power Switch

FireWire Port Current Sense



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

- 0.020 ohm => 2.4A
- 0.025 ohm => 2A
- 0.030 ohm => 1.66A (Ideal)
- 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/03/2005)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT 43 OF 86		
NONE			

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
PROVIDED	FW	FW_110D
BY	FW	FW_110D
PHY	FW	FW_110D
PAGE	FW	FW_110D

Page Notes

Power aliases required by this page:
 - =PPFW_PORT1
 - =PP3V3_S5_FWLATEVG
 - =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

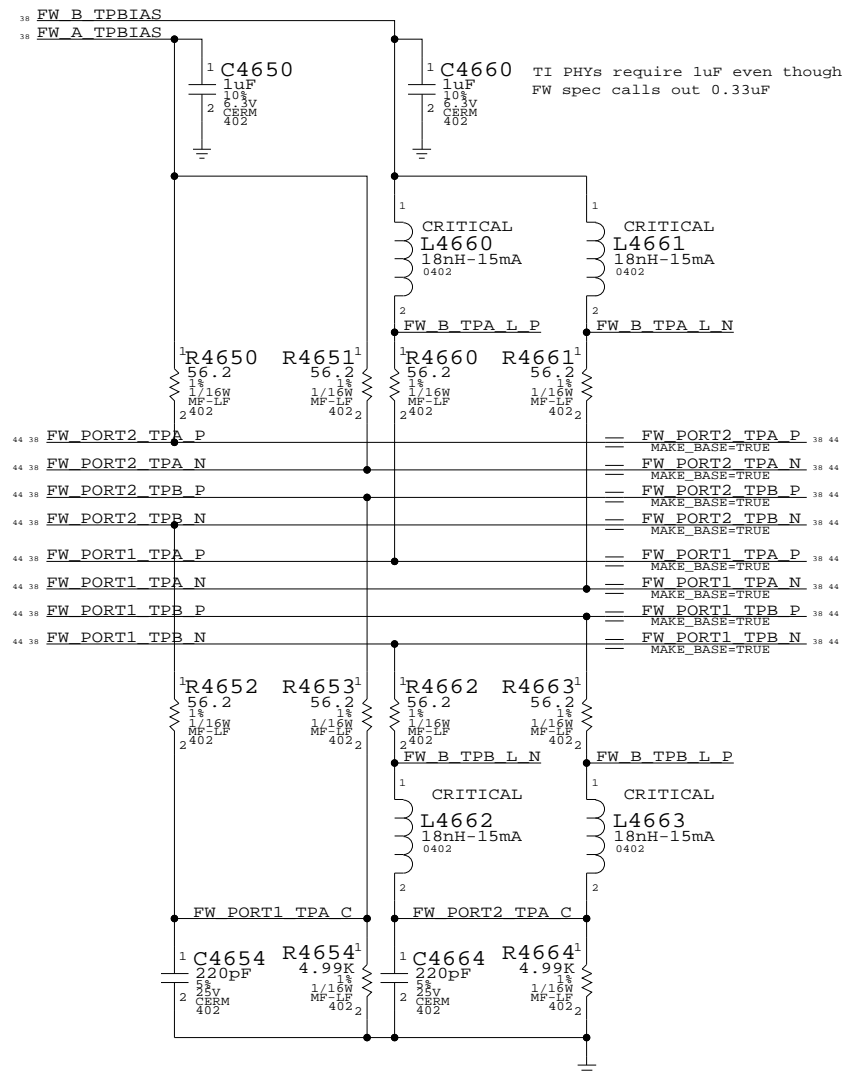
AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

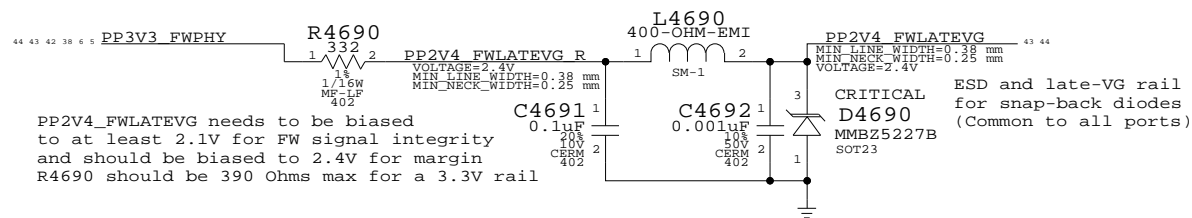
BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Termination

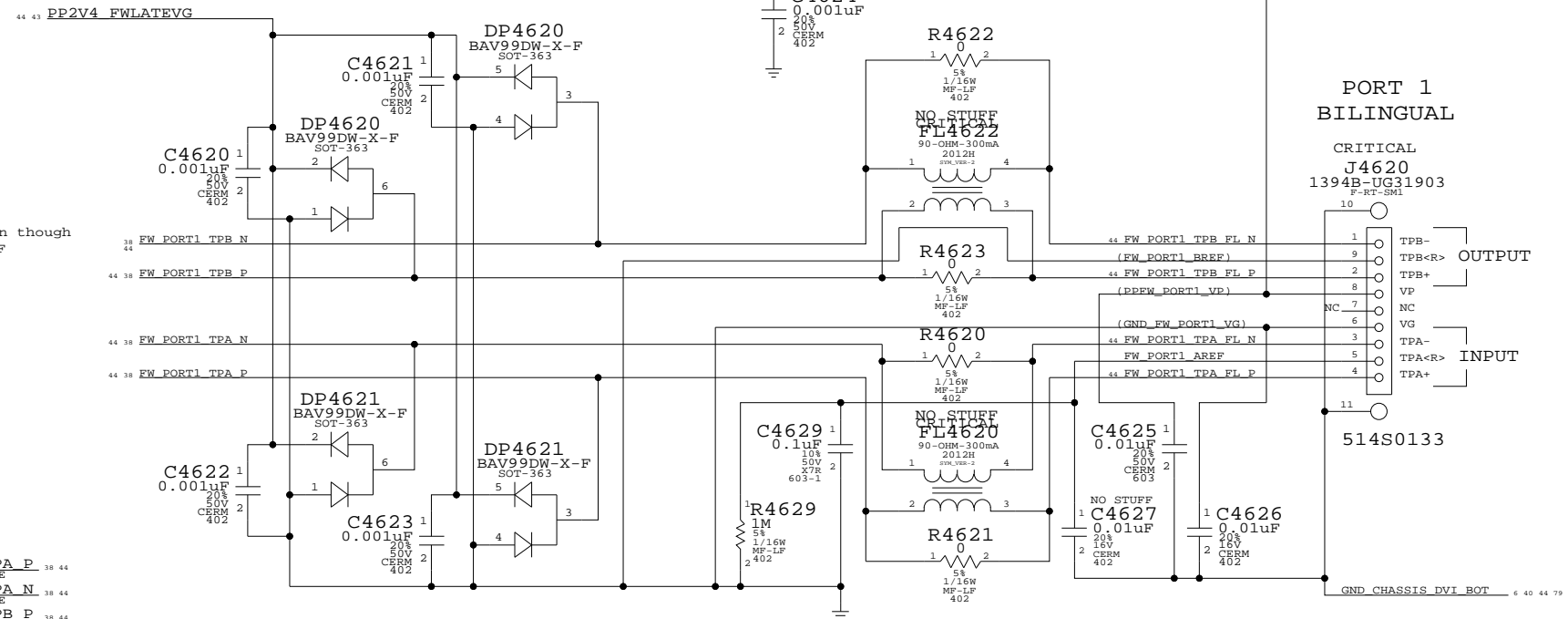
Place close to FireWire PHY



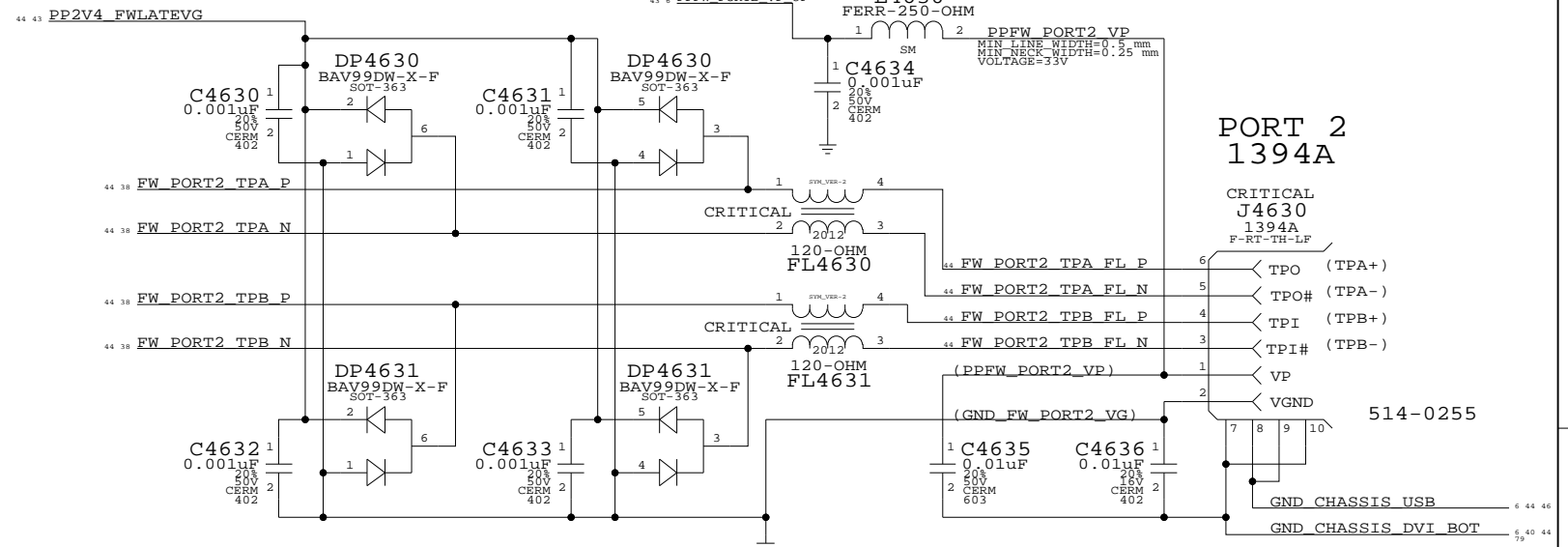
Late-VG Protection Power



"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection



FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE	SHT	OF
NONE	44	86



APPLE COMPUTER INC.

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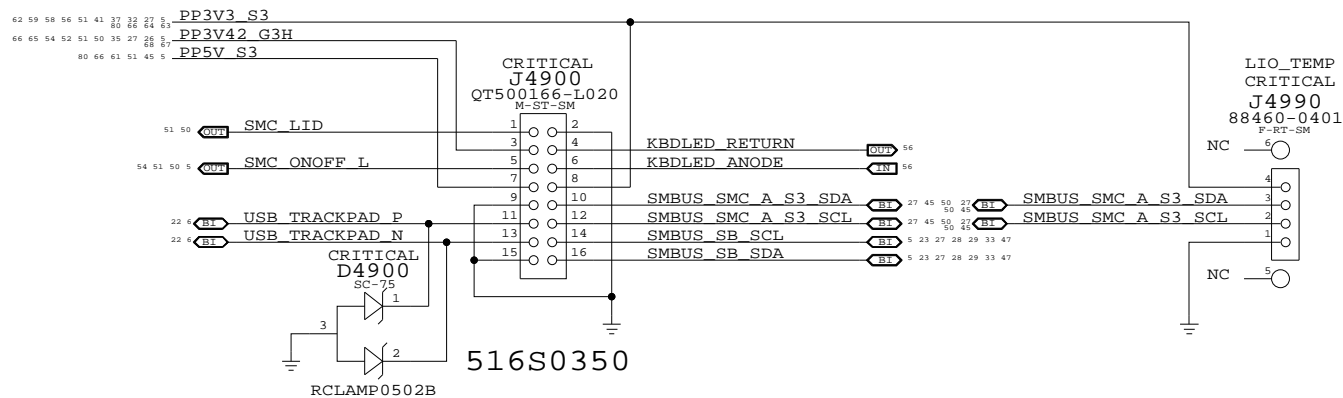
2

1

D

D

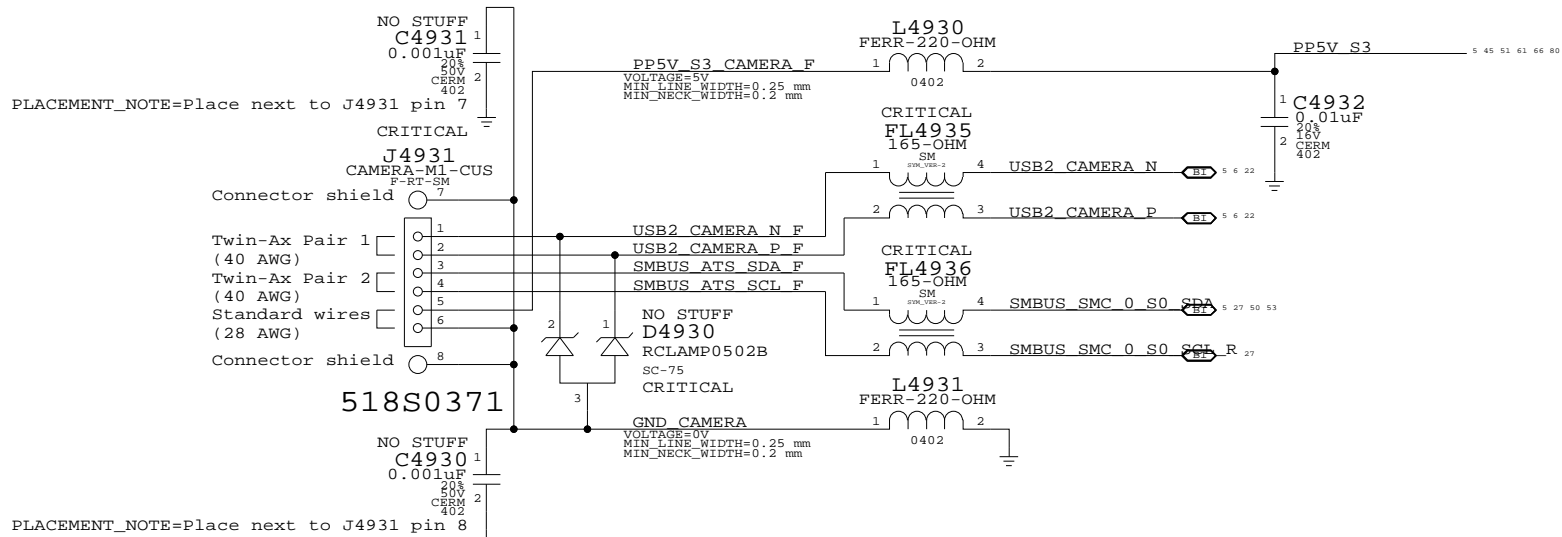
Top-Case Connector LIO Temp Sensor Connector



C

C

Camera Connector



B

B

A

A

Internal USB Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	B
SCALE	SHT	OF	
NONE	45	86	

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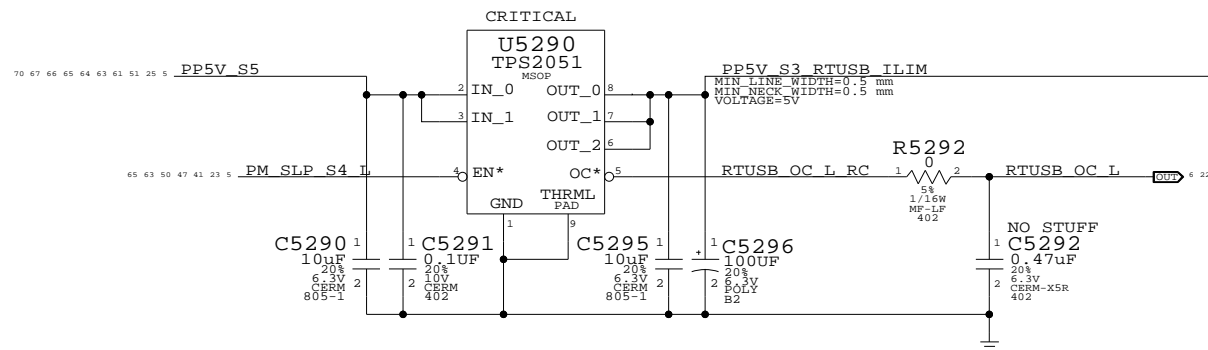
4

3

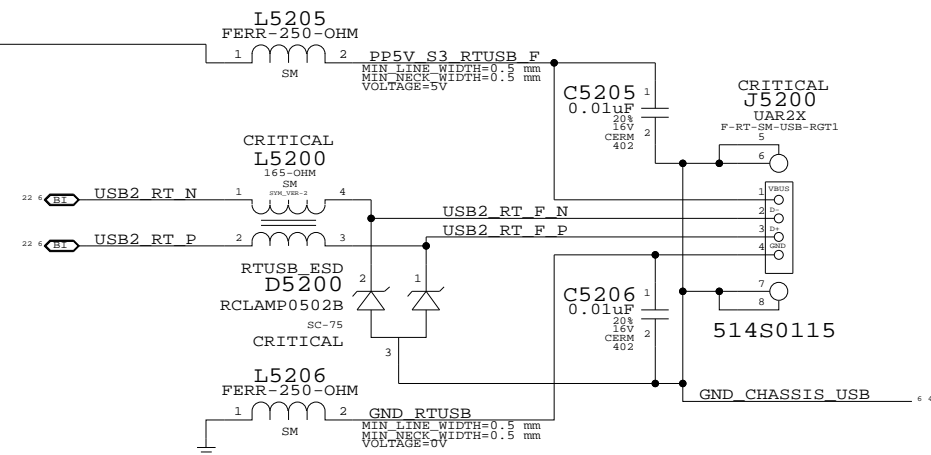
2

1

Port Power Switch



Right USB Port

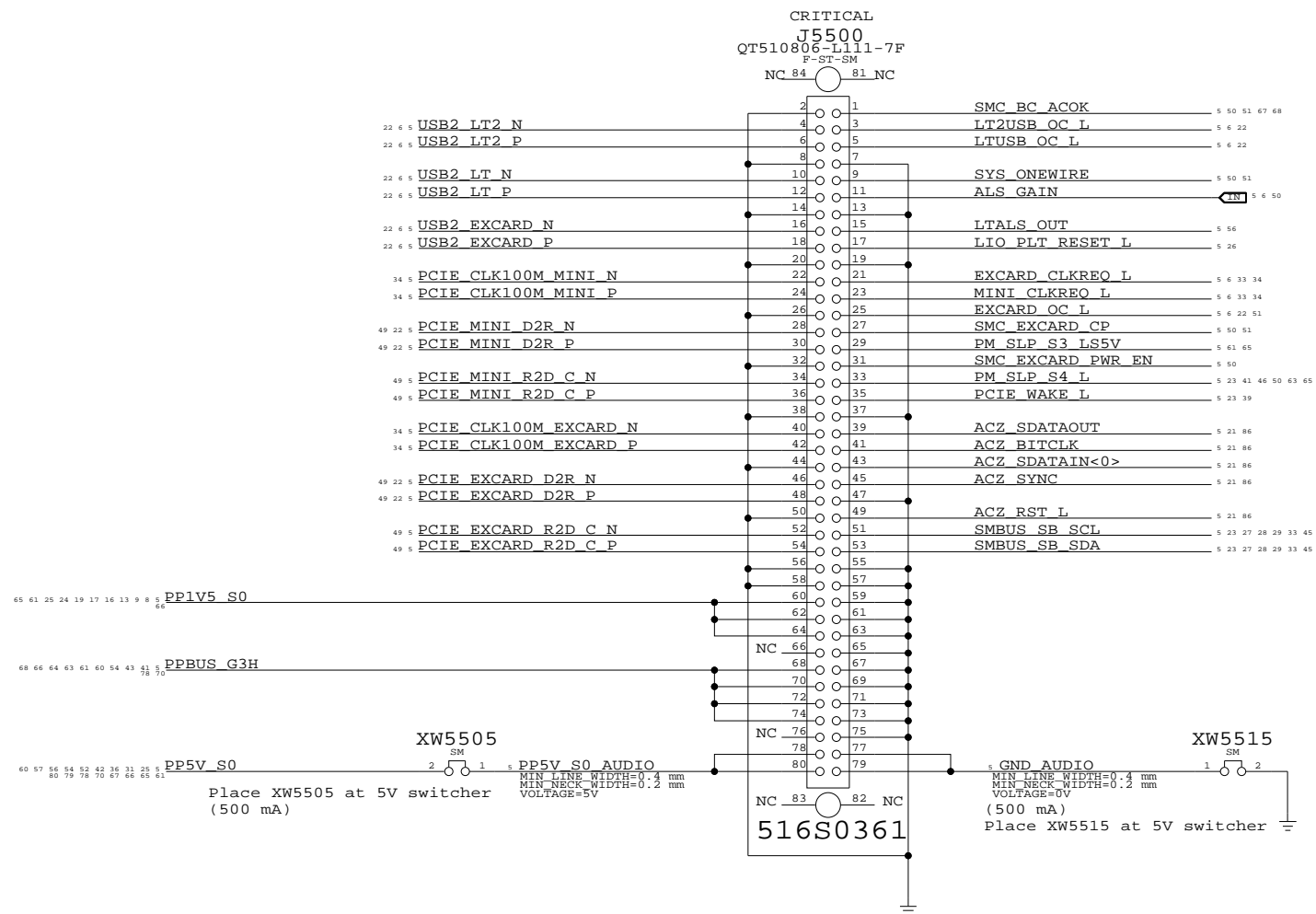


Place L5200, L5205 and L5206 across moat

External USB Connector
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	46	86	

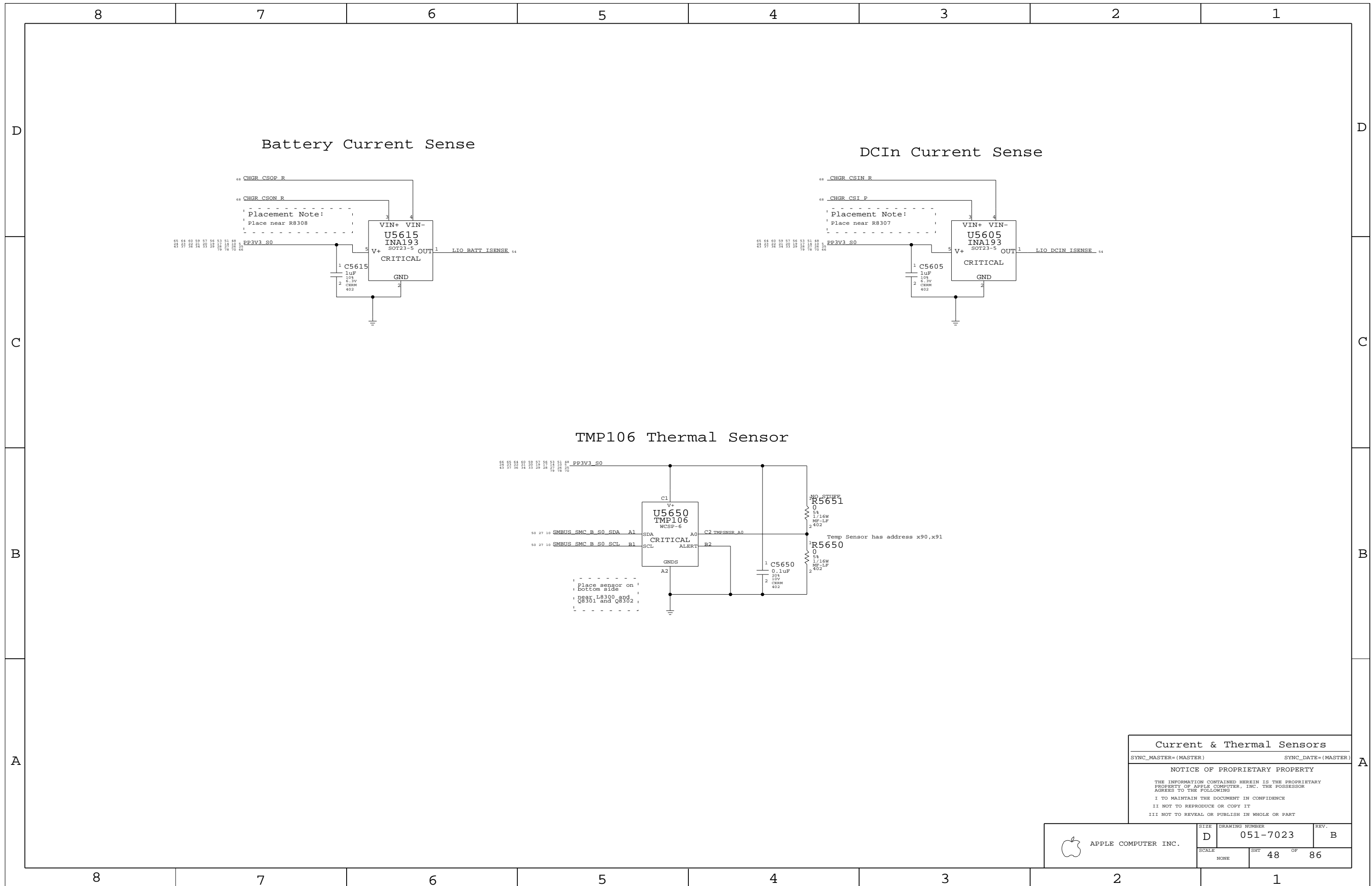
Left I/O Board Connector



Left I/O Board Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7023	B
SCALE	SHT	OF	
NONE	47	86	



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7023	B
SCALE	SHT	OF	
NONE	48	86	

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D

C

C

B

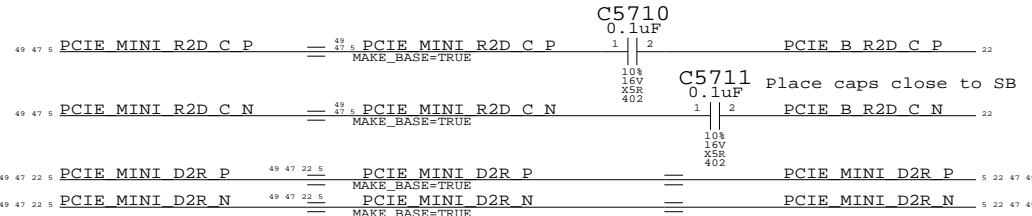
B

A

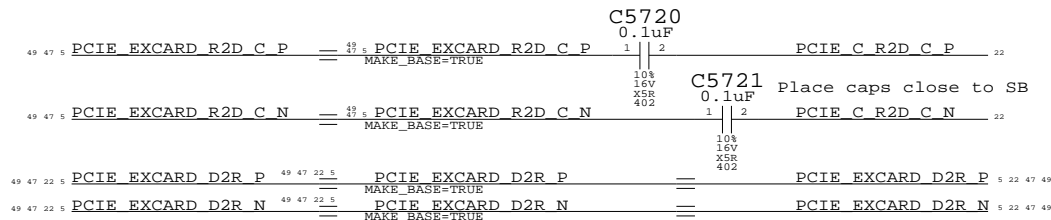
A

PCI-E x1 Port "A" = Ethernet (Yukon)

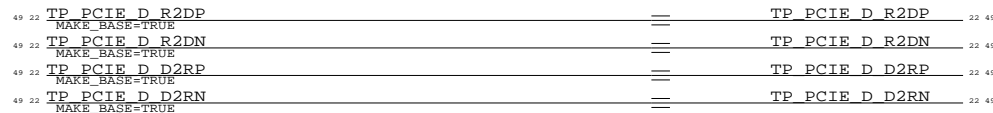
PCI-E x1 Port "B" = PCI-E Mini Card



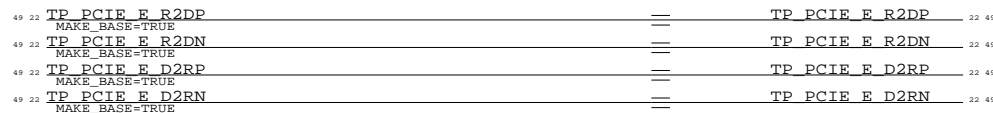
PCI-E x1 Port "C" = ExpressCard



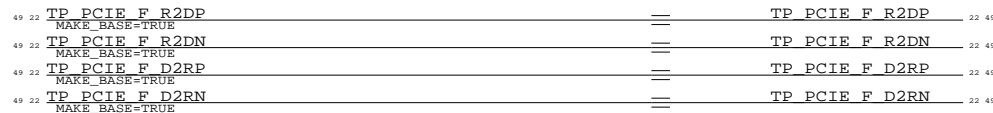
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	B
SCALE	SHT	OF	
NONE	49	86	

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1

UNUSED PINS HAVE THE FORMAT
 THEY ARE WHERE BY SOFTWARE THEY
 CAN BE LEFT NO CONNECTED.

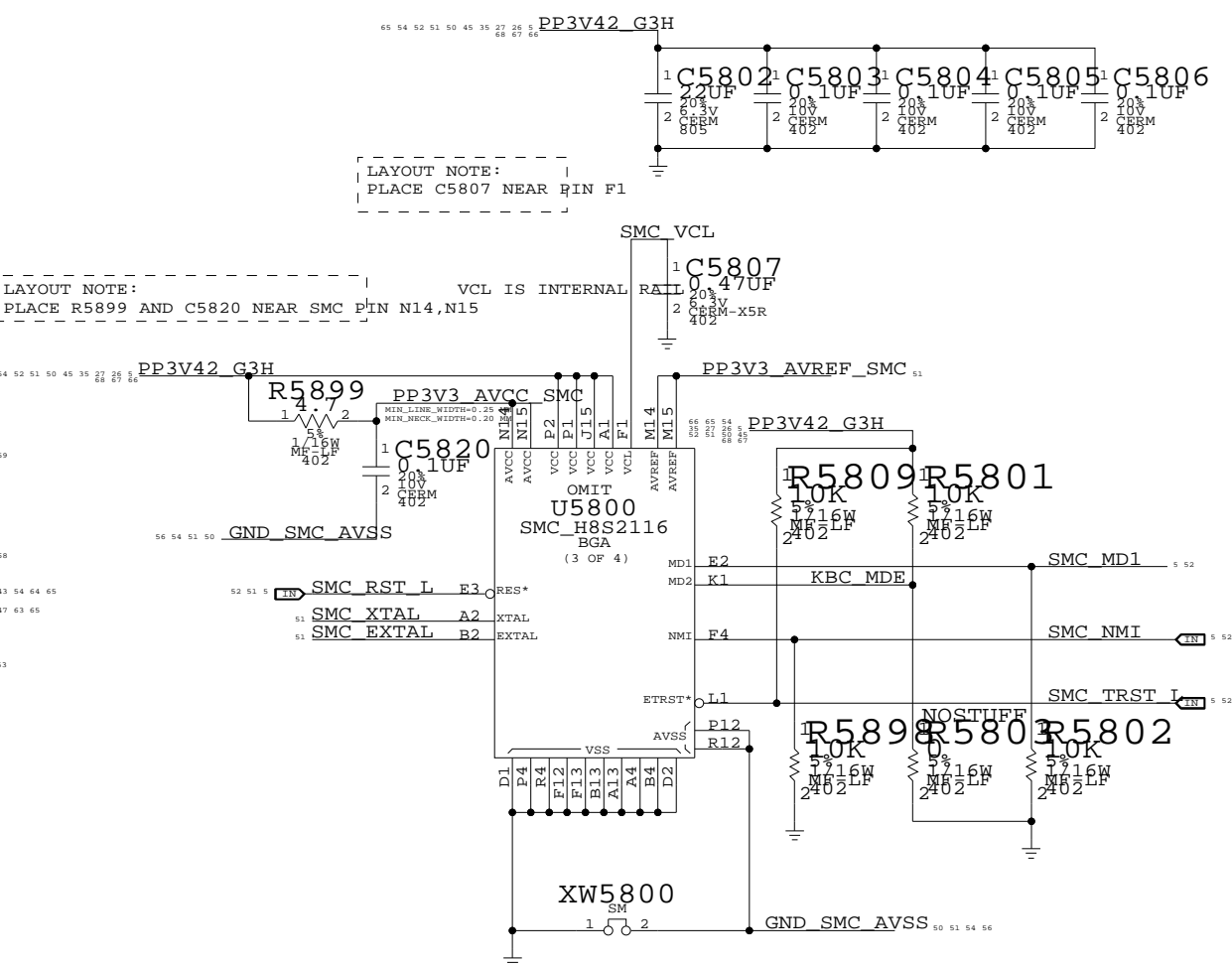
37 5	PM LAN ENABLE	B12	P10	OMIT	U5800	P60/KIN0*	L13	SMC PM G2 EN	51
37 6	SMC RSTGATE L	C13	P11	OMIT	U5800	P61/KIN1*	L14	SMC ADAPTER EN	51 67
65 26	ALL SYS PWRGD	A15	P12	OMIT	U5800	P62/KIN2*	L15	SPI ARB	22
65 27	RSMRST PWRGD	B14	P13	OMIT	U5800	P63/KIN3*	K12	SPI SCLK	22 55
23	SMC SB NMI	B15	P14	OMIT	U5800	P64/KIN4*	K13	SPI SI	22 55
23 5	PM RSMRST L	C14	P15	OMIT	U5800	P65/KIN5*	K14	SPI SO	22 55
60 5	IMVP VR_ON	D12	P16	OMIT	U5800	P66/IRQ6*/KIN6*	J12	SMC PROCHOT 3 3	51
23	PM_PWRBTN L	C15	P17	OMIT	U5800	P67/IRQ7*/KIN7*	J13	FWH INIT L	51 21 51 52
51	TP SMC P20	D13	P20	OMIT	U5800	P70/AN0	N12	SMC CPU ISENSE	54
51	TP SMC P21	D14	P21	OMIT	U5800	P71/AN1	R13	SMC CPU VSENSE	54
51	TP SMC P22	D15	P22	OMIT	U5800	P72/AN2	P13	SMC GPU ISENSE	54
51	TP SMC P23	E12	P23	OMIT	U5800	P73/AN3	R14	SMC GPU VSENSE	54
68 51	SMC BATT TRICKLE EN	E14	P24	OMIT	U5800	P74/AN4	P14	SMC DCIN ISENSE	54
68 51	SMC BATT_CHG EN	E15	P25	OMIT	U5800	P75/AN5	R15	SMC PBUS VSENSE	54
51	TP SMC P26	E13	P26	OMIT	U5800	P76/AN6	N13	SMC BATT ISENSE	54
51	TP SMC P27	F14	P27	OMIT	U5800	P77/AN7	P15	SMC FWIRE ISENSE	54
59 52 21 5	LPC AD<0>	D9	P30/LAD0	OMIT	U5800	P80/PME*	C7	SMC WAKE SCI L	23
59 52 21 5	LPC AD<1>	C9	P31/LAD1	OMIT	U5800	P81/GA20	A7	SMC TPM GPIO	23
59 52 21 5	LPC AD<2>	A9	P32/LAD2	OMIT	U5800	P82/CLKRUN*	B7	PM_CLKRUN L	5 23 52 59
59 52 21 5	LPC AD<3>	B9	P33/LAD3	OMIT	U5800	P83/LPCPD*	D6	PM_SUS_STAT L	5 23 51 52 59
59 52 21 5	LPC FRAME L	D8	P34/LFRAME*	OMIT	U5800	P84/IRQ3*/TXD1	C6	SC TX L	51
26 5	SMC LRESET L	C8	P35/LRESET*	OMIT	U5800	P85/IRQ4*/RXD1	A6	SC RX L	51
34	PCI_CLK_SMC	A8	P36/LCLK	OMIT	U5800	P86/IRQ5*/SCL1/SCL1	B6	SMBUS_SMC_BSB_S0	27
59 52 23 5	INT_SERIRQ	D7	P37/SERIRQ	OMIT	U5800	P90/IRQ2*	K4	SMC_ONOFF L	5 45 51 54
51	TP_SMC_XDP_TMS	A5	P40/TMIO	OMIT	U5800	P91/IRQ1*	J2	SMC_BC_ACOK	5 47 51 67 68
51	SMC_SYS_LED_16B	B5	P41/TMO0	OMIT	U5800	P92/IRQ0*	J1	SMC_BS_ALERT L	5 47 51 67 68
27	SMBUS_SMC_BSB_SDA	D5	P42/SDA1	OMIT	U5800	P93/IRQ12*	J3	PM_SLP_S3 L	5 23 32 39 43 54 64 65
51	SMC_TPM_PP	C3	P43/TM11/EXSCK1	OMIT	U5800	P94/IRQ13*	J4	PM_SLP_S4 L	5 23 41 46 47 63 65
51	TP_SMC_XDP_TRST L	B1	P44/TMO1	OMIT	U5800	P95/IRQ14*	H2	PM_SLP_S5 L	5 23 51
51	TP_SMC_XDP_TCK	C2	P45	OMIT	U5800	P96/EXCL	H1	SMC_CLK32K_SUSC	35
51	TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	OMIT	U5800	P97/IRQ15*/SDA0	G2	SMBUS_SMC_0_S0	5 27 45 53
56	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	OMIT	U5800				
52 51 5	SMC_TX L	G1	P50	OMIT	U5800				
52 51 5	SMC_RX L	G4	P51	OMIT	U5800				
53 27 5	SMBUS_SMC_0_S0_SCL	F2	P52/SCL0	OMIT	U5800				

21	SMC_RCIN L	R3	PA0/KIN8*/PA2CC	OMIT	U5800	PR0	M3	SMC_CASE_OPEN	51
52 22 5	BOOT_LPC_SPI L	P3	PA1/KIN9*/PA2BD	OMIT	U5800	PR1*/ETCK	M2	SMC_TCK	5 51 52
26 23 5	PM_SYSRST L	R2	PA2/KIN10*/PS2AC	OMIT	U5800	PR2*/ETDI	M1	SMC_TDI	5 51 52
59 51	SMC_TPM_RESET L	N3	PA3/KIN11*/PS2AD	OMIT	U5800	PR3*/ETDO	L4	SMC_TDO	5 51 52
51 28 28 14	PM_EXTS L	R1	PA4/KIN12*/PS2BC	OMIT	U5800	PR4*/ETMS	L2	SMC_TMS	5 51 52
27	PM_THRM L	N2	PA5/KIN13*/PS2BD	OMIT	U5800	PF0/IRQ8*/PWM2	M7	TP_SMC_PF0	51
47	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	OMIT	U5800	PF1/IRQ9*/PWM3	P6	TP_SMC_PF1	51
23	PM_BATLOW L	N1	PA7/KIN15*/PS2CD	OMIT	U5800	PF2/IRQ10*/TMOY	R6	SMC_LID	45 51
23	SMC_EXTSMI L	B10	PB0/LSMI*	OMIT	U5800	PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET 3	51
23	SMC_RUNTIME_SCI L	A10	PB1/LSCI	OMIT	U5800	PF4/PWM4	M6	SMC_BATT_ISET	68
36	SMC_ODD_DETECT	D10	PB2	OMIT	U5800	PF5/PWM5	R5	TP_SMC_BATT_VSET	51
54	ISENSE_CAL_EN	A11	PB3	OMIT	U5800	PF6/PWM6	P5	SMC_SYS_ISET	68
51 47 5	SMC_EXCARD_CP	B11	PB4	OMIT	U5800	PF7/PWM7	N5	TP_SMC_SYS_VSET	51
47 5	SMC_EXCARD_PWR_EN	C11	PB5	OMIT	U5800	PG0/EXIRQ8*/TMIX	P9	SPI_CE L	22 55
51	SMC_EXCARD_OC L	A12	PB6	OMIT	U5800	PG1/EXIRQ9*/TMIX	R9	SMC_XDP_TCK 3 3	51
51	SMC_XDP_TDO 3 3	D11	PB7	OMIT	U5800	PG2/EXIRQ10*/SDA2	N9	SMBUS_SMC_BSA_S0	5 27 67
57	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	OMIT	U5800	PG3/EXIRQ11*/SCL2	P8	SMBUS_SMC_BSA_S0	5 27 67
57	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	OMIT	U5800	PG4/EXIRQ12*/EXSDAA	R8	SMBUS_SMC_A_S3	27 45
51	TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	OMIT	U5800	PG5/EXIRQ13*/EXSCLA	M8	SMBUS_SMC_A_S3	27 45
51	TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	OMIT	U5800	PG6/EXIRQ14*/EXSDAB	P7	SMBUS_SMC_B_S0	10 27 48
57	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	OMIT	U5800	PG7/EXIRQ15*/EXSCLB	R7	SMBUS_SMC_B_S0	10 27 48
51	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	OMIT	U5800	PH0/EXIRQ6*	E1	SMC_PROCHOT	51
51	TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	OMIT	U5800	PH1/EXIRQ7*	F3	SMC_THRMTRIP	51
51	TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	OMIT	U5800	PH2/FWE	K2	SMC_FWE	51
56	SMS_X_AXIS	M11	PD0/AN8	OMIT	U5800	PH3/EXEXCL	D4	SMS_INT L	5 6 47
56	SMS_Y_AXIS	F11	PD1/AN9	OMIT	U5800				
56	SMS_Z_AXIS	R11	PD2/AN10	OMIT	U5800				
51	TP_SMC_ANALOG_ID	N11	PD3/AN11	OMIT	U5800				
54 51	SMC_P1V05S0_ISENSE	P10	PD4/AN12	OMIT	U5800				
54 51	SMC_P1V8S3_ISENSE	R10	PD5/AN13	OMIT	U5800				
56	ALS_LEFT	N10	PD6/AN14	OMIT	U5800				
56	ALS_RIGHT	M10	PD7/AN15	OMIT	U5800				

OMIT

U5800
 SMC_H8S2116
 BGA
 (4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		



SMC

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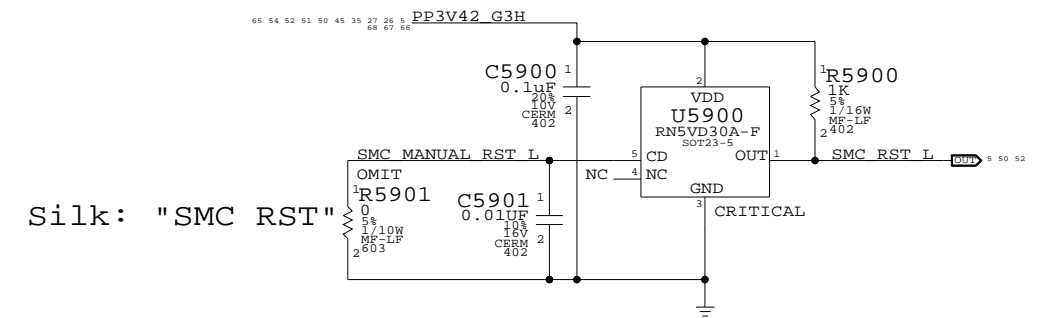
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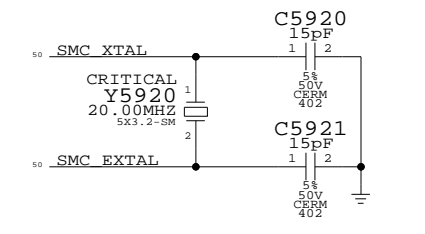
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT	OF	
NONE	50	86	

SMC Reset Button / Brownout Detect

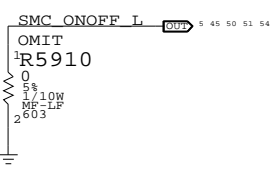


Silk: "SMC_RST"

SMC Crystal Circuit

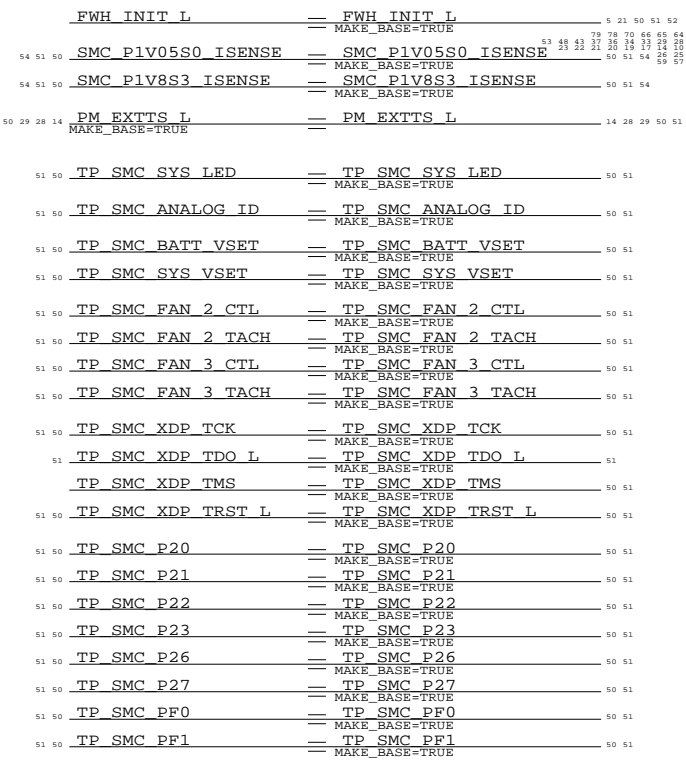
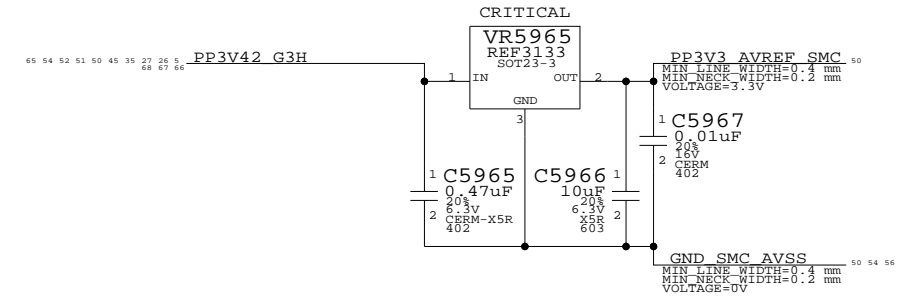


Debug Power Button

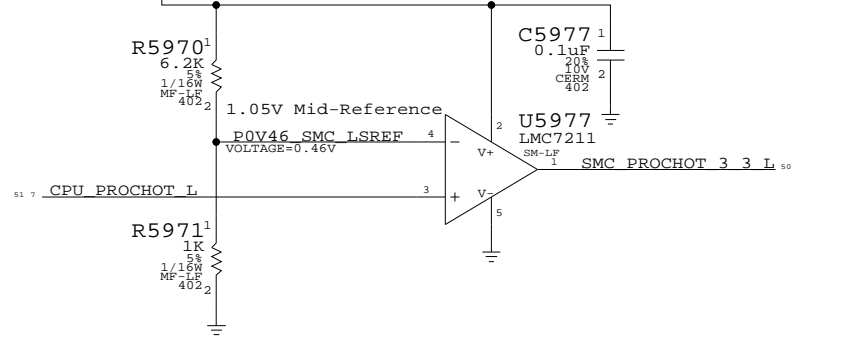


Silk: "PWR_BTN"

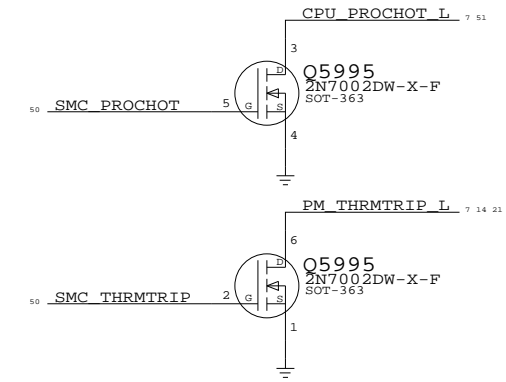
SMC AVREF Supply



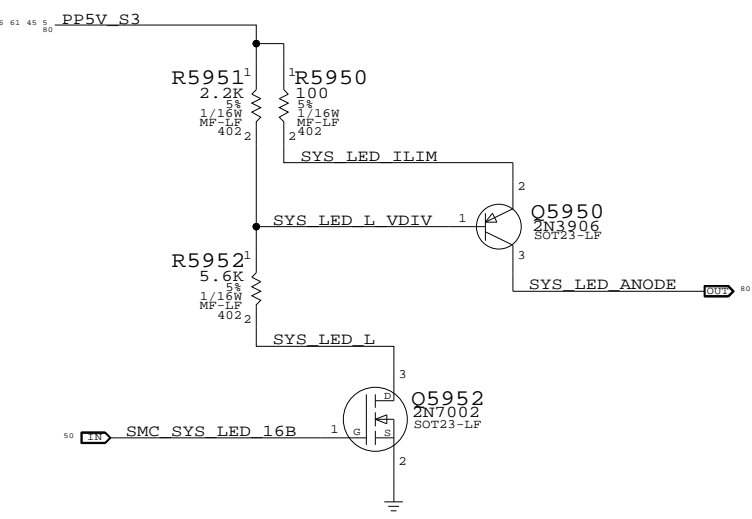
SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting

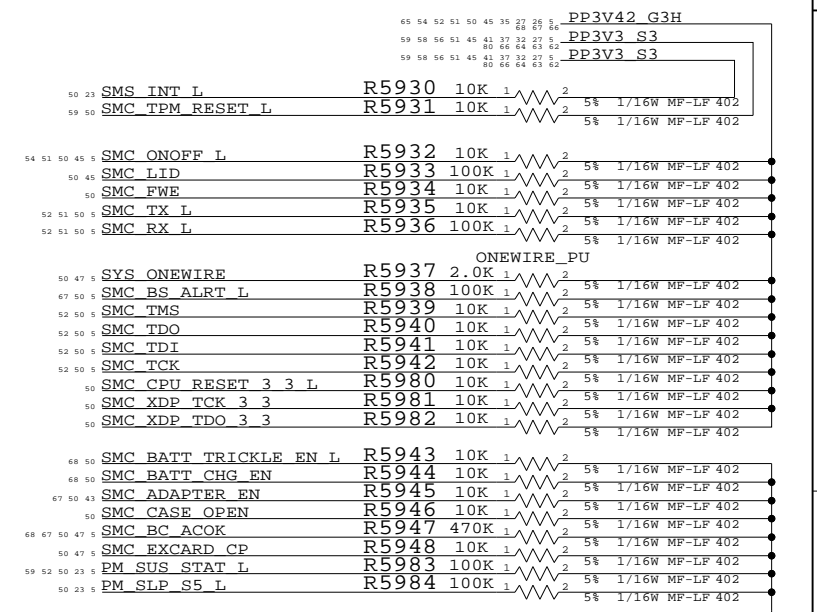
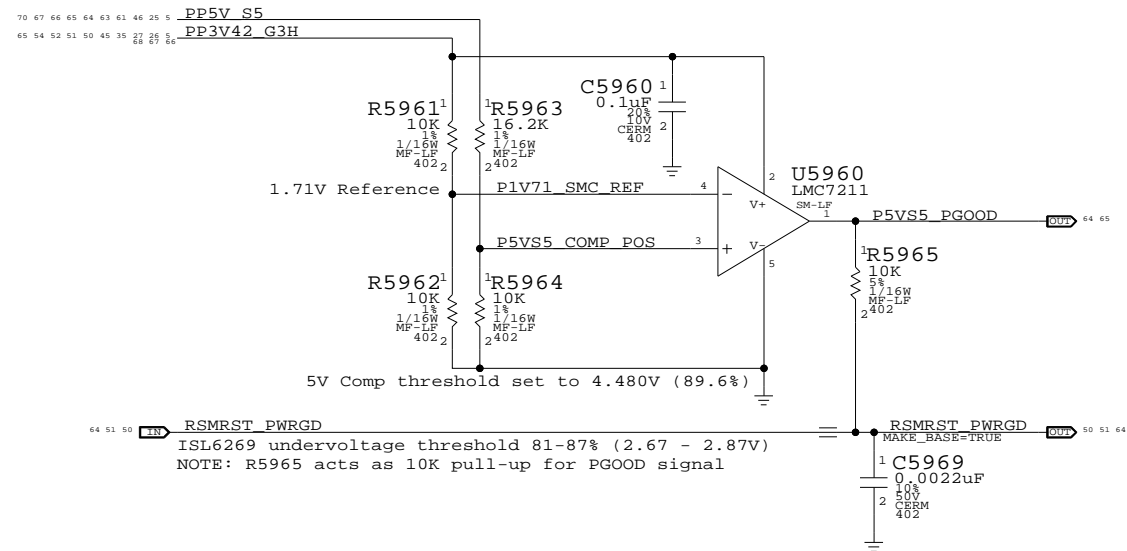


System (Sleep) LED Circuit

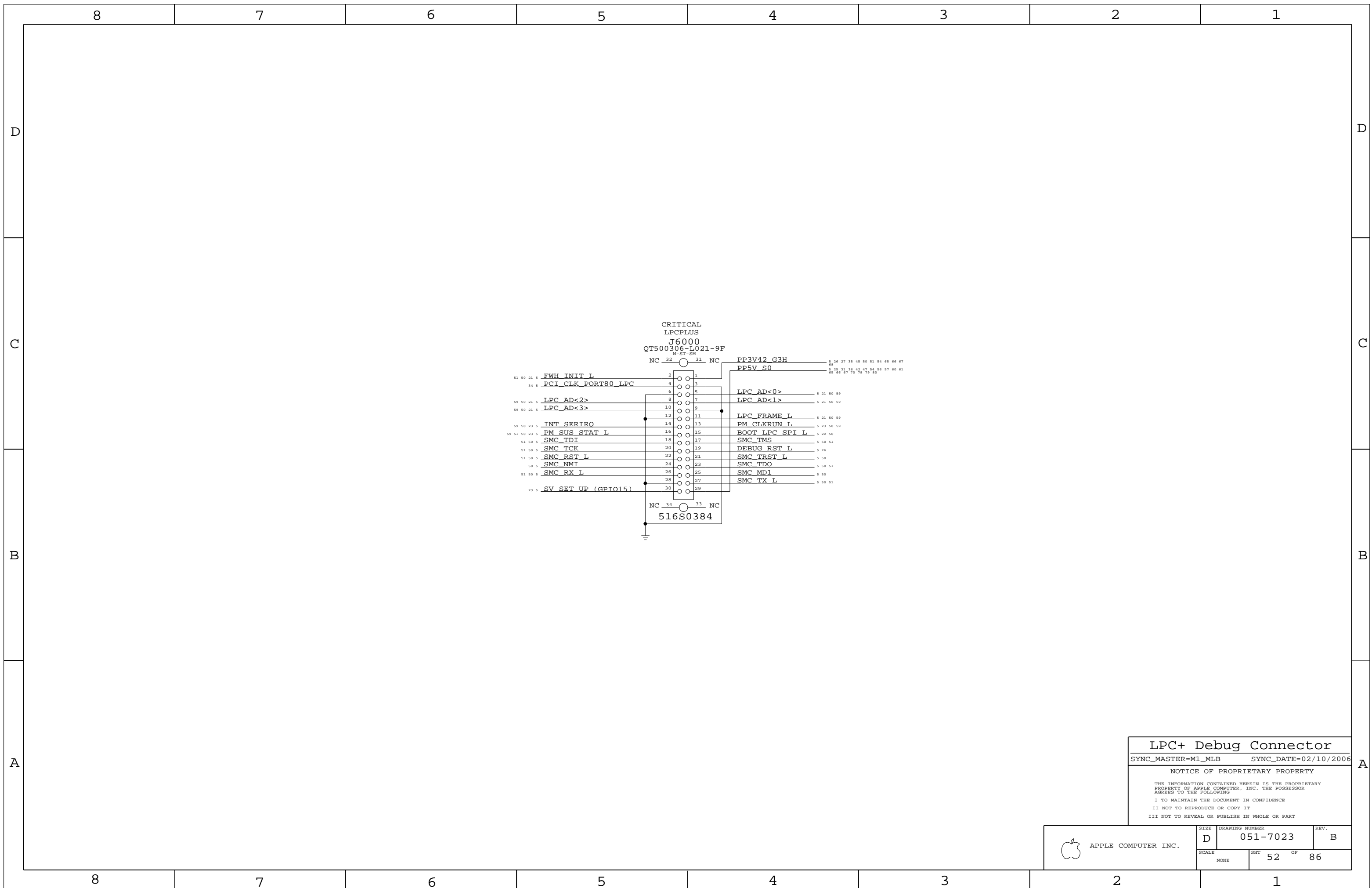


SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC Support
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LPC+ Debug Connector

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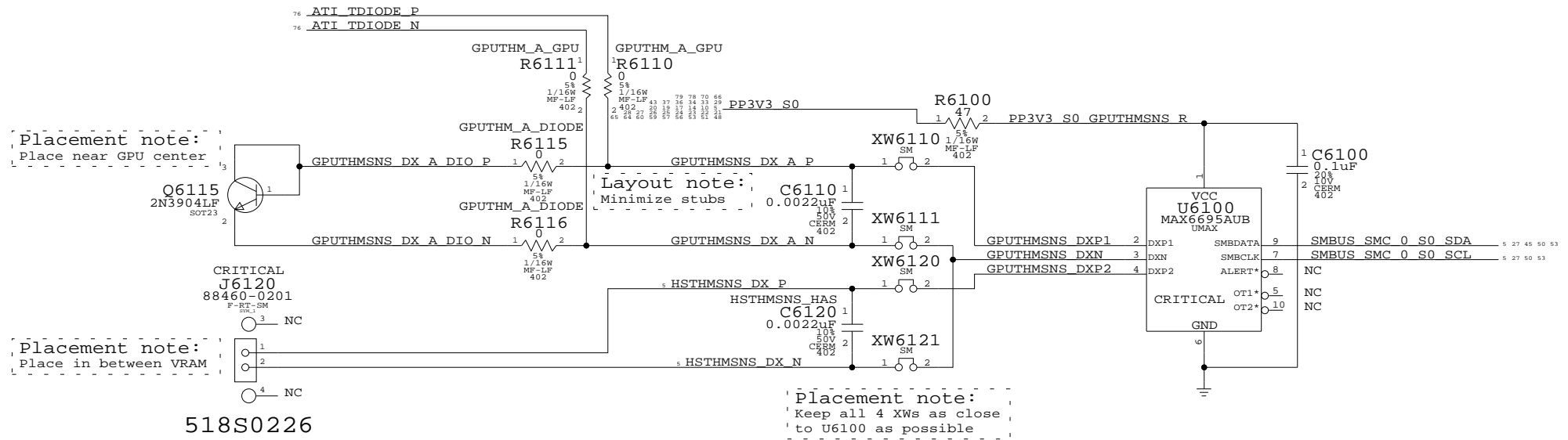
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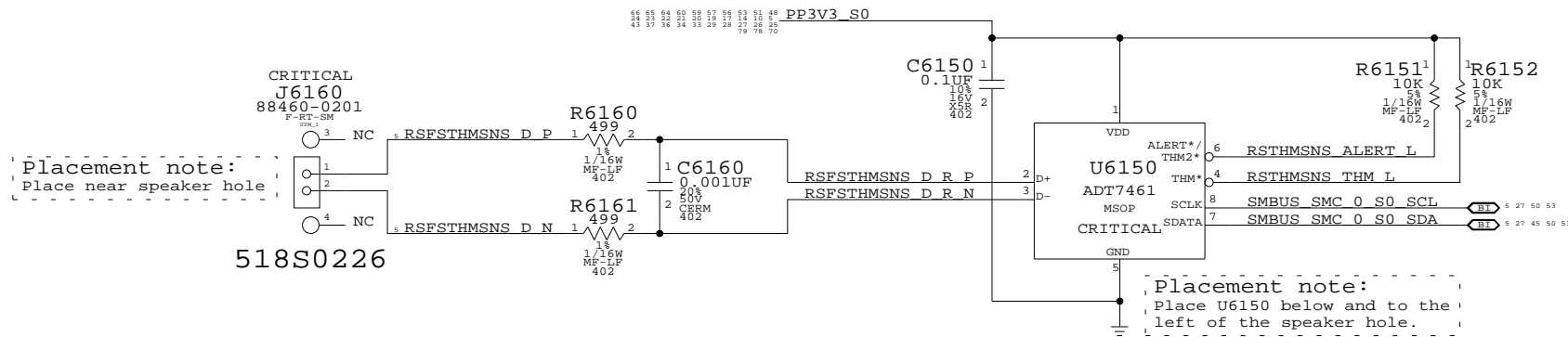
 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHEET 52	OF 86

GPU / Heat Pipe Thermal Sensor

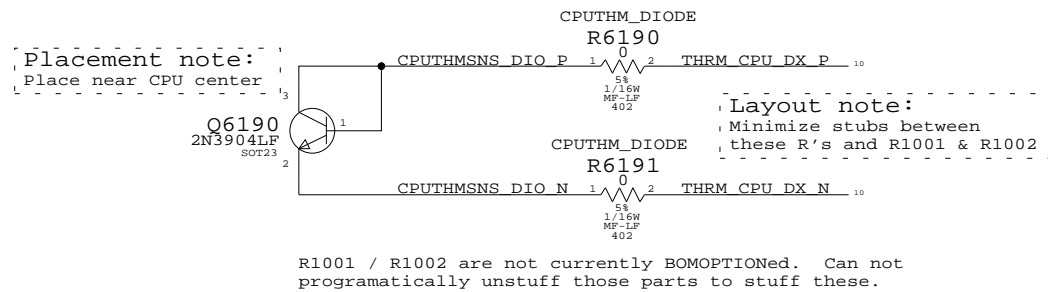


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



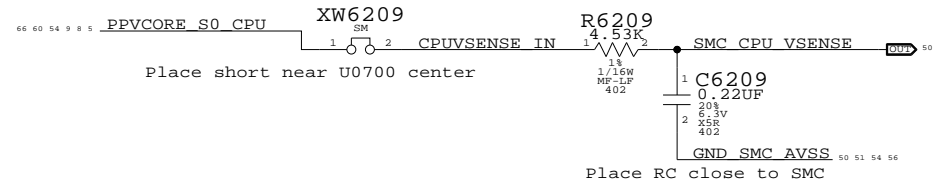
CPU Back-Up Thermal Diode



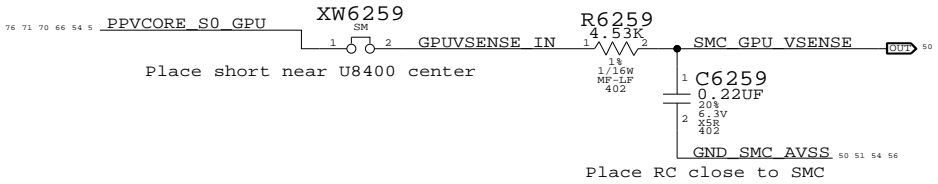
Thermal Sensors		
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006	
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	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	53	86	

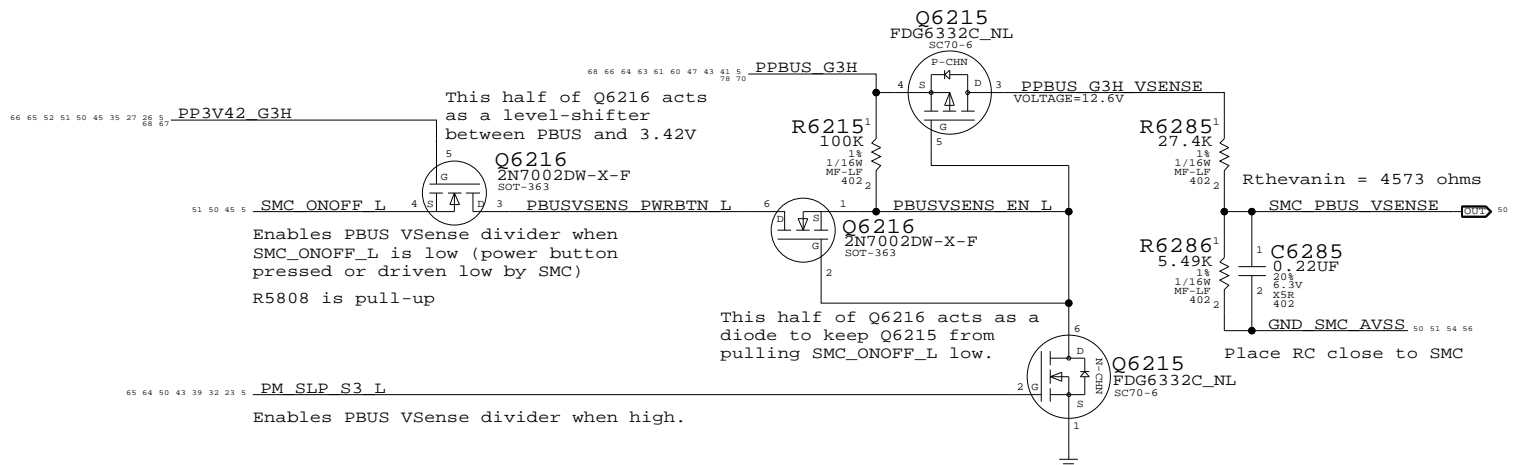
CPU Voltage Sense / Filter



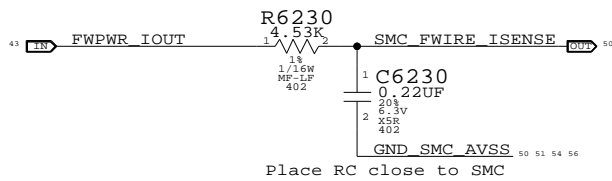
GPU Voltage Sense / Filter



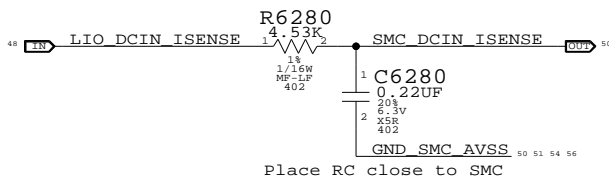
PBUS Voltage Sense Enable & Filter



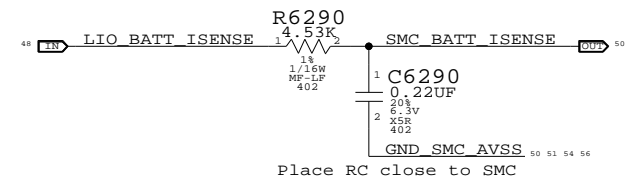
FireWire Current Sense Filter



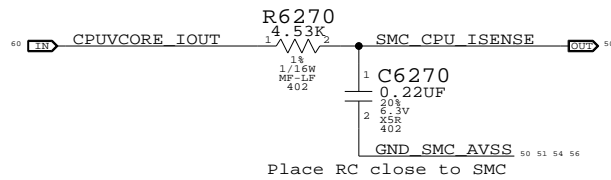
DCIN Current Sense Filter



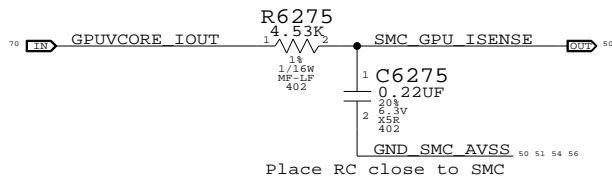
Battery Current Sense Filter



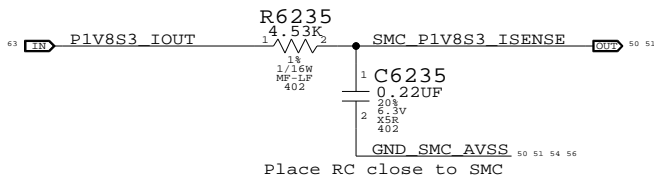
CPU Current Sense Filter



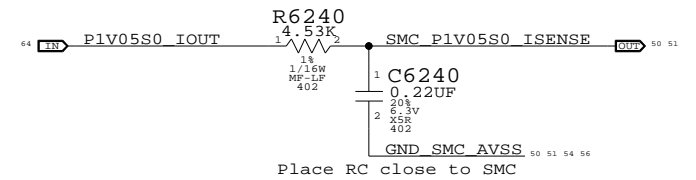
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

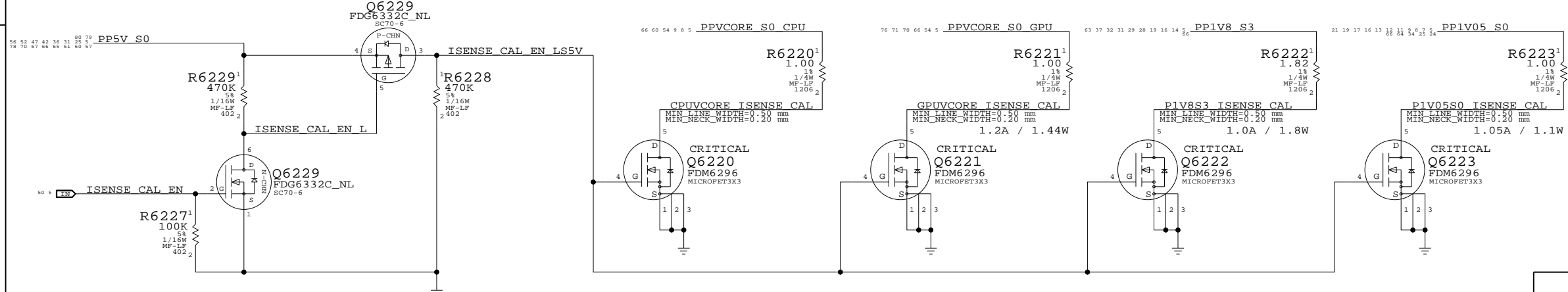


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



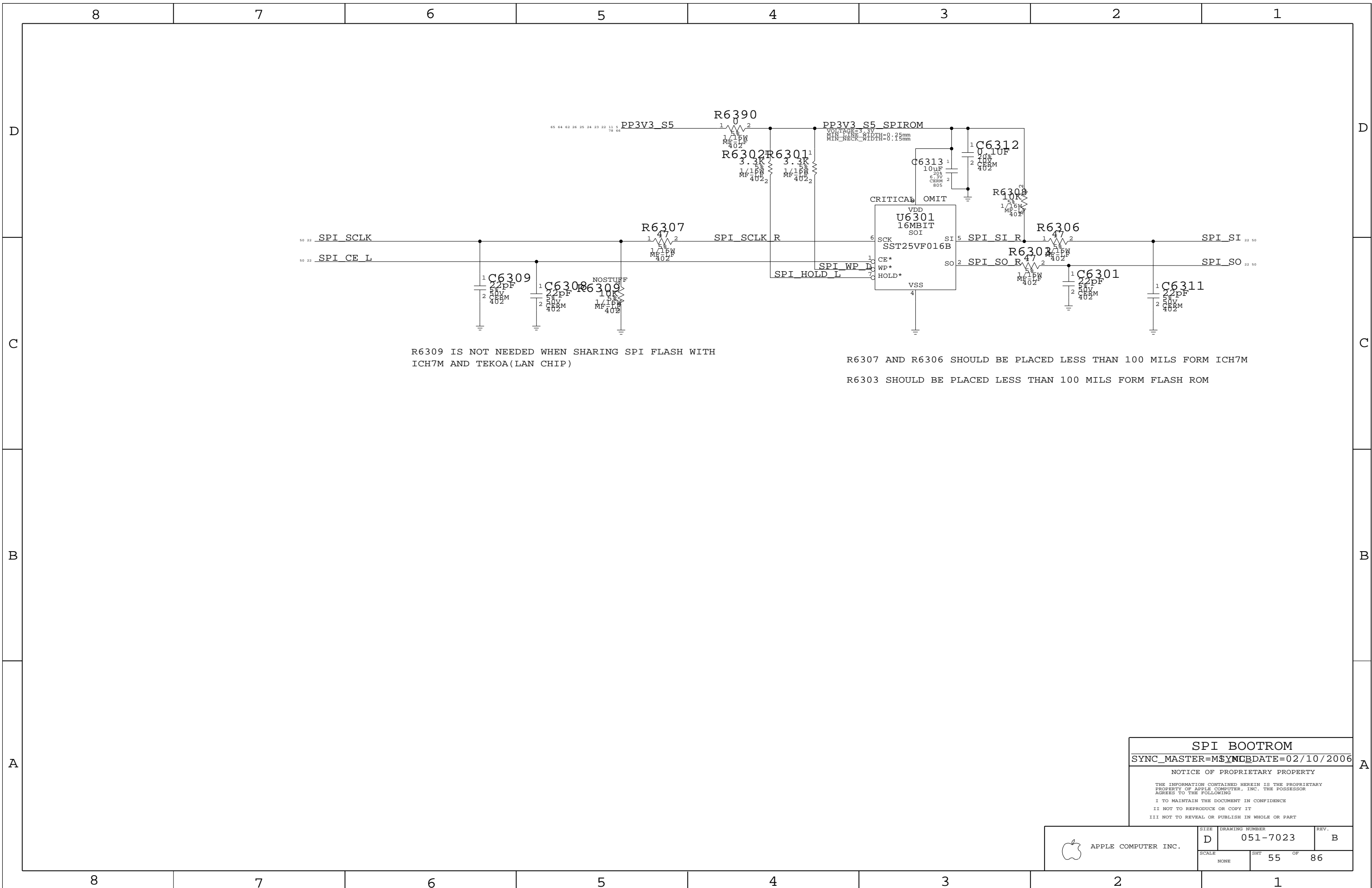
Current & Voltage Sensing

SYNC_MASTER=M1_MLB SYNC_DATE=01/05/2006

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	D	051-7023	B
SCALE	NONE	SHT	54 OF 86



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM
 SYNC_MASTER=MSYNC DATE=02/10/2006


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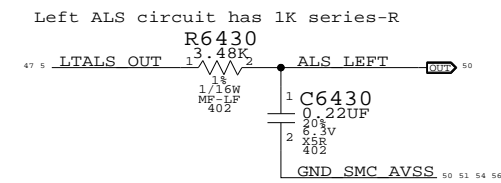
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II NOT TO REPRODUCE OR COPY IT

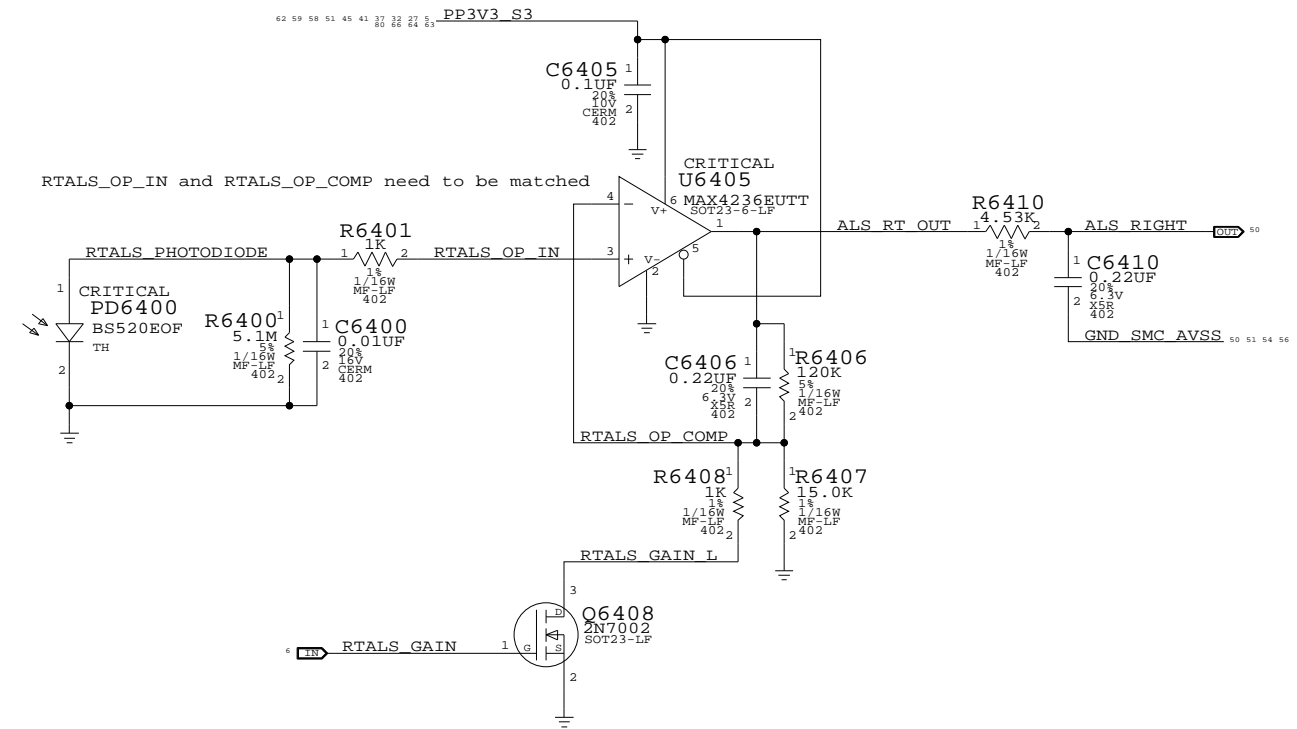
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHIT 55	OF 86

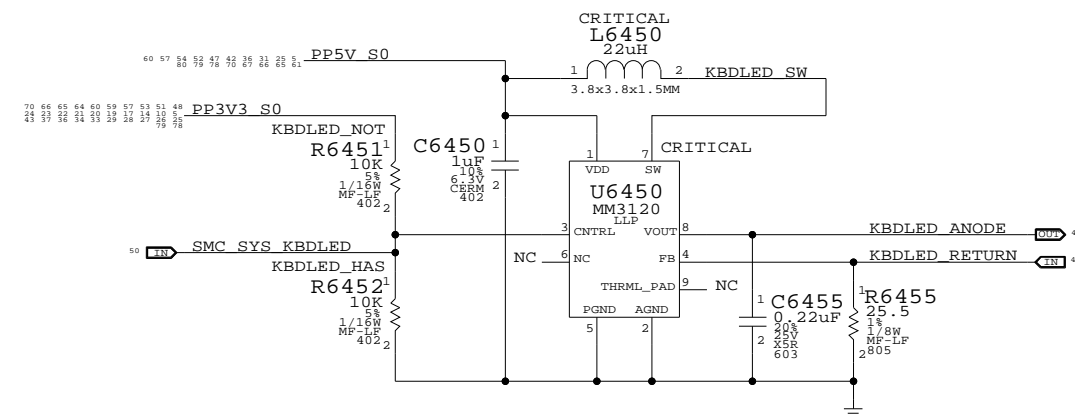
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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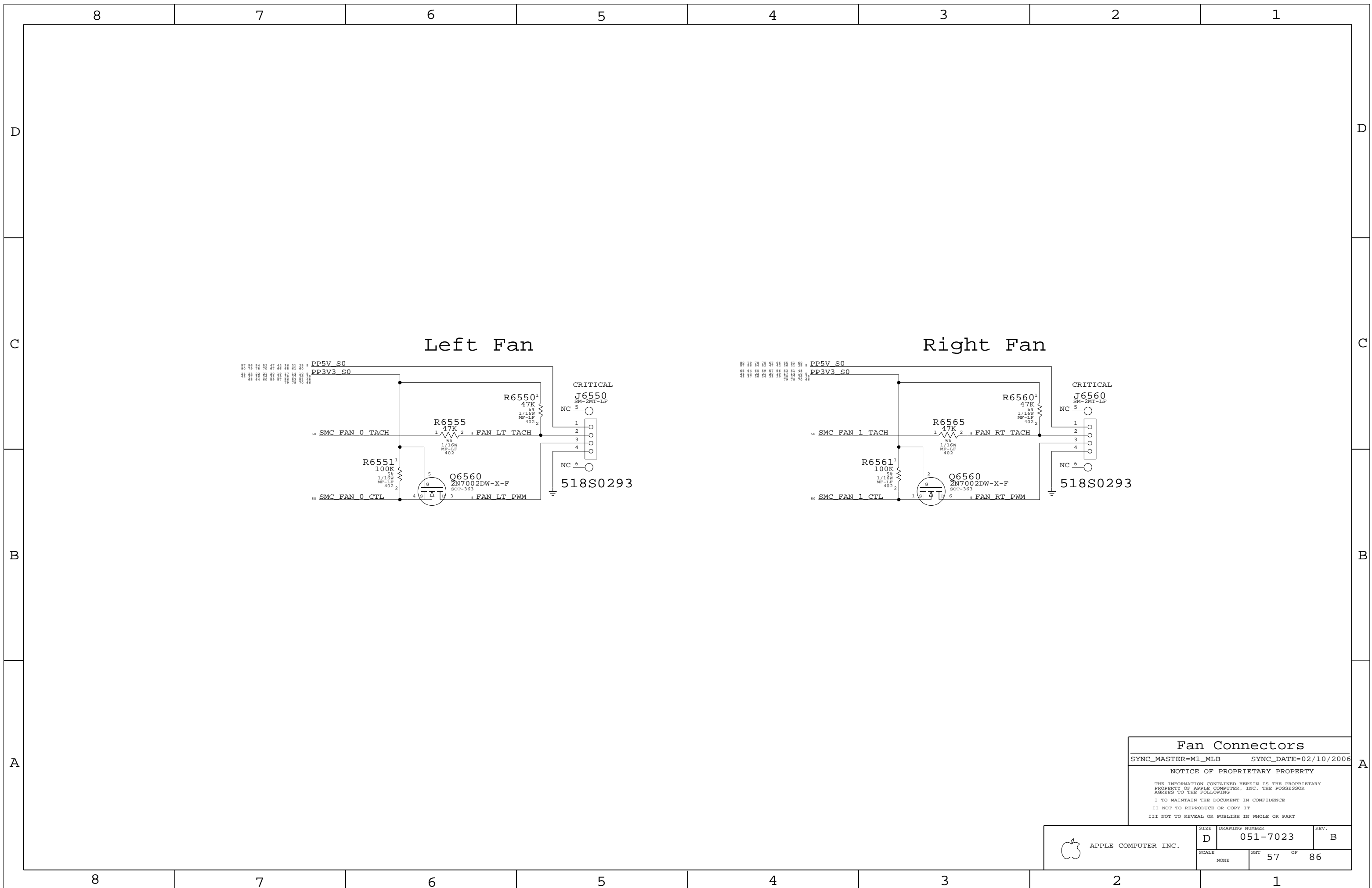
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7023	B
SCALE	SHT	OF
NONE	56	86



Fan Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHT 57	OF 86

8 7 6 5 4 3 2 1

D

D

C

C

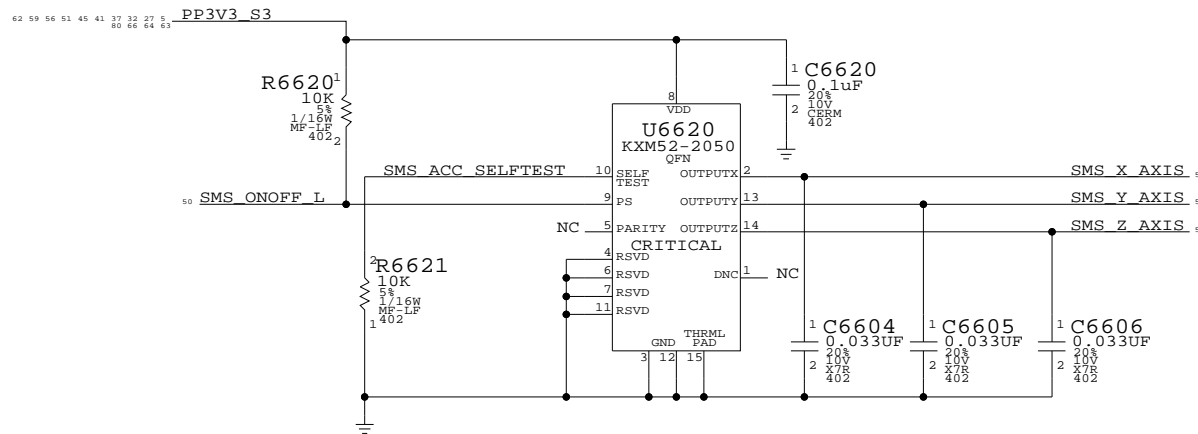
B

B

A

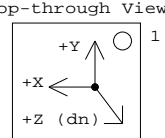
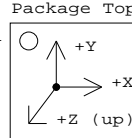
A

8 7 6 5 4 3 2 1



Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

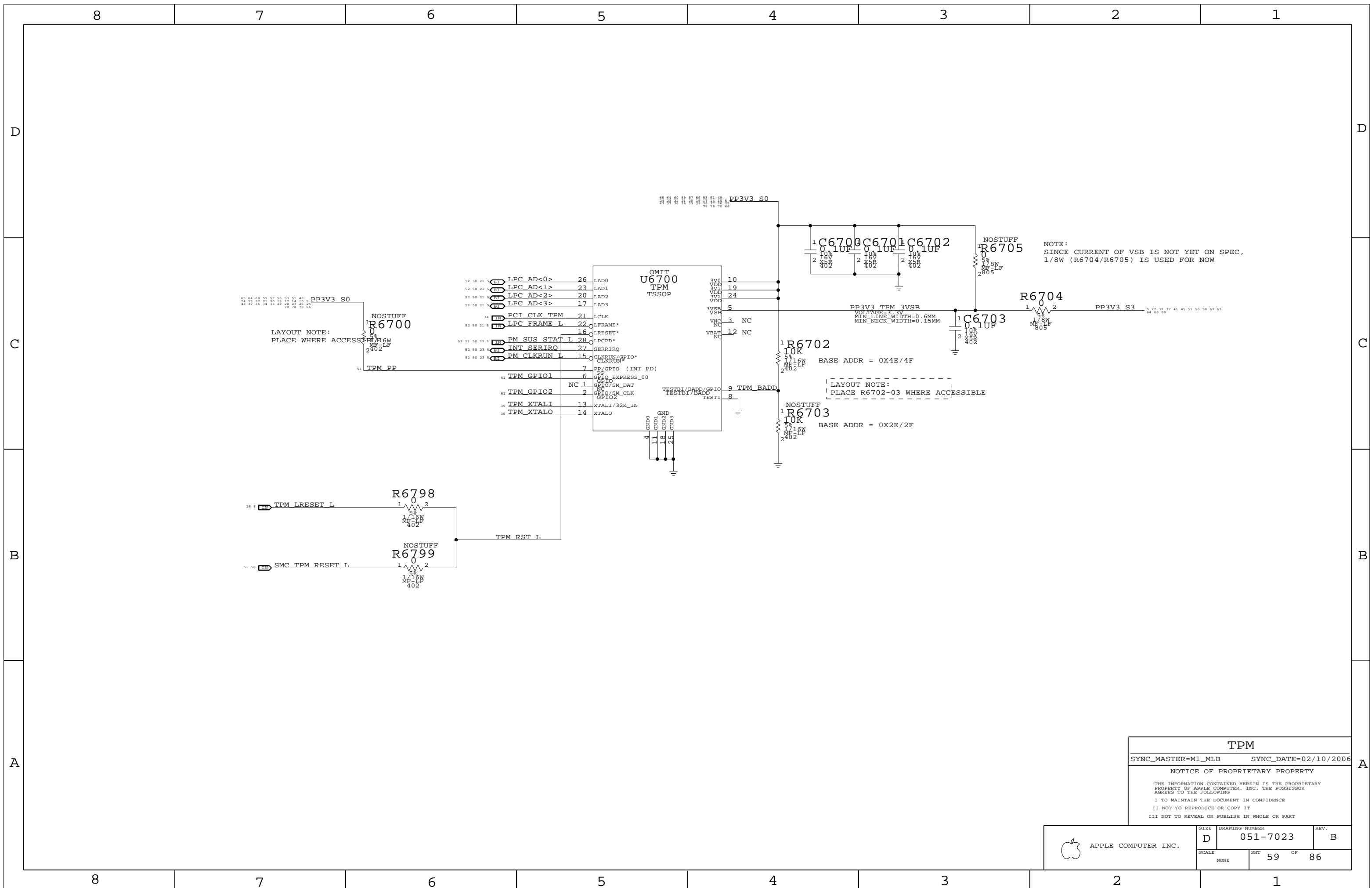


M1 placement: Bottom-side

Sudden Motion Sensor (SMS)
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	B
SCALE	SHT	OF	
NONE	58	86	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

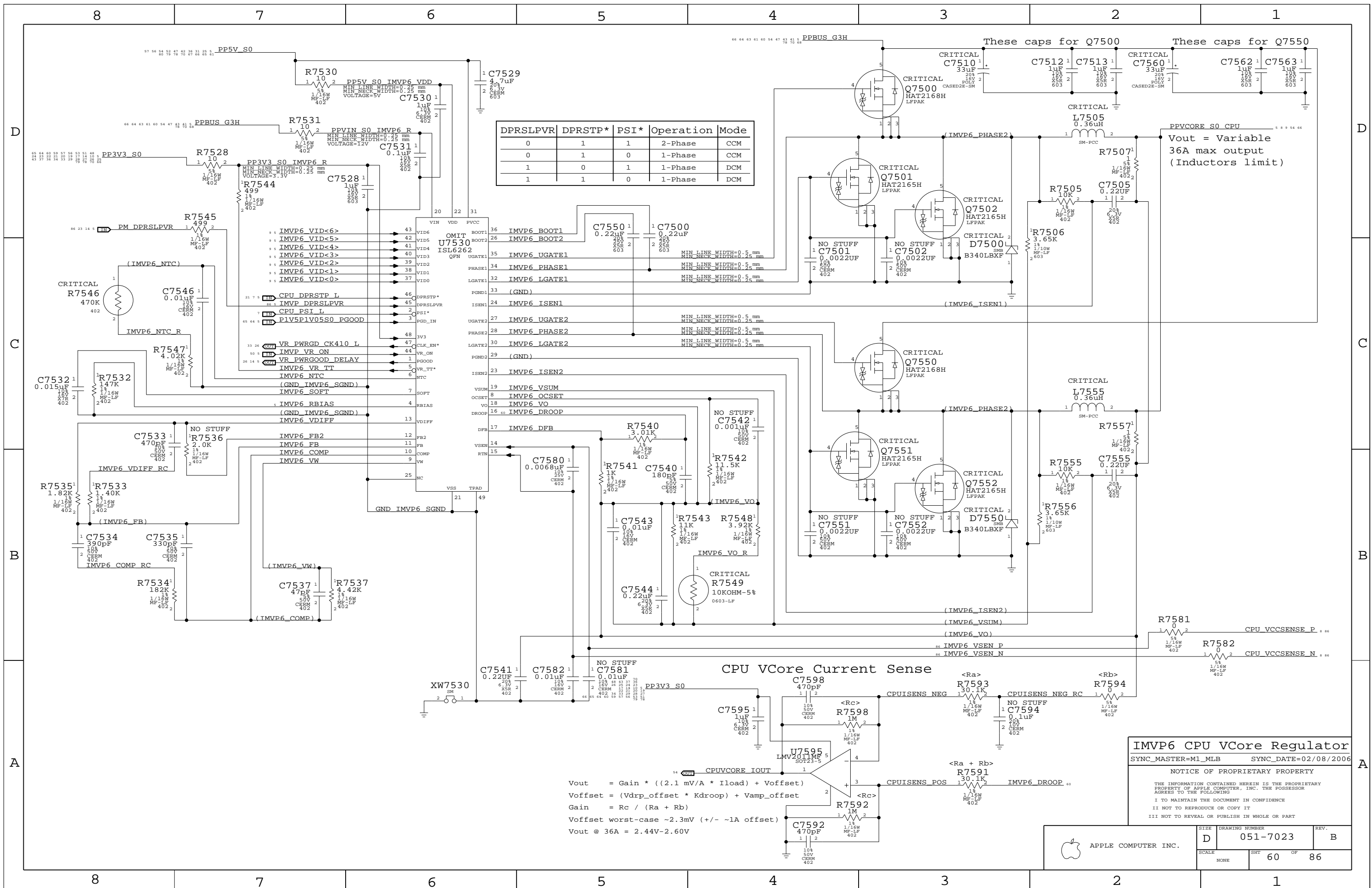
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHT 59	OF 86



DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

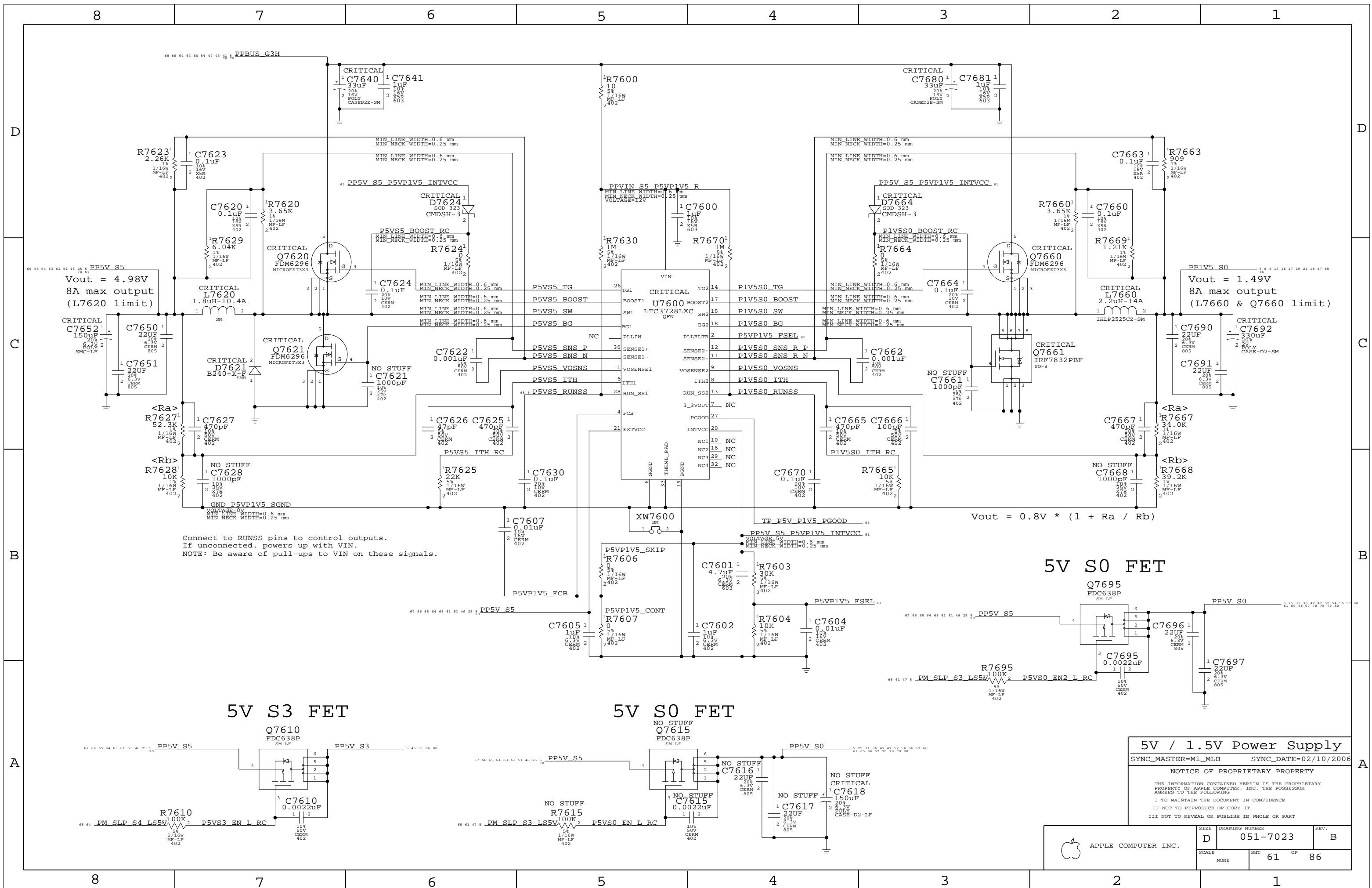
$V_{out} = Gain * ((2.1 \text{ mV/A} * I_{load}) + V_{offset})$
 $V_{offset} = (V_{drp_offset} * K_{droop}) + V_{amp_offset}$
 $Gain = R_c / (R_a + R_b)$
 $V_{offset} \text{ worst-case } \sim 2.3\text{mV} (+/- \sim 1\text{A offset})$
 $V_{out} @ 36\text{A} = 2.44\text{V} - 2.60\text{V}$

IMVP6 CPU VCore Regulator

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	D	051-7023	B
SCALE	SHT	OF	
NONE	60	86	



Vout = 4.98V
8A max output
(L7620 limit)

Vout = 1.49V
8A max output
(L7660 & Q7661 limit)

$$Vout = 0.8V * (1 + Ra / Rb)$$

Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.

5V S3 FET

Q7610
FDC638P

5V S0 FET

NO STUFF
Q7615
FDC638P

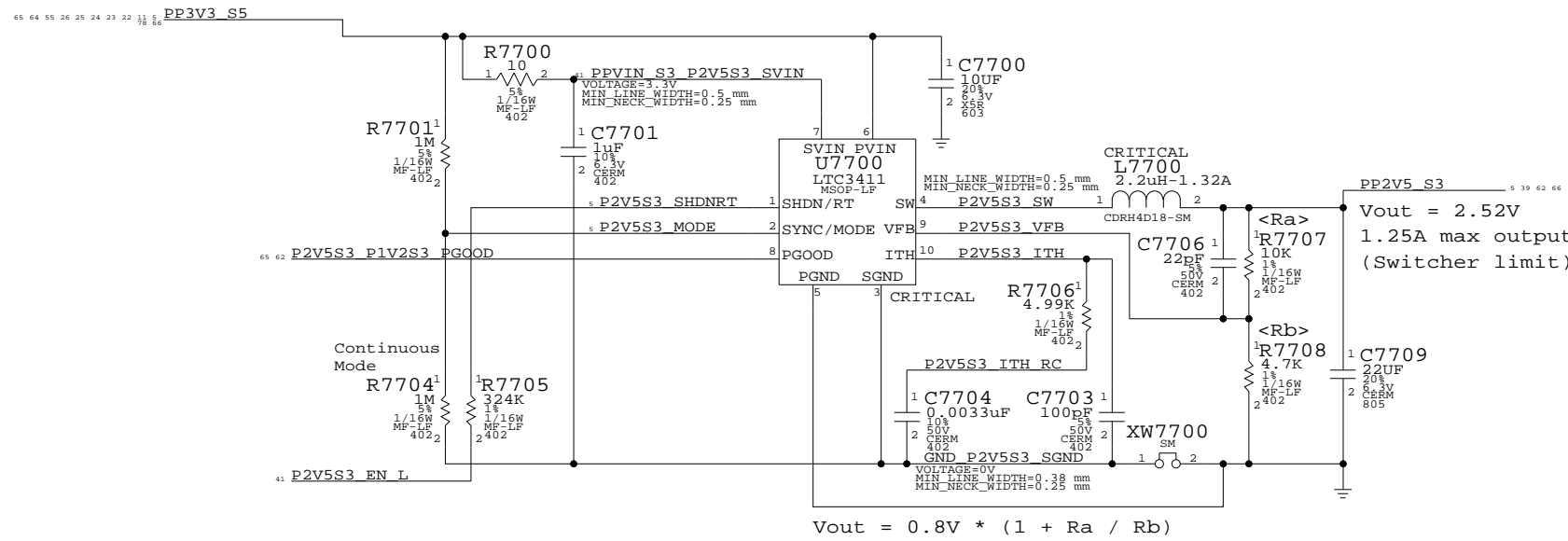
5V / 1.5V Power Supply

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

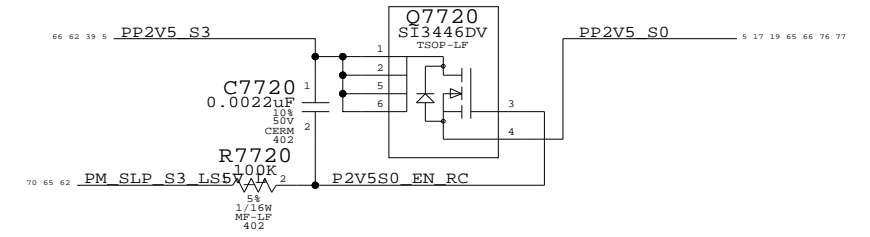
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SCALE	SHT	OF	
NONE	61	86	

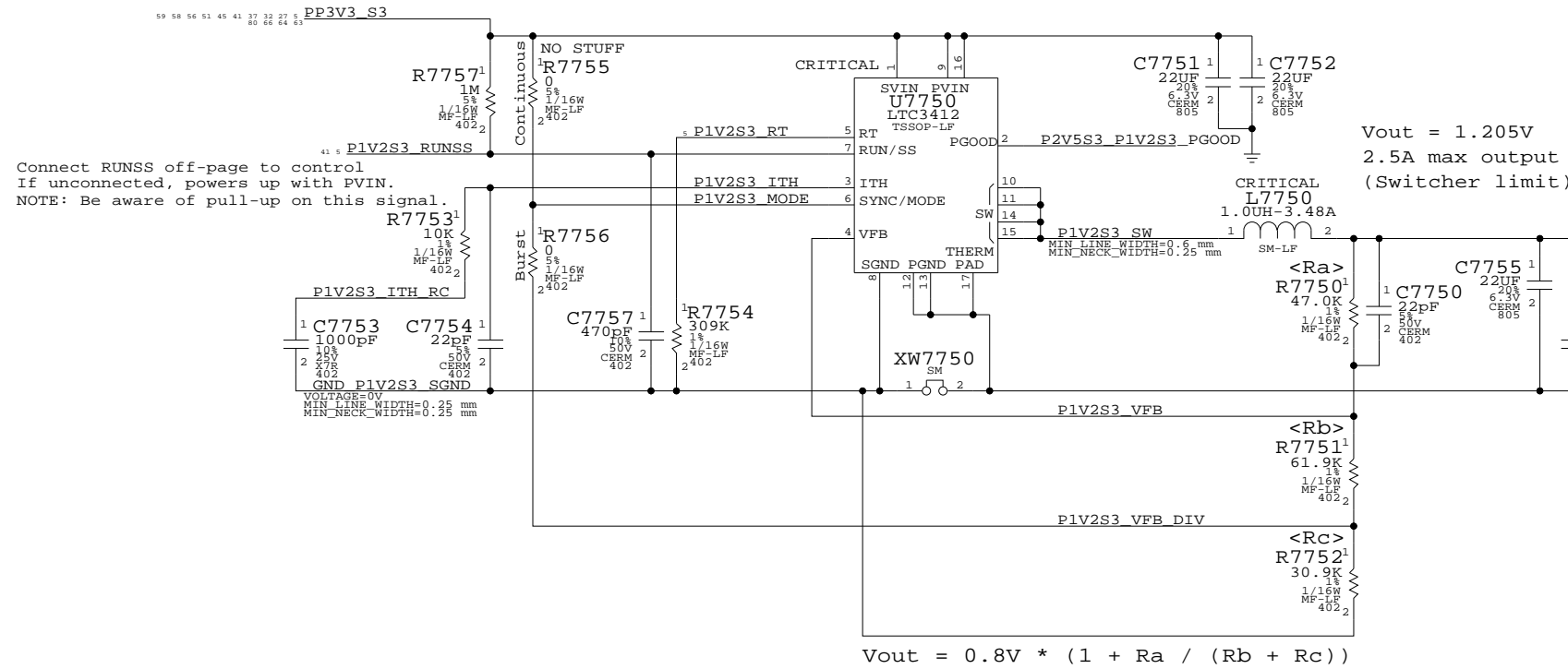
2.5V S3 Regulator



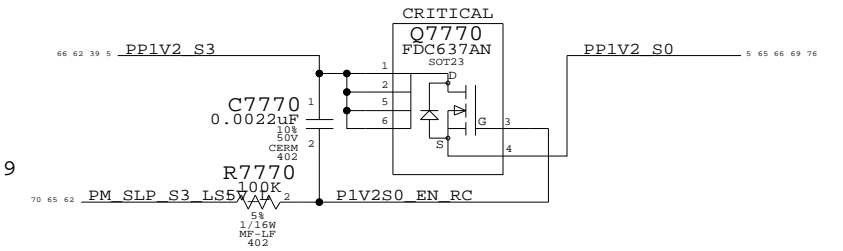
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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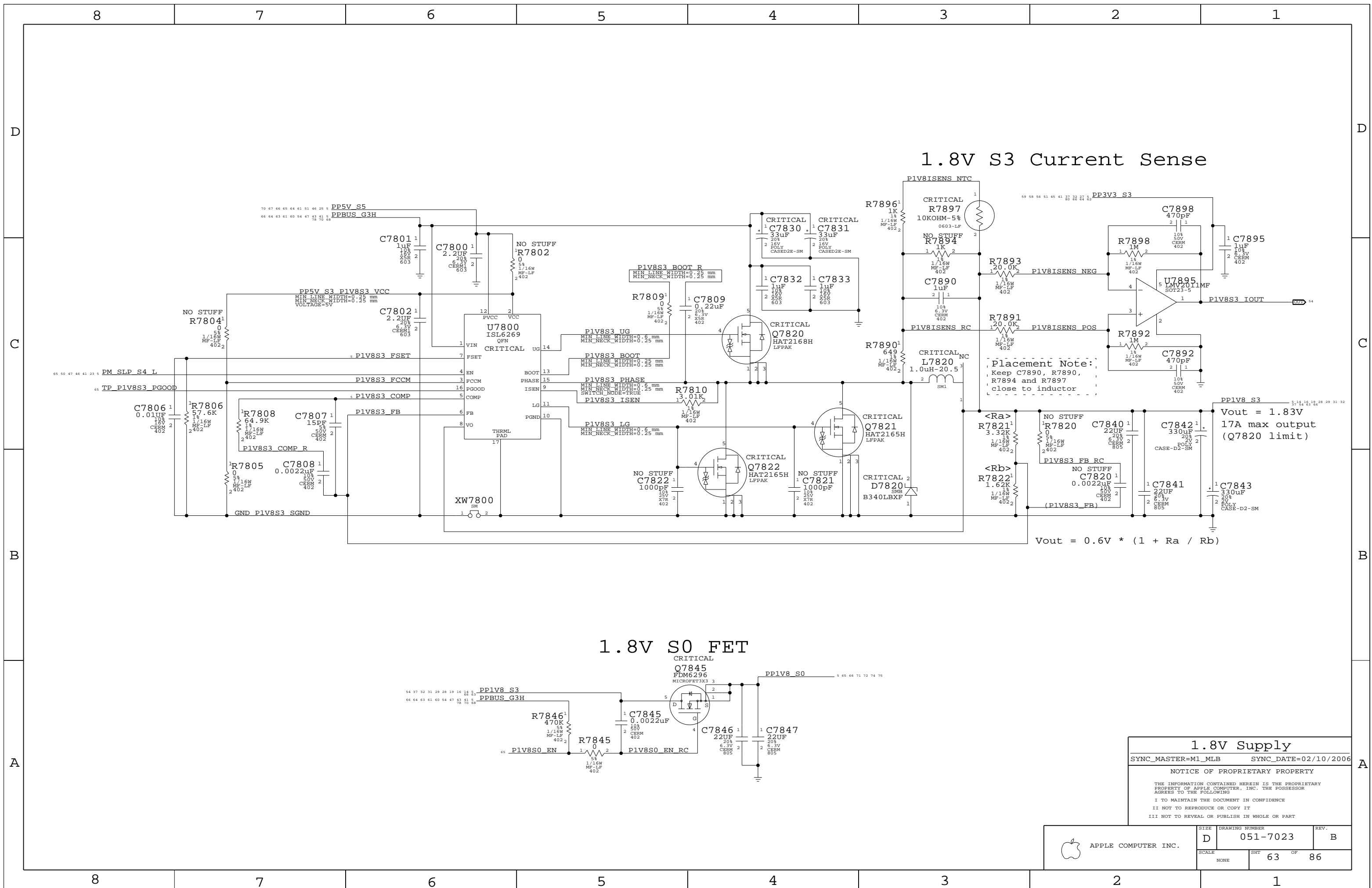
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	D	051-7023	B
SCALE	NONE	SHT	62 OF 86



1.8V S3 Current Sense

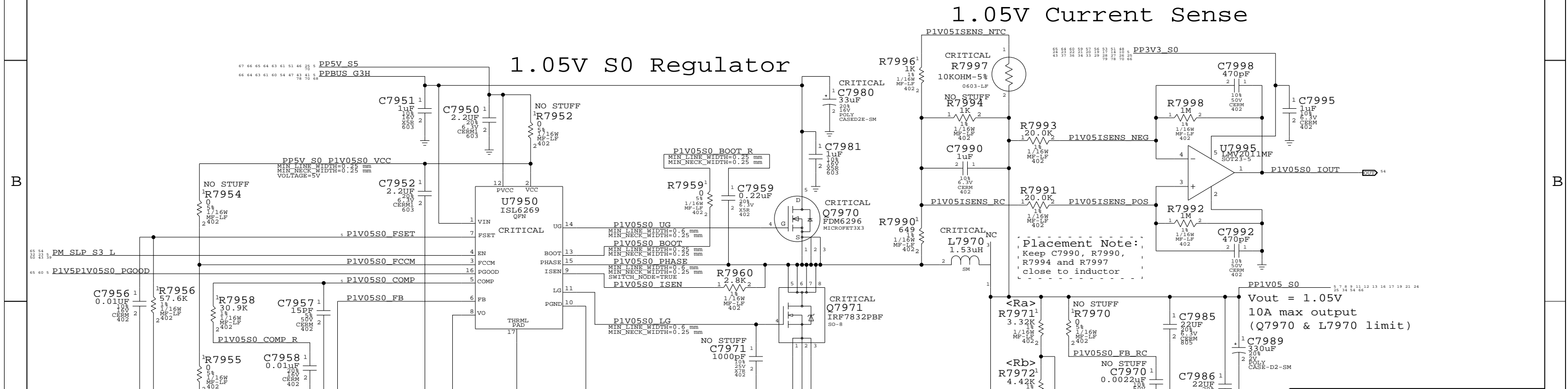
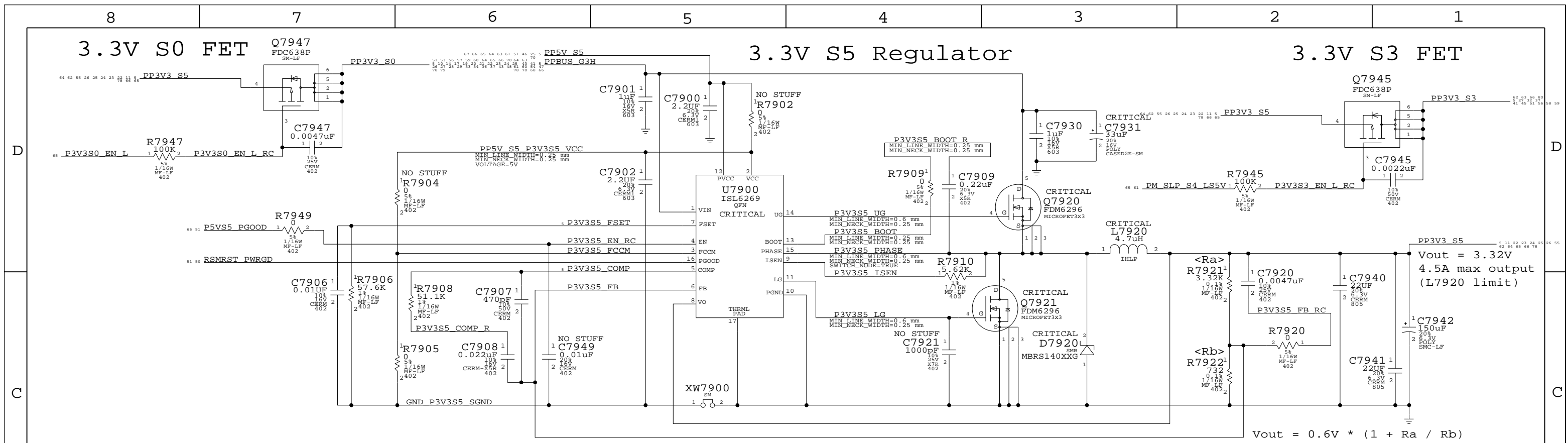
Placement Note:
Keep C7890, R7890,
R7894 and R7897
close to inductor

$$V_{out} = 0.6V * (1 + R_a / R_b)$$

1.8V S0 FET

1.8V Supply
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHT 63	OF 86

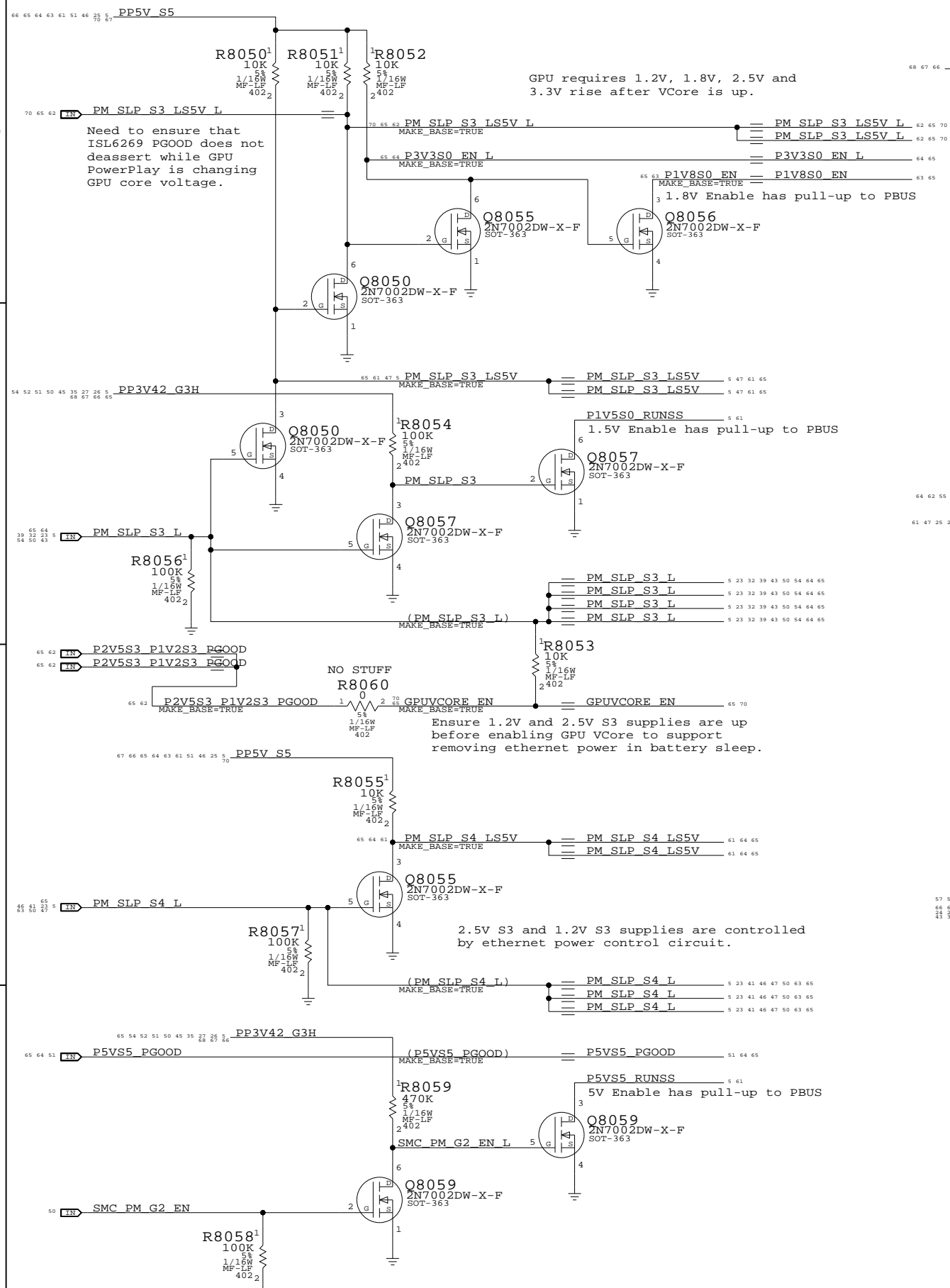


3.3V / 1.05V Power Supplies
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	NONE	SHT	64 OF 86

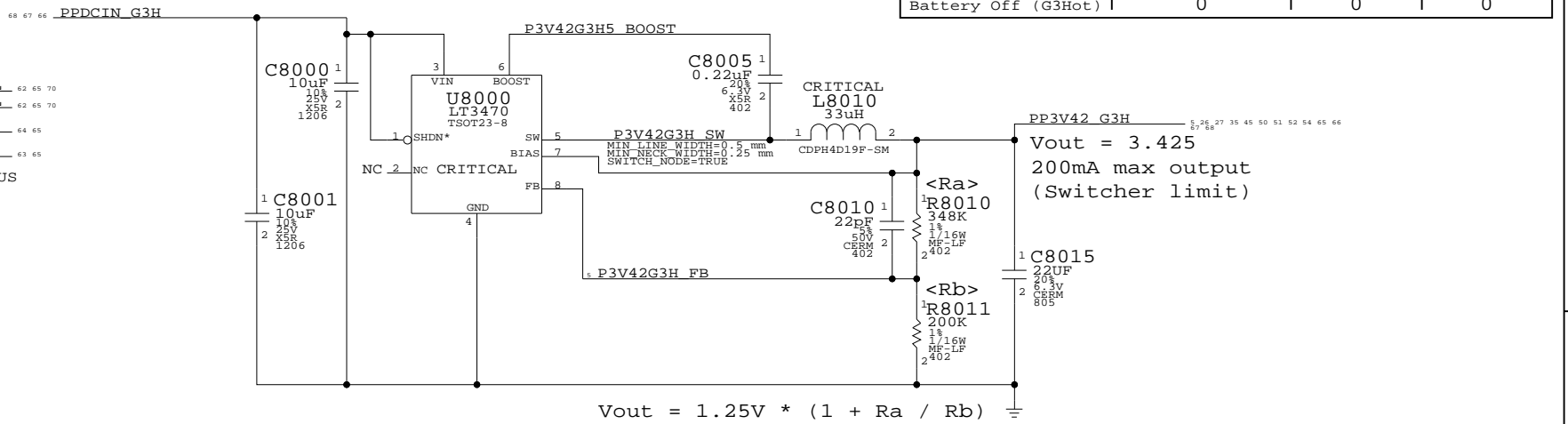
Power Control Signals



3.425V "G3Hot" Supply

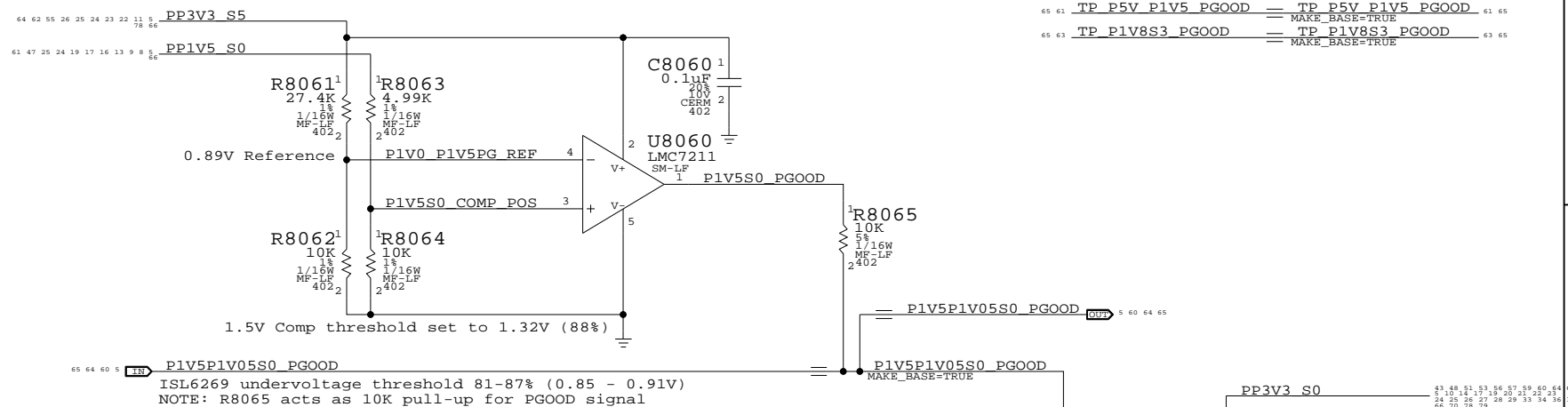
Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

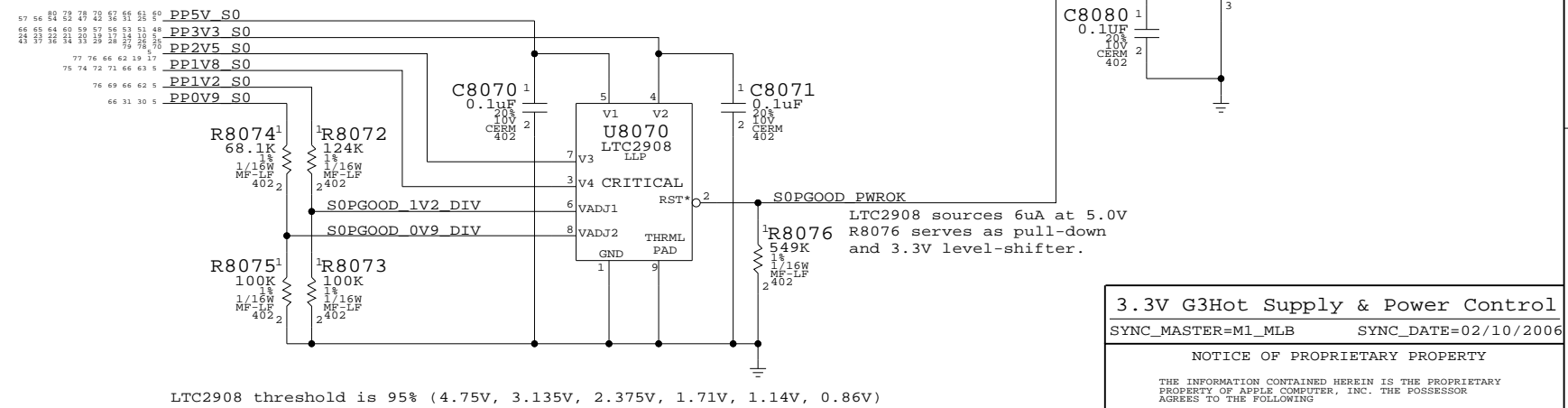


Unused PG0OD Signals

TP_P5V_P1V5_PG0OD	=	TP_P5V_P1V5_PG0OD
TP_P1V8S3_PG0OD	=	TP_P1V8S3_PG0OD

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



3.3V G3Hot Supply & Power Control

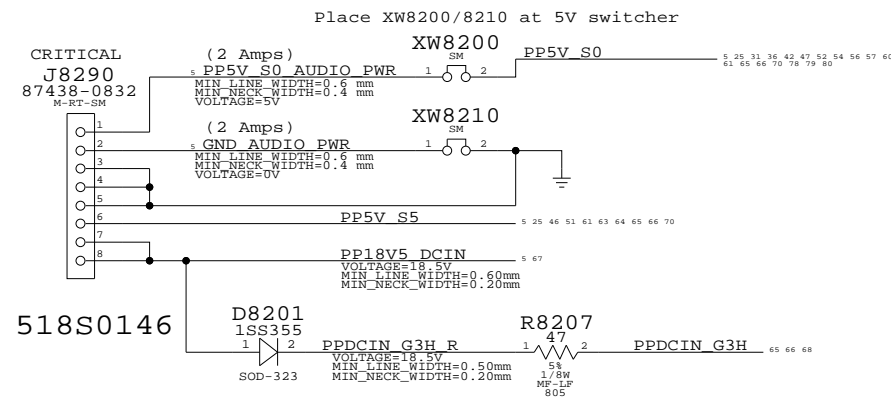
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

NOTICE OF PROPRIETARY PROPERTY

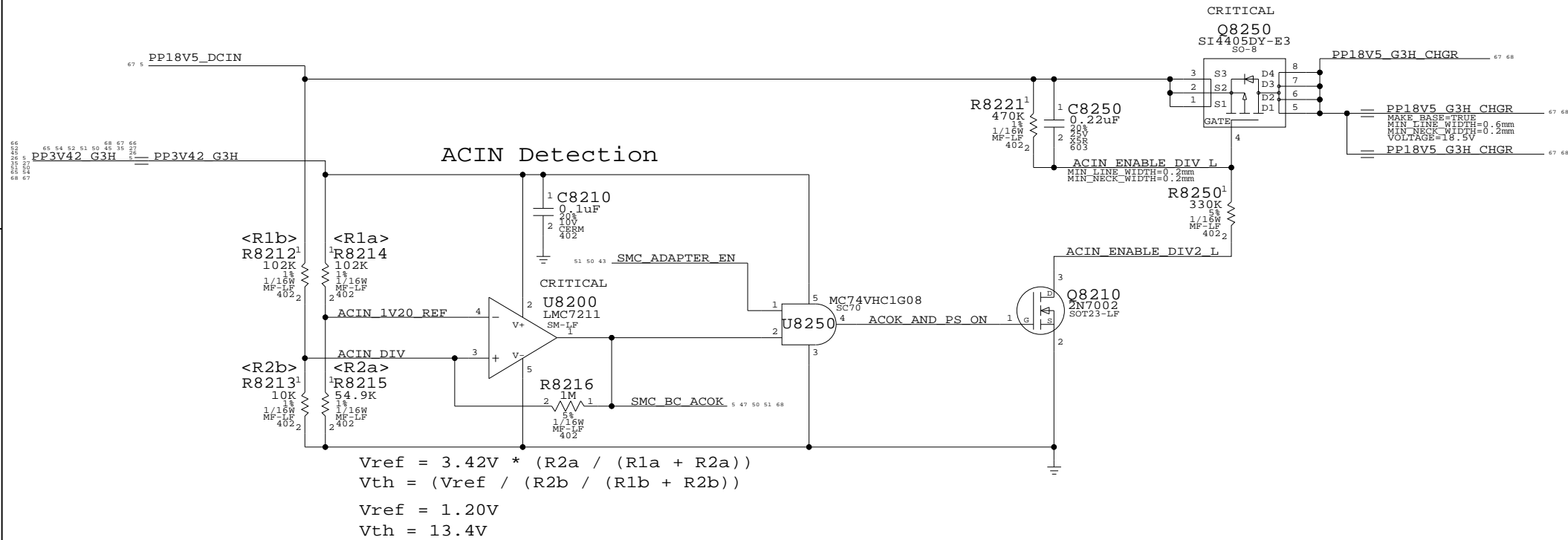
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	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	65	86	

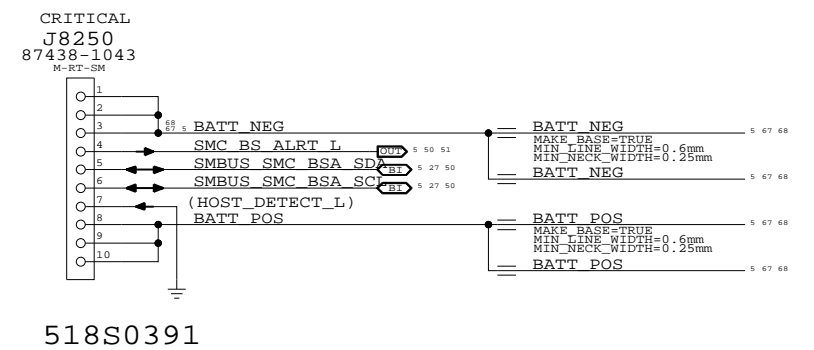
DC-In Connector



Inrush Limiter



Battery Connector



DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	67	86	

PBUS SUPPLY

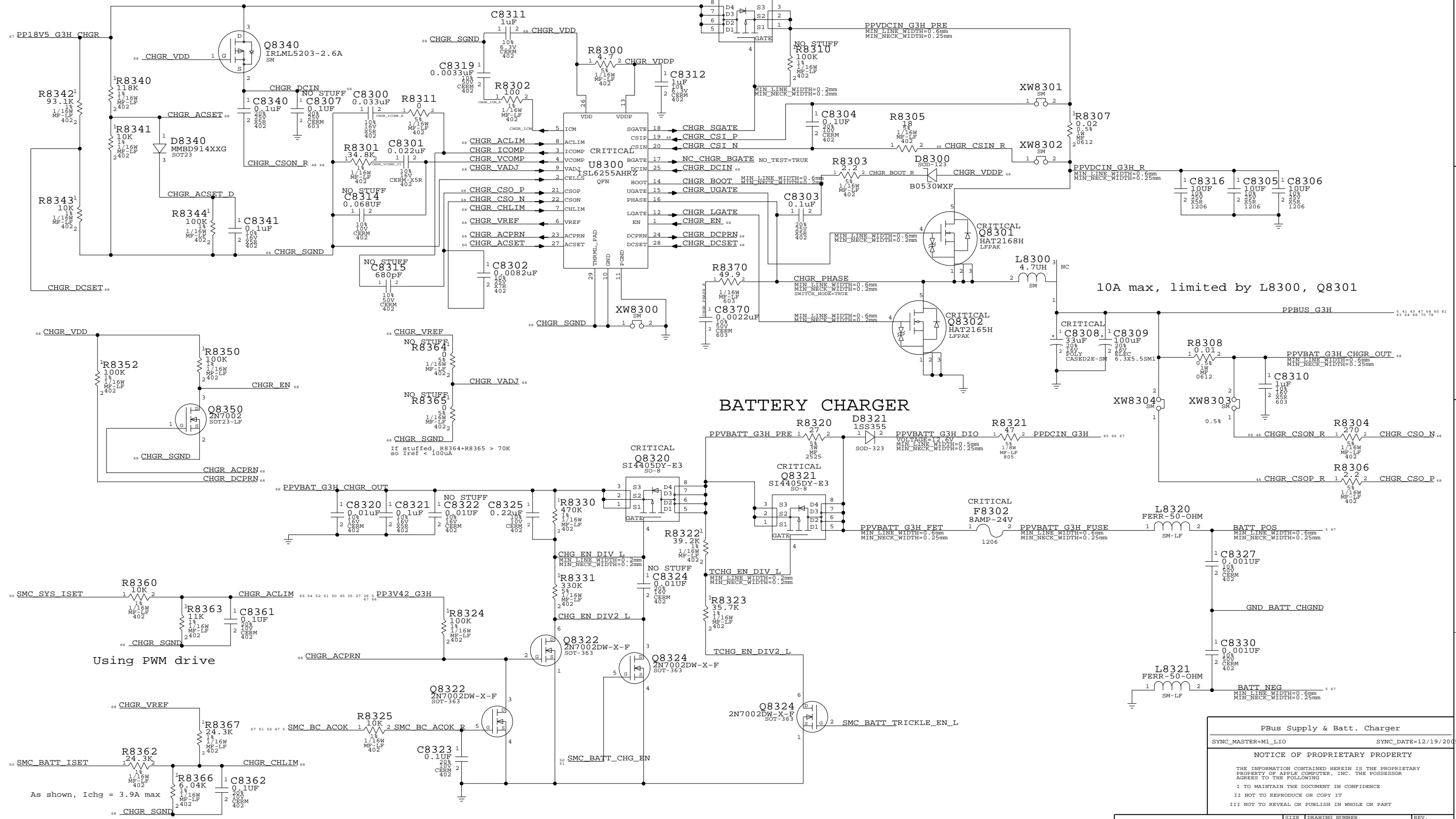
CRITICAL
Q8300
SI4405DY-E3
SO-8

BATTERY CHARGER

CRITICAL
Q8320
SI4405DY-E3
SO-8

CRITICAL
Q8321
SI4405DY-E3
SO-8

CRITICAL
F8302
8AMP-24V



10A max, limited by L8300, Q8301

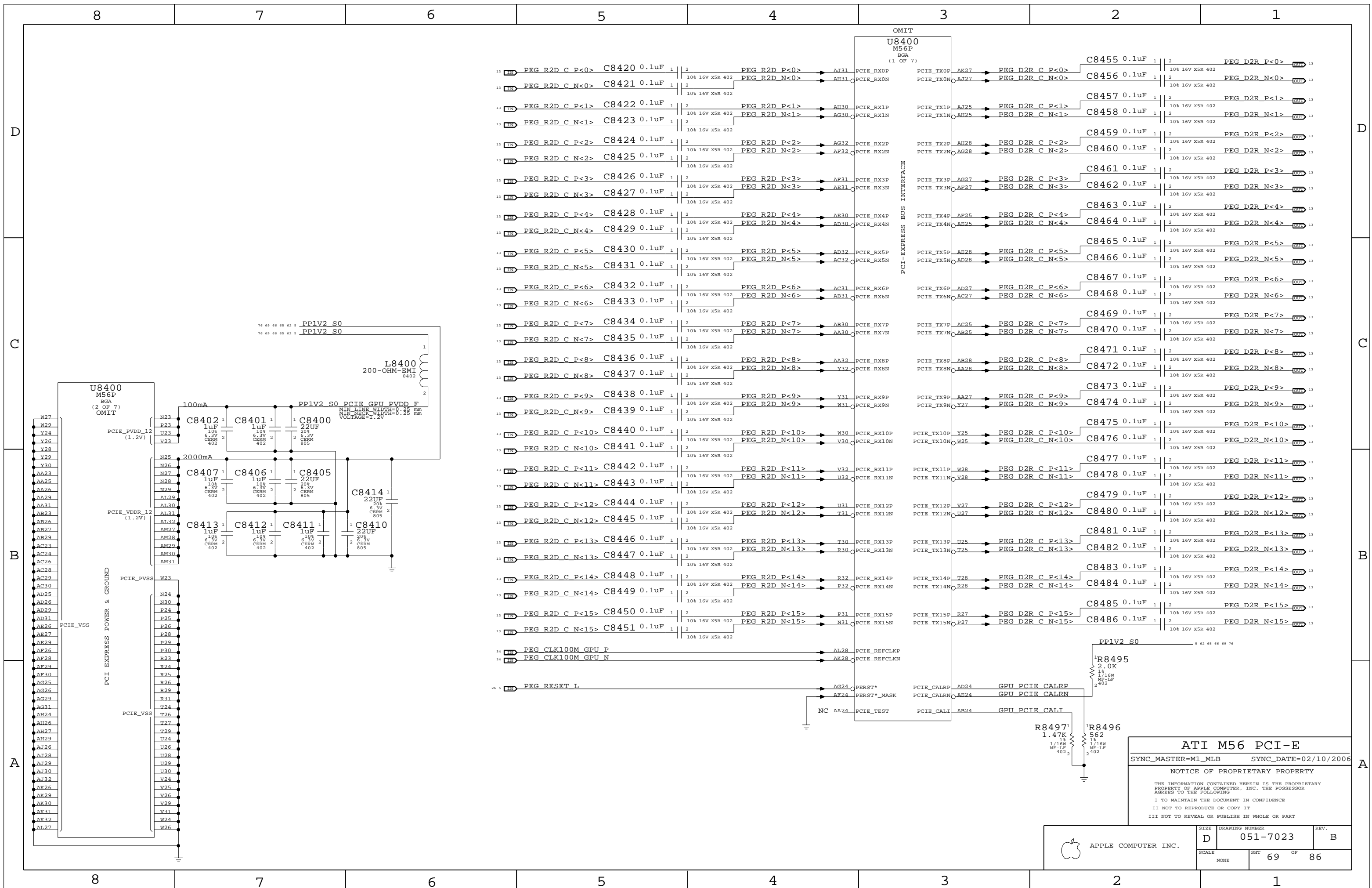
Using PWM drive

Using PWM drive

As shown, I_{chg} = 3.9A max

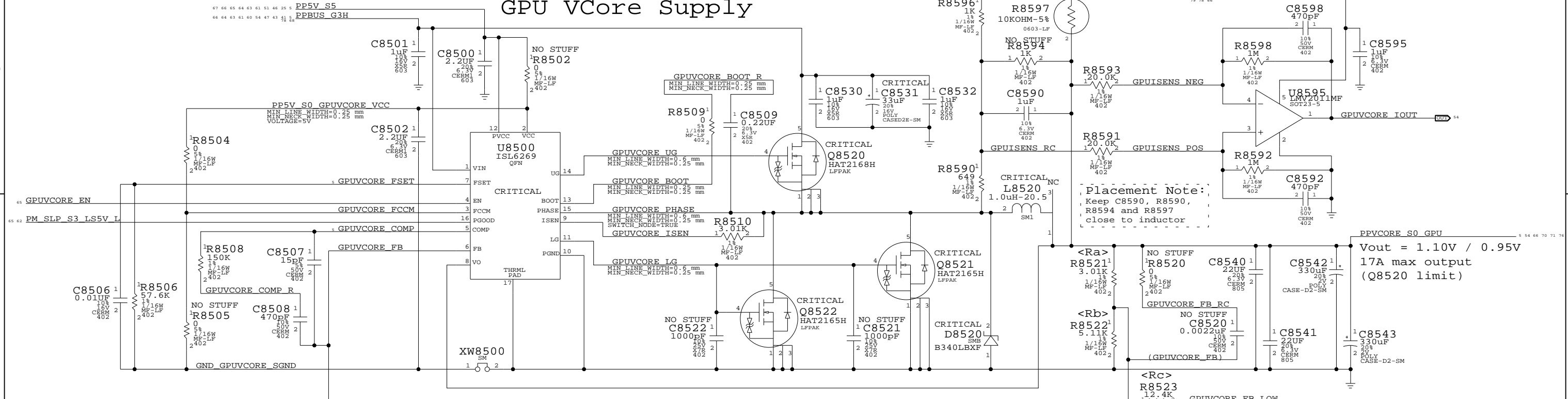
PBus Supply & Batt. Charger
 SYNC_MASTER=M1_LIO SYNC_DATE=12/19/2005
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	D	051-7023	B
SCALE	SHT	OF	REV.
NONE	68	86	



GPU VCore Current Sense

GPU VCore Supply



Placement Note:
 Keep C8590, R8590,
 R8594 and R8597
 close to inductor.

Vout = 1.10V / 0.95V
 17A max output
 (Q8520 limit)

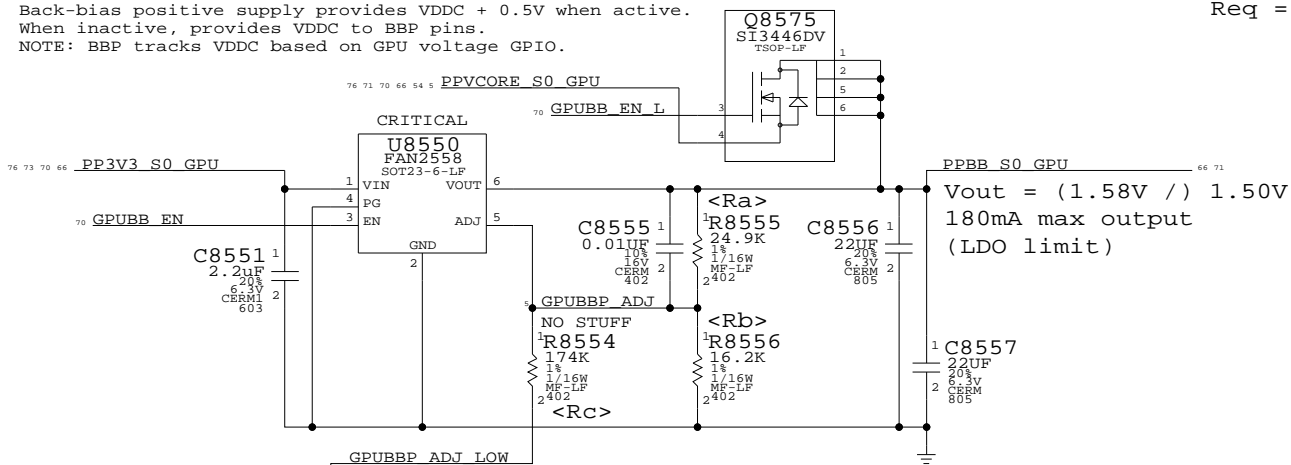
Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to GPU pins.
 NOTE: BBP tracks VDDC based on GPU voltage GPIO.

$$V_{out}(low) = 0.6V * (1 + R_a / R_b)$$

$$V_{out}(high) = 0.6V * (1 + R_a / R_{eq})$$

$$R_{eq} = R_b || R_c$$



$$V_{out}(low) = 0.59V * (1 + R_a/R_b)$$

$$V_{out}(high) = 0.59V * (1 + R_a/R_{eq})$$

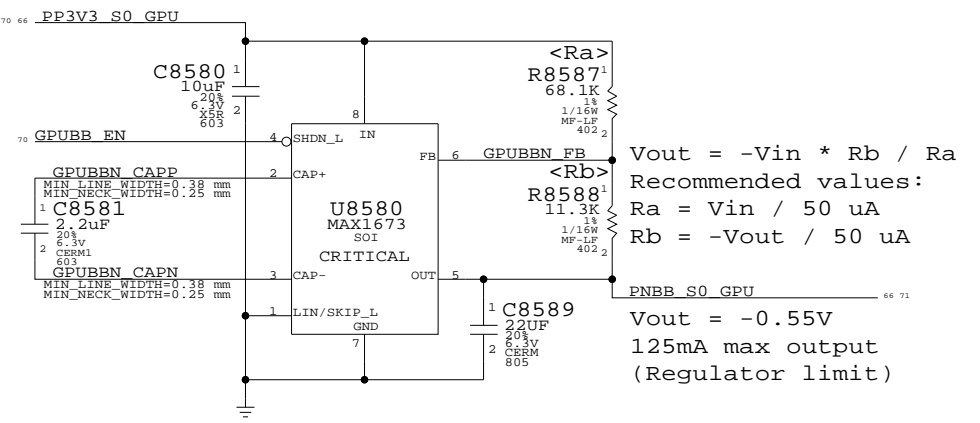
$$R_{eq} = R_b || R_c$$

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
 SI3446DV max Vgs is 1.6V
 Vin must be > 2.8V

For proper M56 power sequence, this pull-up must be powered before VCore

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active. When inactive, provides VSS to BBN pins.



$$V_{out} = -V_{in} * R_b / R_a$$

Recommended values:
 $R_a = V_{in} / 50 \mu A$
 $R_b = -V_{out} / 50 \mu A$

Vout = -0.55V
 125mA max output
 (Regulator limit)

GPU (M56) Core Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT 70 OF 86		

Page Notes

Power aliases required by this page:

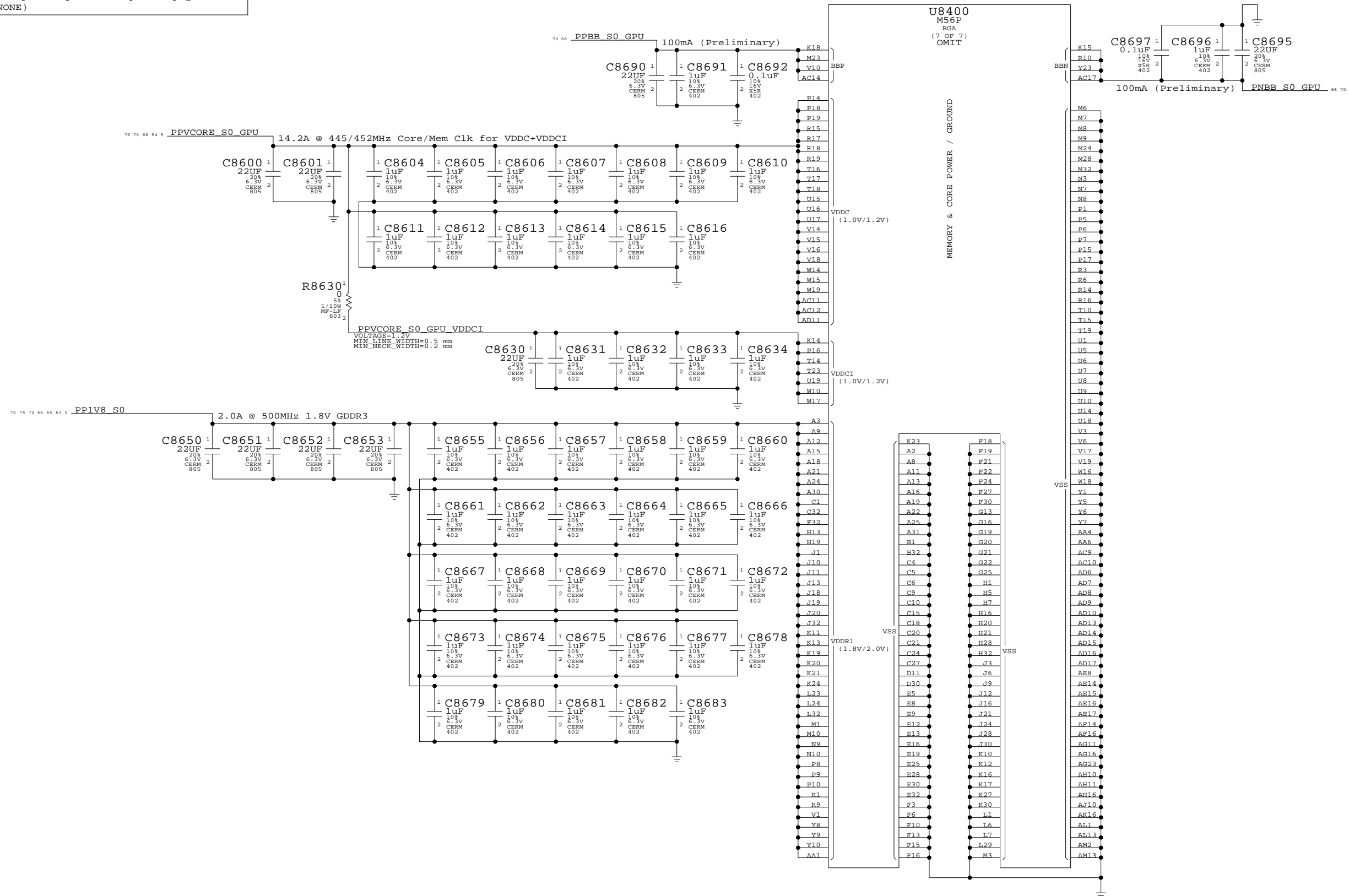
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



ATI M56 Core Power
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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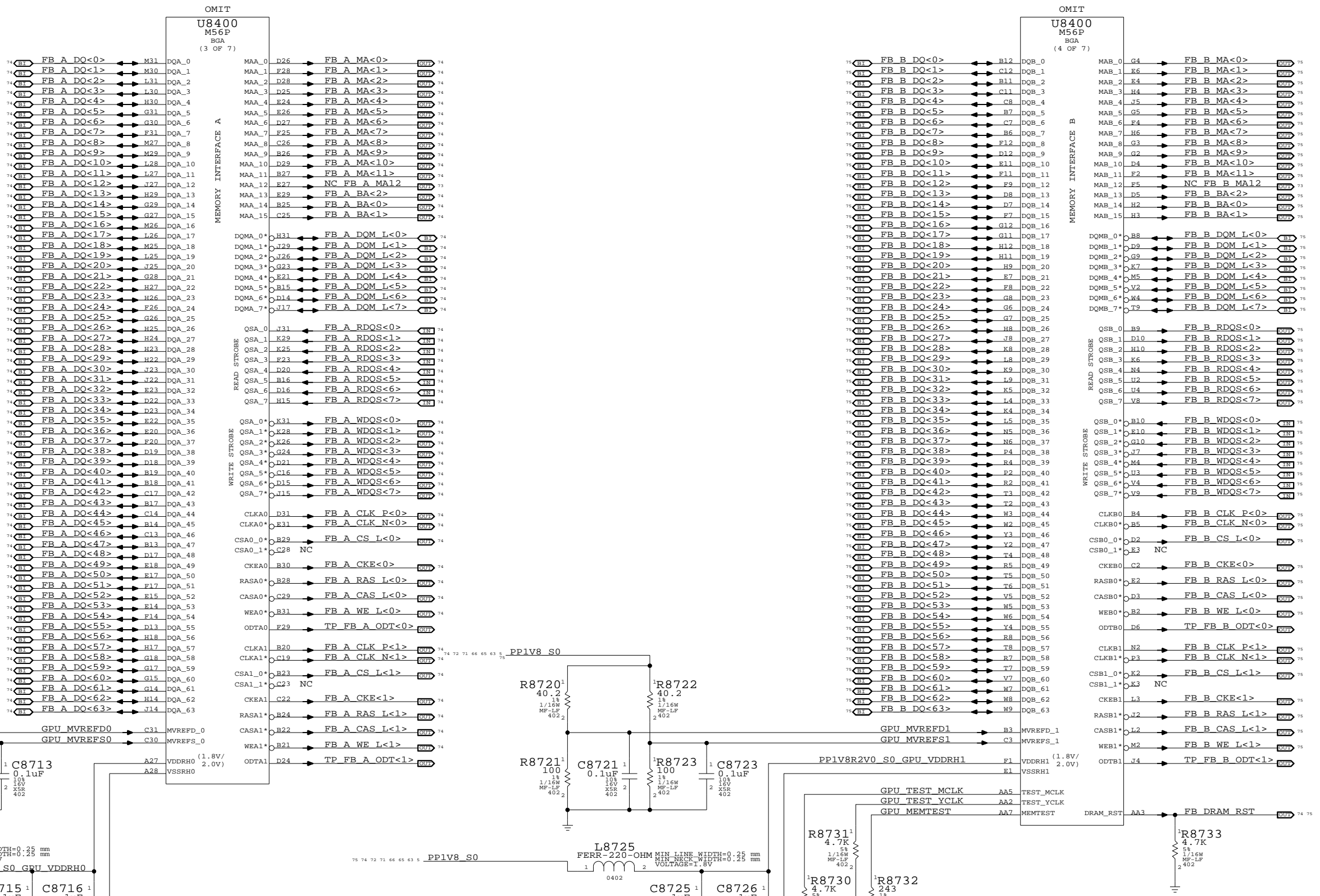
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	NONE	SHT	71 OF 86

Page Notes

Power aliases required by this page:
 - PPIV8R2V0_S0_FB_GPU

Signal aliases required by this page:
 (NONE)

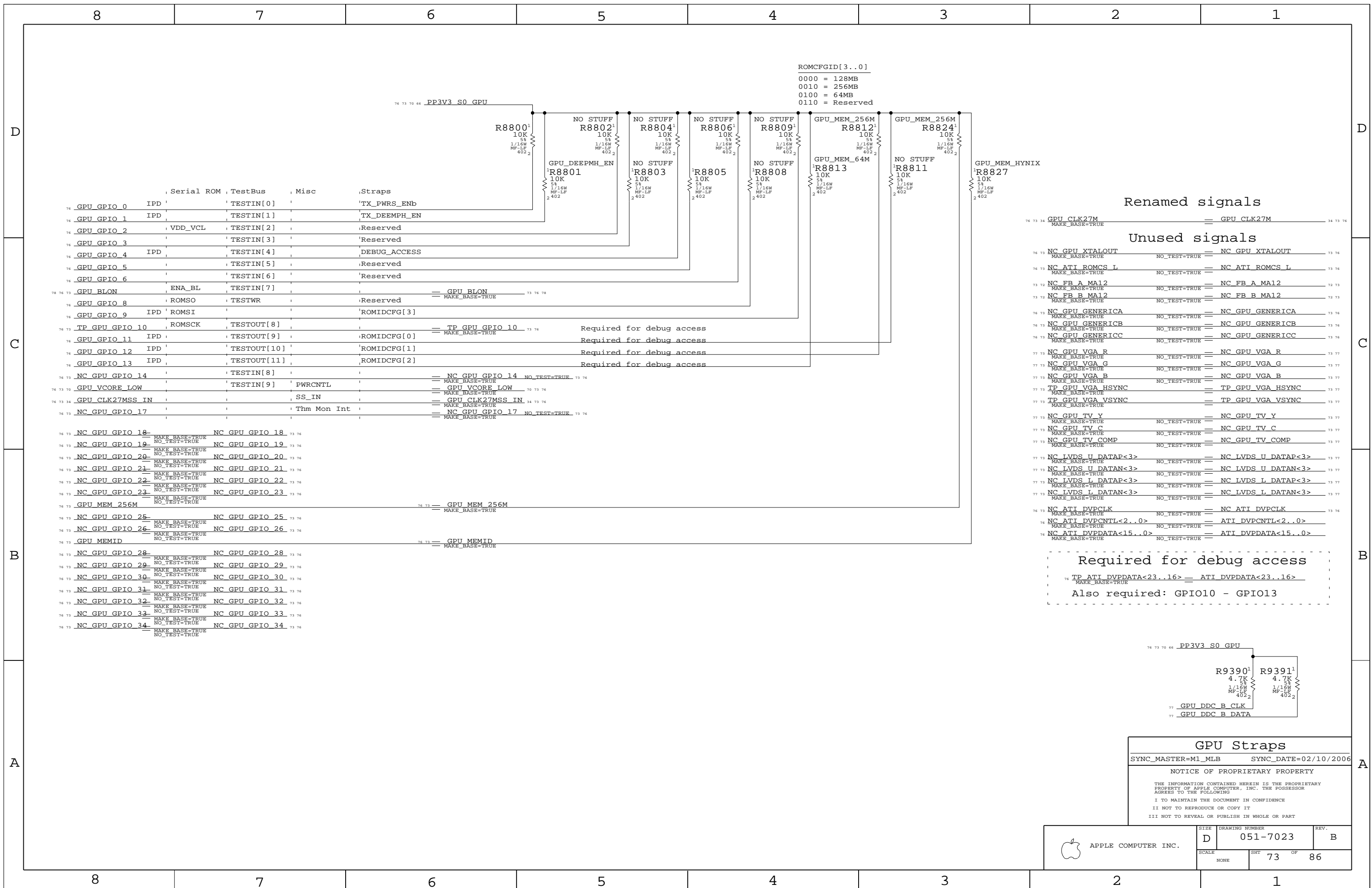
BOM options provided by this page:
 (NONE)



ATI M56 Frame Buffer I/F
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

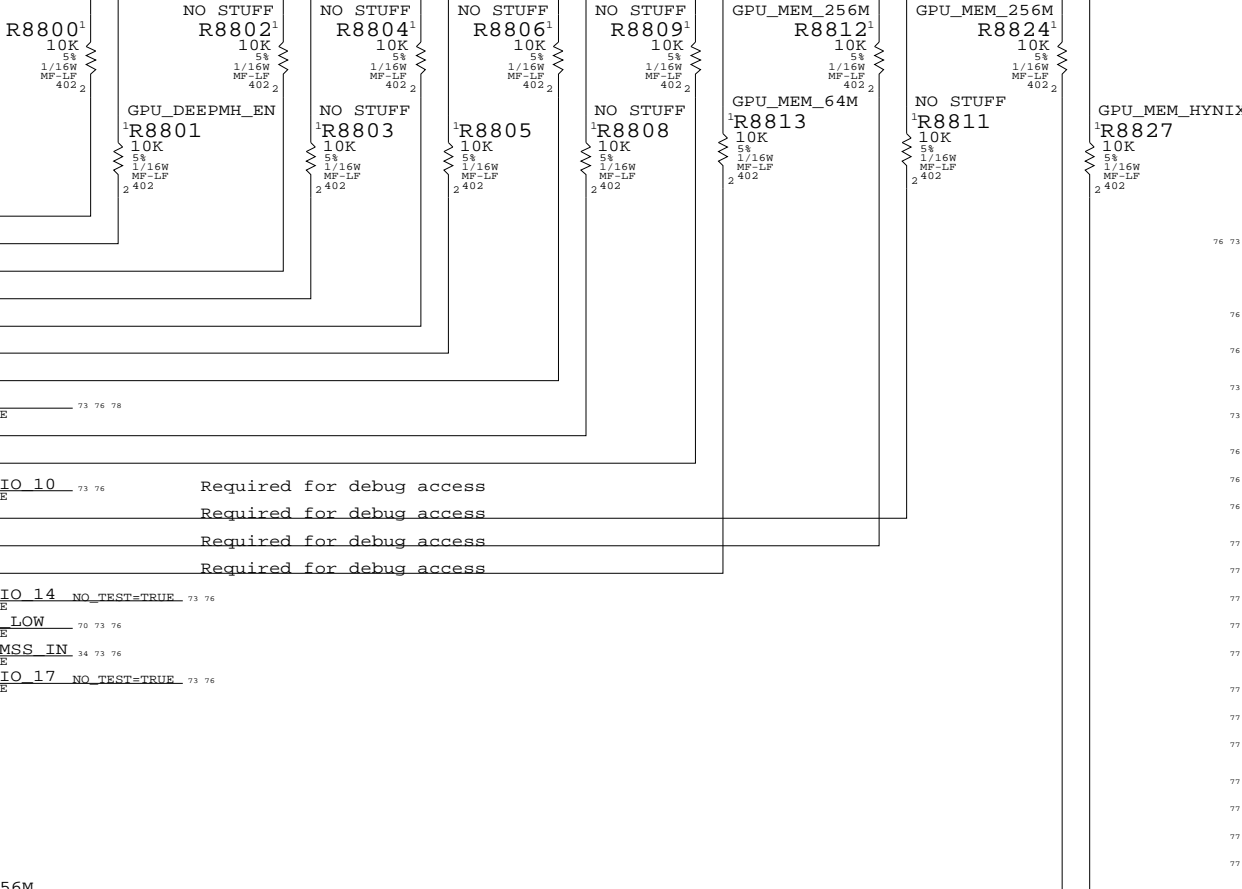
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. B
	SCALE NONE	SHEET 72 OF 86	



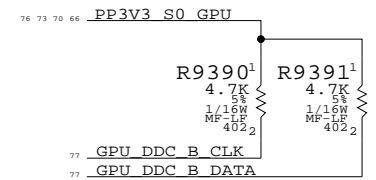
ROMCFGID[3..0]
 0000 = 128MB
 0010 = 256MB
 0100 = 64MB
 0110 = Reserved

76 73 70 66 PP3V3 S0 GPU



Renamed signals		
76 73 34 GPU_CLK27M	==	GPU_CLK27M
Unused signals		
76 73 NC_GPU_XTALOUT	==	NC_GPU_XTALOUT
76 73 NC_ATI_ROMCS_L	==	NC_ATI_ROMCS_L
73 72 NC_FB_A_MAL2	==	NC_FB_A_MAL2
73 72 NC_FB_B_MAL2	==	NC_FB_B_MAL2
76 73 NC_GPU_GENERICA	==	NC_GPU_GENERICA
76 73 NC_GPU_GENERICB	==	NC_GPU_GENERICB
76 73 NC_GPU_GENERICC	==	NC_GPU_GENERICC
73 72 NC_GPU_VGA_R	==	NC_GPU_VGA_R
73 72 NC_GPU_VGA_G	==	NC_GPU_VGA_G
73 72 NC_GPU_VGA_B	==	NC_GPU_VGA_B
73 72 TP_GPU_VGA_HSYNC	==	TP_GPU_VGA_HSYNC
73 72 TP_GPU_VGA_VSYNC	==	TP_GPU_VGA_VSYNC
73 72 NC_GPU_TV_Y	==	NC_GPU_TV_Y
73 72 NC_GPU_TV_C	==	NC_GPU_TV_C
73 72 NC_GPU_TV_COMP	==	NC_GPU_TV_COMP
73 72 NC_LVDS_U_DATAP<3>	==	NC_LVDS_U_DATAP<3>
73 72 NC_LVDS_U_DATAN<3>	==	NC_LVDS_U_DATAN<3>
73 72 NC_LVDS_L_DATAP<3>	==	NC_LVDS_L_DATAP<3>
73 72 NC_LVDS_L_DATAN<3>	==	NC_LVDS_L_DATAN<3>
76 73 NC_ATI_DVPCCLK	==	NC_ATI_DVPCCLK
76 NC_ATI_DVPCNTL<2..0>	==	ATI_DVPCNTL<2..0>
76 NC_ATI_DVPPDATA<15..0>	==	ATI_DVPPDATA<15..0>

Required for debug access
 TP_ATI_DVPPDATA<23..16> == ATI_DVPPDATA<23..16>
 Also required: GPIO10 - GPIO13

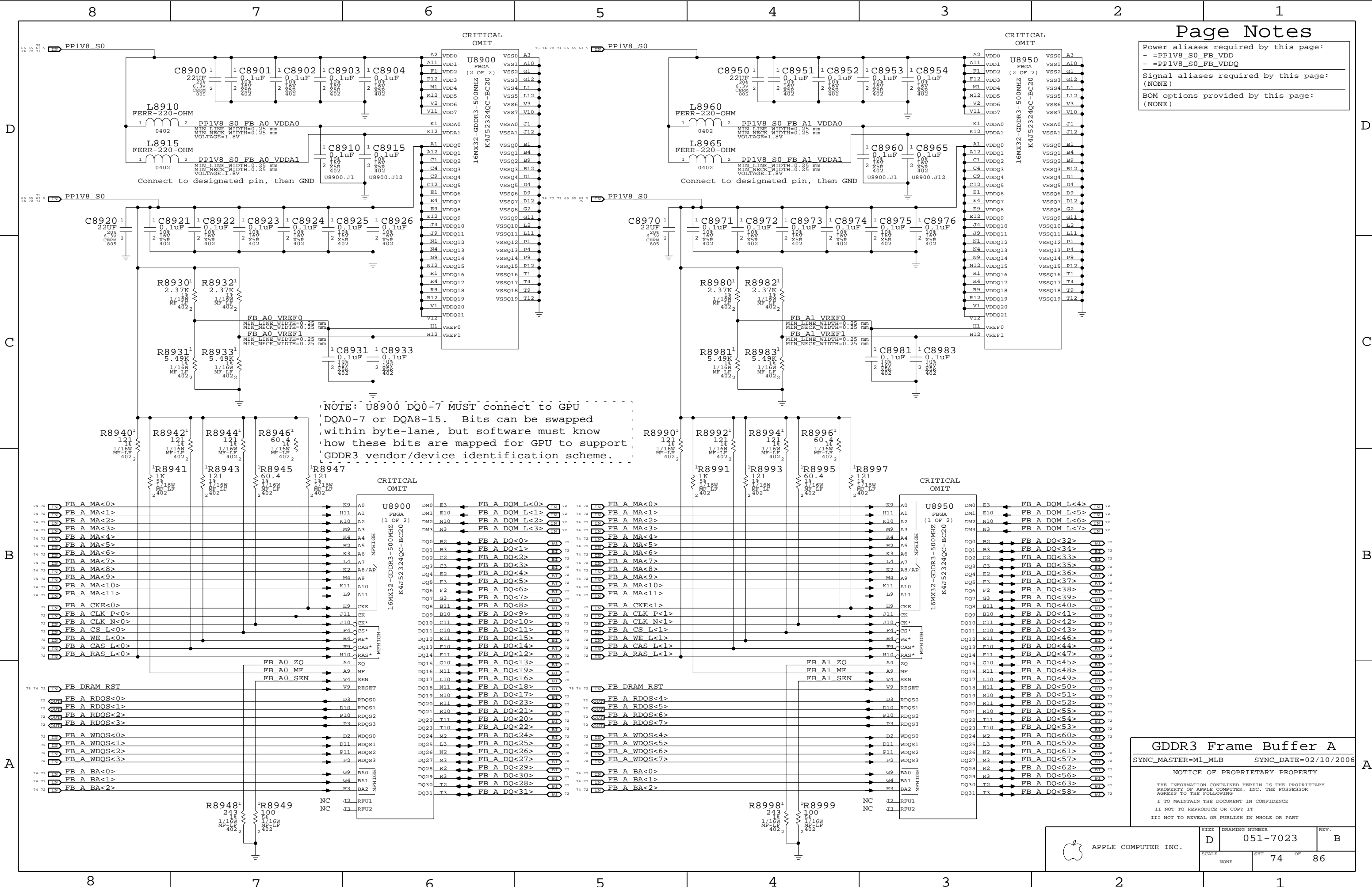


GPU Straps
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT 73 OF 86		
NONE			

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.



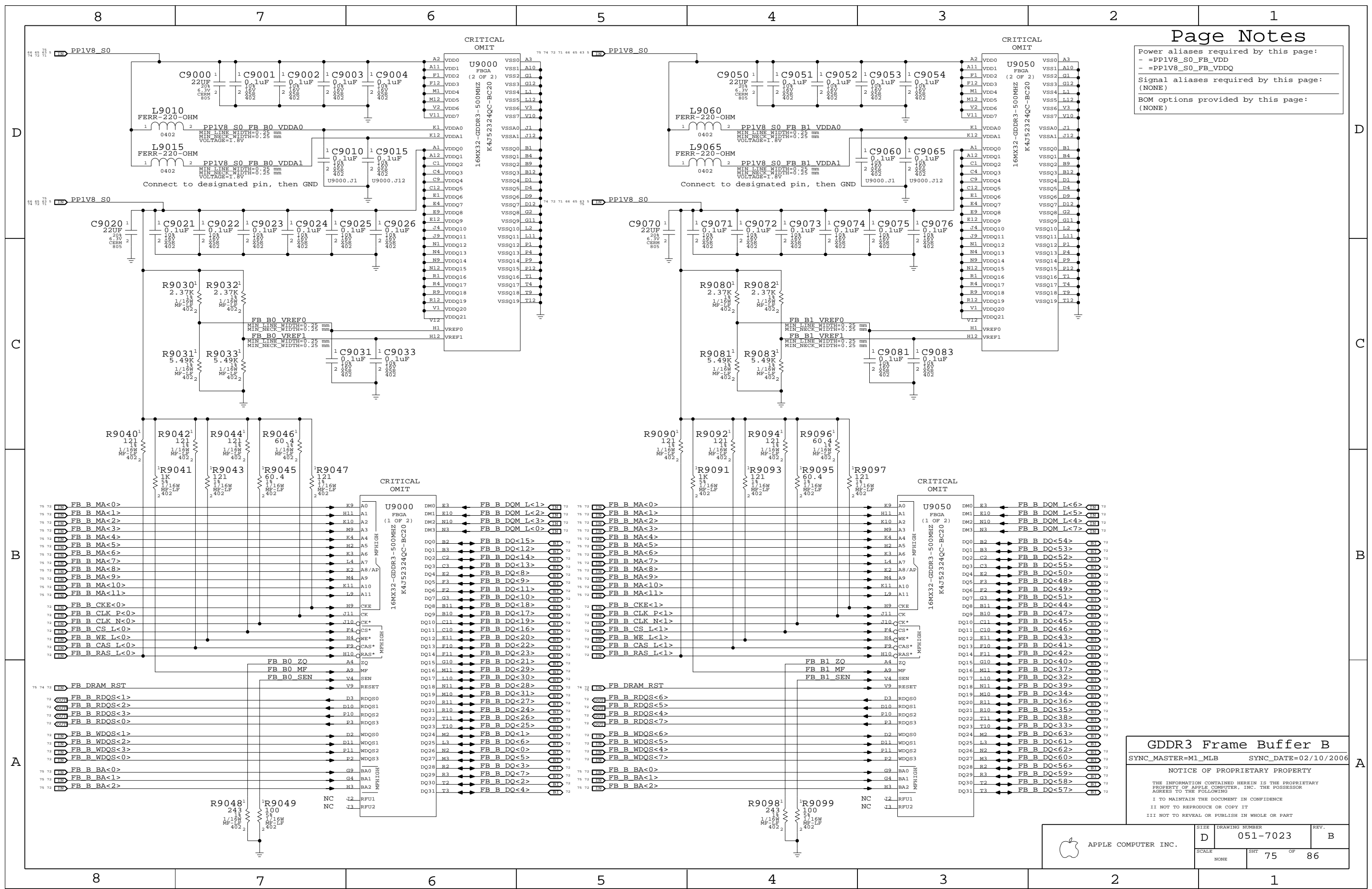
GDDR3 Frame Buffer A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	NONE	SHT	75 OF 86

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D

C

B

A

- 73 NC GPU GPIO 18 AE13 GPIO_18
- 73 NC GPU GPIO 19 AF13 GPIO_19
- 73 NC GPU GPIO 20 AF9 GPIO_20
- 73 NC GPU GPIO 21 AG7 GPIO_21
- 73 NC GPU GPIO 22 AE10 GPIO_22
- 73 NC GPU GPIO 23 AE9 GPIO_23
- 73 GPU_MEM_256M AF7 GPIO_24
- 73 NC GPU GPIO 25 AF8 GPIO_25
- 73 NC GPU GPIO 26 AH6 GPIO_26
- 73 GPU_MEMID AF10 GPIO_27
- 73 NC GPU GPIO 28 AG10 GPIO_28
- 73 NC GPU GPIO 29 AH9 GPIO_29
- 73 NC GPU GPIO 30 AW8 GPIO_30
- 73 NC GPU GPIO 31 AH8 GPIO_31
- 73 NC GPU GPIO 32 AG9 GPIO_32
- 73 NC GPU GPIO 33 AH7 GPIO_33
- 73 NC GPU GPIO 34 AG8 GPIO_34

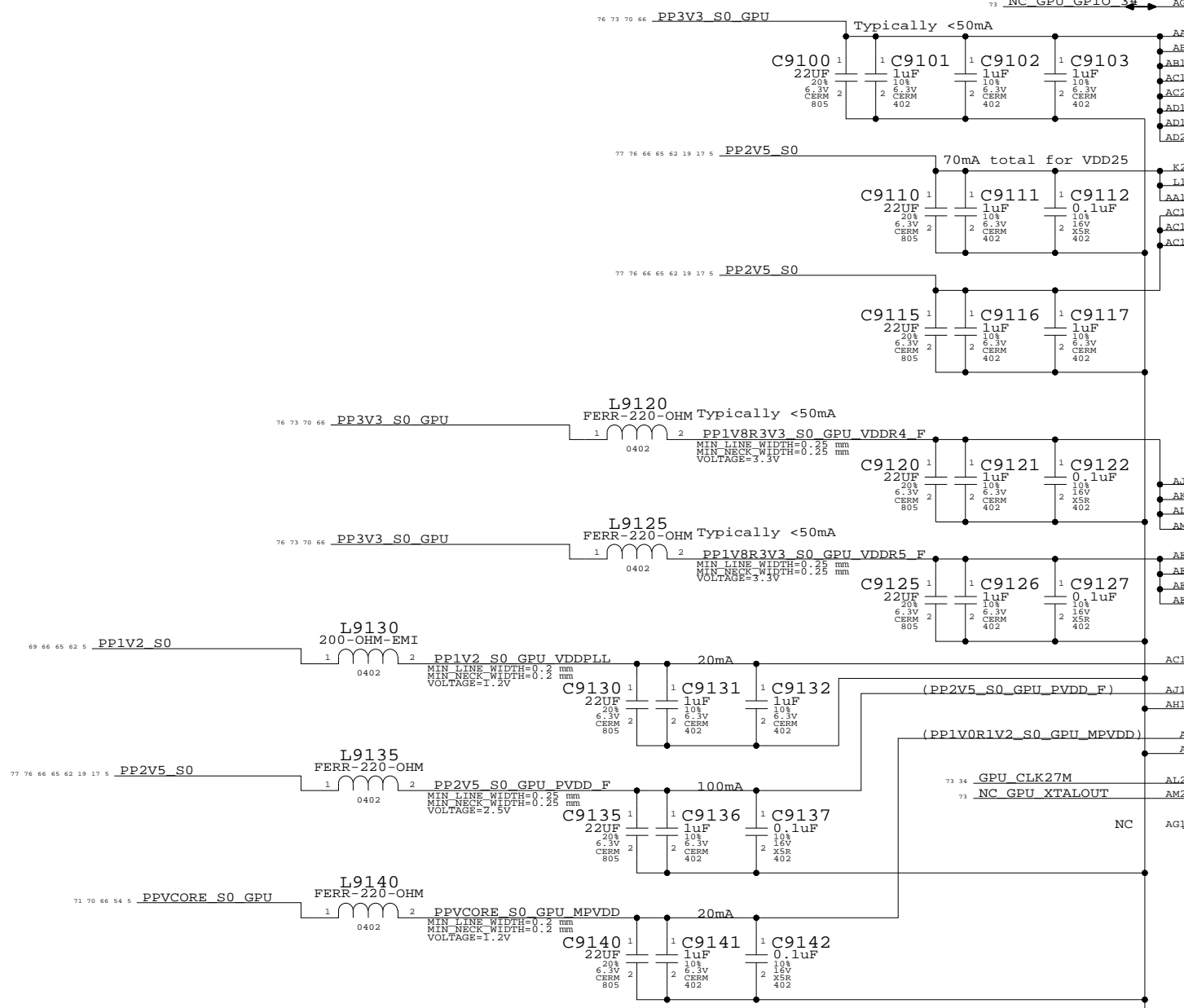
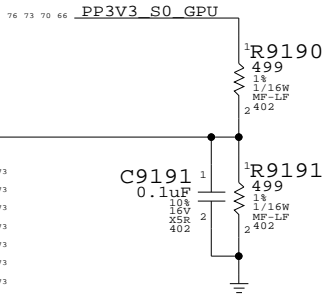
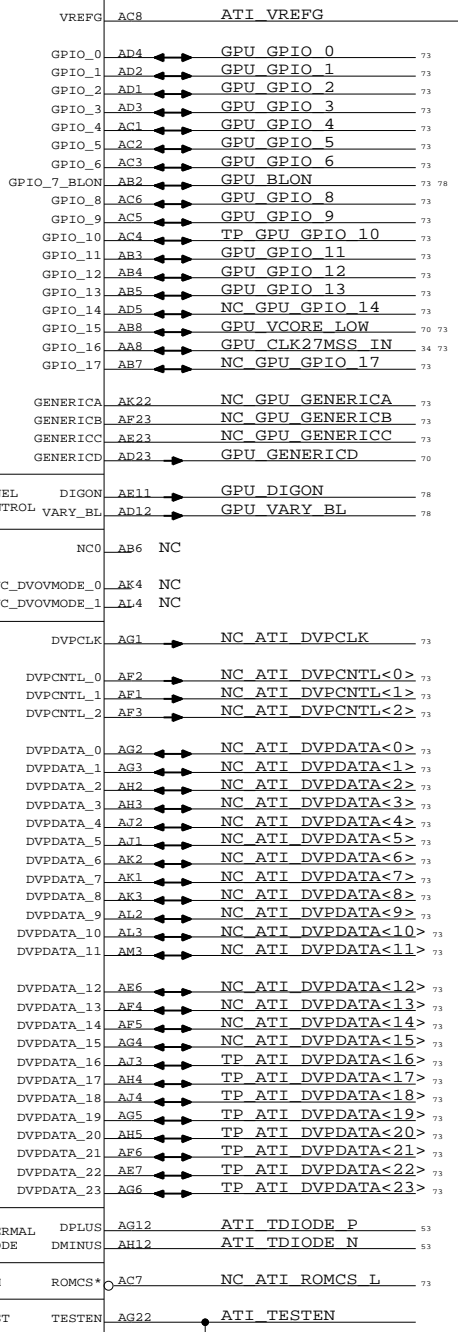
OMIT
 U8400
 M56P
 BGA
 (6 OF 7)

GENERAL PURPOSE I/O

PANEL CONTROL

VIP HOST / EXTERNAL TMDS

PLL & XTAL



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	B
SCALE	SHT	OF	
NONE	76	86	

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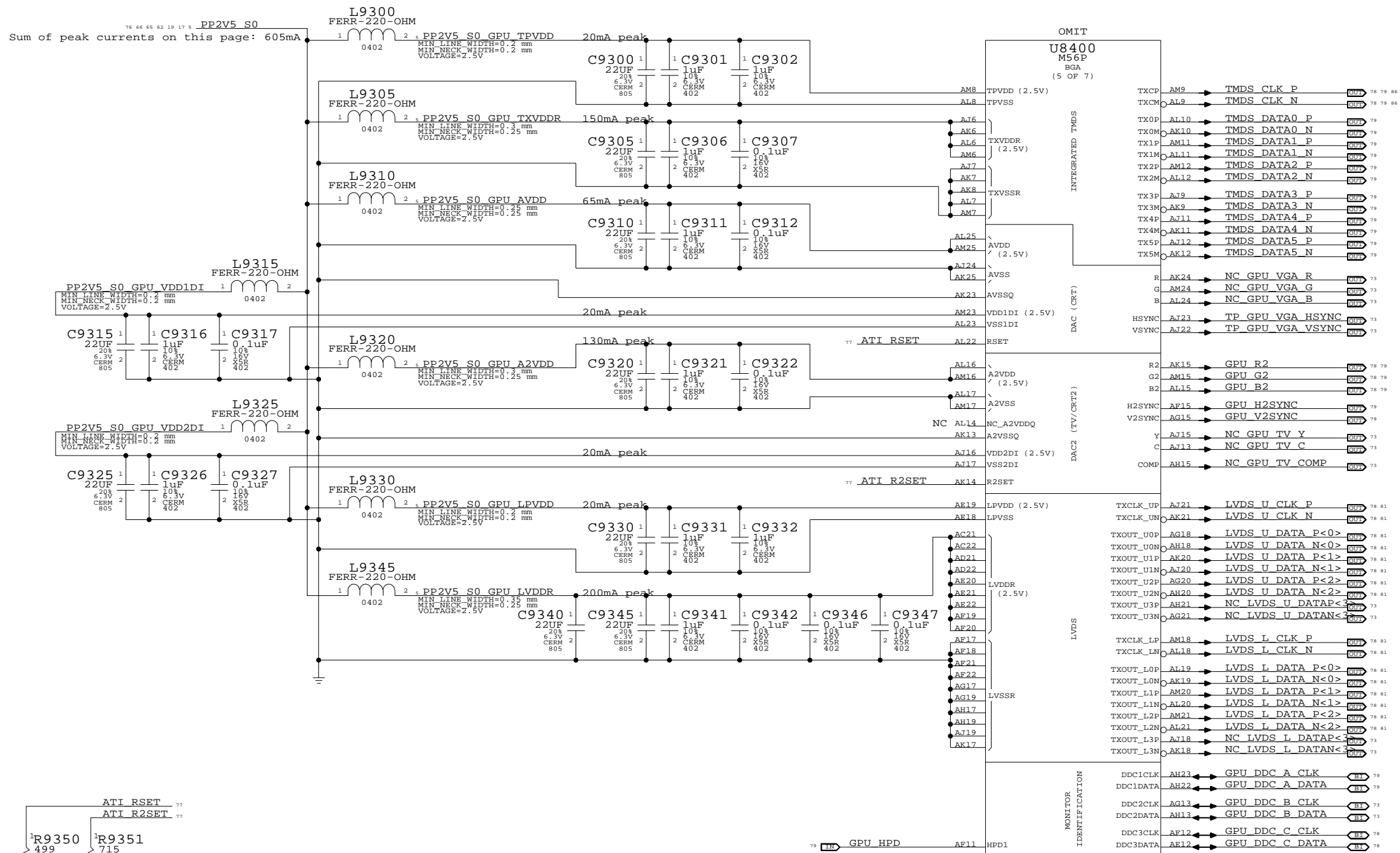
Page Notes

Power aliases required by this page:

- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

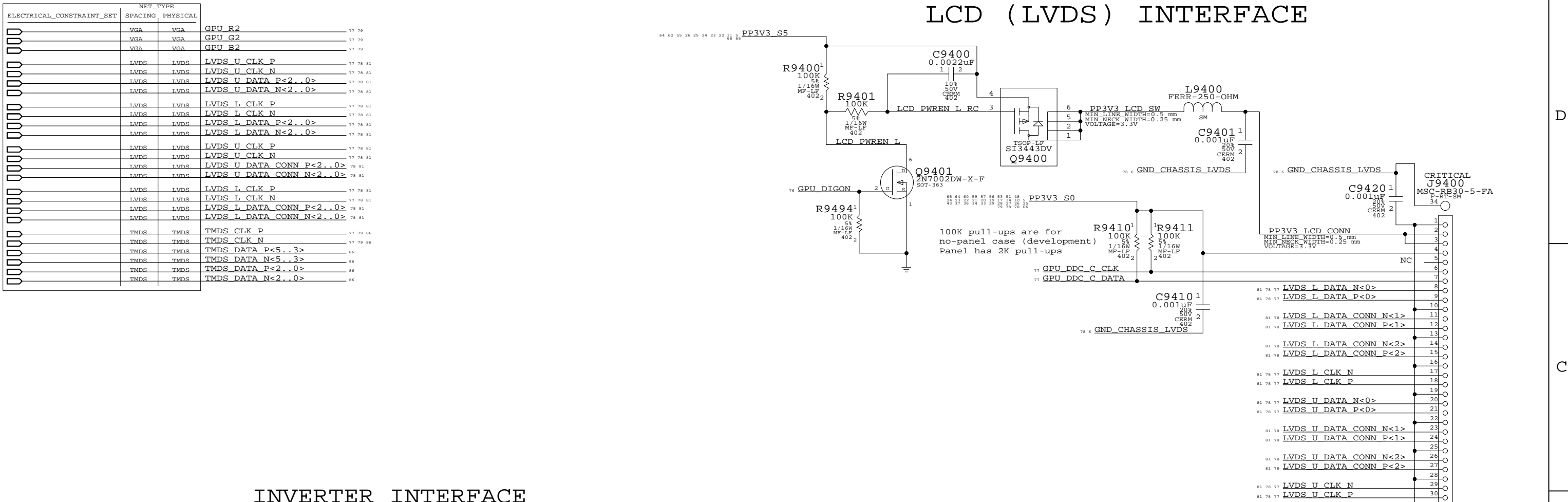
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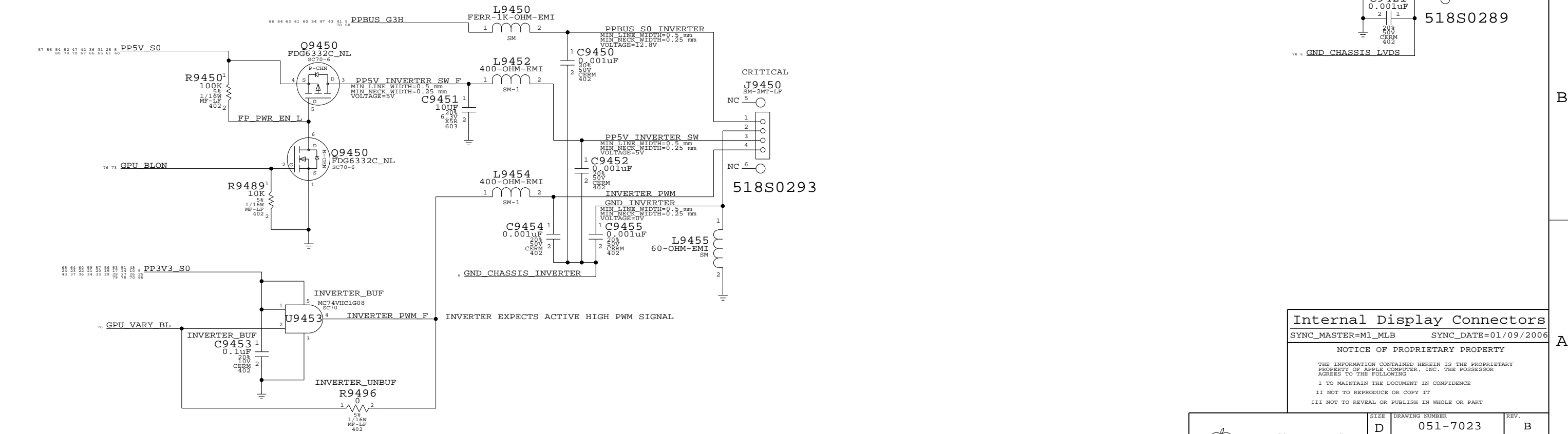
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	NONE	SHT	77 OF 86

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL		
	VGA	VGA	GPU_R2	77 79
	VGA	VGA	GPU_G2	77 79
	VGA	VGA	GPU_B2	77 79
	LVDS	LVDS	LVDS_U_CLK_P	77 78 81
	LVDS	LVDS	LVDS_U_CLK_N	77 78 81
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	77 78 81
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	77 78 81
	LVDS	LVDS	LVDS_L_CLK_P	77 78 81
	LVDS	LVDS	LVDS_L_CLK_N	77 78 81
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	77 78 81
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	77 78 81
	LVDS	LVDS	LVDS_U_CLK_P	77 78 81
	LVDS	LVDS	LVDS_U_CLK_N	77 78 81
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	78 81
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	78 81
	LVDS	LVDS	LVDS_L_CLK_P	77 78 81
	LVDS	LVDS	LVDS_L_CLK_N	77 78 81
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	78 81
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	78 81
	TMDS	TMDS	TMDS_CLK_P	77 79 86
	TMDS	TMDS	TMDS_CLK_N	77 79 86
	TMDS	TMDS	TMDS_DATA_P<5..3>	86
	TMDS	TMDS	TMDS_DATA_N<5..3>	86
	TMDS	TMDS	TMDS_DATA_P<2..0>	86
	TMDS	TMDS	TMDS_DATA_N<2..0>	86



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=01/09/2006

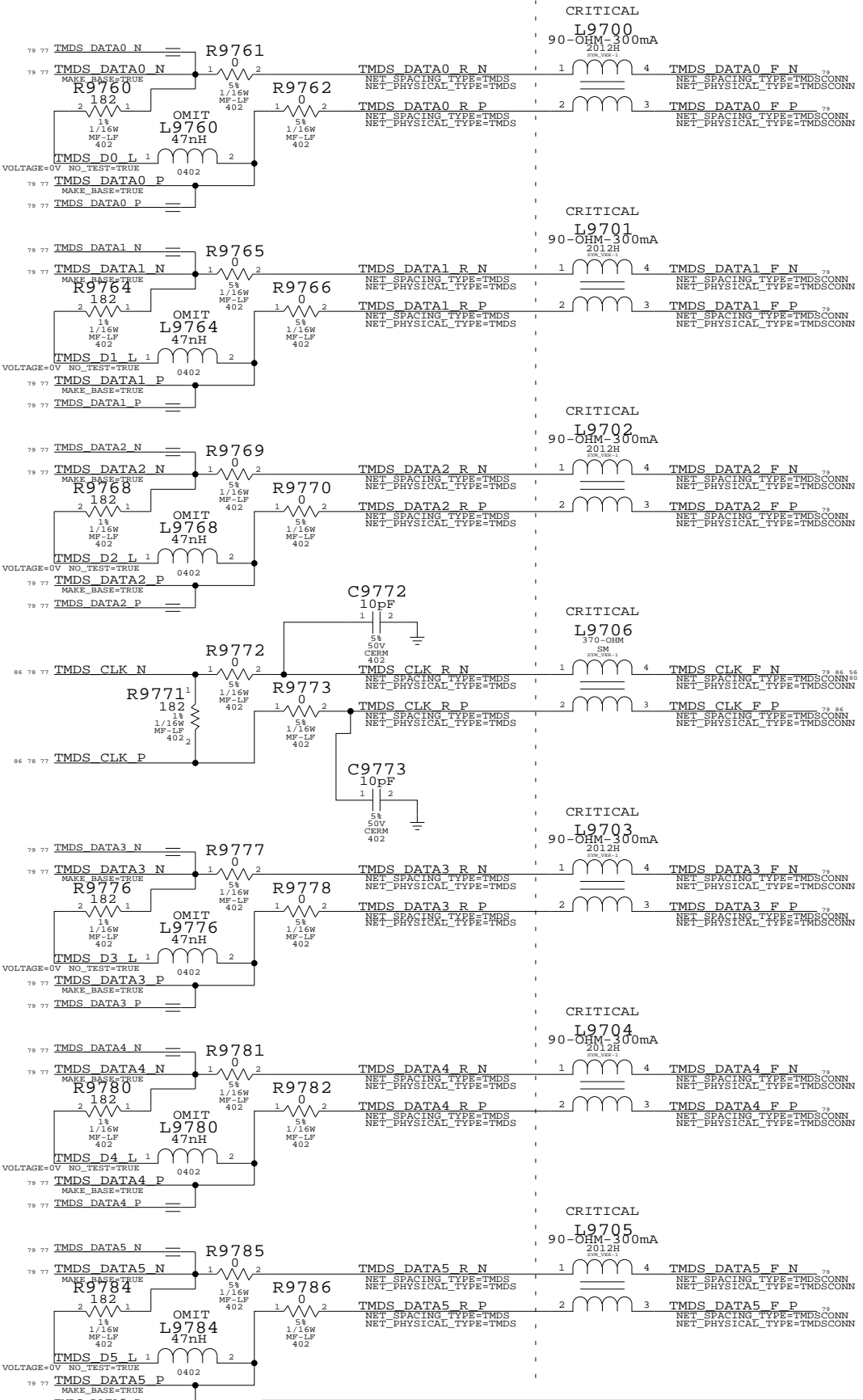
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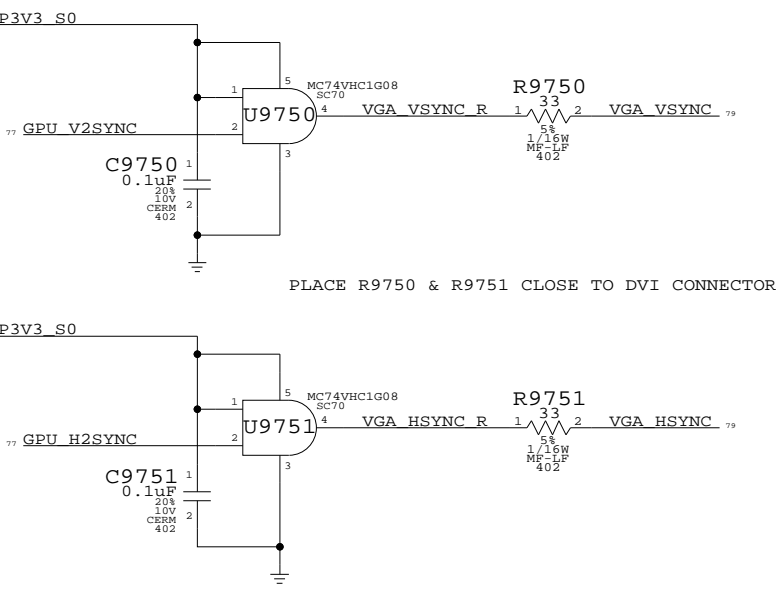
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	NONE	SHT	78 OF 86

TMDS Filtering

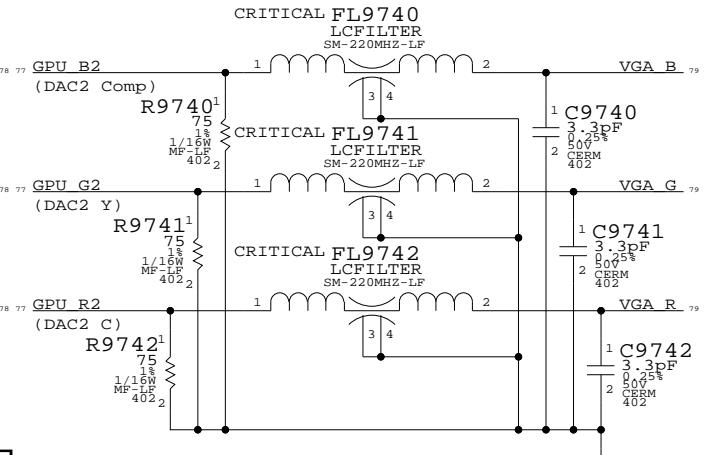
Place series R's and differential termination close to GPU, common mode chokes near connector.



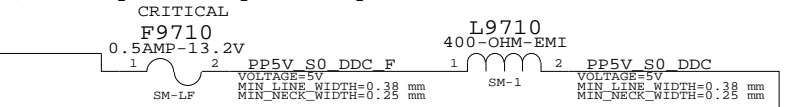
VGA SYNC BUFFERS



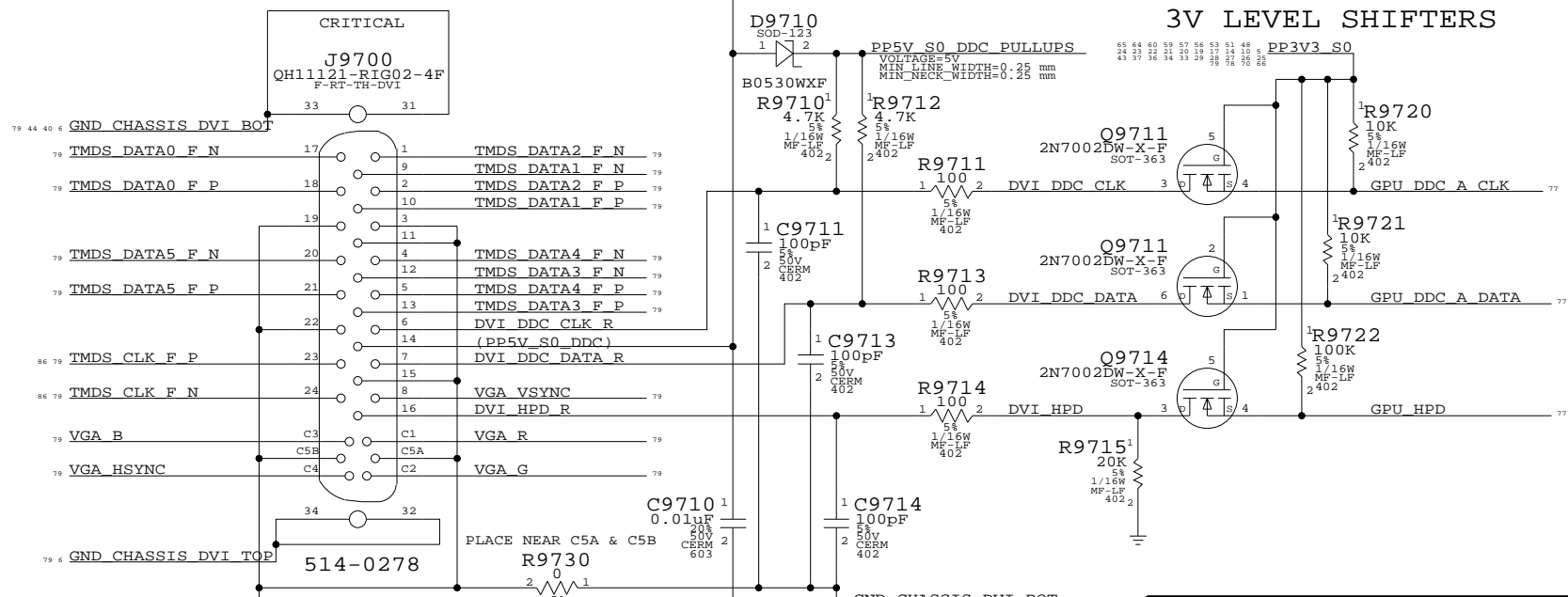
ANALOG FILTERING PLACE CLOSE TO CONNECTOR



DVI DDC CURRENT LIMIT (55mA requirement per DVI spec)



DVI INTERFACE



External Display Connector

SYNC_MASTER=M1_MLB SYNC_DATE=11/18/2005

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0419	6	IND, 47NH, 2%, 1.30HM, 0402, LF	L9760, L9764, L9768, L9776, L9780, L9784	CRITICAL	TMDS_PEAKING_IND
116S0004	6	RES, 00HM, 5%, 0402, LF	R9760, R9764, R9768, R9776, R9780, R9784		TMDS_NO_PEAKING_IND

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7023	REV.: B
	SCALE: NONE	SHEET: 79 OF 86	

8

7

6

5

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3

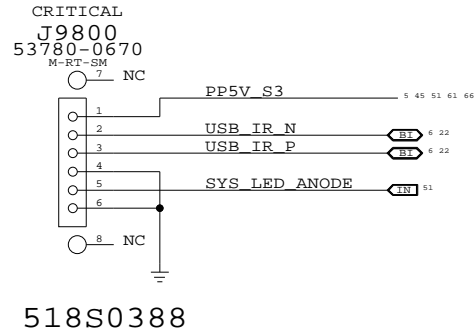
2

1

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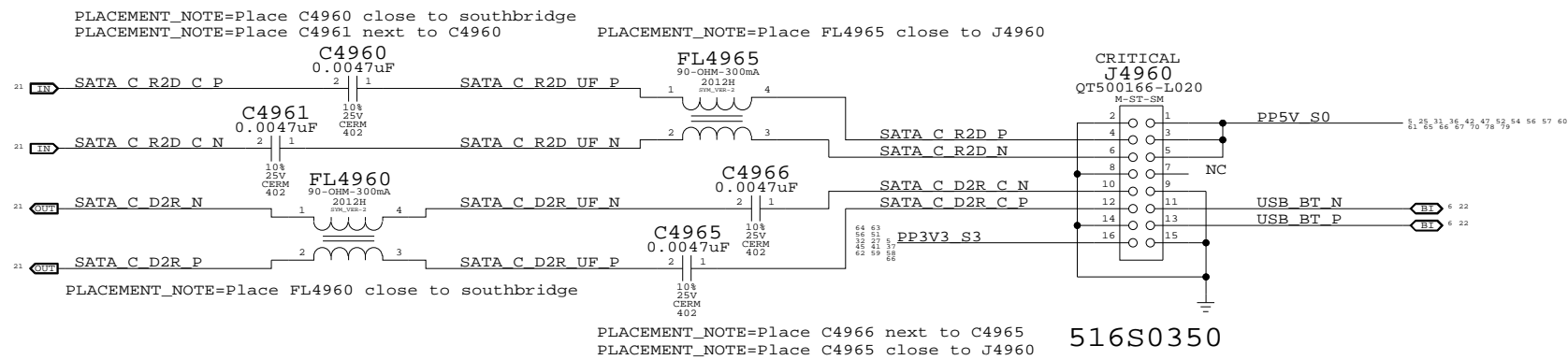
IR & Sleep LED Connector



C

C

Bluetooth (M13P) & SATA HDD Flex Connector



B

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M9 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	B
SCALE	SHT 80 OF 86		
NONE			

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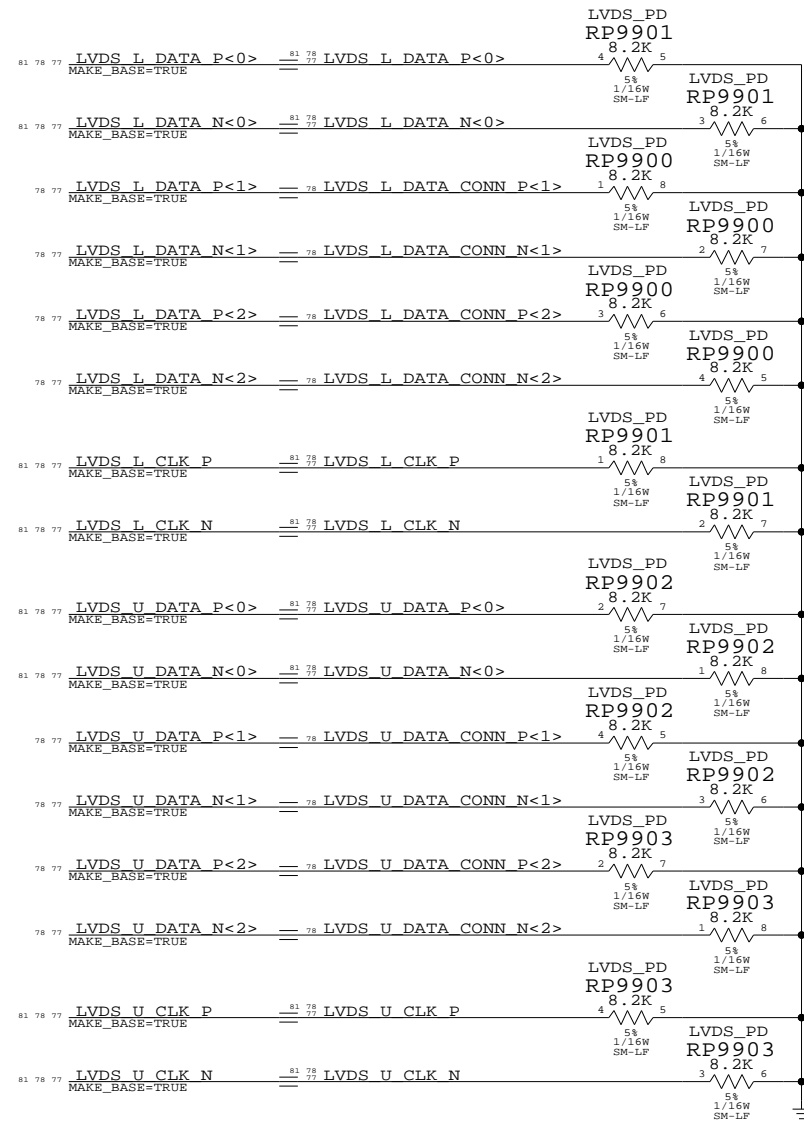
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LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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SCALE	SHT		OF
NONE	81		86

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Revision History

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Revision History	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	82	86	

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR	*	=3:1_SPACING
FSB_ADDR2ADDR	*	=2:1_SPACING
FSB_ADSTB	*	=3:1_SPACING
FSB_ADDR2ADSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA	*	=3:1_SPACING
FSB_DATA2DATA	*	=2:1_SPACING
FSB_DSTB	*	=3:1_SPACING
FSB_DATA2DSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_COMMON	*	=2:1_SPACING

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CPU_2T01	*	=2:1_SPACING
CPU_COMP	*	25 MIL
CPU_GTLREF	*	25 MIL
CPU_ITP	*	=2:1_SPACING
CPU_VCCSENSE	*	25 MIL

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_CLK2MEM	*	=4:1_SPACING
MEM_CTRL2CTRL	*	=2:1_SPACING
MEM_CTRL2MEM	*	=3:1_SPACING
MEM_CMD2CMD	*	=1.5:1_SPACING
MEM_CMD2MEM	*	=3:1_SPACING
MEM_DATA2DATA	*	=1.5:1_SPACING
MEM_DATA2MEM	*	=3:1_SPACING
MEM_DQS2MEM	*	=3:1_SPACING
MEM_2OTHER	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CTRL2MEM
MEM_CLK	MEM_CMD	*	MEM_CMD2MEM
MEM_CLK	MEM_DATA	*	MEM_DATA2MEM
MEM_CLK	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2MEM
MEM_CTRL	MEM_DATA	*	MEM_DATA2MEM
MEM_CTRL	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCIE	*	20 MIL
DMI	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
IDE	*	=1.8:1_SPACING
SATA	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
AUDIO	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
USB2	*	=4:1_SPACING
USB2_2CLK	*	25 MIL

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
SMB	*	=3:1_SPACING
SPI	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	*	25 MIL
CLK_PCIE	*	20 MIL
CLK_MED	*	20 MIL
CLK_SLOW	*	10 MIL

Napa Platform Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHEET	OF	
NONE	83	86	

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FB_ADCTRL	*	=2.5:1_SPACING
FB_CLK	*	=2.5:1_SPACING
FB_DATA	*	=2.5:1_SPACING

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
 CTRL lines are 55-ohm single-ended impedance.
 DQ/DQM/DQS lines are 40-ohm single-ended impedance.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
 NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
 SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS	*	=3:1_SPACING
TMDS	*	=3:1_SPACING
VGA	*	15 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS_PAIR2PAIR	*	25 MIL
TMDS_PAIR2PAIR	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedance.
 LVDS and TMDS pairs should be kept at least 25 mils apart.
 Ground shields can be used around each pair if spacing cannot be met.
 VGA should be routed as close to 75-ohms single-ended impedance as possible.
 VGA signals should be kept at least 15 mils from other traces.
 Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
 SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
ENET	*	=3:1_SPACING
FW	*	=3:1_SPACING

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCI	*	=2:1_SPACING

More System Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF	REV.
NONE	84	86	

M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA				MM	15.2
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM				
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
50_OHM_SE	TOP, BOTTOM	Y	0.124 MM	0.124 MM				
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM				
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM				
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
35_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.230 MM				
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM				
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
35_55_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.100 MM				
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM	
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM	
75_OHM_DIFF	TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM	
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM	
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM	
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM	
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM	
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM	

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
DEFAULT	*	0.1 MM
STANDARD	*	=DEFAULT
BGA_P1MM	*	=DEFAULT
BGA_P2MM	*	=DEFAULT
BGA_P3MM	*	=DEFAULT

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	*	0.15 MM
1.8:1_SPACING	*	0.18 MM
2:1_SPACING	*	0.2 MM
2.5:1_SPACING	*	0.25 MM
3:1_SPACING	*	0.3 MM
4:1_SPACING	*	0.4 MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	ISL2, ISL11	0.1 MM
1.8:1_SPACING	ISL2, ISL11	0.1 MM
2:1_SPACING	ISL2, ISL11	0.1 MM
2.5:1_SPACING	ISL2, ISL11	0.1 MM
3:1_SPACING	ISL2, ISL11	0.1 MM
4:1_SPACING	ISL2, ISL11	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	ISL2, ISL11	0.1 MM
CLK_PCIE	ISL2, ISL11	0.1 MM
CLK_MED	ISL2, ISL11	0.1 MM
CLK_SLOW	ISL2, ISL11	0.1 MM
CPU_COMP	ISL2, ISL11	0.1 MM
CPU_GTLREF	ISL2, ISL11	0.1 MM
CPU_VCCSENSE	ISL2, ISL11	0.1 MM
DMI	ISL2, ISL11	0.1 MM
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM
MEM_2OTHER	ISL2, ISL11	0.1 MM
PCIE	ISL2, ISL11	0.1 MM
SATA	ISL2, ISL11	0.1 MM
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM
VGA	ISL2, ISL11	0.1 MM

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR OVERRIDE	*	=2:1_SPACING
FSB_ADDR2ADDR OVERRIDE	*	=STANDARD
FSB_ADSTB OVERRIDE	*	=2:1_SPACING
FSB_ADDR2ADSTB OVERRIDE	*	=2:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA OVERRIDE	*	=2:1_SPACING
FSB_DATA2DATA OVERRIDE	*	=STANDARD
FSB_DSTB OVERRIDE	*	=2:1_SPACING
FSB_DATA2DSTB OVERRIDE	*	=2:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_2OTHER OVERRIDE	*	0.5 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCI_2PCI OVERRIDE	*	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

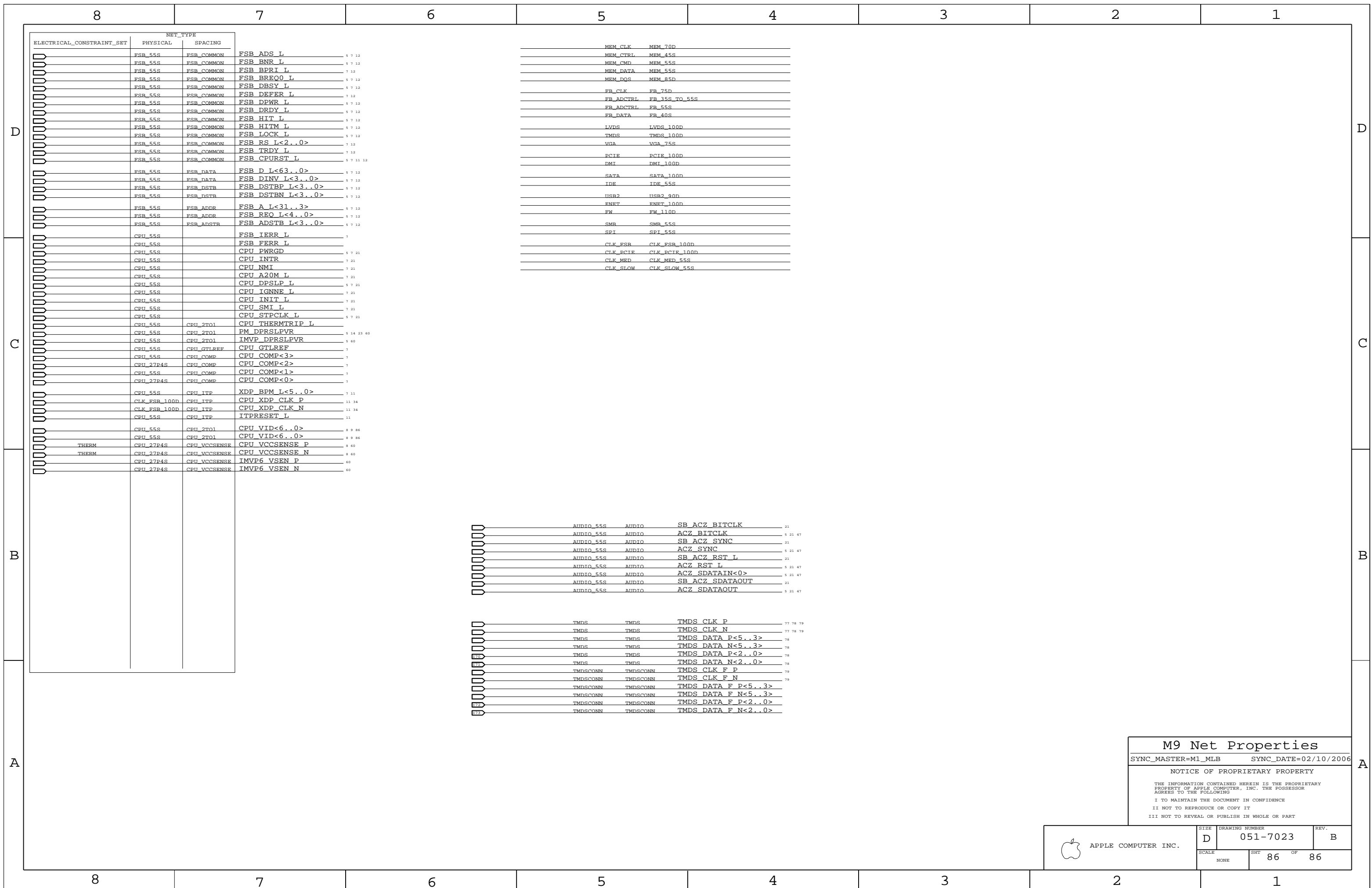
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI
PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.100 MM	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
FSB_55S	FSB_COMMON	FSB ADS L
FSB_55S	FSB_COMMON	FSB BNR L
FSB_55S	FSB_COMMON	FSB BPRI L
FSB_55S	FSB_COMMON	FSB BREQ0 L
FSB_55S	FSB_COMMON	FSB DBSY L
FSB_55S	FSB_COMMON	FSB DEFER L
FSB_55S	FSB_COMMON	FSB DPWR L
FSB_55S	FSB_COMMON	FSB DRDY L
FSB_55S	FSB_COMMON	FSB HIT L
FSB_55S	FSB_COMMON	FSB HITM L
FSB_55S	FSB_COMMON	FSB LOCK L
FSB_55S	FSB_COMMON	FSB RS L<2..0>
FSB_55S	FSB_COMMON	FSB TRDY L
FSB_55S	FSB_COMMON	FSB CPURST L
FSB_55S	FSB_DATA	FSB D L<63..0>
FSB_55S	FSB_DATA	FSB DINV L<3..0>
FSB_55S	FSB_DSTR	FSB DSTBP L<3..0>
FSB_55S	FSB_DSTR	FSB DSTBN L<3..0>
FSB_55S	FSB_ADDR	FSB A L<31..3>
FSB_55S	FSB_ADDR	FSB REQ L<4..0>
FSB_55S	FSB_ADSTR	FSB ADSTB L<3..0>
CPU_55S		FSB IERR L
CPU_55S		FSB FERR L
CPU_55S		CPU PWRGD
CPU_55S		CPU INTR
CPU_55S		CPU NMI
CPU_55S		CPU A20M L
CPU_55S		CPU DPSLP L
CPU_55S		CPU IGNNE L
CPU_55S		CPU INIT L
CPU_55S		CPU SMI L
CPU_55S		CPU STPCLK L
CPU_55S	CPU_2T01	CPU THERMTRIP L
CPU_55S	CPU_2T01	PM DPRSLPVR
CPU_55S	CPU_2T01	IMVP DPRSLPVR
CPU_55S	CPU_GTLREF	CPU GTLREF
CPU_55S	CPU_COMP	CPU COMP<3>
CPU_27P4S	CPU_COMP	CPU COMP<2>
CPU_55S	CPU_COMP	CPU COMP<1>
CPU_27P4S	CPU_COMP	CPU COMP<0>
CPU_55S	CPU_ITP	XDP BPM L<5..0>
CLK_FSB_100D	CPU_ITP	CPU XDP CLK P
CLK_FSB_100D	CPU_ITP	CPU XDP CLK N
CPU_55S	CPU_ITP	ITPRESET L
CPU_55S	CPU_2T01	CPU VID<6..0>
CPU_55S	CPU_2T01	CPU VID<6..0>
THERM	CPU_27P4S	CPU VCCSENSE P
THERM	CPU_27P4S	CPU VCCSENSE N
	CPU_27P4S	IMVP6 VSEN P
	CPU_27P4S	IMVP6 VSEN N

MEM_CLK	MEM_70D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIE	PCIE_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

AUDIO_55S	AUDIO	SB ACZ BITCLK	21
AUDIO_55S	AUDIO	ACZ BITCLK	5 21 47
AUDIO_55S	AUDIO	SB ACZ SYNC	21
AUDIO_55S	AUDIO	ACZ SYNC	5 21 47
AUDIO_55S	AUDIO	SB ACZ_RST L	21
AUDIO_55S	AUDIO	ACZ_RST L	5 21 47
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 47
AUDIO_55S	AUDIO	SB ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 47
TMDS	TMDS	TMDS_CLK P	77 78 79
TMDS	TMDS	TMDS_CLK N	77 78 79
TMDS	TMDS	TMDS_DATA P<5..3>	78
TMDS	TMDS	TMDS_DATA N<5..3>	78
TMDS	TMDS	TMDS_DATA P<2..0>	78
TMDS	TMDS	TMDS_DATA N<2..0>	78
TMDSCONN	TMDSCONN	TMDS_CLK F P	79
TMDSCONN	TMDSCONN	TMDS_CLK F N	79
TMDSCONN	TMDSCONN	TMDS_DATA F P<5..3>	79
TMDSCONN	TMDSCONN	TMDS_DATA F N<5..3>	79
TMDSCONN	TMDSCONN	TMDS_DATA F P<2..0>	79
TMDSCONN	TMDSCONN	TMDS_DATA F N<2..0>	79

M9 Net Properties
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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