

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, CANNAREGIO, K20, DVT1

12/12/08

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
31		657084	ENGINEERING RELEASED	12/12/08	?

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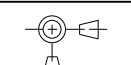
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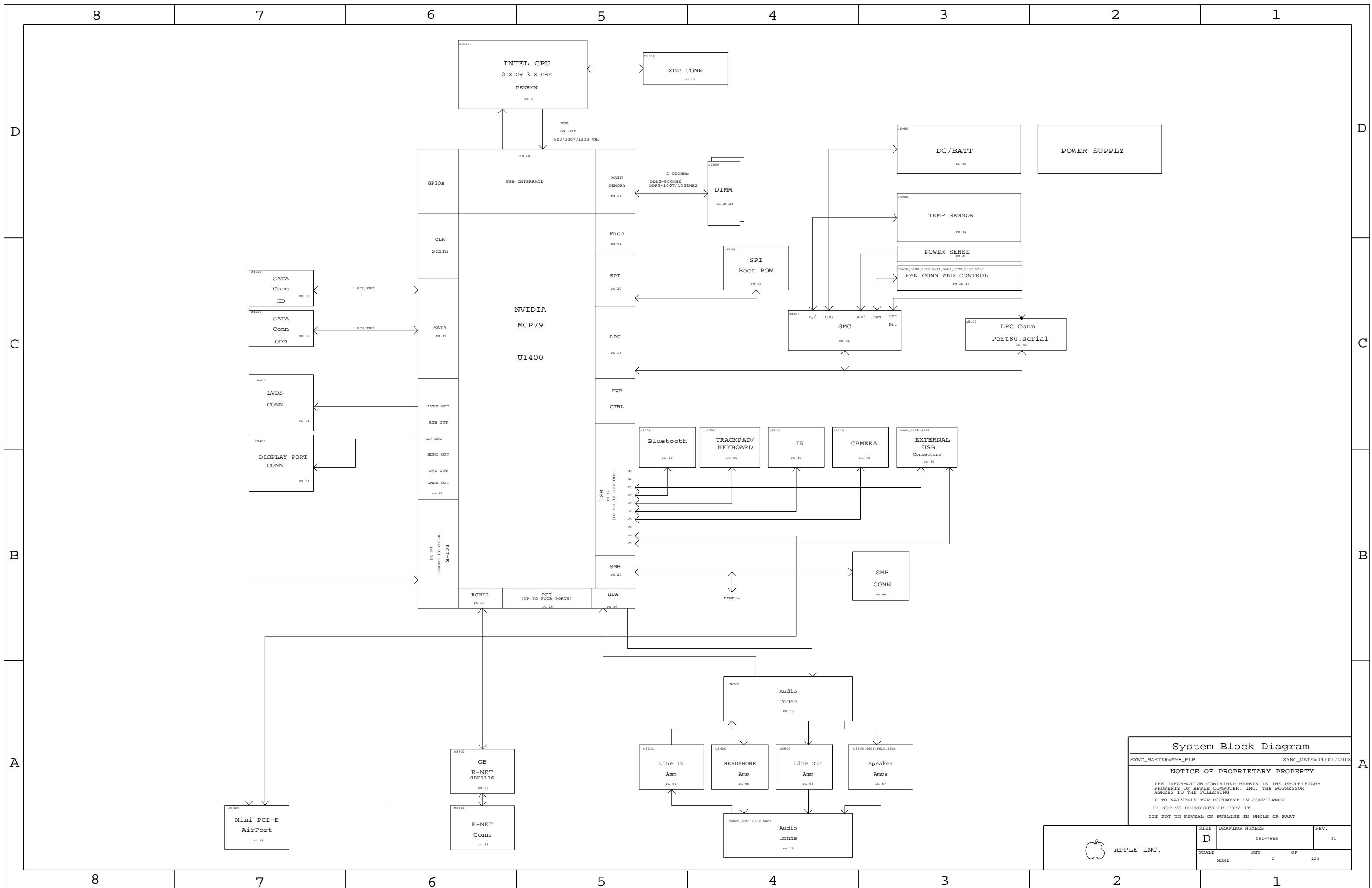
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98	PROJECT SPECIFIC CONNS	N/A	N/A

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7656	1	SCHEM, CANNAREGIO, K20	SCH	CRITICAL	
820-2390	1	PCBF, CANNAREGIO, K20	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST MODIFIED=Fri Dec 12 16:50:42 2008

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X.XXX ± _____		ENG APPD	MFG APPD		
ANGLES ± _____		QA APPD	DESIGNER		
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 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	DRAWING NUMBER	
				051-7656	REV. 31
				SHT 1 OF 123	



System Block Diagram

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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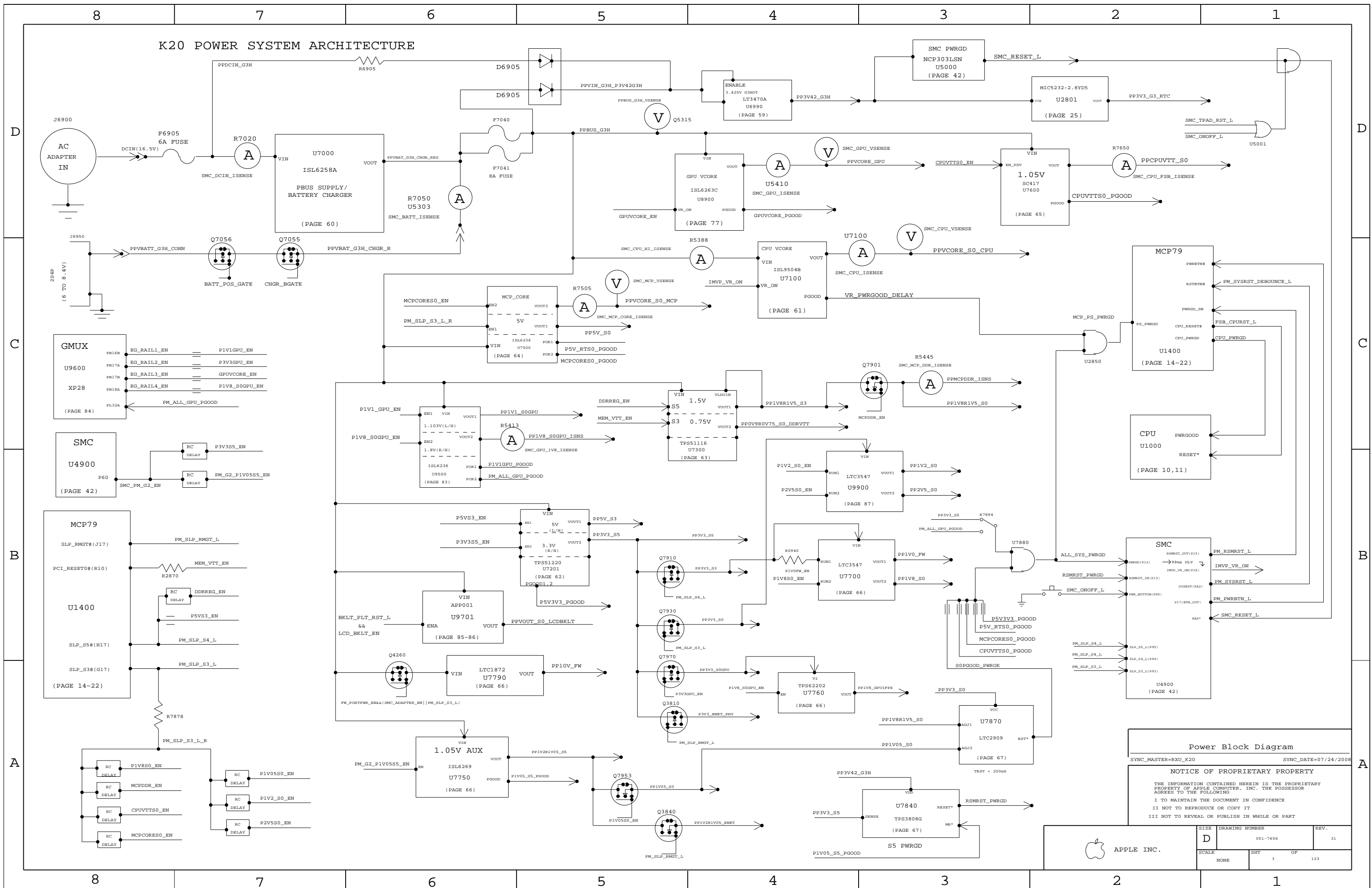
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	D	051-7656	31
SCALE	SHT	OF	
NONE	2	123	

K20 POWER SYSTEM ARCHITECTURE



Power Block Diagram
 SYNC_MASTER=RXU_K20 SYNC_DATE=07/24/2008

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APPLE INC.	SIZE: D SCALE: NONE	DRAWING NUMBER: 051-7656 SHEET: 3 OF 123	REV.: 31
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Proto:

See earlier schematics for info about proto changes

Pre-EVT:

See earlier schematics for info about Pre-EVT changes

EVT:

10/29/08

csa. 5 Added BKLT_PLL_NOT BOM option K20_COMMON2 BOM group. This stuffs R9713.
csa. 68 Changed net name on input to U6860 from PP3V3_S0_AUDIO to =PP3V3_S0_AUDIO.
See <rdar://problem/6327731> K20 PreEVT: iPhone headset detection test fail
csa. 97 Changed R9707 to 2.87K per <rdar://problem/6327135> Change R9707 to 2.87k, 1% resistor

10/29/08

csa. 9 Changed SH0924 to 870-1698 tall emi pogo pin.

11/5/08

csa. 4 Updated Revision History.
csa. 8 Tied =PP3V3_FW_FWPHY and =PP3V3_FW_P1V0FW aliases to PP3V3_S0.
csa. 9 Removed R0942 and R0943 which were for selecting from S0 or S3 for =PP3V3_FW_FWPHY.
Removed R0940 and R0941 which were for selecting from S0 or S3 for =PP3V3_FW_P1V0FW.
Tied =PP3V3_S3_GMUX alias to PP3V3_S3.
csa. 75 Changed U7500 from 353S2312 Intersil ISL6236 to 353S2203 TI SN0802043.
Changed TONSEL from GND to PP5V_S0_MCPREQ_VCC. This changes output frequencies to 200/300KHz for 5V/MCPCore.
Added C7562 330uF cap on =PPMPCORE_S0_REG.
Changed snubber resistors R7598 and R7599 to 1/6W 0402, APN 11480548.

csa. 87 Changed pulldown values to 10K on GPIO7_FBVDDQ_ALTV0, R8794.

Changed pulldowns R8792 and R8793 from 1K to 4.7K for power consumption.

csa. 90 Removed R9094. Replaced by R9678 on csa. 96 to tie to GMUX_S3_PD_GND.

csa. 96 Added Q9607 dual FET for disabling GMUX power sequence enable configuration pulldowns during S0.

Moved R9094 to R9678 and tied to GMUX_S3_PD_GND.

csa. 97 Changed R9707 to 2.67K 1%. This gives 22.5mA on LED current.

11/10/08

csa. 68 Changed R6885 from 0 ohms to 2.2K.

Changed C6885 from 470 pF to 0.0082 uF.

csa. 87 Changed R8792 and R8793 from 4.7K to 10K pulldowns on EG_LCD_PWR_EN and EG_BKLT_EN.

csa. 96 Changed R9678 pulldown on LCD_PWR_EN from 10K to 4.7K.

Removed BOM options on FET circuit for GMUX_S3_PD_GND.

Added R9684 NO STUFF 0 ohms to tie ALL_SYS_PWRGD to Q9607.

11/11/08

csa. 8 removed =PP3V3_S3_P1V0FW and =PP3V3_S3_BKL_VDDIO

csa. 41 changed R4160 from 274K to 200K <rdar://6292976>

csa. 68 changed R6885 from 0 ohm to 2.2K for Mic LPF

csa. 75 NO STUFF R7598, R7599, C7599 (snubbers)

csa. 87 changed R8795 from 1K to 10K pull down

csa. 96 NO STUFF R9677, C9695, STUFF R9684

11/12/08

csa. 5 removed MCP79 B01 from Module Parts table and added B03

csa. 39 added Bom table for J3900 (514-0636)

csa. 46 added Bom table for J4600, J4610 (514-0638)

csa. 94 added Bom table for J9400 (514-0637)

csa. 123 added Bom table for JC320 (514-0638)

11/13/08

csa. 1 change title to DVT

csa. 32 Added alternate table for J3200 (516S0709, Molex DIMM connector)

11/19/08

csa. 5 changed MCP79 B03 to 338S0710; change to binned G96 338S0714;

added PROD_DIGSMS and TPDT_DEBOUNCE to BOM groups

csa. 68 added bom option TPDT_BYPASS to R6865; TPDT_DEBOUNCE to U6860, C6861, R6860, R6862

csa. 97 changed Q9701 to 376S0757 <rdar://6383480>

11/25/08

csa. 5 changed BOM option MCP_B02 to MCP_B03; added BOM option GMUX_1V8

added Mag Layer alternate 155S0457 to Murata 155S0329

csa. 93 added BOM table for 16 LVDS termination resistors to select GMUX_2V5 or GMUX_1V8

added BOM option GMUX_2V5 to 8 parallel resistors so they'll be NO STUFFed for GMUX_1V8

csa. 97 reverted Q9701 to 376S0678 due to parts availability

csa. 99 added BOM table for R9900 to select either 2.5V output or 1.8V output

DVT:

12/02/08

Start of PVT.

csa. 5 removed JTAG_ALLDEV bom option to remove U0600, R0601, C0601, C0602

added 516-0213 (Molex TH SODIMM CONN) as alternate to 516-0201 (Foxconn)

added GMUX_JTAG_CONN bom option to the bom table

csa. 6 added GMUX_JTAG_CONN bom option to J0600

csa. 99 moved OMIT from R9900 to R9901 to select either 150K (GMUX_2V5) or 237K (GMUX_1V8)

12/03/08

csa. 32 removed redundant alternate table for J3200

csa. 97 Per radar 6383480, Change the FET Q9701 from APN: 376S0678 to 376S0757

diode D9701 from APN: 371S0551 to 371S0572

12/09/08

csa. 1 changed title to DVT(1)

csa. 26 NO STUFF C2690, R2690

csa. 32 Refreshed symbol for J3200 for update to BGA SODIMM conn.

csa. 54 changed R5498 to 4.02K for 1.4x gain and R5493 to 2.87K <rdar://6423810>

csa. 89 changed L8920 to 152S0955 (25A Isat); R8900 to 7.15K for 24.6A OCP <rdar://6423810>

12/12/08

csa. 1 changed title to DVT1

csa. 4 removed pre-EVT check in notes from Rev. History

csa. 99 changed text note to reflect 2.5V to 1.8V GMUX rail change

31
SYNC_MASTER=NA SYNC_DATE=NA

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	D	051-7656	31
	SCALE	SHT	OF
	NONE	4	123

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9728	PCBA,BEST,2.66,512SAM_VRAM,K20	K20_COMMON,EEE_4CM,CPU_2_66GHZ,FB_512_SAMSUNG
630-9727	PCBA,BEST,2.66,512QIM_VRAM,K20	K20_COMMON,EEE_4CM,CPU_2_66GHZ,FB_512_QIMONDA
630-9730	PCBA,BEST,2.93,512SAM_VRAM,K20	K20_COMMON,EEE_4CQ,CPU_2_93GHZ,FB_512_SAMSUNG
630-9729	PCBA,BEST,2.93,512QIM_VRAM,K20	K20_COMMON,EEE_4CP,CPU_2_93GHZ,FB_512_QIMONDA

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung
152S0684	152S0368		ALL	Maglayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cytec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to FW resistor
341S2367	341S2366		ALL	Macromix alt to SST
152S0876	152S0782		ALL	Maglayer alt to Delta
157S0058	157S0055		ALL	Delta alt to THE Magnetics
514-0612	514-0607		ALL	FUELINK ALT TO FORCORN S076
514-0613	514-0608		ALL	FUELINK ALT TO FORCORN S076
152S0684	152S0421		ALL	MSG LAYERS ALT TO VISHAY
152S0896	152S0518		ALL	MSG LAYERS ALT TO CYRTEC
152S0915	152S0796		ALL	MSG LAYERS ALT TO CYRTEC
516S0709	516S0706		ALL	MSLEX ALT TO FORCORN
155S0457	155S0329		ALL	MSG LAYERS ALT TO MERATA
516-0213	516-0201		ALL	MSLEX ALT TO FORCORN

K20 BOM GROUPS

BOM GROUP	BOM OPTIONS
K20_COMMON	ALTERNATE,COMMON,K20_COMMON1,K20_COMMON2,K20_DEBUG,K20_PROGPARTS
K20_COMMON1	ONEWIRE_PU,ISL6258,MMRESETHW,MMRESETHMCP,MCP_B03,MCP_PROD,MCPSEQ_SMC,MMON_ENG,MCP_CS1_NO,FM_LVG_NEW_PROD,DIGEMS,TPDT_DEBOUNCE
K20_COMMON2	BOOT_MODE_USER,GPUVID_1P00V,MUXGFX,DPMUX_EN_S0,DP_ESD,EG_PWRSEQ_GMUX,DP_CA_DET_EG_PLD,BKLT_PLL_NOT_GMUX_1V8
K20_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TPAD_DEBUG,GMUX_JTAG_CONN
K20_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_1024_SAMSUNG	VRAM8,VRAM_1024_SAMSUNG
FB_1024_QIMONDA	VRAM8,VRAM_1024_QIMONDA
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_QIMONDA	VRAM4,VRAM_512_QIMONDA

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CH]	CRITICAL	EEE_4CH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CM]	CRITICAL	EEE_4CM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CP]	CRITICAL	EEE_4CP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4CQ]	CRITICAL	EEE_4CQ

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3645	1	IC,POC,QXXX,QS,2.66,35W,1066,80,8M,8GA	U1000	CRITICAL	CPU_2_66GHZ
337S3644	1	IC,POC,QXXX,QS,2.66,35W,1066,80,8M,8GA	U1000	CRITICAL	CPU_2_86GHZ
338S0714	1	IC,ASBP,GPU,NV,096-QE,LOWLKG,MDA969,LP	U8000	CRITICAL	
338S0694	1	IC,RTL8251CA-VB-GB,GIGE TRANSCEIVER,48P LGFP	U3700	CRITICAL	
338S0654	1	IC,FW43-R,1394B,PRO/CMC,139K/PCT-R,12	U4100	CRITICAL	
338S0710	1	IC,MCP79XT-R3,35X35MM,8GA1437	U1400	CRITICAL	MCP_B03
338S0563	1	IC,SMC,HSB/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2355	1	IC,SMC,DEVELOPMENT,K20	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-ROD	U6100	CRITICAL	BOOTROM_BLANK
341S2356	1	IC,EFI ROM,DEVELOPMENT,K20	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	SR,EMCORE II, CY7C63833-LFXC	U4800	CRITICAL	
338S0603	1	IC,GMCP,MCP79-A01Q,35X35MM,8GA1437	U1400	CRITICAL	MCP_A01Q
341S2383	1	IC,PSOC +W/USB,56PIN,MLF,M98	U5701	CRITICAL	TPAD_PROG
337S3643	1	IC,POC,QXXX,QS,2.93,35W,1066,80,8M,8GA	U1000	CRITICAL	CPU_2_93GHZ
337S3640	1	IC,POC,EL388,FRQ,2.93,35W,1066,80,8M,8GA	U1000	CRITICAL	CPU_2_53GHZ
337S3641	1	IC,POC,EL843,FRQ,2.80,35W,1066,80,8M,8GA	U1000	CRITICAL	CPU_2_80GHZ
338S0635	1	IC,GMCP,MCP79-B02,35X35MM,8GA1437	U1400	CRITICAL	MCP_B02
333S0481	4	IC,SGRAM,GDDR3,32MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC,SGRAM,GDDR3,32MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_QIMONDA
333S0481	8	IC,SGRAM,GDDR3,32MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U8510,U8515,U8520,U8525	CRITICAL	VRAM_1024_SAMSUNG
333S0472	8	IC,SGRAM,GDDR3,32MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550,U8510,U8515,U8520,U8525	CRITICAL	VRAM_1024_QIMONDA

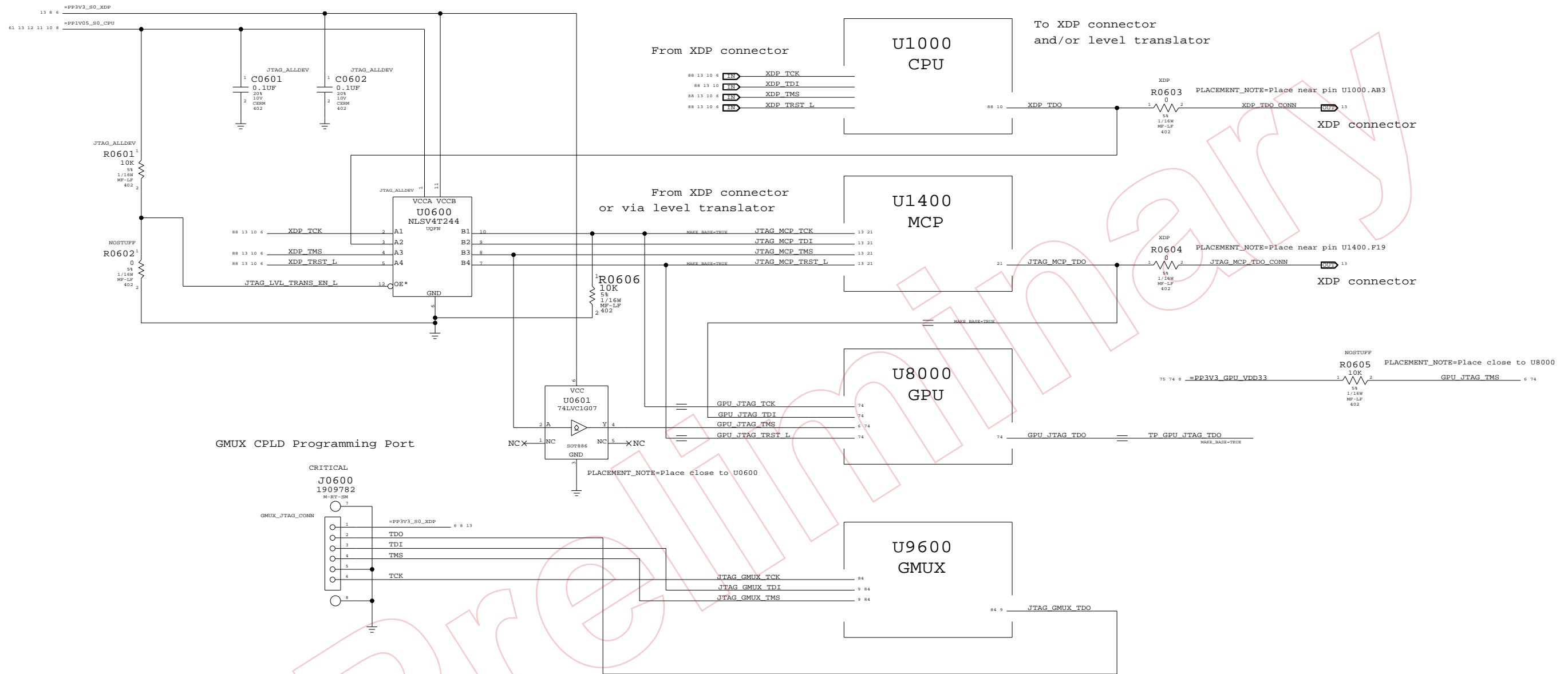
BOM Configuration
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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	5	123

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN_K20 SYNC_DATE=07/11/2008

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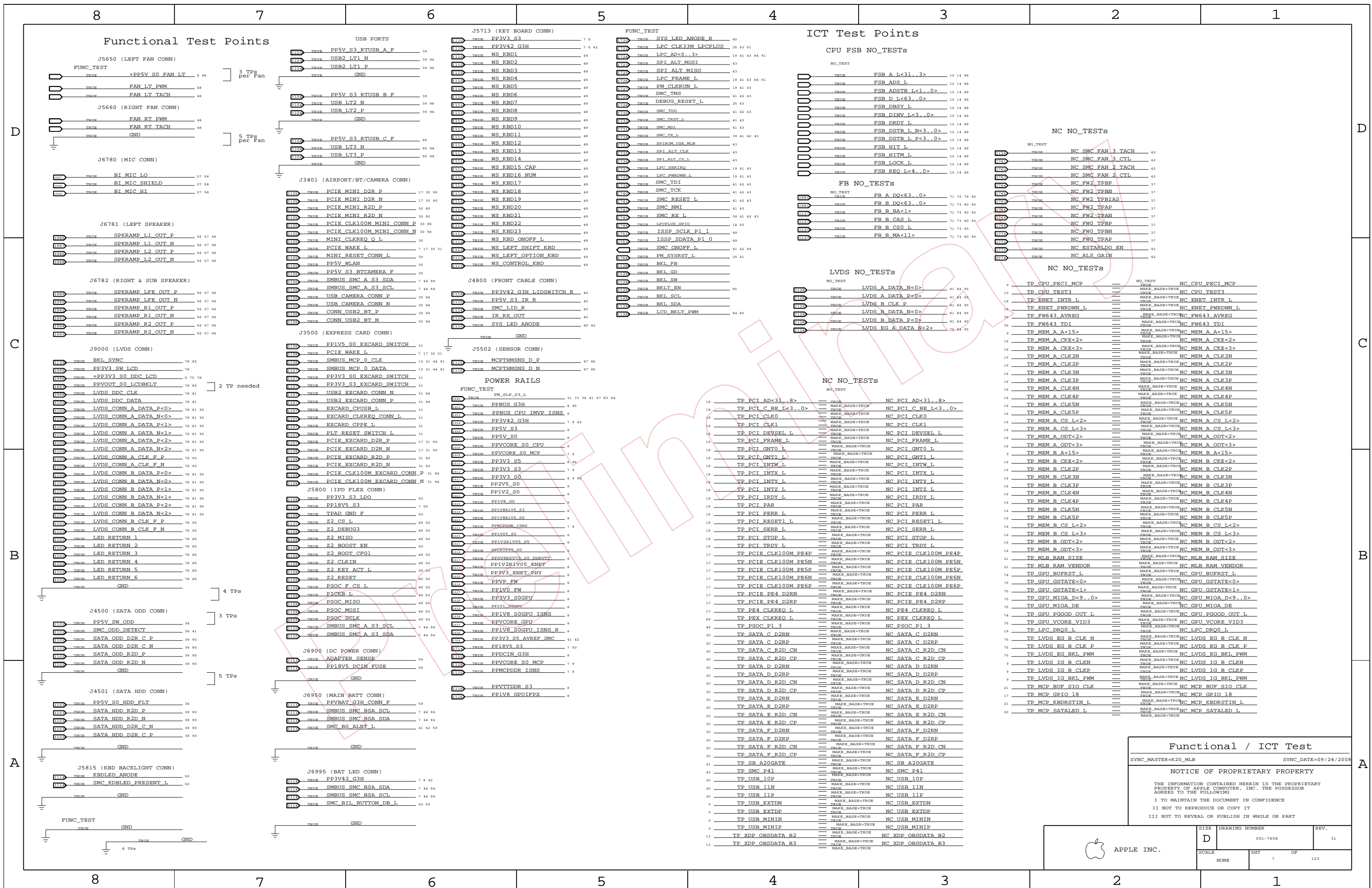
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	6		



Functional Test Points

ICT Test Points

CPU FSB NO_TESTS

NC NO_TESTS

FB NO_TESTS

LVDS NO_TESTS

NC NO_TESTS

POWER RAILS

Functional / ICT Test

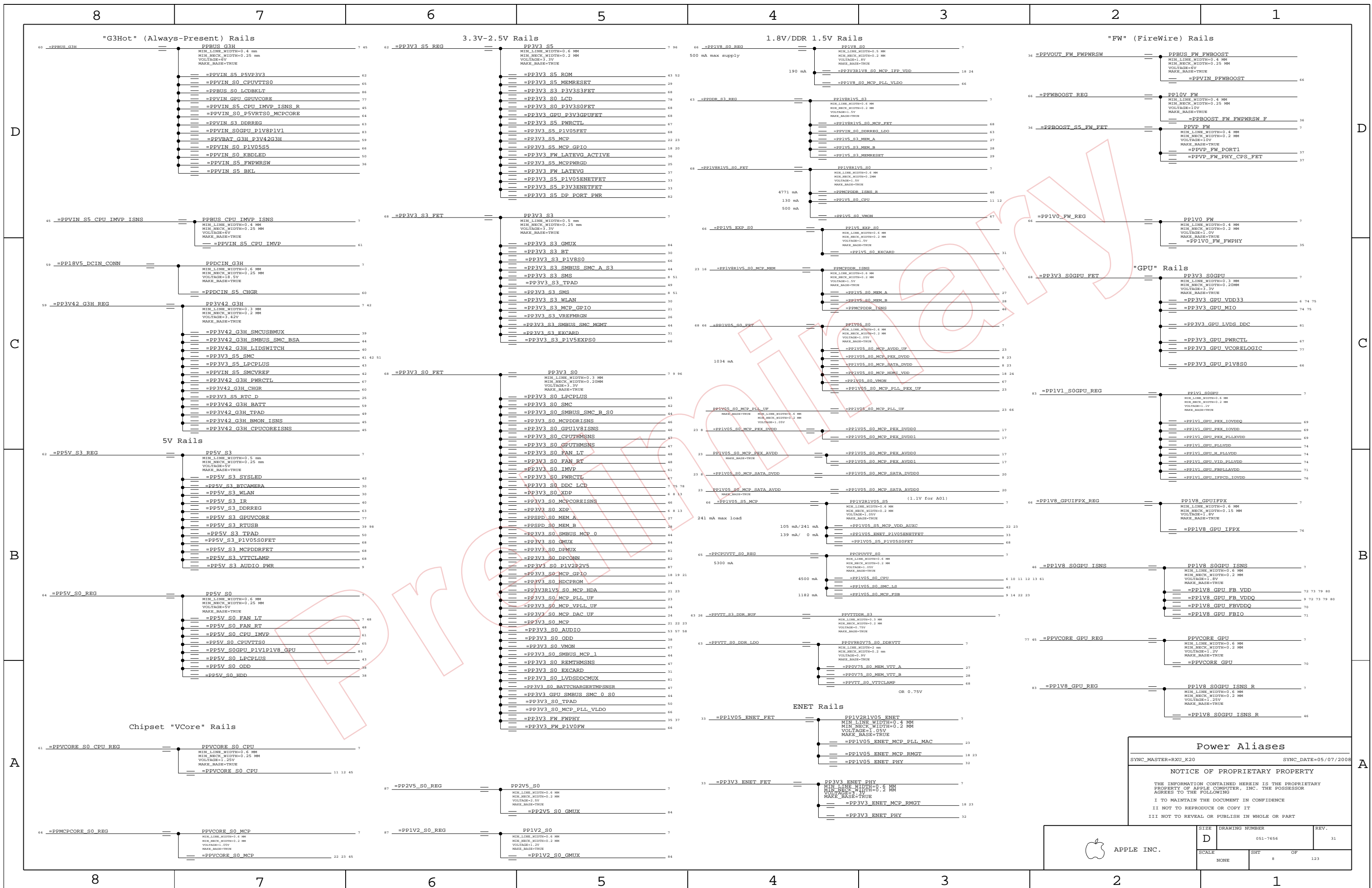
SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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D	051-7656	31
SCALE	SHT	OF
NONE	7	123



Power Aliases		
SYNC_MASTER=RXU_K20		SYNC_DATE=05/07/2008

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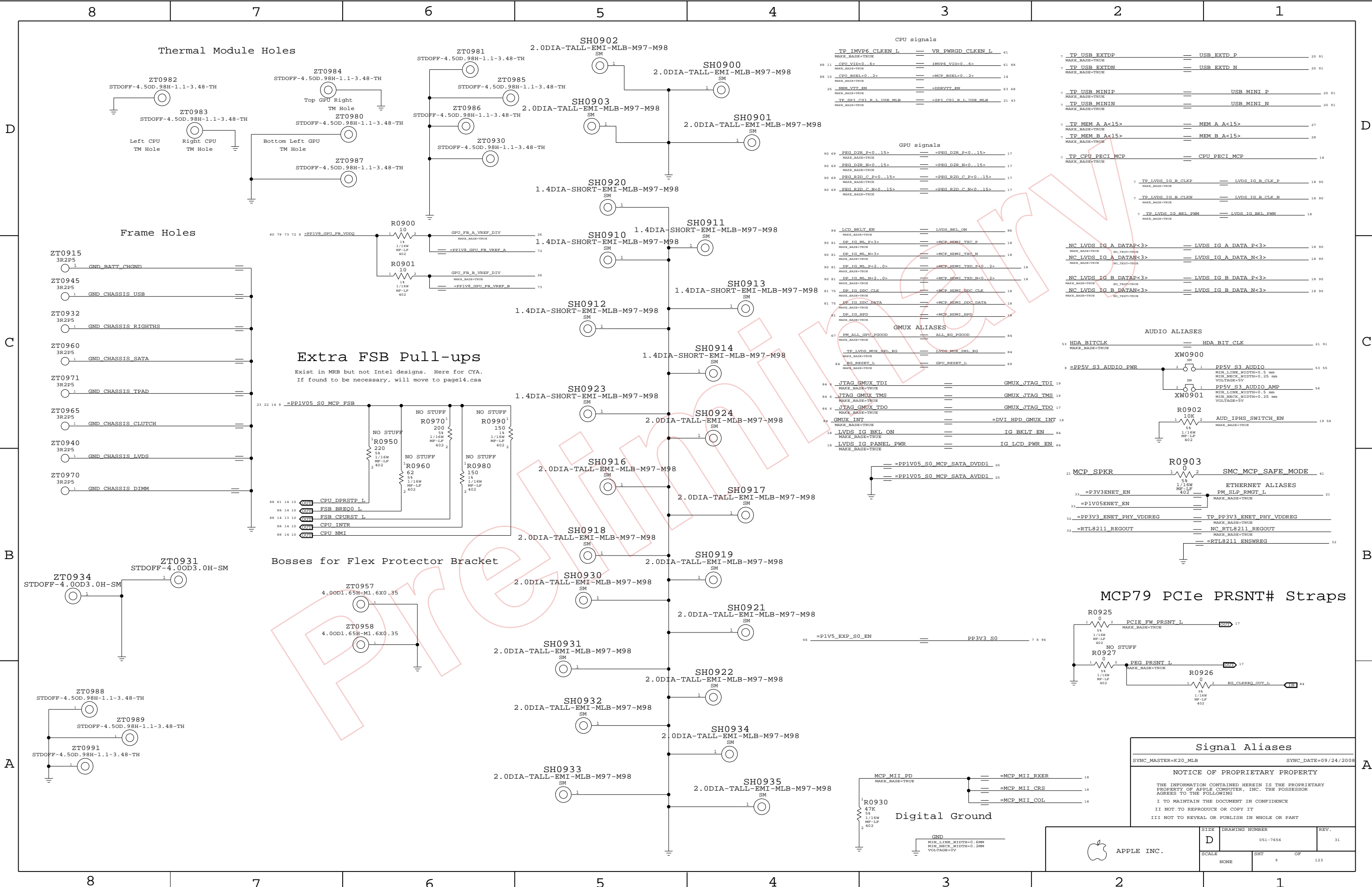
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

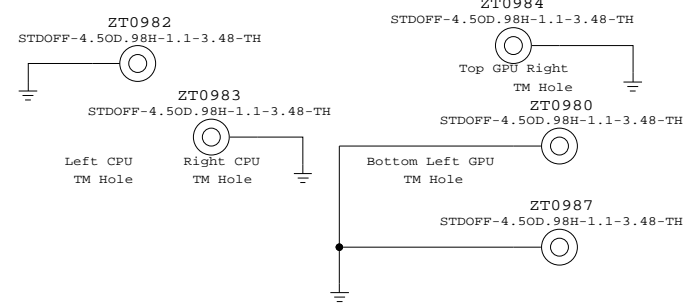
SCALE	DRAWING NUMBER		REV.
	NONE	051-7656	31
SCALE	SHEET		OF
	NONE	8	123



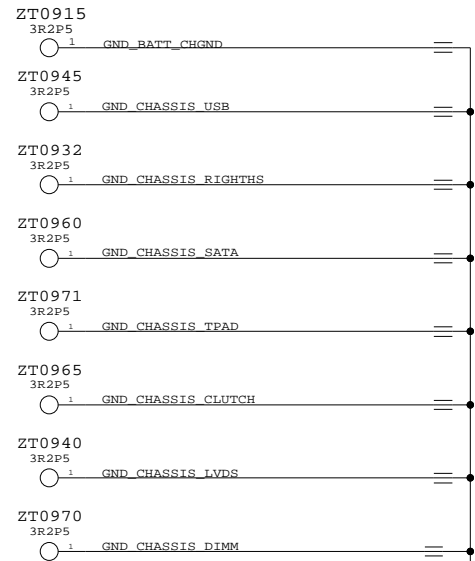
APPLE INC.



Thermal Module Holes

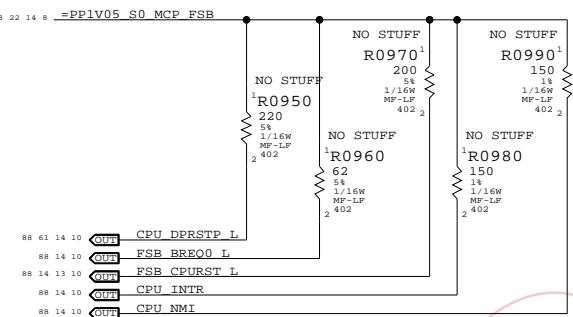


Frame Holes

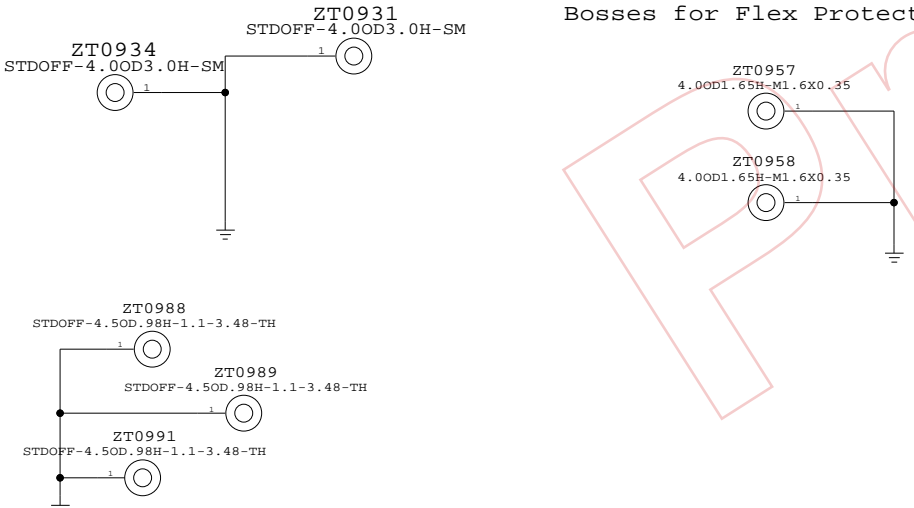


Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to pagel4.csa



Bosses for Flex Protector Bracket



CPU signals

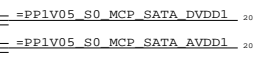
TP_IMVP6_CLKEN_L	==	VR_PWRGD_CLKEN_L	61
MAKE_BASE=TRUE			
88 11 CPU_VID<0..6>	==	IMVP6_VID<0..6>	61 88
MAKE_BASE=TRUE			
88 10 CPU_BSEL<0..2>	==	MCP_BSEL<0..2>	14
MAKE_BASE=TRUE			
25 MEM_VTT_EN	==	DDR_VTT_EN	63 68
MAKE_BASE=TRUE			
TP_SPI_CS1_B_L_USER_MLB	==	SPT_CS1_B_L_USER_MLB	21 43
MAKE_BASE=TRUE			

GPU signals

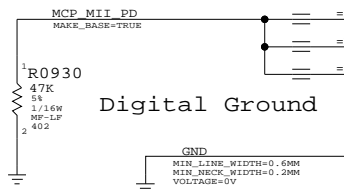
90 69 PEG_D2R_P<0..15>	==	PEG_D2R_P<0..15>	17
MAKE_BASE=TRUE			
90 69 PEG_D2R_N<0..15>	==	PEG_D2R_N<0..15>	17
MAKE_BASE=TRUE			
90 69 PEG_R2D_C_P<0..15>	==	PEG_R2D_C_P<0..15>	17
MAKE_BASE=TRUE			
90 69 PEG_R2D_C_N<0..15>	==	PEG_R2D_C_N<0..15>	17
MAKE_BASE=TRUE			

GMUX ALIASES

67 PM_ALL_GPU_PGOOD	==	ALL_EG_PGOOD	84
MAKE_BASE=TRUE			
TP_LVDS_MUX_SEL_EG	==	LVDS_MUX_SEL_EG	84
MAKE_BASE=TRUE			
84 EG_RESET_L	==	GPU_RESET_L	69
MAKE_BASE=TRUE			
84 JTAG_GMUX_TDI	==	GMUX_JTAG_TDI	19
MAKE_BASE=TRUE			
84 JTAG_GMUX_TMS	==	GMUX_JTAG_TMS	19
MAKE_BASE=TRUE			
84 JTAG_GMUX_TDO	==	GMUX_JTAG_TDO	17
MAKE_BASE=TRUE			
84 GMUX_INT	==	DVI_HPD_GMUX_INT	18
MAKE_BASE=TRUE			
18 LVDS_IG_BKLT_ON	==	IG_BKLT_EN	84
MAKE_BASE=TRUE			
18 LVDS_IG_PANEL_PWR	==	IG_LCD_PWR_EN	84
MAKE_BASE=TRUE			



Digital Ground



7 TP_USB_EXTDP	==	USB_EXTD_P	20 91
MAKE_BASE=TRUE			
7 TP_USB_EXTDN	==	USB_EXTD_N	20 91
MAKE_BASE=TRUE			
7 TP_USB_MINIP	==	USB_MINI_P	20 91
MAKE_BASE=TRUE			
7 TP_USB_MININ	==	USB_MINI_N	20 91
MAKE_BASE=TRUE			
7 TP_MEM_A_A<15>	==	MEM_A_A<15>	27
MAKE_BASE=TRUE			
7 TP_MEM_B_A<15>	==	MEM_B_A<15>	28
MAKE_BASE=TRUE			
7 TP_CPU_PECI_MCP	==	CPU_PECI_MCP	14
MAKE_BASE=TRUE			
7 TP_LVDS_IG_B_CLKP	==	LVDS_IG_B_CLK_P	18 90
MAKE_BASE=TRUE			
7 TP_LVDS_IG_B_CLKN	==	LVDS_IG_B_CLK_N	18 90
MAKE_BASE=TRUE			
7 TP_LVDS_IG_BKLT_PWM	==	LVDS_IG_BKLT_PWM	18
MAKE_BASE=TRUE			
NC_LVDS_IG_A_DATAP<3>	==	LVDS_IG_A_DATA_P<3>	18 90
MAKE_BASE=TRUE			
NC_LVDS_IG_A_DATAN<3>	==	LVDS_IG_A_DATA_N<3>	18 90
MAKE_BASE=TRUE			
NC_LVDS_IG_B_DATAP<3>	==	LVDS_IG_B_DATA_P<3>	18 90
MAKE_BASE=TRUE			
NC_LVDS_IG_B_DATAN<3>	==	LVDS_IG_B_DATA_N<3>	18 90
MAKE_BASE=TRUE			

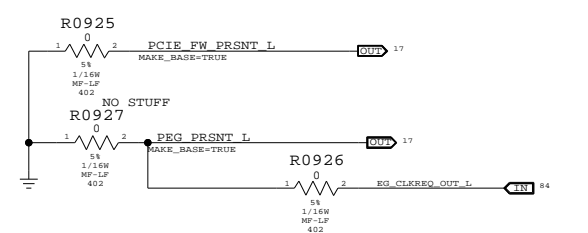
AUDIO ALIASES

53 HDA_BITCLK	==	HDA_BIT_CLK	21 91
MAKE_BASE=TRUE			
8 PPSV_S3_AUDIO_PWR	==	PPSV_S3_AUDIO	53 55
MAKE_BASE=TRUE			
8 PPSV_S3_AUDIO_PWR	==	PPSV_S3_AUDIO_AMP	56
MAKE_BASE=TRUE			
8 PPSV_S3_AUDIO_PWR	==	AUD_IPHS_SWITCH_EN	19 58
MAKE_BASE=TRUE			

ETHERNET ALIASES

21 MCP_SPKR	==	SMC_MCP_SAFE_MODE	41
MAKE_BASE=TRUE			
33 P3V3ENET_EN	==	PM_SLP_RMGT_L	21
MAKE_BASE=TRUE			
33 P1V05ENET_EN	==	TP_PP3V3_ENET_PHY_VDDREG	32
MAKE_BASE=TRUE			
32 PP3V3_ENET_PHY_VDDREG	==	TP_PP3V3_ENET_PHY_VDDREG	32
MAKE_BASE=TRUE			
32 RTL8211_REGOUT	==	NC_RTL8211_REGOUT	32
MAKE_BASE=TRUE			
32 RTL8211_REGOUT	==	RTL8211_ENSWREG	32
MAKE_BASE=TRUE			

MCP79 PCIe PRSNT# Straps



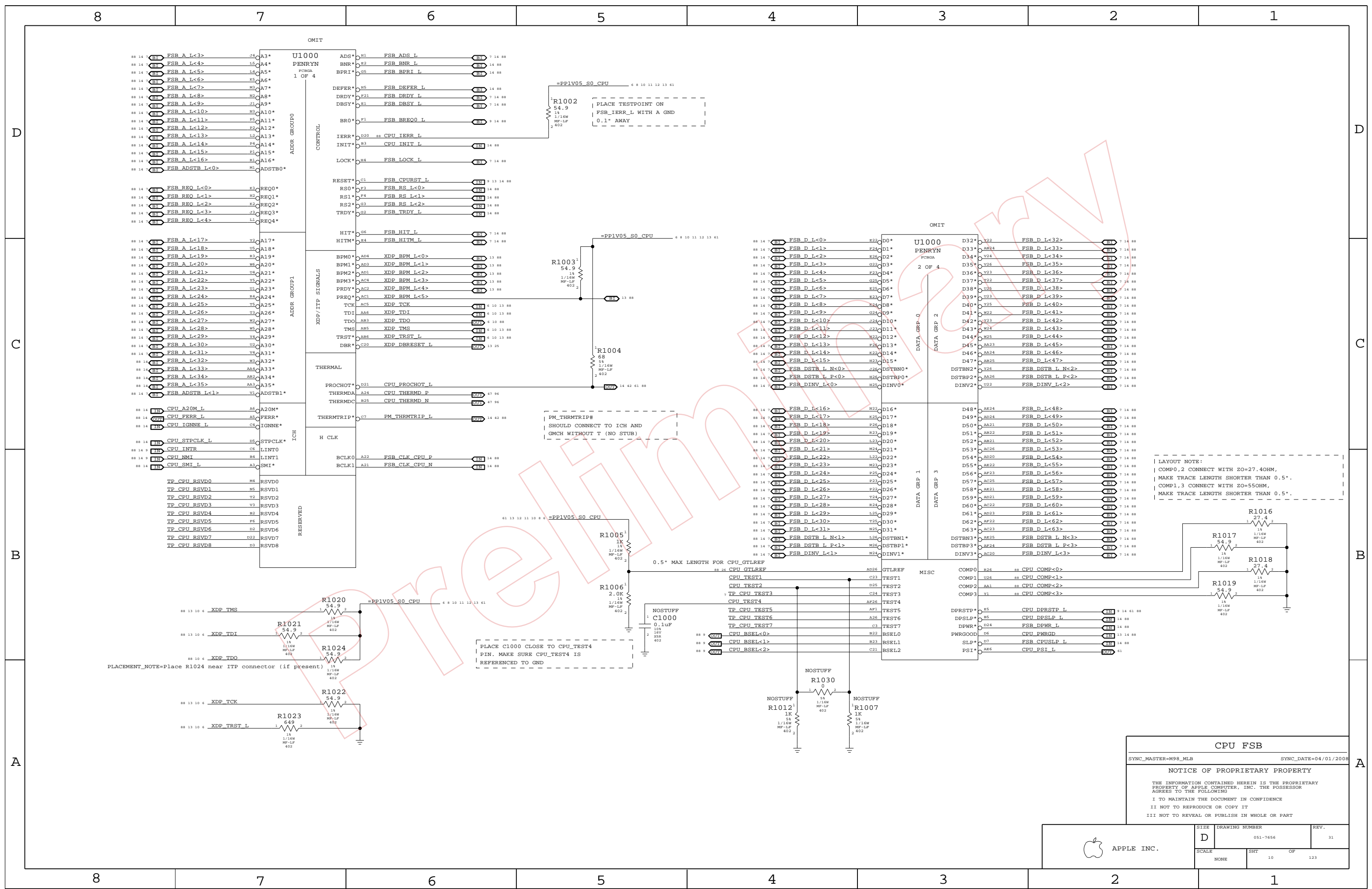
Signal Aliases

SYNC_MASTER=K20_MLB	==	SYNC_DATE=09/24/2008	
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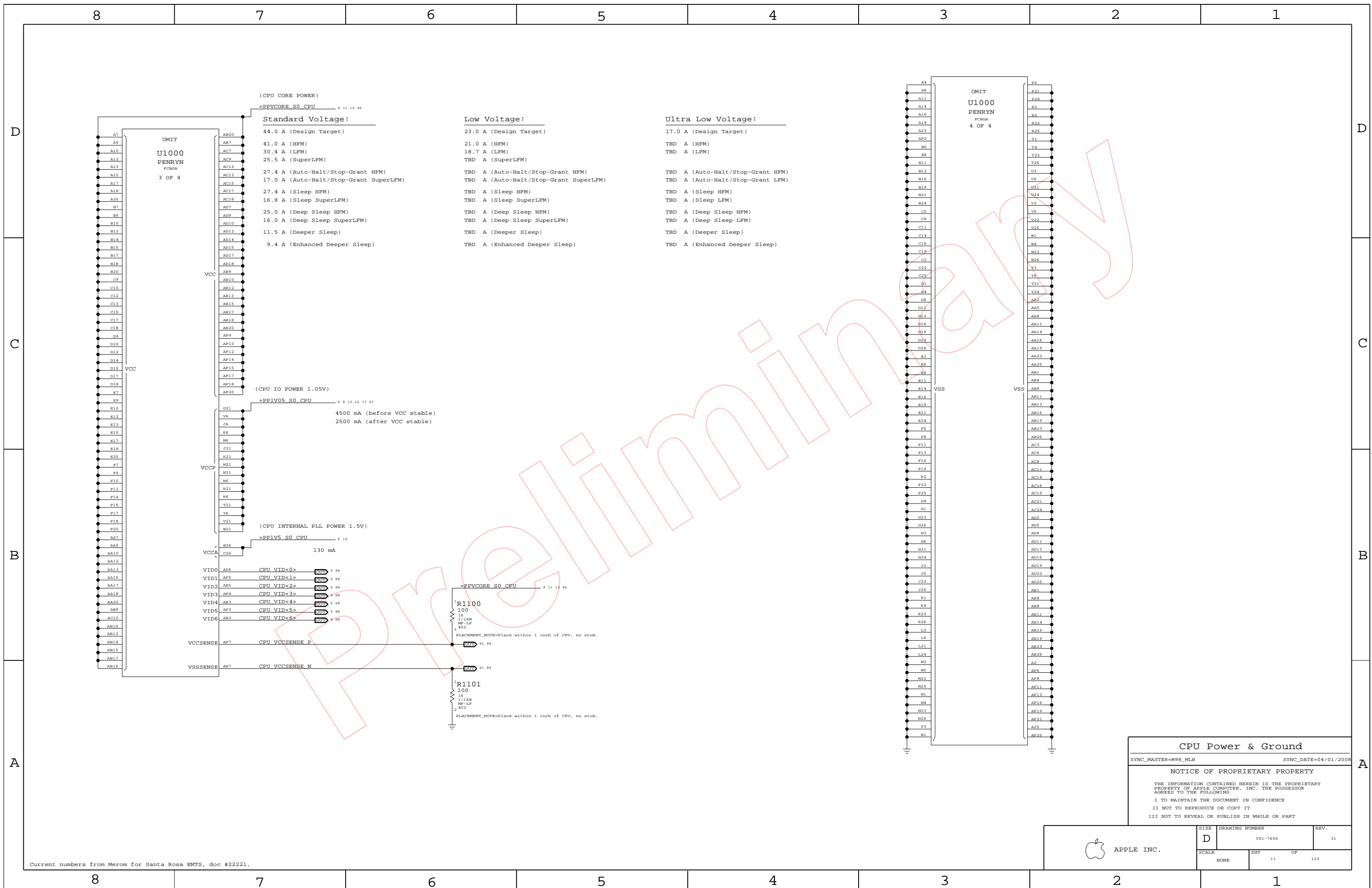
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	9		



LAYOUT NOTE:
 COMP0,2 CONNECT WITH Z0=27.4OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMP1,3 CONNECT WITH Z0=55OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB
 SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008
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	D	051-7656	31
SCALE	SHT	OF	123
NONE	10		



(CPU CORE POWER)
=PPVCORE_S0_CPU # 11 12 45

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

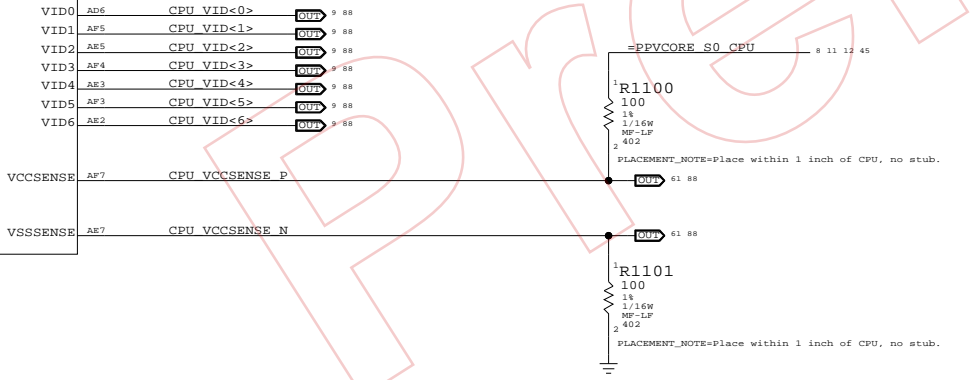
- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)
=PP1V05_S0_CPU # 8 10 12 13 61

- 4500 mA (before VCC stable)
- 2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)
=PP1V5_S0_CPU # 12

- 130 mA



CPU Power & Ground

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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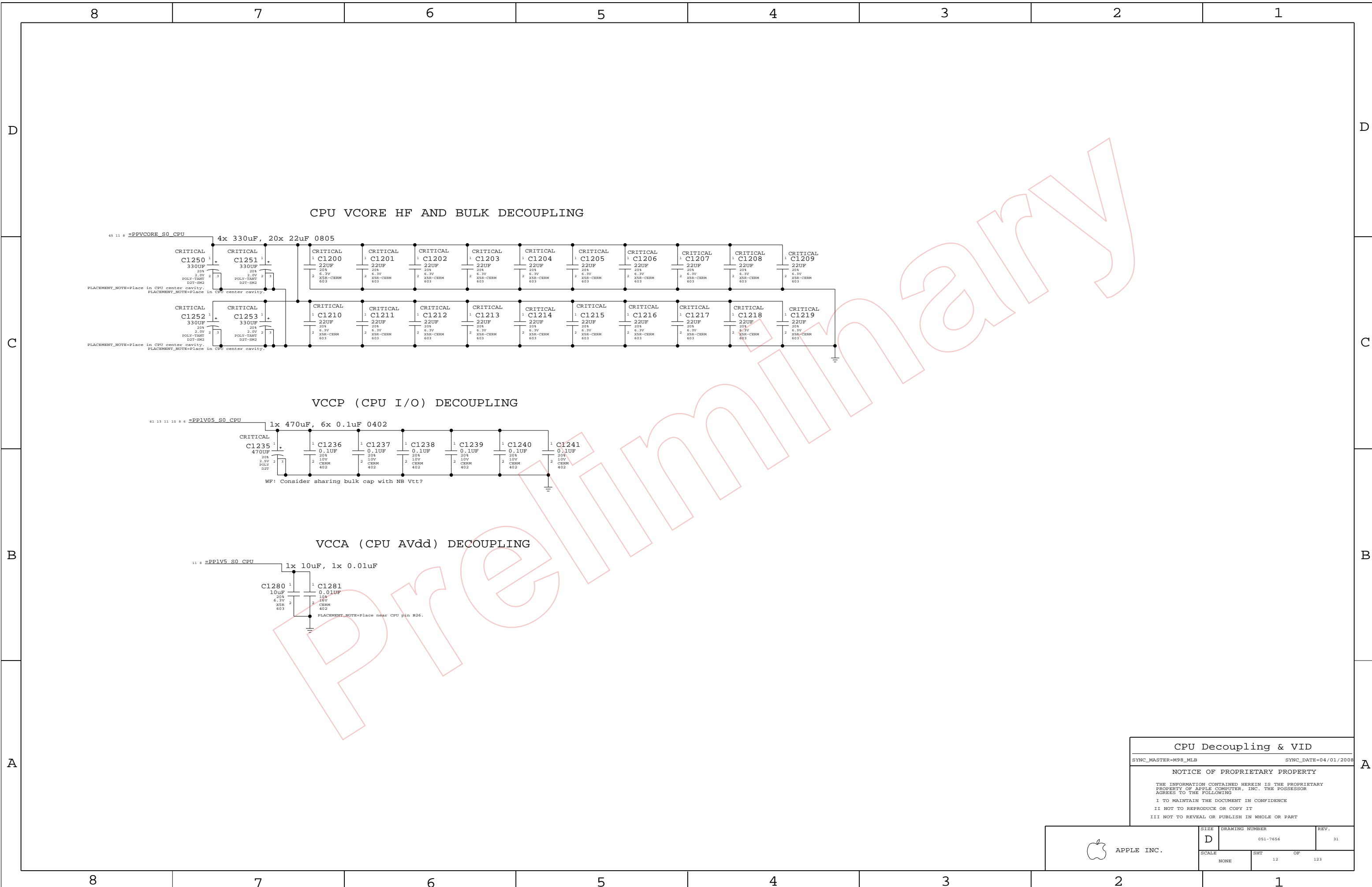
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	D	051-7656	31
SCALE	SHT	OF	123
NONE	11		

Current numbers from Merom for Santa Rosa EMTS, doc #22221.



CPU Decoupling & VID

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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	D	051-7656	31
SCALE	SHT		OF
NONE	12		123

8

7

6

5

4

3

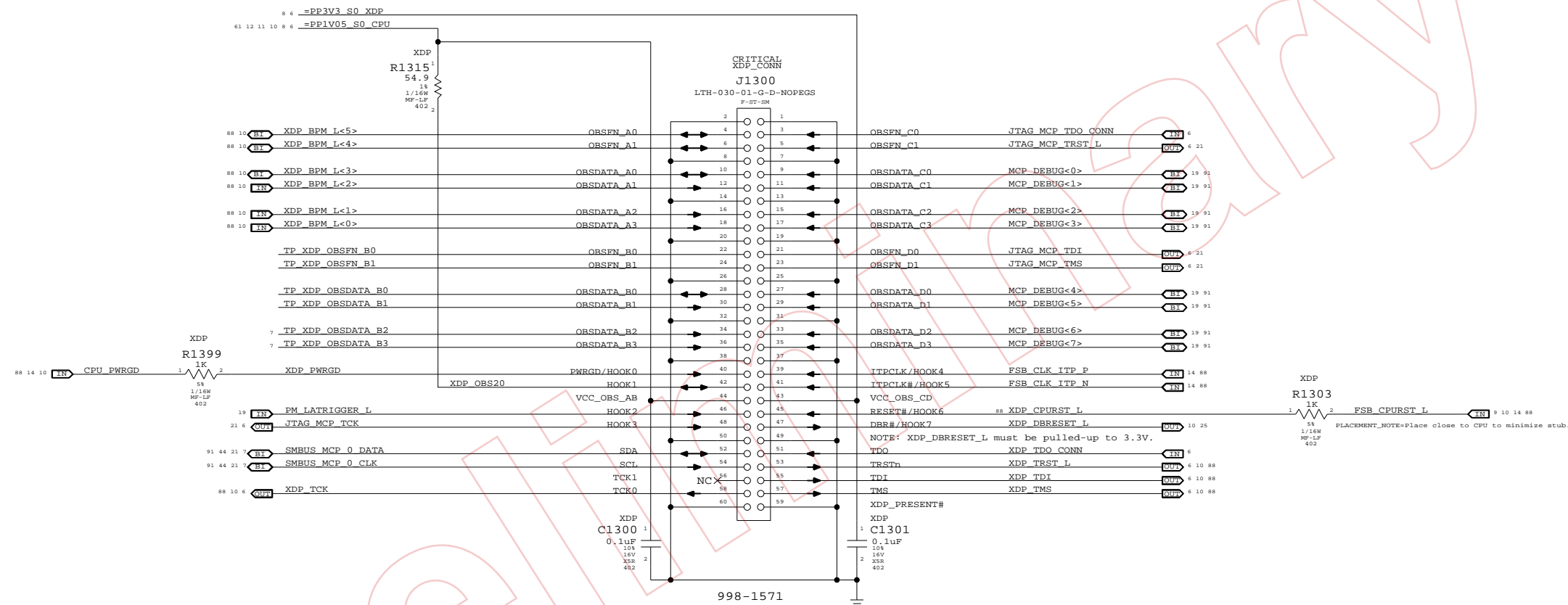
2

1

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

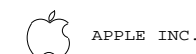
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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APPLE INC.

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D	051-7656	31
SCALE	SHT	OF
NONE	13	123

8

7

6

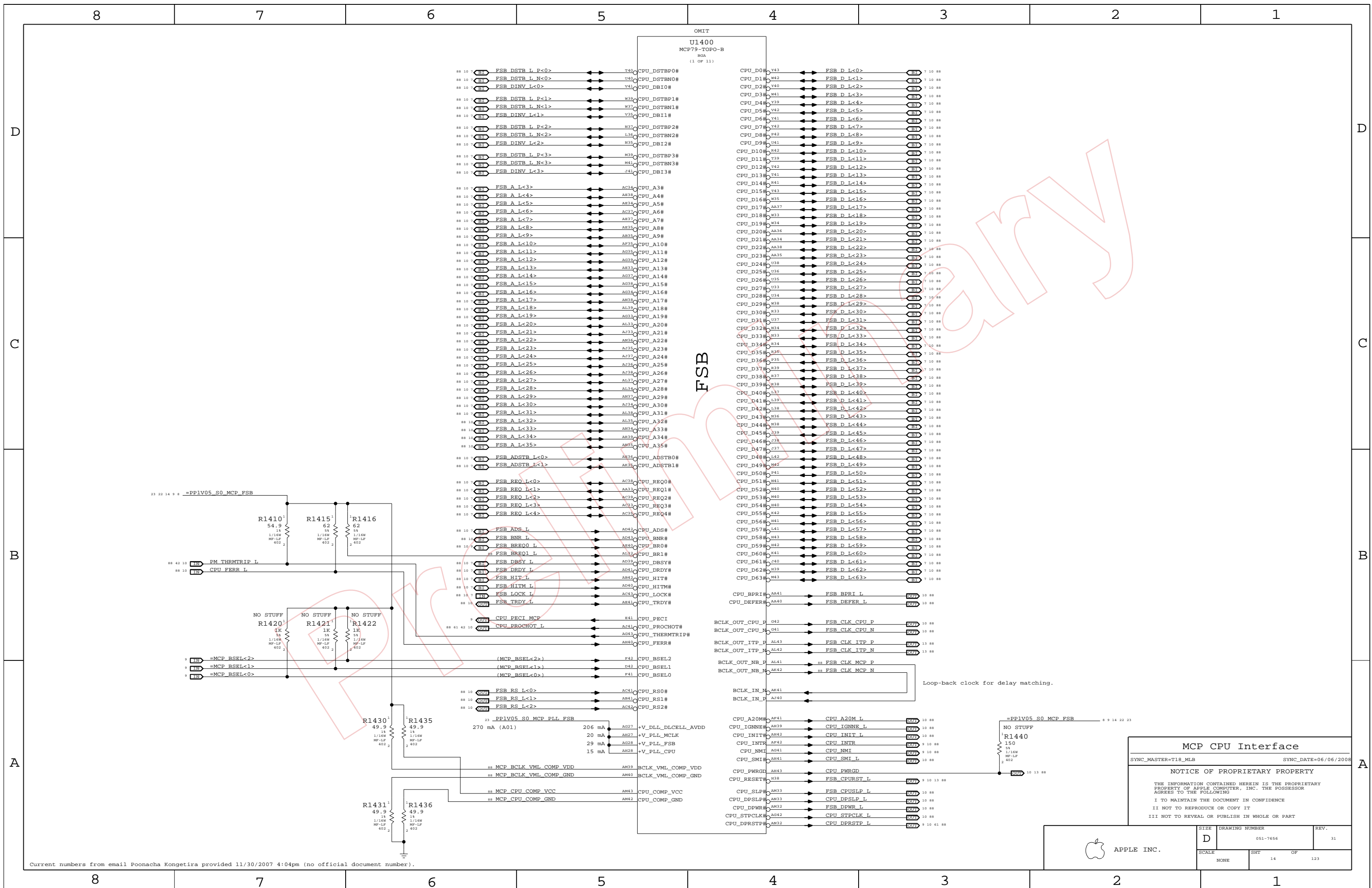
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4

3

2

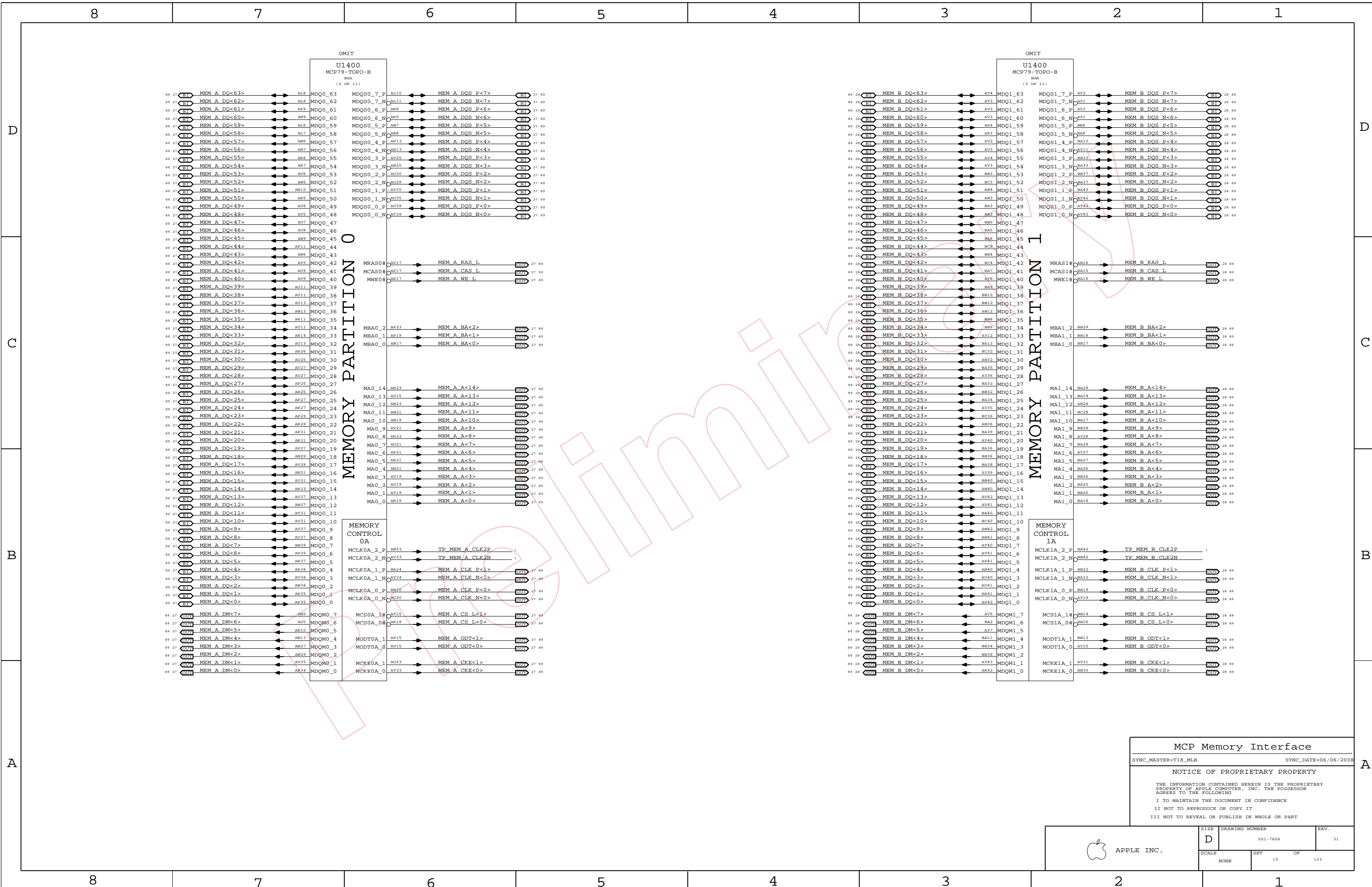
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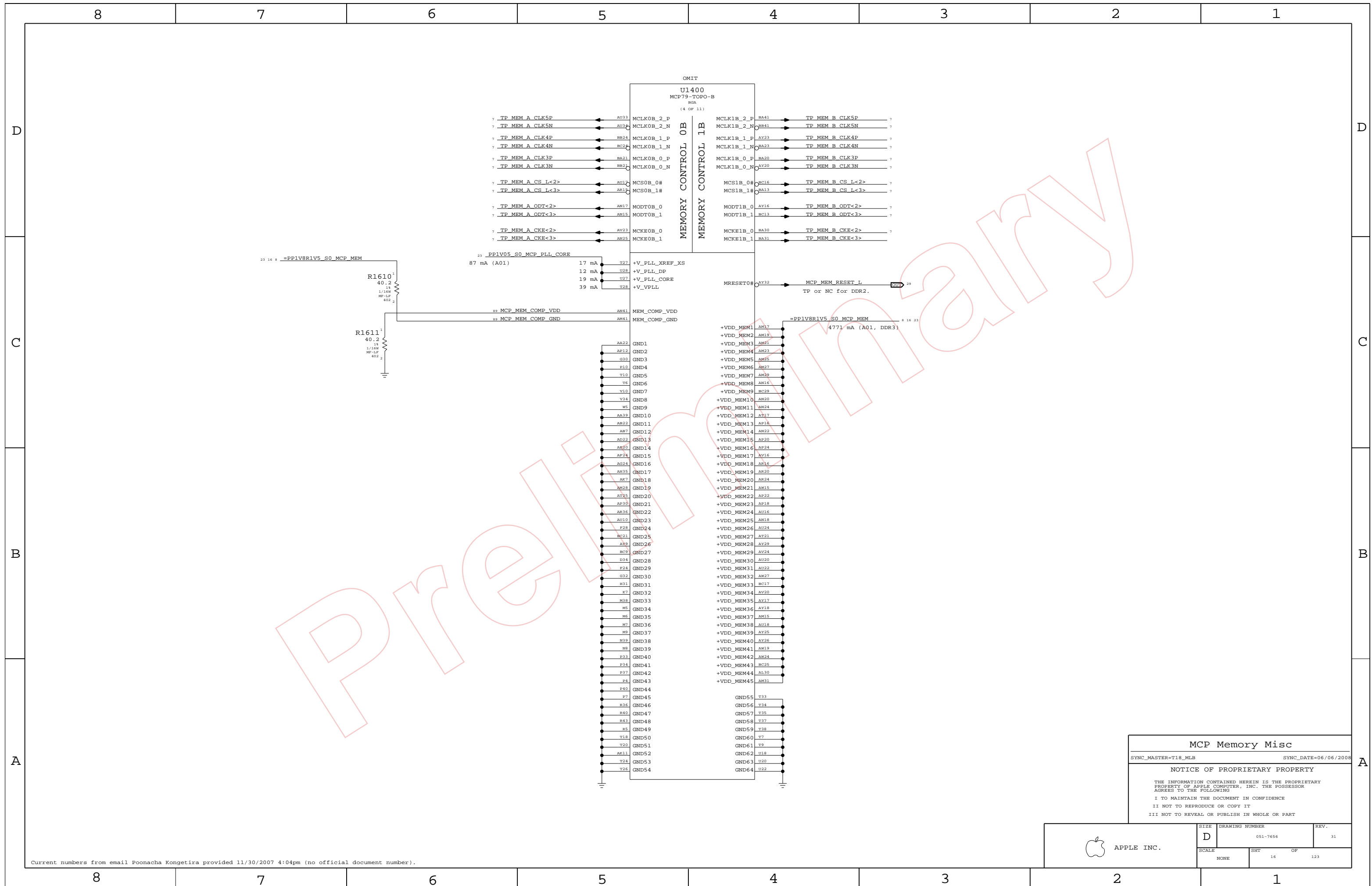
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface
 SYNC_MASTER=TI8_MLB SYNC_DATE=06/06/2008
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SCALE	NONE	SHT	14 OF 123



MCP Memory Interface
 SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008
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MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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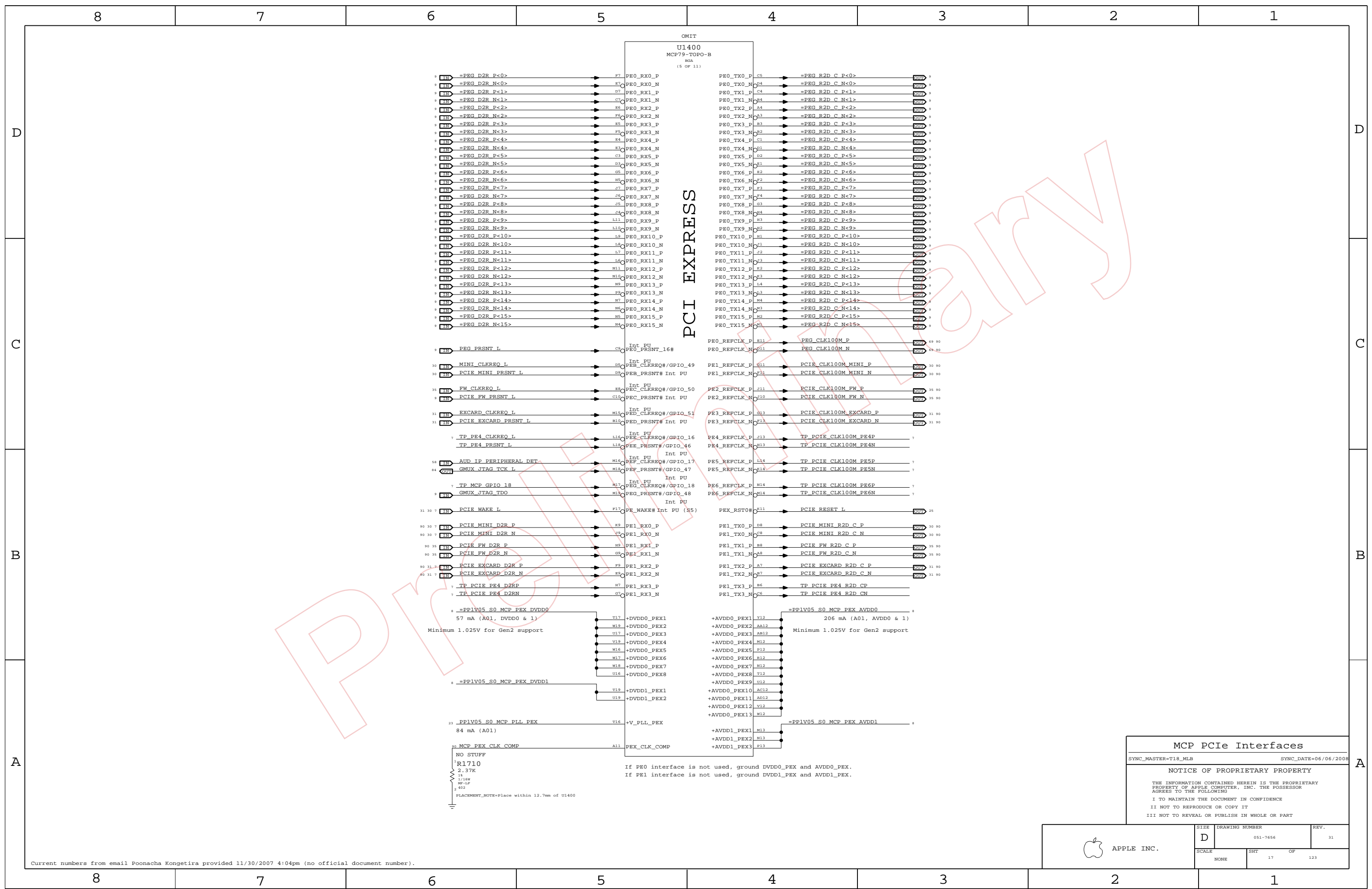
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	D	051-7656	31
SCALE	SHT		OF
NONE	16		123

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PCI EXPRESS

MCP PCIe Interfaces

SYNC_MASTER=TI8_MLB SYNC_DATE=06/06/2008

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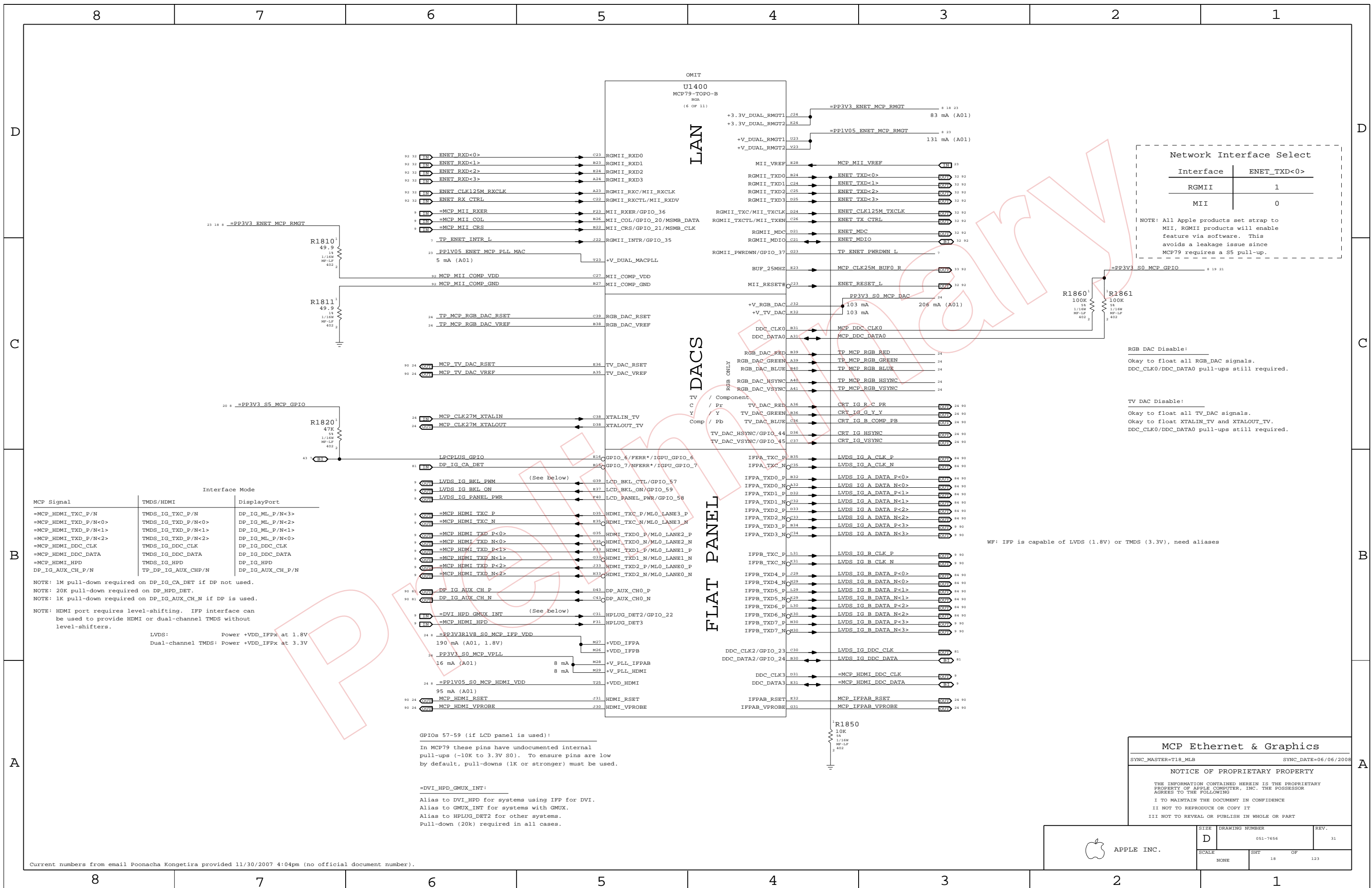
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHT 17	OF 123

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
 Okay to float all TV_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Signal	Interface Mode	
	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
 NOTE: 20K pull-down required on DP_HPD_DET.
 NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

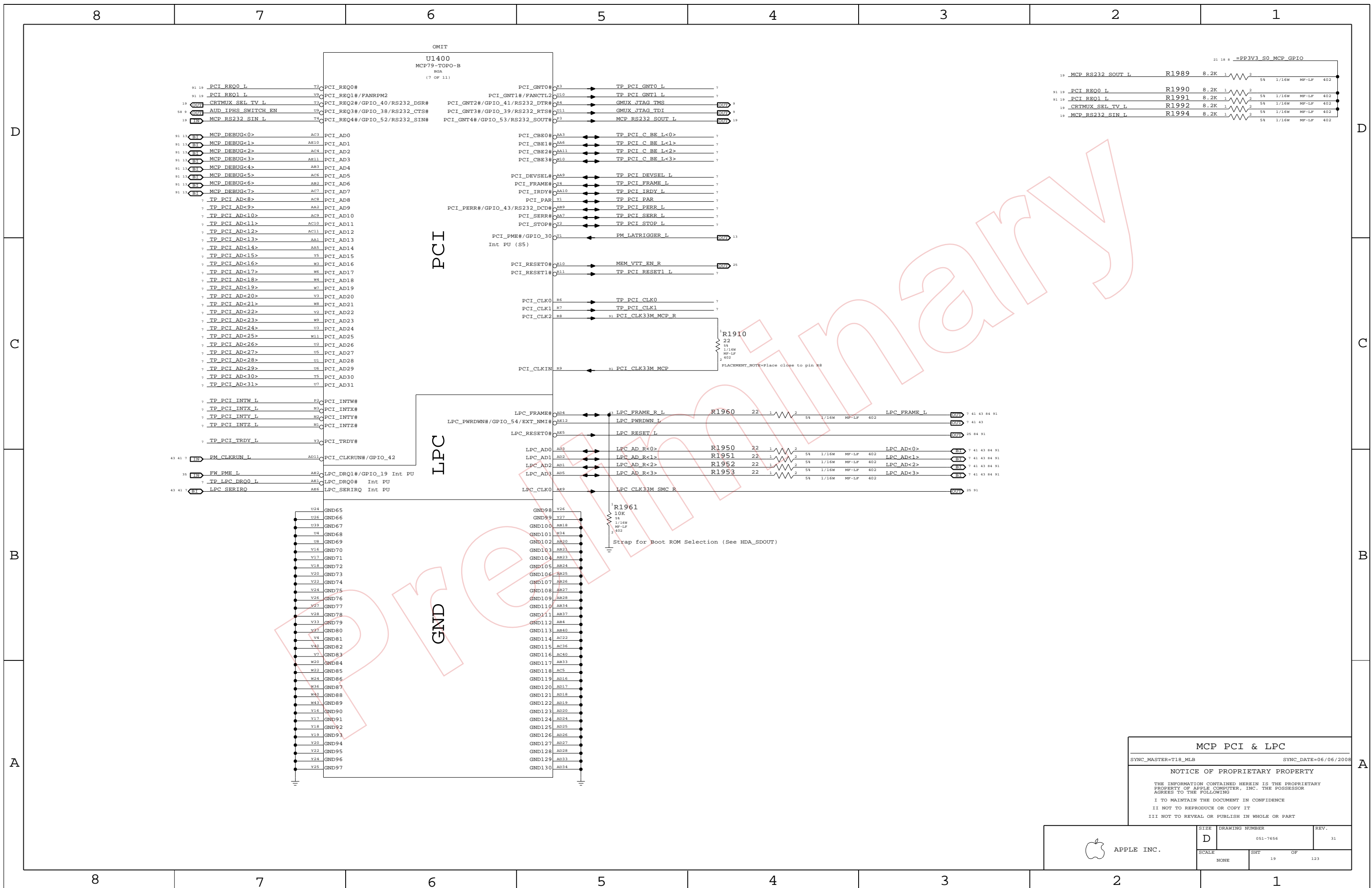
LVDS: Power +VDD_IPFX at 1.8V
 Dual-channel TMDS: Power +VDD_IPFX at 3.3V

GPIOs 57-59 (if LCD panel is used):
 In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
 Alias to DVI_HPD for systems using IFP for DVI.
 Alias to GMUX_INT for systems with GMUX.
 Alias to HPLUG_DET2 for other systems.
 Pull-down (20k) required in all cases.

MCP Ethernet & Graphics			
SYNC_MASTER=T18_MLB	SYNC_DATE=06/06/2008		REV.
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	D	051-7656	31
SCALE	SHT	OF	123
NONE	18		



MCP PCI & LPC

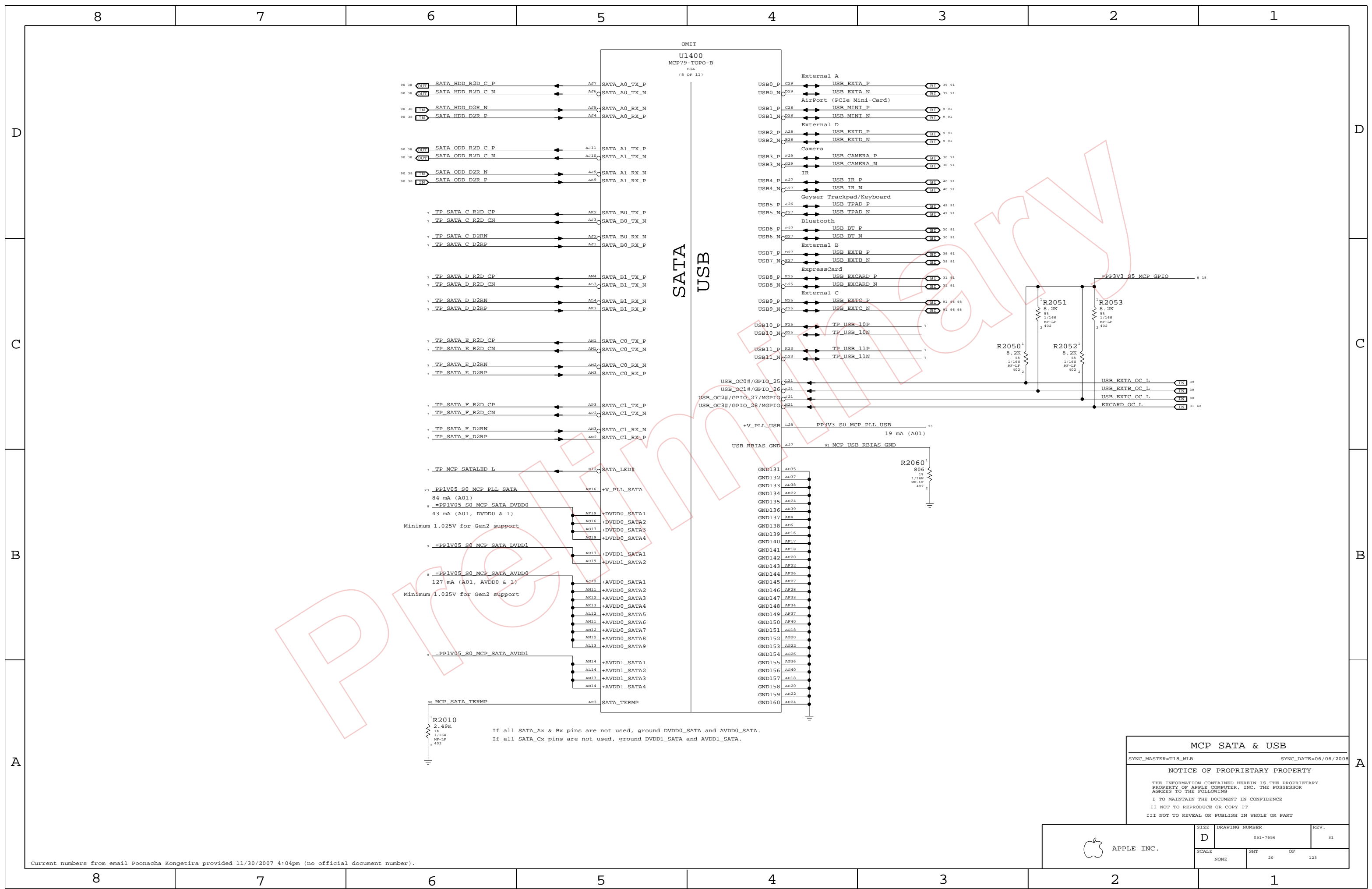
SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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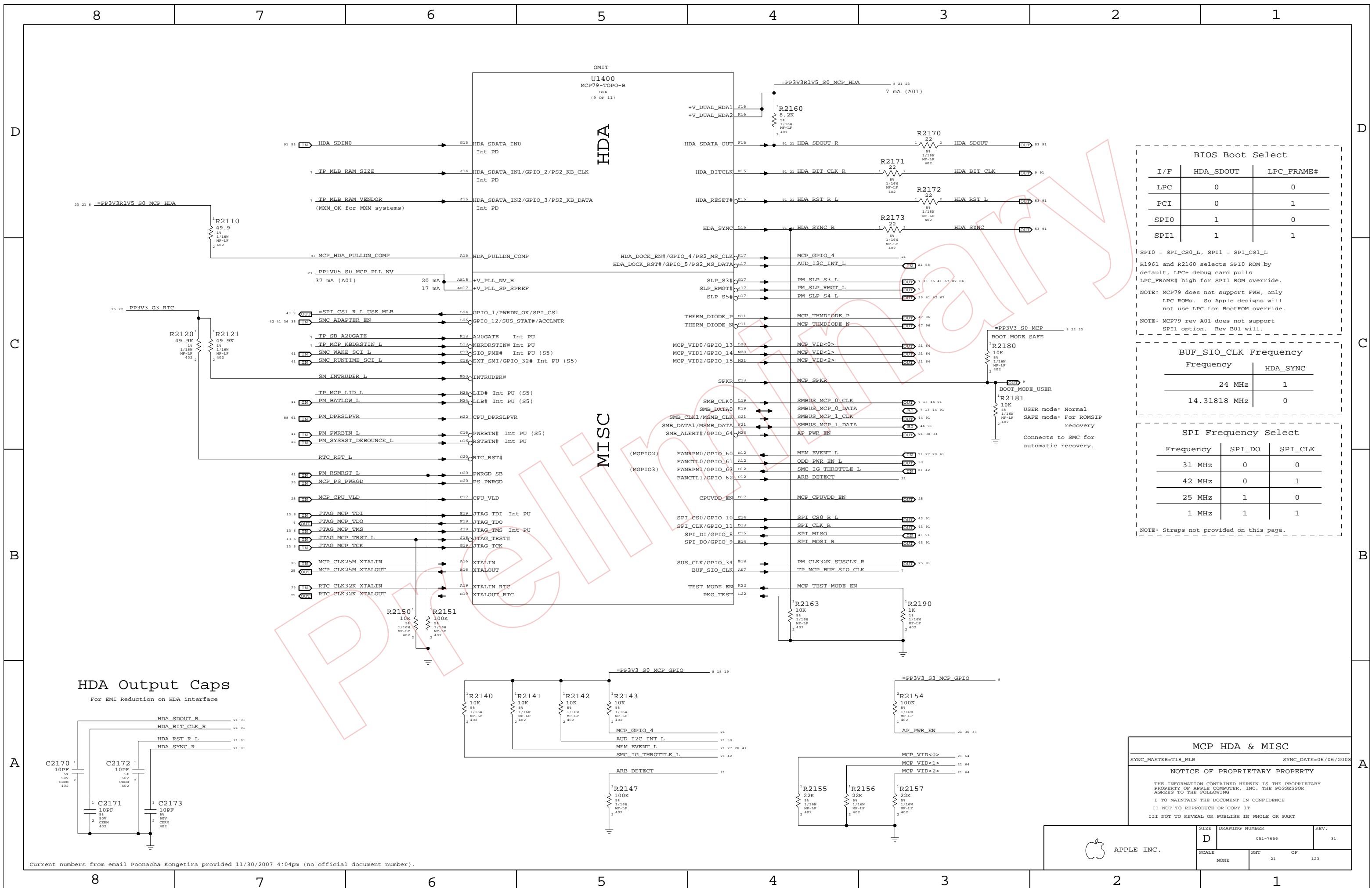
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	19		



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
 If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB			
SYNC_MASTER=T18_MLB	SYNC_DATE=06/06/2008		
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	20		



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
 NOTE: MCP79 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

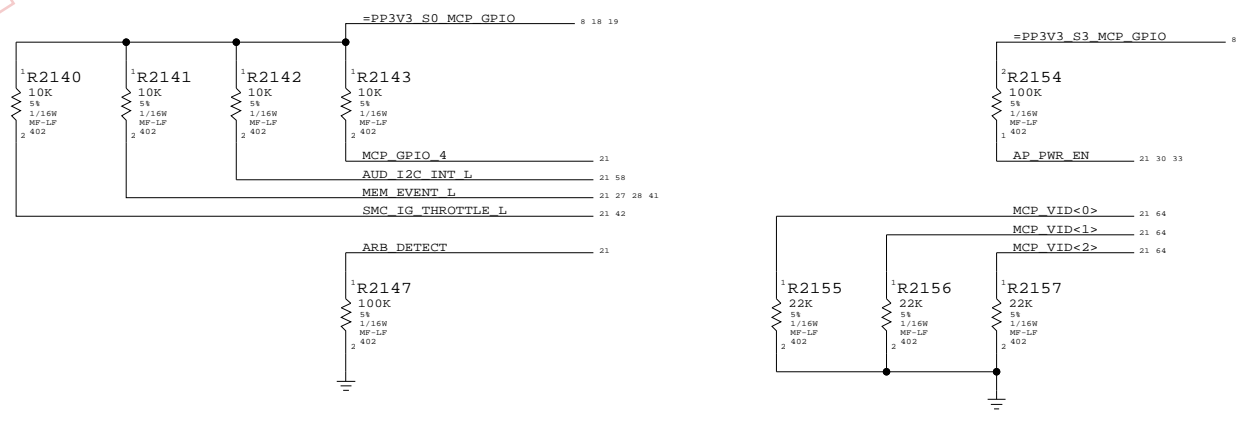
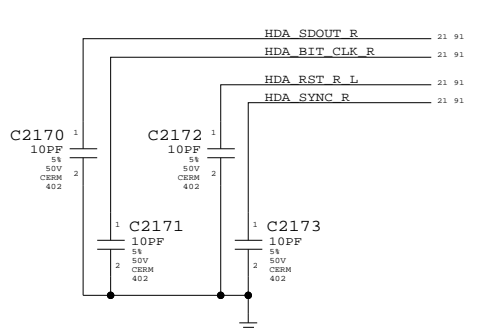
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps
 For EMI Reduction on HDA interface



MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008

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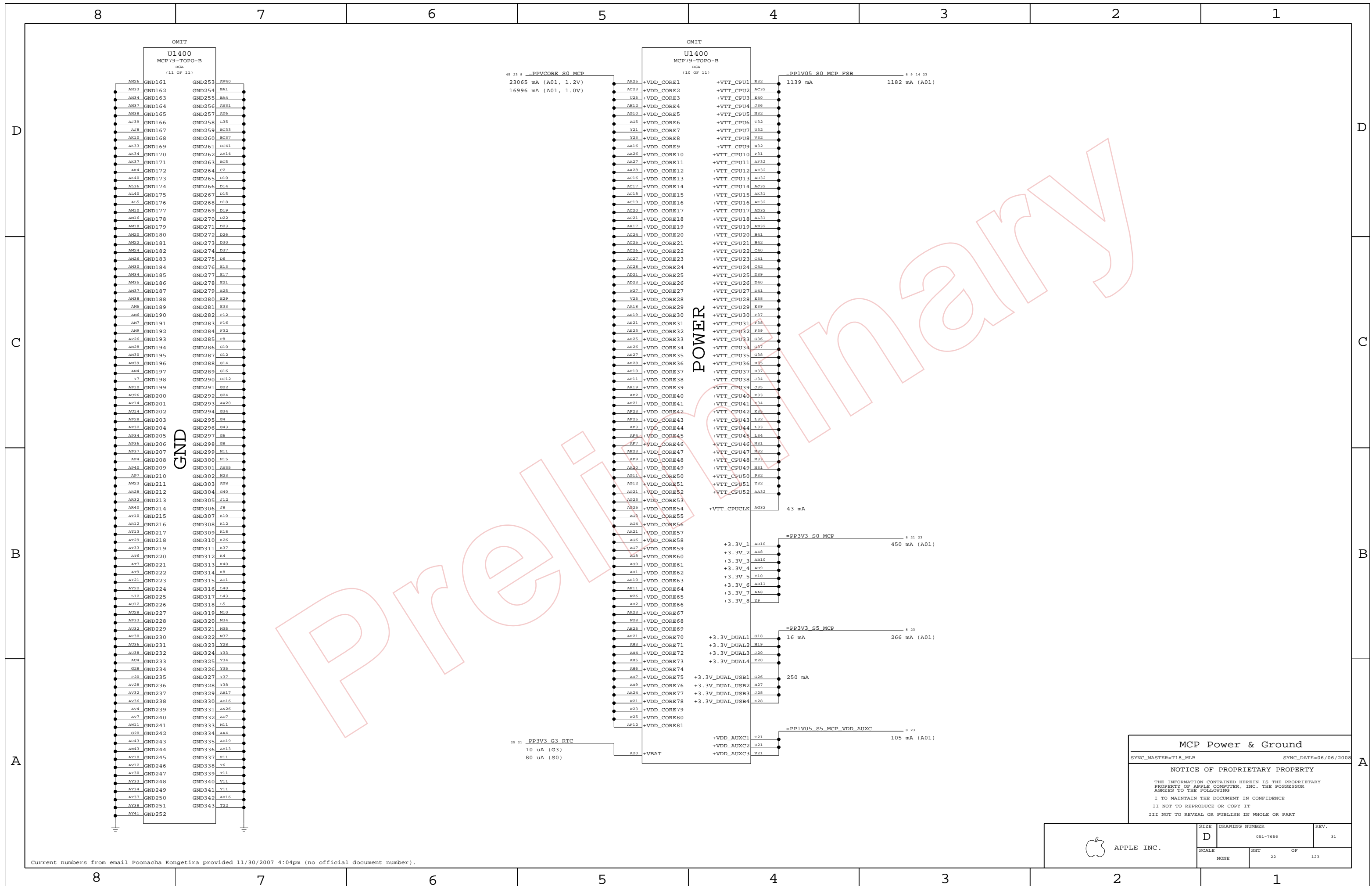
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	NONE	SHT	OF
		21	123

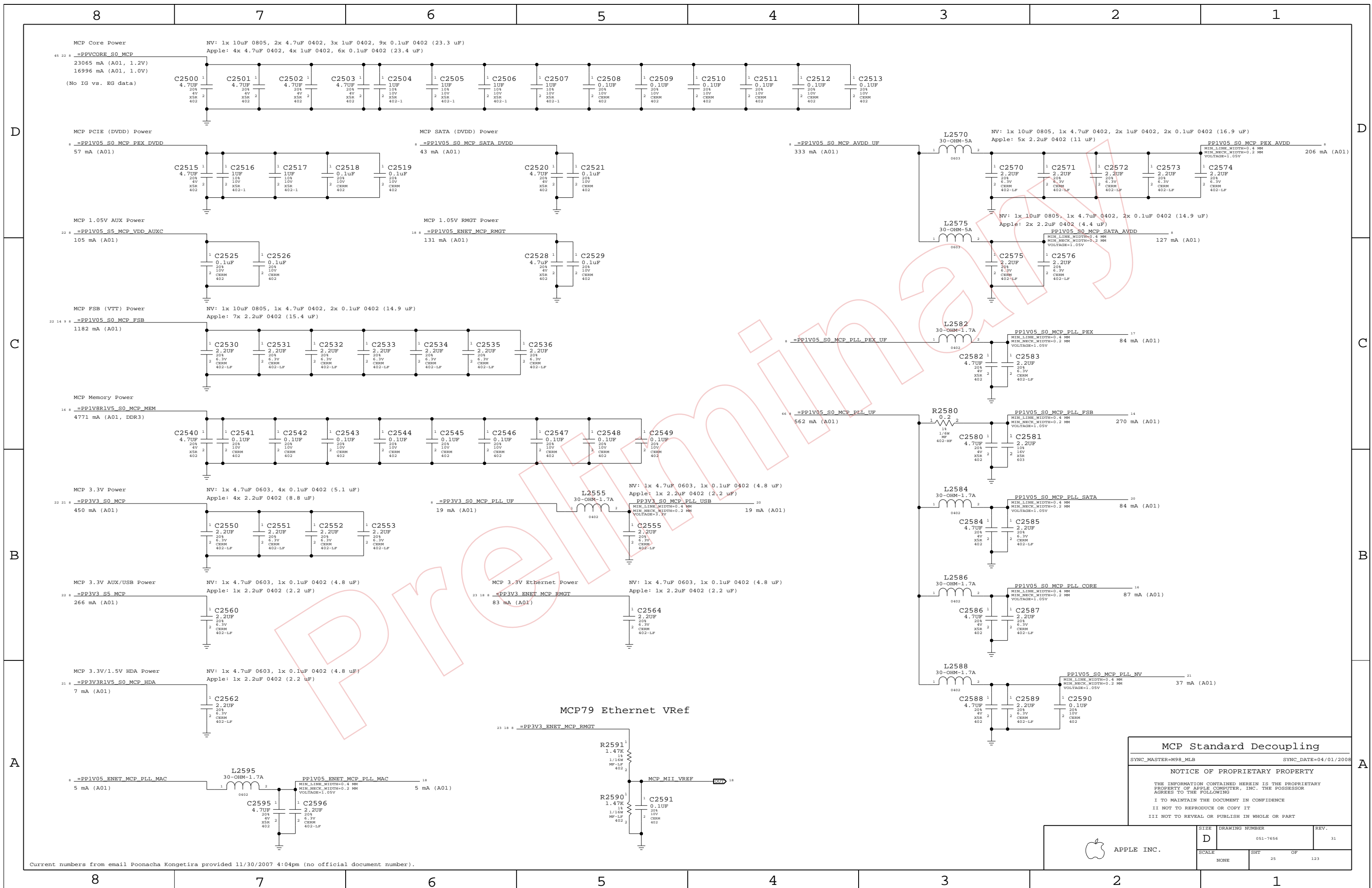
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



MCP Power & Ground
 SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008
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SCALE NONE	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE		SHT 22
APPLE INC.		OF 123	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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SCALE	DRAWING NUMBER		REV.
	D 051-7656		
NONE		SHT 25	OF 123



APPLE INC.

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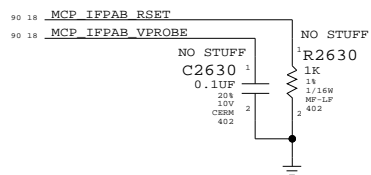
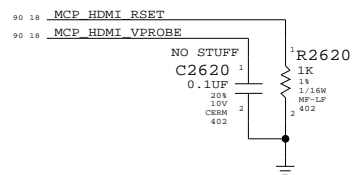
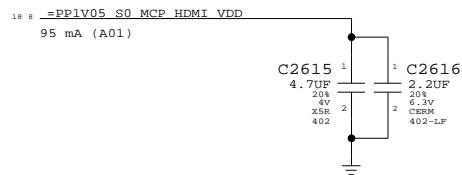
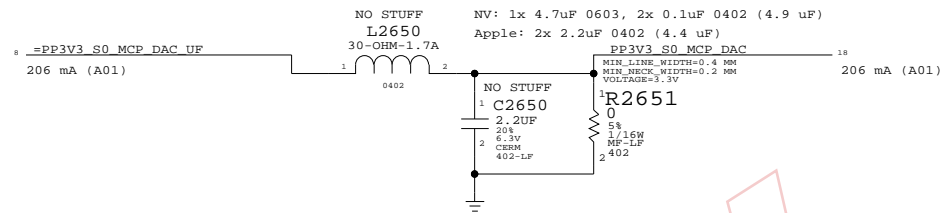
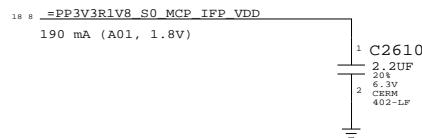
3

2

1

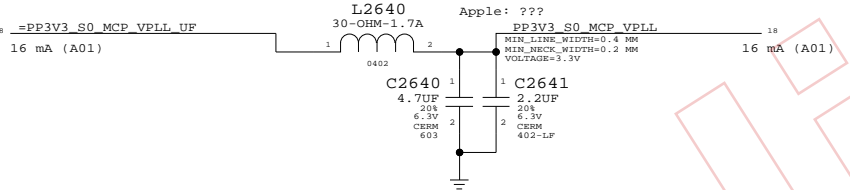
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

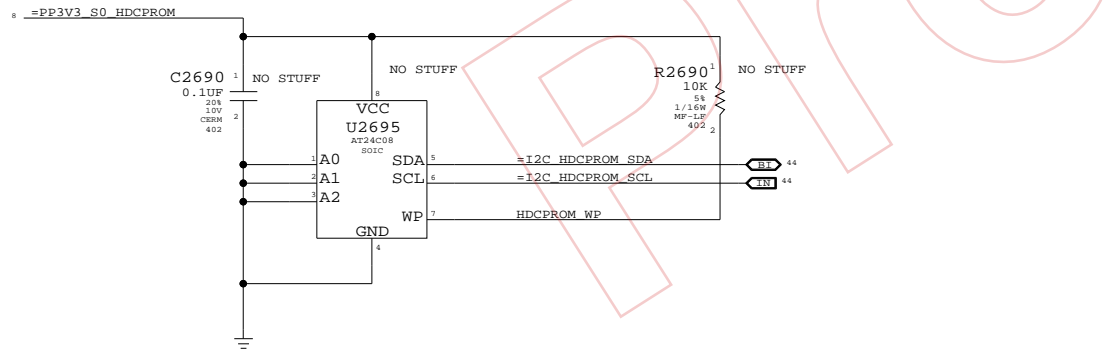
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



18	TP MCP RGB RED	==	NC MCP RGB RED	NO_TEST-TRUE
18	TP MCP RGB GREEN	==	NC MCP RGB GREEN	NO_TEST-TRUE
18	TP MCP RGB BLUE	==	NC MCP RGB BLUE	NO_TEST-TRUE
18	TP MCP RGB HSYNC	==	NC MCP RGB HSYNC	NO_TEST-TRUE
18	TP MCP RGB VSYNC	==	NC MCP RGB VSYNC	NO_TEST-TRUE
90 18	CRT IG R C PR	==	NC CRT IG R C PR	NO_TEST-TRUE
90 18	CRT IG G Y Y	==	NC CRT IG G Y Y	NO_TEST-TRUE
90 18	CRT IG B_COMP PB	==	NC CRT IG B_COMP PB	NO_TEST-TRUE
90 18	CRT IG HSYNC	==	NC CRT IG HSYNC	NO_TEST-TRUE
90 18	CRT IG VSYNC	==	NC CRT IG VSYNC	NO_TEST-TRUE
18	TP MCP RGB_DAC_RSET	==	NC MCP RGB_DAC_RSET	NO_TEST-TRUE
18	TP MCP RGB_DAC_VREF	==	NC MCP RGB_DAC_VREF	NO_TEST-TRUE
90 18	MCP_TV_DAC_RSET	==	NC MCP_TV_DAC_RSET	NO_TEST-TRUE
90 18	MCP_TV_DAC_VREF	==	NC MCP_TV_DAC_VREF	NO_TEST-TRUE
18	MCP_CLK27M_XTALIN	==	NC MCP_CLK27M_XTALIN	NO_TEST-TRUE
18	MCP_CLK27M_XTALOUT	==	NC MCP_CLK27M_XTALOUT	NO_TEST-TRUE

HDCP ROM

WF: Open question on which package option(s) nVidia can support.



MCP Graphics Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

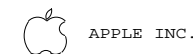
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	26	123

8

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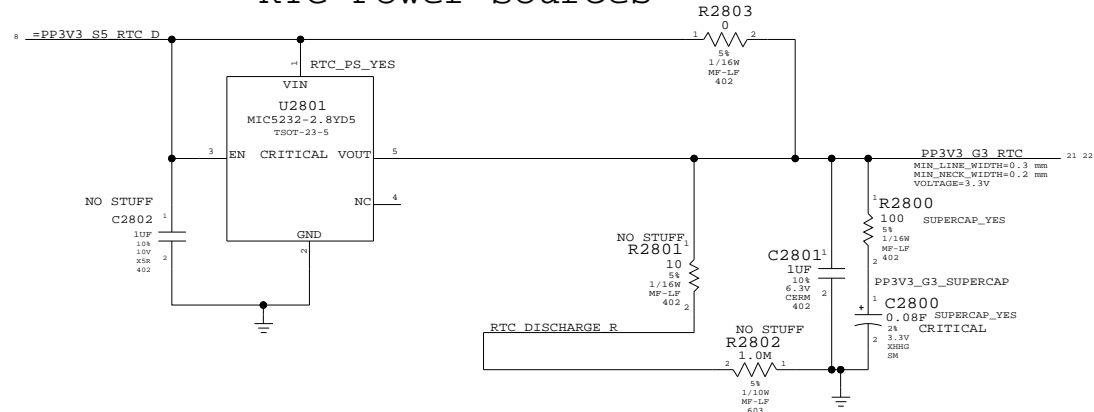
4

3

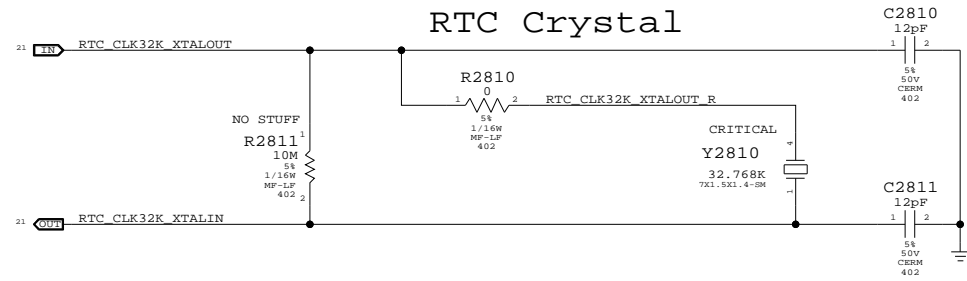
2

1

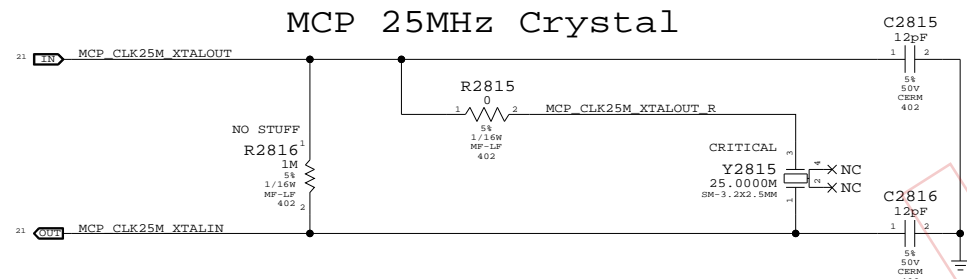
RTC Power Sources



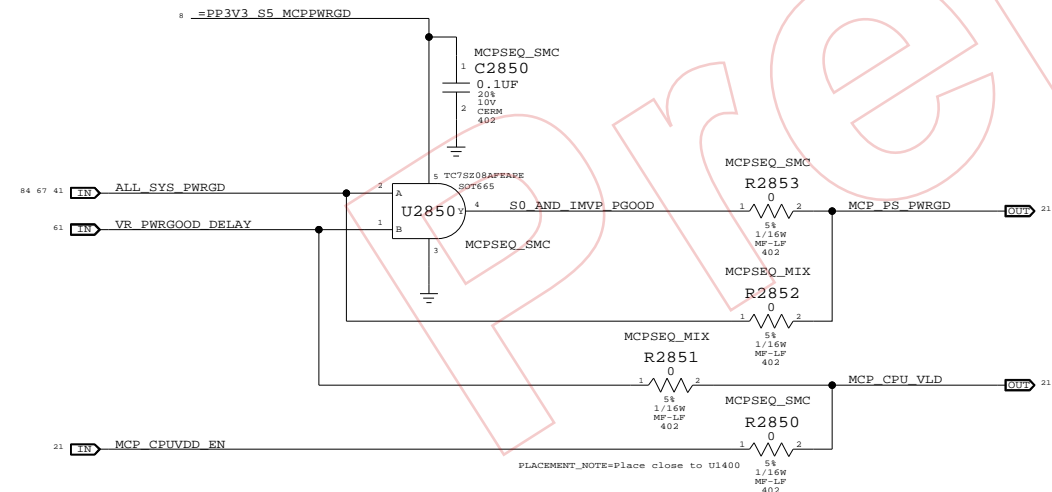
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

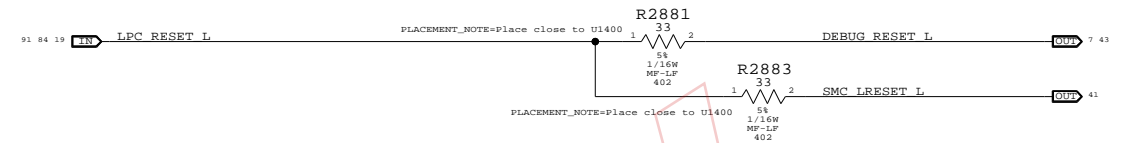
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

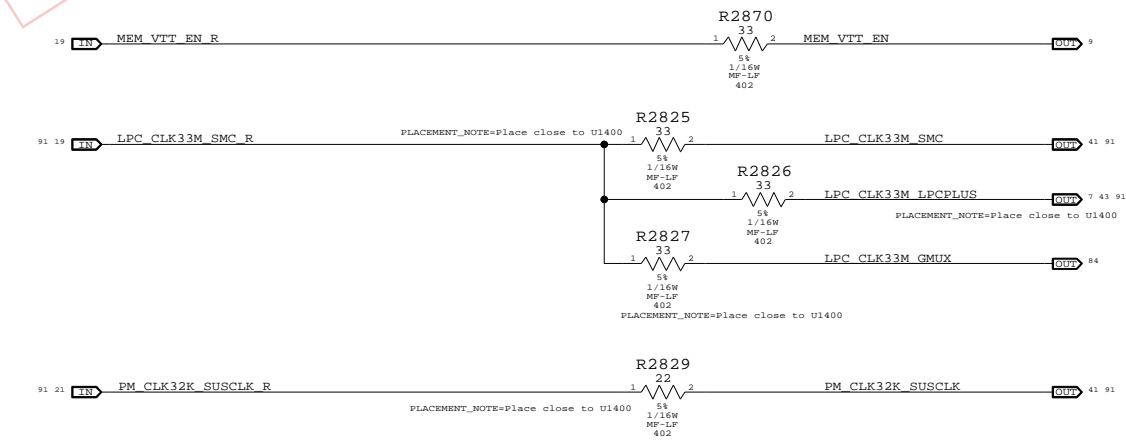
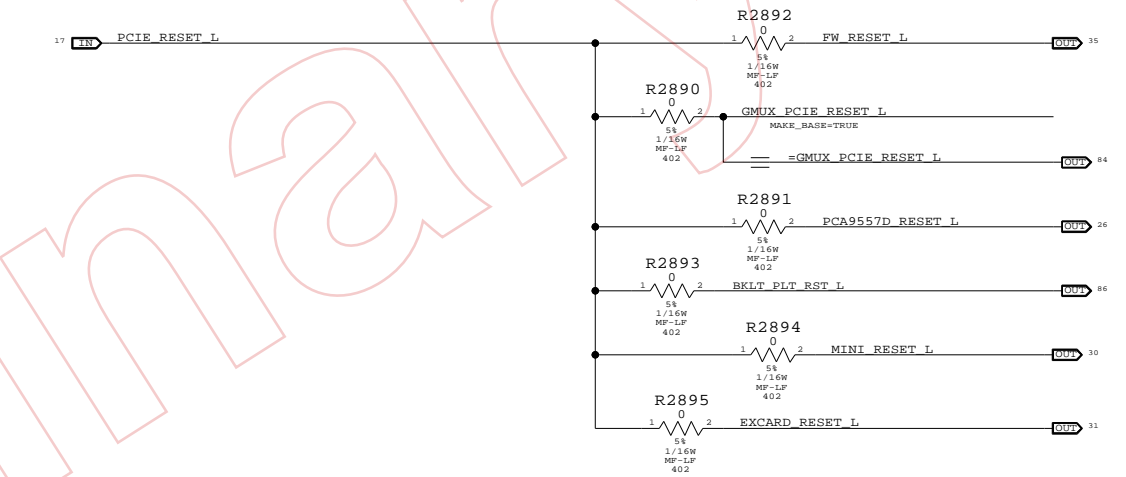
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

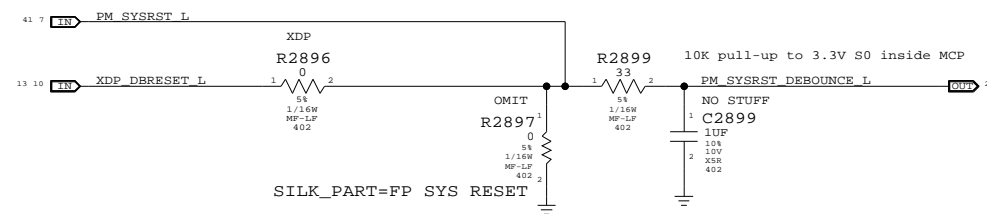
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

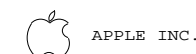
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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	28	123

Page Notes

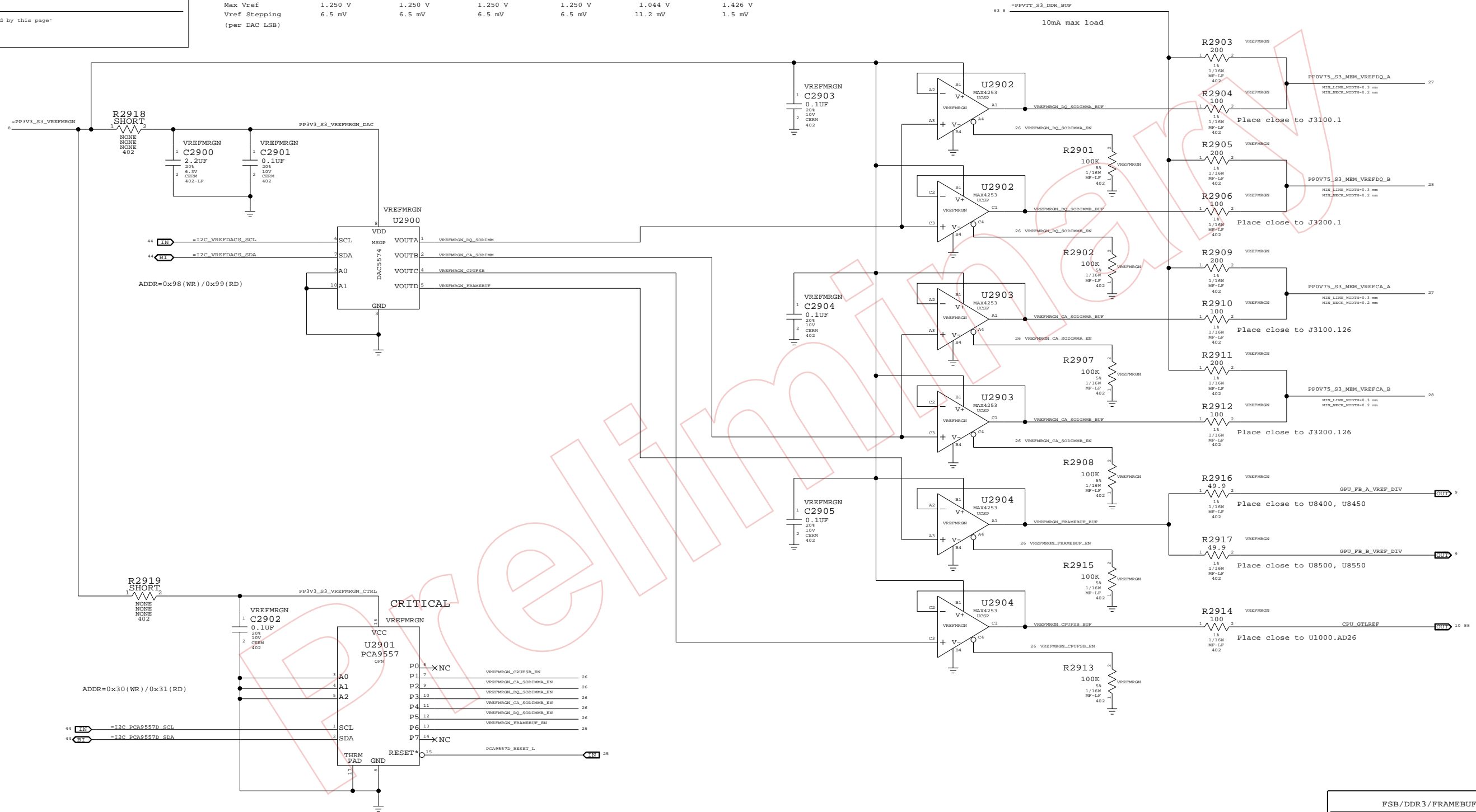
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DCR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN
 NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES_MTL_FILM,0.5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES_MTL_FILM,0.5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES_MTL_FILM,0.5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES_MTL_FILM,0.5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining
 SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008

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APPLE INC.	SCALE	DRAWING NUMBER	REV.
	NONE	051-7656	31
NONE		SHT	OF
NONE		29	123

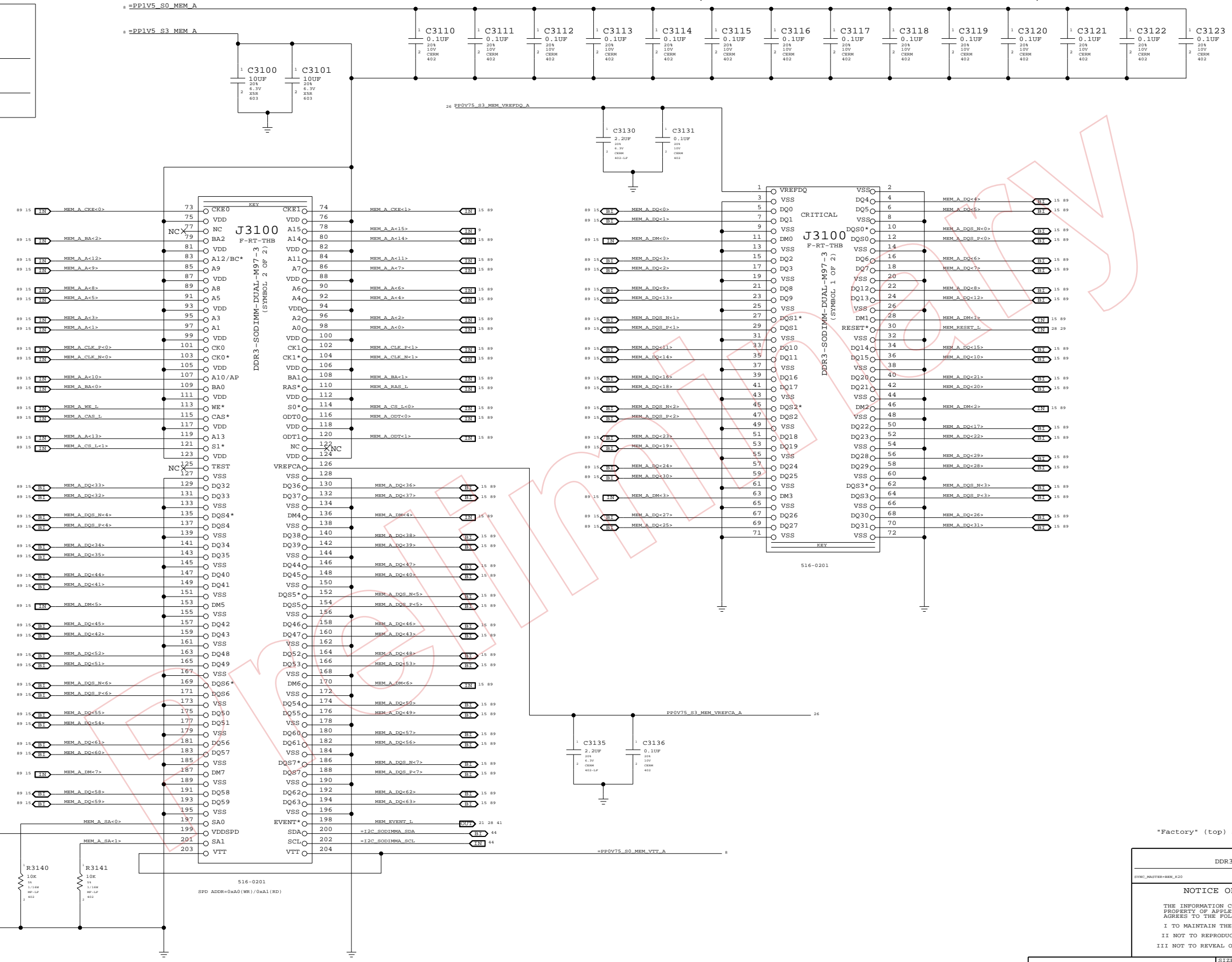
Page Notes

Power aliases required by this page:
 - P1V5_S0_MEM_A
 - P1V5_S3_MEM_A
 - P1V5_S3_MEM_VTT_A
 - P1V5_S0_MEM_A (2.5 - 3.0V)

Signal aliases required by this page:
 - I2C_S0D1MMA_SCL
 - I2C_S0D1MMA_SDA

SDM options provided by this page:
 (NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYMC_MASTER=MEM_E20 SYMC_DATE=06/10/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	NONE	SHT	OF
		31	123

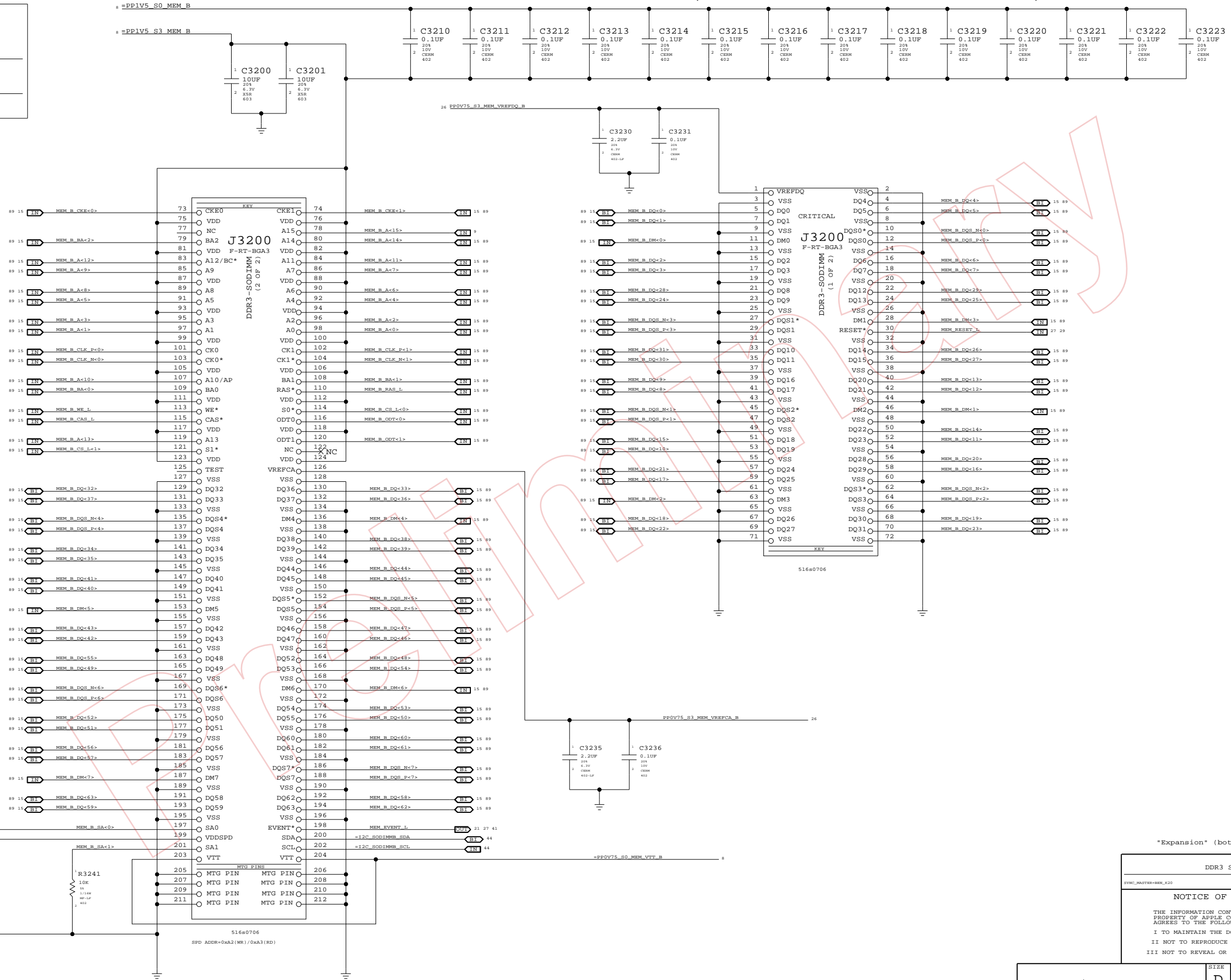
Page Notes

Power aliases required by this page:
 - PP1V5_S0_MEM_B
 - PP1V5_S3_MEM_B
 - PP0V75_S0_MEM_VTT_B
 - PP0V75_S3_MEM_VTT_B
 - PP0V75_S0_MEM_B (2.5 - 3.3V)
 - PP0V75_S3_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
 - I2C_S0D3MMB_SCL
 - I2C_S0D3MMB_SDA

SDM options provided by this page:
 (None)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B
 SYNC_MASTER=MEM_E20 SYNC_DATE=07/14/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	32	123

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D

D

C

C

B

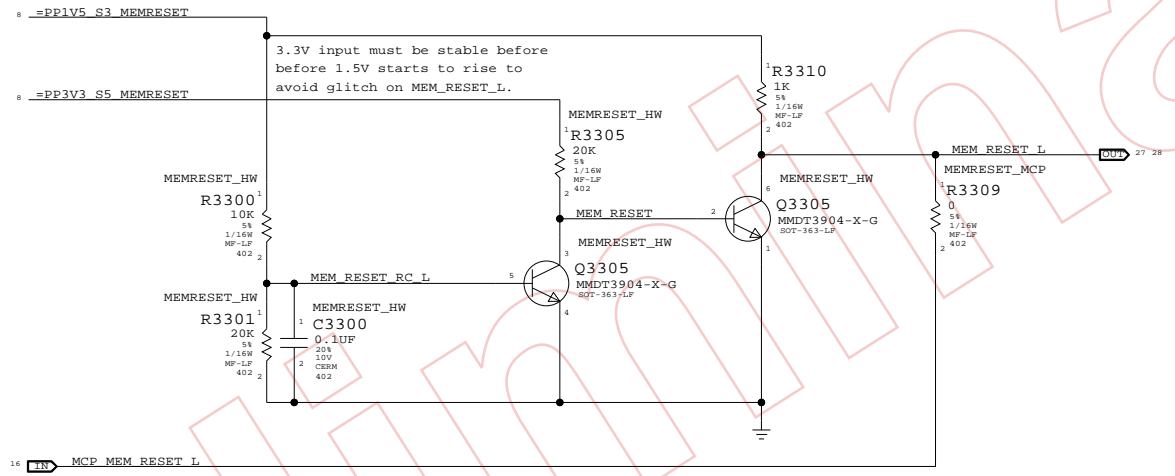
B

A

A

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



Pre-release

DDR3 Support

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	33		

8

7

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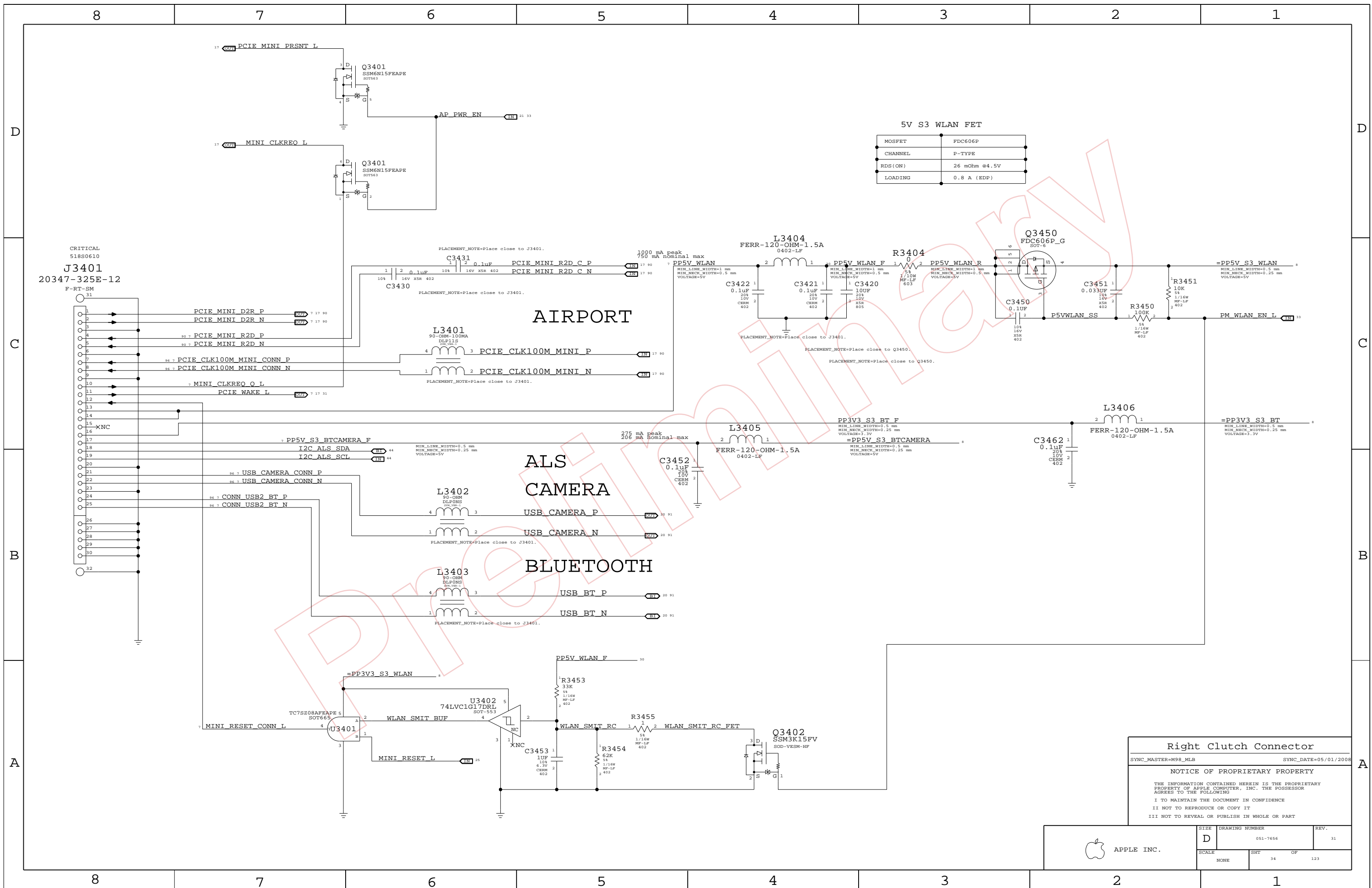
5

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2

1



CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

AIRPORT

ALS CAMERA

BLUETOOTH

Right Clutch Connector

SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

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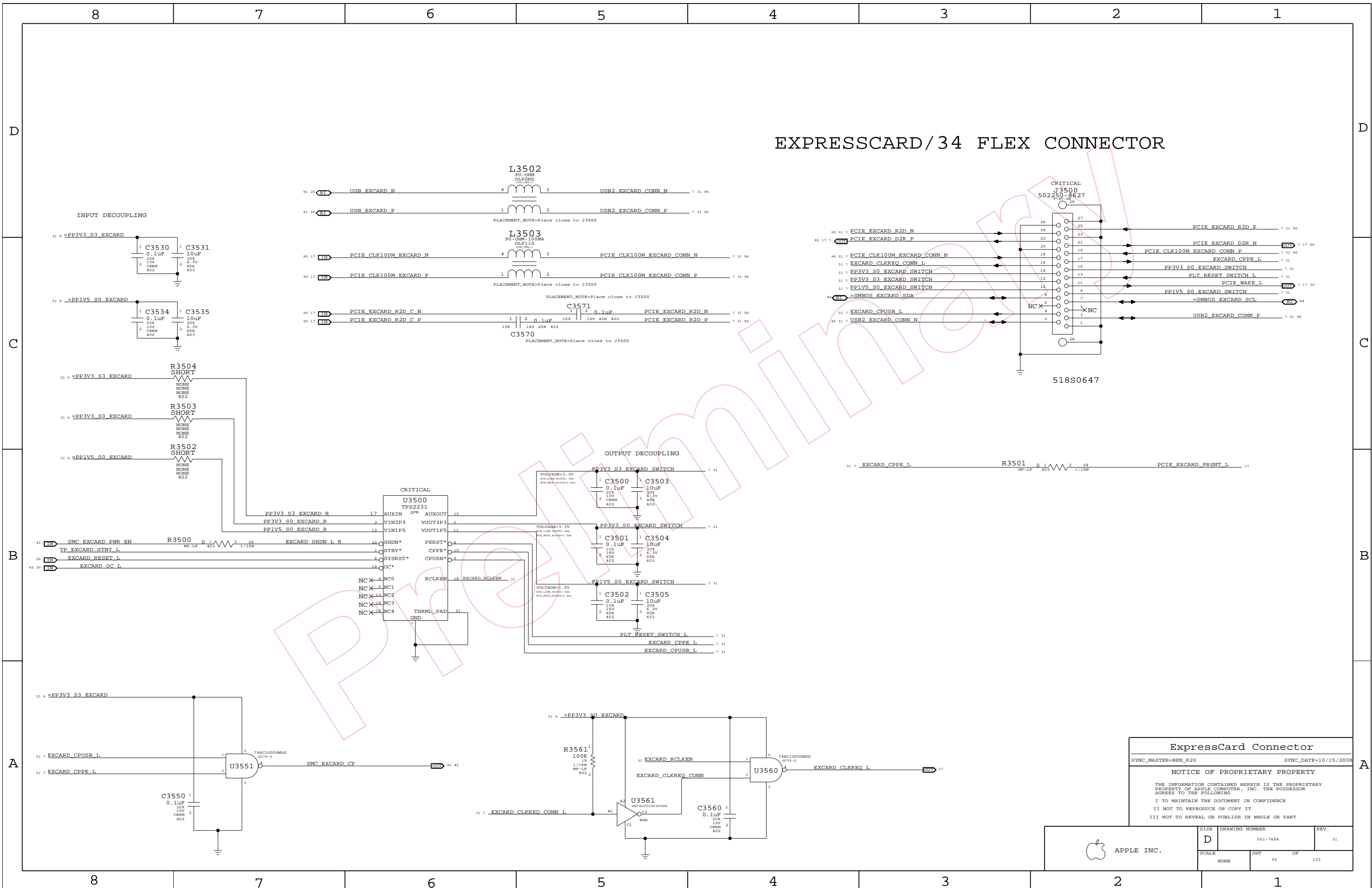
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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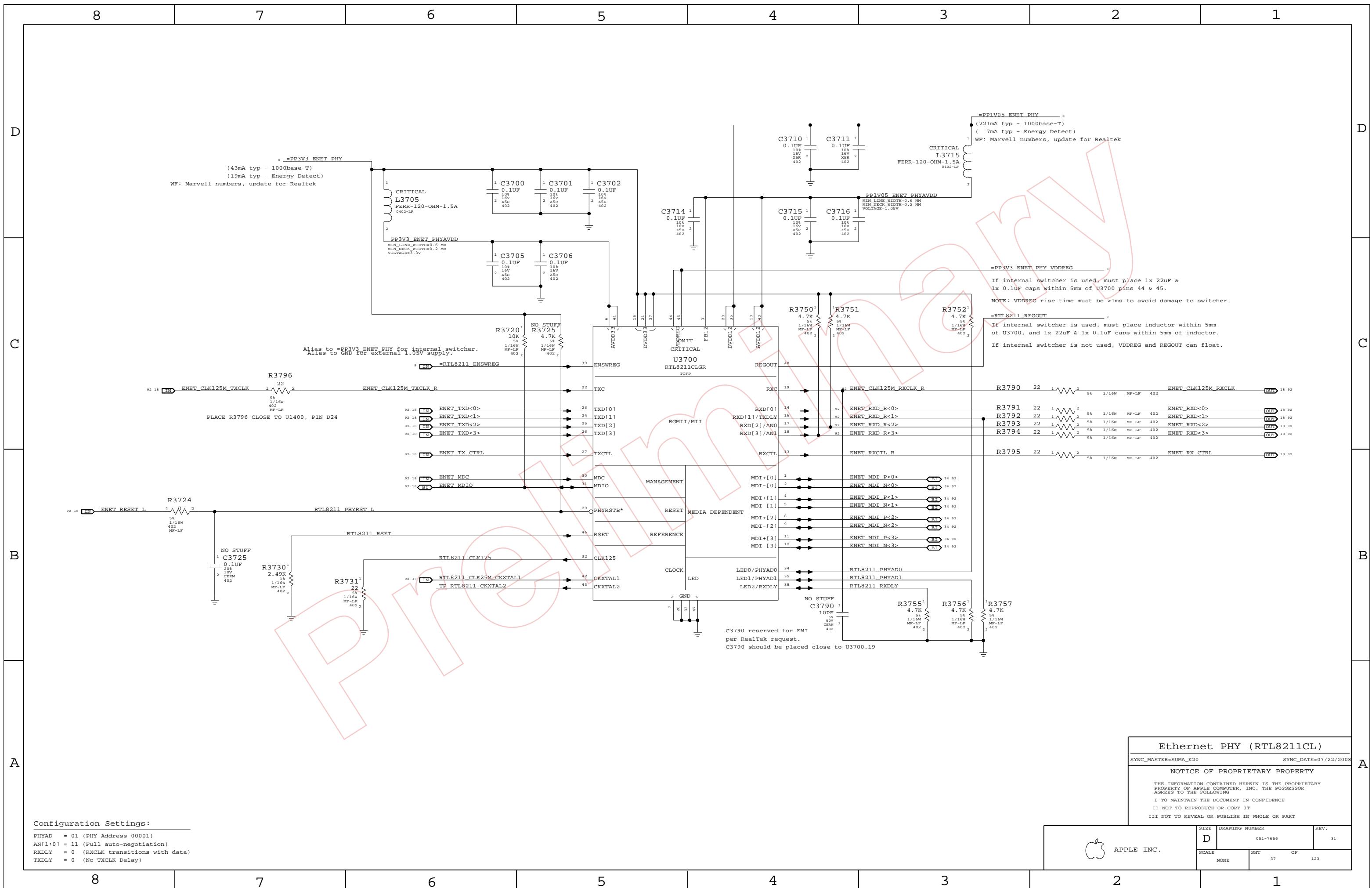
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	34		

EXPRESSCARD/34 FLEX CONNECTOR



ExpressCard Connector
 SYNC_MASTER=BEN_K20 SYNC_DATE=10/15/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	35		



=PP3V3_ENET_PHY
(43mA typ - 1000base-T)
(19mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek

=PP1V05_ENET_PHY
(221mA typ - 1000base-T)
(7mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek

Alias to =PP3V3_ENET_PHY for internal switcher.
Alias to GND for external 1.05V supply.

=PP3V3_ENET_PHY_VDDREG
If internal switcher is used, must place 1x 22uF &
1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

=RTL8211_REGOUT
If internal switcher is used, must place inductor within 5mm
of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.

C3790 reserved for EMI
per RealTek request.
C3790 should be placed close to U3700.19

PLACE R3796 CLOSE TO U1400, PIN D24

Configuration Settings:
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

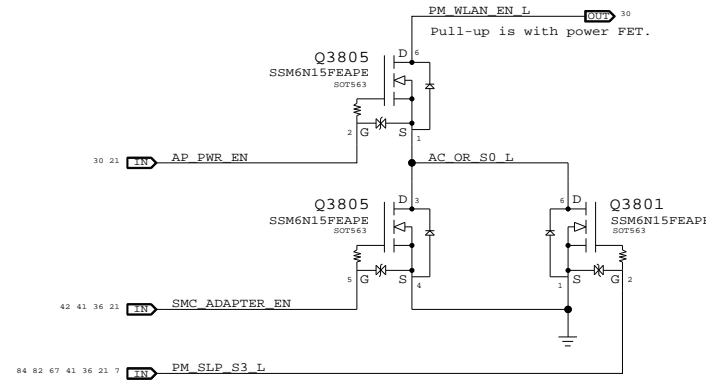
Ethernet PHY (RTL8211CL)
SYNC_MASTER=SUMA_K20 SYNC_DATE=07/22/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	37		

WLAN Enable Generation

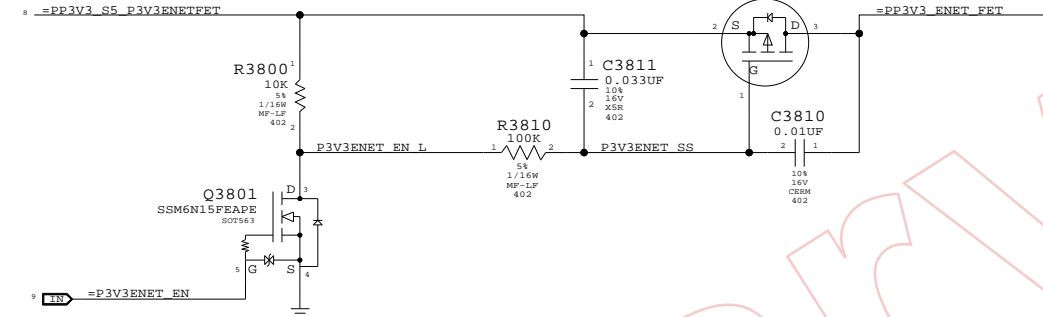
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

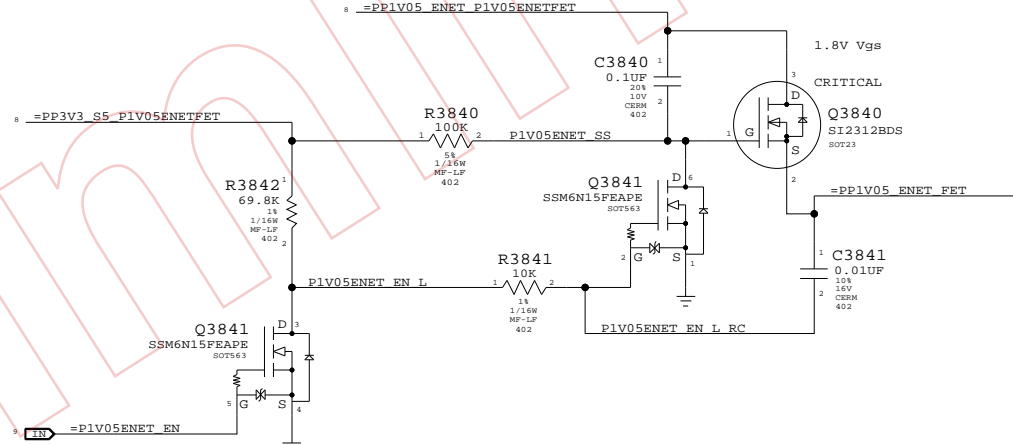
@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)
CRITICAL
Q3810
NTR4101P
SOT-23-NP



MOBILE:
Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

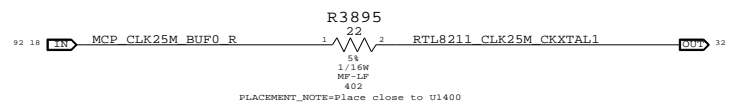
1.8V Vgs
CRITICAL
Q3840
SI2312BDS
SOT23



Non-ARB:
Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

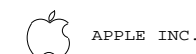


Ethernet & AirPort Support

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

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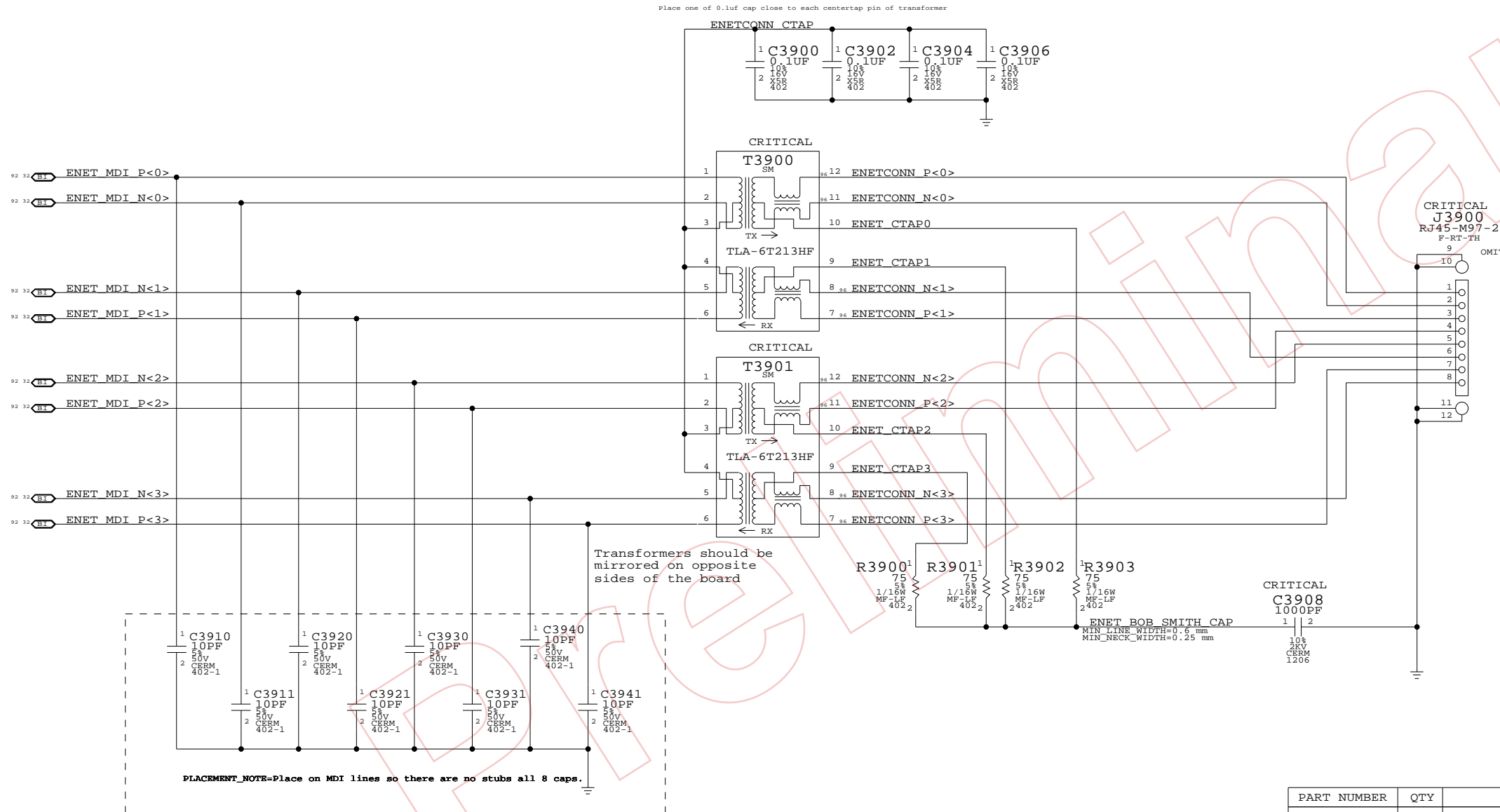
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	38	123

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0636	1	CONN, RJ45, HB, 10/100TX	J3900	CRITICAL	

Ethernet Connector

SYNC_MASTER=SUMA_K20 SYNC_DATE=07/15/2008

NOTICE OF PROPRIETARY PROPERTY

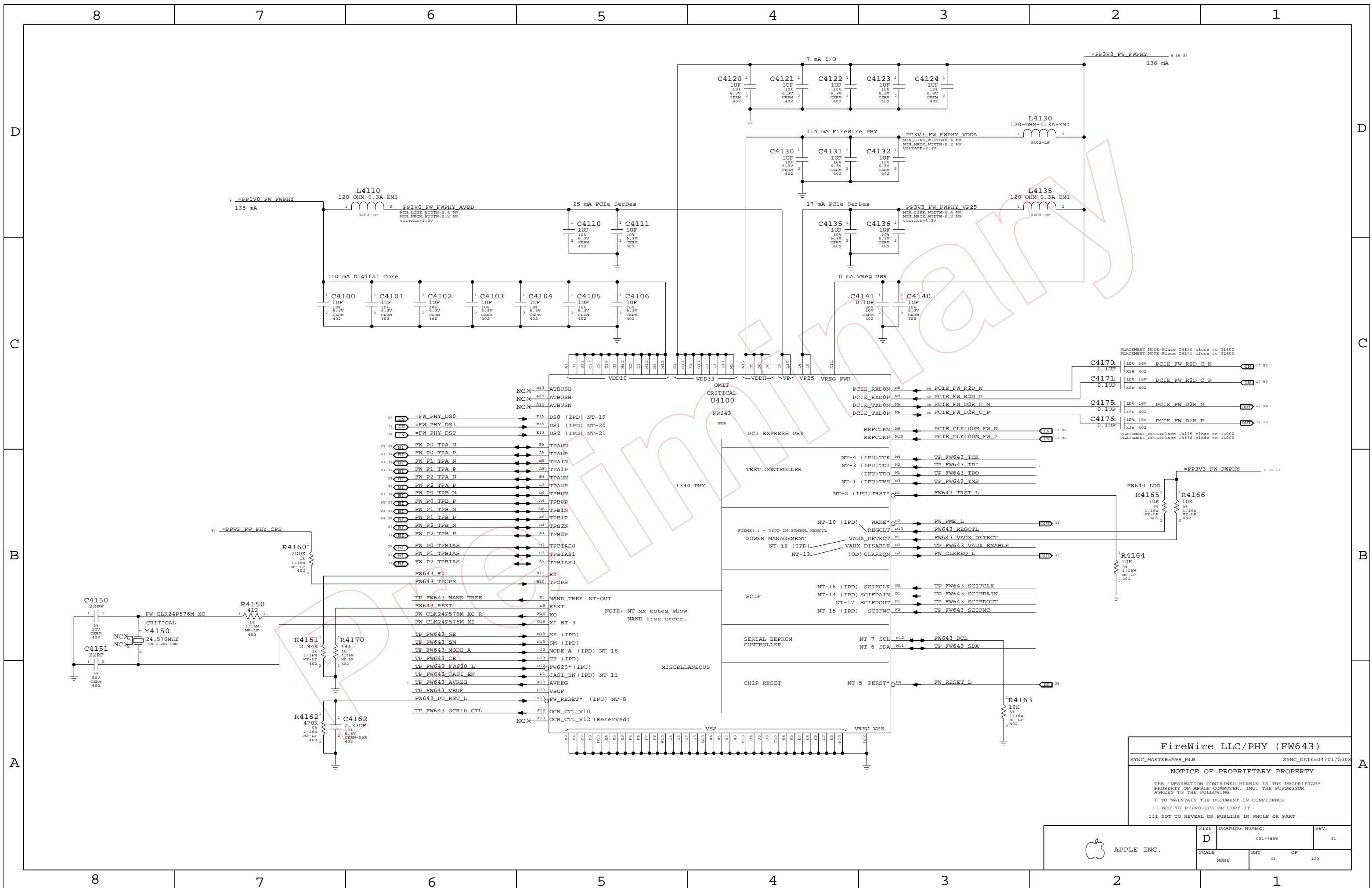
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	39		



FireWire LLC/PHY (FW643)

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHEET 41	OF 123

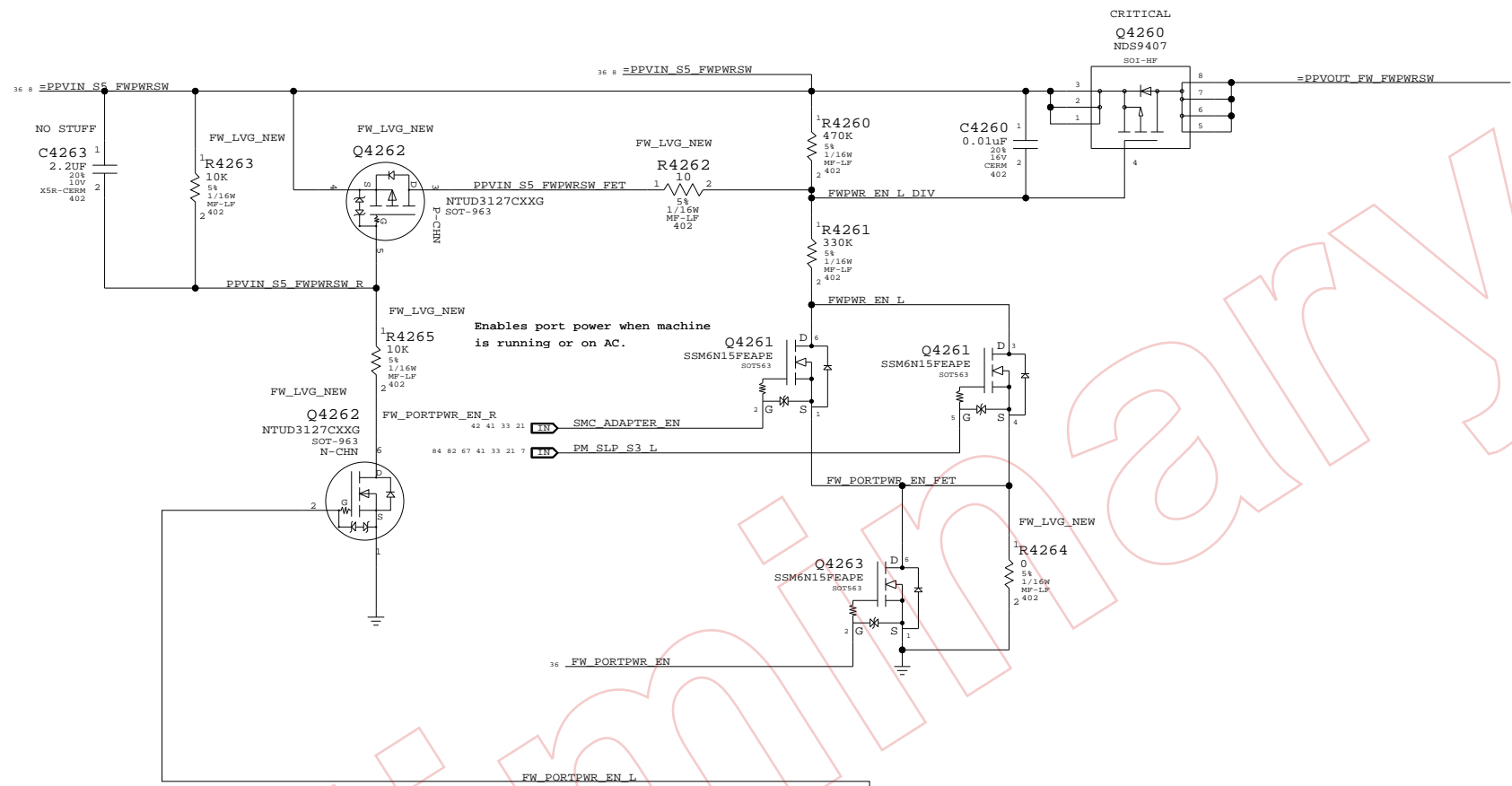
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWRSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

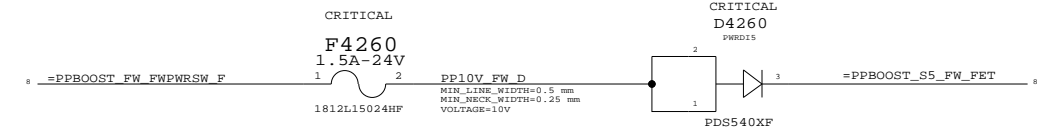
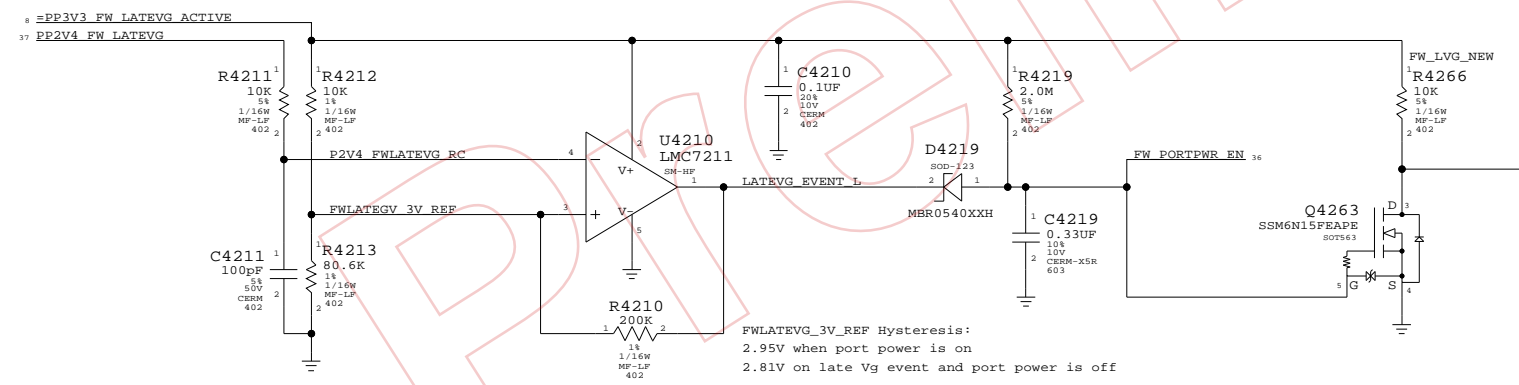
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



FireWire Port Power
 SYNC_MASTER=YWU_K20 SYNC_DATE=05/28/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	42		

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

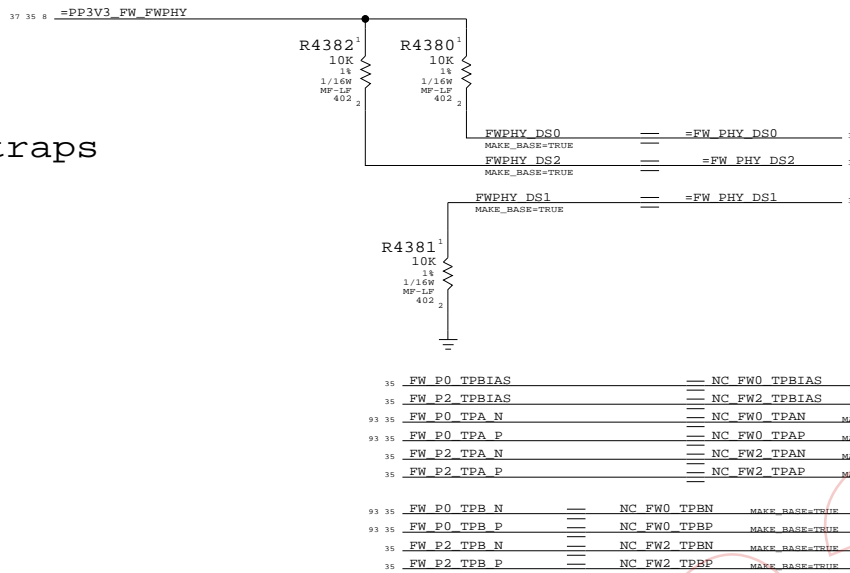
NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

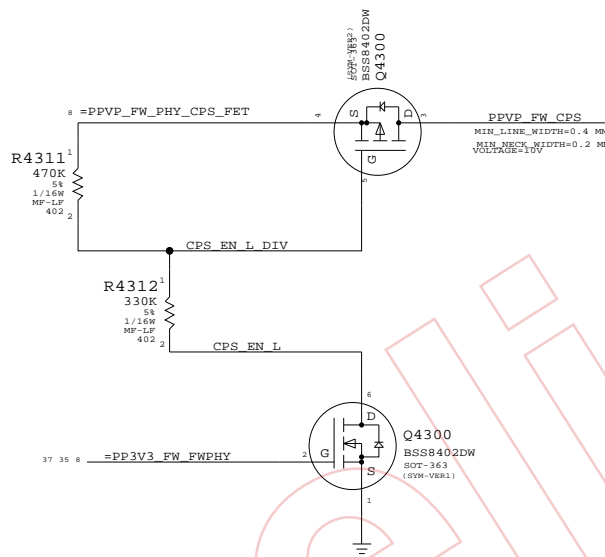
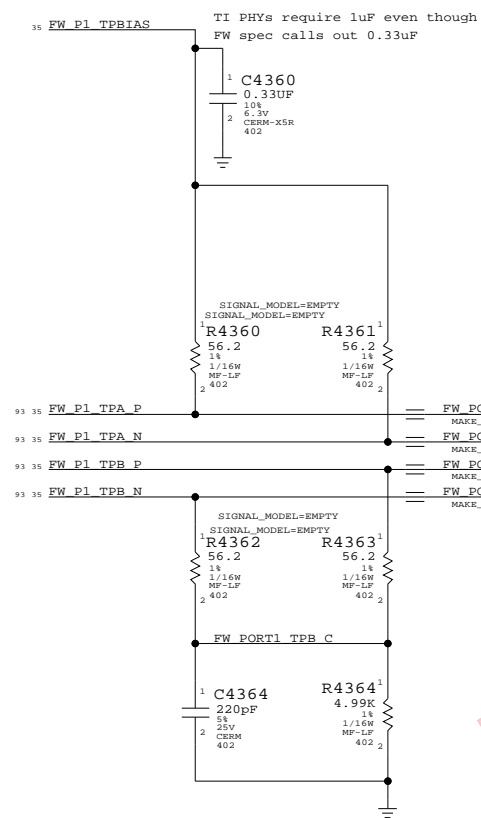
Configures PHY for:

- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

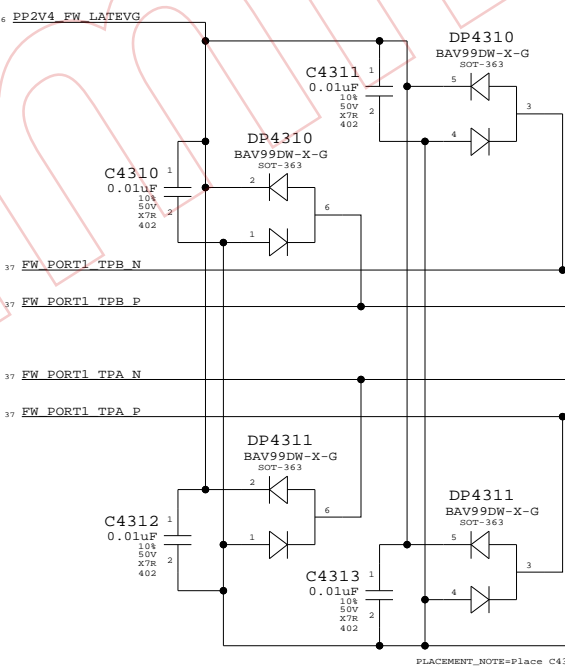


Termination

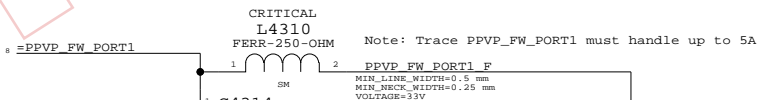
Place close to FireWire PHY



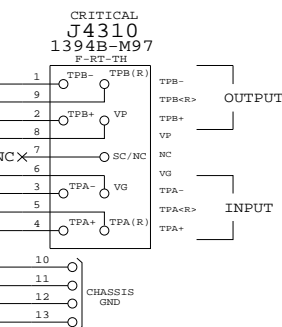
"Snapback" & "Late VG" Protection



Cable Power



PORT 1 BILINGUAL

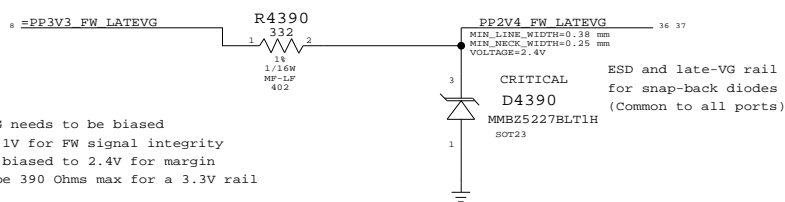


AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power



FireWire Ports		
SYNC_MASTER=M98_MLB	SYNC_DATE=07/14/2008	
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	D	051-7656	31
SCALE	SHT	OF	123
NONE	43		

8

7

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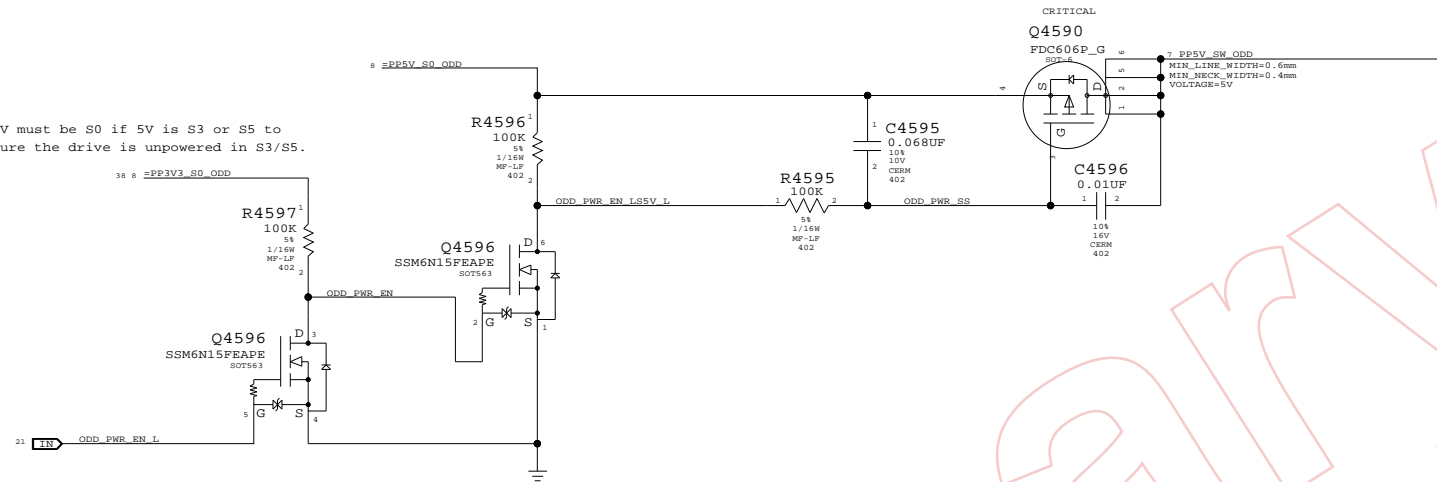
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2

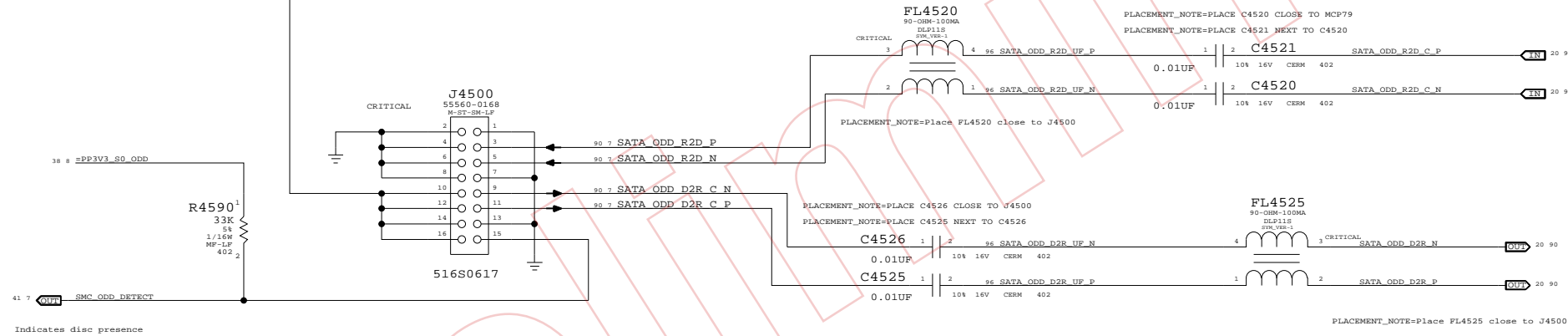
1

ODD Power Control

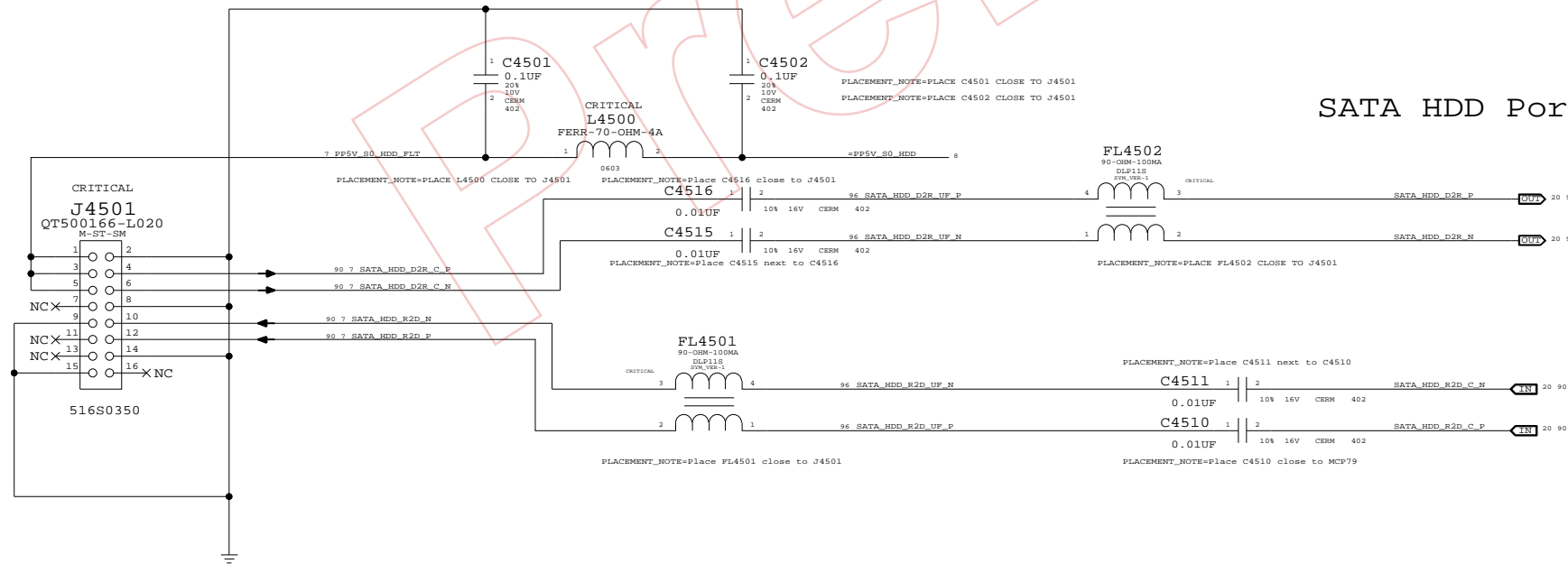
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.



SATA ODD Port



SATA HDD Port



SATA Connectors		
SYNC_MASTER=M98_MLB	SYNC_DATE=05/01/2008	
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SCALE	SHT	OF	123
NONE	45		

8

7

6

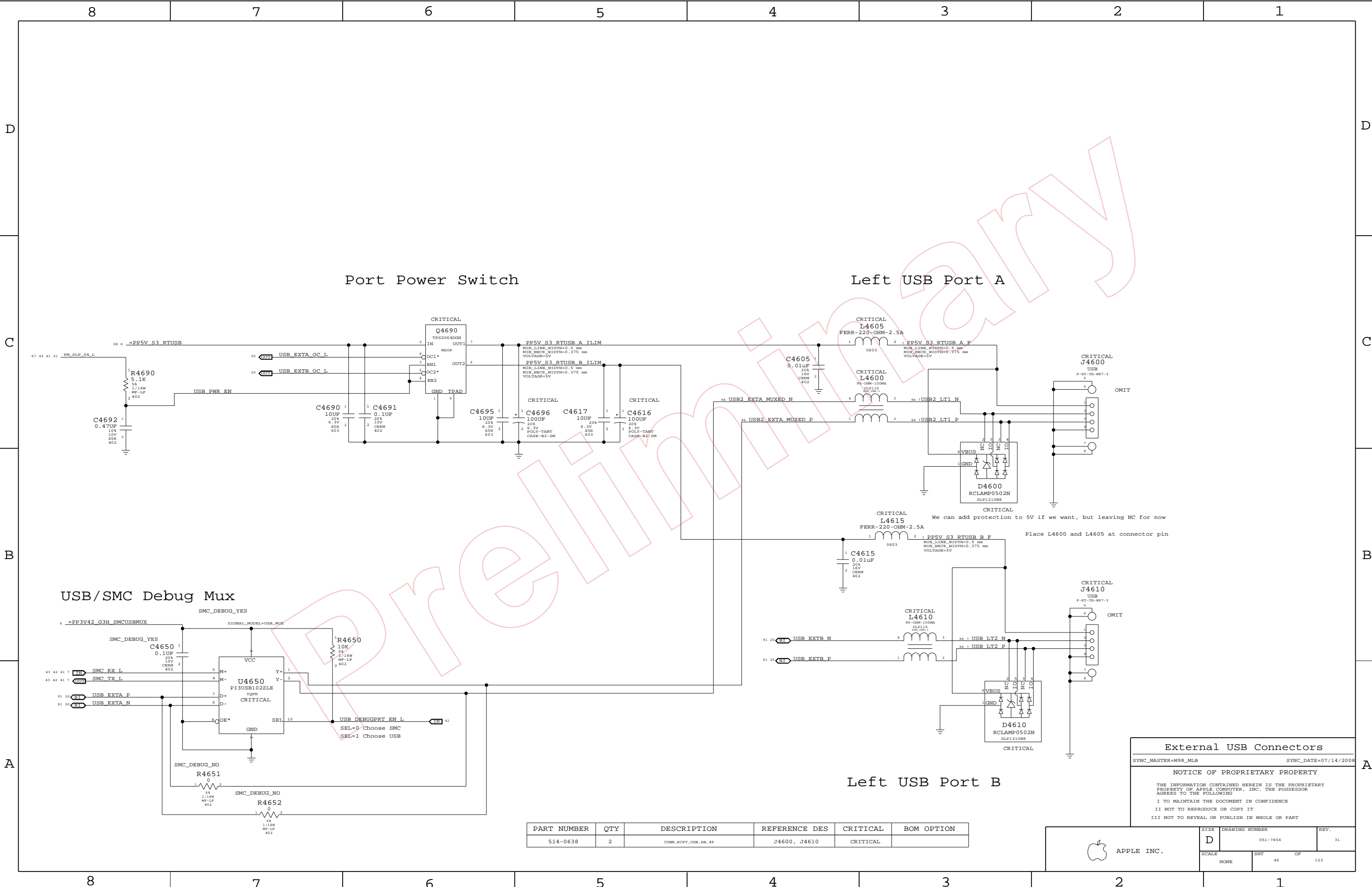
5

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1



External USB Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=07/14/2008

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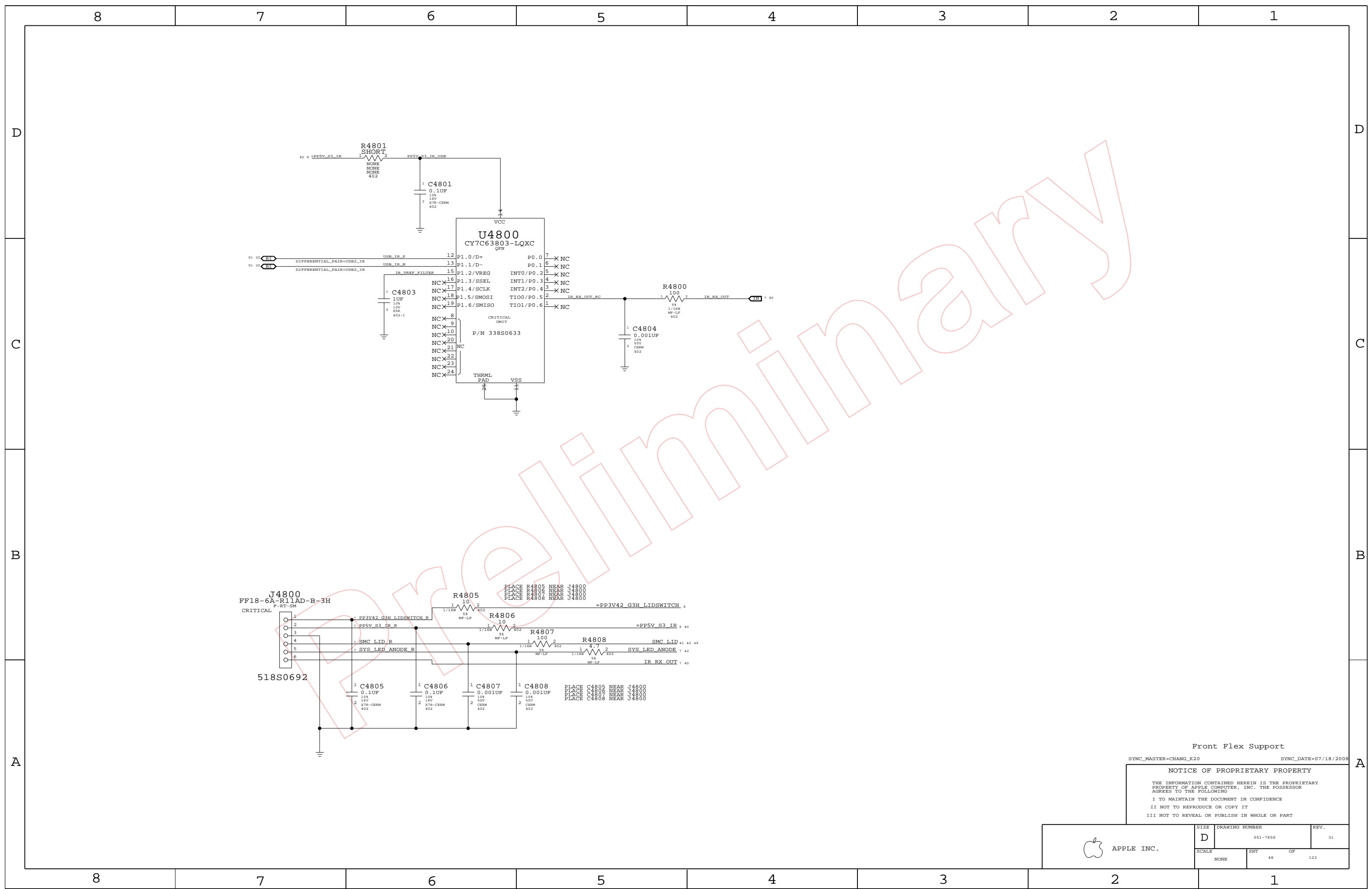
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	2	CONN, RCPT, USB, HB, 4P	J4600, J4610	CRITICAL	

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	46		



Front Flex Support

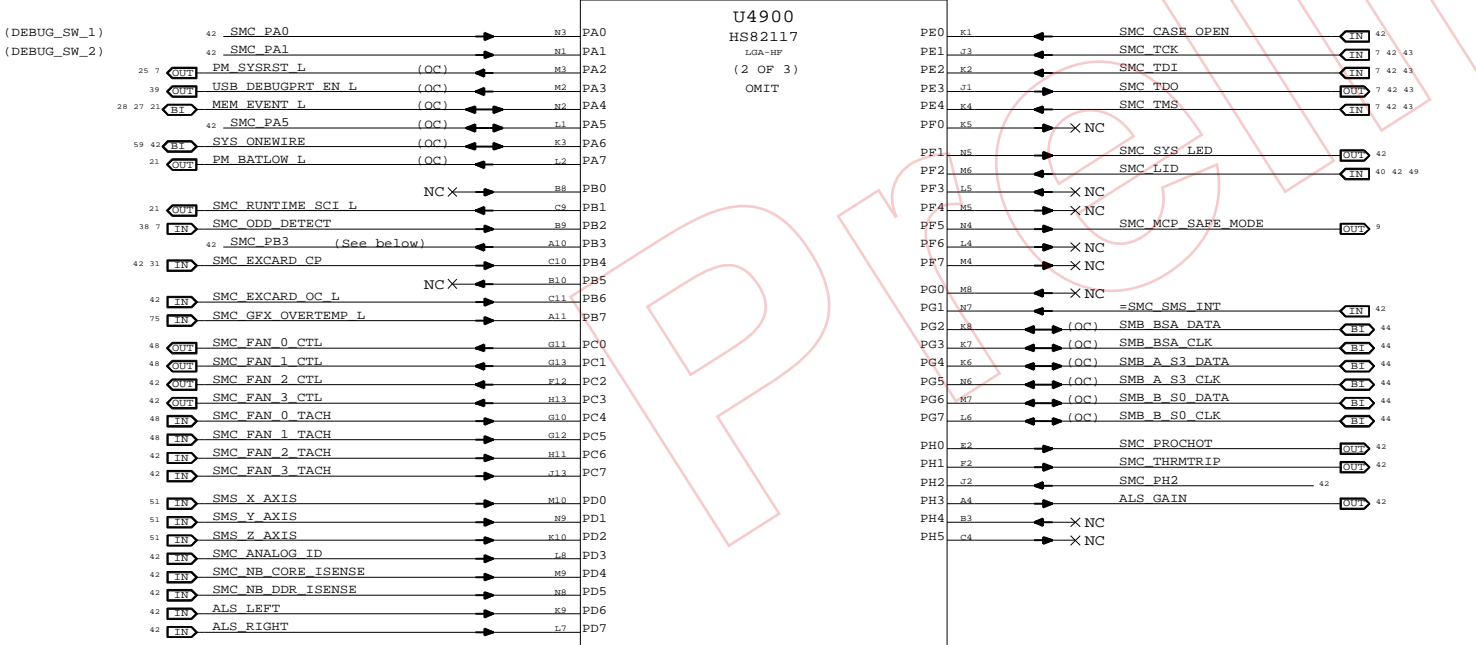
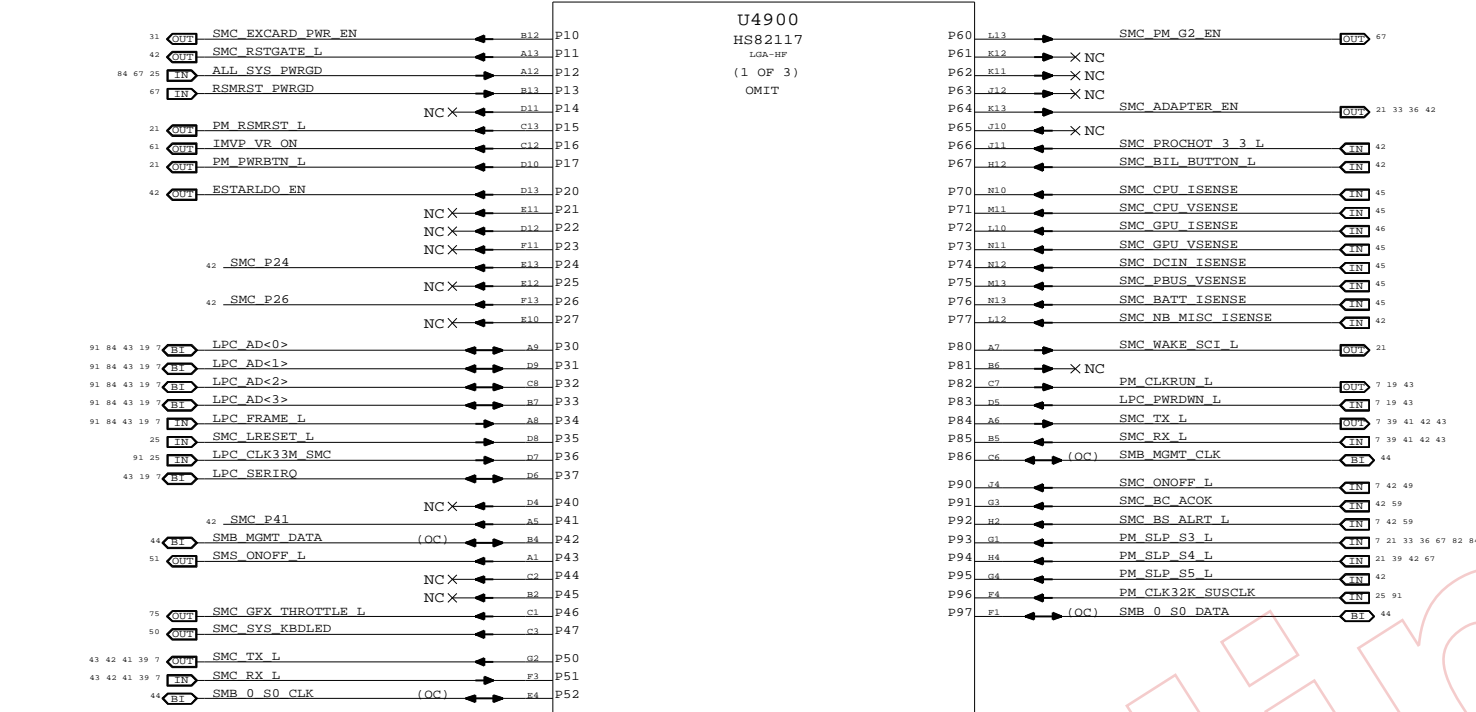
SYNC_MASTER=CHANG_K20 SYNC_DATE=07/18/2008

NOTICE OF PROPRIETARY PROPERTY

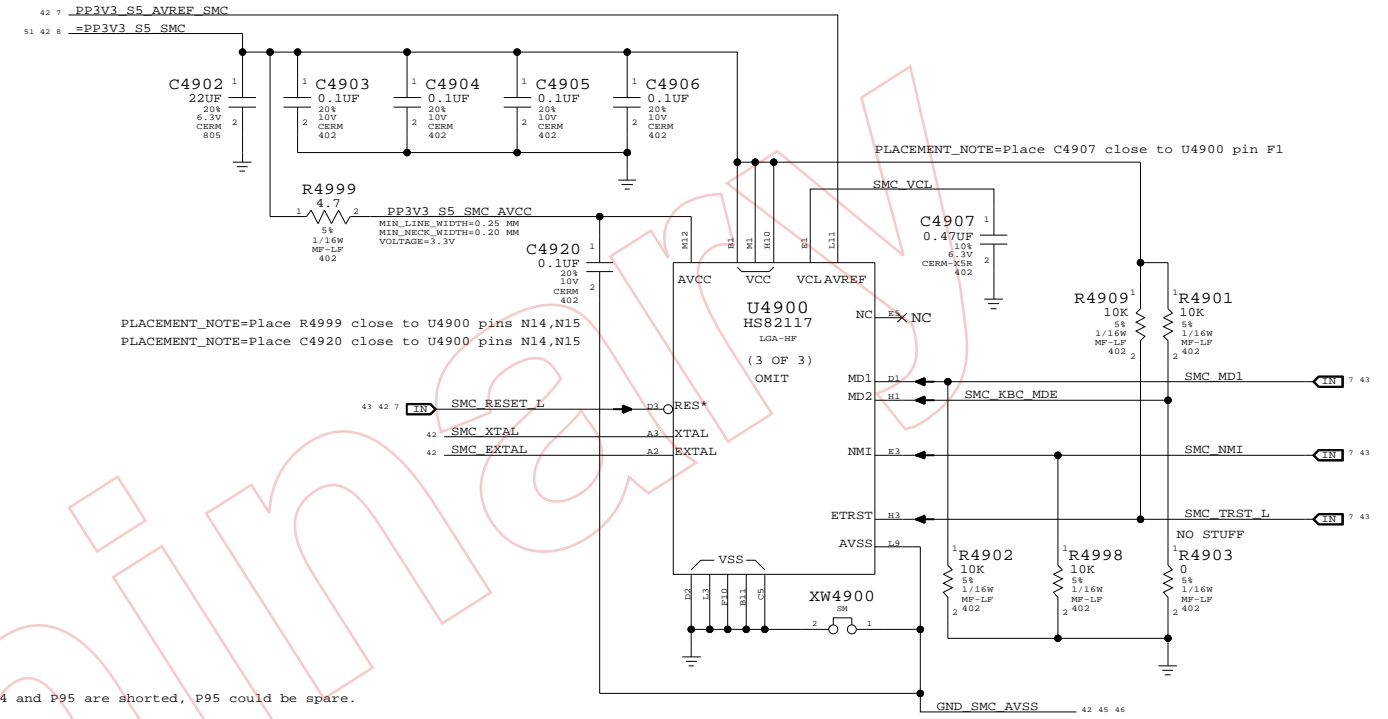
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	48		

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



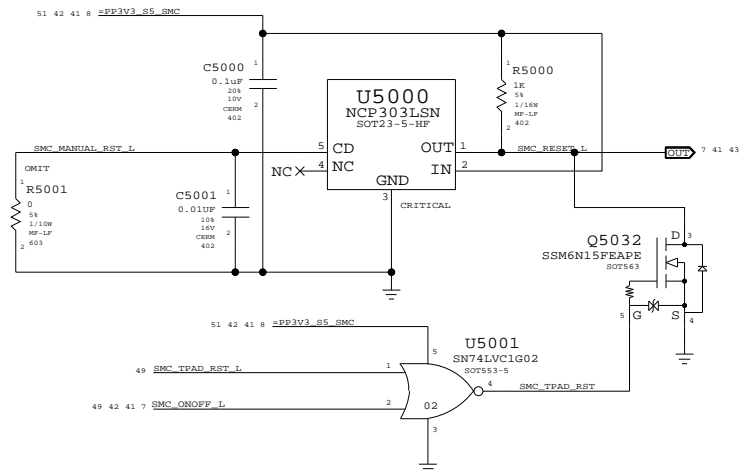
NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

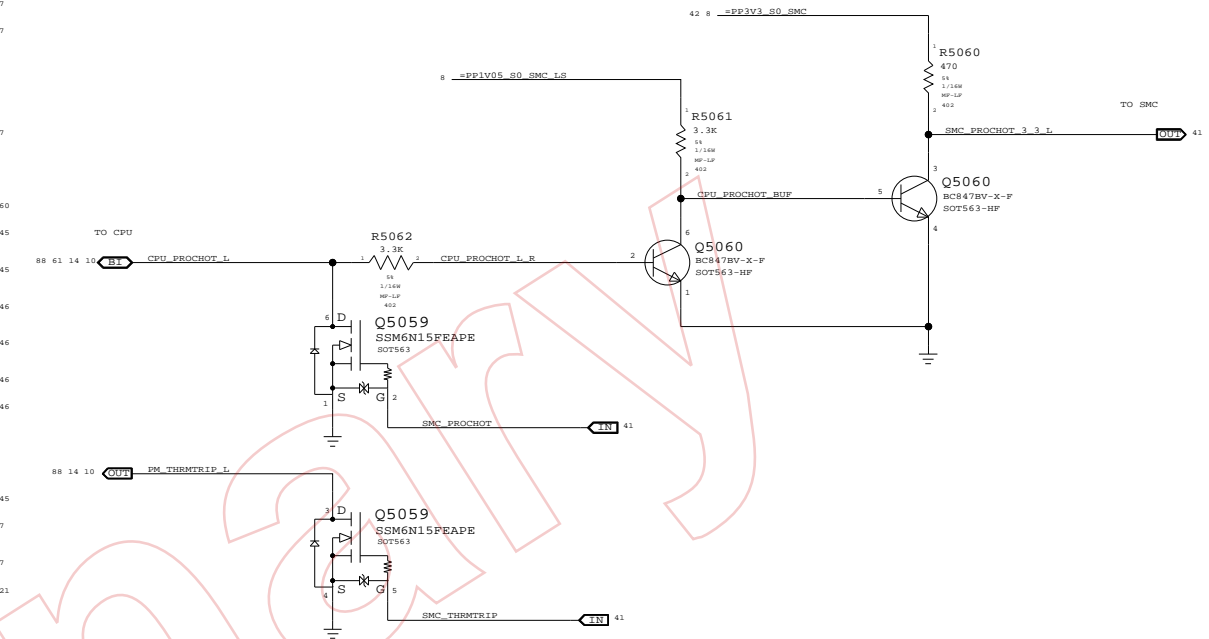
SMC
SYNC_MASTER=T18_MLB SYNC_DATE=06/06/2008
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	D	051-7656	31
SCALE	NONE	SHT	OF 123

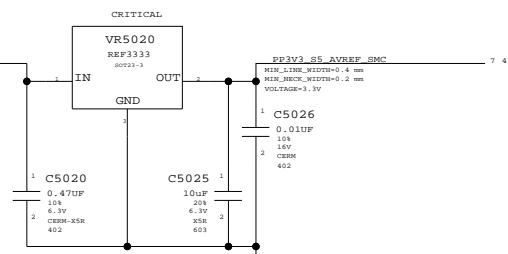
SMC Reset "Button" / Brownout Detect



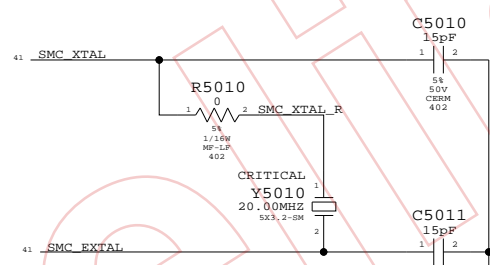
SMC FSB to 3.3V Level Shifting



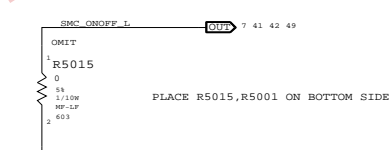
SMC AVREF Supply



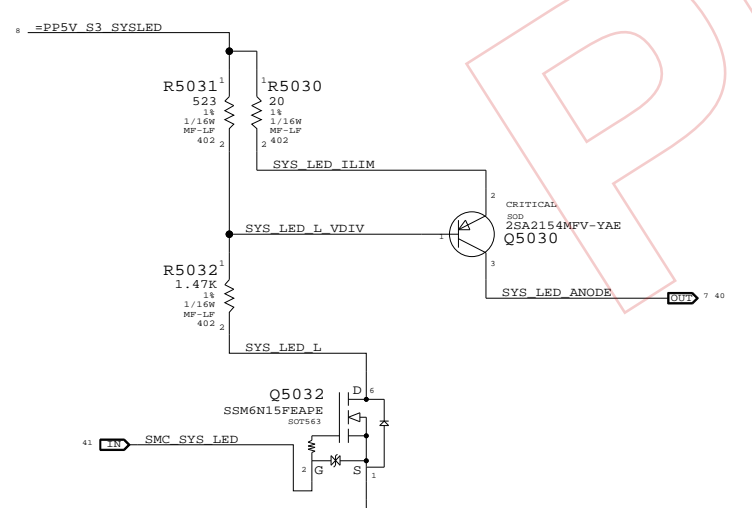
SMC Crystal Circuit



Debug Power "Button"



System (Sleep) LED Circuit



41_SMC_FAN_2_CTL	==	NC_SMC_FAN_2_CTL	7
41_SMC_FAN_2_TACH	==	NC_SMC_FAN_2_TACH	7
41_SMC_FAN_3_CTL	==	NC_SMC_FAN_3_CTL	7
41_SMC_FAN_3_TACH	==	NC_SMC_FAN_3_TACH	7
41_ESTARLDO_EN	==	NC_ESTARLDO_EN	7
59_42_41_SMC_BC_ACLK	==	CHRG_ACLK	60
41_ALS_LEFT	==	SMC_MCP_VSENSE	45
41_ALS_RIGHT	==	SMC_CPU_HI_ISENSE	45
41_SMC_NB_CORE_ISENSE	==	SMC_MCP_CORE_ISENSE	46
41_SMC_NB_DDR_ISENSE	==	SMC_MCP_DDR_ISENSE	46
41_SMC_NB_MISC_ISENSE	==	SMC_CPU_FSB_ISENSE	46
41_SMC_ANALOG_ID	==	SMC_GPU_1VB_ISENSE	46
41_SMC_P24	==	TP_SMC_P24	45
41_SMC_P26	==	SMC_BMON_MUX_SEL	45
41_SMC_P41	==	TP_SMC_P41	7
41_ALS_GAIN	==	NC_ALS_GAIN	7
41_SMC_PB3	==	SMC_TG_THROTTLE_L	21
41_SMC_RSTGATE_L	==	TP_SMC_RSTGATE_L	21

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
9580381	9580393		ALL	Internal 064000-33

41_SMC_BA0	R5091	100K	5A	1/16W	MP-LP	402
41_SMC_PA1	R5092	100K	5A	1/16W	MP-LP	402
49_42_41_7_SMC_ONOFF_L	R5070	10K	5A	1/16W	MP-LP	402
49_41_40_SMC_LID	R5071	100K	5A	1/16W	MP-LP	402
41_SMC_PH2	R5072	10K	5A	1/16W	MP-LP	402
43_41_39_7_SMC_TX_L	R5073	10K	5A	1/16W	MP-LP	402
43_41_39_7_SMC_RX_L	R5074	100K	5A	1/16W	MP-LP	402
59_41_SYS_ONWIRE	R5075	2.0K	5A	1/16W	MP-LP	402
59_41_7_SMC_BS_ALERT_L	R5076	100K	5A	1/16W	MP-LP	402
43_41_7_SMC_TMS	R5077	10K	5A	1/16W	MP-LP	402
43_41_7_SMC_TDO	R5078	10K	5A	1/16W	MP-LP	402
43_41_7_SMC_TDI	R5079	10K	5A	1/16W	MP-LP	402
43_41_7_SMC_TCK	R5080	10K	5A	1/16W	MP-LP	402
42_41_SMC_BIL_BUTTON_L	R5081	10K	5A	1/16W	MP-LP	402
59_42_41_SMC_BC_ACLK	R5087	470K	5A	1/16W	MP-LP	402

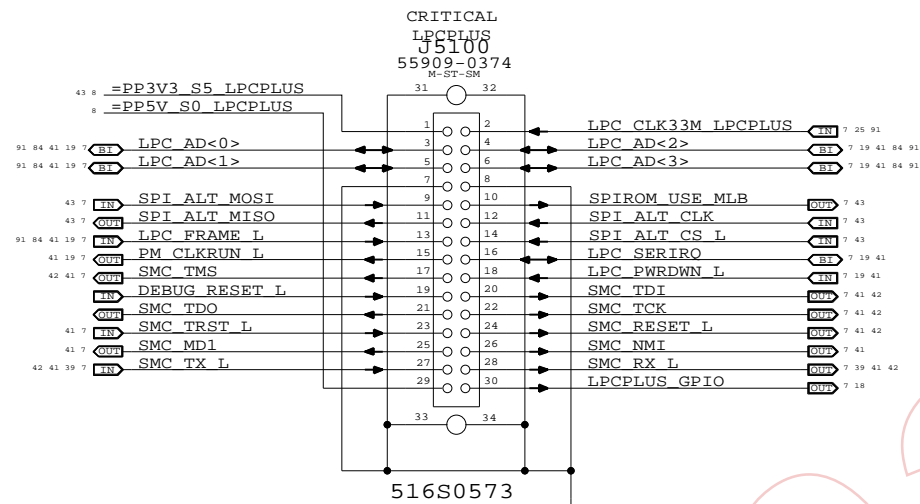
41_36_33_21_SMC_ADAPTER_EN	R5085	10K	5A	1/16W	MP-LP	402
41_SMC_CASE_OPEN	R5086	10K	5A	1/16W	MP-LP	402
41_31_SMC_EXCARD_CP	R5088	10K	5A	1/16W	MP-LP	402
41_PM_SLP_SS_L	R5090	100K	5A	1/16W	MP-LP	402
67_41_39_21_PM_SLP_SS_L	R5090	100K	5A	1/16W	MP-LP	402
41_SMC_PA5	R5089	10K	5A	1/16W	MP-LP	402

SMC Support
SYNC_MASTER=M98_MLS SYNC_DATE=05/01/2008

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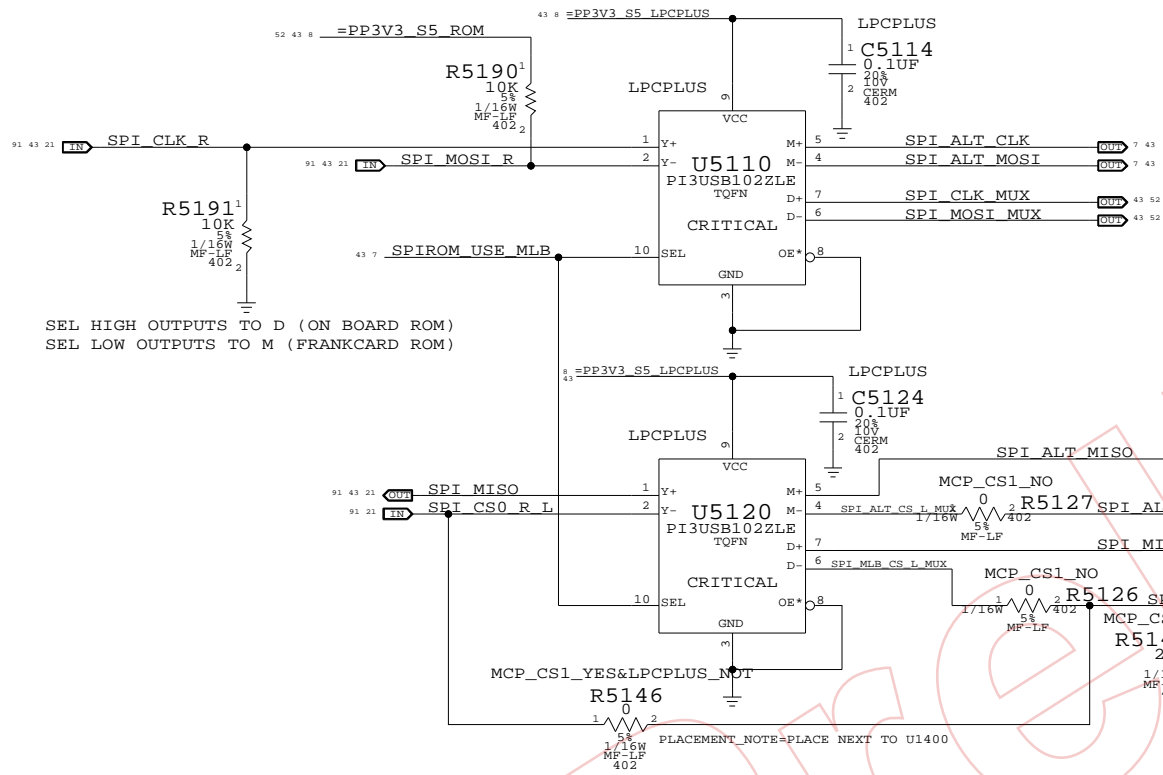
APPLE INC.	SIZE	D	DRAWING NUMBER	051-7656	REV.	31
	SCALE	NONE	SHT	50	OF	123

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

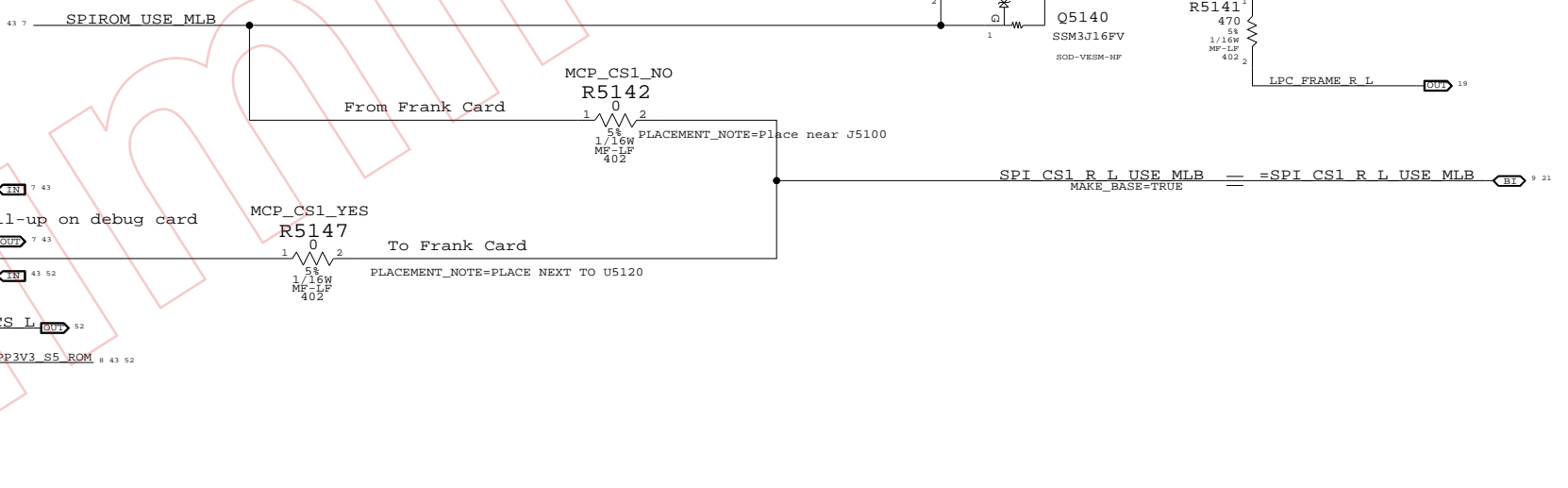


MCP79 Internal SPI MUX Support

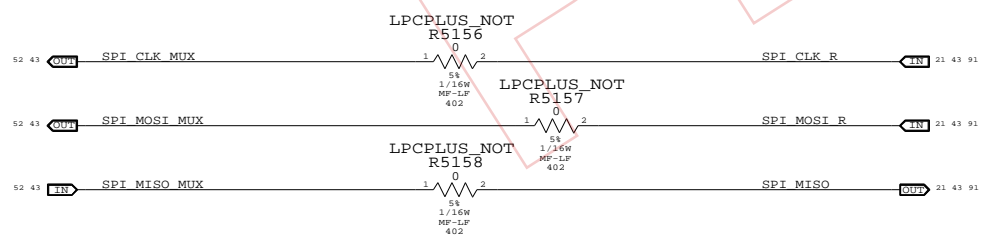
NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX



SPI MUX BYPASS

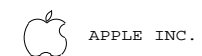


LPC+SPI Debug Connector

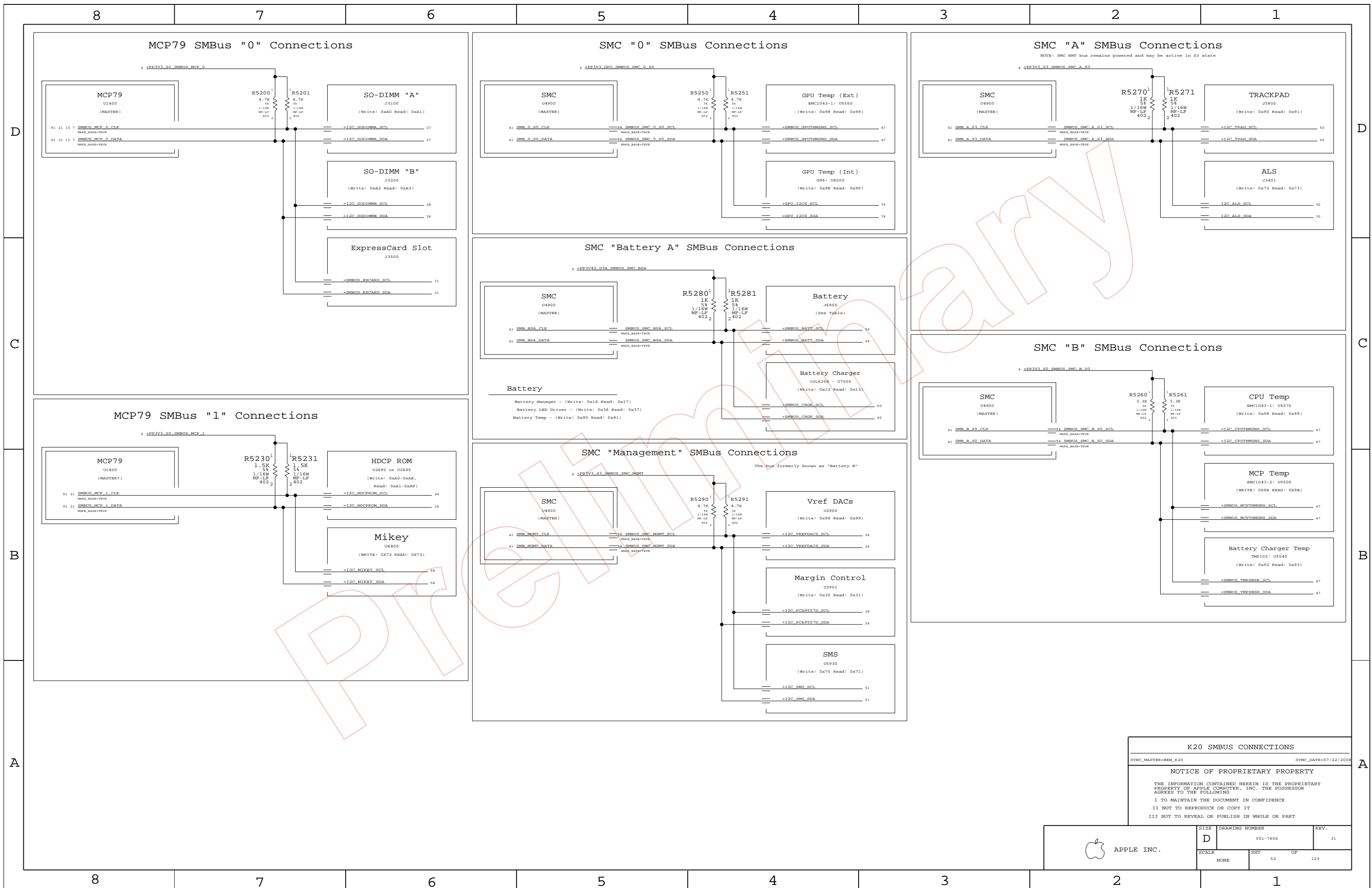
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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	51	123



K20 SMBUS CONNECTIONS

SYNC_MASTER=BEN_K20 SYNC_DATE=07/22/2008

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	D	051-7656	31
SCALE	SHT	OF	123
NONE	52		

D

D

C

C

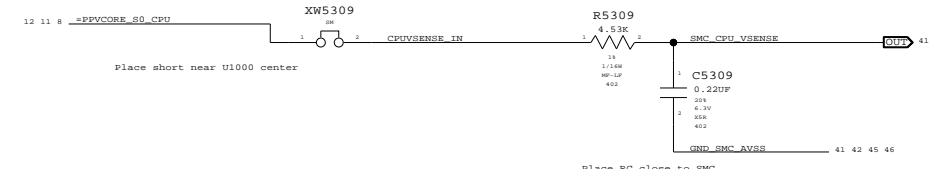
B

B

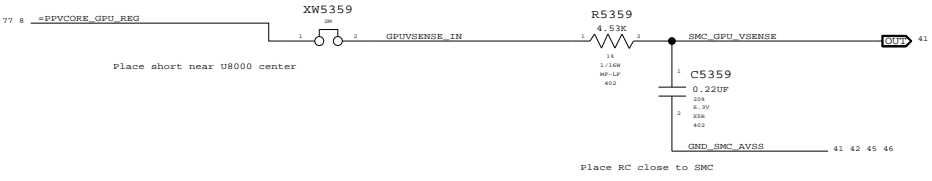
A

A

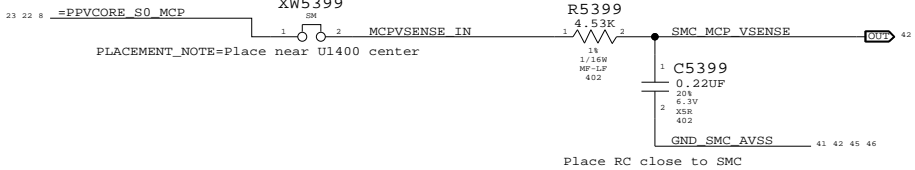
CPU Voltage Sense / Filter



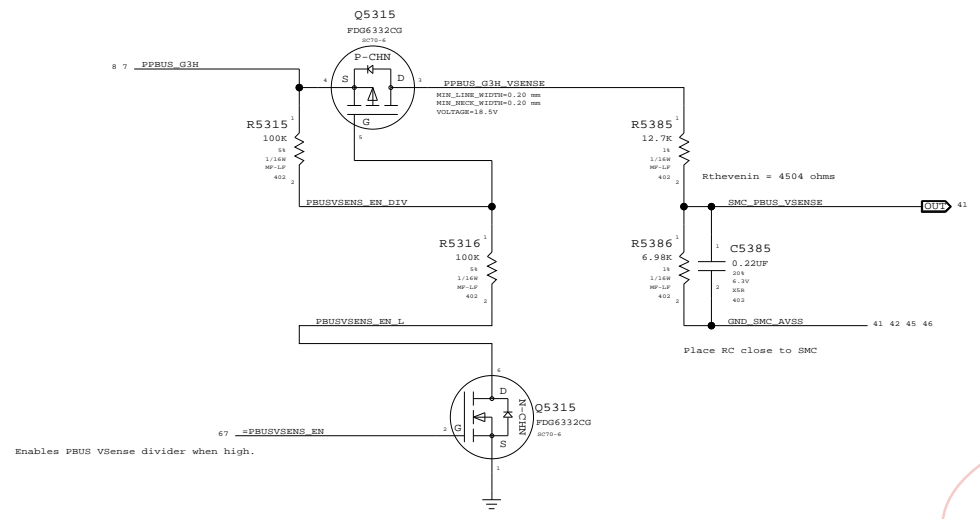
GPU Voltage Sense / Filter



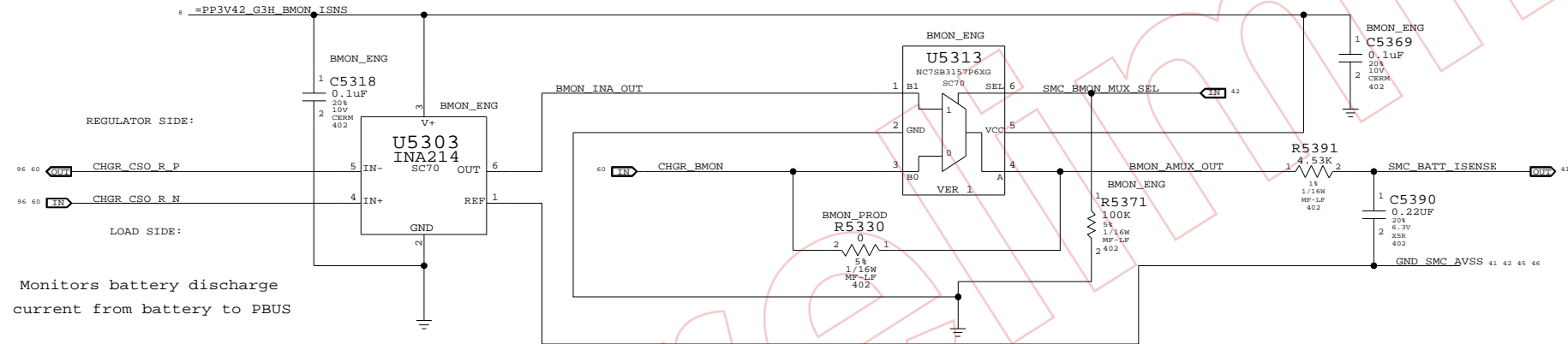
MCP Voltage Sense / Filter



PBUS Voltage Sense & Filter

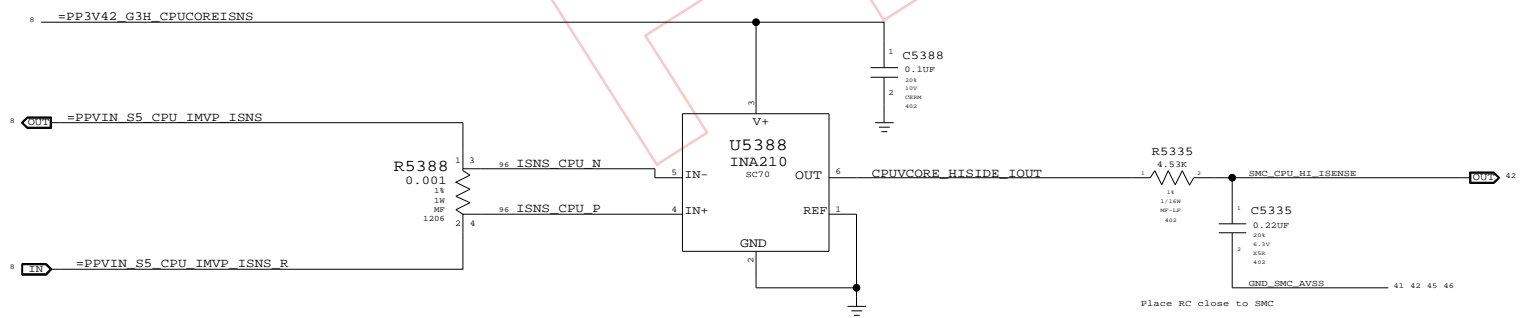


BMON Current Sense - Entire circuit must be near SMC (U4900)



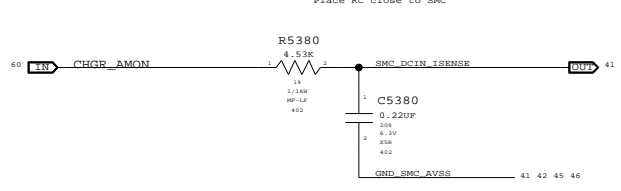
INA214 has gain of 100V/V
U5303 only senses current up to 6.6A

CPU VCore High Side Current Sensor

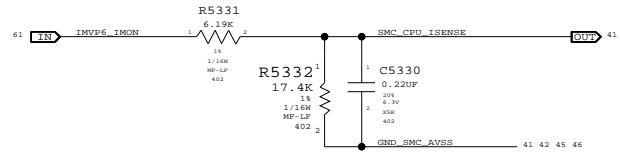


Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

DCIN Current Sense Filter

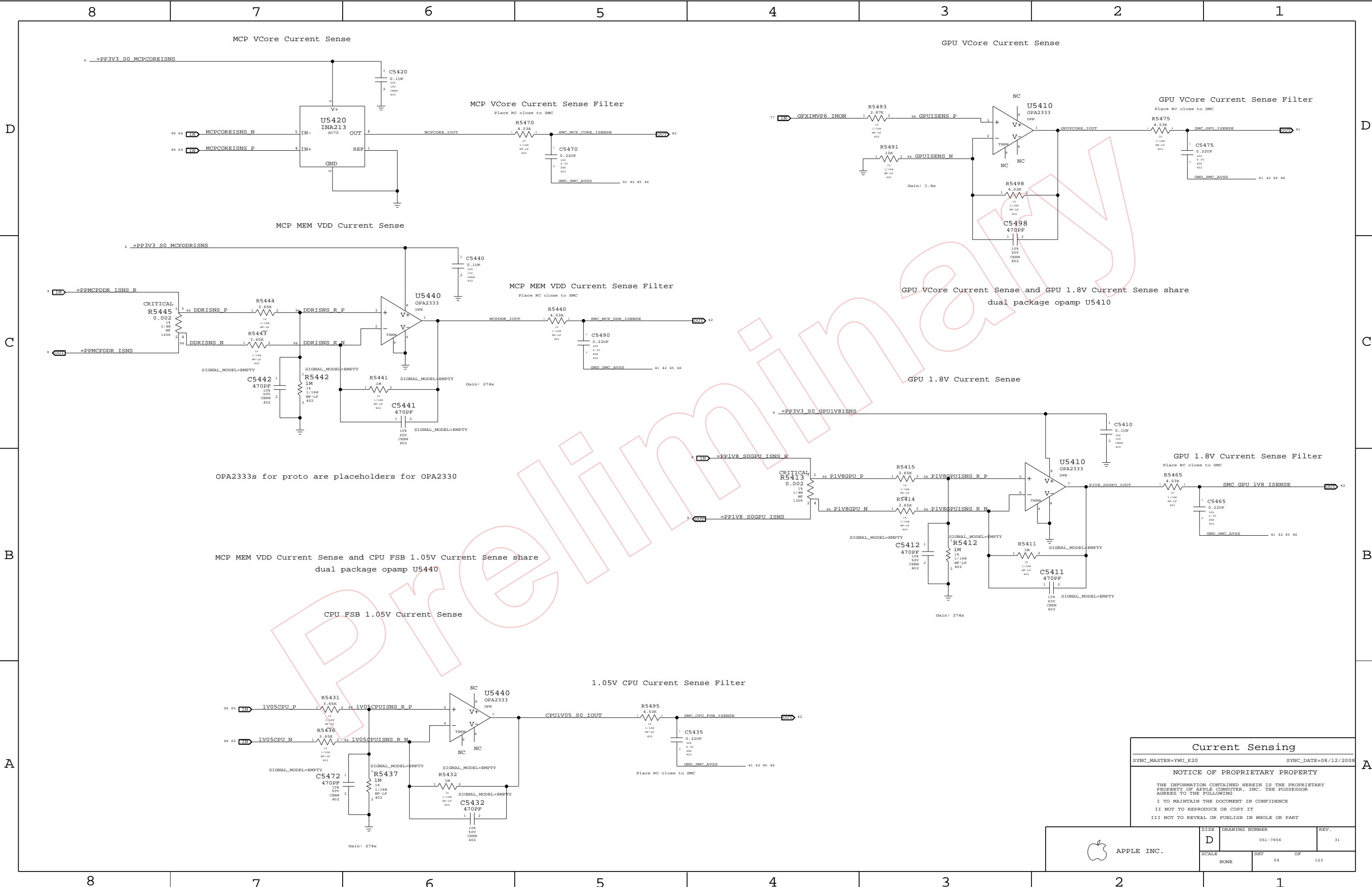


CPU VCore Load Side Current Sense / Filter



Current & Voltage Sensing
 SYNC_MASTER=YVU_K20 SYNC_DATE=08/20/2008
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SCALE	NONE	SHT	OF 123



OPA2333s for proto are placeholders for OPA2330

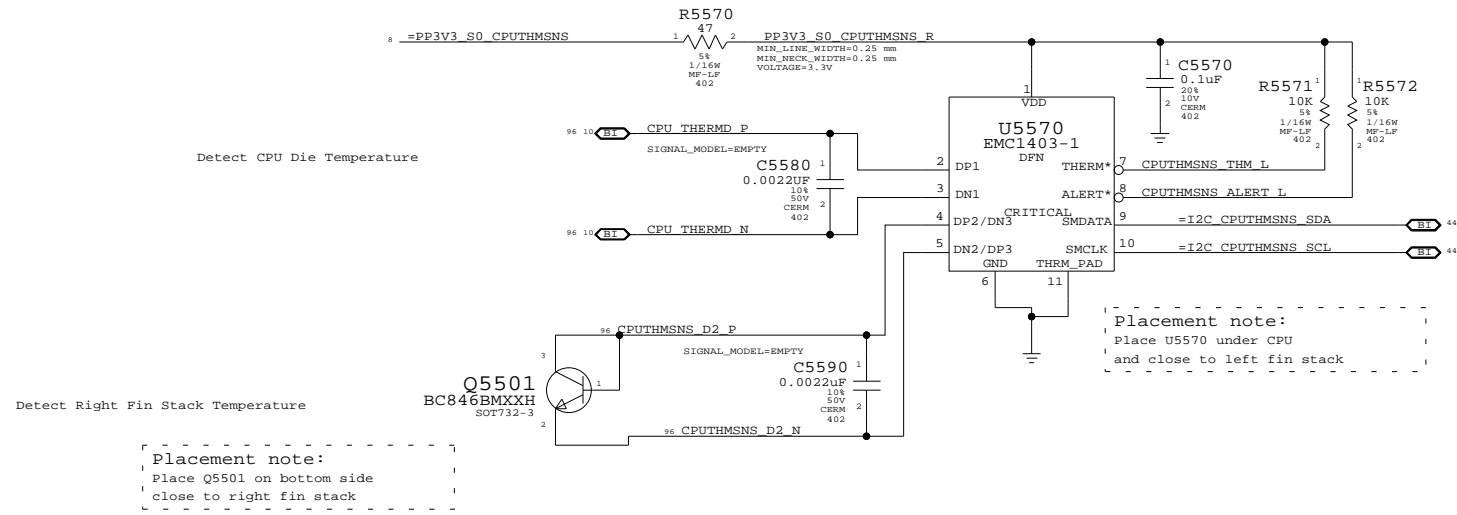
MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

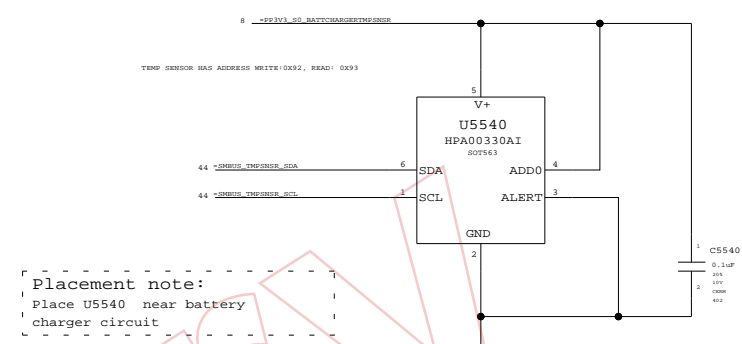
Current Sensing		
SYNC_MASTER=YWU_K20	SYNC_DATE=08/12/2008	
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	D	051-7656	31
SCALE	NONE	SHT	OF
		54	123

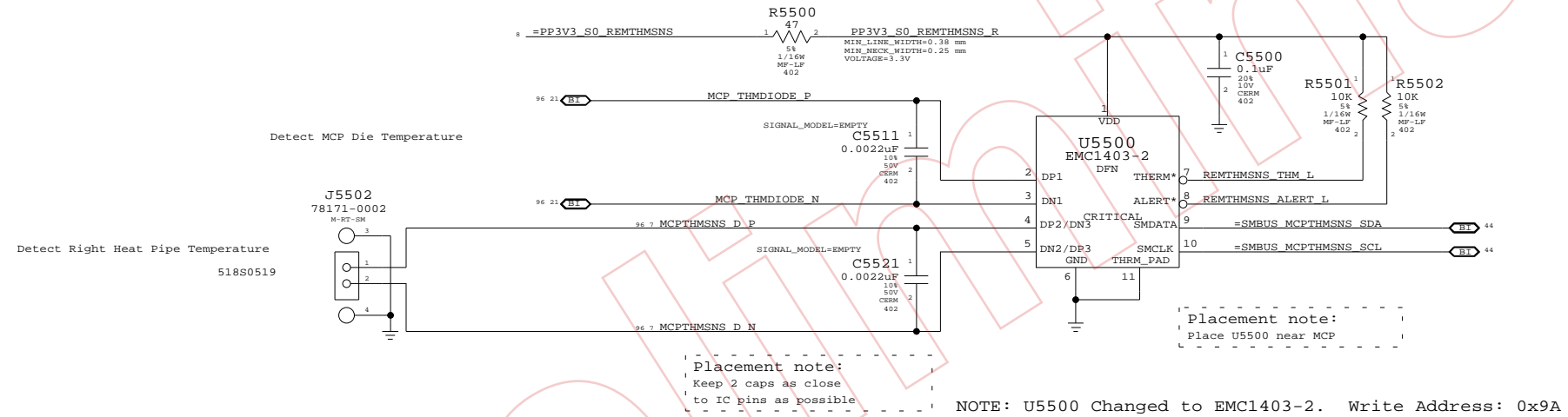
CPU Proximity/CPU Die/Right Fin Stack



Battery Charger Proximity

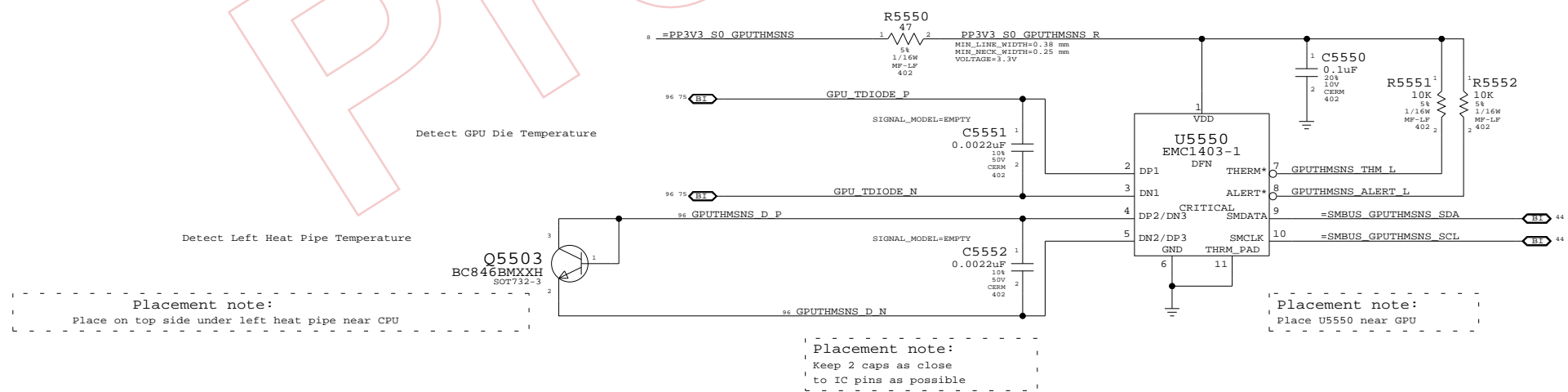


MCP Proximity/MCP Die/Right Heat Pipe



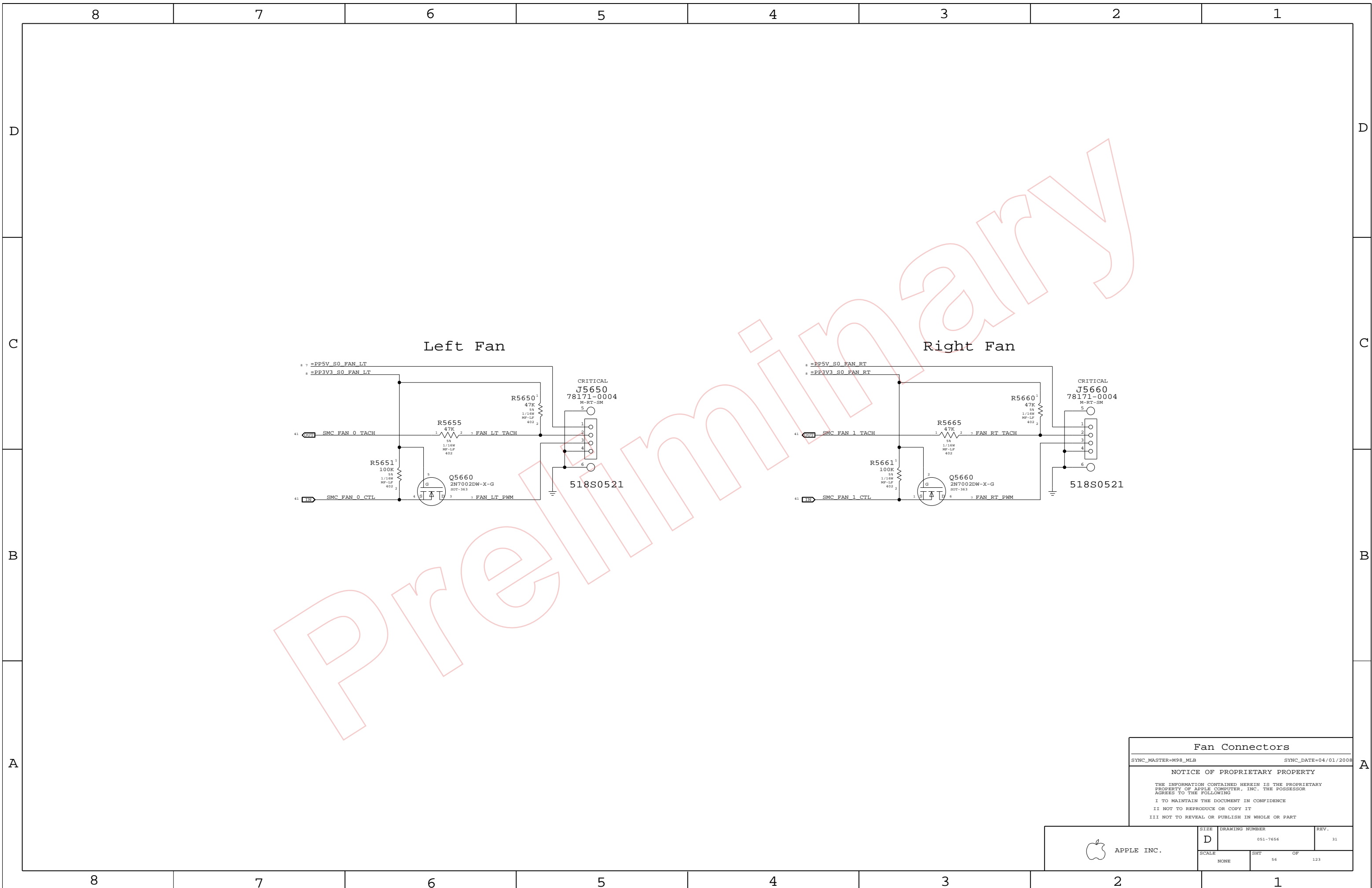
Note: EMC1403 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



Thermal Sensors		
SYNC_MASTER=YWU_K20	SYNC_DATE=05/28/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	55		



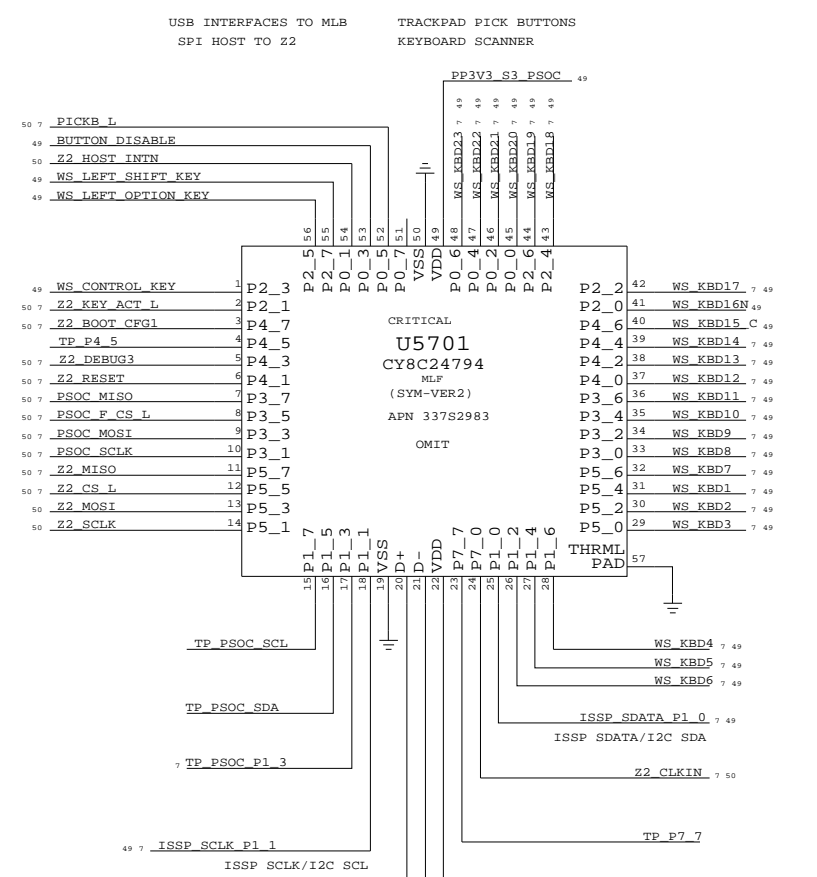
Preliminary

Fan Connectors

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008
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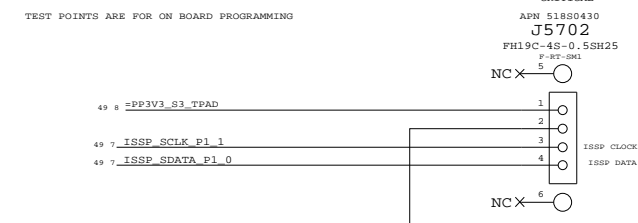
APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHEETS 56	OF 123

PSOC USB CONTROLLER

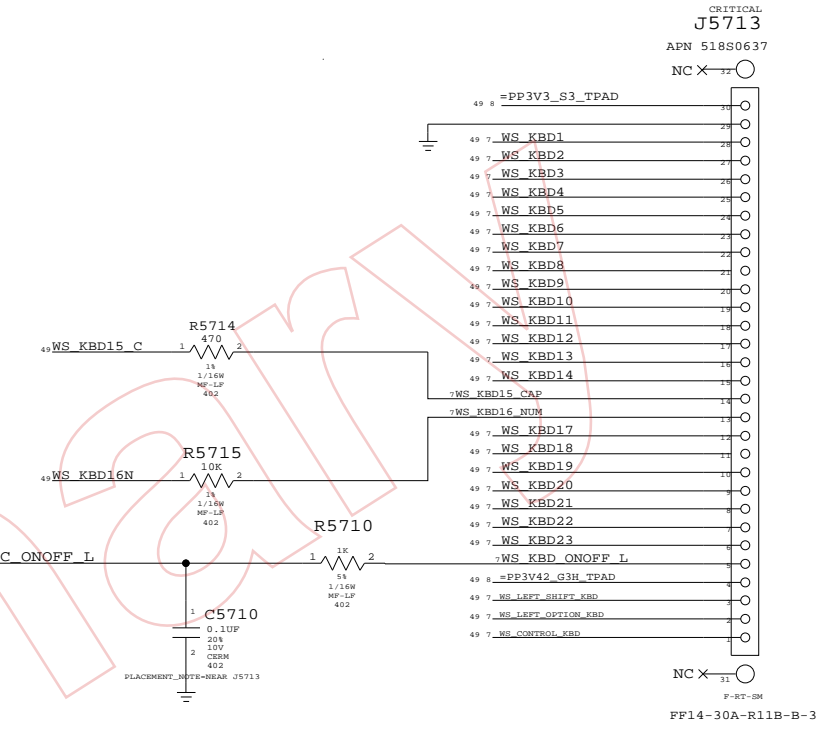


IC	PIN NAME	CURRENT	R_SMS	V_SMS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A	10 OHM	0.204 V	16.32E-6 W
PSOC	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-6 W
	VDD	8MA (TVP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
1.8V BOOSTER	VIN	48A (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

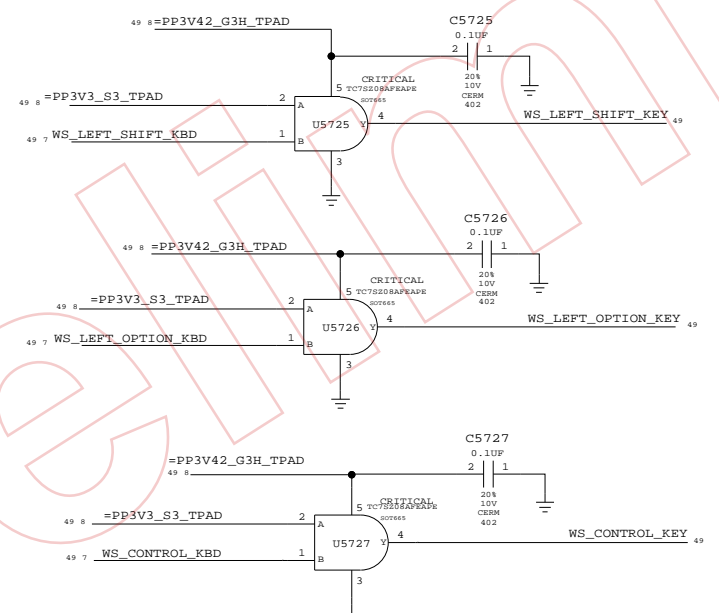
PSOC PROGRAMMING CONNECTOR



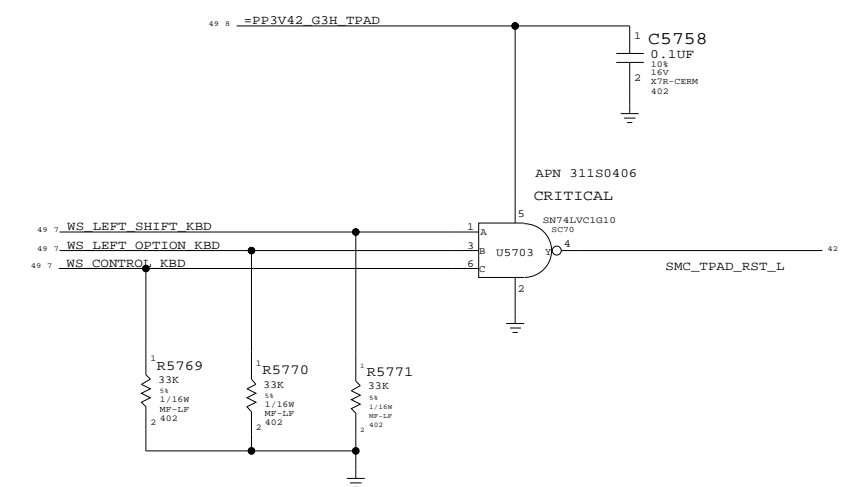
KEYBOARD CONNECTOR



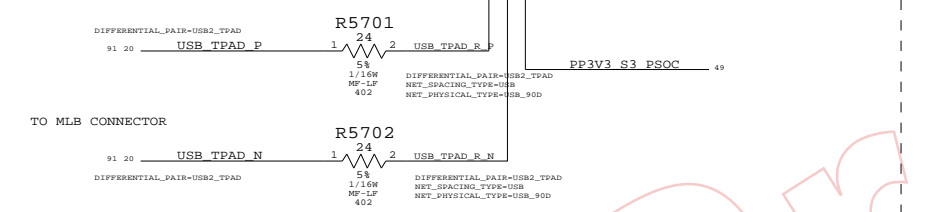
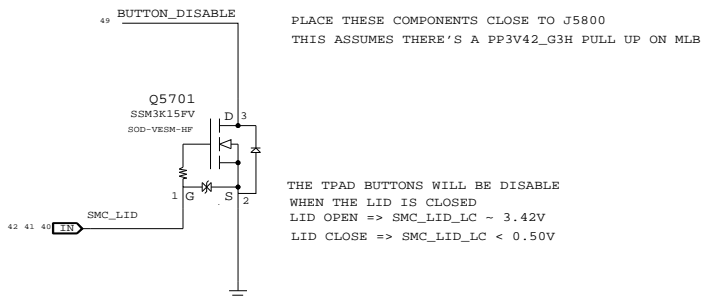
ISOLATION CIRCUIT



SMC_MANUAL_RESET LOGIC



TPAD BUTTONS DISABLE



WELLSPRING 1

SYNC_MASTER=YMA_K20 SYNC_DATE=05/19/2008

NOTICE OF PROPRIETARY PROPERTY

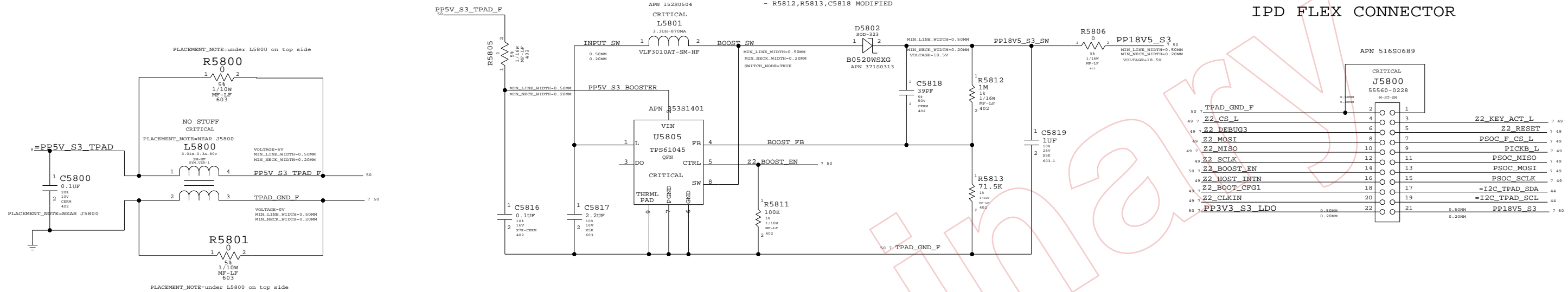
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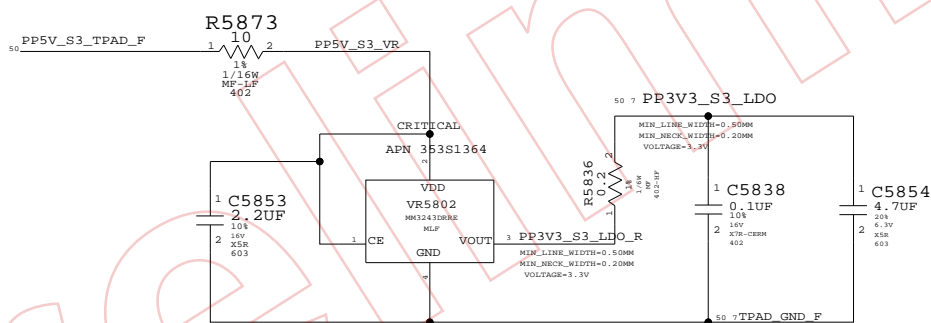
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	NONE	SHT	OF 123
		57	

BOOSTER +18.5VDC FOR SENSORS

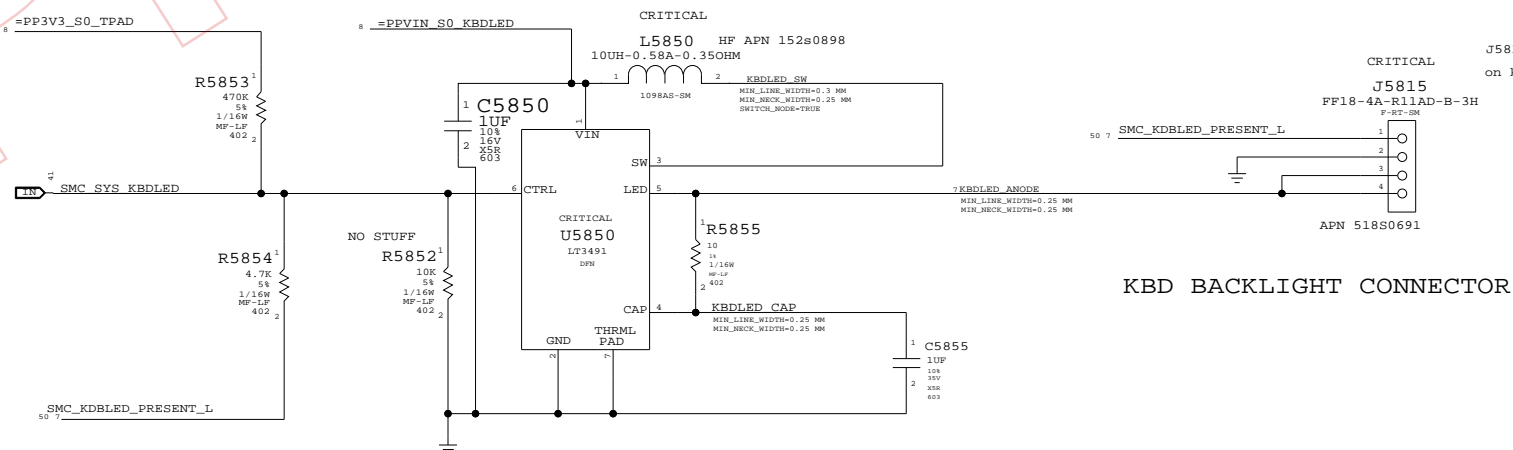
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812, R5813, C5818 MODIFIED



3V3 LDO FOR IPD



Keyboard LED Driver



To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
 LOW = keyboard backlight present
 HIGH= keyboard backlight not present
 BOM OPTION: KBDLED_YES
 R5853 ALWAYS PRESENT

J5815 pin 1 is grounded on keyboard backlight flex

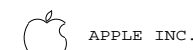
KBD BACKLIGHT CONNECTOR

WELLSPRING 2

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	58	123

8

7

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5

4

3

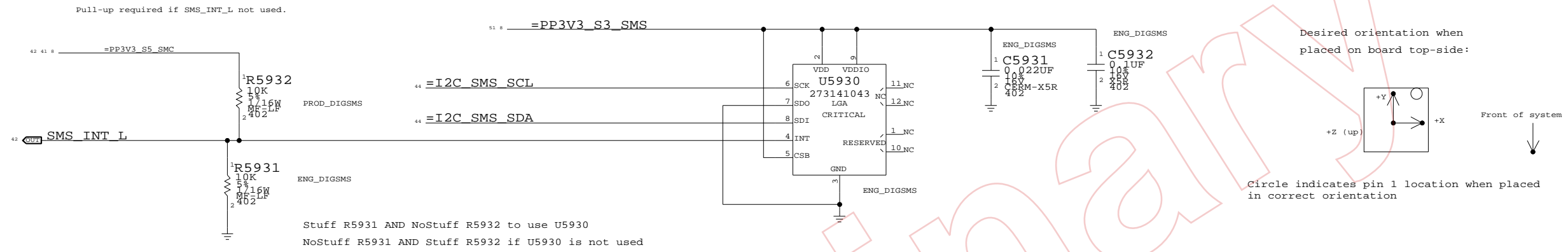
2

1

D

D

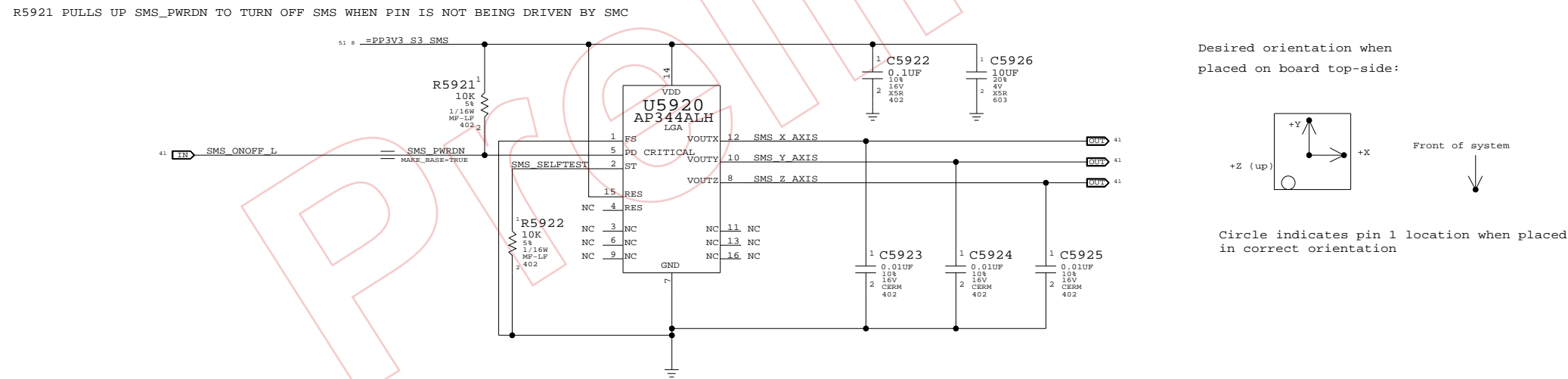
Digital SMS



C

C

Analog SMS



B

B

A

A

Sudden Motion Sensor (SMS)

SYNC_MASTER=YWU_K20 SYNC_DATE=06/17/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT		OF
NONE	59		123

8

7

6

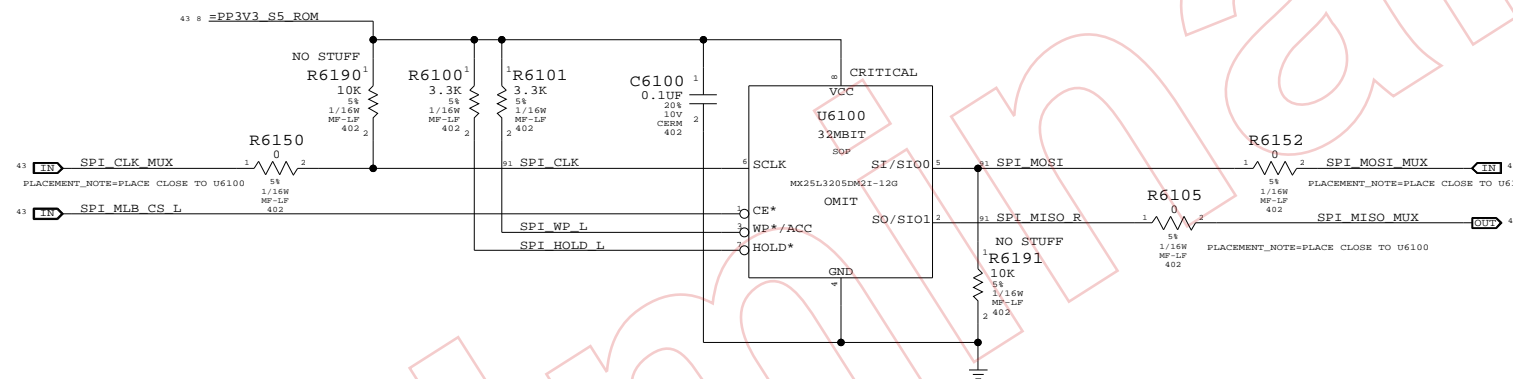
5

4

3

2

1



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
 Any of the 4 frequencies can be selected
 with R6190, R6191, R5190 and R5191

SPI ROM

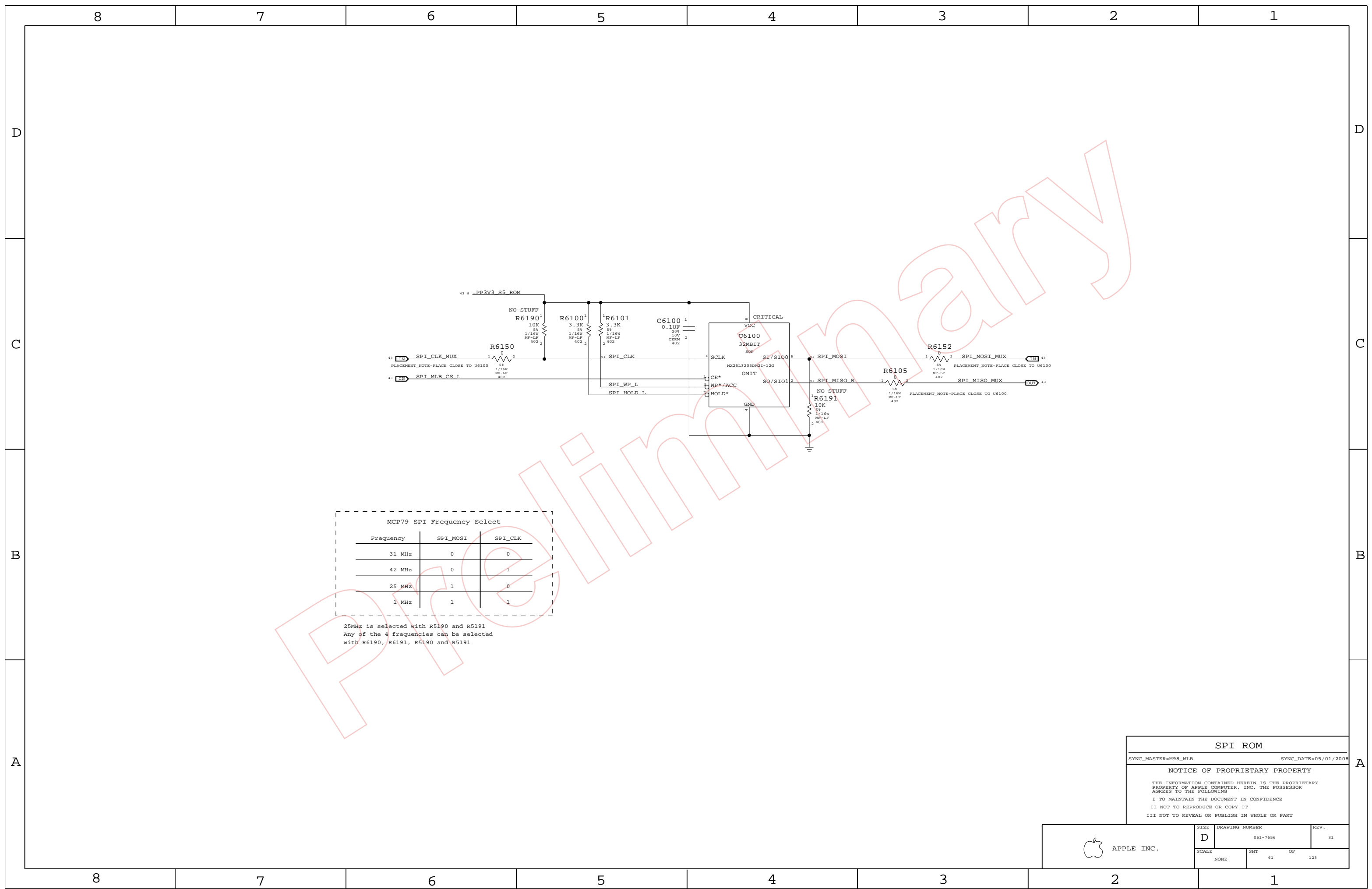
SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008

NOTICE OF PROPRIETARY PROPERTY

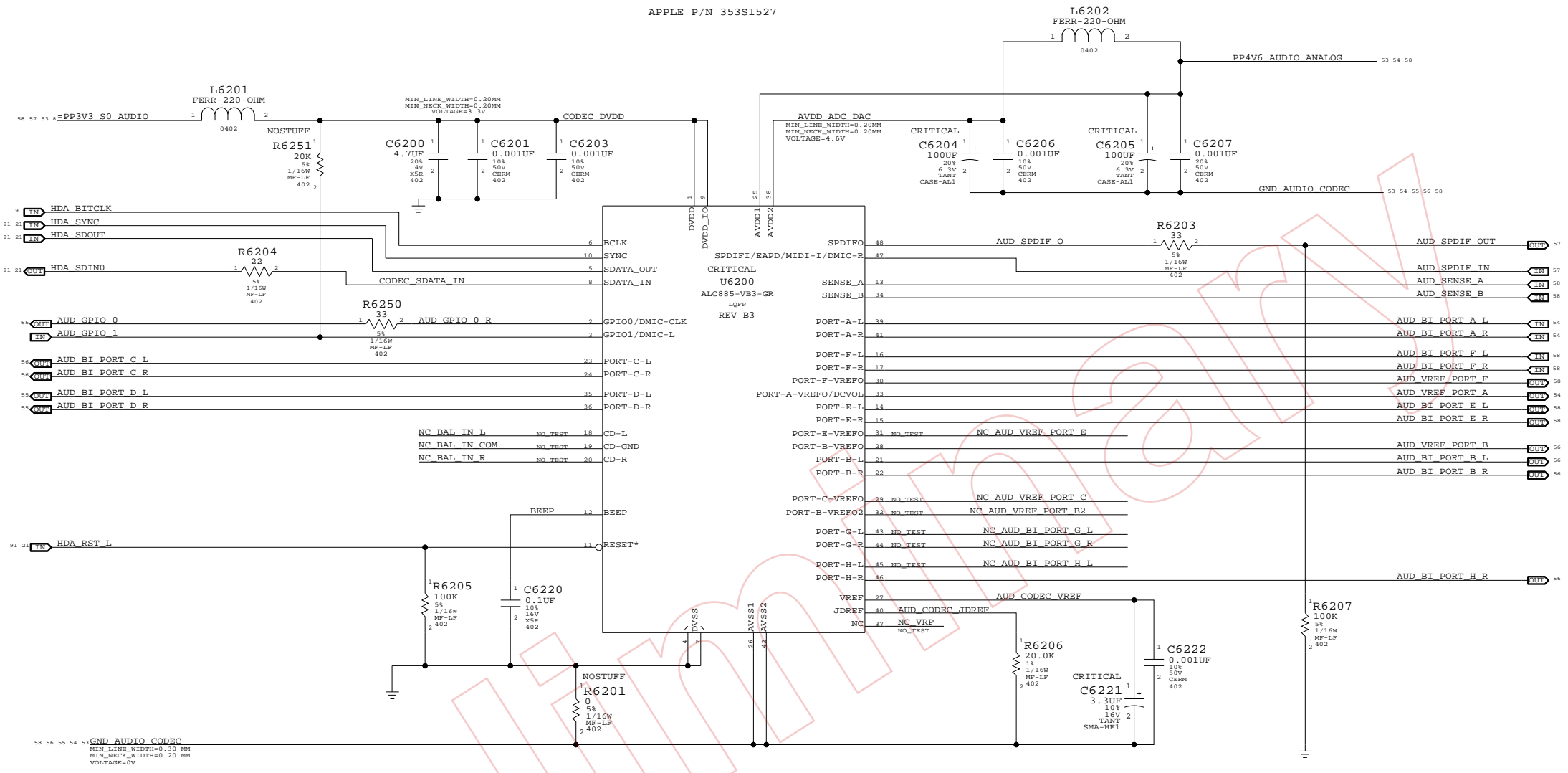
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	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT OF		
NONE	61 OF 123		

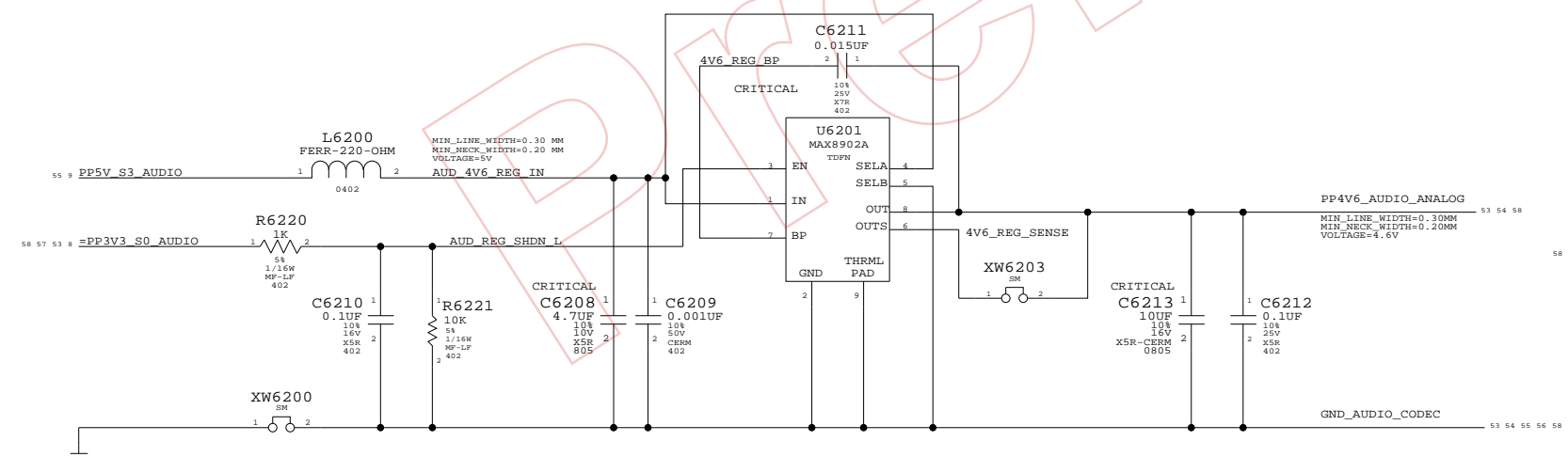


AUDIO CODEC
APPLE P/N 353S1527



AUDIO 4.6 V REGULATOR
APPLE P/N 353S1897

MIKEY 3.3 V REGULATOR
APPLE P/N 353S1860



AUDIO: CODEC
 SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	62		

8

7

6

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2

1

D

D

C

C

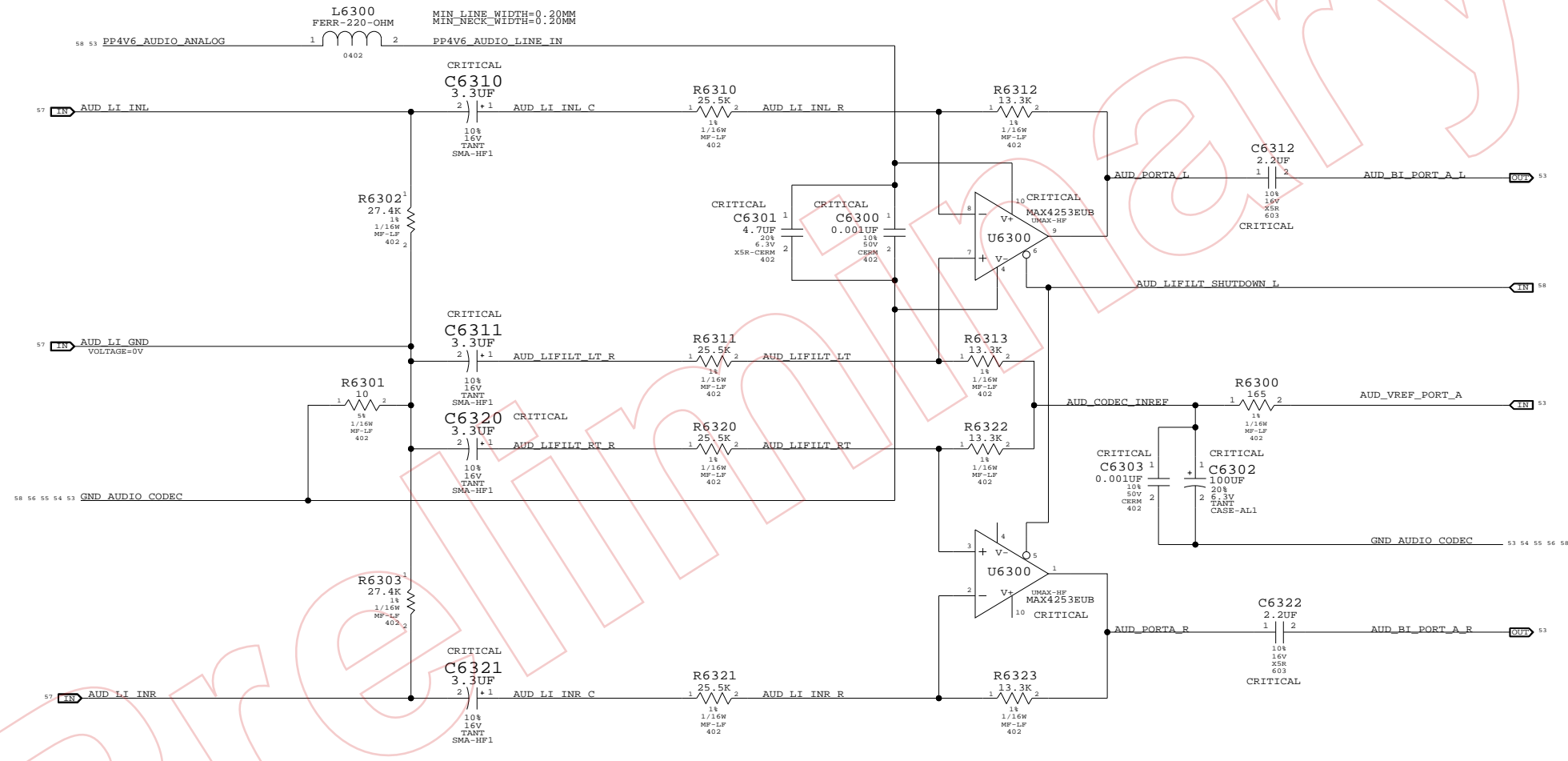
B

B

A

A

Pseudo-Diff Line-In Filter
 GAIN = -5.4 DB AV = 0.52
 FC = 1.89 HZ



AUDIO: LINE IN
 SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT OF		
NONE	63 OF		123

8

7

6

5

4

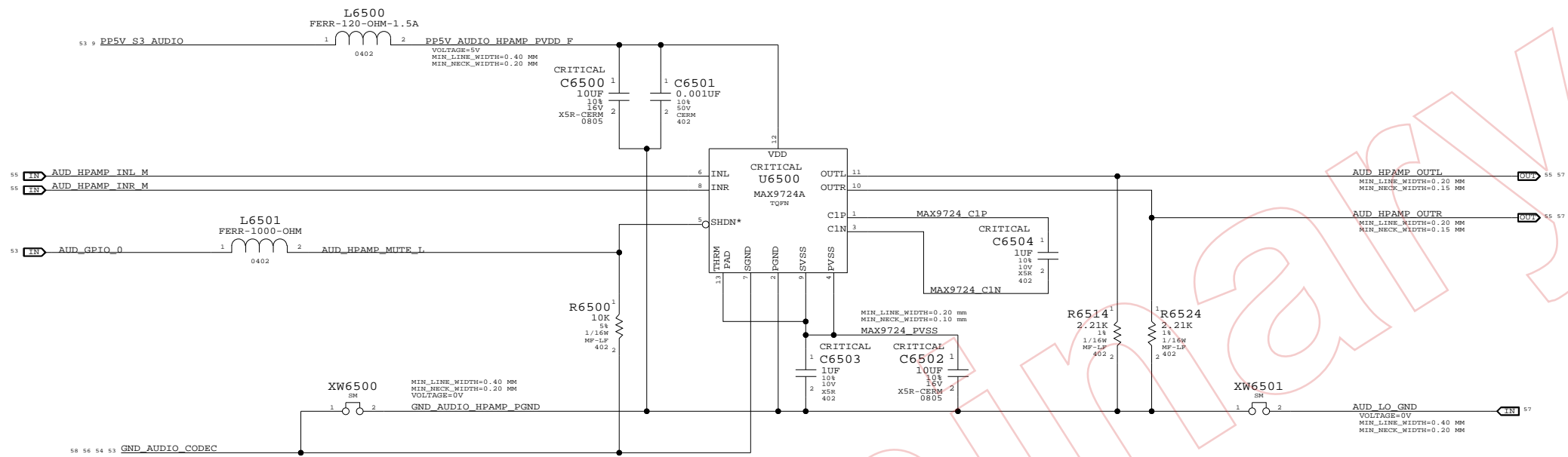
3

2

1

Headphone Amplifier (MAX9724A)

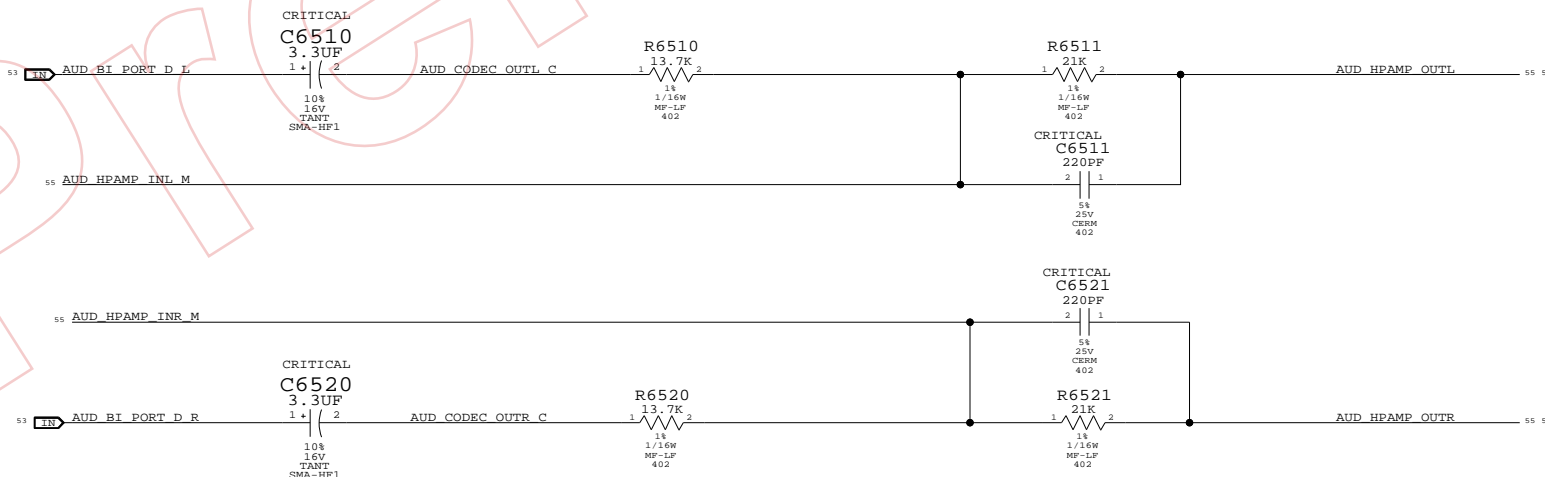
APN:353S1637



1st Order DAC Filter

HP:3.52 HZ LP:34 KHZ

VOLTAGE GAIN:1.53



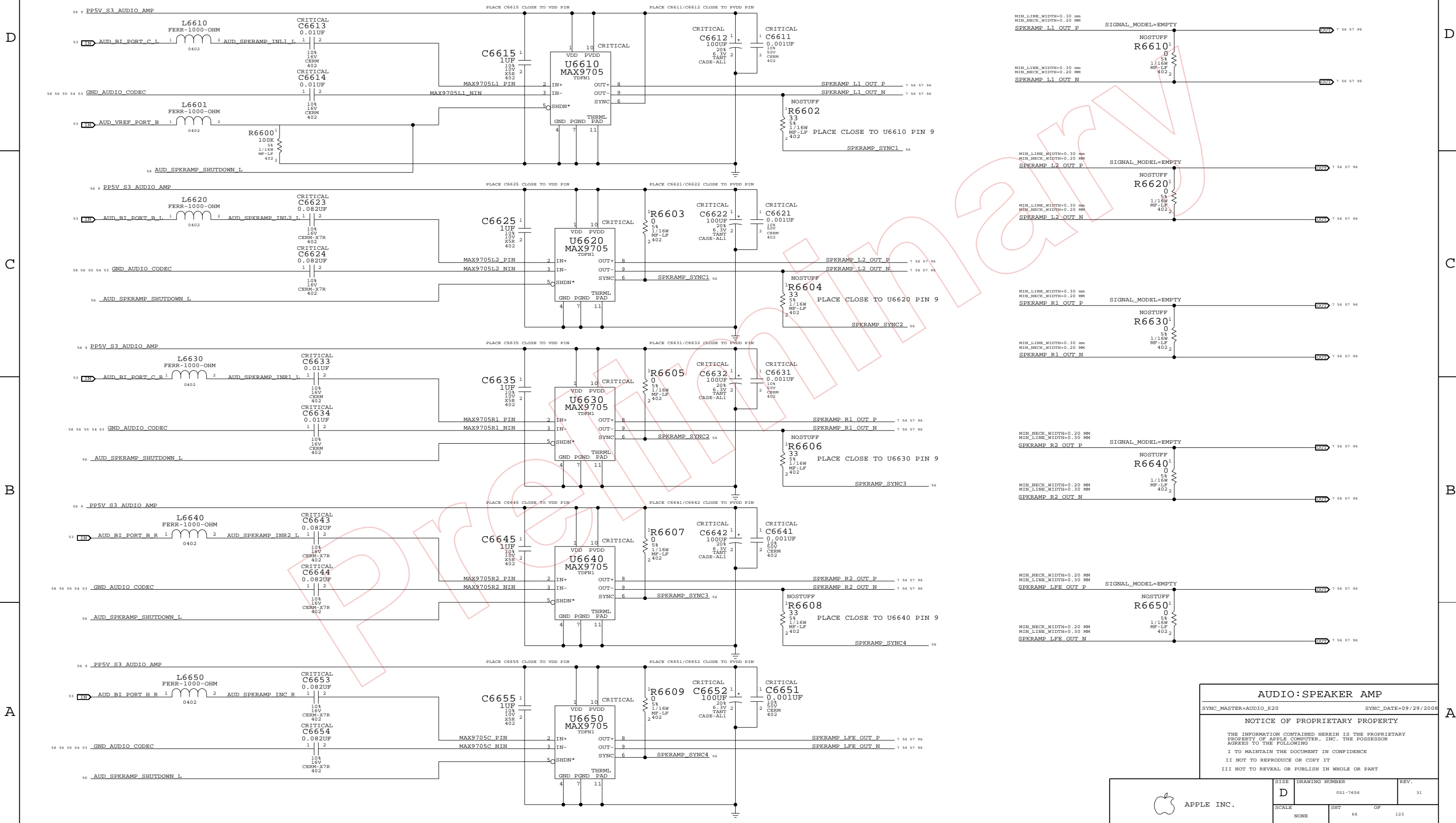
AUDIO: HEADPHONE AMP
 SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHEET 65	OF 123

4X MONO SPEAKER AMPLIFIERS (MAX9705)
 APN: 353S1595
 GAIN = 12 DB
 FC (SPEAKERS L1/R1) = ~796 HZ
 FC (SPEAKERS L2/R2/LFE) = ~97 HZ

SPEAKER CHECKPOINTS



AUDIO: SPEAKER AMP
 SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	66		

AUDIO JACK 1 LO/HP JACK, SPDIF TX

MIC CONNECTOR
APN: 518S0520

SPEAKER CONNECTORS
APN: 518S0521

APN: 518S0672

AUDIO JACK 2 LINE IN JACK, SPDIF RX

AUDIO: JACKS

SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008

NOTICE OF PROPRIETARY PROPERTY

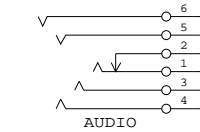
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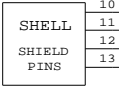
SCALE	DRAWING NUMBER	REV.
NONE	051-7656	31
SHT	OF	123
67		

APN: 514-0632

CRITICAL
J6700
SPDIF-TX-K20
F-RT-TH

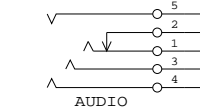


A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF

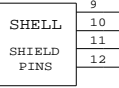


APN: 514-0633

CRITICAL
J6750
SPDIF-RX-K20
F-RT-TH



A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF



RETURN FOR HF NOISE



GND CHASSIS AUDIO JACK

GND CHASSIS AUDIO JACK

GND CHASSIS AUDIO JACK

D

C

B

A

D

C

B

A

8

7

6

5

4

3

2

1

8

7

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3

2

1

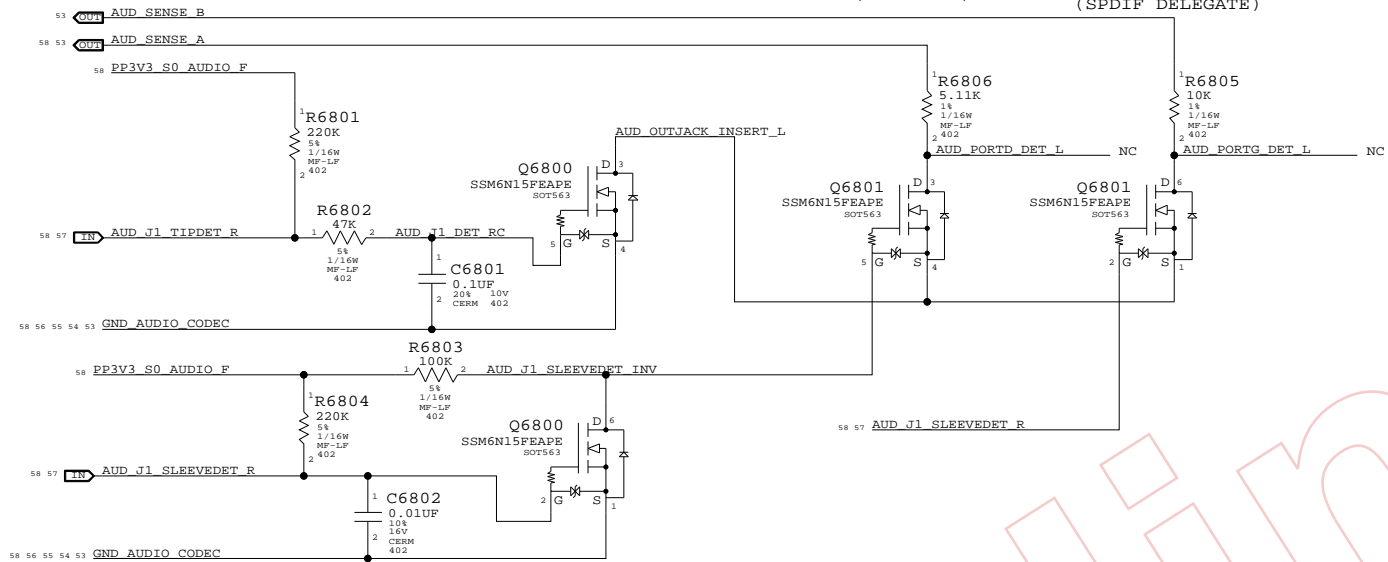
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	OX0C (12)	OX02 (2)	OX0C (12)	OX14 (20,D)	GPIO_0	OX14 (20,D)
SPEAKERS L1/R1	OX0F (15)	OX05 (5)	OX0F (15)	OX1A (26,C)	VREF_B (100%)	N/A
SPEAKERS L2/R2	OX0D (13)	OX03 (3)	OX0D (13)	OX18 (24,B)	VREF_B (100%)	N/A
SPEAKER LFE	OX0E (14)	OX04 (4)	OX0E (14)	OX17 (23,H)	VREF_B (100%)	N/A
SPDIF OUT	N/A	OX06 (6)	N/A	OX1E (SPDIF OUT)	N/A	OX16 (22,G)

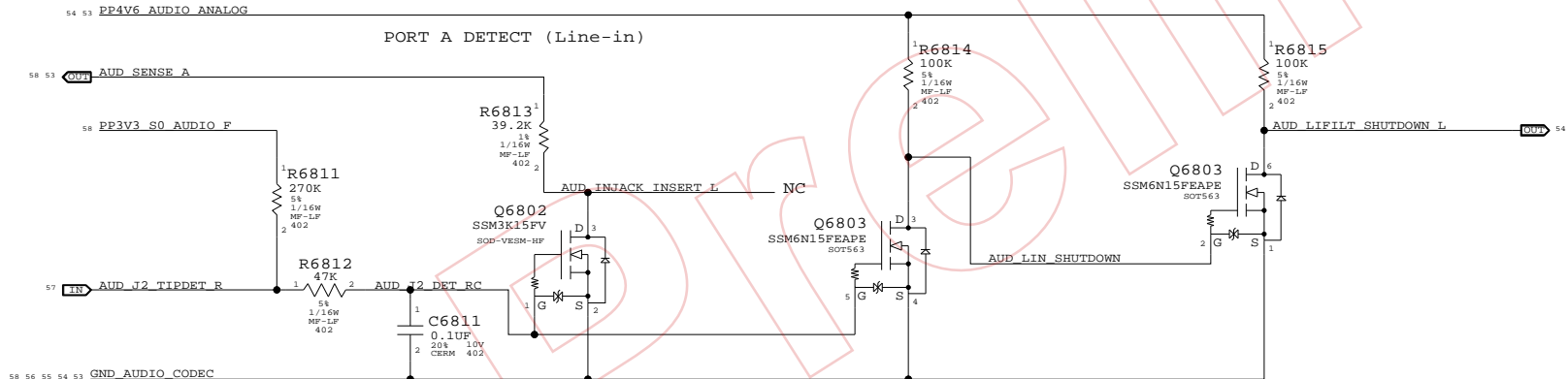
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	OX23 (35)	OX08 (8)	OX15 (21,A)	VREF_A (50%)	OX15 (21,A)
SPDIF IN	N/A	OX0A (10)	OX1F (SPDIF IN)	N/A	N/A
MIC	OX24 (36)	OX07 (7)	OX19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	OX24 (36)	OX07 (7)	OX1B (27,E)	MIKEY	MIKEY

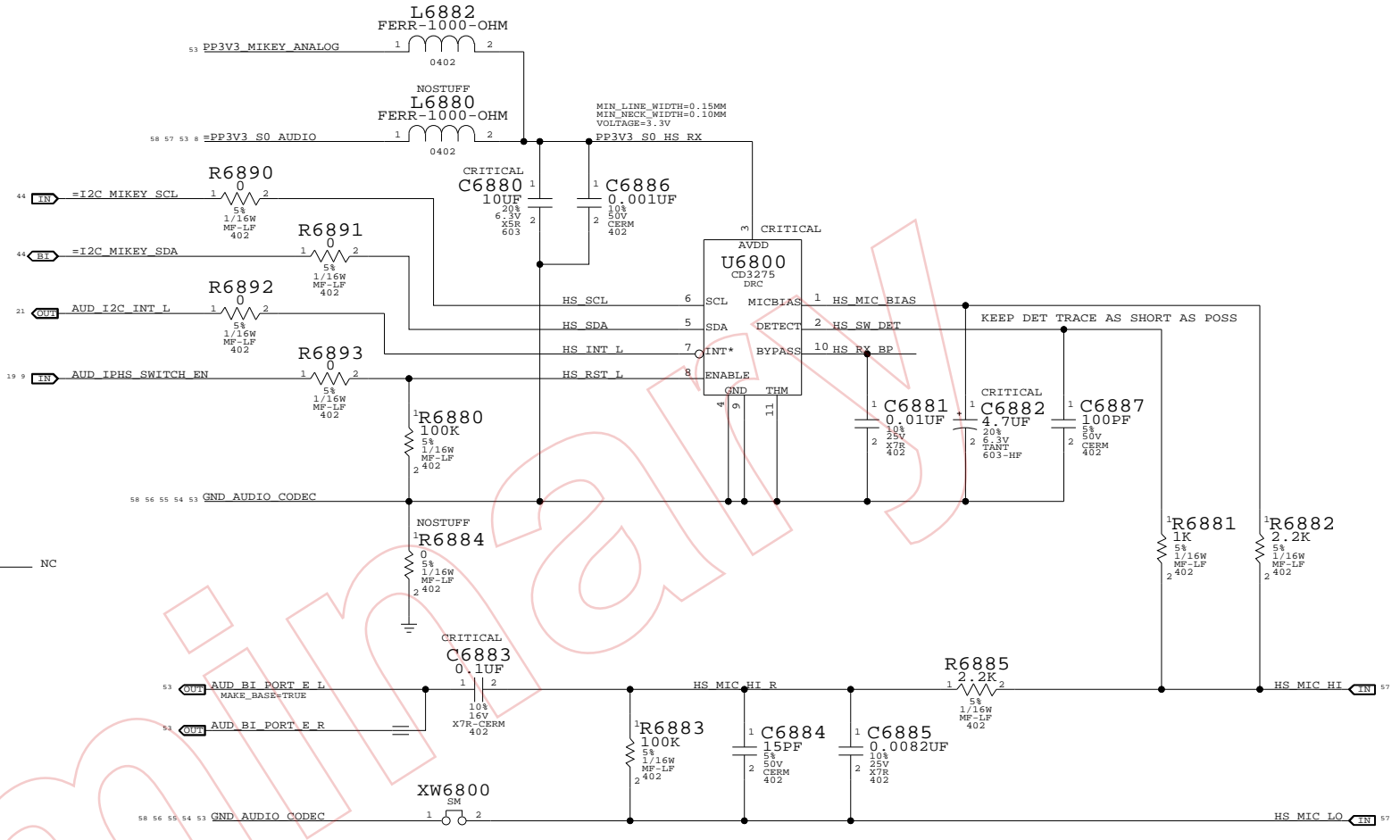
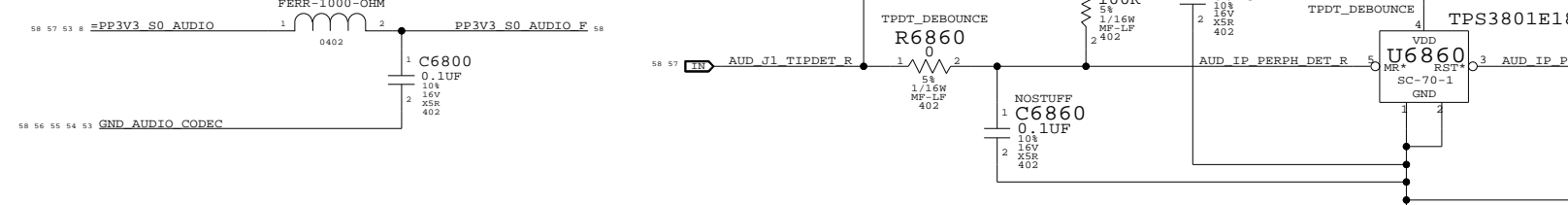
PORT D DETECT (Line-out) PORT G DETECT (SPDIF DELEGATE)



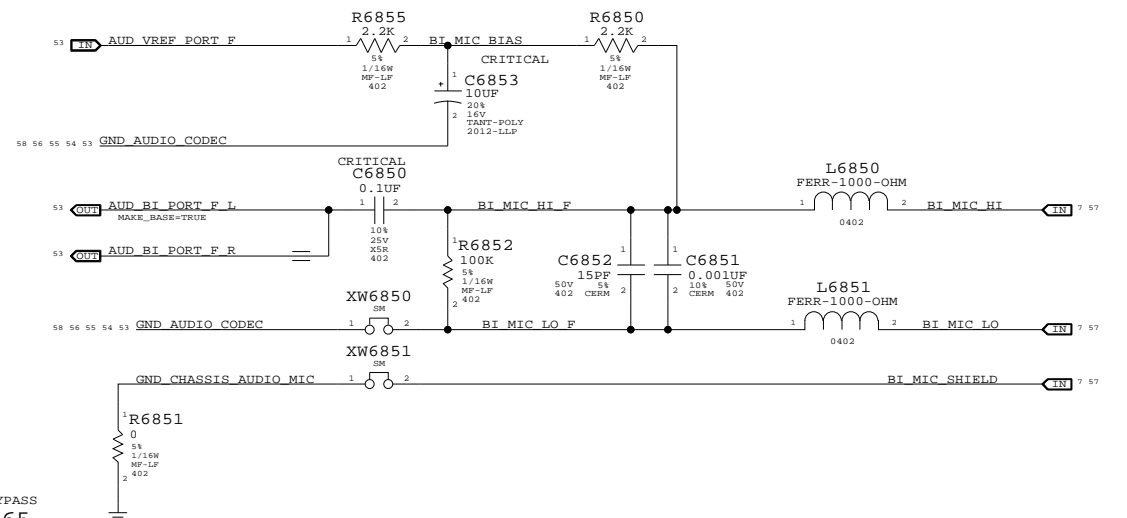
LINE_IN AMP SHUTDOWN CONTROL



PLACE L6800/C6800 CLOSE TO Q6800/01/02
L6800
FERR-1000-OHM

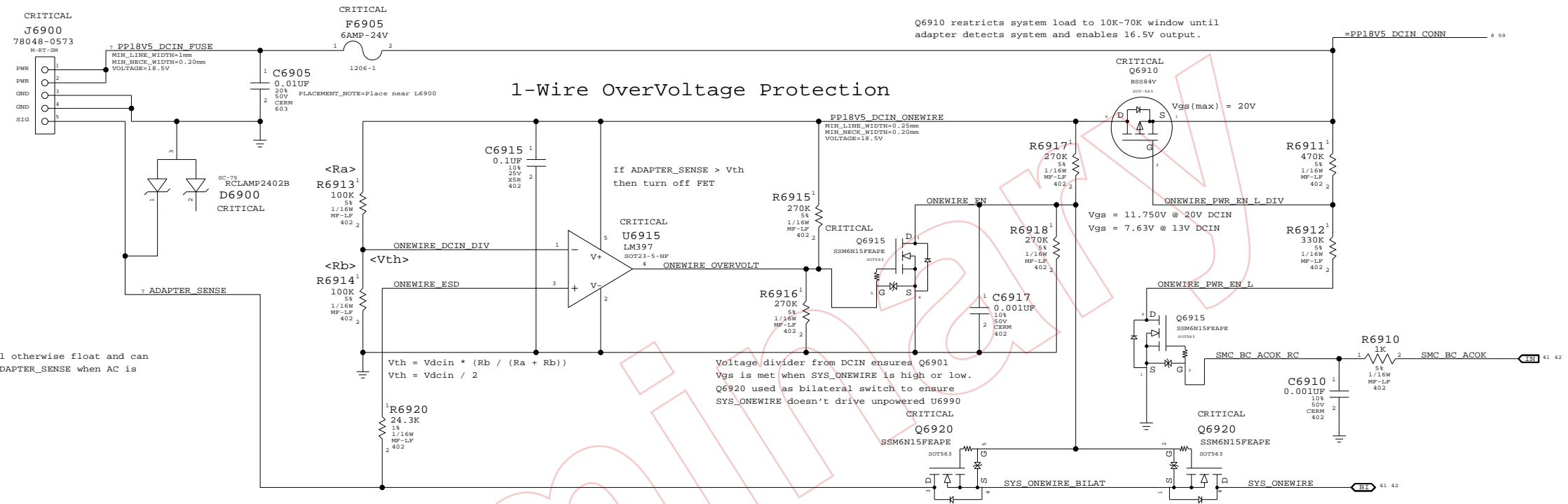


PORT F (BUILT-IN MIC)



AUDIO: JACK TRANSLATORS
 SYNC_MASTER=AUDIO_K20 SYNC_DATE=09/29/2008
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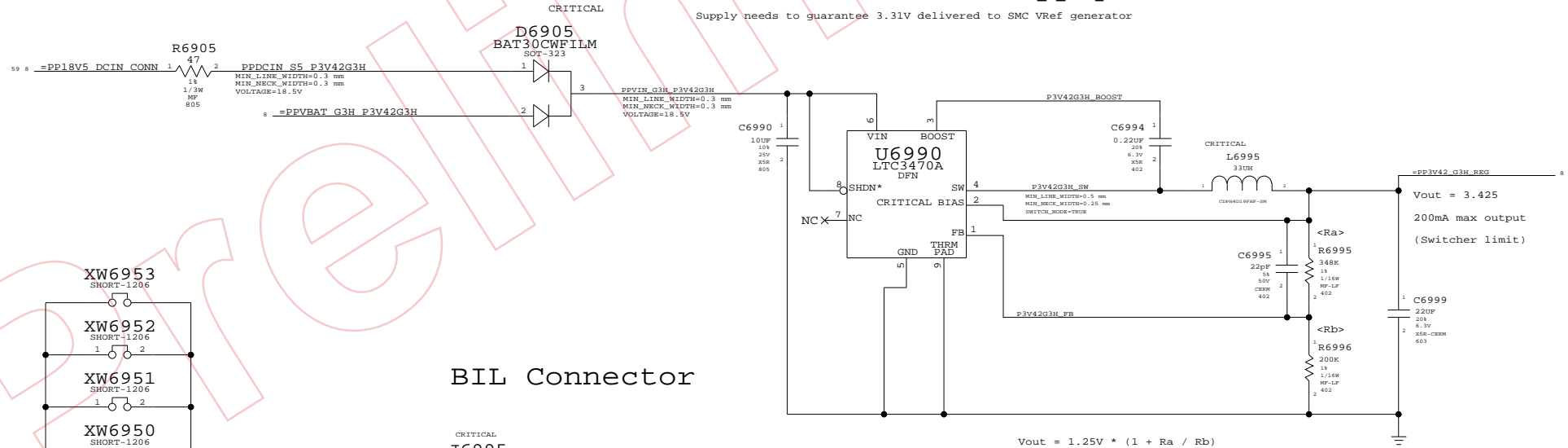
MagSafe DC Power Jack



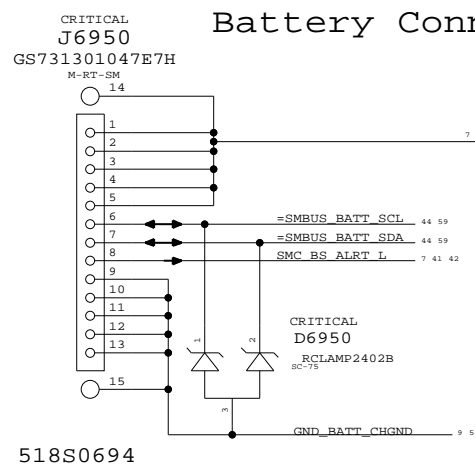
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

3.425V "G3Hot" Supply

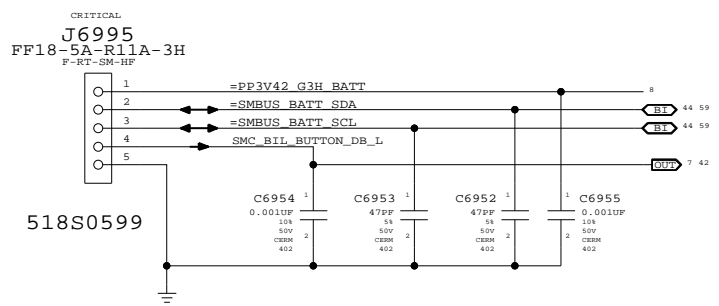
Supply needs to guarantee 3.31V delivered to SMC VREF generator



Battery Connector

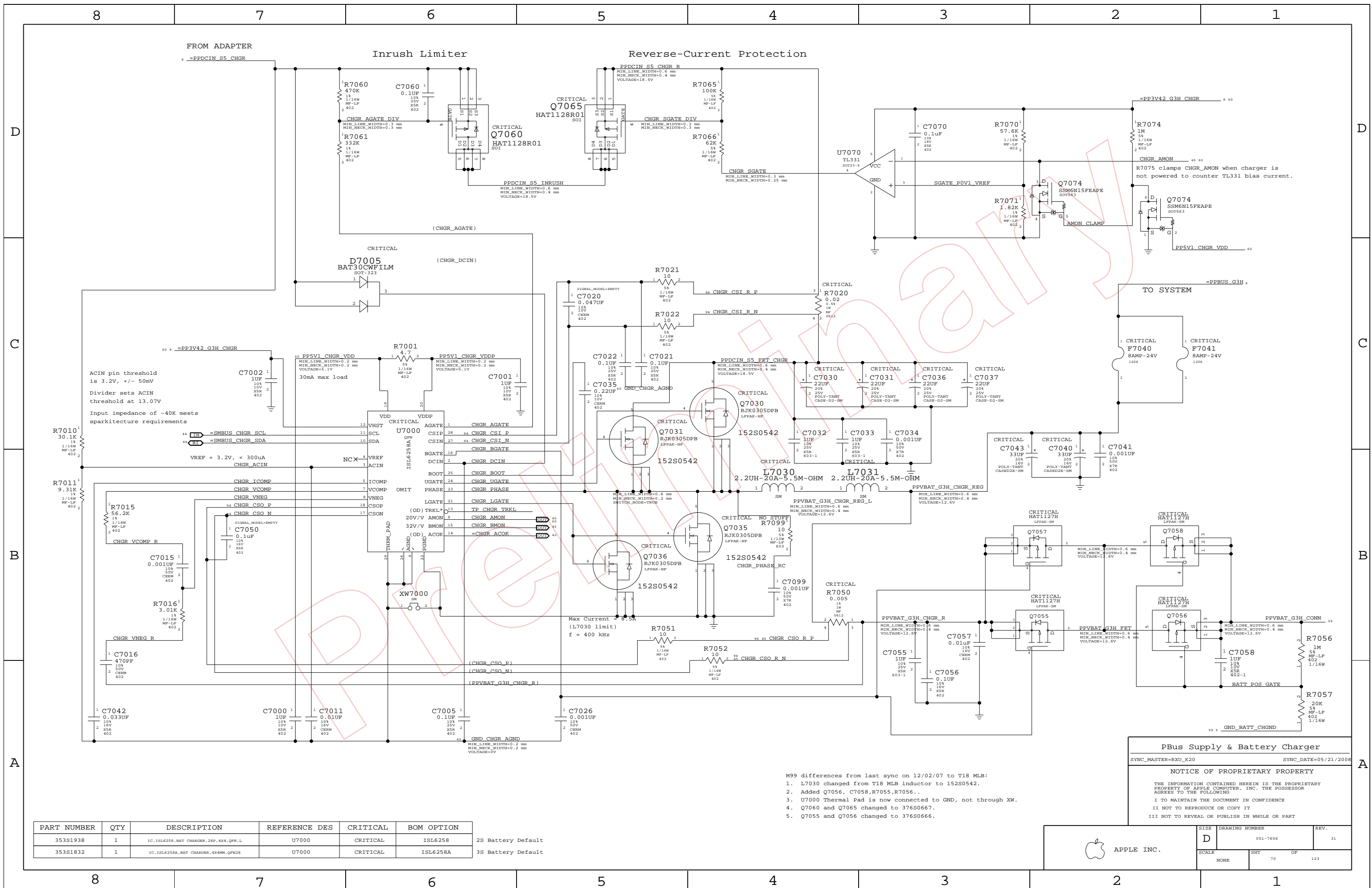


BIL Connector



DC-In & Battery Connectors
 SYNC_MASTER=RKU_K20 SYNC_DATE=05/21/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	NONE	SHT	OF 123
		69	



8 7 6 5 4 3 2 1

D
C
B
A

D
C
B
A

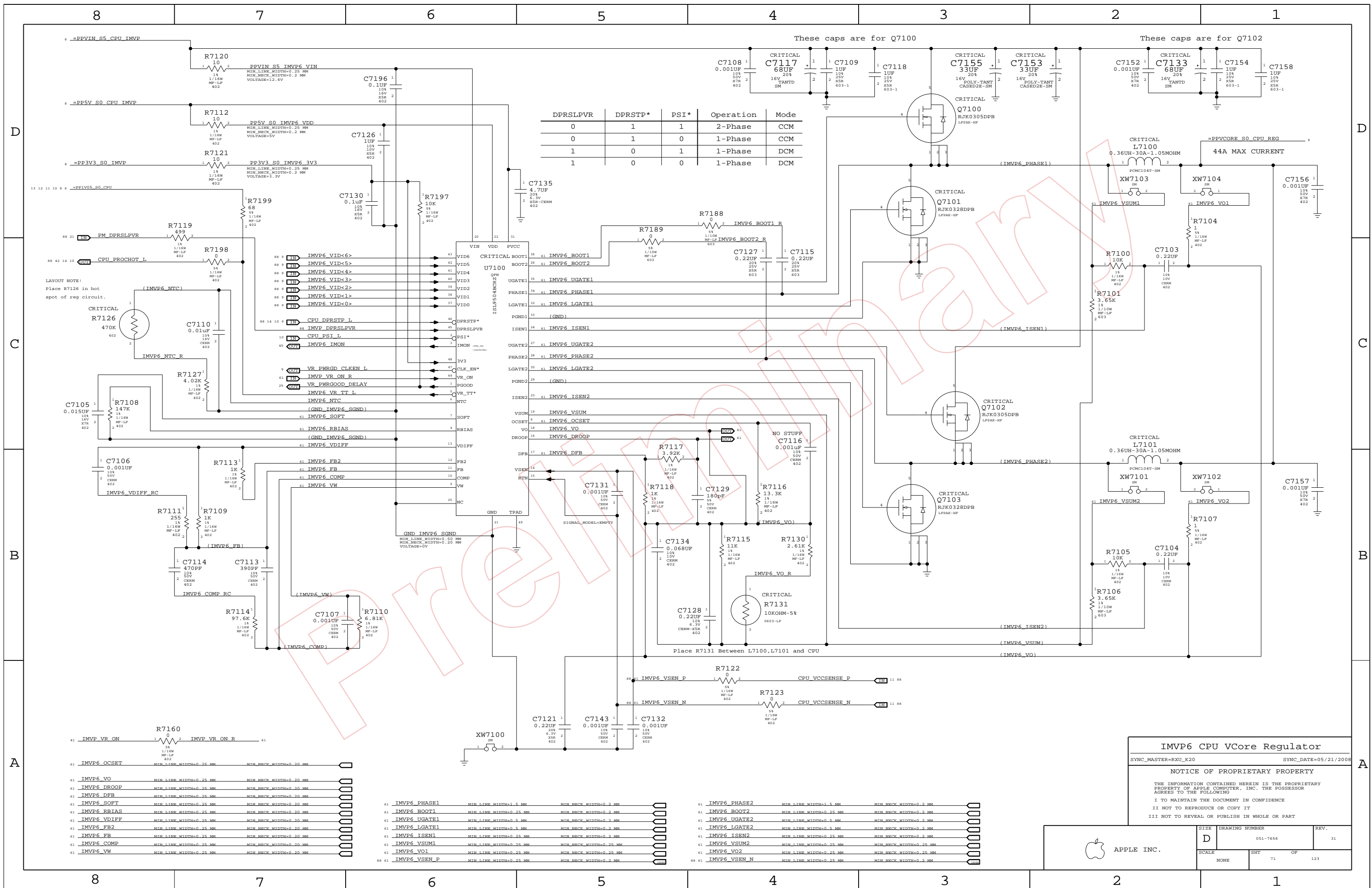
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1938	1	IC, ISL6258, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	ISL6258 2S Battery Default
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	ISL6258A 3S Battery Default

- M99 differences from last sync on 12/02/07 to T18 MLB:
- L7030 changed from T18 MLB inductor to 152S0542.
 - Added Q7056, C7058, R7055, R7056..
 - U7000 Thermal Pad is now connected to GND, not through XW.
 - Q7060 and Q7065 changed to 376S0667.
 - Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger
 SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008
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APPLE INC.	SIZE	D	DRAWING NUMBER	051-7656	REV.	31
	SCALE	NONE	SHT	70	OF	123

8 7 6 5 4 3 2 1



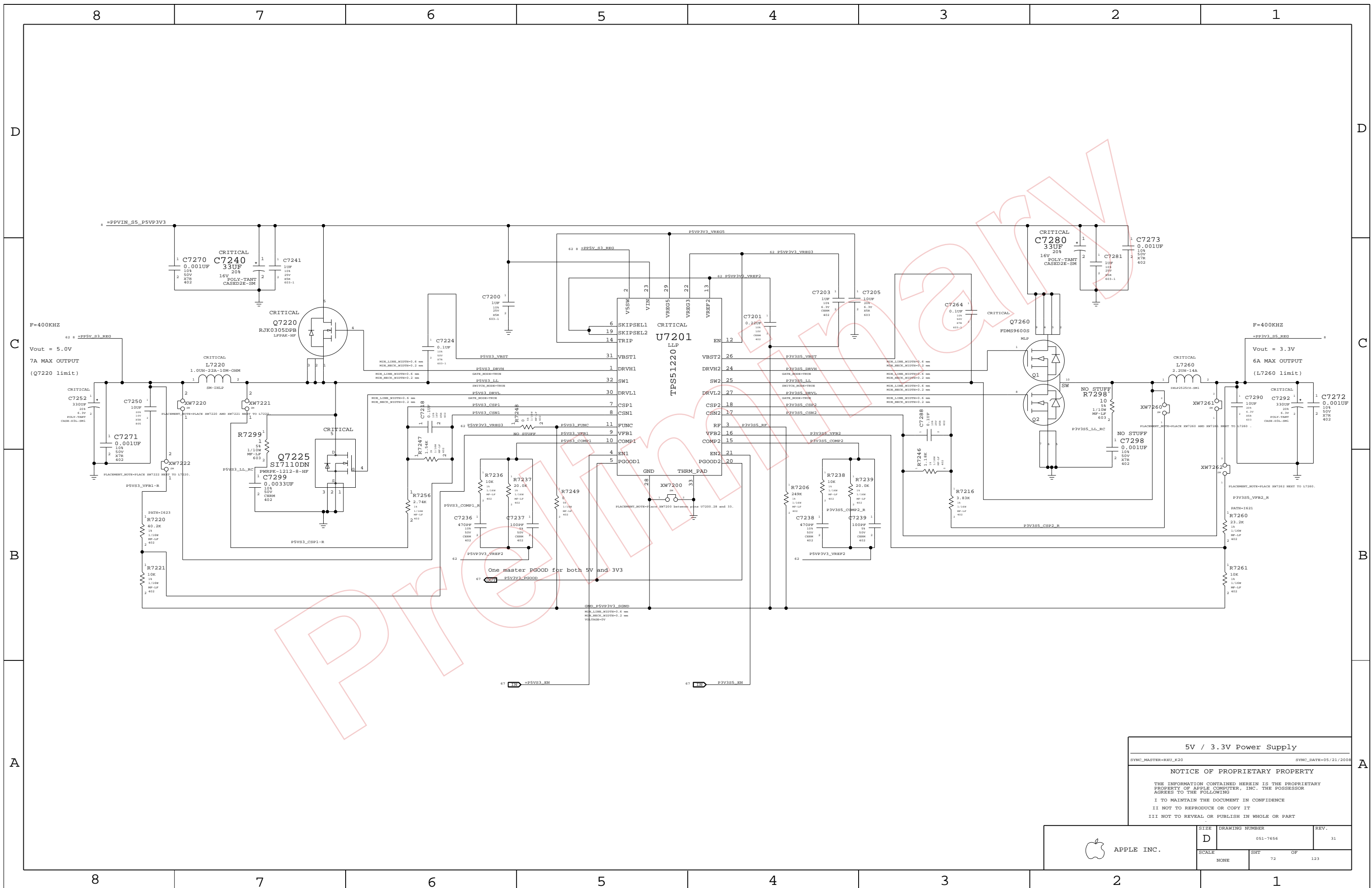
DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

Pin	Signal	Min Line Width	Min Neck Width
61	IMVP6 PHASE1	1.5 MM	0.2 MM
61	IMVP6 BOOT1	0.25 MM	0.2 MM
61	IMVP6 BOOT2	0.25 MM	0.2 MM
61	IMVP6 UGATE1	0.5 MM	0.2 MM
61	IMVP6 LGATE1	0.5 MM	0.2 MM
61	IMVP6 ISEN1	0.25 MM	0.2 MM
61	IMVP6 VSUM1	0.25 MM	0.2 MM
61	IMVP6 VO1	0.25 MM	0.2 MM
61	IMVP6 PHASE2	1.5 MM	0.2 MM
61	IMVP6 BOOT2	0.25 MM	0.2 MM
61	IMVP6 UGATE2	0.5 MM	0.2 MM
61	IMVP6 LGATE2	0.5 MM	0.2 MM
61	IMVP6 ISEN2	0.25 MM	0.2 MM
61	IMVP6 VSUM2	0.25 MM	0.2 MM
61	IMVP6 VO2	0.25 MM	0.2 MM
61	IMVP6 VSEN P	0.25 MM	0.2 MM
61	IMVP6 VSEN N	0.25 MM	0.2 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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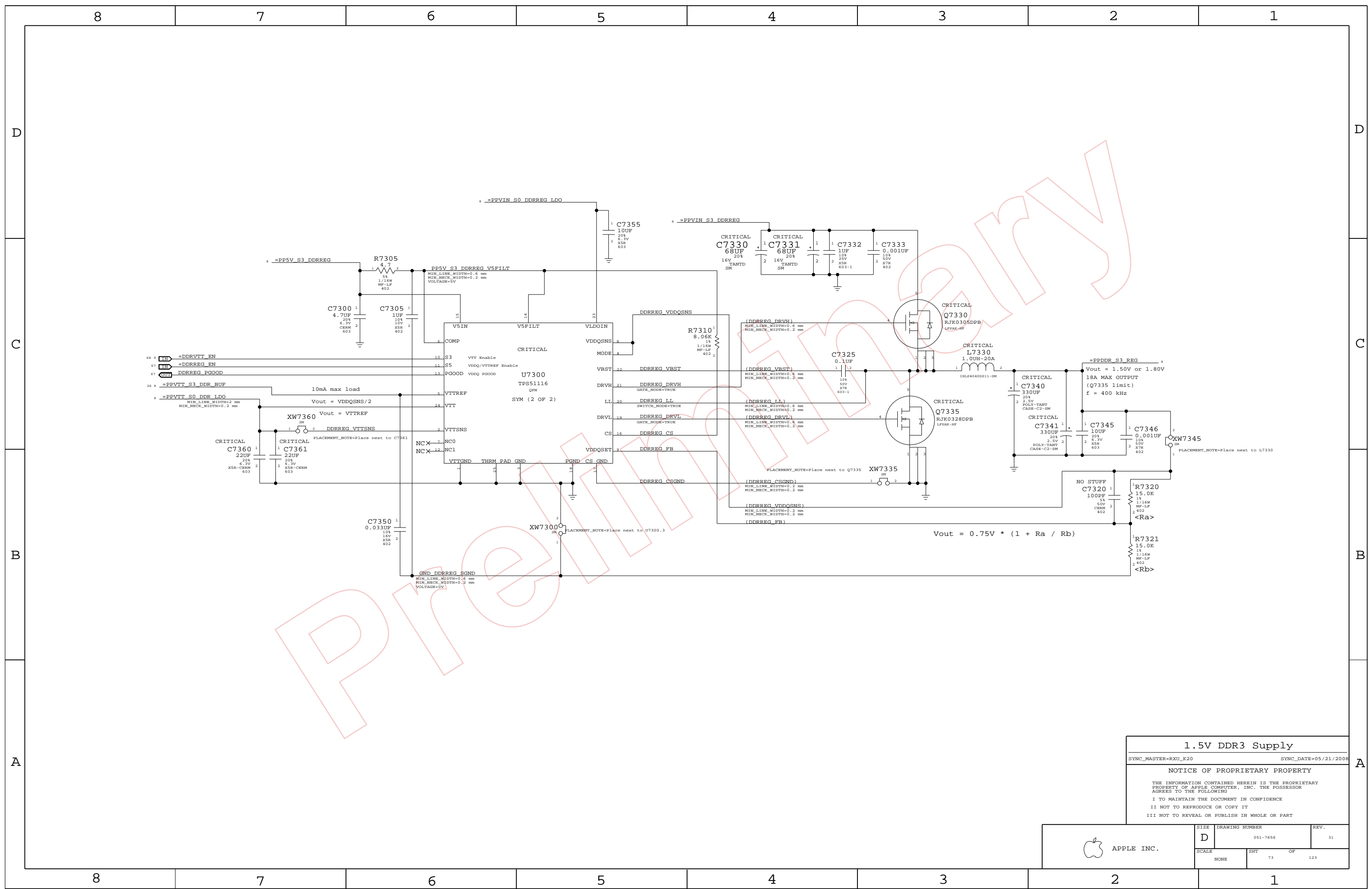
APPLE INC.	SCALE	SHEET	OF	REV.
	NONE	71	123	31



5V / 3.3V Power Supply
 SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	72		



1.5V DDR3 Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

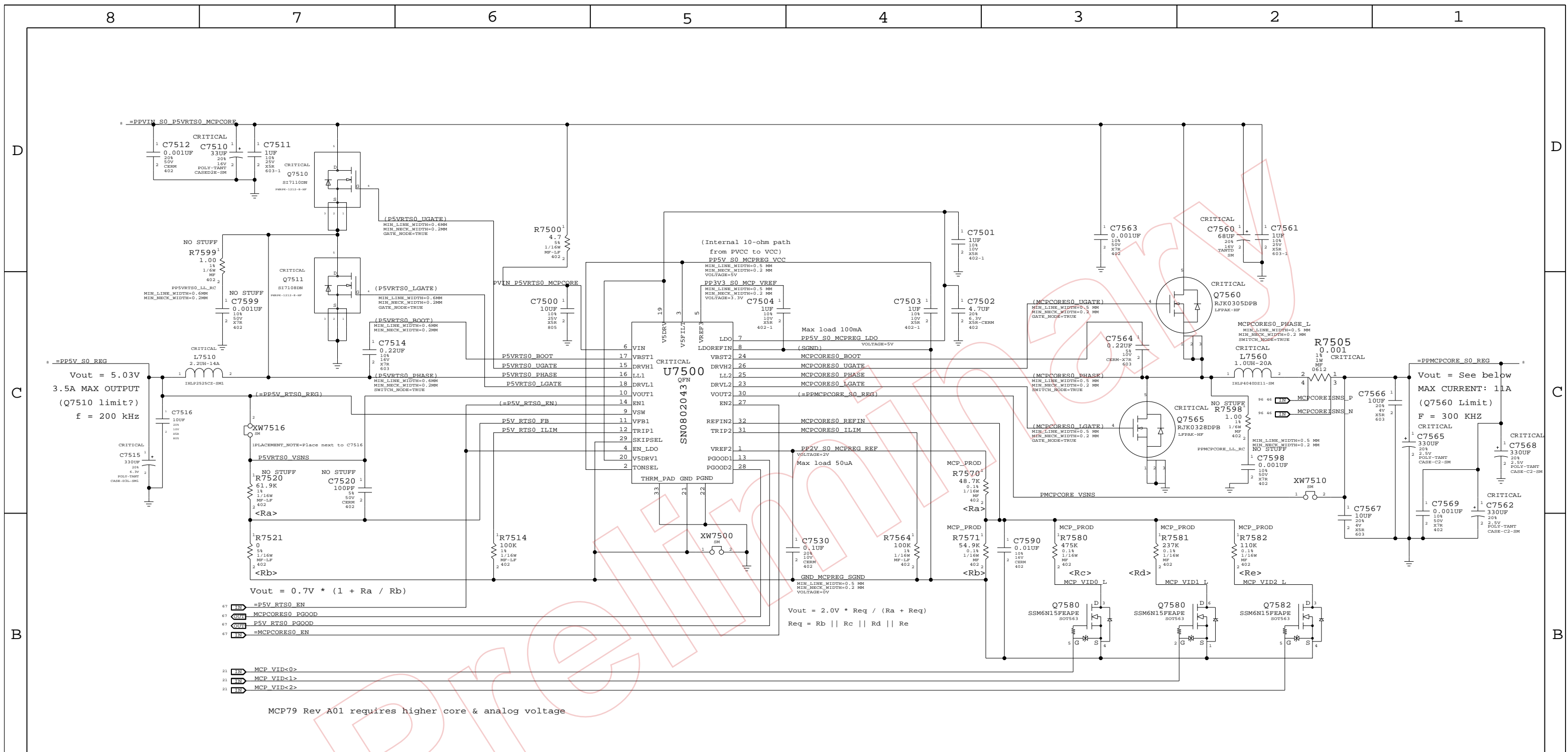
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHT 73	OF 123

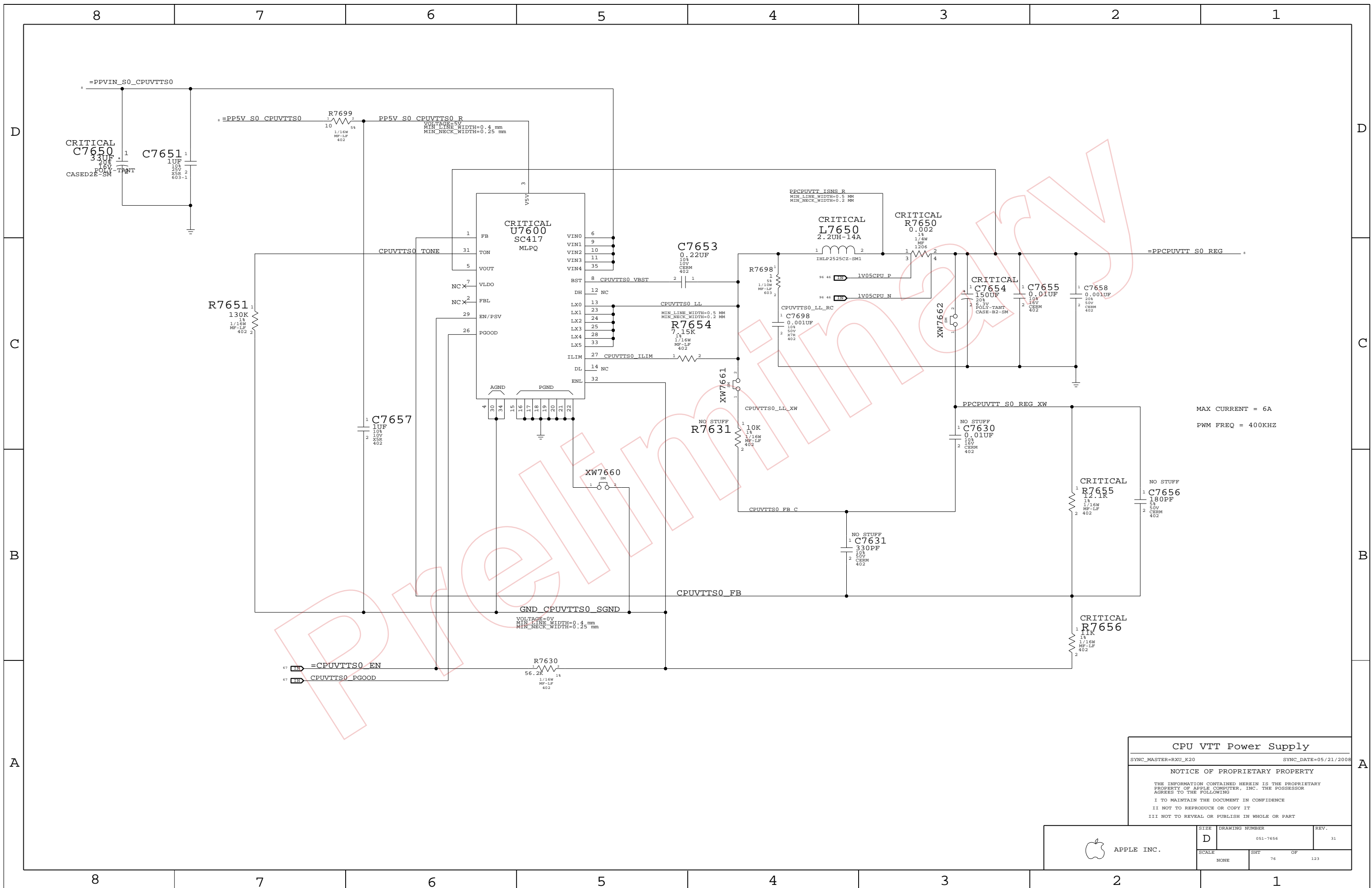


MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES,MTL FILM,1/16W,48.7K,1.0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES,MTL FILM,1/16W,76.8K,1.0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES,MTL FILM,1/16W,523K,1.0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES,MTL FILM,1/16W,267K,1.0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES,MTL FILM,1/16W,130K,1.0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1.0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1.0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1.0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1.0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1.0402,SMD,LF	R7582		MCP_A01Q

VID<2:0>	Rev A01			MCP Target
	Voltage	Voltage	Voltage	
000	+1.224V	+1.060V	+1.05V	
001	+1.159V	+0.994V	+1.00V	
010	+1.101V	+0.937V	+0.95V	
011	+1.049V	+0.885V	+0.90V	
100	+0.995V	+0.830V	+0.85V	
101	+0.952V	+0.789V	+0.80V	
110	+0.913V	+0.752V	+0.75V	
111	+0.876V	+0.719V	+0.70V	

5V_S0 / MCP CORE REGULATOR
 SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008
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CPU VTT Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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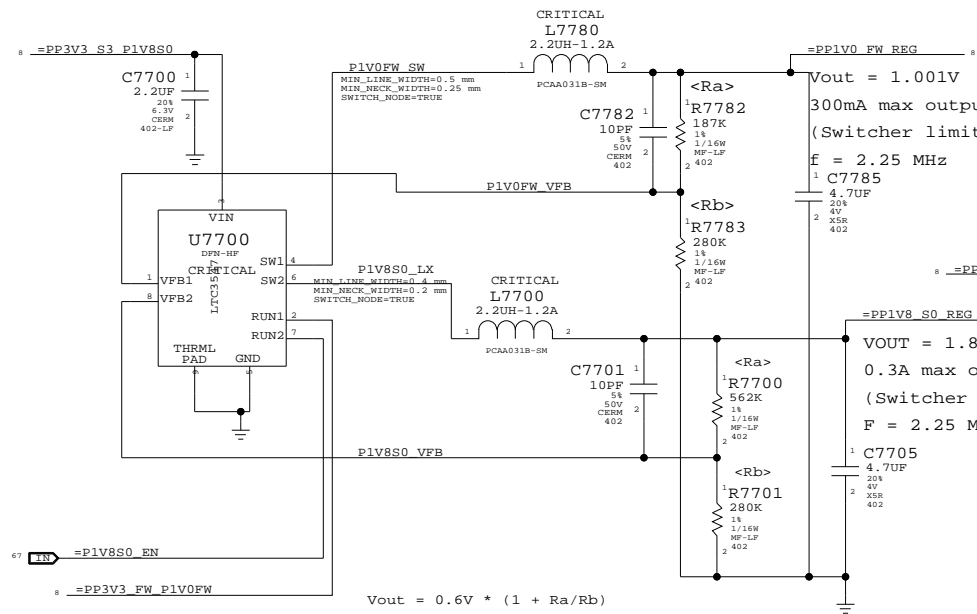
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

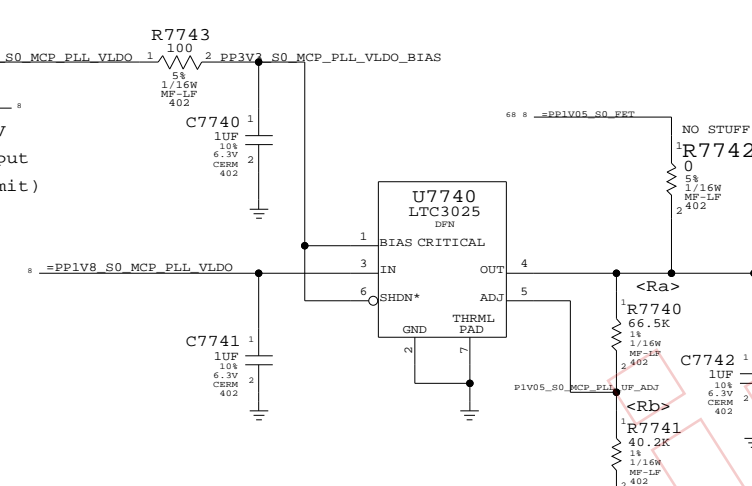
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	76		

1.8V S0 Switcher / 1.0VFW SWITCHER

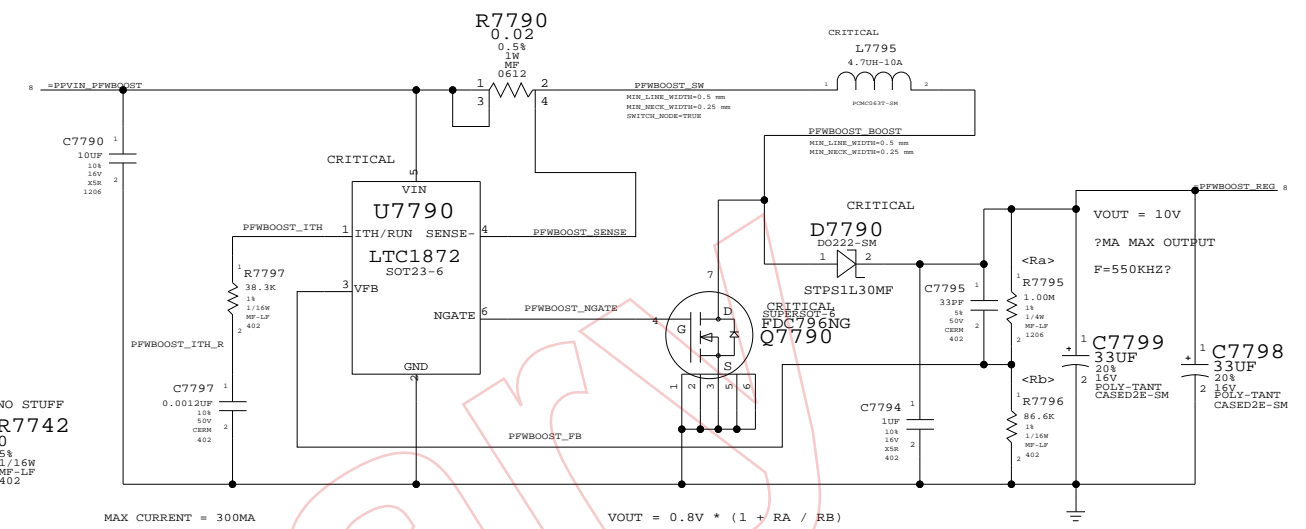
S5 power required for output discharge feature



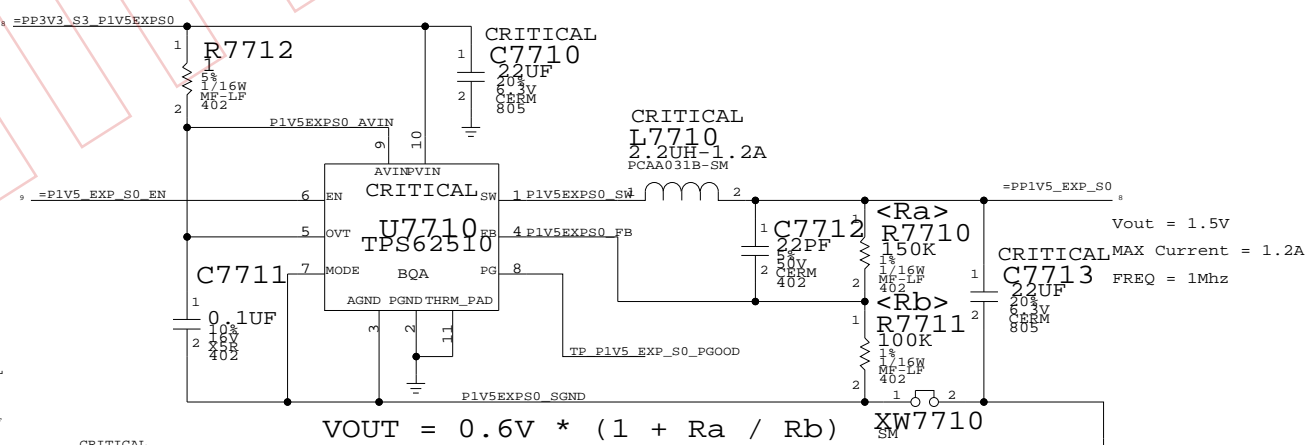
MCP79 PLL VLDO



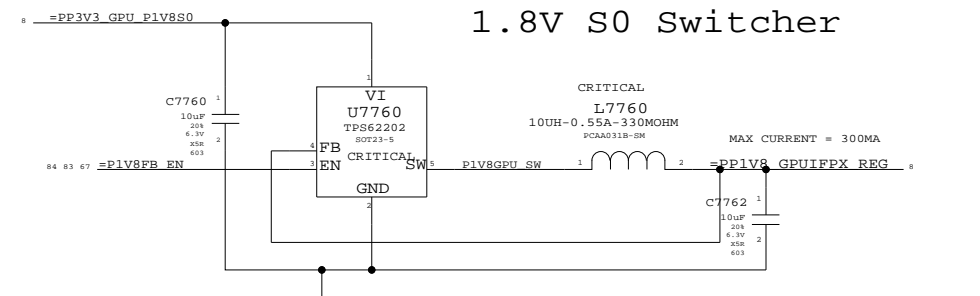
FW BOOST POWER



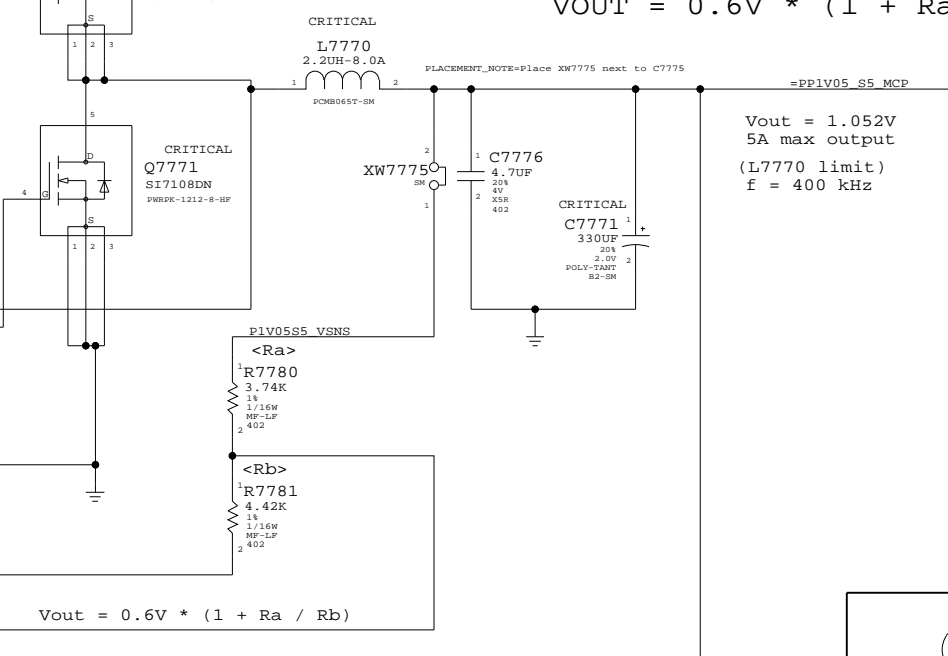
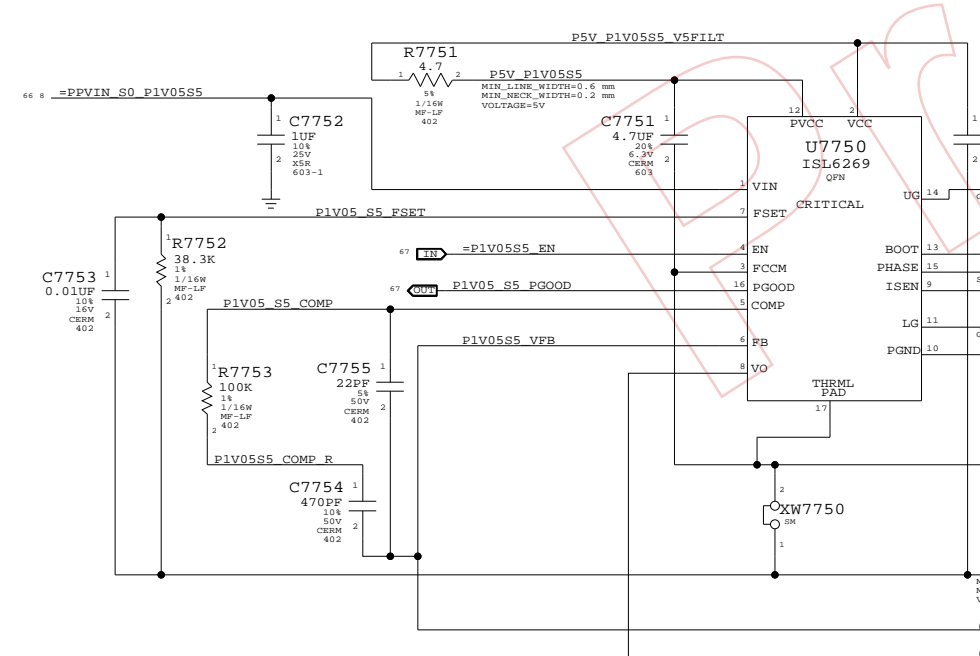
EXPRESSCARD 1.5V_S0 SUPPLY



1.8V S0 Switcher



MCP 1.05V AUXC Supply



Misc Power Supplies

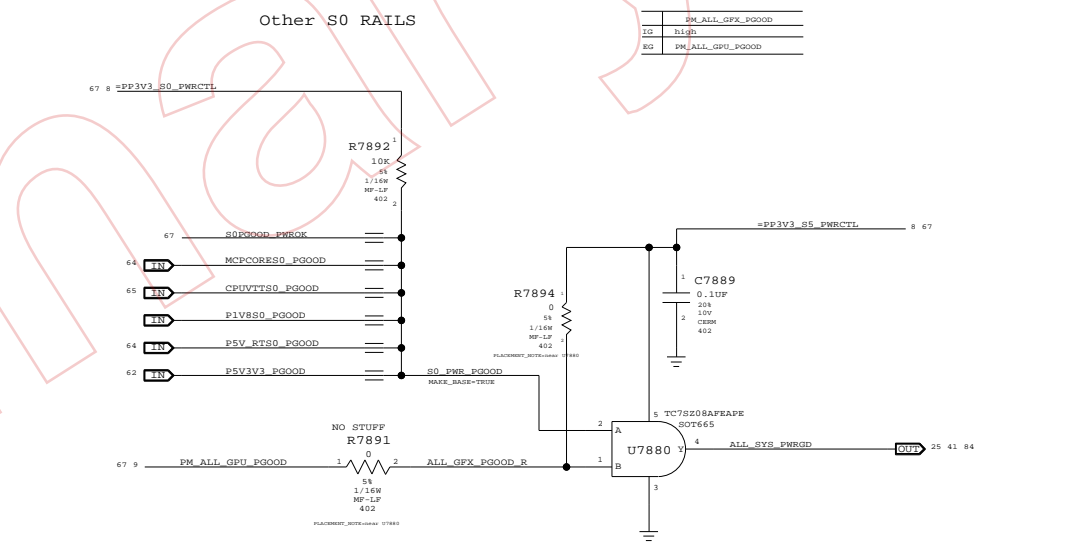
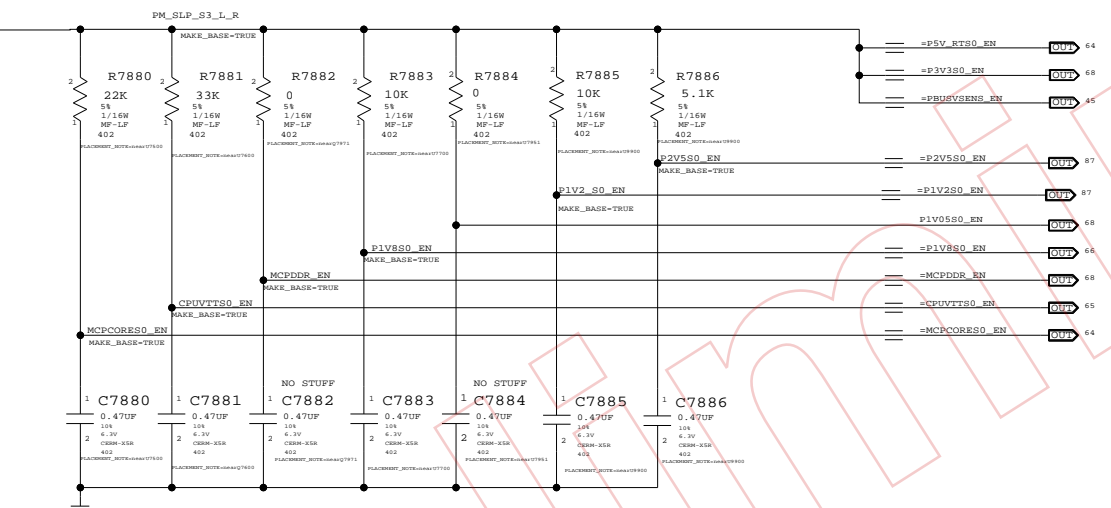
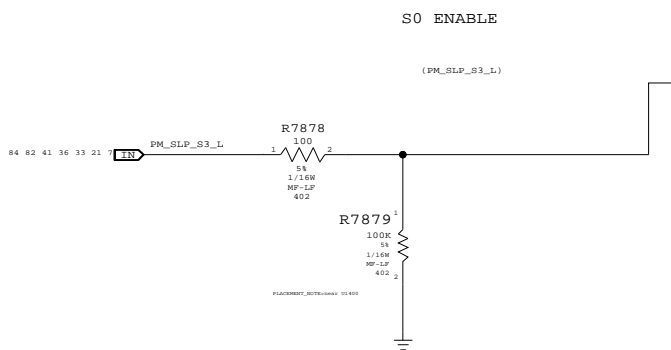
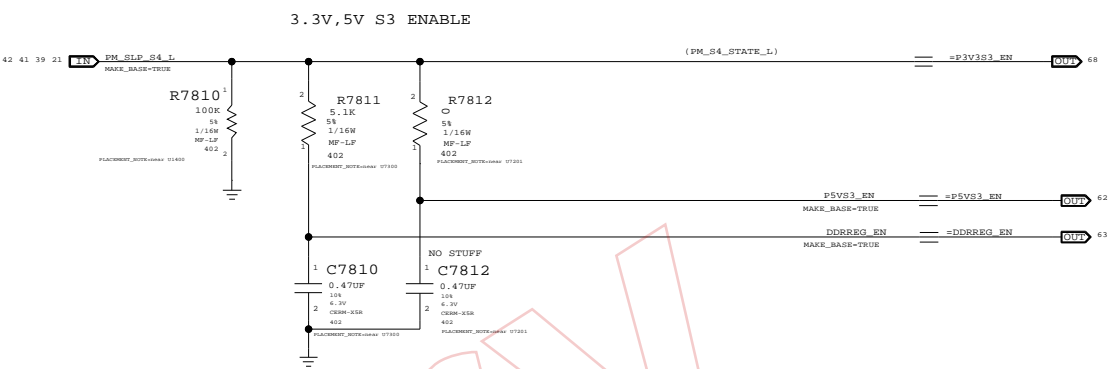
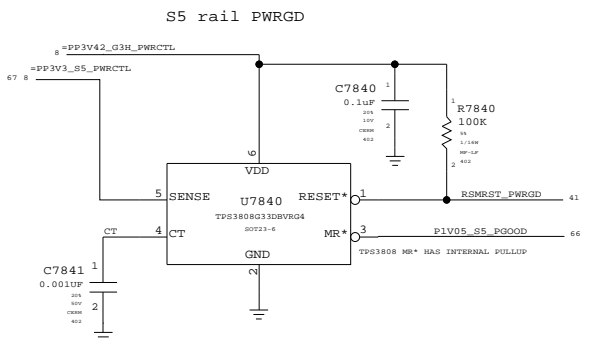
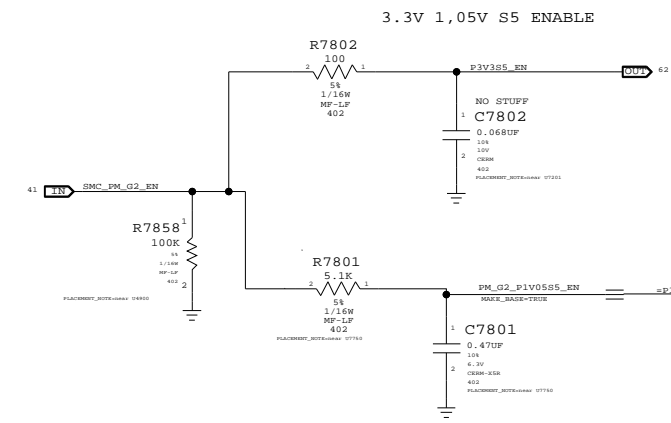
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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	77	123



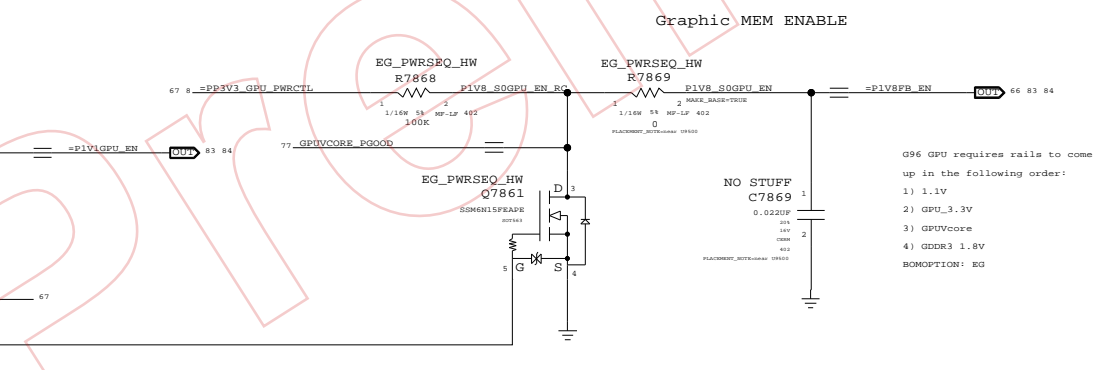
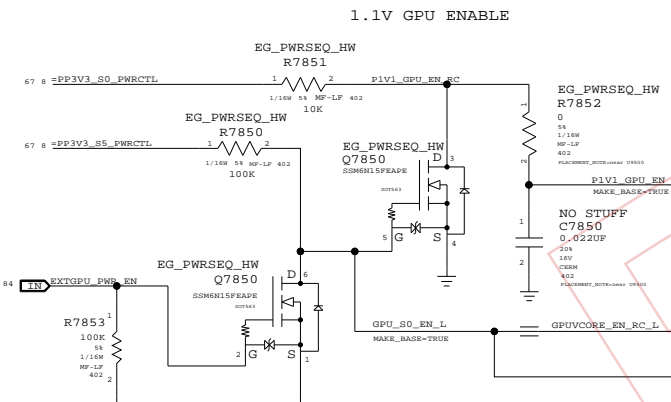
APPLE INC.

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



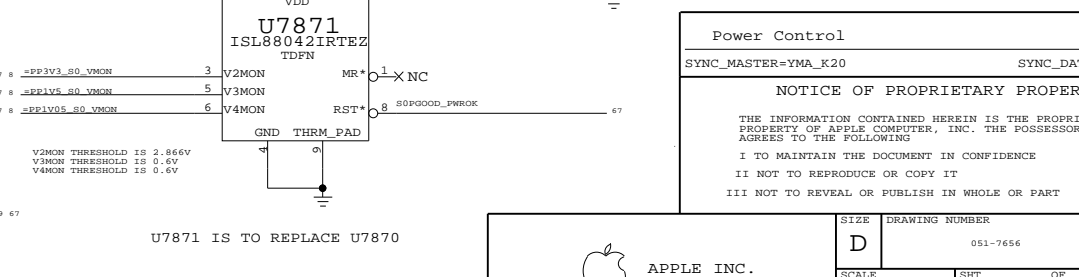
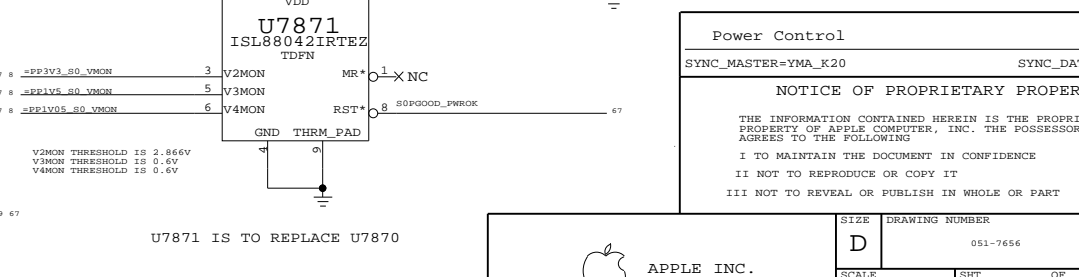
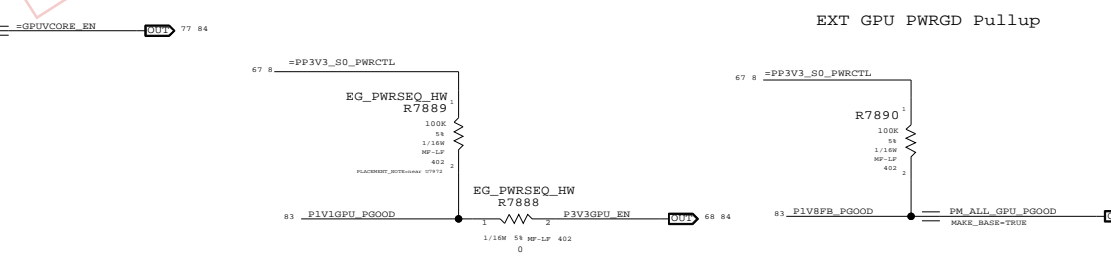
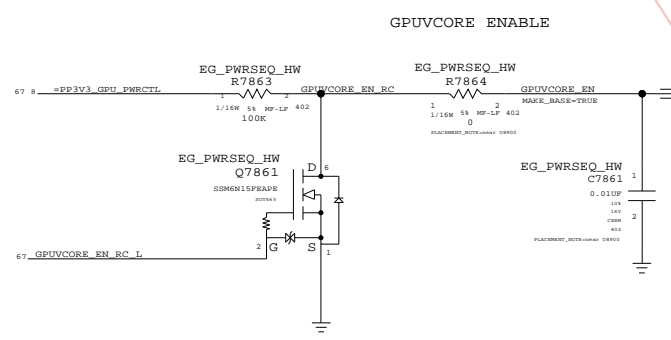
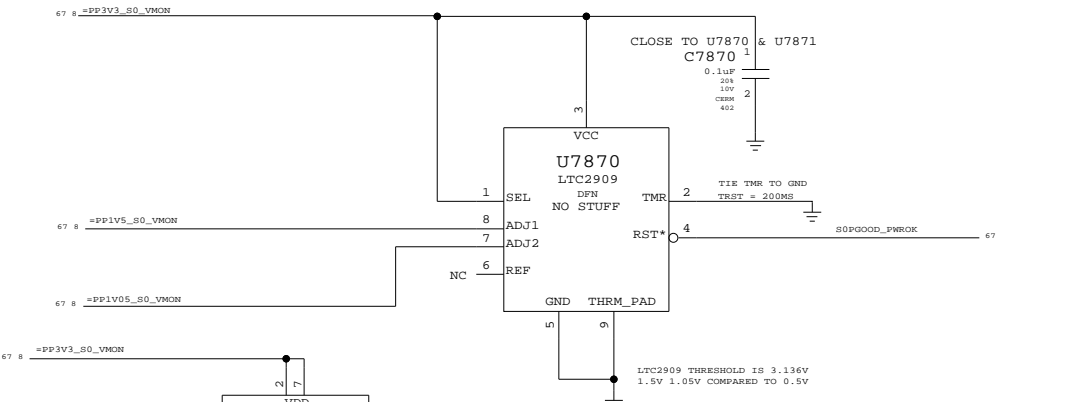
Unused PGOOD signal

TP_DDRREG_PGOOD



3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

place XM0402 if needed to save trace space for pin 7, 8



Power Control

SYNC_MASTER=YMA_K20 SYNC_DATE=09/09/2008

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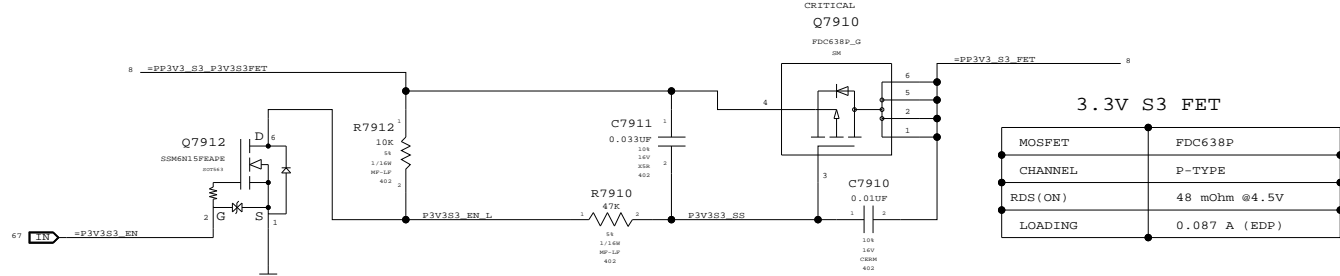
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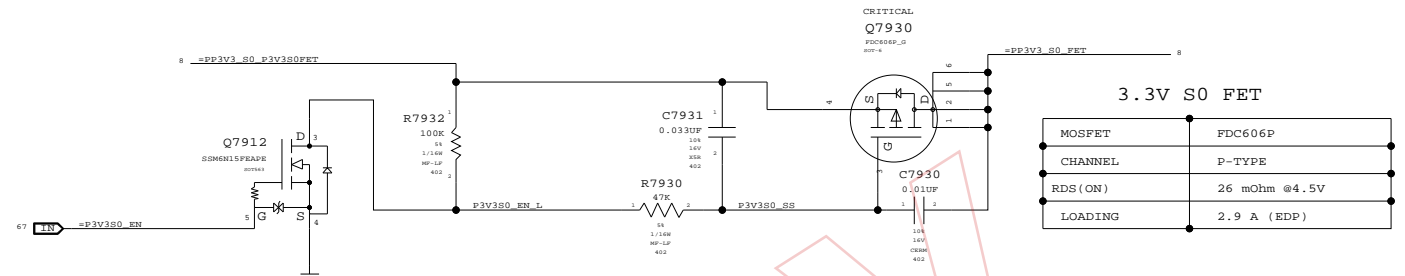
U7871 IS TO REPLACE U7870

3.3V S3 FET



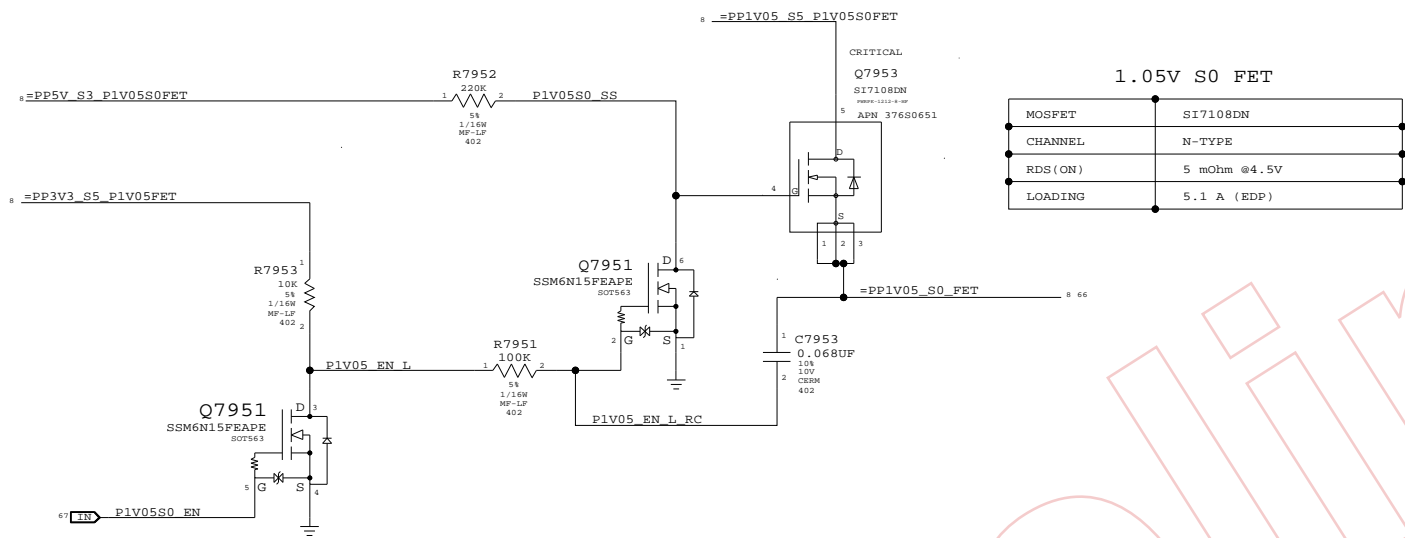
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



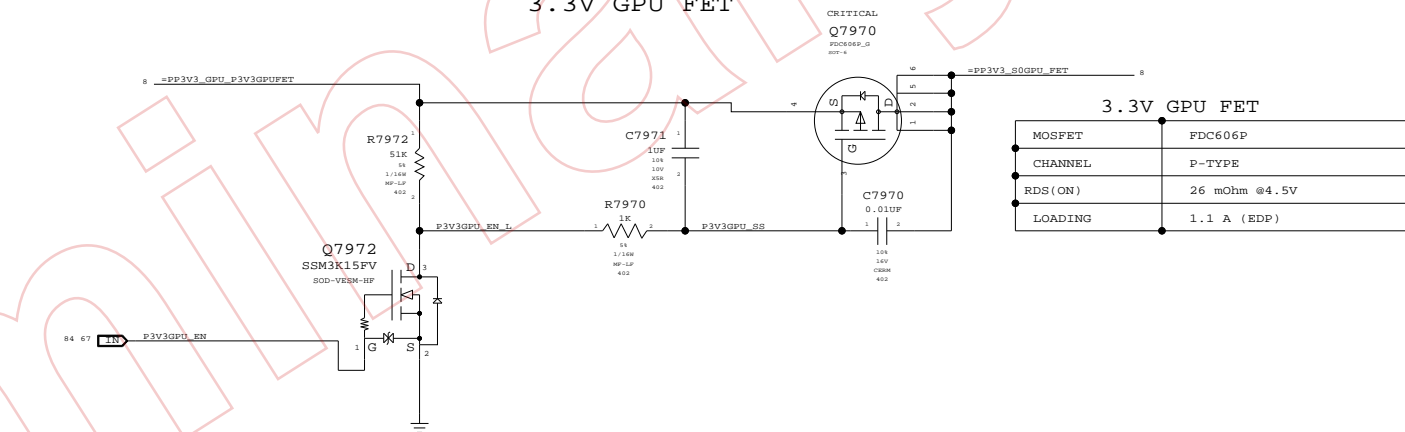
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET



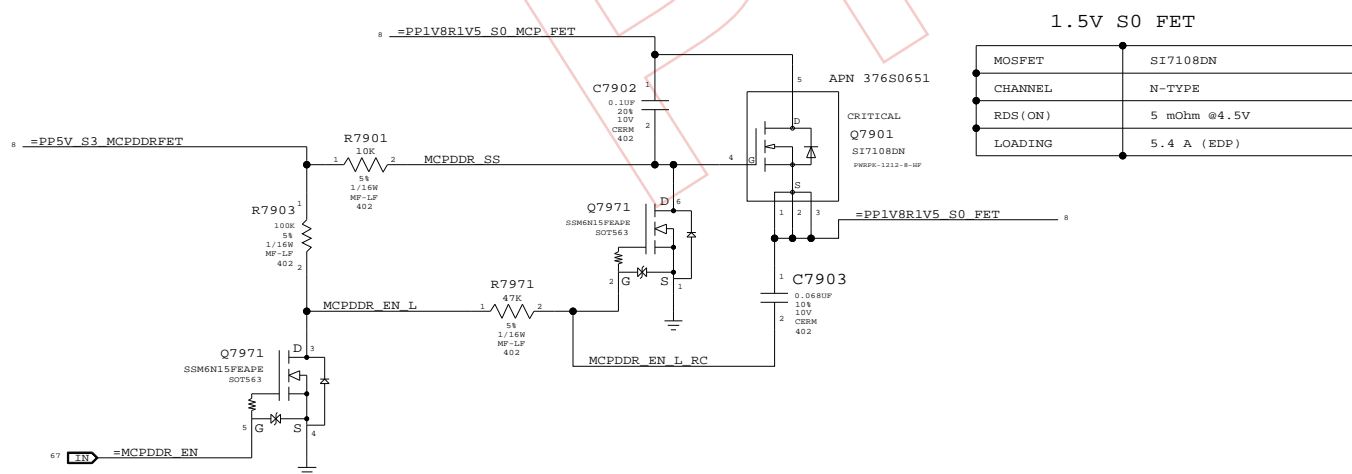
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.1 A (EDP)

3.3V GPU FET



MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)

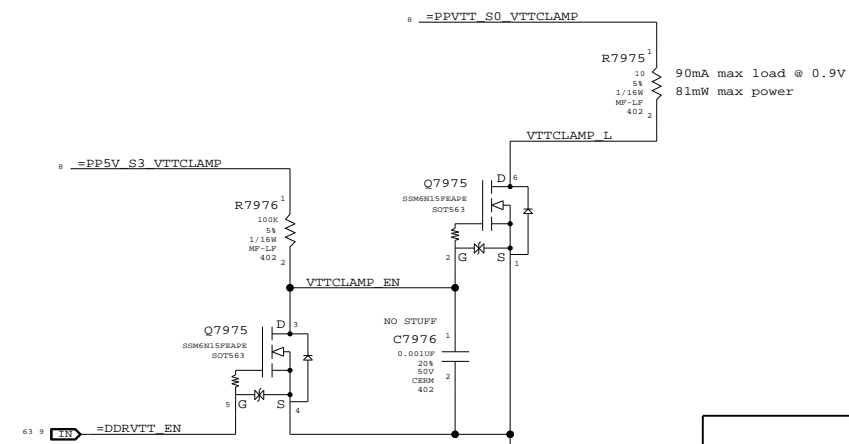
1.5V S0 FET



MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.



Power FETs		
SYNC_MASTER=YMA_K20	SYNC_DATE=05/19/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	NONE	SHT	79 OF 123

Page Notes

Power aliases required by this page:
Signal aliases required by this page:
BOM options provided by this page:

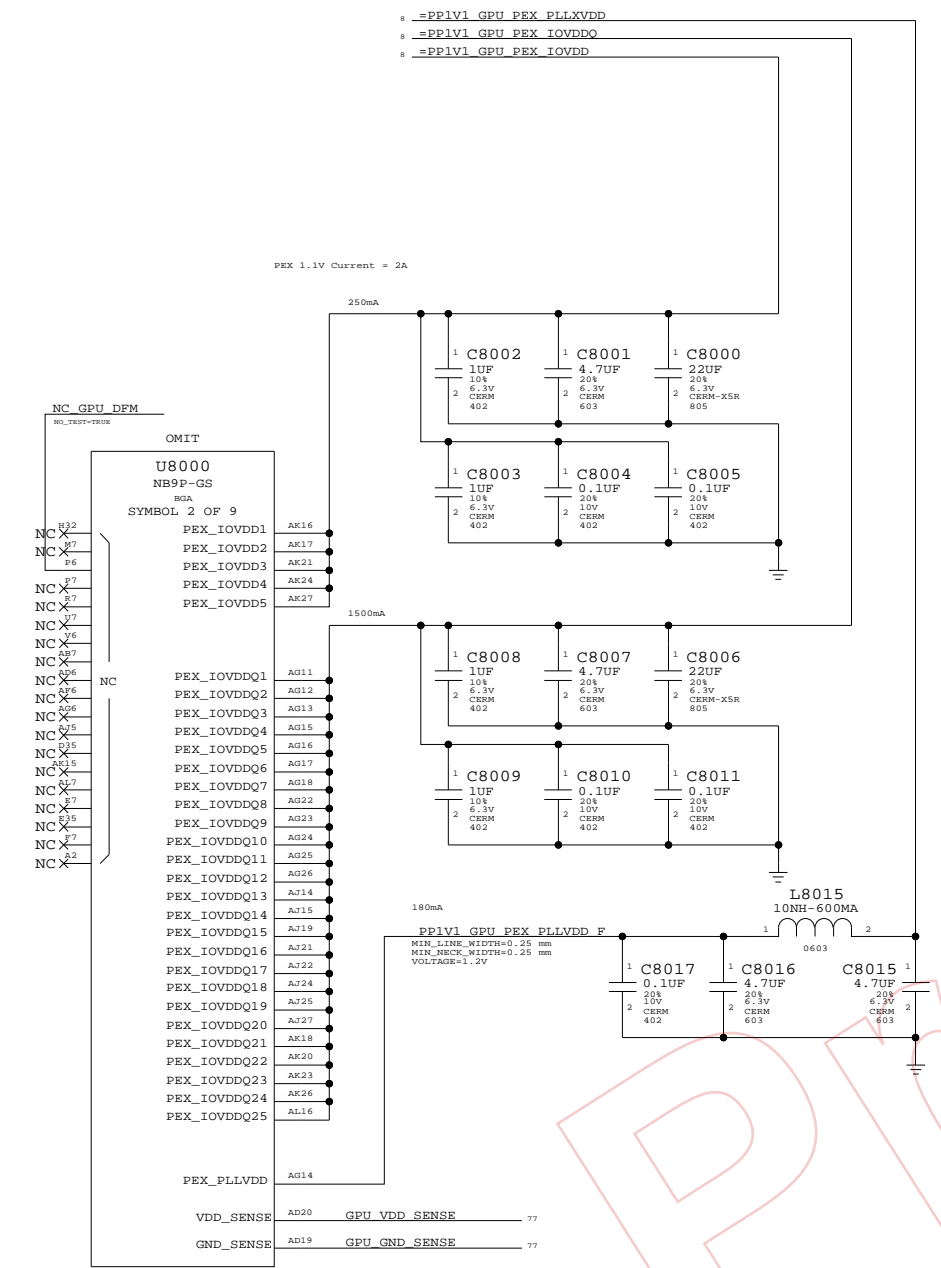
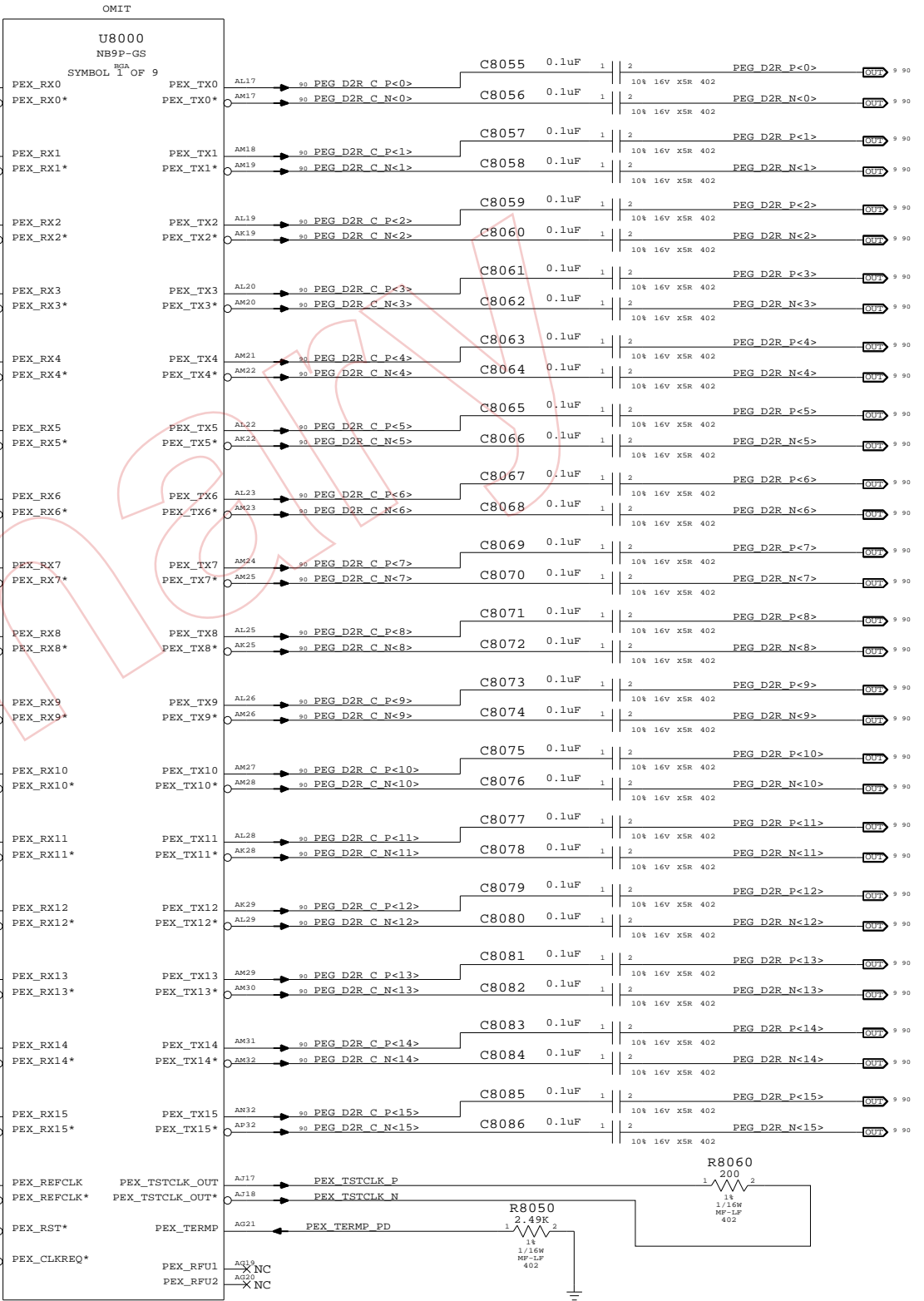
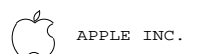


Table listing component values and connections for PEG R2D C P<n> and PEG R2D C N<n> signals. Columns include component ID (e.g., C8020), value (e.g., 0.1uF), and connection points (e.g., AP17, AM17).



NV G96 PCI-E
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Table with columns for SCALE, SHEET, OF, DRAWING NUMBER, and REV. Values include NONE, 80, 123, 051-7656, and 31.



8

7

6

5

4

3

2

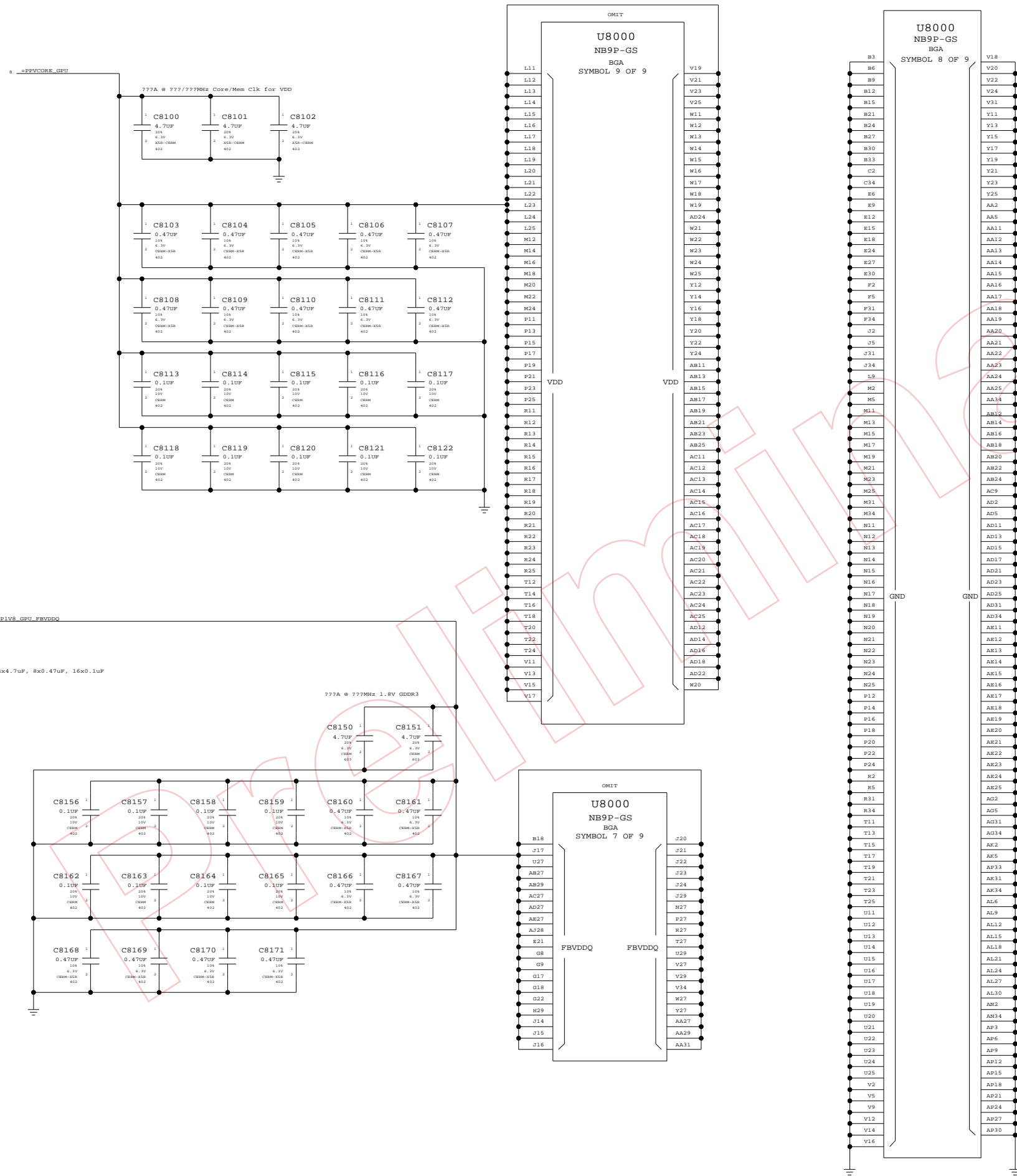
1

Page Notes

Power aliases required by this page:
 - =PPVCORE_GPU
 - =FP1V8_GPU_FBVDQD

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



NV G96 CORE/FB POWER

SYNC_MASTER=M98_MLS SYNC_DATE=04/01/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT		OF
NONE	81		123

8

7

6

5

4

3

2

1

Page Notes

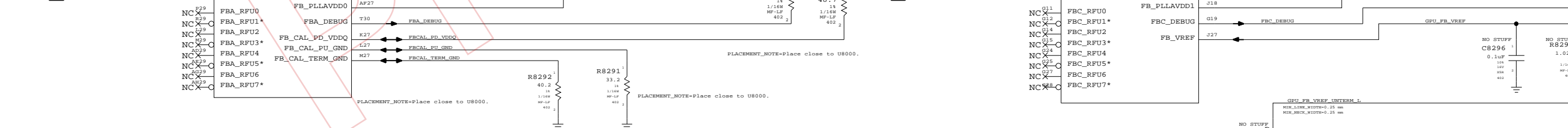
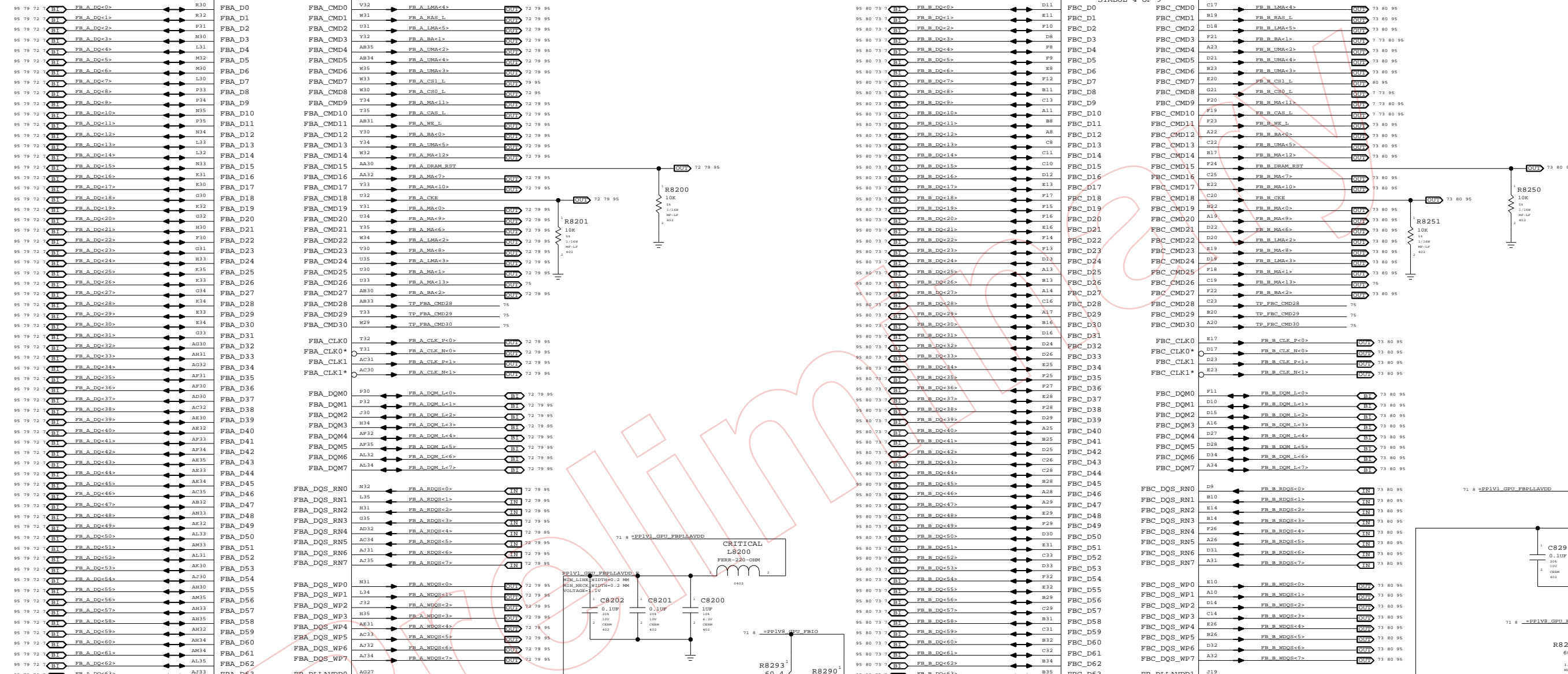
Power aliases required by this page:
 - =PP1V2_GPU_FBLLAVDD
 - =PP1V8_GPU_FBIO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

U8000
 NB9P-GS
 BGA
 SYMBOL 3 OF 9

U8000
 NB9P-GS
 BGA
 SYMBOL 4 OF 9



SIZE		DRAWING NUMBER		REV.	
D		051-7656		31	
SCALE		SHEET		OF	
NONE		82		123	

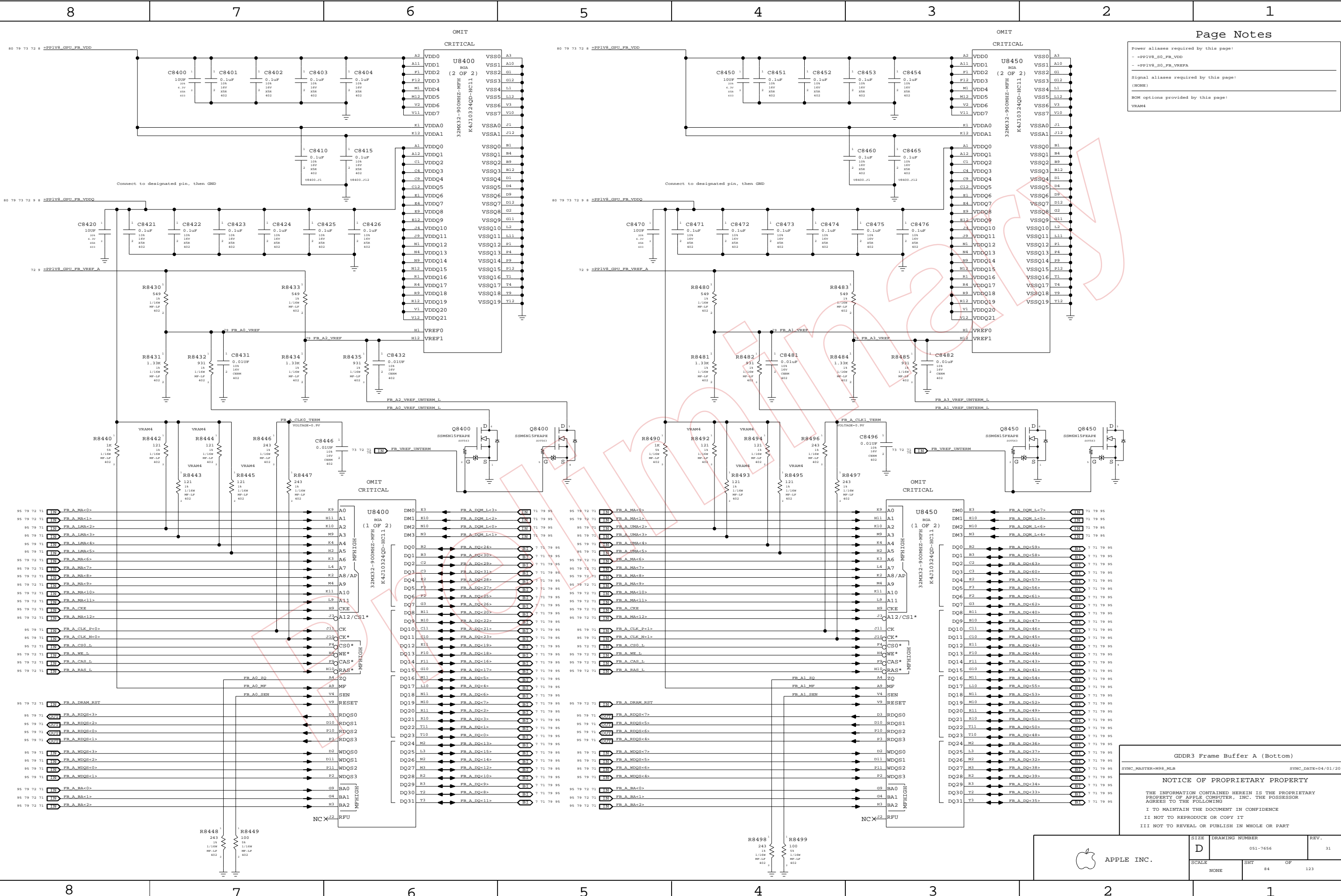


APPLE INC.

Power aliases required by this page:
 - =PP1V8_S0_FB_VDD
 - =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 VRAM4



GDDR3 Frame Buffer A (Bottom)

SYNC_MASTER=M98_MLS SYNC_DATE=04/01/2008

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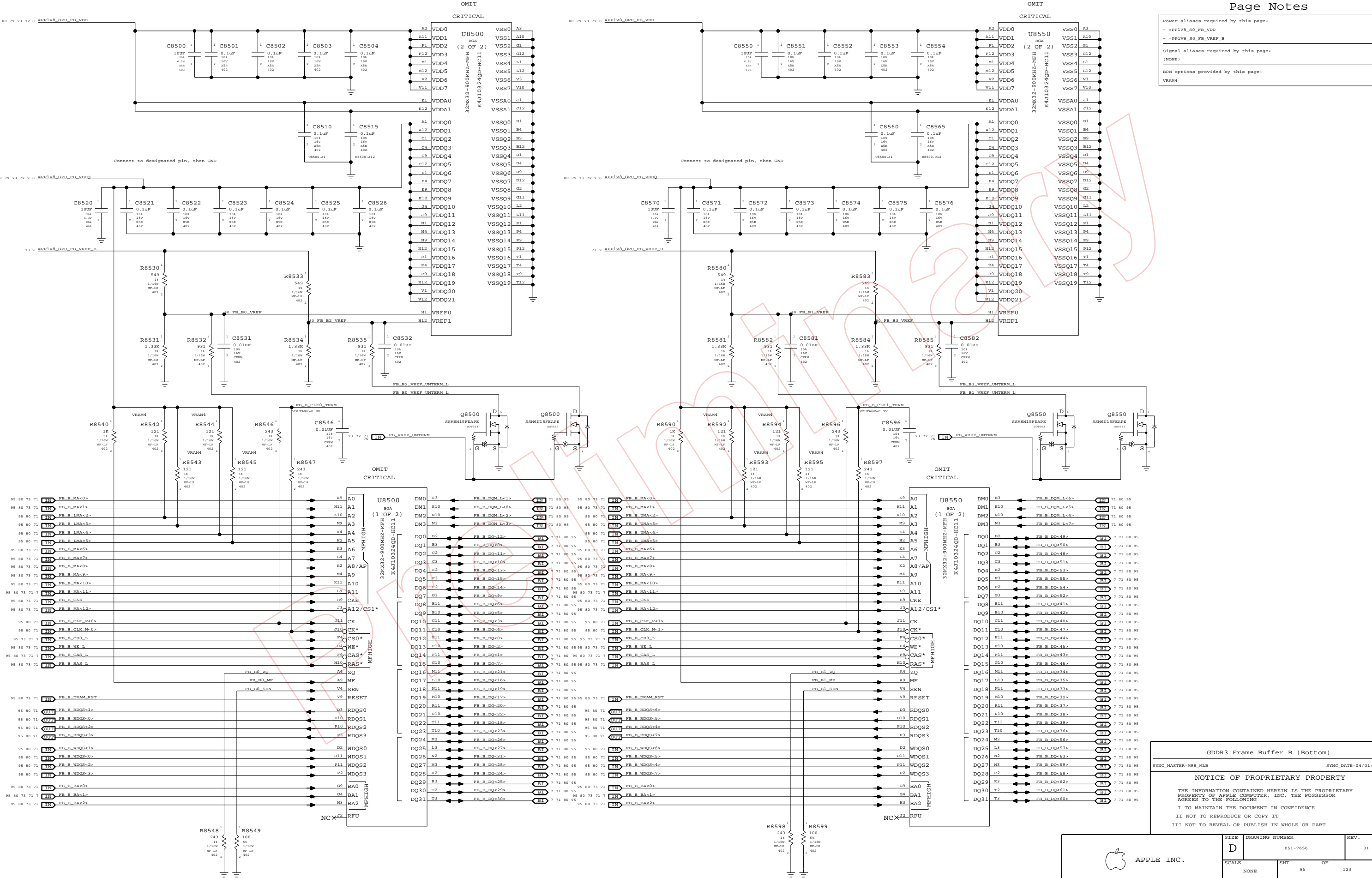
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	84	123



Power aliases required by this page:
 - =PP1V8_S0_FB_VDD
 - =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 VRAM4



GDDR3 Frame Buffer B (Bottom)

SYNC_MASTER=M98_MLS SYNC_DATE=04/01/2008

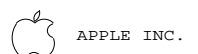
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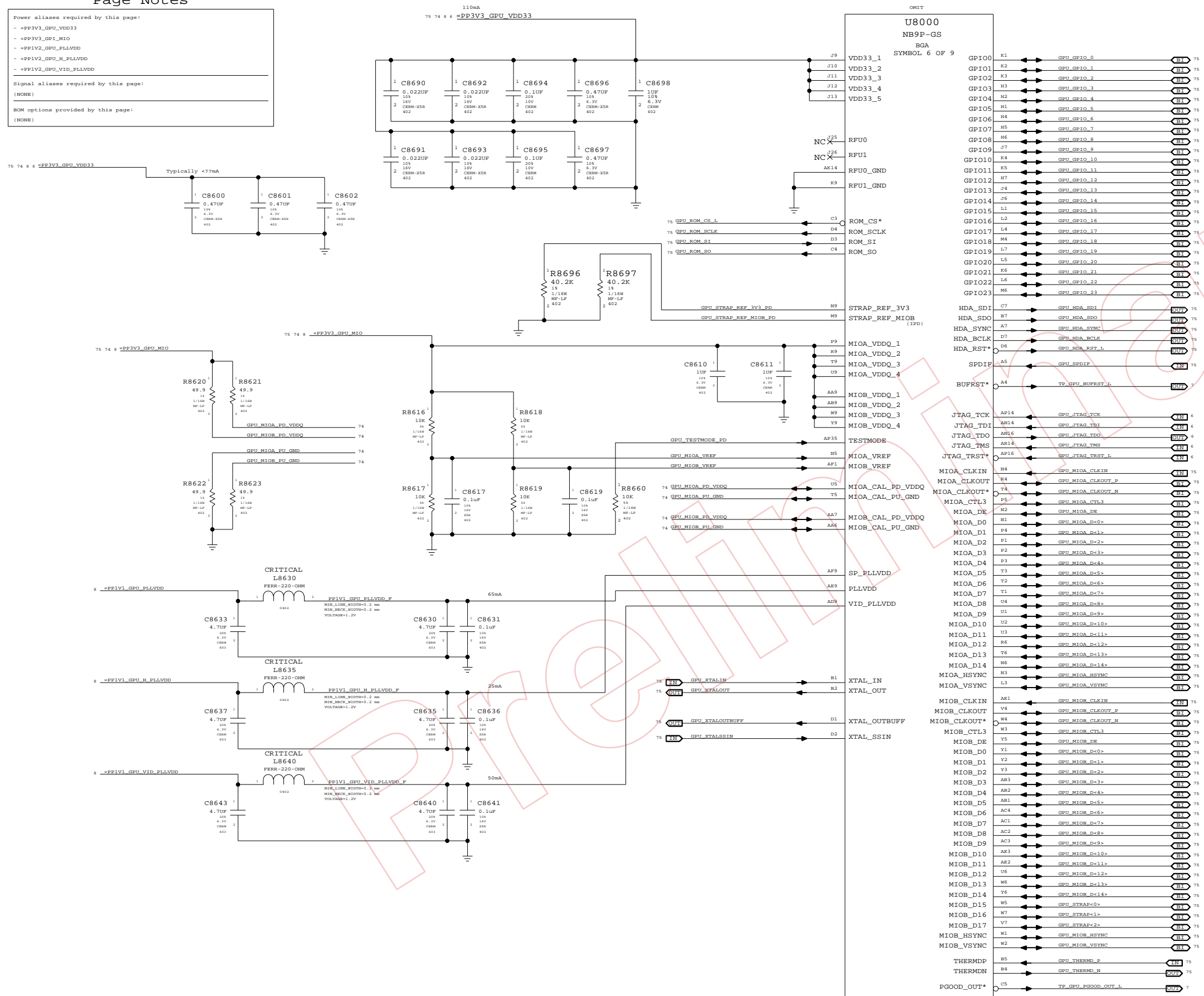
SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	85	123

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_VDD33
 - =PP3V3_GPU_MIO
 - =PP1V2_GPU_PLLVDD
 - =PP1V2_GPU_M_PLLVDD
 - =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
 (NONE)

NOM options provided by this page:
 (NONE)



NV G96 GPIO/MIO/MISC

SYNC_MASTER=K20_MLS SYNC_DATE=09/24/2008

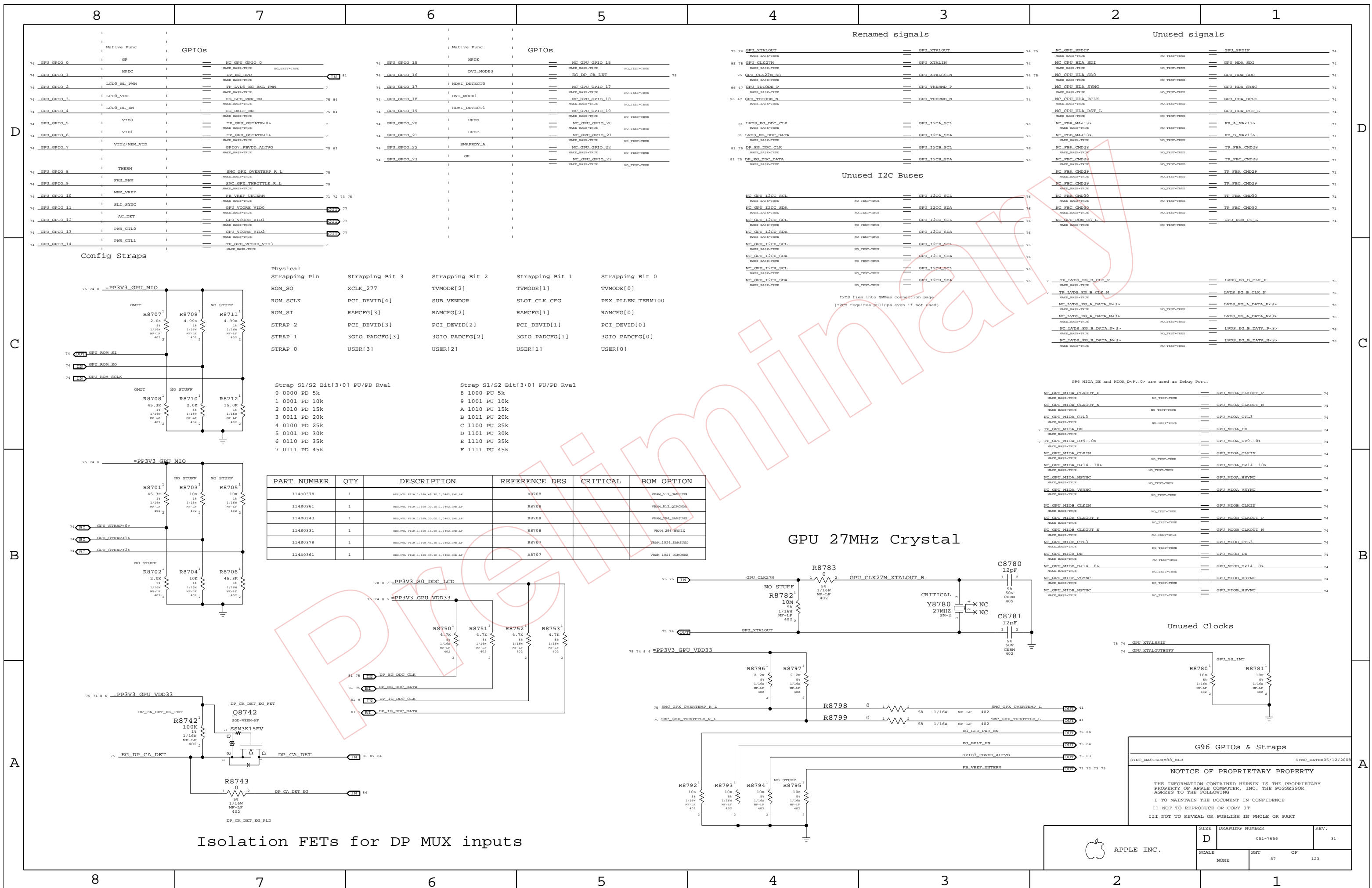
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Physical Strapping Pin

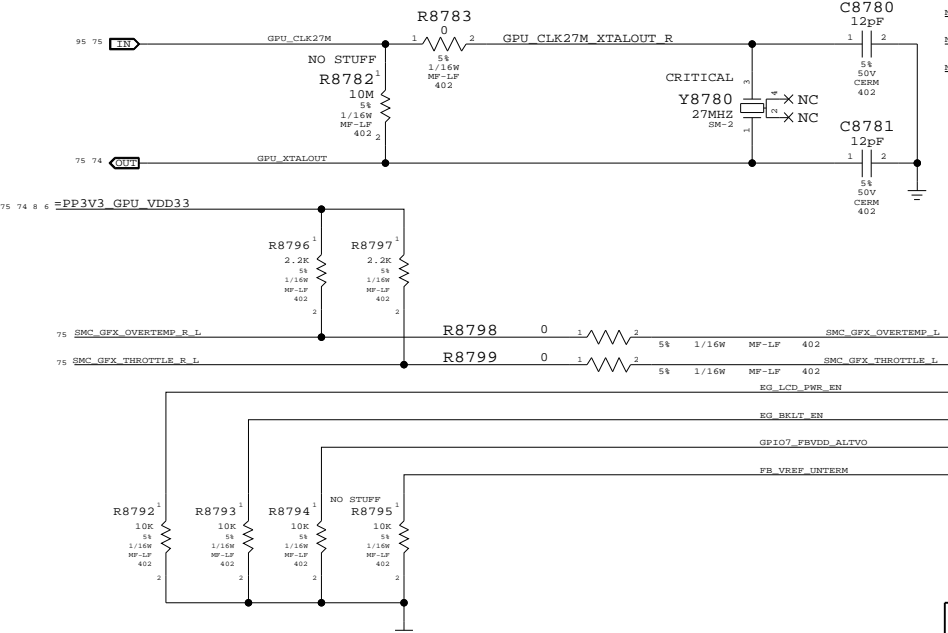
Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP 0	USER[3]	USER[2]	USER[1]
			USER[0]

Strap S1/S2 Bit[3:0] PU/PD Rval

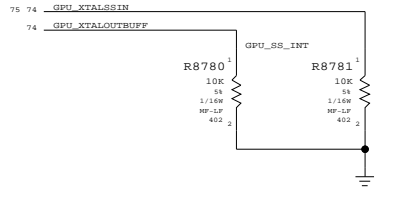
Strap S1/S2 Bit[3:0] PU/PD Rval	Strap S1/S2 Bit[3:0] PU/PD Rval
0 0000 PD 5k	8 1000 PU 5k
1 0001 PD 10k	9 1001 PU 10k
2 0010 PD 15k	A 1010 PU 15k
3 0011 PD 20k	B 1011 PU 20k
4 0100 PD 25k	C 1100 PU 25k
5 0101 PD 30k	D 1101 PU 30k
6 0110 PD 35k	E 1110 PU 35k
7 0111 PD 45k	F 1111 PU 45k

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11480378	1	RES.MEL.F12M,1/16W,45.3K,1,0402,080,LF	R8708		VRAM_S12_SAMSUNG
11480361	1	RES.MEL.F12M,1/16W,30.1K,1,0402,080,LF	R8708		VRAM_S12_QIMONDA
11480343	1	RES.MEL.F12M,1/16W,20.5K,1,0402,080,LF	R8708		VRAM_S14_SAMSUNG
11480331	1	RES.MEL.F12M,1/16W,15.0K,1,0402,080,LF	R8708		VRAM_S14_SAMSUNG
11480378	1	RES.MEL.F12M,1/16W,45.3K,1,0402,080,LF	R8707		VRAM_1024_SAMSUNG
11480361	1	RES.MEL.F12M,1/16W,30.1K,1,0402,080,LF	R8707		VRAM_1024_QIMONDA

GPU 27MHz Crystal



Unused Clocks



G96 GPIOs & Straps

SYNC_MASTER=M98_MLS SYNC_DATE=05/12/2008

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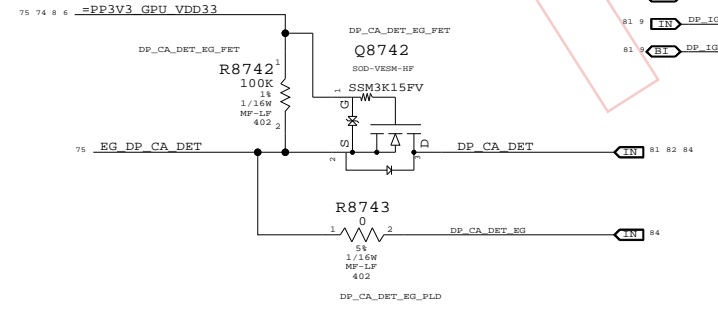
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	D	051-7656	31
	SCALE	SHT	OF
	NONE	87	123

Isolation FETs for DP MUX inputs



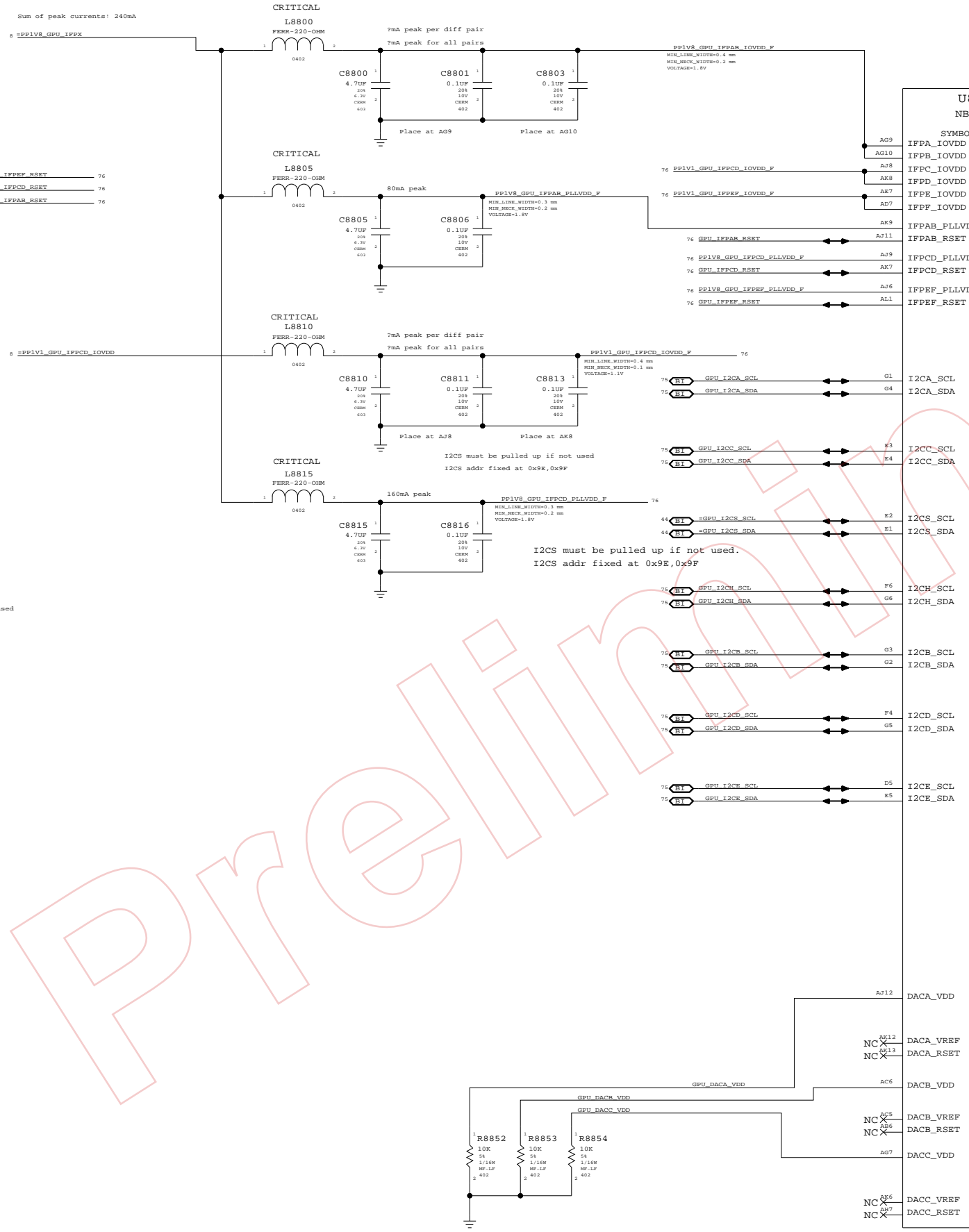
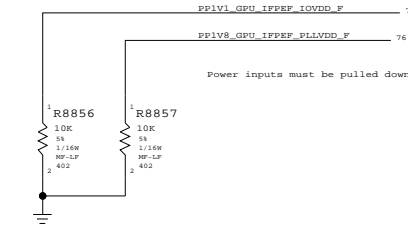
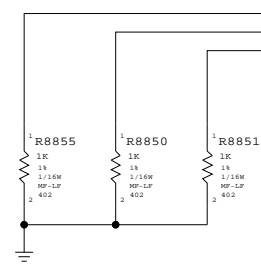
Page Notes

Power aliases required by this page:
 - =PP1V8_GPU_IPFX
 - =PP3V3_GPU_IPFCD_IOVDD

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Sum of peak currents: 240mA



U8000 NB9P-GS BGA SYMBOL 5 OF 9

AM11	IFPA_TXC	LVDS EG A_CLK_P	84	95	
AM12	IFPA_TXC*	LVDS EG A_CLK_N	84	95	
AM9	IFPA_TXD0	LVDS EG A_DATA_P<0>	84	95	
AL9	IFPA_TXD0*	LVDS EG A_DATA_N<0>	84	95	
AM10	IFPA_TXD1	LVDS EG A_DATA_P<1>	84	95	
AM9	IFPA_TXD1*	LVDS EG A_DATA_N<1>	84	95	
AK10	IFPA_TXD2	LVDS EG A_DATA_P<2>	84	95	
AL10	IFPA_TXD2*	LVDS EG A_DATA_N<2>	7	84	95
AK11	IFPA_TXD3	LVDS EG A_DATA_P<3>	75		
AL11	IFPA_TXD3*	LVDS EG A_DATA_N<3>	75		
AP13	IFPB_TXC	LVDS EG B_CLK_P	75		
AN13	IFPB_TXC*	LVDS EG B_CLK_N	75		
AM9	IFPB_TXD4	LVDS EG B_DATA_P<0>	84	95	
AP9	IFPB_TXD4*	LVDS EG B_DATA_N<0>	84	95	
AP10	IFPB_TXD5	LVDS EG B_DATA_P<1>	84	95	
AN10	IFPB_TXD5*	LVDS EG B_DATA_N<1>	84	95	
AK11	IFPB_TXD6	LVDS EG B_DATA_P<2>	84	95	
AK10	IFPB_TXD6*	LVDS EG B_DATA_N<2>	84	95	
AN11	IFPB_TXD7	LVDS EG B_DATA_P<3>	75		
AP11	IFPB_TXD7*	LVDS EG B_DATA_N<3>	75		
AP2	IFPC_AUX	DP EG AUX_CH_P			
AN3	IFPC_AUX*	DP EG AUX_CH_N			
AM7	IFPC_L0	DP EG ML_P<0>	81	95	
AL5	IFPC_L0*	DP EG ML_N<0>	81	95	
AM5	IFPC_L1	DP EG ML_P<1>	81	95	
AM3	IFPC_L1*	DP EG ML_N<1>	81	95	
AM4	IFPC_L2	DP EG ML_P<2>	81	95	
AP1	IFPC_L2*	DP EG ML_N<2>	81	95	
AR2	IFPC_L3	DP EG ML_P<3>	81	95	
AR2	IFPC_L3*	DP EG ML_N<3>	81	95	
AN4	IFPD_AUX	NC			
AN4	IFPD_AUX*	NC			
AN5	IFPD_L0	NC			
AN5	IFPD_L0*	NC			
AN7	IFPD_L1	NC			
AN7	IFPD_L1*	NC			
AN5	IFPD_L2	NC			
AN5	IFPD_L2*	NC			
AN5	IFPD_L3	NC			
AN5	IFPD_L3*	NC			
AN4	IFPE_AUX	NC			
AN4	IFPE_AUX*	NC			
AN5	IFPF_L0	NC			
AN5	IFPF_L0*	NC			
AN5	IFPF_L1	NC			
AN5	IFPF_L1*	NC			
AN5	IFPF_L2	NC			
AN5	IFPF_L2*	NC			
AN5	IFPF_L3	NC			
AN5	IFPF_L3*	NC			
AN3	IFPF_AUX	NC			
AN3	IFPF_AUX*	NC			
AN4	DACA_RED	NC			
AN4	DACA_GREEN	NC			
AL3	DACA_BLUE	NC			
AN1	DACA_HSYNC	NC			
AL3	DACA_VSYNC	NC			
AN4	DACB_RED	NC			
AN4	DACB_GREEN	NC			
V4	DACB_BLUE	NC			
AN5	DACB_CS	NC			
AN5	DACC_RED	NC			
AN5	DACC_GREEN	NC			
AN5	DACC_BLUE	NC			
AN5	DACC_HSYNC	NC			
AN5	DACC_VSYNC	NC			

NV G96 Video Interfaces

SYNC_MASTER=K20_MLS SYNC_DATE=09/24/2008

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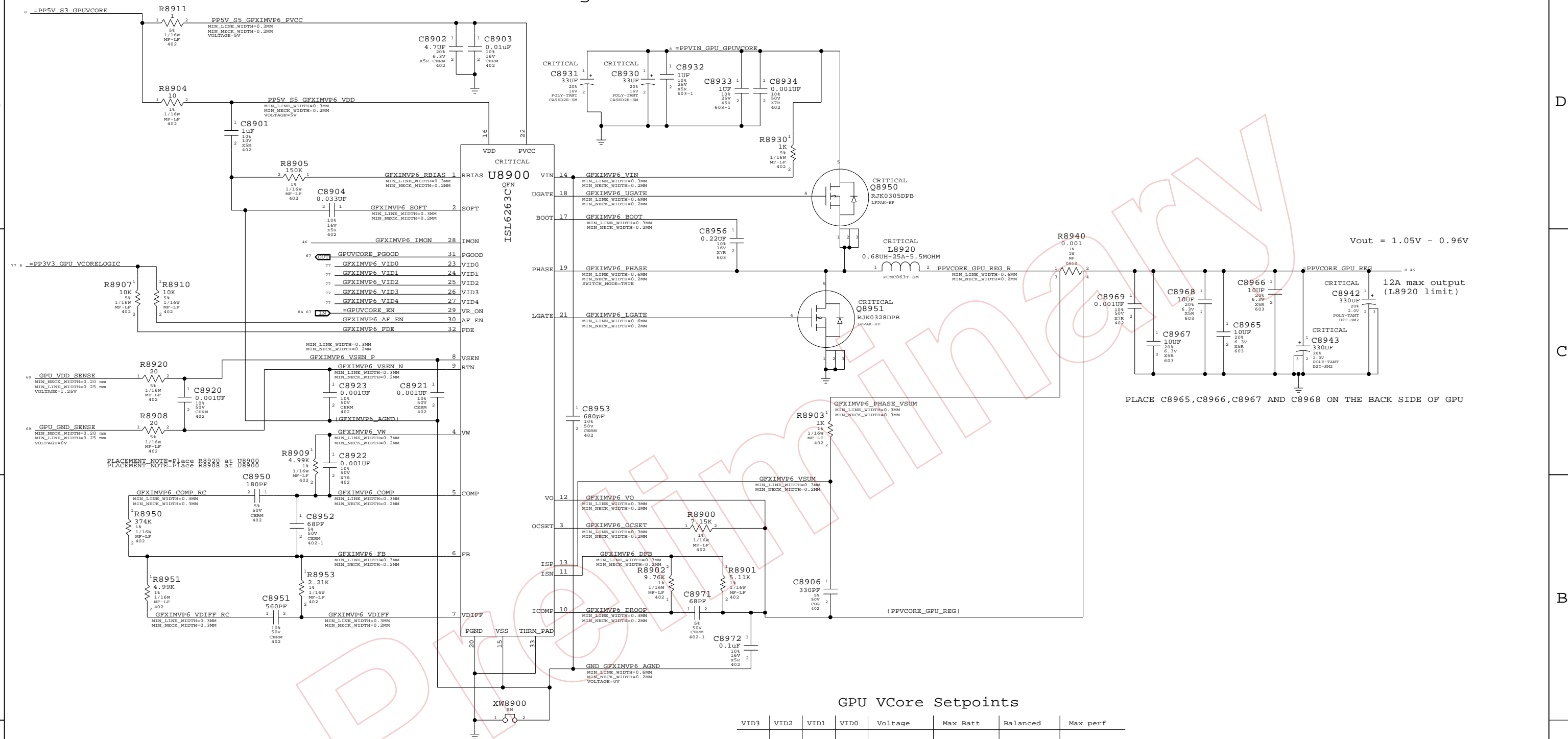
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GPU VCore Regulator



PLACE C8965, C8966, C8967 AND C8968 ON THE BACK SIDE OF GPU

GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	X		-
1	1	1	0	0.92700V	-	X	-
1	0	1	1	1.00425V	-	-	X

Other VID states may not be valid

Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1, GPUVID1_1, GPUVID0_1
GPUVID_1P00V	GPUVID2_0, GPUVID1_1, GPUVID0_1

GPU (G96) CORE SUPPLY

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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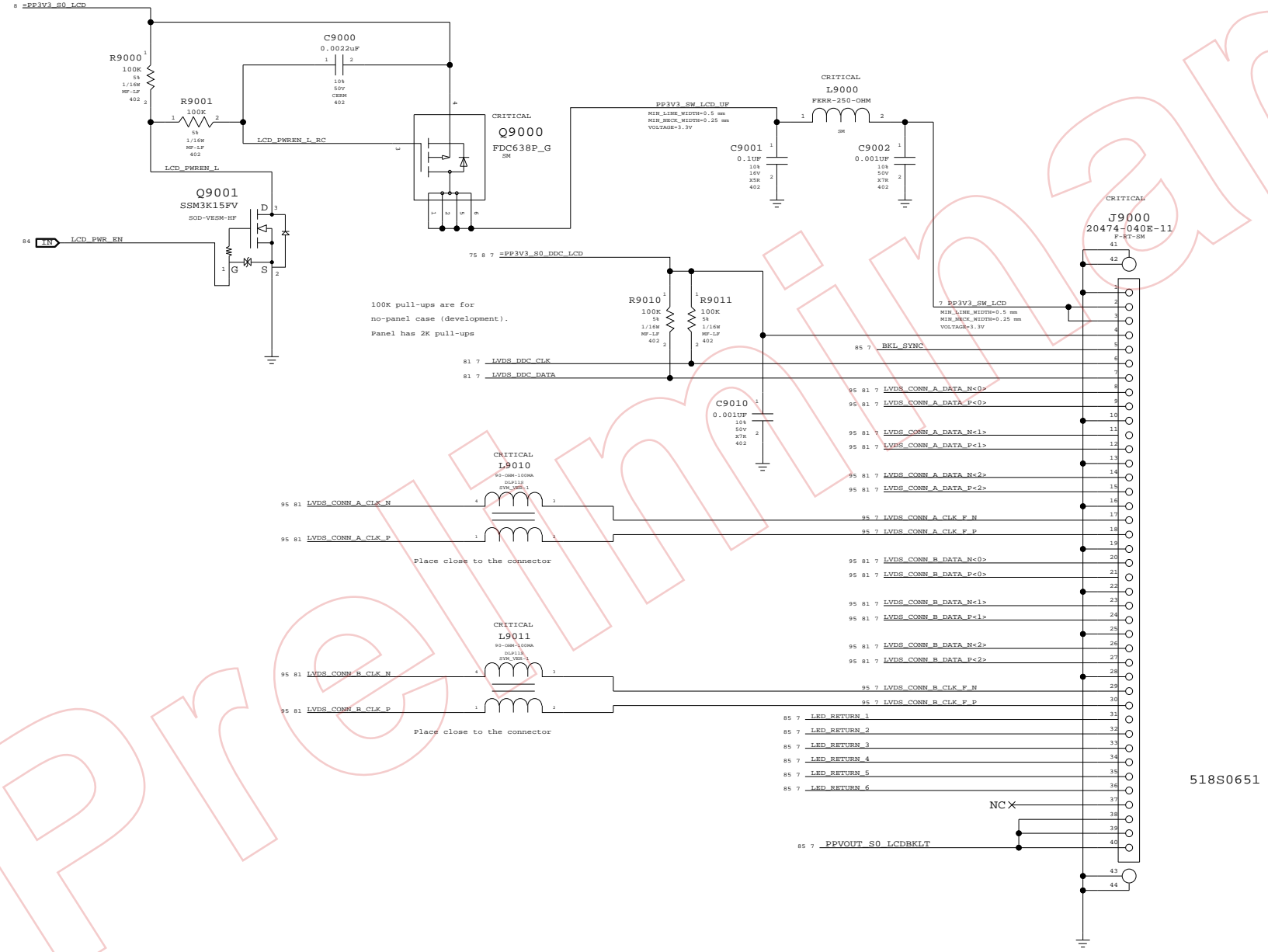
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	89	123

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=M98_MLS SYNC_DATE=07/14/2008

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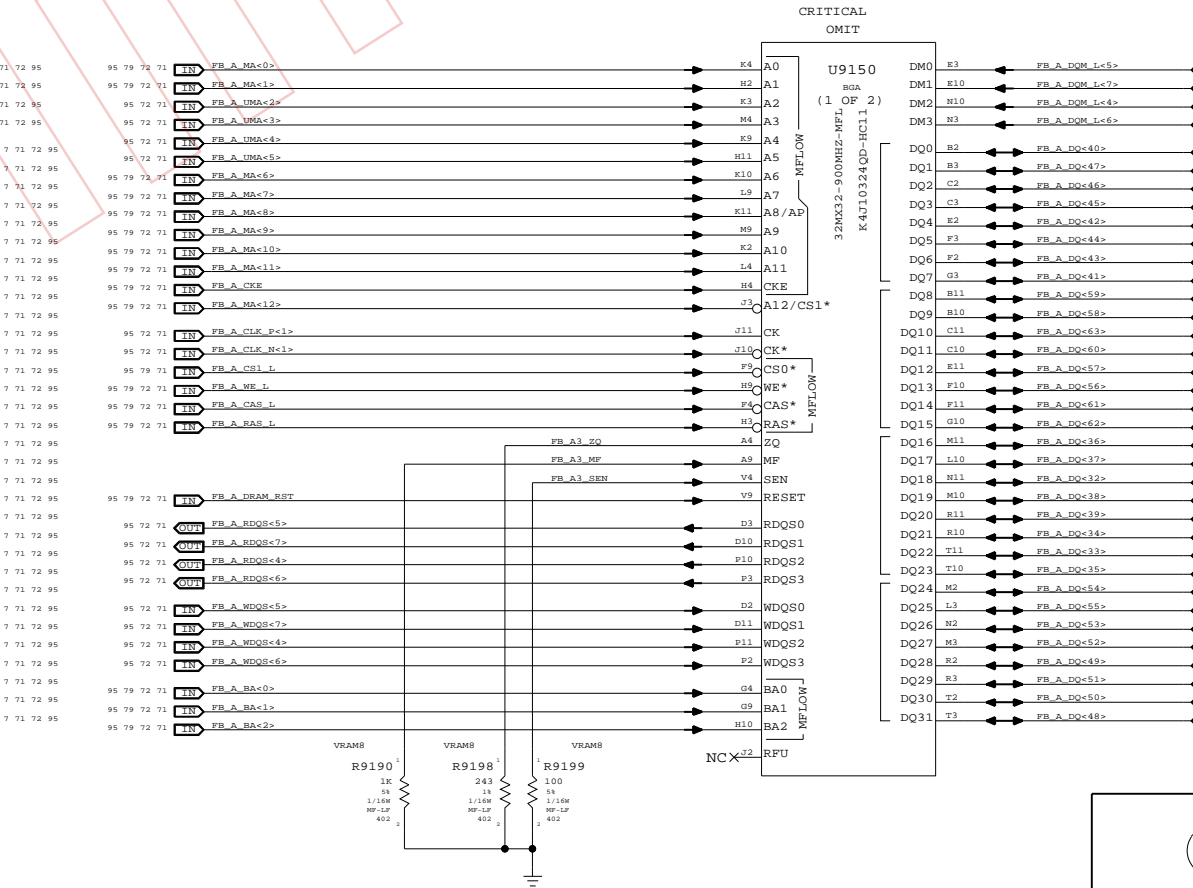
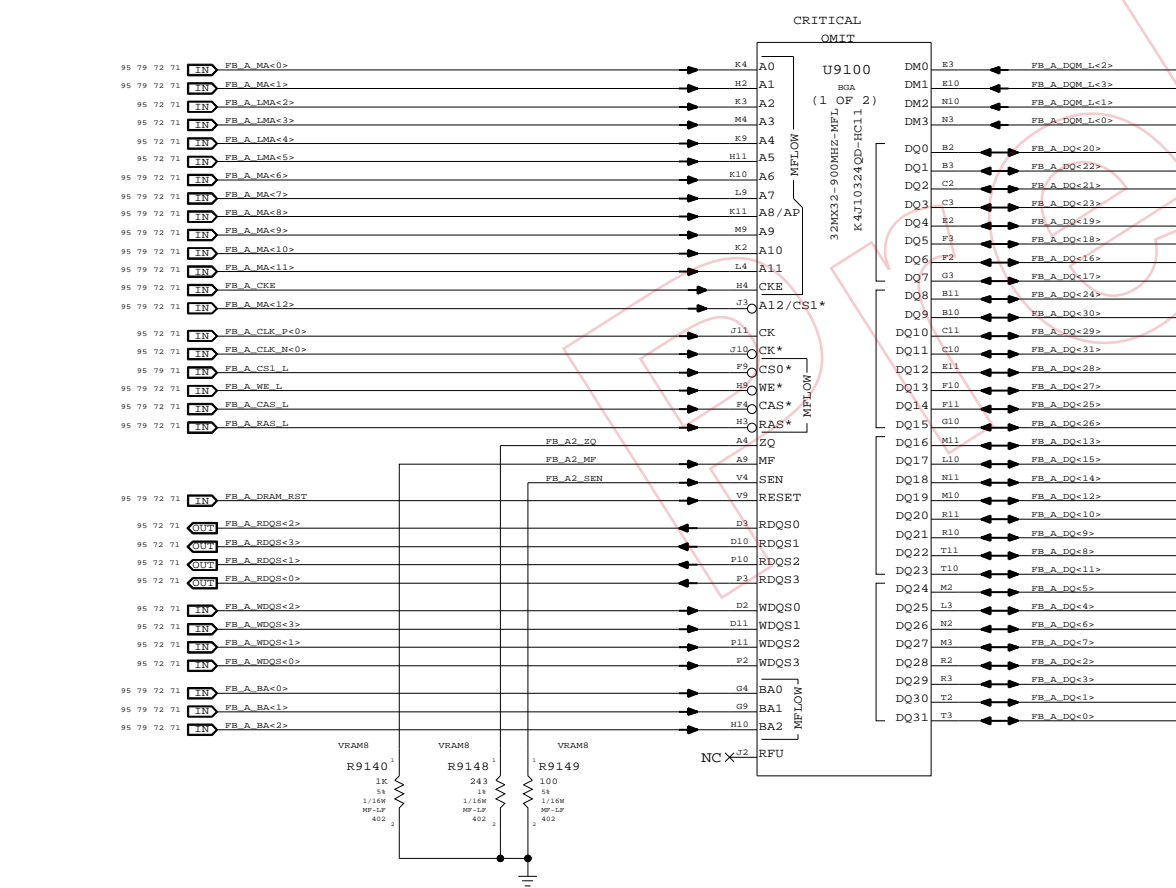
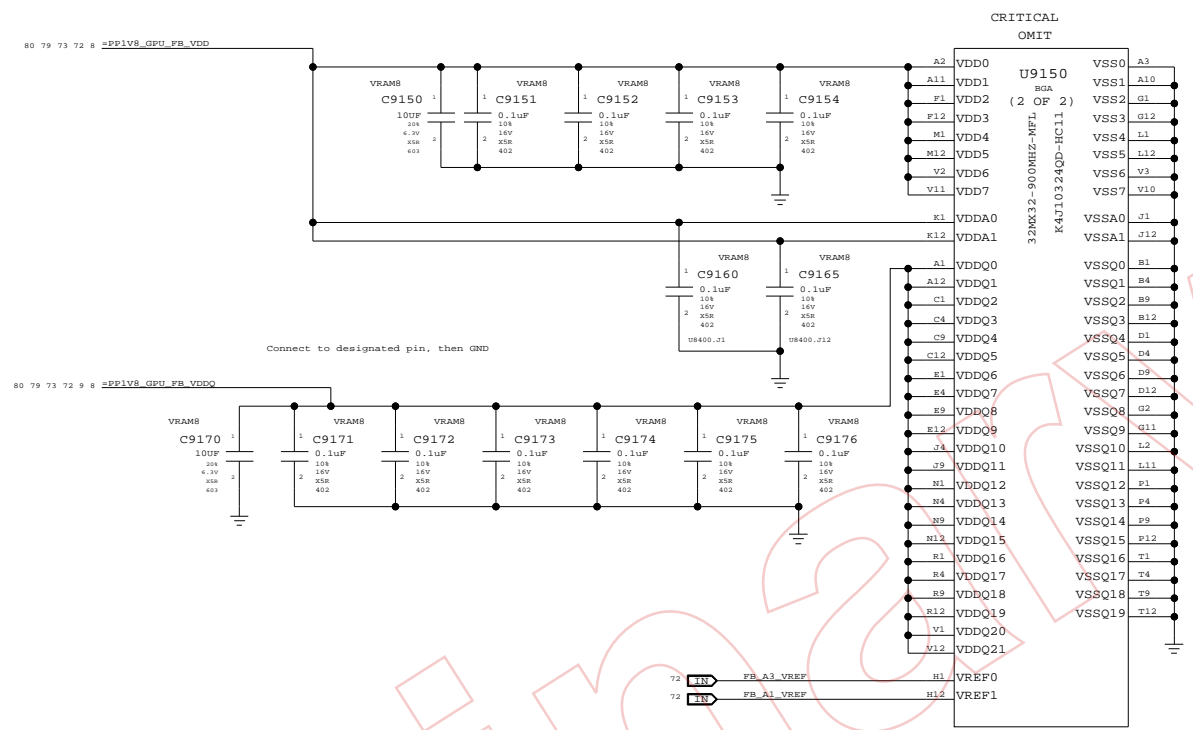
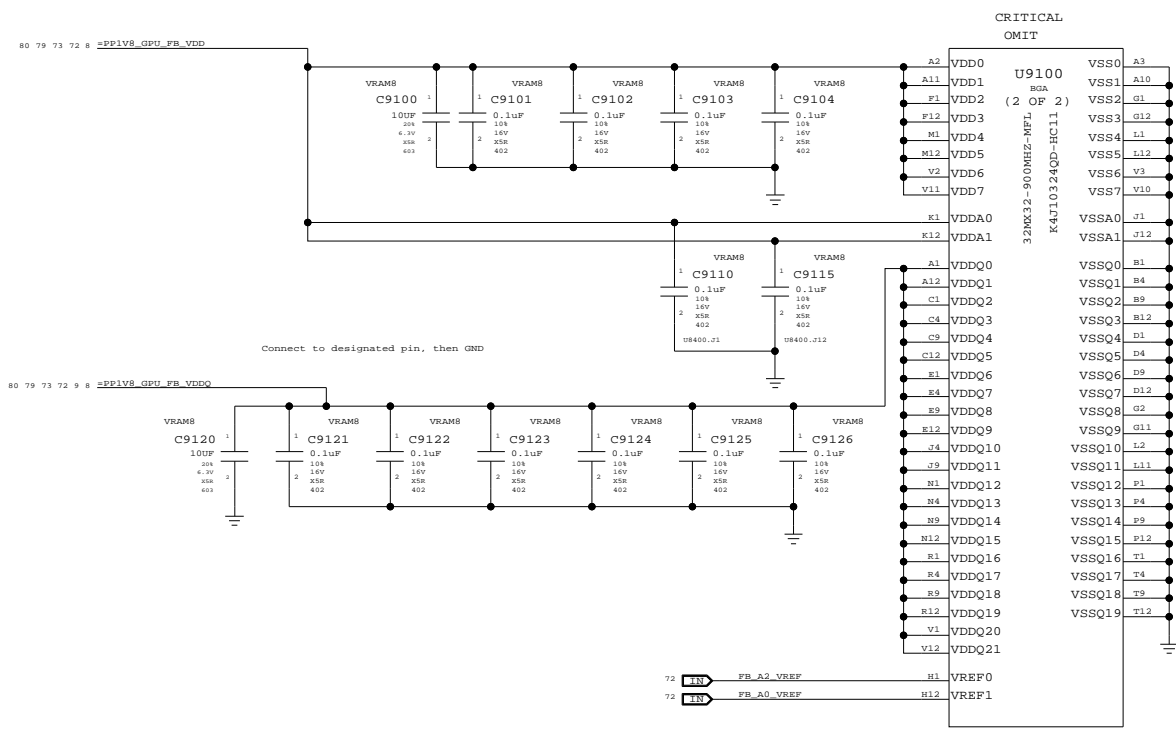
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHT 90	OF 123

Power aliases required by this page:
 - =PFI18_S0_FB_VDD
 - =PFI18_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 VRAMB



GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M99_MLS SYNC_DATE=04/04/2008

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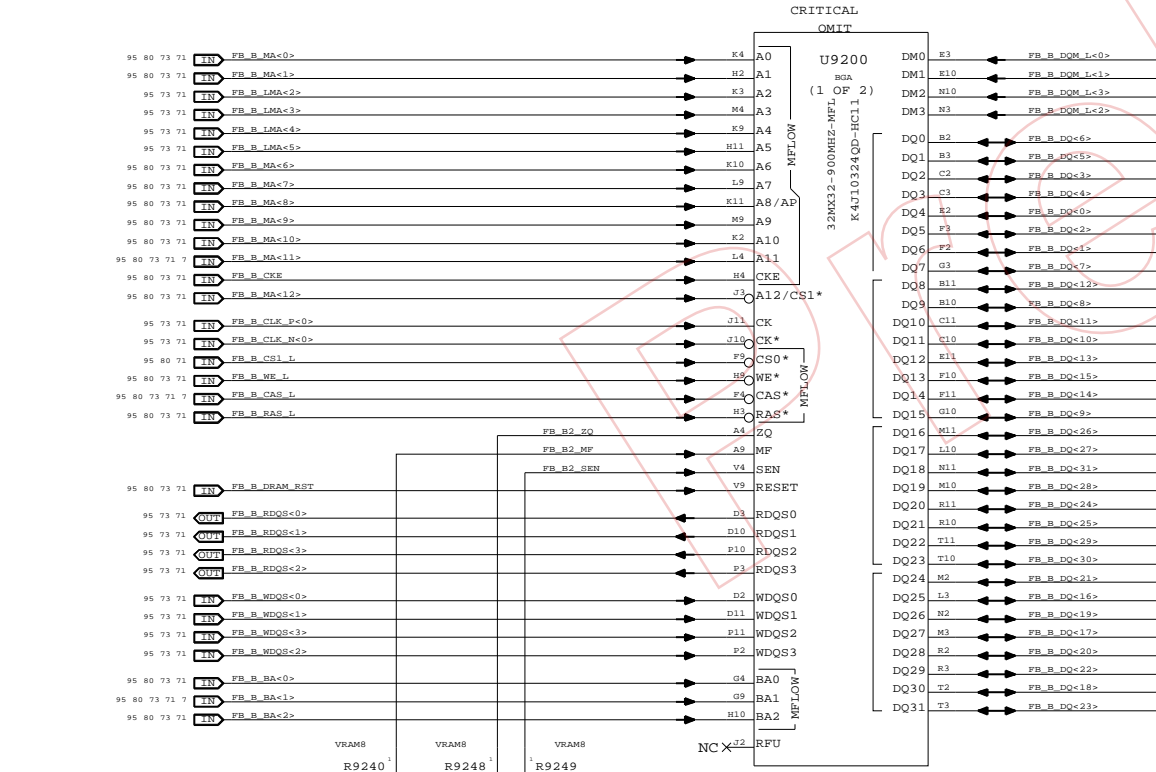
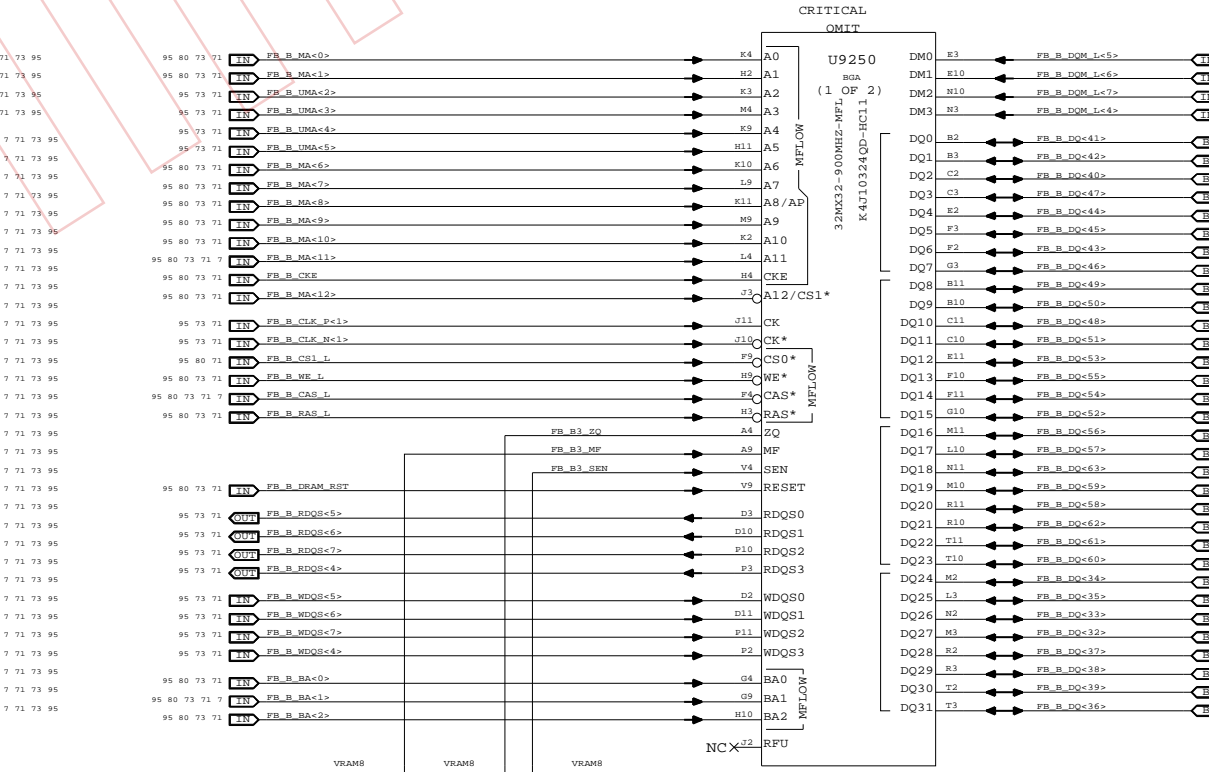
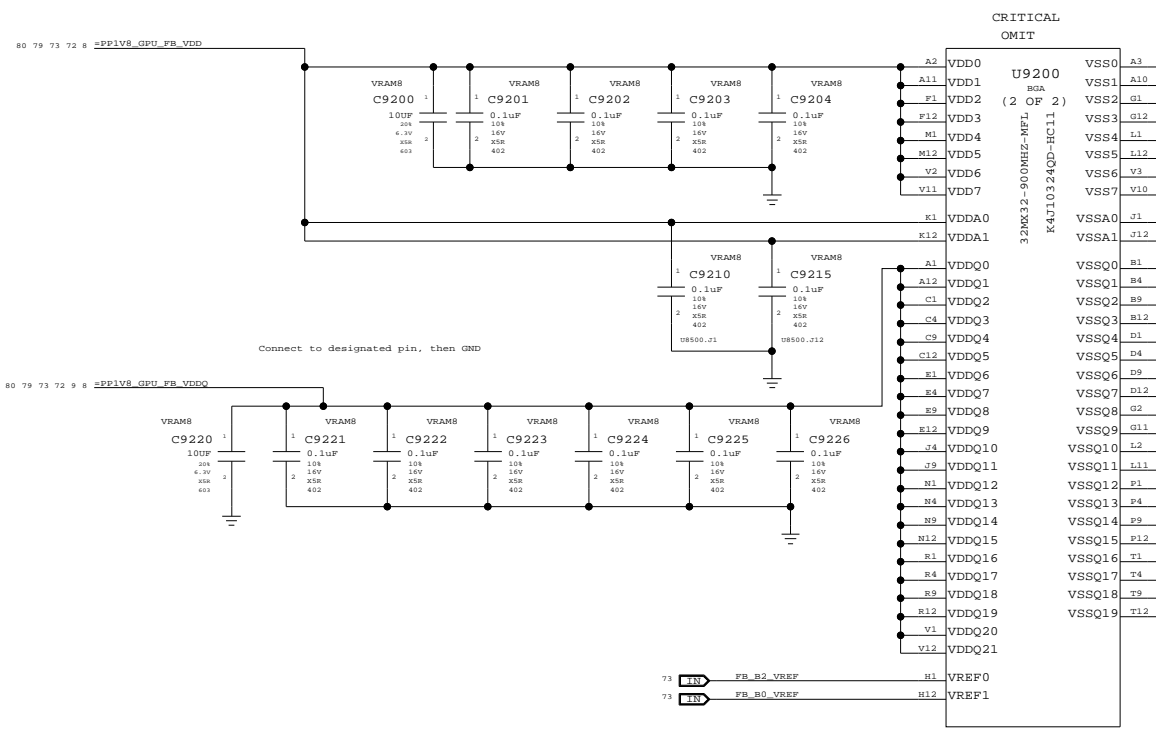
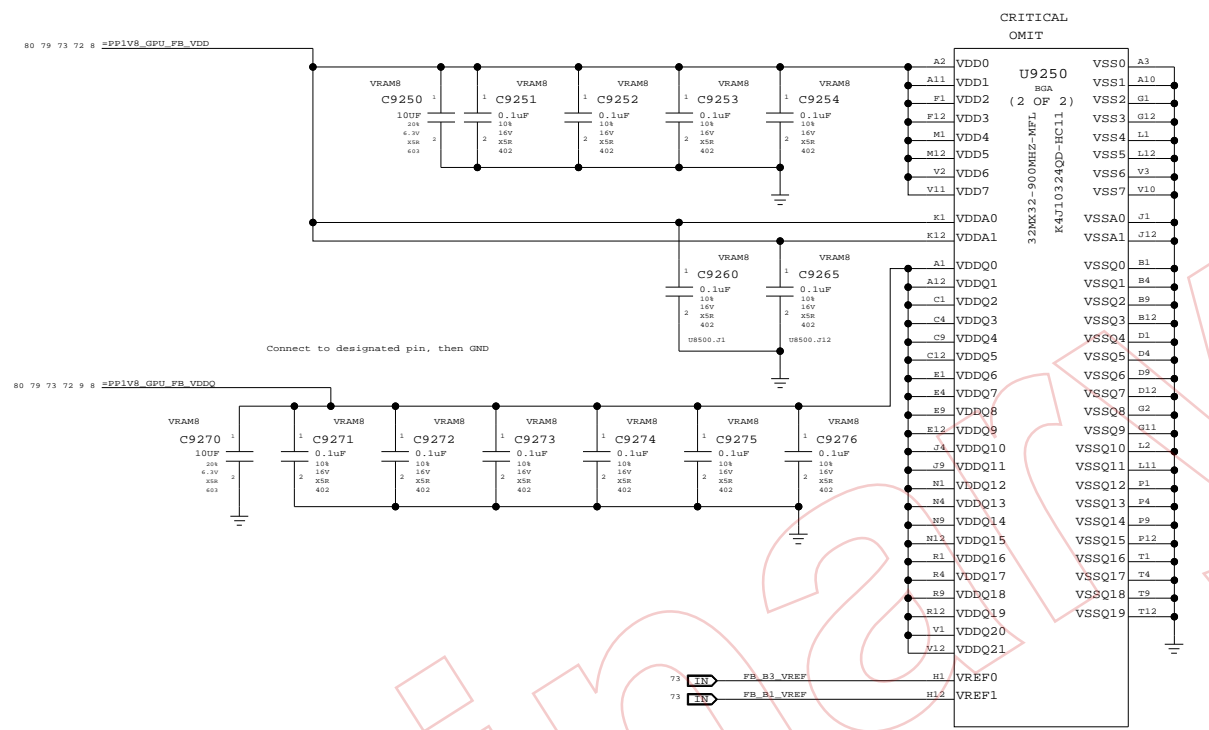


SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	91	123

Power aliases required by this page:
 - =PFI18_S0_FB_VDDQ
 - =PFI18_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 VRAMB



GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M8B_MLS SYNC_DATE=11/01/2007

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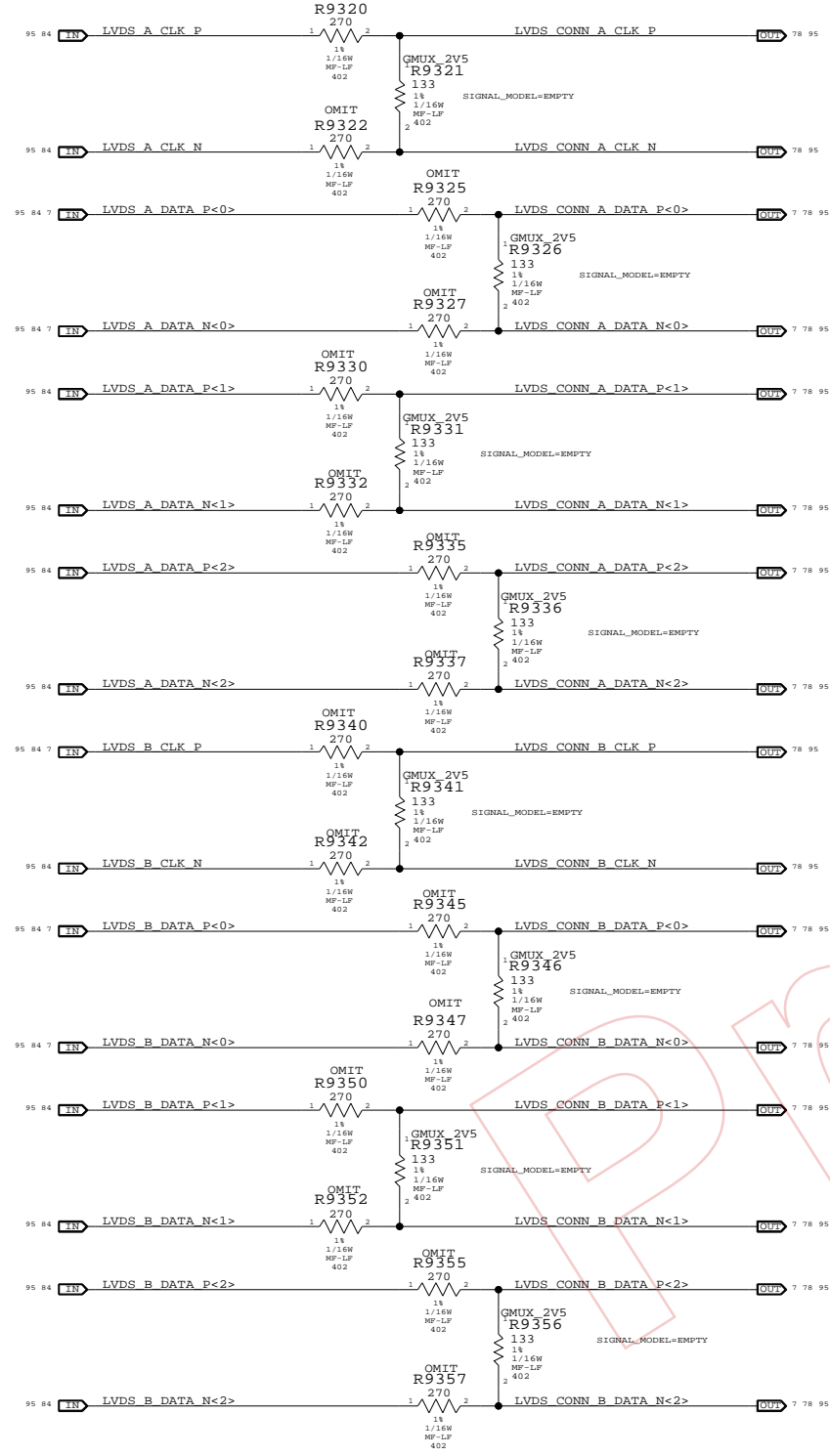
SCALE	DRAWING NUMBER		REV.
	051-7656		
NONE	SHT	OF	123



APPLE INC.

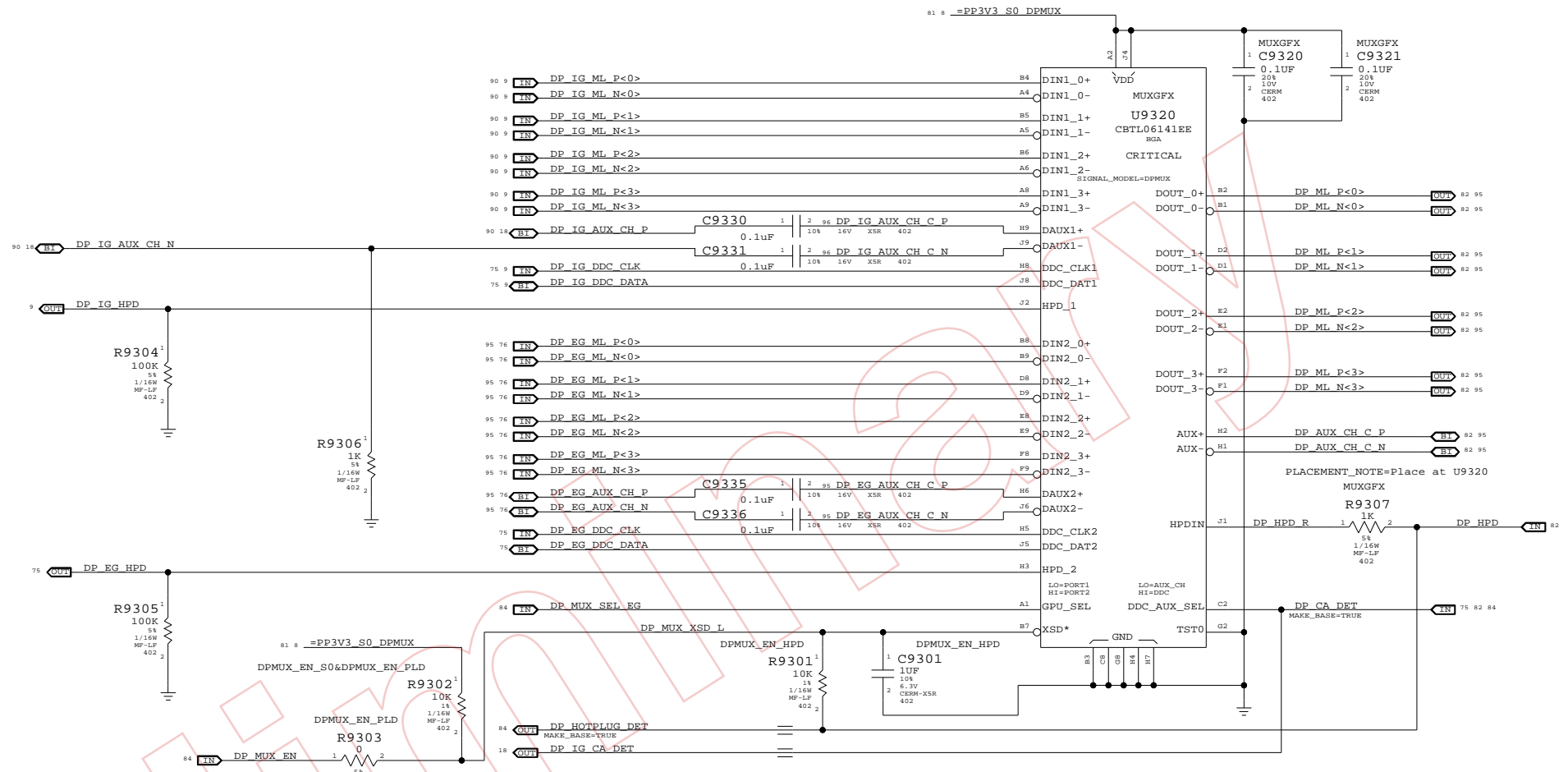
LVDS Transmitter Termination

All emulated LVDS outputs require this termination
PLACEMENT NOTE=Place at U9600 (All 24 resistors)

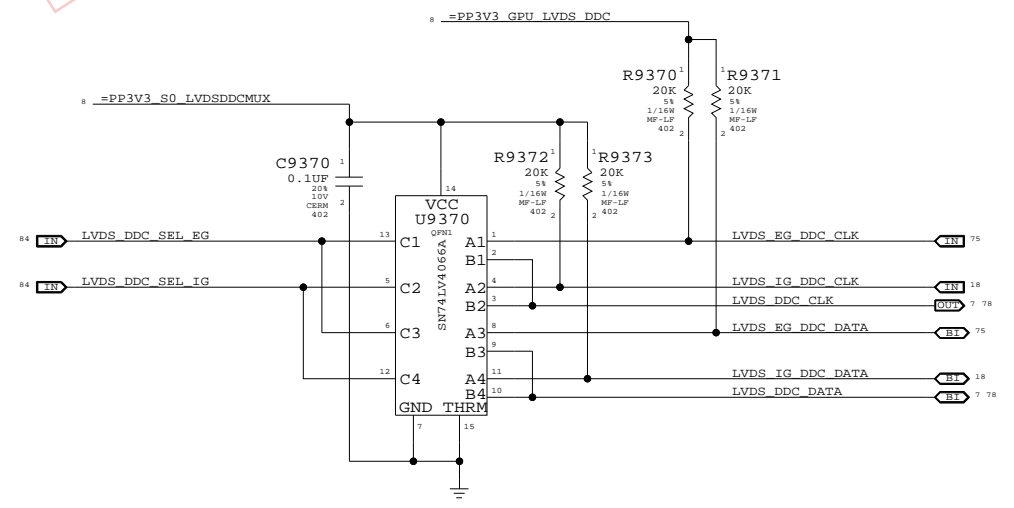


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
1148017	16	RES_MTX_P124_270 09M_14_1/16W_402_0D_1	R9320-R9332		GMUX_2V5
11480174	16	RES_MTX_P124_270 09M_14_1/16W_402_0D_1	R9333-R9357		GMUX_1V8

DisplayPort Mux

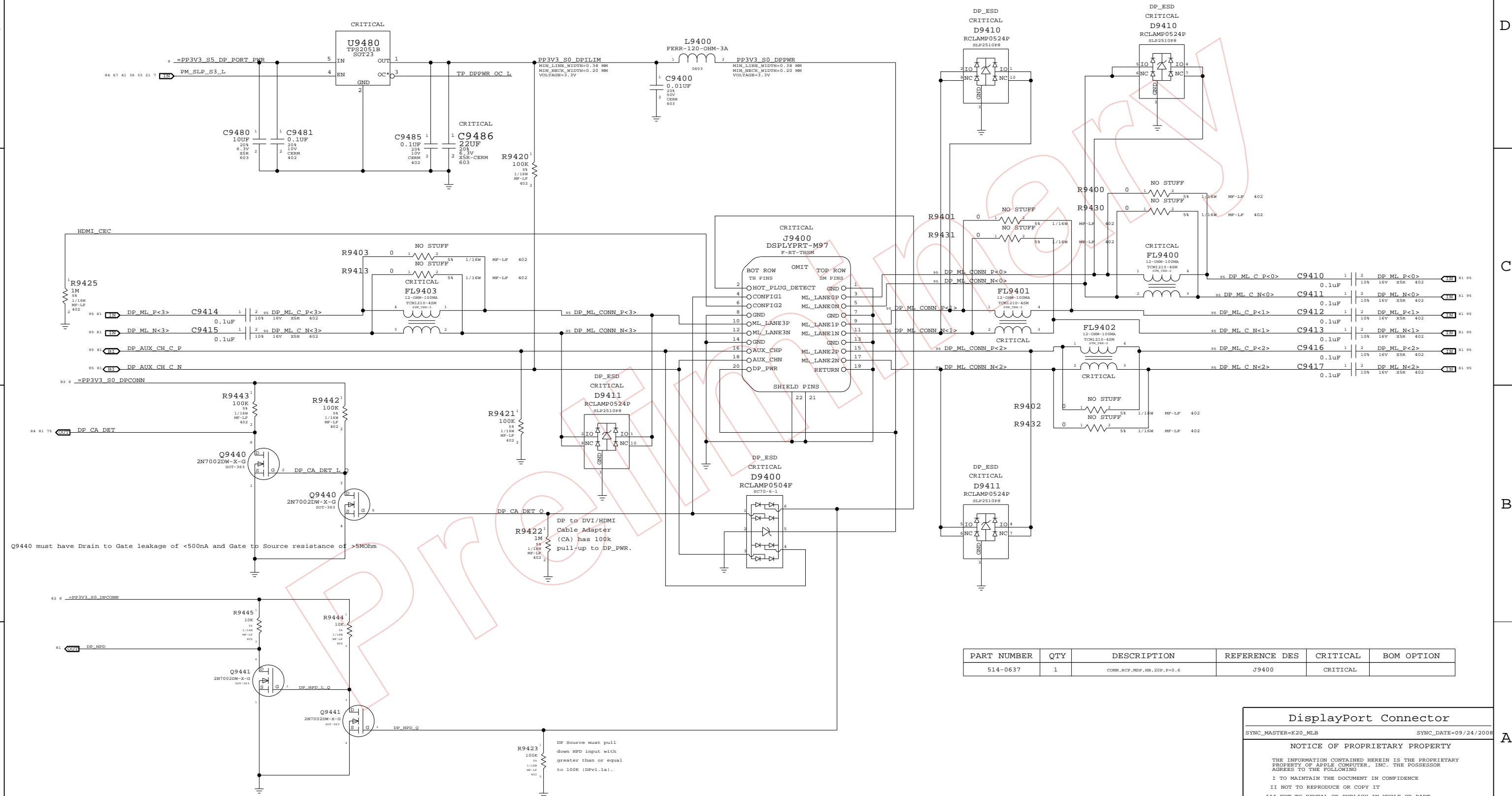


LVDS DDC MUX



Muxed Graphics Support
 SYNC_MASTER=M98_MLB SYNC_DATE=05/01/2008
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Port Power Switch



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0637	1	CONN, RCP, MDP, HS, ZDP, P=0.6	J9400	CRITICAL	

DisplayPort Connector

SYNC_MASTER=K20_MLB SYNC_DATE=09/24/2008

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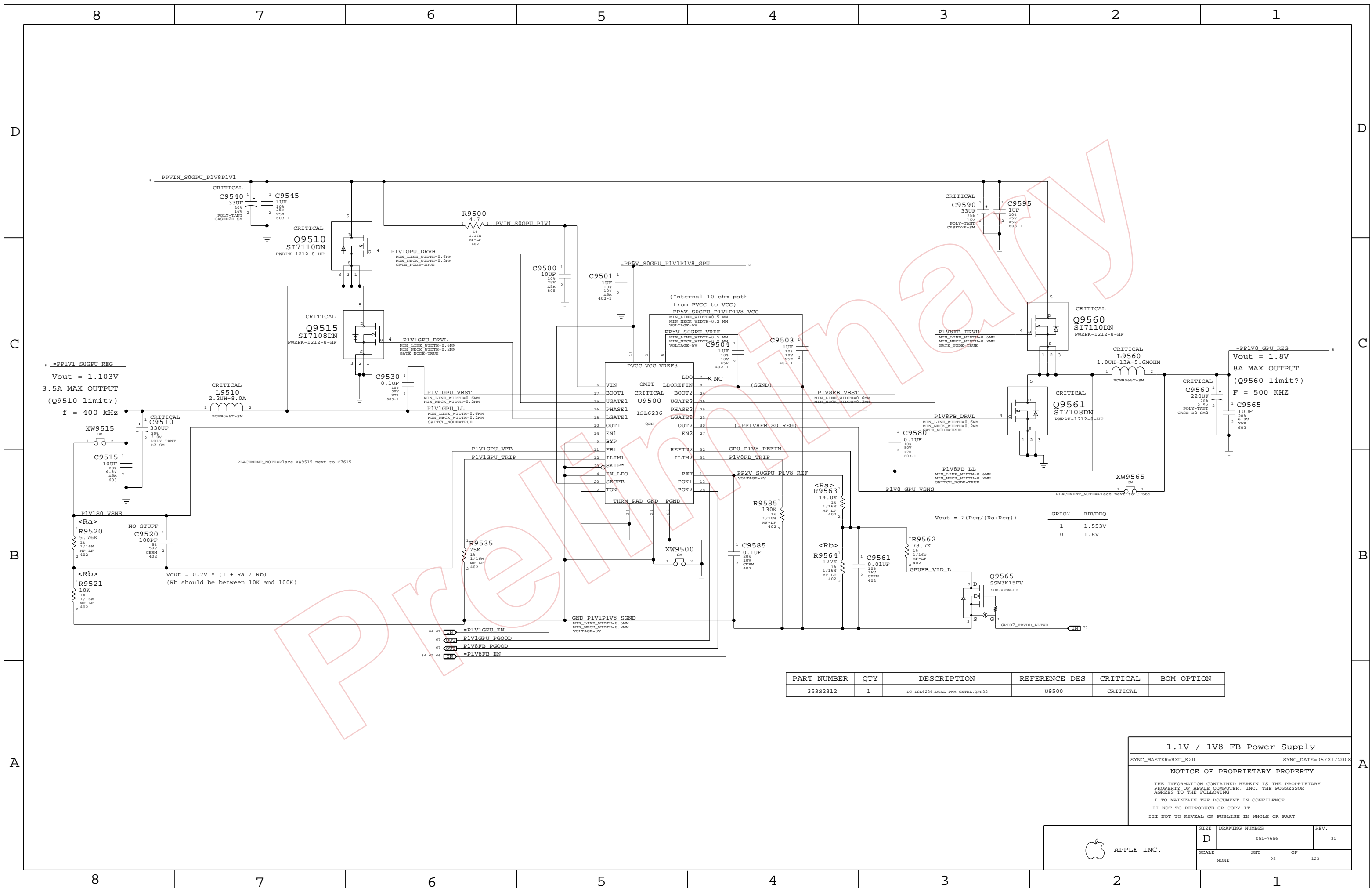
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	123
NONE	94		

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MΩhm

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

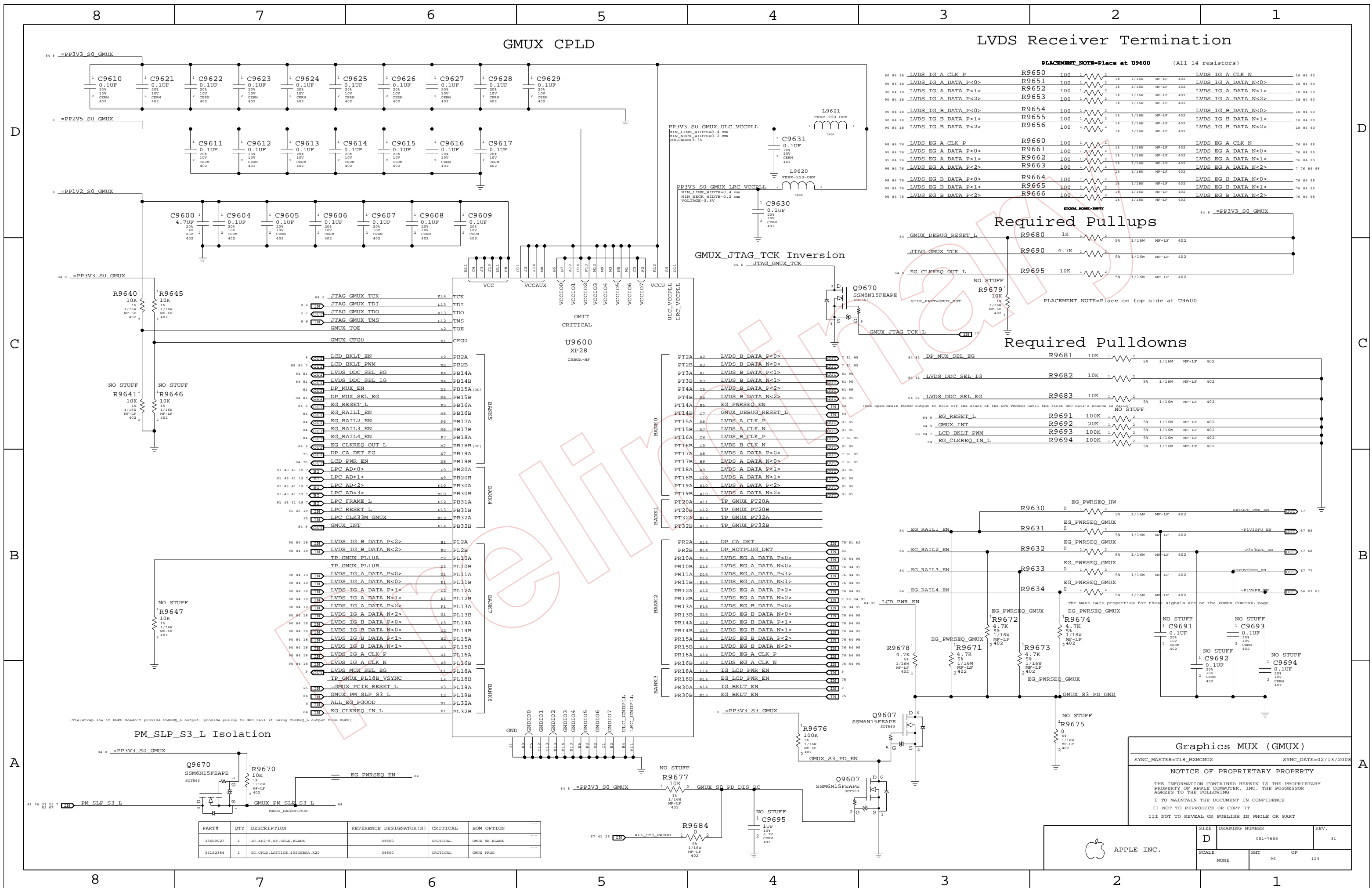
DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC, ISL6236, DUAL PWM CNTRL, QFN32	U9500	CRITICAL	

1.1V / 1V8 FB Power Supply
 SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	NONE	SHT	OF 123
		95	



GMUX CPLD

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9600 (All 14 resistors)

Required Pullups

Required Pulldowns

PM_SLP_S3_L Isolation

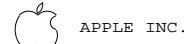
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
3360027	1	IC, XP2-8, HF, CPLD, BLANK	U9600	CRITICAL	GMUX_BK_BLANK
34182354	1	IC, CPLD, LATTICE, 132CSBGA, K20	U9600	CRITICAL	GMUX_PROD

Graphics MUX (GMUX)

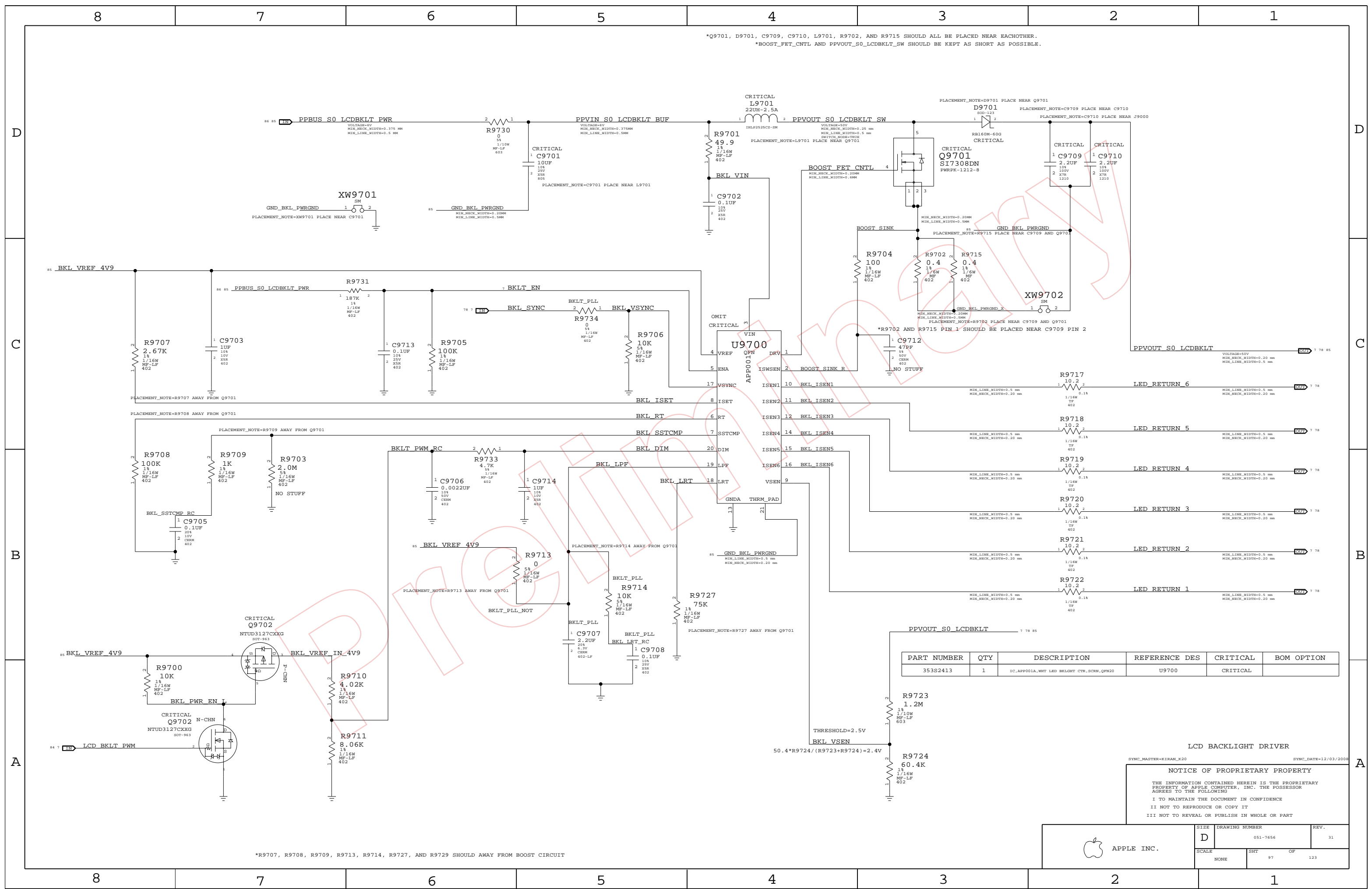
SYNC_MASTER=T18_MXMGMUX SYNC_DATE=02/13/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	96	123



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2413	1	IC.APP001A, WHT LED BKLGHT CTR, SCRN.OPN20	U9700	CRITICAL	

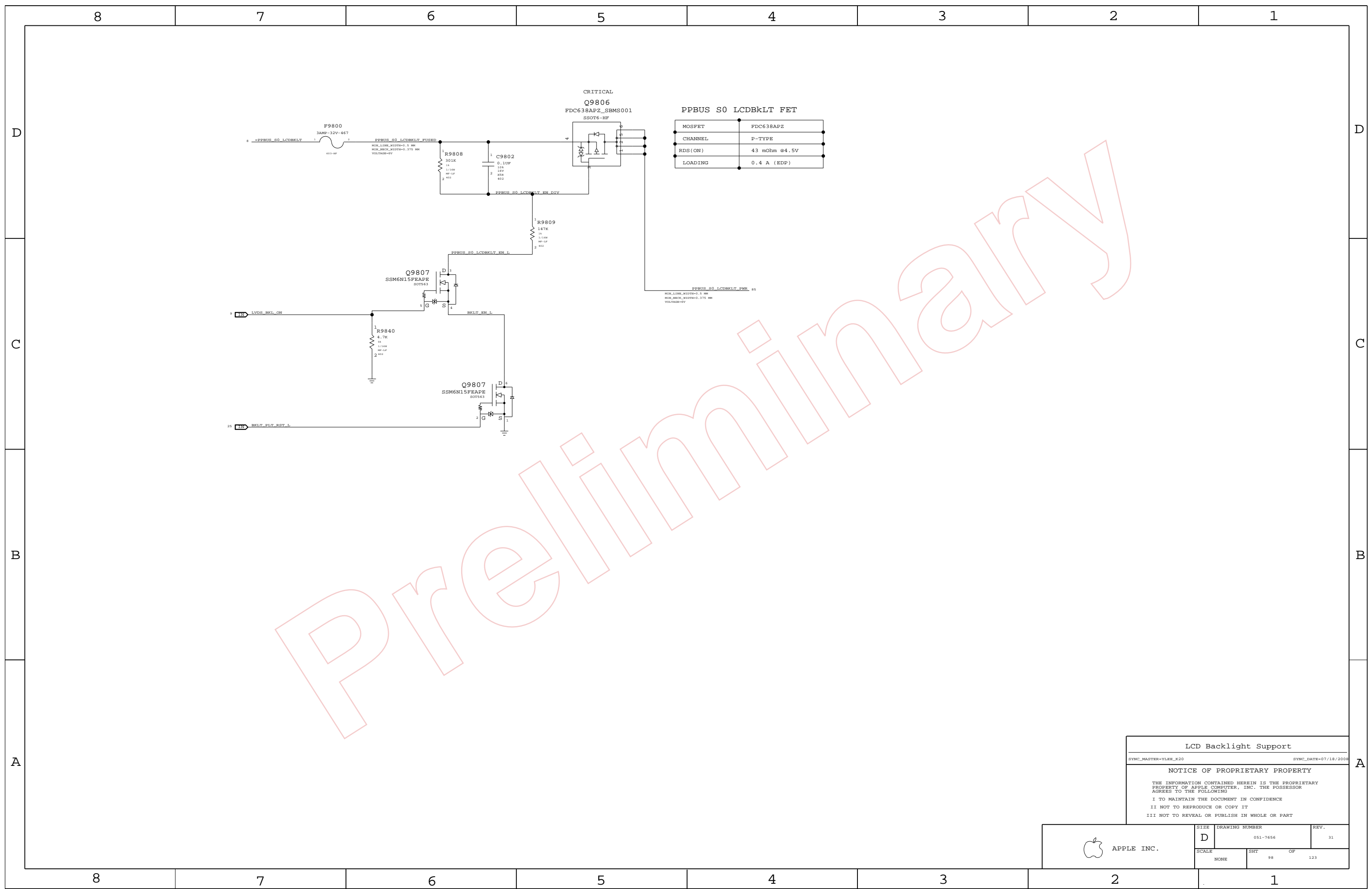
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	D	051-7656	31
SCALE	SHT	OF	123
NONE	97		

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

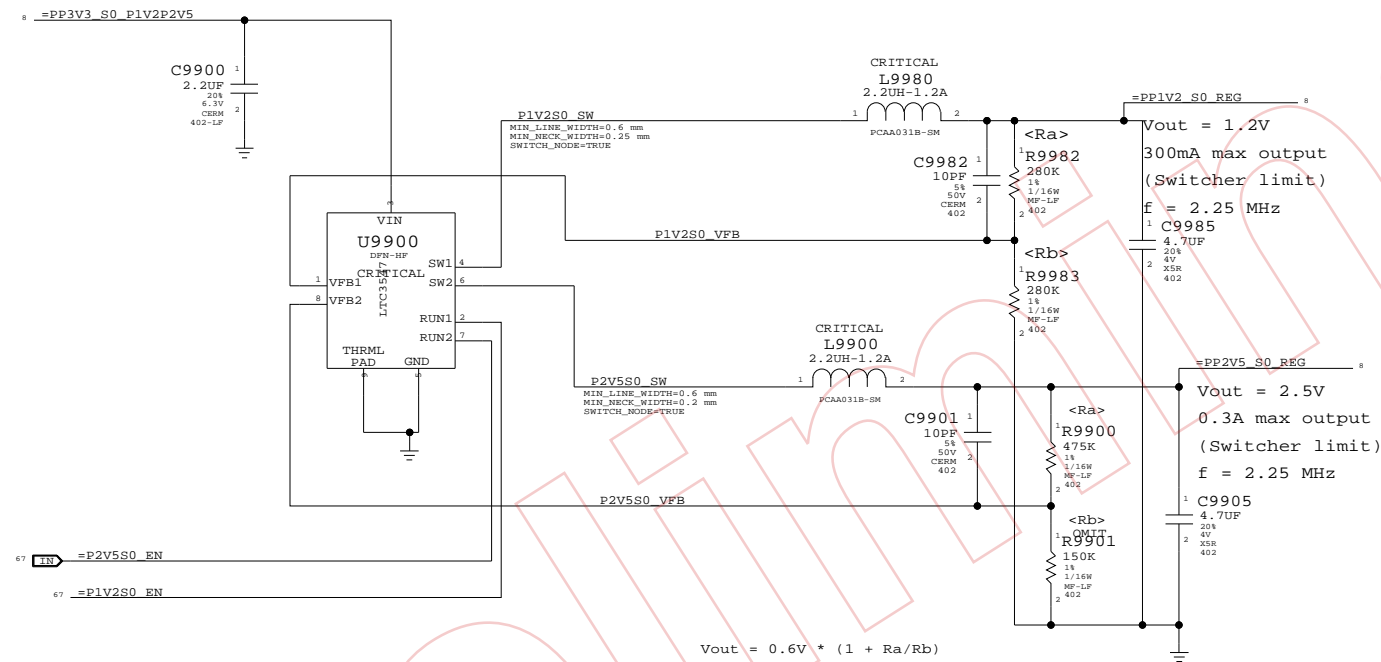


Preliminary

LCD Backlight Support
 SYNC_MASTER=VLEE_K20 SYNC_DATE=07/18/2008
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	SIZE	DRAWING NUMBER	REV.
	D	051-7656	31
SCALE	SHT	OF	
NONE	98	123	

GMUX 1.8V/1.2V S0 Switcher



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11450428	1	RES_MTL_FILM,1/16W,150K,1,0402,SMD,LF	R9901		GMUX_V5
11450447	1	RES_MTL_FILM,1/16W,237K,1,0402,SMD,LF	R9901		GMUX_V8

Misc Power Supplies

SYNC_MASTER=RXU_K20 SYNC_DATE=05/07/2008

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	SIZE D	DRAWING NUMBER 051-7656	REV. 31
	SCALE NONE	SHT 99	OF 123

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
 Signals within each 4x group should be matched within 5 ps of strobe.
 DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
 Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
 DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
 Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
 Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
 Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
 Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
 SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
 Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
 SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB ADSTB L<1>	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	7 10 14
FSB_BREQ0	FSB_50S	FSB_1X	FSB BREQ0 L	9 10 14
FSB_BREQ1	FSB_50S	FSB_1X	FSB BREQ1 L	14
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB BPR L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	7 10 14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	7 10 14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	9 10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB BS L<2..0>	10 14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR_L	CPU_50S	CPU_BMI	CPU FERR L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGARNE L	10 14
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 10 14
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10 14 42 61
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPECLK L	10 14
PM_THERMTRIP_L	CPU_50S	CPU_BMI	PM_THERMTRIP L	10 14 42
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB CPURST L	10 14
CPU_PDRSR	CPU_50S	CPU_AGTL	CPU_DPSLP L	10 14
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9 10 14 61
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10 14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR_L	CPU_50S		CPU IERR L	10
PM_DPSLPVPR	CPU_50S	CPU_AGTL	PM_DPSLPVPR	21 61
(See above)	CPU_50S	CPU_AGTL	IMVP6 DPSLPVPR	61
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 26
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6 10 13
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6 10
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6 10 13
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6 10 13
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	6 10 13
XDP_BPM_1	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_15	CPU_50S	CPU_ITP	XDP BPM L<5>	10 13
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	13
	CPU_50S	CPU_BMI	CPU VID<6..0>	9 11
	CPU_50S	CPU_BMI	IMVP6 VID<6..0>	9 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN P	61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN N	61

CPU/FSB Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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APPLE INC.	SCALE	DRAWING NUMBER	REV.
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	SHT	OF	
	100	123	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_DATA	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM*-style wildcards!

DDR2:
 DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK P<5..0>
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK N<5..0>
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS L<3..0>
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A A<14..0>
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A BA<2..0>
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A RAS L
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A CAS L
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A WE L
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A DQ<63..56>
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A DM<0>
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A DM<1>
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A DM<2>
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A DM<3>
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A DM<4>
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A DM<5>
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A DM<6>
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A DM<7>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A DQS P<0>
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A DQS N<0>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A DQS P<1>
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A DQS N<1>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A DQS P<2>
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A DQS N<2>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A DQS P<3>
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A DQS N<3>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A DQS P<4>
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A DQS N<4>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A DQS P<5>
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A DQS N<5>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A DQS P<6>
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A DQS N<6>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A DQS P<7>
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A DQS N<7>
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK P<5..0>
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK N<5..0>
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS L<3..0>
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B A<14..0>
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B BA<2..0>
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B RAS L
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B CAS L
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B WE L
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B DQ<63..56>
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B DM<0>
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B DM<1>
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B DM<2>
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B DM<3>
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B DM<4>
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B DM<5>
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B DM<6>
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B DM<7>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B DQS P<0>
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B DQS N<0>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B DQS P<1>
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B DQS N<1>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B DQS P<2>
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B DQS N<2>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B DQS P<3>
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B DQS N<3>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B DQS P<4>
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B DQS N<4>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B DQS P<5>
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B DQS N<5>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B DQS P<6>
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B DQS N<6>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B DQS P<7>
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B DQS N<7>
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND

Memory Constraints

SYNC_MASTER=M98_MLB SYNC_DATE=04/01/2008

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	*	=3X_DIELECTRIC	?
CLK_PCI_E	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PEG_R2D_P<15..0>	PCI_E_90D	PCI_E	9 69
PEG_R2D_N<15..0>	PCI_E_90D	PCI_E	9 69
PEG_R2D_C_P<15..0>	PCI_E_90D	PCI_E	9 69
PEG_R2D_C_N<15..0>	PCI_E_90D	PCI_E	9 69
PEG_D2R_P<15..0>	PCI_E_90D	PCI_E	9 69
PEG_D2R_N<15..0>	PCI_E_90D	PCI_E	9 69
PEG_D2R_C_P<15..0>	PCI_E_90D	PCI_E	9 69
PEG_D2R_C_N<15..0>	PCI_E_90D	PCI_E	9 69
PCI_E_MINI_R2D_P	PCI_E_90D	PCI_E	7 30
PCI_E_MINI_R2D_N	PCI_E_90D	PCI_E	7 30
PCI_E_MINI_R2D_C_P	PCI_E_90D	PCI_E	7 30
PCI_E_MINI_R2D_C_N	PCI_E_90D	PCI_E	7 30
PCI_E_MINI_D2R_P	PCI_E_90D	PCI_E	7 17 30
PCI_E_MINI_D2R_N	PCI_E_90D	PCI_E	7 17 30
PCI_E_FW_R2D_P	PCI_E_90D	PCI_E	35
PCI_E_FW_R2D_N	PCI_E_90D	PCI_E	35
PCI_E_FW_R2D_C_P	PCI_E_90D	PCI_E	17 35
PCI_E_FW_R2D_C_N	PCI_E_90D	PCI_E	17 35
PCI_E_FW_D2R_P	PCI_E_90D	PCI_E	17 35
PCI_E_FW_D2R_N	PCI_E_90D	PCI_E	17 35
PCI_E_FW_D2R_C_P	PCI_E_90D	PCI_E	35
PCI_E_FW_D2R_C_N	PCI_E_90D	PCI_E	35
PCI_E_EXCARD_R2D_P	PCI_E_90D	PCI_E	7 31
PCI_E_EXCARD_R2D_N	PCI_E_90D	PCI_E	7 31
PCI_E_EXCARD_R2D_C_P	PCI_E_90D	PCI_E	17 31
PCI_E_EXCARD_R2D_C_N	PCI_E_90D	PCI_E	17 31
PCI_E_EXCARD_D2R_P	PCI_E_90D	PCI_E	7 17 31
PCI_E_EXCARD_D2R_N	PCI_E_90D	PCI_E	7 17 31
PEG_CLK100M_P	CLK_PCI_E_100D	CLK_PCI_E	17 69
PEG_CLK100M_N	CLK_PCI_E_100D	CLK_PCI_E	17 69
PCI_E_CLK100M_MINI_P	CLK_PCI_E_100D	CLK_PCI_E	17 30
PCI_E_CLK100M_MINI_N	CLK_PCI_E_100D	CLK_PCI_E	17 30
PCI_E_CLK100M_FW_P	CLK_PCI_E_100D	CLK_PCI_E	17 35
PCI_E_CLK100M_FW_N	CLK_PCI_E_100D	CLK_PCI_E	17 35
PCI_E_CLK100M_EXCARD_P	CLK_PCI_E_100D	CLK_PCI_E	17 31
PCI_E_CLK100M_EXCARD_N	CLK_PCI_E_100D	CLK_PCI_E	17 31
MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_COMP	17
CRT_IG_R_C_PR	CRT_50S	CRT	18 24
CRT_IG_G_Y_Y	CRT_50S	CRT	18 24
CRT_IG_B_COMP_PB	CRT_50S	CRT	18 24
CRT_IG_HSYNC	CRT_50S	CRT_SYNC	18 24
CRT_IG_VSYNC	CRT_50S	CRT_SYNC	18 24
MCP_DAC_RSET	MCP_DAC_COMP	MCP_DAC_COMP	18 24
MCP_TV_DAC_VREF	MCP_DAC_COMP	MCP_DAC_COMP	18 24
TMDS_IG_TXC_P	DP_100D	DISPLAYPORT	
TMDS_IG_TXC_N	DP_100D	DISPLAYPORT	
TMDS_IG_TXD_P<2..0>	DP_100D	DISPLAYPORT	
TMDS_IG_TXD_N<2..0>	DP_100D	DISPLAYPORT	
DP_IG_ML_P<3..0>	DP_100D	DISPLAYPORT	9 81
DP_IG_ML_N<3..0>	DP_100D	DISPLAYPORT	9 81
DP_IG_AUX_CH_P	DP_100D	DISPLAYPORT	18 81
DP_IG_AUX_CH_N	DP_100D	DISPLAYPORT	18 81
MCP_HDMI_RSET	MCP_DV_COMP	MCP_DV_COMP	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_DV_COMP	18 24
LVDS_IG_A_CLK_P	LVDS_100D	LVDS	18 84
LVDS_IG_A_CLK_N	LVDS_100D	LVDS	18 84
LVDS_IG_A_DATA_P<2..0>	LVDS_100D	LVDS	18 84
LVDS_IG_A_DATA_N<2..0>	LVDS_100D	LVDS	18 84
LVDS_IG_A_DATA_P<3>	LVDS_100D	LVDS	9 18
LVDS_IG_A_DATA_N<3>	LVDS_100D	LVDS	9 18
LVDS_IG_B_CLK_P	LVDS_100D	LVDS	9 18
LVDS_IG_B_CLK_N	LVDS_100D	LVDS	9 18
LVDS_IG_B_DATA_P<2..0>	LVDS_100D	LVDS	18 84
LVDS_IG_B_DATA_N<2..0>	LVDS_100D	LVDS	18 84
LVDS_IG_B_DATA_P<3>	LVDS_100D	LVDS	9 18
LVDS_IG_B_DATA_N<3>	LVDS_100D	LVDS	9 18
MCP_IFFAB_RSET	MCP_DV_COMP	MCP_DV_COMP	18 24
MCP_IFFAB_VPROBE	MCP_DV_COMP	MCP_DV_COMP	18 24
SATA_HDD_R2D_C_P	SATA_100D	SATA	20 38
SATA_HDD_R2D_C_N	SATA_100D	SATA	20 38
SATA_HDD_R2D_P	SATA_100D	SATA	7 38
SATA_HDD_R2D_N	SATA_100D	SATA	7 38
SATA_HDD_D2R_P	SATA_100D	SATA	20 38
SATA_HDD_D2R_N	SATA_100D	SATA	20 38
SATA_HDD_D2R_C_P	SATA_100D	SATA	7 38
SATA_HDD_D2R_C_N	SATA_100D	SATA	7 38
SATA_ODD_R2D_C_P	SATA_100D	SATA	20 38
SATA_ODD_R2D_C_N	SATA_100D	SATA	20 38
SATA_ODD_R2D_P	SATA_100D	SATA	7 38
SATA_ODD_R2D_N	SATA_100D	SATA	7 38
SATA_ODD_D2R_P	SATA_100D	SATA	20 38
SATA_ODD_D2R_N	SATA_100D	SATA	20 38
SATA_ODD_D2R_C_P	SATA_100D	SATA	7 38
SATA_ODD_D2R_C_N	SATA_100D	SATA	7 38
MCP_SATA_TERM	SATA_100D	SATA_TERM	20

MCP Constraints 1

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REV: 31

MCP RGMI (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	MIN_LENGTH	MAX_LENGTH
	PHYSICAL	SPACING			
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18	
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18	33
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	32	33
ENET_INTR_I	ENET_MII_55S	ENET_MII	ENET_INTR_L		
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18	32
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18	32
ENET_PWDWN_I	ENET_MII_55S	ENET_MII	ENET_PWDWN_L		
ENET_CLK125M_RXCLK_R	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	32	
ENET_CLK125M_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18	32
ENET_RXD<3..0>	ENET_MII_55S	ENET_MII	ENET_RXD<3..0>	32	
ENET_RXD<0>	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18	32
ENET_RXD<3..1>	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18	32
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18	32
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18	32
ENET_TXD<0>	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18	32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18	32
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18	32
ENET_RESET_L	ENET_MII_55S	ENET_MII	ENET_RESET_L	18	32
ENET_MDI_P<3..0>	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	32	34
ENET_MDI_N<3..0>	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	32	34

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Ethernet Constraints		
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NONE		104	123

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	COUNT
	PHYSICAL	SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	35 37
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	35 37
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	35 37
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	35 37
Port 2 Not Used				

Preliminary

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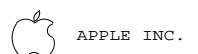
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FireWire Constraints

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NONE	105	123

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	SHEET
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 55G	SMB	SMBUS_SMC_A_S3_SCL	7 44
SMBUS_SMC_A_S3_SDA	SMB 55G	SMB	SMBUS_SMC_A_S3_SDA	7 44
SMBUS_SMC_B_S0_SCL	SMB 55G	SMB	SMBUS_SMC_B_S0_SCL	44
SMBUS_SMC_B_S0_SDA	SMB 55G	SMB	SMBUS_SMC_B_S0_SDA	44
SMBUS_SMC_O_S0_SCL	SMB 55G	SMB	SMBUS_SMC_O_S0_SCL	44
SMBUS_SMC_O_S0_SDA	SMB 55G	SMB	SMBUS_SMC_O_S0_SDA	44
SMBUS_SMC_BSA_SCL	SMB 55G	SMB	SMBUS_SMC_BSA_SCL	7 44
SMBUS_SMC_BSA_SDA	SMB 55G	SMB	SMBUS_SMC_BSA_SDA	7 44
SMBUS_SMC_MGMT_SCL	SMB 55G	SMB	SMBUS_SMC_MGMT_SCL	44
SMBUS_SMC_MGMT_SDA	SMB 55G	SMB	SMBUS_SMC_MGMT_SDA	44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	SHEET
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	60
			CHGR_CSI_N	60
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	60
			CHGR_CSO_N	60

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_L101_55S	*	+1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_L101_55S	*	+1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	+2:1_SPACING	?
THERM	*	+2:1_SPACING	?
AUDIO	*	+2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
FP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P20M
MEM_CMD	GND	*	GND_P20M
MEM_CTRL	GND	*	GND_P20M
MEM_DATA	GND	*	GND_P20M
MEM_DQS	GND	*	GND_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_40S_VDD	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_70D	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
MEM_70D_VDD	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
PCIE_90D	*	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
USB_90D	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_DV_COMP	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_MEM_COMP	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_M11_COMP	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_USB_BIAS	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_DV_COMP	*	OVERWRITE	OVERWRITE	0.25 MM	250 MIL	OVERWRITE	OVERWRITE
CFU_27F4S	BOTTOM	OVERWRITE	OVERWRITE	0.23 MM	100 MIL	OVERWRITE	OVERWRITE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	ISL4, ISL9	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE
MEM_40S_VDD	ISL3, ISL10	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE
MEM_70D	ISL4, ISL9	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE
MEM_70D_VDD	ISL3, ISL10	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

FLASH MEMORY BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FLASH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
ENETCONN_P<3..0>	ENETCONN_P<3..0>	ENETCONN_P<3..0>	34
ENETCONN_R<3..0>	ENETCONN_R<3..0>	ENETCONN_R<3..0>	34
SATA_QDD_R2D_UF_P	SATA_QDD_R2D_UF_P	SATA_QDD_R2D_UF_P	38
SATA_QDD_R2D_UF_N	SATA_QDD_R2D_UF_N	SATA_QDD_R2D_UF_N	38
SATA_QDD_D2R_UF_P	SATA_QDD_D2R_UF_P	SATA_QDD_D2R_UF_P	38
SATA_QDD_D2R_UF_N	SATA_QDD_D2R_UF_N	SATA_QDD_D2R_UF_N	38
SATA_HDD_R2D_UF_P	SATA_HDD_R2D_UF_P	SATA_HDD_R2D_UF_P	38
SATA_HDD_R2D_UF_N	SATA_HDD_R2D_UF_N	SATA_HDD_R2D_UF_N	38
SATA_HDD_D2R_UF_P	SATA_HDD_D2R_UF_P	SATA_HDD_D2R_UF_P	38
SATA_HDD_D2R_UF_N	SATA_HDD_D2R_UF_N	SATA_HDD_D2R_UF_N	38
MPCOREIHSN_P	MPCOREIHSN_P	MPCOREIHSN_P	46 64
MPCOREIHSN_N	MPCOREIHSN_N	MPCOREIHSN_N	46 64
CPUTHMENS_D2_P	CPUTHMENS_D2_P	CPUTHMENS_D2_P	47
CPUTHMENS_D2_N	CPUTHMENS_D2_N	CPUTHMENS_D2_N	47
CPU_THERMD_P	CPU_THERMD_P	CPU_THERMD_P	10 47
CPU_THERMD_N	CPU_THERMD_N	CPU_THERMD_N	10 47
GPUTHMENS_D_P	GPUTHMENS_D_P	GPUTHMENS_D_P	47
GPUTHMENS_D_N	GPUTHMENS_D_N	GPUTHMENS_D_N	47
GPU_TDIODE_P	GPU_TDIODE_P	GPU_TDIODE_P	47 75
GPU_TDIODE_N	GPU_TDIODE_N	GPU_TDIODE_N	47 75
MCP_THMENSN_P	MCP_THMENSN_P	MCP_THMENSN_P	47
MCP_THMENSN_N	MCP_THMENSN_N	MCP_THMENSN_N	47
MCP_THMENSN_P	MCP_THMENSN_P	MCP_THMENSN_P	47 75
MCP_THMENSN_N	MCP_THMENSN_N	MCP_THMENSN_N	47 75
MCP_THMENSN_P	MCP_THMENSN_P	MCP_THMENSN_P	21 47
MCP_THMENSN_N	MCP_THMENSN_N	MCP_THMENSN_N	21 47
IV05CPUISNS_R_P	IV05CPUISNS_R_P	IV05CPUISNS_R_P	46
IV05CPUISNS_R_N	IV05CPUISNS_R_N	IV05CPUISNS_R_N	46
DDRISNS_R_P	DDRISNS_R_P	DDRISNS_R_P	46
DDRISNS_R_N	DDRISNS_R_N	DDRISNS_R_N	46
GPUISENS_P	GPUISENS_P	GPUISENS_P	46
GPUISENS_N	GPUISENS_N	GPUISENS_N	46
IV05CPU_P	IV05CPU_P	IV05CPU_P	46 65
IV05CPU_N	IV05CPU_N	IV05CPU_N	46 65
DDRISNS_P	DDRISNS_P	DDRISNS_P	46
DDRISNS_N	DDRISNS_N	DDRISNS_N	46
PIV8GPU_P	PIV8GPU_P	PIV8GPU_P	46
PIV8GPU_N	PIV8GPU_N	PIV8GPU_N	46
ISNS_CPU_P	ISNS_CPU_P	ISNS_CPU_P	45
ISNS_CPU_N	ISNS_CPU_N	ISNS_CPU_N	45
GND	GND	GND	
PP3V3_5S	PP3V3_5S	PP3V3_5S	7 8
PP3V3_50	PP3V3_50	PP3V3_50	7 8 9
PP1V5_50	PP1V5_50	PP1V5_50	
PIV8GPUISNS_P	PIV8GPUISNS_P	PIV8GPUISNS_P	46
PIV8GPUISNS_N	PIV8GPUISNS_N	PIV8GPUISNS_N	46
PIV8GPUISNS_P	PIV8GPUISNS_P	PIV8GPUISNS_P	46
PIV8GPUISNS_N	PIV8GPUISNS_N	PIV8GPUISNS_N	46
NF_CLE_R	NF_CLE_R	NF_CLE_R	96
NF_ALE_R	NF_ALE_R	NF_ALE_R	96
NF_CEO_L_R	NF_CEO_L_R	NF_CEO_L_R	96
NF_CE1_L_R	NF_CE1_L_R	NF_CE1_L_R	96
NF_RE0_L_R	NF_RE0_L_R	NF_RE0_L_R	96
NF_WEO_L_R	NF_WEO_L_R	NF_WEO_L_R	96
NF_CLE_R	NF_CLE_R	NF_CLE_R	96
NF_ALE_R	NF_ALE_R	NF_ALE_R	96
NF_CEO_L	NF_CEO_L	NF_CEO_L	96
NF_CE1_L	NF_CE1_L	NF_CE1_L	96
NF_RE0_L	NF_RE0_L	NF_RE0_L	96
NF_WEO_L	NF_WEO_L	NF_WEO_L	96

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
CLK_PCIE_100D	CLK_PCIE_100D	CLK_PCIE	7 30
PCIE_CLK100M_MINI_CONN_P	PCIE_CLK100M_MINI_CONN_P	PCIE_CLK100M_MINI_CONN_P	7 30
PCIE_CLK100M_MINI_CONN_N	PCIE_CLK100M_MINI_CONN_N	PCIE_CLK100M_MINI_CONN_N	7 30
CHGR_CSI_R_P	CHGR_CSI_R_P	CHGR_CSI_R_P	60
CHGR_CSI_R_N	CHGR_CSI_R_N	CHGR_CSI_R_N	60
CHGR_CSO_R_P	CHGR_CSO_R_P	CHGR_CSO_R_P	45 60
CHGR_CSO_R_N	CHGR_CSO_R_N	CHGR_CSO_R_N	45 60
USB2_EXTA_MIXED_P	USB2_EXTA_MIXED_P	USB2_EXTA_MIXED_P	39
USB2_EXTA_MIXED_N	USB2_EXTA_MIXED_N	USB2_EXTA_MIXED_N	39
USB2_LT1_P	USB2_LT1_P	USB2_LT1_P	7 39
USB2_LT1_N	USB2_LT1_N	USB2_LT1_N	7 39
CONN_TPAD_USB_P	CONN_TPAD_USB_P	CONN_TPAD_USB_P	
CONN_TPAD_USB_N	CONN_TPAD_USB_N	CONN_TPAD_USB_N	
USB_CAMERA_CONN_P	USB_CAMERA_CONN_P	USB_CAMERA_CONN_P	7 30
USB_CAMERA_CONN_N	USB_CAMERA_CONN_N	USB_CAMERA_CONN_N	7 30
CONN_USB2_ST_P	CONN_USB2_ST_P	CONN_USB2_ST_P	7 30
CONN_USB2_ST_N	CONN_USB2_ST_N	CONN_USB2_ST_N	7 30
USB_LT2_P	USB_LT2_P	USB_LT2_P	7 39
USB_LT2_N	USB_LT2_N	USB_LT2_N	7 39
USB2_EXCARD_CONN_P	USB2_EXCARD_CONN_P	USB2_EXCARD_CONN_P	7 31
USB2_EXCARD_CONN_N	USB2_EXCARD_CONN_N	USB2_EXCARD_CONN_N	7 31
DP_IG_AUX_CH_C_P	DP_IG_AUX_CH_C_P	DP_IG_AUX_CH_C_P	81
DP_IG_AUX_CH_C_N	DP_IG_AUX_CH_C_N	DP_IG_AUX_CH_C_N	81
PCIE_CLK100M_FC_P	PCIE_CLK100M_FC_P	PCIE_CLK100M_FC_P	81
PCIE_CLK100M_FC_N	PCIE_CLK100M_FC_N	PCIE_CLK100M_FC_N	81
PCIE_FC_R2D_C_P	PCIE_FC_R2D_C_P	PCIE_FC_R2D_C_P	81
PCIE_FC_R2D_C_N	PCIE_FC_R2D_C_N	PCIE_FC_R2D_C_N	81
PCIE_FC_D2R_P	PCIE_FC_D2R_P	PCIE_FC_D2R_P	81
PCIE_FC_D2R_N	PCIE_FC_D2R_N	PCIE_FC_D2R_N	81
PCIE_FC_R2D_N	PCIE_FC_R2D_N	PCIE_FC_R2D_N	81
PCIE_CLK100M_EXCARD_CONN_N	PCIE_CLK100M_EXCARD_CONN_N	PCIE_CLK100M_EXCARD_CONN_N	7 31
PCIE_CLK100M_EXCARD_CONN_P	PCIE_CLK100M_EXCARD_CONN_P	PCIE_CLK100M_EXCARD_CONN_P	7 31
SPKRAMP_L1_OUT_P	SPKRAMP_L1_OUT_P	SPKRAMP_L1_OUT_P	7 56 57
SPKRAMP_L1_OUT_N	SPKRAMP_L1_OUT_N	SPKRAMP_L1_OUT_N	7 56 57
SPKRAMP_L2_OUT_P	SPKRAMP_L2_OUT_P	SPKRAMP_L2_OUT_P	7 56 57
SPKRAMP_L2_OUT_N	SPKRAMP_L2_OUT_N	SPKRAMP_L2_OUT_N	7 56 57
SPKRAMP_R1_OUT_P	SPKRAMP_R1_OUT_P	SPKRAMP_R1_OUT_P	7 56 57
SPKRAMP_R1_OUT_N	SPKRAMP_R1_OUT_N	SPKRAMP_R1_OUT_N	7 56 57
SPKRAMP_R2_OUT_P	SPKRAMP_R2_OUT_P	SPKRAMP_R2_OUT_P	7 56 57
SPKRAMP_R2_OUT_N	SPKRAMP_R2_OUT_N	SPKRAMP_R2_OUT_N	7 56 57
SPKRAMP_LFE_OUT_P	SPKRAMP_LFE_OUT_P	SPKRAMP_LFE_OUT_P	7 56 57
SPKRAMP_LFE_OUT_N	SPKRAMP_LFE_OUT_N	SPKRAMP_LFE_OUT_N	7 56 57
USB_EXTC_P	USB_EXTC_P	USB_EXTC_P	20 91 98
USB_EXTC_N	USB_EXTC_N	USB_EXTC_N	20 91 98
USB_LT3_P	USB_LT3_P	USB_LT3_P	7 98
USB_LT3_N	USB_LT3_N	USB_LT3_N	7 98

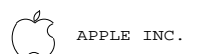
Project Specific Constraints

SYNC_MASTER=M99_MLS SYNC_DATE=04/01/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7656	31
SCALE	SHT	OF
NONE	108	123



M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MILS OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				ML, PFF, BGA				MM	16.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	+50_OHM_SE	+50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	-DEFAULT	-DEFAULT	10 MM	-DEFAULT	-DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
2704_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
2704_OHM_SE	*	Y	0.250 MM	0.250 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	-DEFAULT	?
BGA_P1MM	*	-DEFAULT	?
BGA_P2MM	*	-DEFAULT	?
BGA_P3MM	*	-DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:5:1_SPACING	*	0.15 MM	?
1:8:1_SPACING	*	0.18 MM	?
2:1:1_SPACING	*	0.2 MM	?
2:5:1_SPACING	*	0.25 MM	?
3:1:1_SPACING	*	0.3 MM	?
4:1:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FBP_D0TB	FBP_D0TB	BGA	BGA_P3MM

NOTE: From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	-STANDARD	-STANDARD	-STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M98_MLS SYNC_DATE=04/01/2008


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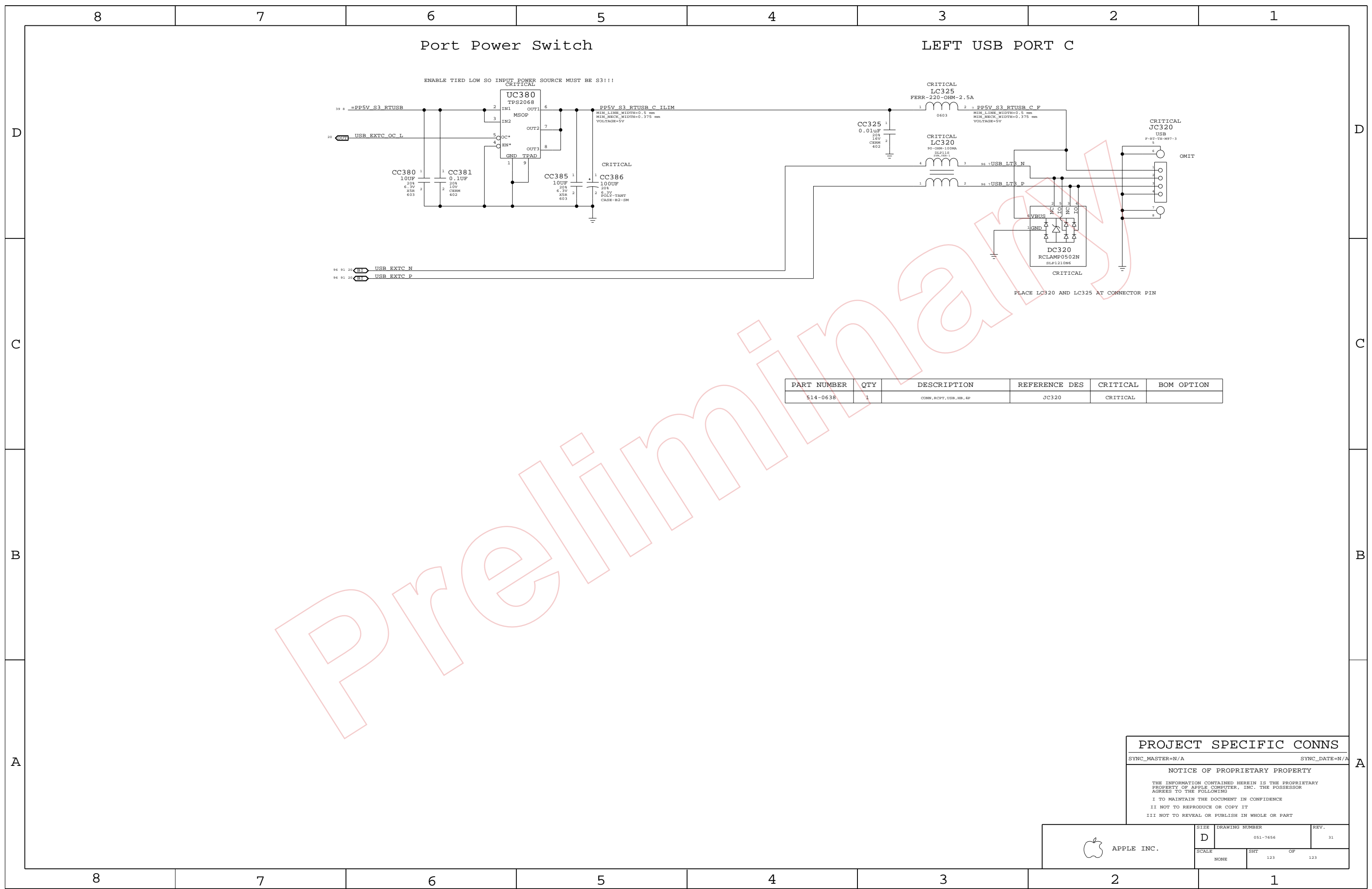
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SCALE	SHT	OF	
NONE	109	123	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-0638	1	CONN, RCPT, USB, HB, 4P	JC320	CRITICAL	

PROJECT SPECIFIC CONNS

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF	
NONE	123	123	