

# Compal Confidential

Model Name : EA/EG50\_CX (Z5WE1)

File Name : LA-9535P

# Compal Confidential

## EA/EG50\_CX (Z5WE1) M/B Schematics Document

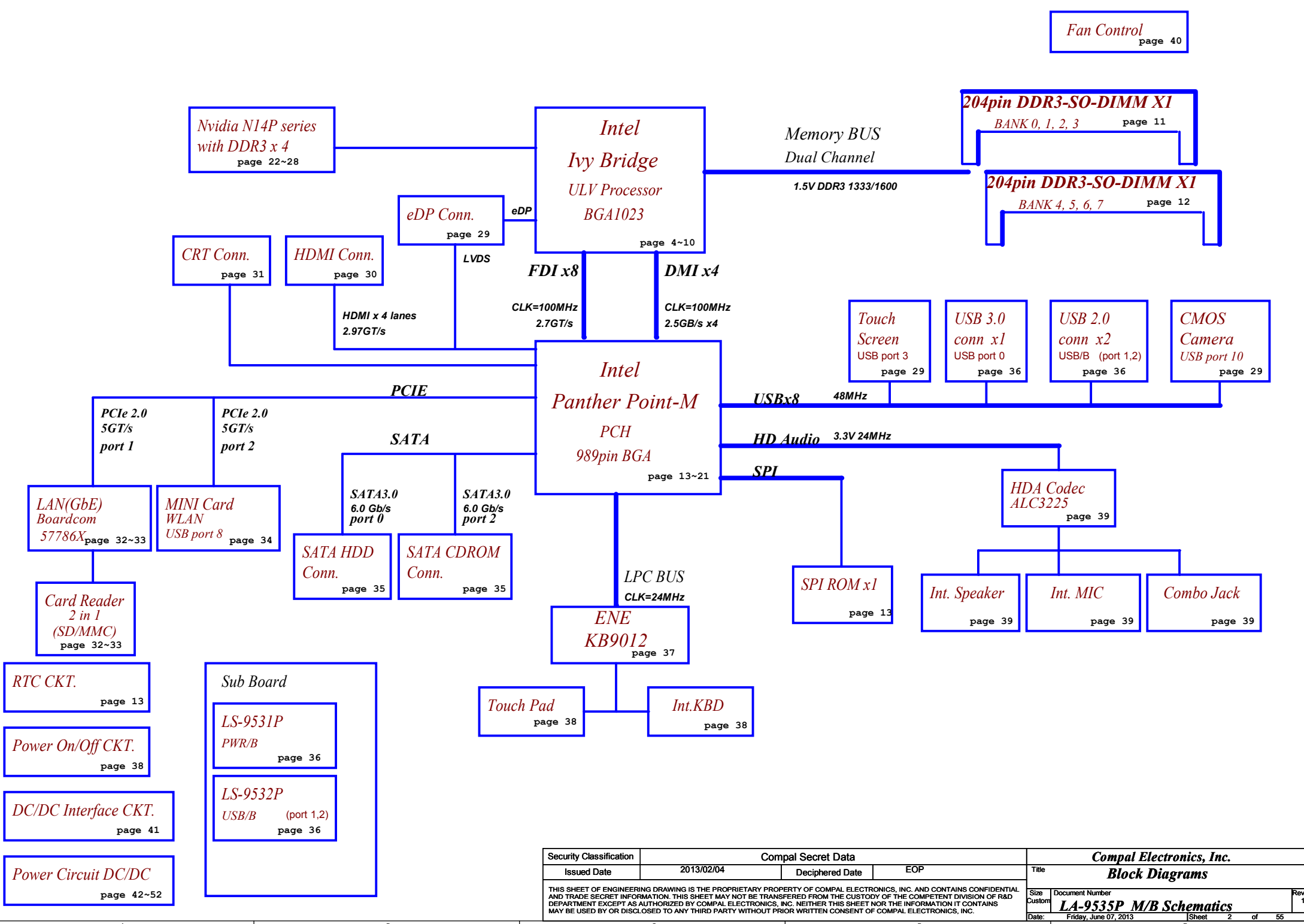
Intel Ivy Bridge ULV Processor + Panther Point PCH

Nvidia N14M-GE & N14P-GV2

2013-06-07

REV: 1.0

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>	
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				Date: Friday, June 07, 2013	Rev 1.0
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Date: Friday, June 07, 2013				Document Number	
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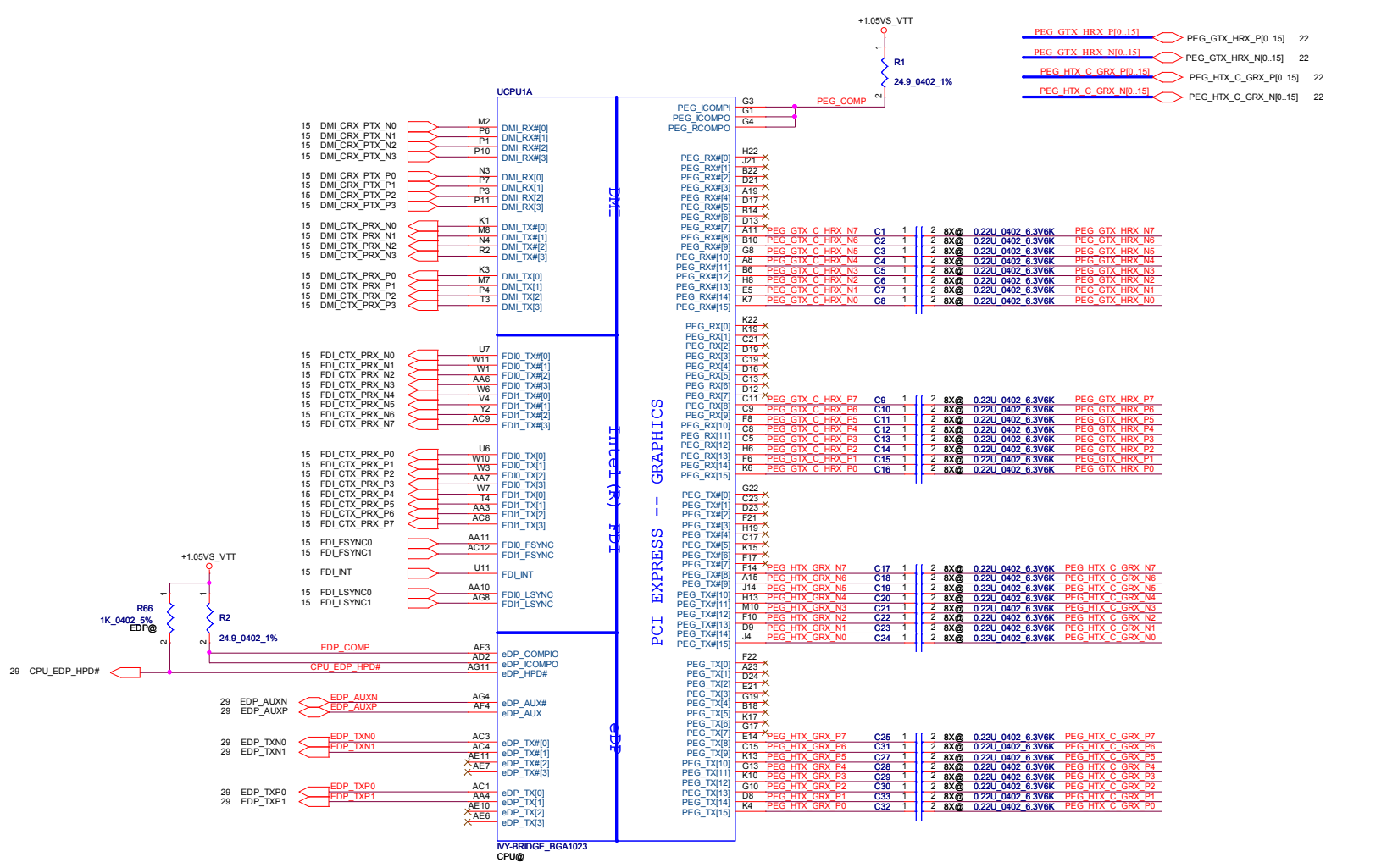
Part Number	Description	REVO DA6000ZK00
DAZ10000100	PCB Z5WE1 LA-9535P LS-9531P/LS-9532P	REV1 DA6000ZK010
LA9535_PCB		

UCPU1 I3327@	S IC AV8063801119500 SR0XF L1 1.9G ABO! SA00006D990	<b>IVY BRIDGE</b>
UCPU1 I5337@	S IC AV8063801129900 SR0XL L1 1.8G ABO! SA00006D860	
UCPU1 I73537@	S IC AV8063801119700 SR0XG L1 2G ABO! SA00006DB90	
UCPU1 847@	S IC AV8062700852800 SR08N Q0 1.1G ABO! SA00005VK20	
UCPU1 1007@	S IC AV8063801118700 SR109 P0 1.5G ABO! SA00006EW30	
UCPU1 1017@	S IC AV8063801130300 SR10A P0 1.6G ABO! SA00006UH50	
UCPU1 2117@	S IC AV8063801058800 SR0VQ P0 1.8G ABO! SA000061240	
UCPU1 2127@	S IC AV8063801119100 SR105 P0 1.9G ABO! SA00006UG30	
UCPU1 I33217@	S IC AV8063801058401 SR0N9 L1 1.8G ABO! SA00005L5C0	
U1010 HM77@	S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO! SA00005AGI0	<b>PCH</b>
U1010 HM70@	S IC BD82HM70 SJTNV C1 BGA 989P PCH ABO ! SA00005MQ60	
U1010 NM70@	S IC BD82NM70 SLJTA C1 BGA 989P PCH ABO! SA00005WU20	
U1010 NM70@	S IC BD82NM70 SLJTA C1 BGA 989P PCH ABO! SA00005WU20	

eDP\_COMPIO and eDP\_ICOMPO should be connected to R247 respectively.

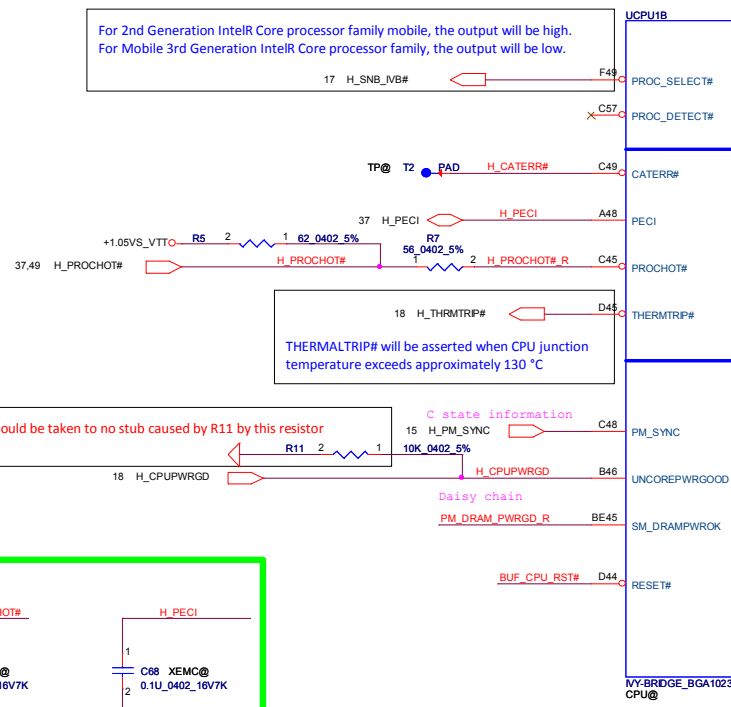
**eDP\_COMPIO**  
Trace Width to R2= 4-mil  
Trace Spacing to Other Signals= 15-mil  
Max. Routing Length= 500-mil

**eDP\_ICOMPO**  
Trace Width to R2= 12-mil  
Trace Spacing to Other Signals= 15-mil  
Routing Length= 500-mil



1. PEG\_RCOMPO and PEG\_ICOMPI should be connected together with 4-mil width first. Then be connected to R1 from ball of PEG\_ICOMPI.  
2. PEG\_ICOMPO should be connected to R1 with width 12-mil.  
3. No longer than 500-mil to above two.

For 2nd Generation Intel® Core processor family mobile, the output will be high.  
 For Mobile 3rd Generation Intel® Core processor family, the output will be low.



For LVDS  
 DPLL\_REF\_CLK R517 2 LVDS@ 1 1K 0402 5%  
 DPLL\_REF\_CLK# R518 2 LVDS@ 1 1K 0402 5%  
 +1.05VS\_VTT

If use External Graphic or use integrated without eDP  
 DPLL\_REF\_SSCLK PD 1K 5% to GND  
 DPLL\_REF\_SSCLK# PH 1K 5% to +1.05VS\_VTT

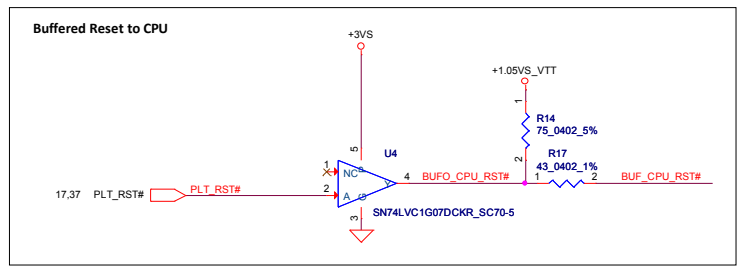
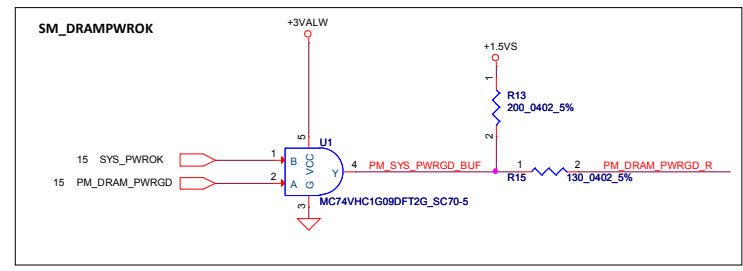
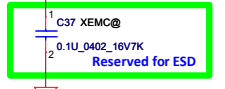
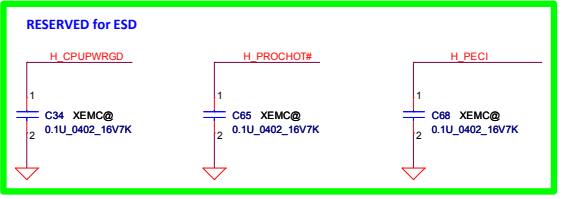
	Width	Spacing	Length
SM_RCOMP0	20-mil	20-mil	< 500-mil
SM_RCOMP1	20-mil	20-mil	< 500-mil
SM_RCOMP2	15-mil	20-mil	< 500-mil

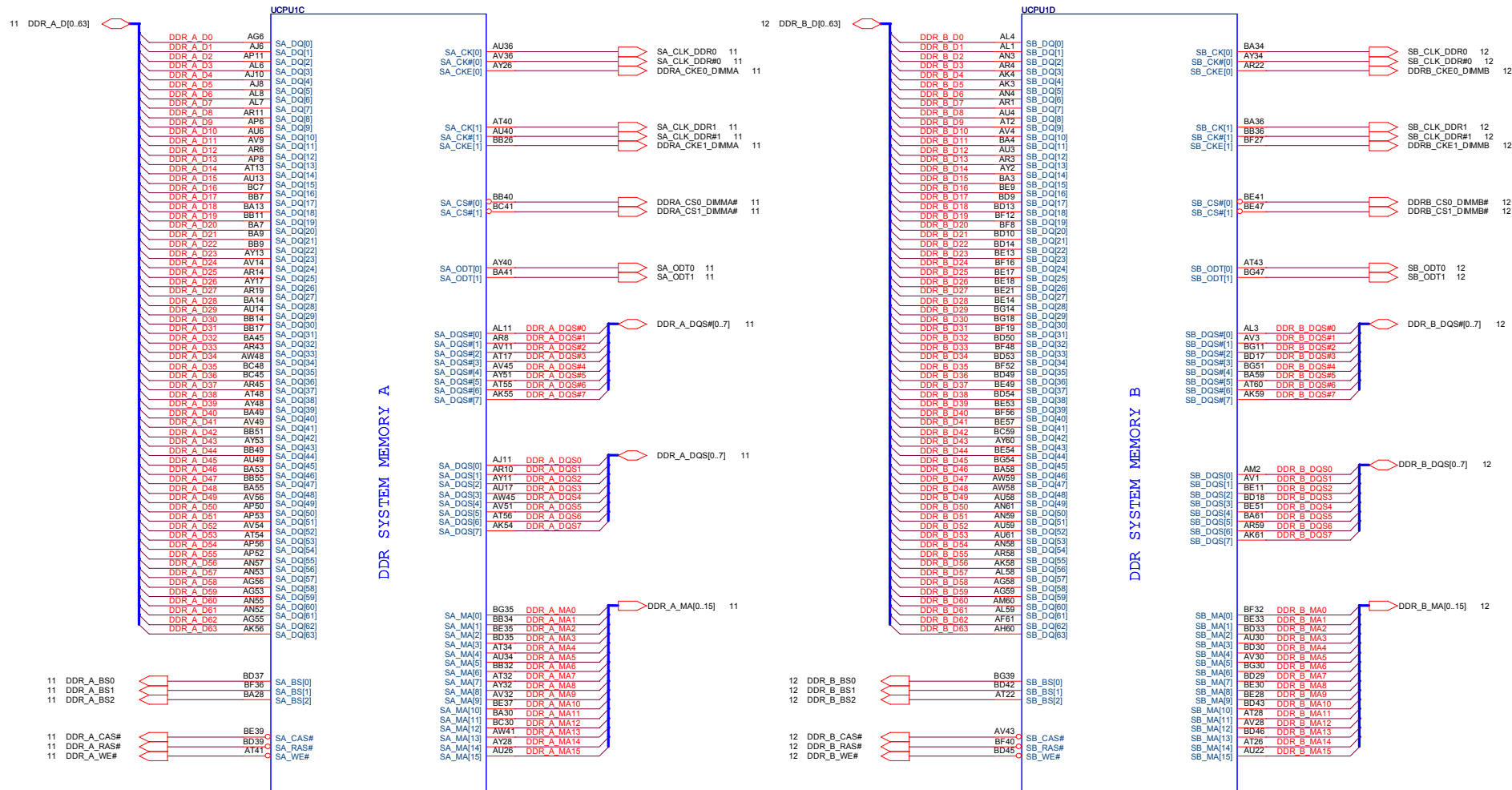
care should be taken to no stub caused by R11 by this resistor

C state information

Daisy chain

THERMALTRIP# will be asserted when CPU junction temperature exceeds approximately 130 °C



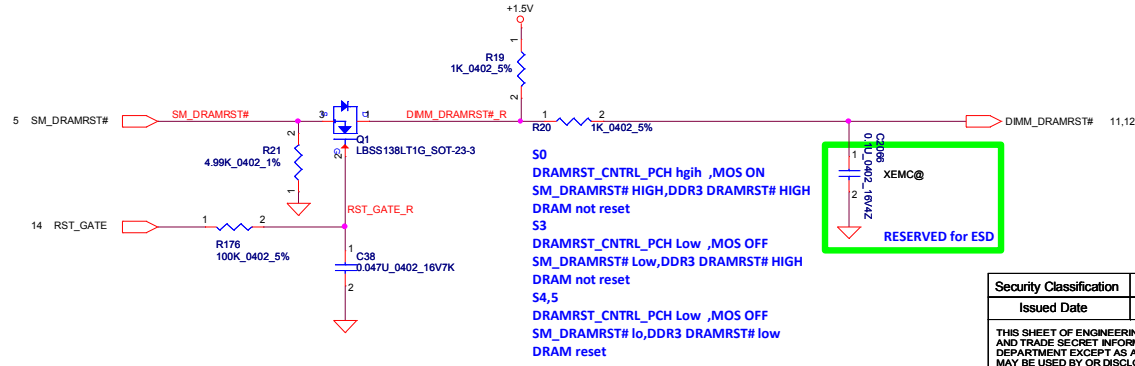


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

NY-BRIDGE\_BGA1023 CPU@

NY-BRIDGE\_BGA1023 CPU@

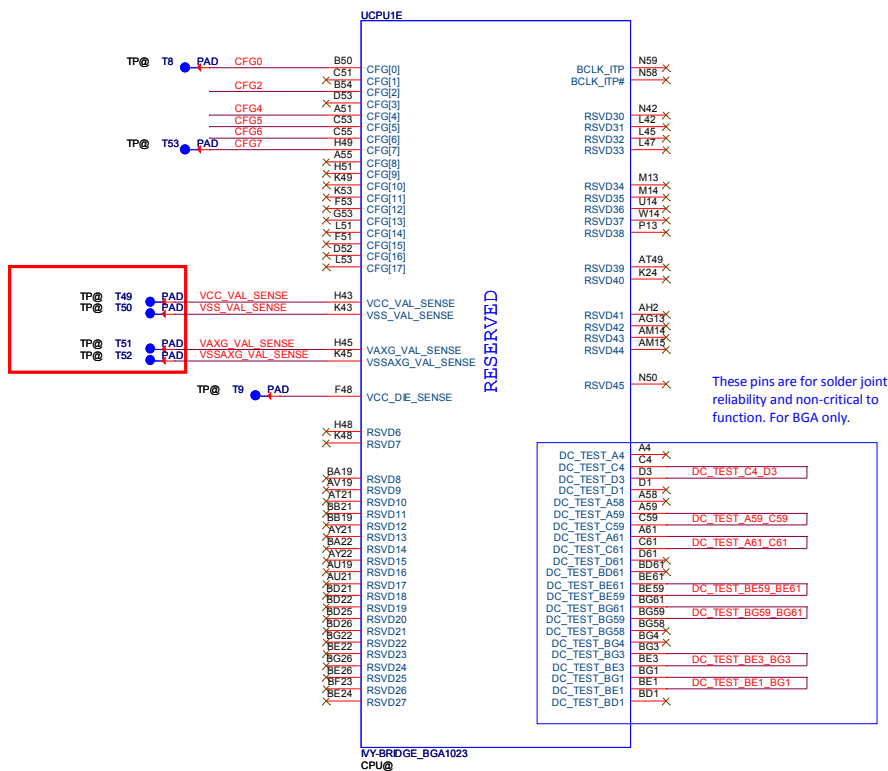


S0  
 DRAMRST\_CNTRL\_PCH hgh, \_MOS ON  
 SM\_DRAMRST# HIGH, DDR3 DRAMRST# HIGH  
 DRAM not reset

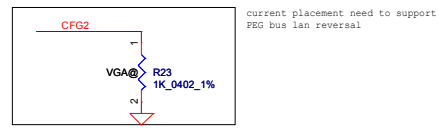
S3  
 DRAMRST\_CNTRL\_PCH Low, \_MOS OFF  
 SM\_DRAMRST# Low, DDR3 DRAMRST# HIGH  
 DRAM not reset

S4,5  
 DRAMRST\_CNTRL\_PCH Low, \_MOS OFF  
 SM\_DRAMRST# Lo, DDR3 DRAMRST# low  
 DRAM reset

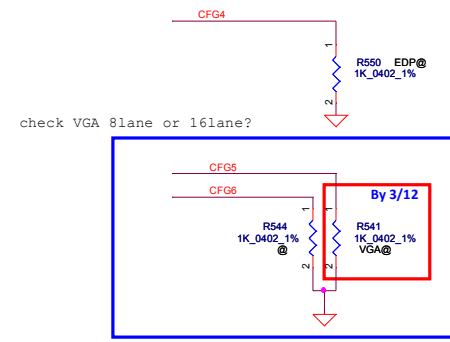
Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP
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Title			Compal Electronics, Inc.
Size Custom			PROCESSOR(3/7) DDRIII
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### CFG Straps for Processor



PCIe Static x16 Lane Numbering Reversal	
CFG2	1: (Default)Normal Operation Lane # definition matches socket pin map definition * 0: Lane Reversed



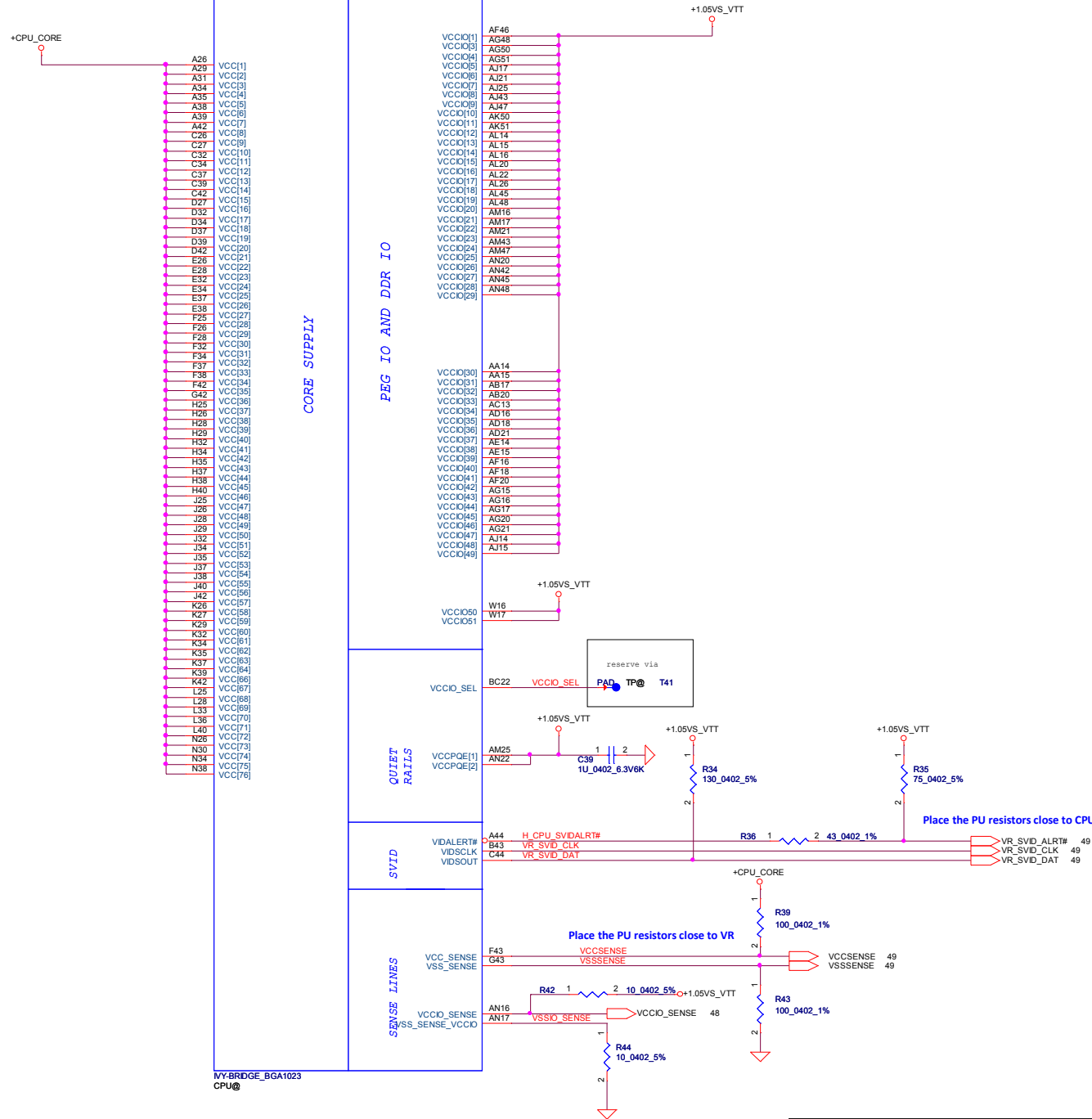
eDP Enable Strap	
CFG4	1: (Default)Disable *0: Enable

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express *10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING Tacoma_Fall2 1.0 P.12	
CFG7	* 1: (Default) PEG Trains immediately and follows xxRESETB de-assertion 0: PEG Wait for BIOS for training

# POWER

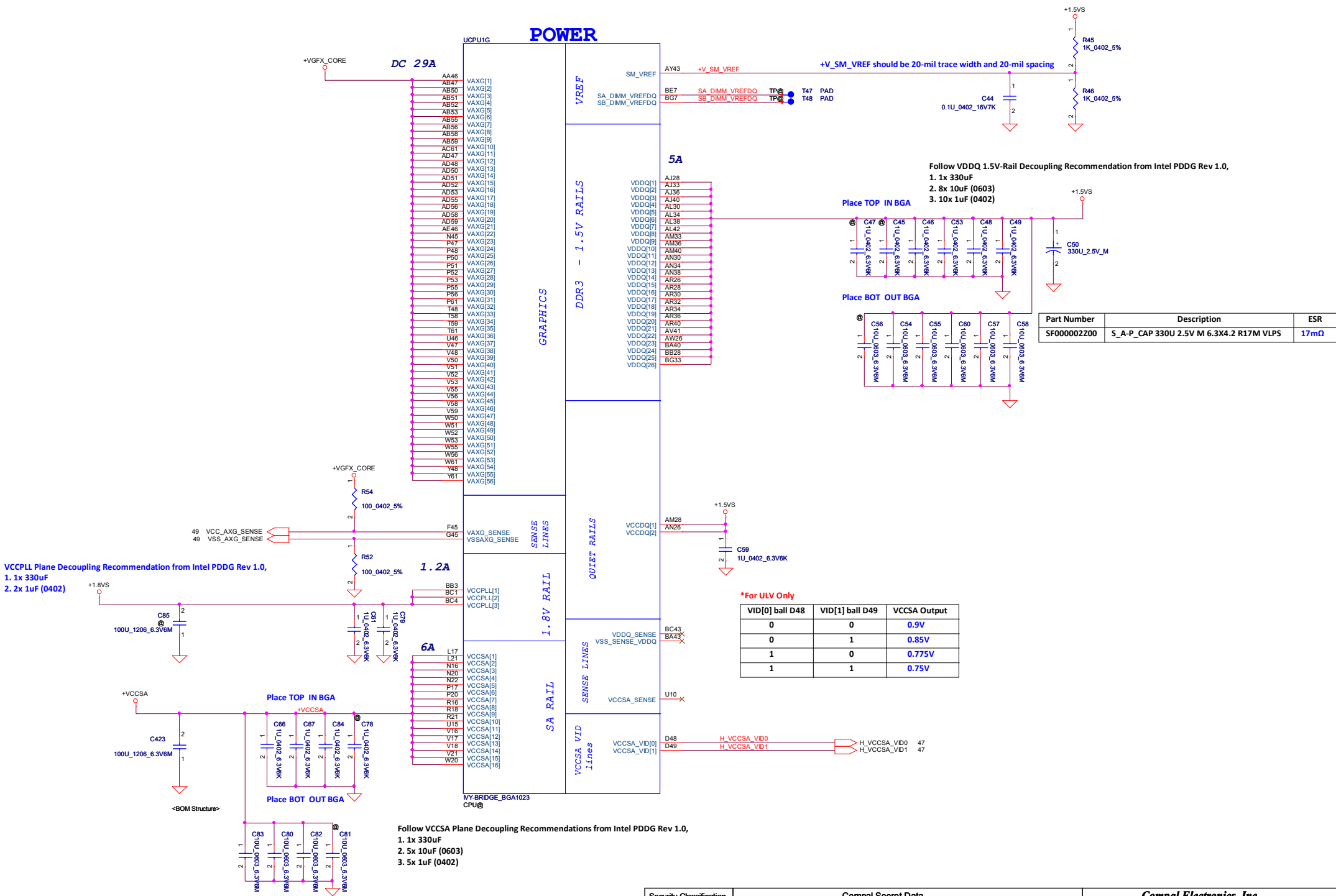


CPU Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
VCC	0.65~1.2	33	Processor Core Voltage
VCCIO	1.05	8.5	Processor Uncore Voltage
VDDQ	1.5	5	Memory Controller Voltage
VCCSA	0.675~0.9	4	System Agent Voltage
VCCPLL	1.8	1.2	Processor PLL Voltage
VAXG	0.65~1.25	29	Processor Graphics Voltage

Refer to Mobile 3rd Generation Intel® Core Processor Family External Design Specification (EDS) Volume 1 of 2 Revision 2.2

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Size	Customer	Document Number	Date	Rev	1.0
		LA-9535P M/B Schematics	Friday, June 07, 2013	Sheet	8 of 55

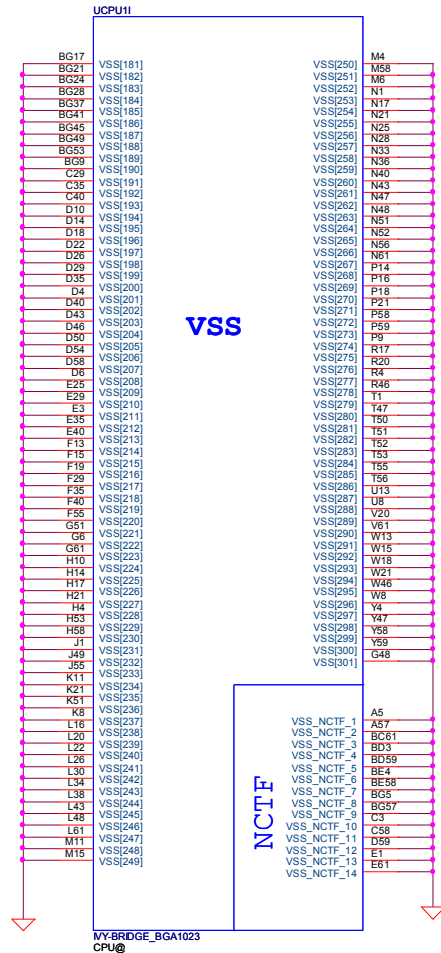
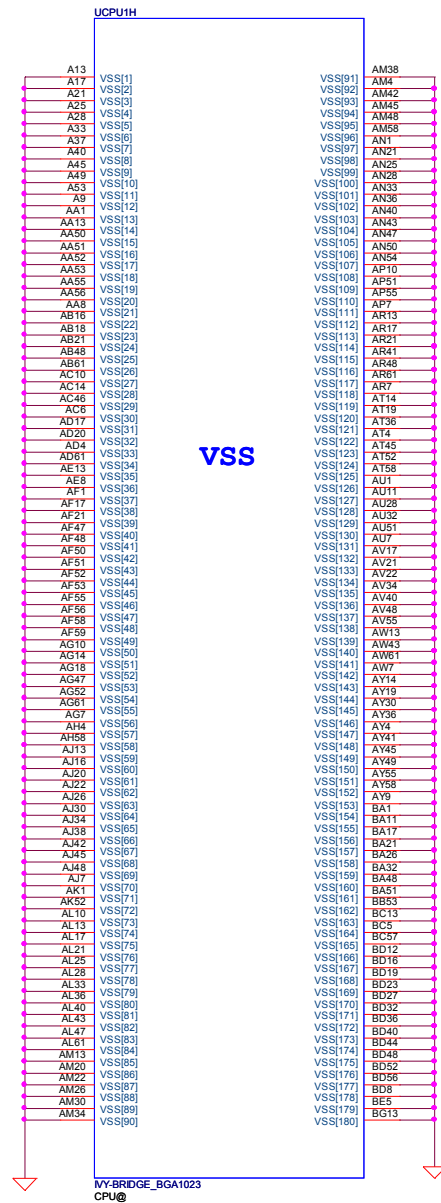


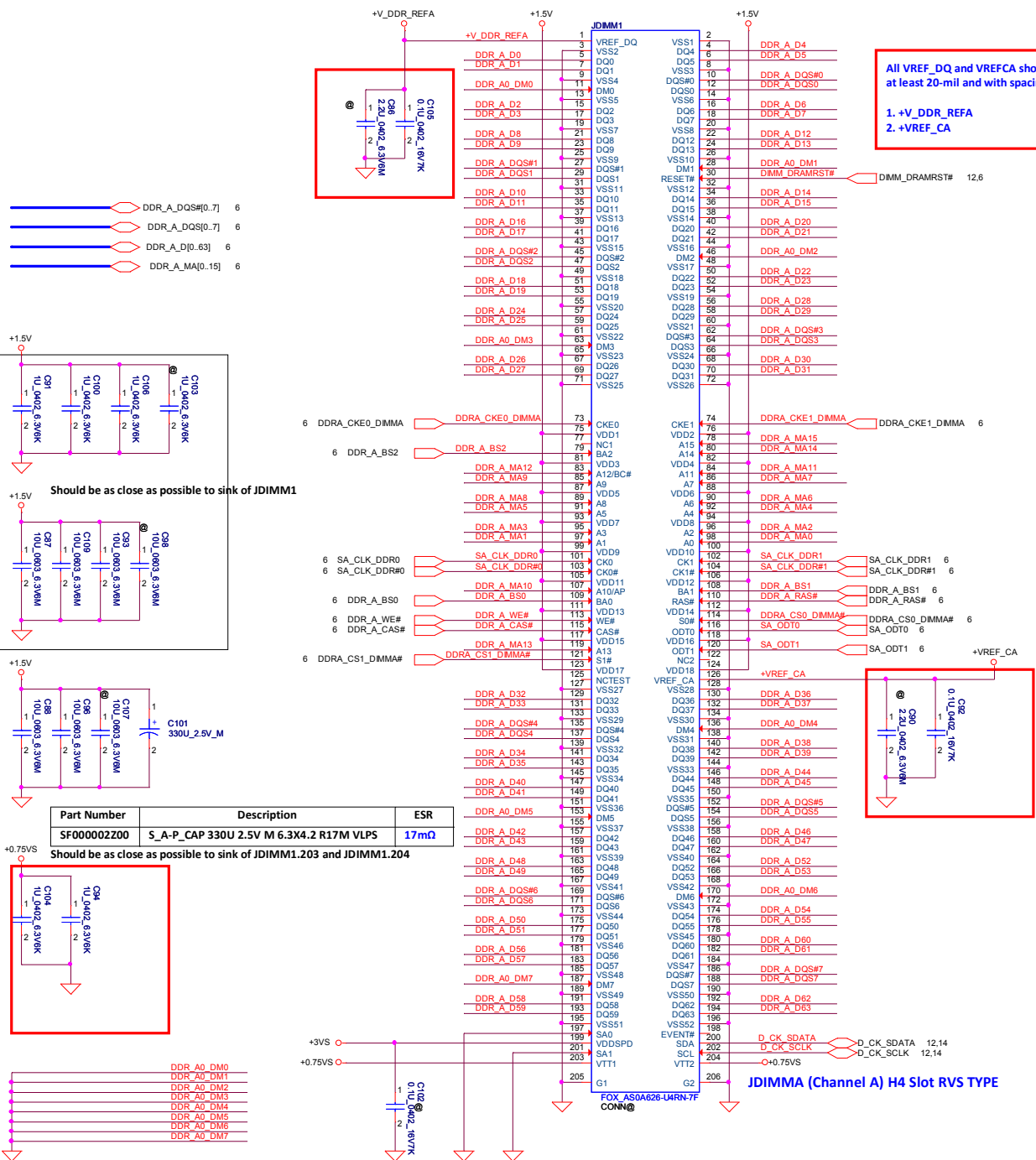


Part Number	Description	ESR
SF000002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLPS	17mΩ

**\*For ULV Only**

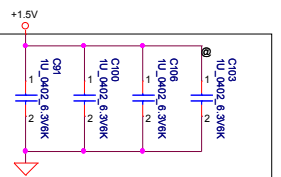
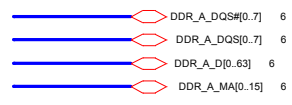
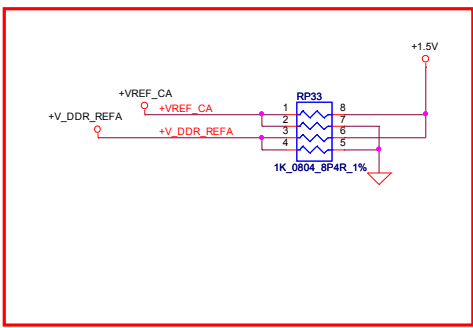
VID[0] ball D48	VID[1] ball D49	VCCSA Output
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V



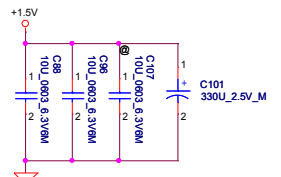
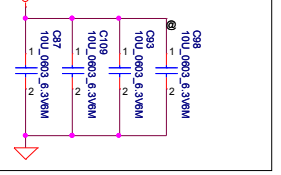


All VREF\_DQ and VREFCA should be routed with width at least 20-mil and with spacing at least 20-mil.

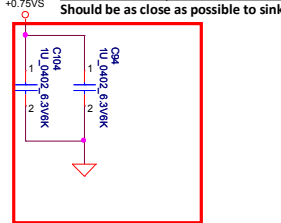
1. +V\_DDR\_REFA  
2. +VREF\_CA

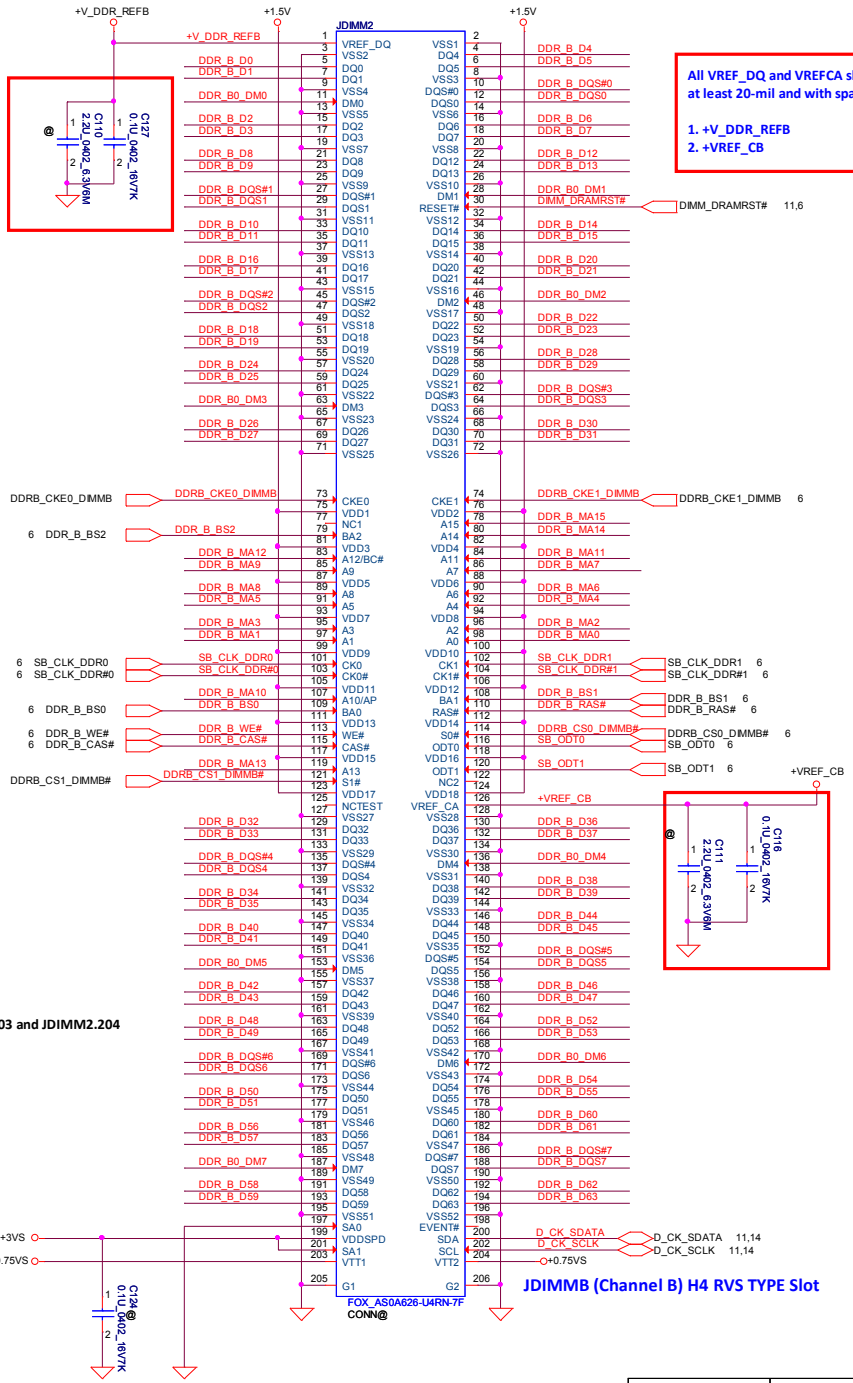
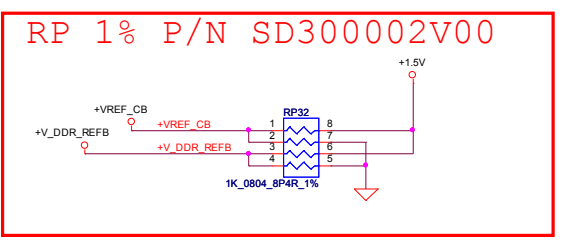


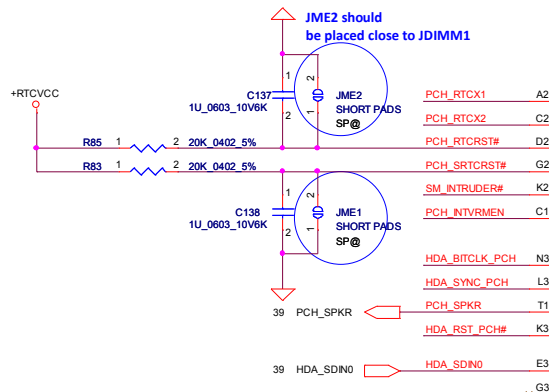
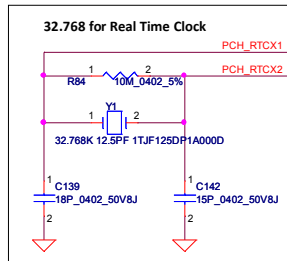
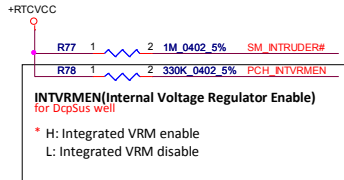
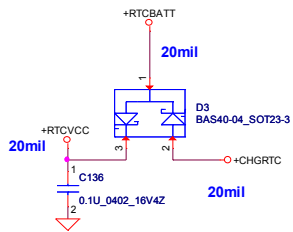
Should be as close as possible to sink of JDIMM1



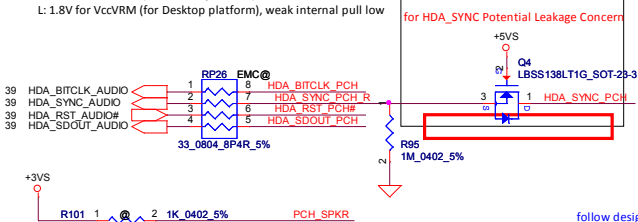
Part Number	Description	ESR
SF000002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLPs	17mΩ







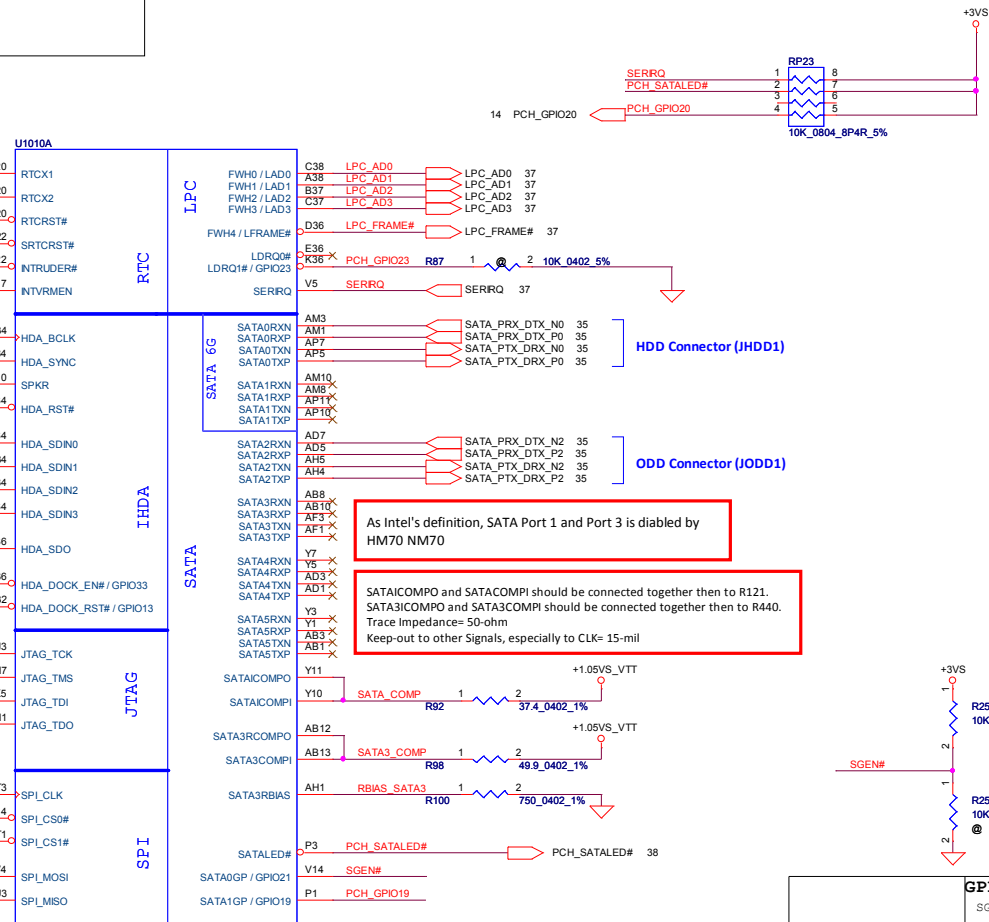
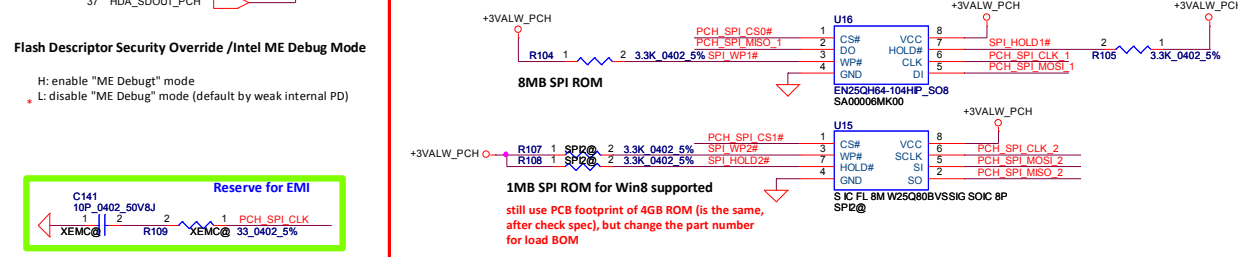
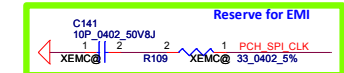
\* H: 1.5V for VccVRM (for Mobile platform)  
L: 1.8V for VccVRM (for Desktop platform), weak internal pull low



**No Reboot**  
H: enable "No Reboot" mode  
L: disable "No Reboot" mode (default by weak internal PD)

**Flash Descriptor Security Override /Intel ME Debug Mode**

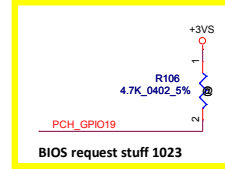
H: enable "ME Debug" mode  
L: disable "ME Debug" mode (default by weak internal PD)



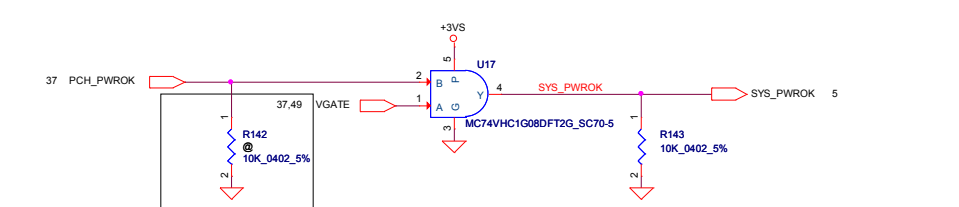
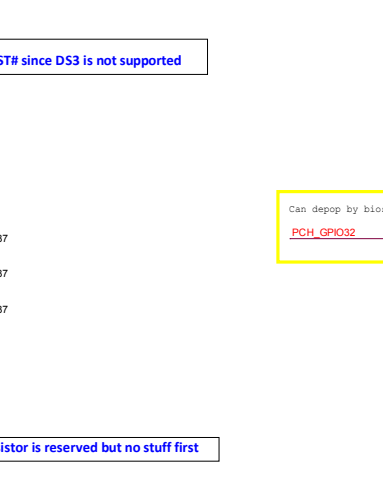
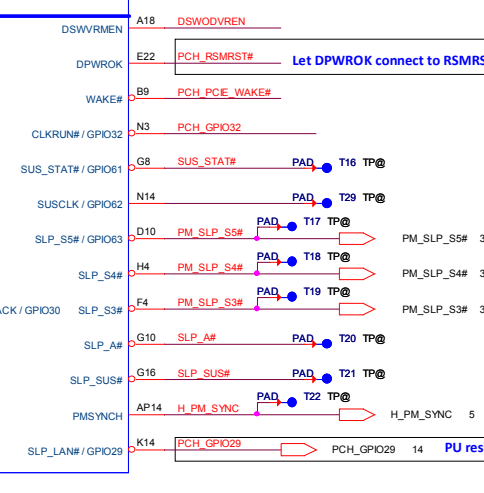
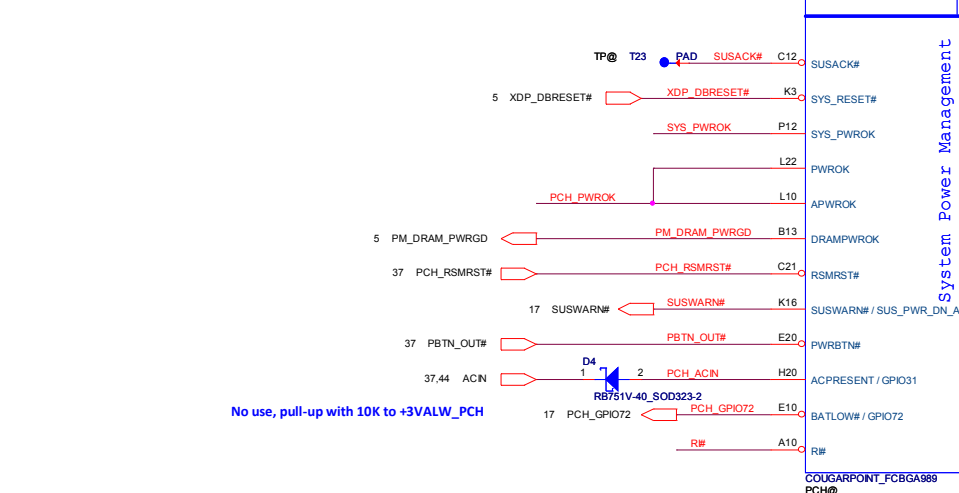
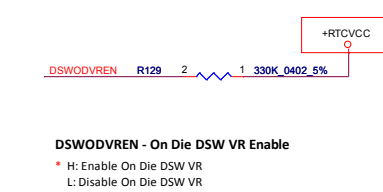
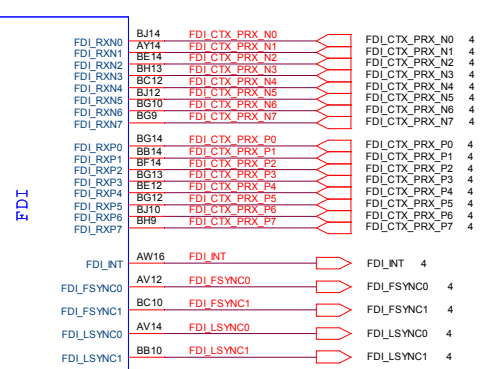
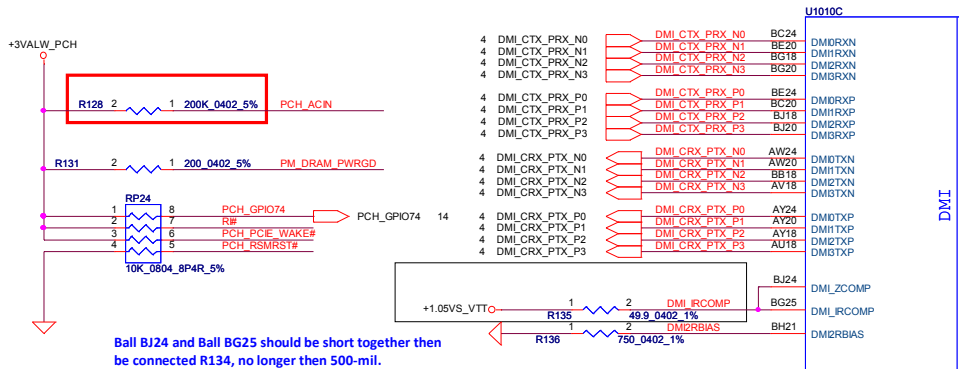
	GPIO21
SGEN#	
Switchable GPU	0
*Non-Switchable	1

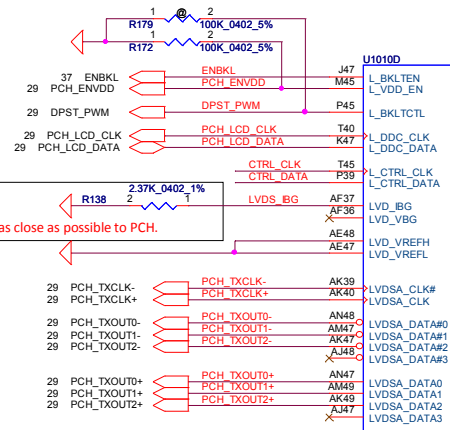
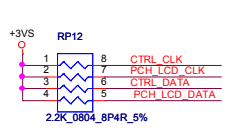
In accordance with design guide 2.0 page 274, if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary.

	Boot BIOS Destination Selection	
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1



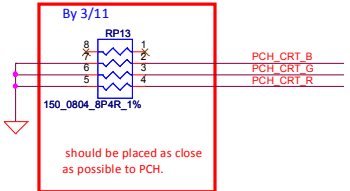




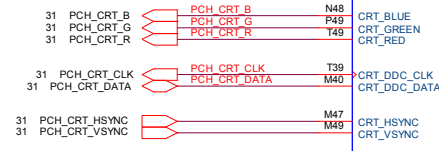


should be placed as close as possible to PCH.

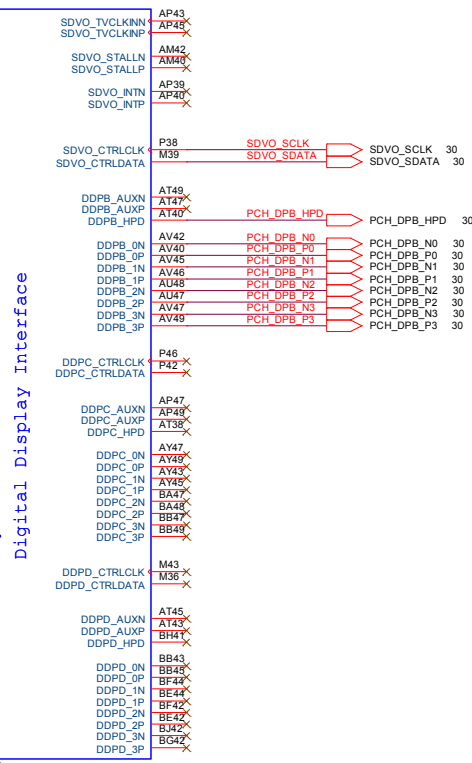
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VCC1X\_LVDS and VCCA\_LVD can be connected to ground. DG 471984 P.193



should be placed as close as possible to PCH.

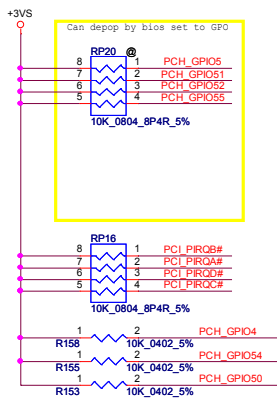


should be placed as close as possible to PCH T43, and keep the trace is at least 30-mil away from other signals (especially clocks).



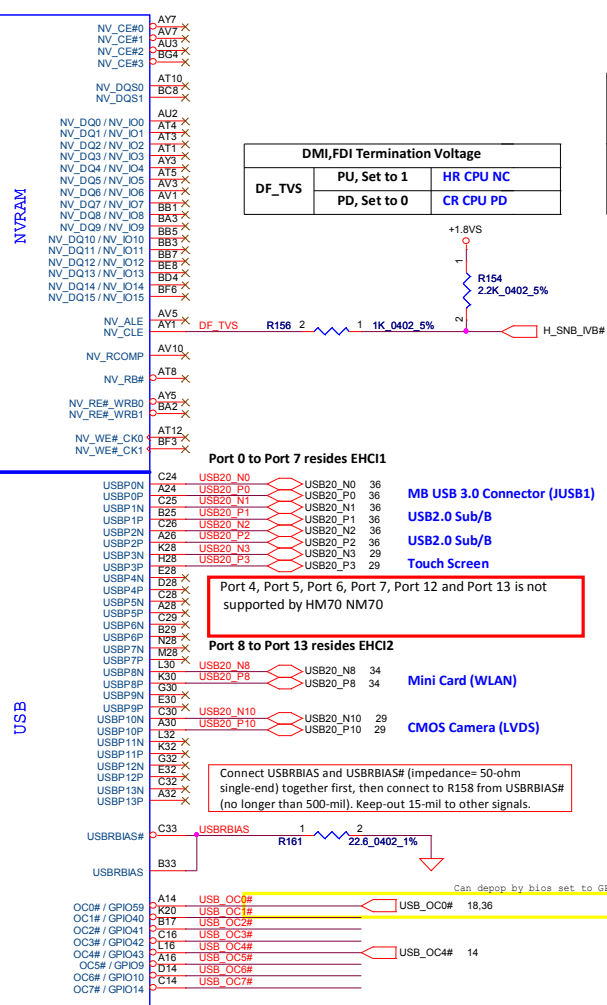
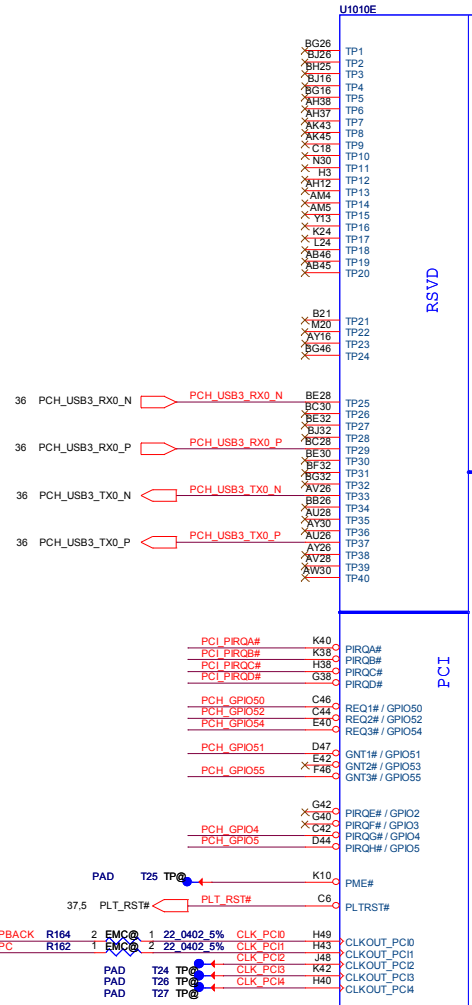
Security Classification		Compal Secret Data		Title	
Issued Date	2013/02/04	Deciphered Date	EOP	Compal Electronics, Inc. PCH (4/9) LVDS,CRT,DP,HDMI	
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In accordance with design guide 2.0 page 274, if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary.

Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BB51)	SATA1GP/GPIO19 (BB50)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1



**BDS**  
Processor Select: This pin is an output that indicates if the processor used is Sandy Bridge or Ivy Bridge. For Sandy Bridge the output will be high, and for Ivy Bridge the output will be low.

**PG**  
Sandy Bridge + Ivy Bridge Compatible: Connect DF\_TVS signal of the PCH to PROC\_SELECT# of the processor through a 1K±5 series resistor. PROC\_SELECT# also needs a 2.2K±5 pull up resistor to PCH VccDPTERM rail.

DMI, FDI Termination Voltage		
DF_TVS	PU, Set to 1	HR CPU NC
	PD, Set to 0	CR CPU PD

Port 0 to Port 7 resides EHC11

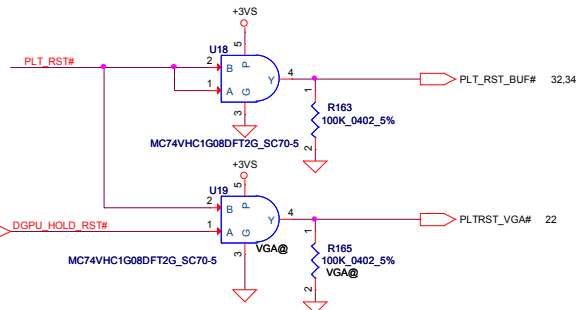
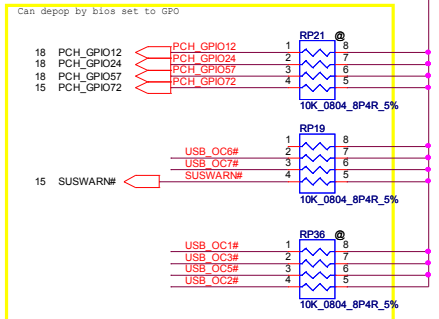
- MB USB 3.0 Connector (IUSB1)
- USB2.0 Sub/B
- USB2.0 Sub/B
- Touch Screen

Port 4, Port 5, Port 6, Port 7, Port 12 and Port 13 is not supported by HM70 NM70

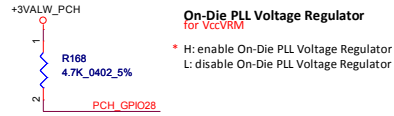
Port 8 to Port 13 resides EHC12

- Mini Card (WLAN)
- CMOS Camera (LVDS)

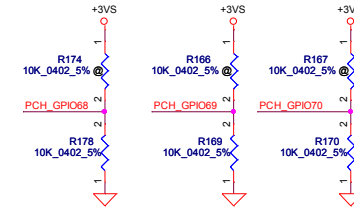
Connect USBRBIAS and USBRBIAS# (impedance=50-ohm single-end) together first, then connect to R158 from USBRBIAS# (no longer than 500-mil). Keep-out 15-mil to other signals.



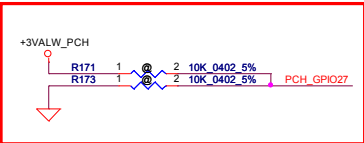
	HM77	HM70	NM70	Note
USB2.0	14	8	8	HM70/NM70 USB port 4, 5, 6, 7, 12 and 13 are disabled on 8 port SKUs.
USB3.0	4	2	0	USB 3.0 port 3 and 4 are disabled on HM70 USB 3.0 are all disabled on NM70
PCIe	8	4	4	HM70/NM70 PCIe port 5-8 are disabled on this SKU.
SATA	6	4	4	HM70/NM70 SATA port 1 and 3 are disabled on 4 port SKUs. HM70/NM70 SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s & 1.5 Gb/s HM77 SATA 6 Gb/s support on port 0 & port 1. SATA port 0 and 1 also support 3 Gb/s & 1.5 Gb/s.



For common BIOS code



Project ID	GPIO68	GPIO69	GPIO70
Q5WE0	1	0	0
Q7YE0	1	0	1
Q5Wxx-QC	1	1	0
V5VT1	1	1	1
*Z5WE1_CR	0	0	0



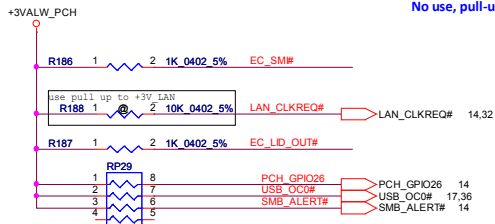
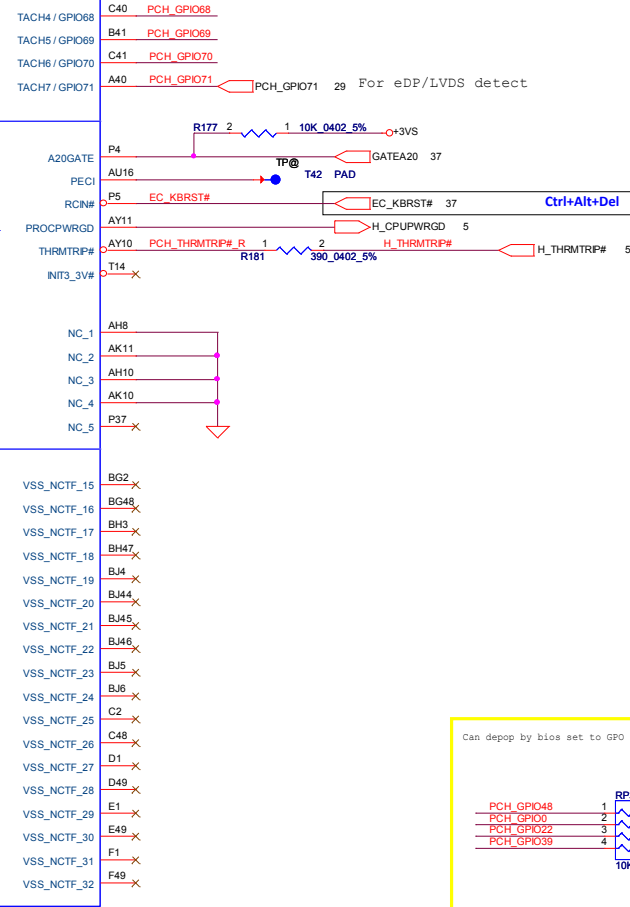
- No use, pull-up with 10K to +3VS PCH\_GPIO0 T7
- No use, pull-up with 10K to +3VS PCH\_GPIO1 A42
- No use, pull-up with 10K to +3VS PCH\_GPIO6 H36
- EC\_SC# EC\_SC# E38
- EC\_SM# EC\_SM# C10
- No use, pull-up with 10K to +3VALW\_PCH PCH\_GPIO12 C4
- EC\_LID\_OUT# EC\_LID\_OUT# G2
- No use, pull-up with 10K to +3VS PCH\_GPIO16 U2
- VGA\_PWROK R110 1 2 0\_0402\_5% D40
- On Board DRAM Flag PCH\_GPIO22 T5
- No use, pull-up with 10K to +3VALW\_PCH PCH\_GPIO24 E8
- PCH\_GPIO27 E16
- PCH\_GPIO28 P8
- TP@ PAD K1
- TP@ PAD K4
- TP@ PAD V8
- TP@ PAD M5
- OPTIMUS\_EN# N2
- On Board DRAM Flag PCH\_GPIO39 M3
- On Board DRAM Flag PCH\_GPIO48 V13
- TP@ PAD V3
- No use, pull-up with 10K to +3VALW\_PCH PCH\_GPIO57 D6

- U1010F
- BMBUS# / GPIO0
- TACH1 / GPIO1
- TACH2 / GPIO6
- TACH3 / GPIO7
- GPIO8
- LAN\_PHY\_PWR\_CTRL / GPIO12
- GPIO15
- SATA4GP / GPIO16
- TACH0 / GPIO17
- SCLOCK / GPIO22
- GPIO24 / MEM\_LED
- GPIO27
- GPIO28
- STP\_PC# / GPIO34
- GPIO35
- SATA2GP / GPIO36
- SATA3GP / GPIO37
- SLOAD / GPIO38
- SDATAOUT0 / GPIO39
- SDATAOUT1 / GPIO48
- SATA5GP / GPIO49
- GPIO57
- VSS\_NCTF\_1 A4
- VSS\_NCTF\_2 A44
- VSS\_NCTF\_3 A45
- VSS\_NCTF\_4 A46
- VSS\_NCTF\_5 A5
- VSS\_NCTF\_6 A6
- VSS\_NCTF\_7 B3
- VSS\_NCTF\_8 B47
- VSS\_NCTF\_9 BD1
- VSS\_NCTF\_10 BD49
- VSS\_NCTF\_11 BE1
- VSS\_NCTF\_12 BE49
- VSS\_NCTF\_13 BF1
- VSS\_NCTF\_14 BF49
- COULGAPPOINT\_FCBGA889
- PCH@

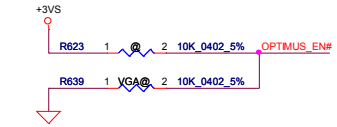
GPIO

CPU/MISC

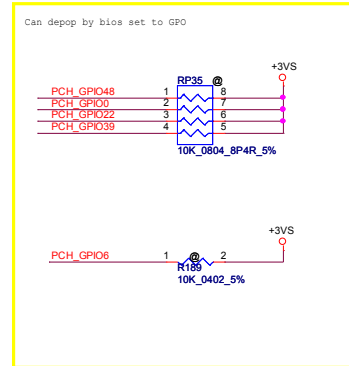
NCTF

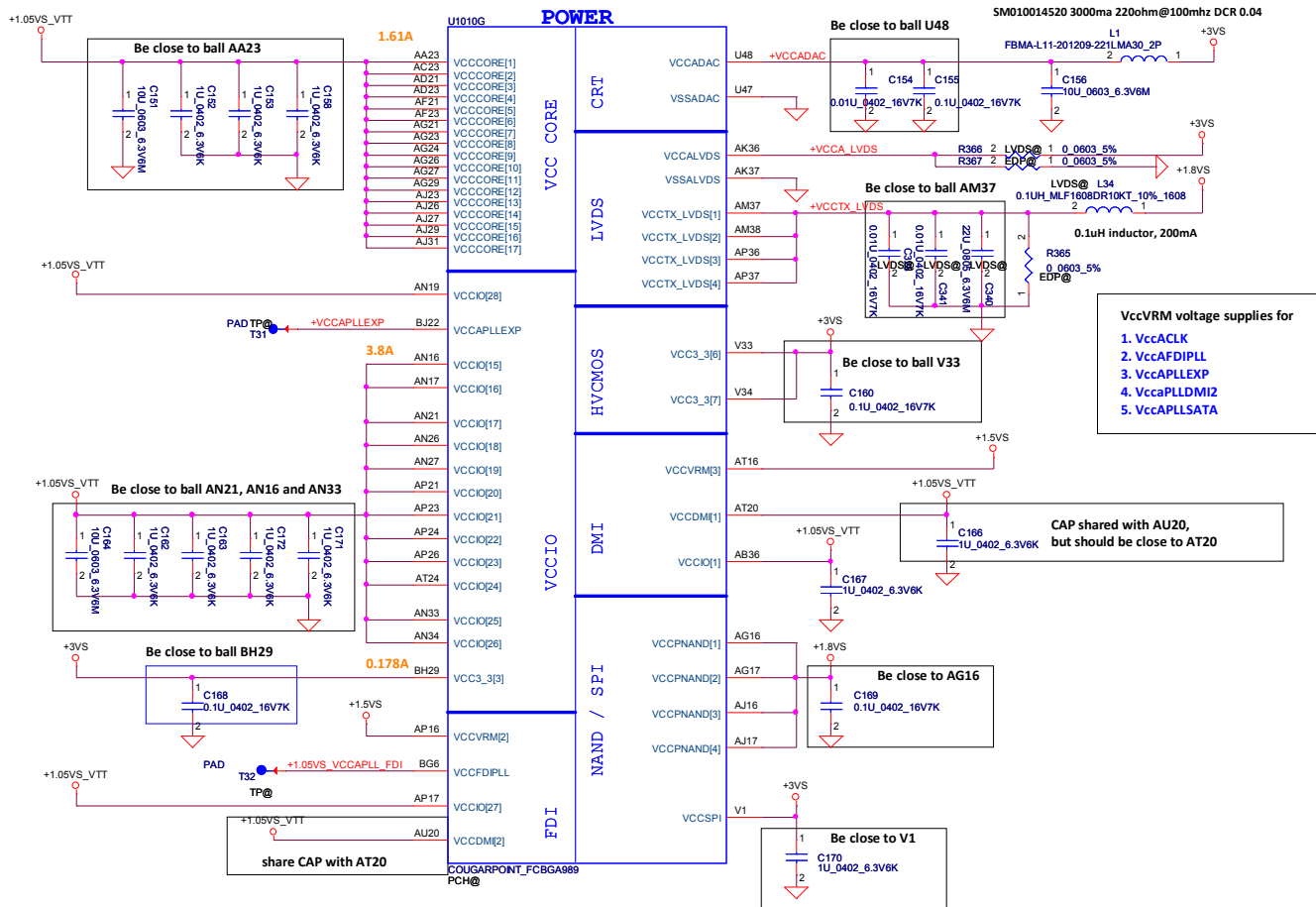


in accordance with Chief River check list 1.7, when Unused as GPIO or SATA\*GP Use 8.2K-10K pull-down to ground



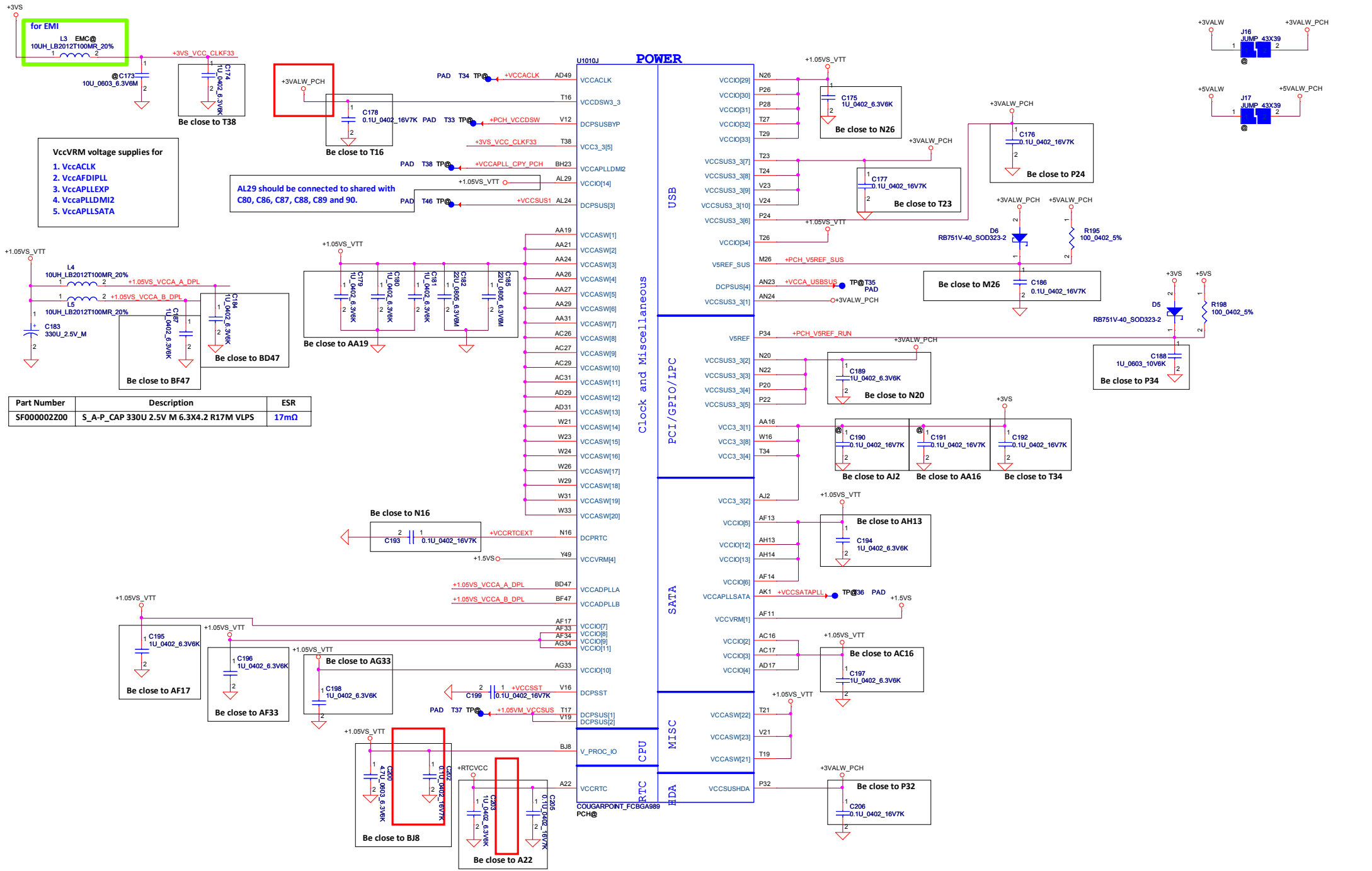
	GPIO38
OPTIMUS	0
DIS Only	1



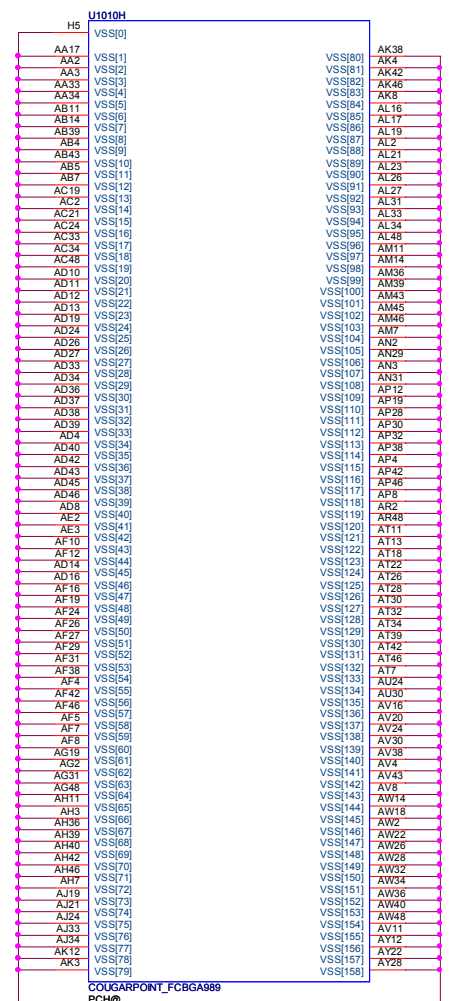


Refer to Intel R 7 Series / C216 Chipset Family Platform Controller Hub (PCH) External Design Specification (EDS) Revision 2.1

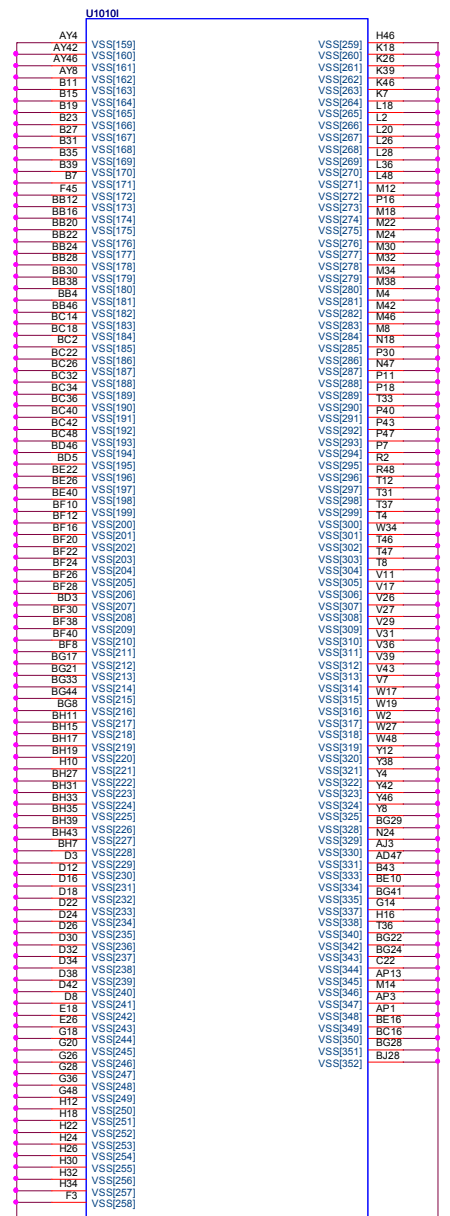
PCH Power Rail Table			
Voltage Rail	Voltage	SO Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/O
VSREF	5	0.001	PCH Core Well Reference Voltage
VSREF_Sus	5	0.001	Suspend Well Reference Voltg
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLL	1.05	0.075	Display PLL A power
VccADPLL	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW3_3	3.3	0.001	3.3v supply for Deep Sx well
VccDFTERN (VccPNAND)	1.8	0.002	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	RTC Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.5	0.147	1.5 V Internal PLL and VRMs
VccCLKDMI	1.05	0.075	DMI differential Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.05	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.04	I/O power supply for LVDS (Mobile Only)



Part Number	Description	ESR
SF00002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLP5	17mΩ

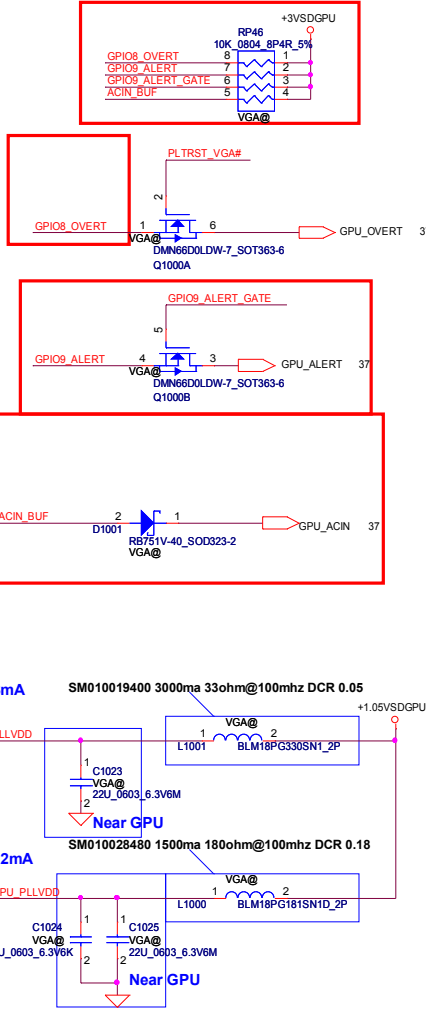
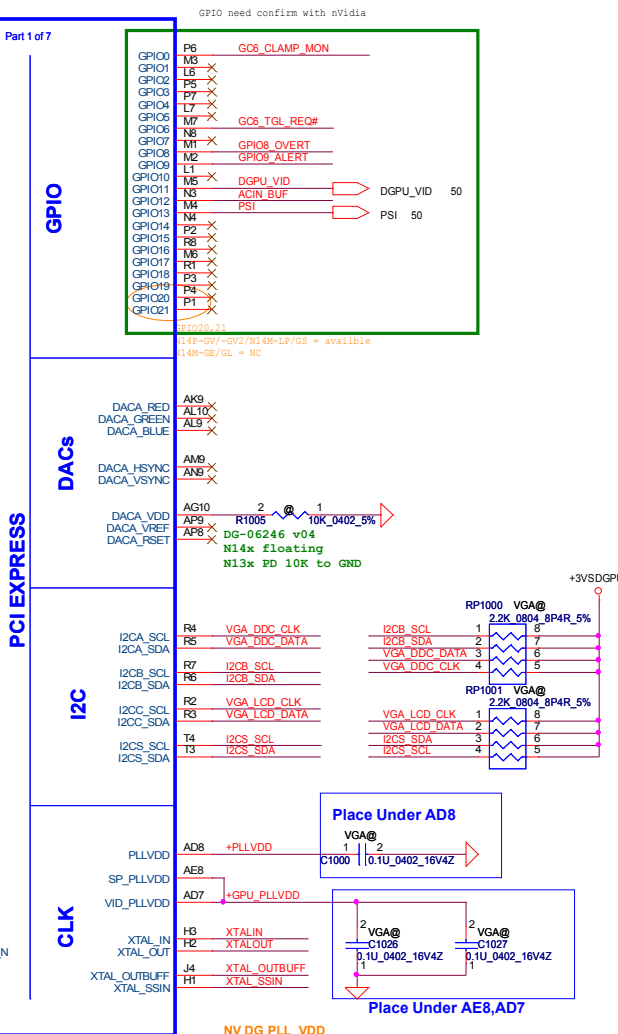
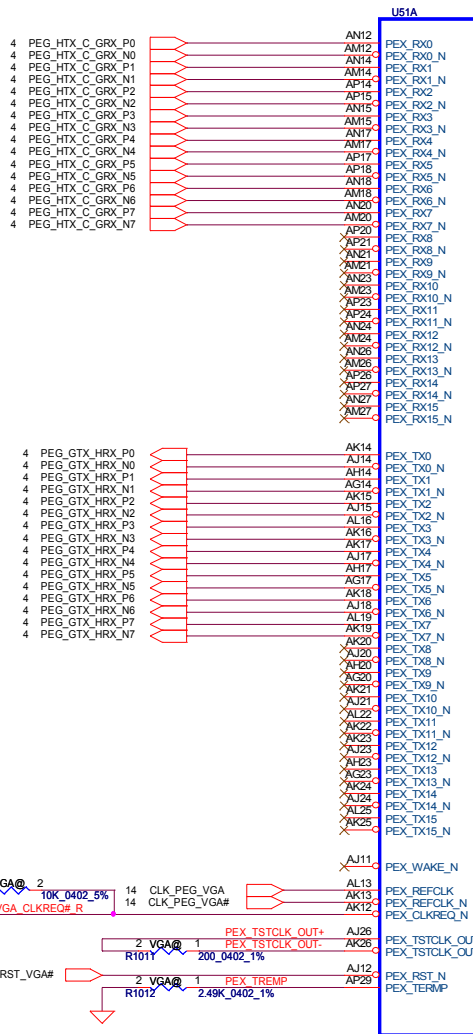


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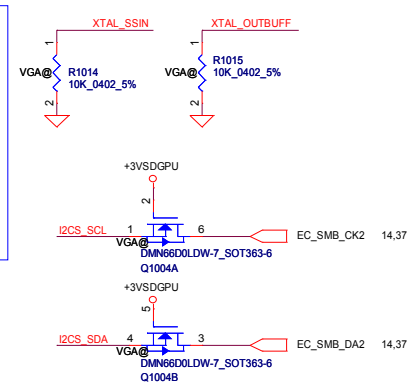
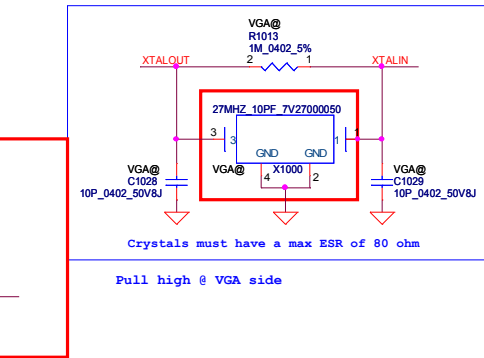
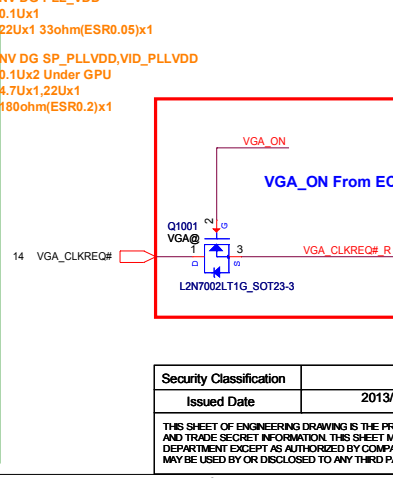
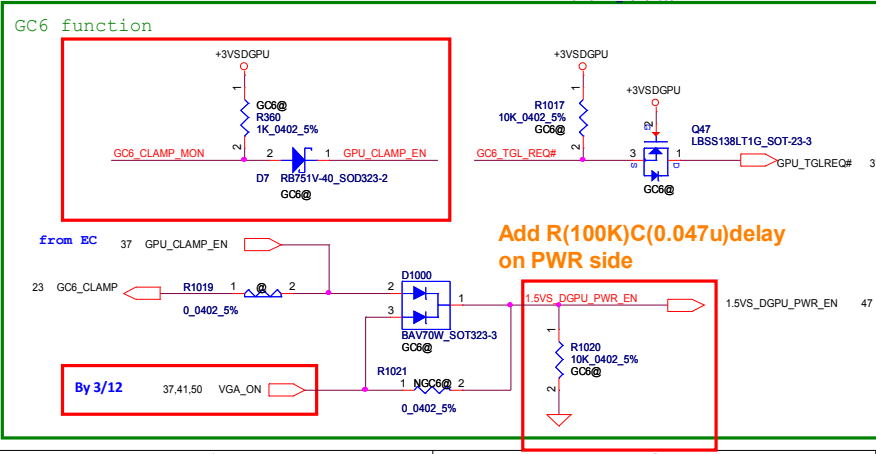


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GPIO	I/O	USAGE
GPIO0	I	FB_CLAMP_MON
GPIO1	O	MEM_VD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	Reserved
GPIO6	O	FB_CLAMP_TGL_REQ
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	O	FRM_CLK
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21		Reserved
GPIO22		
GPIO23		
GPIO24		

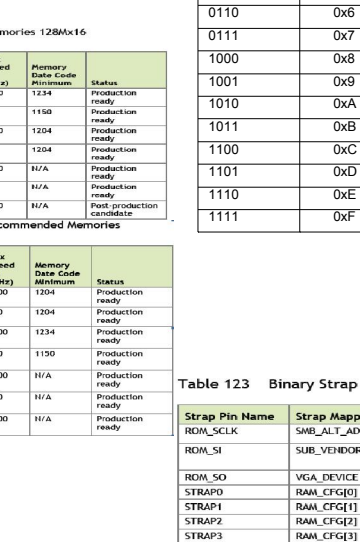
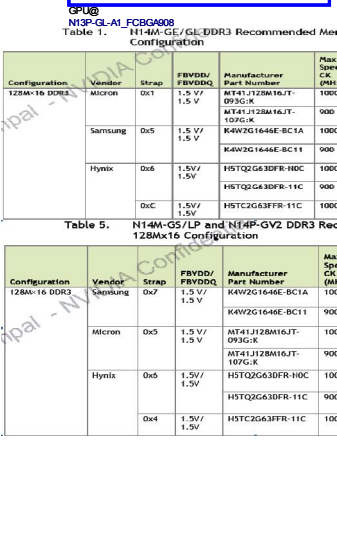
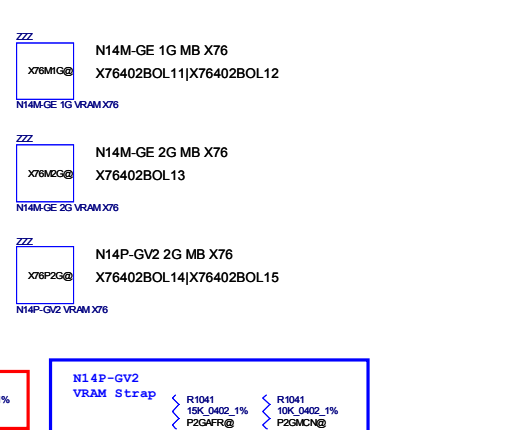
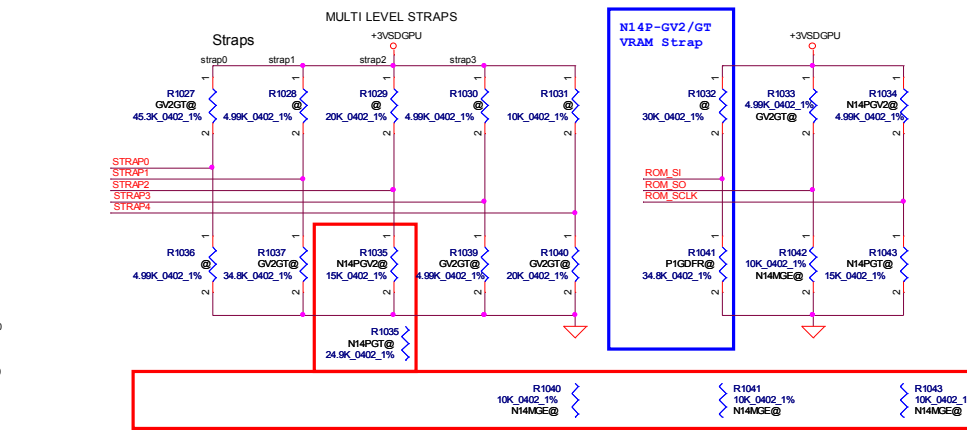
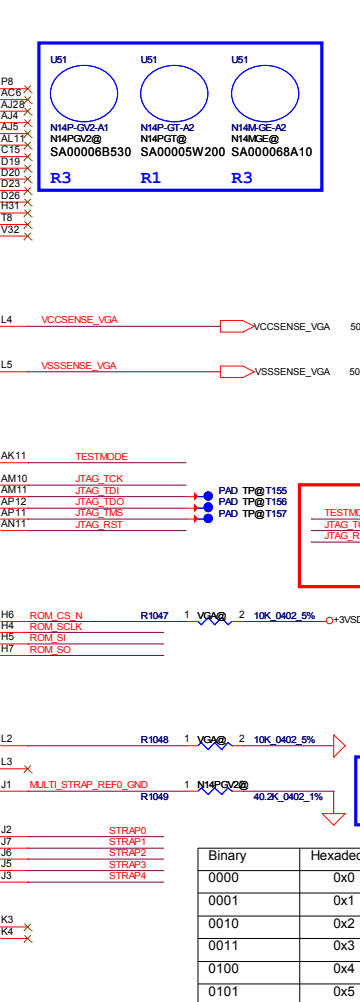
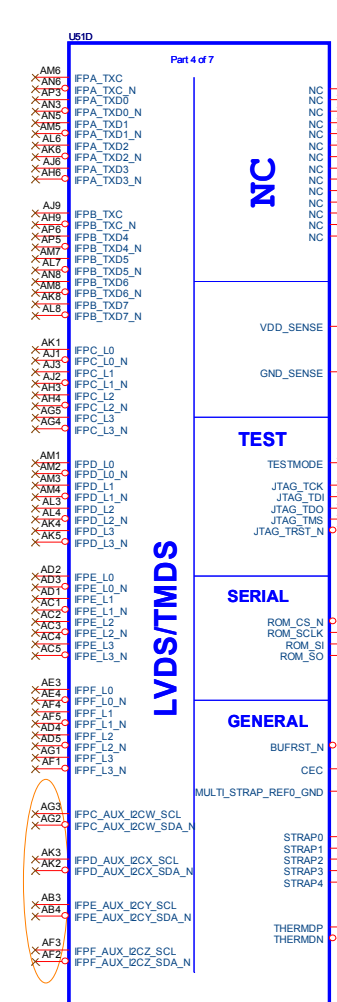


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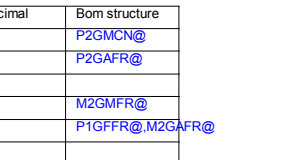
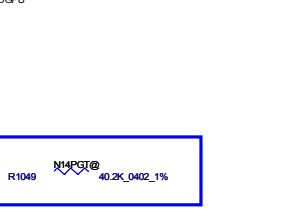
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<b>N14P PEG 1/7</b>			
Size	Document Number	Rev	
Custom	<b>LA-9535P M/B Schematics</b>	1.0	
Date:	Friday, June 07, 2013	Sheet	22 of 55





**For N14P-GV2 strap table** Decide ID : 0x1292  
**For N14P-GT strap table** Decide ID : 0xFE4

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	900 MHz	128M 16* 4 GB	0x4: HYNIX SA0000H430 R3 H5TC2G63FR-11C 0x6: HYNIX SA0000Y090 R3 H5TC2G63DR-11C	R PU 45.3K	R PD 34.8K	R PD 15K	R PD 4.99K	R PD 20K	PD 34.8K PD 24.9K	R PU 4.99K	R PU 4.99K
	900 MHz	256M 16* 4 GB	0x1: MICRON SA0006D10 R3 MT41K25M16HA-107GE 0x2: HYNIX SA0000E840 R3 H5TC4G63AFR-11C						PD 10K PD 15K		
N14P-GT	900 MHz	128M 16* 4 GB	Hynix SA0000Y090			R PD 24.9K			PD 34.8K PH 30.1K		R PD 15K
	900 MHz	256M 16* 4 GB	Micron SA0006D10								



**Resistor Values**

Resistor Value	Pull-up to +3V	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

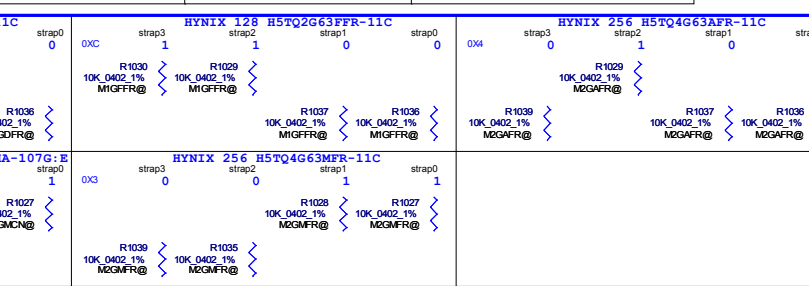
Strap Name	Bit3	Bit2	Bit1	Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	RAM_CFG[2]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GNE3	PCIE_MAX_SPEED	DP_PLL_VDD33V

**SUB\_VENDOR**      **PEX\_PLL\_EN\_TERM**      **FB[1:0]**      **SMB\_ALT\_ADDR**      **VGA\_DEVICE**      **DP\_PLL\_VDD33V**  
 0: No Video BIOS ROM\*      0: Disable\*      0: Reserved      0: 0x9E (Default)\*      0: 3D Device\*      0: Reserved  
 1: BIOS ROM is present      1: Enable      1: Reserved      1: 0x9C (Multi-GPU usage)      1: VGA Device      1: Default\*

**3GIO\_PADCFG[3:0]**      **SOR[3:0]\_EXPOSED**      **PCIE\_SPEED\_CHANGE\_GNE3**      **PCIE\_MAX\_SPEED**  
 0110: GEN1/GEN2 support only\*      Define audio on each      0: Disable PCIE Gen3 operation\*      0: Limit booting to PCIE Gen1  
 0000: GEN3 support      0: Enable display port      0: Enable PCIE Gen3 operation      1: Allow booting to PCIE Gen2/3\*  
 0000: Not in Use\*

**For N14M-GE Binary strap table** Decide ID : 0x1140

GPU	Freq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0	strap4	ROM_SCLK	ROM_SI	ROM_SO
N14M-GE	900MHz	128Mx16x4	0x6: HYNIX SA0000Y090 R3 H5TC2G63DR-11C	PD10K	PH10K	PH10K	PD10K				
	900MHz	128Mx16x4	0x0: HYNIX SA0000H430 R3 H5TC2G63FR-11C	PH10K	PH10K	PD10K	PD10K				
	900MHz	256Mx16x4	0x0: MICRON SA0006D10 R3 MT41K25M16HA-107GE 0x3: HYNIX SA0000E840 R3 H5TC4G63AFR-11C 0x4: HYNIX SA0000E840 R3 H5TC4G63AFR-11C	PH10K PD10K PD10K	PH10K PD10K PD10K	PH10K PD10K PD10K	PH10K PD10K PD10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K



**Table 1. N14M-GE/LE/DDR3 Recommended Memories 128Mx16 Configuration**

Configuration	Vendor	Strap	FBVDD/FBVDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1644E-BC1A	1000	1150	Production ready
				K4W2G1644E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DR-11C	1000	N/A	Production ready
				H5TQ2G63DR-11C	900	N/A	Post-production candidate

**Table 5. N14M-GE/LE and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration**

Configuration	Vendor	Strap	FBVDD/FBVDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1644E-BC1A	1000	1204	Production ready
				K4W2G1644E-BC11	900	1204	Production ready
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JF-093G:K	1000	1234	Production ready
				MT41J128M16JF-107G:K	900	1150	Production ready
Hynix	0x5	1.5V/ 1.5V	H5TQ2G63DR-11C	1000	N/A	Production ready	
			H5TQ2G63DR-11C	900	N/A	Production ready	

**Table 123 Binary Strap Mode Mapping**

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10K Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10K Ω	Pull-up to 3V3 if BIOS ROM exists; Pull-down to GND if no BIOS ROM; Pull-down to GND (no display)
ROM_SO	VGA_DEVICE	10K Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10K Ω	See Note below
STRAP1	RAM_CFG[1]	10K Ω	See Note below
STRAP2	RAM_CFG[2]	10K Ω	See Note below
STRAP3	RAM_CFG[3]	10K Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10K Ω	Pull-down to GND

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**Document Number**      **N14P LVDS 3/7**      **Rev 1.0**

**Customer**      **LA-9535P M/B Schematics**      **Date**      Friday, June 07, 2013      **Sheet**      24      **of**      55



NV 14x DG FBVDDQ(DDR3) GB4-128  
 0.1Ux4, 1Ux4, 4.7Ux4 Under GPU  
 10Ux2, 22Ux2 Near GPU

NV DG PEX\_IOVVD/Q combined  
 1Ux4 Under GPU  
 4.7Ux2 Near GPU  
 10Ux4, 22Ux4 Midway GPU & Power supply

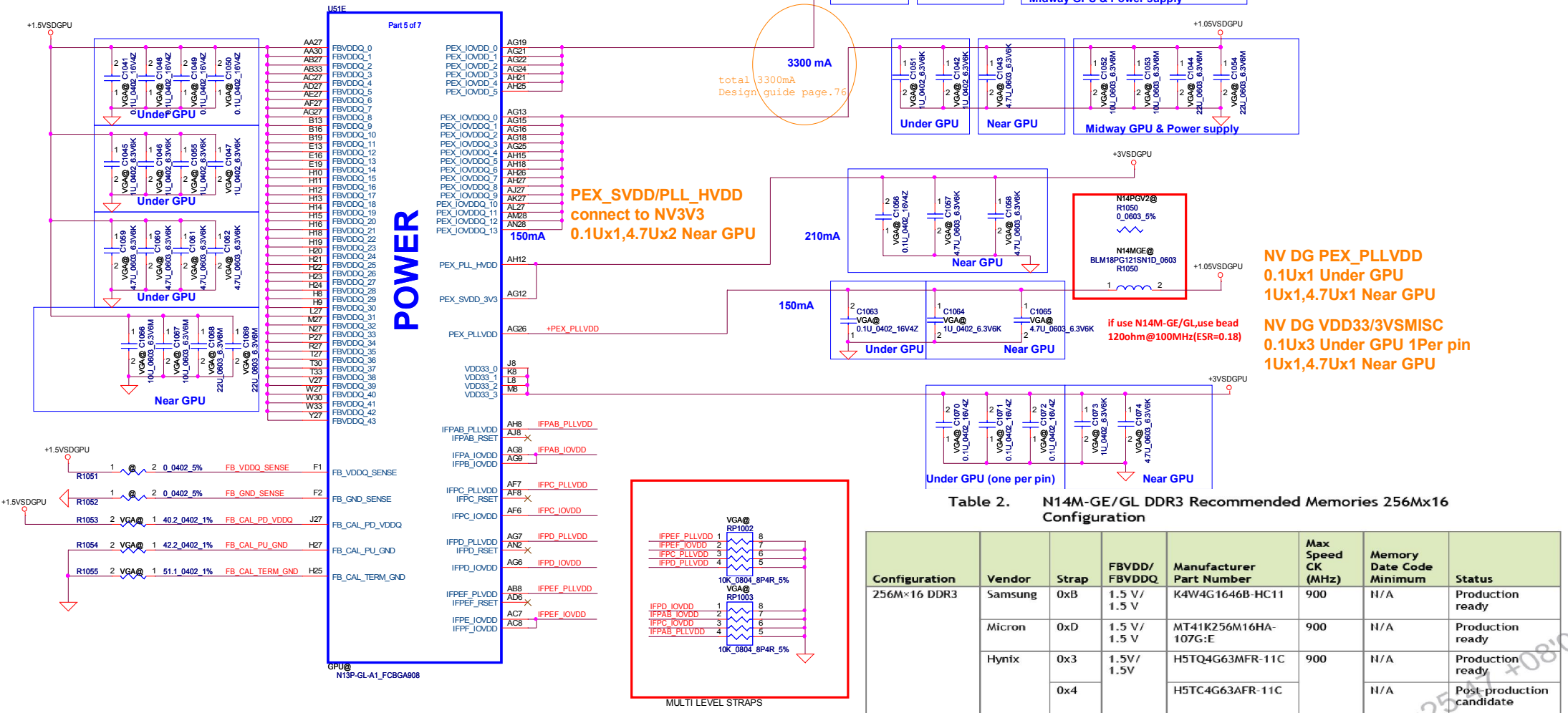
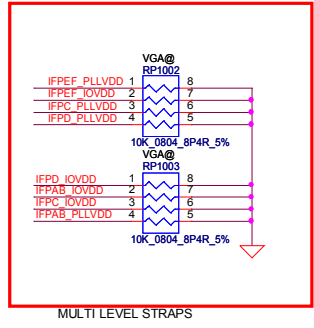


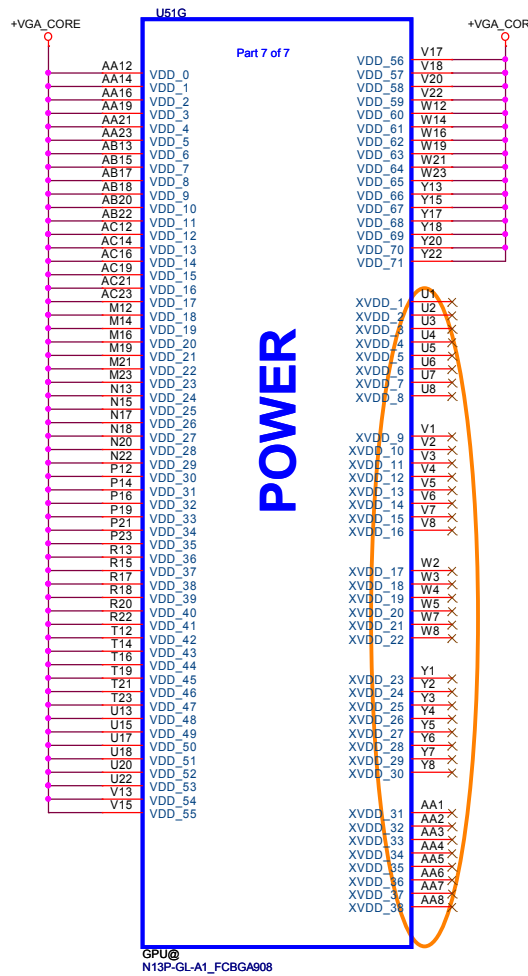
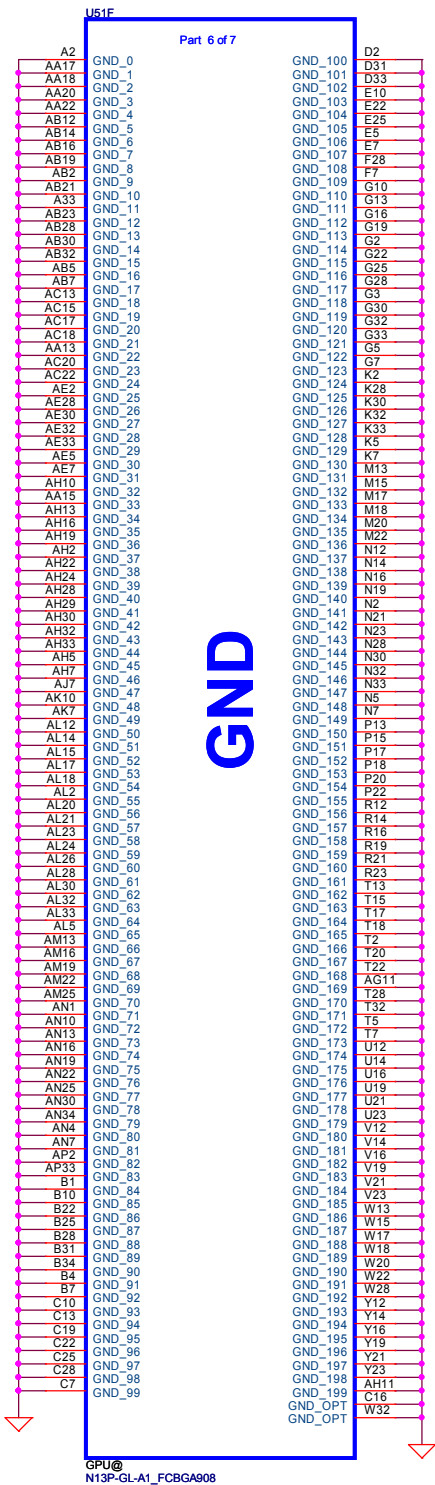
Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0xB	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
		0xD	1.5 V / 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x3	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TC4G63AFR-11C		N/A	Post-production candidate

Table 7. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V / 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
		0x1	1.5 V / 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x2	1.5V / 1.5V	H5TC4G63AFR-11C	900	N/A	Production ready



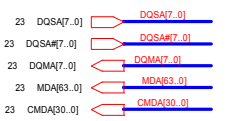


**N14M-GE 35A**  
**N14P-GV2 45A**  
**N14P-GT 55A**

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Size	Custom	Document Number	LA-9535P M/B Schematics	Rev	1.0
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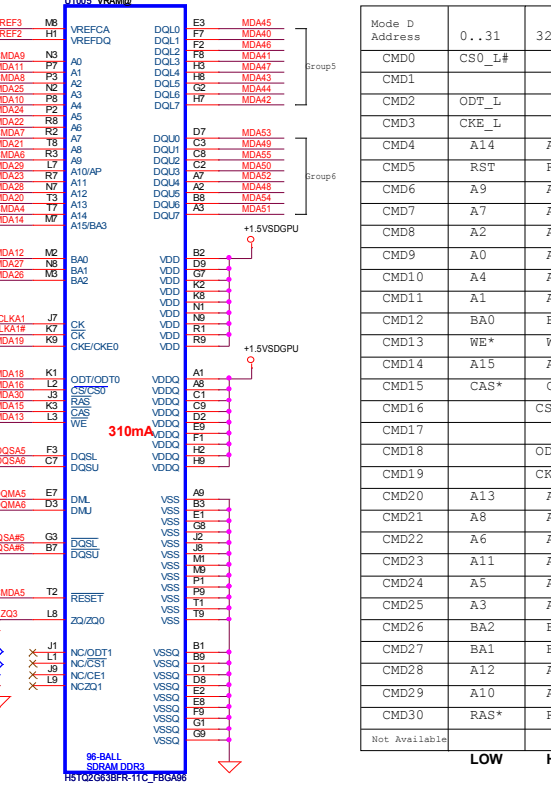
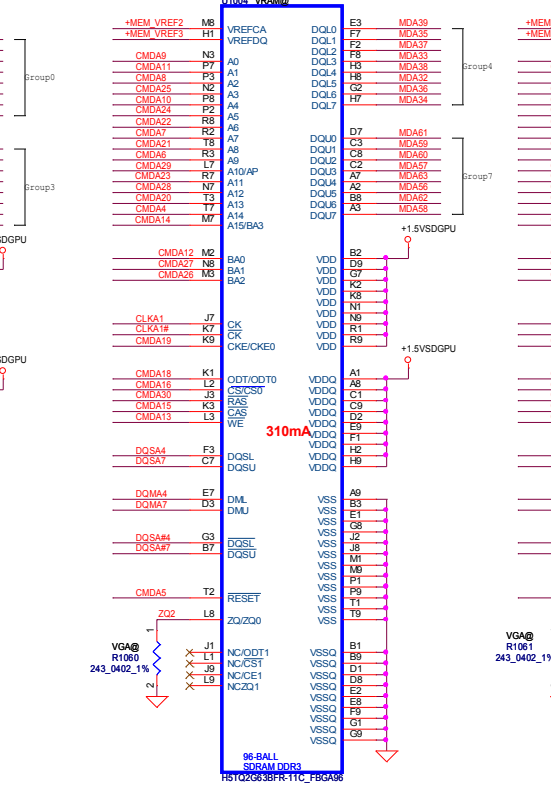
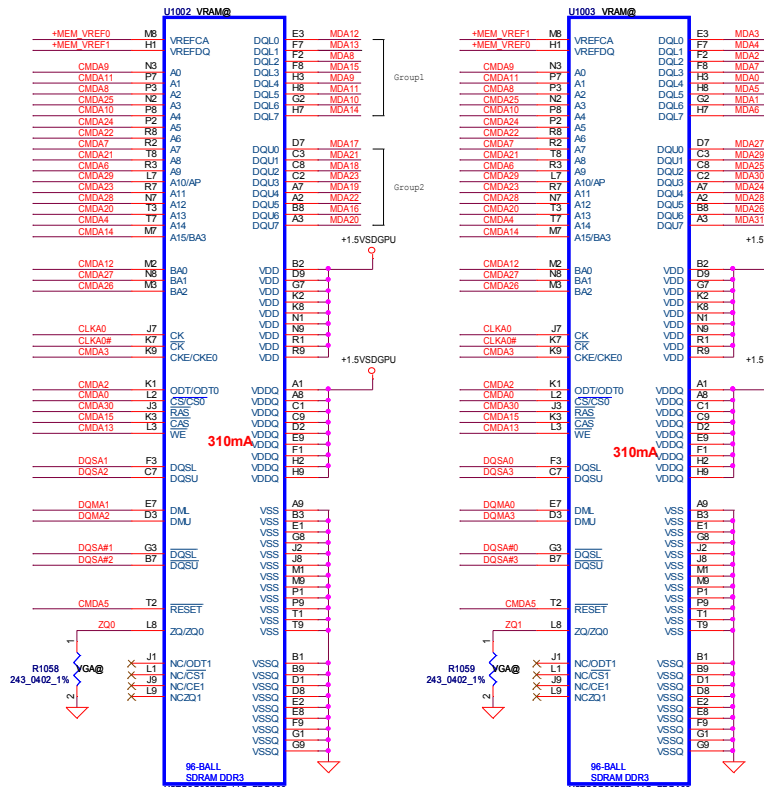
# VRAM DDR3 chips

128Mx16 DDR3 \*8==>2GB  
256Mx16 DDR3 \*8==>4GB

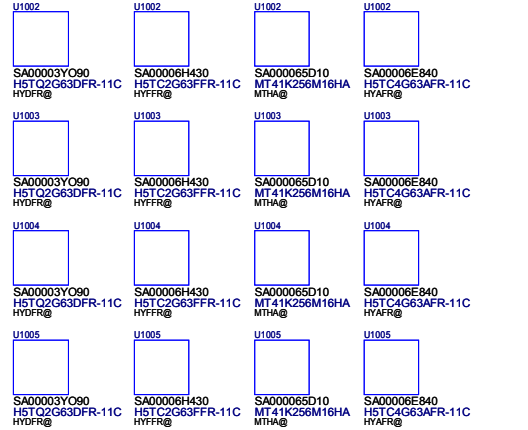
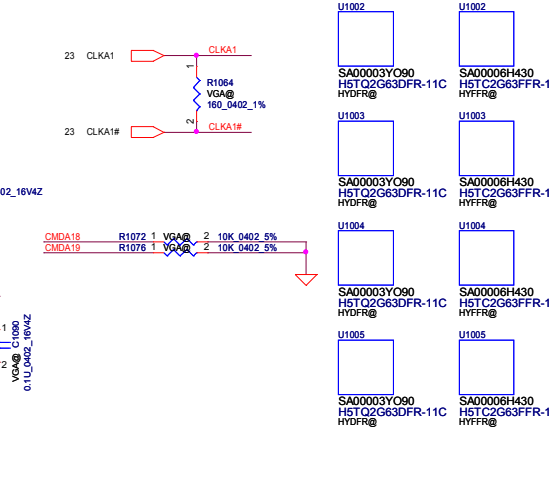
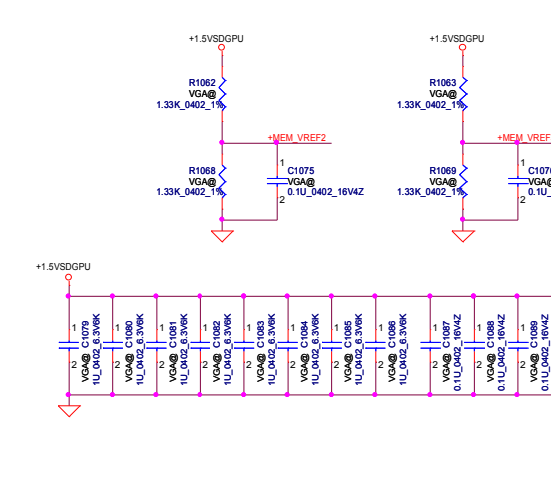
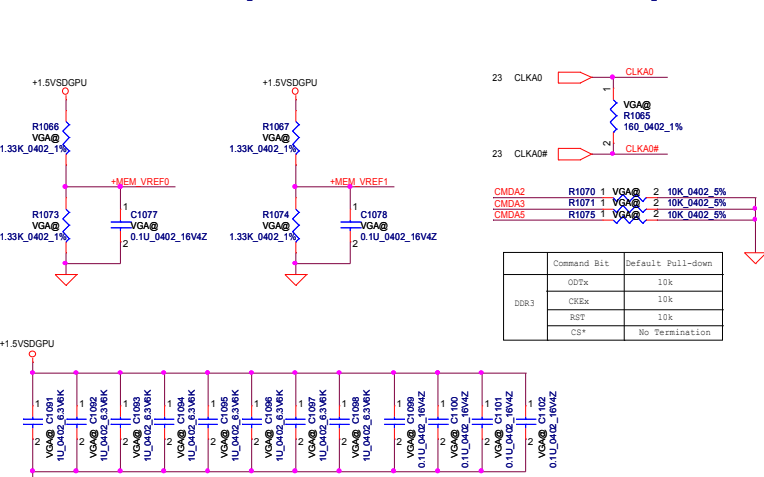


## Low 32

## High 32

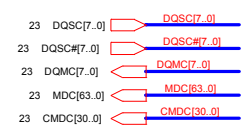


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*



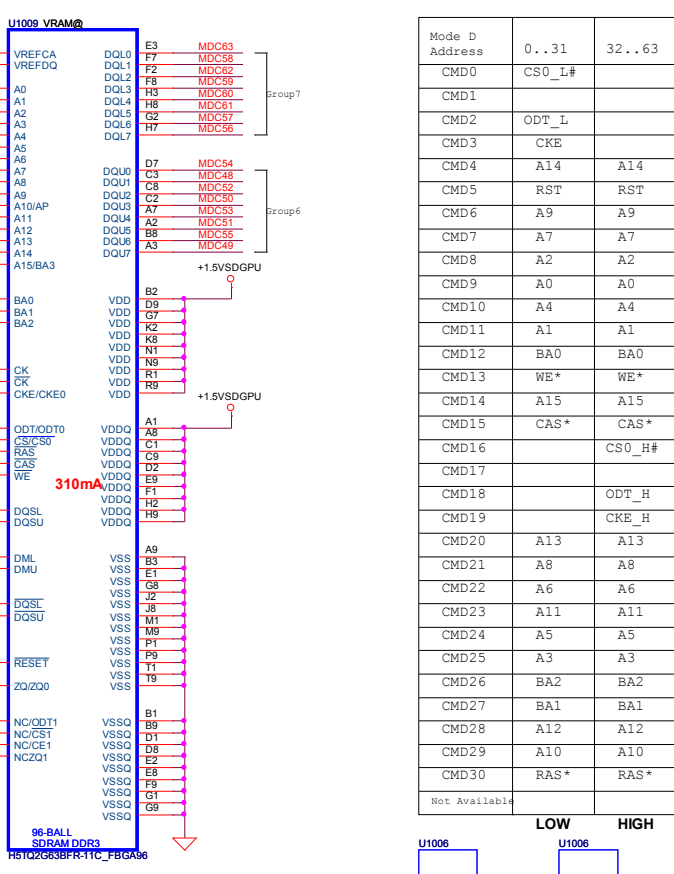
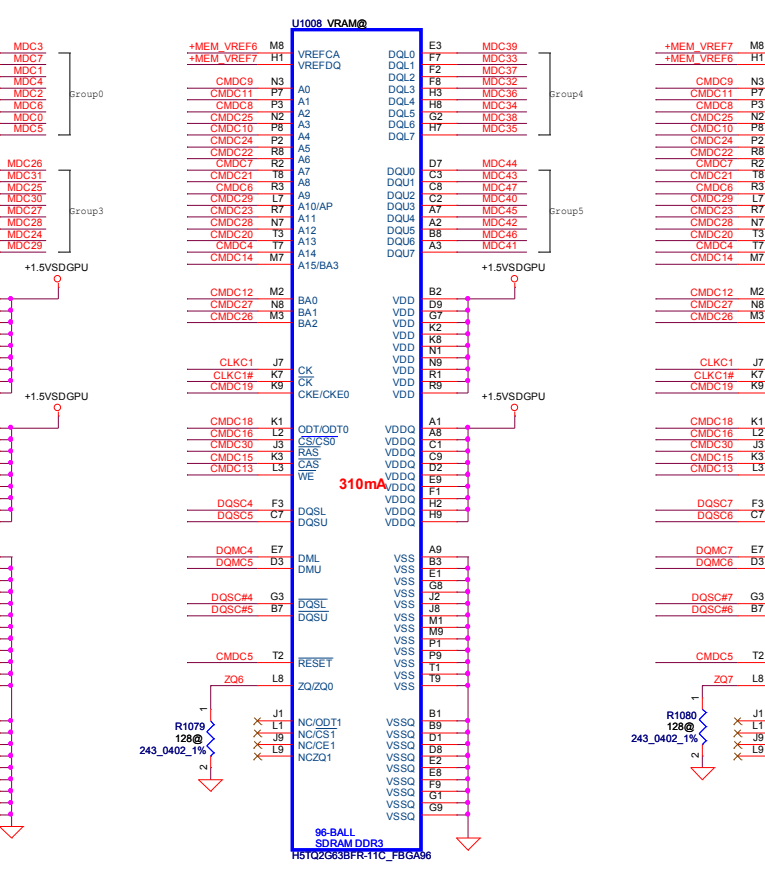
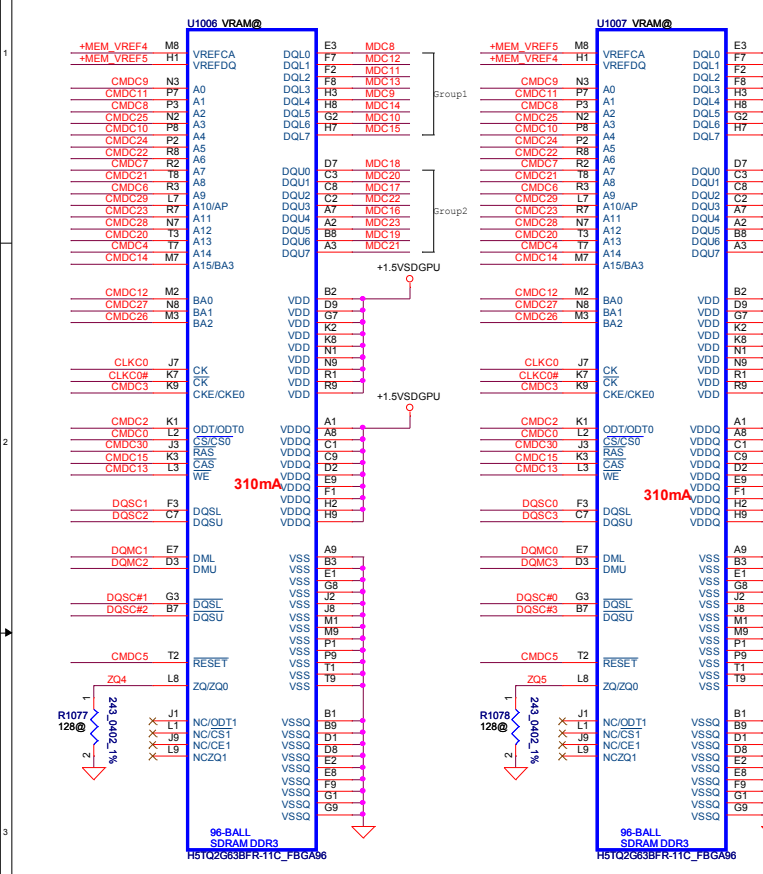
# VRAM DDR3 chips

128Mx16 DDR3 \*8==>2GB  
256Mx16 DDR3 \*8==>4GB

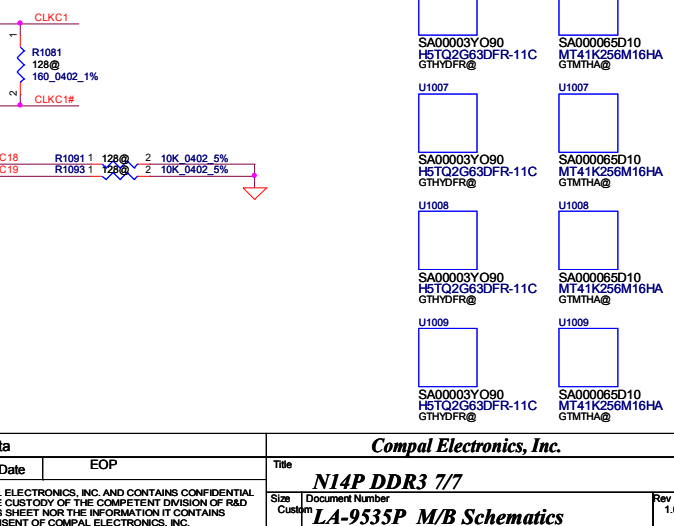
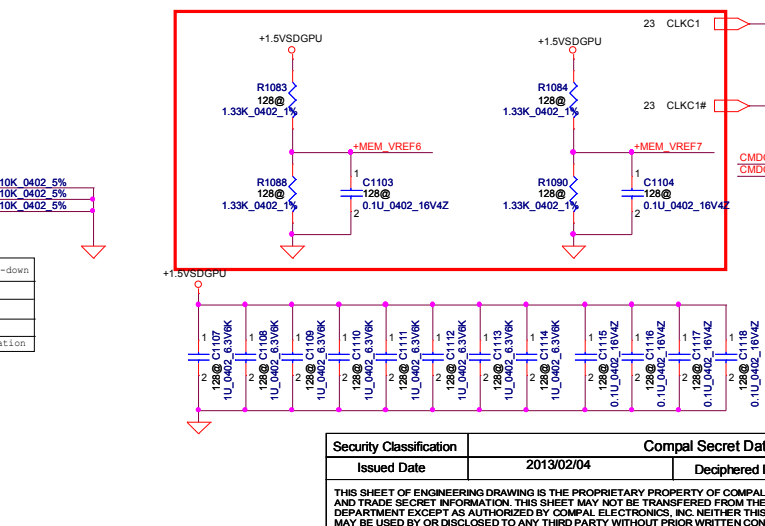
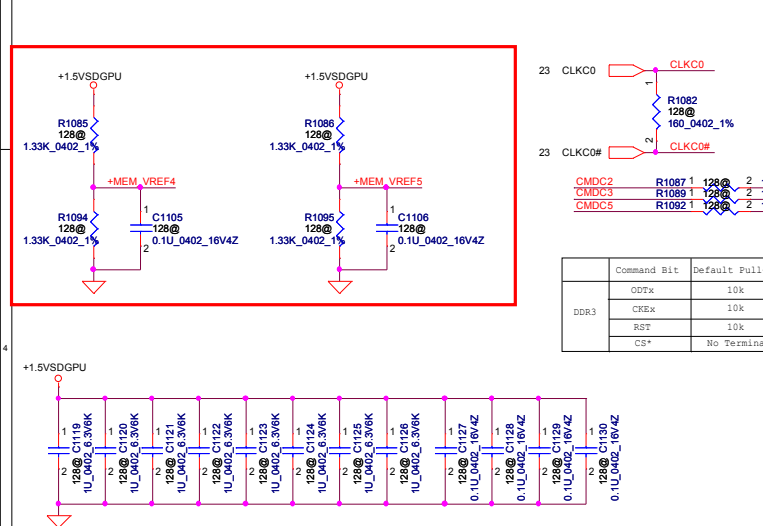


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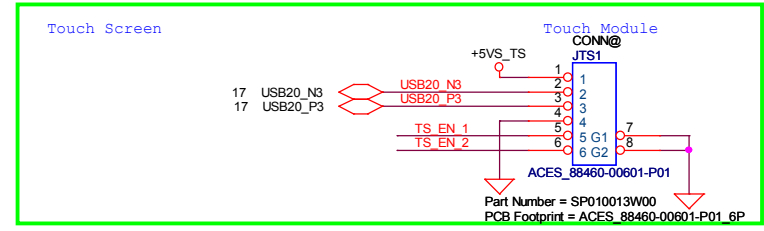
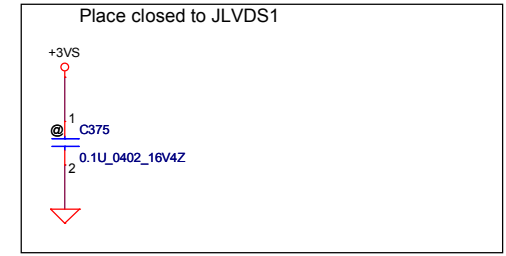
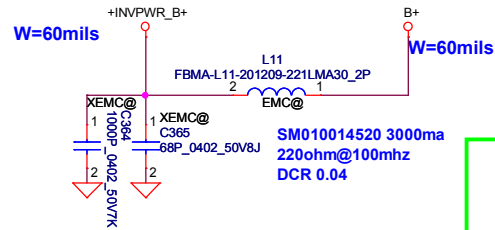
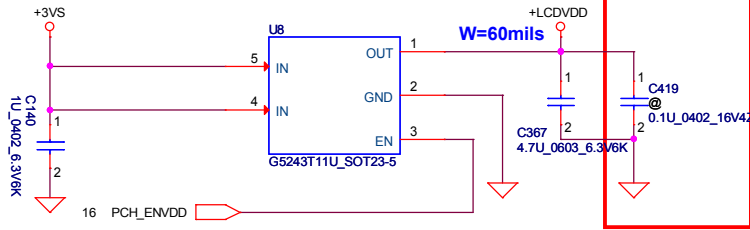
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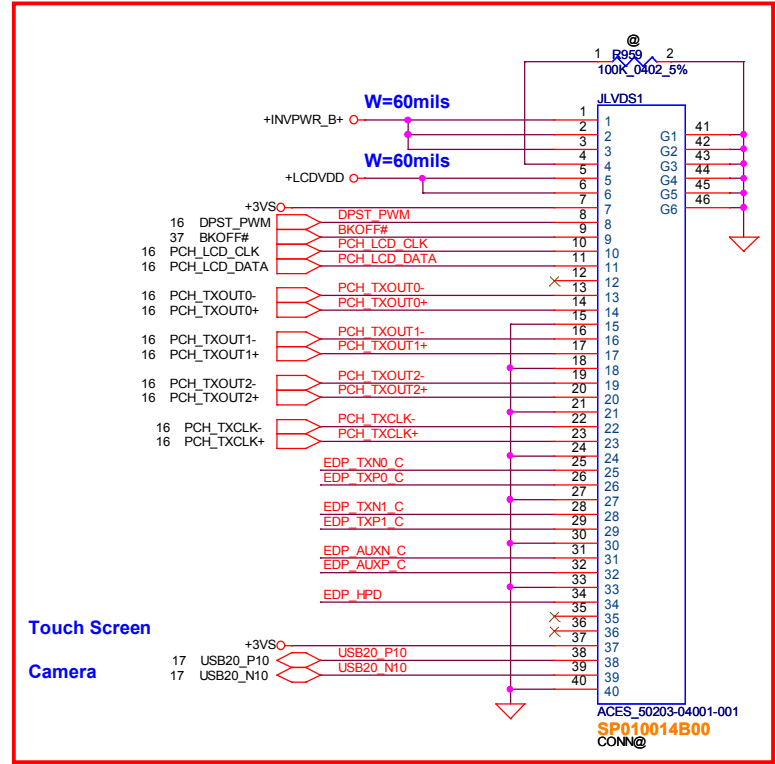
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18	ODT_H	
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		



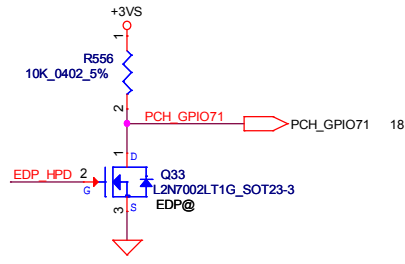
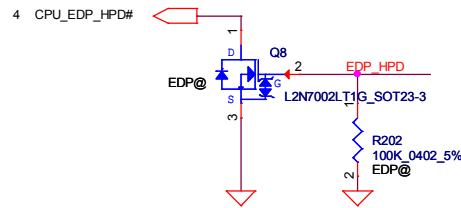
# LCD POWER CIRCUIT



## LCD/LED PANEL Conn.

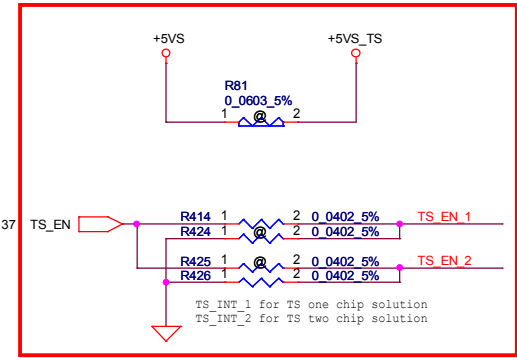
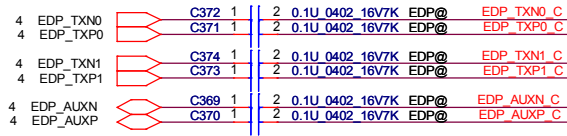


## HPD

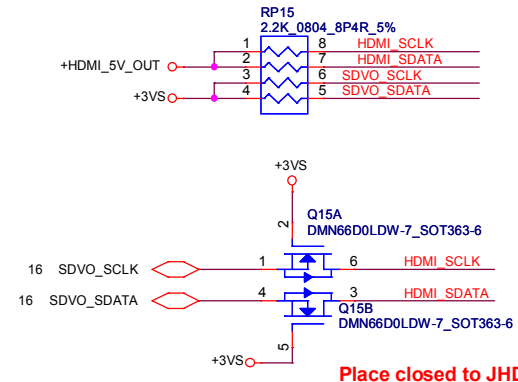
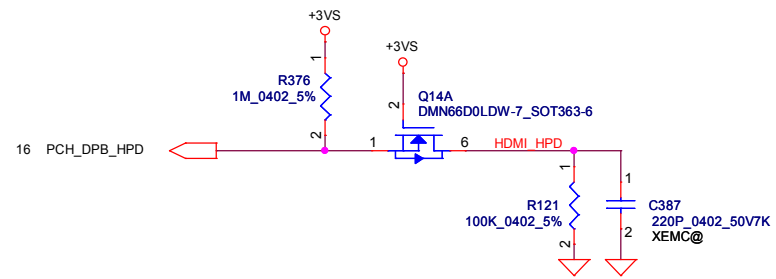
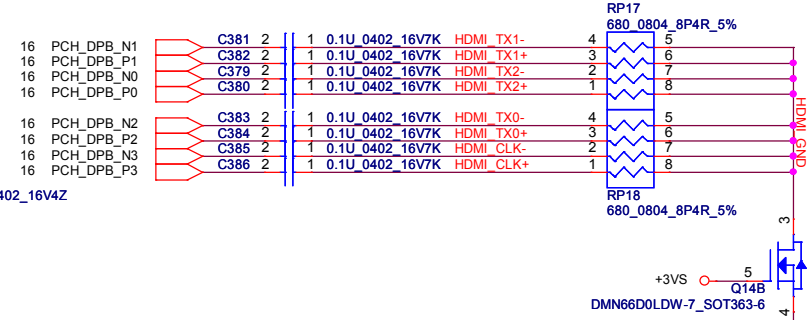
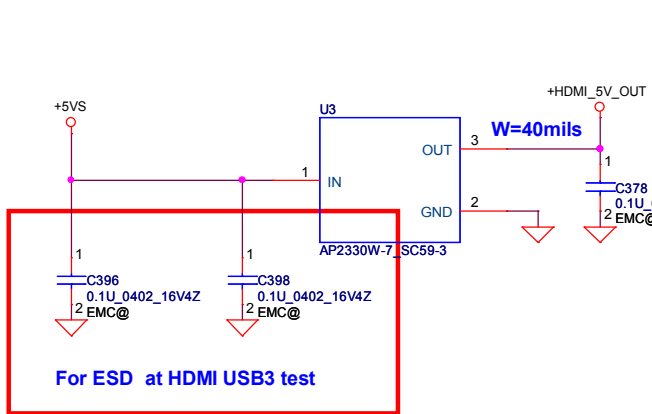


	GPIO71
	PCH_GPIO71
eDP	0
LVDS	1

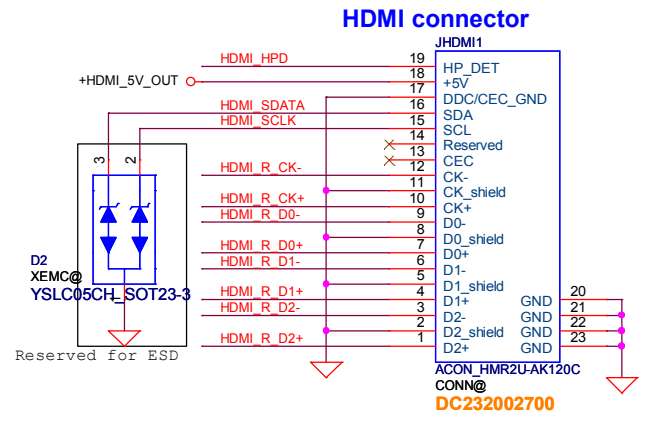
## eDP



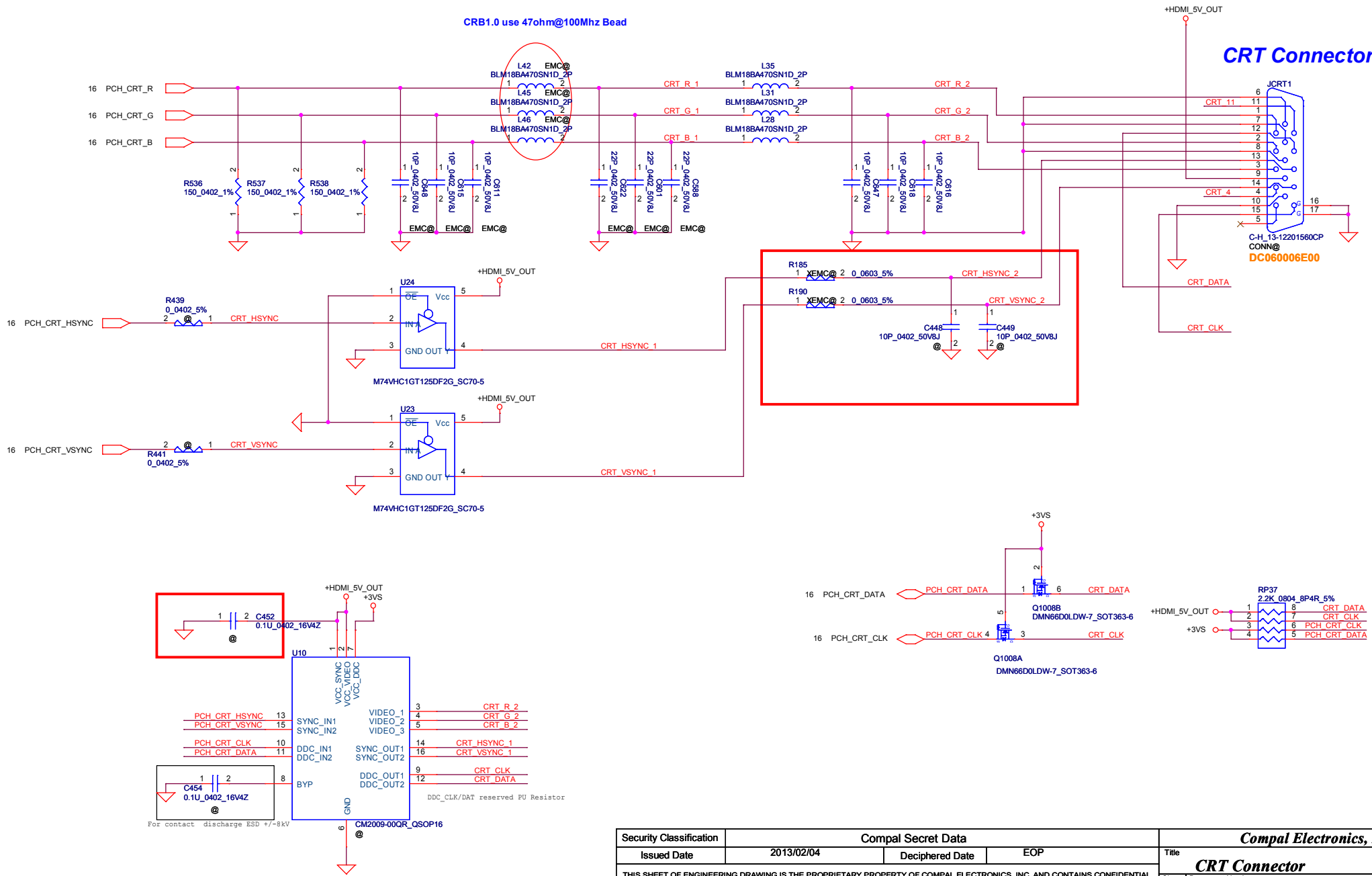
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Issued Date	2013/02/04	Deciphered Date	EOP	Title	eDP Connector
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Place closed to JHDMI1



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Size	Document Number	Date:		Sheet	Rev
Custom	LA-9535P M/B Schematics	Friday, June 07, 2013		30	1.0
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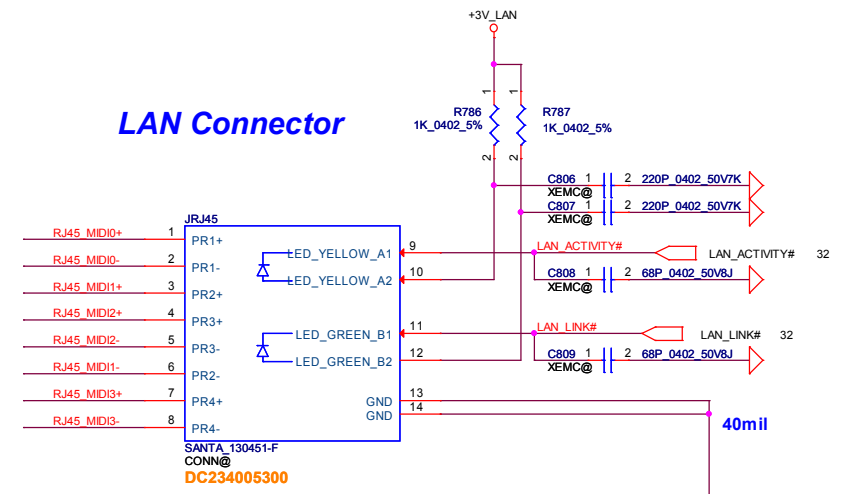
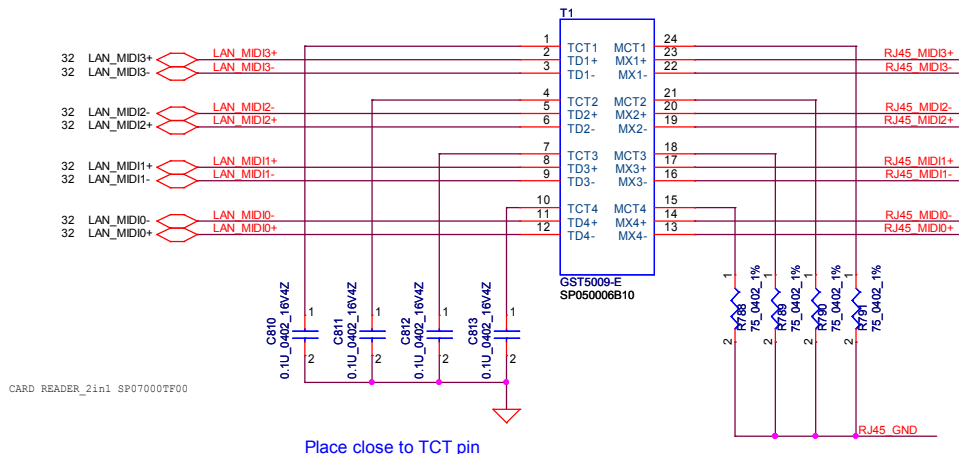
**CRT Connector**

C-HL-13-12201560CP  
CONN  
DC060006E00

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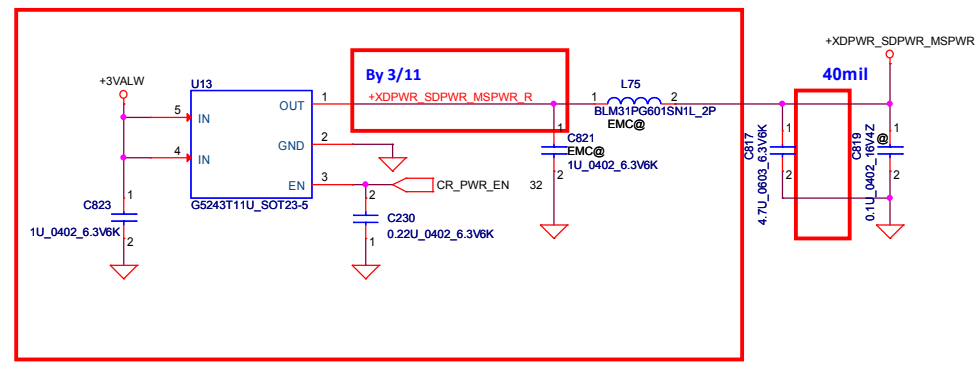
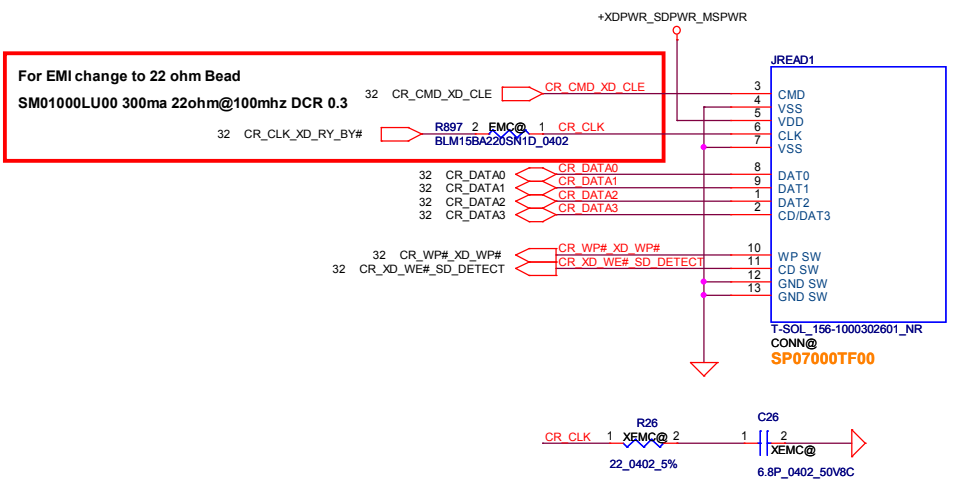






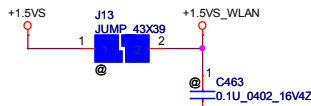
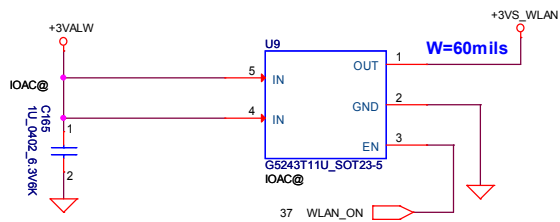
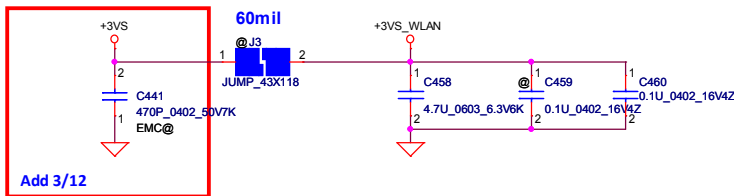
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 TIMAG:S X'FORM\_IH-160 LAN, SP050006F00  
 FCE:S X'FORM\_NS892407 1G, SP050006800

### Card Reader Connector

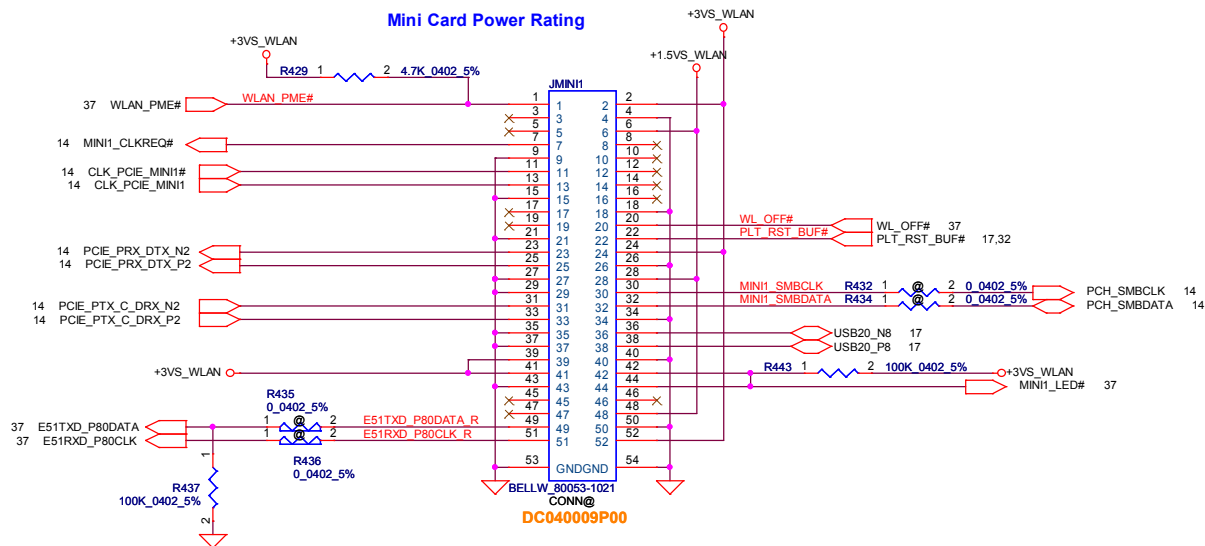


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				Customer	LA-9535P M/B Schematics	1.0
				Date:	Friday, June 07, 2013	Sheet 33 of 55

# For Wireless LAN

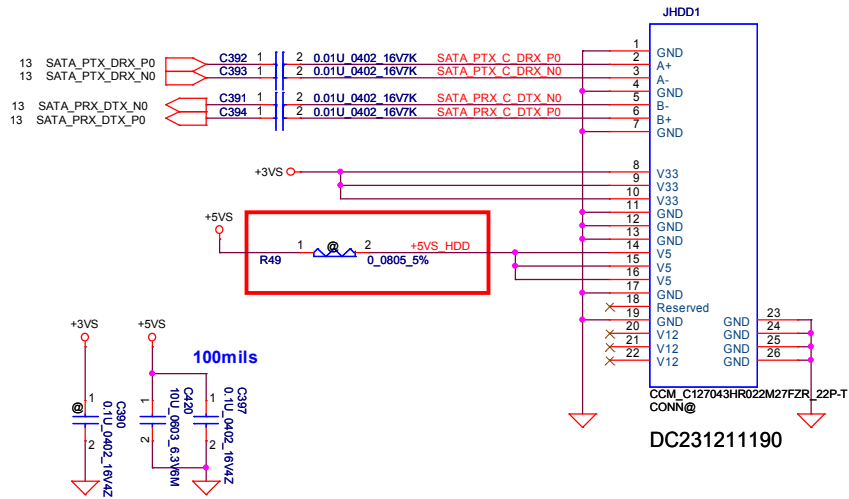


## Mini Card Power Rating

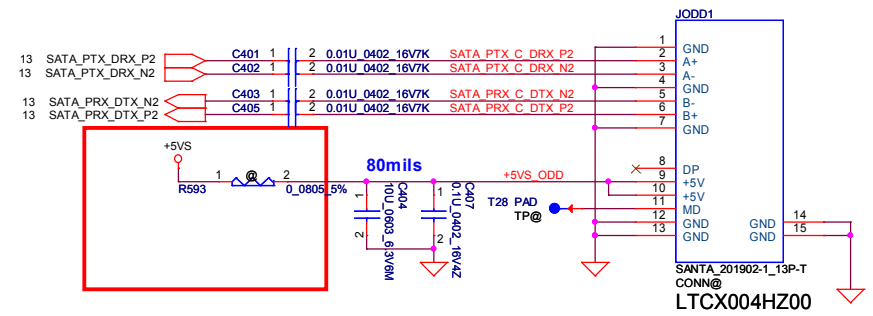


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Date:	Friday, June 07, 2013	Sheet	34	of	55

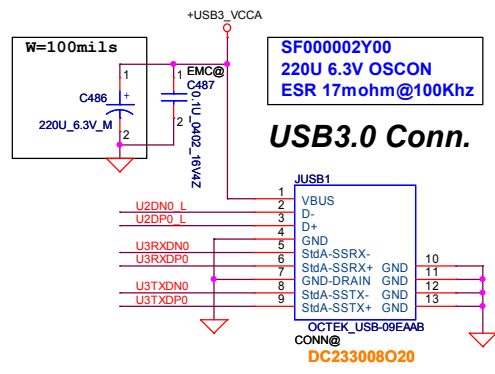
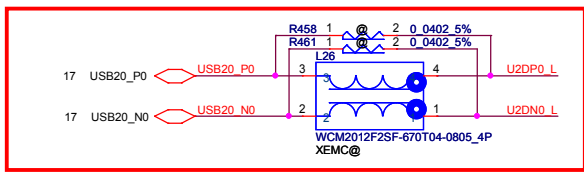
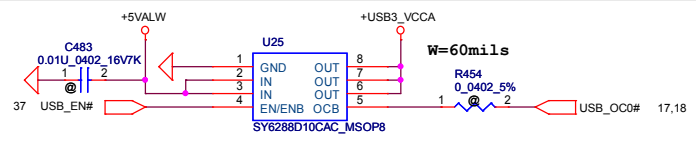
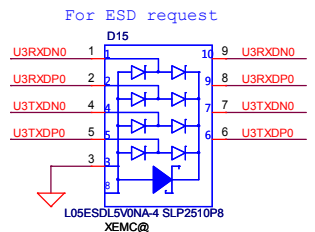
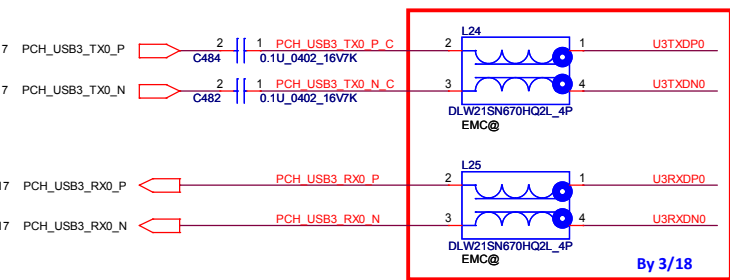
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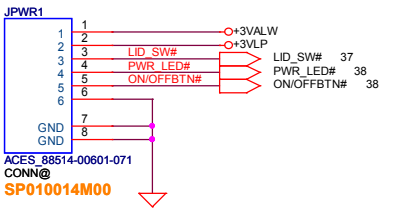
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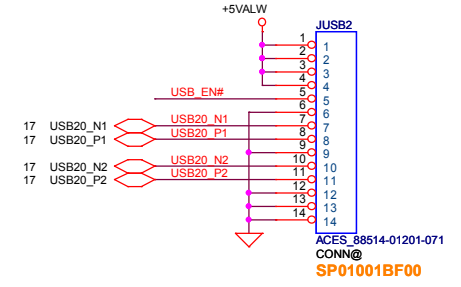
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Issued Date	2013/02/04	Deciphered Date	EOP	Title	<b>HDD/ODD</b>	
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				Customer	<b>LA-9535P M/B Schematics</b>	1.0
				Date:	Friday, June 07, 2013	Sheet 35 of 55



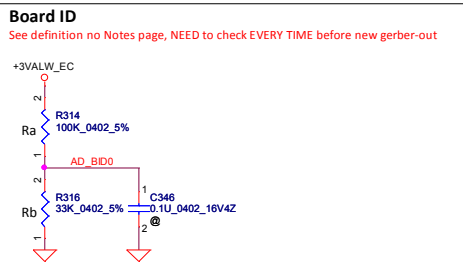
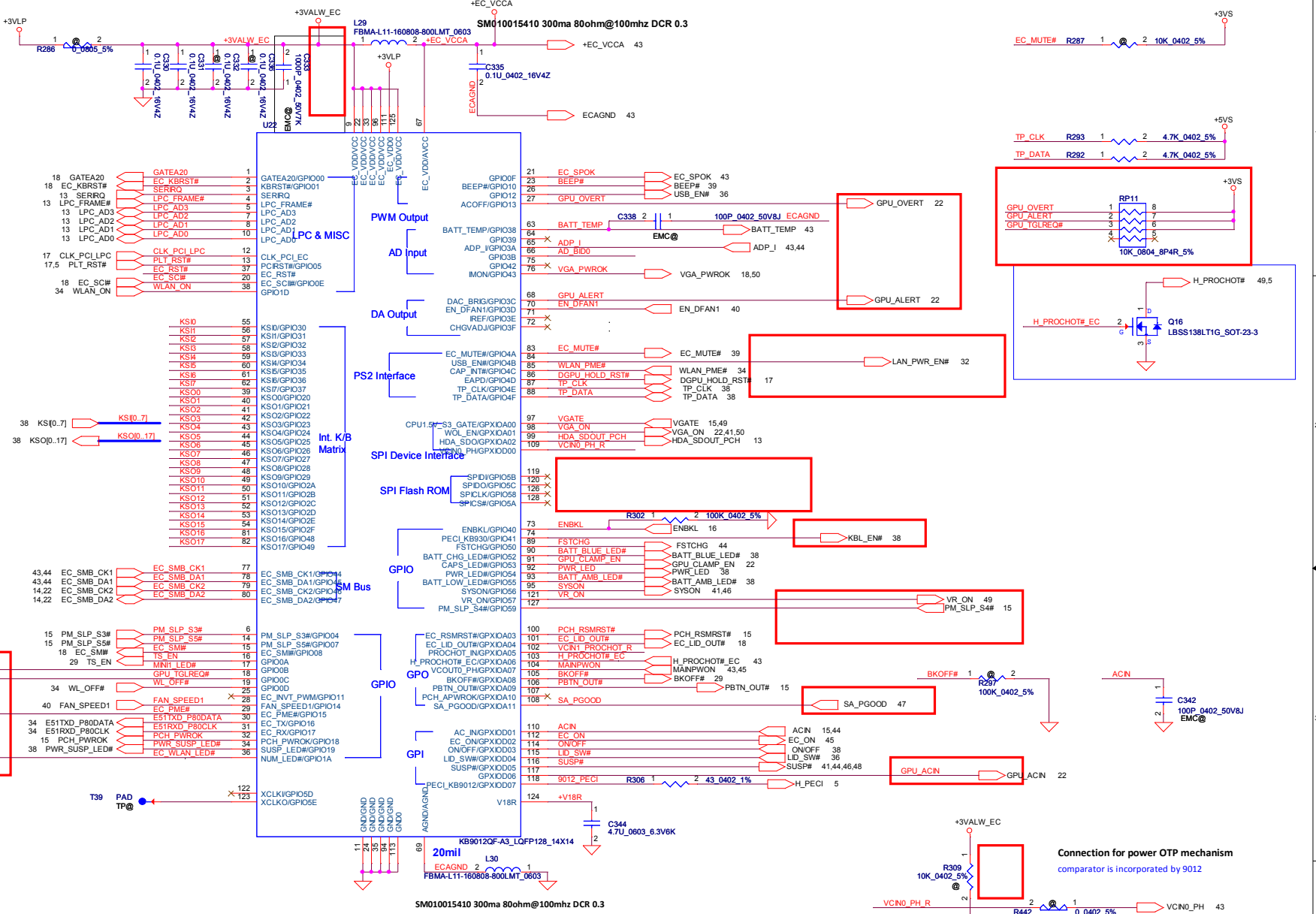
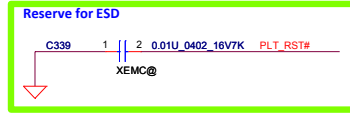
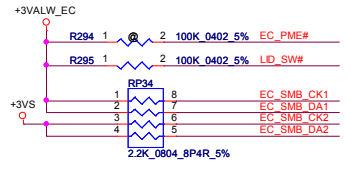
**PWR/B**



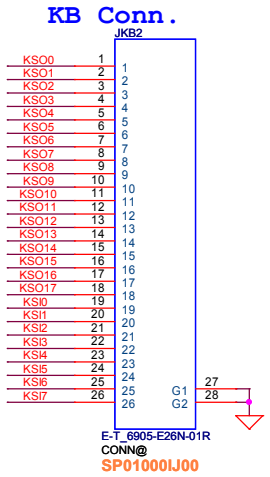
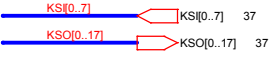
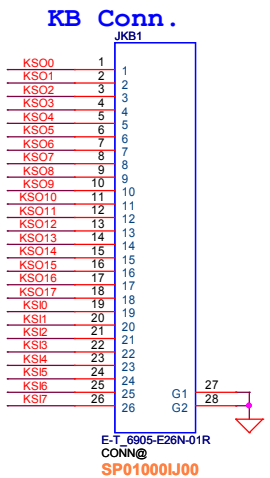
**USB/B  
(USB Port 1, Port2)**



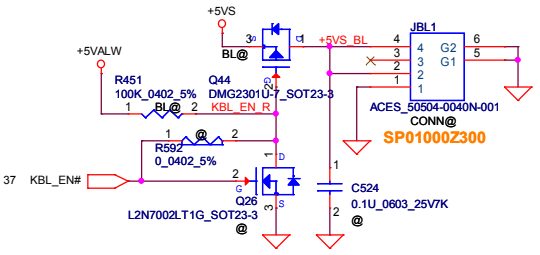
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Issued Date	2013/02/04	Deciphered Date	EOP	Title	USB3.0 Conn/USB B/PWR B	
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				Customer	LA-9535P M/B Schematics	1.0
				Date:	Friday, June 07, 2013	Sheet 36 of 55



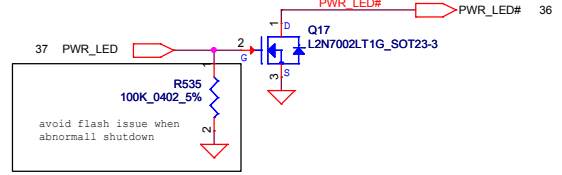
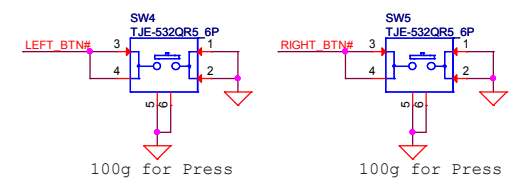
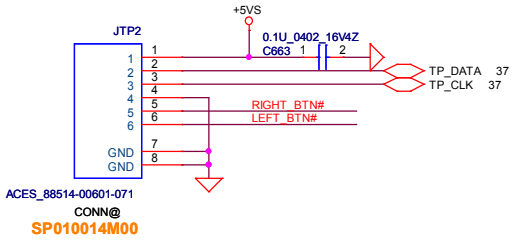
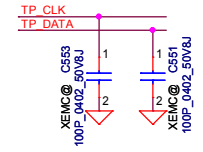
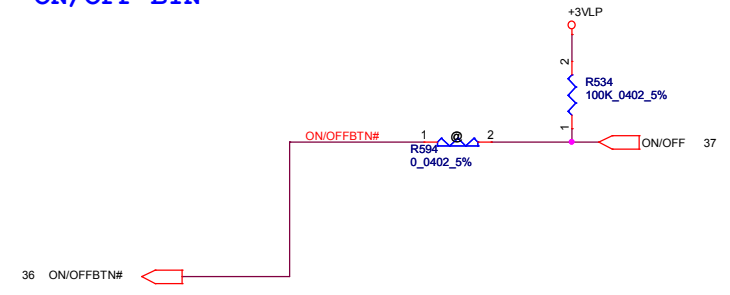
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PVT2	0.3	2	X
MP	1.0	3	X



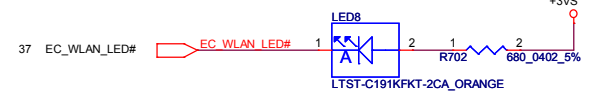
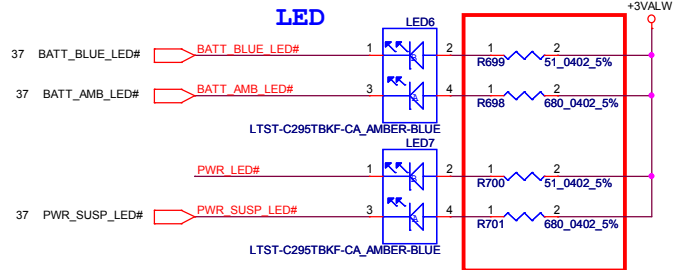
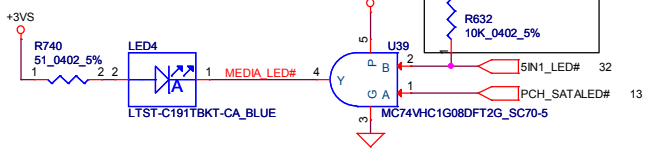
### KB BackLight Conn.



### ON/OFF BTN



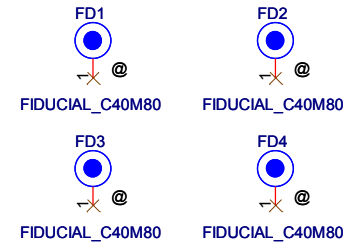
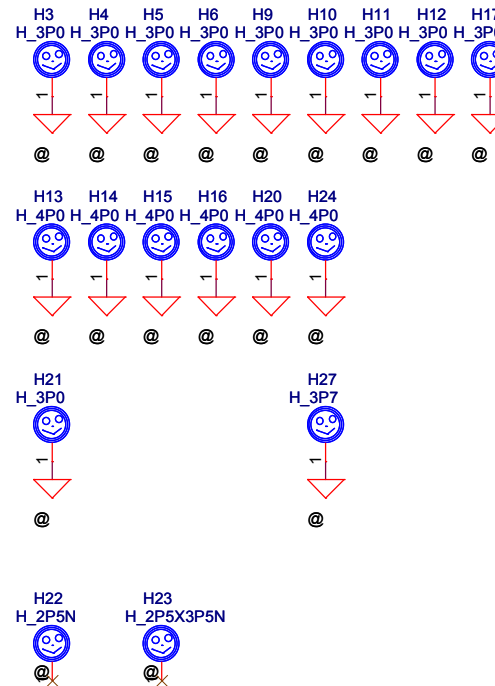
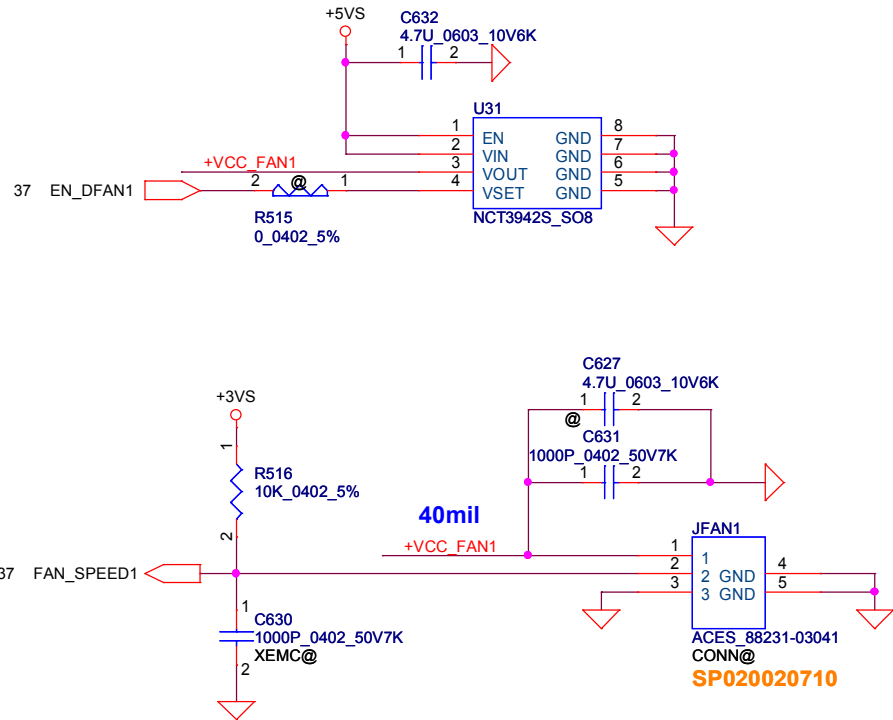
### HDD LED



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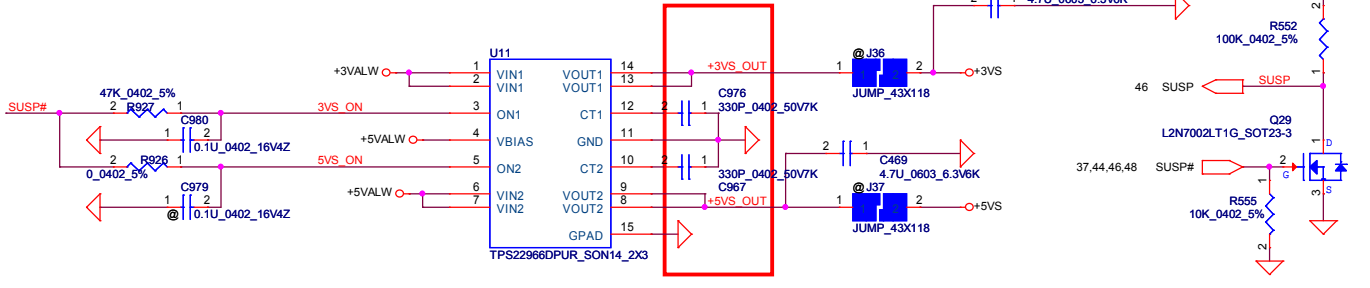
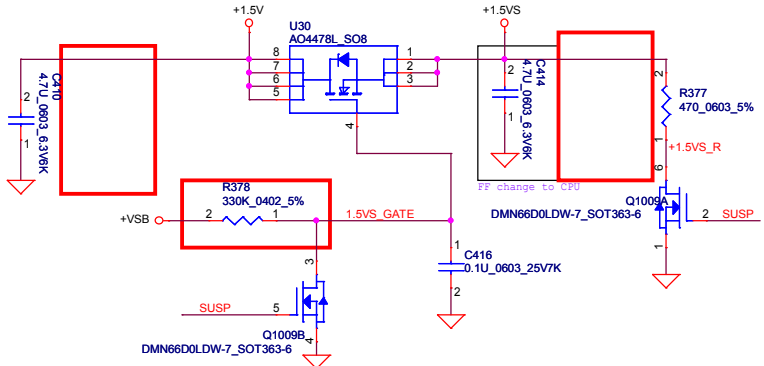
# FAN1 Conn



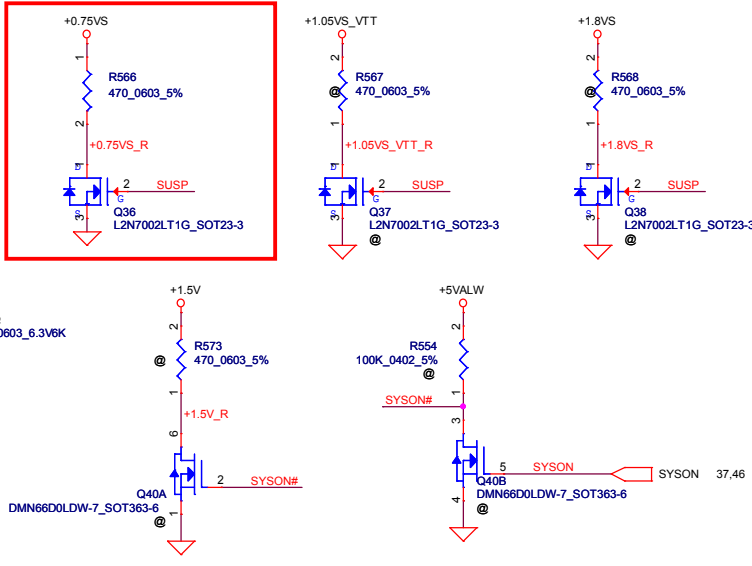
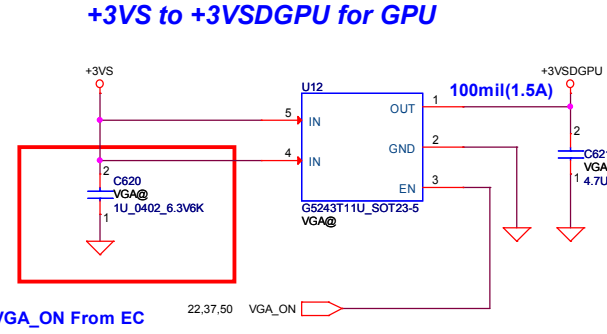
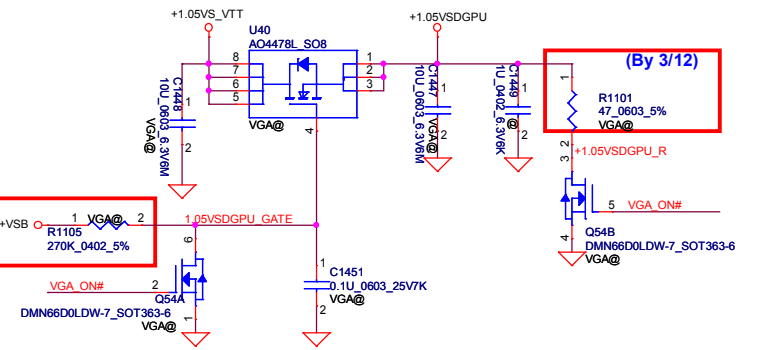
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
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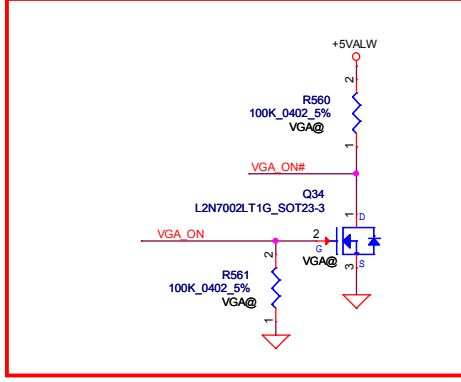
**+1.5V to +1.5VS**



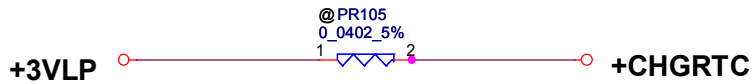
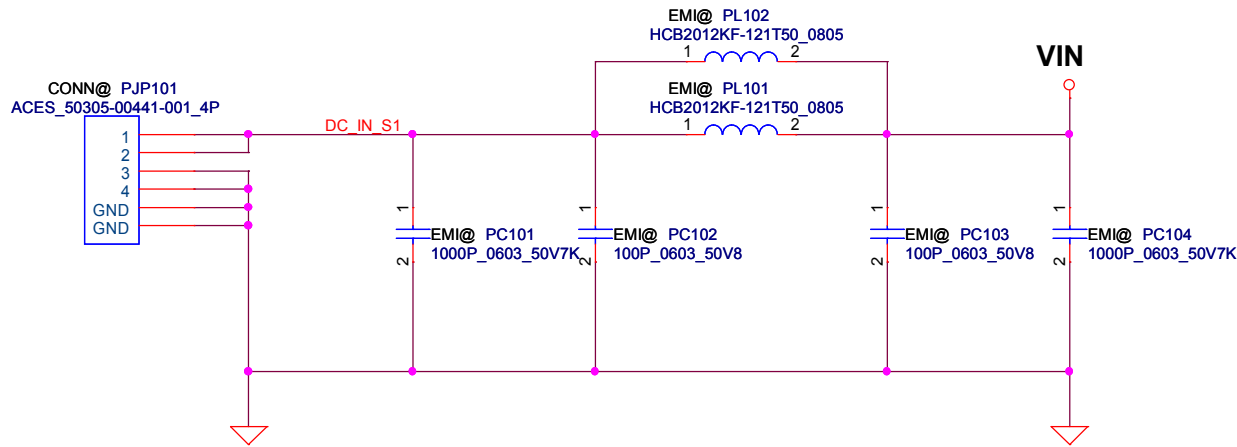
**+1.05VS\_VTT to +1.05VSDGPU**



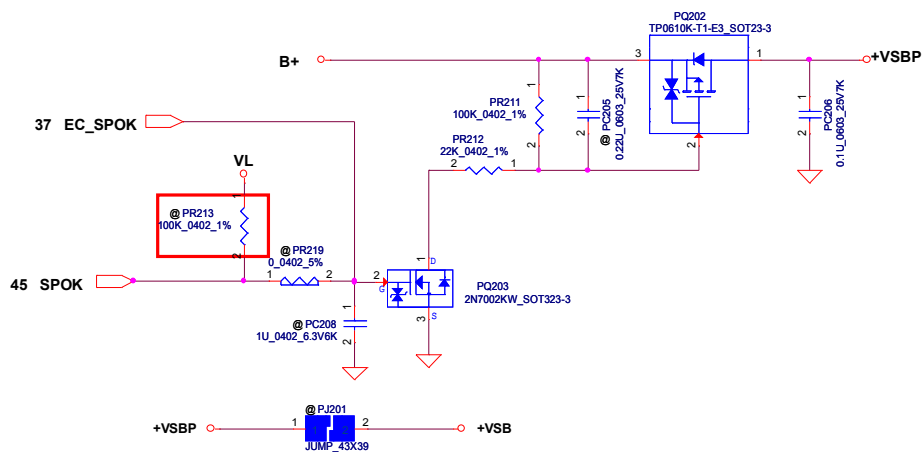
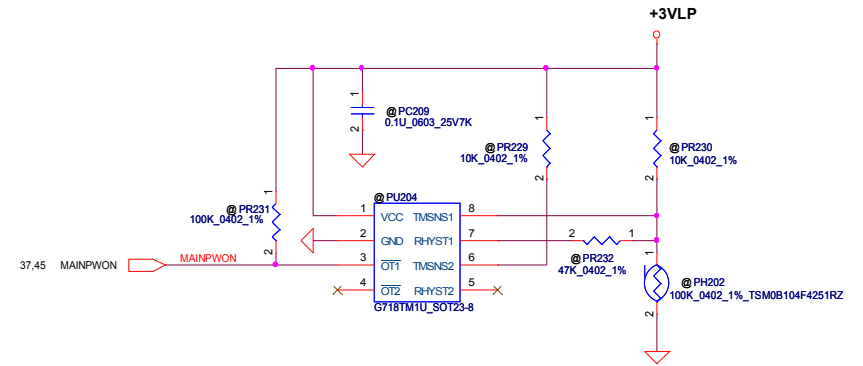
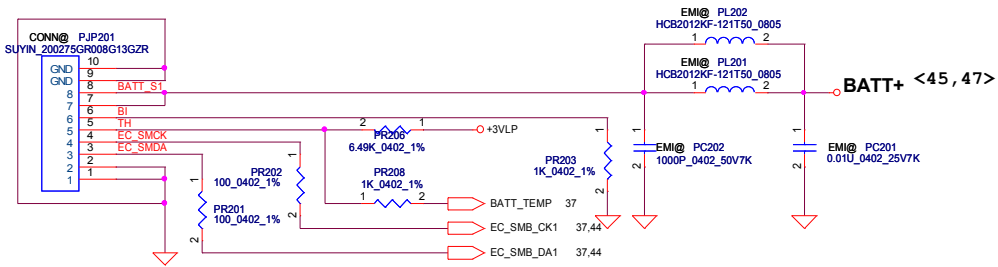
**注意S3 reduce +0.75V sequence**



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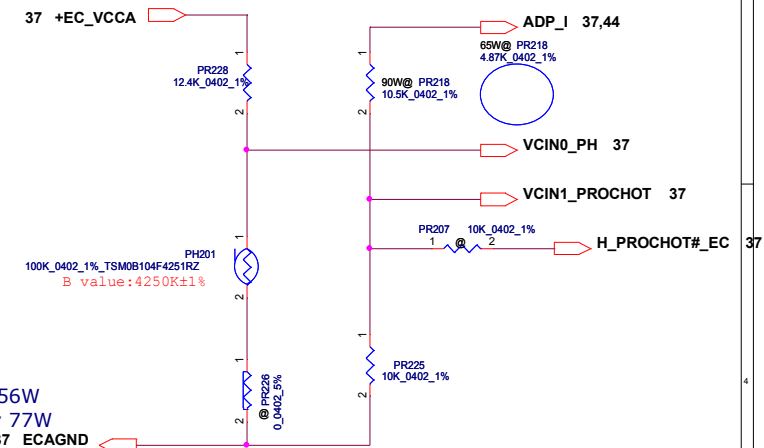
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For KB9012 OTP		
92°C	1.2V, Active	
56°C	2.255V, Recovery	

For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 0.793V
90W	117W, 1.2V	77W, 0.791V
120W		

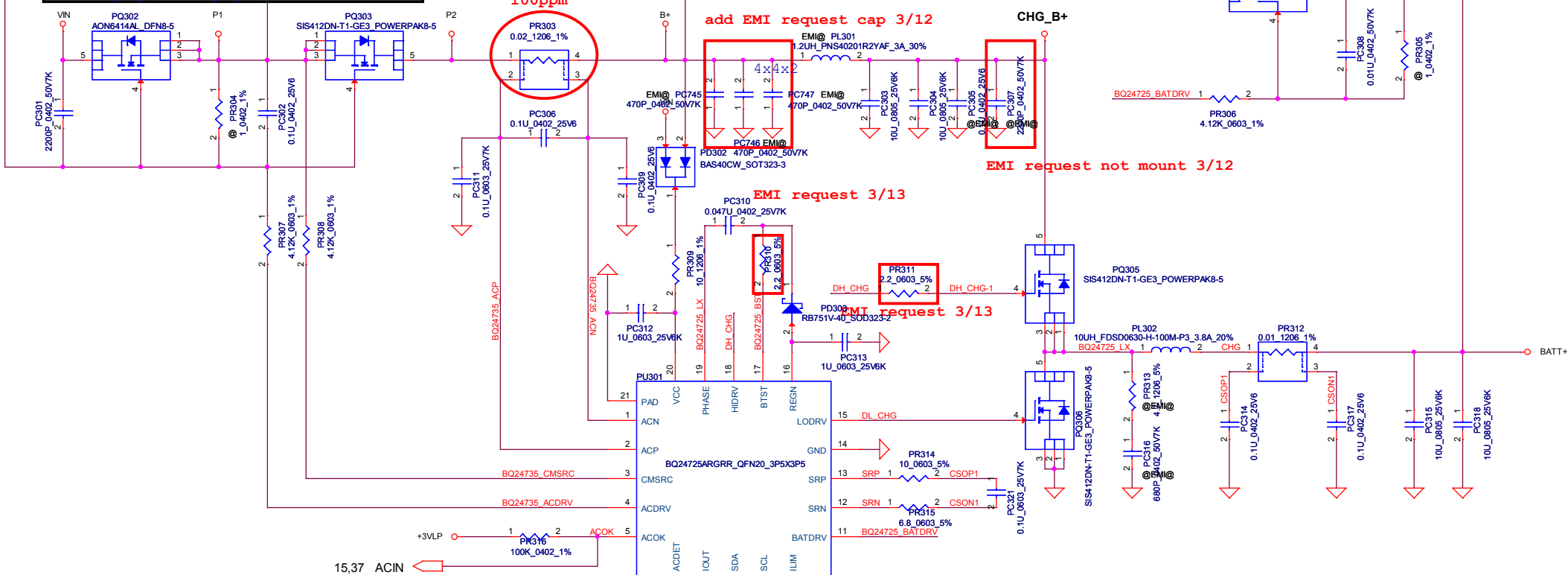
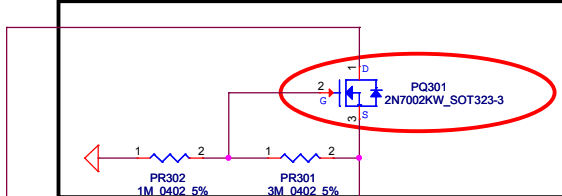
PH201 under CPU bottom side :  
 CPU thermal protection at 92 degree C ( shutdown )  
 Recovery at 56 degree C



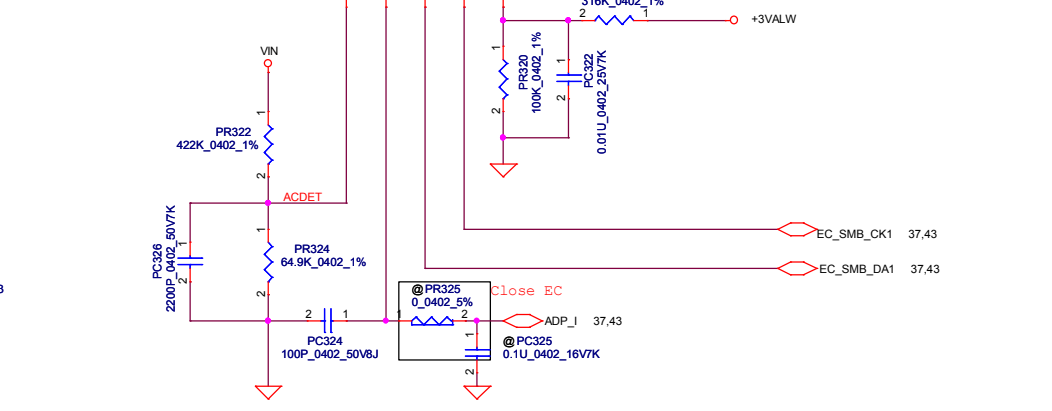
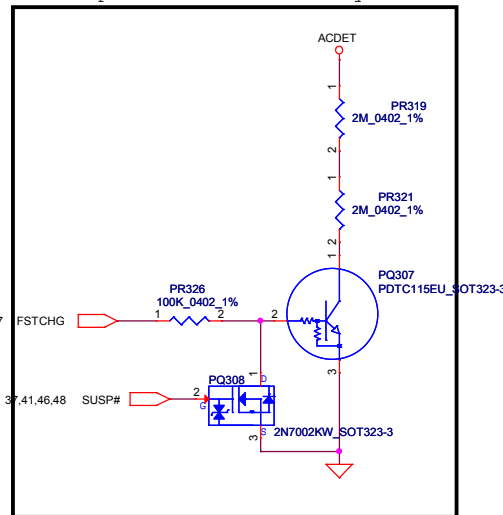
For 65W adapter ==> action 84W , Recovery 56W  
 For 90W adapter ==> action 117W , Recovery 77W

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for reverse input protection

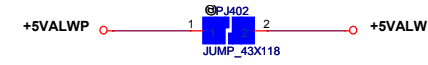
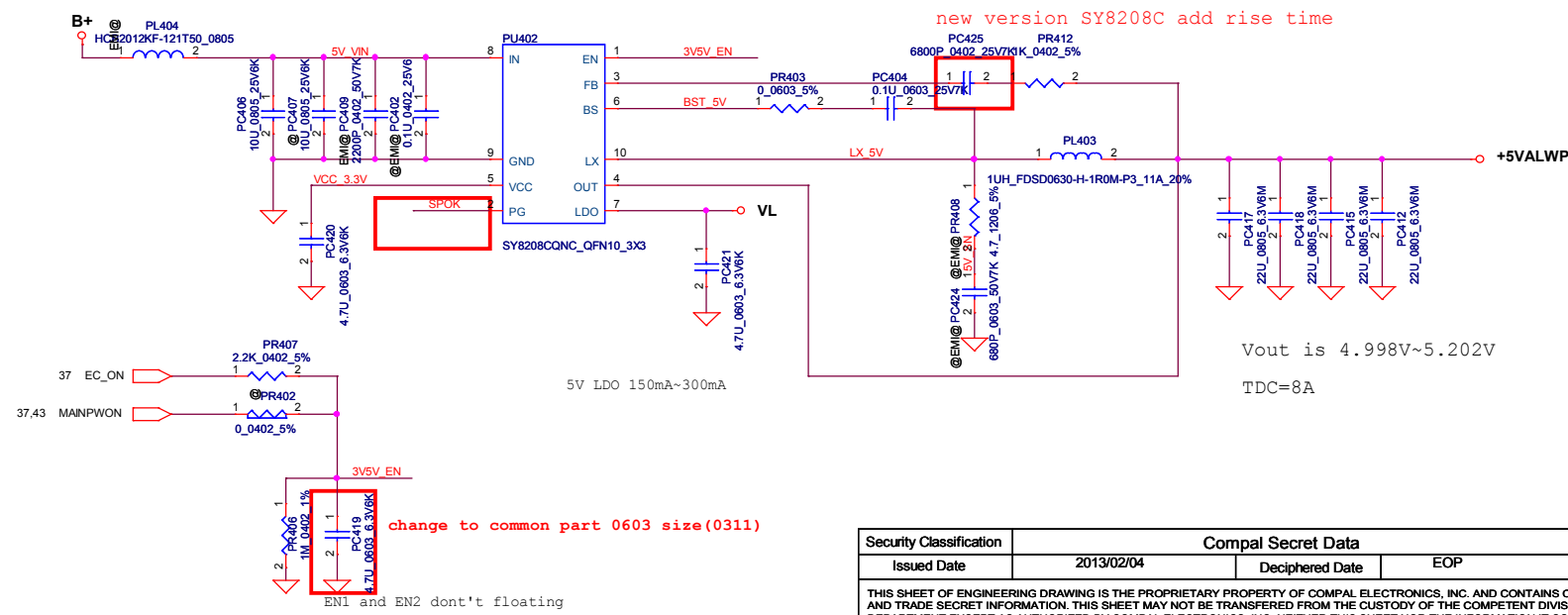
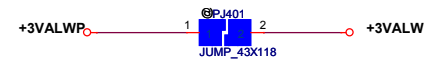
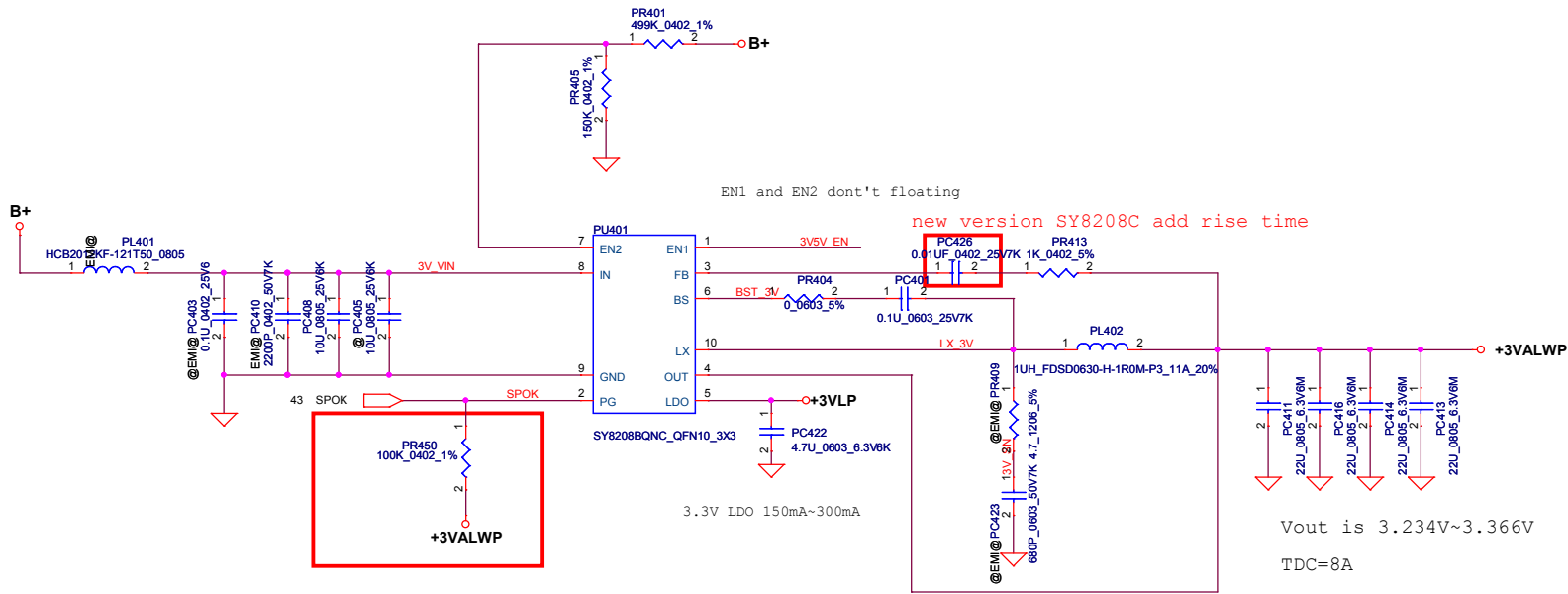


For 4S per cell 4.35V battery



Vin Detector			
	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V
ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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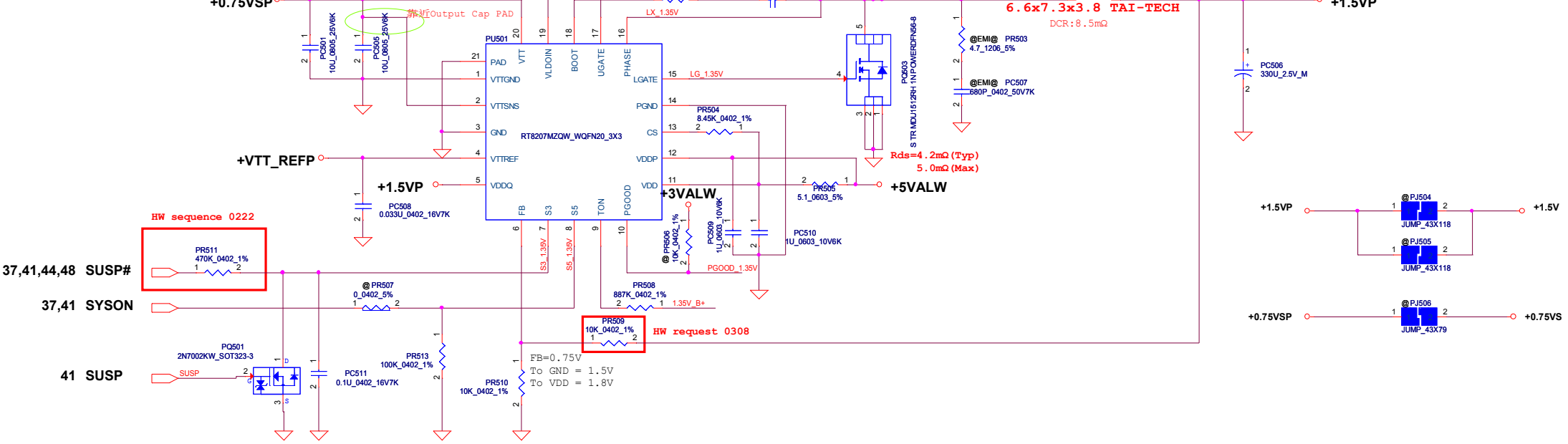
Security Classification	Compal Secret Data			Title	
Issued Date	2013/02/04	Deciphered Date	EOP	3VALW/5VALW	
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```

+1.35VP
Ipeak = max{ 0.7*Ibudget, 1st +2nd max loading}
Ipeak = max{ 12.34*0.7 , 4.2+8.14 }
Ipeak=12.34A ; 1.2Ipeak=14.808A ; Imax=8.638A
1/2Delta I=0.7353A (F=300K Hz)
PR504=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2/9uA=8.45Kohm
choose PR504=8.45Kohm (for safety >1.2Ipeak)
Rds(on)=5.0m ohm(max) ; Rds(on)=4.2m ohm(typical)
Ilimit_min=(8.366K*9uA) / (5.0m*1.2)=15.058A
Ilimit_max=(8.535K*11uA) / (4.2m*1.2)=22.352A
Iocp=Ilimit+1/2Delta I=15.79A~23.09A
Iocp(min)>1.2Ipeak
  
```

2012/9/6

OVP=110% 115% 120%



- 37,41,44,48 SUSP#
- 37,41 SYSON
- 41 SUSP

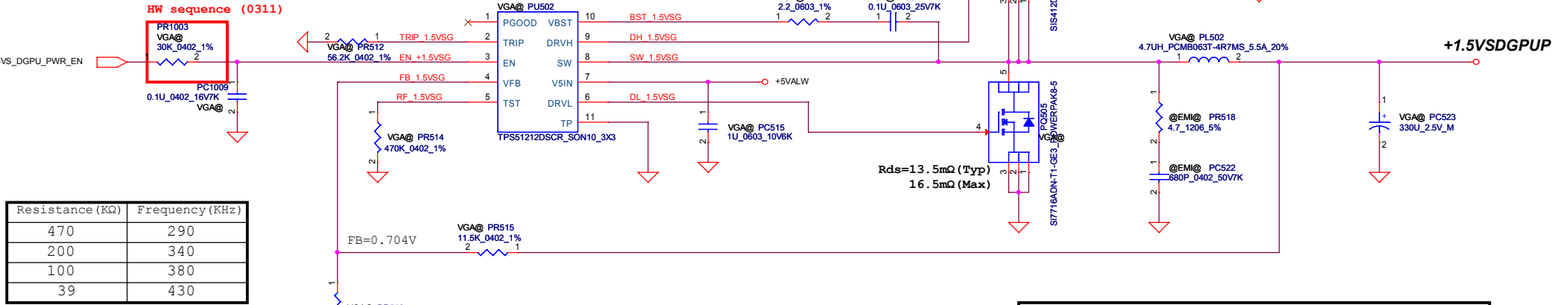
STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

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$V_{FB} = 0.704V$   
 $V_o = V_{FB} * (1 + 11.5K/10K) = 1.5V$   
 $Freq = 290KHz (typ)$   
 $C_{esr} = 15m\ ohm$   
 $I_{peak} = 4.7A$   $I_{max} = 3.29A$   $I_{ocp} = 5.64A$   
 $I_{ocp} = 5.72A \sim 6.43A$

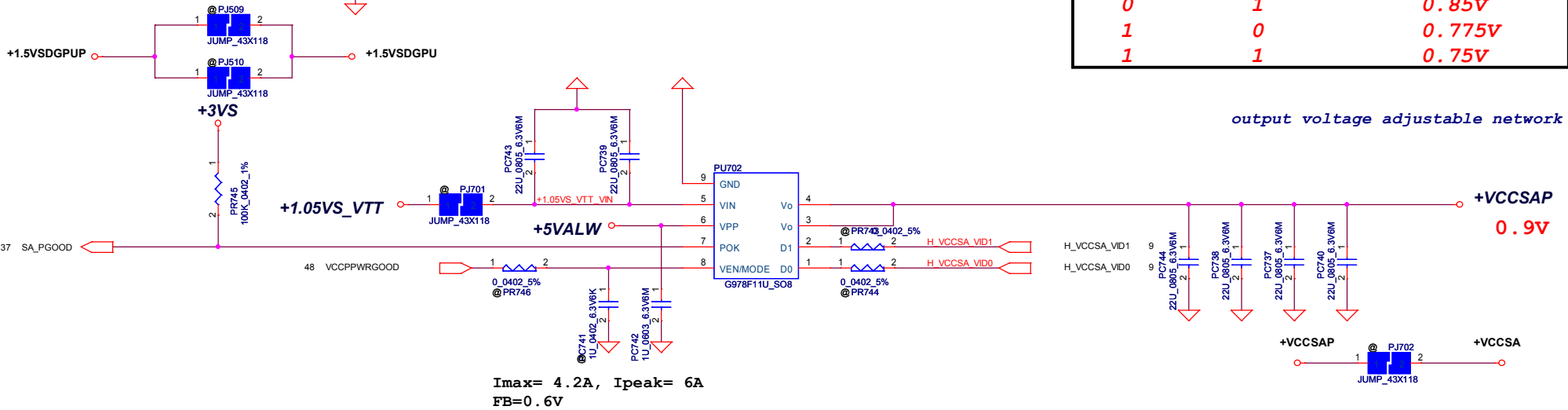
HW sequence (0311)



Resistance (KΩ)	Frequency (KHz)
470	290
200	340
100	380
39	430

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

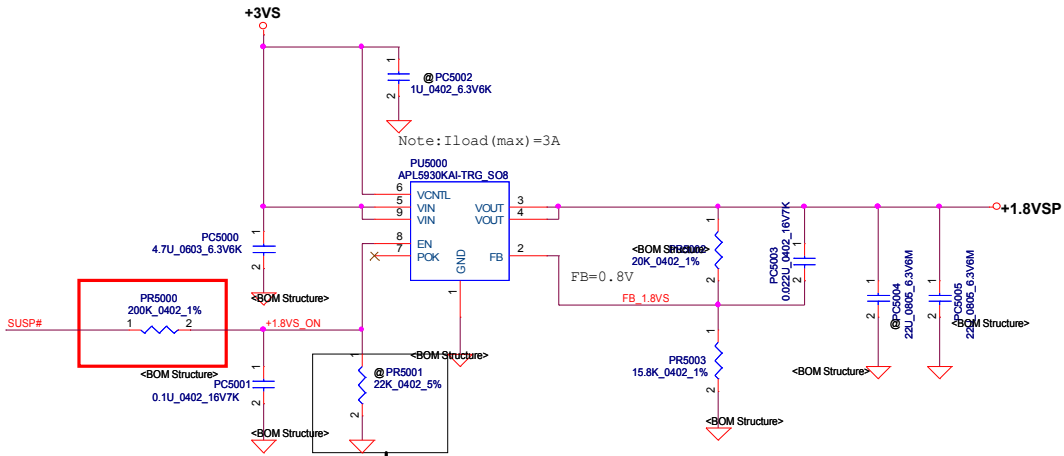
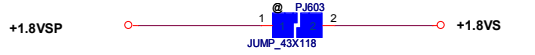
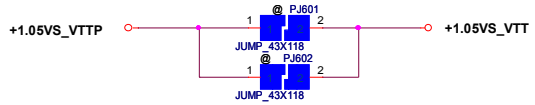
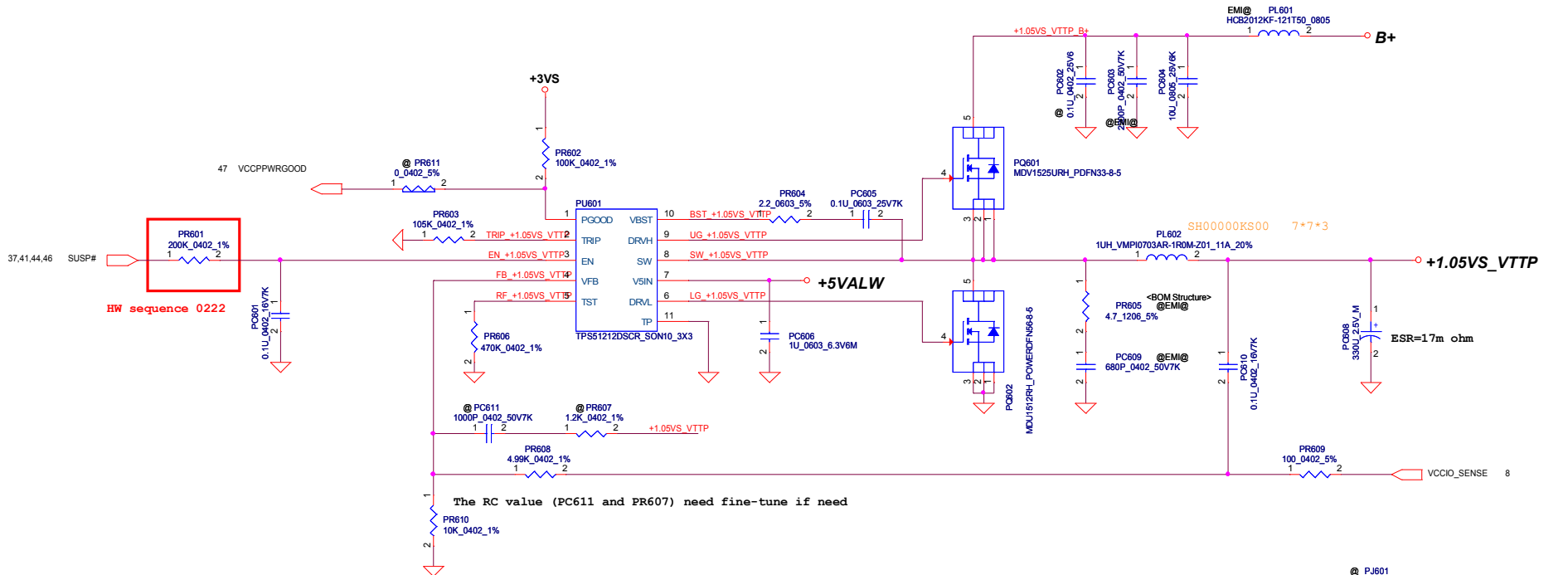
output voltage adjustable network



$I_{max} = 4.2A$ ,  $I_{peak} = 6A$   
 $F_{B} = 0.6V$

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+1.05VSP Ipeak=5.36A ; I<sub>max</sub>=3.752A ; 1.2I<sub>peak</sub>=6.432  
 Delta I=0.xxxxA=>1/2Delta I=0.xxxxA,F= 800K Hz(typ)

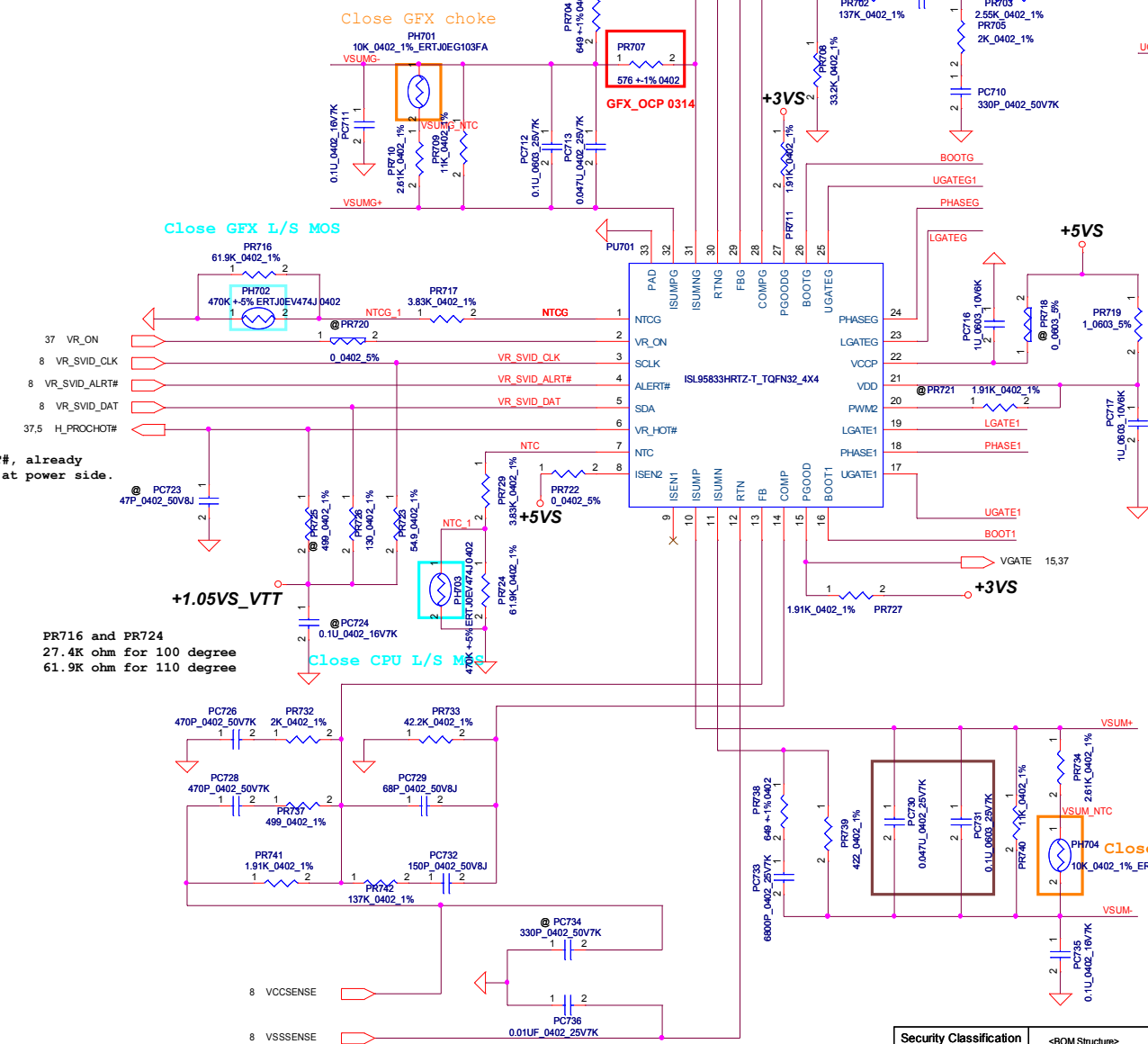


I<sub>en</sub>=10uA, V<sub>th</sub>=0.3V, notice the res. and pull high voltage from HW

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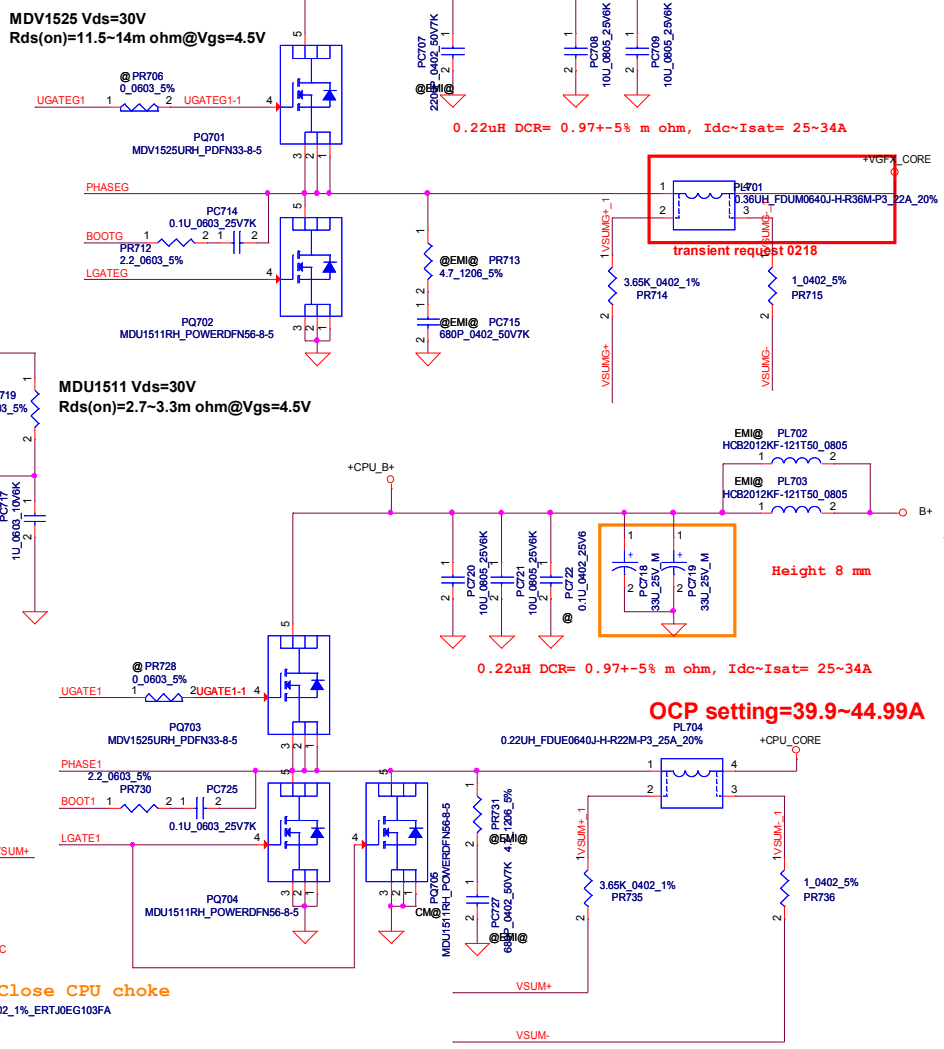
**Layout Note**  
 SVID routing  
 1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date  
 2. SVID spacing requirement is 18mils(0.475mm).  
 3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).  
 4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.  
 5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.  
 6. When SVID signal changes layer, GND return path may be changed also. We need add GND via for GND reference.



**Layout Note**  
 Reduce Acoustic Noise  
 1. The AL bulk capacitor of B+ should be very close to CPU\_CORE MOSFET.  
 2. Input ceramic caps must place on symmetry same location on top side and bottom side.

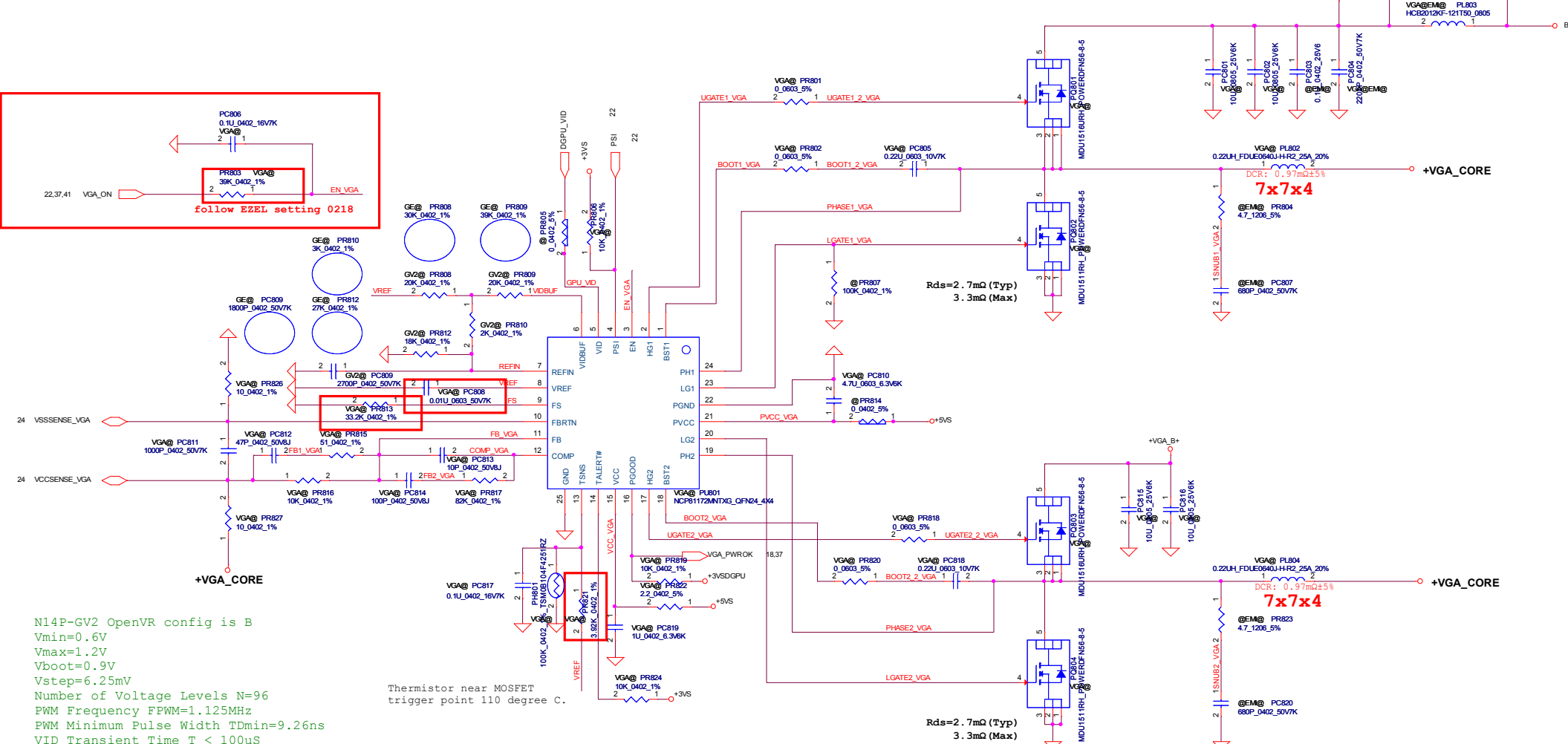
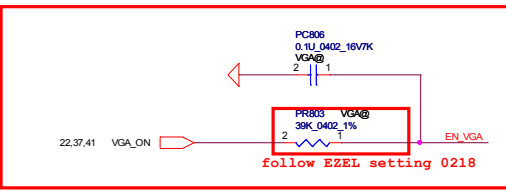
OCP setting=39.9-44.99A

VDD source use +5VS and PGOOD source use +3VS  
 Please confirm power on and down sequence, make sure VGATE after CPU\_CORE on.



PL701 PL702 Footprint用SH00000HQ00代替, 因為SH00000NM00\_R22為2PIN 2012/07/05

Security Classification	<BOM Structure> Compal Secret Data		EOP		Title		Compal Electronics, Inc.	
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N14P-GV2 OpenVR config is B  
 Vmin=0.6V  
 Vmax=1.2V  
 Vboot=0.9V  
 Vstep=6.25mV  
 Number of Voltage Levels N=96  
 PWM Frequency FPWM=1.125MHz  
 PWM Minimum Pulse Width Tdmin=9.26ns  
 VID Transient Time T < 100us

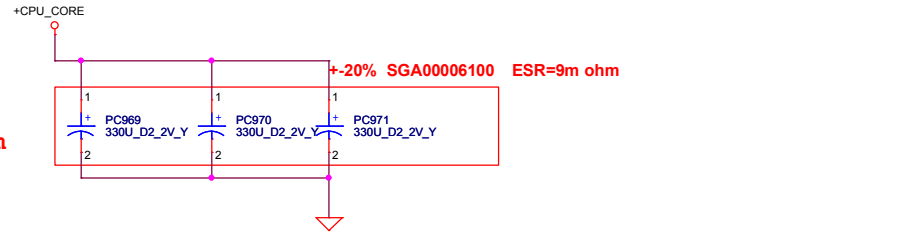
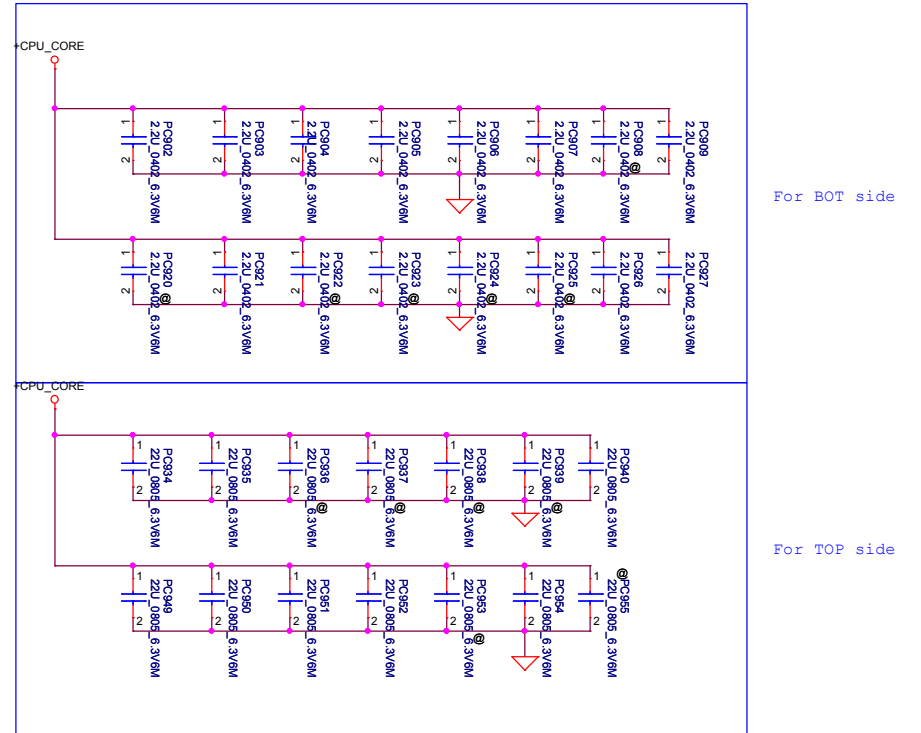
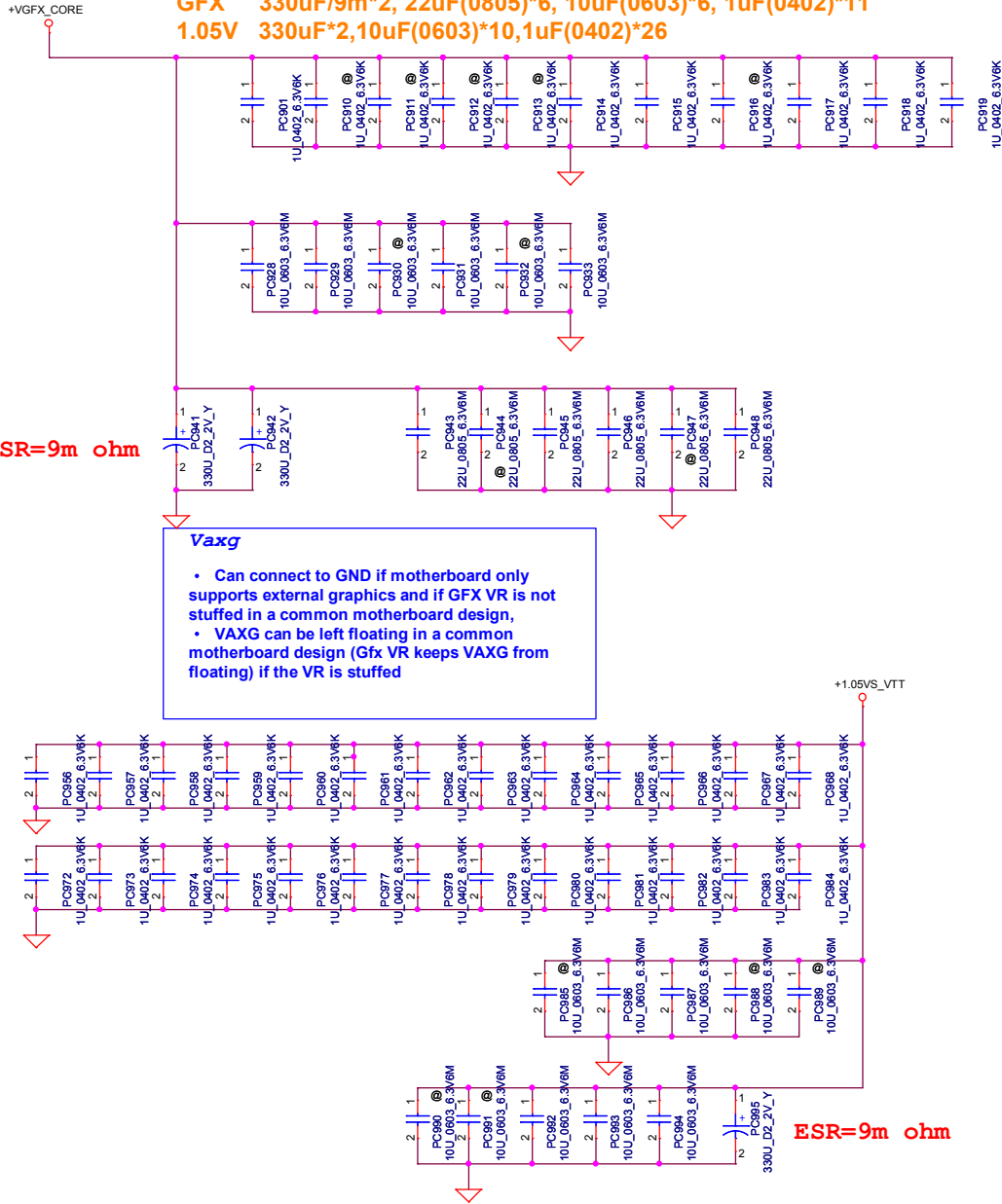
N14P-GE OpenVR config is C  
 Vmin=0.65V  
 Vmax=1.15V  
 Vboot=0.9V  
 Vstep=25mV  
 Number of Voltage Levels N=20  
 PWM Frequency FPWM=0.676MHz  
 PWM Minimum Pulse Width Tdmin=74ns  
 VID Transient Time T < 100us

N14P-GV2 TDP 25W  
 Ipeak=55A  
 Imax=25A  
 Iocp=72A  
 Fsw=450KHz  
 bulk cap 560uF\*2

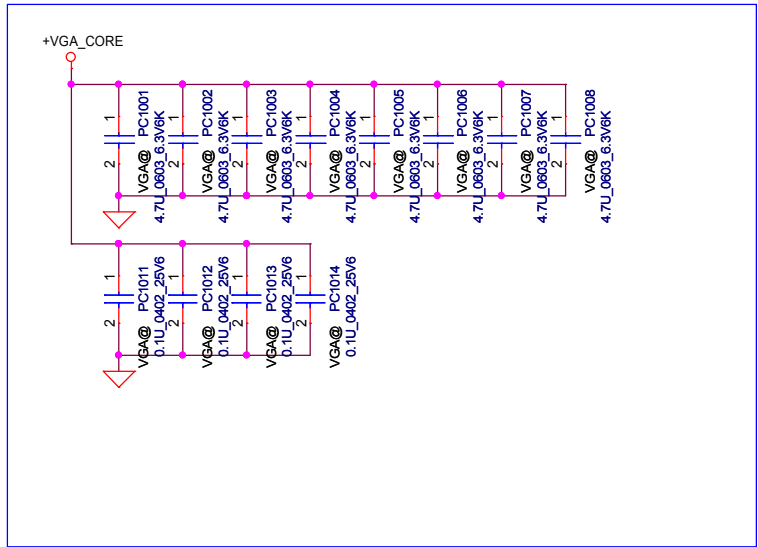
Thermistor near MOSFET trigger point 110 degree C.

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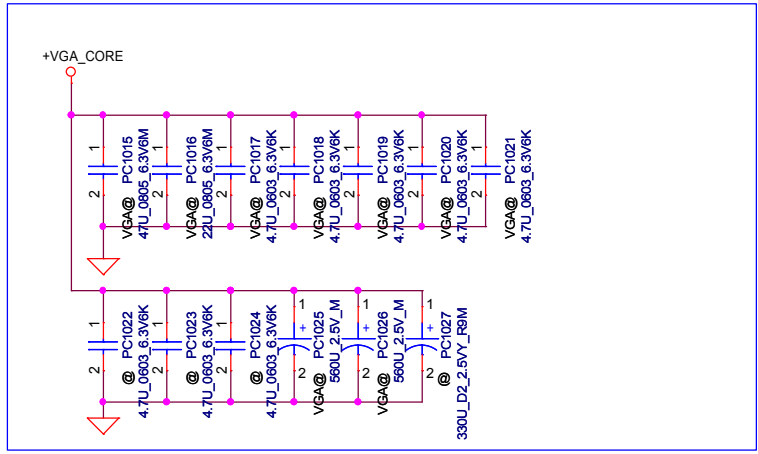
**PWR Rule 17W@ULV(CR BGA1023\_GT2) CPU2.9m GFx3.9m**  
**CPU 330uF/9m \*3, 22uF(0805) \*12, 2.2uF(0402)\*16**  
**GFX 330uF/9m\*2, 22uF(0805)\*6, 10uF(0603)\*6, 1uF(0402)\*11**  
**1.05V 330uF\*2, 10uF(0603)\*10, 1uF(0402)\*26**



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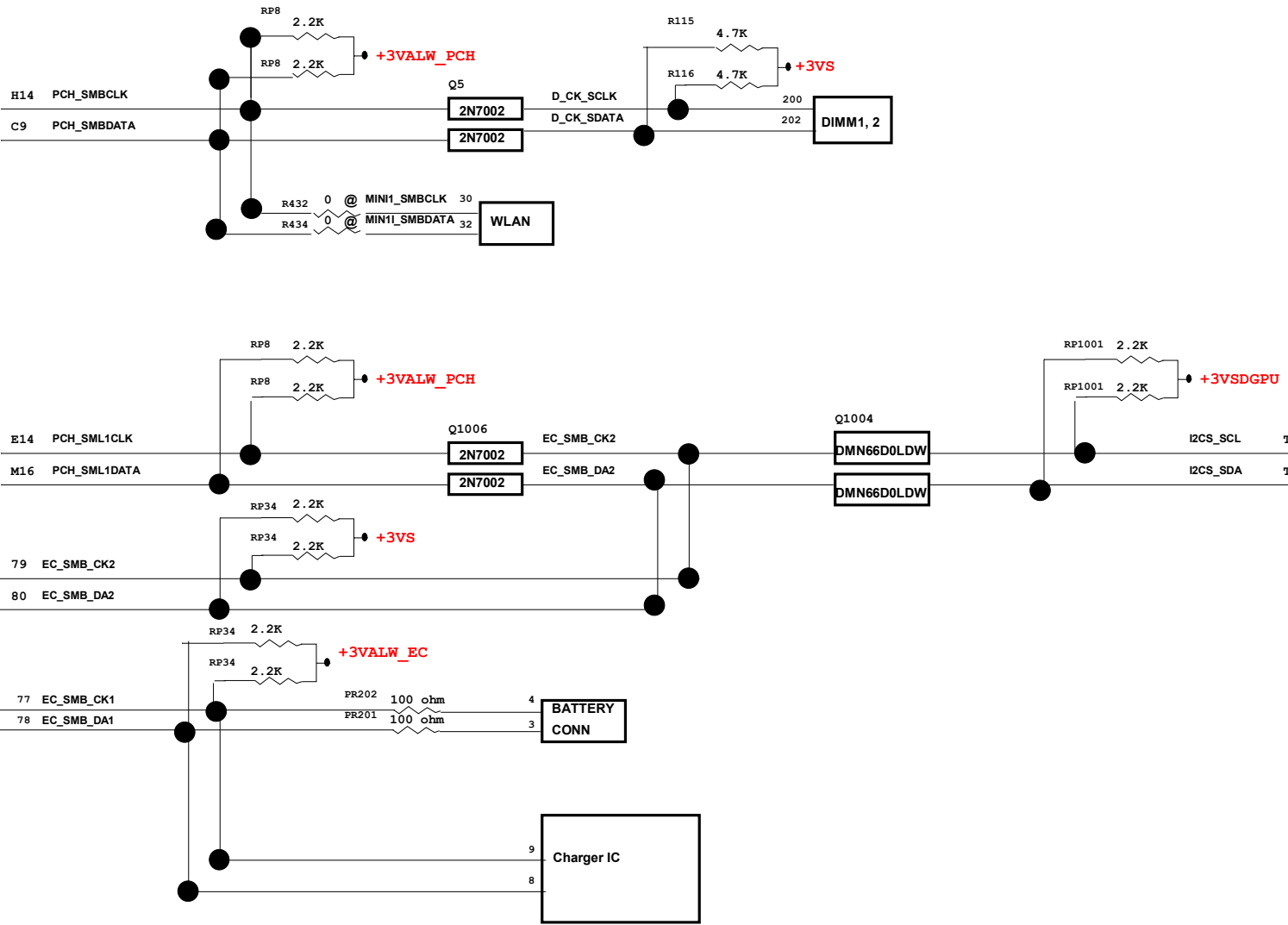
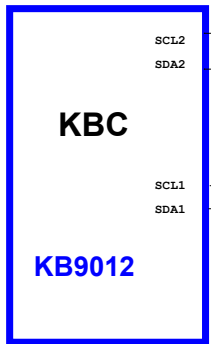
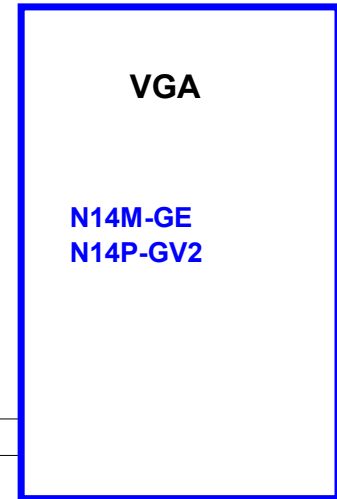
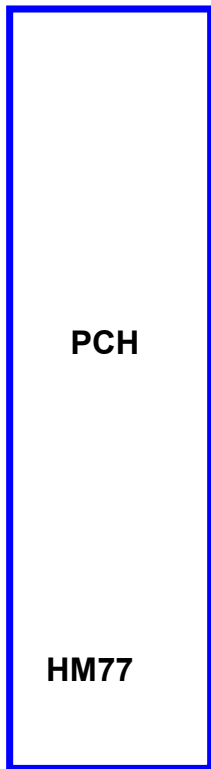


nVidia GB4-128 package  
Under GPU  
4.7uF 0603 \* 10  
0.1uF 0402 \* 4



nVidia GB4-128 package  
Near GPU  
47uF 0805 \* 1  
22uF 0805 \* 1  
4.7uF 0805 \* 5 (0603)  
330uF POS \* 1 <6mΩ

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Item	Reason for change	PG#	Modify List	Date	Phase
1	For 4S battery request	44	mount PR319,PR321,PR326,PQ307,PQ308	0310	C
2	change size to common part	45	PC419 change to 0603 common part	0310	C
3	HW sequence request	47	PR1003 to 30k	0311	C
4	EMI request	44	not mount PC307	0312	C
5	EMI request	44	add PC745 PC746 PC747	0313	C
6	EMI request	44	change PR311 PR310 to 2.2Ohm	0313	C
7	GFX_OCP	49	change PR707 to 576hm	0314	C
8					
9					
10					
11					
12					
13				3/5	EVT
14				3/5	EVT
15					
16					
17					
18					
19					
20					

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03/06  
 Change R1033 from 4.99K to 10K(ROM\_SO VGA\_DEVICE)  
 Change U51 N14P-GV2 from SA00006B500 to SA00006B510  
 Change Y6 P/N to SJ10000E800(合併用料)

03/11  
 Add net +XDPWR\_SDPWR\_MSPWR\_R  
 Add share rom feature  
 Add R112 R140 R141 R144  
 Add EC\_SPI\_MISO\_1 , PCH\_SPI\_MISO\_1  
 Add EC\_SPI\_CS0# , PCH\_SPI\_CS0#  
 Add EC\_SPI\_CLK\_1 , PCH\_SPI\_CLK\_1  
 Add EC\_SPI\_MOSI\_1 , PCH\_SPI\_MOSI\_1  
 R541 pop 1K VGA@  
 R1101 470-->47 SD013470A80  
 D1000.3 VGA\_PWROK changes into VGA\_ON

SW3 @ 拿掉不上  
 Removed U15,R107,R108  
 Removed R151,R159,R160,R184,R97  
 Removed R524,R525,R526 換 RP13 5%-->1%

03/12  
 Add C441 470pF(SE074471K80),EMC@, EMI solution  
 Change U51 N14P-GV2 SA00006B510-->SA00006B530 R3 P/N  
 Change U51 N14M-GE SA000068A00-->SA000068A10 R3 P/N

0313a  
 Combine with PWR\_Z5WE1\_LA9535PR02\_PWR\_0313.DSN

0313b  
 Remove RP14,  
 PCH\_GPIO2 不接  
 PCH\_GPIO3 不接  
 PCH\_GPIO53 不接

RP13 5%-->1%(SD300002Y00)

0313C  
 2nd rom 加回去  
 Add U15,R107,R108  
 Add R97 R151 R159 R160 R184  
 Del R112 R140 R141 R144

0314  
 R285 XEMC@-->EMC@  
 C329 22P-->10P, XEMC@-->EMC@

Add C230 0.1U for card reader enable

Board ID  
 R316 0ohm 改 8.2K 上件  
 R314 @-->改上件  
 C346 @-->改上件

0314C  
 R774 change from 10 to 56ohm  
 R1027,R1028,R1029,R1030,R1035,R1036,R1039,R1033,R1042  
 at N14M-GE SKU 10K\_0402\_5% change to 10K\_0402\_1%

0314d  
 L33 changes into SM010014520

0315a  
 Add net CRT\_4, CRT\_11 for 測點  
 R541 bom structure-->VGA@  
 C346 board ID cap改@ 不上

0318  
 L24,L25 change from SM070001600 (12ohm USB3.0 common mode choke)  
 to SM070001R00 (Murata 67ohm )

0419  
 Add Touch screen feature and JTS1

0422  
 Remove PEG 16X

0425  
 Add HM70 NM70 文字敘述  
 Add FFR VRAM strap for N14M-GE N14P-GV2

0502  
 Update CPU,PCH,VRAM P/N

0505  
 Pop RP16 for LAN loopback

0528  
 N14M-GE ROM\_SO keep 10K pull low.  
 N14P-GV2 need change be to EVT R1033 as 4.99K\_0402\_1%

C142-->15pF(SE071150J80) to meet off mode timing

0604  
 Correct page1 date code  
 Update page24 3D device/vga device notice

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