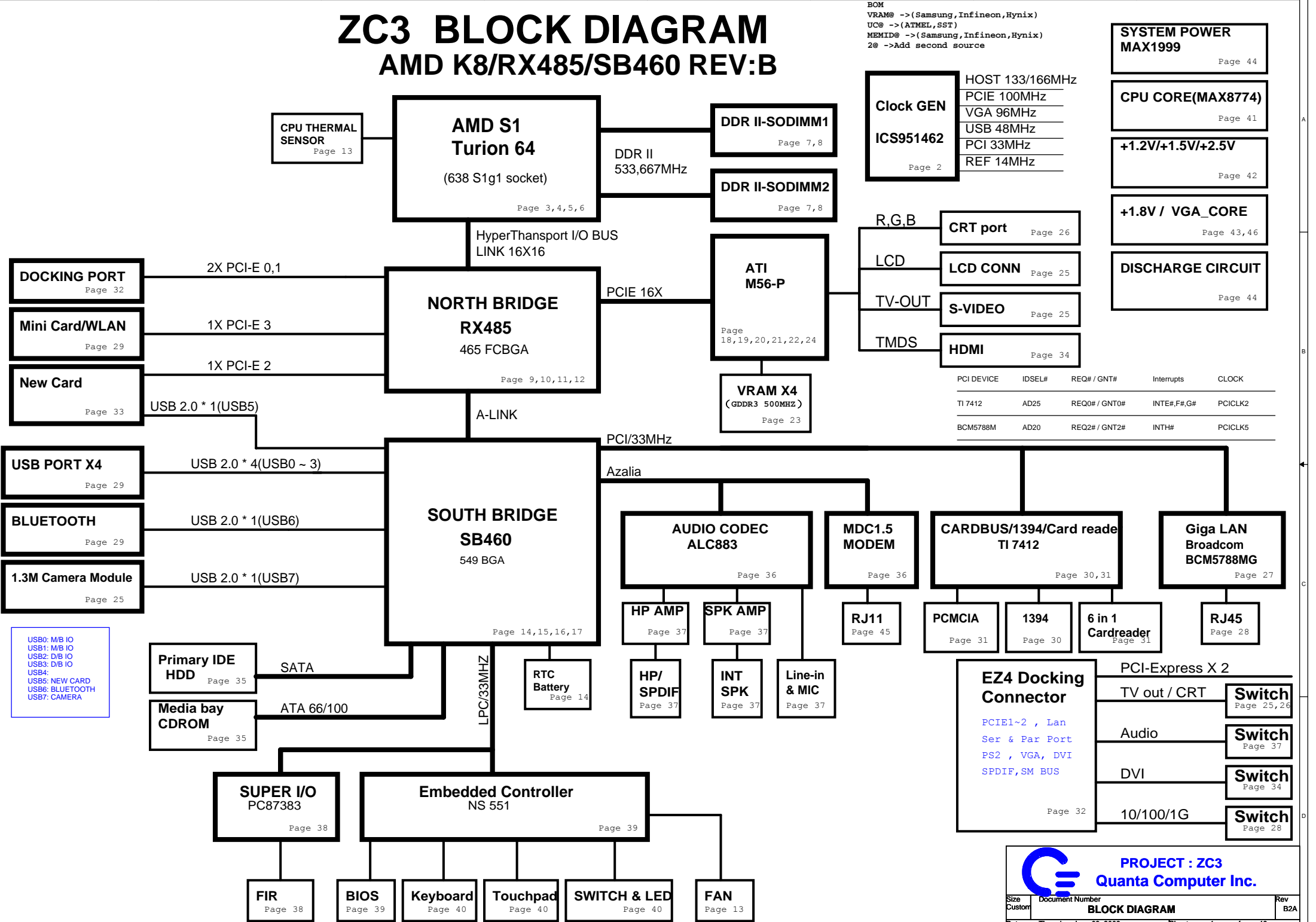


# ZC3 BLOCK DIAGRAM

## AMD K8/RX485/SB460 REV:B

BOM  
 VRAM@ ->(Samsung,Infineon,Hynix)  
 UC@ ->(ATMEL,SST)  
 MEMID@ ->(Samsung,Infineon,Hynix)  
 2@ ->Add second source



**SYSTEM POWER**  
 MAX1999  
 Page 44

**CPU CORE(MAX8774)**  
 Page 41

**+1.2V/+1.5V/+2.5V**  
 Page 42

**+1.8V / VGA\_CORE**  
 Page 43,46

**DISCHARGE CIRCUIT**  
 Page 44

**Clock GEN**  
 ICS951462  
 Page 2

HOST	133/166MHz
PCI-E	100MHz
VGA	96MHz
USB	48MHz
PCI	33MHz
REF	14MHz

R,G,B  
 LCD  
 TV-OUT  
 TMD5

**CRT port** Page 26  
**LCD CONN** Page 25  
**S-VIDEO** Page 25  
**HDMI** Page 34

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
TI 7412	AD25	REQ0# / GNT0#	INTE#,F#,G#	PCICLK2
BCM5788M	AD20	REQ2# / GNT2#	INTH#	PCICLK5

**DOCKING PORT**  
 Page 32

**Mini Card/WLAN**  
 Page 29

**New Card**  
 Page 33

**USB PORT X4**  
 Page 29

**BLUETOOTH**  
 Page 29

**1.3M Camera Module**  
 Page 25

USB0: M/B IO  
 USB1: M/B IO  
 USB2: D/B IO  
 USB3: D/B IO  
 USB4:  
 USB5: NEW CARD  
 USB6: BLUETOOTH  
 USB7: CAMERA

**Primary IDE HDD**  
 Page 35

**Media bay CDROM**  
 Page 35

**SUPER I/O**  
 PC87383  
 Page 38

**Embedded Controller**  
 NS 551  
 Page 39

**FIR**  
 Page 38

**BIOS**  
 Page 39

**Keyboard**  
 Page 40

**Touchpad**  
 Page 40

**SWITCH & LED**  
 Page 40

**FAN**  
 Page 13

**AUDIO CODEC**  
 ALC883  
 Page 36

**HP AMP**  
 Page 37

**SPK AMP**  
 Page 37

**HP/SPDIF**  
 Page 37

**INT SPK**  
 Page 37

**Line-in & MIC**  
 Page 37

**MDC1.5 MODEM**  
 Page 36

**RJ11**  
 Page 45

**CARDBUS/1394/Card reader**  
 TI 7412  
 Page 30,31

**PCMCIA**  
 Page 31

**1394**  
 Page 30

**6 in 1 Cardreader**  
 Page 31

**Giga LAN**  
 Broadcom  
 BCM5788MG  
 Page 27

**RJ45**  
 Page 28

**EZ4 Docking Connector**  
 Page 32

PCI-E1-2 , Lan  
 Ser & Par Port  
 PS2 , VGA, DVI  
 SPDIF, SM BUS

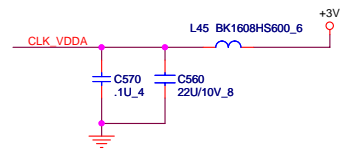
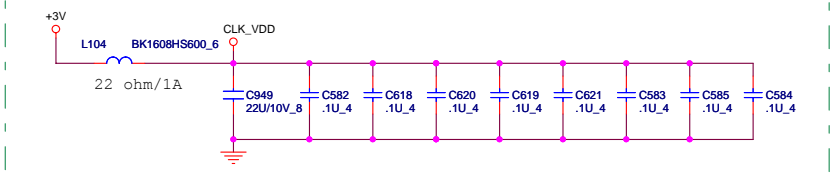
PCI-Express X 2

TV out / CRT **Switch** Page 25,26

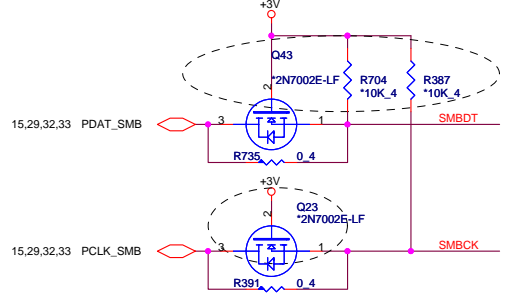
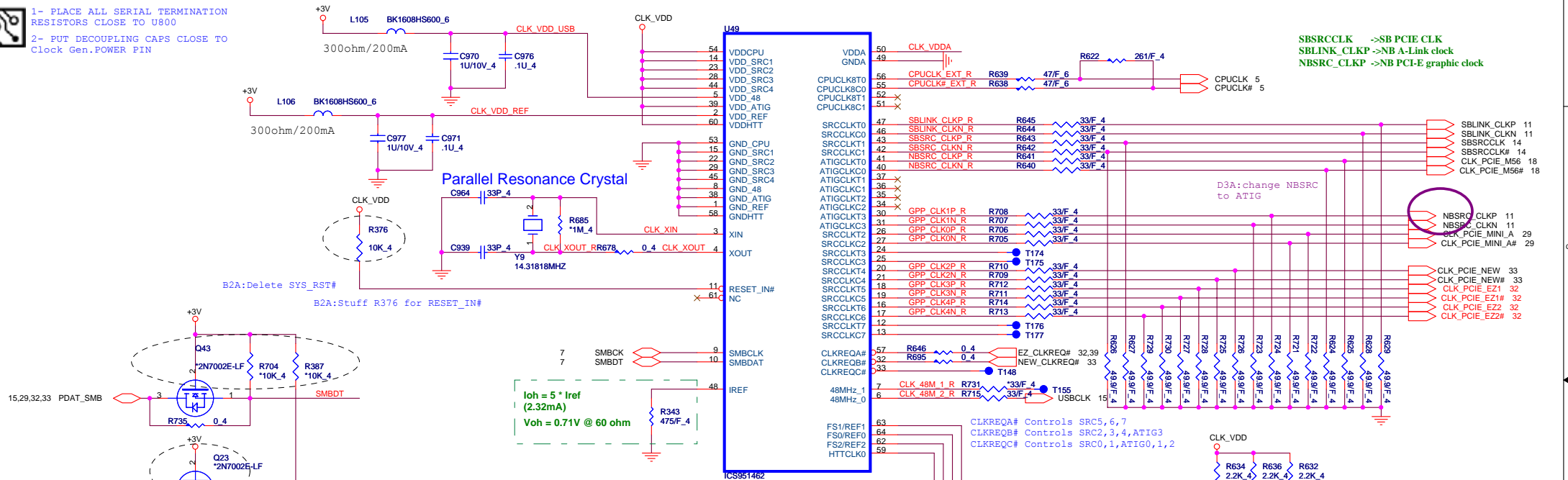
Audio **Switch** Page 37

DVI **Switch** Page 34

10/100/1G **Switch** Page 28



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO Clock Gen.POWER PIN



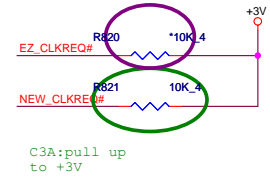
$I_{oh} = 5 \cdot I_{ref}$   
 $(2.32mA)$   
 $V_{oh} = 0.71V @ 60\ ohm$

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

D3A:remove R820 , docking side already pull low 10K



C3A:pull up to +3V

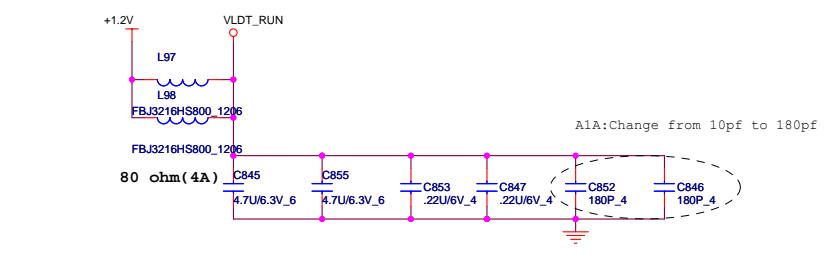
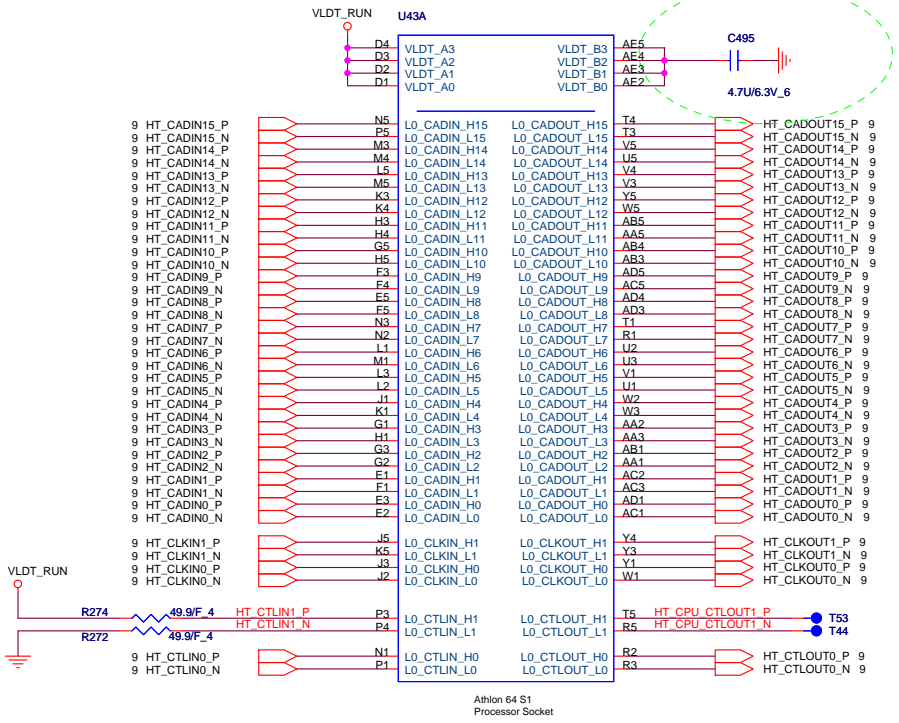
**PROJECT : ZC3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>EXTERNAL CLOCK GENERATOR</b>	1A
Date:	Thursday, June 08, 2006	Sheet 2 of 46



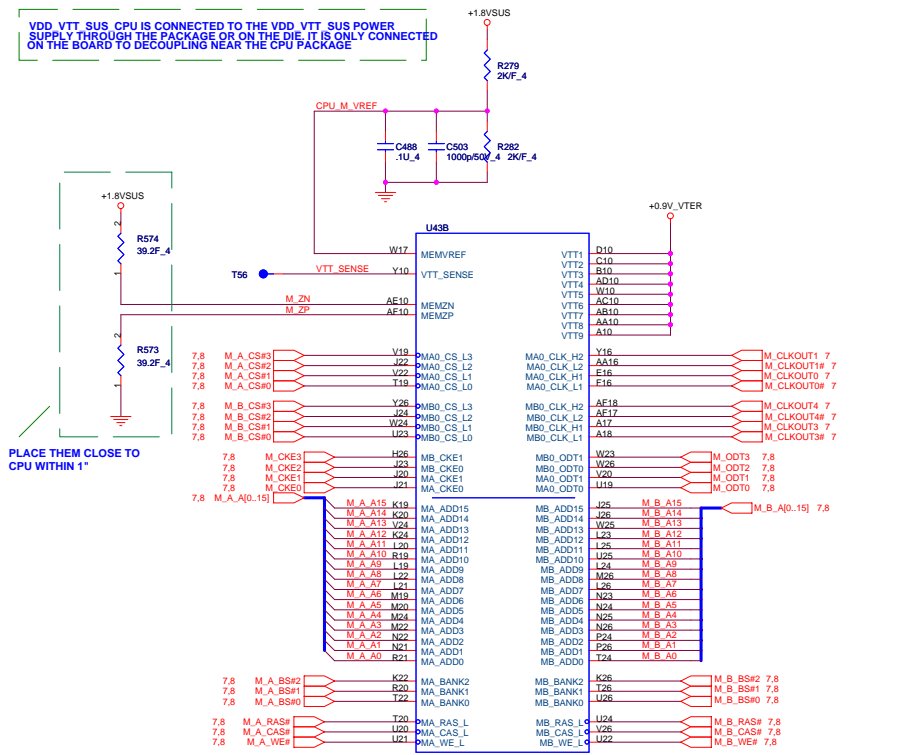
# PROCESSOR HYPERTRANSPORT INTERFACE

VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

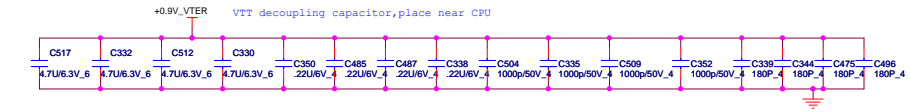


**LAYOUT: Place bypass cap on topside of board**  
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
 PLACE CLOSE TO VLDT0 POWER PINS

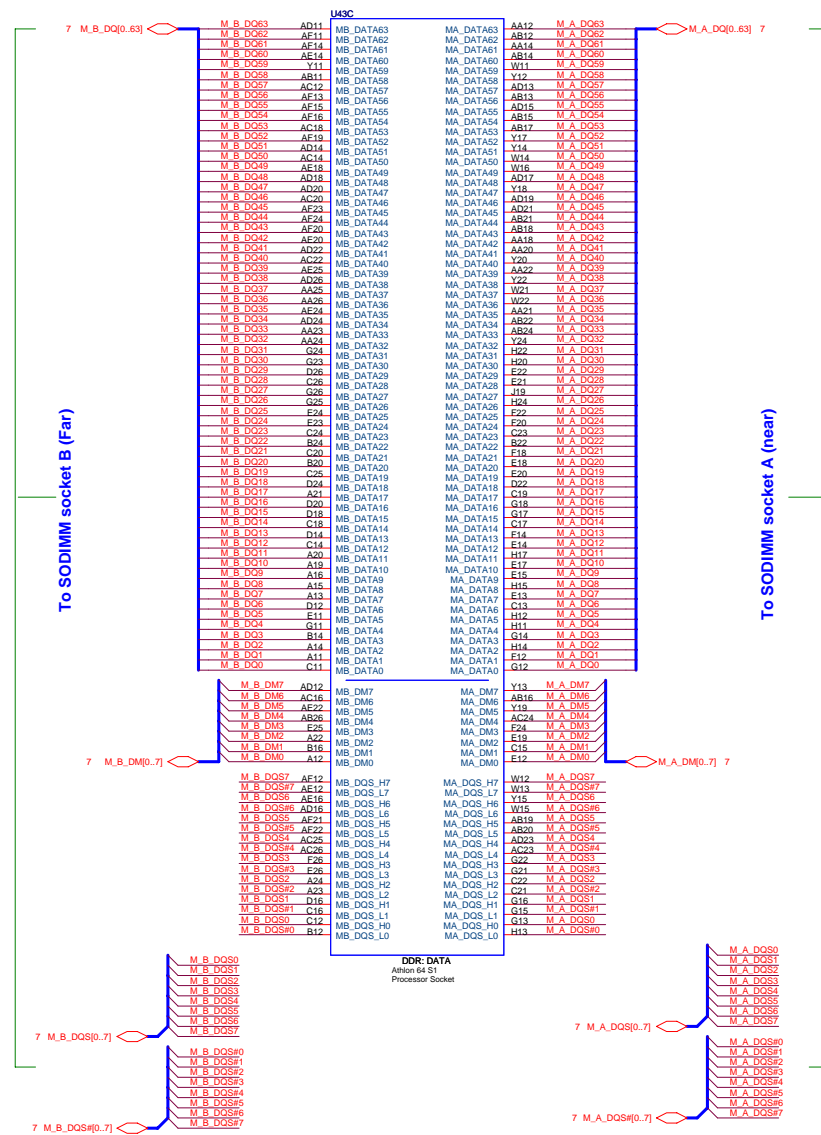
VDD VTT SUS CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



PLACE THEM CLOSE TO CPU WITHIN 1"



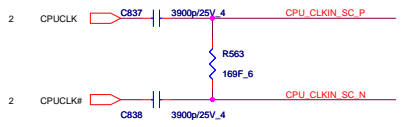
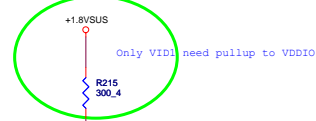
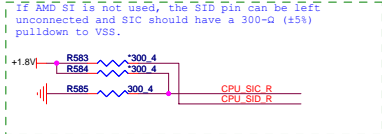
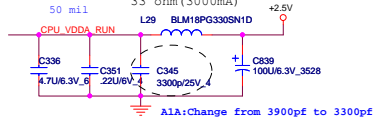
## Processor DDR2 Memory Interface



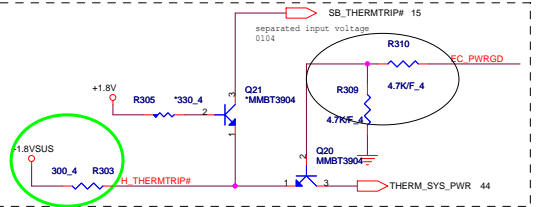
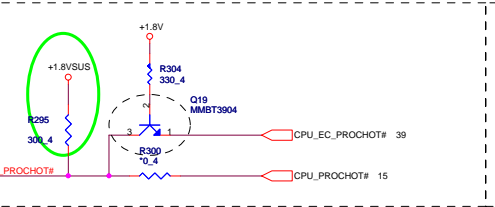
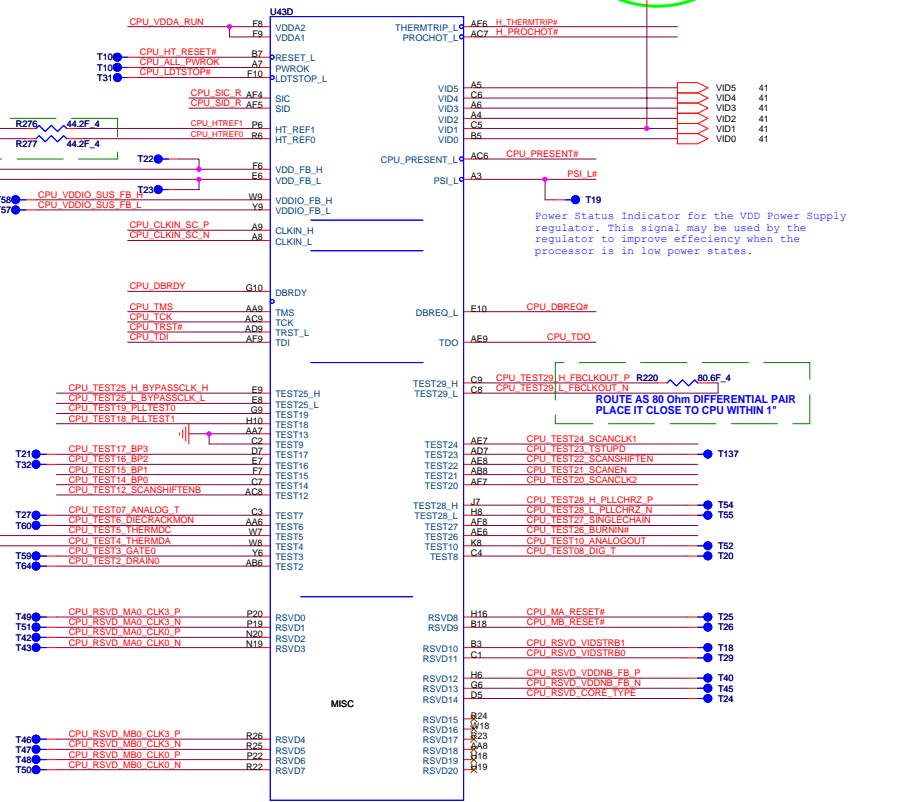
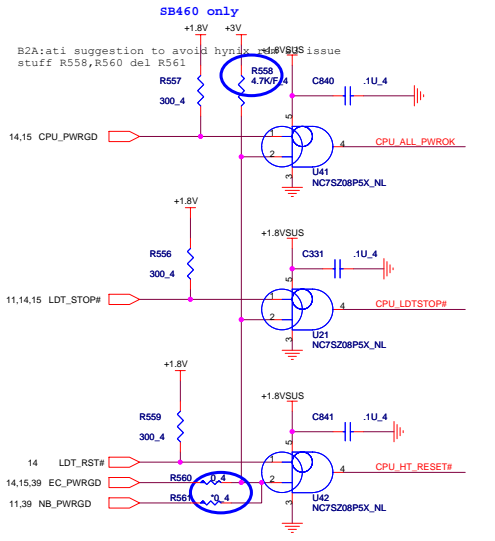
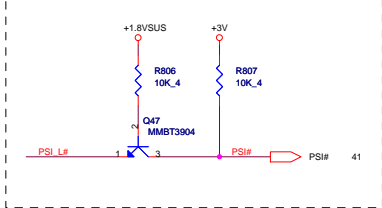
# ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

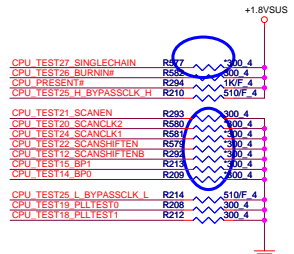
## CPU\_VDDA\_RUN



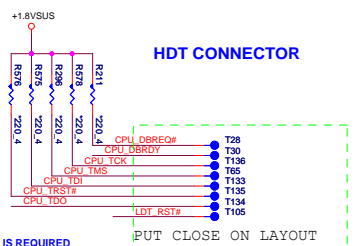
B2A: Add LEVEL-SHIFT circuit (R806, R807, Q47) on PS1# that between CPU and POWER.



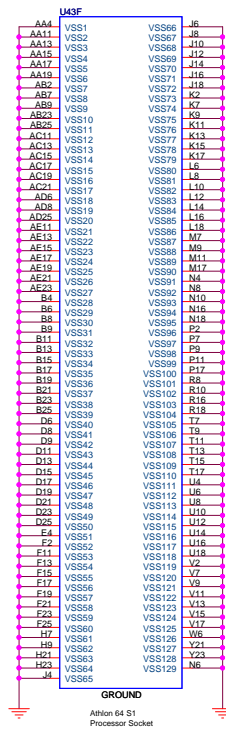
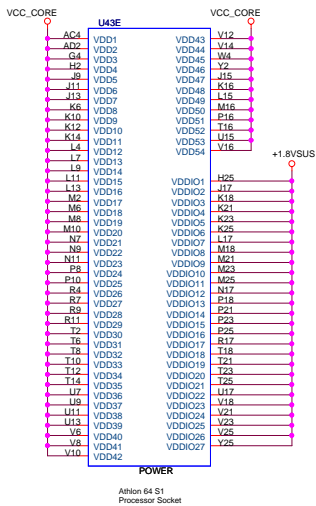
B2A: AMD suggestion not stuff  
 R577, R580, R581, R579, R292, R213, R209



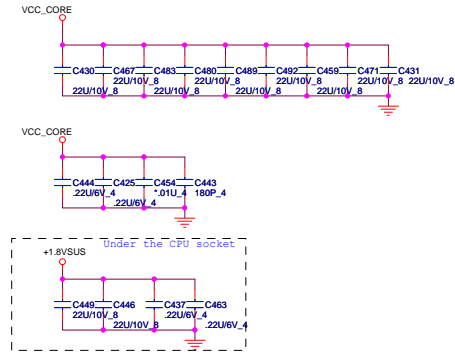
If no use which Net need pull-up or down



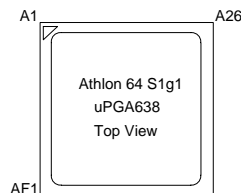
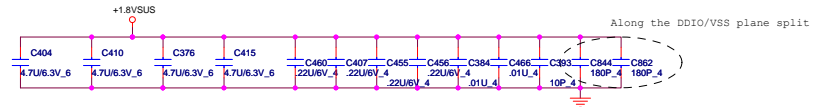
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.



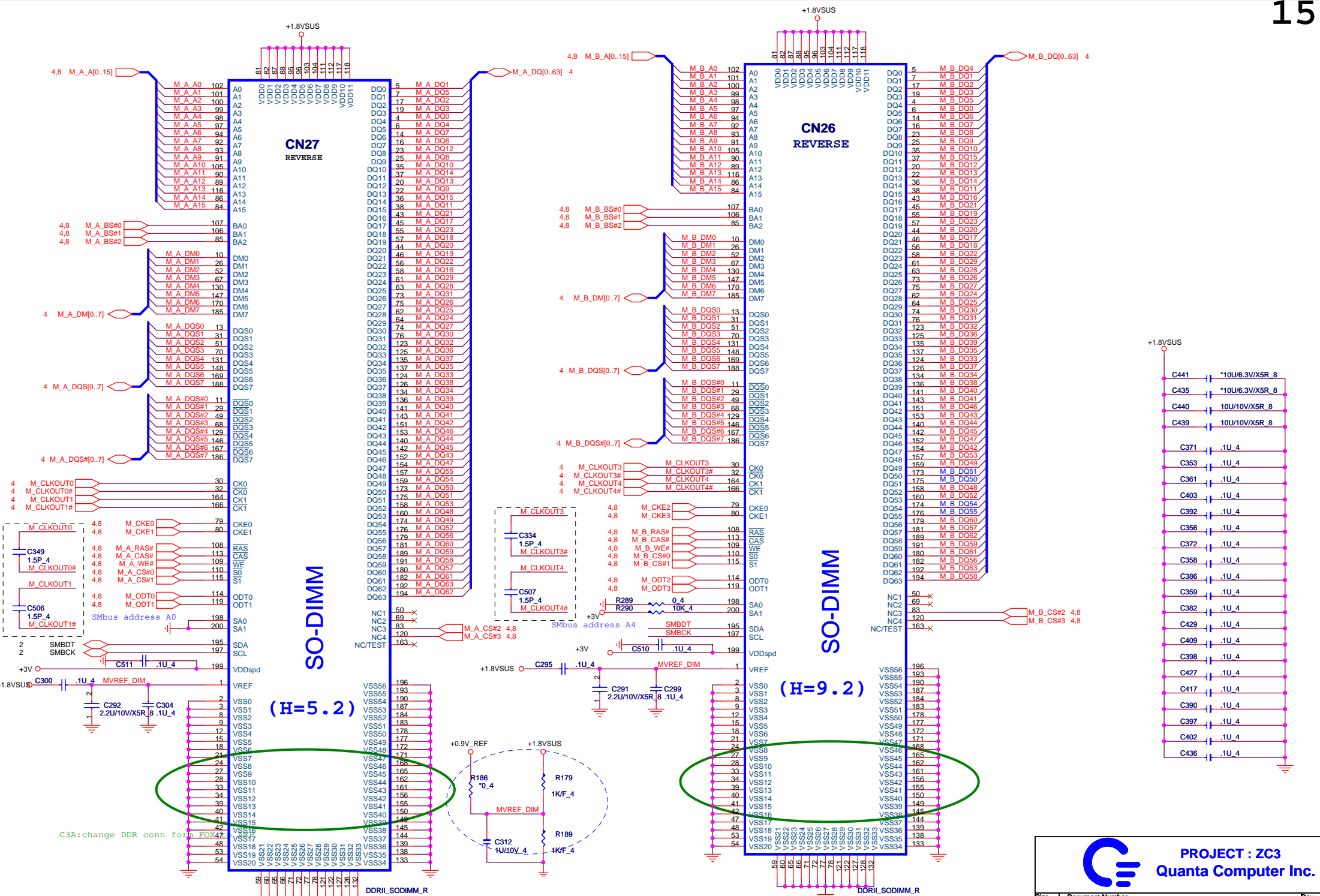
### BOTTOMSIDE DECOUPLING



### DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



## PROCESSOR POWER AND GROUND

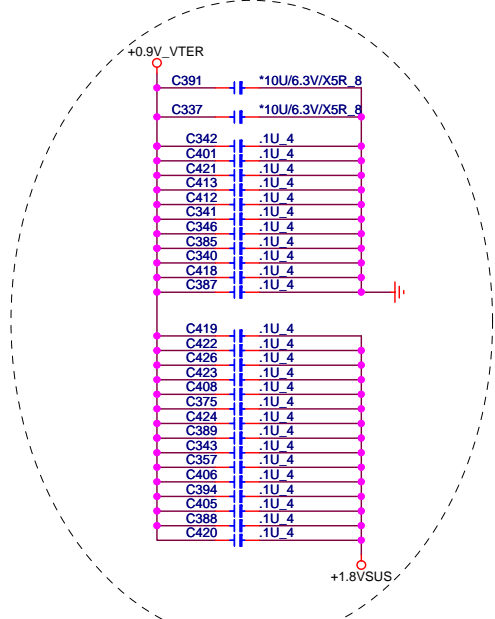


**PROJECT : ZC3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR-II SODIMM*2</b>	1A

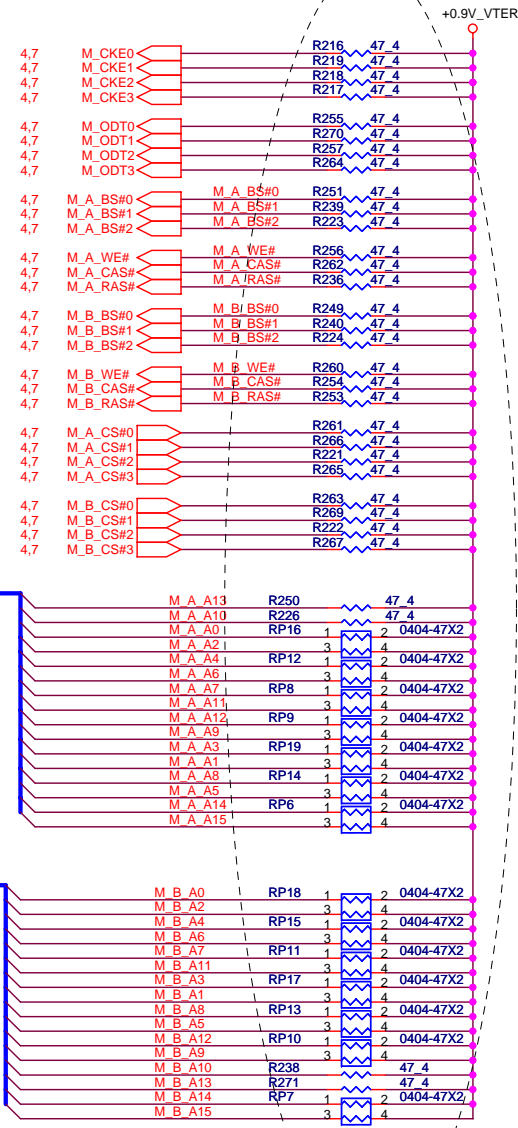


VTT is decoupled to VDDIO, VTT is decoupled to VSS



decoupling capacitors from VTT (+0.9V\_VTER) to VDDIO (+1.8V\_VSUS). Which is (1) decoupling capacitor for every (4) signals terminated to VTT

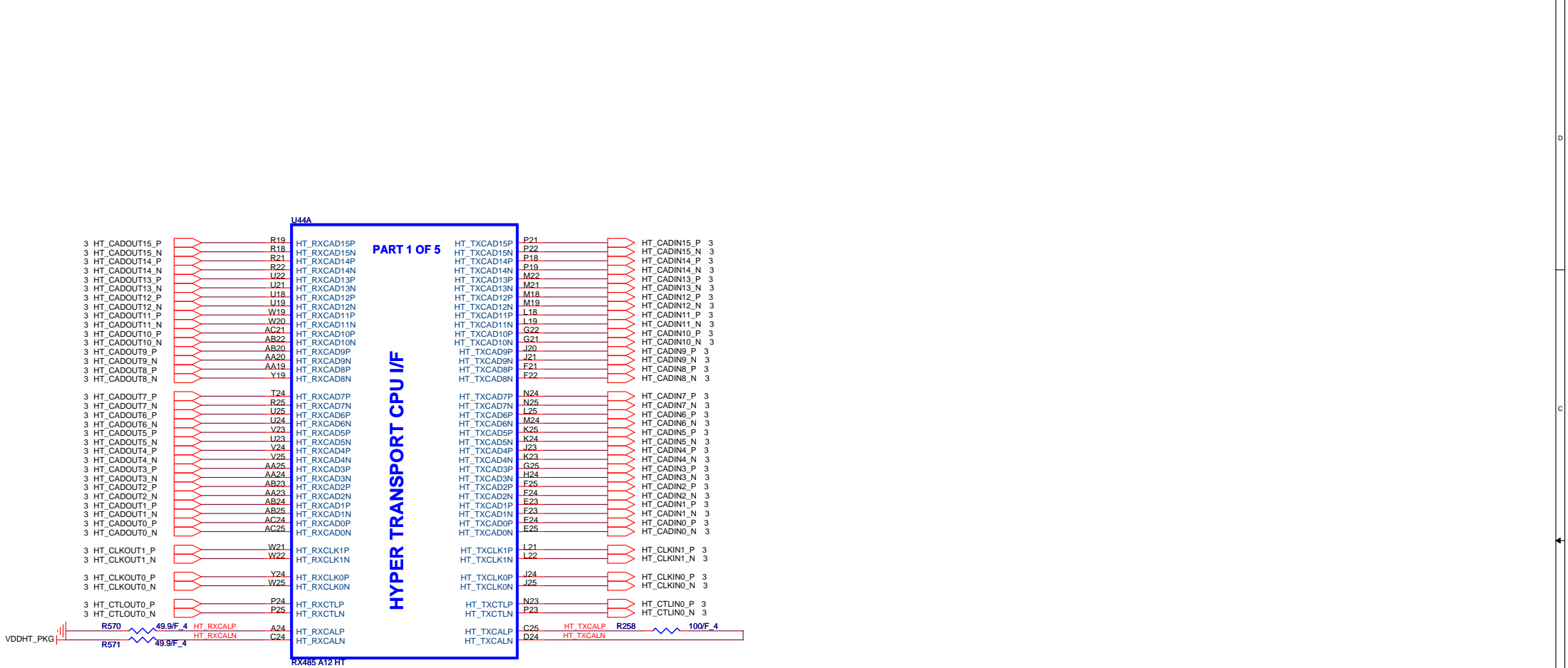
A1A: Change RTT termination from 56 to 47 ohm

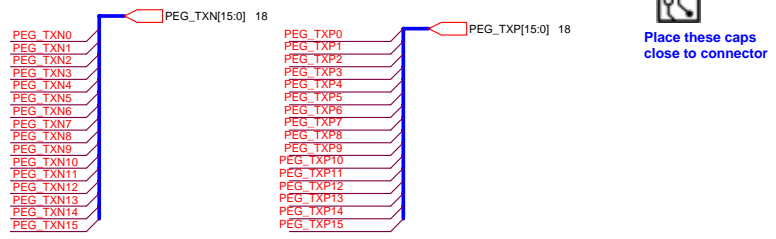
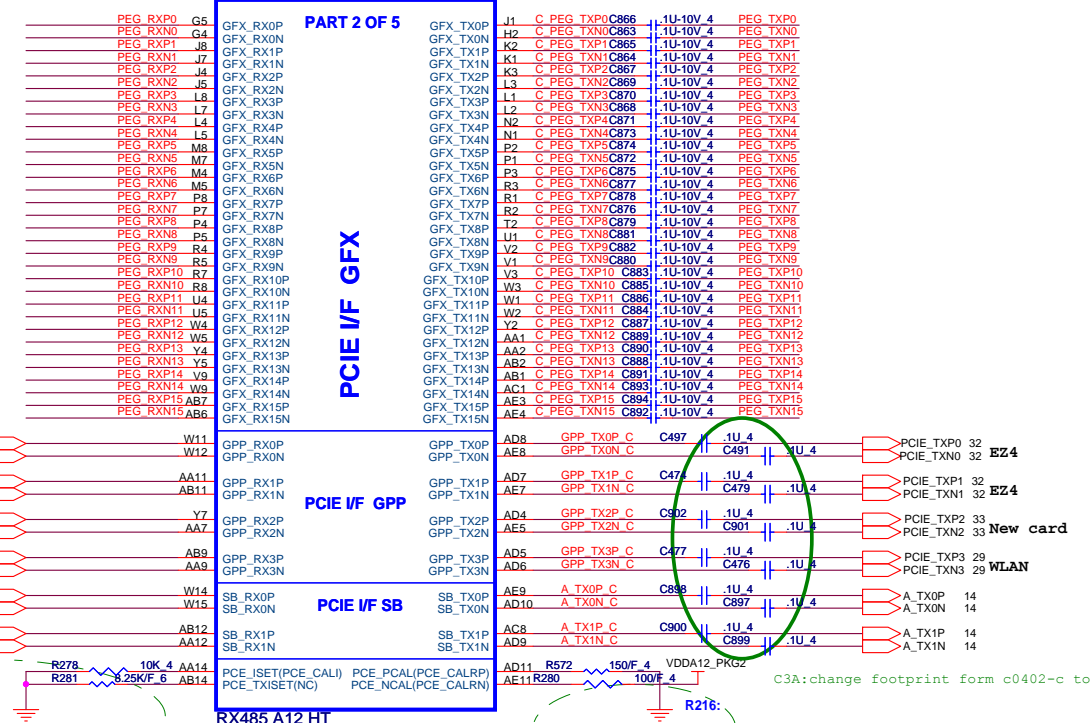
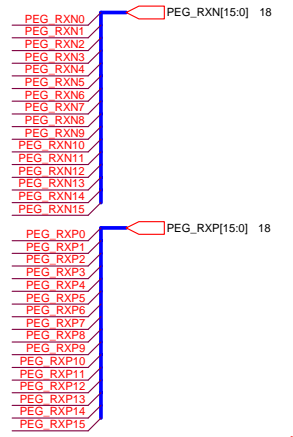
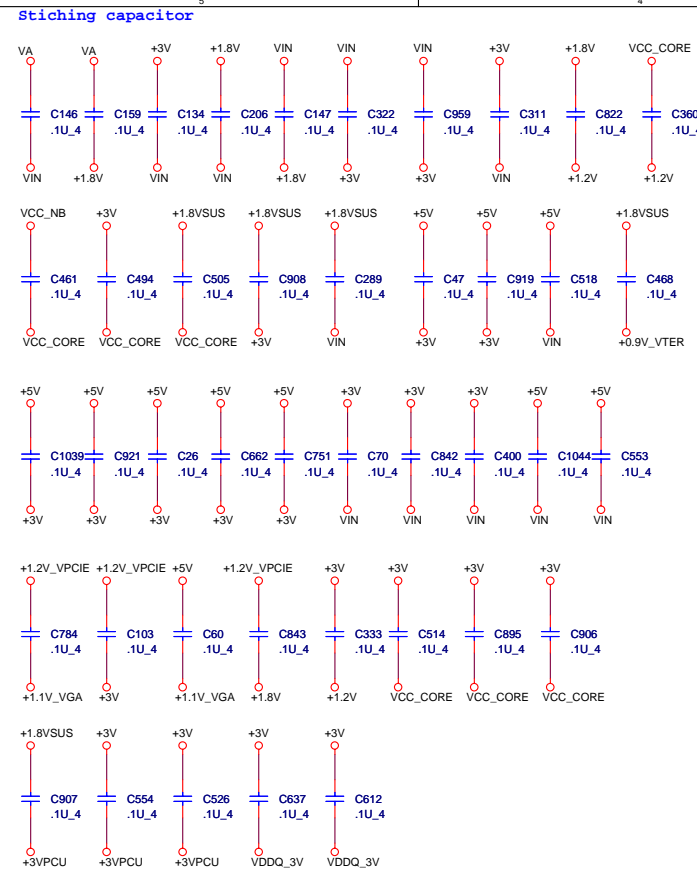


**PROJECT : ZC3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR-II TERMINATION</b>	1A
Date:	Thursday, June 08, 2006	Sheet 8 of 46

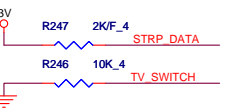
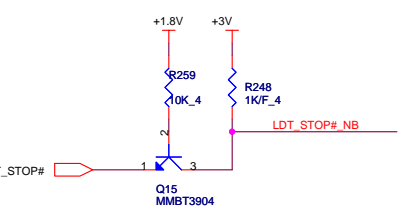
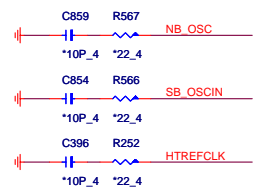
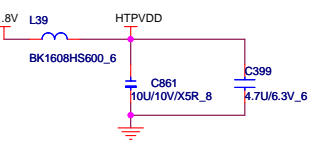
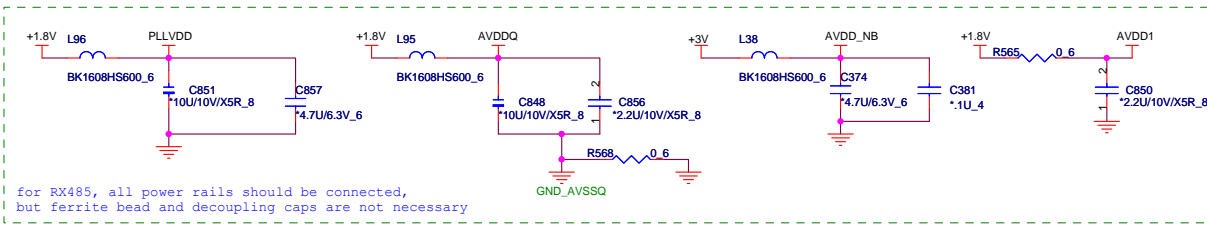




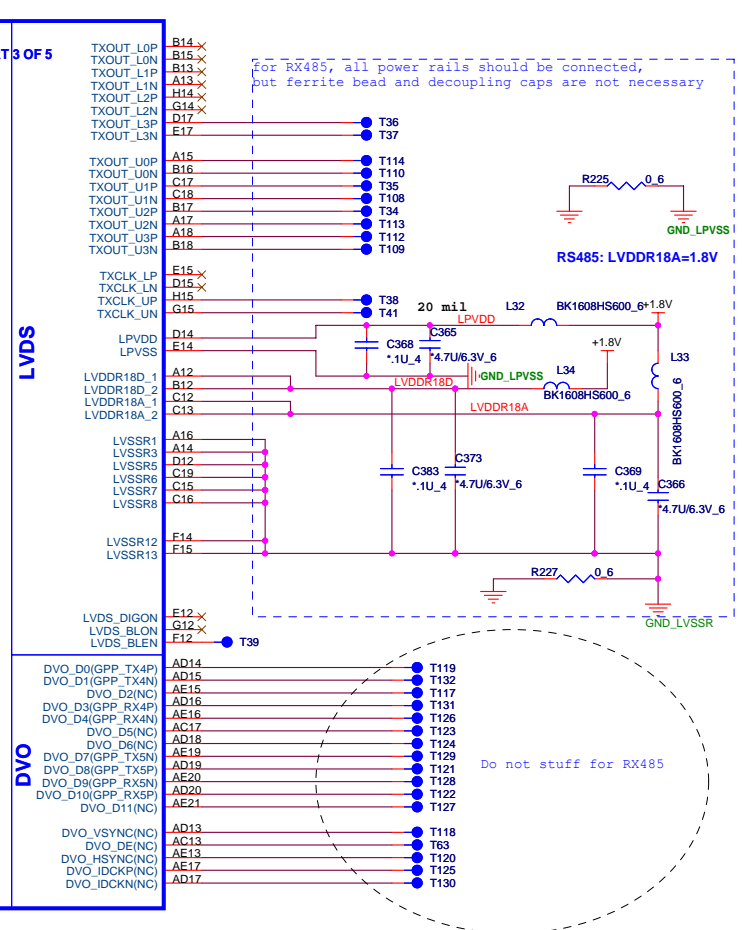
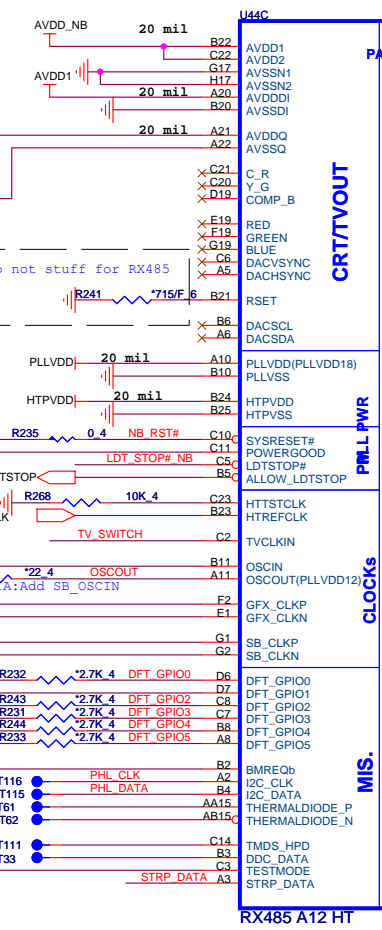
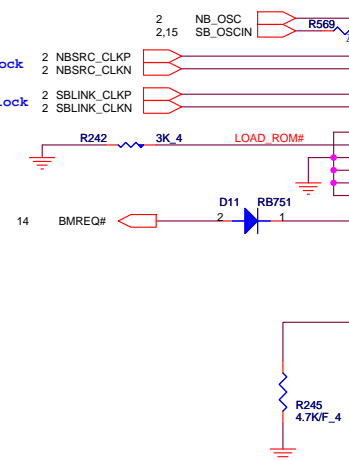


**PROJECT : ZC3**  
**Quanta Computer Inc.**

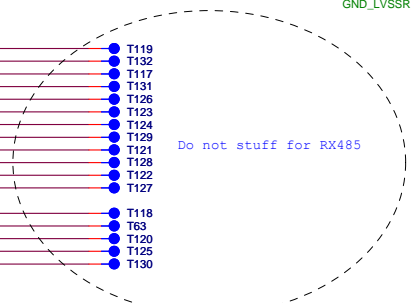
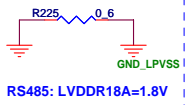
Size	Document Number	Rev
	<b>RS485-PCIE LINK I/F</b>	1A
Date:	Thursday, June 08, 2006	Sheet 10 of 46



**LOAD\_ROM#: LOAD ROM STRAP ENABLE**  
 High, LOAD ROM STRAP DISABLE  
 Low, LOAD ROM STRAP ENABLE

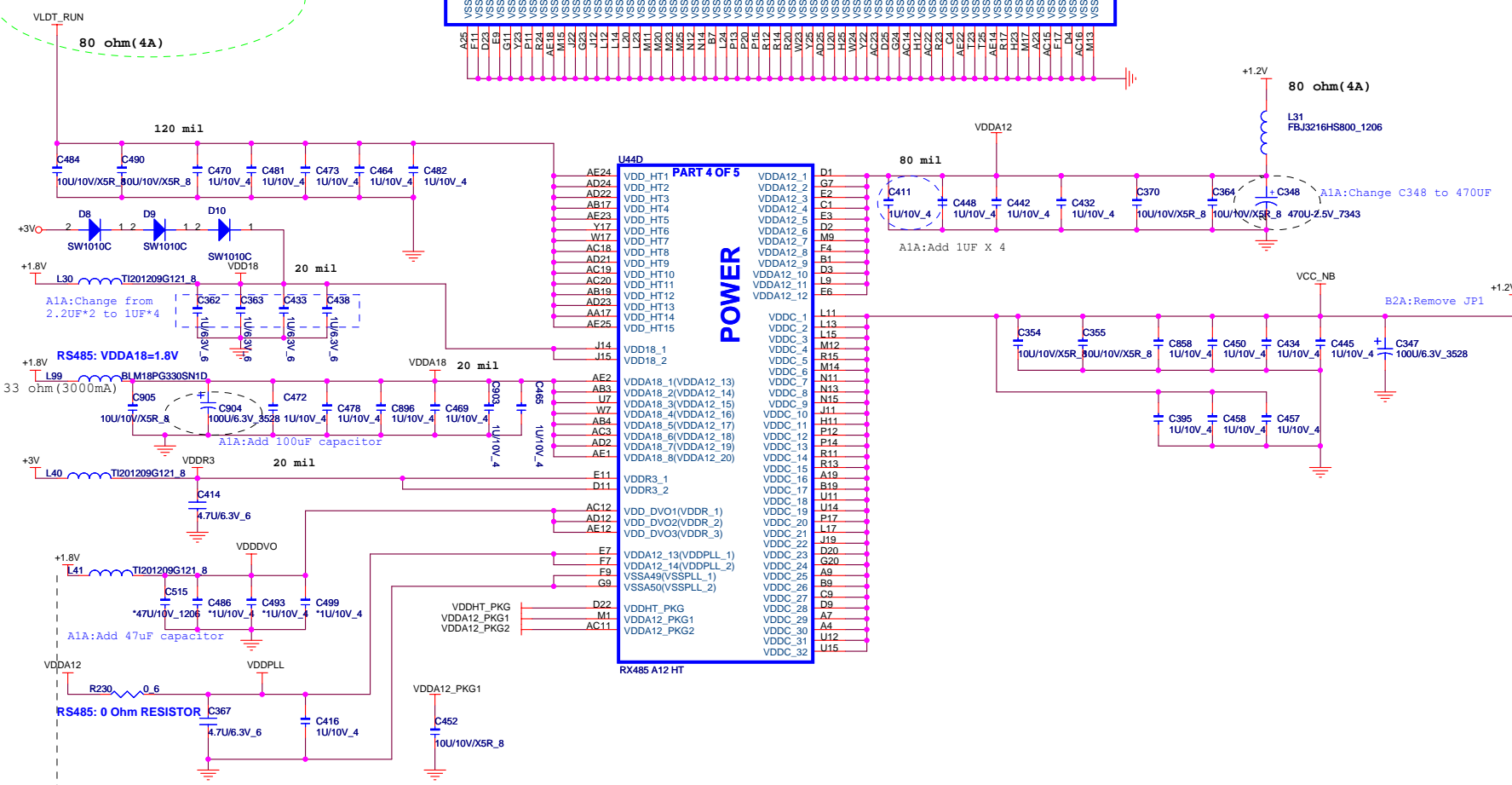
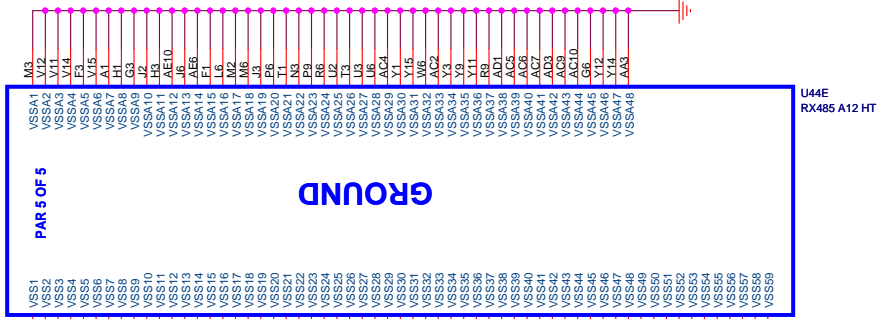


for RX485, all power rails should be connected, but ferrite bead and decoupling caps are not necessary



	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_RX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4N
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

SUGGEST REMOVE L11 BEAD SAME AS CPU  
1.2 PLAN FSB UNDER THIS PLAN



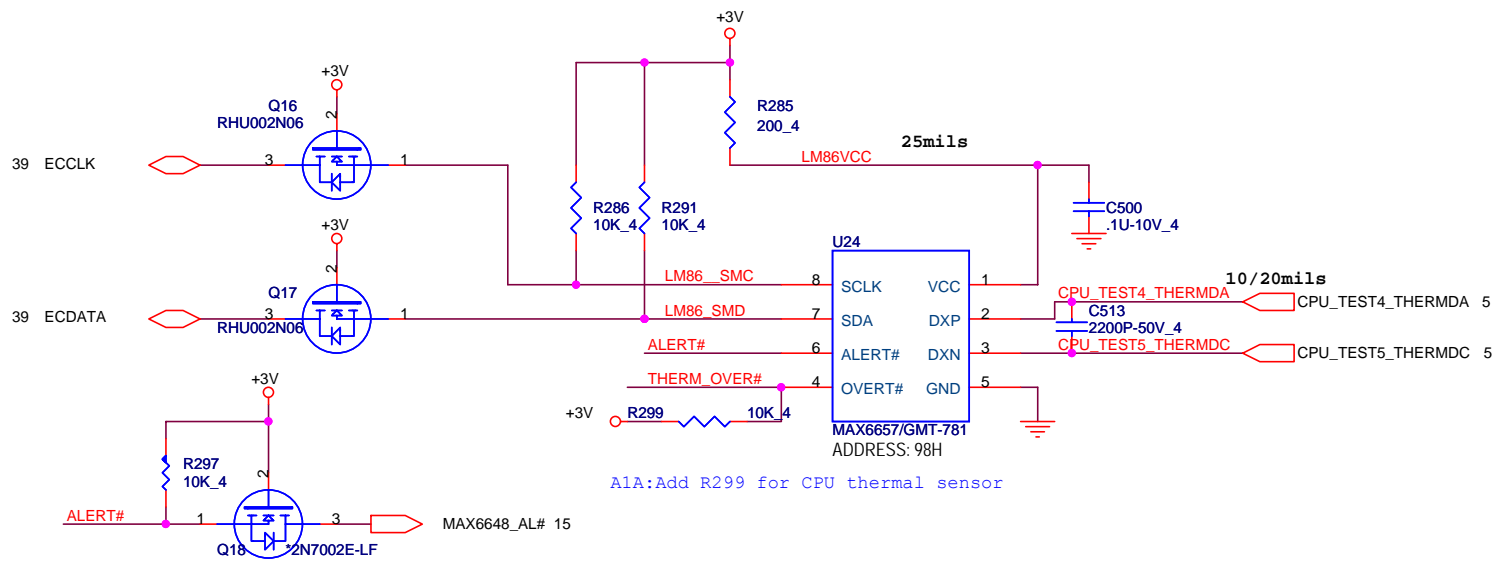
for RX485, VDD\_DVO should be connected to +1.8V, but ferrite bead and decoupling caps are not necessary

NB RS485 POWER STATES

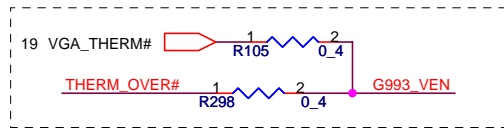
Power Signal	s0	s1	s3	s4/s5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

**PROJECT : ZC3**  
**Quanta Computer Inc.**

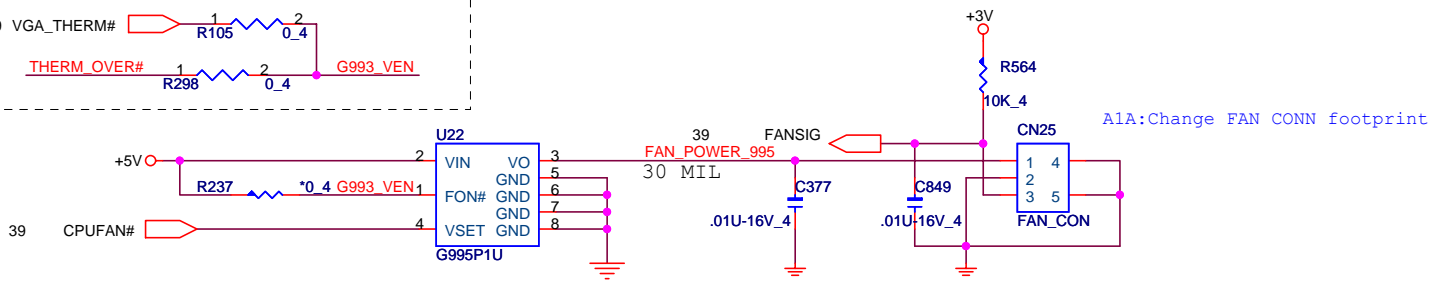
Size	Document Number	Rev
	<b>RS485-POWER</b>	1A
Date:	Thursday, June 08, 2006	Sheet 12 of 46



A1A:Add R105 for VGA thermal sensor



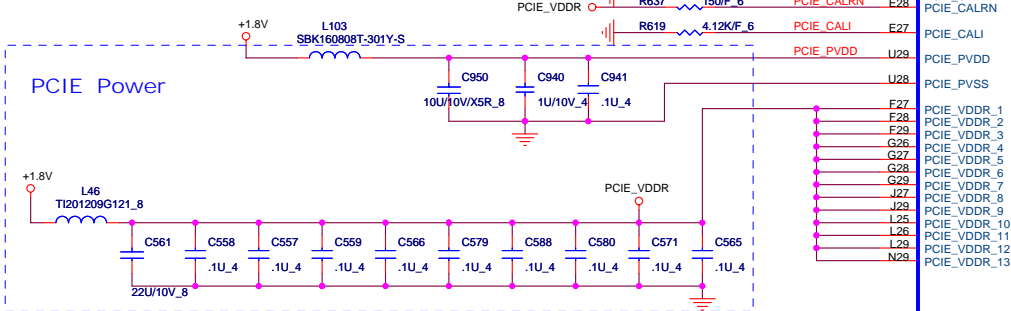
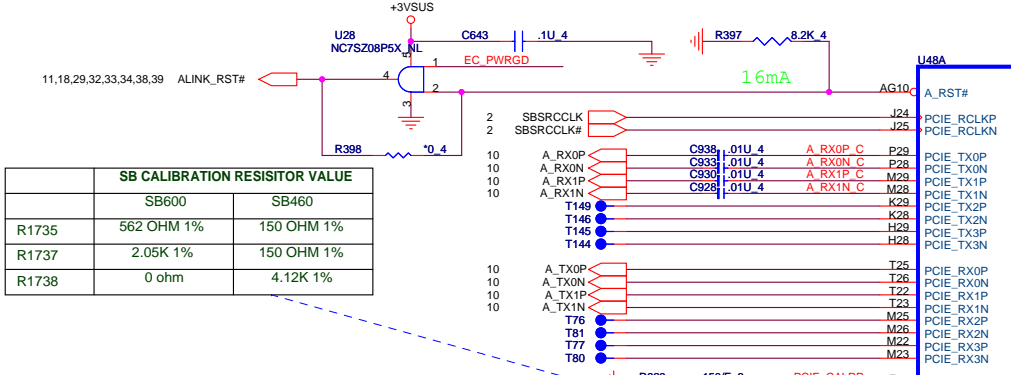
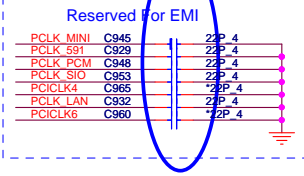
### CPU FAN



PROJECT : ZC3  
Quanta Computer Inc.

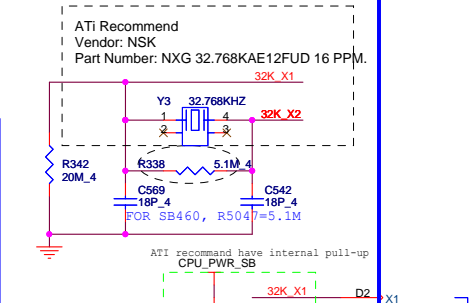
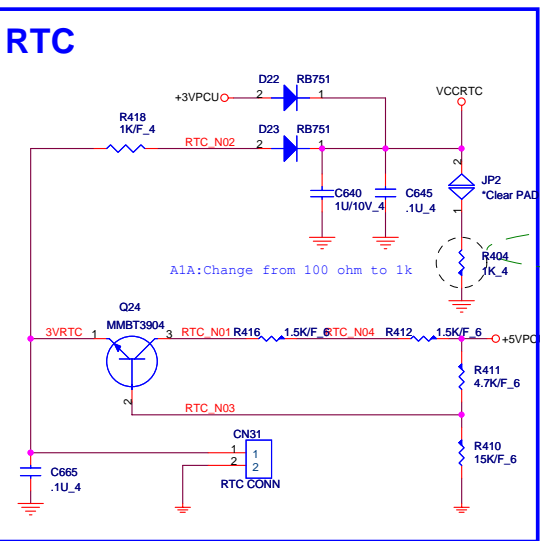
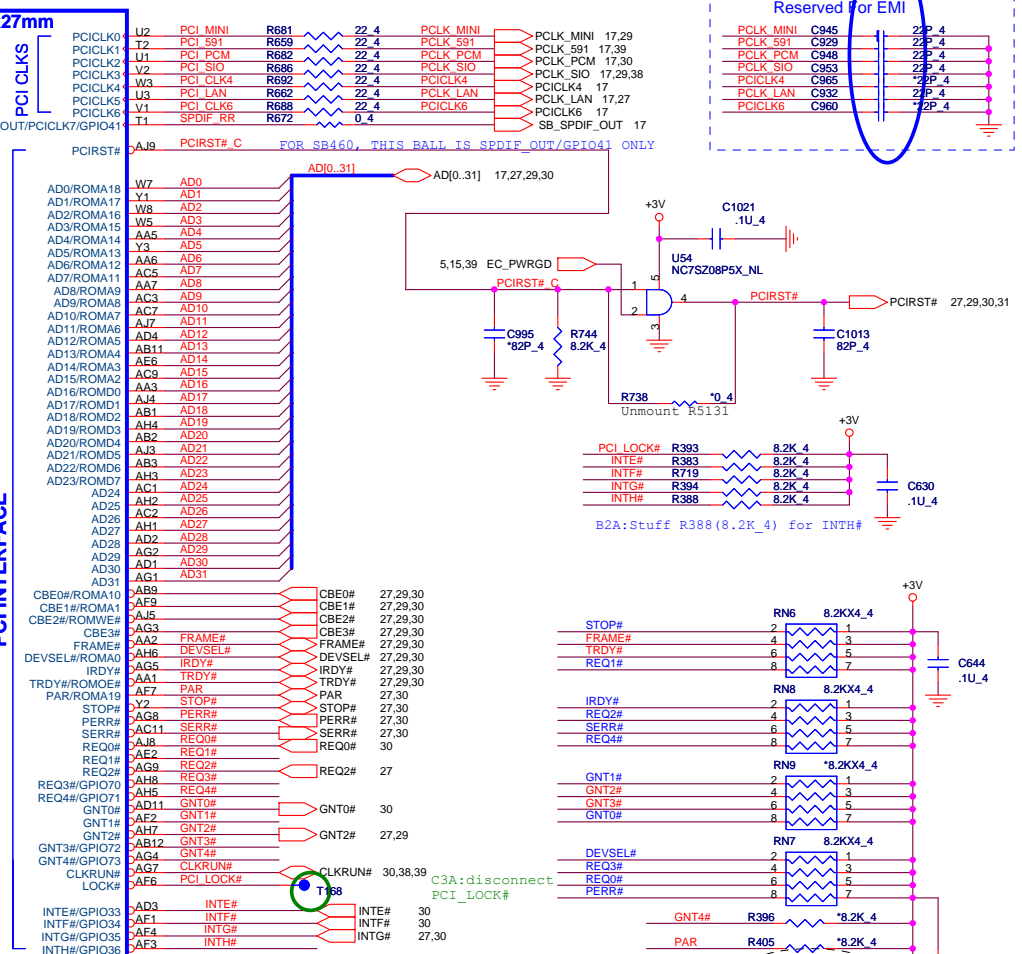
Size	Document Number	Rev
	Thermal Sensor,FAN	1A
Date:	Thursday, June 08, 2006	Sheet 13 of 46

B2A: For EMI stuff c945, c929, c948, c953, c932

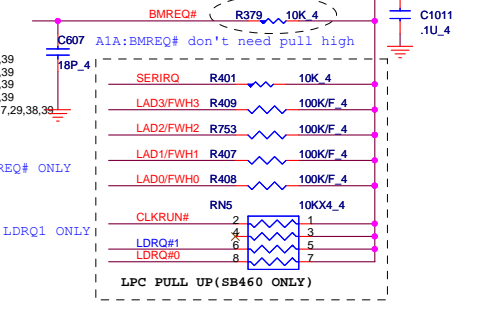
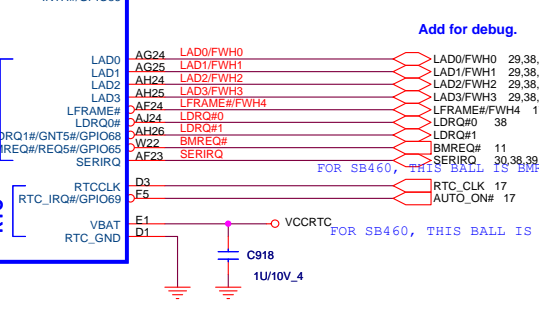
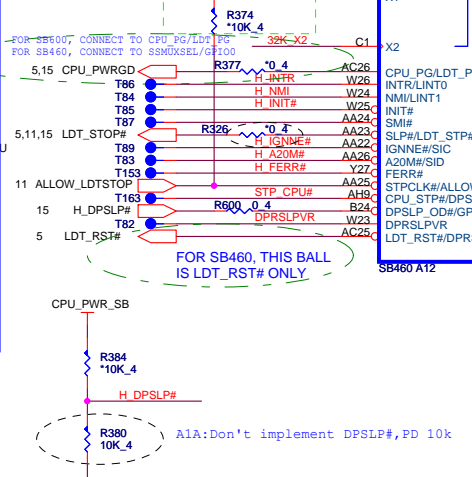


**PCI EXPRESS INTERFACE**

Part 1 of 4

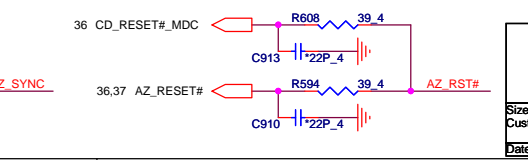
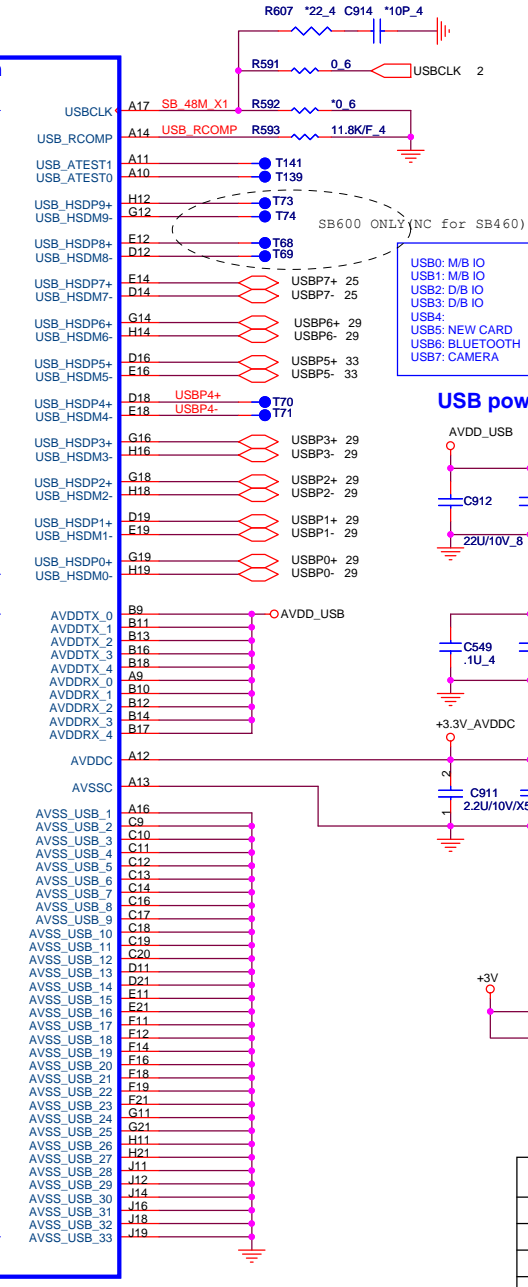
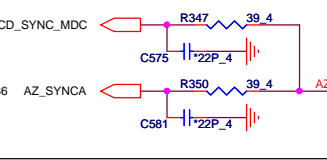
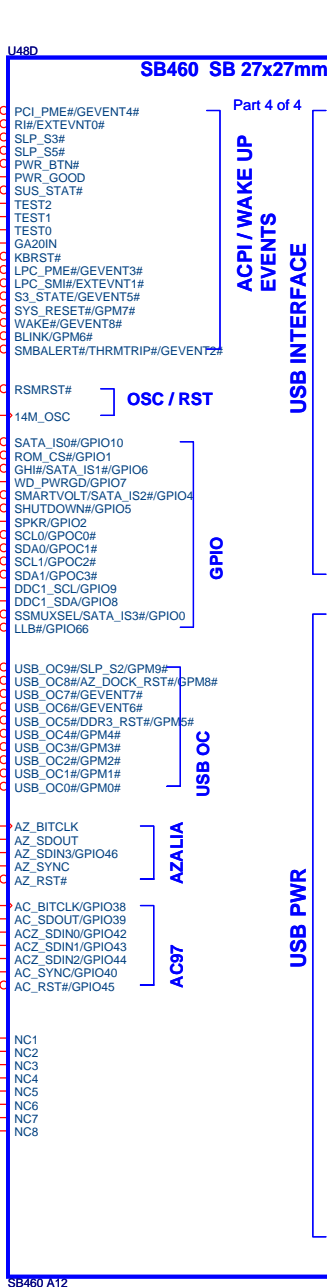
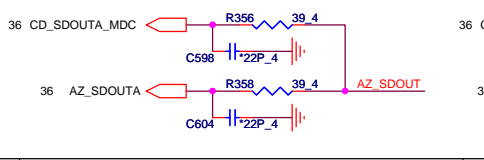
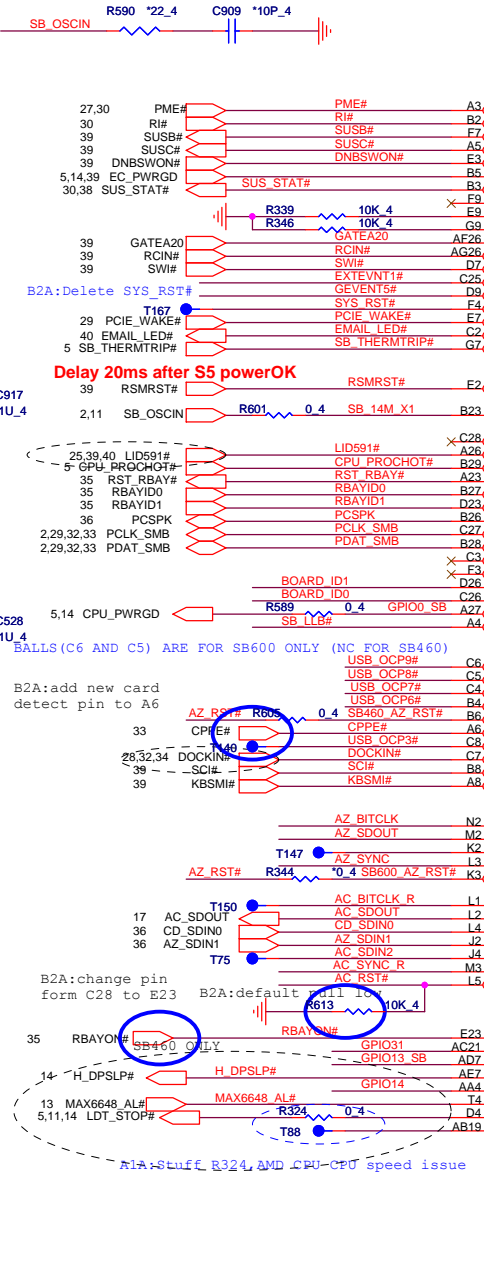
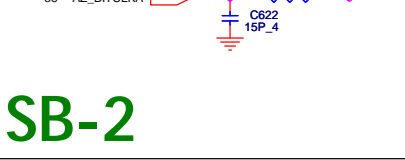
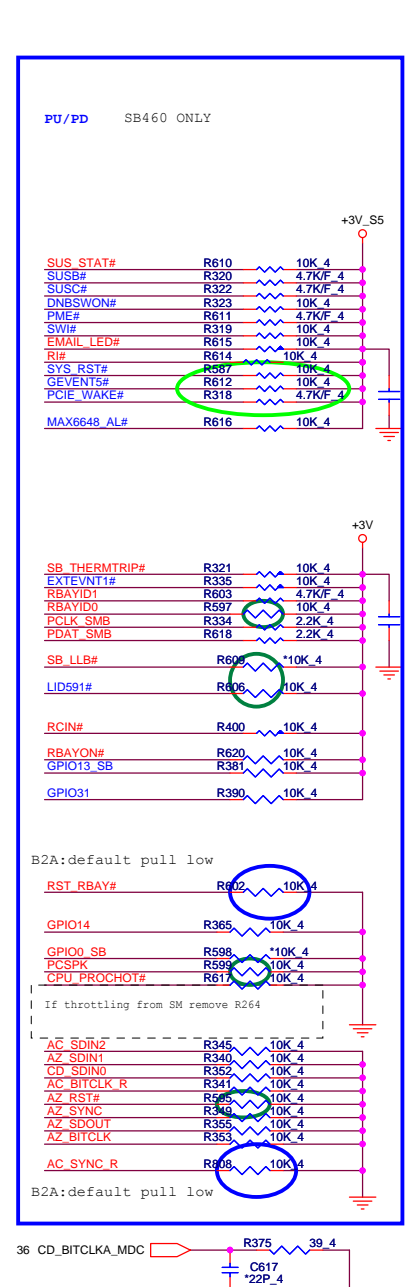


**XTAL**

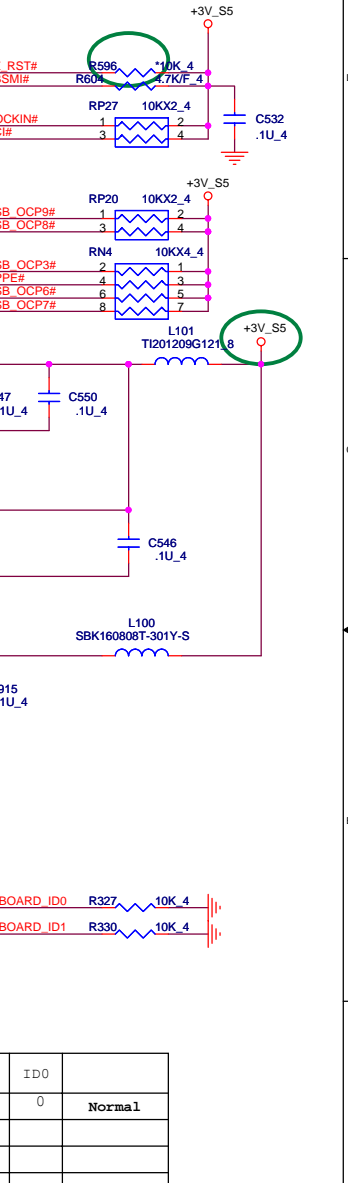


PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
TI 7412	AD25	REQ0# / GNT0#	INTE#, F#, G#	PCICLK2
BCM5788M	AD20	REQ2# / GNT2#	INTH#	PCICLK5

**SB-1**

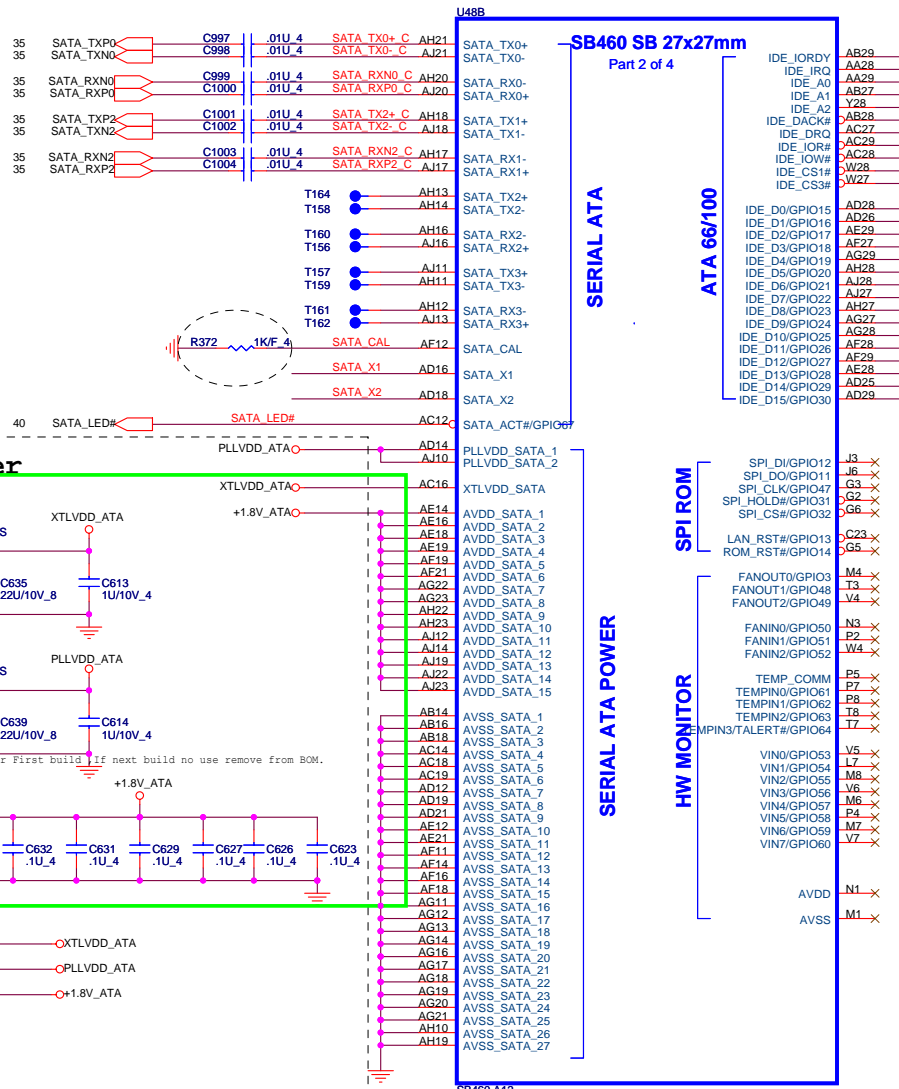


USB power use S3 power,But Over current signal datasheet is S5 only,BUT ATI FAE say use S3 is ok

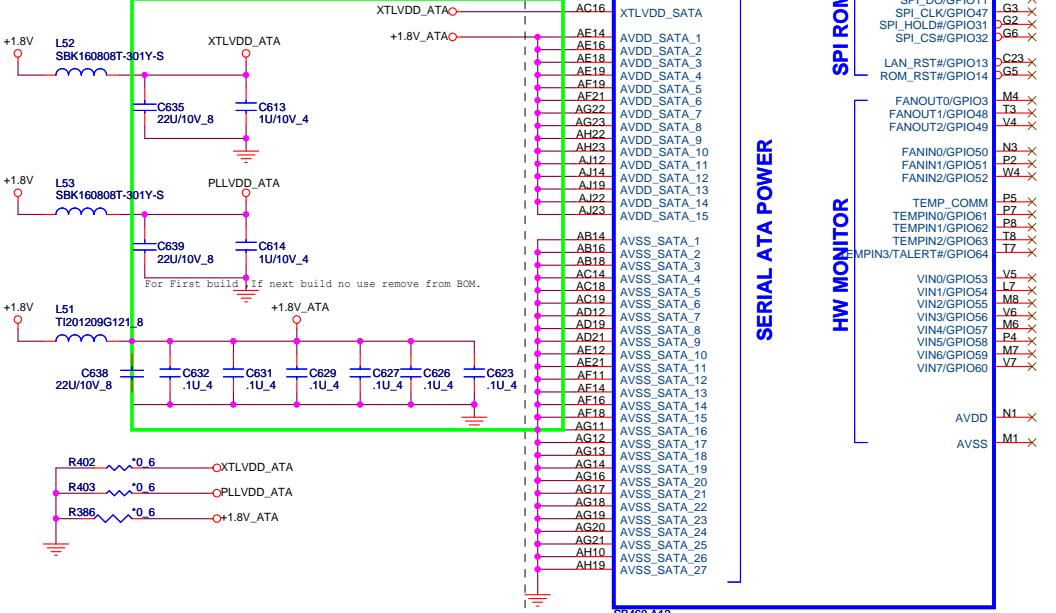


Board ID	ID1	ID0	Rev
00	0	0	Normal
01			
10			
11			

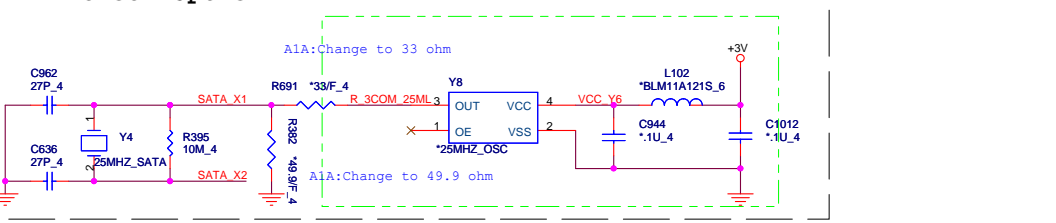




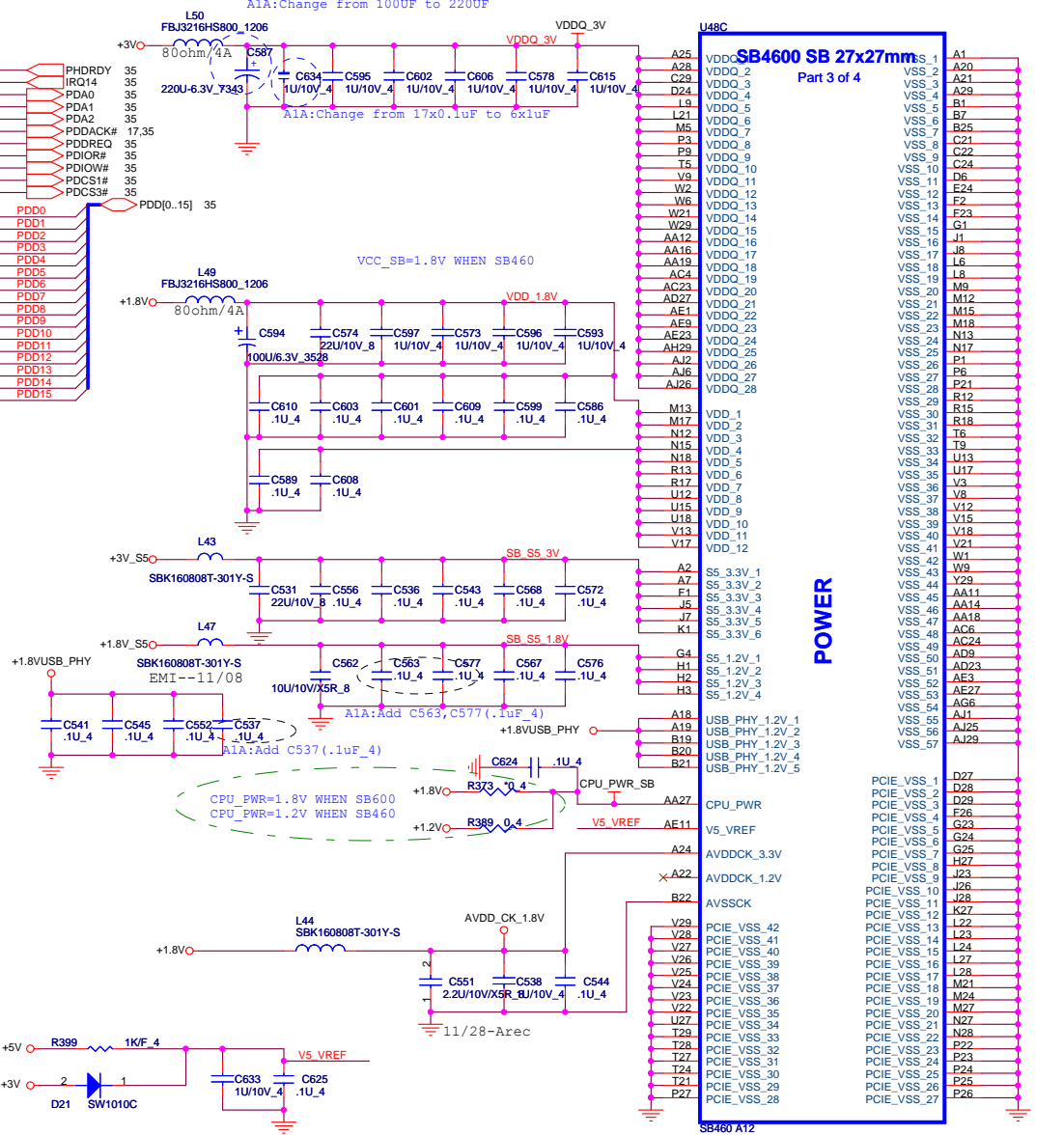
**SATA Power**



**SATA clock Option**



SB-3



SB460 SB 27x27mm Part 2 of 4

SB460 SB 27x27mm Part 3 of 4

SERIAL ATA

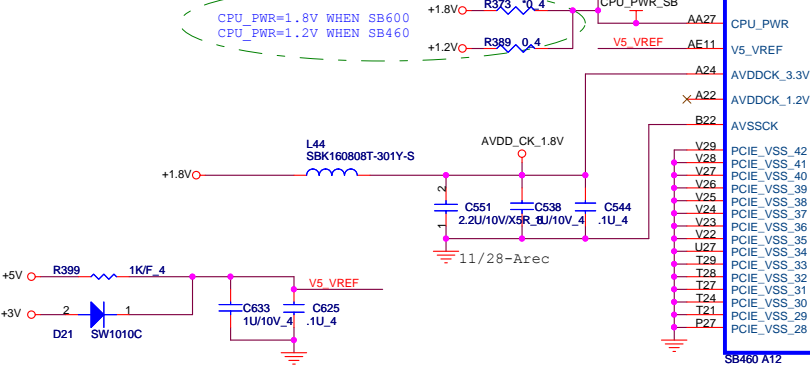
ATA 6E/100

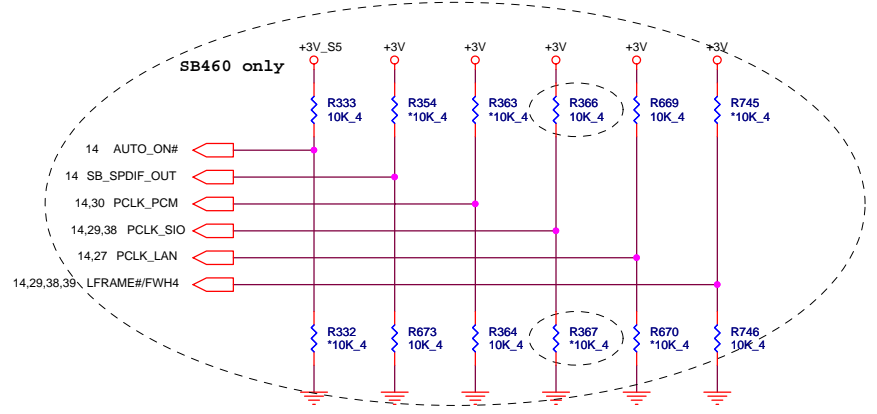
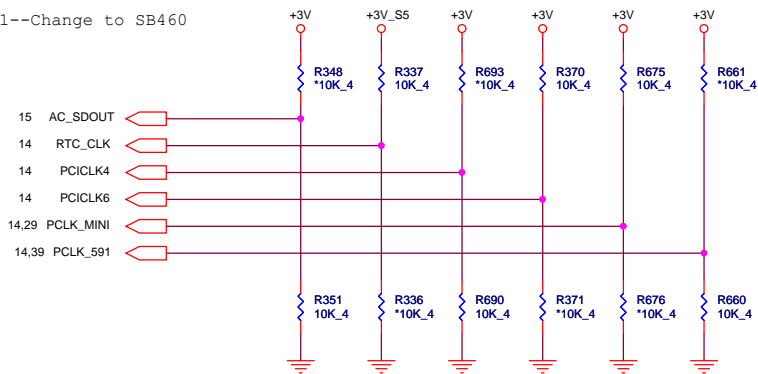
SPI ROM

HW MONITOR

SERIAL ATA POWER

POWER





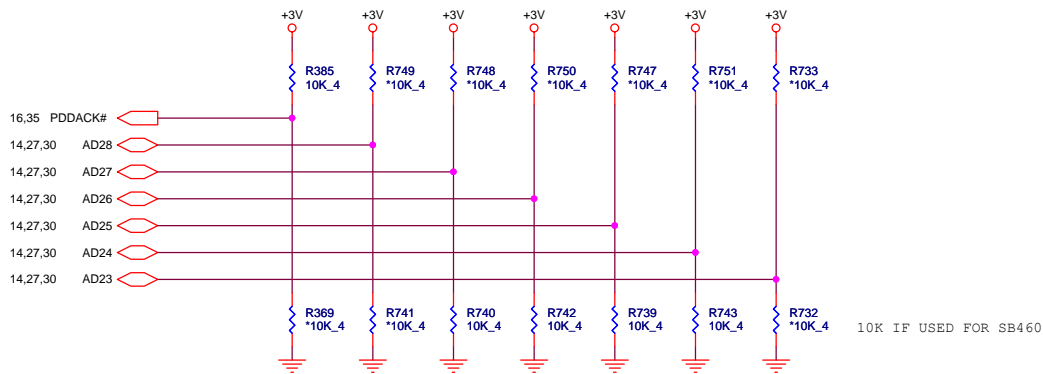
A1A:USB PHY POWERDOWN DISABLE

# REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI	PCLK_591
<b>PULL HIGH</b>	USE DEBUG STRAPS <i>DEFAULT</i>	INTERNAL RTC <i>DEFAULT</i>	USE INT. PLL48	CPU IF=K8 <i>DEFAULT</i>	PCI_CLK0	PCI_CLK1
<b>PULL LOW</b>	IGNORE DEBUG STRAPS <i>DEFAULT</i>	EXTERNAL RTC	USE EXT. 48MHZ <i>DEFAULT</i>	CPU IF=P4	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM L, L = FWH ROM NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
<b>PULL HIGH</b>	ACPWRON <i>DEFAULT</i>	SPDIF_OUT SIO 24MHz	PCI_CLK2 XTAL MODE <i>NOT SUPPORTED</i>	PCI_CLK3 USB PHY POWERDOWN DISABLE <i>DEFAULT</i>	PCI_CLK5 <i>DEFAULT</i>	LFRAME# ENABLE THERMTRIP#
<b>PULL LOW</b>	AUTO PWR ON	SIO 48MHz <i>DEFAULT</i>	48MHZ OSC MODE <i>DEFAULT</i>	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



# DEBUG STRAPS

	PDAK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET <i>DEFAULT</i>	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
<b>PULL LOW</b>	USE SHORT RESET		USE PCI PLL <i>DEFAULT</i>	USE ACPI BCLK <i>DEFAULT</i>	USE IDE PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	

SB460 only SB600 only

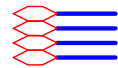


**PROJECT : ZC3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>SB460M STRAPS</b>	1A
Date:	Thursday, June 08, 2006	Sheet 17 of 46

PCIE TEST PADS  
 PCIE TEST POINTS MUST BE WITHIN 250 MILS  
 OF THE ASIC BALL WITH POSITIVE AND NEGATIVE  
 SIGNALS THE SAME DISTANCE

10 PEG\_RXP[15:0]  
 10 PEG\_RXN[15:0]  
 10 PEG\_TXP[15:0]  
 10 PEG\_TXN[15:0]



A1A:PCI-E 16X LAN are Swap

U38A

PART 1 OF 7



P  
C  
I  
-  
E  
X  
P  
R  
E  
S  
S  
  
I  
N  
T  
E  
R  
F  
A  
C  
E



Clock

PCIE\_REFCLKP

PCIE\_REFCLKN

PERSTB

PCIE\_TEST

PERSTB\_MASK

EV@M56-P B26

Change M56 to B26 version

Calibration

PCIE\_CALRN

PCIE\_CALRP

PCIE\_CALI



FOR M52P, M54P, M56P  
 PCIE\_CALRN = 2K  
 PCIE\_CALRP = 562R  
 PCIE\_CALI = 1.47K

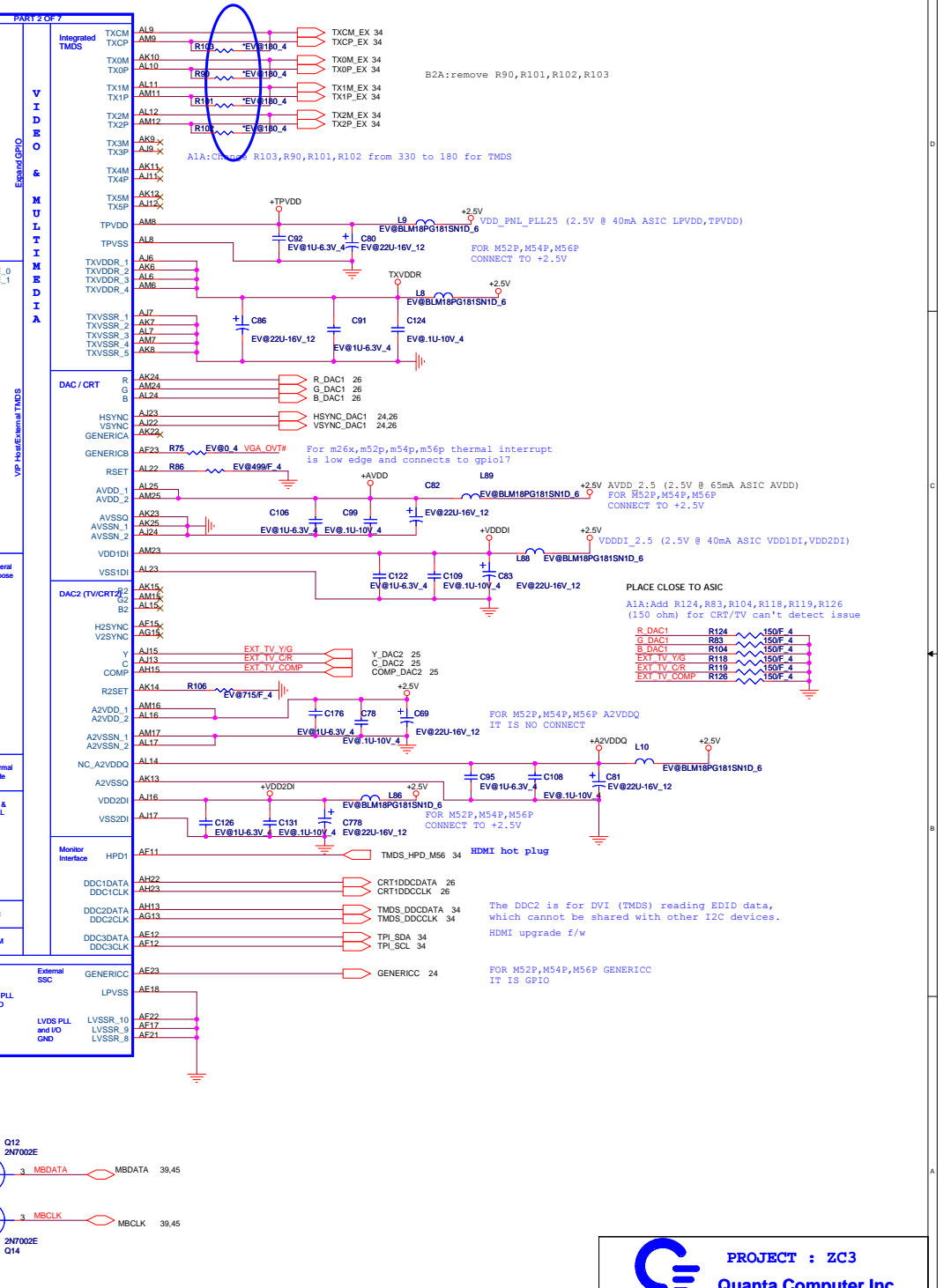
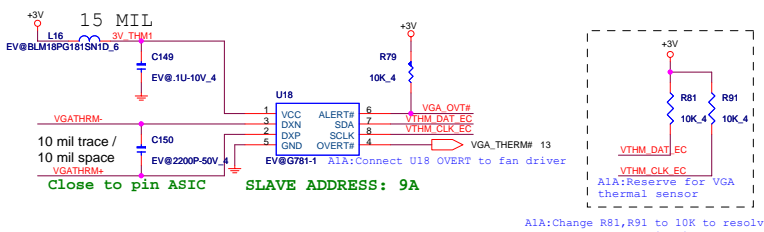
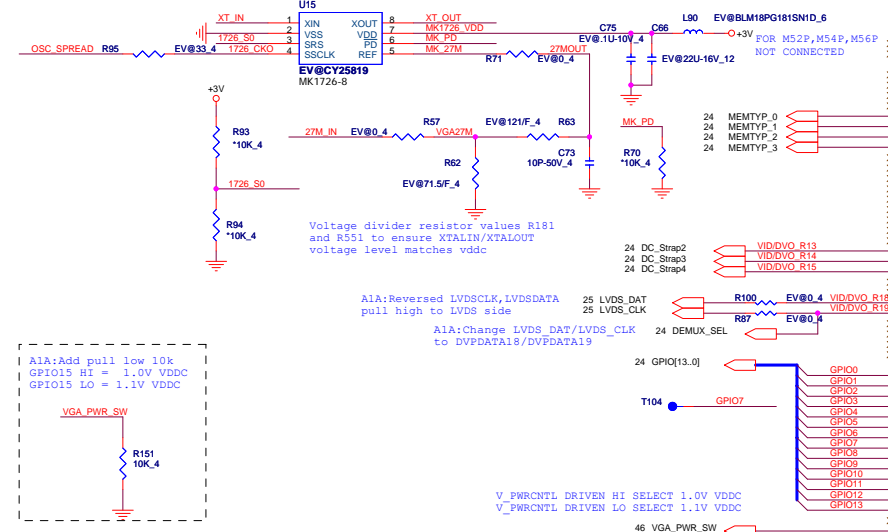


PROJECT : ZC3  
 Quanta Computer Inc.

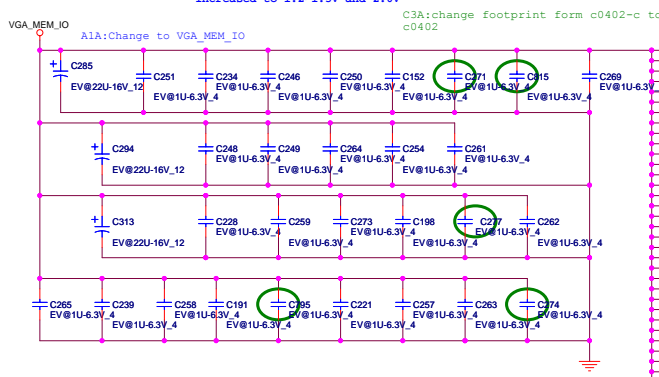
Size	Document Number	Rev
	<b>M56P 1 OF 7</b>	1A
Date:	Thursday, June 08, 2006	Sheet 18 of 46

MEMORY CLOCK SPREAD SPECTRUM

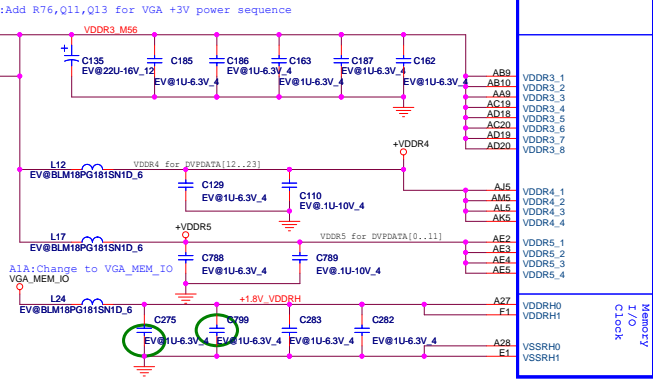
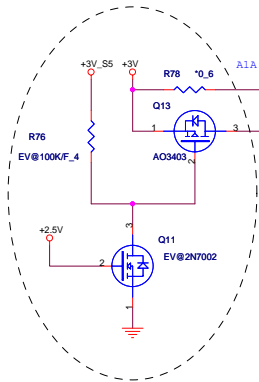
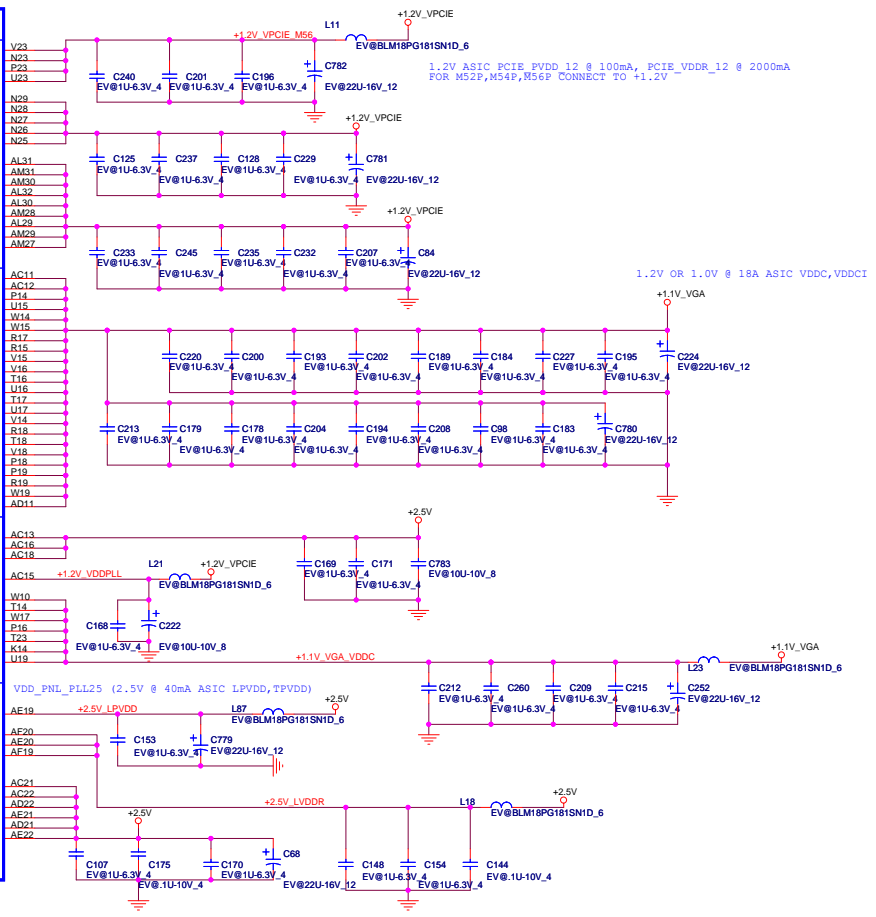
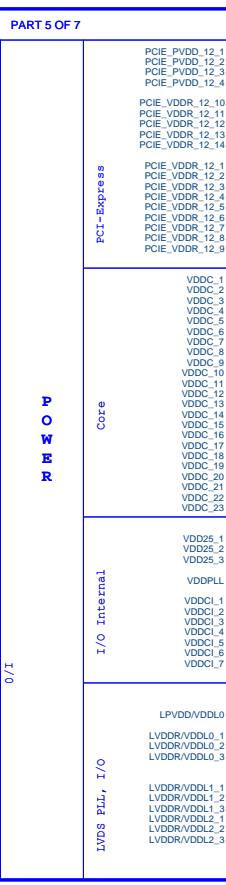
ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS  
**For HDMI use**  
 34 GPU\_SWRSTR T5  
 34 GPU\_GPIO\_PGMM T5  
 34 TPL\_SCL\_GATE T5  
 T103 T5  
 T6 T5  
 T10 T5  
 T1 T5  
 T2 T5  
 T3 T5  
 T8 T5  
 T11 T5  
 T7 T5  
 T9 T5  
 T13 T5  
 AG8 GPIO\_34  
 AH7 GPIO\_33  
 AG9 GPIO\_32  
 AH8 GPIO\_31  
 AJ8 GPIO\_30  
 AG10 GPIO\_29  
 AH9 GPIO\_28  
 AF10 GPIO\_27  
 AH5 GPIO\_26  
 AE8 GPIO\_25  
 AE9 GPIO\_24  
 AE7 GPIO\_23  
 AE4 GPIO\_22  
 AE5 GPIO\_21  
 AE6 GPIO\_20  
 AF12 GPIO\_19  
 AF13 GPIO\_18



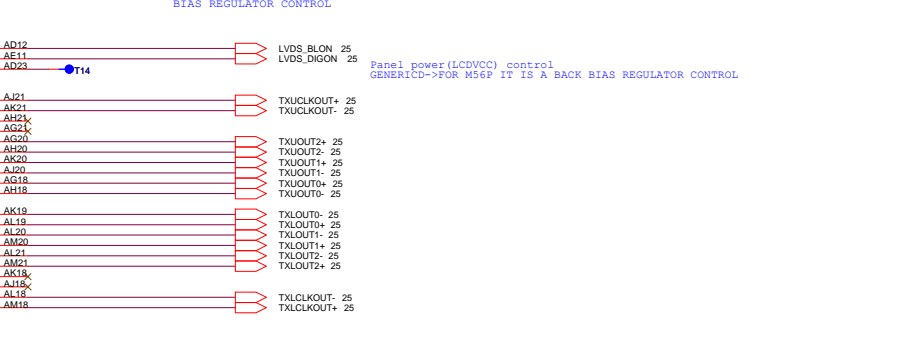
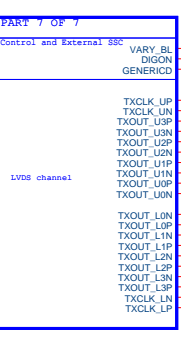
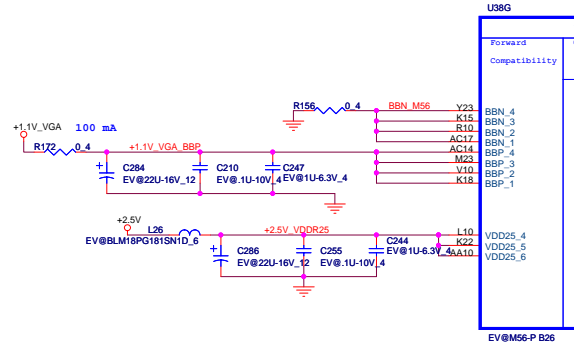
If memory interface has to be up to 600MHz or above, the GPU core voltage and memory I/O voltage may need to be increased to 1.2-1.3V and 2.0V

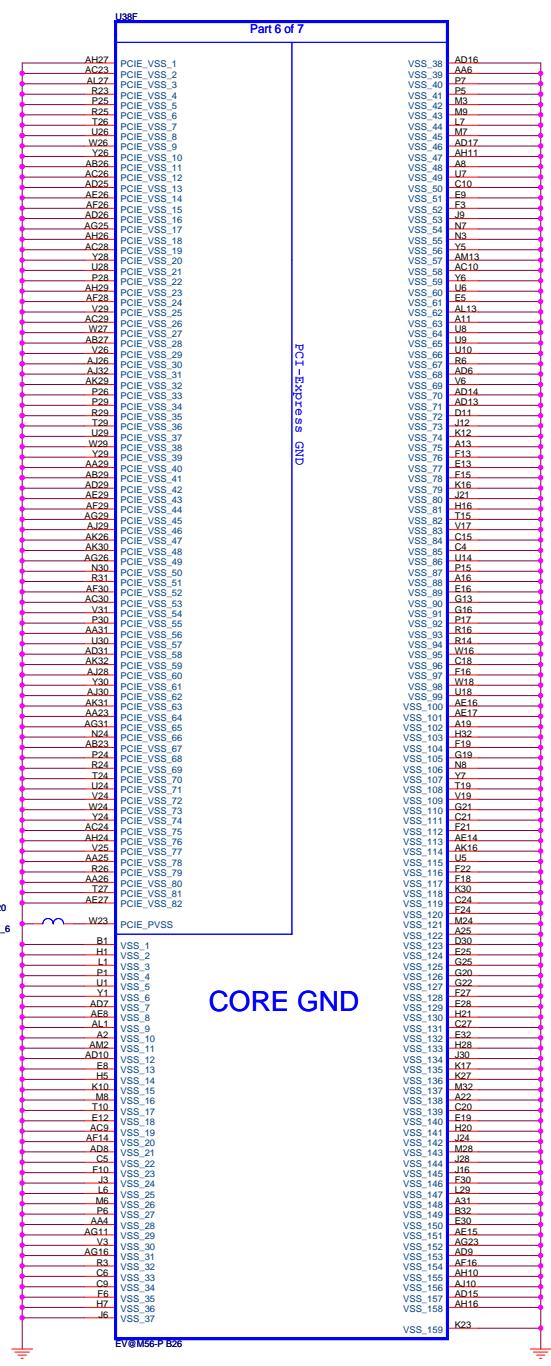


Pin	Signal
C1	VDDR1_1
J1	VDDR1_2
R1	VDDR1_3
L1	VDDR1_4
V1	VDDR1_5
A1	VDDR1_6
A3	VDDR1_7
P9	VDDR1_8
N9	VDDR1_9
N10	VDDR1_10
P10	VDDR1_11
A9	VDDR1_12
P8	VDDR1_13
C9	VDDR1_14
Y9	VDDR1_15
J11	VDDR1_17
A21	VDDR1_18
M10	VDDR1_20
N10	VDDR1_21
V21	VDDR1_22
J18	VDDR1_23
K21	VDDR1_24
A12	VDDR1_25
H12	VDDR1_26
A15	VDDR1_27
J20	VDDR1_28
J13	VDDR1_29
K11	VDDR1_30
K19	VDDR1_31
A18	VDDR1_32
L23	VDDR1_33
K24	VDDR1_34
K20	VDDR1_35
H19	VDDR1_36
A24	VDDR1_37
K13	VDDR1_38
J32	VDDR1_39
A30	VDDR1_40
C32	VDDR1_41
A30	VDDR1_42
C32	VDDR1_43
F32	VDDR1_45
L32	VDDR1_46



GENERIC : FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

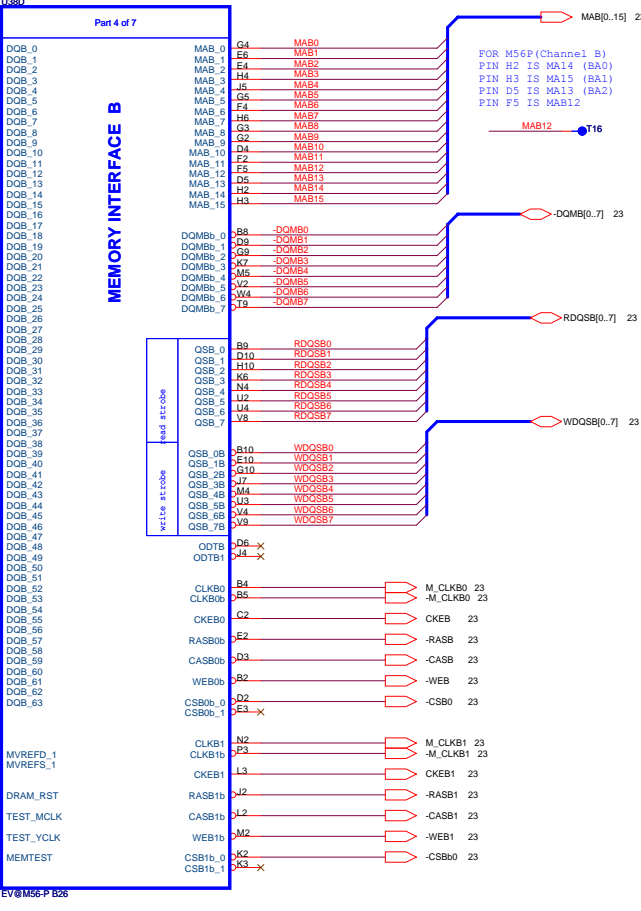
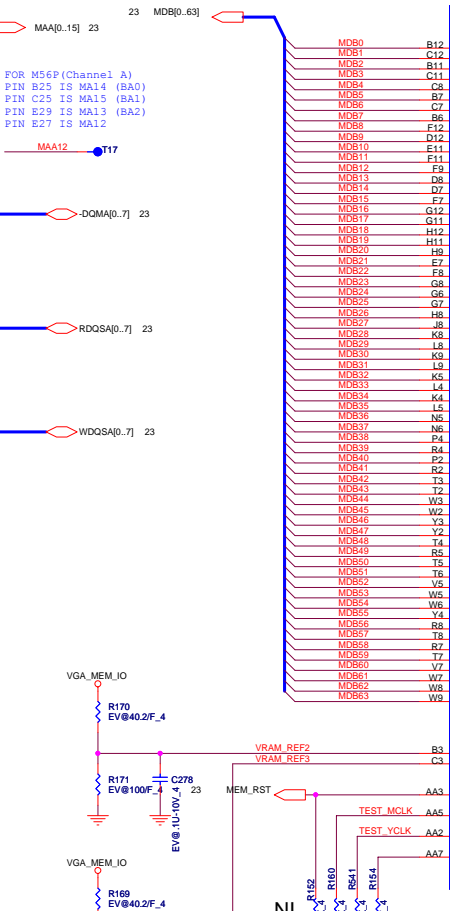
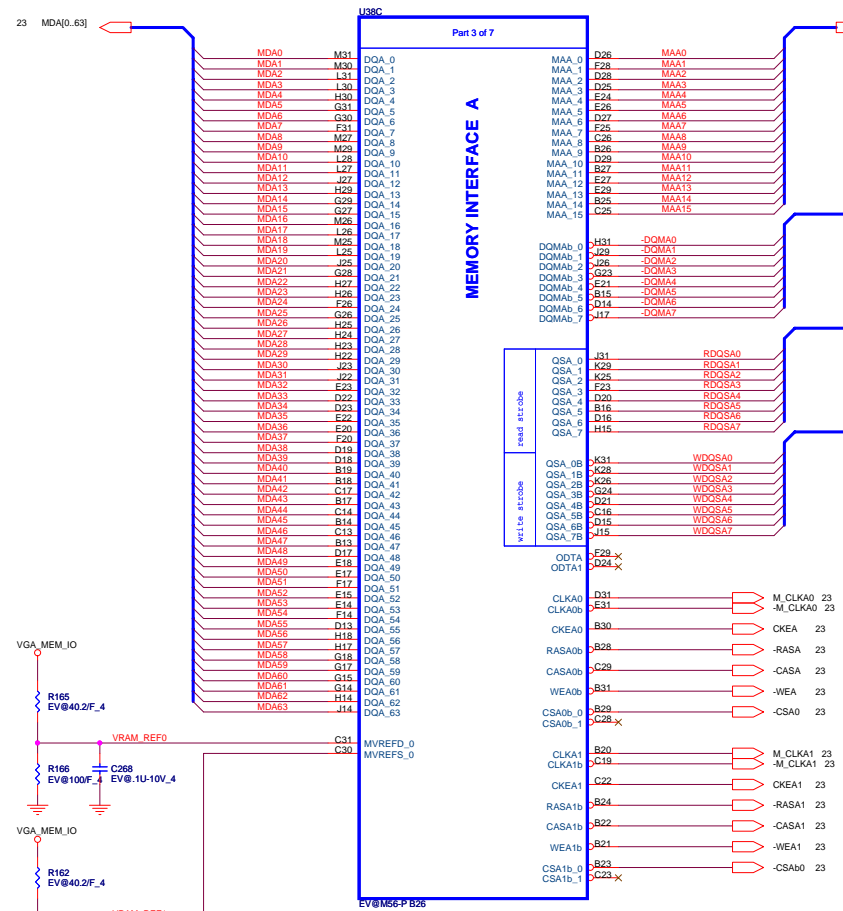




# RV410 MEMORY CHANNELS A and B

## Channel A

## Channel B



Place VRAM\_REF0, VRAM\_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)  
 MVREFD\_[0:1] (0.7 \* VDDR1) (for GDDR3)  
 MVREFS\_[0:1] (0.7 \* VDDR1) (for GDDR3)

Reference voltage per channel (memory data/strobe)  
 MVREFD\_[0:1] (0.7 \* VDDR1) (for GDDR3)  
 MVREFS\_[0:1] (0.7 \* VDDR1) (for GDDR3)

Reference voltage per channel (memory data/strobe)  
 MVREFD\_[0:1] (0.7 \* VDDR1) (for GDDR3)  
 MVREFS\_[0:1] (0.7 \* VDDR1) (for GDDR3)



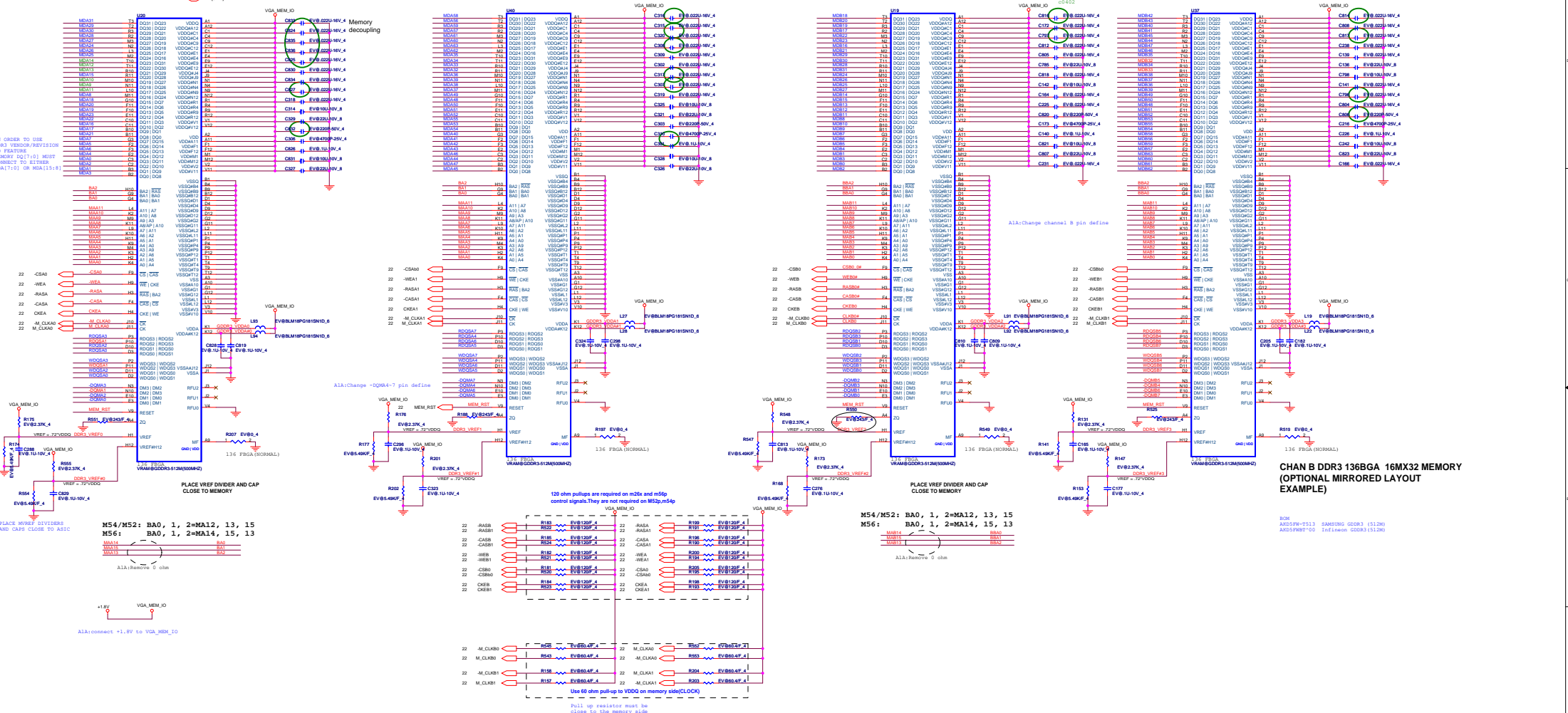
# 512 Mbit GDDR3 Channels A and B Rank 1

ROMAN: J1 22  
ROGAE: J1 22  
VOCAS: R1 22  
MAD: R1 22  
MAD: R1 22

C3A:change footprint form c0402-c to c0402

ROMAN: J1 22  
ROGAE: J1 22  
VOCAS: R1 22  
MAD: R1 22  
MAD: R1 22

C3A:change footprint form c0402-c to c0402



IN ORDER TO USE  
DUAL VENDOR PARTITION  
ID PARTNER  
MEMORY S0[10] MUST  
CONNECT TO EITHER  
M0A[10] OR M0B[10]

PLACE VREF DIVIDERS  
AND CAPS CLOSE TO ASIC

M54/M52: BA0, 1, 2=MA12, 13, 15  
M56: BA0, 1, 2=MA14, 15, 13

A1A:mem7=0 ohm

+1.8V VGA\_MEM\_I0

A1A:connect +1.8V to VGA\_MEM\_I0

Use 80 ohm pull-up to VDD on memory sdn(CLOCK)

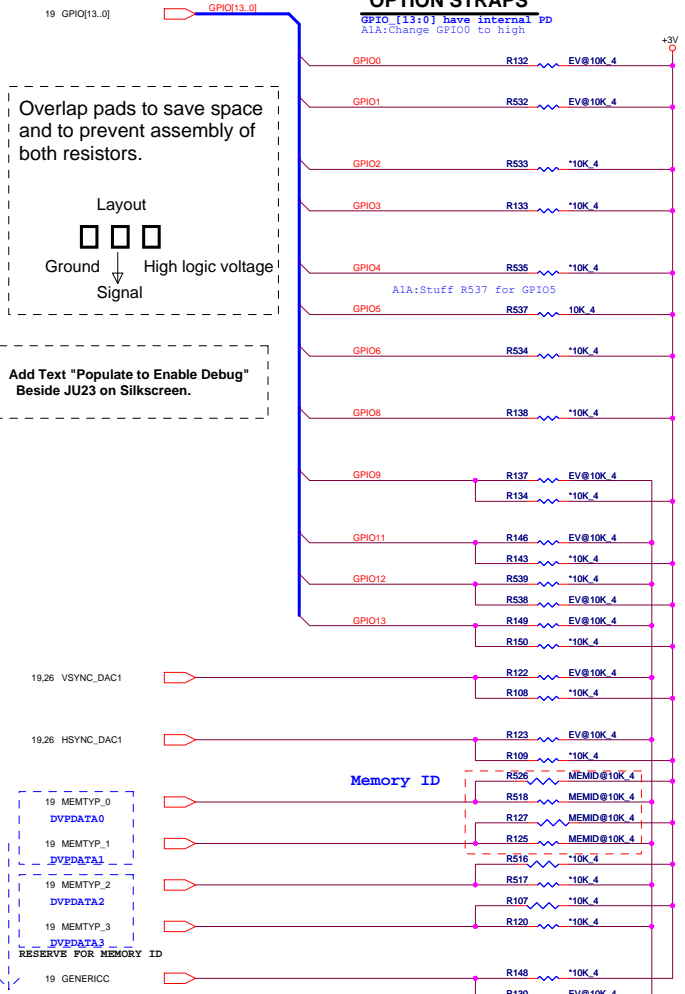
Pull up resistor must be close to the memory side

CHAN B DDR3 136GBA 16MX32 MEMORY  
(OPTIONAL MIRROR LAYOUT  
EXAMPLE)

B0A  
ARD5PW-TS13 SAM800 GDDR3 (512M)  
ARD5PW-TS13 SAM800 GDDR3 (512M)

### OPTION STRAPS

GPIO [13:0] have internal PD  
A1A:Change GPIO0 to high



### M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPHLEN	GPIO1	TRANSMITTER DC-EMPHASIS ENABLE FOR M56, M50P: INSTALL WITH ATI R540, R540D, R540E, R5410, R5452 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M28X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM MEM_AP_SIZE=0(128MB) 001x - No ROM MEM_AP_SIZE=0(128MB) 010x - No Rom MEM_AP_SIZE=10(64MB) 011x - No ROM MEM_AP_SIZE=1(Reserved) 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45D5011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NX25F01B ROM (ISSI), chip IDs from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0 - Slave VIP host port device present, 1 - No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

### Board Straps

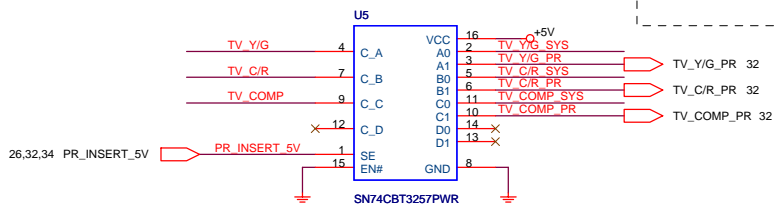
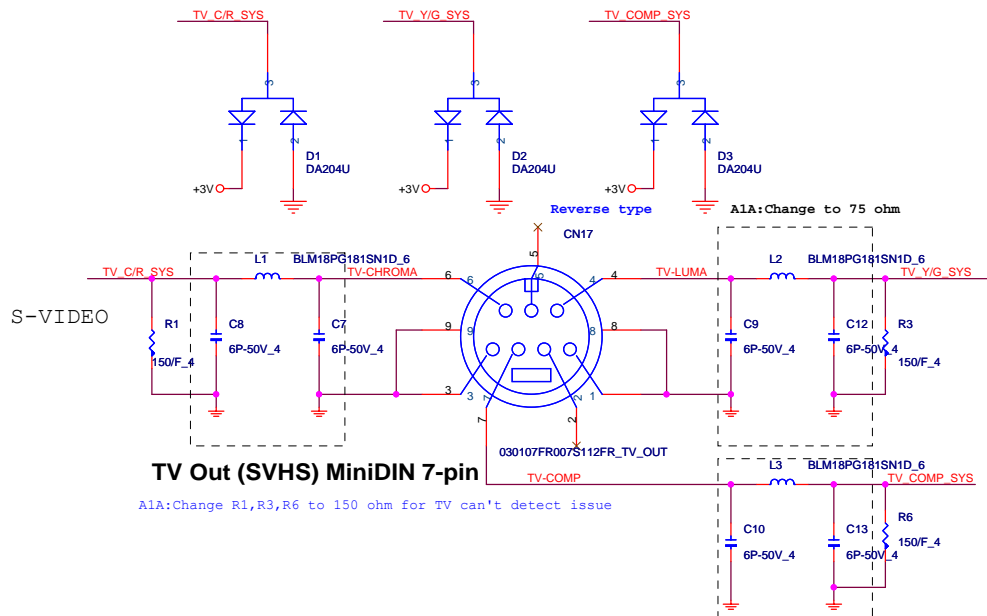
REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVPDATA(1:0)	MEMORY TYPE AND SIZE SELECT->DVPDATA(1:0) 00 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 01 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Hynix GDDR 3 memory(512Mb) 136 Ball BGA package 11 - Reserved	00
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Not detected	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	10
PALNTSC	LCDDATA(18)	TV0 Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1

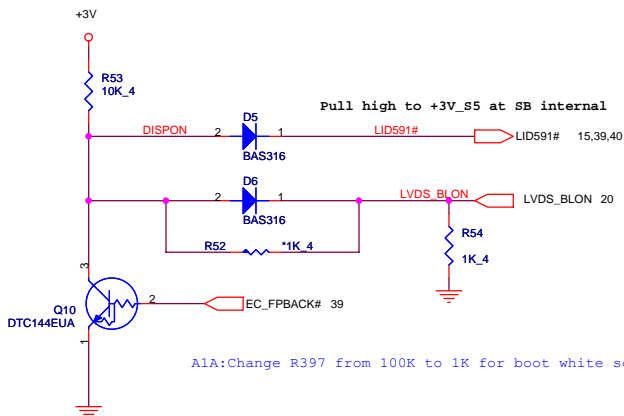
MEMORY TYPE AND SPEED SELECT

A1A:change video capture enable setting

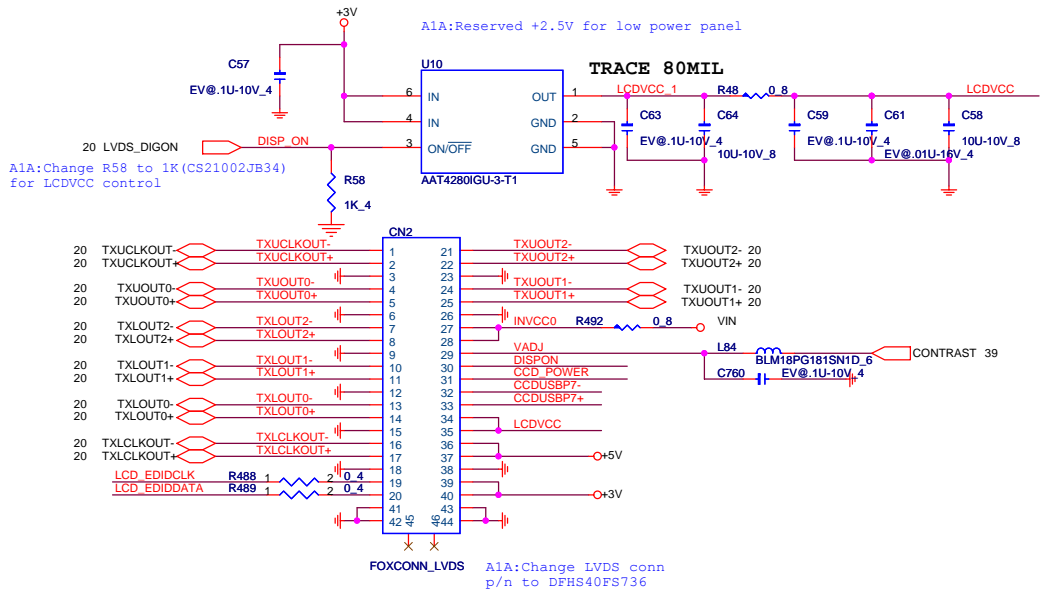
**PROJECT : ZC3**  
**Quanta Computer Inc.**



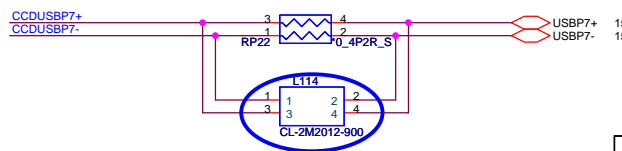
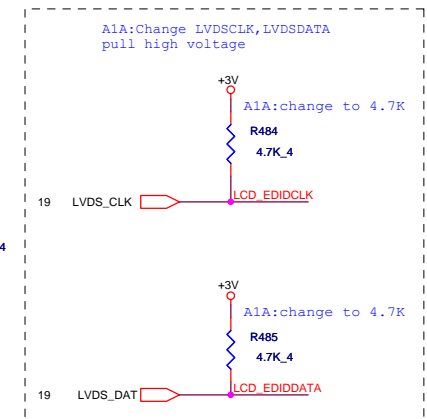
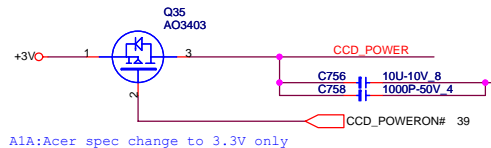
A1A:Change to SN74CBT3257PWR (Vin 5V)



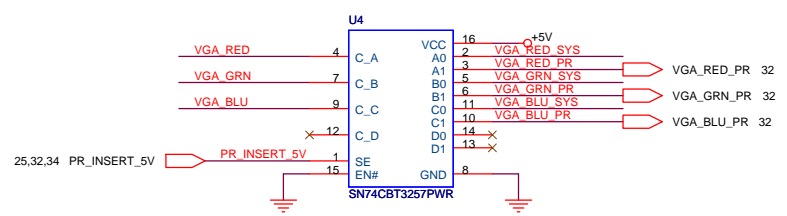
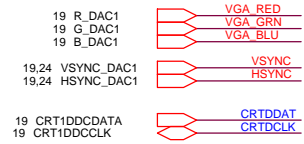
A1A:Change R397 from 100K to 1K for boot white screen issue



**CAMERA MODULE CONNECTOR**



C3A: change EMI FILTER to CL-2M2012-900JT for EMI request

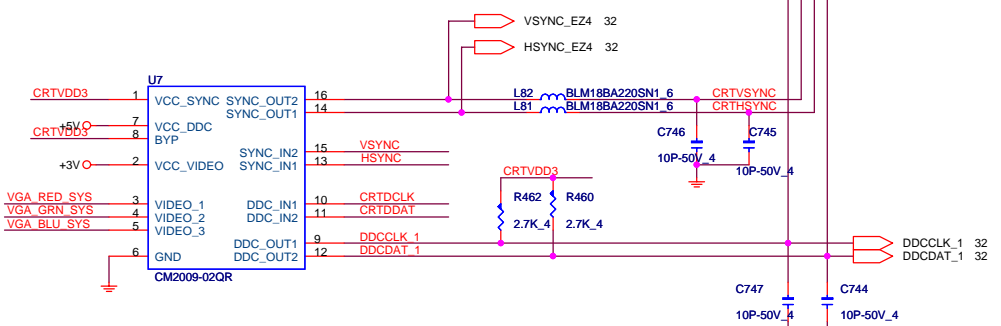
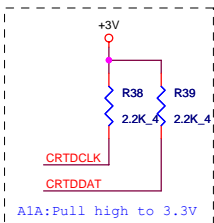
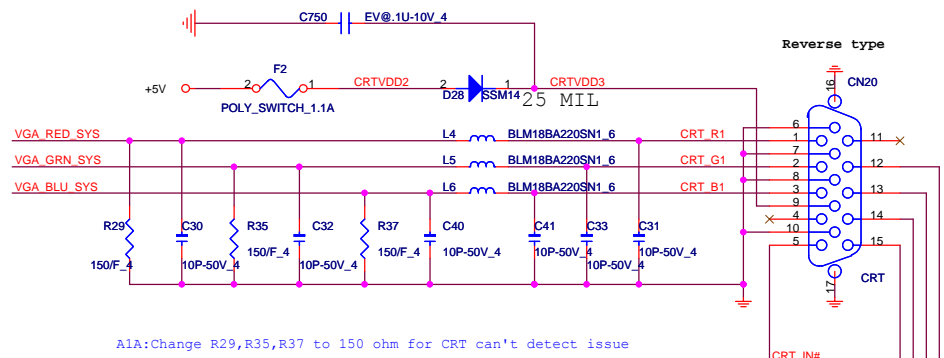
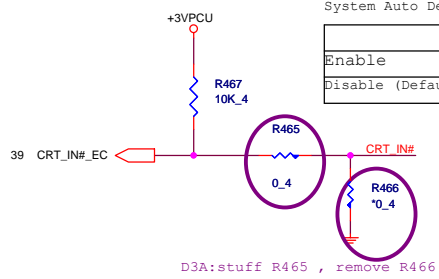



A1A: Change to SN74CBT3257PWR (Vin 5V)

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

System Auto Detect External CRT Device

	R7059	R7058	R27
Enable	Not stuffed	Stuffed	Stuffed
Disable (Default)	Stuffed	Not stuffed	Stuffed



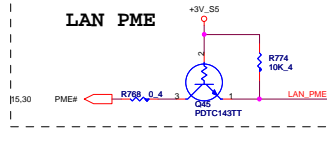
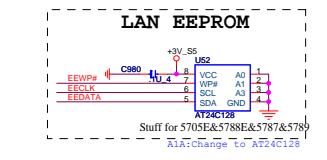
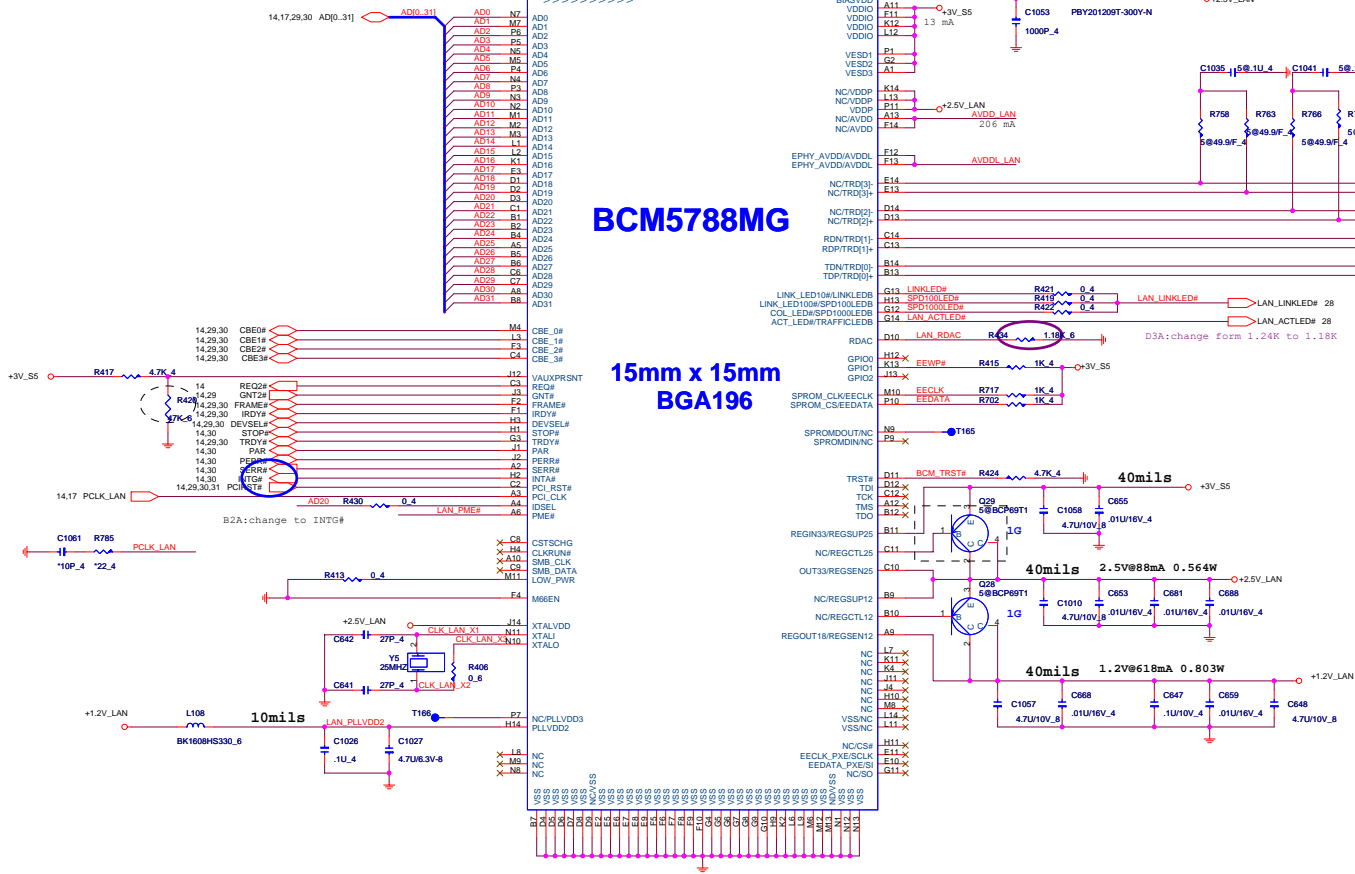
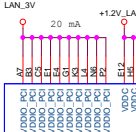


**PROJECT : ZC3**  
**Quanta Computer Inc.**

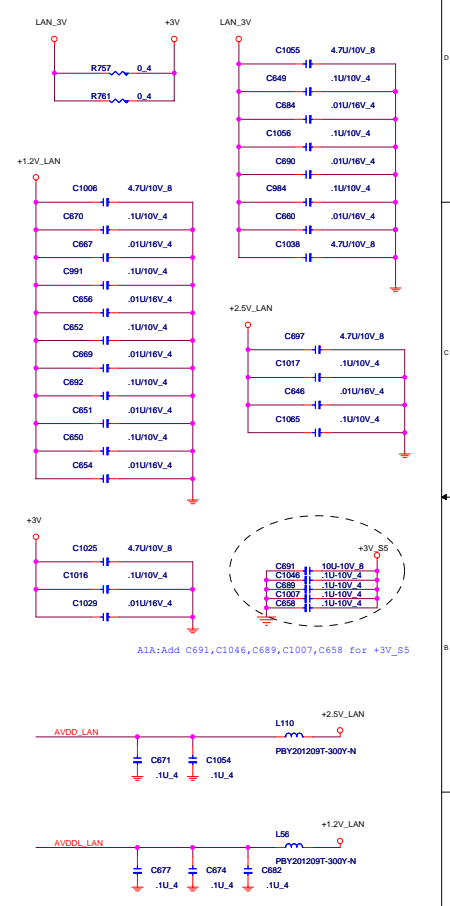
Size	Document Number	Rev
	<b>CRT-PORT</b>	1A
Date:	Thursday, June 08, 2006	Sheet 26 of 46

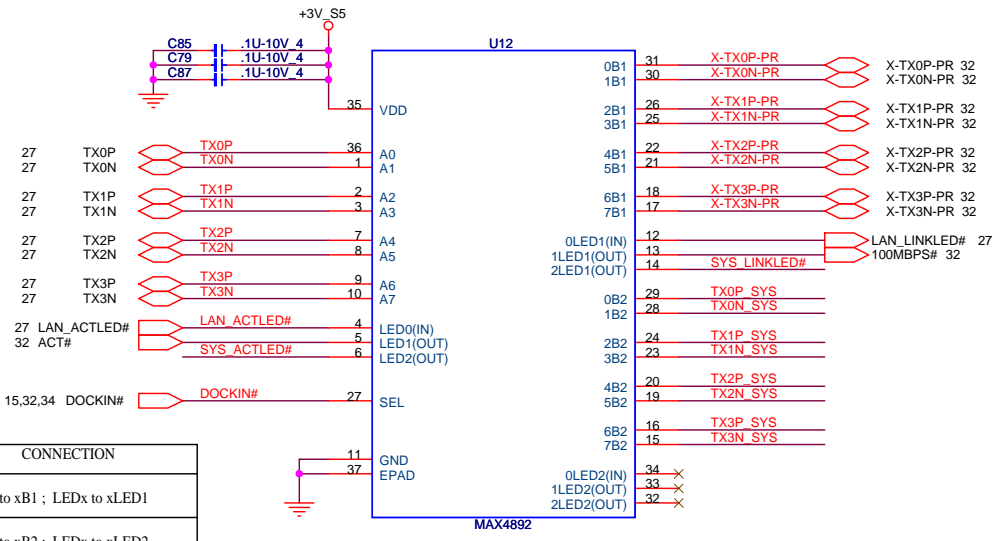
Voltage Rail	BCM5788MG
VDDIO_PCI	+3VBRUN (PCI SW)
2.5V_LAN	2.5V
1.2V_LAN	1.2V

LAN  
BCM5787MKFBG :  
AD20 RBQ2#  
GNT2# INTF#



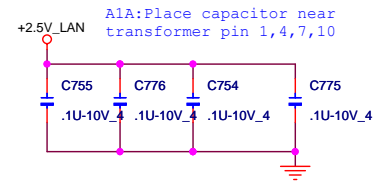
## BCM 5788M LAN Power



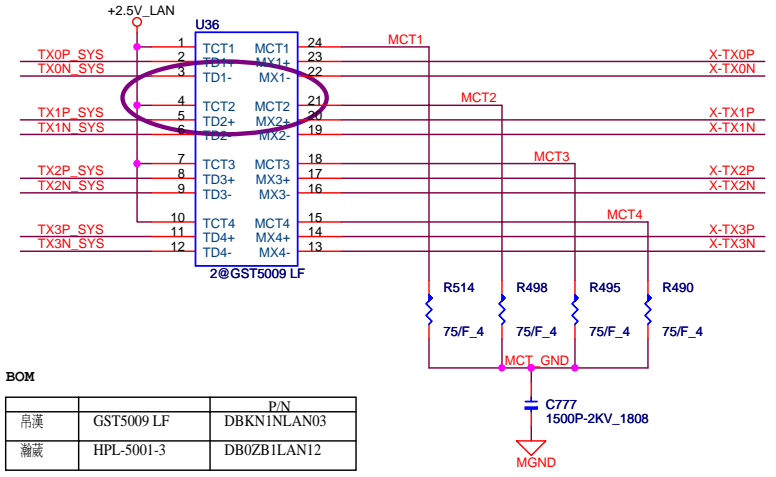


SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2

A1A:Change RJ45 CONN to C100A2-108A4L  
 A1A:Change RJ45 TX,RX pin define

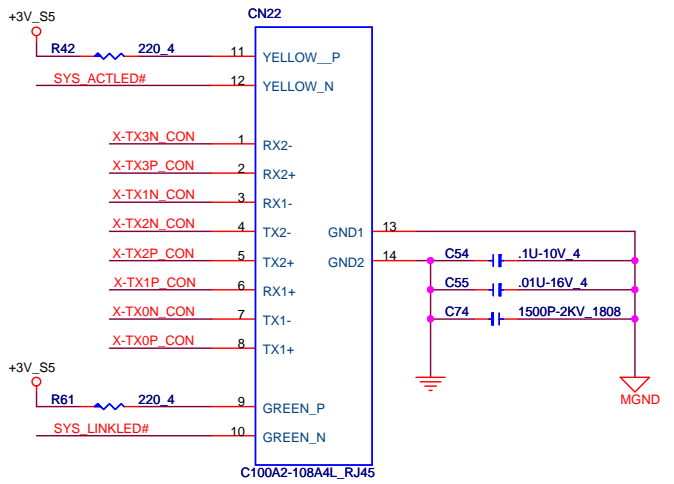
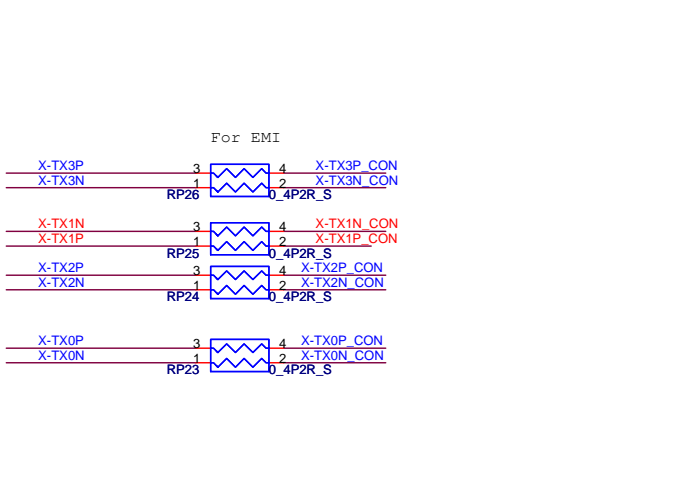


D3A:change transformer to meet IEEE test, update to ???????????



**BOM**

料號	規格	P/N
用漢	GST5009 LF	DBKN1NLAN03
翰藏	HPL-5001-3	DB0ZB1LAN12



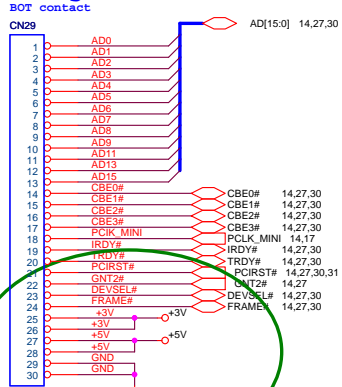
LED1	A1(+)	A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+)	B2(-)	LINK 10/100/1000	GREEN

A1A:Add diode for 10/100M & 1000M led control

**PROJECT : ZC3**  
**Quanta Computer Inc.**

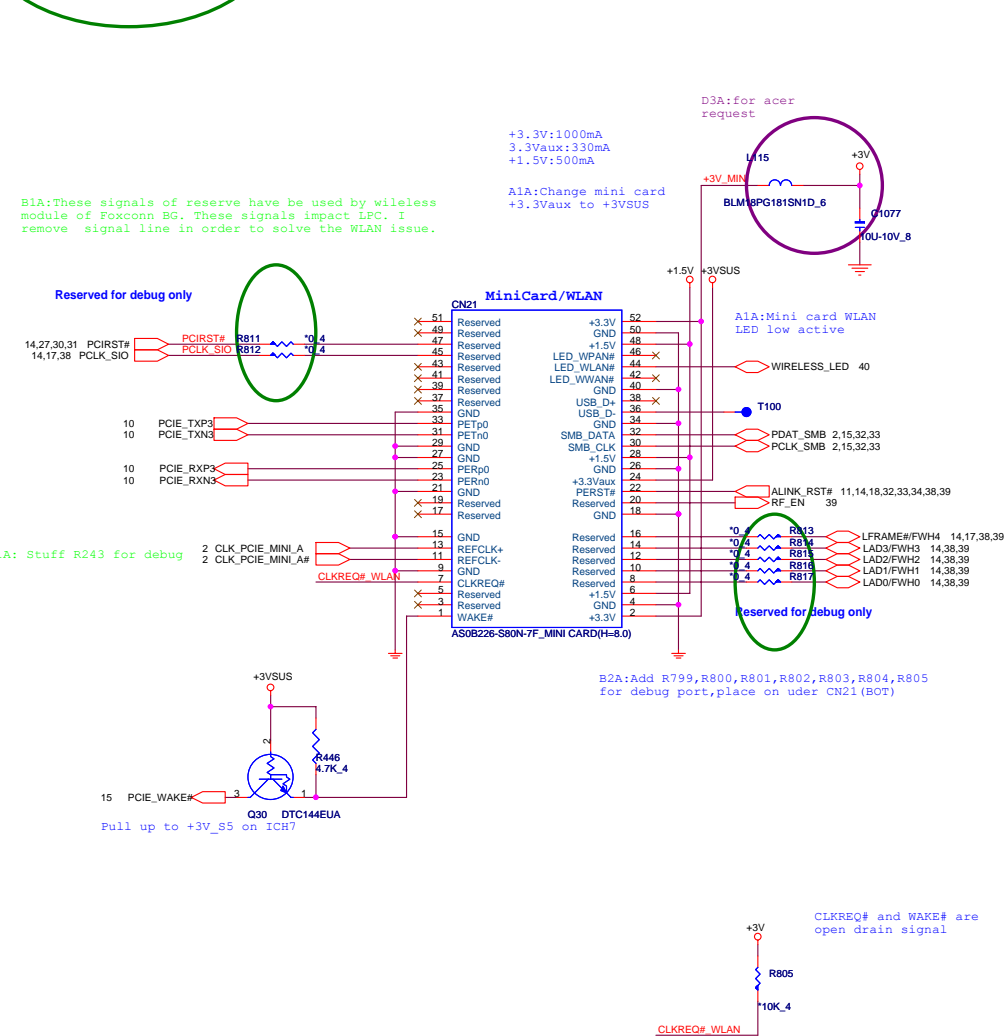
Size	Document Number	Rev
	<b>TRANSFORMER/RJ45</b>	1A
Date:	Thursday, June 08, 2006	Sheet 28 of 46

### Debug card interface

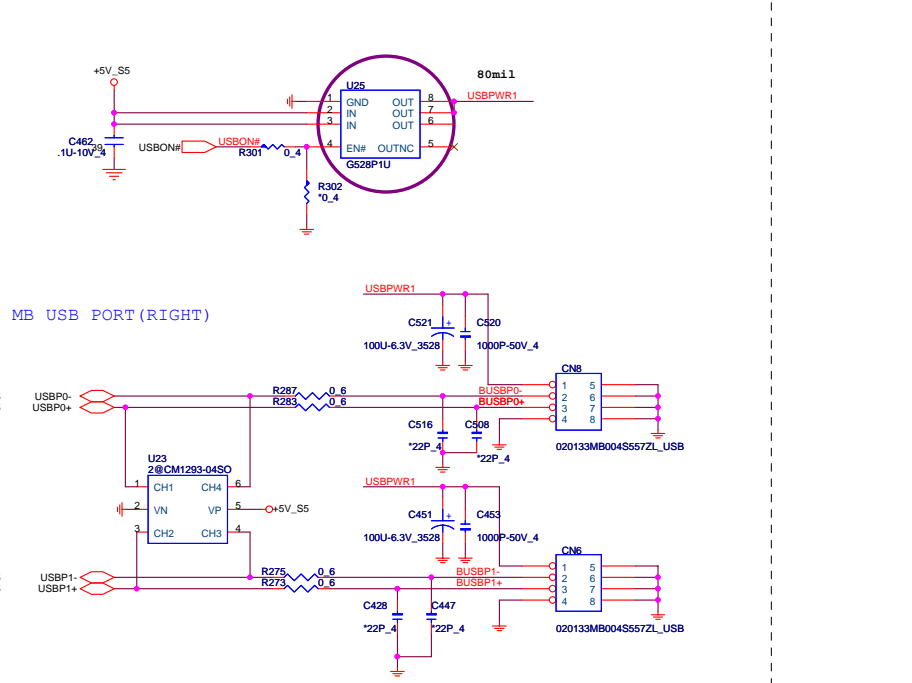
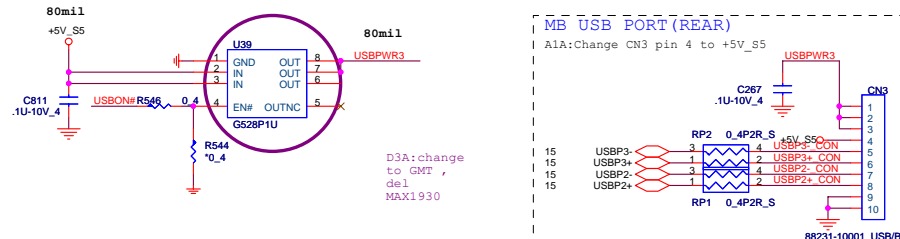
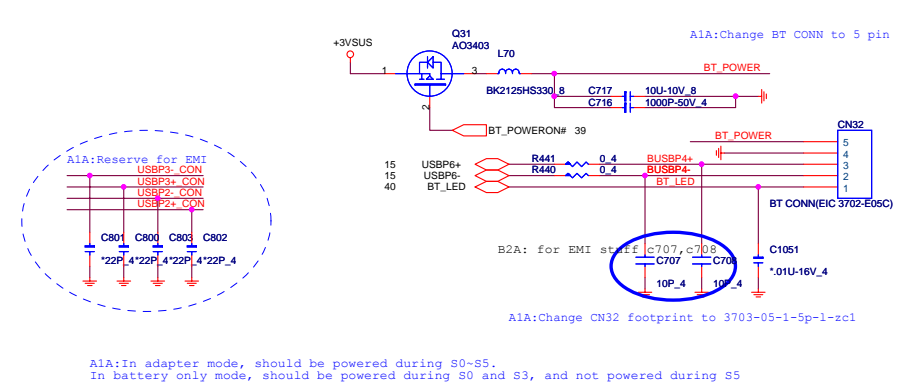


C3A: remove PCI debug conn

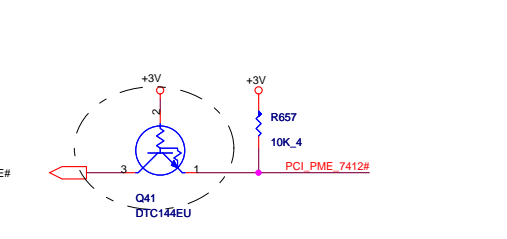
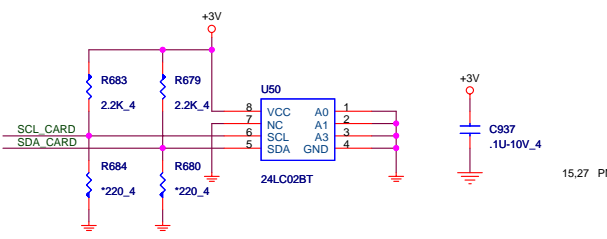
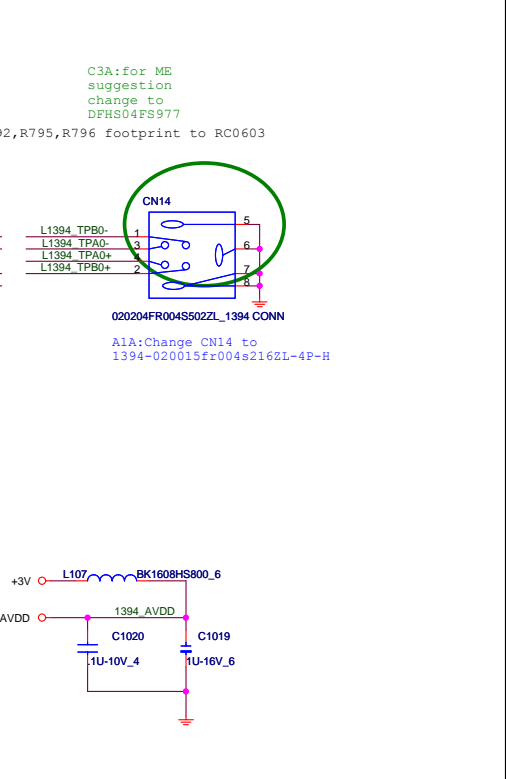
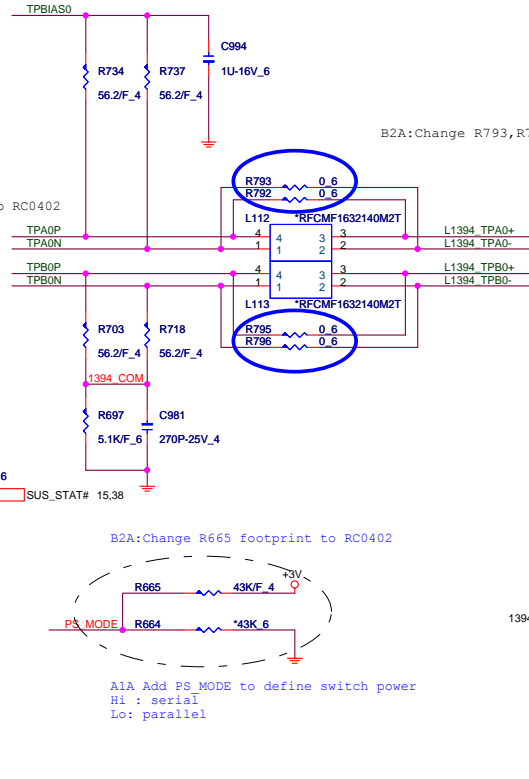
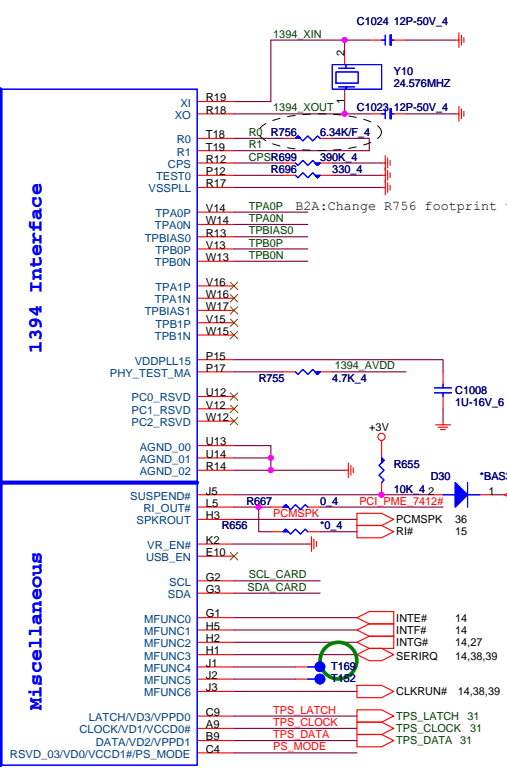
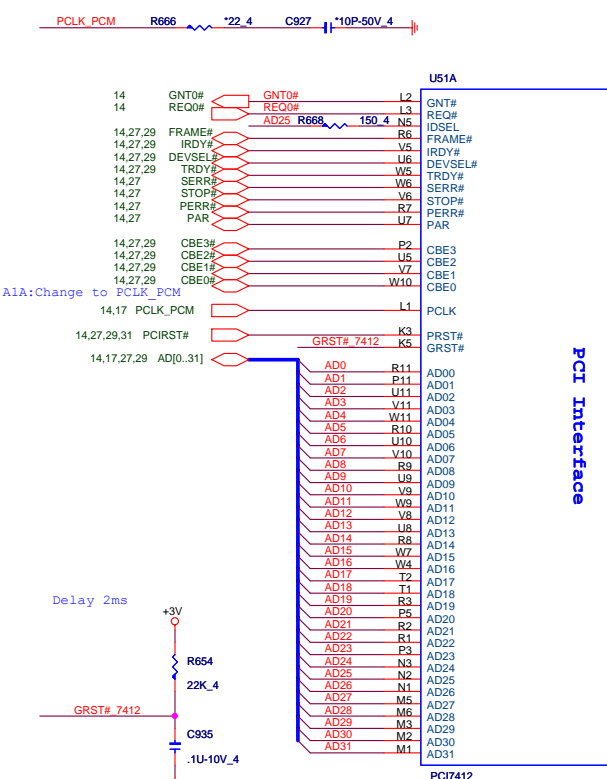
\*AF#800-N2G12\_DEBUG

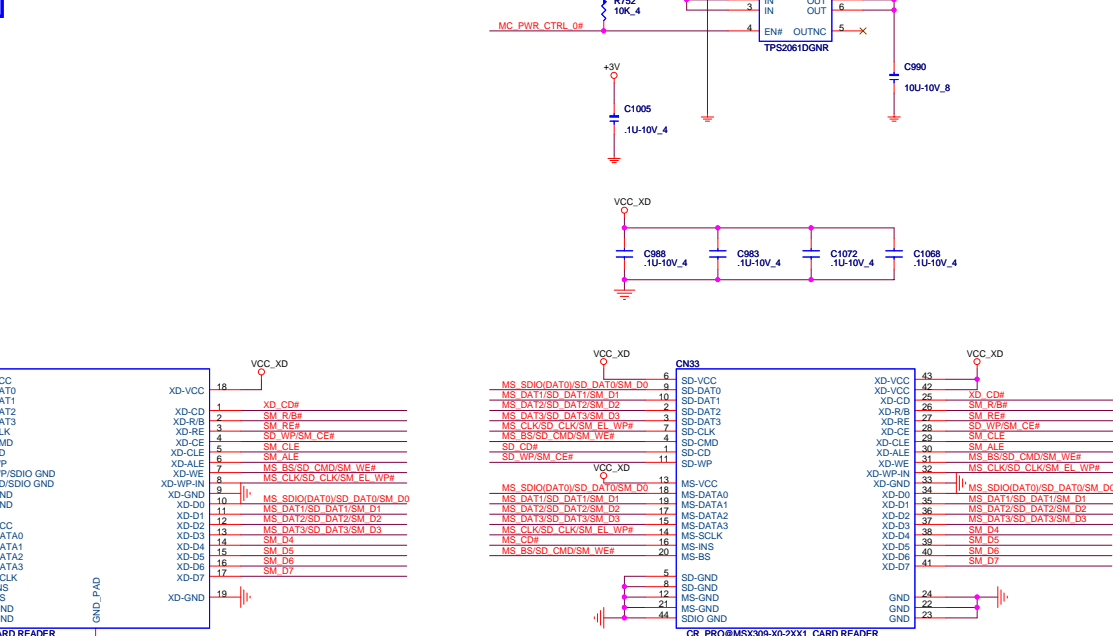
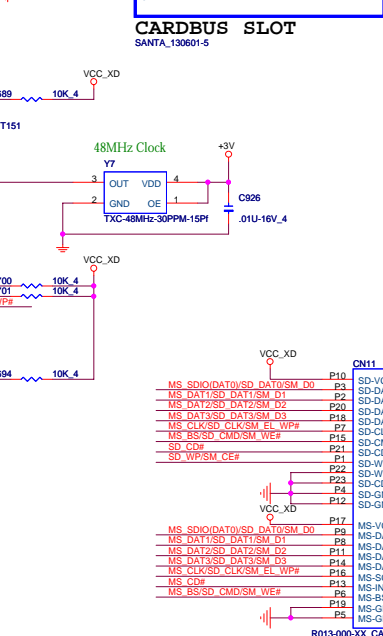
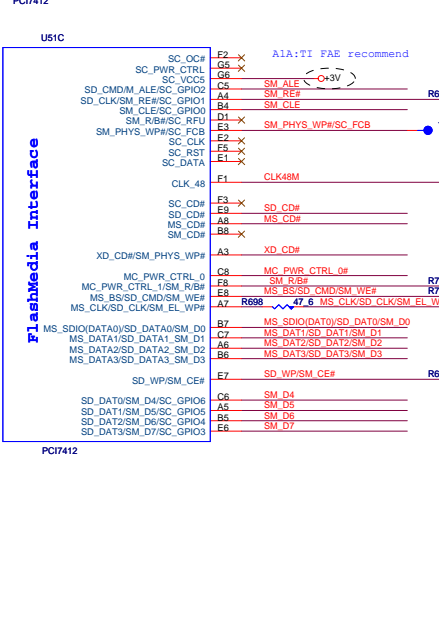
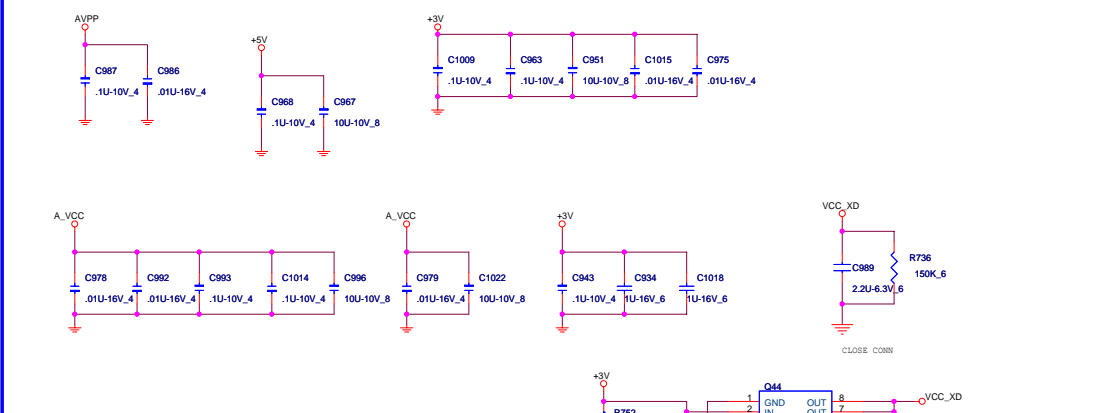
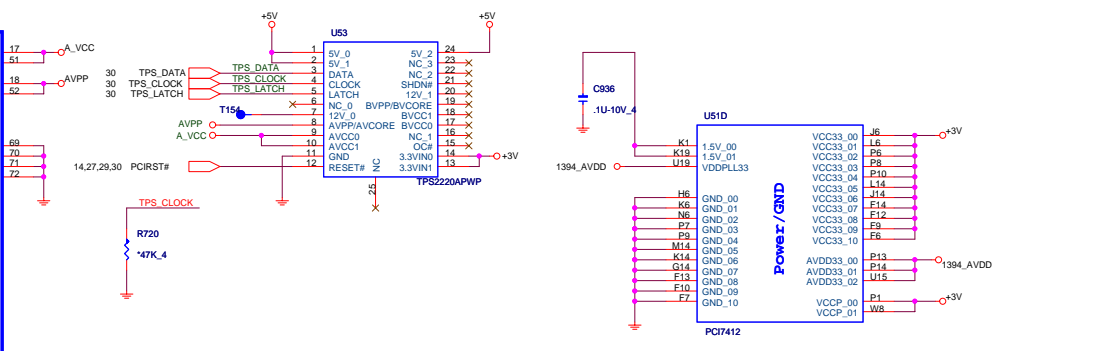
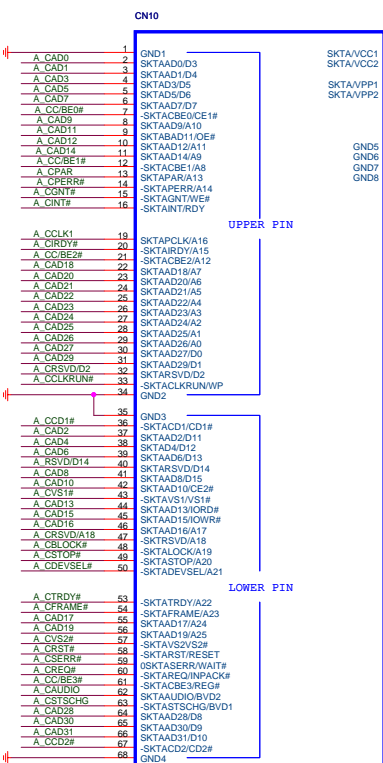
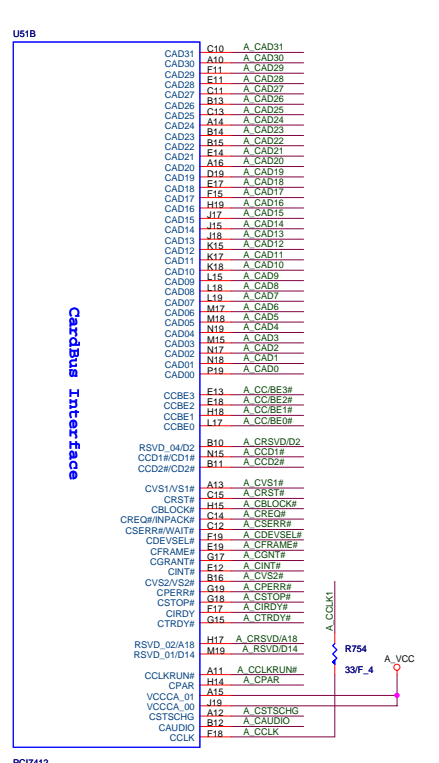


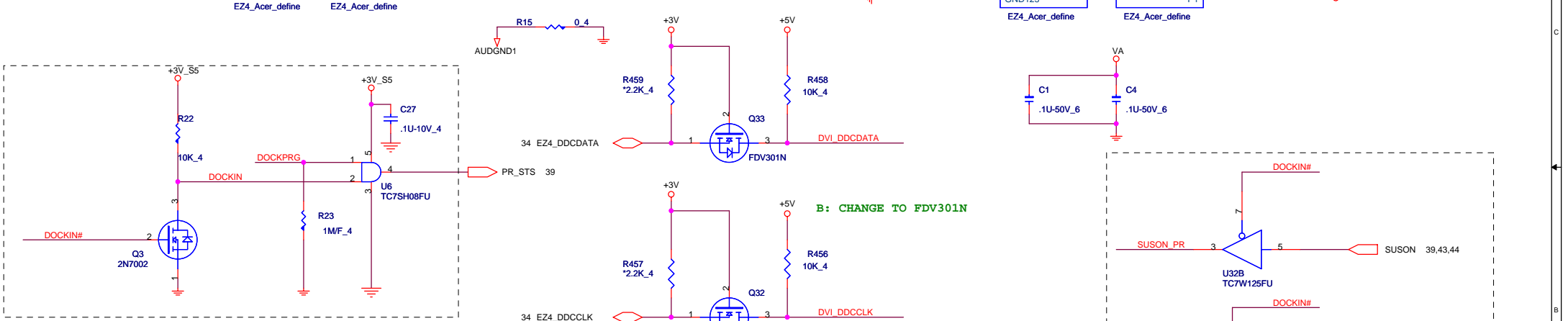
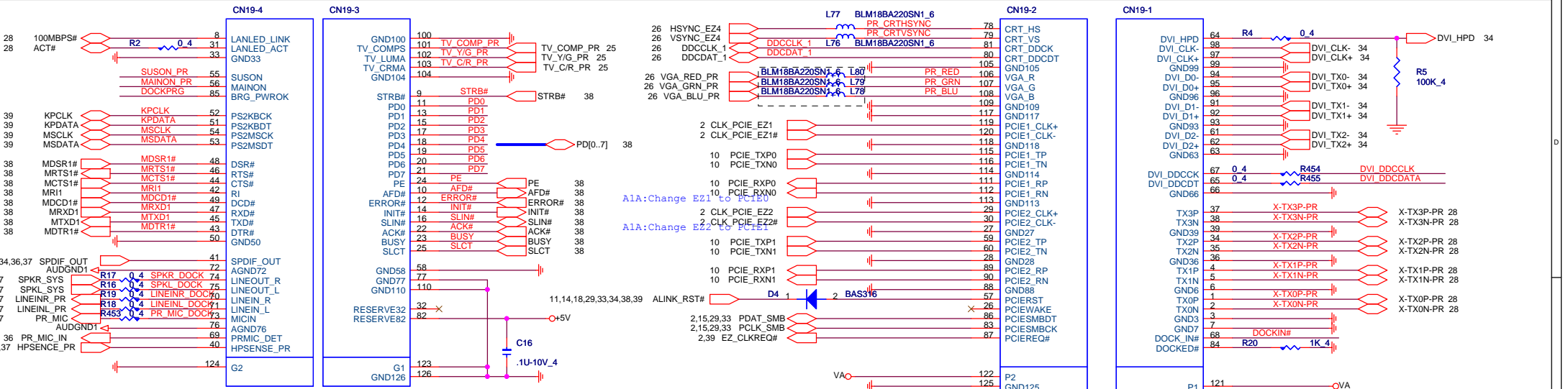
### BLUETOOTH MODULE CONNECTOR





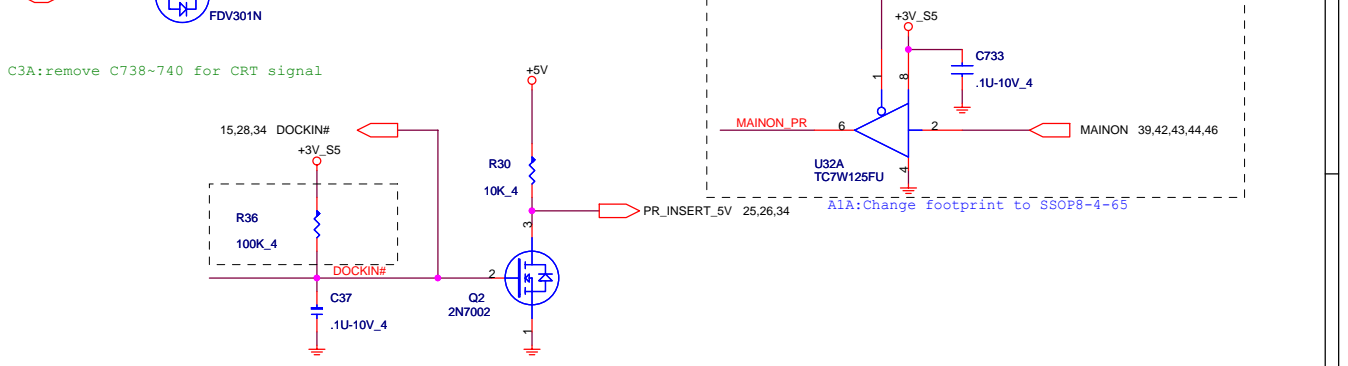






A1A: Reserve 100ps for KPCLK, KPDATA, MScLK, MsDATA

KPCLK	C731	*100P-50V_6	PR_CRTHSYNC	C737	*10P_4
KPDATA	C732	*100P-50V_6	PR_CRTVSYNC	C735	*10P_4
MScLK	C728	*100P-50V_6	PR_BLU	C738	*10P-50V_4
MsDATA	C730	*100P-50V_6	PR_GRN	C739	*10P-50V_4
SPDIF_OUT	C728	*100P-50V_6	PR_RED	C740	*10P-50V_4
SPKL_SYS	C17	220P-50V_4	HSYNC_EZ4	C736	*10P_4
SPKR_SYS	C18	220P-50V_4	VSynch_EZ4	C734	*10P_4
LINEINL_PR	C19	220P-50V_4	DDCCLK_1	C14	10P-50V_4
LINEINR_PR	C20	220P-50V_4	DDCCDAT_1	C15	10P-50V_4
PR_MIC_IN	C722	47P-50V_4	X-TX1P-PR	C6	*10P-50V_4
PR_MIC	C721	47P-50V_4	X-TX1N-PR	C5	*10P-50V_4
100MBPS#	C723	1000P-50V_4	X-TX2P-PR	C2	*10P-50V_4
ACT#	C11	1000P-50V_4	X-TX2N-PR	C3	*10P-50V_4
TV_COMP_PR	C743	10P-50V_4	X-TX3P-PR	C725	*10P-50V_4
TV_C/R_PR	C741	10P-50V_4	X-TX3N-PR	C724	*10P-50V_4
TV_Y/G_PR	C742	10P-50V_4	X-TX2P-PR	C727	*10P-50V_4
			X-TX2N-PR	C726	*10P-50V_4



**PROJECT : ZC3**  
**Quanta Computer Inc.**

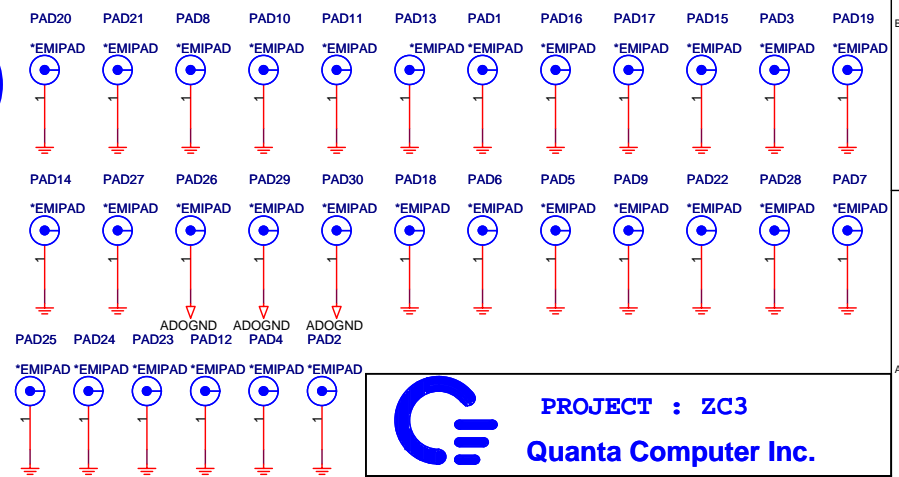
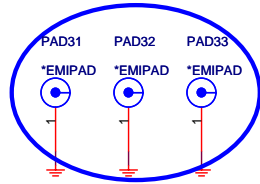
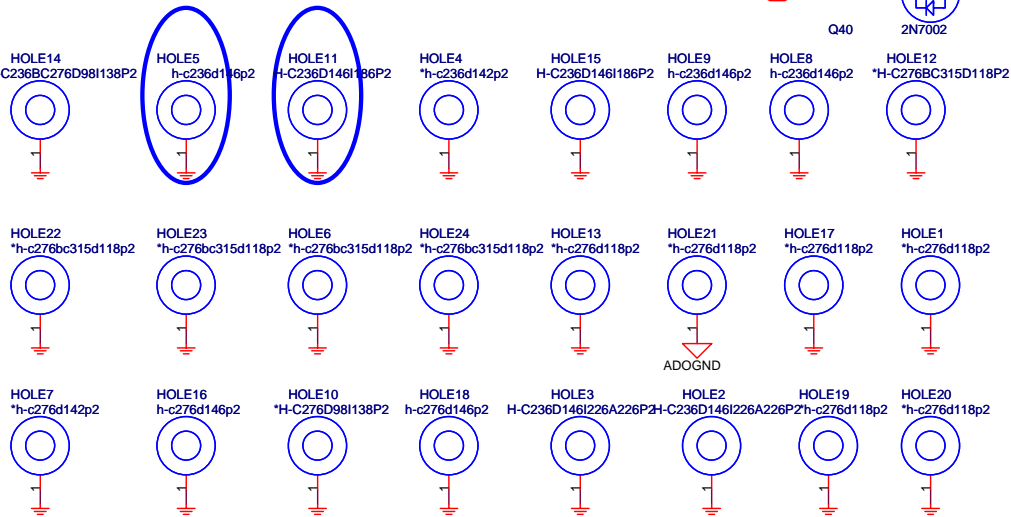
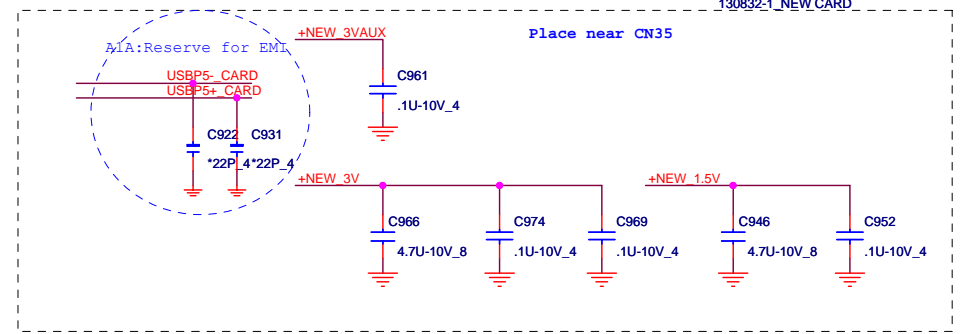
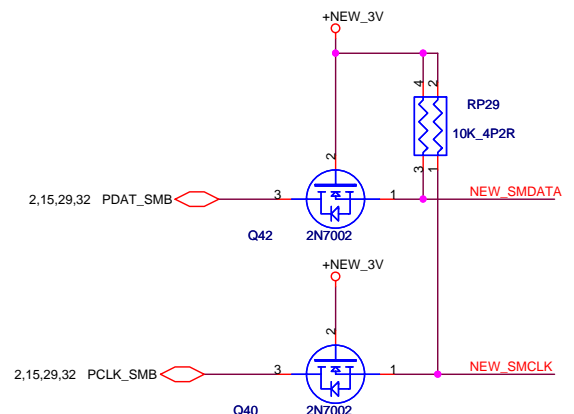
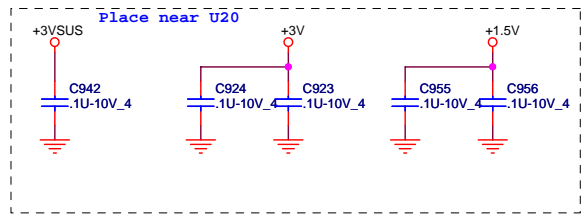
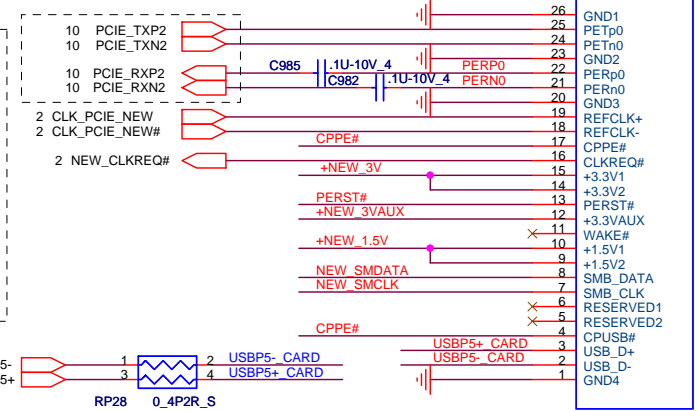
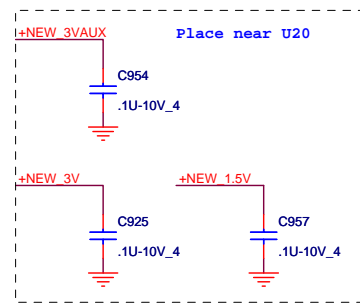
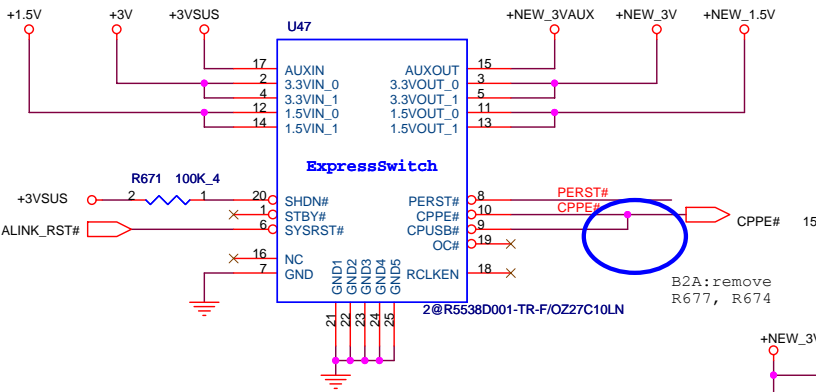
Size	Document Number	Rev
	<b>EZ4 CONN</b>	1A

Date: Thursday, June 08, 2006 Sheet 32 of 46

+NEW\_1.5V Max. 650mA, Average 500mA.  
 +NEW\_3V Max. 1300mA, Average 1000mA.

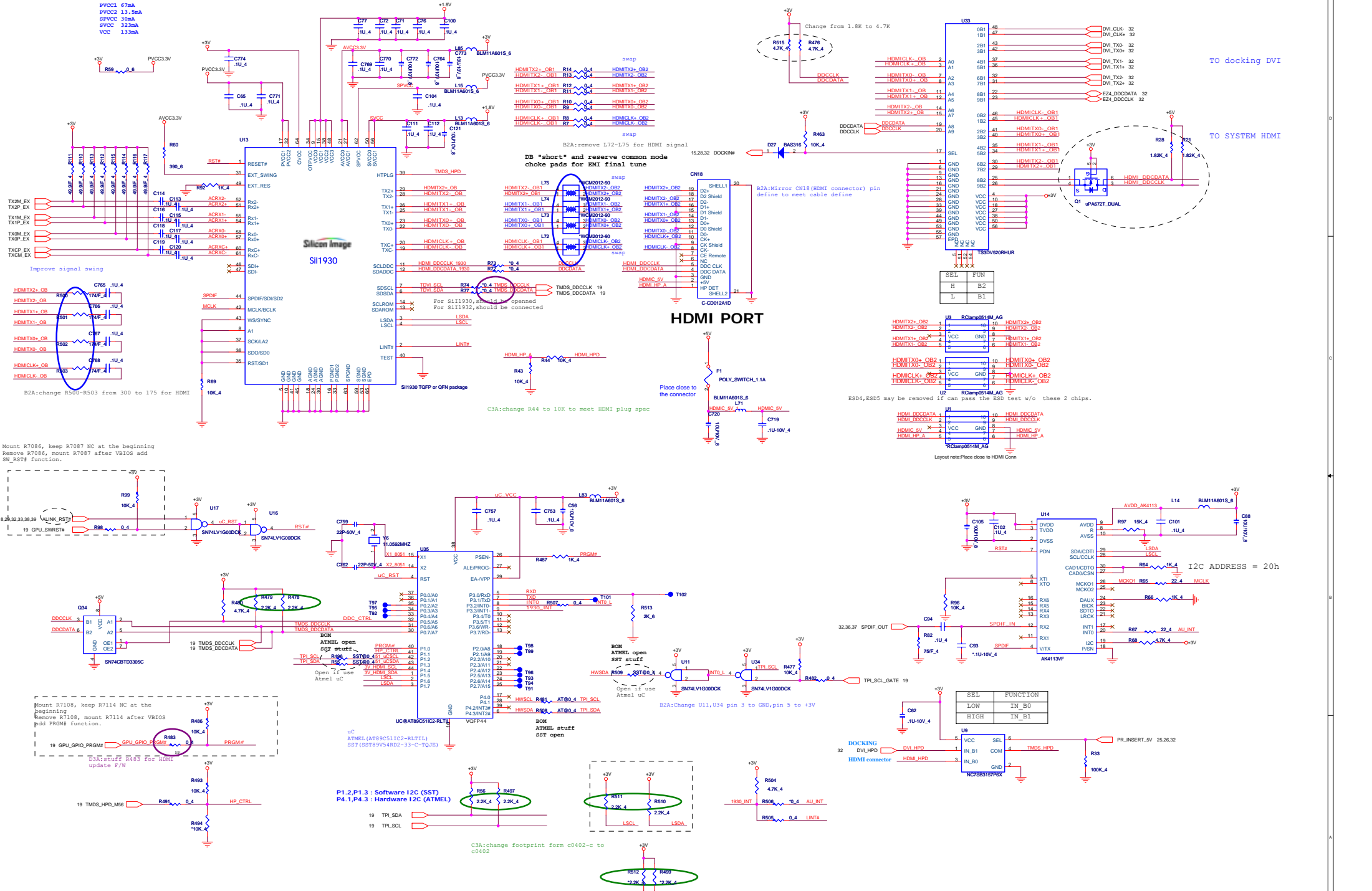
A1A:Change New card to small type(130832-1)  
 Reverse

A1A:Change New card power sw to Oz27c10



**PROJECT : ZC3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>NEW CARD &amp; HOLE</b>	1A
Date:	Thursday, June 08, 2006	Sheet 33 of 46



PVCC1 67mA  
 PVCC2 13.5mA  
 SPVCC 30mA  
 SVCC 32.3mA  
 VCC 133mA

Change from 1.8K to 4.7K

TO docking DVI

TO SYSTEM HDMI

### HDMI PORT

SEL	FUN
H	B.2
L	B.1

Layout note: Place close to HDMI Conn

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

Mount R7086, keep R7087 NC at the beginning  
 Remove R7086, mount R7087 after VB108 add SW\_RST# function.

Mount R7108, keep R7114 NC at the beginning  
 Remove R7108, mount R7114 after VB108 add PRGM# function.

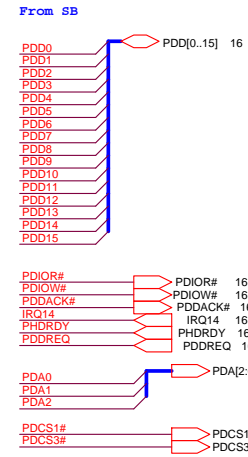
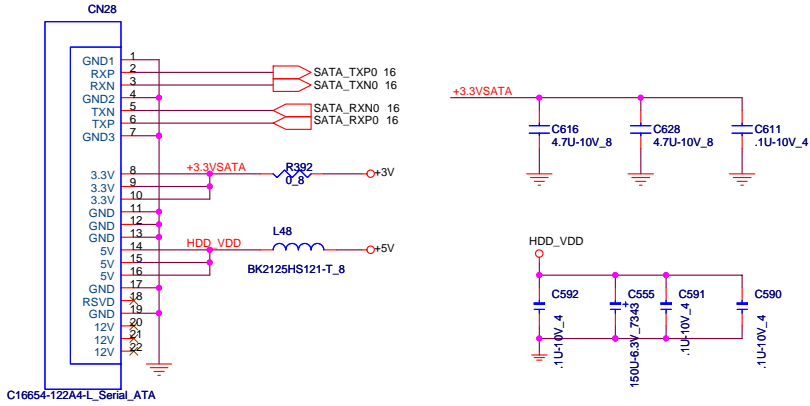
B3A:stuff R483 For HDMI update F/W

P1.2,P1.3 : Software I2C (SST)  
 P4.1,P4.3 : Hardware I2C (ATMEL)

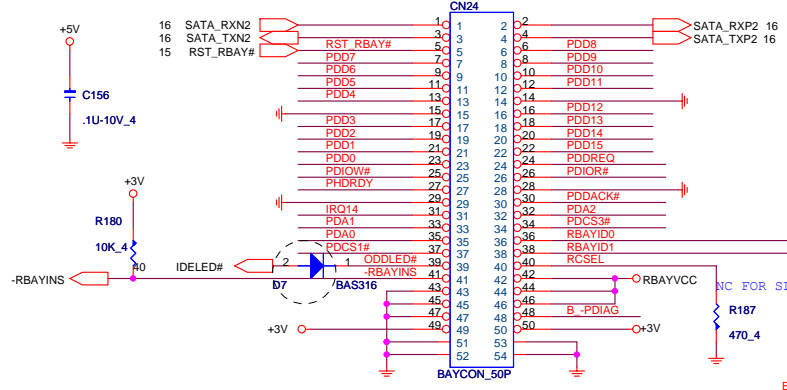
C3A:change footprint form c0402-c to c0402

HDMI\_SDA & HDMI\_SCL capacitance MUST less than 50PF

# SATA HDD

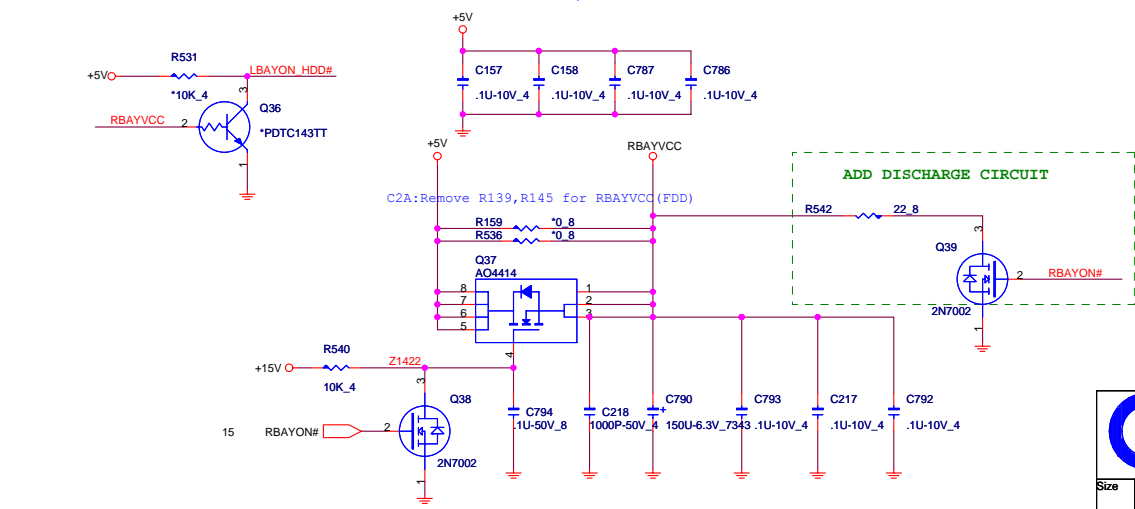
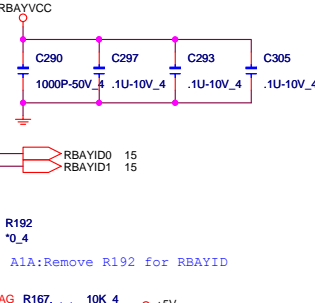


## Media Bay Connector



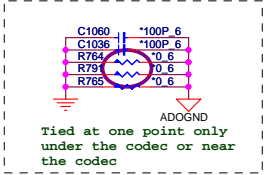
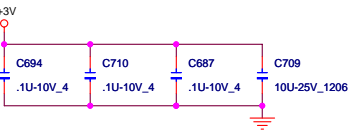
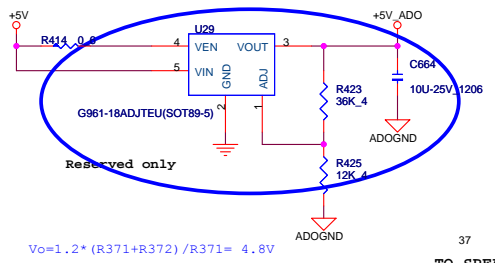
## BAY ID STATUS

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD



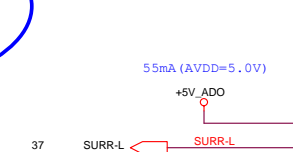
B2A: for audio noise  
 del  
 L55,C657,C661,C1063,C675,C679,C1064  
 stuff U29,R414,R423,R425,C664

Option of External Volume  
 Control or Standby  
 Mode/De-Pop

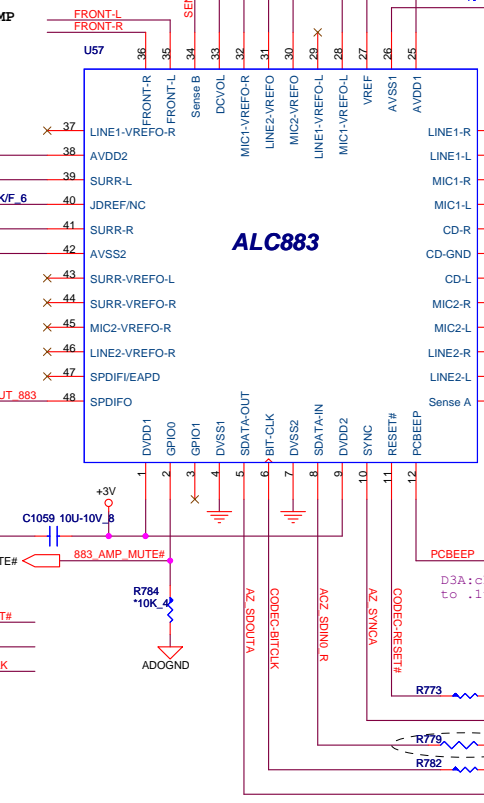
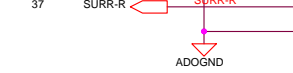


D3A:remove R791

TO Headphone AMP

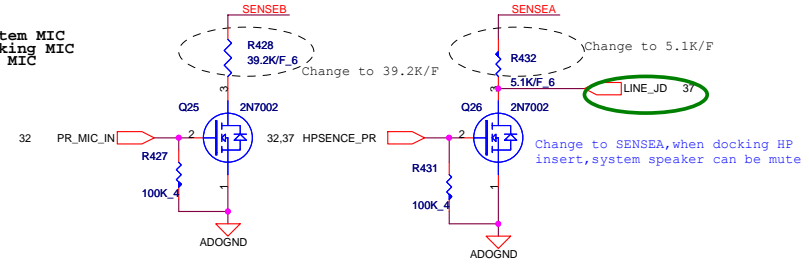
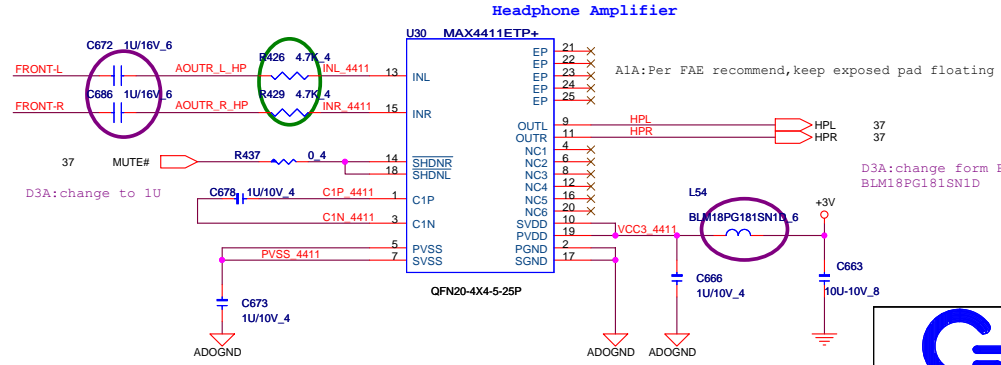
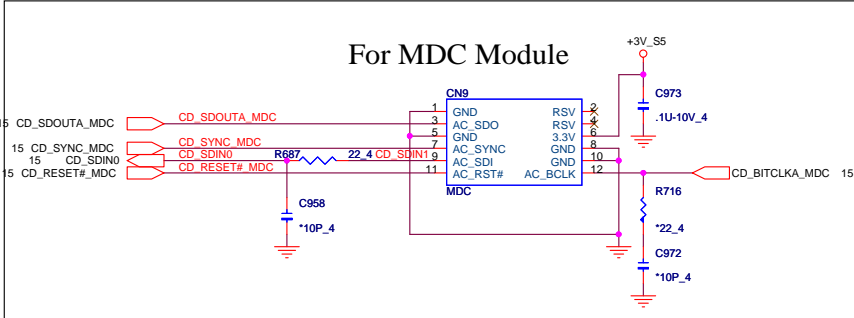


TO SPEAKER AMP



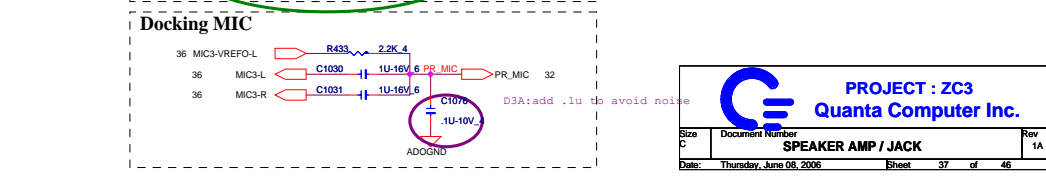
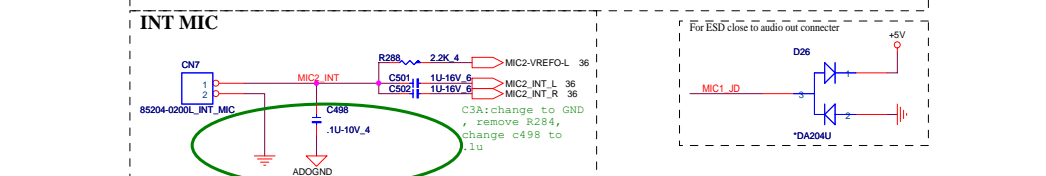
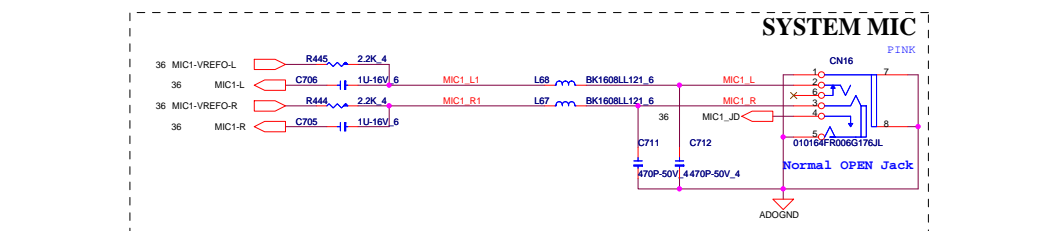
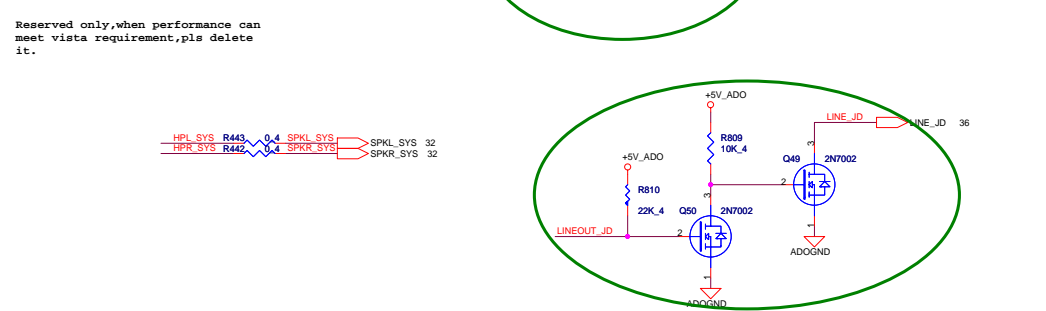
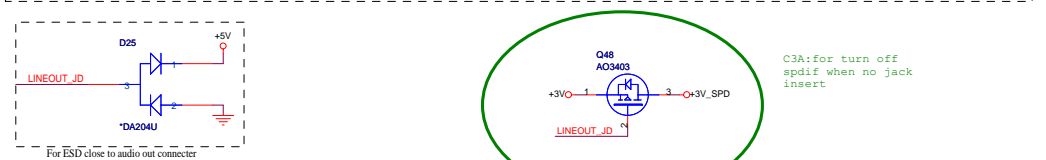
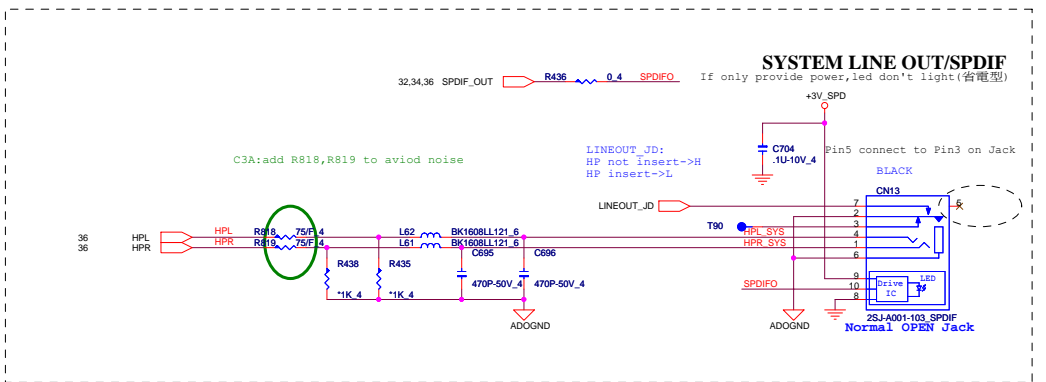
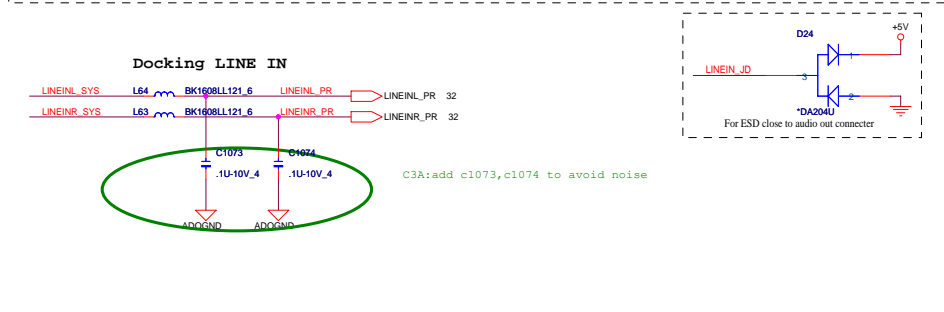
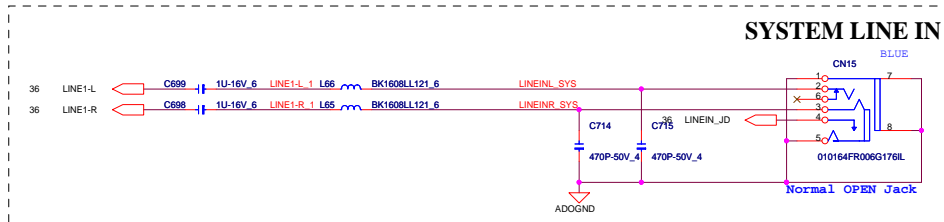
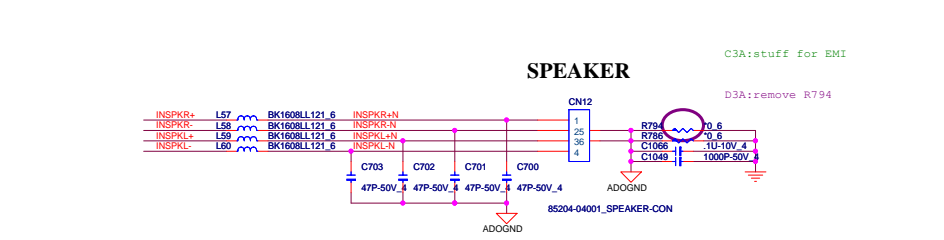
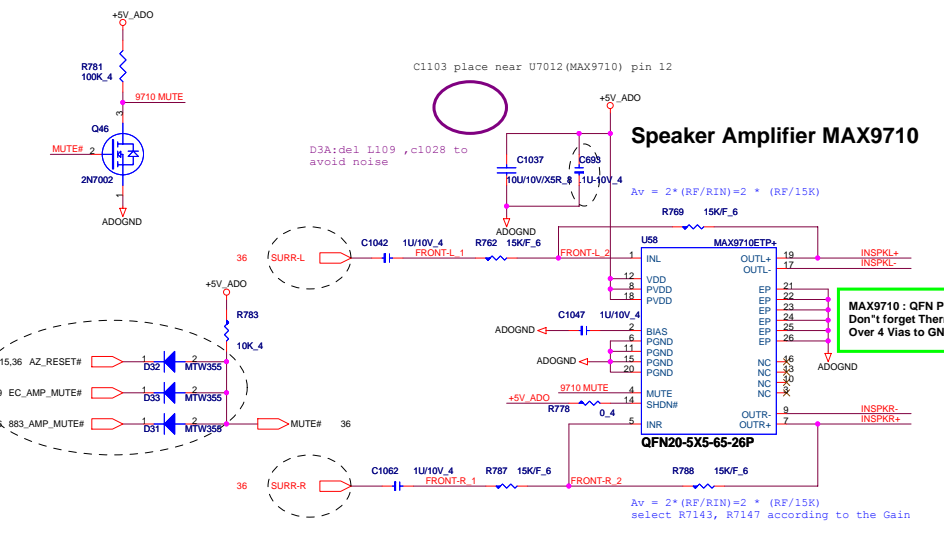
A1A:Change AZ\_SDIN1 series resistor from 33 to 22 ohm

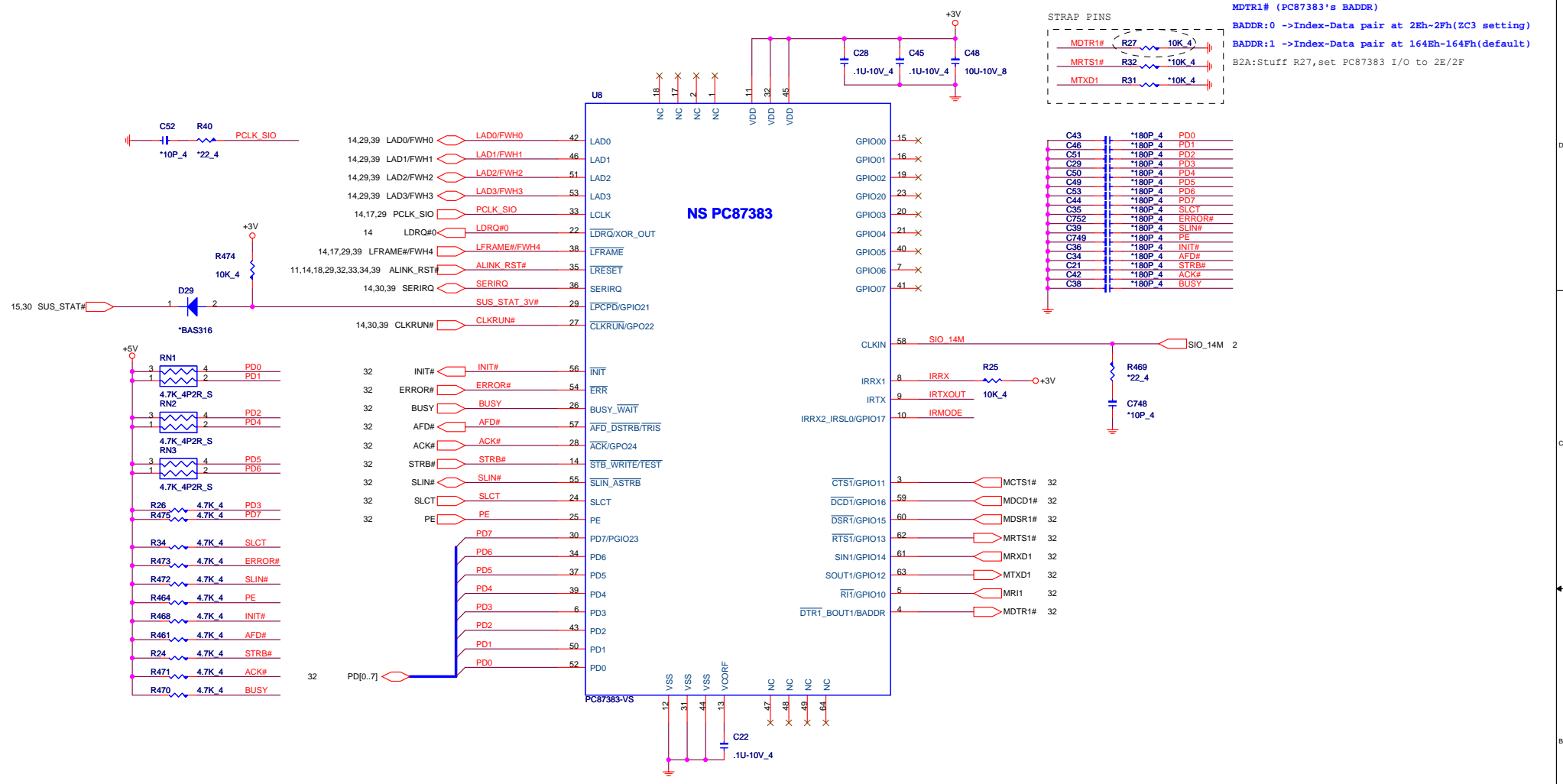
Change from 1uF to 4.7uF to meet vista performance requirement C3A:change 0 to 4.7k to avoid noise



- Sense A 5.1k 1% Front out (pin35.36)
- Sense A 10k 1% Line1 (pin23.24)
- Sense A 20k 1% Mic1 (pin21.22)
- Sense A 39.2k 1% Surr out (pin39.41)
- Sense B 5.1k 1% Side out (pin45.46)
- Sense B 10k 1% Cen/Lfe out (pin43.44)
- Sense B 20k 1% Mic2 (pin16.17)
- Sense B 39.2k 1% Line2 (pin14.15)





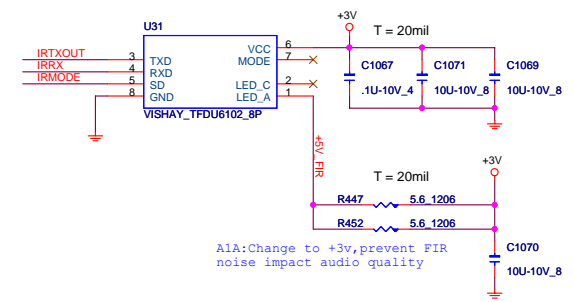


MDTR1# (PC87383's BADDR)  
 BADDR:0 ->Index-Data pair at 2Eh-2Fh(ZC3 setting)  
 BADDR:1 ->Index-Data pair at 164Eh-164Fh(default)  
 B2A: Stuff R27, set PC87383 I/O to 2E/2F

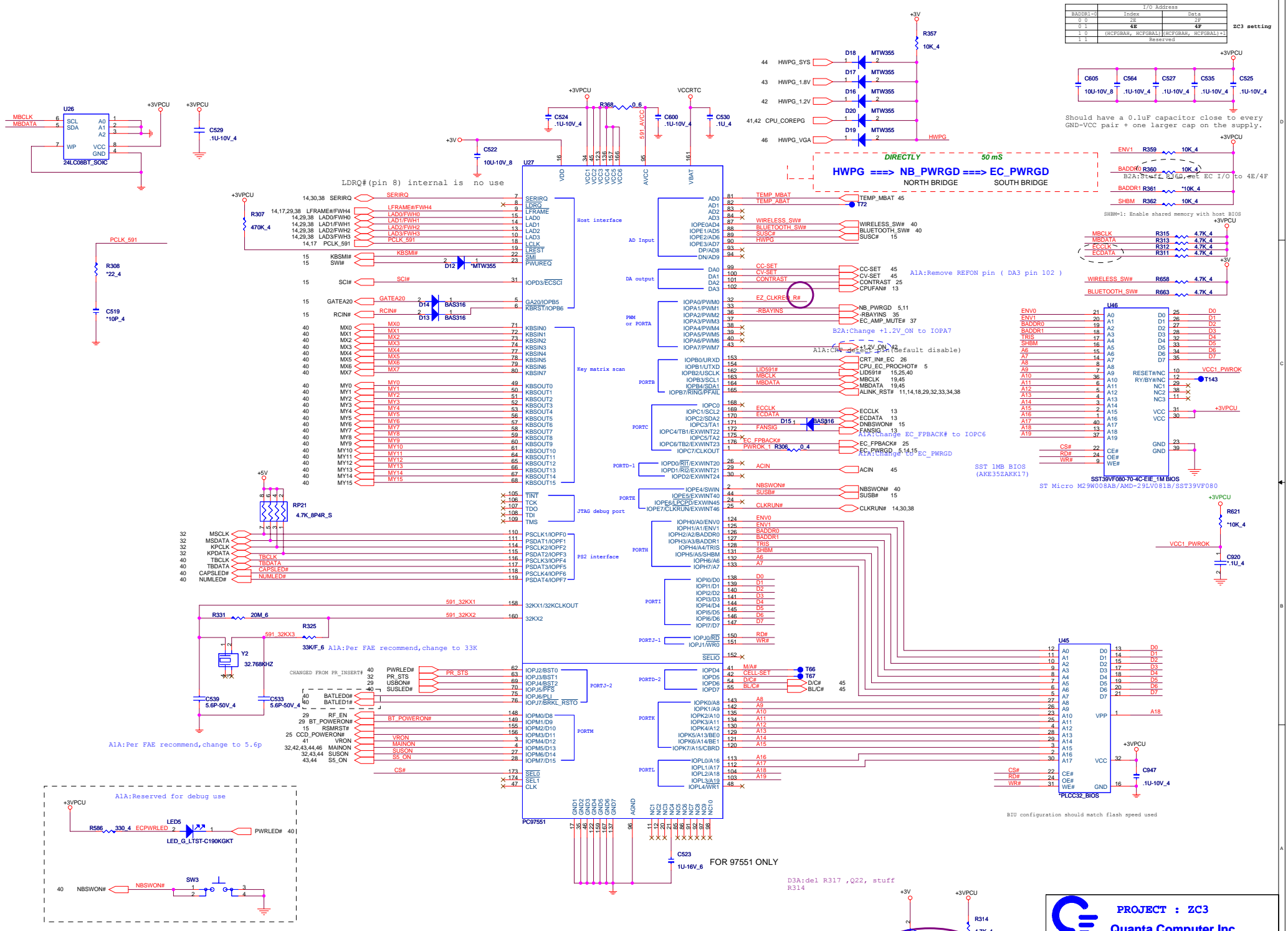
STRAP PINS

- MDTR1# R27 \*10K\_4
- MRTS1# R32 \*10K\_4
- MTXD1 R31 \*10K\_4

### FIR

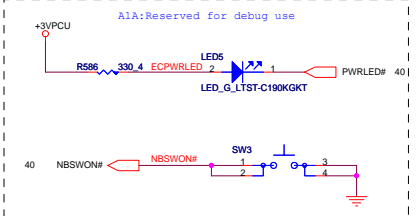
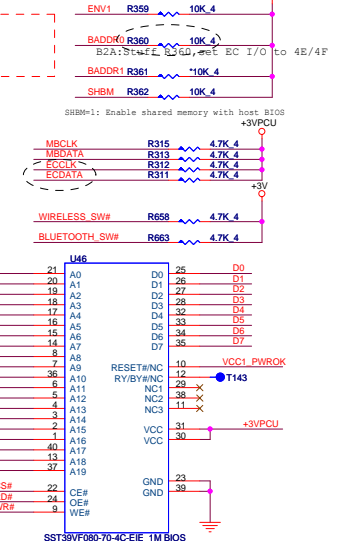


I/O Address		
BADDR1-0	Index	Data
0	2E	2F
0	4E	4F
1	(HCFG0BAR, HCFG0BAL)	(HCFG0BAR, HCFG0BAL)+1
1		Reserved



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

**DIRECTLY** 50mS  
HWPG ==> NB\_PWRGD ==> EC\_PWRGD  
NORTH BRIDGE SOUTH BRIDGE



A1A:Per FAE recommend,change to 5.6p

A1A:Per FAE recommend,change to 33k

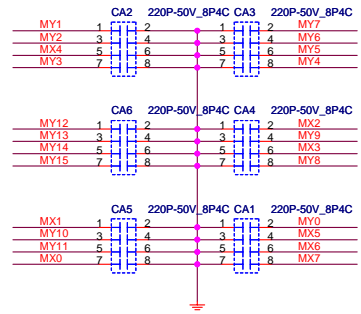
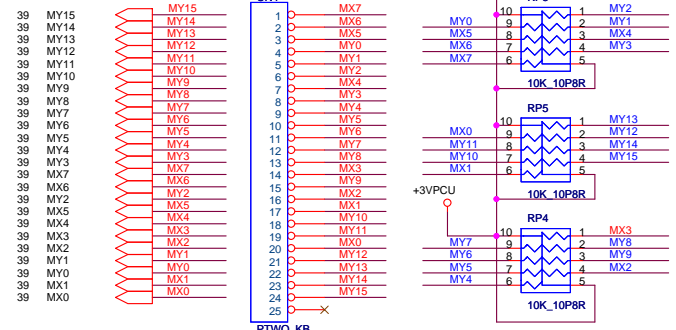
A1A:Reserved for debug use

**PROJECT : ZC3**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>97551 &amp; FLASH</b>	1A

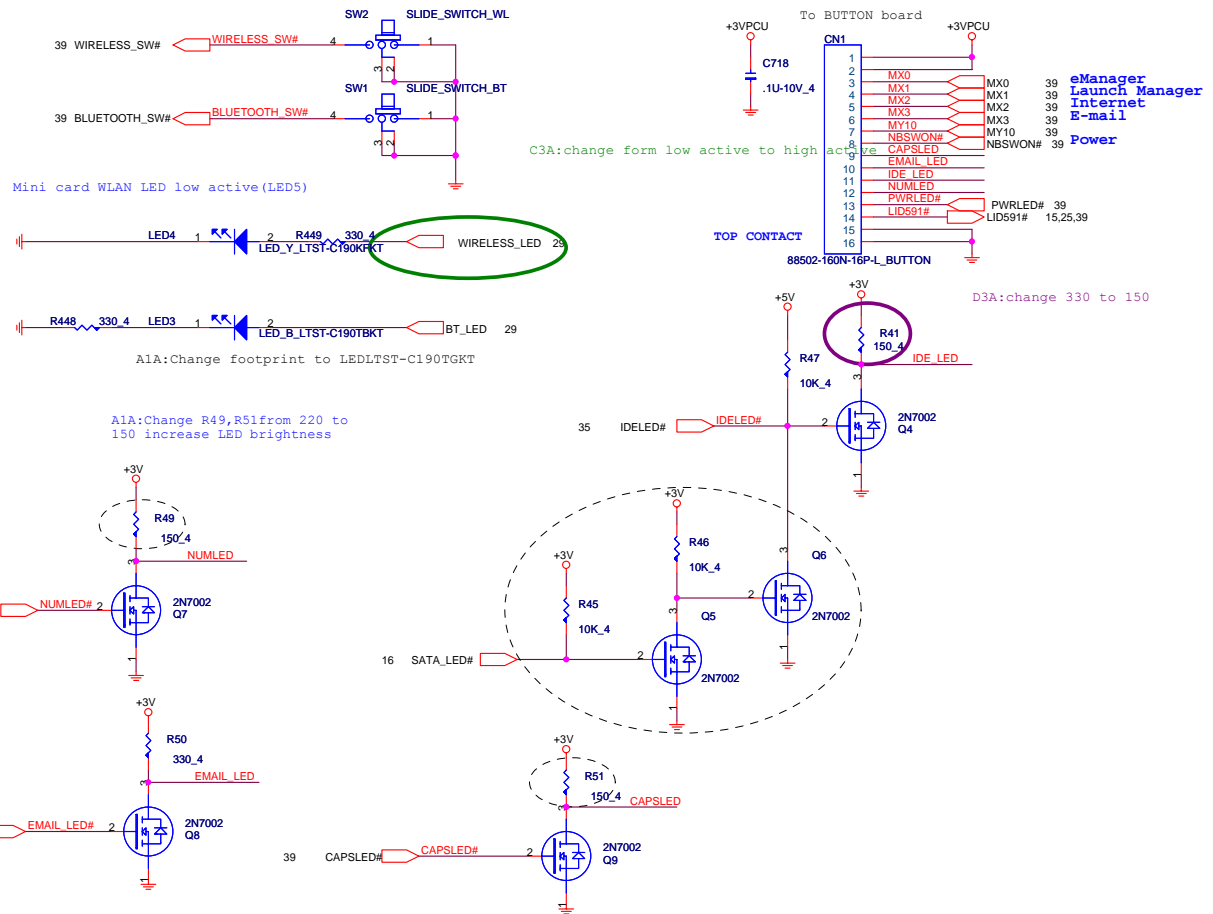
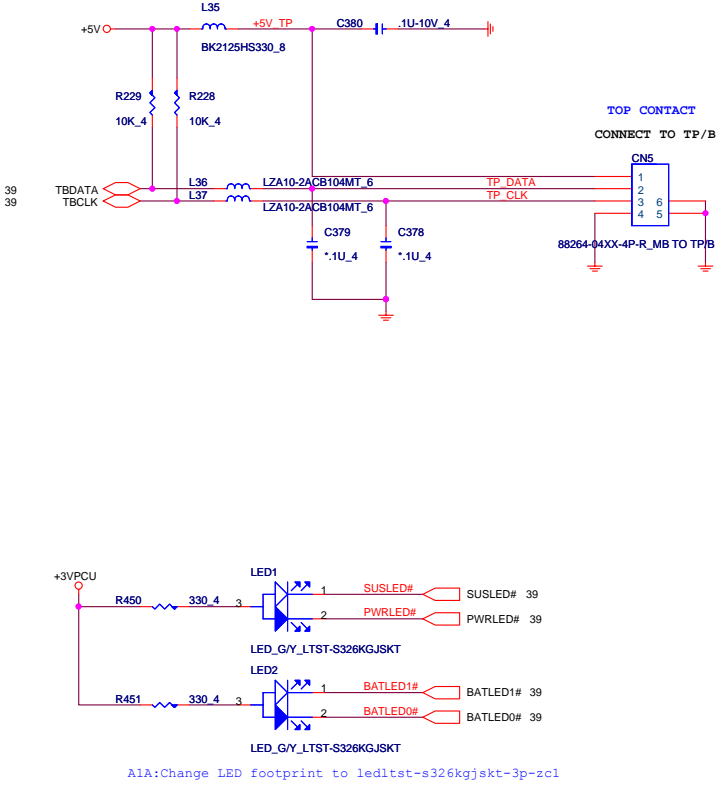
Date: Thursday, June 08, 2006 Sheet 39 of 46

INTERNAL PULLUP IN SB  
5.2K EZ\_CLKREQ#



TOUCH PAD

20 MIL



B2A: Stuff PR40 for CPU PWRGD

39,42 CPU\_COREPG

5 VID0 D0 PR79 0.6 31 D0

5 VID1 D1 PR74 0.6 32 D1

5 VID2 D2 PR72 0.6 33 D2

5 VID3 D3 PR70 0.6 34 D3

5 VID4 D4 PR68 0.6 35 D4

5 VID5 D5 PR66 0.6 36 D5

39 VRON PR63 0.4 38 SHDN

5 PSI# PR60 0.4 8774SKIP# 39 SKIP

VCC\_CORE PR42 20K/F\_6 PC27 470P\_50V\_4 9 CCI

PR48 71.5K/F\_6 8774TIME 6 TIME

PC28 470P\_50V\_4 8774CCV 8 CCV

PC26 22U/25V\_6 8774REF 10 REF

C3A: change form 169K to 301K

PR43 301K/F\_6 8774QPS 2 OFS

PSI# 2

+5VPCU PR56 100K/F\_4 VRHOT# 4 VRHOT

PR54 10K/F\_6 3 POUT

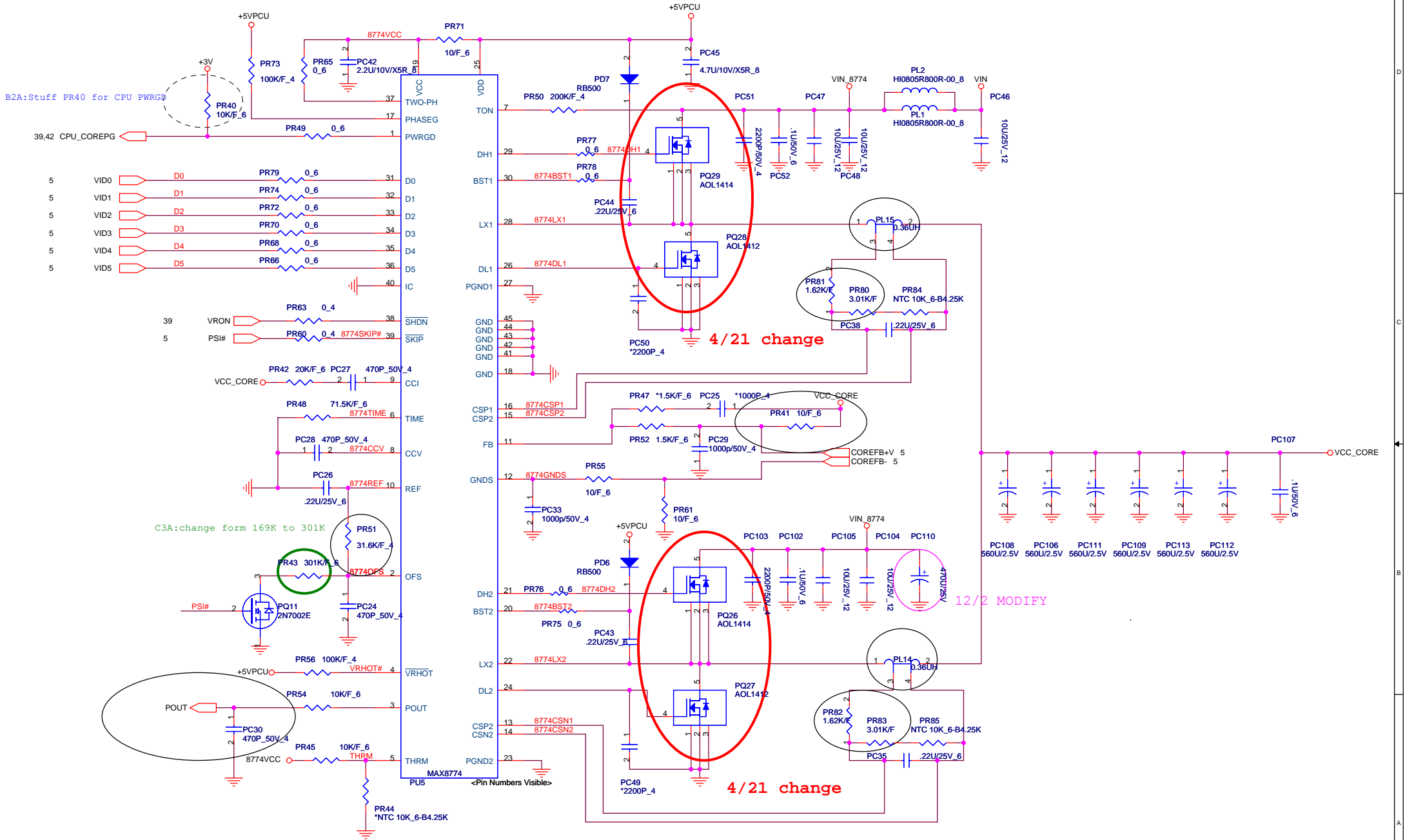
PC30 470P\_50V\_4


8774VCC PR45 10K/F\_6 THRM 5 THRM

PR44 NTC 10K\_6-B4.25K PUS

MAX8774

<Pin Numbers Visible>

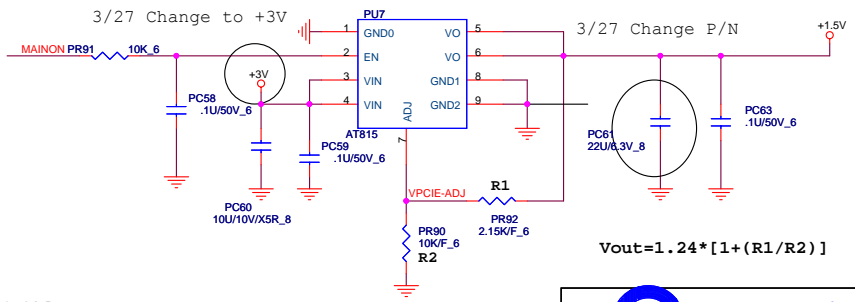
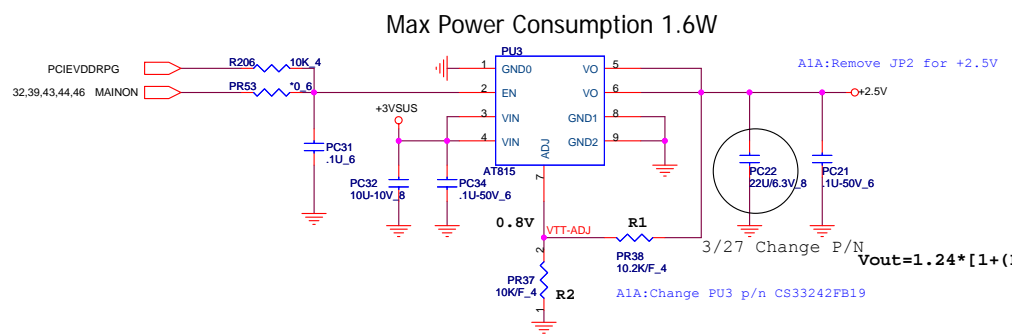
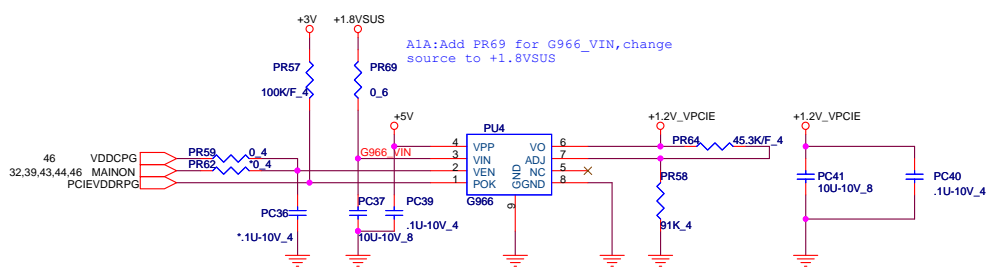
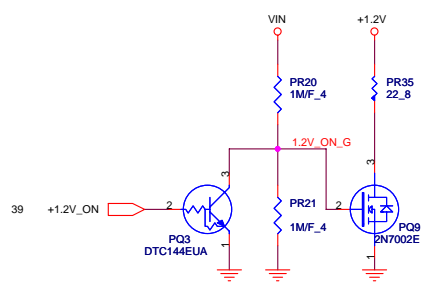
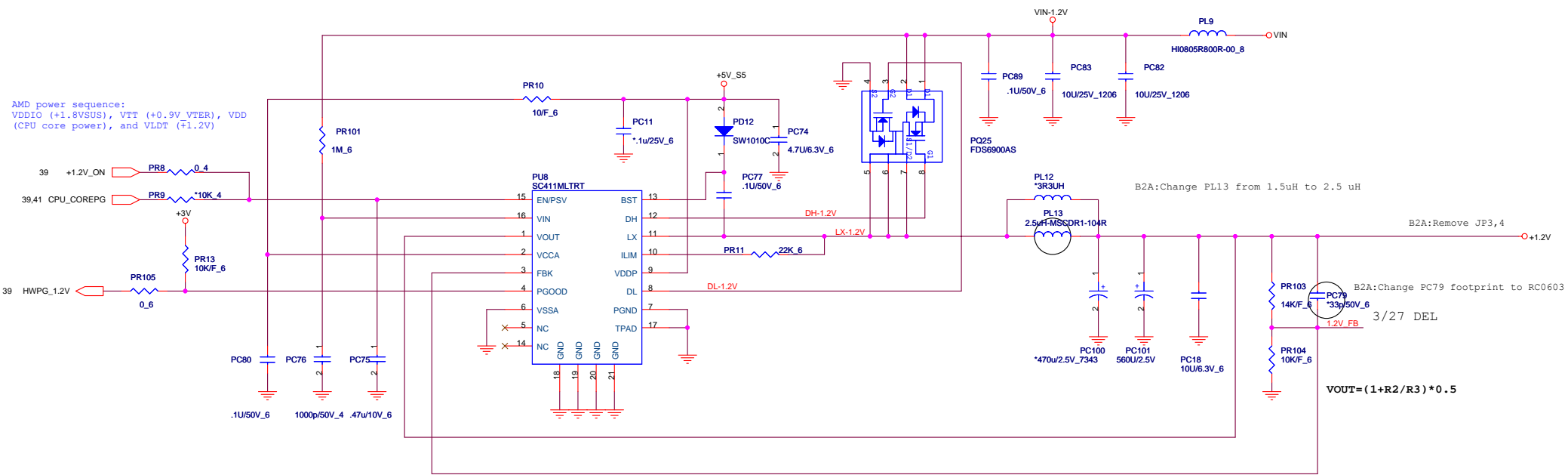




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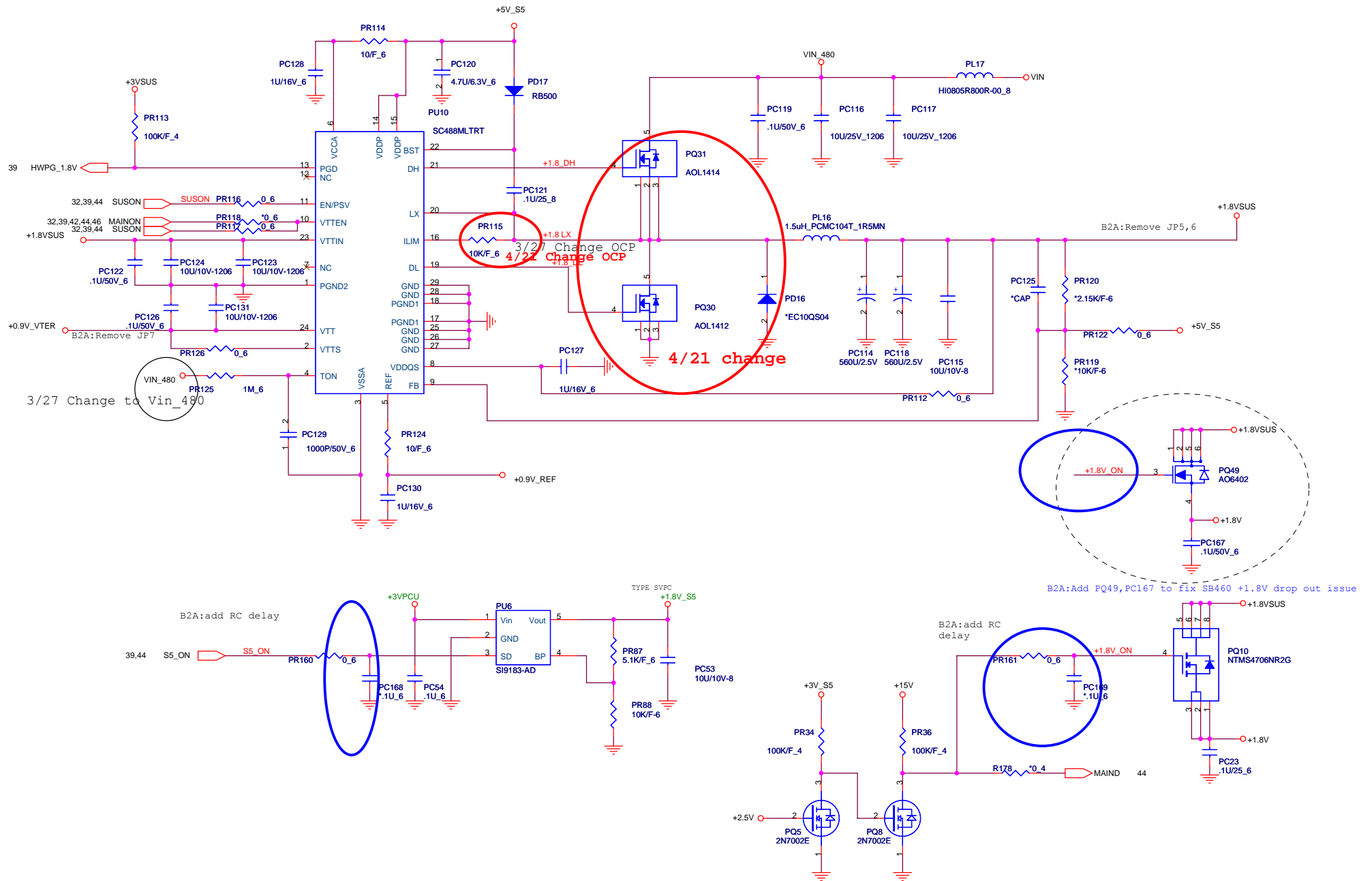
Size	Document Number	Rev
	<b>CPU CORE MAX8760</b>	1A
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AMD power sequence:  
 VDDIO (+1.8VSUS), VTT (+0.9V\_VTER), VDD  
 (CPU core power), and VLDT (+1.2V)

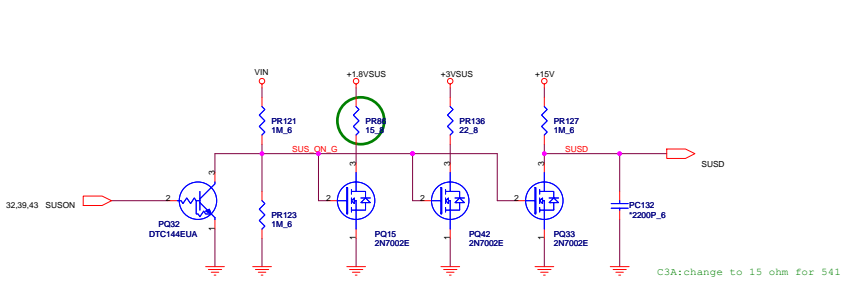
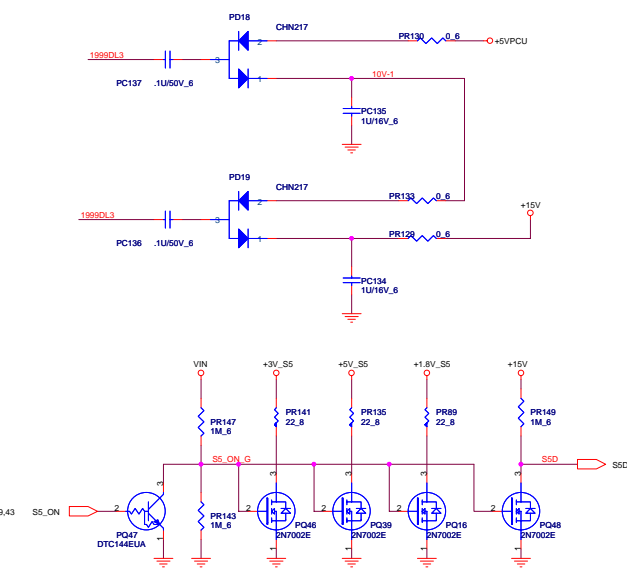
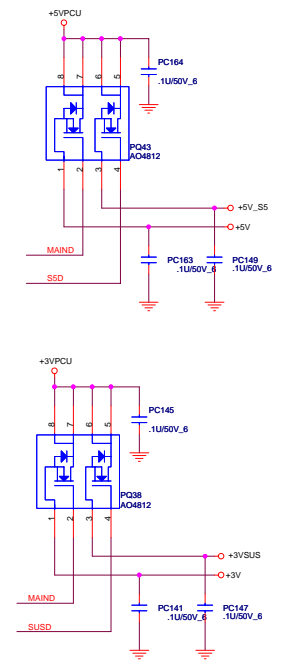
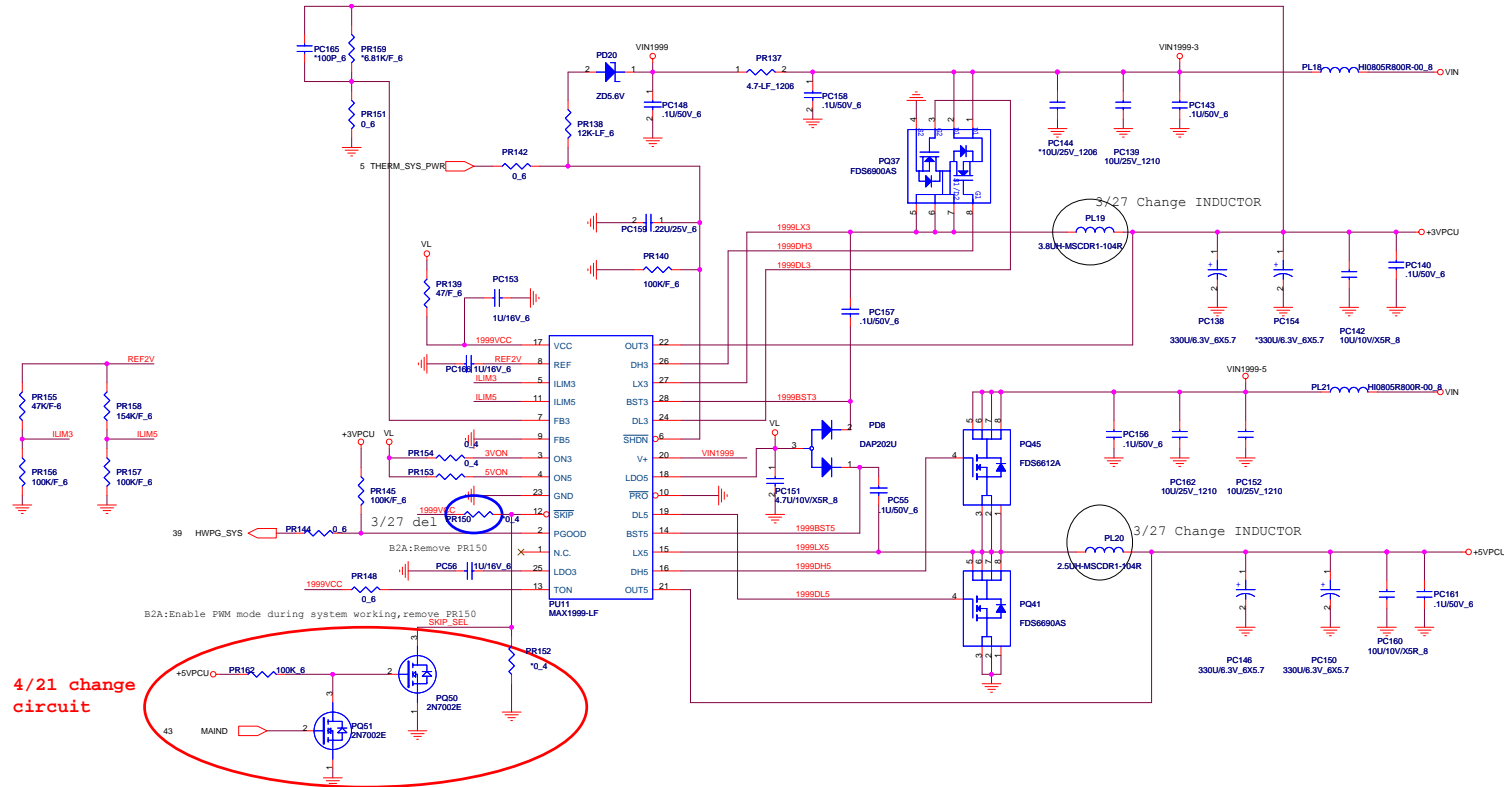


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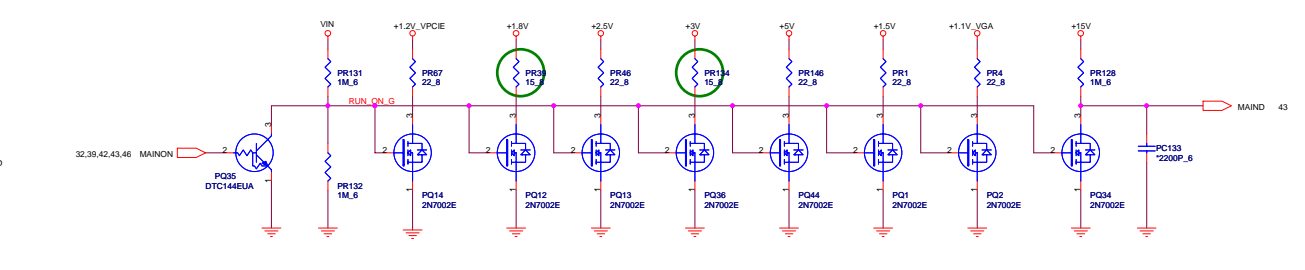
Size	Document Number	Rev
Custom	<b>+1.2V/+1.5V/+2.5V</b>	A1A
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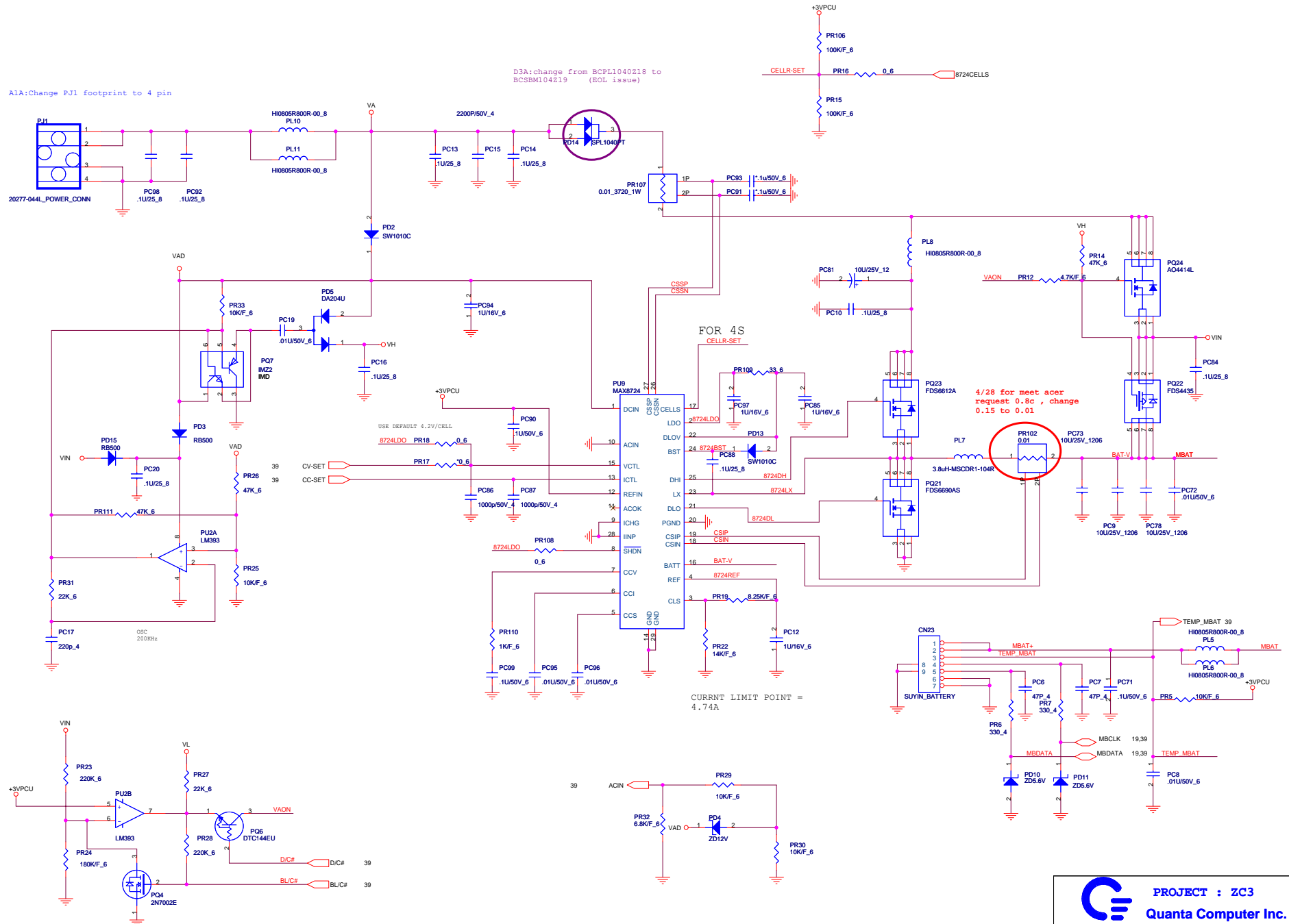


C3A: change to 15 ohm for 541



A1A:Change PJ1 footprint to 4 pin

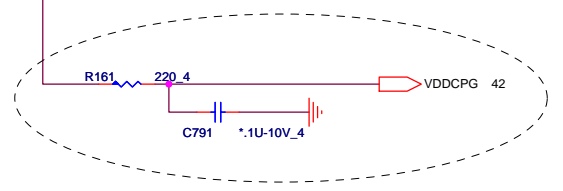
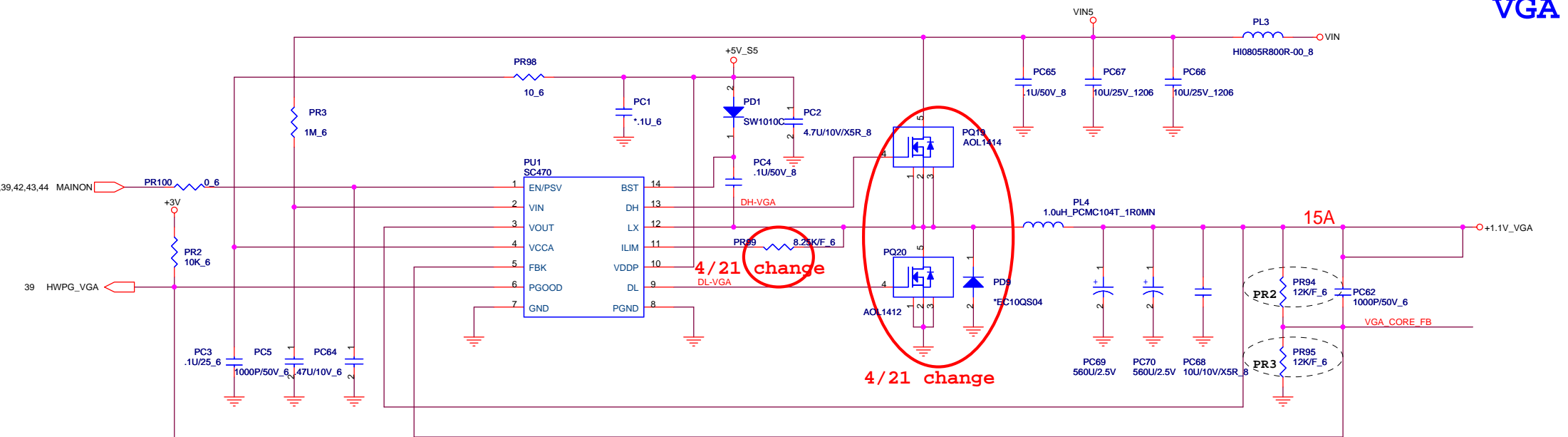
D3A:change from BCPL1040218 to BCSEMI04219 (EOL issue)



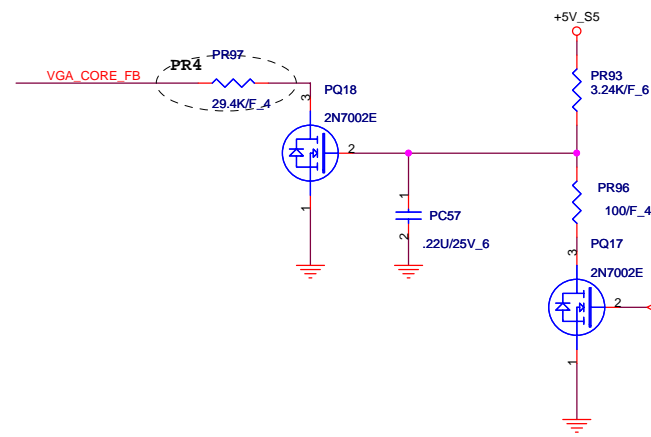
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C	<b>BATTERY CHARGER</b>	1A

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A1A:Add for M56 power sequence




HI-->  $V_{OUT} = (1 + R2/R3) * 0.5$   
 LO-->  $V_{OUT} = (1 + R2 / (R3 / R4)) * 0.5$

- M52P (G)**
- PR2 : 10K
- PR3 : 11K
- PR4 : 110K
- M54P**
- PR2 : 12K
- PR3 : 12K
- PR4 : 60.4K
- M56P**
- PR2 : 12K
- PR3 : 12K
- PR4 : 29.4K

**Power Play Mode**

VGA_PWR_SW	VGA_CORE
HI	0.95V--M52P (G)
	1.0V --M54P
	1.0V --M56P
Default	LO
	1.0V--M52P (G)
	1.1V--M54P
	1.2V--M56P



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