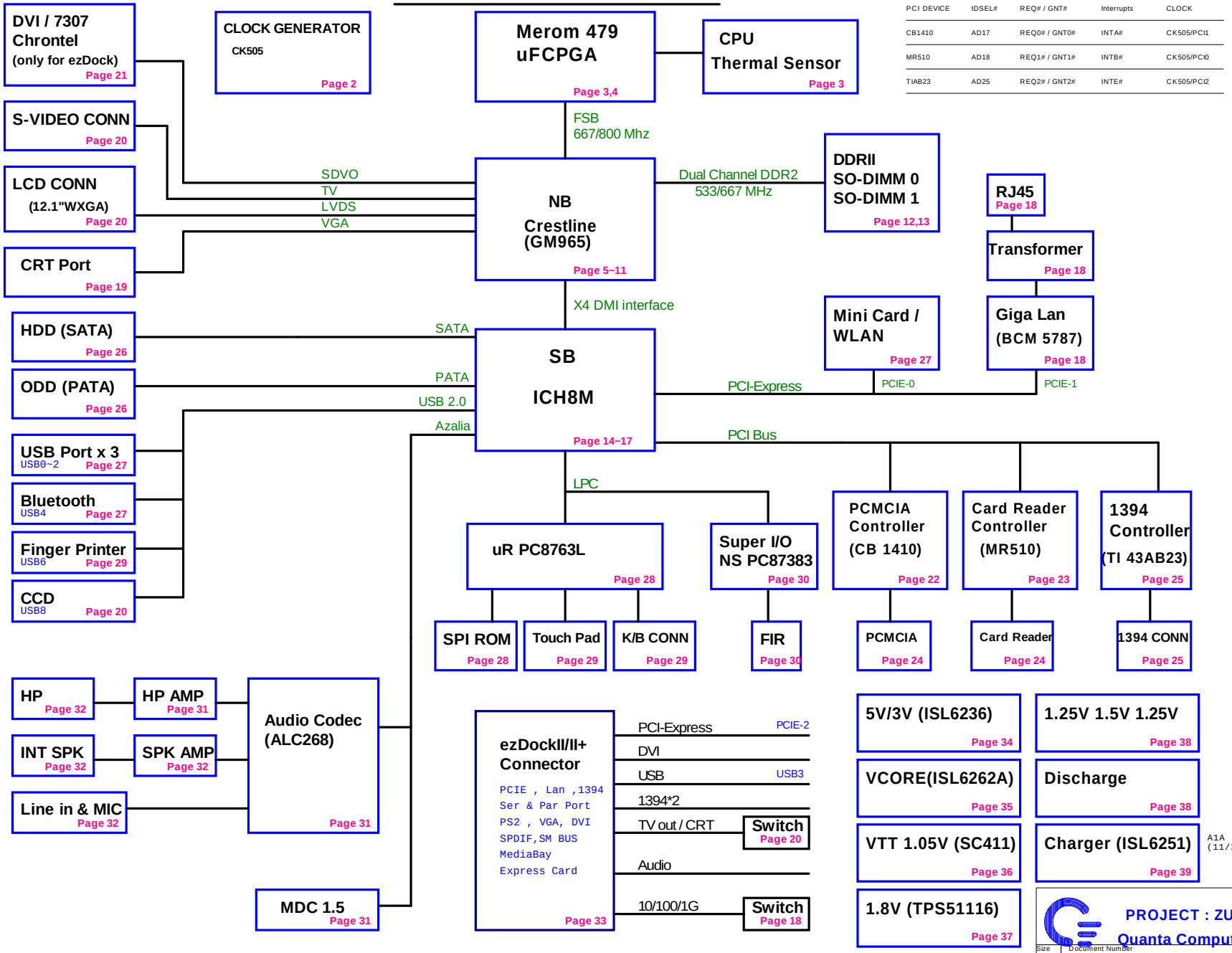
ZU1 SYSTEM BLOCK DIAGRAM



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTA#	CK505/PCI1
MR510	AD18	REQ1# / GNT1#	INTB#	CK505/PCI0
TIAB23	AD25	REQ2# / GNT2#	INTE#	CK505/PCI2

A1A
(11/2):(1) Re-name.
(2) Gerber out

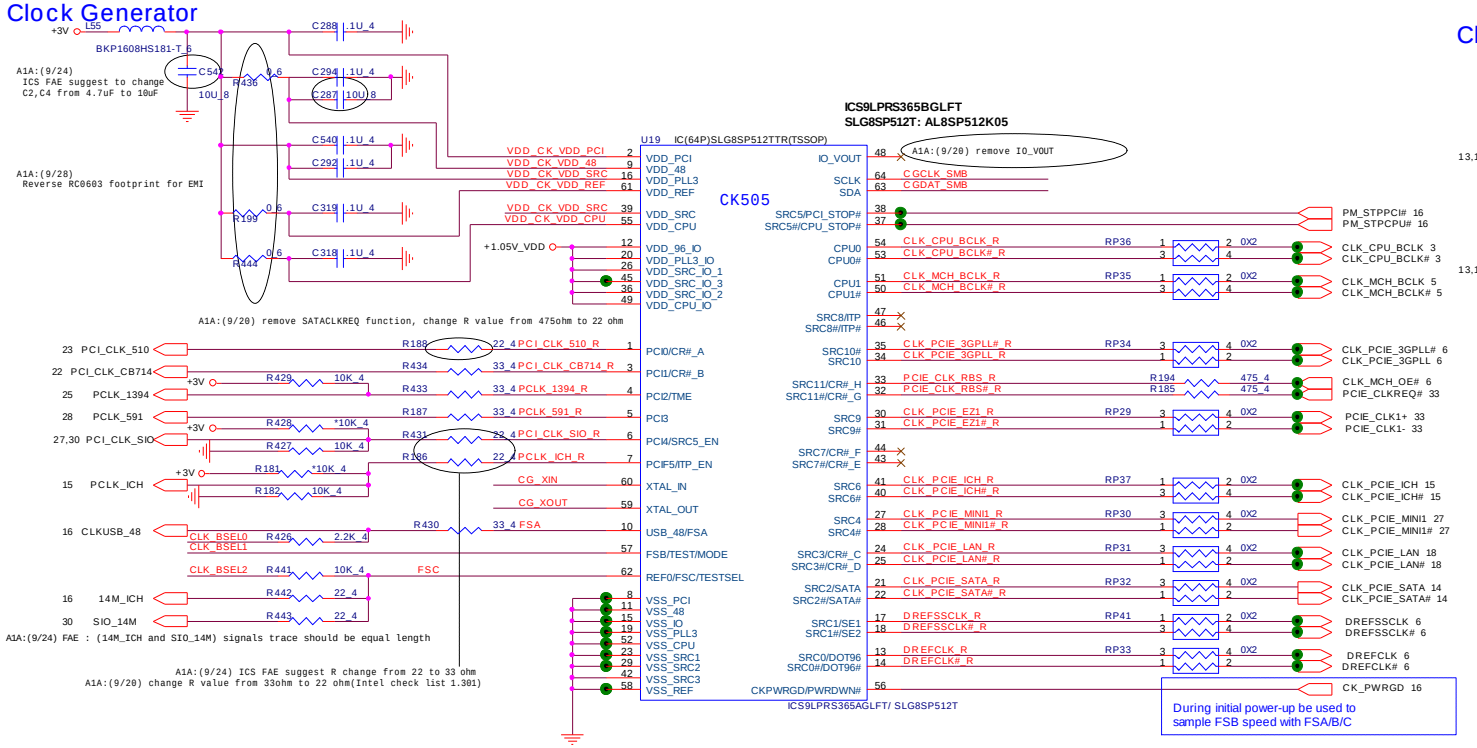
PROJECT : ZU1

Quanta Computer Inc.

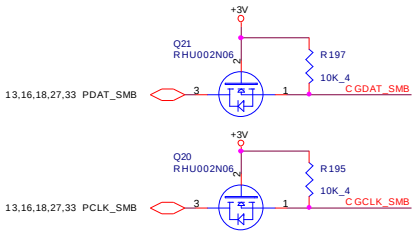
Size	Document Number	Rev
	Block Diagram	1A

Date: Thursday, November 02, 2006 Sheet 1 of 39

Clock Generator

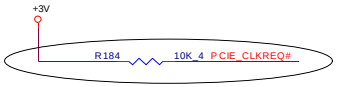


Clock Gen I2C

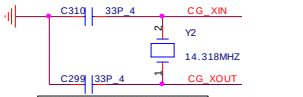


Pin	Active	Control signal
32	Low	SRC9/9#
33	Low	SRC10/10#

A1A:(9/24) Base on above table, SWAP SRC3 and SRC9



A1A:(9/24) Add PCIE_CLKREQ# PU to +3V



<check list>
XTAL length < 500mils

28 PCLK_DEBUG R432 *33_4 PCLK_1394_R

BIOS/ ERIC
IF M/B NEED LPC DEBUG PORT, \THEN STUFF THIS RESITER.

<check list>
(1)PCI2/TME: PU be used, the CK505 cannot over clock any of the clock for Trust Mode security purposes.

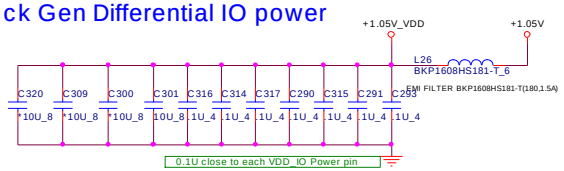
(2)PCI4/SRC5_EN: PU be used, the CK505 will be configured to use Pin37/38 to SRC5 clock.
If PD be detect at powe-on,the CK505 will setting Pin 37/38 to PCI_STOP/CUP_SOTP
(Default is setting to PCI_STOP/CUP_SOTP)

(3)PCIF5/ITP_EN: PU be used, the CK505 will be configured to use Pin46/47 to CPU ITP clock.
If PD be detect at powe-on,the CK505 will setting Pin 46/47 to SRC8
(Default is setting to SRC8)

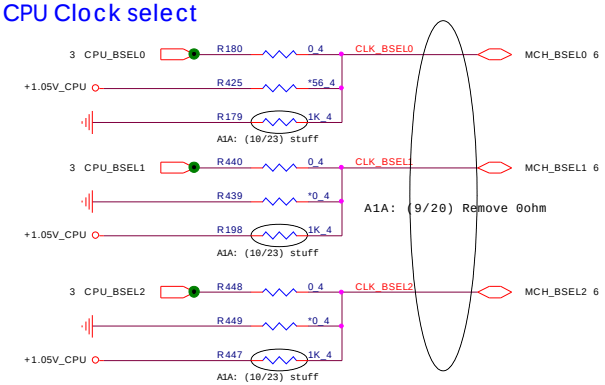
(4)SLG8SP512 Pin 6 select Pin 17, 18 output is LCDCLK or 27 M, PD is LCDCLK, PU is 27 M ,
Pin 37, 38 will fixed be use CPU_Stop and PCI_Stop.

(5)SLG505YC64 CK505 Standar parts follow standar setting

Clock Gen Differential IO power



CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	CLK. GEN./ CK505	1A

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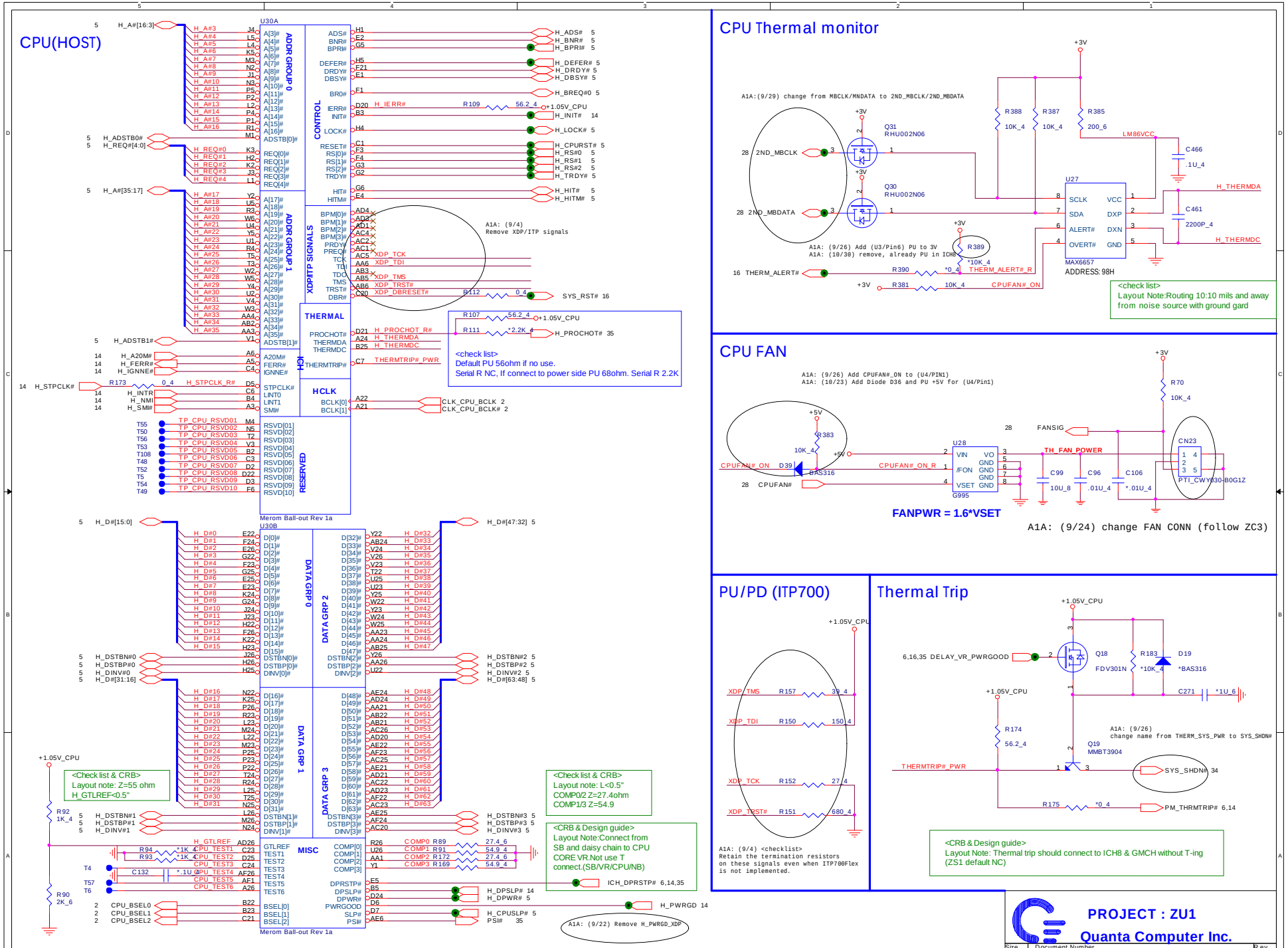
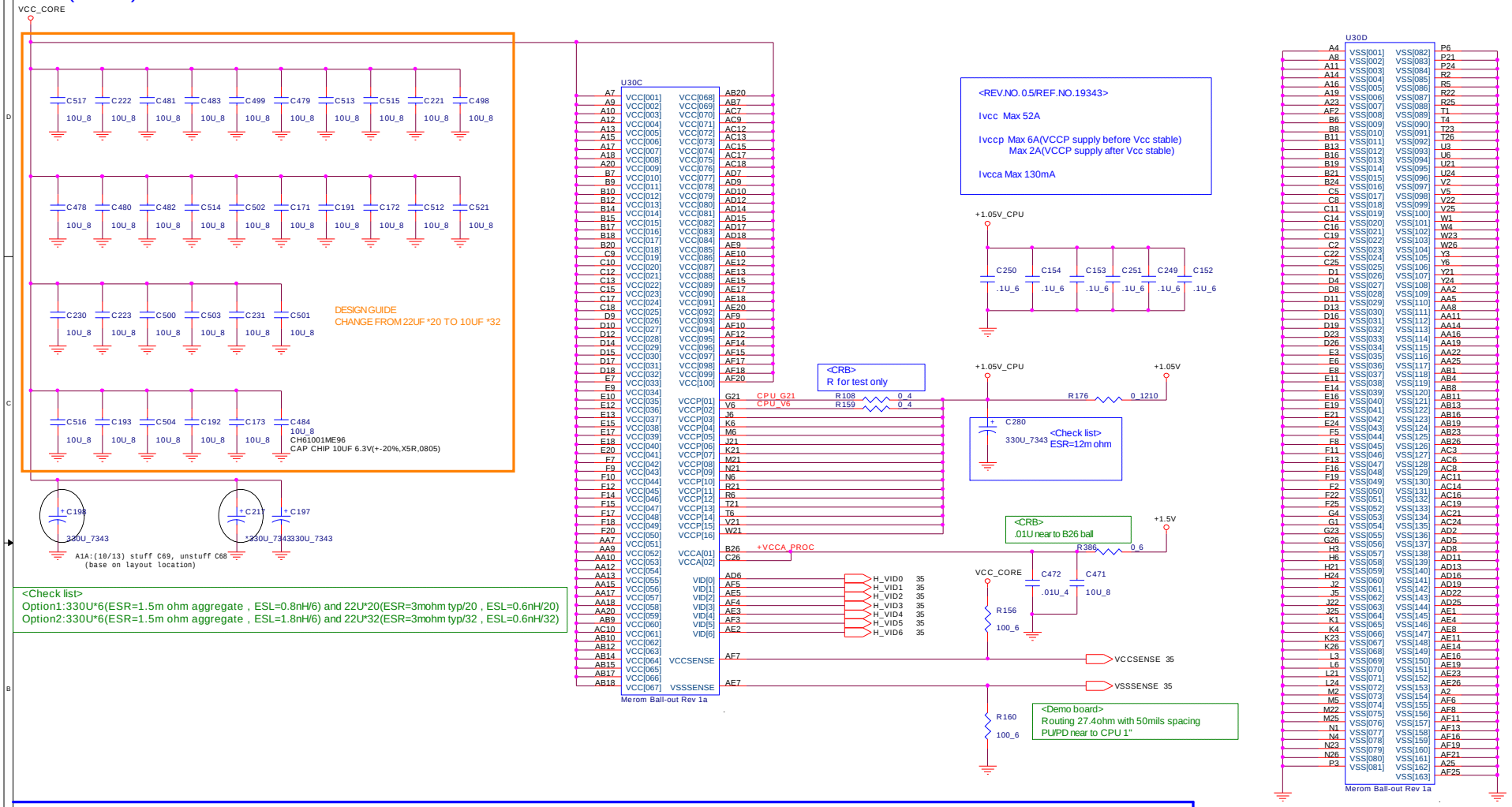

CPU(HOST)
U30A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
Merom Ball-out Rev 1a
U30B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Merom Ball-out Rev 1a
A1A: (9/4) Remove XDP/ITP signals
<check list>
Default PU 56ohm if no use.
Serial R NC, If connect to power side PU 68ohm. Serial R 2.2K
<Check list & CRB>
Layout note: Z=55 ohm
H_GTLREF<0.5"
<Check list & CRB>
Layout note: L<0.5"
COMP0/2 Z=27.4ohm
COMP1/3 Z=54.9
<CRB & Design guide>
Layout Note:Connect from
SB and daisy chain to CPU
CORE VR.Not use T
connect.(SB/VR/CPU/NB)
A1A: (9/22) Remove H_PWRGD_XDP
CPU Thermal monitor
A1A:(9/29) change from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA
Q31 RHU002N06
Q30 RHU002N06
U27
MAX6657
ADDRESS: 98H
A1A: (9/26) Add (U3/Pin6) PU to 3V
A1A: (10/30) remove, already PU in ICH8
<check list>
Layout Note:Routing 10:10 mils and away
from noise source with ground gard
CPU FAN
A1A: (9/26) Add CPUFAN#_ON to (U4/PIN1)
A1A: (10/23) Add Diode D36 and PU +5V for (U4/Pin1)
U28
G995
CN23
PTI_CWY030-B0G1Z
FANPWR = 1.6*VSET
A1A: (9/24) change FAN CONN (follow ZC3)
PU/PD (ITP700)
A1A: (9/4) <checklist>
Retain the termination resistors
on these signals even when ITP700Flex
is not implemented.
Thermal Trip
Q18 FDV301N
Q19 MMBT3904
A1A: (9/26)
change name from THERM_SYS_PWR to SYS_SHDN#
<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing
(ZS1 default NC)
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
CPU(1 of 2)/FAN/Thermal
Rev
1A
Date: Thursday, November 02, 2006
Sheet 3 of 39

CPU(Power)



<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2 of 2)	1A

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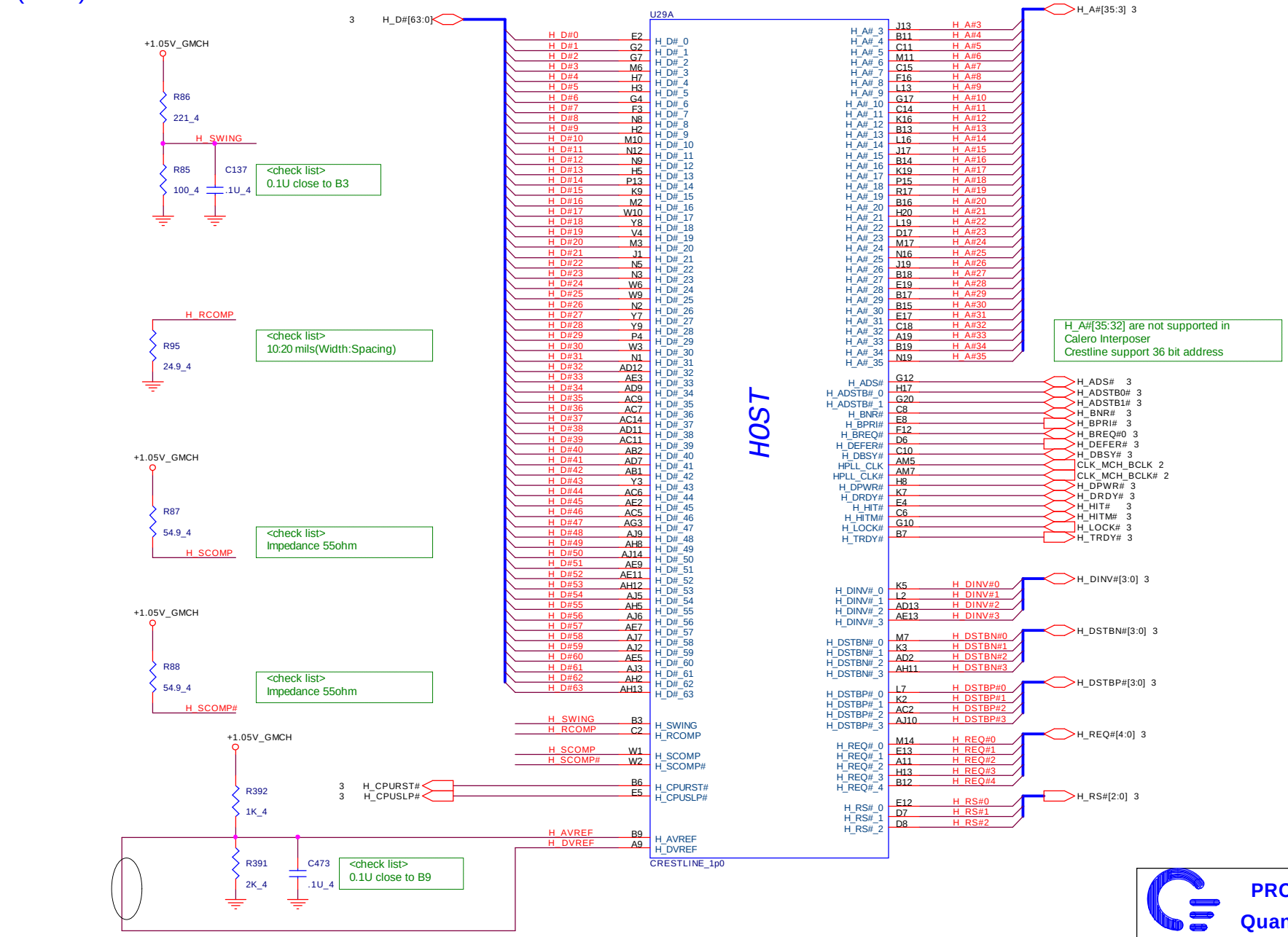
NB(HOST)



A1A:(9/20) remove R74 (0 ohm)

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A

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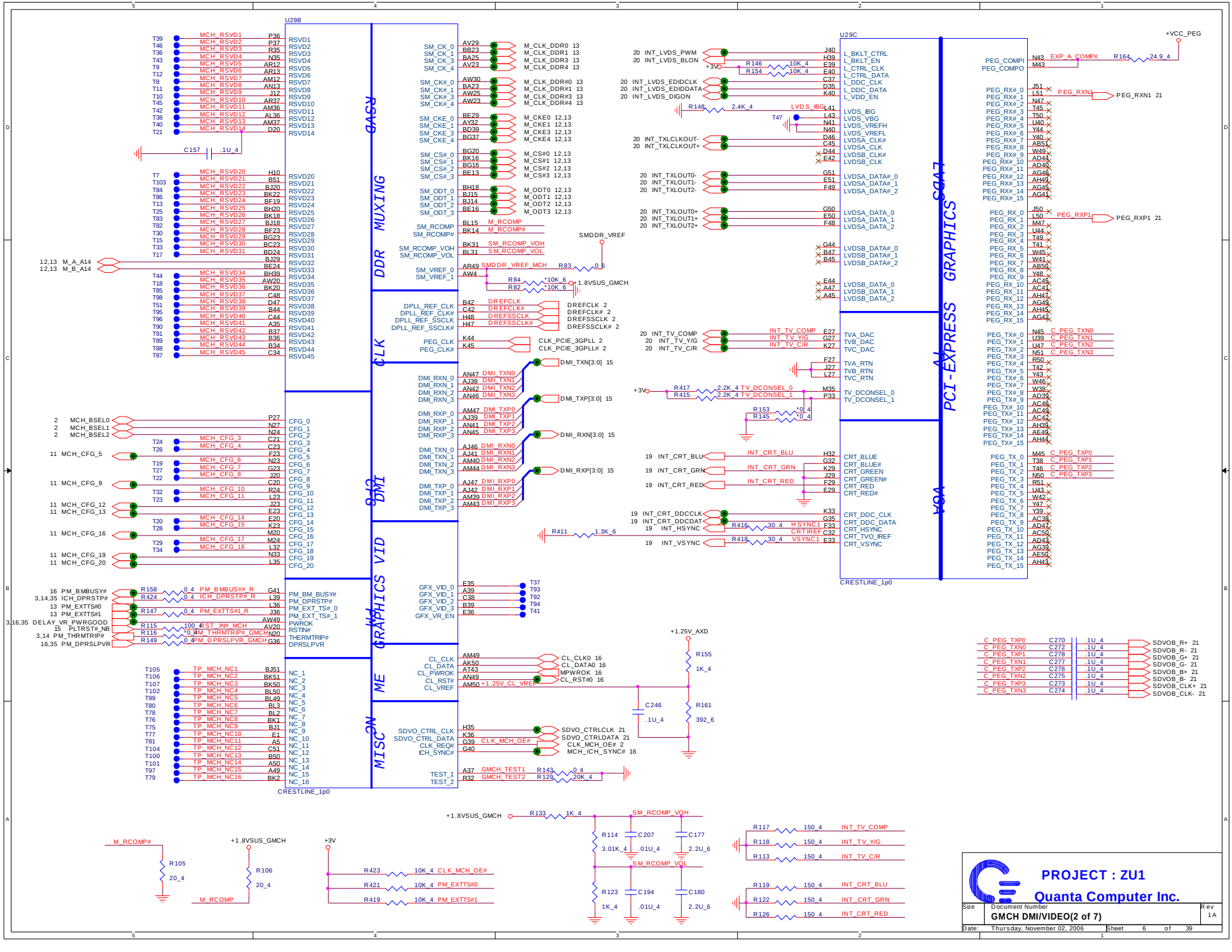
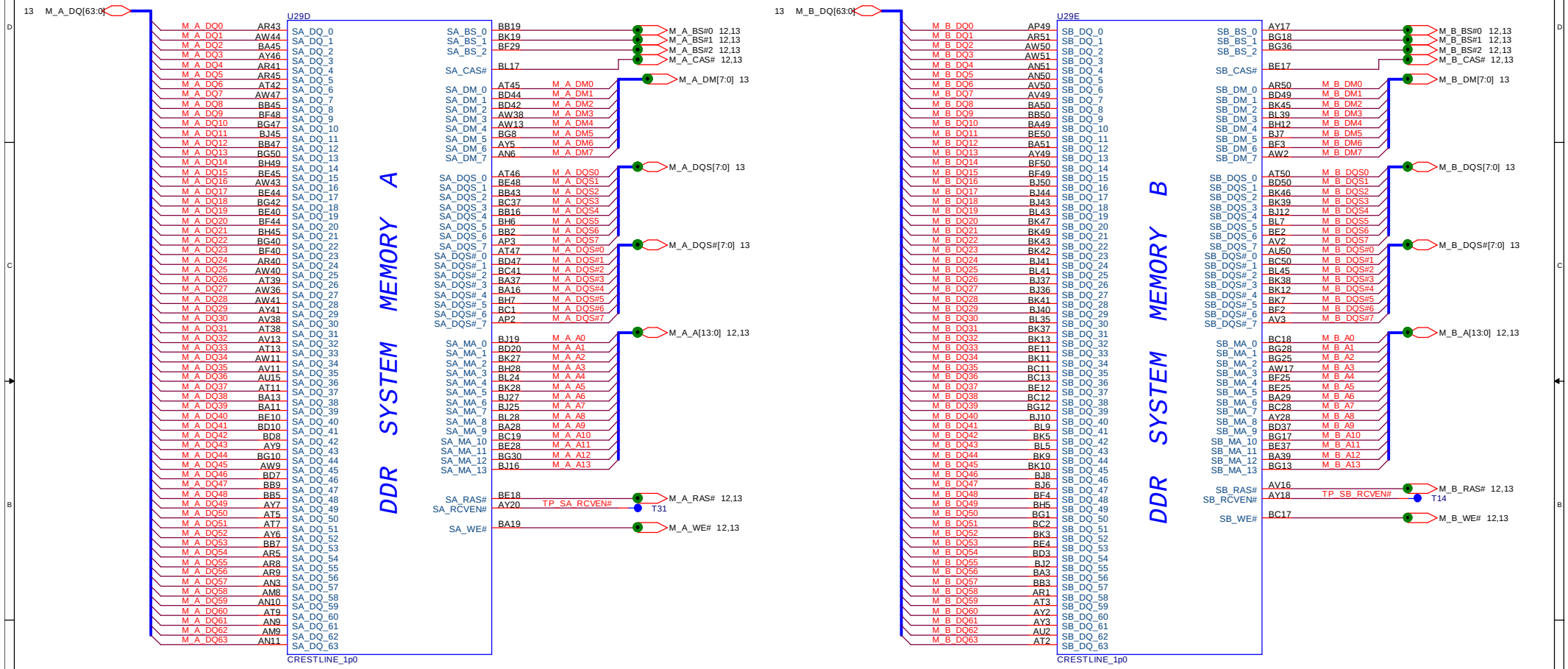

U29B
U29C
CRESTLINE_1p0
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
PCI-EXPRESS GRAPHICS
VGA
SMDDR_VREF
+1.8VSUS_GMCH
+1.25V_AXD
+VCC_PEG
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
GMCH DMI/VIDEO(2 of 7)
Rev
1A
Date: Thursday, November 02, 2006
Sheet 6 of 39

NB(Memory controller)



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	MCH DDR(3 of 7)	1A

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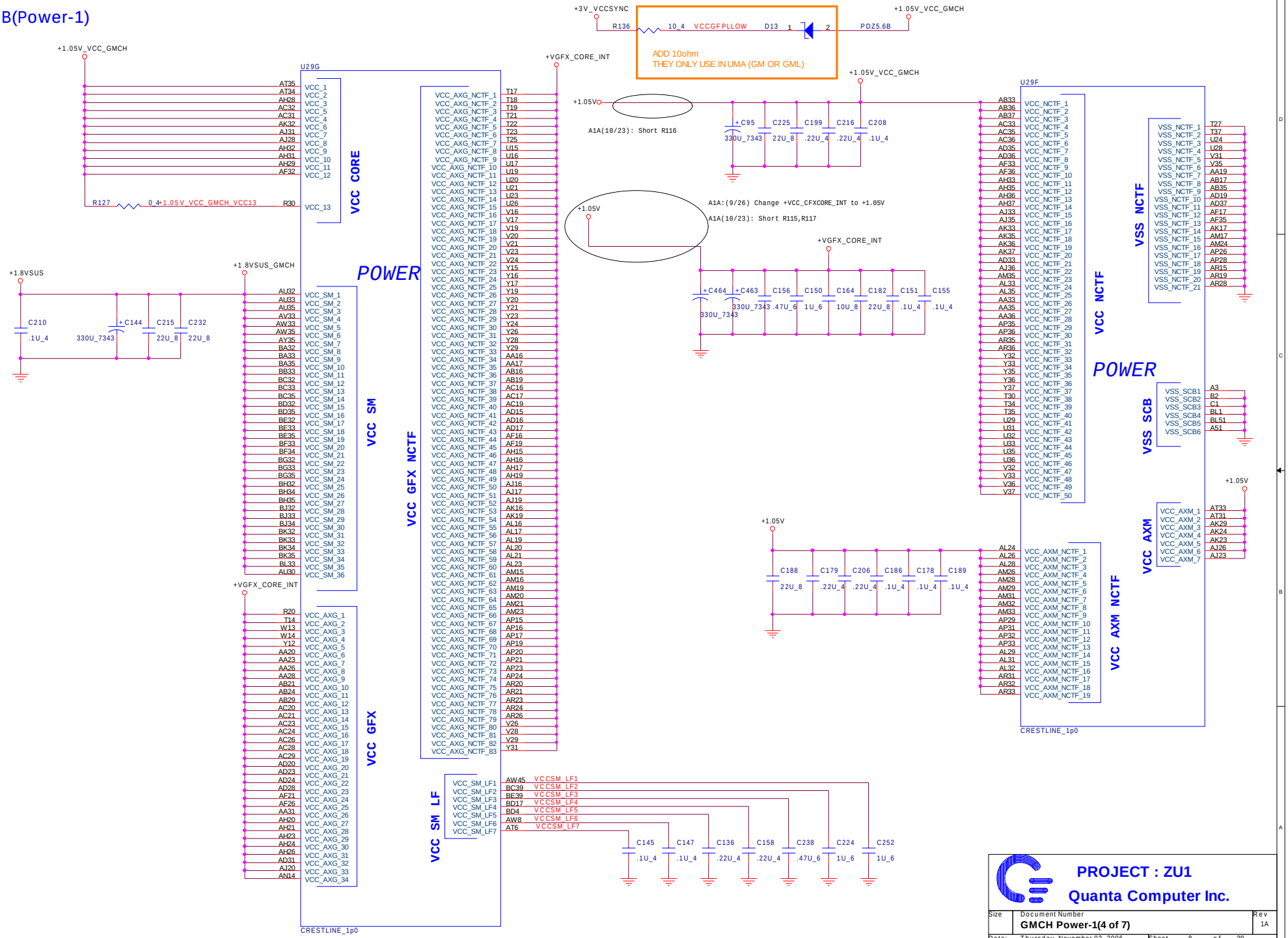
NB(Power-1)



Size	Document Number	Rev
	GMCH Power-1(4 of 7)	1A
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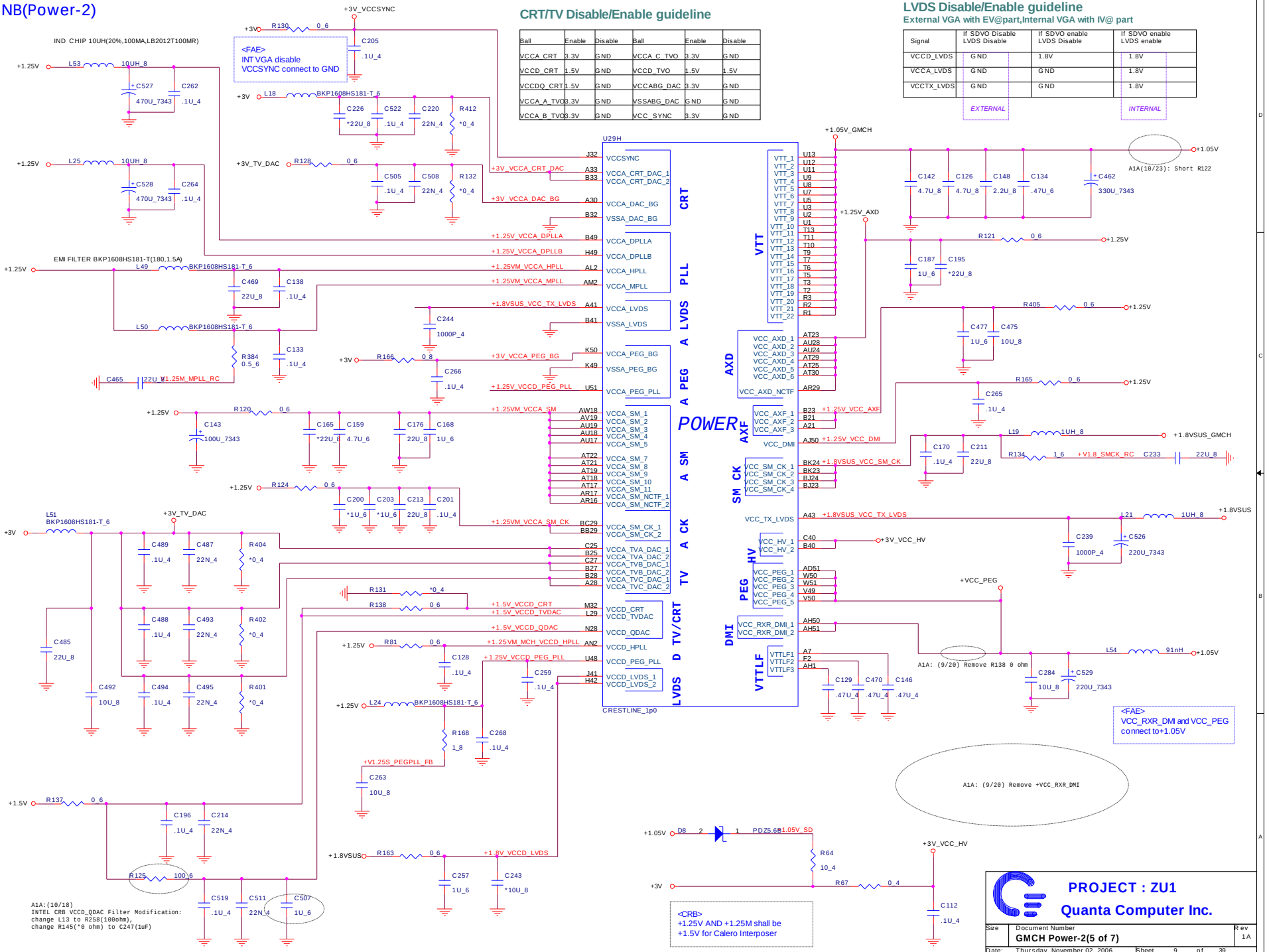
Quanta Computer Inc.

NB(Power-2)



CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V
	EXTERNAL		INTERNAL

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-2(5 of 7)	1A

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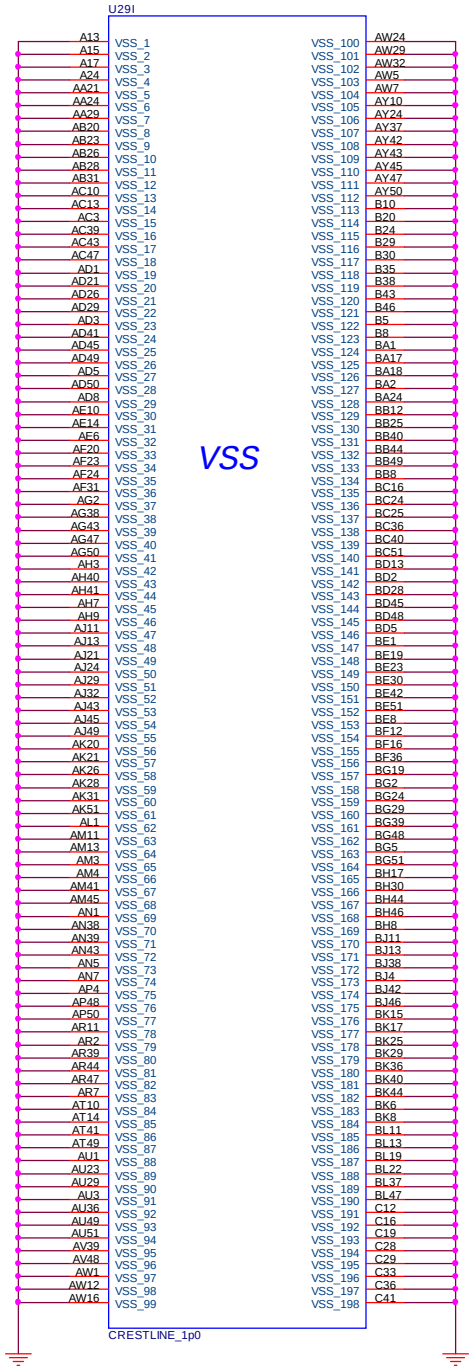
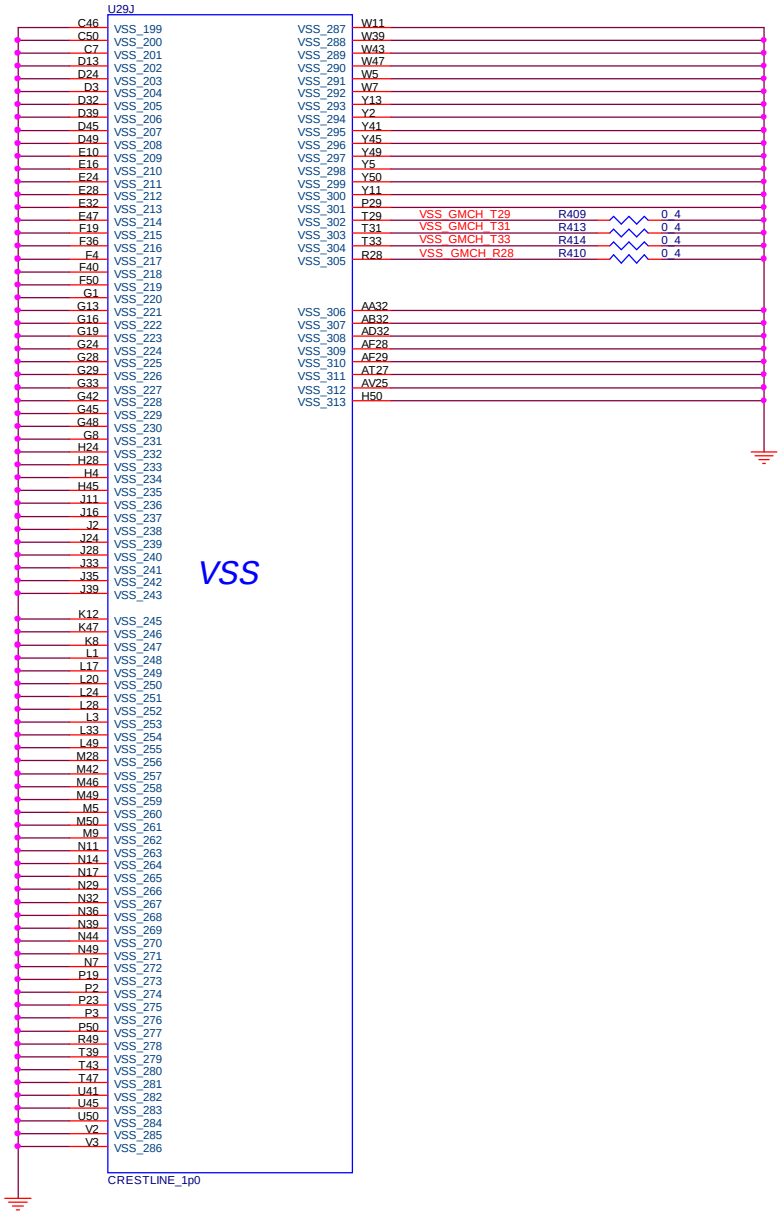
NB(Power-3)





PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-3(6 of 7)	1A

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Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

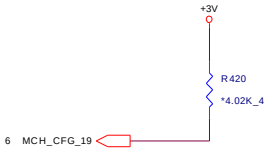
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)

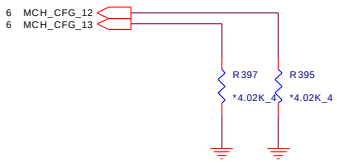
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

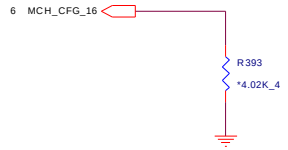
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

SDVO Present

Strap define at External DVI control page

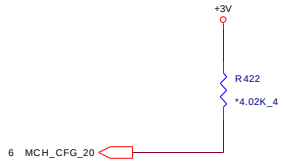
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A

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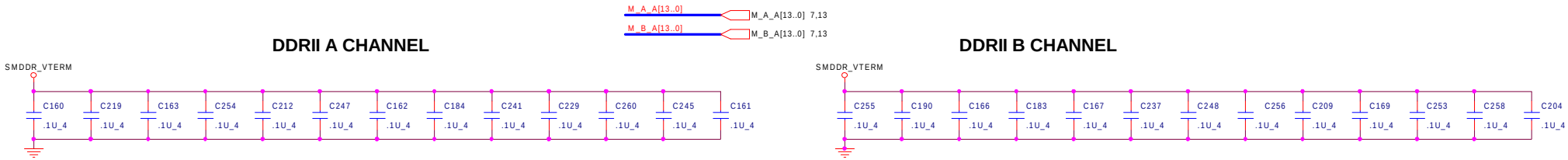
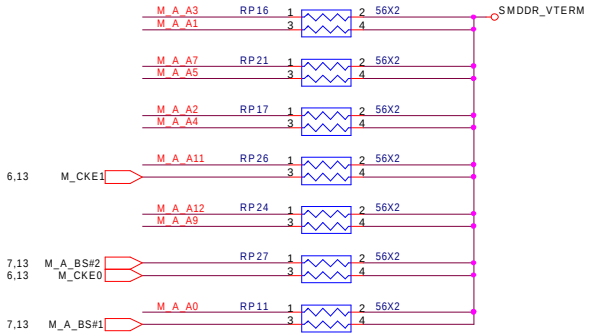
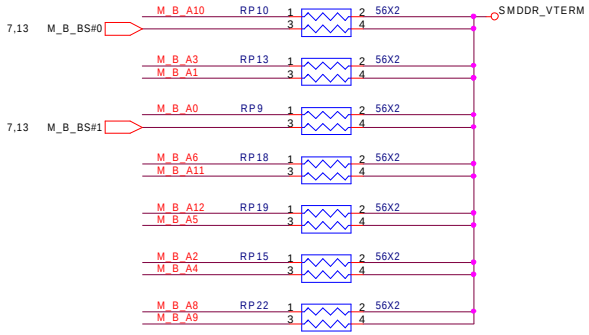
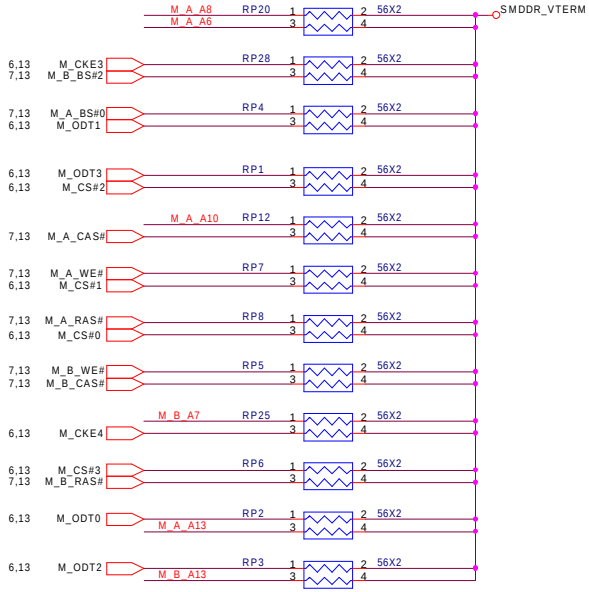
DDR2 Dual channel A/B PU



Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM







INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	1A

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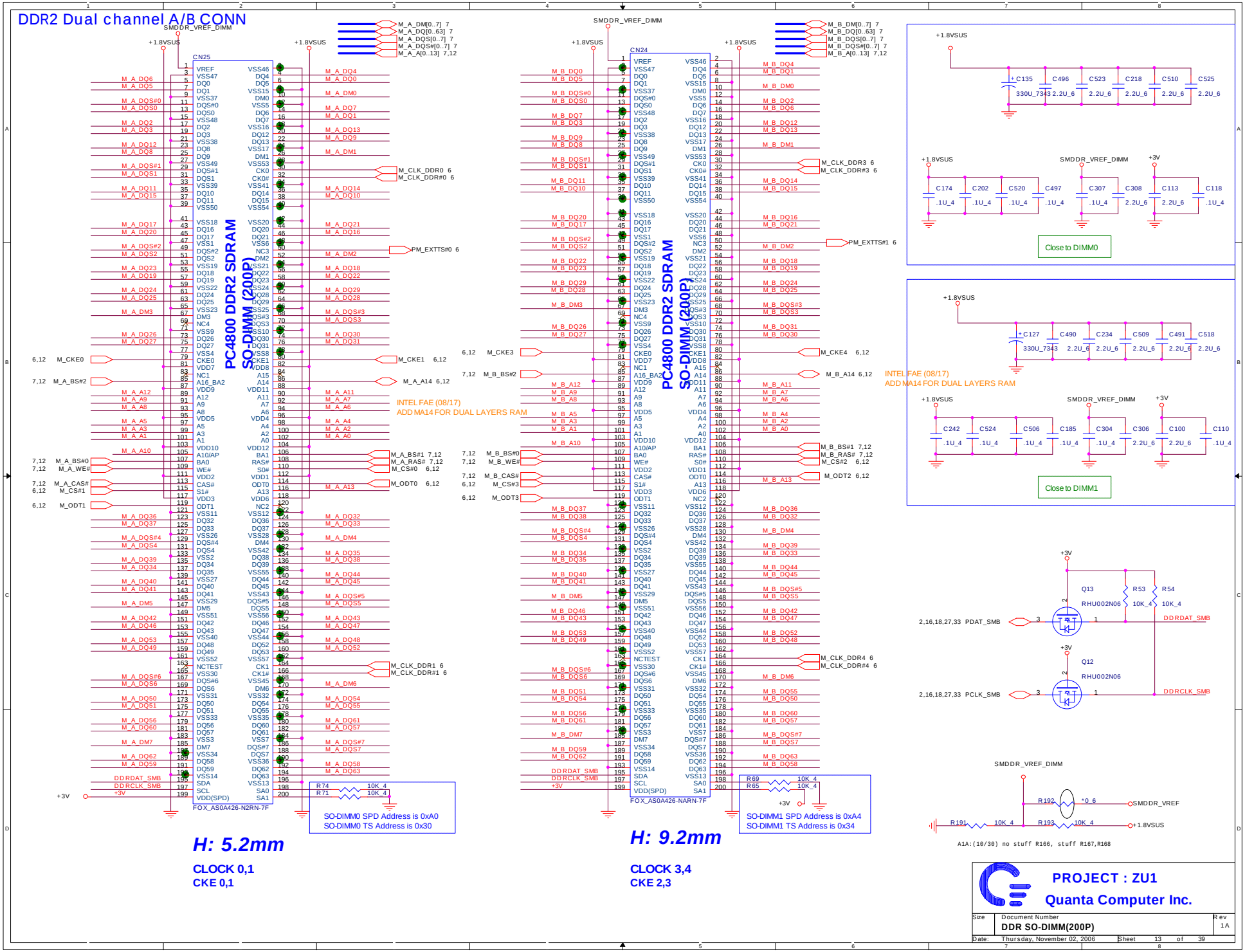
DDR2 Dual channel A/B CONN



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR SO-DIMM(200P)	1A

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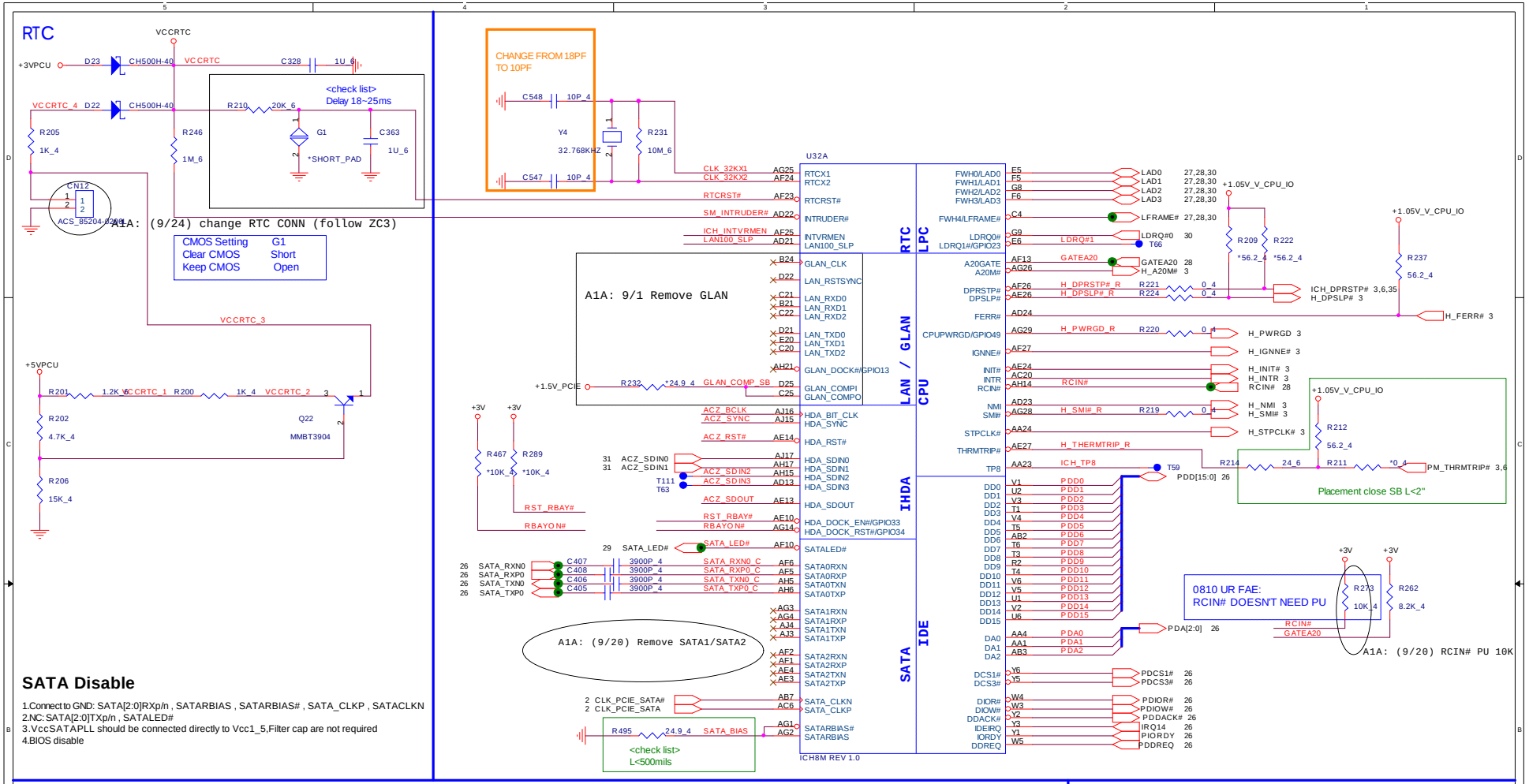


SATA Disable

1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable

SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

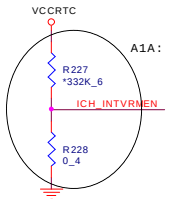
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

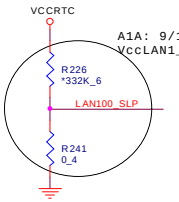
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

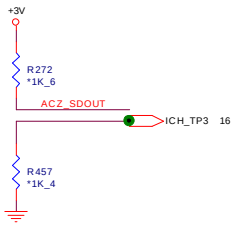
ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



A1A: (9/20) Change INTVRMEN from PU to PD

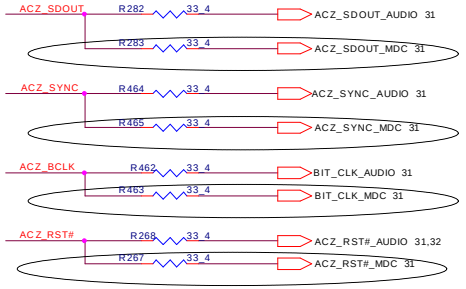


A1A: 9/1 Disable the internal VR powering VccLAN1_05, and VccCL1_05



HDA

A1A: 9/6 base on Intel design guide, add it.



PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M HOST(1 of 4)	1A

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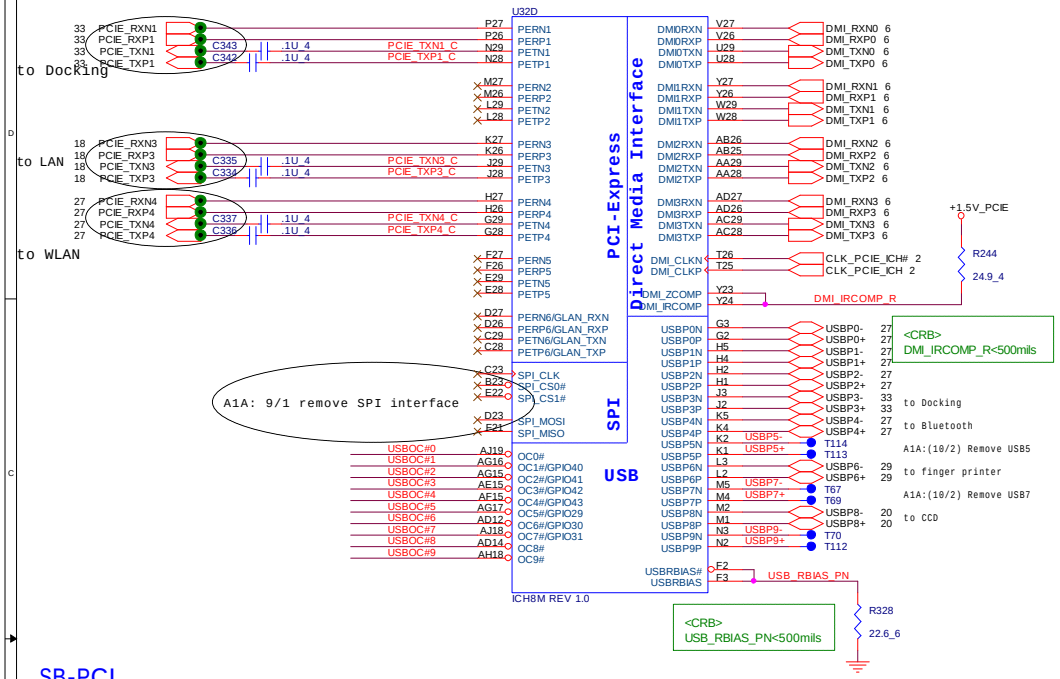
SB-PCIE/USB/DMI

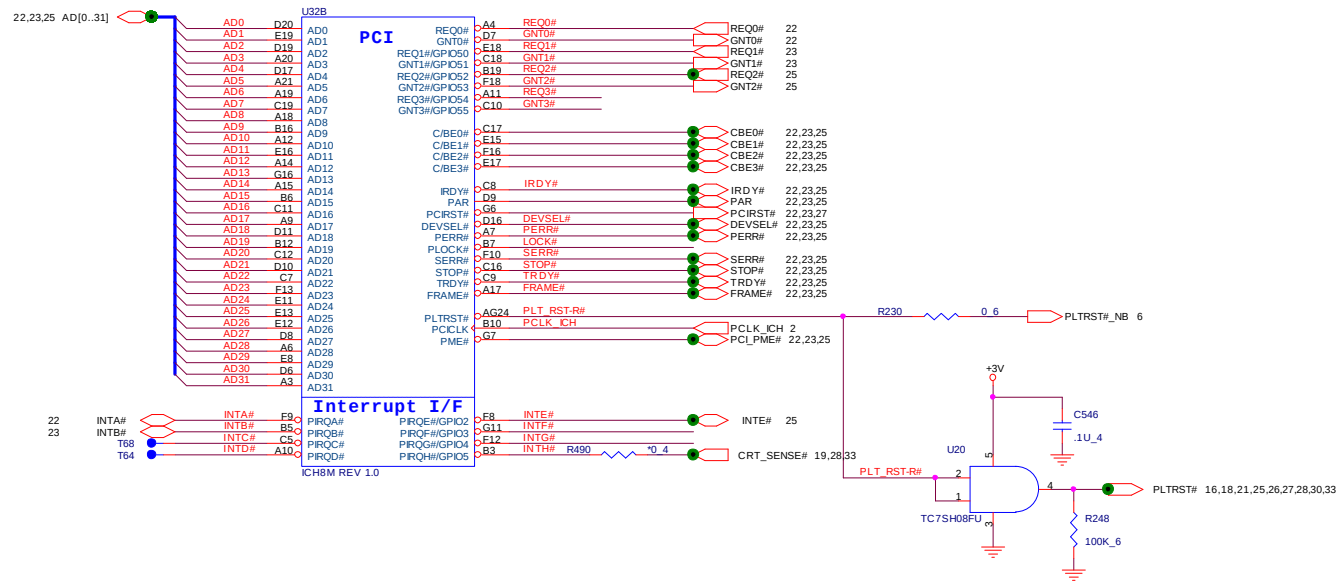


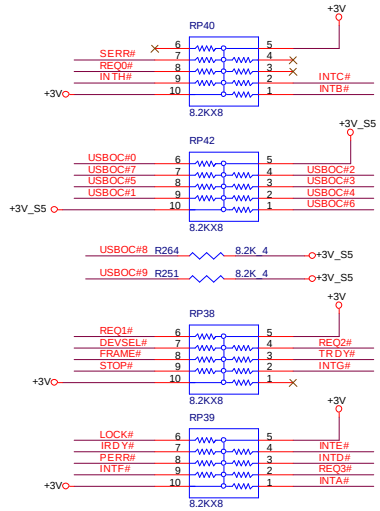
A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R301 *1K_4

SB-PCI





PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	1A

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SB-GPIO

NEW ADD SMB OF CL
NEW ADD CL_RST#1 FOR WLAN

<FAE>
CRB STP_PCI# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK_MCH_BCLK# must keep alive to make ME work)
I think there will be update for this design,
I suggest you to keep PU and 0 isolation resistors for this signal.

U32C

Signal	Pin	Block
PCLK_SMB	AJ26	SMBCLK
PDAT_SMB	AD19	SMBDATA
CL_RST#1	AG21	LINKALERT#
	AC17	SMLINK0
	AE19	SMLINK1
R I#	AF17	RI#
SYS_RST#	AD15	SUS_STAT#/LPCPD# / SYS_RESET#
	F4	
PM_BMBUSY#	AG12	BMBUSY#/GPIO0
SMB_ALERT#	AG22	SMBALERT#/GPIO11
PM_STPPCI_ICH#	AE20	STP_PCI#/GPIO15
PM_STPCPU_ICH#	AG18	STP_CPU#/GPIO25
CLKRUN#	AH11	CLKRUN#/GPIO32
PCIE_WAKE#	AE17	WAKE#
SERIRQ	AF12	SERIRQ
THERM_ALERT#	AC13	THRM#
VR_PWRGD_CLKEN	AJ20	VRMPWRGD
ICH_TP7	AJ22	TP7
KBSMI#	AJ8	TACH1/GPIO1
	AJ9	TACH2/GPIO6
DOCKIN#_R	AH9	TACH3/GPIO7
SCI#	AE16	GPIO8
GPIO12	AC19	GPIO12
	AG8	TACH0/GPIO17
BOARD_ID0	AH12	GPIO18
BOARD_ID1	AE11	GPIO20
BOARD_ID3	AG10	SCLOCK/GPIO22
ICH_GPIO22	AH25	QRT_STATE0/GPIO27
ICH_GPIO27	AD16	QRT_STATE1/GPIO28
ICH_GPIO28	AG13	SATACLKREQ#/GPIO35
GPIO35	AF9	SLOAD/GPIO38
RST_HDD#	AJ11	SDATAOUT0/GPIO39
ICH_GPIO39	AD10	SDATAOUT1/GPIO48
ICH_GPIO48	AD9	SPKR
ACZ_SPKR	AJ13	MCH_SYNC#
MCH_ICH_SYNC#_R	AJ21	TP3
ICH_TP3		

ICH8M REV 1.0

SMB / SATA GPIO / Clocks / SYS GPIO / Power MGT / GPIO / Controller Link / MISC

Signal	Pin	Block
SATA0GP/GPIO21	AJ12	SATA0GP/GPIO21
SATA1GP/GPIO19	AJ10	SATA1GP/GPIO19
SATA2GP/GPIO36	AF11	SATA2GP/GPIO36
SATA3GP/GPIO37	AG11	SATA3GP/GPIO37
CLK14	AG9	CLK14
CLK48	G5	CLK48
SUSCLK	D3	SUSCLK
SLP_S3#	AG23	SLP_S3#
SLP_S4#	AF21	SLP_S4#
SLP_S5#	AD18	SLP_S5#
S4_STATE#/GPIO26	AH27	S4_STATE#/GPIO26
PWROK	AE23	PWROK
DPRSLPVR/GPIO16	AJ14	DPRSLPVR/GPIO16
BATLOW#	AE21	BATLOW#
PWRBTN#	C2	PWRBTN#
LAN_RST#	AH20	LAN_RST#
RSMRST#	AG27	RSMRST#
CK_PWRGD	E1	CK_PWRGD
CLPWROK	E3	CLPWROK
SLP_M#	AJ25	SLP_M#
CL_CLK0	F23	CL_CLK0
CL_CLK1	AE18	CL_CLK1
CL_DATA0	F22	CL_DATA0
CL_DATA1	AF19	CL_DATA1
CL_VREF0	D24	CL_VREF0
CL_VREF1	AH23	CL_VREF1
CL_RST#	AJ23	CL_RST#
MEM_LED/GPIO24	AJ27	MEM_LED/GPIO24
ME_EC_ALERT/GPIO10	AJ24	ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14	AE22	EC_ME_ALERT/GPIO14
WOL_EN/GPIO9	AG19	WOL_EN/GPIO9

EMAIL LED OUT THAT IS ACTIVE LOW.

SIO/PC87383 DOES NOT NEED 32KHz

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST#
should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

A1A: (9/26) change name from VR_PWRGD_CLKEN# to VR_PWRGD_CK410#

A1A: (9/20)change neme to DOCKIN#

A1A: (9/11) Remove LAN_PHYPC

A1A: (9/26) Remove SATACLKREQ#

A1A: (9/29) no support iAMT, remove SMB_CLK_ME,SMB_DATA_ME

A1A: (9/11) Remove RI#

A1A: (9/26) Remove S4_STAT#, need be confirm?

A1A: (9/16) need be confirm? Remove SUSM# used to control power planes to the Intel AMT subsystem

A1A: 9/1 change to PLTRST#

A1A: (9/26) Remove (1)ME_EC_ALERT# (2)EC_ME_ALERT

A1A: (9/11) Remove LAN_WOL_EN circuit

FOR CONTROLLER LINK ADD CL1 BUS

Controller Link 1 VREF for IAMT support only

A1A:(10/12) change from +3V to +3VSUS (Refer to ZC1)

A1A:(9/29) no support iAMT, remove 2ND_MBCLK,2ND_MBDATA,Q11,Q12

A1A:(9/20) Refer to ZD1, Add ICH_PWROK circuit

A1A:(10/30) change DOCKIN#_R PU from +3V to +3V_S5

INTEL CRB: PU +3V

BIOS/ERIC: UNSTUFF

INTEL CRB NEED THOSE PU & PD.

INTEL CRB SHOW IT

INTEL CRB SHOW IT

DISABLE LAN: STUFF

INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"

TO ICH8

FROM uR(EC)

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

Internal Pull up

ECN 2A
INTEL CRB V1.301
CL_RST# NO NEED PU.

A1A:(9/29) no support iAMT, remove PU +3V_S5 circuit (R259/R258)

Board ID	ID3	ID2	ID1	ID0
With EZ Dock	0	0	0	0
W/O EZ Dock	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	1A

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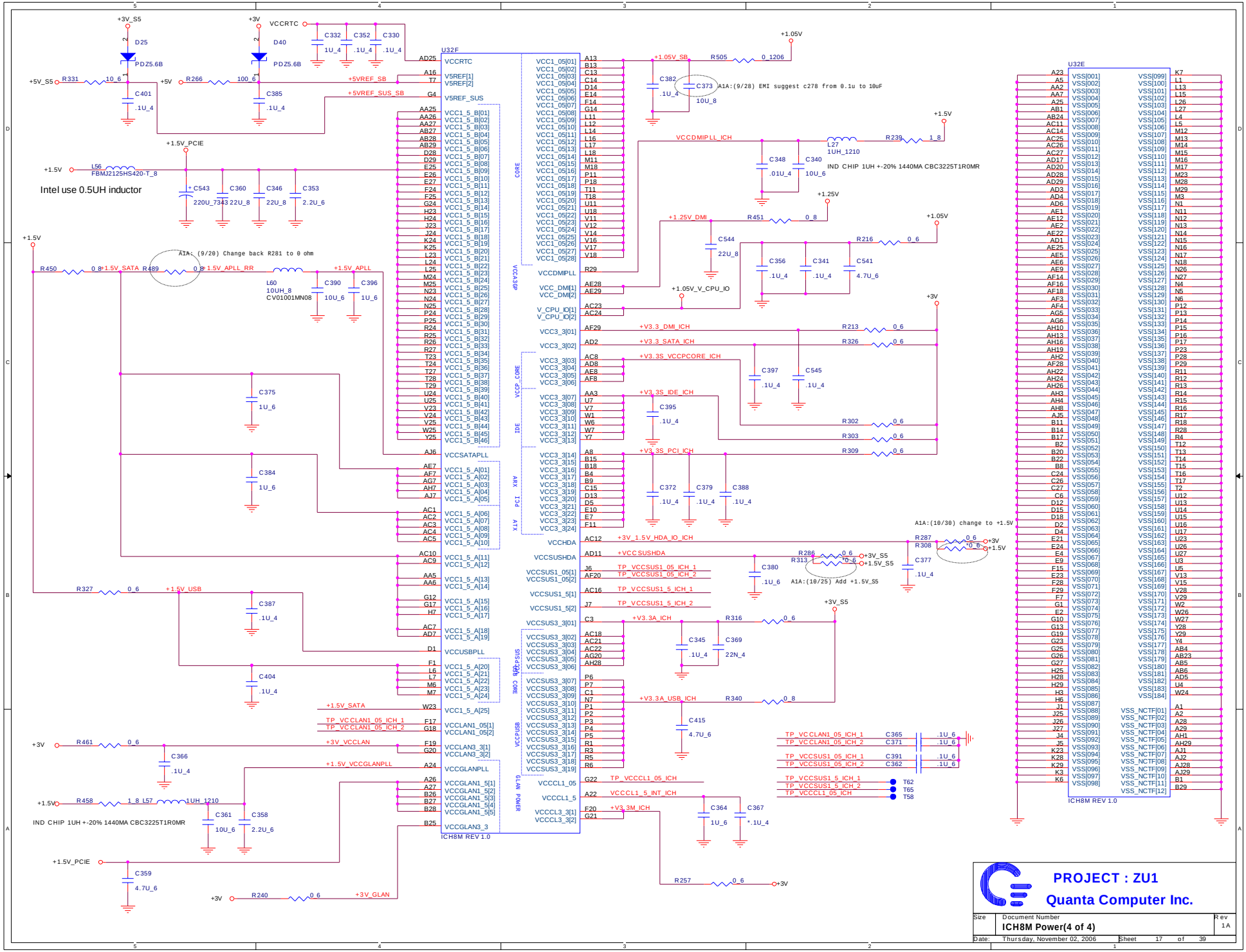
U32F
ICH8M REV 1.0
U32E
ICH8M REV 1.0
Intel use 0.5UH inductor
IND CHIP 1UH +-20% 1440MA CBC3225T1R0MR
A1A:(9/28) EMI suggest c278 from 0.1u to 10uF
A1A: (9/20) Change back R281 to 0 ohm
A1A:(10/30) change to +1.5V
A1A:(10/25) Add +1.5V_S5
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
ICH8M Power(4 of 4)
Rev
1A
Date: Thursday, November 02, 2006
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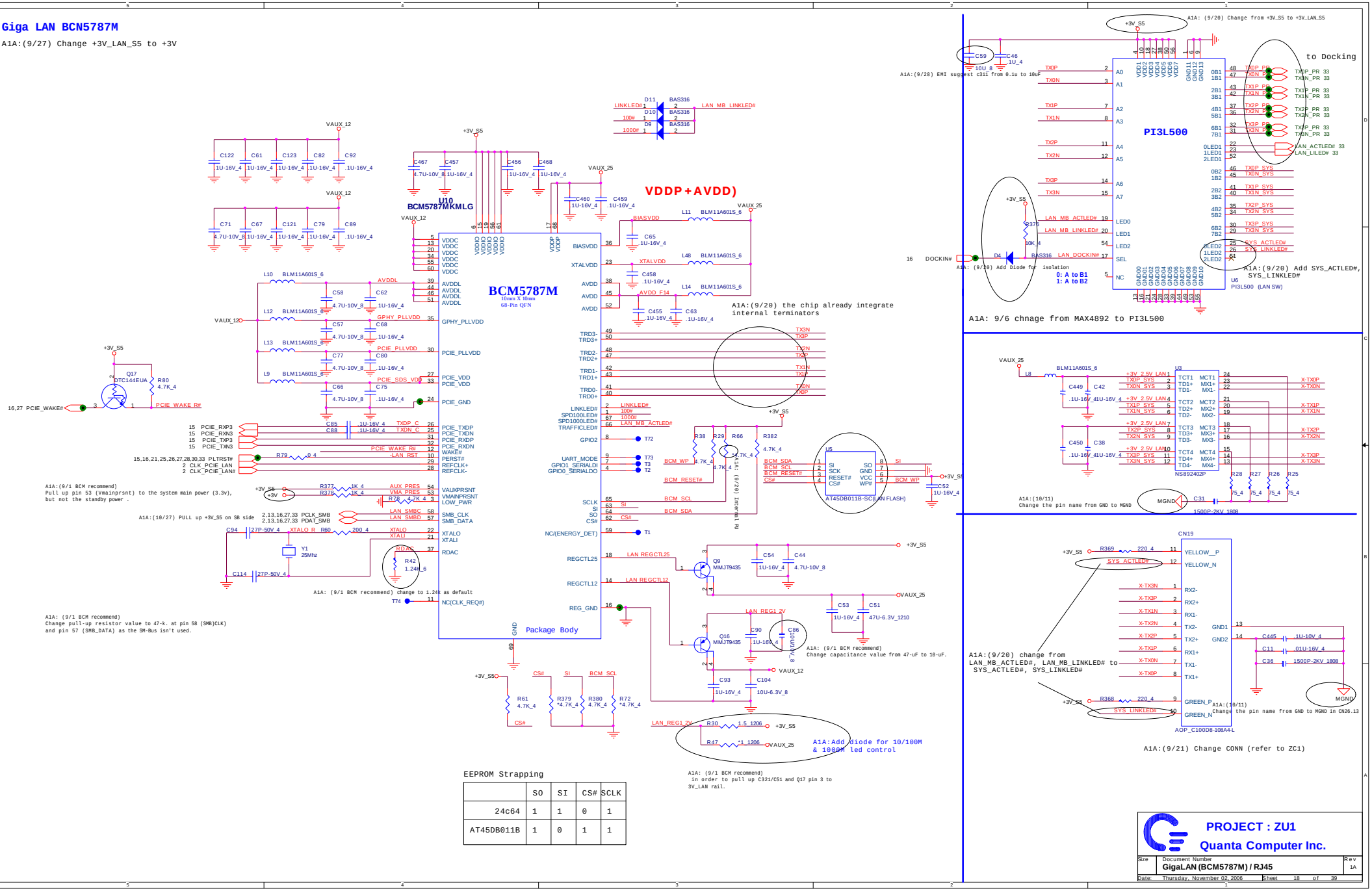
Giga LAN BCN5787M

A1A:(9/27) Change +3V_LAN_S5 to +3V



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	GigaLAN (BCM5787M) / RJ45	1A

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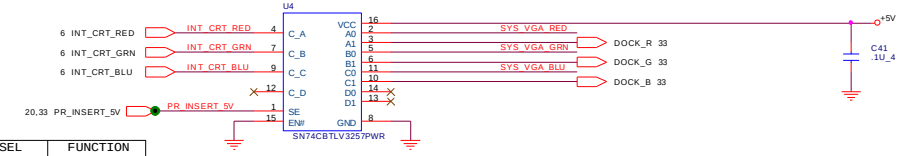
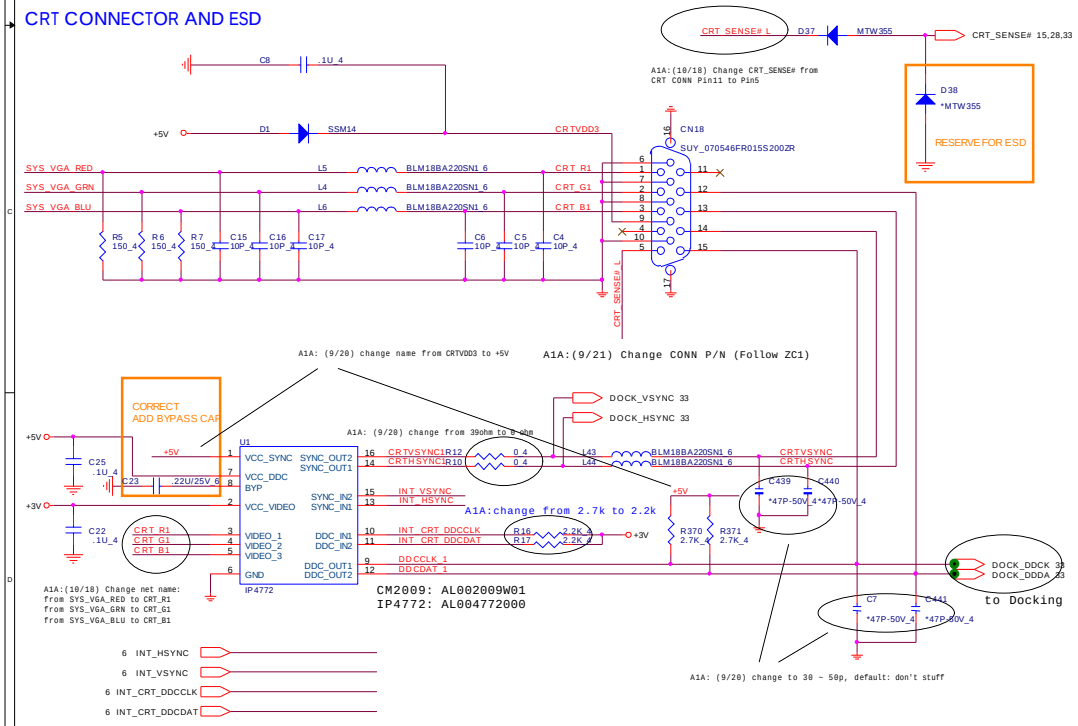
CRT Select



SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

A1A: (9/20) Remove NEZ@ ciucuit

CRT CONNECTOR AND ESD



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	CRT	1A

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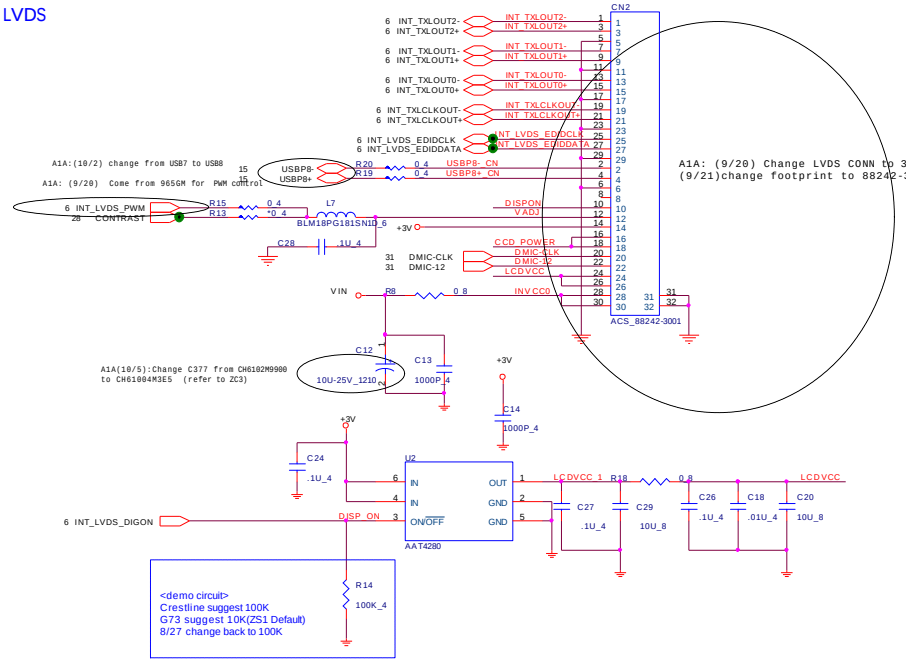
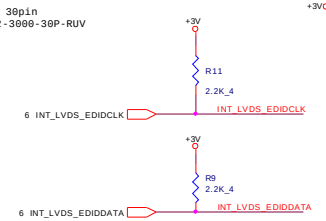
LVDS

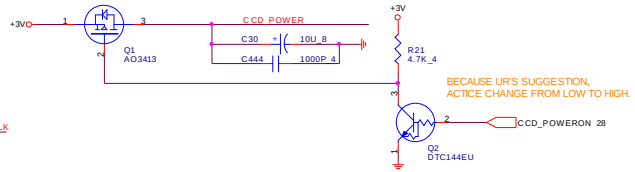


A1A(10/5):Change C377 from CH6102M9900 to CH61004M3E5 (refer to ZC3)

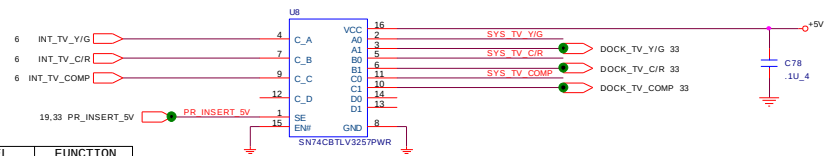
C12 10U-25V_1210 C13 1000P_4 C14 1000P_4



CAMERA MODULE

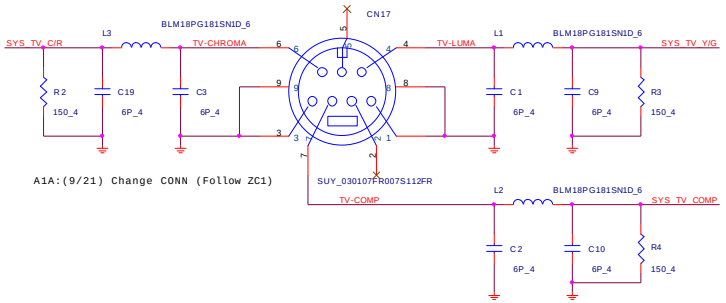


TV Out (SVHS) MiniDIN 7-pin

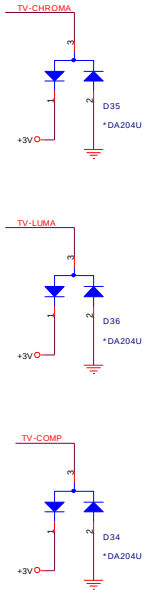


SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

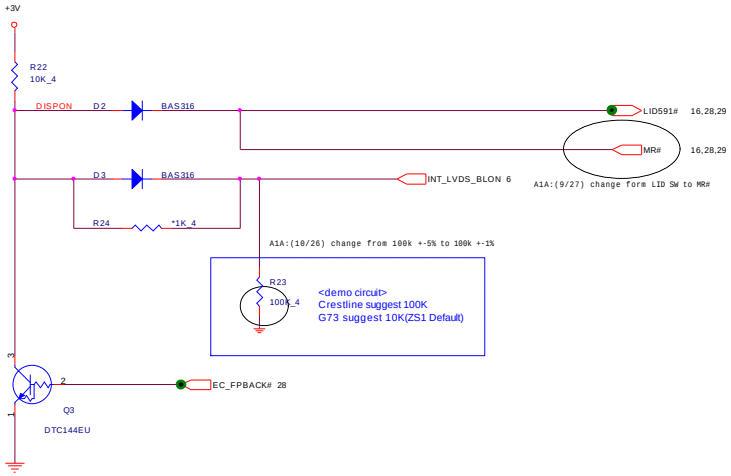
A1A: (9/20) Remove "NEZ@" circuit



A1A:(9/21) Change CONN (Follow ZC1)



MR Sensor



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/MR senseor/SVIDEO	1A

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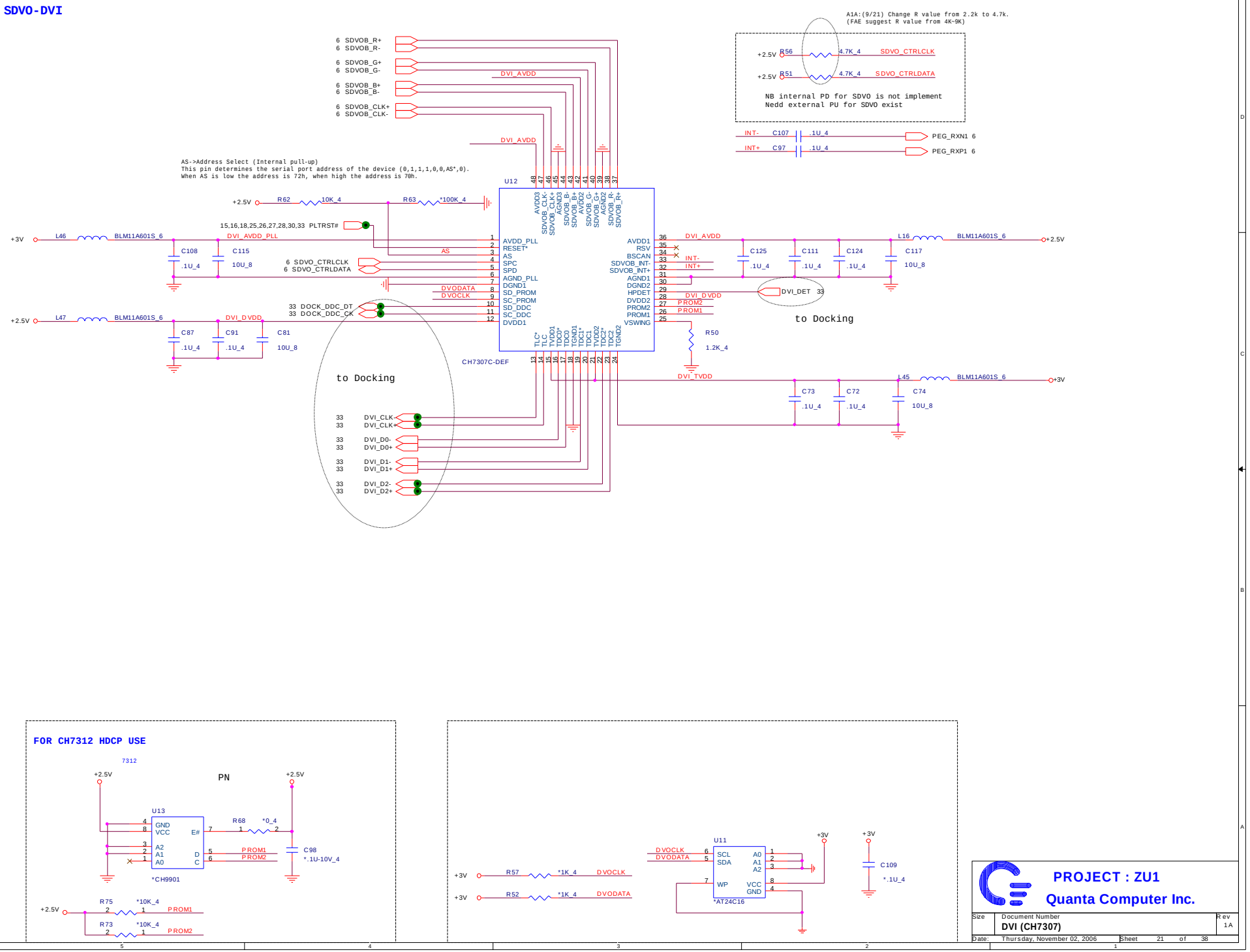
SDVO-DVI



FOR CH7312 HDCP USE

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	DVI (CH7307)	1A

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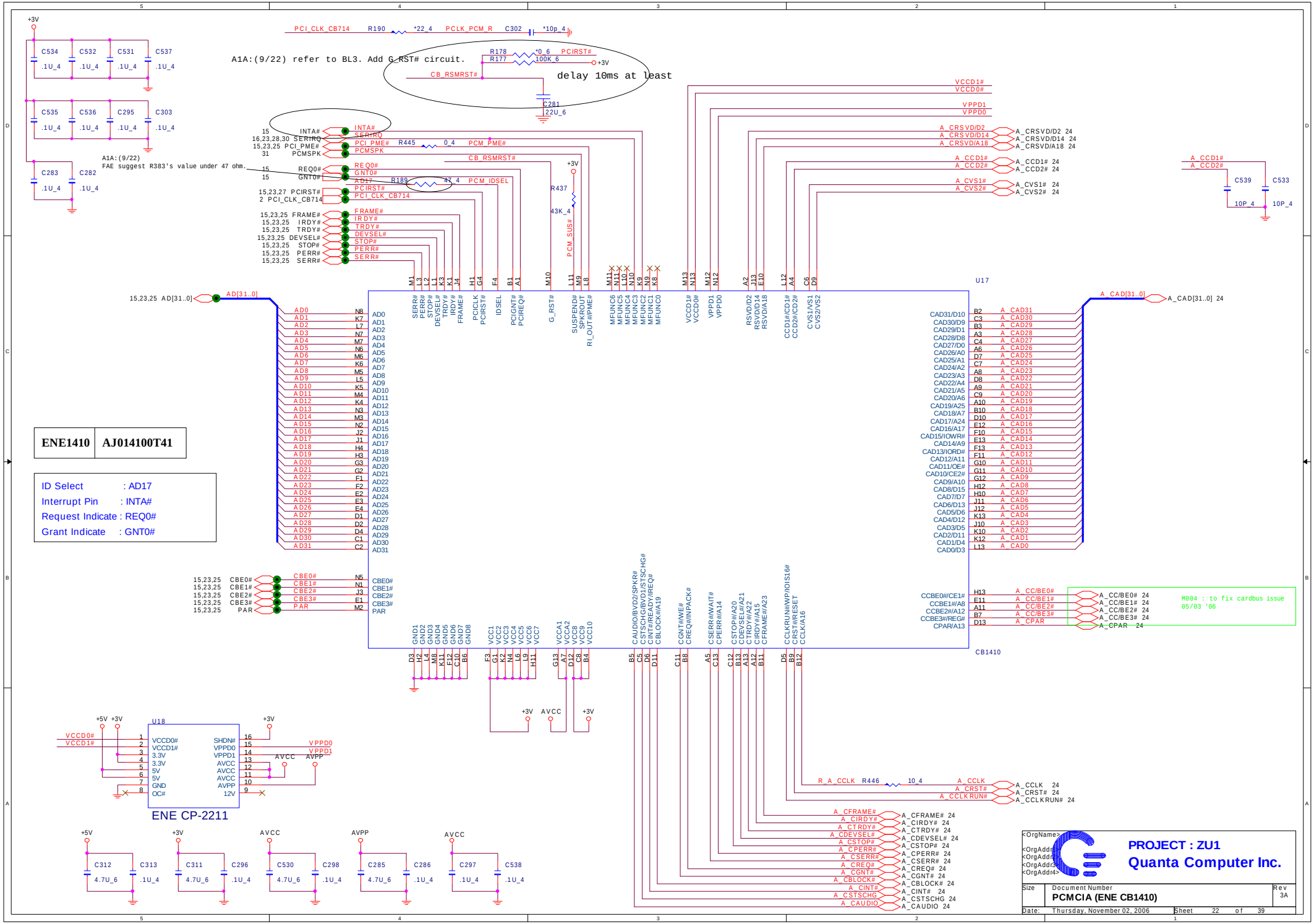
ENE1410 AJ014100T41
ID Select : AD17
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#
A1A:(9/22) refer to BL3. Add G_RST# circuit.
delay 10ms at least
A1A:(9/22)
FAE suggest R383's value under 47 ohm.
U17
CB1410
U18
ENE CP-2211
M004 : to fix cardbus issue 05/03 '06
PROJECT : ZU1
Quanta Computer Inc.
PCMCIA (ENE CB1410)
Thursday, November 02, 2006
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ID Select : AD18
Interrupt Pin : INTB#
Request Indicate : REQ1#
Grant Indicate : GNT1#

A1A:(9/22) remove R634,R636

GRST# should connect to Power On reset if support S3

A1A:(9/22) XMDAT4B is for 8 bit MMC,remove it.

A1A:(9/22) FAE suggest R value under 47 ohm

A1A:(9/26) For EMI solution (close to MR510)

A1A:(9/26) For EMI solution

A1A:(9/22) Add PU/PD resister

48MHz Clock

A1A:(9/26) Add 22ohm for R490 and 10p for C839
Change Y7 from 50MHz to 48MHz

A1A:(9/28) base on EMI suggest: remove R490,C839

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Quanta Computer Inc.

Size	Document Number	Rev
	Card Reader (MR510)	1A

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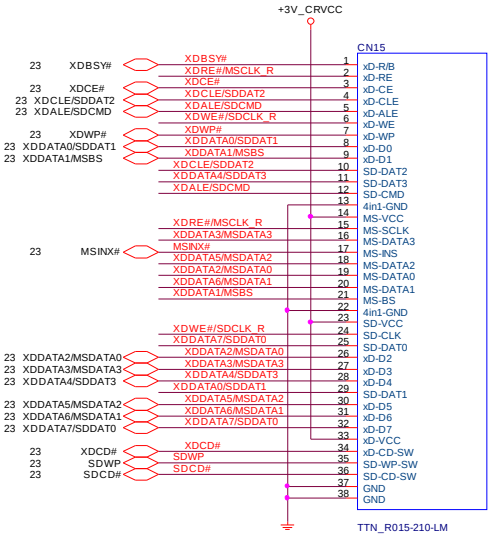
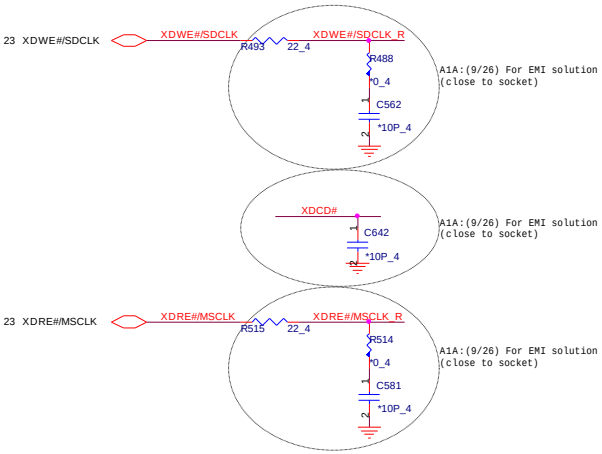
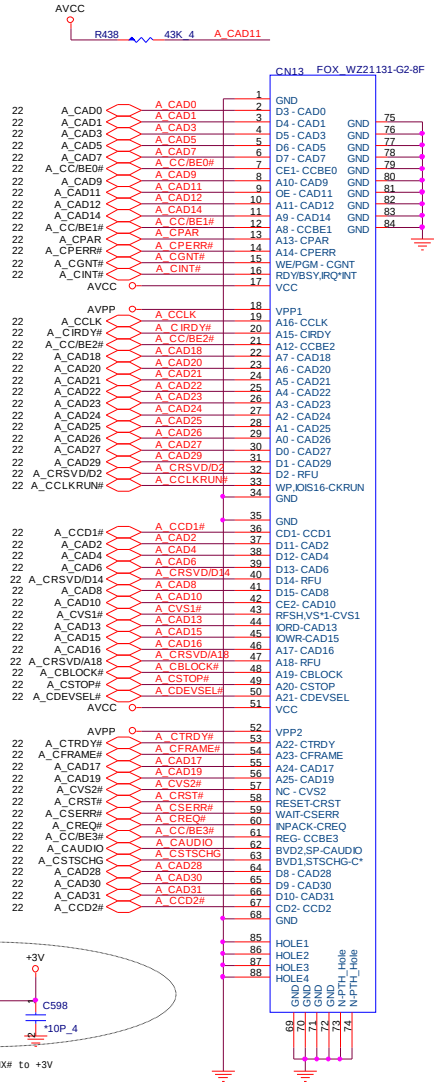
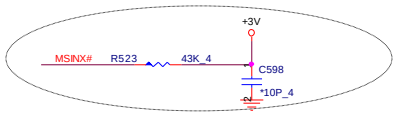
A1A:(9/21) Change CONN (P/N not ready)



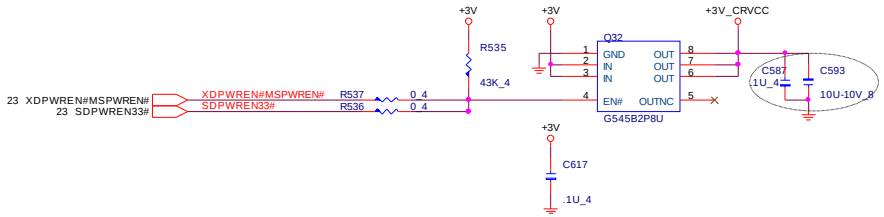




A1A:(9/22) Change PCMCIA CONN (follow BH1)



A1A:(9/26) PU MSINX# to +3V



A1A:(9/26)Change C437 from 0.1u to 10uF
A1A:(9/28)EMI suggest add C484 0.1uF

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	CARD Reader & PCMCIA SLOT	1A

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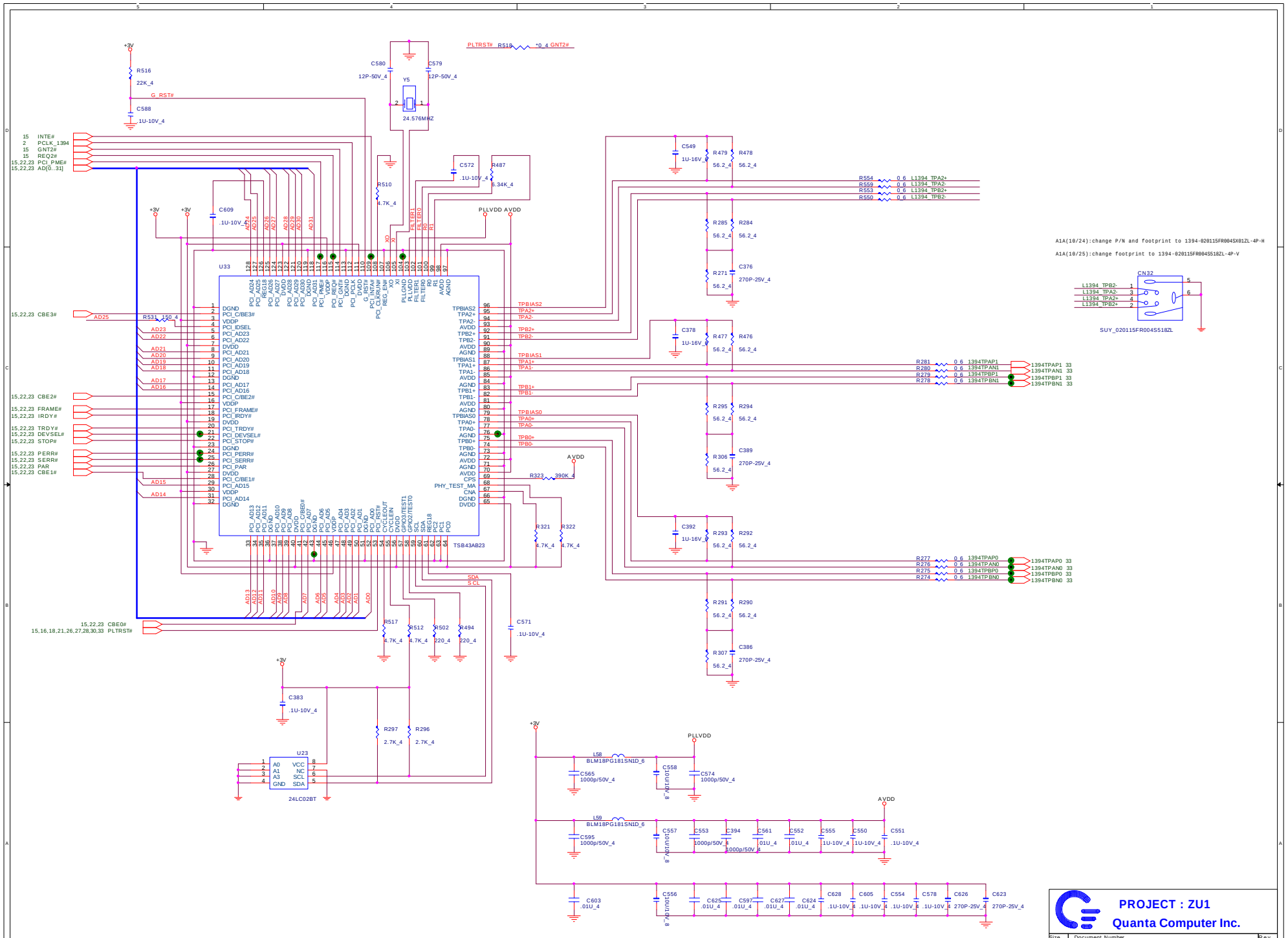
U33
TSB43AB23
U23
24LC02BT
Y5
24.576MHZ
CN32
SUY_020115FR004S518ZL
A1A(10/24):change P/N and footprint to 1394-020115FR004SX012L-4P-H
A1A(10/25):change footprint to 1394-020115FR004S518ZL-4P-V
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
1394(TSB43AB23)
Rev
1A
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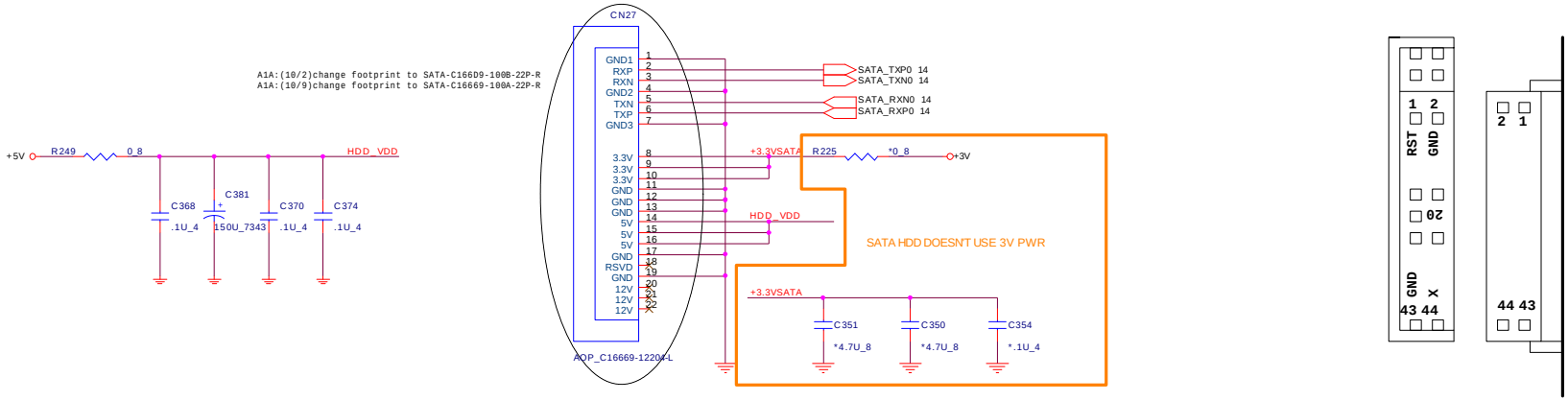
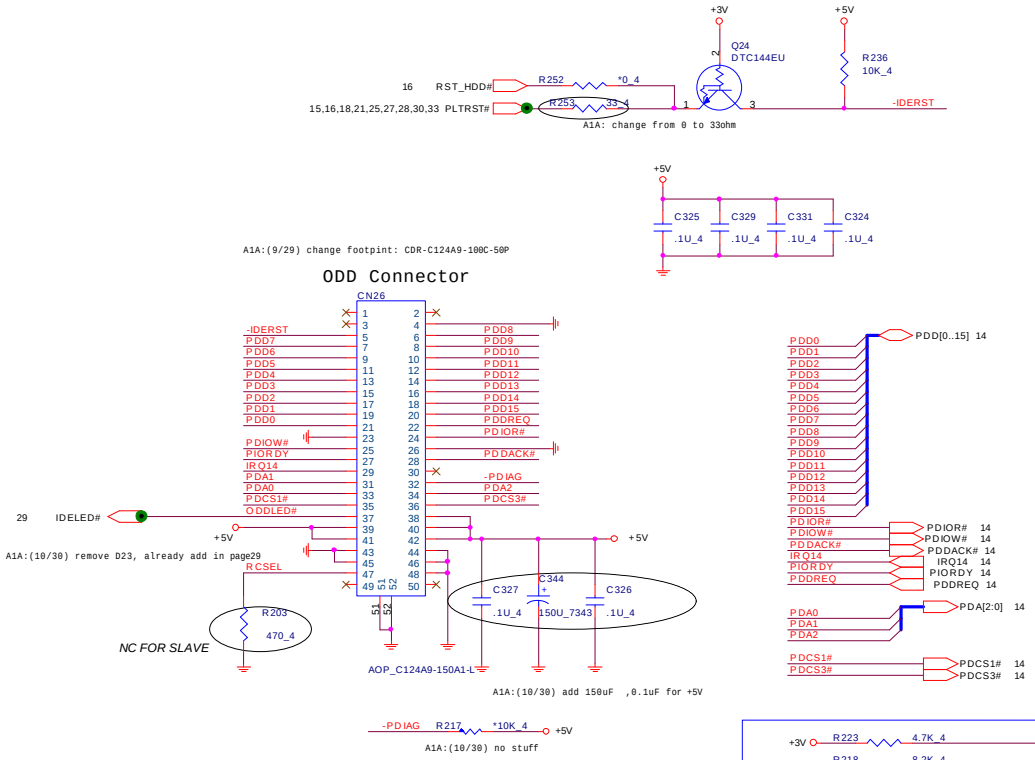
SATA HDD



PATA ODD



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD & PATA-ODD	1A

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MINI-Card

A1A: (9/20) Change from +3V to +3V_WL_VDD
A1A: (10/23)change +3V to +3VSUS

+3VSUS
L28
FBJ3216HS800_1206
+3V_WL_VDD
C398 10U/10V/X5R_8
C413 .1U_4
C414 .1U_4
C419 .1U_4

+1.5V
C402 10U_8
C403 .1U_4
POWER DECOUPLING

A1A:9/4 Reserved for debug only

15,22,23 PCIRST#
2,30 PCI_CLK_SIO
PCIRST# R349 *0_4 CL_DATA1_CN
PCLK_SIO R350 *0_4 CL_CLK1_CN

+1.5V
0_4 R336 +1.5V_MINI-Card
+3V_WL_VDD +3V_WL_VDD
A1A:(10/30)change form +3VSUS to +3V_WL_VDD
C424 10U_8
C422 .1U_4

A1A(10/30): +3V_WL_VDD
Add (CN20/Pin39,41) to
+3V_WL_VDD (follow ZO1)

16 CL_RST#1 R353 0_4 CL_RST#0_CN
16 CL_DATA1 R348 0_4 CL_DATA1_CN
16 CL_CLK1 R356 0_4 CL_CLK1_CN
R354 0_4 KEDRON_GND_43
R351 *0_6 KEDRON_VCC
R355 0_4 KEDRON_GND_37

15 PCIE_TXP4
15 PCIE_TXN4
15 PCIE_RXP4
15 PCIE_RXN4
PCIE_RXP4
PCIE_RXN4
A1A:(10/30) Remove 0.1uF *2pcs
28 uR_SOUT_CR
28 uR_SWD

CN28
ACS_88911-5204

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	GND	USB_D-	36
33	PETp0	GND	34
31	PETn0	SMB_DATA	32
29	GND	SMB_CLK	30
27	GND	+1.5V	28
25	PERp0	GND	26
23	PERn0	+3.3Vaux	24
21	GND	PERST#	22
19	Reserved	Reserved	20
17	Reserved	GND	18
15	GND	Reserved	16
13	REFCLK+	Reserved	14
11	REFCLK-	Reserved	12
9	GND	Reserved	10
7	CLKREQ#	Reserved	8
5	Reserved	+1.5V	6
3	Reserved	GND	4
1	WAKE#	+3.3V	2

A1A: (9/26) Remove (CN20/Pin46)BT_LED
WIRELESS_LED# 29
A1A: (9/20) Remove USB circuit
MINI_DAT_SMB
MINI_CLK_SMB
RF_EN_RR R343 0_4
PLTRST# 15,16,18,21,25,26,28,30,33
RF_EN 28

0_4 R337 LFRAME# 14,28,30
0_4 R338 LAD3 14,28,30
0_4 R340 LAD2 14,28,30
0_4 R339 LAD1 14,28,30
0_4 R339 LAD0 14,28,30

A1A:9/4 Reserved for debug only

+3VSUS 2 CLK_PCIE_MINI1
2 CLK_PCIE_MINI1#

Q25
DTC144EU
R357 4.7K_4
16,18 PCIE_WAKE#
PCIE_WAKE# MINI-Card

+3V
Q14 RHU002N06
R48 10K_4
2,13,16,18,33 PDAT_SMB
MINI_DAT_SMB

+3V
Q15 RHU002N06
R58 10K_4
2,13,16,18,33 PCLK_SMB
MINI_CLK_SMB

BLUETOOTH MODULE CONNECTOR

A1A: (9/25) change CONN (follow ZH3)

Q10
AO3413
+3VSUS
BT_POWER_R
L15
BK2125HS330_8
BT_POWER
C105 10U_8
C101 1000P_4
BT_POWERON# 28

15 USBP4+
15 USBP4-
29 BT_LED
BT_POWER
BT_LED
CN5
ACS_88266-05001-06
A1A:(10/25) SI suggest to remove 22pF*2
C102 .01U_4

USB CONN

+5V_S5
U16
IN1 IN2 OUT3 OUT2 OUT1 EN# GND GND-C OC#
TPS2061DGNR
USBPWR1
28 USBON#
R435 *6.34K_4
C305 .1U_4
C279 100U_3528
C289 1000P_4
CN11
SUY_02013MB0045557ZL
15 USBP0-
15 USBP0+
U15
CM1293-04SO
CH1 CH4 VN VP CH2 CH3
A1A: (9/24)change USB CONN (follow ZC3)
A1A:(10/25) SI suggest to remove 22pF*2

CN21
(B-B) ACS 88028-1210M
15 USBP1-
15 USBP1+
15 USBP2-
15 USBP2+
USBON#
C45 .1U_4

A1A: (10/13) change CONN (follow ZH2 Audio DB)

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Mini card/USB/Bluetooth	1A

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A1A:(9/16)Change from WPC8769 to WPC8763

A1A: (9/25) change VBAT from +3VPCU to +A3VPCU

1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC

1/13 Comfirm by vendor mail:
VBAT for keep PLL let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.

A1A: (9/25) place the above capacitors as close to the pins as possible

08/10 FAE: 0.1UF

A1A: (9/26) Add it. Capacitors as close to EC as possible

A1A: (9/26) Remove TEMP_ABAT

A1A: (9/24) remove ME_EC_ALERT#

A1A:(9/29)SWAP GPIO3 & GPIO6 (follow EC team)

A1A: (9/26) Remove LAN_WOL_EN

A1A: (9/26) Remove RBAYINS#

A1A: (9/26) Remove M/A#

A1A: (9/26) Remove BL/C#

08/10 FAE: SMI DOESN'T NEED DIODE

08/10 FAE: ADD TP FOR DEBUG

CCD_POWERON ACITVE LO => HI

FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.

A1A: (9/26) Remove MY16

A1A: (9/25)
FAE: PUT Y6 with EC in the same side

A1A:(9/27)change C554,C555 from 6.8p to 5.6p

08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.

1/13 Comfirm by vendor mail :
Connect to AGND

8769AGND

A1A: (9/26) Add HWPG_CPUIO

08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.

ZS1 STILL USE BEAD FOR SAFE.

0~AVCC power for DA pin power reference

08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.

SM BUS PU

MBCLK	R98	4.7K_4
MBDATA	R99	4.7K_4
2ND_MBCLK	R102	4.7K_4
2ND_MBDATA	R100	4.7K_4
EC_GPIO42	R139	4.7K_4
CRT_SENSE#	R398	4.7K_4

I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0	CCD_POWERON#	R408	10K_4
BADDR1	SOUT_CR_DEBUG	R407	*10K_4
SHBM	RF_EN	R399	10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ACER ID

A1A:(9/29) change from MBCLK/MNDATA to 2ND_MBCLK/2ND_MBDATA

SPI FLASH

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

BUTTON ON KEYBOARD MATRIX

DEBUG PORTS

A1A(10/5):Change LPC debug CONN to DFFC10FR103

EC Debug Port

Reserved for LPC debug card

INTERNAL KEYBOARD STRIP SET

MY0	R110	10K_4	+3VPCU

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	EC (PC8763LDG)/ FLASH	1A

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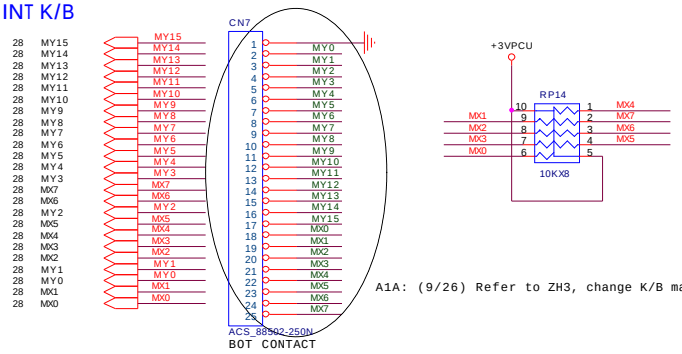
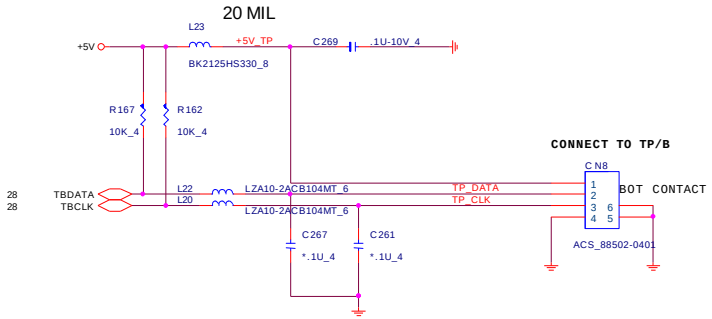
INT K/B



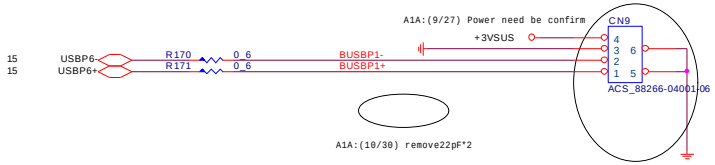
A1A: (9/26) Refer to ZH3, change K/B matrix

uR REQUEST
MY DOES NOT NEED PU.
MY CAN NOT USE EMI BYPASS CAP, DUE TO FLASH.

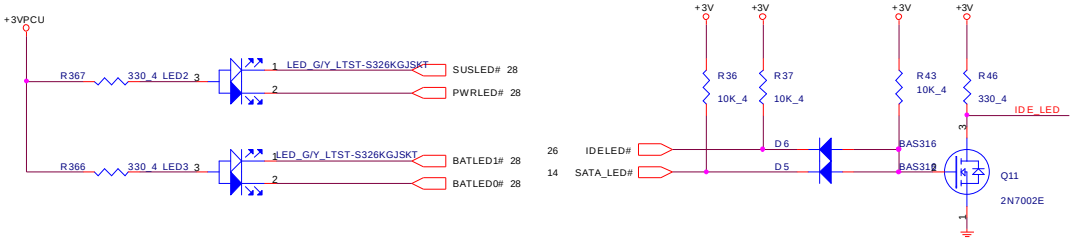
TOUCH PAD

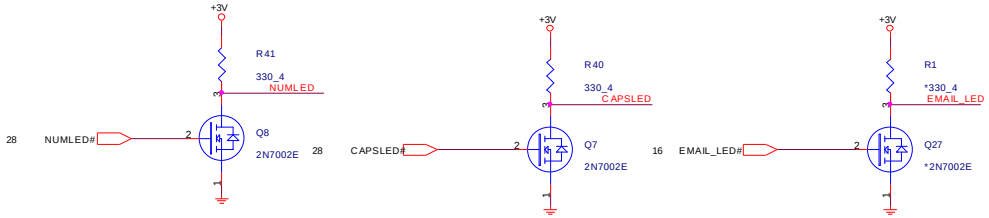


Finger Printer



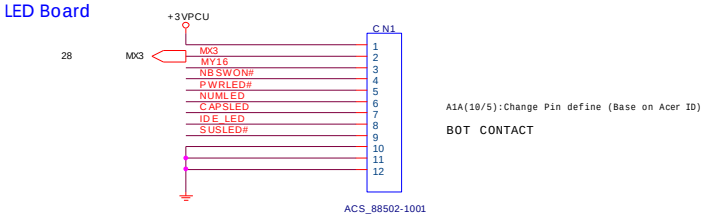
LED





A1A:(10/30) no stuff (ZU1 no support EMAIL LED)

LED Board

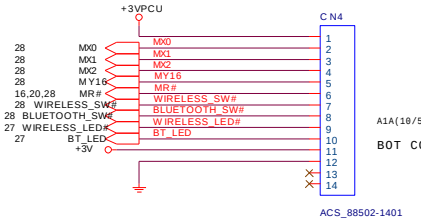


A1A(10/5):Change Pin define (Base on Acer ID)

A1A:(9/27) Add LED Board CONN (10pin)

A1A:(10/26) Add SUSLED#

Function Board



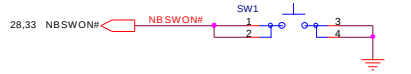
A1A(10/5):Change Pin define (Base on Acer ID)

BOT CONTACT

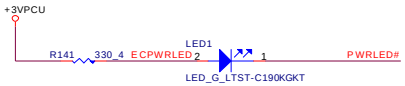
A1A:(9/27) Add Function Board CONN (14pin)

A1A:(10/30) add +3V for Daughter Board use

Keyboard Matrix	Button
MX0/MY16	acer EAP Buttton
MX1/MY16	acer EMAIL Buttton
MX2/MY16	acer WWW Buttton
MX3/MY16	acer EPM Buttton
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button



A1A: (9/24) change SW CONN (follow ZC3)



A1A: (10/30) Reserved LED for debug use

+3VPCU

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	SWITCH,LED,KB,Finger,TP	1A

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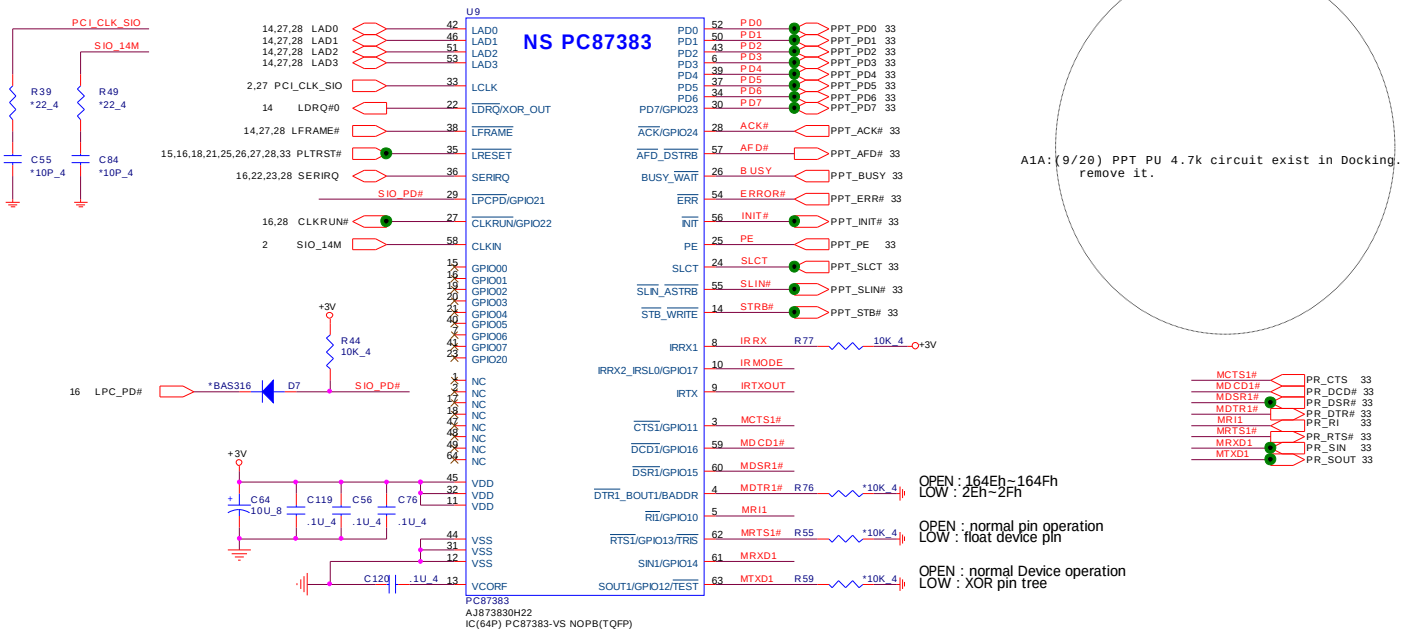
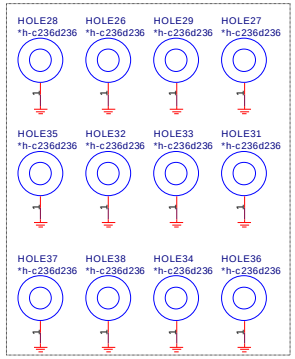
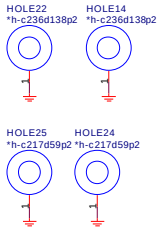
NS SIO PC87383

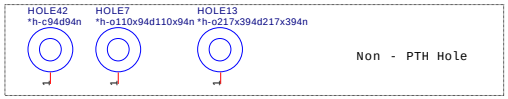


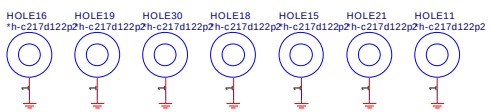
A1A:(9/20) PPT PU 4.7k circuit exist in Docking.
remove it.

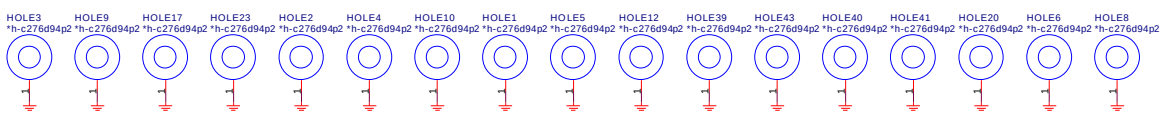
HOLE





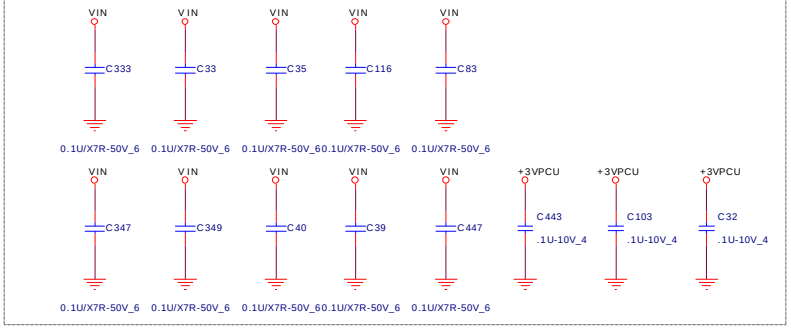




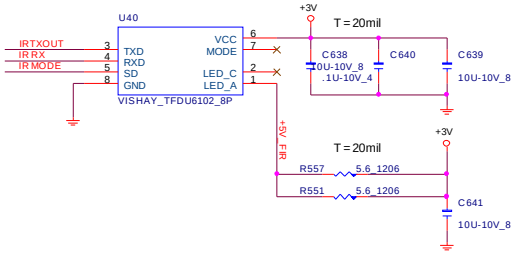


EMI Cap

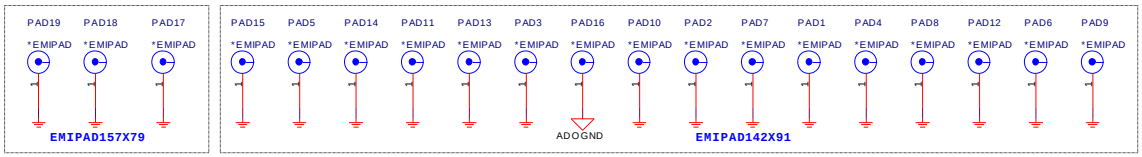
A1A:(10/19) EMI suggest :Add the VIN power shape
bypass cap 0.1uF x 10pcs
Add the +3VPCU power traces bypass cap 0.1uF x 3pcs



FIR



ESDPad



PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	SUPER-IO/FIR/HOLE	1A

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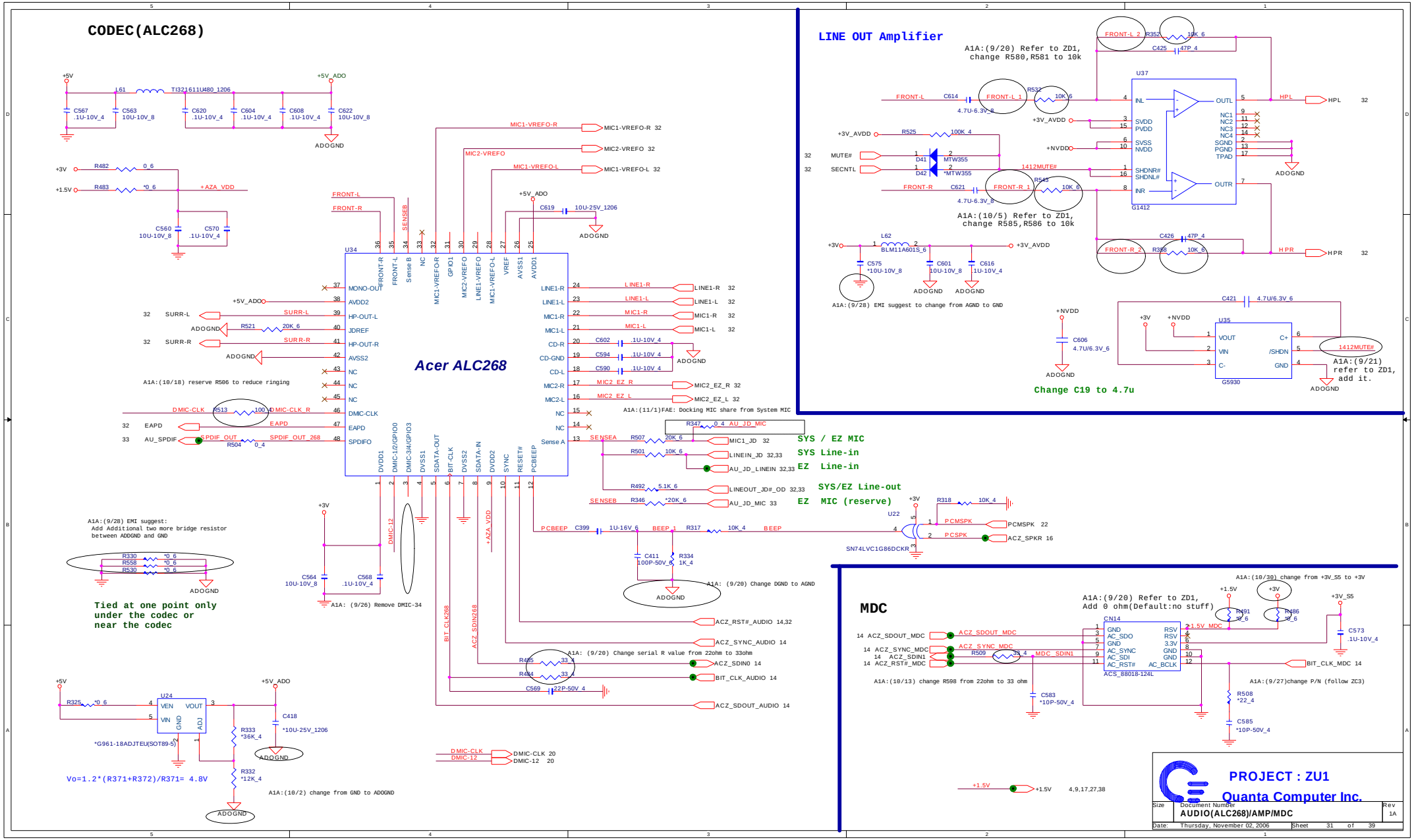
CODEC(ALC268)
Acer ALC268
U34
LINE OUT Amplifier
A1A:(9/20) Refer to ZD1, change R580,R581 to 10k
A1A:(10/5) Refer to ZD1, change R585,R586 to 10k
A1A:(9/28) EMI suggest to change from AGND to GND
Change C19 to 4.7u
A1A:(9/21) refer to ZD1, add it.
U37
G1412
U35
G5930
A1A:(10/18) reserve R506 to reduce ringing
A1A:(11/1)FAE: Docking MIC share from System MIC
SYS / EZ MIC
SYS Line-in
EZ Line-in
SYS/EZ Line-out
EZ MIC (reserve)
U22
SN74LVC1G86DCKR
A1A:(9/28) EMI suggest: Add Additional two more bridge resistor between ADDGND and GND
Tied at one point only under the codec or near the codec
A1A: (9/26) Remove DMIC-34
A1A: (9/20) Change DGND to AGND
A1A: (9/20) Change serial R value from 22ohm to 33ohm
U24
*G961-18ADJTEU(SOT89-5)
Vo=1.2*(R371+R372)/R371= 4.8V
A1A:(10/2) change from GND to ADDGND
MDC
A1A:(10/30) change from +3V_S5 to +3V
A1A:(9/20) Refer to ZD1, Add 0 ohm(Default:no stuff)
CN14
ACS_88018-124L
A1A:(10/13) change R598 from 22ohm to 33 ohm
A1A:(9/27)change P/N (follow ZC3)
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
AUDIO(ALC268)/AMP/MDC
Rev
1A
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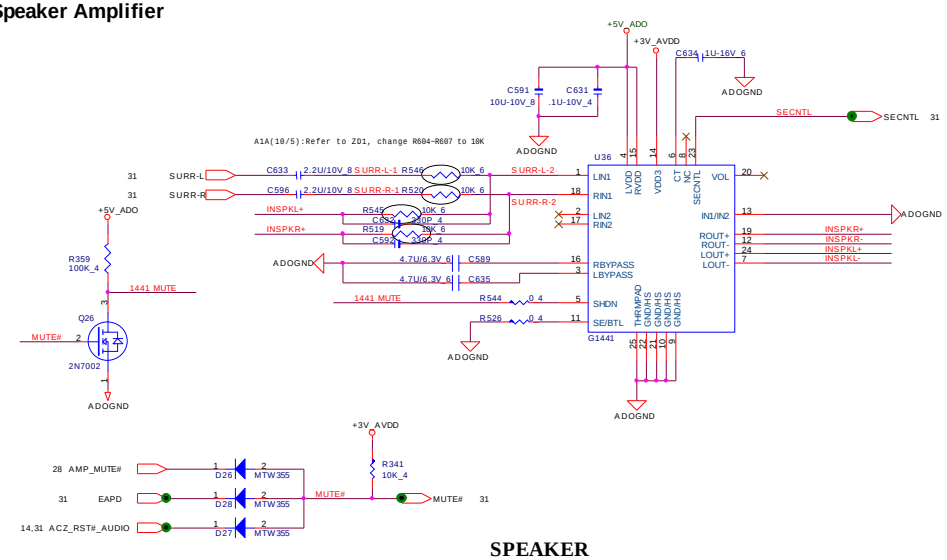
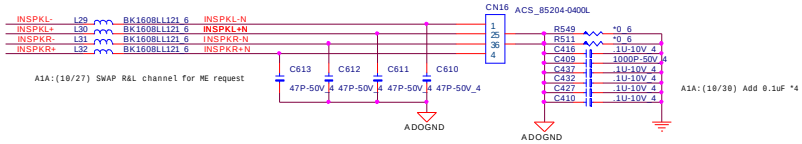
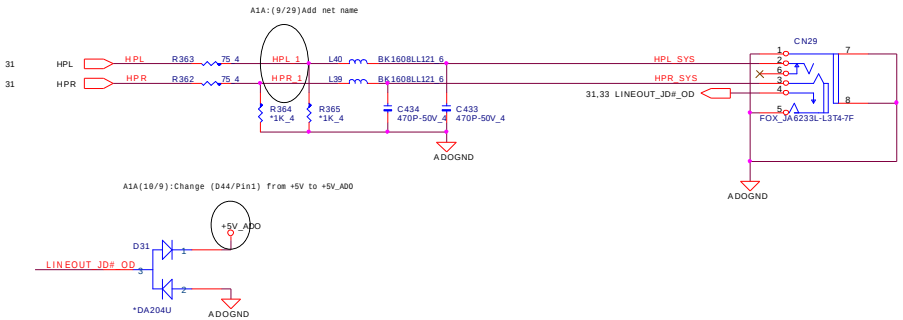
Speaker Amplifier



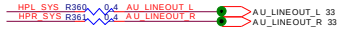
SPEAKER



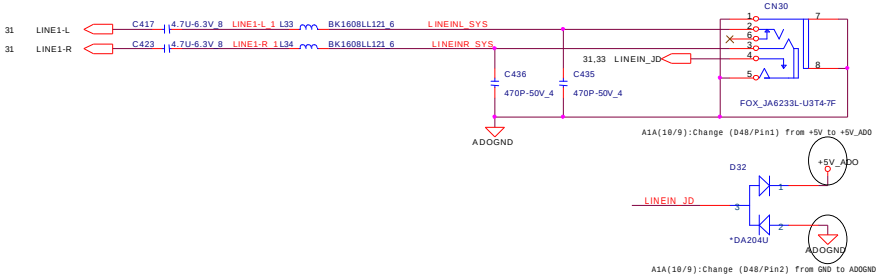
SYSTEM LINE OUT



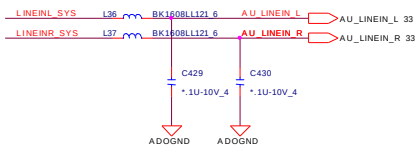
Docking LINE OUT/SPDIF



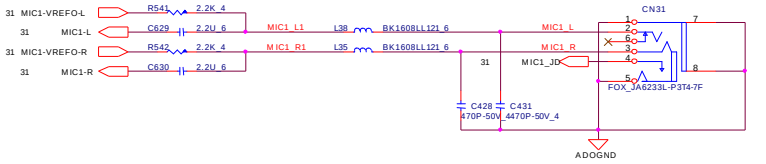
SYSTEM LINE IN



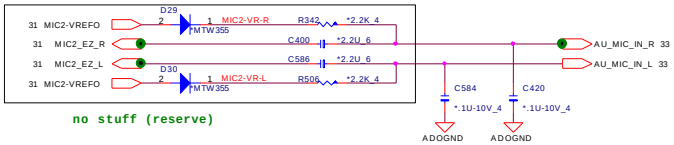
Docking LINE IN



SYSTEM MIC

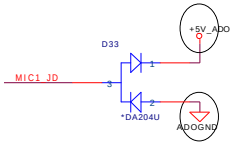


Docking MIC



no stuff (reserve)

A1A:(11/1)FAE: Docking MIC share from System MIC



A1A(10/9):Change (D50/Pin2) from GND to ADOGND

PROJECT : ZU1

Quanta Computer Inc.

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	Speaker AMP / Audio JACK	1A

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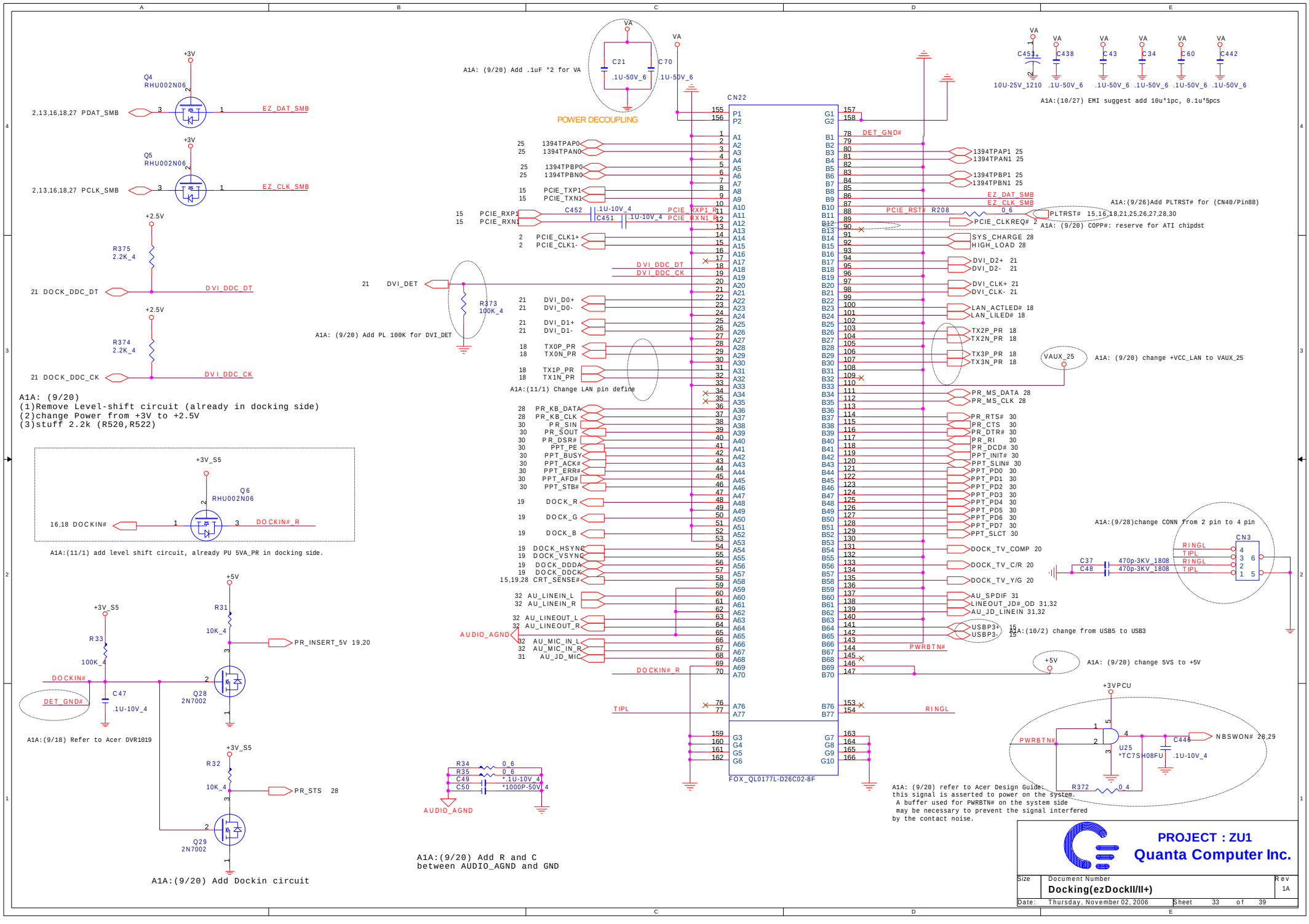
A1A: (9/20) Add .1uF *2 for VA
POWER DECOUPLING
C21 .1U-50V_6
C70 .1U-50V_6
VA
C451 10U-25V_1210
C438 .1U-50V_6
C43 .1U-50V_6
C34 .1U-50V_6
C60 .1U-50V_6
C442 .1U-50V_6
A1A:(10/27) EMI suggest add 10u*1pc, 0.1u*5pcs
Q4 RHU002N06
2,13,16,18,27 PDAT_SMB
EZ_DAT_SMB
Q5 RHU002N06
2,13,16,18,27 PCLK_SMB
EZ_CLK_SMB
+3V
+2.5V
R375 2.2K_4
21 DOCK_DDC_DT
DVI_DDC_DT
R374 2.2K_4
21 DOCK_DDC_CK
DVI_DDC_CK
A1A: (9/20)
(1)Remove Level-shift circuit (already in docking side)
(2)change Power from +3V to +2.5V
(3)stuff 2.2k (R520,R522)
+3V_S5
Q6 RHU002N06
16,18 DOCKIN#
DOCKIN#_R
A1A:(11/1) add level shift circuit, already PU 5VA_PR in docking side.
+5V
R31 10K_4
PR_INSERT_5V 19,20
R33 100K_4
DOCKIN#
DET_GND#
C47 .1U-10V_4
Q28 2N7002
A1A:(9/18) Refer to Acer DVR1019
R32 10K_4
PR_STS 28
Q29 2N7002
A1A:(9/20) Add Dockin circuit
CN22
FOX_QL0177L-D26C02-8F
1394TPAP0
1394TPAN0
1394TPBP0
1394TPBN0
PCIE_TXP1
PCIE_TXN1
PCIE_RXP1
PCIE_RXN1
C452 .1U-10V_4
C451 .1U-10V_4
PCIE_RXP1_R
PCIE_RXN1_R
PCIE_CLK1+
PCIE_CLK1-
DVI_DDC_DT
DVI_DDC_CK
21 DVI_DET
R373 100K_4
A1A: (9/20) Add PL 100K for DVI_DET
DVI_D0+
DVI_D0-
DVI_D1+
DVI_D1-
TX0P_PR
TX0N_PR
TX1P_PR
TX1N_PR
A1A:(11/1) Change LAN pin define
PR_KB_DATA
PR_KB_CLK
PR_SIN
PR_SOUT
PR_DSR#
PPT_PE
PPT_BUSY
PPT_ACK#
PPT_ERR#
PPT_AFD#
PPT_STB#
DOCK_R
DOCK_G
DOCK_B
DOCK_HSYNC
DOCK_VSYNC
DOCK_DDDA
DOCK_DDCK
CRT_SENSE#
AU_LINEIN_L
AU_LINEIN_R
AU_LINEOUT_L
AU_LINEOUT_R
AUDIO_AGND
AU_MIC_IN_L
AU_MIC_IN_R
AU_JD_MIC
DOCKIN#_R
TIPL
RINGL
R34 0_6
R35 0_6
C49 *.1U-10V_4
C50 *1000P-50V_4
AUDIO_AGND
A1A:(9/20) Add R and C between AUDIO_AGND and GND
DET_GND#
PCIE_RST# R208 0_6
PCIE_CLKREQ# 2
A1A:(9/26)Add PLTRST# for (CN40/Pin88)
PLTRST# 15,16,18,21,25,26,27,28,30
A1A: (9/20) COPP#: reserve for ATI chipdst
SYS_CHARGE 28
HIGH_LOAD 28
DVI_D2+ 21
DVI_D2- 21
DVI_CLK+ 21
DVI_CLK- 21
LAN_ACTLED# 18
LAN_LILED# 18
TX2P_PR 18
TX2N_PR 18
TX3P_PR 18
TX3N_PR 18
VAUX_25
A1A: (9/20) change +VCC_LAN to VAUX_25
PR_MS_DATA 28
PR_MS_CLK 28
PR_RTS# 30
PR_CTS 30
PR_DTR# 30
PR_RI 30
PR_DCD# 30
PPT_INIT# 30
PPT_SLIN# 30
PPT_PD0 30
PPT_PD1 30
PPT_PD2 30
PPT_PD3 30
PPT_PD4 30
PPT_PD5 30
PPT_PD6 30
PPT_PD7 30
PPT_SLCT 30
DOCK_TV_COMP 20
DOCK_TV_C/R 20
DOCK_TV_Y/G 20
AU_SPDIF 31
LINEOUT_JD#_OD 31,32
AU_JD_LINEIN 31,32
USBP3+ 15
USBP3- 15
A1A:(10/2) change from USB5 to USB3
PWRBTN#
+5V
A1A: (9/20) change 5VS to +5V
A1A:(9/28)change CONN from 2 pin to 4 pin
CN3
C37 470p-3KV_1808
C48 470p-3KV_1808
RINGL
TIPL
+3VPCU
PWRBTN#
U25 *TC7SH08FU
C446 .1U-10V_4
NBSWON# 28,29
R372 0_4
A1A: (9/20) refer to Acer Design Guide: this signal is asserted to power on the system. A buffer used for PWRBTN# on the system side may be necessary to prevent the signal interfered by the contact noise.
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
Docking(ezDockII/II+)
Rev
1A
Date: Thursday, November 02, 2006
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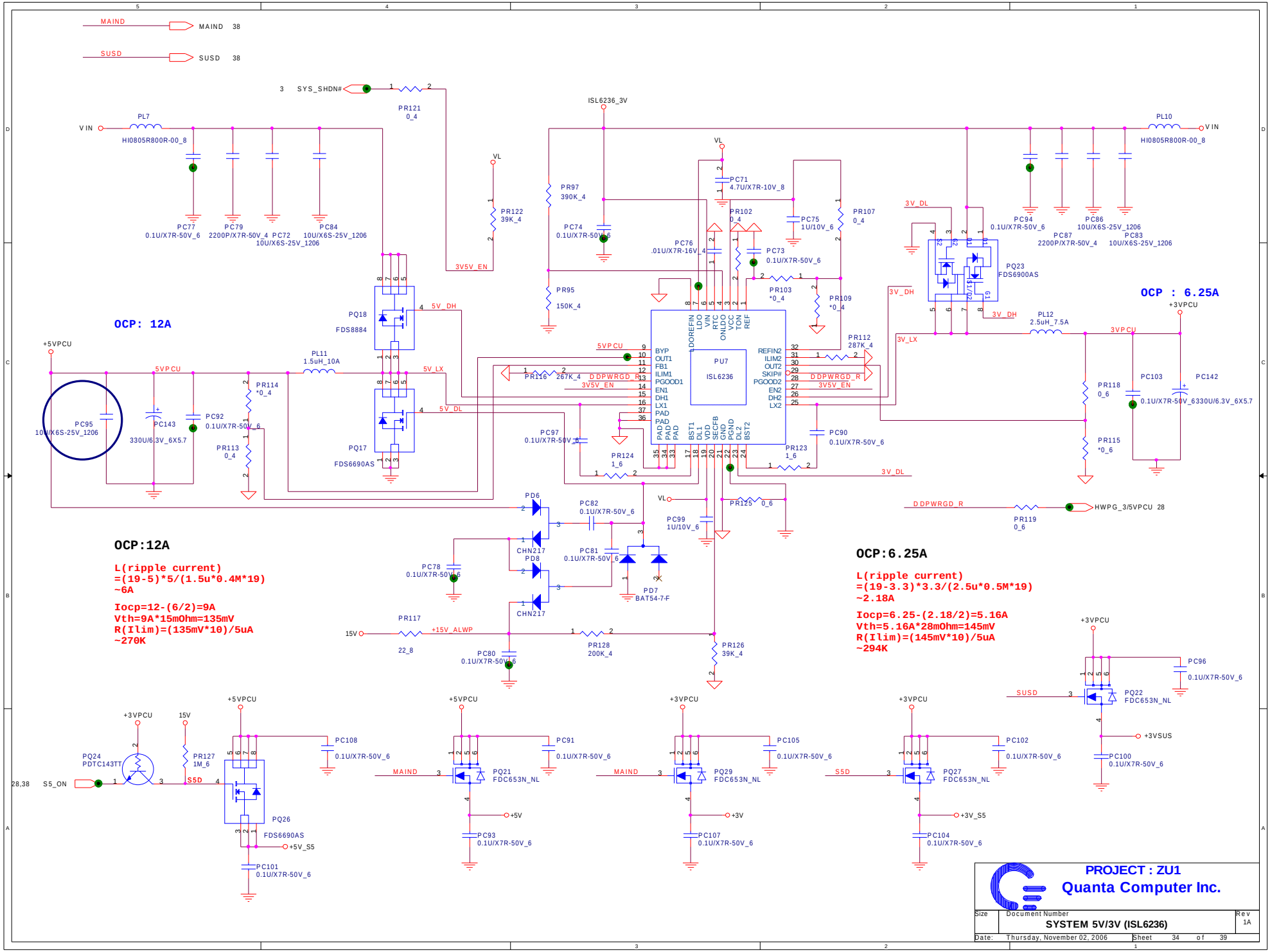
MAIND
MAIND 38
SUSD
SUSD 38
3 SYS_SHDN#
PR121 0_4
VIN
PL7
HI0805R800R-00_8
PC77 0.1U/X7R-50V_6
PC79 2200P/X7R-50V_4
PC72 10U/X6S-25V_1206
PC84 10U/X6S-25V_1206
VL
PR122 39K_4
3V5V_EN
ISL6236_3V
PR97 390K_4
PC74 0.1U/X7R-50V_6
PR95 150K_4
PC71 4.7U/X7R-10V_8
PR102 0_4
PC75 1U/10V_6
PR107 0_4
PC76 .01U/X7R-16V_4
PC73 0.1U/X7R-50V_6
PR103 *0_4
PR109 *0_4
PL10
HI0805R800R-00_8
PC94 0.1U/X7R-50V_6
PC87 2200P/X7R-50V_4
PC86 10U/X6S-25V_1206
PC83 10U/X6S-25V_1206
3V_DL
PQ23 FDS6900AS
3V_DH
3V_LX
PL12 2.5uH_7.5A
OCP : 6.25A
+3VPCU
3VPCU
PR118 0_6
PC103 0.1U/X7R-50V_6330U/6.3V_6X5.7
PC142
PR115 *0_6
OCP: 12A
+5VPCU
5VPCU
PC95 10U/X6S-25V_1206
PC143 330U/6.3V_6X5.7
PC92 0.1U/X7R-50V_6
PR113 0_4
PR114 *0_4
PL11 1.5uH_10A
PQ18 FDS8884
PQ17 FDS6690AS
5V_DH
5V_LX
5V_DL
PU7 ISL6236
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
BST1
DL1
VDD
SECFB
GND
PGND
DL2
BST2
LDOREFIN
LDO
VIN
RTC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR116 267K_4
DDPWRGD_R
3V5V_EN
PR112 287K_4
PC97 0.1U/X7R-50V_6
PR124 1_6
PC90 0.1U/X7R-50V_6
PR123 1_6
PR125 0_6
PC99 1U/10V_6
PD6
PD8
CHN217
PC82 0.1U/X7R-50V_6
PC81 0.1U/X7R-50V_6
PC78 0.1U/X7R-50V_6
PD7 BAT54-7-F
PR119 0_6
HWPG_3/5VPCU 28
OCP:12A
L(ripple current)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp=12-(6/2)=9A
Vth=9A*15mOhm=135mV
R(Ilim)=(135mV*10)/5uA
~270K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
15V
PR117 22_8
+15V_ALWP
PC80 0.1U/X7R-50V_6
PR128 200K_4
PR126 39K_4
PC96 0.1U/X7R-50V_6
PQ22 FDC653N_NL
+3VSUS
PC100 0.1U/X7R-50V_6
PQ24 PDTC143TT
PR127 1M_6
28,38 S5_ON
S5D
PQ26 FDS6690AS
+5V_S5
PC101 0.1U/X7R-50V_6
PC108 0.1U/X7R-50V_6
PC91 0.1U/X7R-50V_6
PQ21 FDC653N_NL
+5V
PC93 0.1U/X7R-50V_6
PC105 0.1U/X7R-50V_6
PQ29 FDC653N_NL
+3V
PC107 0.1U/X7R-50V_6
PC102 0.1U/X7R-50V_6
PQ27 FDC653N_NL
+3V_S5
PC104 0.1U/X7R-50V_6
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (ISL6236)
Rev 1A
Date: Thursday, November 02, 2006
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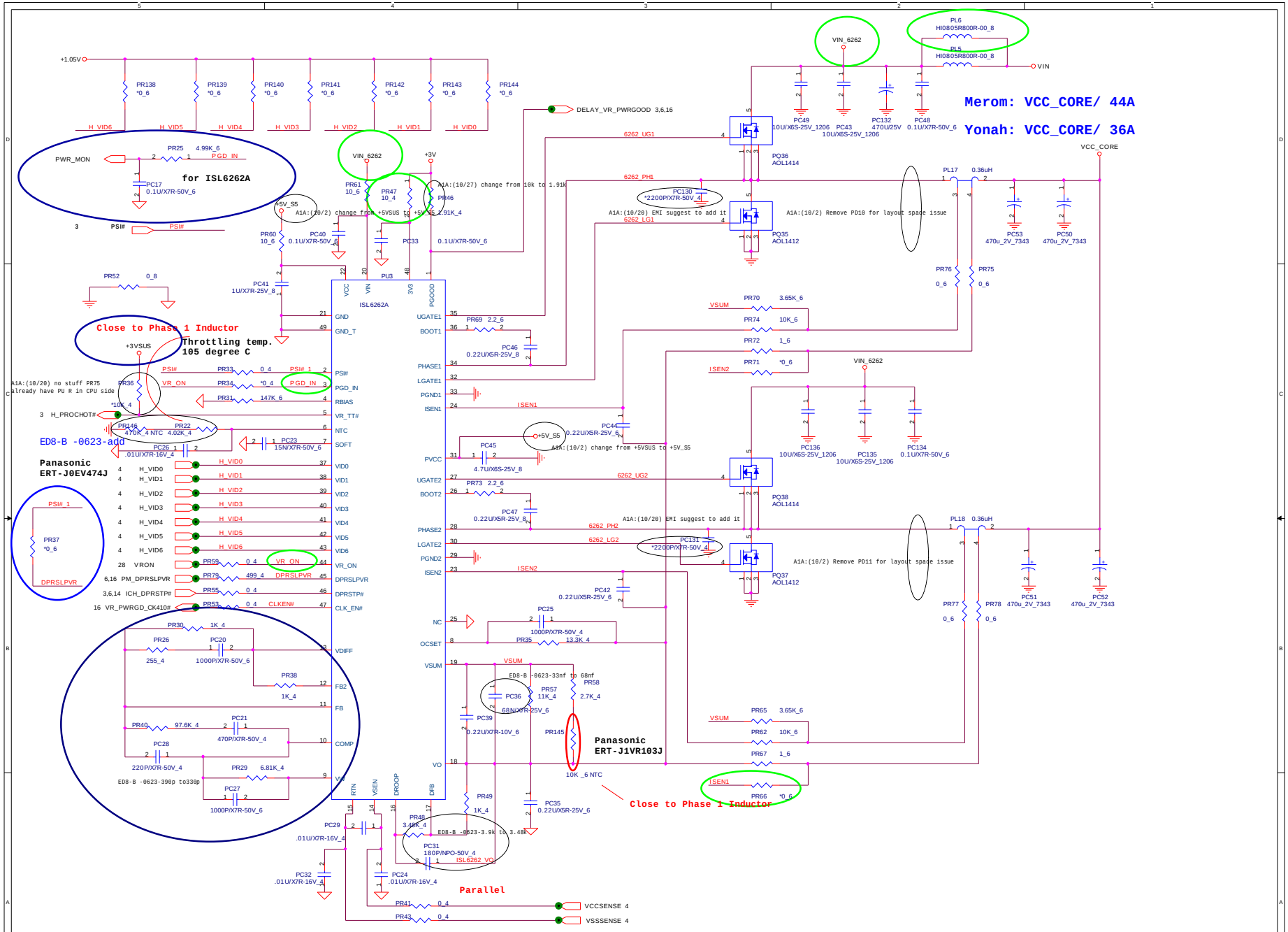
Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
ED8-B -0623-add
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
ISL6262A
VCC_CORE
VIN
VIN_6262
DELAY_VR_PWRGOOD 3,6,16
PWR_MON
PSI#
VR_ON
PGD_IN
H_PROCHOT#
VCCSENSE 4
VSSSENSE 4
PROJECT : ZU1
Quanta Computer Inc.
Size Custom
Document Number
CPU Core (ISL6262A)
Rev 1A
Date: Thursday, November 02, 2006
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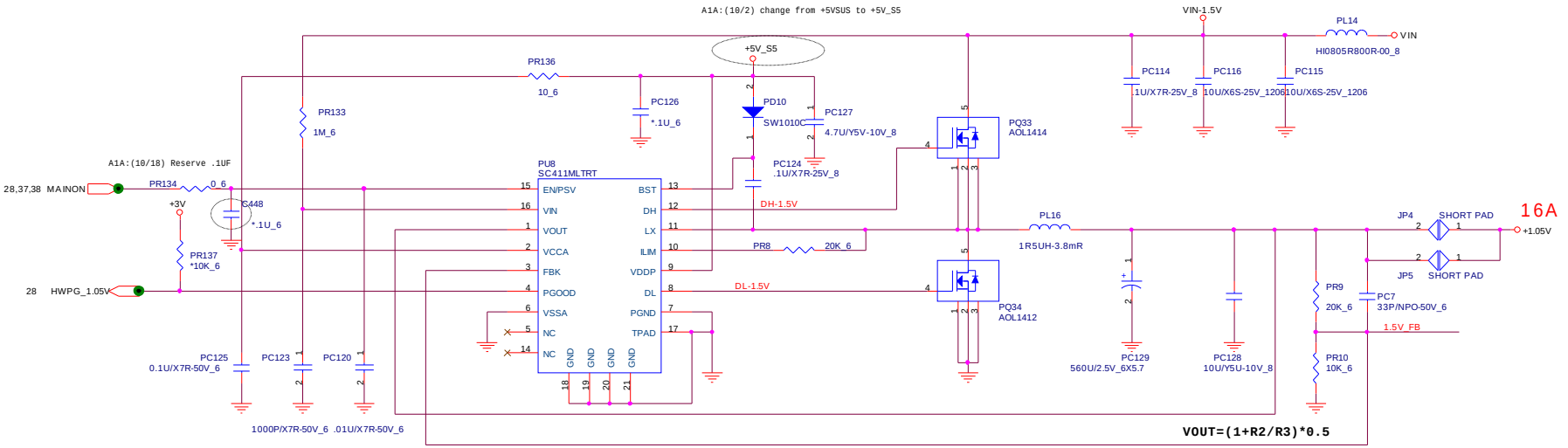

PROJECT : ZU1

Quanta Computer Inc.

Size	Document Number	Rev
	VTT 1.05V (SC411)	1A

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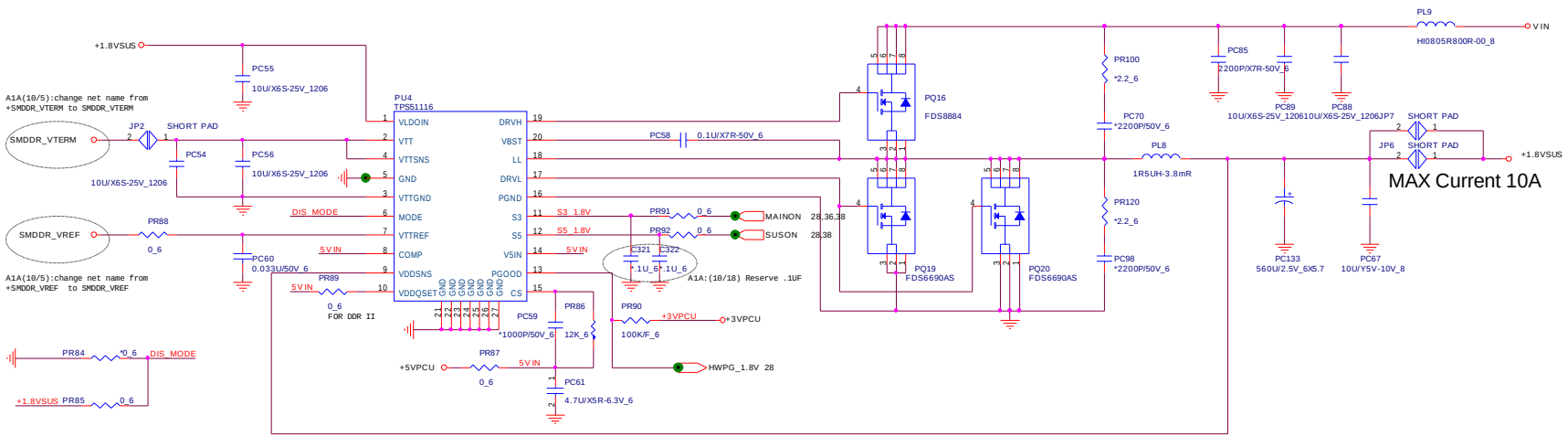

A1A(10/5):Remove +1.8V circuit

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A

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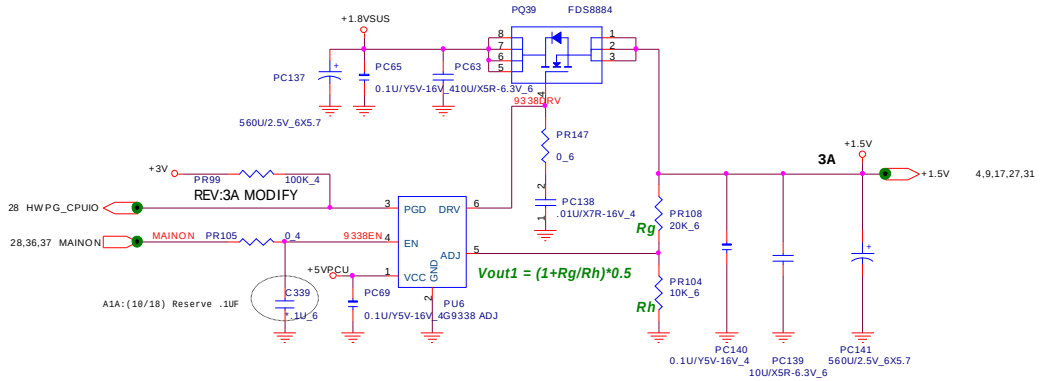

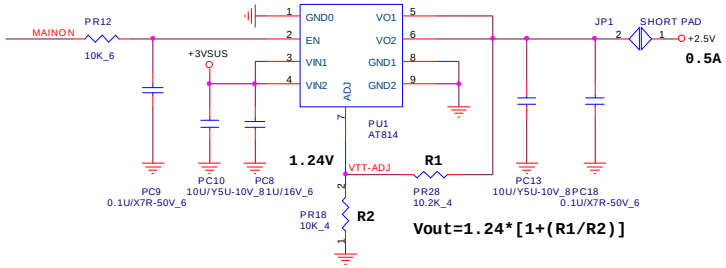

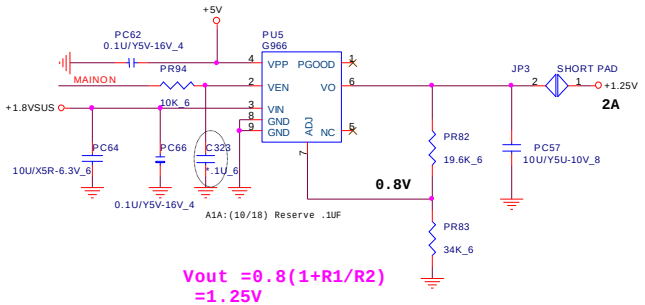

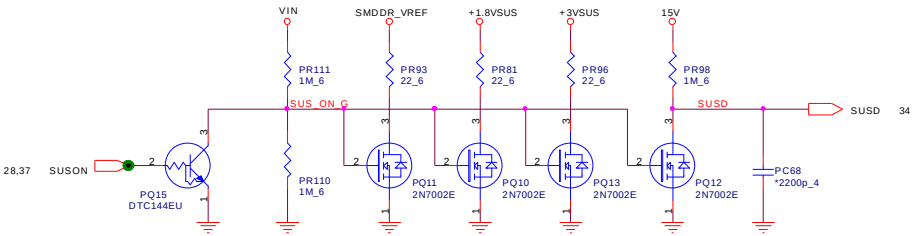

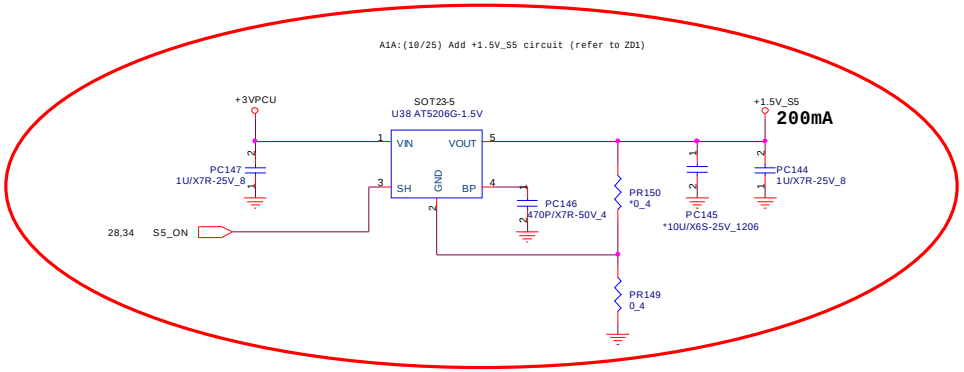

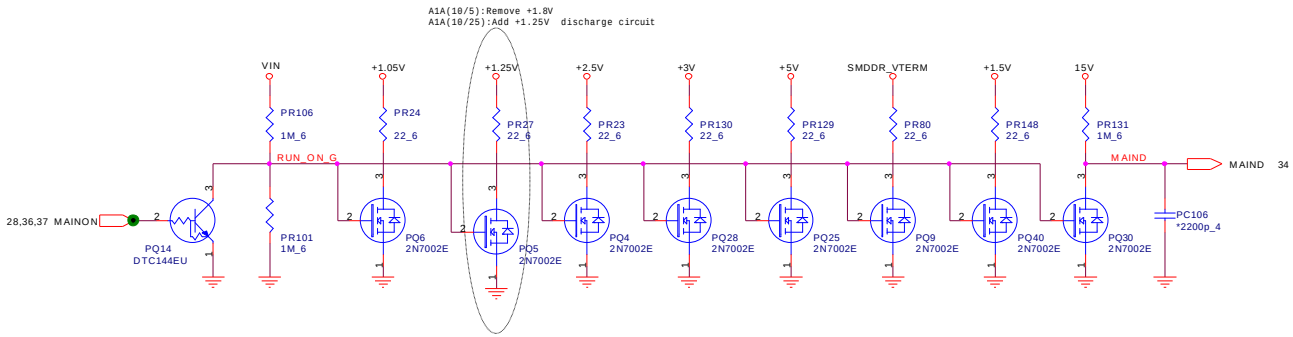

PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	1A

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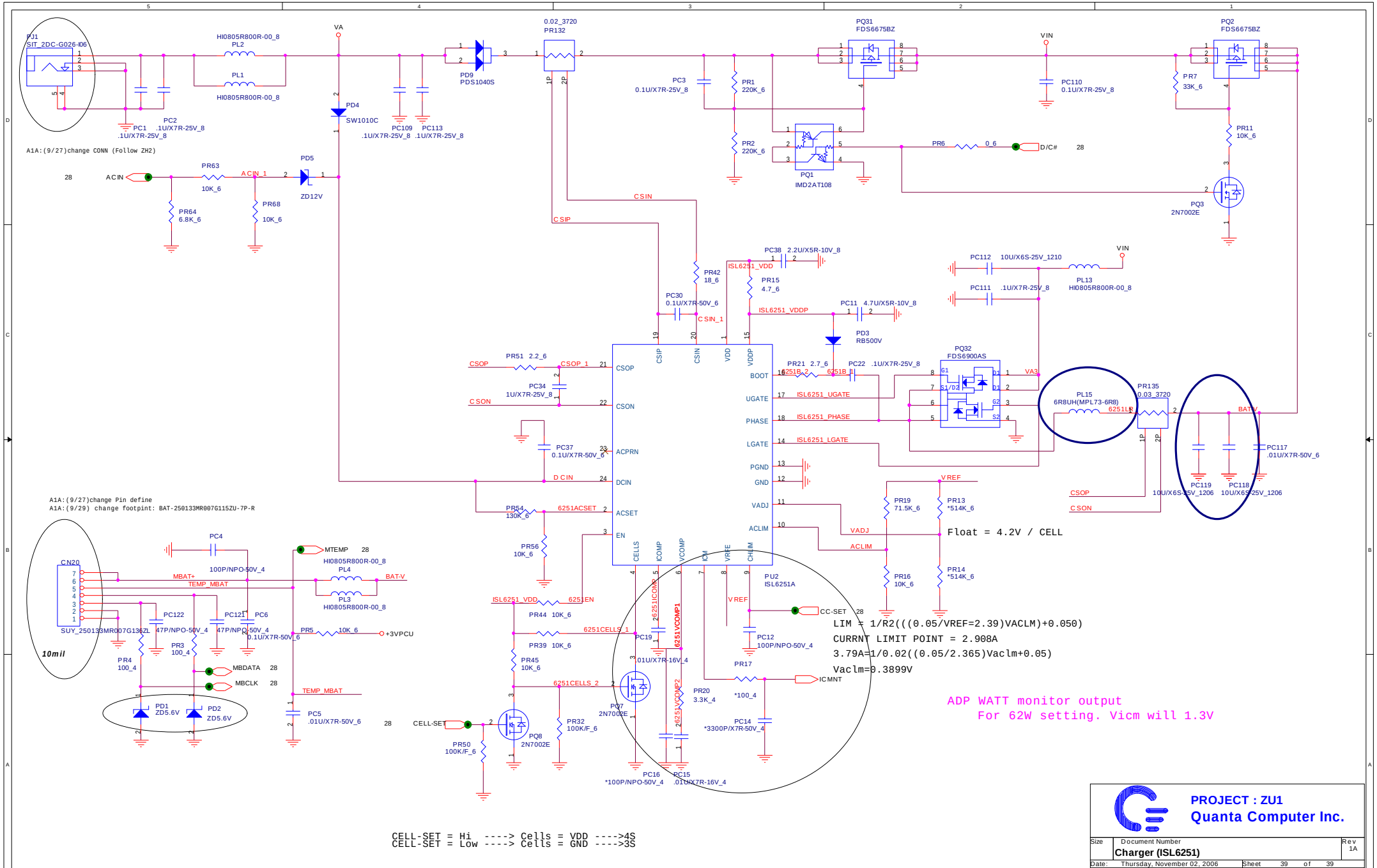
FJ1
SIT_2DC-G026-I06
HI0805R800R-00_8
PL2
PL1
HI0805R800R-00_8
PC1 .1U/X7R-25V_8
PC2 .1U/X7R-25V_8
VA
PD4
SW1010C
PC109 .1U/X7R-25V_8
PC113 .1U/X7R-25V_8
PD9
PDS1040S
0.02_3720
PR132
PC3 0.1U/X7R-25V_8
PR1 220K_6
PR2 220K_6
PQ31
FDS6675BZ
PQ1
IMD2AT108
VIN
PC110 0.1U/X7R-25V_8
PQ2
FDS6675BZ
PR7 33K_6
PR11 10K_6
PR6 0_6
D/C#
28
PQ3
2N7002E
A1A:(9/27)change CONN (Follow ZH2)
ACIN
PR63 10K_6
ACIN_1
PD5
ZD12V
PR64 6.8K_6
PR68 10K_6
CSIN
CSIP
PC38 2.2U/X5R-10V_8
ISL6251_VDD
PR42 18_6
PR15 4.7_6
PC30 0.1U/X7R-50V_6
CSIN_1
ISL6251_VDDP
PC11 4.7U/X5R-10V_8
PD3
RB500V
PC112 10U/X6S-25V_1210
PC111 .1U/X7R-25V_8
PL13
HI0805R800R-00_8
PQ32
FDS6900AS
PR51 2.2_6
CSOP_1
CSOP
PC34 1U/X7R-25V_8
CSON
PC37 0.1U/X7R-50V_6
DCIN
PR21 2.7_6
PC22 .1U/X7R-25V_8
6251B_2
6251B_1
VA3
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PL15
6R8UH(MPL73-6R8)
PR135
0.03_3720
BAT-V
PC117 .01U/X7R-50V_6
PC119 10U/X6S-25V_1206
PC118 10U/X6S-25V_1206
CSOP
CSON
PR54 130K_6
6251ACSET
PR56 10K_6
VREF
PR19 71.5K_6
PR13 *514K_6
Float = 4.2V / CELL
VADJ
ACLIM
PR16 10K_6
PR14 *514K_6
A1A:(9/27)change Pin define
A1A:(9/29) change footprint: BAT-250133MR007G115ZU-7P-R
CN20
SUY_250133MR007G136ZL
10mil
PC4 100P/NPO-50V_4
MTEMP
28
HI0805R800R-00_8
PL4
PL3
HI0805R800R-00_8
MBAT+
TEMP_MBAT
BAT-V
PC122 47P/NPO-50V_4
PC121 47P/NPO-50V_4
PC6 0.1U/X7R-50V_6
PR3 100_4
PR4 100_4
PR5 10K_6
+3VPCU
MBDATA
MBCLK
PD1 ZD5.6V
PD2 ZD5.6V
PC5 .01U/X7R-50V_6
ISL6251_VDD
6251EN
PR44 10K_6
6251CELLS_1
PR39 10K_6
PR45 10K_6
6251CELLS_2
PC19 .01U/X7R-16V_4
PQ7 2N7002E
PR32 100K/F_6
PQ8 2N7002E
CELL-SET
PR50 100K/F_6
PC16 *100P/NPO-50V_4
PC15 .01U/X7R-16V_4
6251ICOMP
6251VCOMP1
6251VCOMP2
PR20 3.3K_4
PU2
ISL6251A
CC-SET
PC12 100P/NPO-50V_4
PR17 *100_4
ICMNT
PC14 *3300P/X7R-50V_4
LIM = 1/R2(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT = 2.908A
3.79A=1/0.02((0.05/2.365)Vaclm+0.05)
Vaclm=0.3899V
ADP WATT monitor output
For 62W setting. Vicm will 1.3V
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
PROJECT : ZU1
Quanta Computer Inc.
Size
Document Number
Charger (ISL6251)
Rev 1A
Date: Thursday, November 02, 2006
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