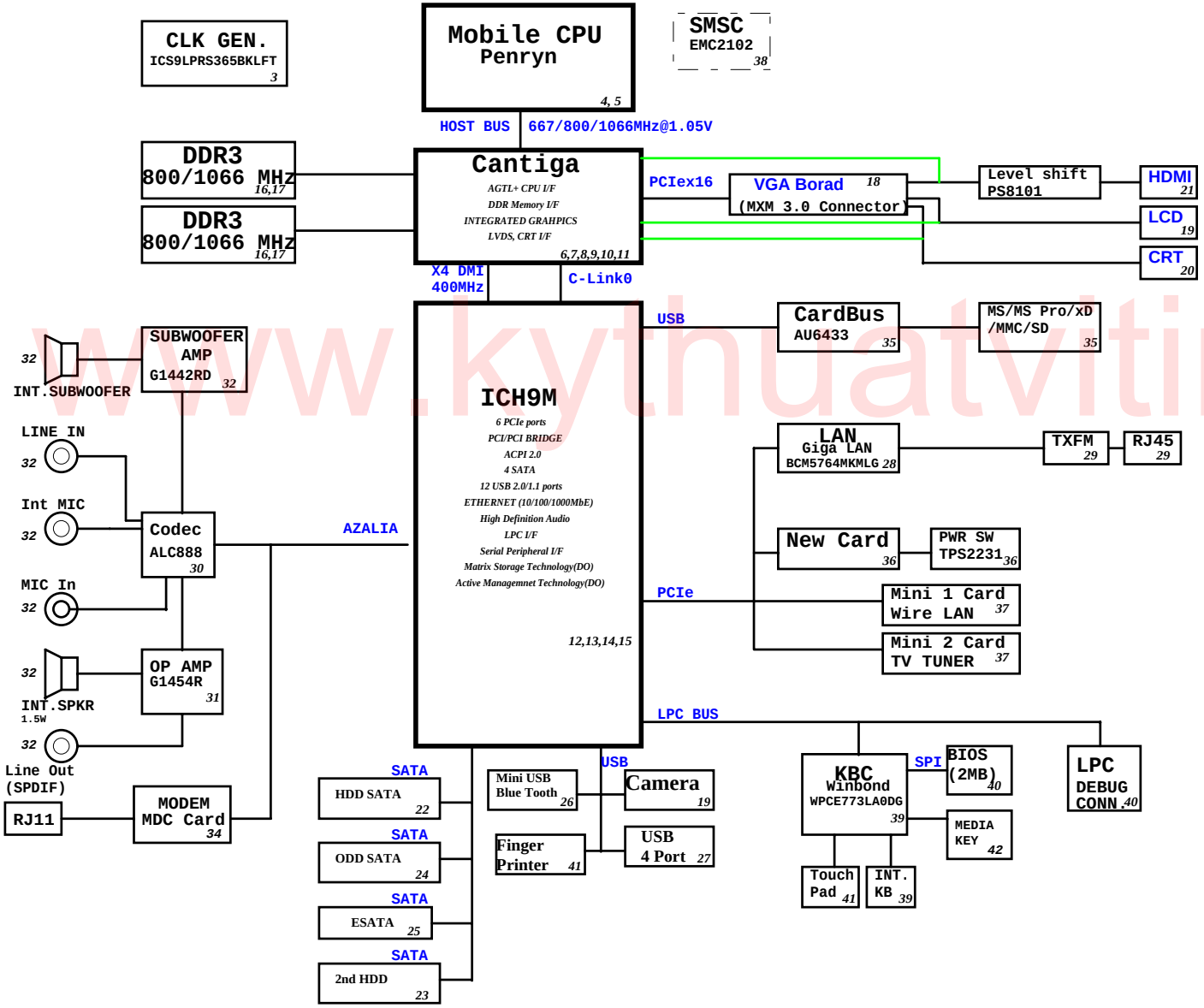
Project code: 91.4AN01.001
PCB P/N : 48.4AN01.0SA
REVISION : SB 08246

JM70 -MV Block Diagram



SYSTEM DC/DC ISL62392 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 46	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)
RT9026 49	
1.5V_S3	DDR_VREF_S3 (1.2A)
G9198-15 14	
3D3V_S5	1D5V_S5 (300mA)

CHARGER ISL88731A 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3208C 51	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

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Title: BLOCK DIAGRAM
Size: A2 | Document Number: JM70-MV | Rev: SB
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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Size: A3 | Document Number: JM70-MV | Rev: SB

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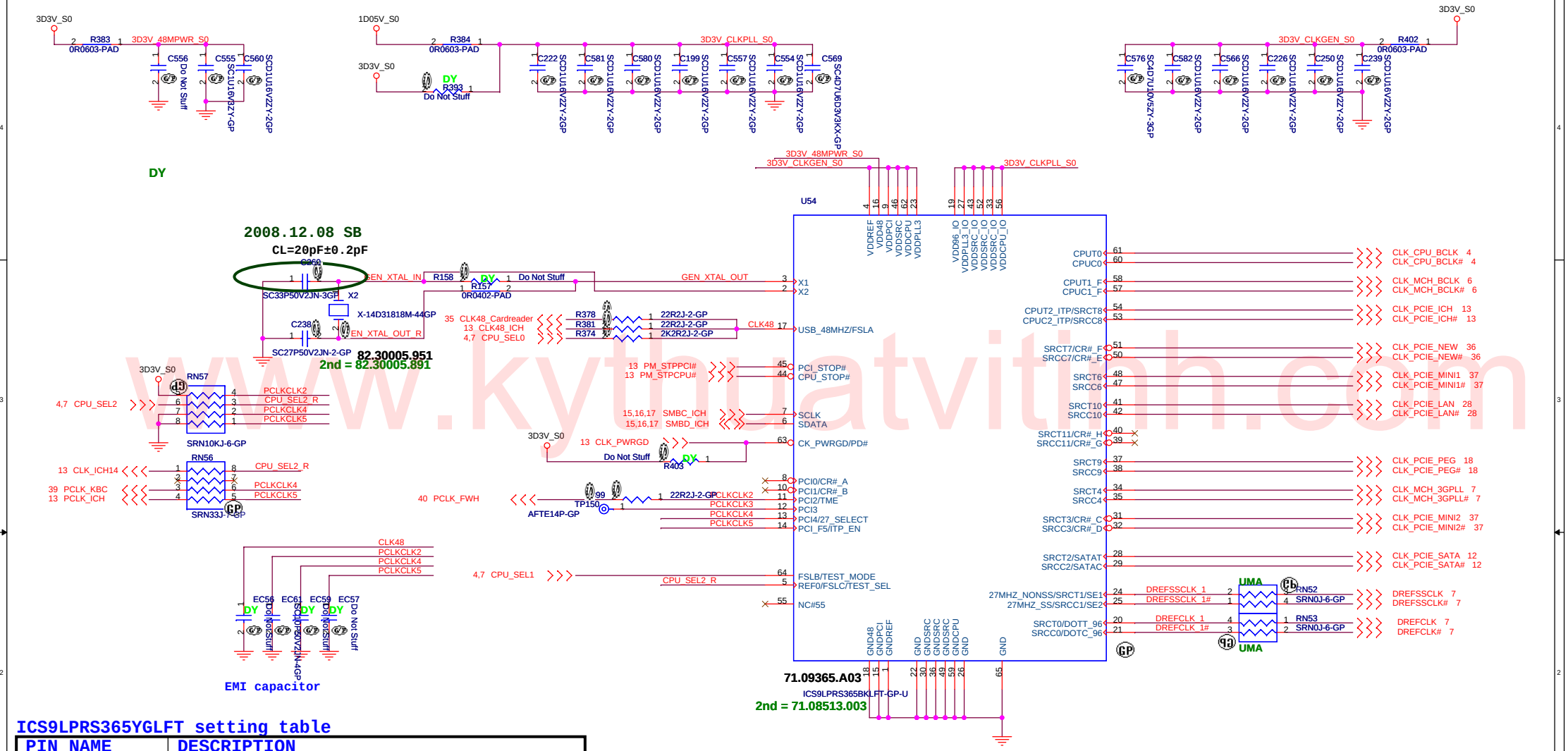

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ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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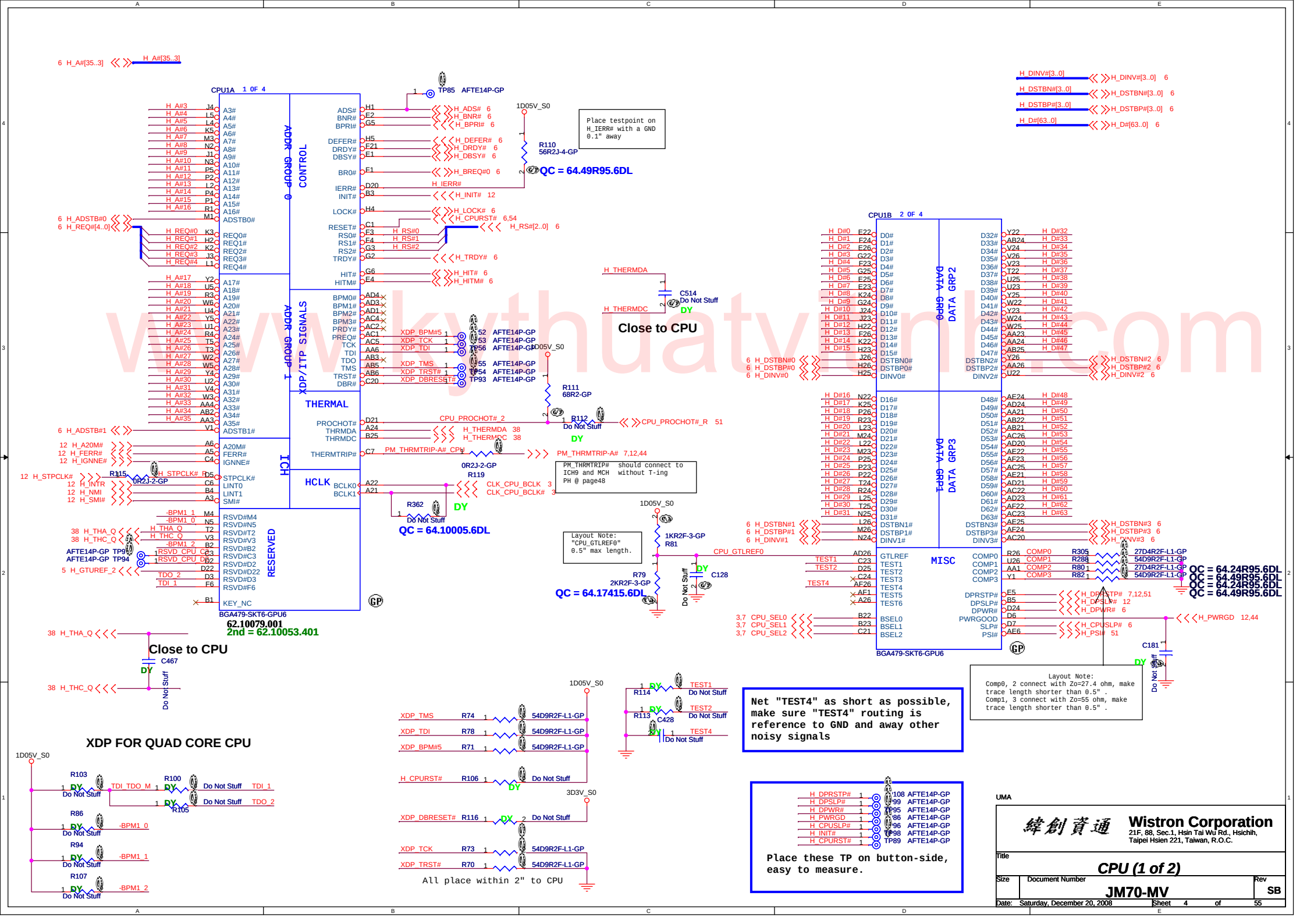

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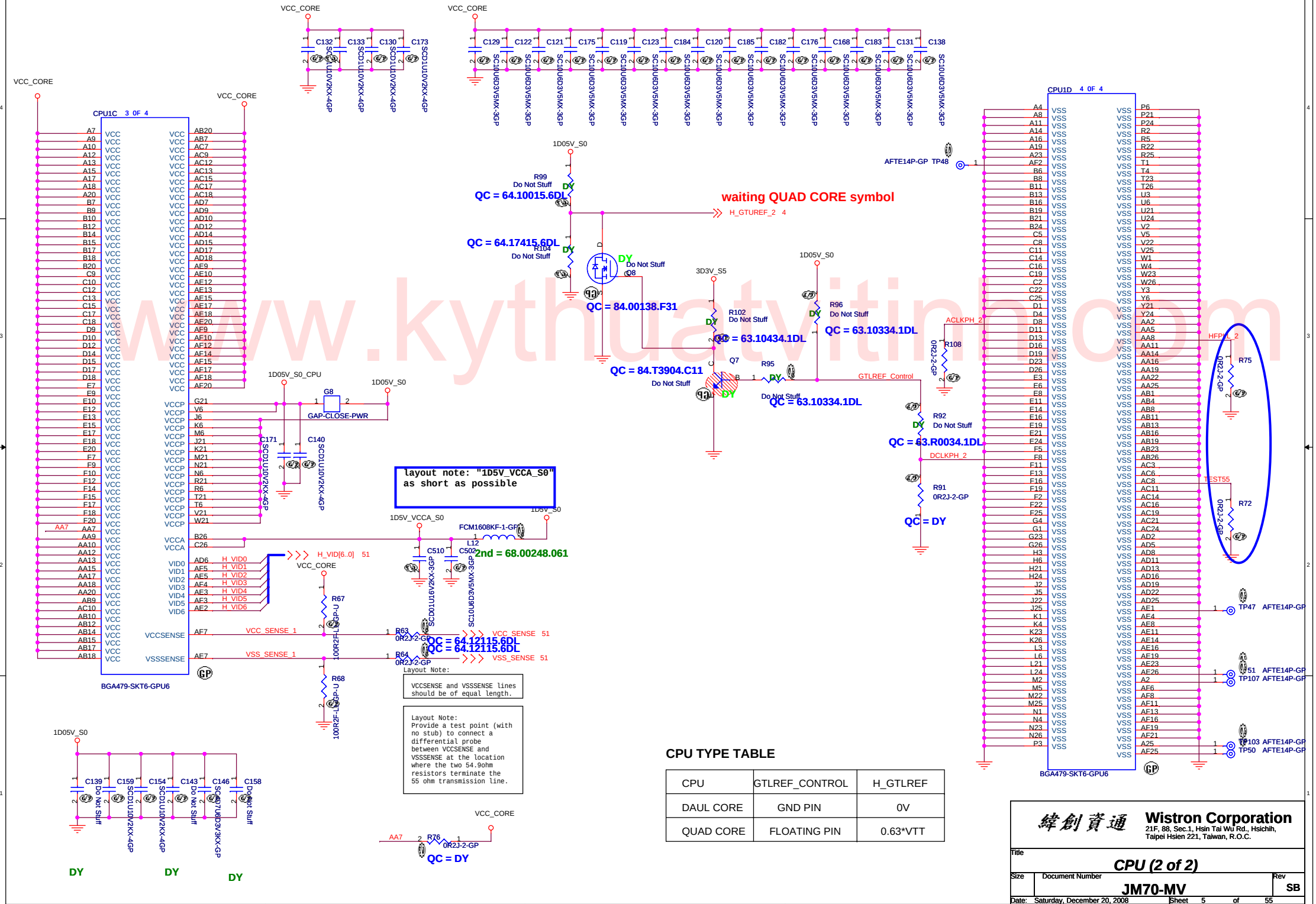

CPU TYPE TABLE

CPU	GTLREF_CONTROL	H_GTLREF
DAUL CORE	GND PIN	0V
QUAD CORE	FLOATING PIN	0.63*VTT

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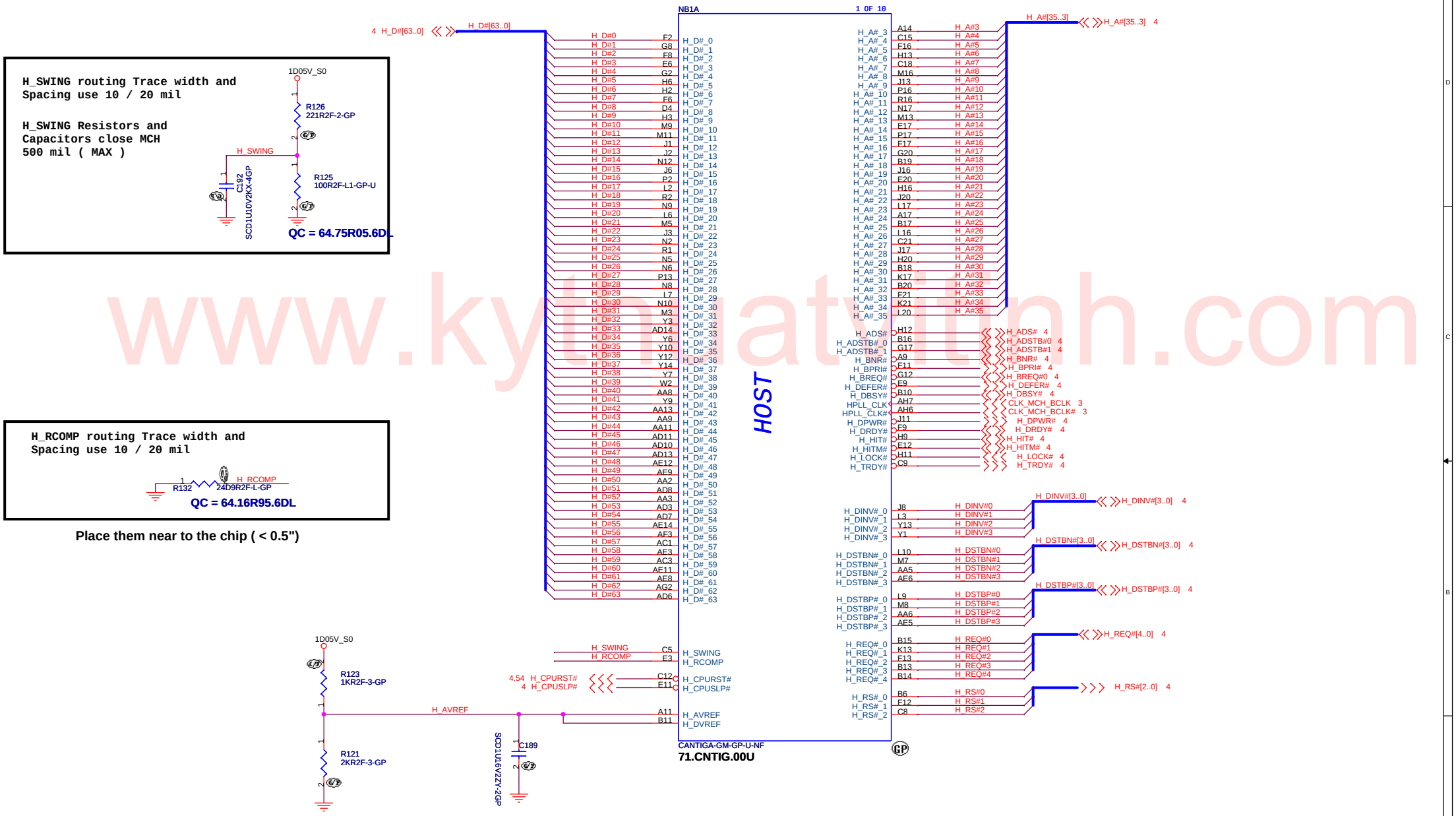

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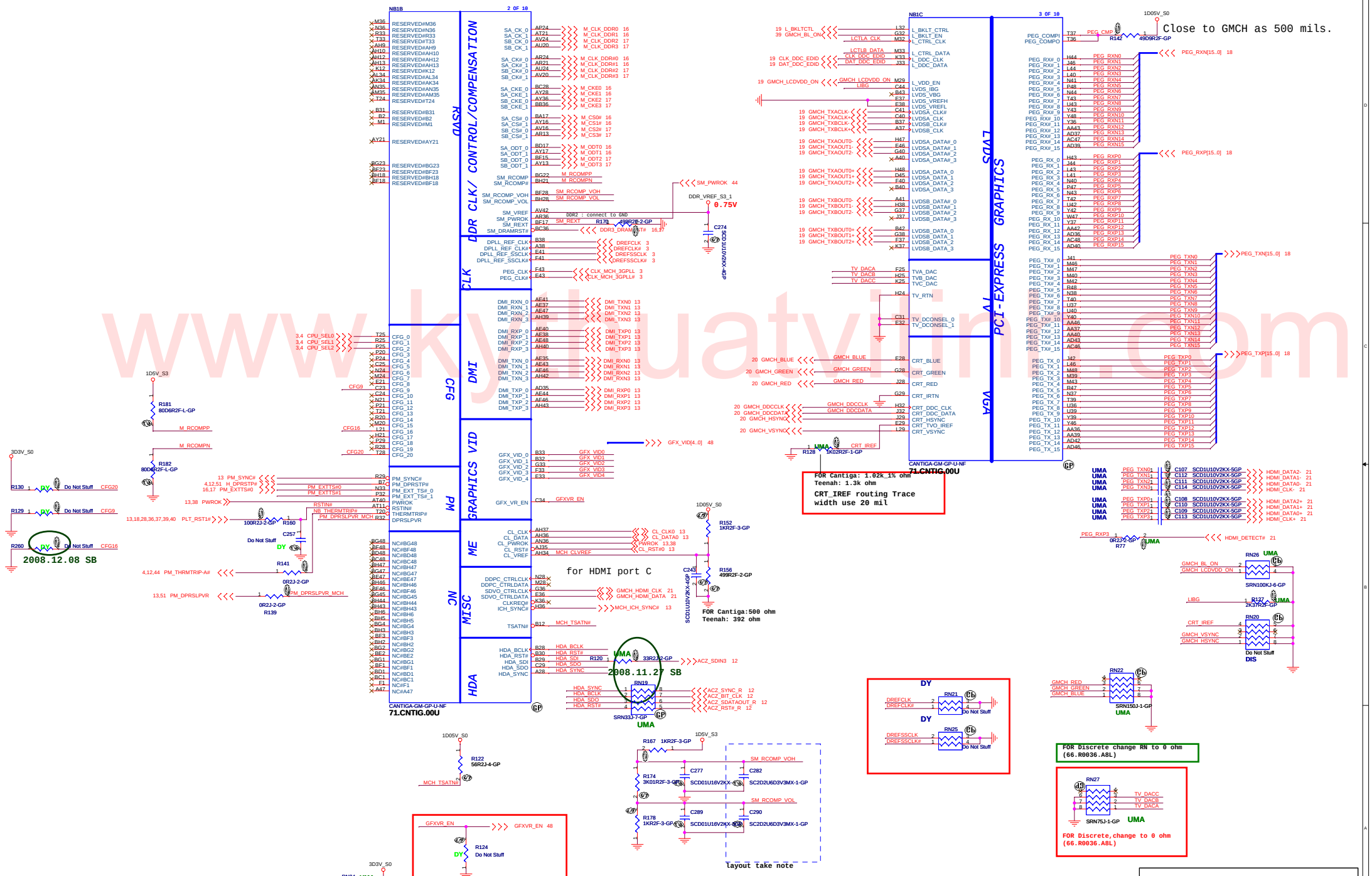

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Title	Cantiga (2 of 6)
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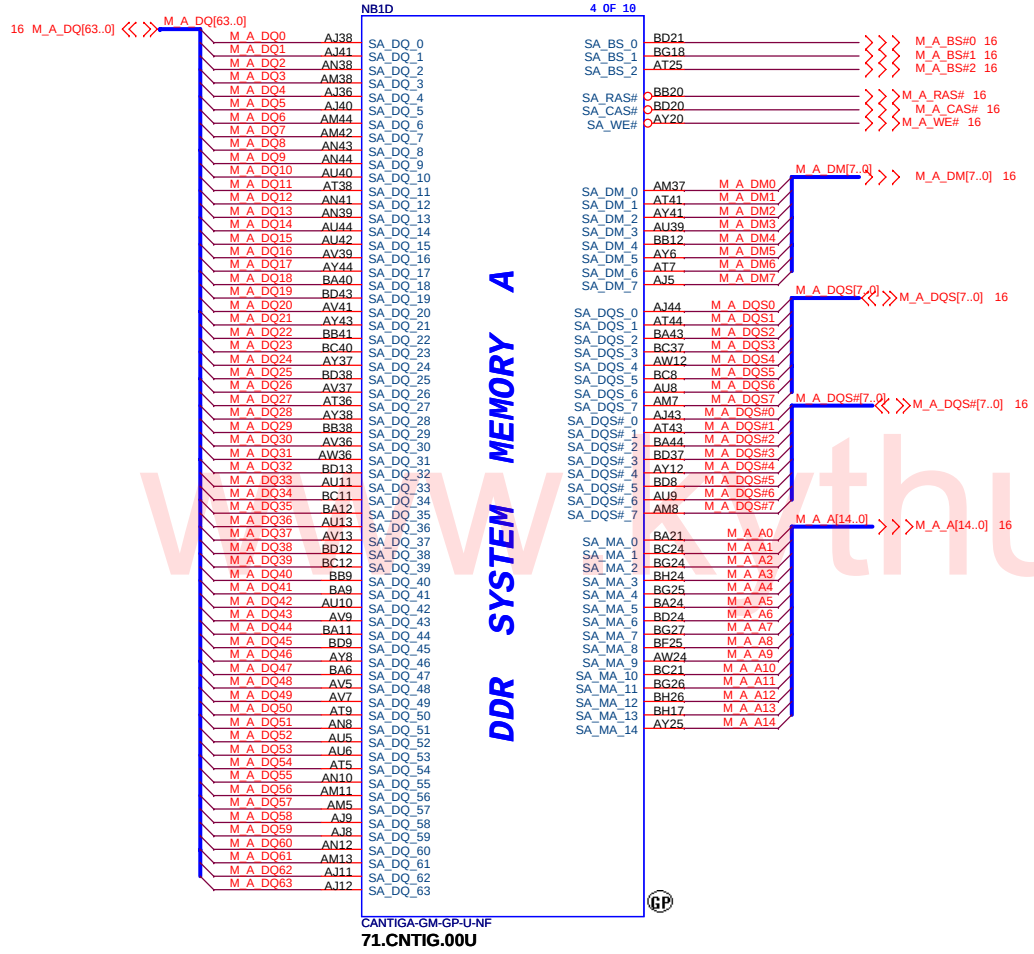

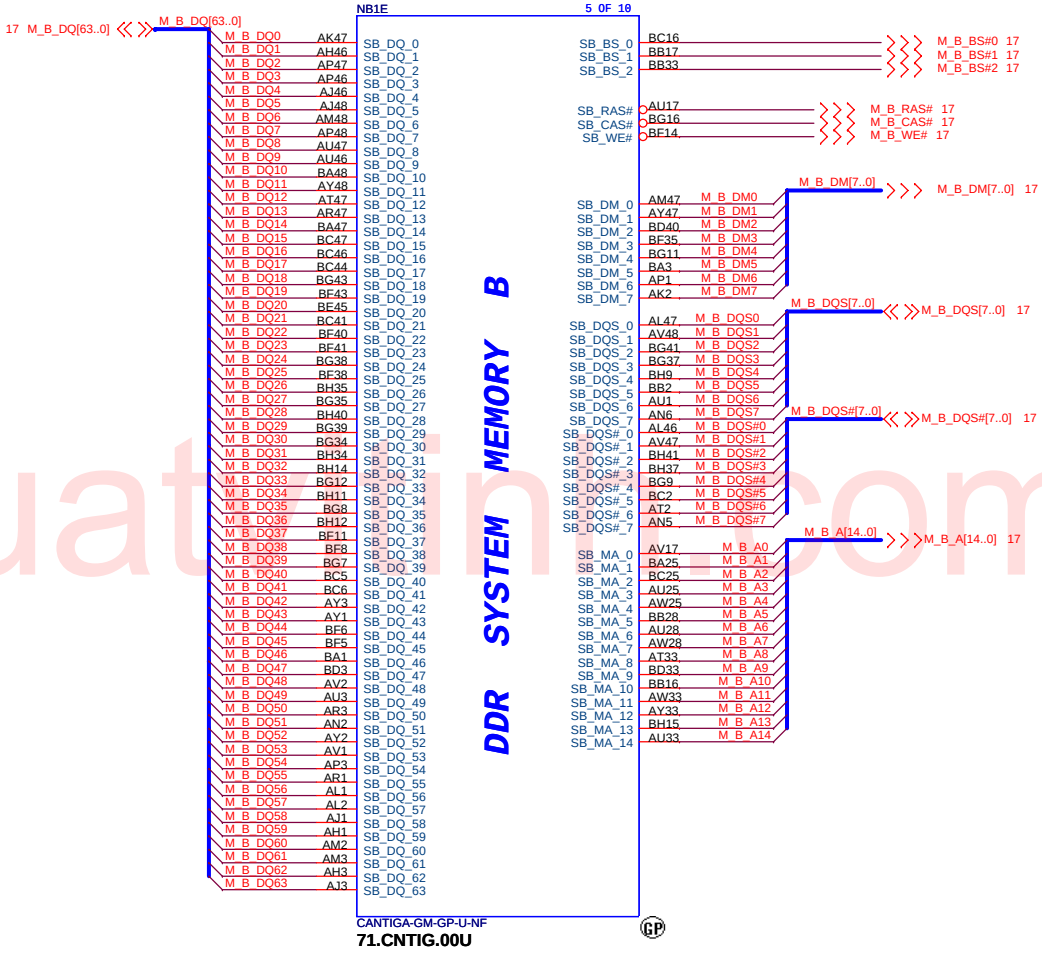

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Title	***Cantiga (3 of 6)***	
Size	Document Number: **JM70-MV**	Rev: **SB**
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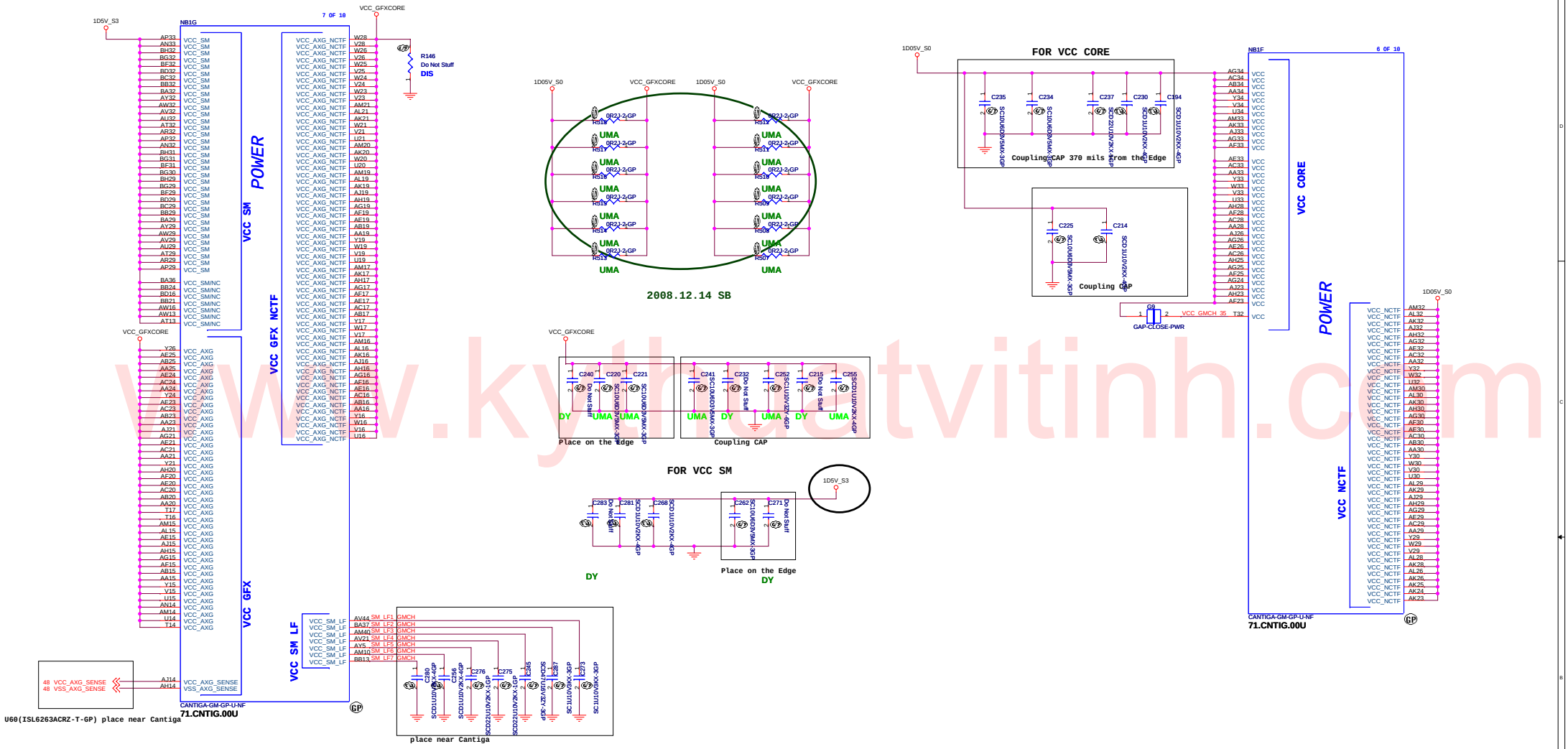

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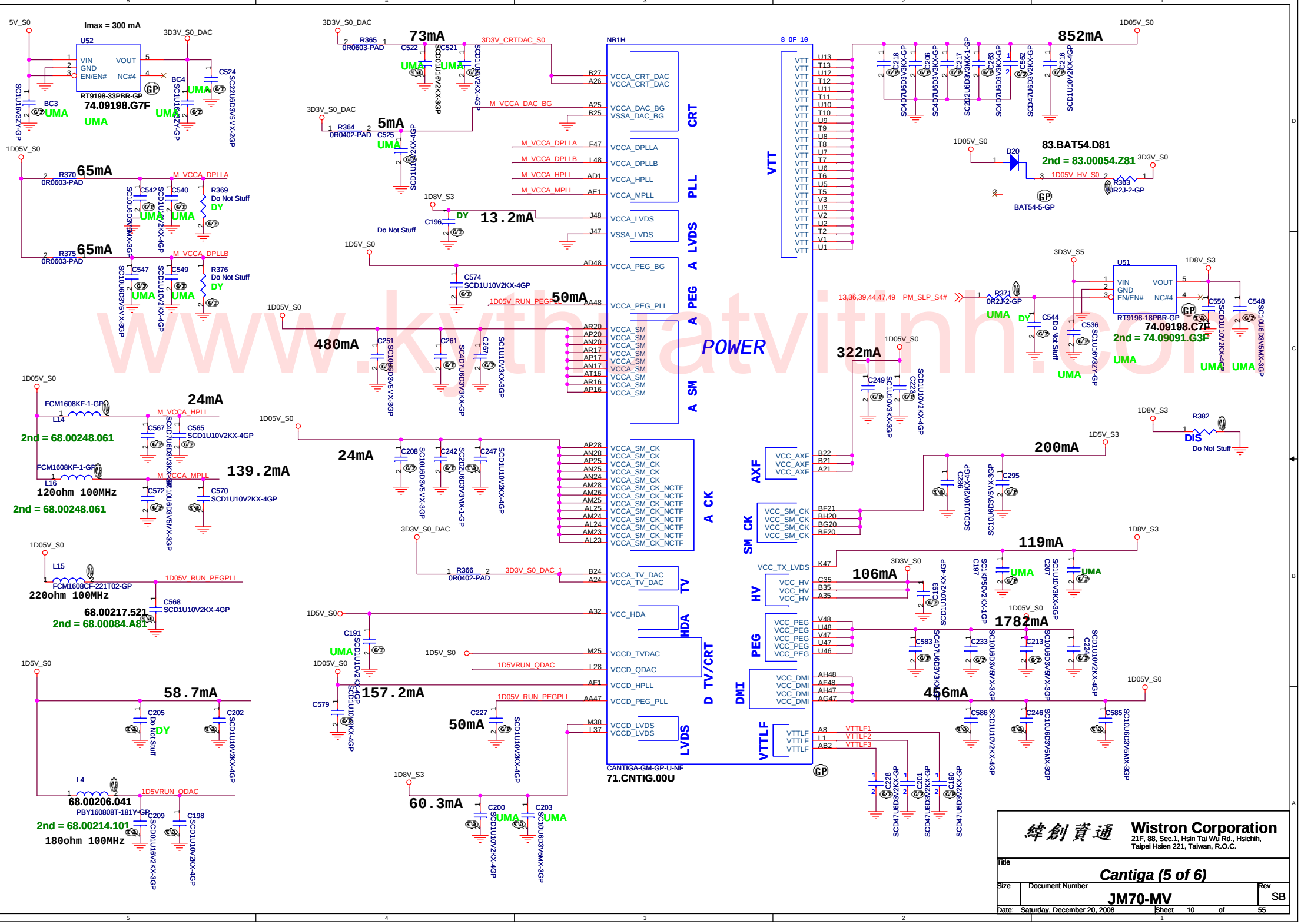

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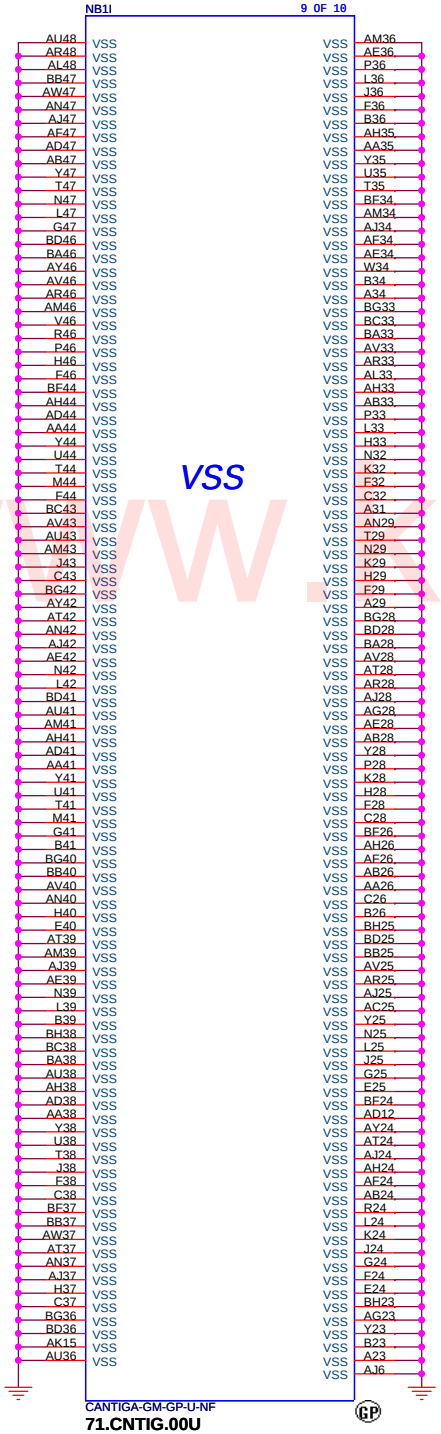

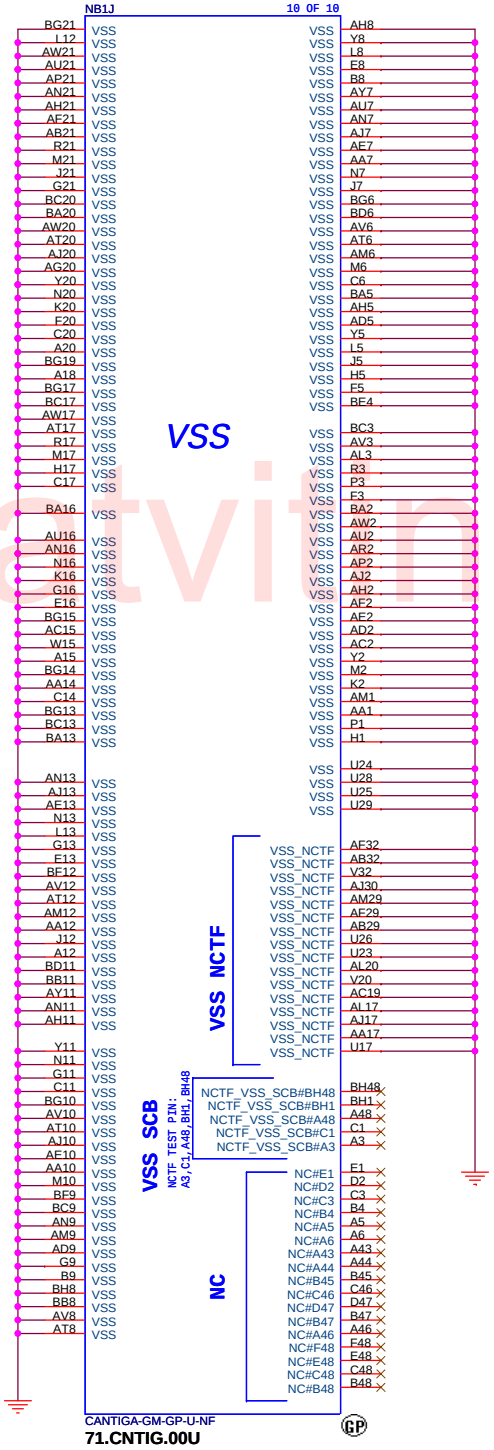

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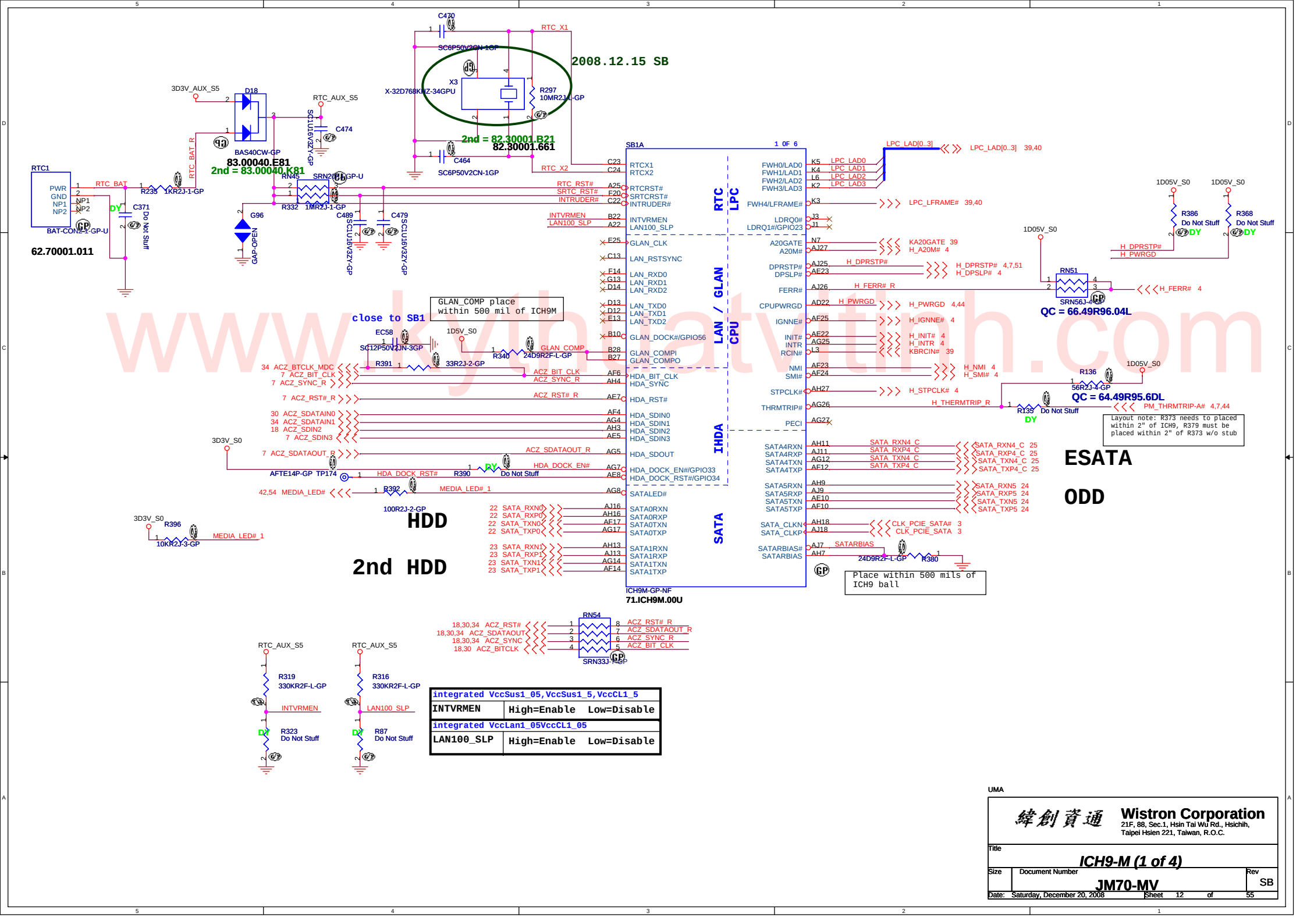

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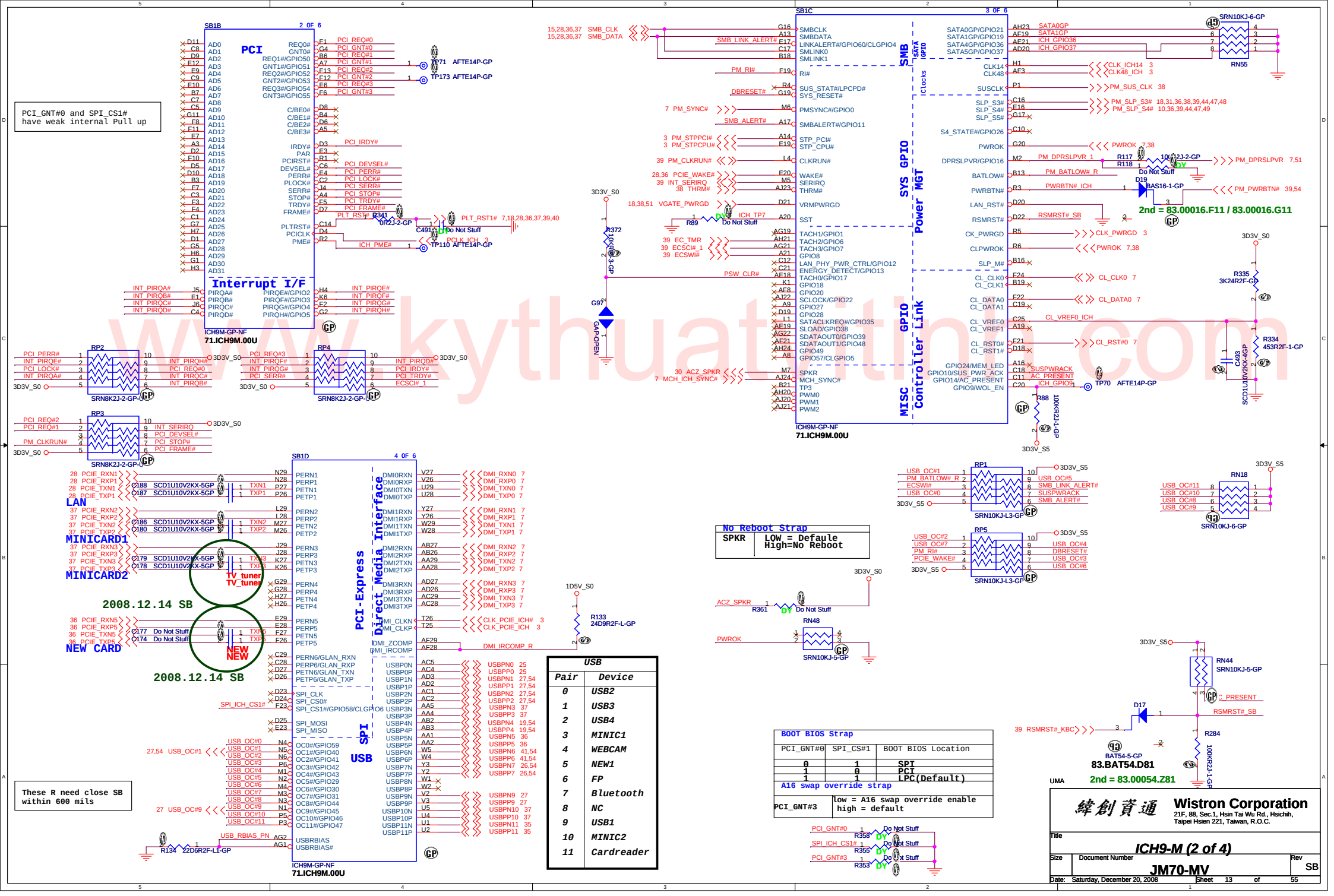

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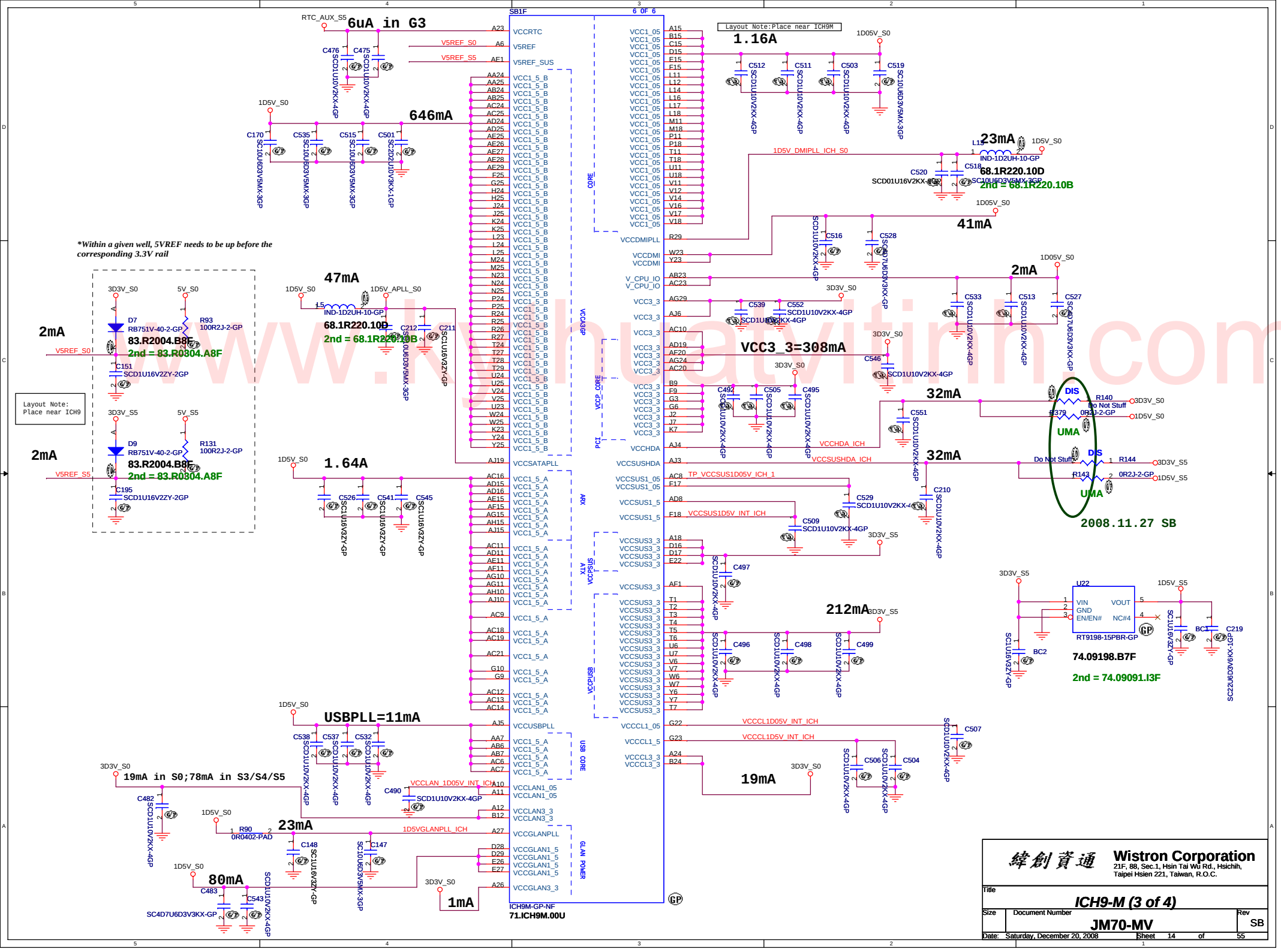

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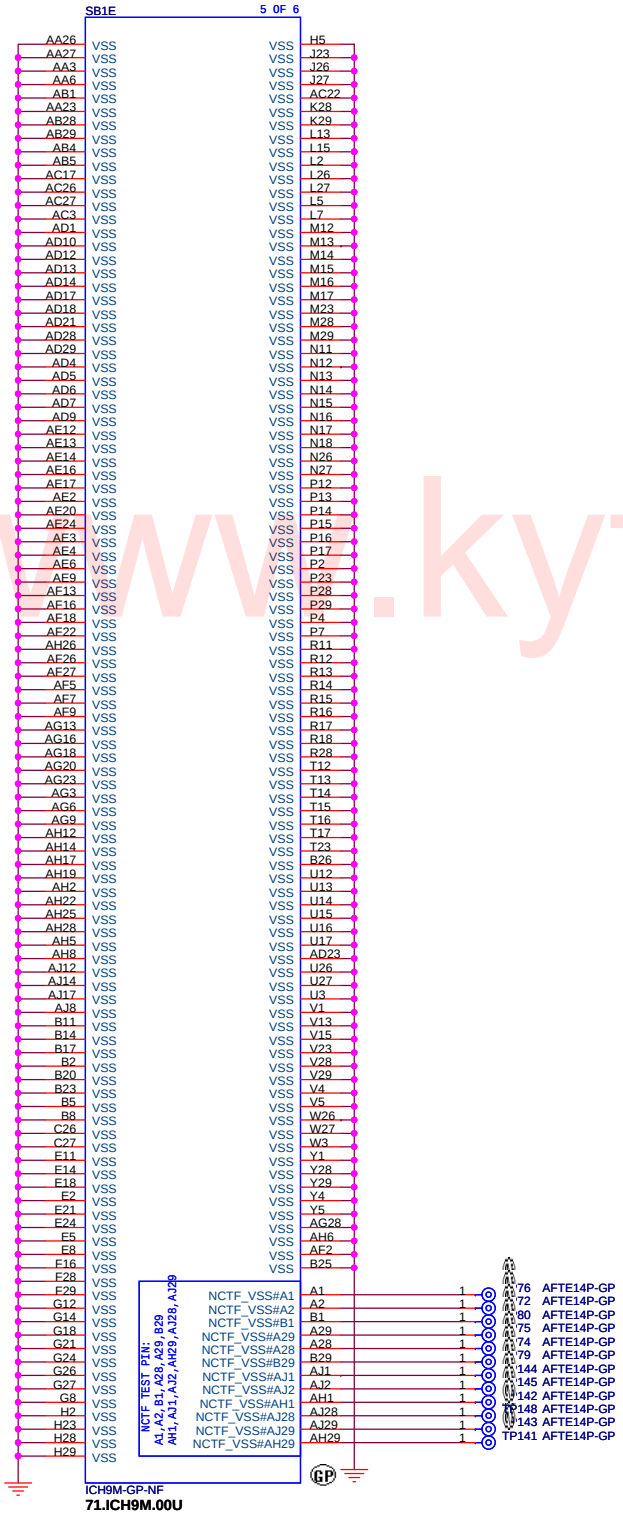

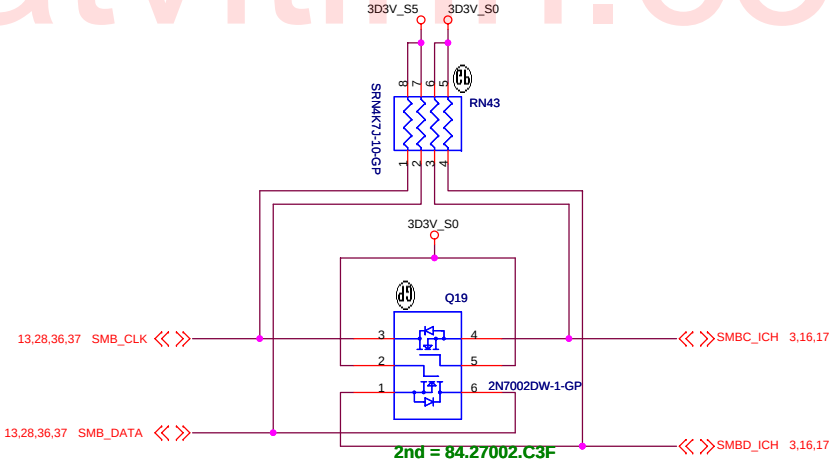

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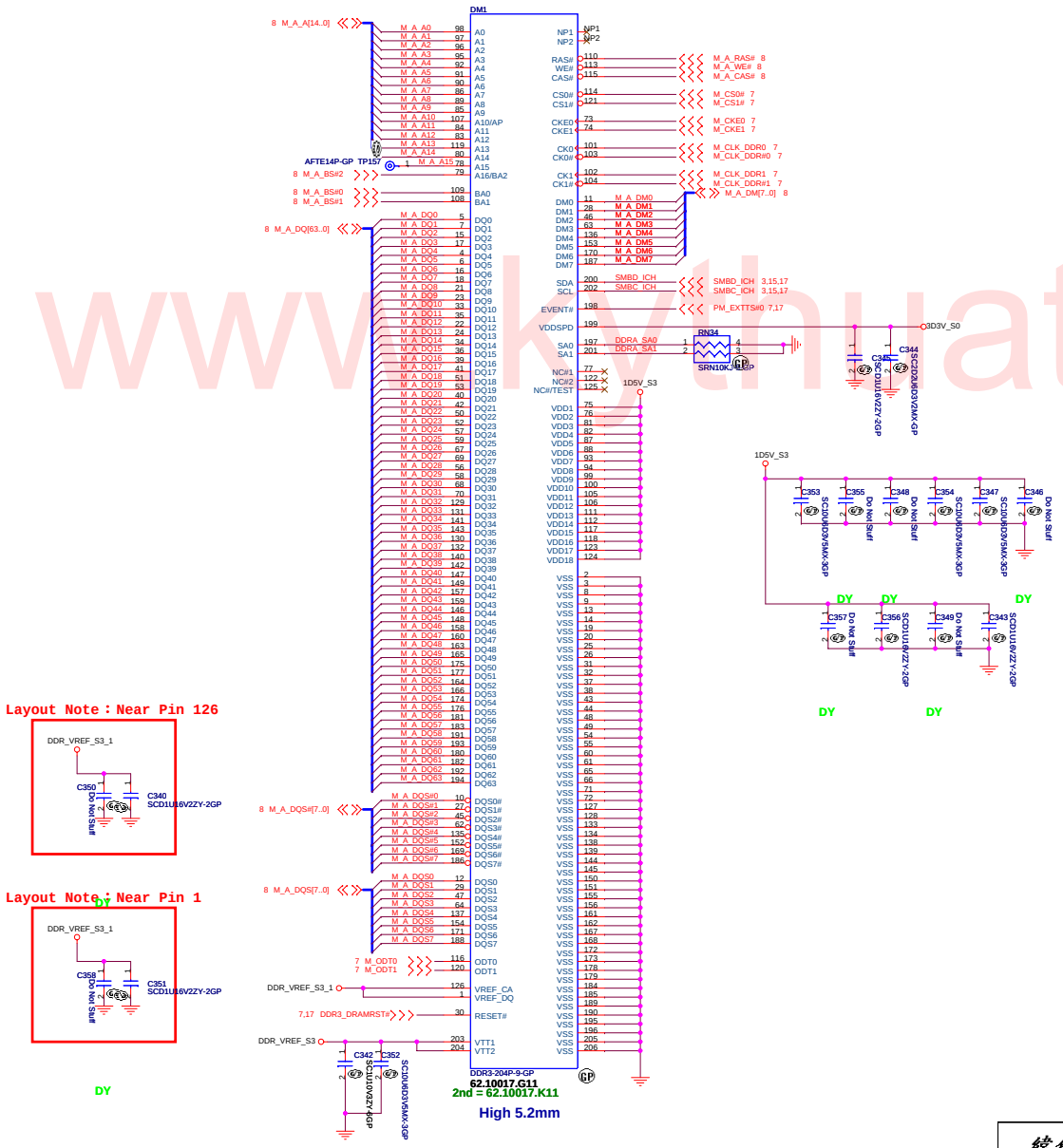
DDR3 SOCKET_1



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Title	DDR3 Socket
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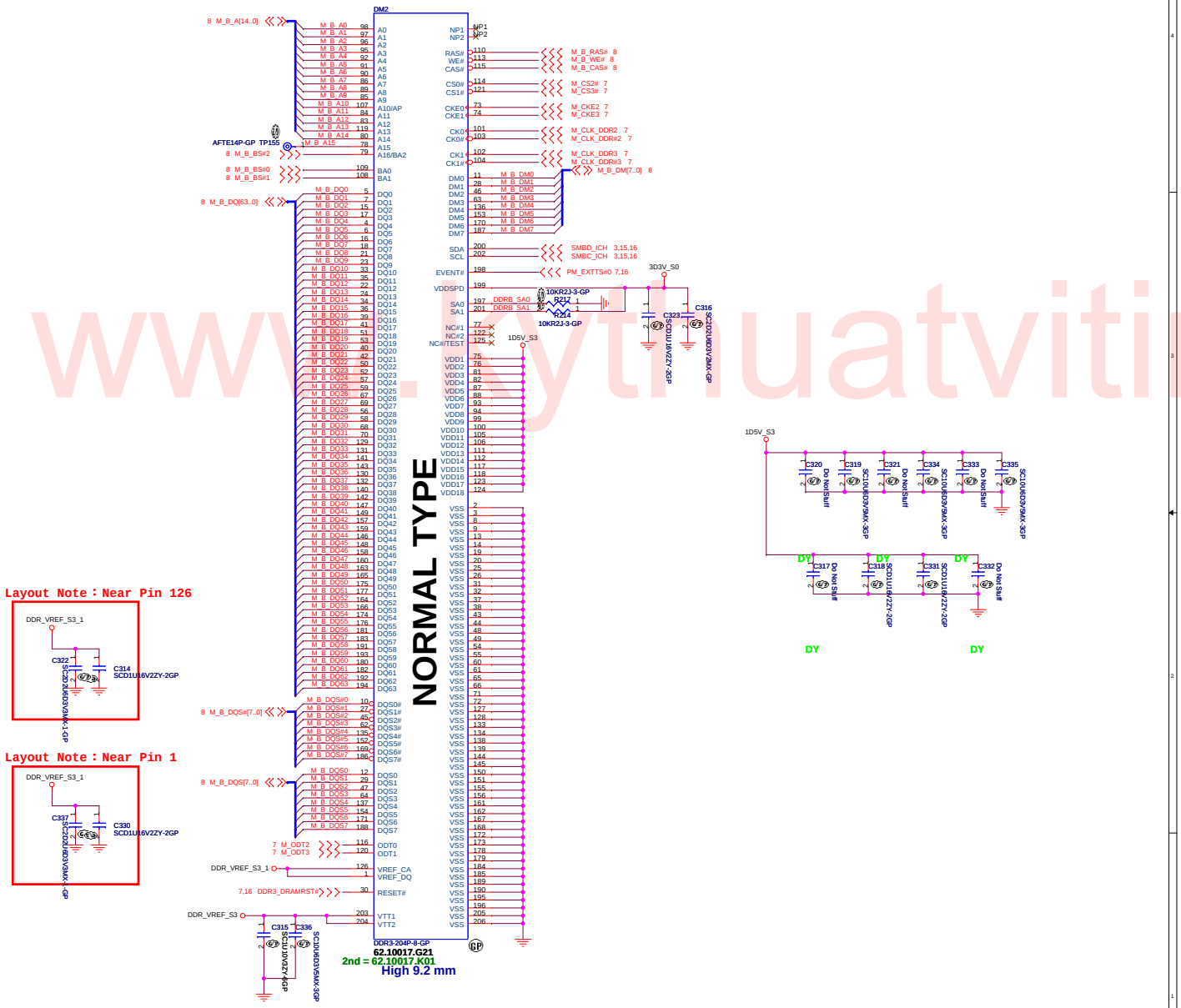
DDR3 SOCKET_2



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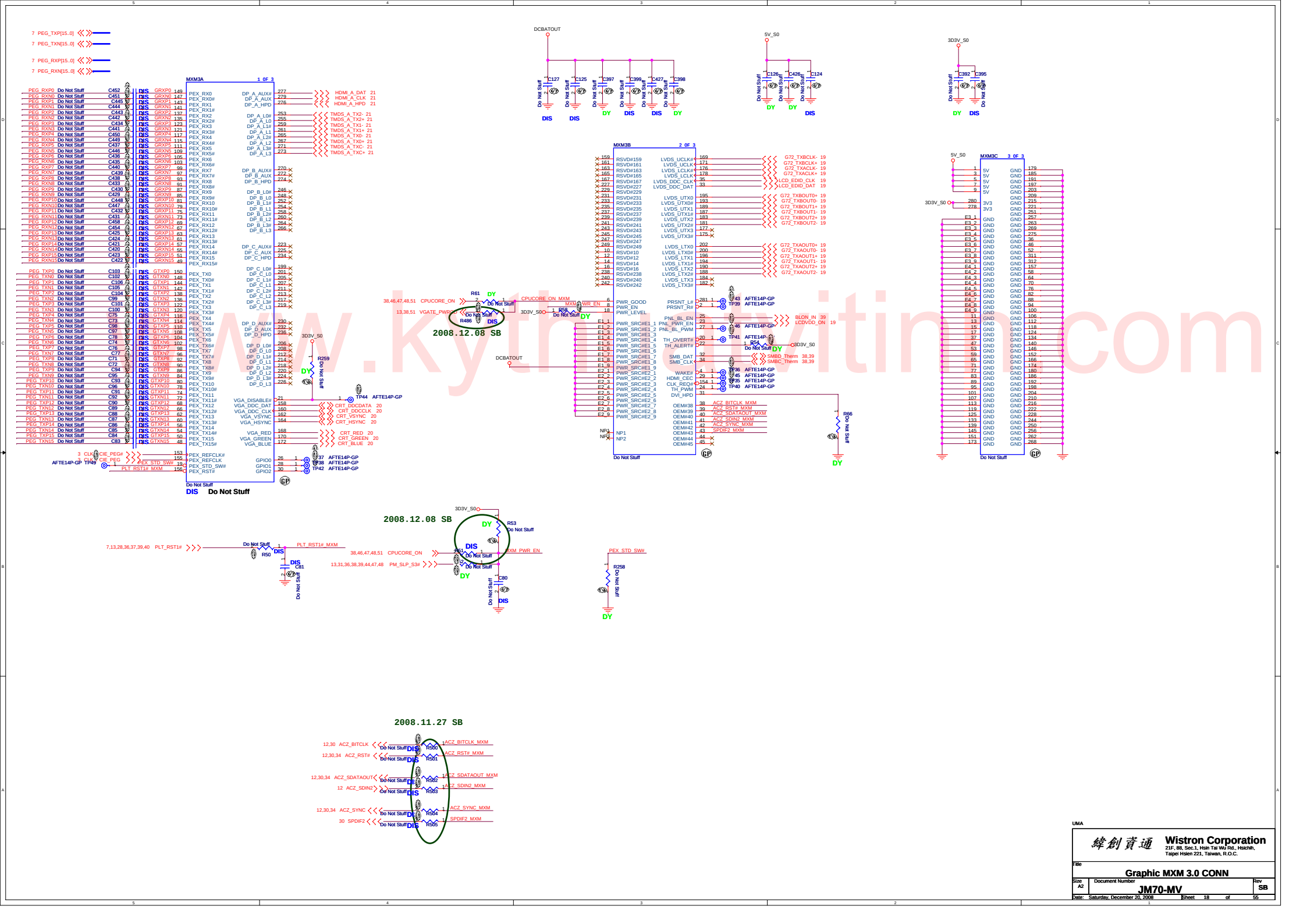

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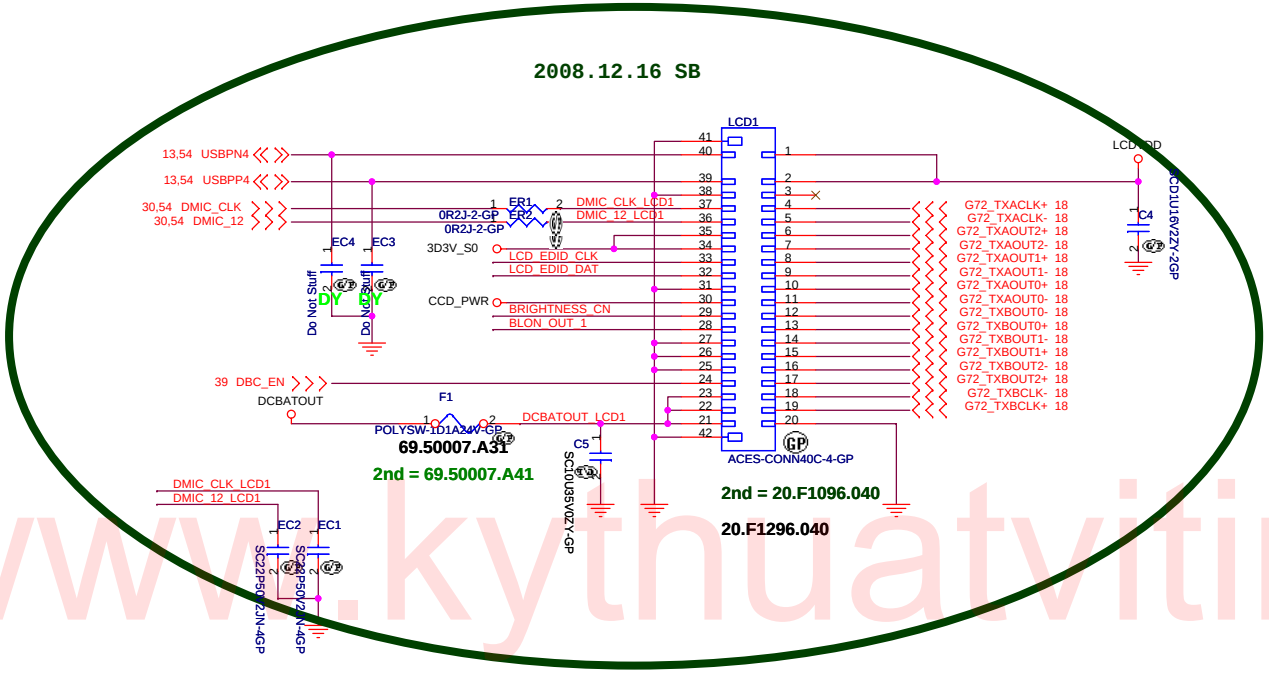

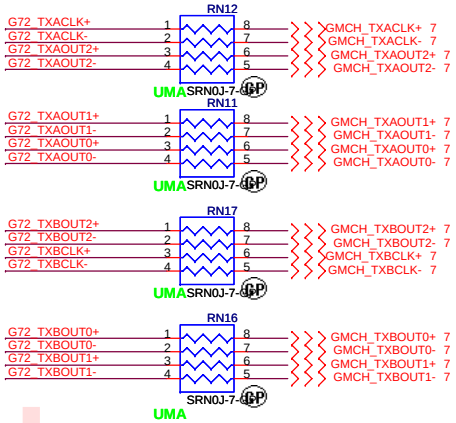

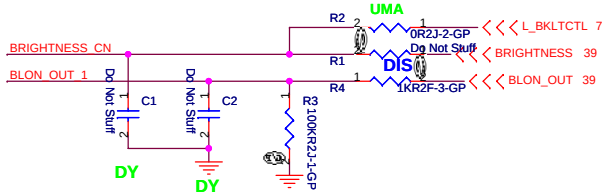

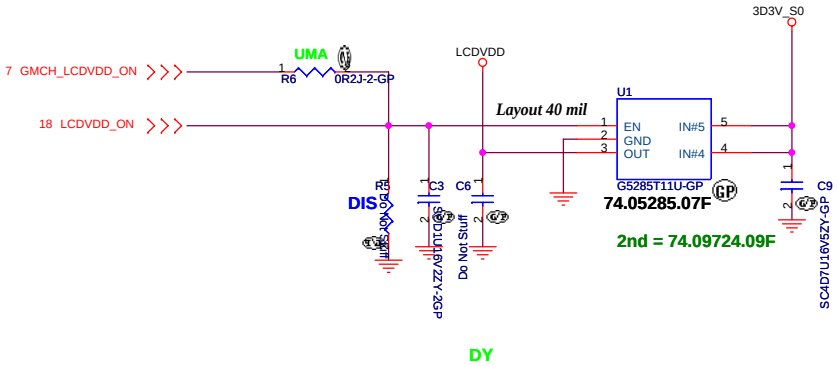

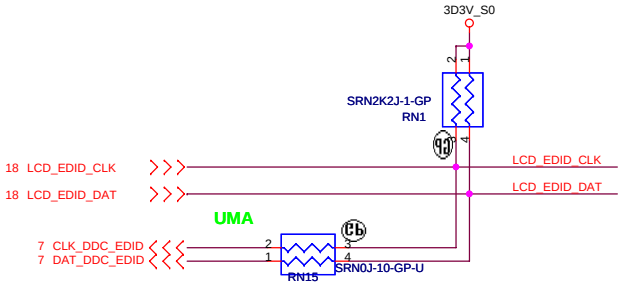

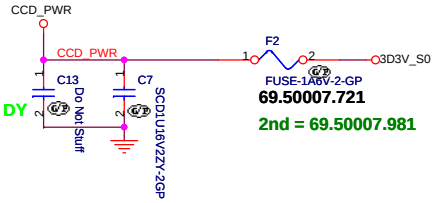

UMA

Wistron Corporation
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Title: **LCD CONN**

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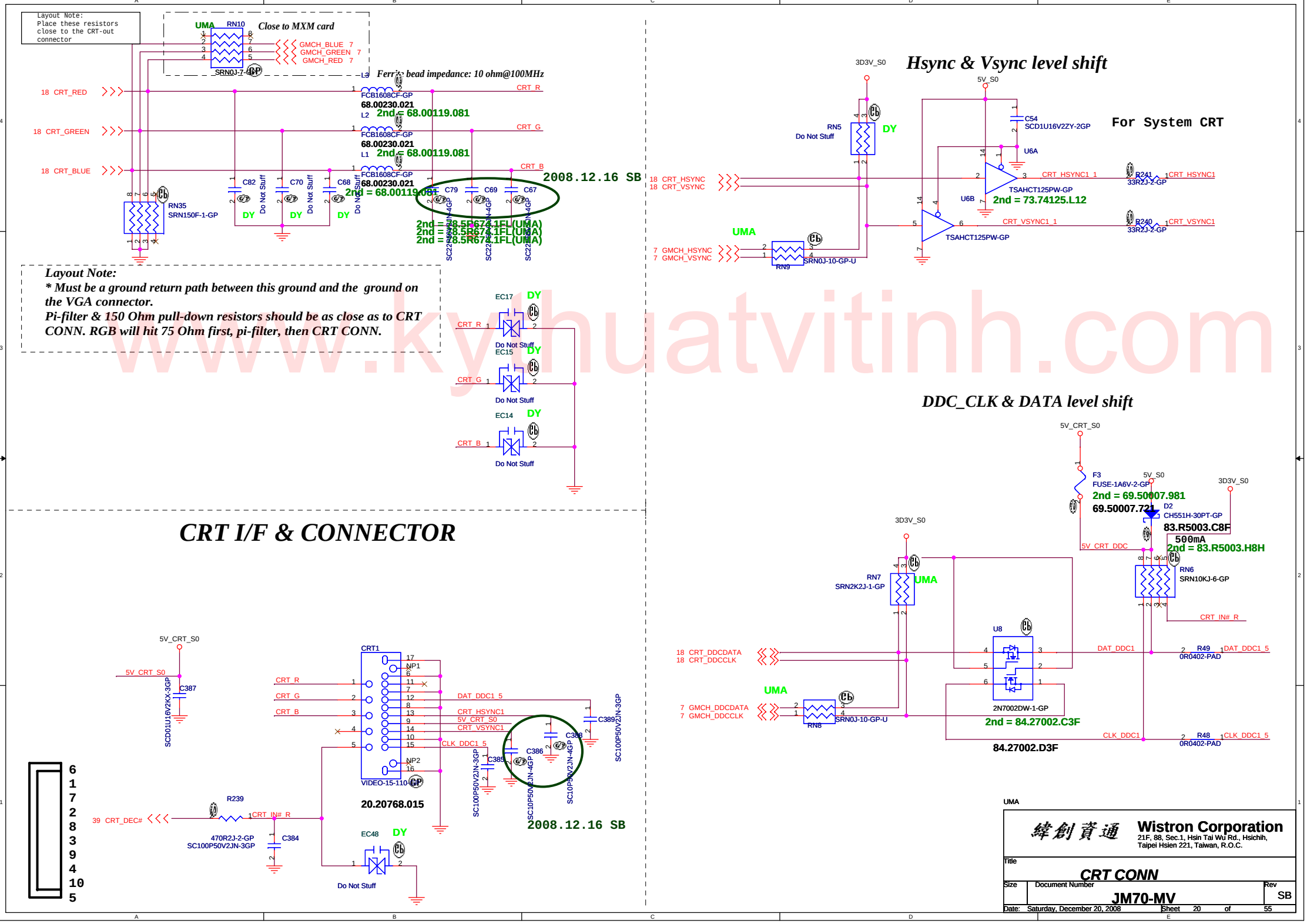

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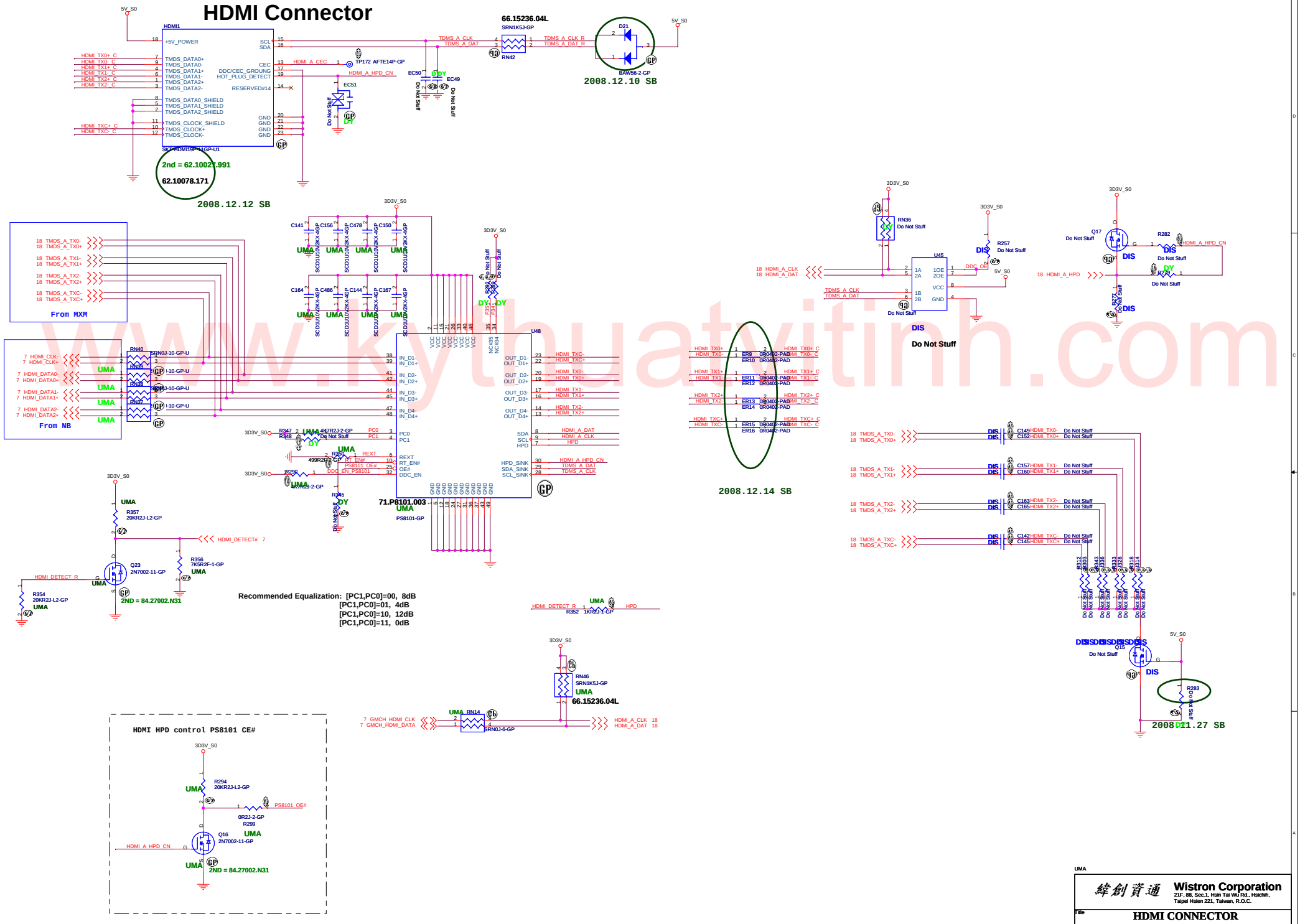
HDMI Connector



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Title: **HDMI CONNECTOR**

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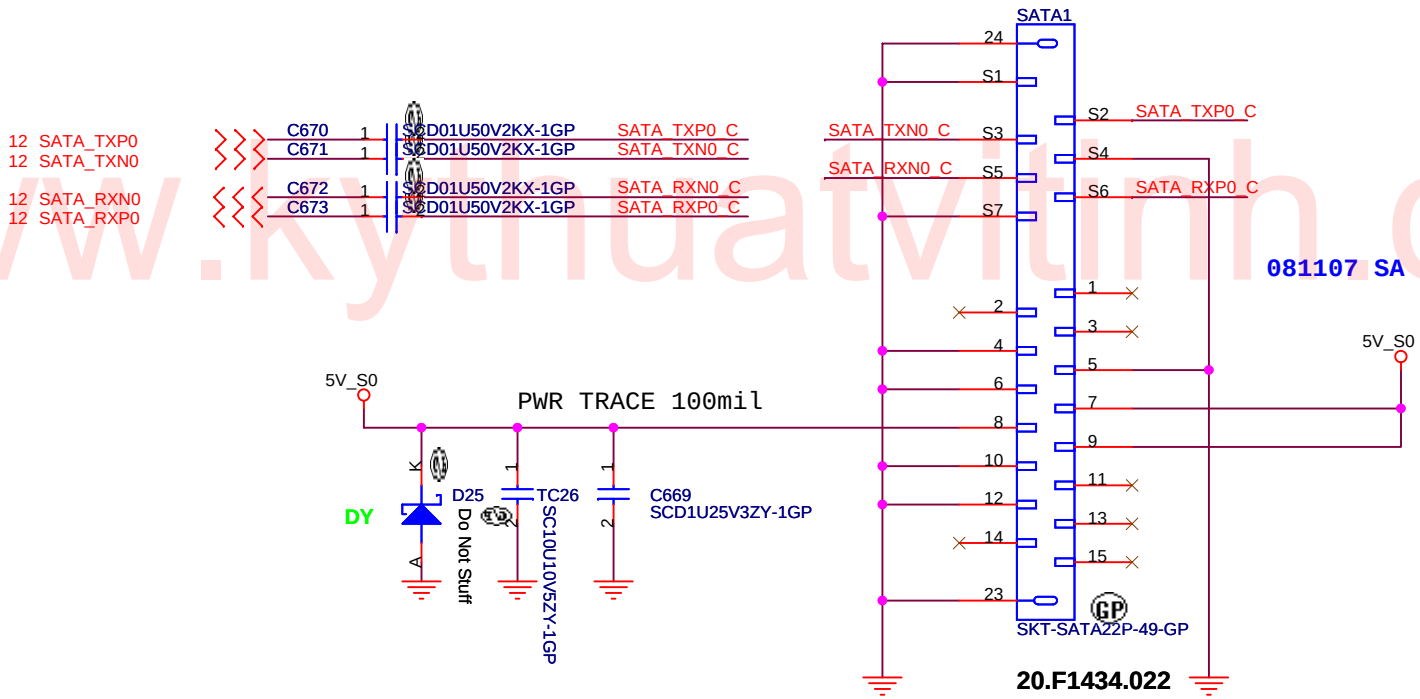
SATA Connector



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Title		
	HDD CONN	
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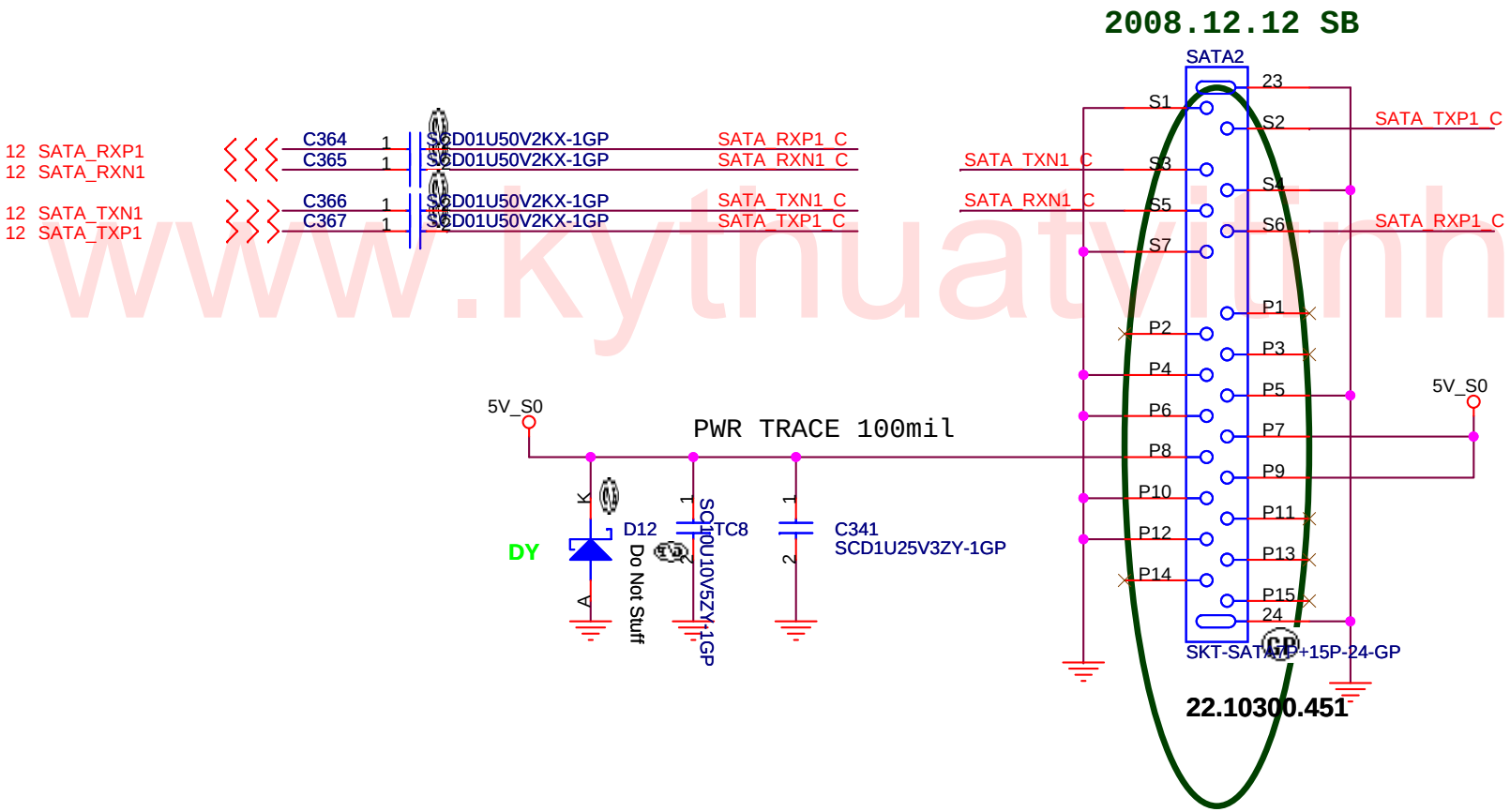
2nd HDD SATA Connector



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Title	***2nd HDD***	
Size	Document Number **JM70-MV**	Rev SB
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ODD Connector

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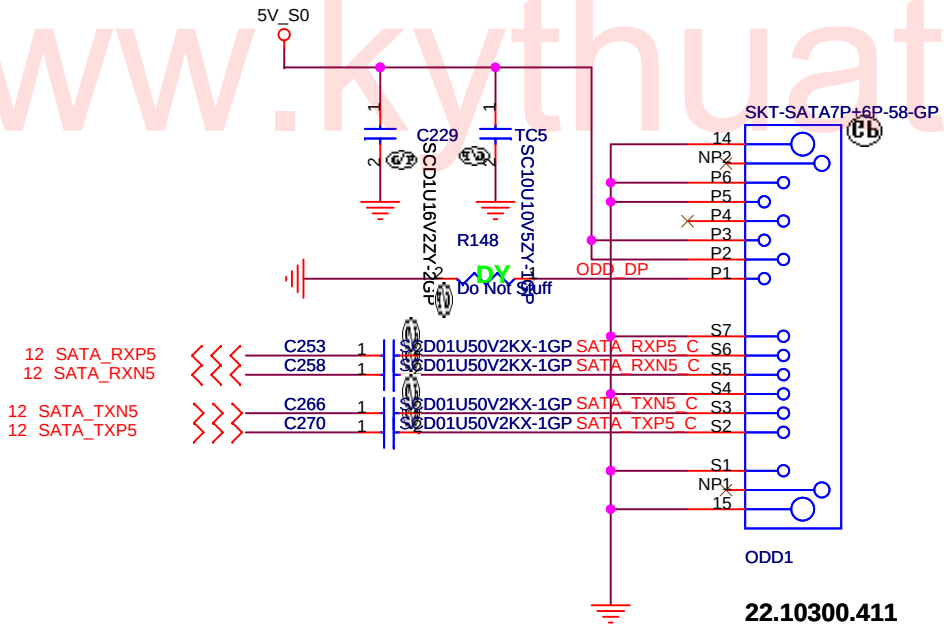

UMA

緯創資通 **Wistron Corporation**
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Title		
	ODD	
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ESATA Connector

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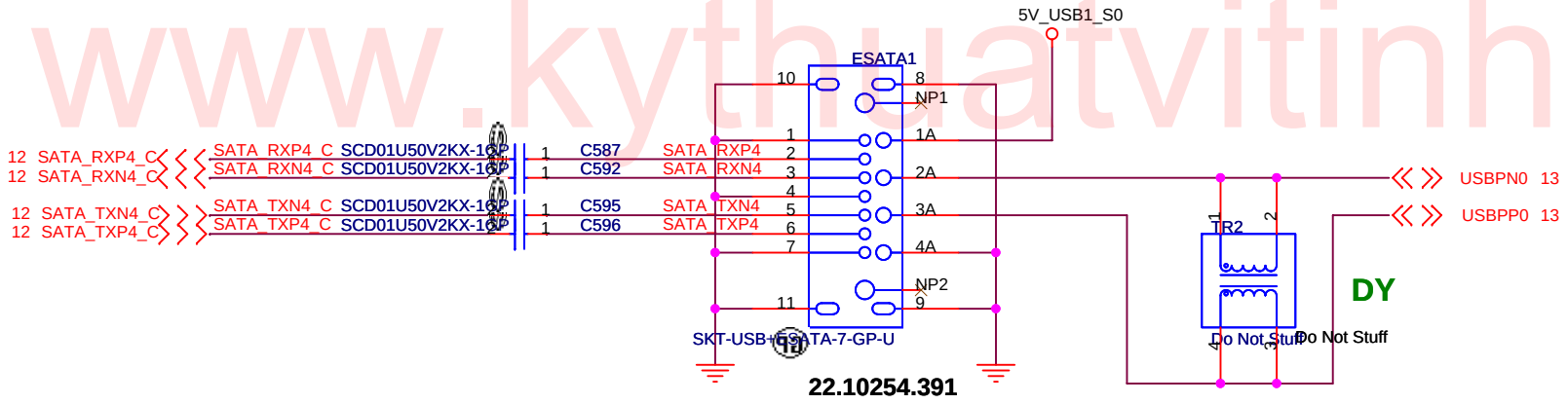

UMA

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Title	***ESATA***	
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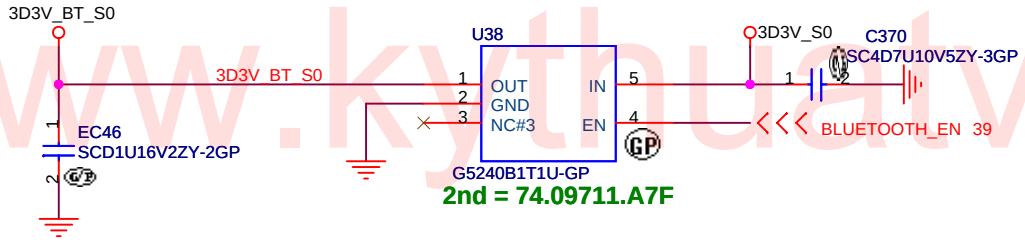
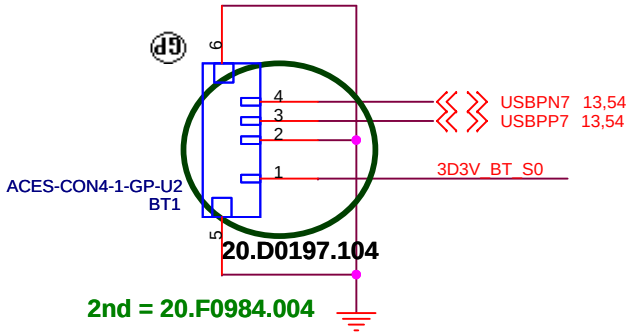
BLUETOOTH MODULE



EC20 put near BLUE1 / all USB put one choke near connector by EMI request

2008.12.08 SB



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Title	***BLUETOOTH***	
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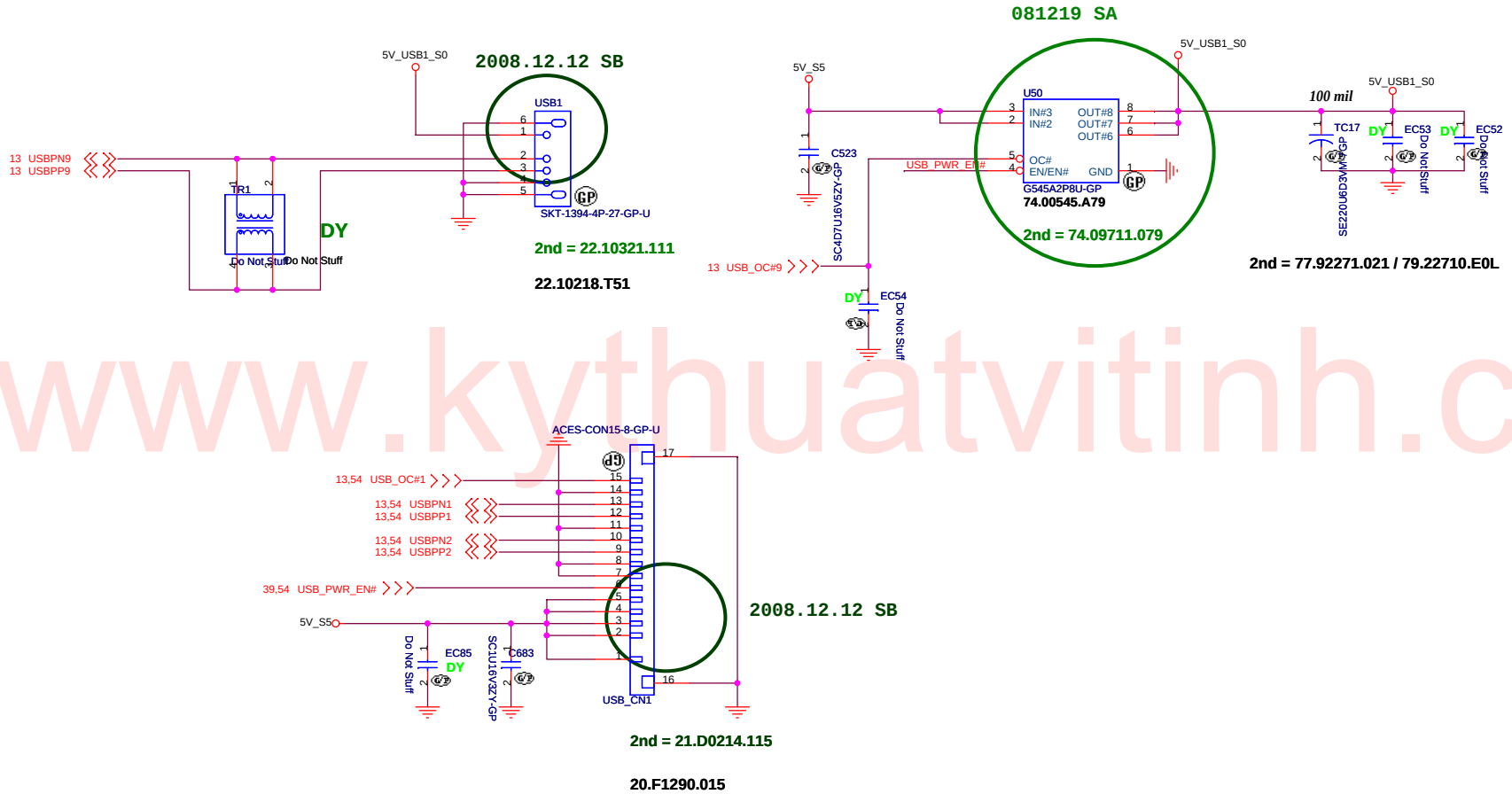
USB1 Connector



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Title	*USB CONN*	
Size	Document Number JM70-MV	Rev SB
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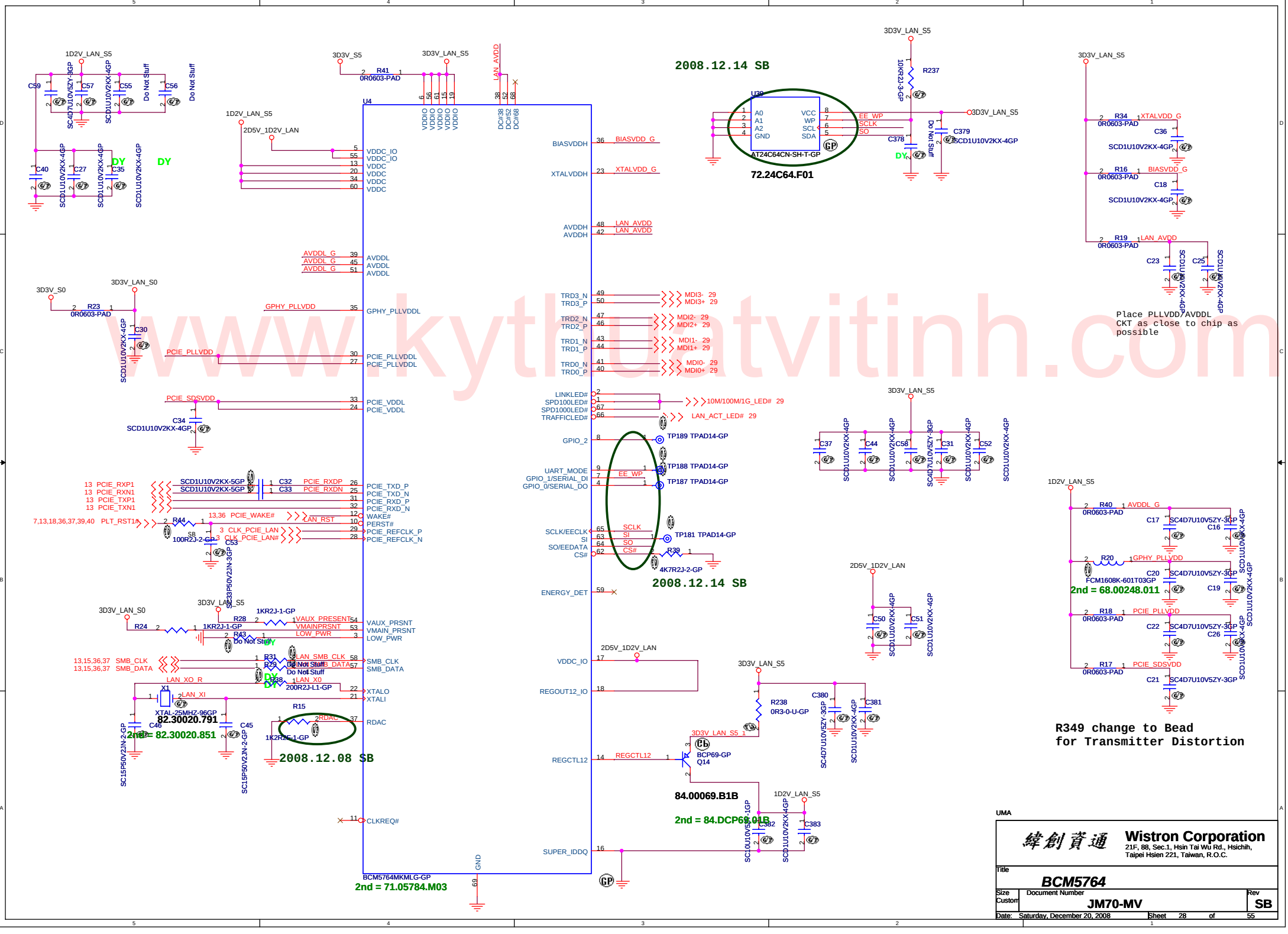

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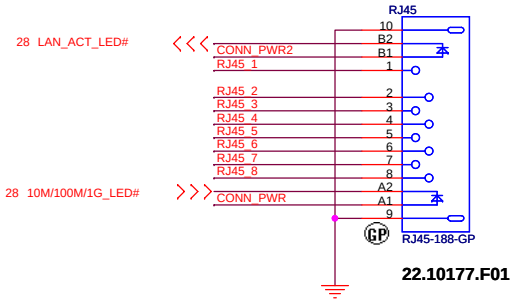
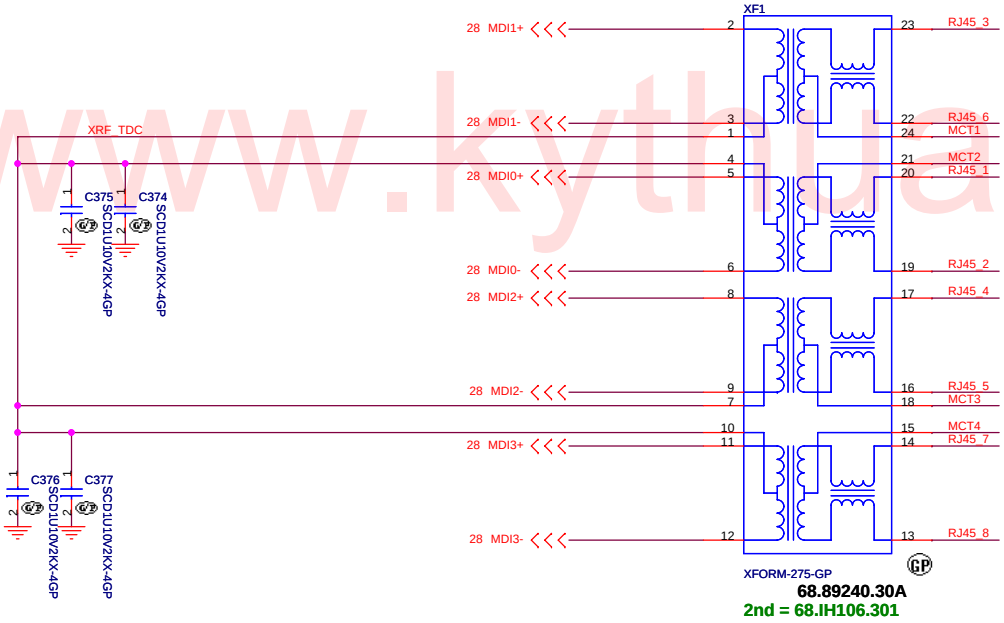
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

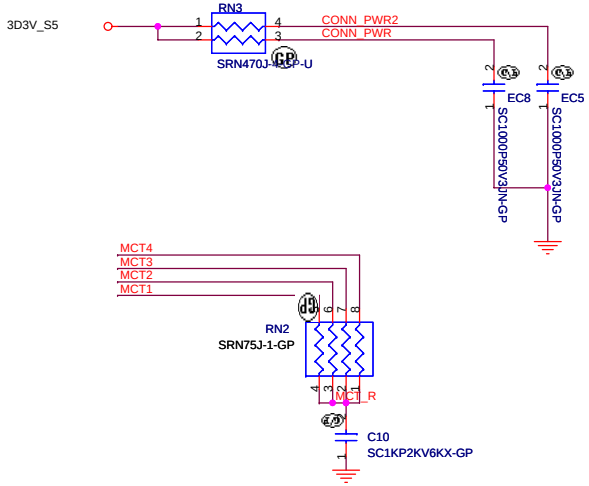
LAN Connector

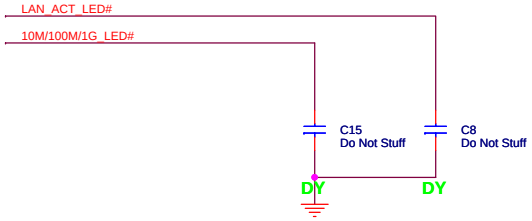
LAN Connector



GIGA Lan Transformer







UMA

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Title	LAN CONN	
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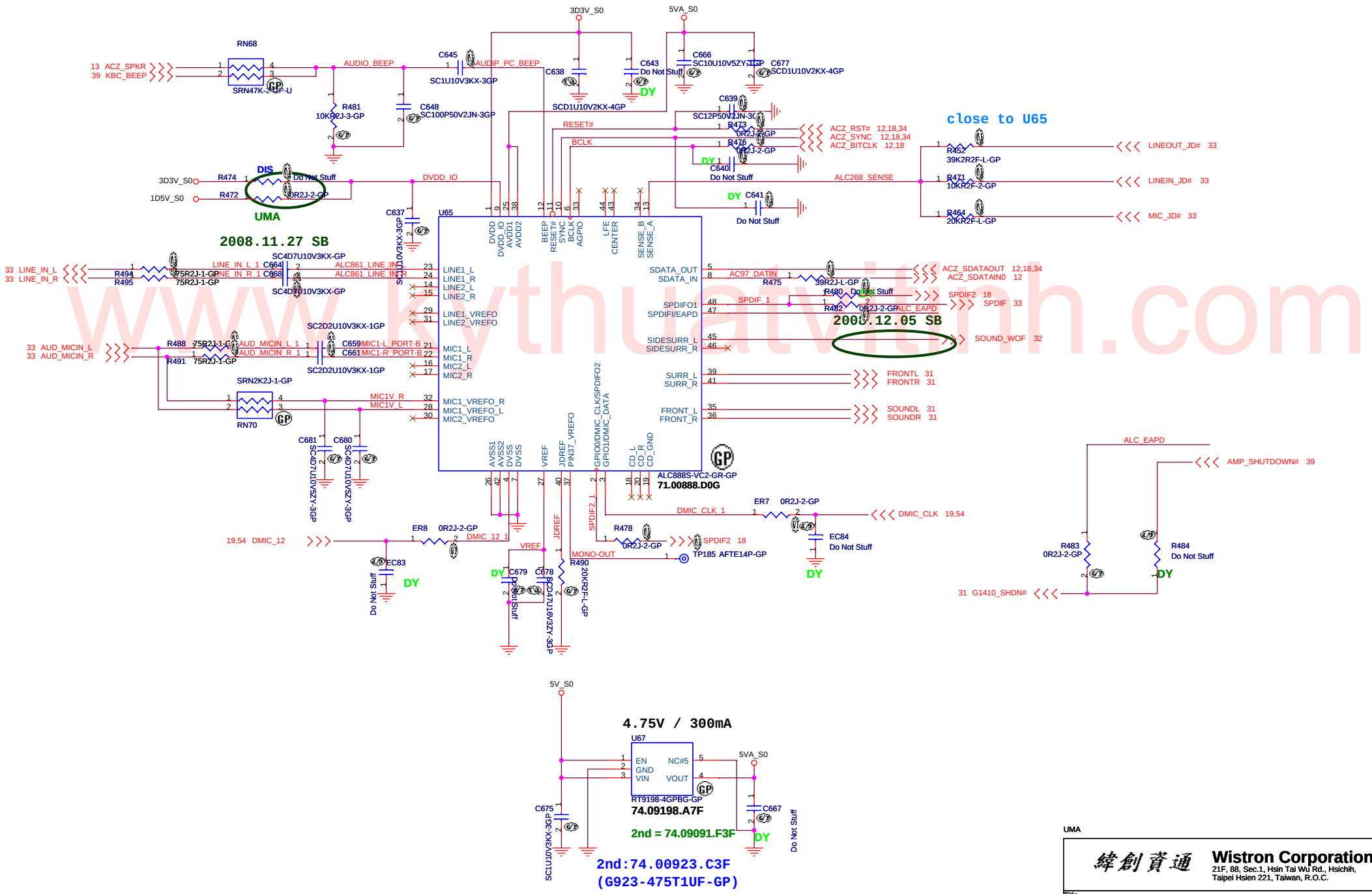

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UMA

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Title: ***Azalia codec ALC888***

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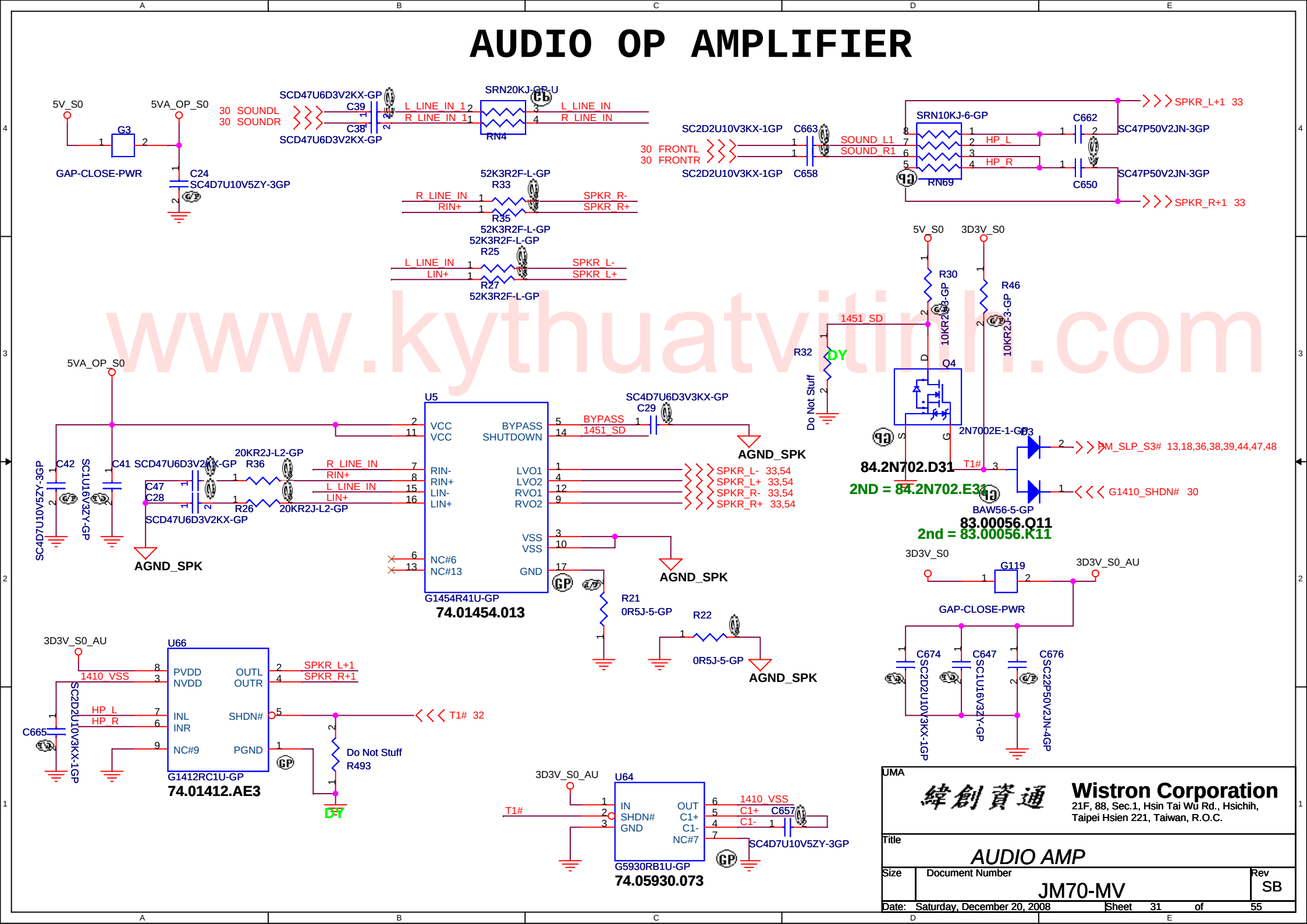
AUDIO OP AMPLIFIER



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緯創資通

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Title: *AUDIO AMP*

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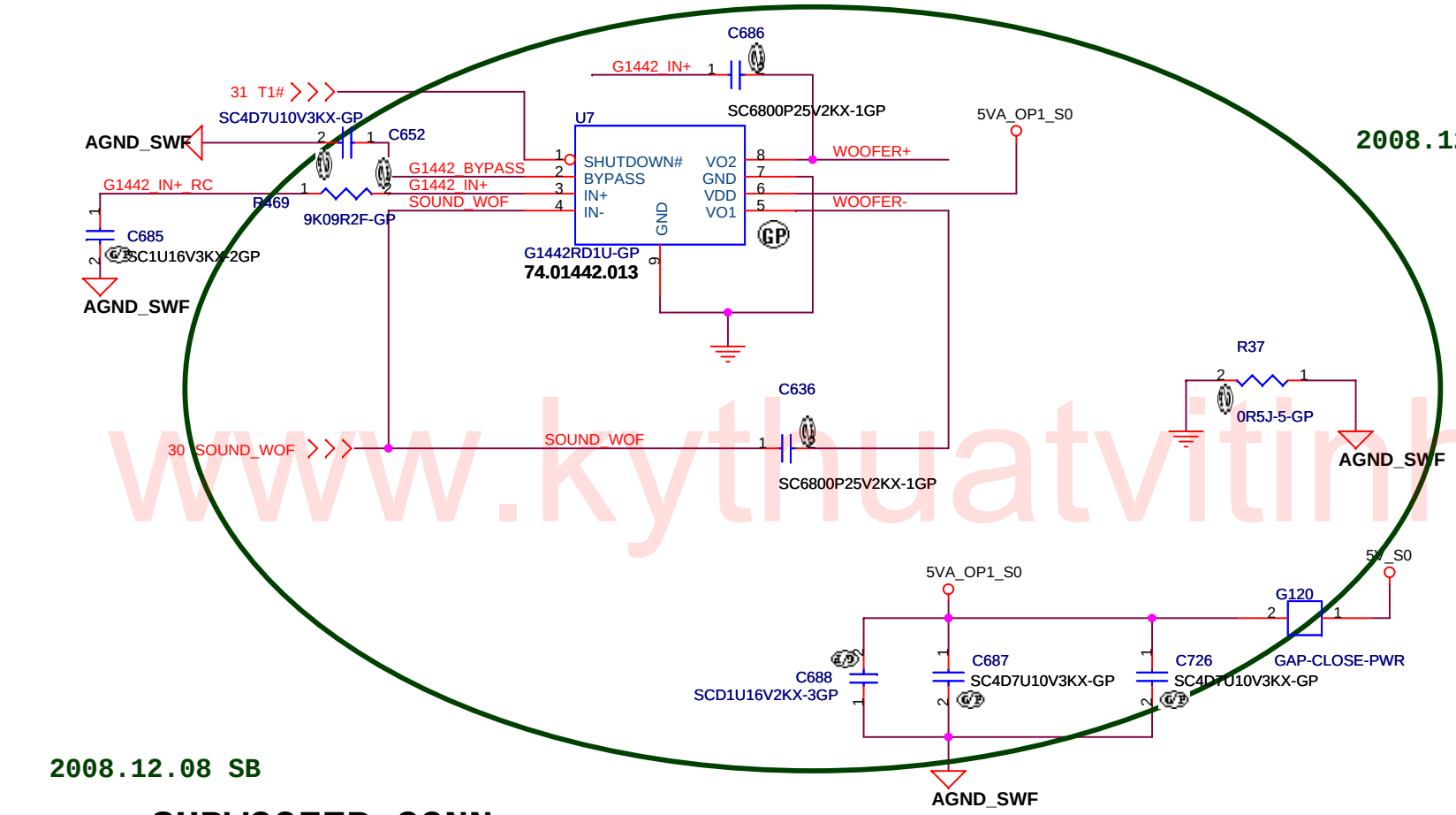

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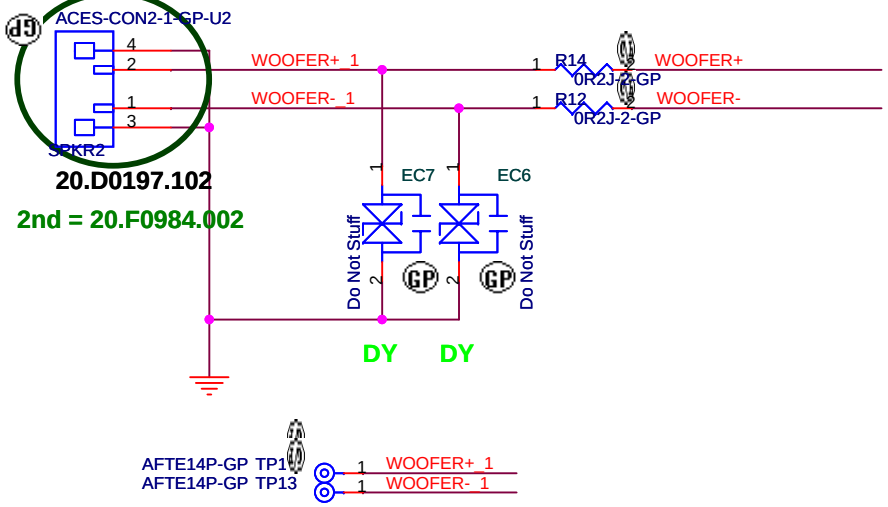
2008.12.08 SB

SUBWOOFER CONN.



UMA

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Title	***SUBWOOFER CONN.***	
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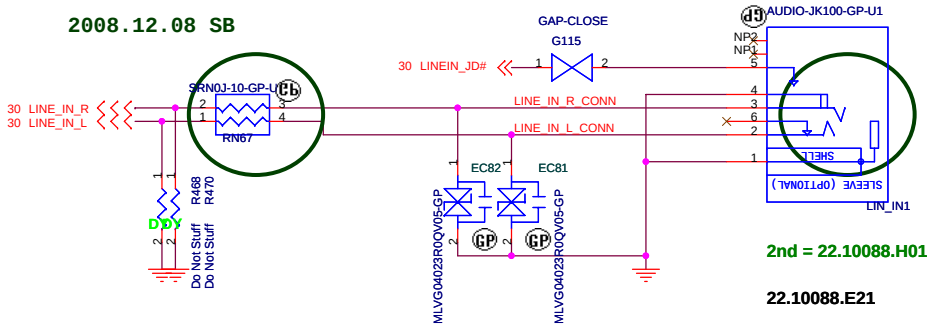
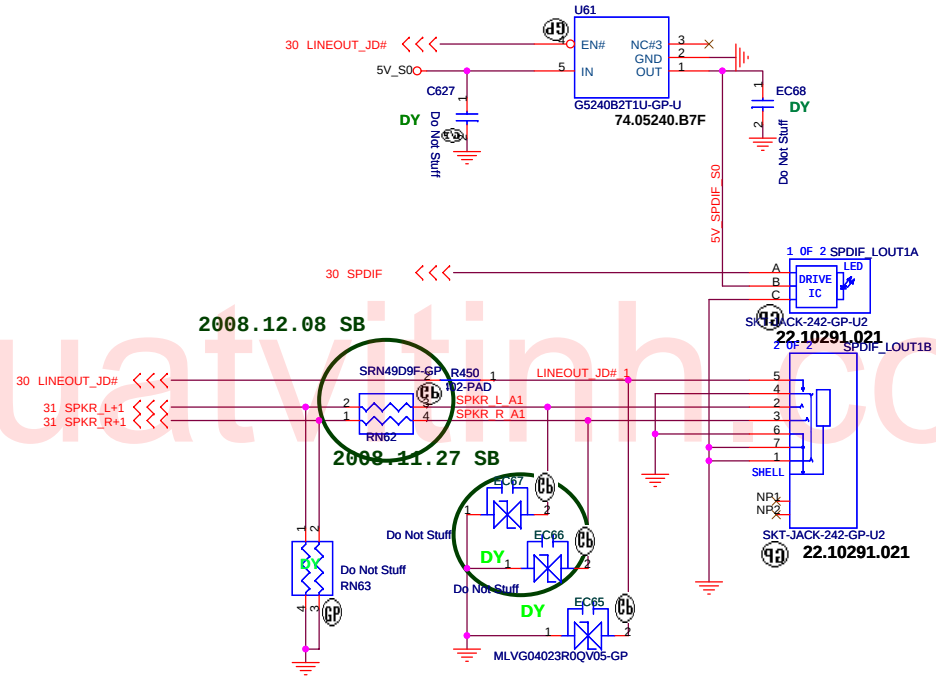
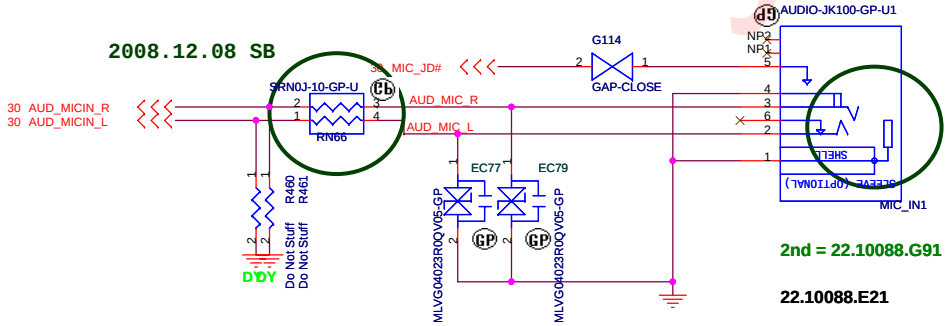
LINE IN



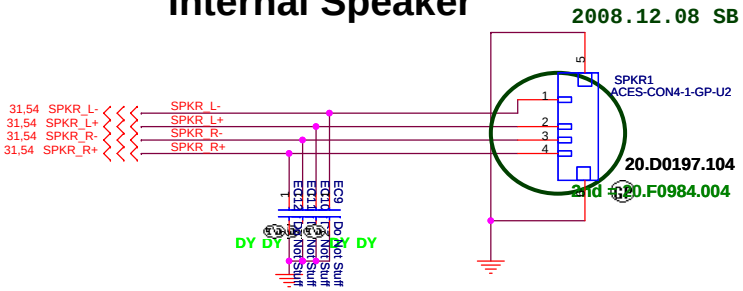
LINE OUT / SPDIF



MIC IN



Internal Speaker



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Title	*AUDIO jack*	
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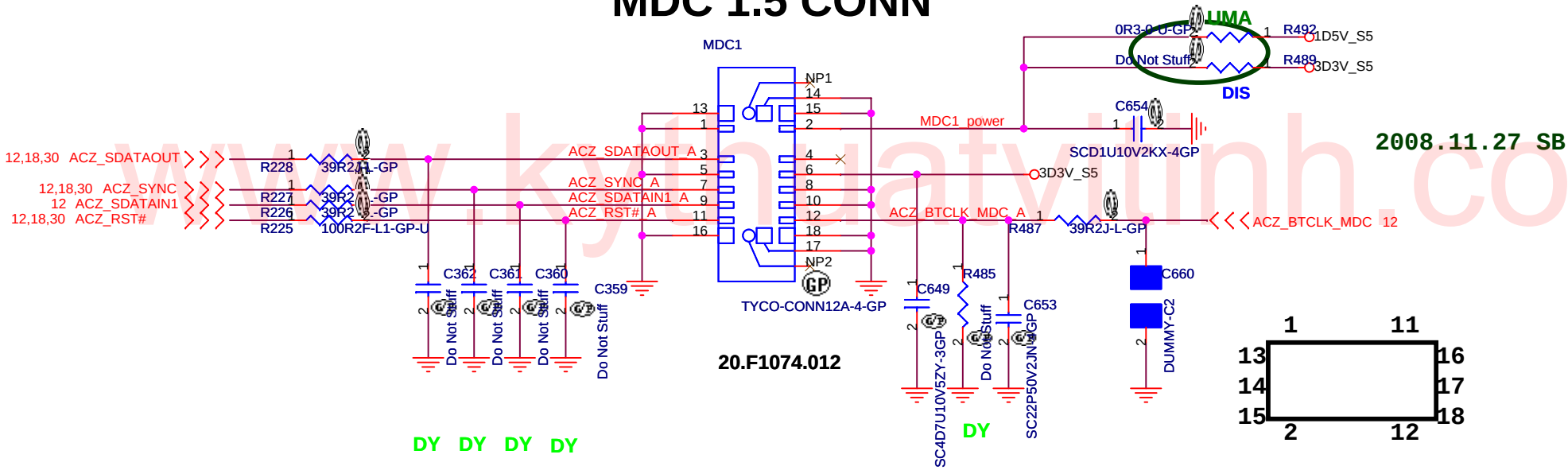
MDC 1.5 CONN



2008.11.27 SB

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Title		
MDC		
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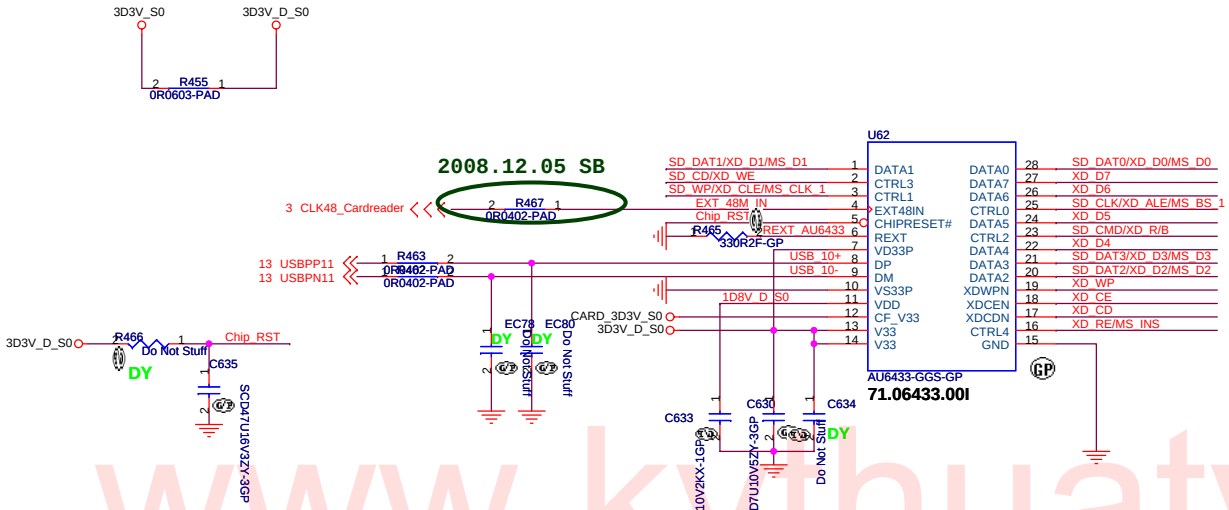

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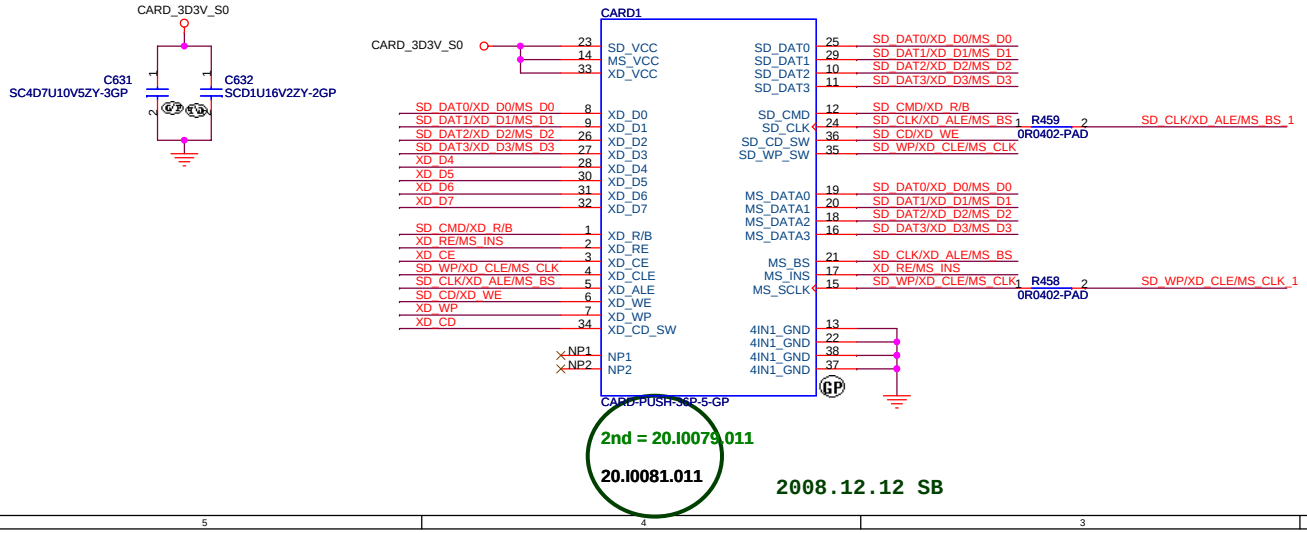
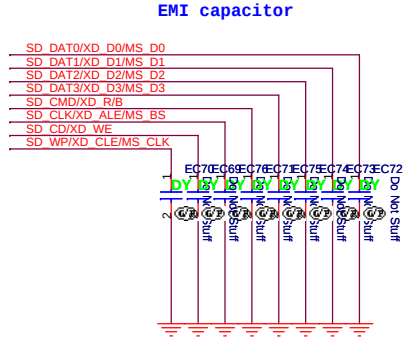
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Cardreader*	
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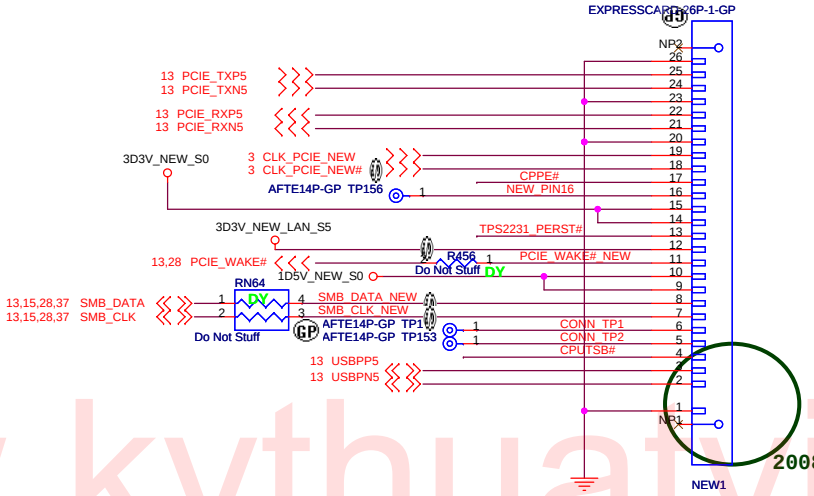

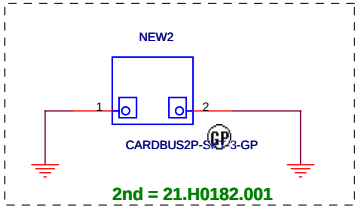

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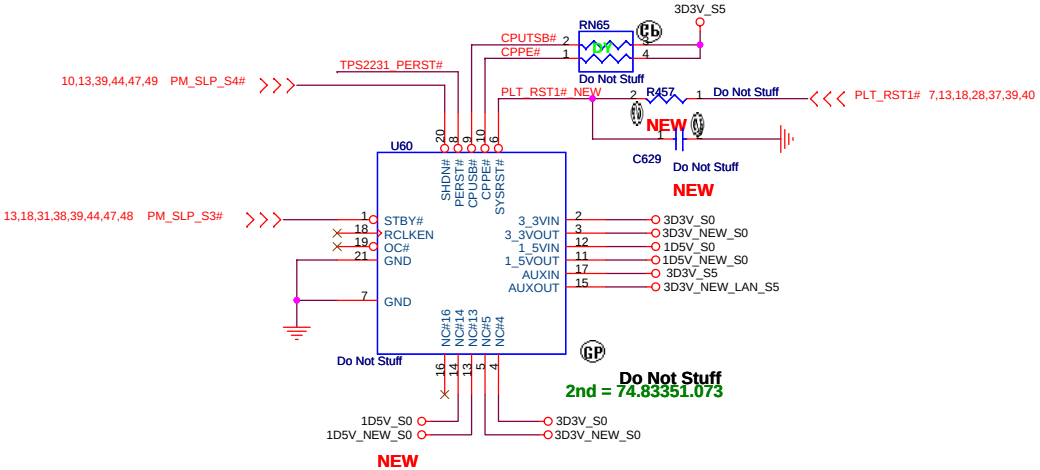
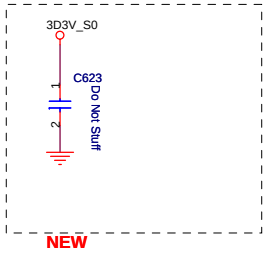
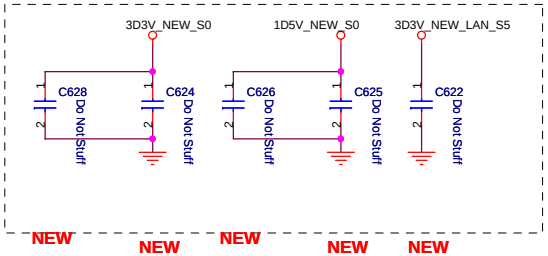


Place them Near to Chip



Place them Near to Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***NEW CARD***	
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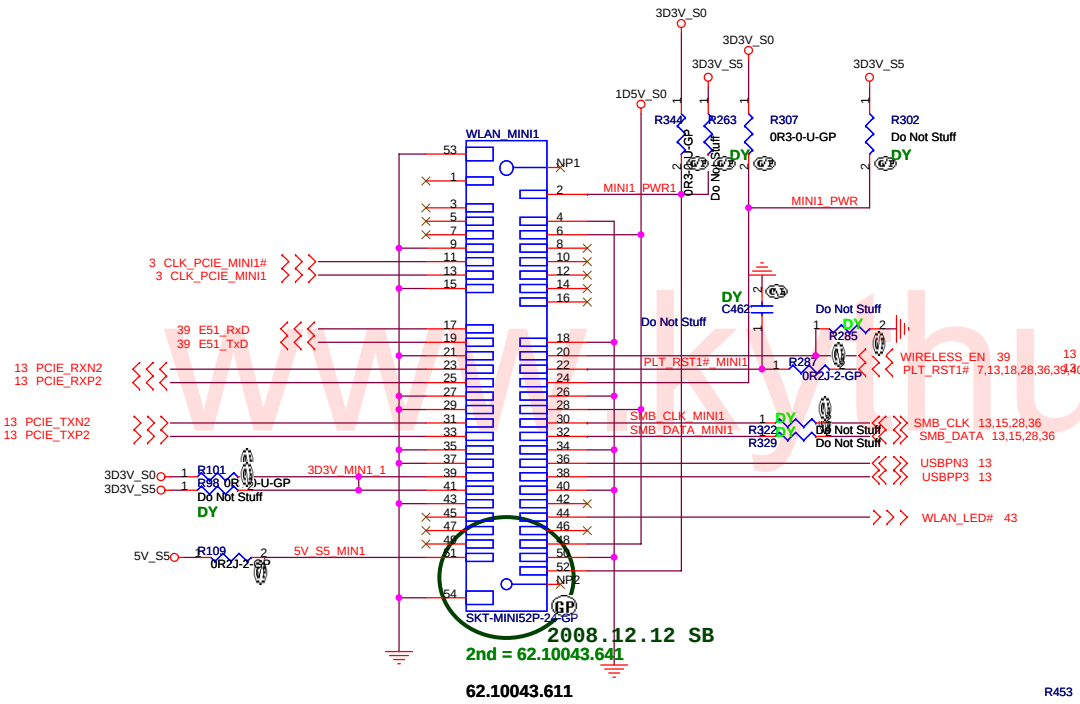
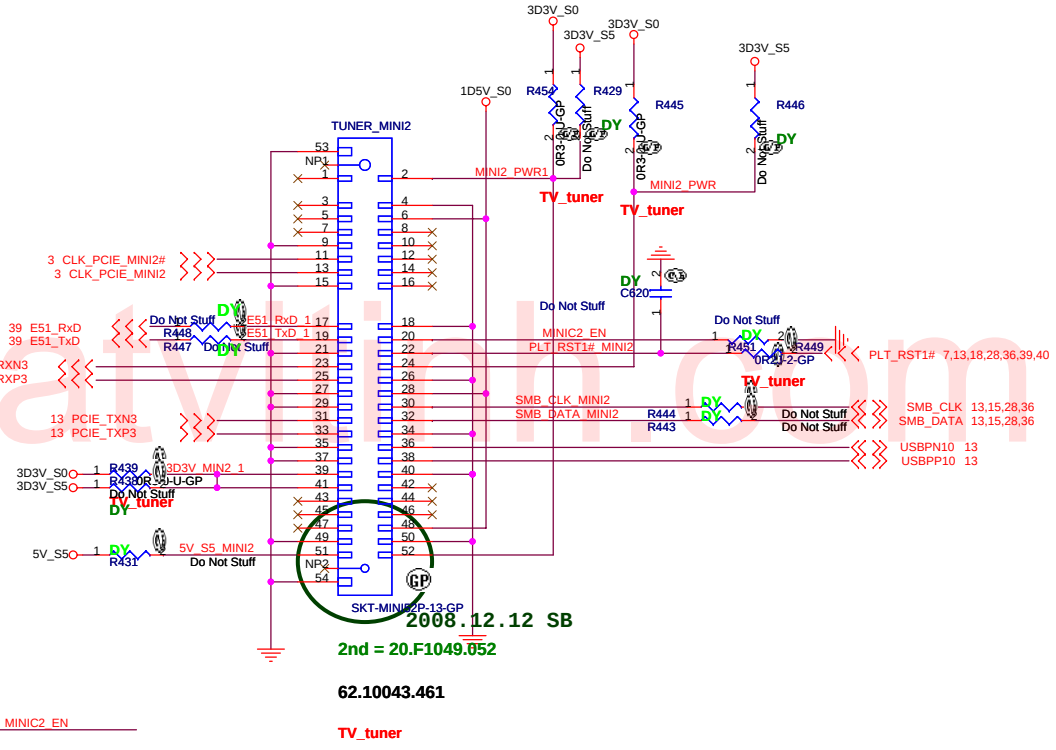
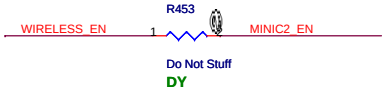
Mini1 Card Connector(WLAN)
Support debug-card

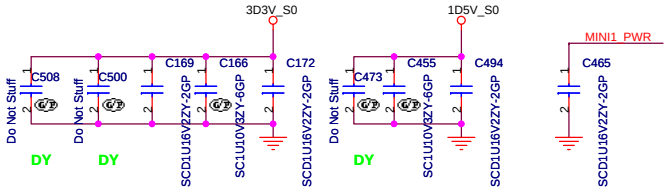


Mini2 Card Connector(TV tuner)

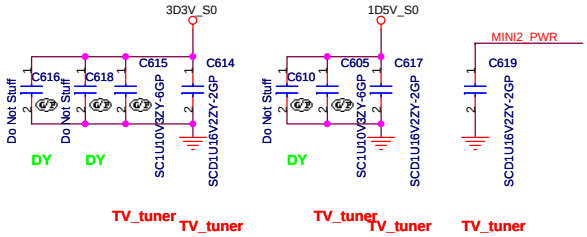




Place near MINI1



Place near MINIC2



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD***	
Size A3	Document Number **JM70-MV**	Rev **SB**
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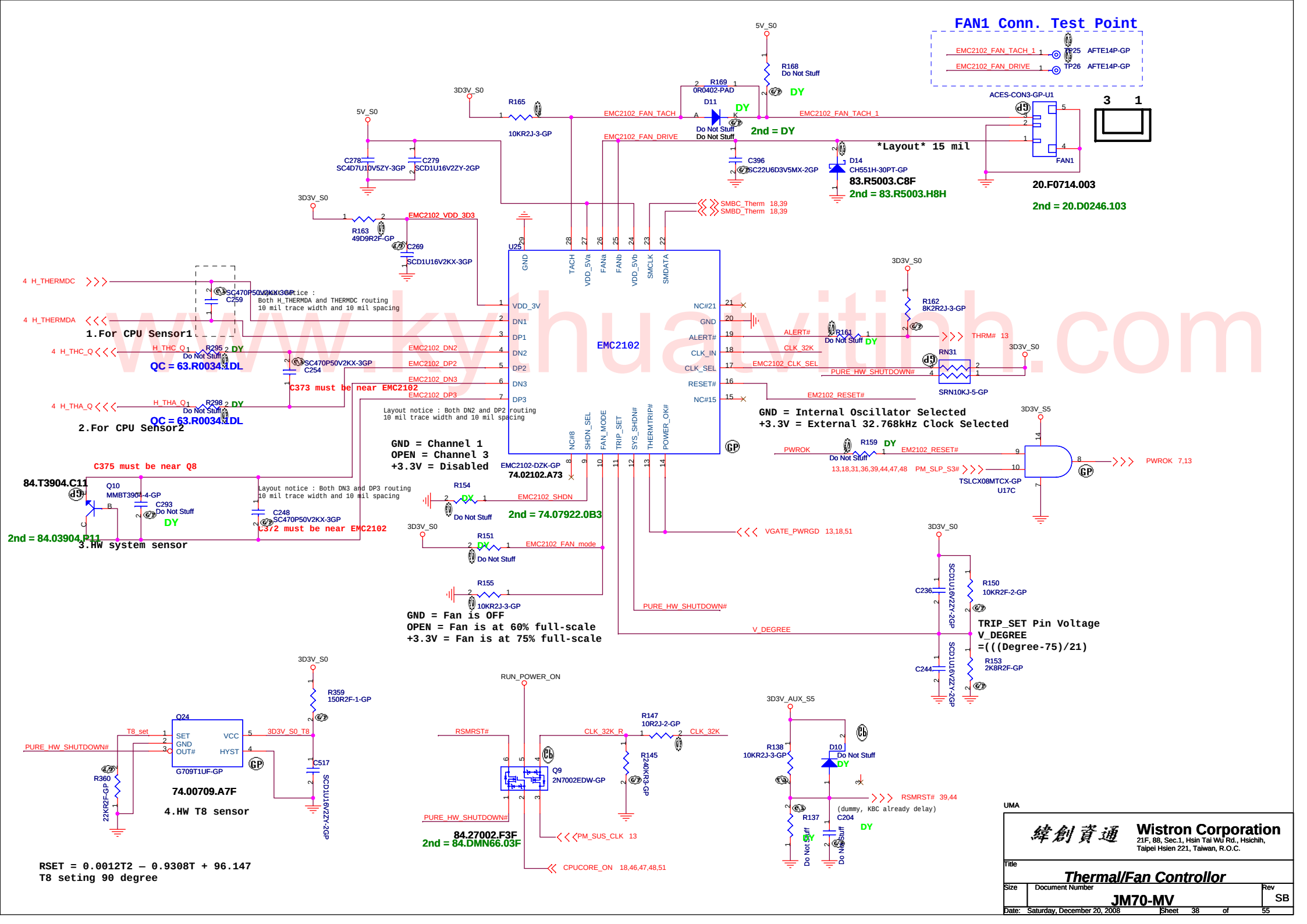

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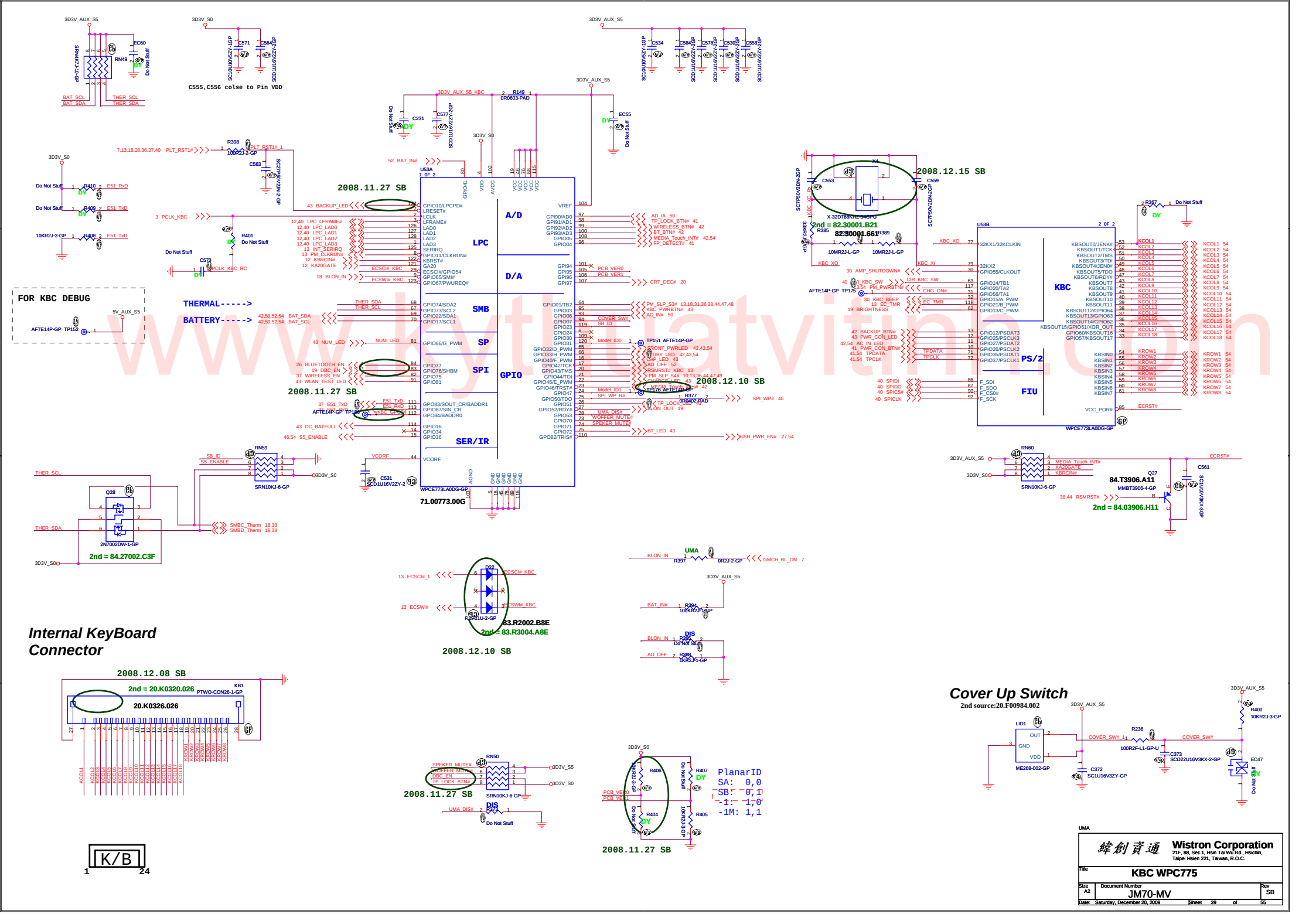

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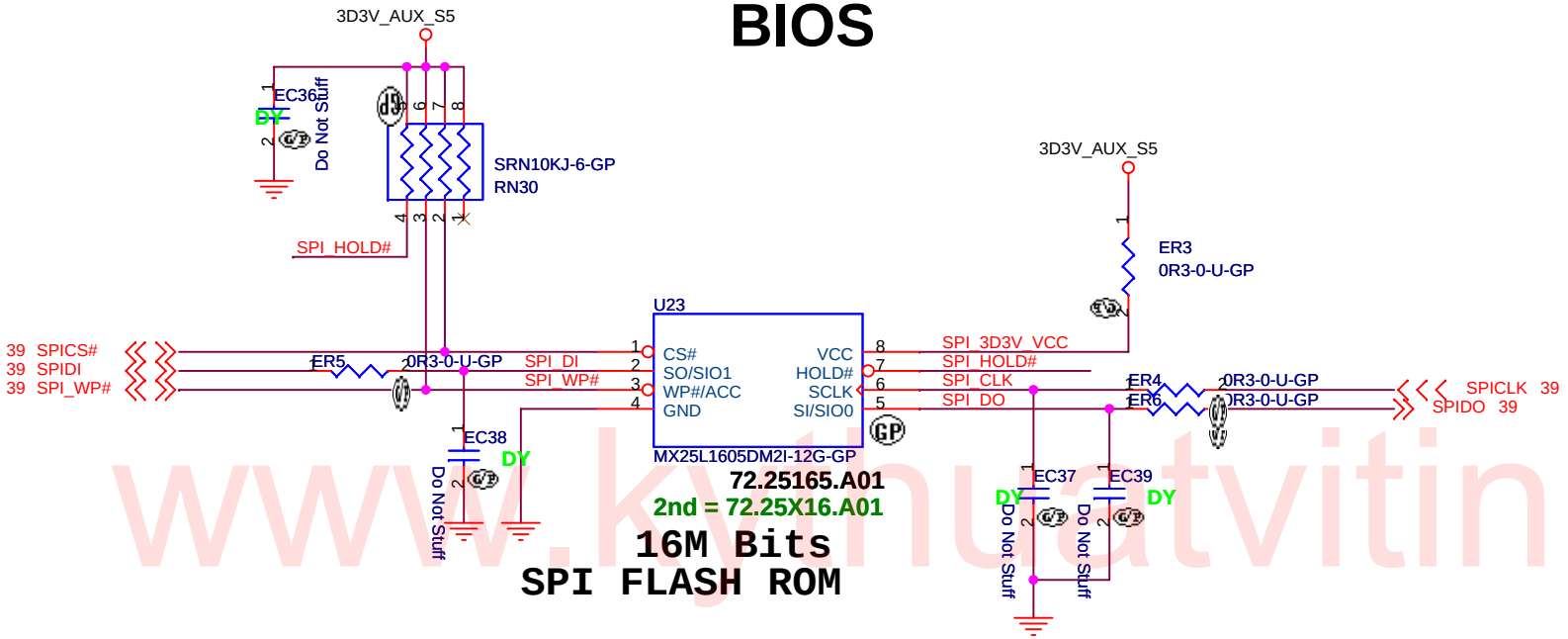
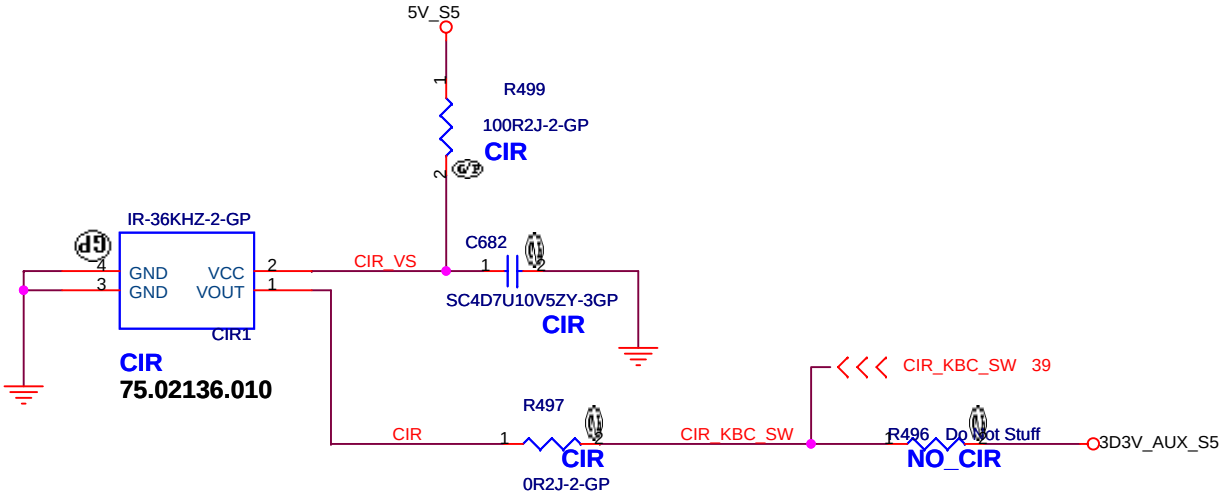
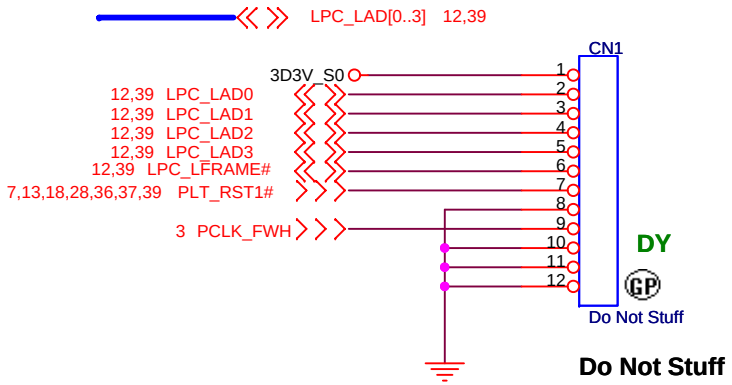
BIOS



VISHAY CIR Module



GOLDEN FINGER FOR DEBUG BOARD



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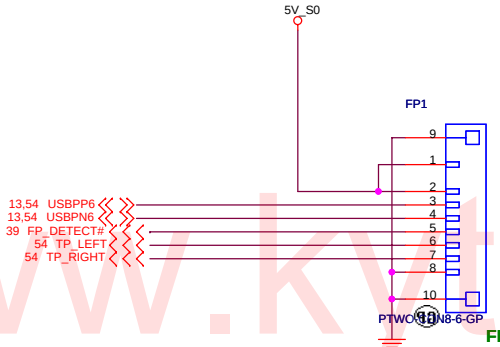
Finger printer

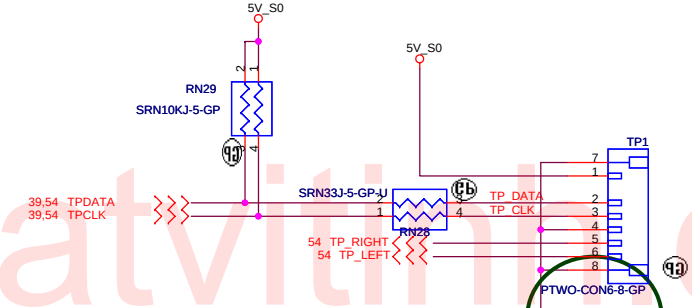


FP
20.K0381.008

F/P
8 1

2nd = 20.K0315.008

Touch Pad



T/P
6 1

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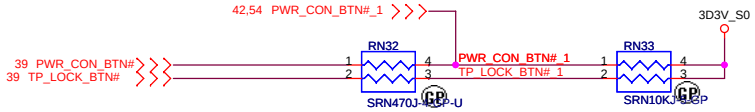
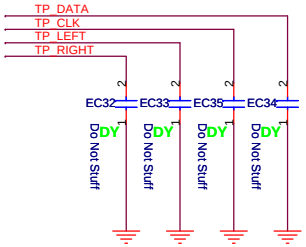
2nd = 20.K0403.006

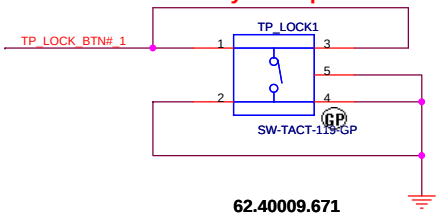
2008.12.08 SB





TP_LOCK key

Note. main with 2nd symbol pin define different



62.40009.671

2nd = 62.40012.101

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Title	*Touch PAD and FP*	
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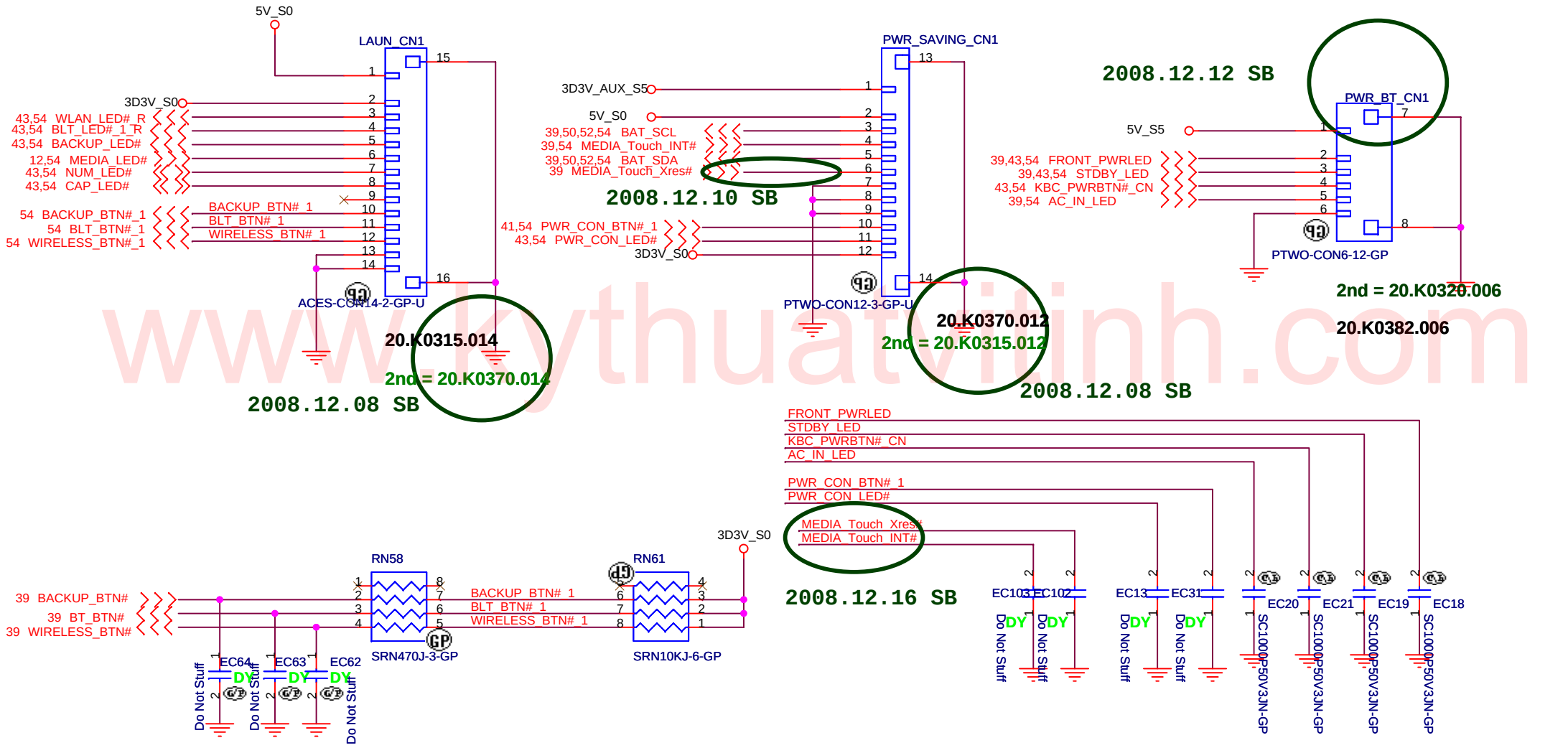

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Title	***Launch CN***	
Size A4	Document Number **JM70-MV**	Rev **SB**
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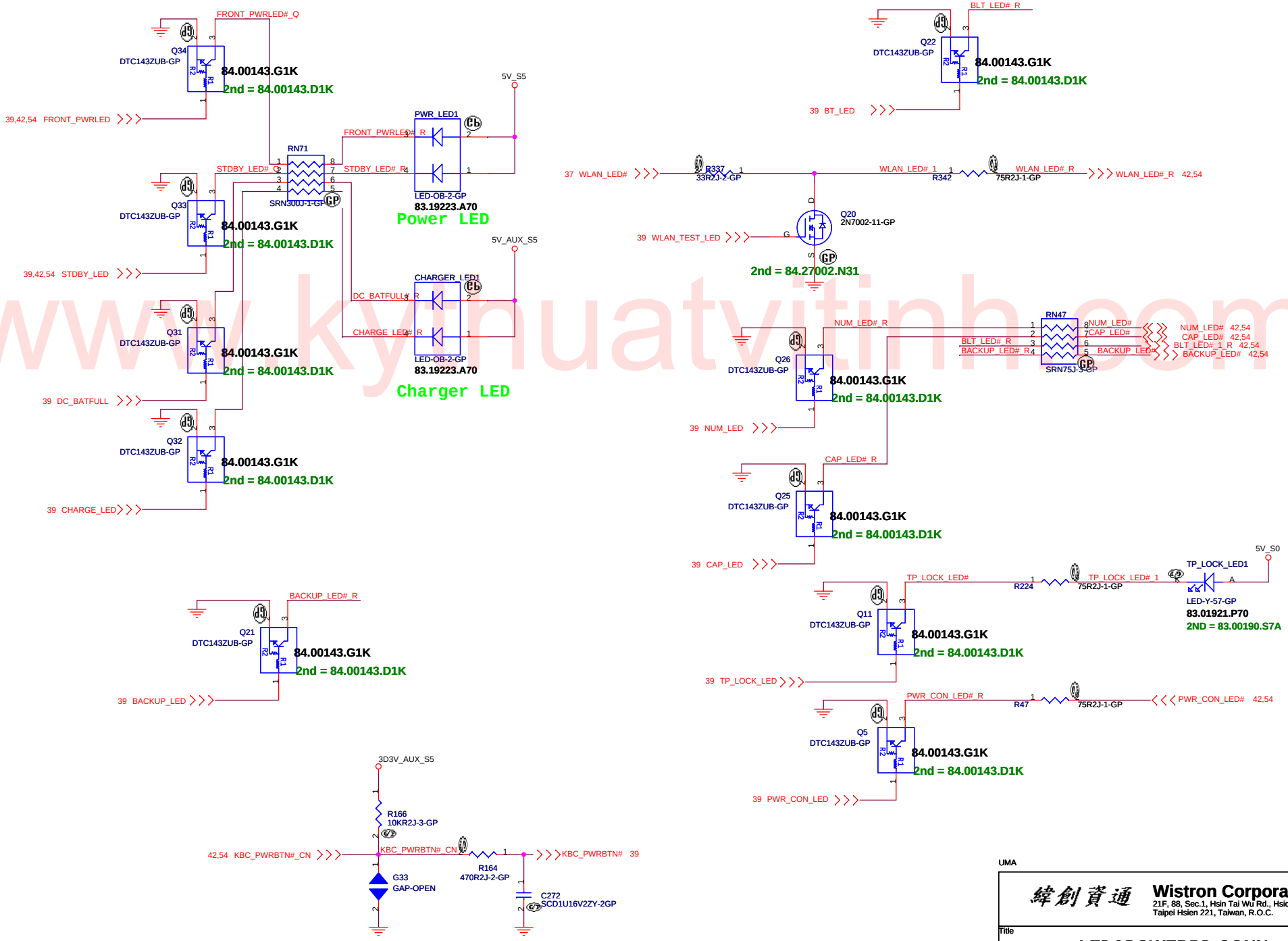
LED



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Title: ***LED&POWERBD CONN***

Size | Document Number: **JM70-MV** | Rev: SB

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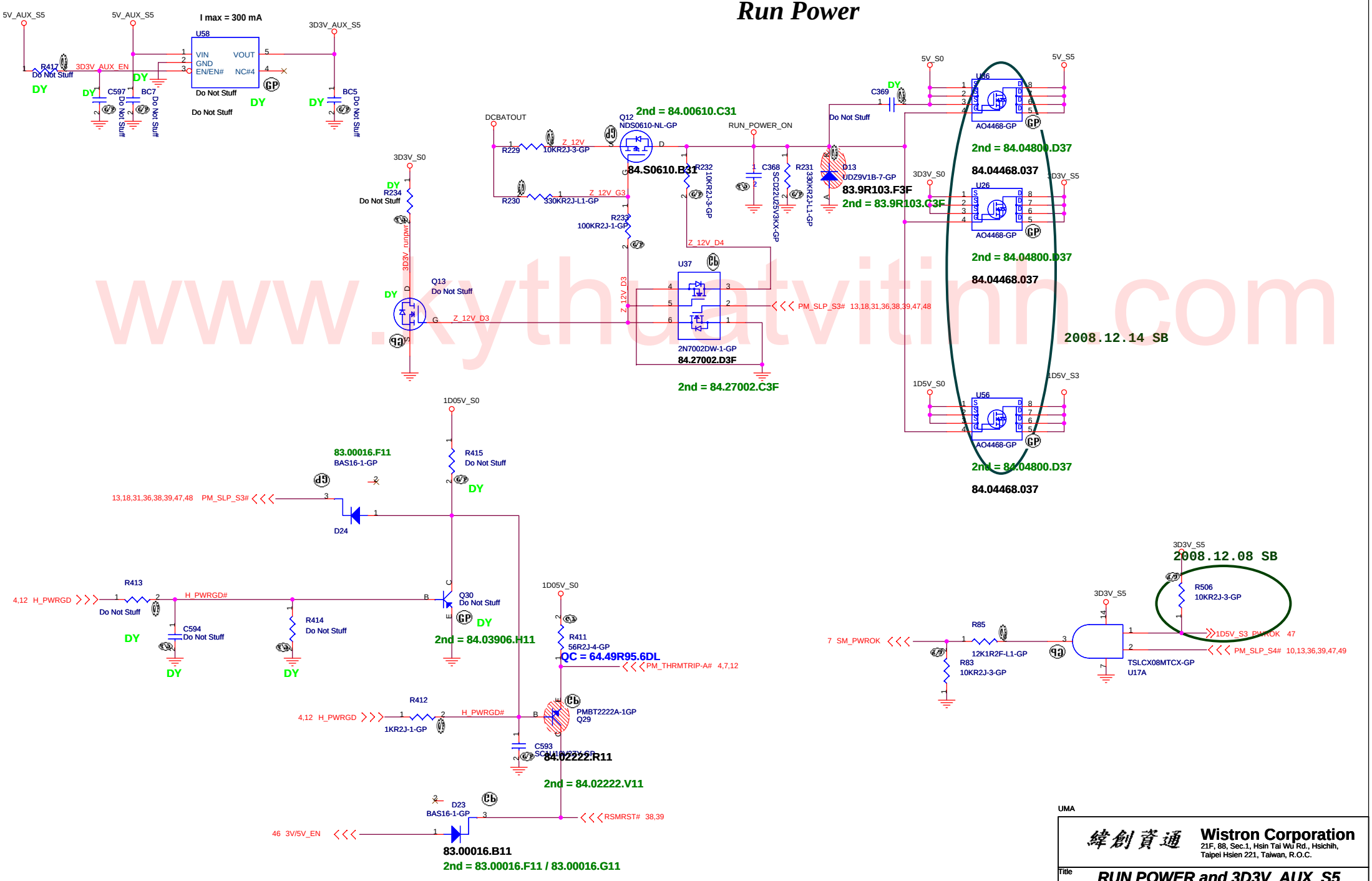
Aux Power 3D3V_AUX_S5

Run Power



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Title: RUN POWER and 3D3V_AUX_S5

Size | Document Number: JM70-MV | Rev: SB

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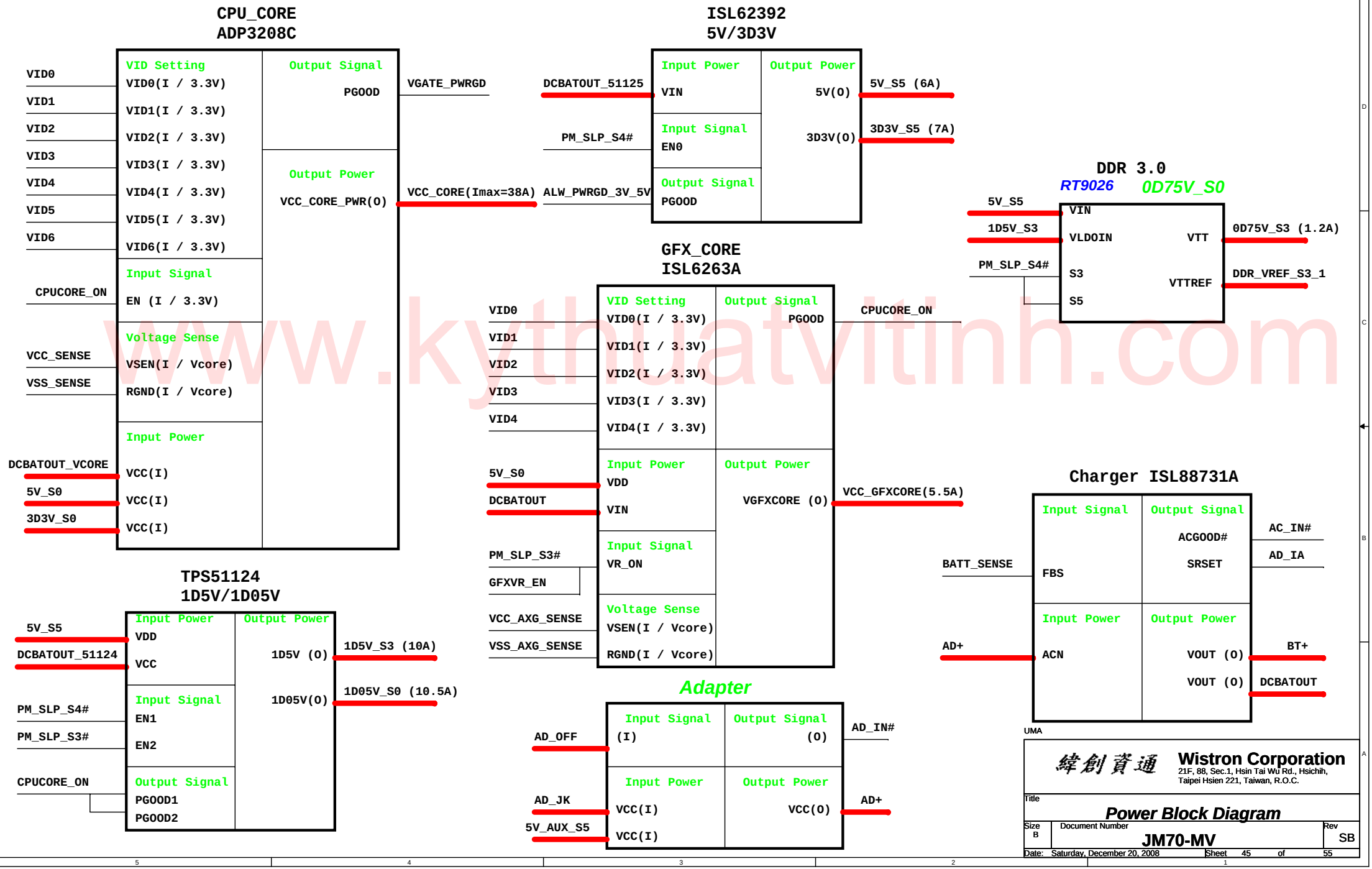

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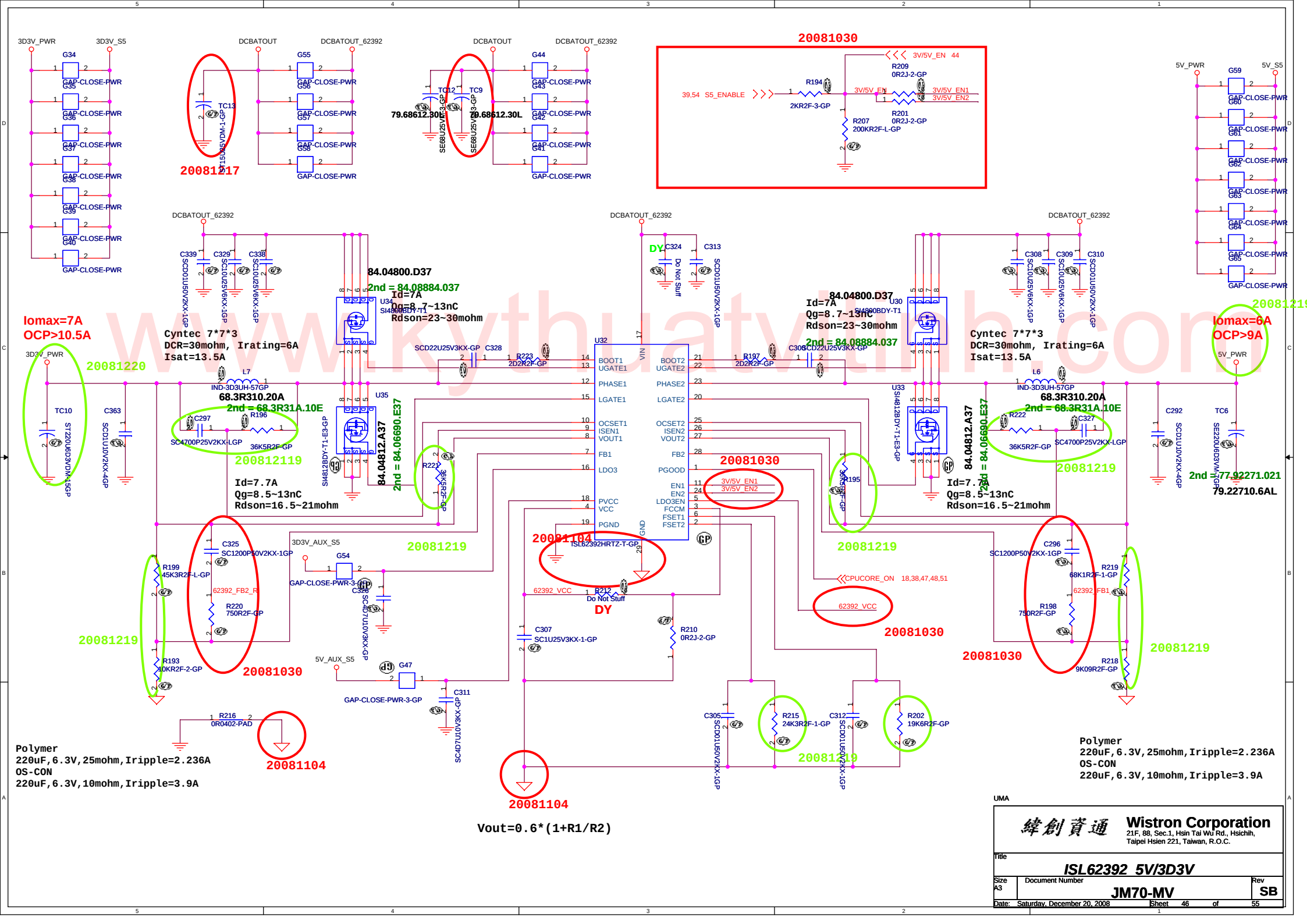

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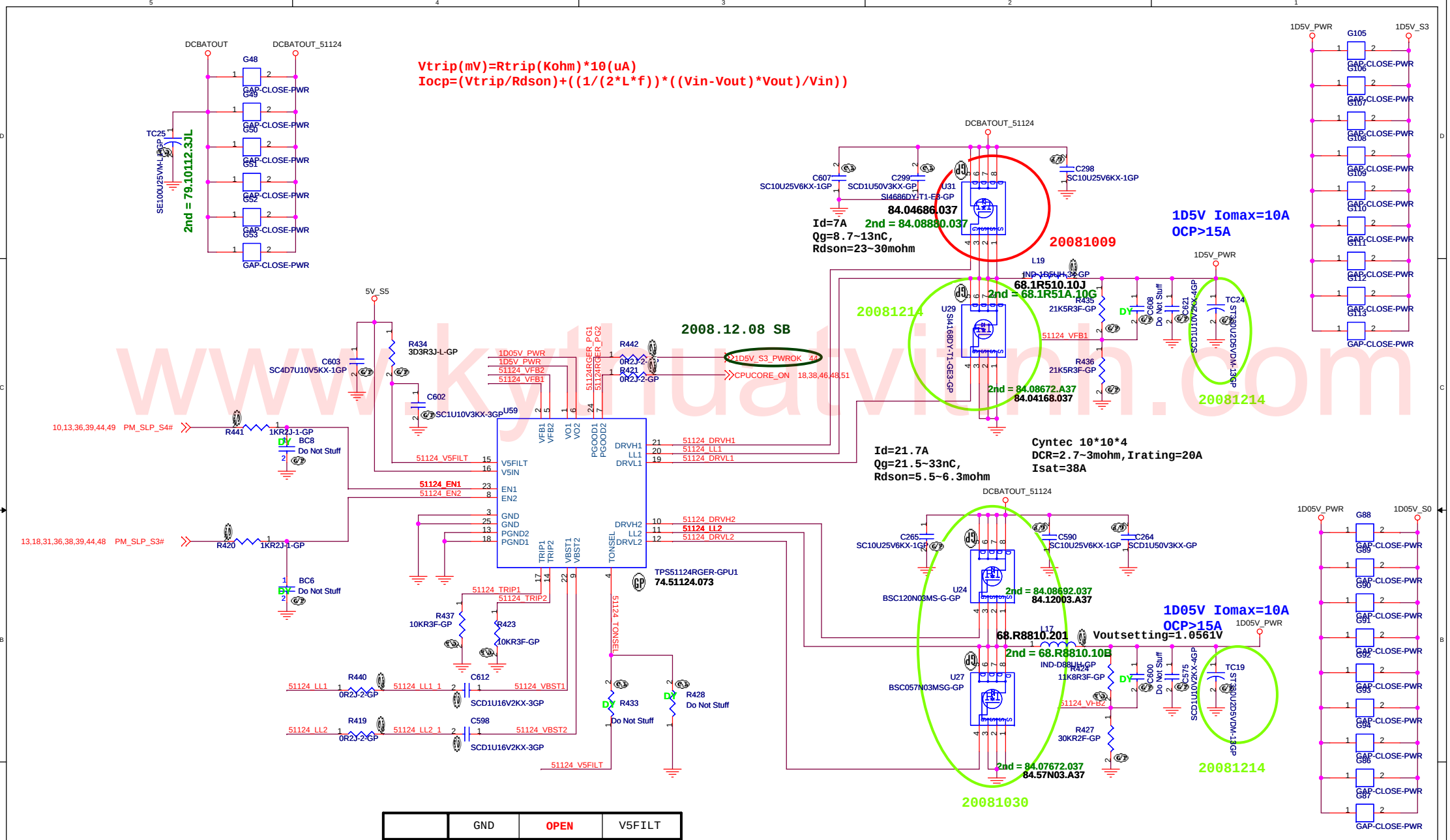

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

UMA

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Title: ***TPS51124_1D5V_1D05V***

Size: A3 | Document Number: **JM70-MV** | Rev: **SB**

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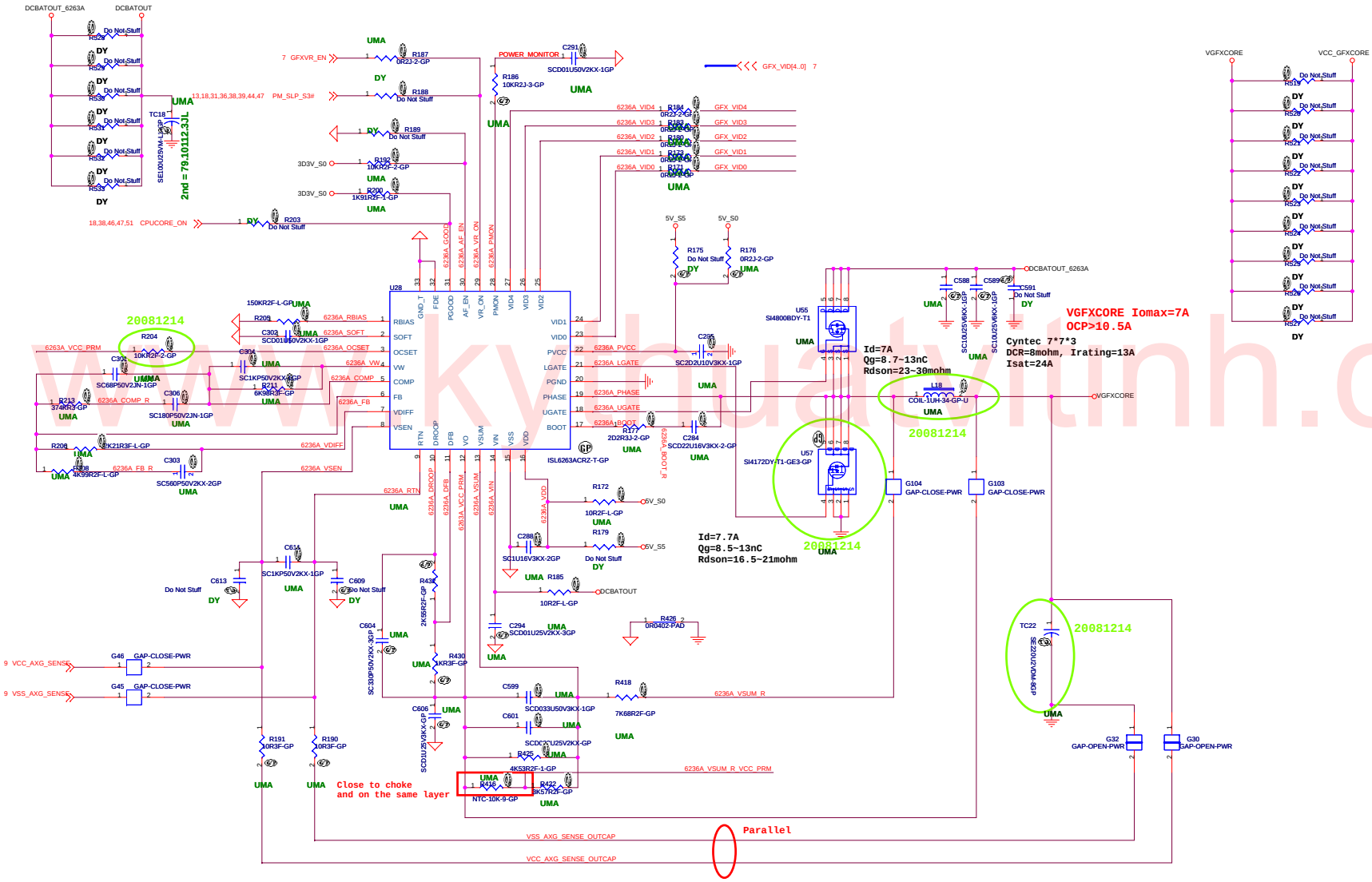

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Title: *ISL6263A_GFX CORE*

Size	Document Number	Rev
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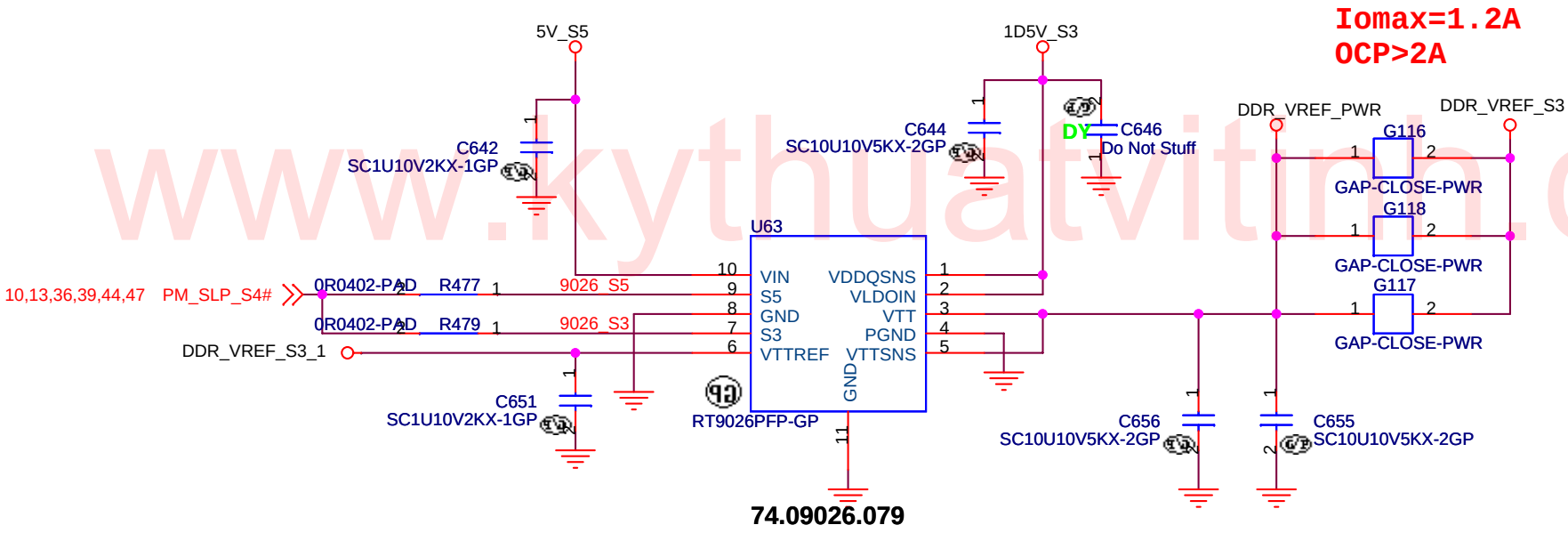

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Title	***0D75V***	
Size A	Document Number **JM70-MV**	Rev **SB**
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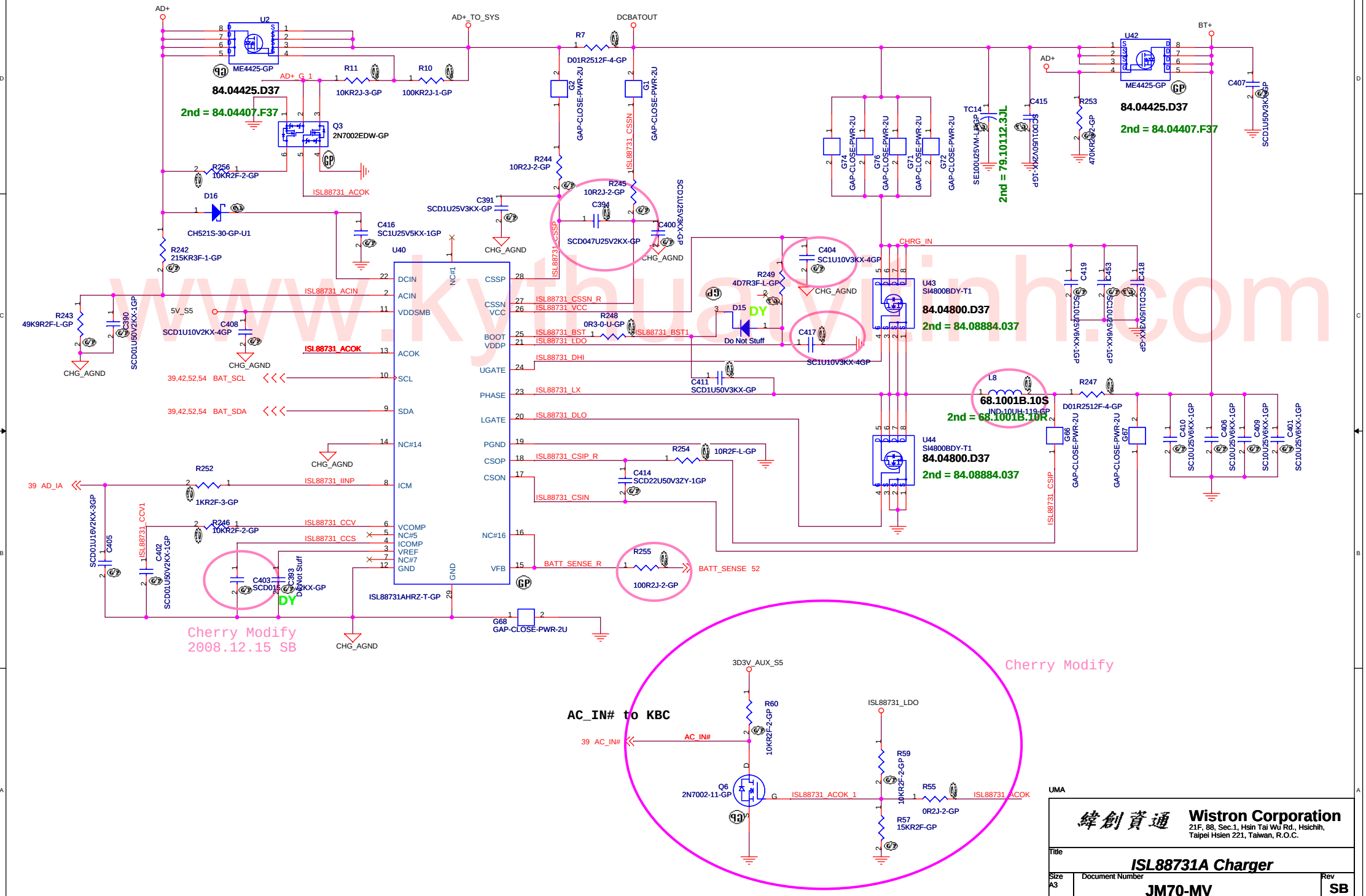

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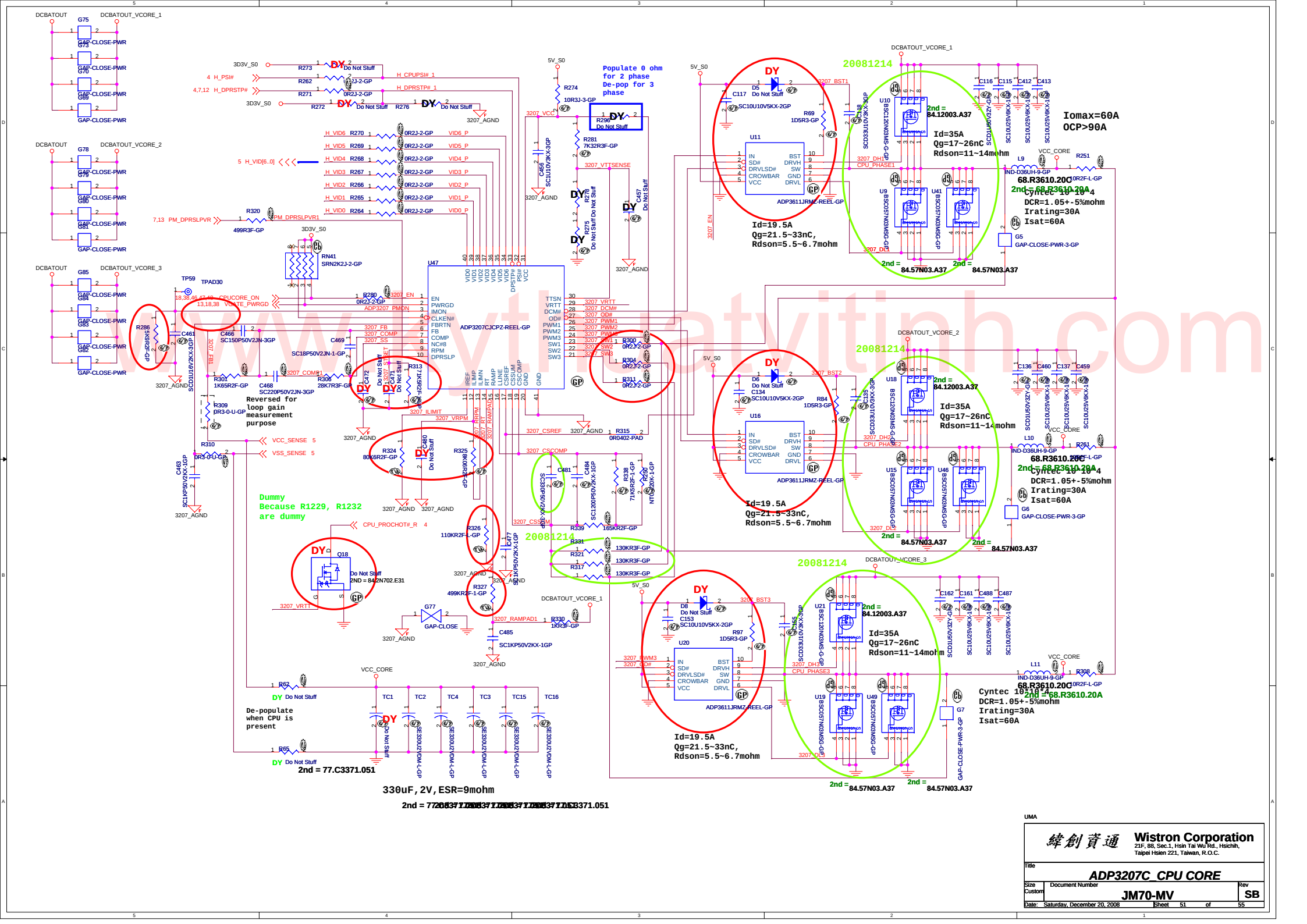

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Title: ADP3207C_CPU CORE

Size: Custom | Document Number: JM70-MV | Rev: SB

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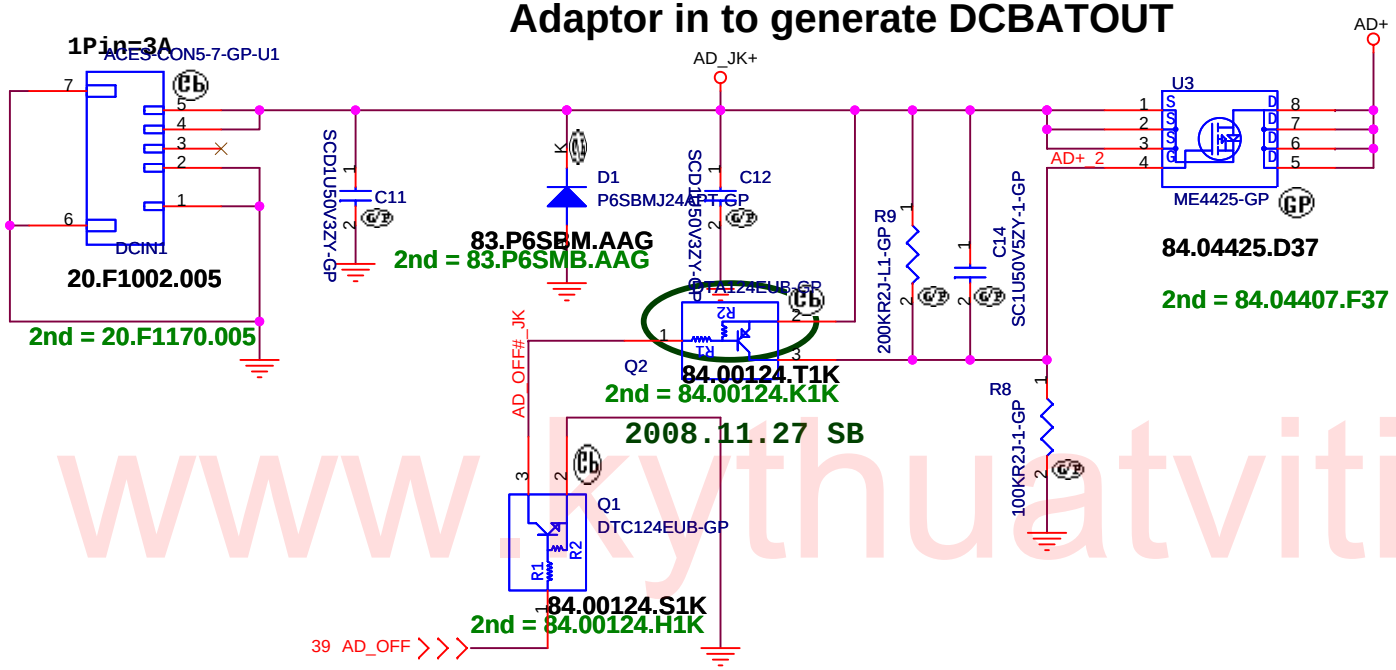
Adaptor in to generate DCBATOUT



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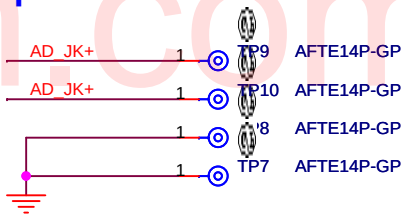
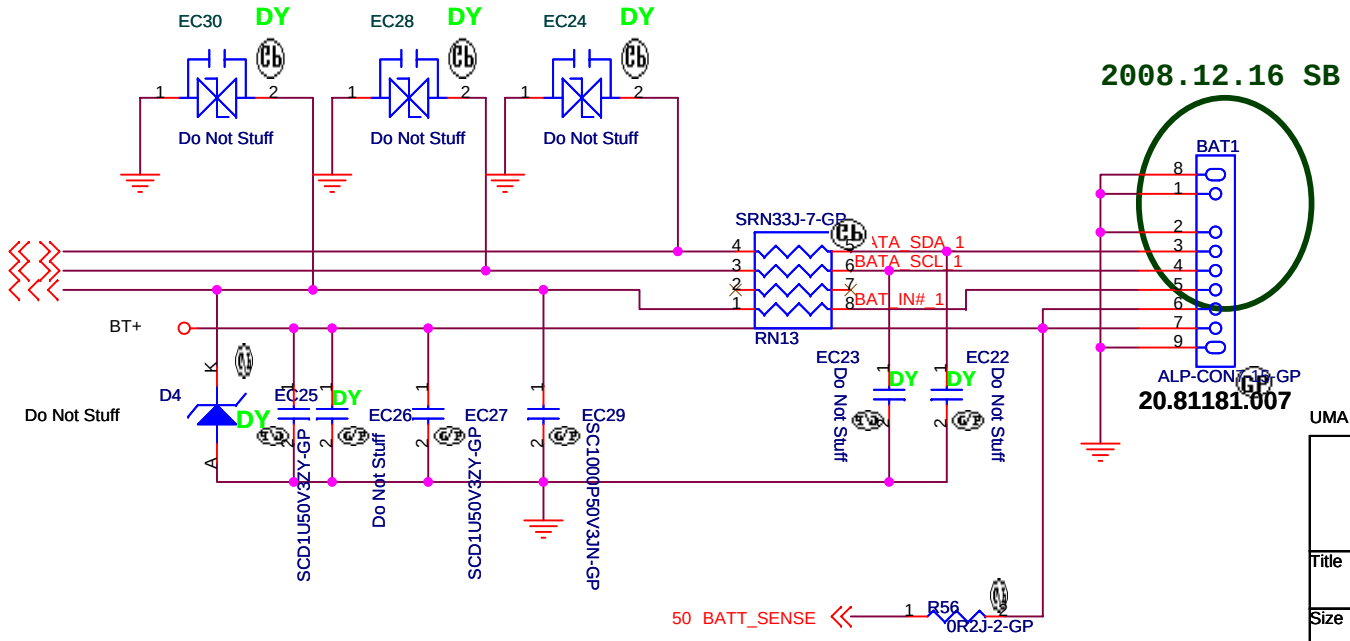
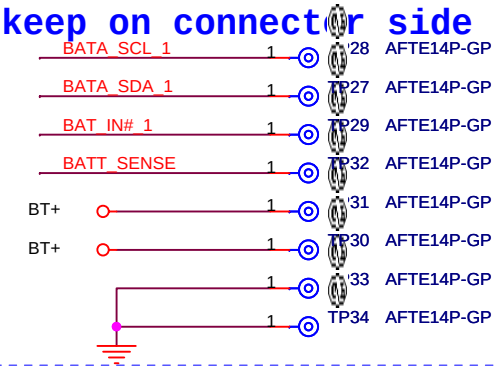
KB Conn. Test Point keep on connector side



MAIN BATTERY CONNECTOR



BAT1 Conn. Test Point keep on connector side



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Title	AD&BTY CONNECTER	
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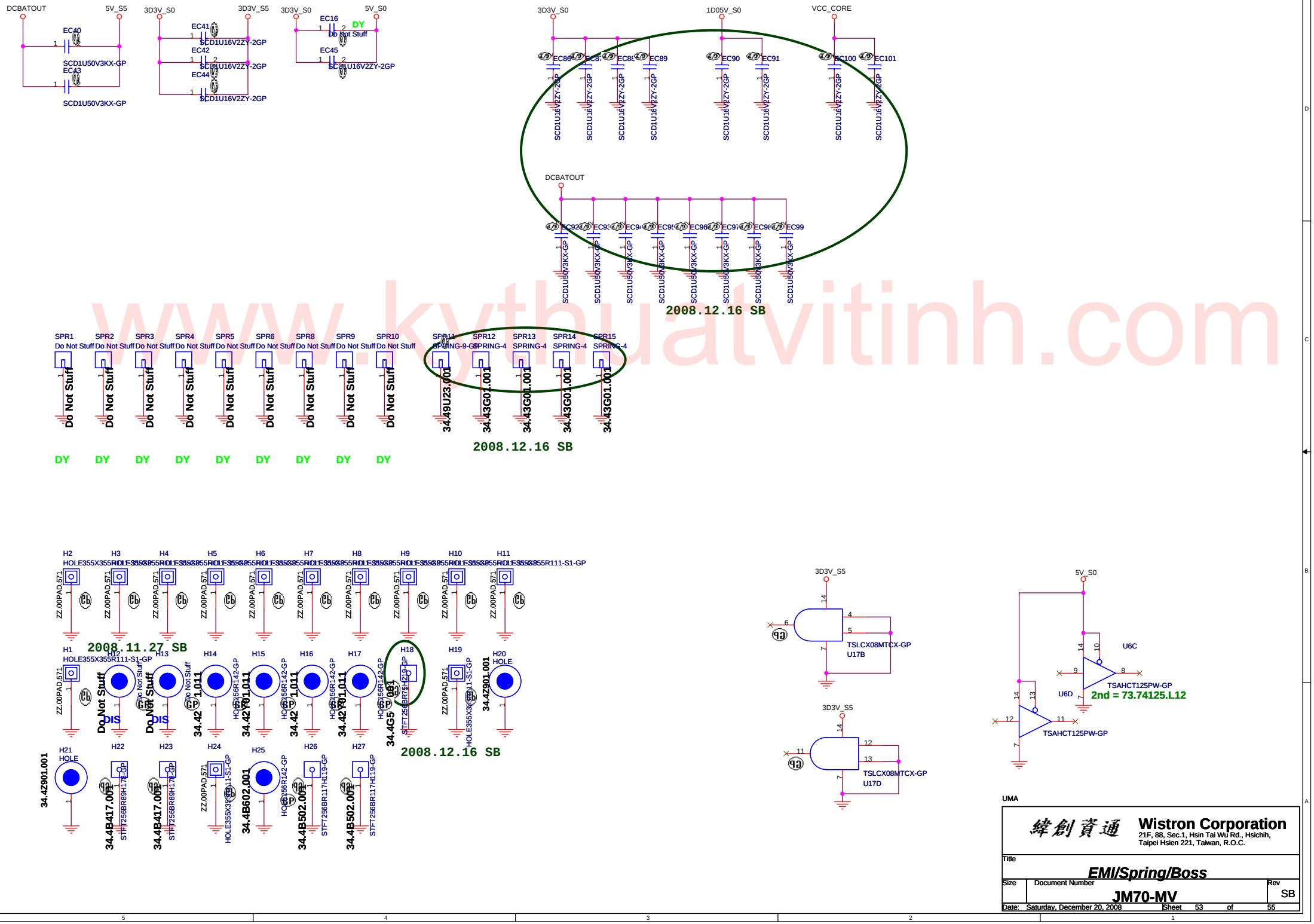

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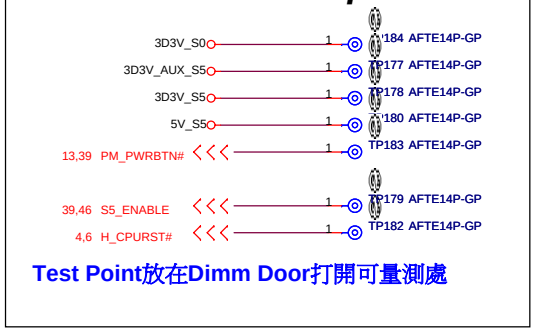
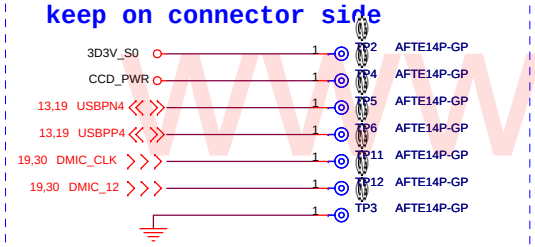
Check test point

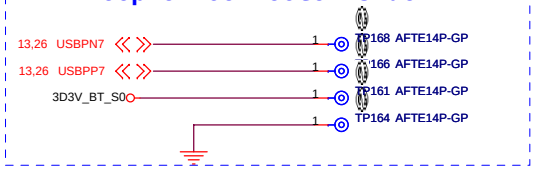


Test Point放在Dimm Door打開可量測處

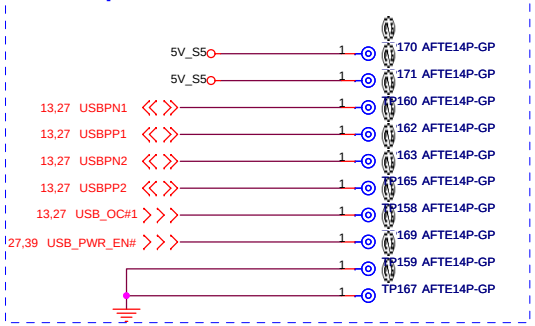
CCD_DMIC_CN1 Conn. Test Point keep on connector side



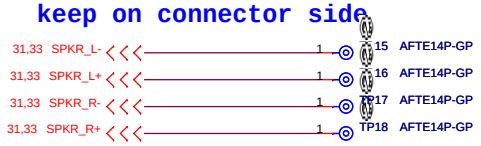
BT Conn. Test Point keep on connector side



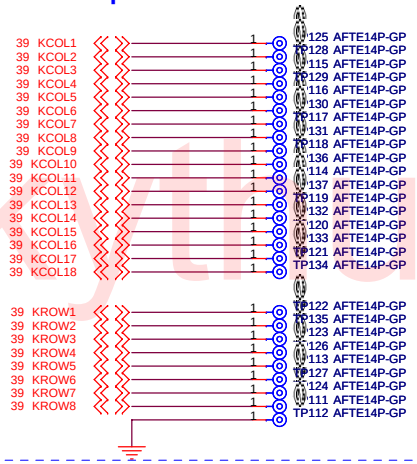
USB_CN1 Conn. Test Point keep on connector side



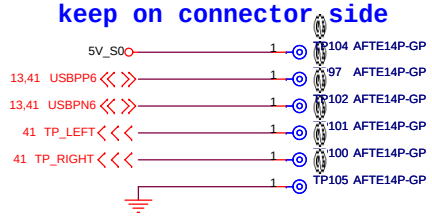
SPKR1 Conn. Test Point keep on connector side



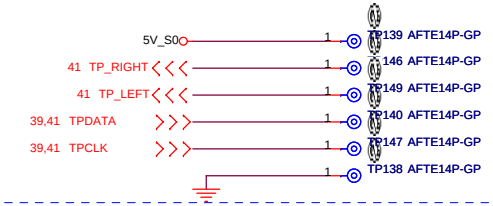
KB1 Conn. Test Point keep on connector side



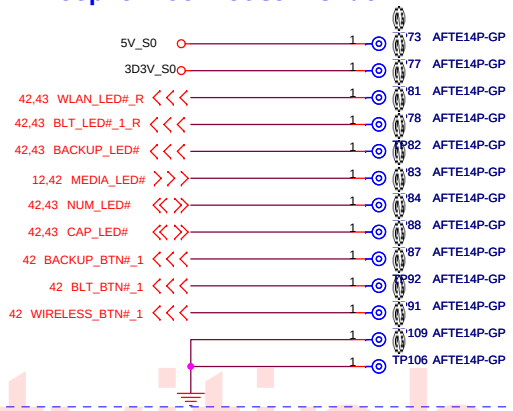
FP test Point keep on connector side



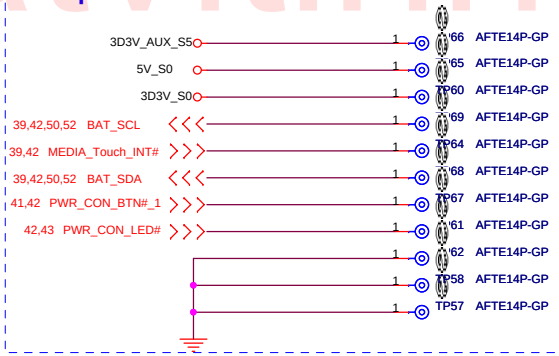
TOUCH PAD Conn. Test Point keep on connector side



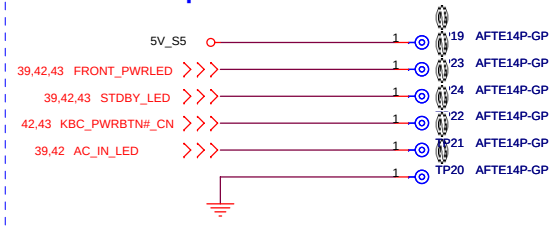
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side



PWR_BT_CN1 Conn. Test Point keep on connector side



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Title		
AFTE_TP		
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Title: ***HISTORY***

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