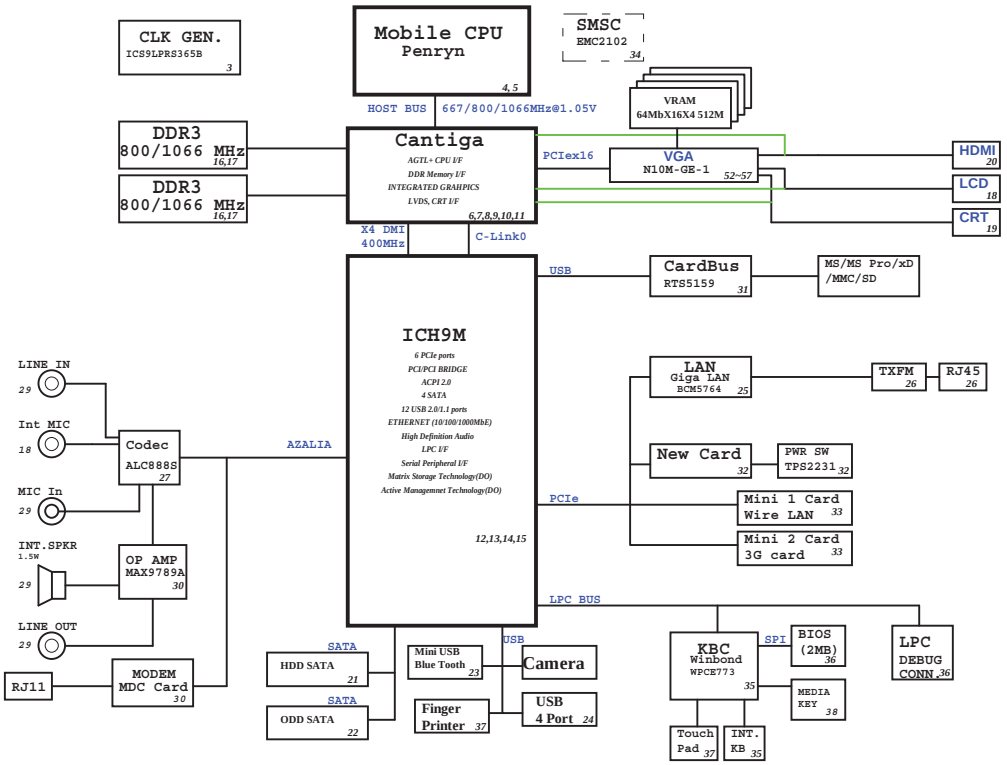
JV50 Block Diagram

Project code: 91.4CG01.001
PCB P/N : 48.4CG01.0SA
REVISION : 08245-SA



PCB STACKUP

TOP		L1
GND		L2
S		L3
S		L4
GND		L5
BOTTOM		L6

SYSTEM DC/DC ISL62392 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44	
1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44	
1D5V_S3	1D1V_S0(2A)

TPS51117 45	
DCBATOUT	FBVDD(4A)

CHARGER ISL88731A 47	
INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC ISL6266A 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE RT8202A 47	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE ISL6263A 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

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File

BLOCK DIAGRAM

Size	Document Number	Rev
A2	JV50	SB

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIE is operational (Default) 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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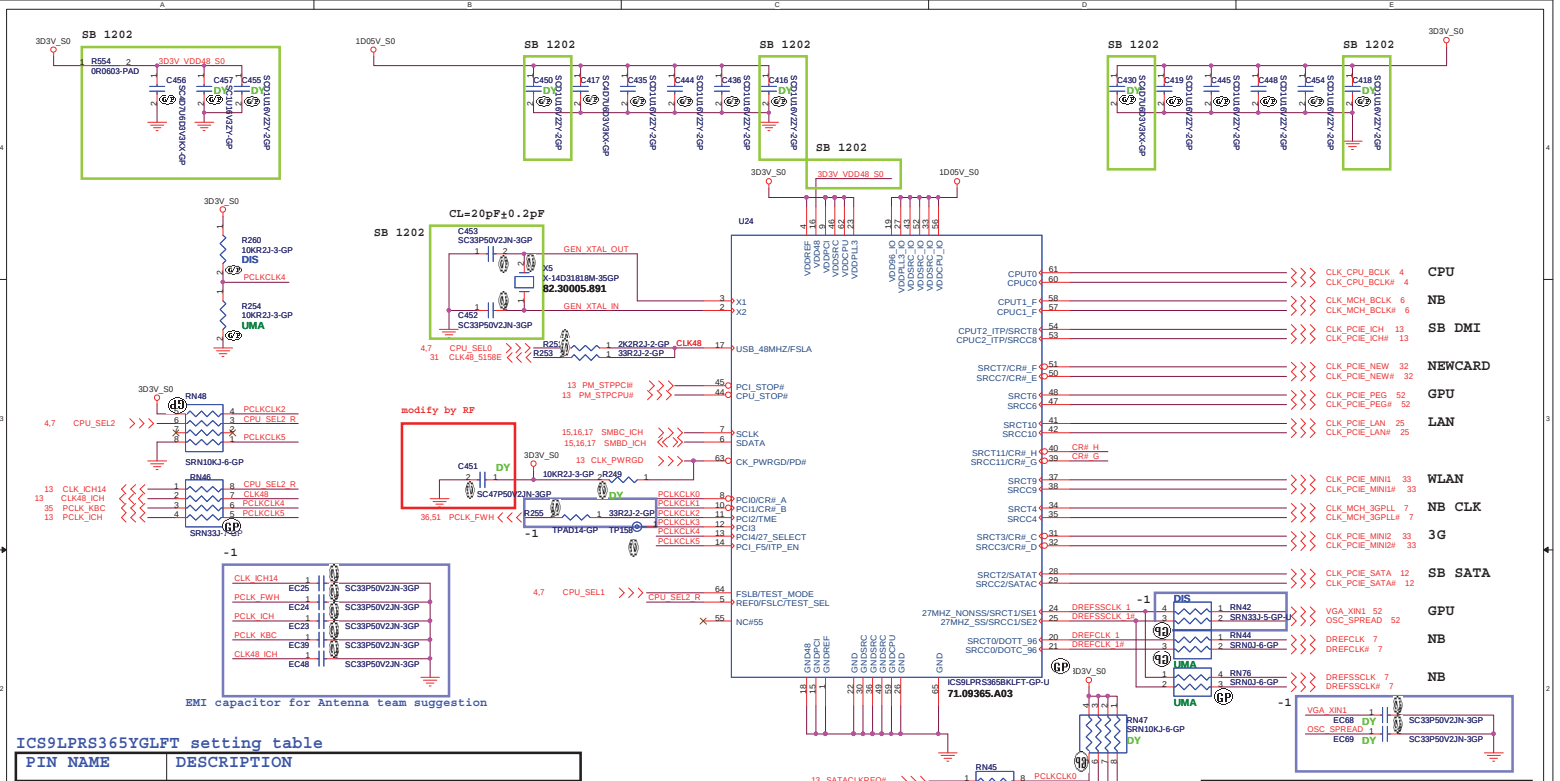
Title: Reference

Size	Document Number	Rev
A3	JV50	SB

Date: Thursday, January 08, 2009 Sheet 2 of 60



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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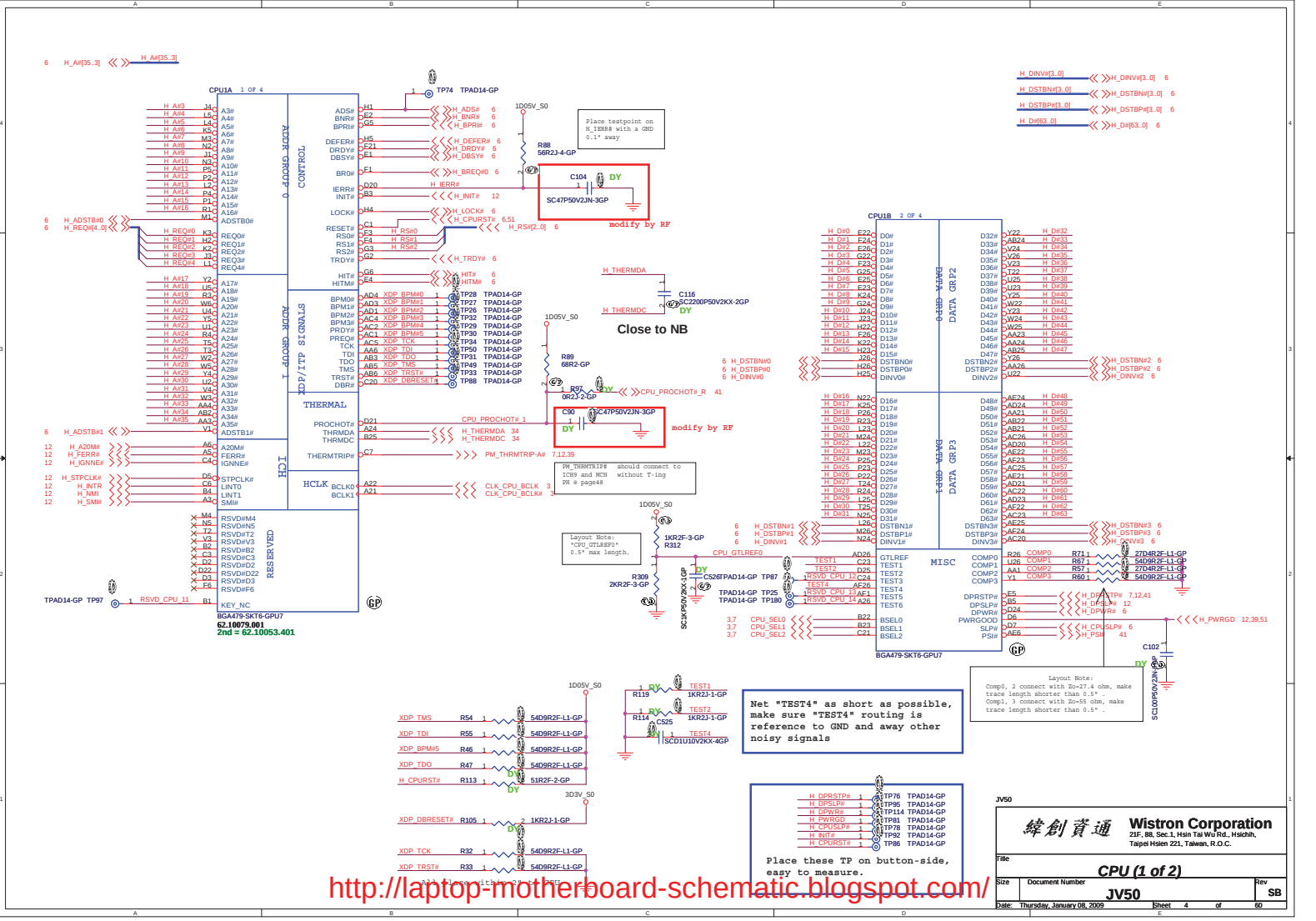
Title: Clock Generator

Size: | Document Number: JV50 | Rev: SB

Date: Thursday, January 08, 2009 | Sheet 3 of 60



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Title: CPU (1 of 2)

Size	Document Number	Rev
	JV50	SB

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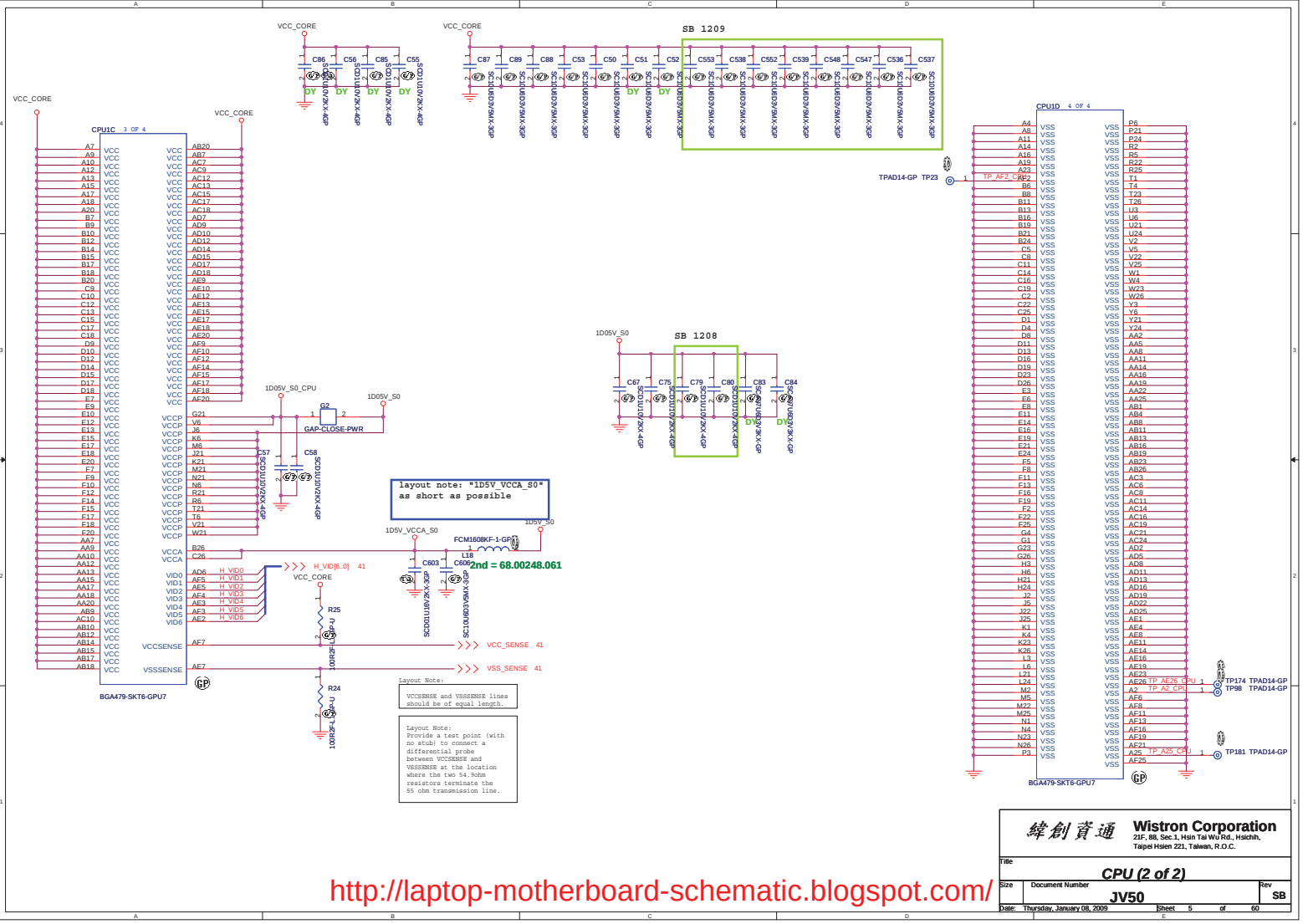

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Title	CPU (2 of 2)	
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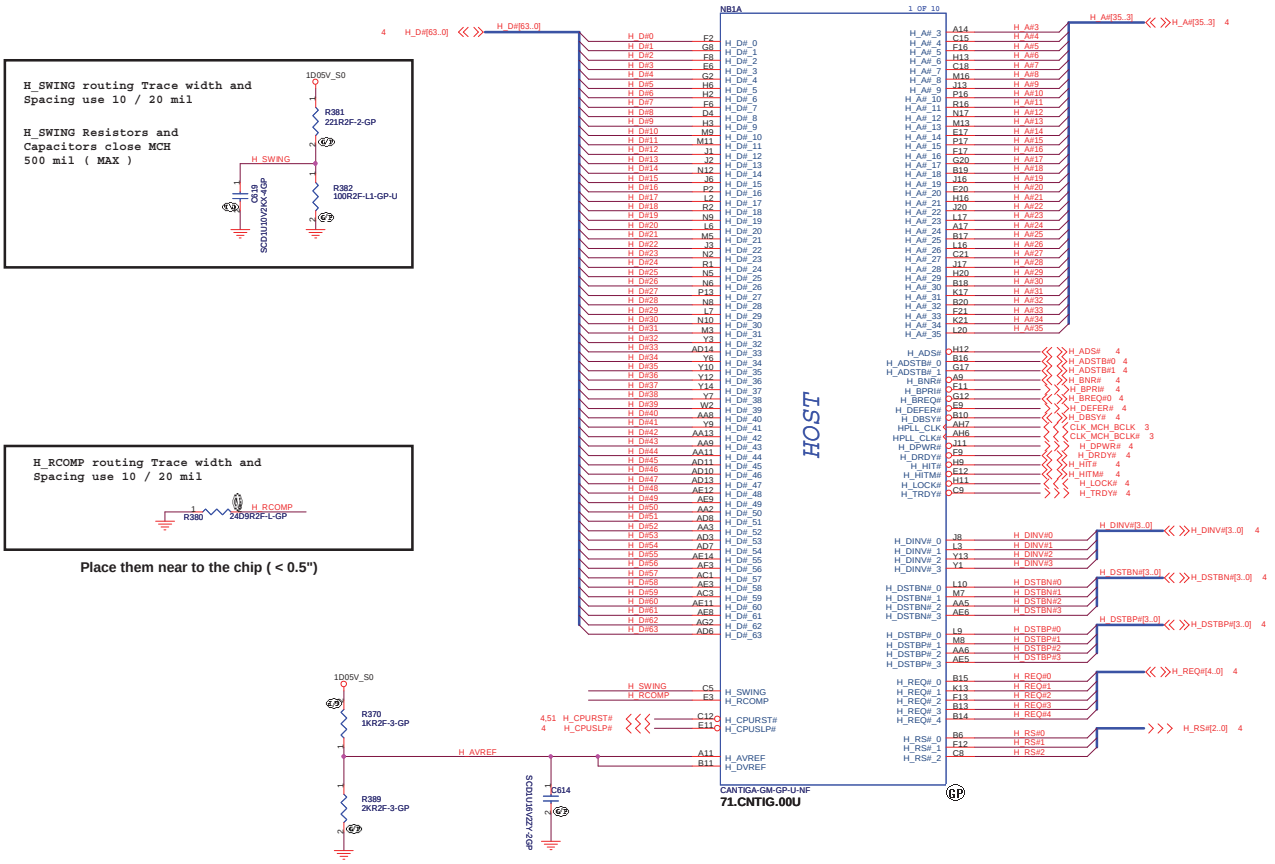

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Title: *Cantiga (1 of 6)*

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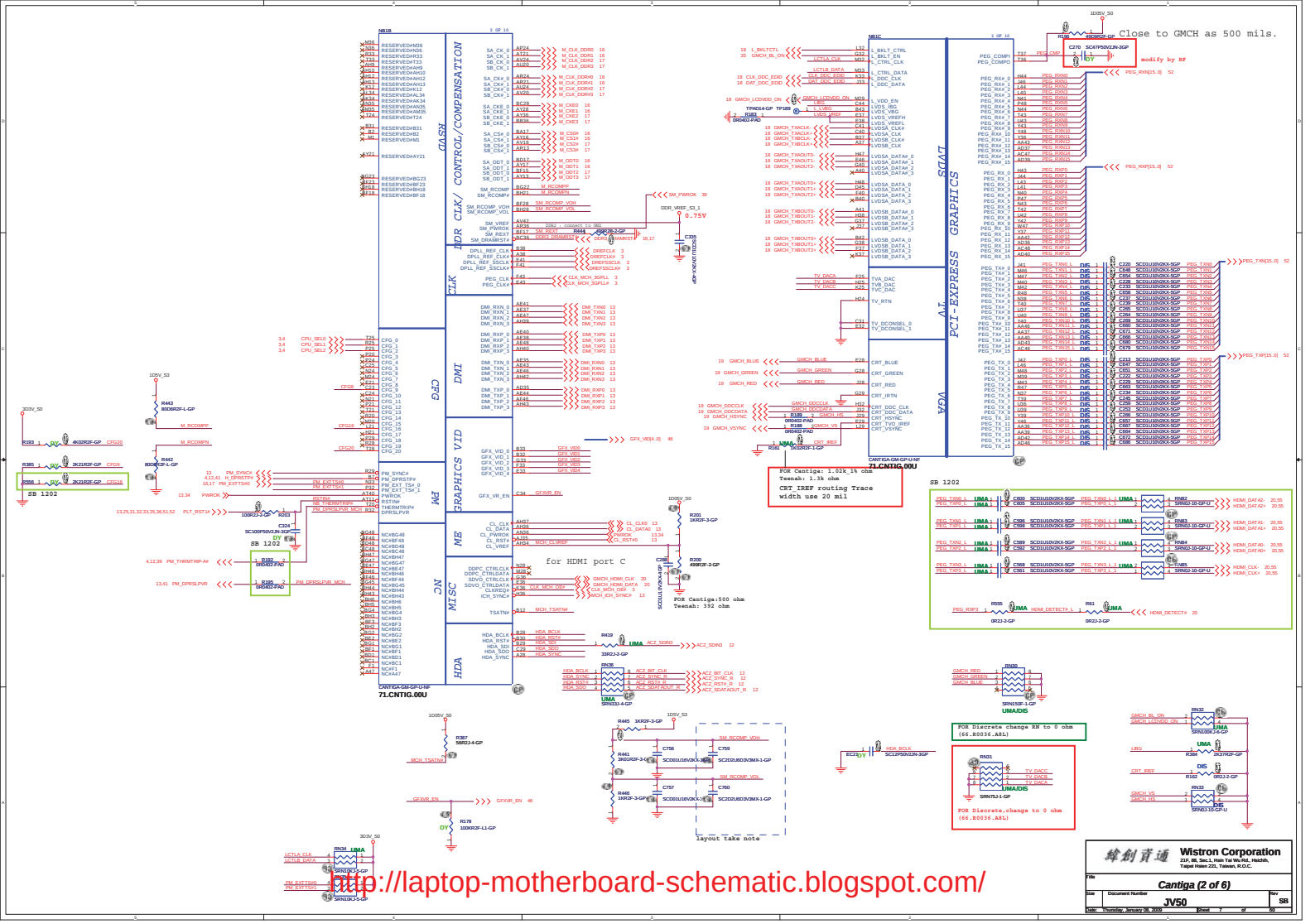

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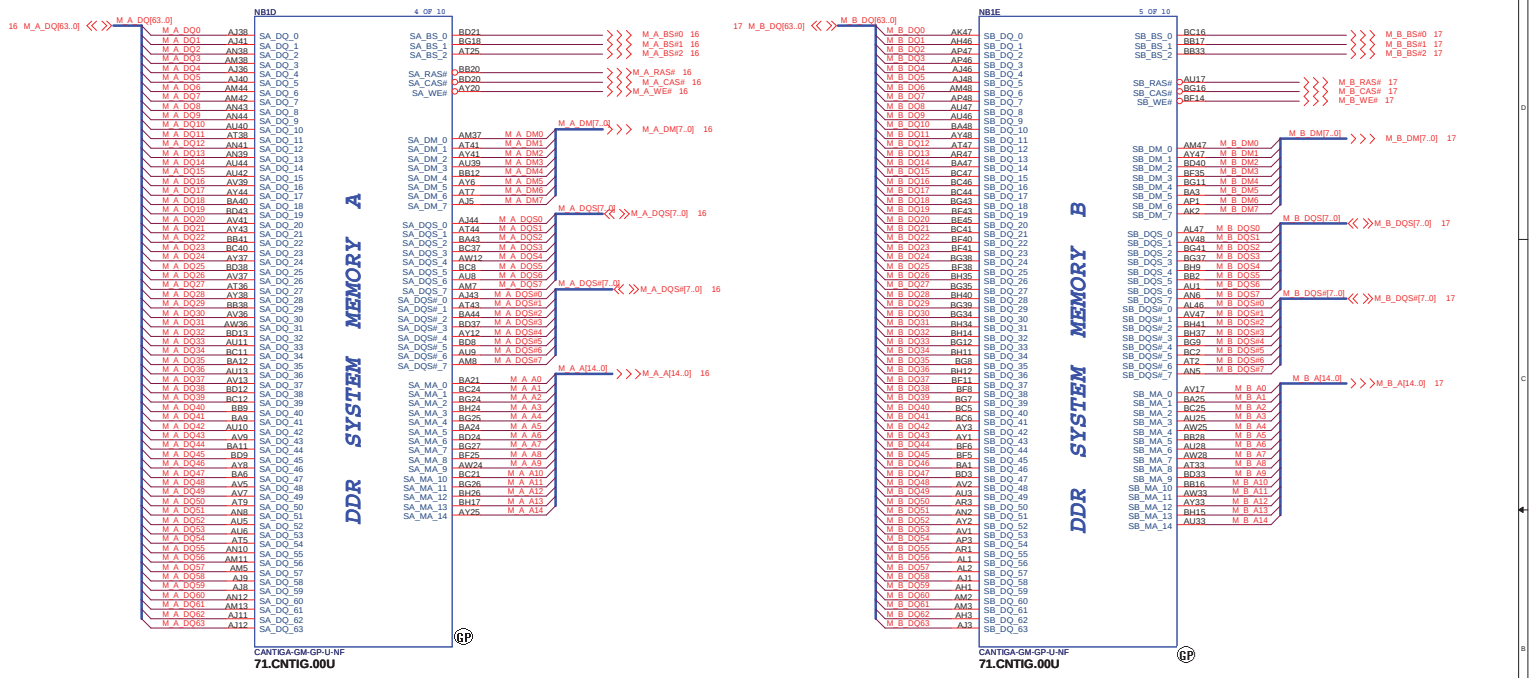

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Title: ***Cantiga (3 of 6)***

Size	Document Number	Rev
	JV50	SB

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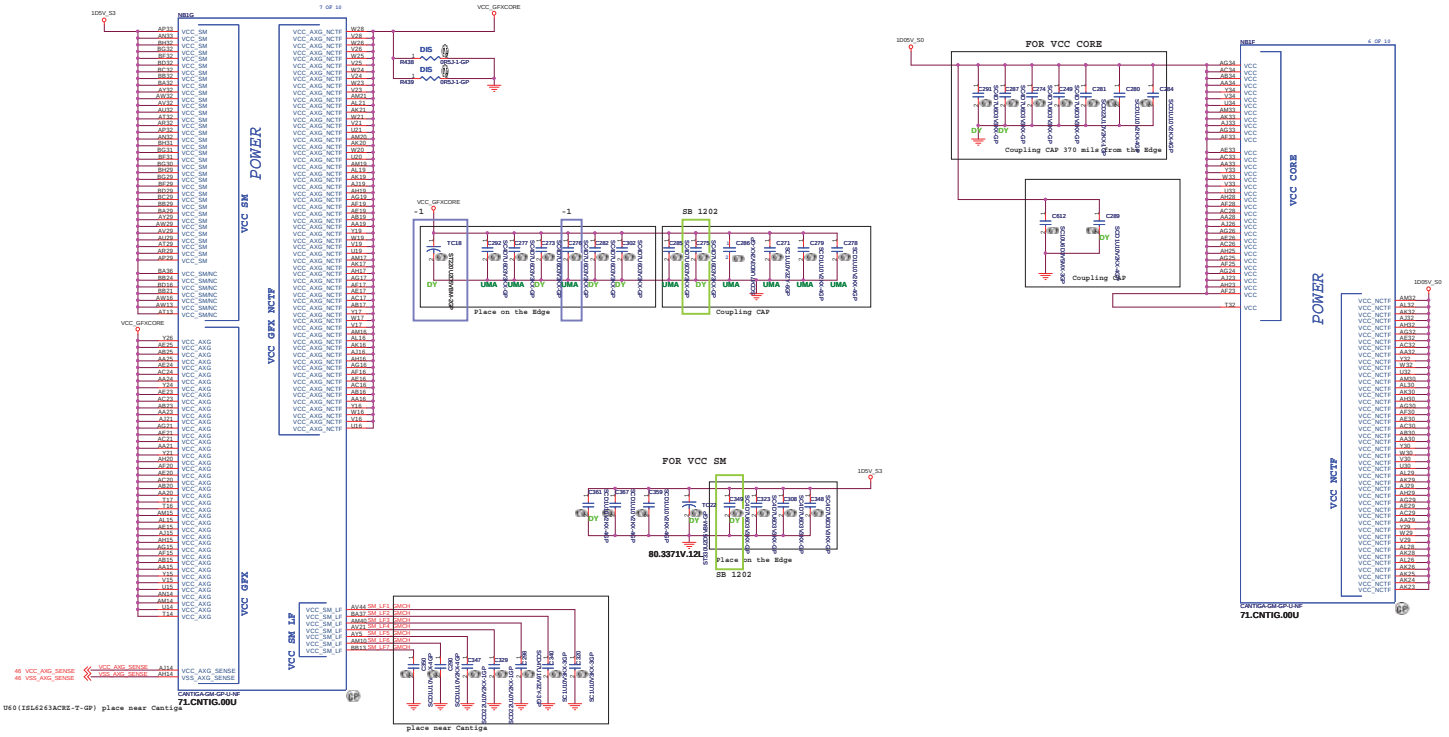

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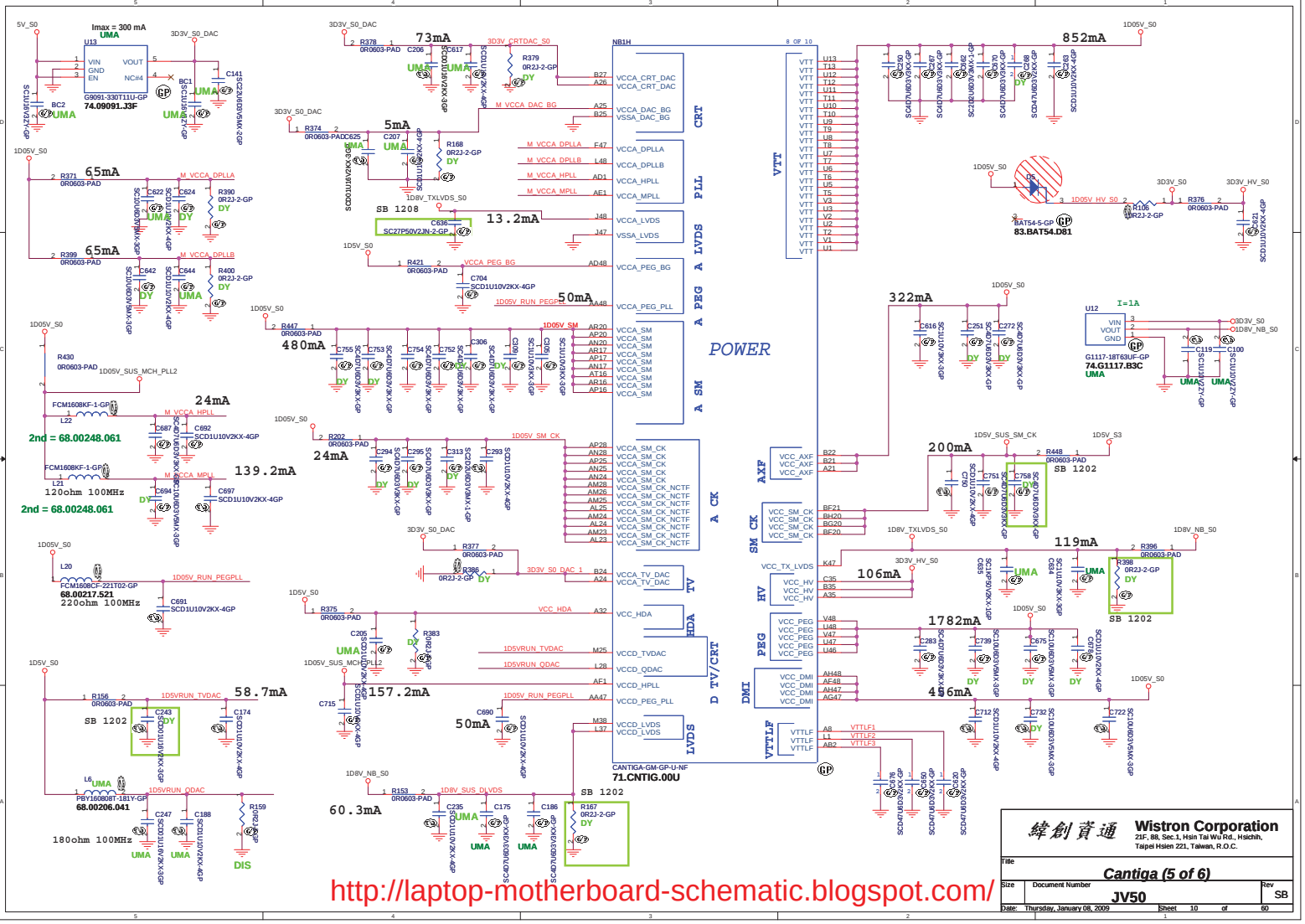

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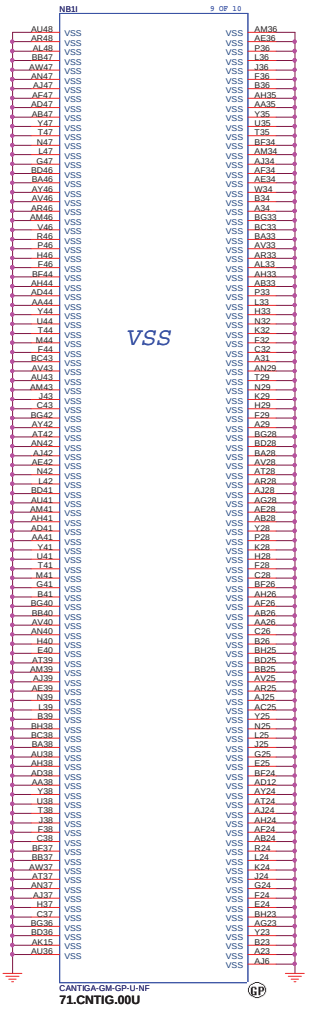

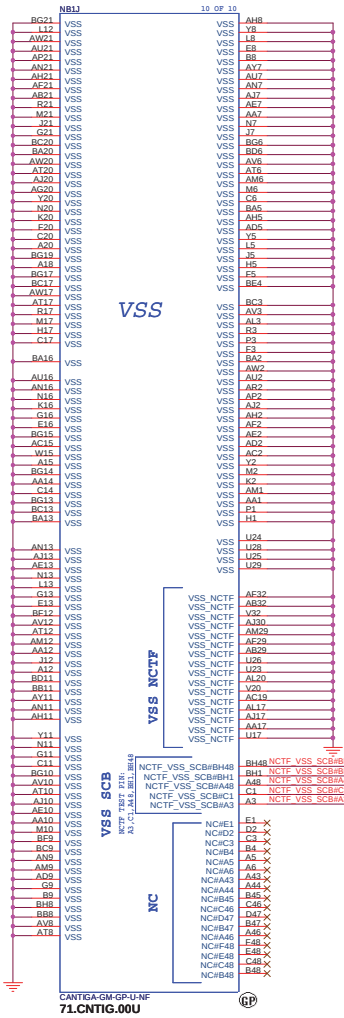

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Title: Cantiga (6 of 6)

Size	Document Number	Rev
	JV50	SB

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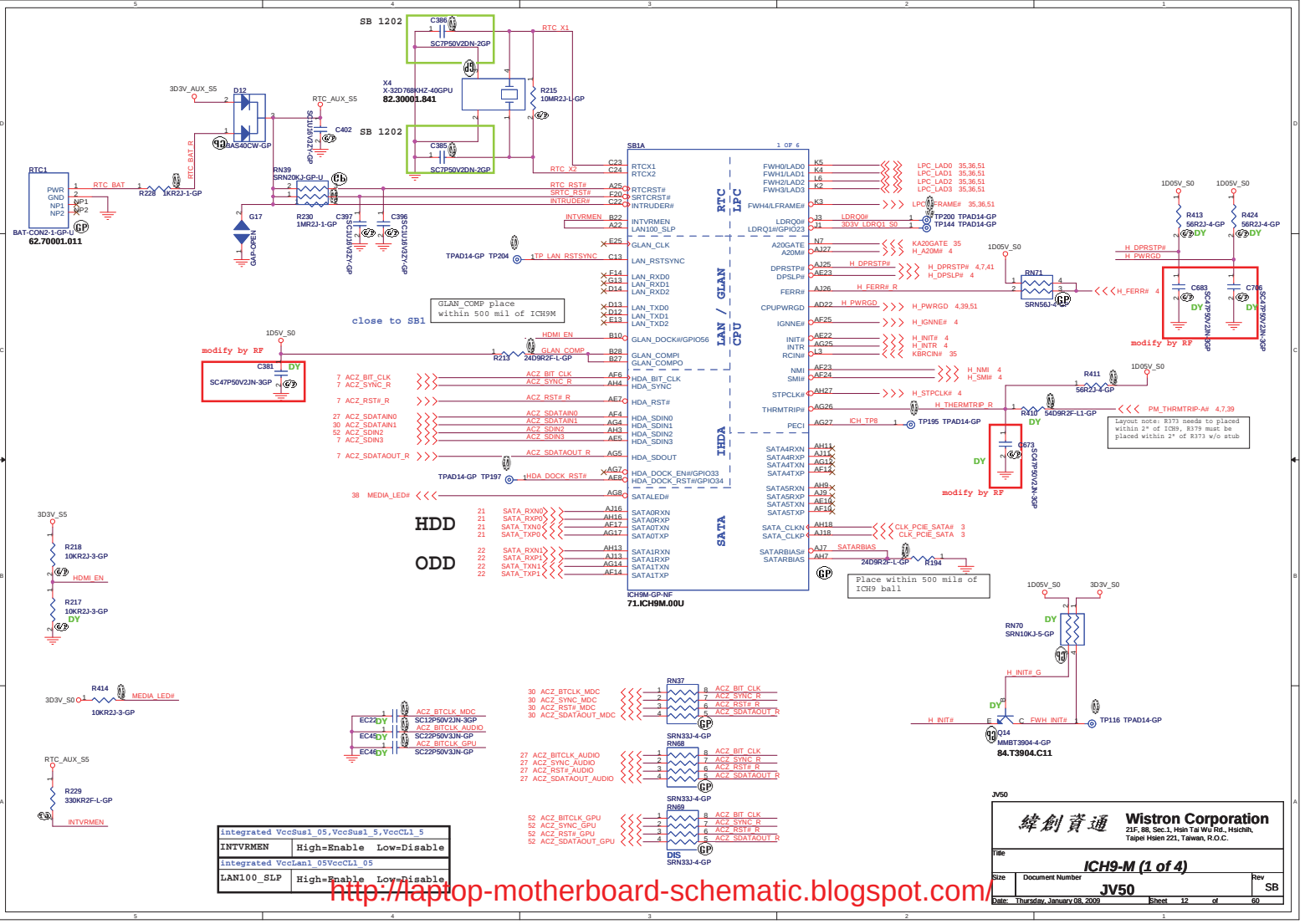
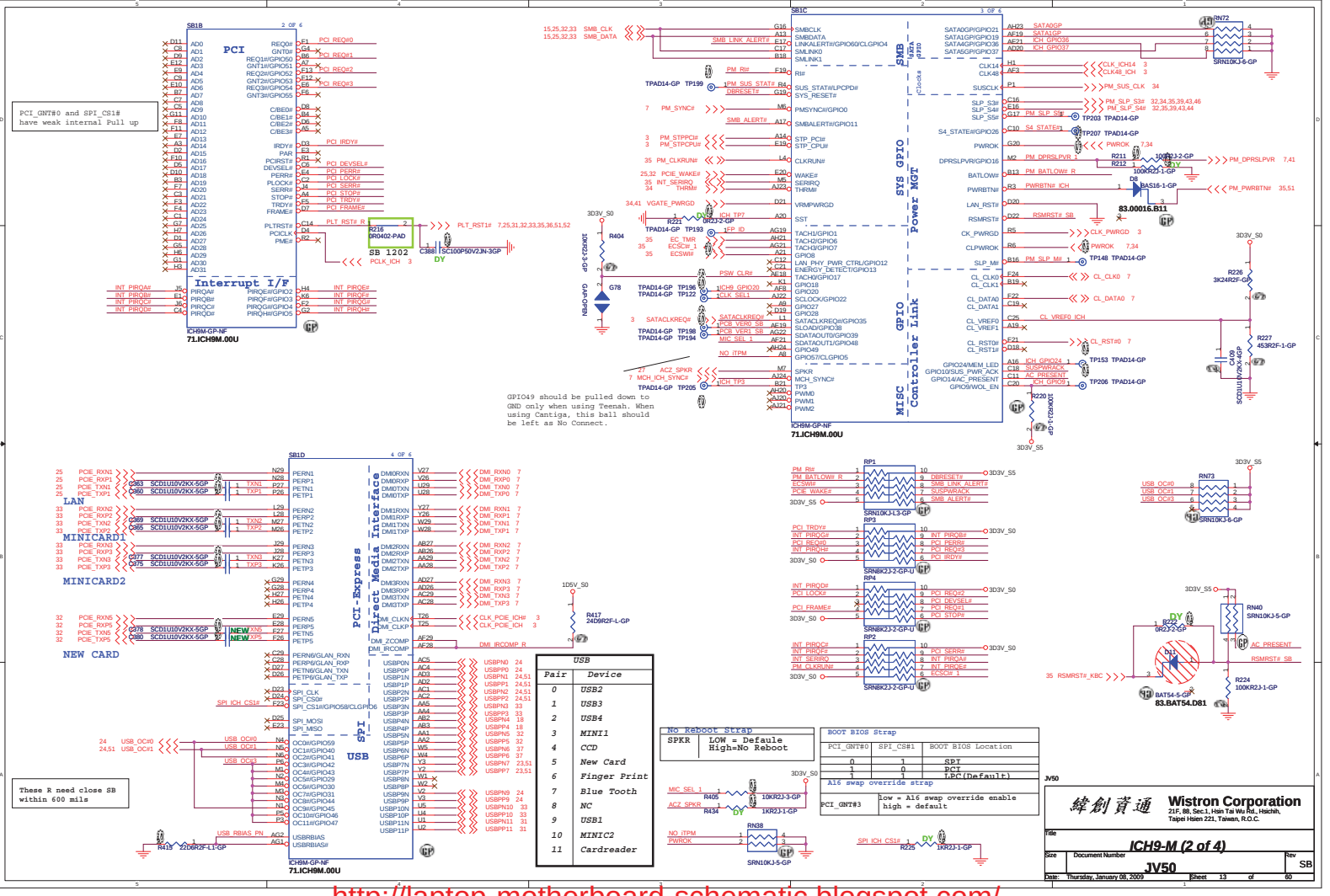
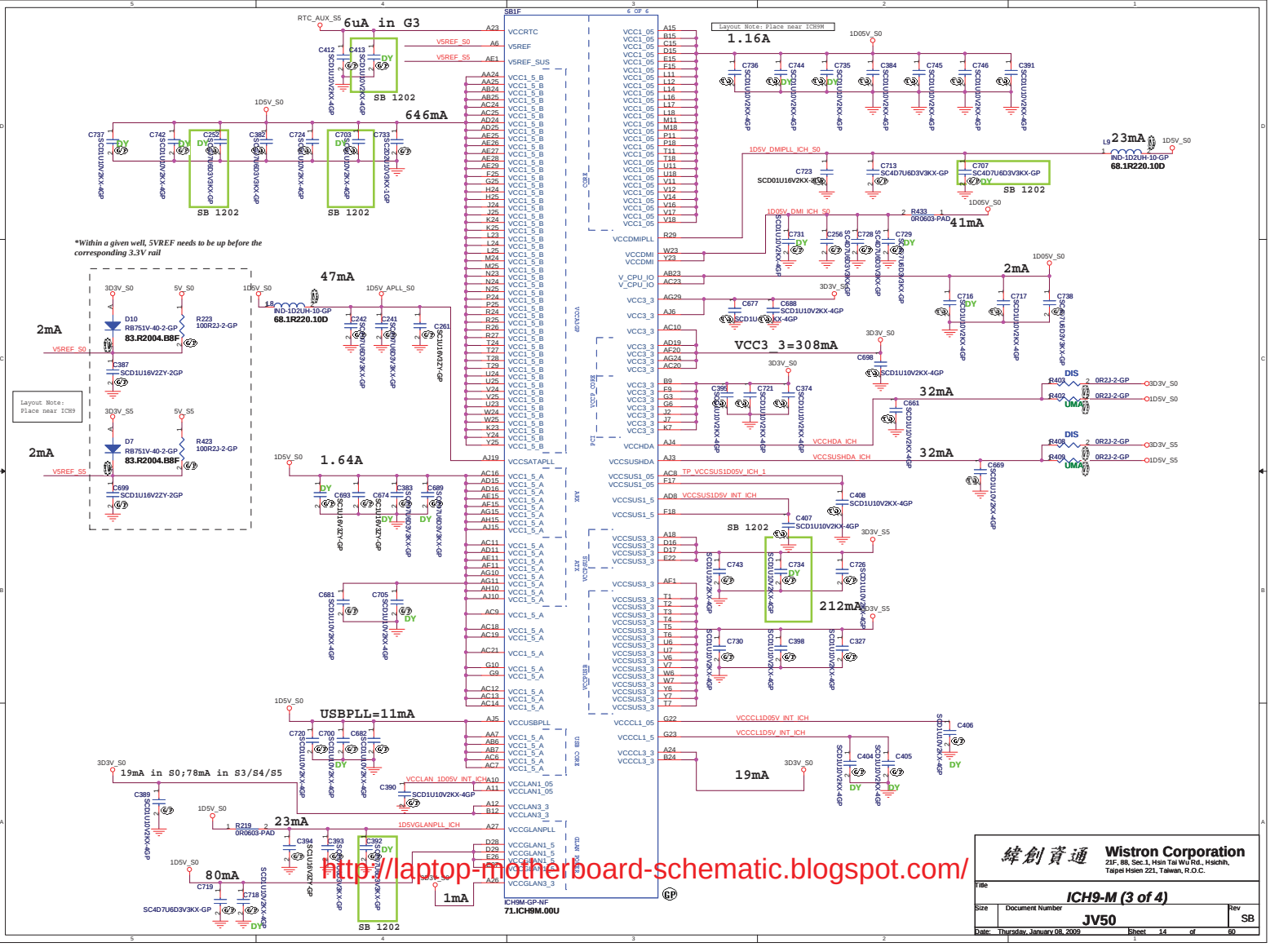
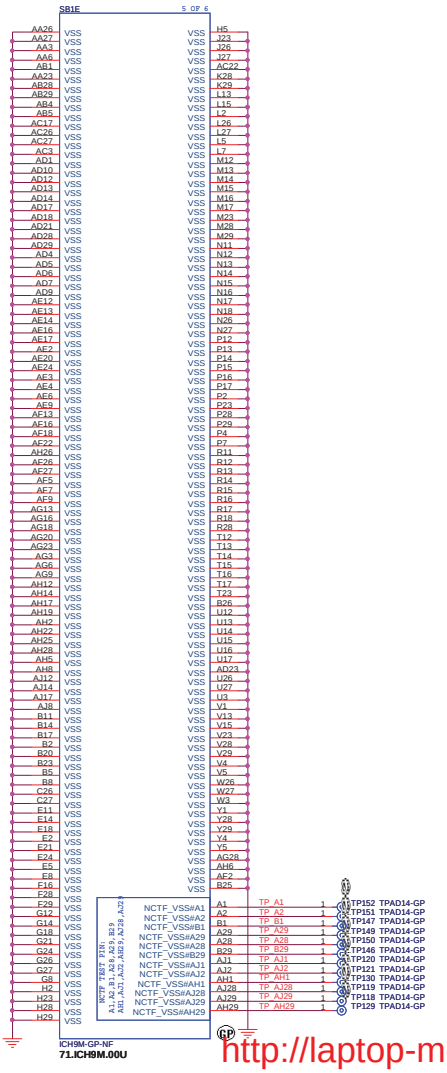
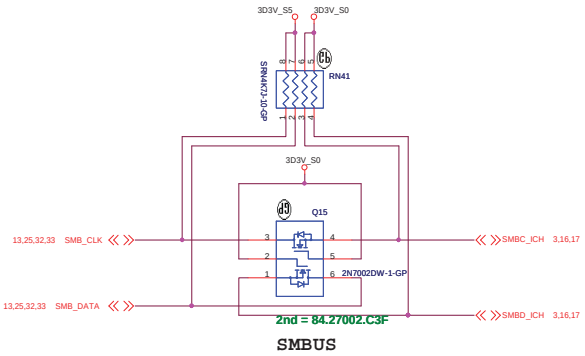




USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1
4	CCD
5	New Card
6	Finger Print
7	Blue Tooth
8	NC
9	USB1
10	MINIC2
11	Cardreader







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Title: ICH9-M (4 of 4)

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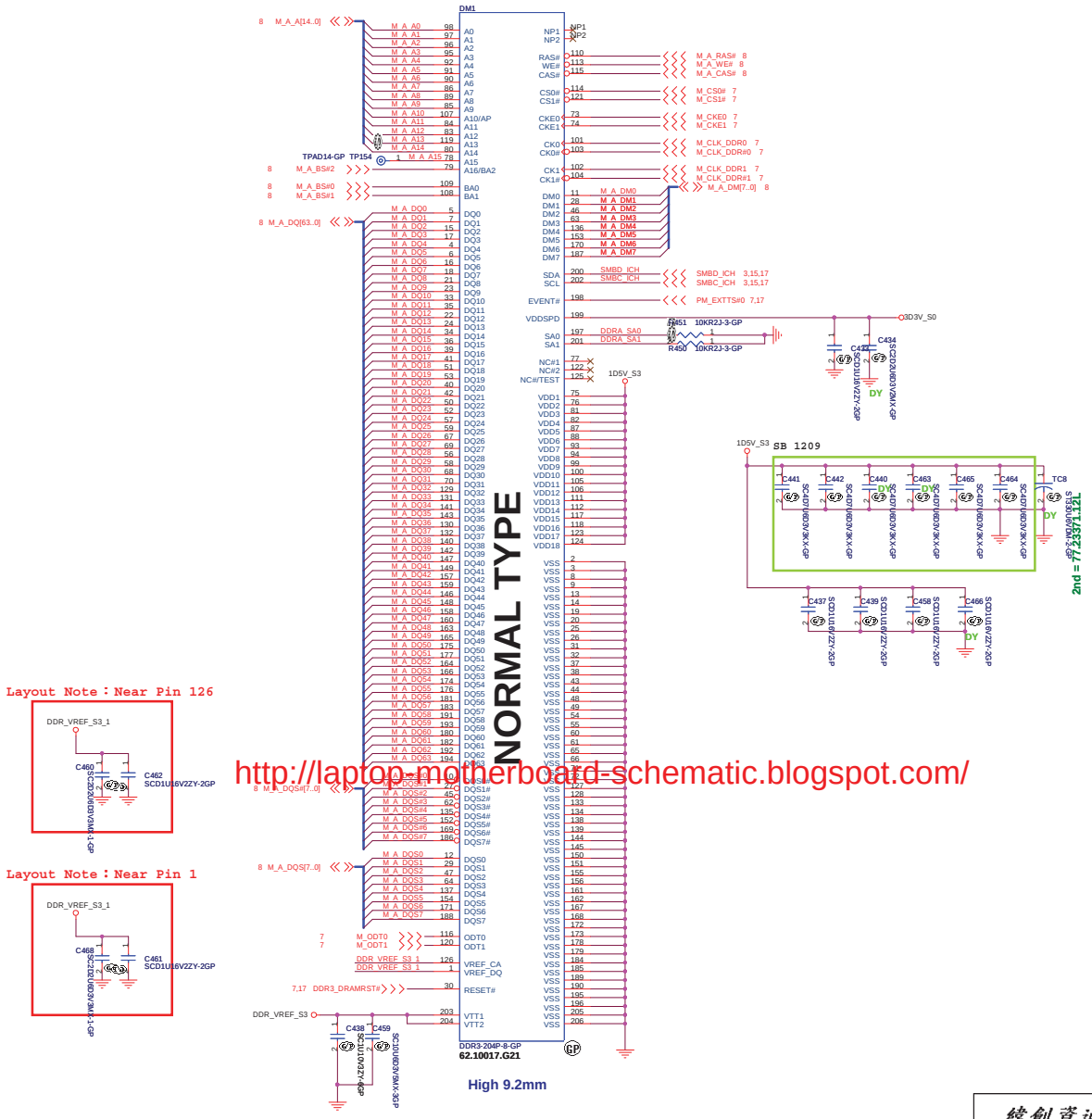
DDR3 SOCKET_1



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Title	DDR3 Socket	
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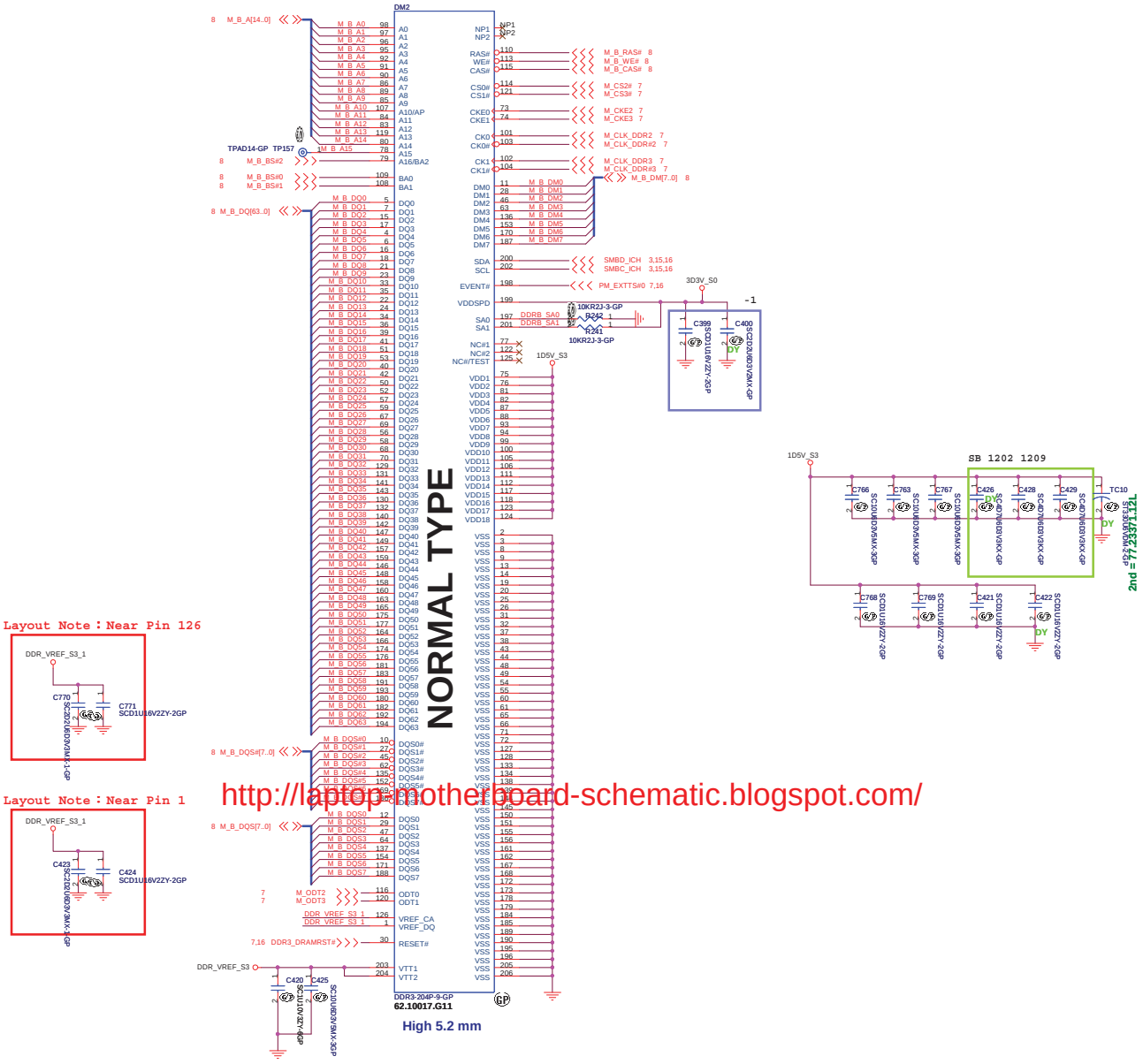
DDR3 SOCKET_2



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Title	DDR3 Socket2		
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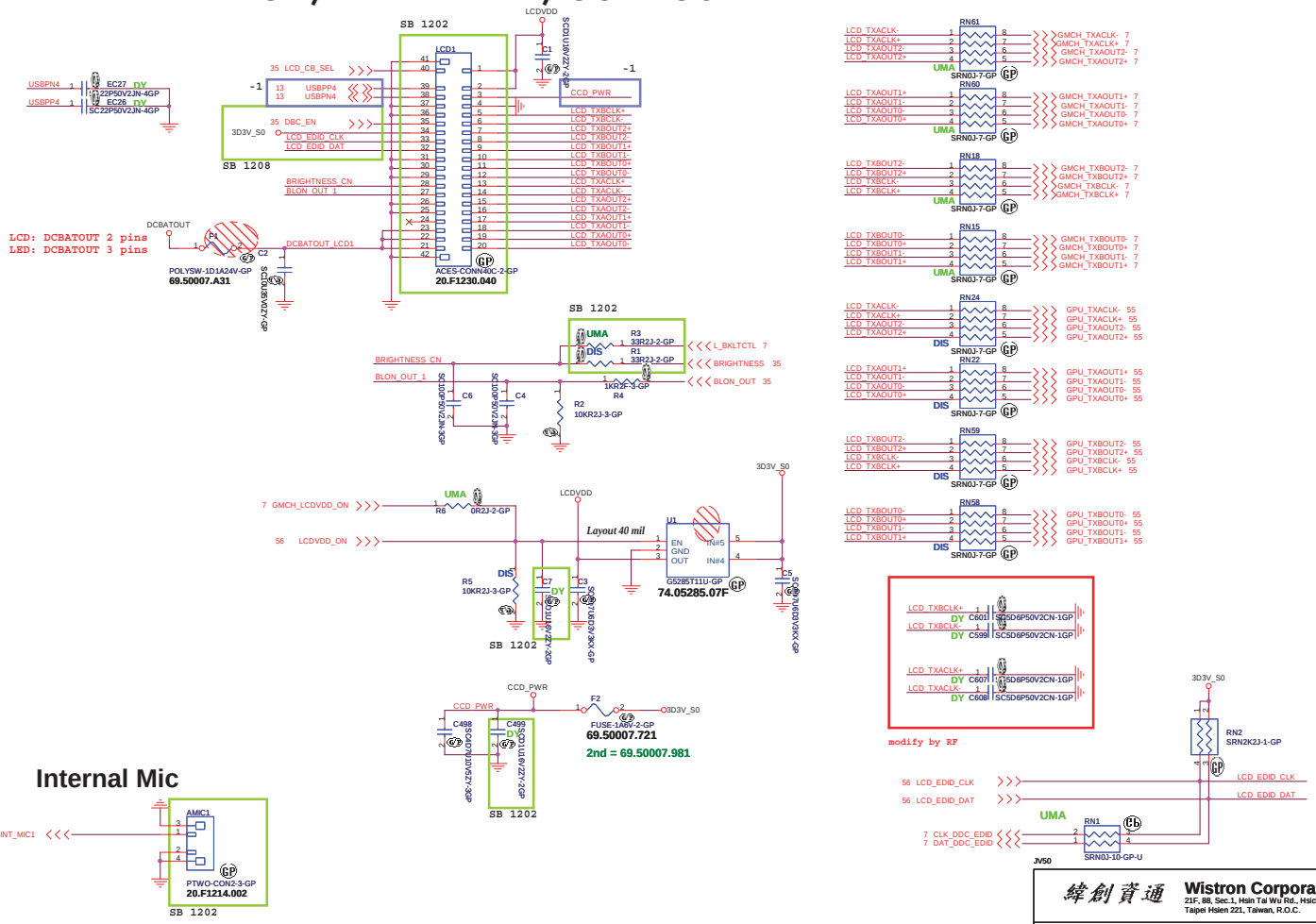
LCD/INVERTER/CCD CONN



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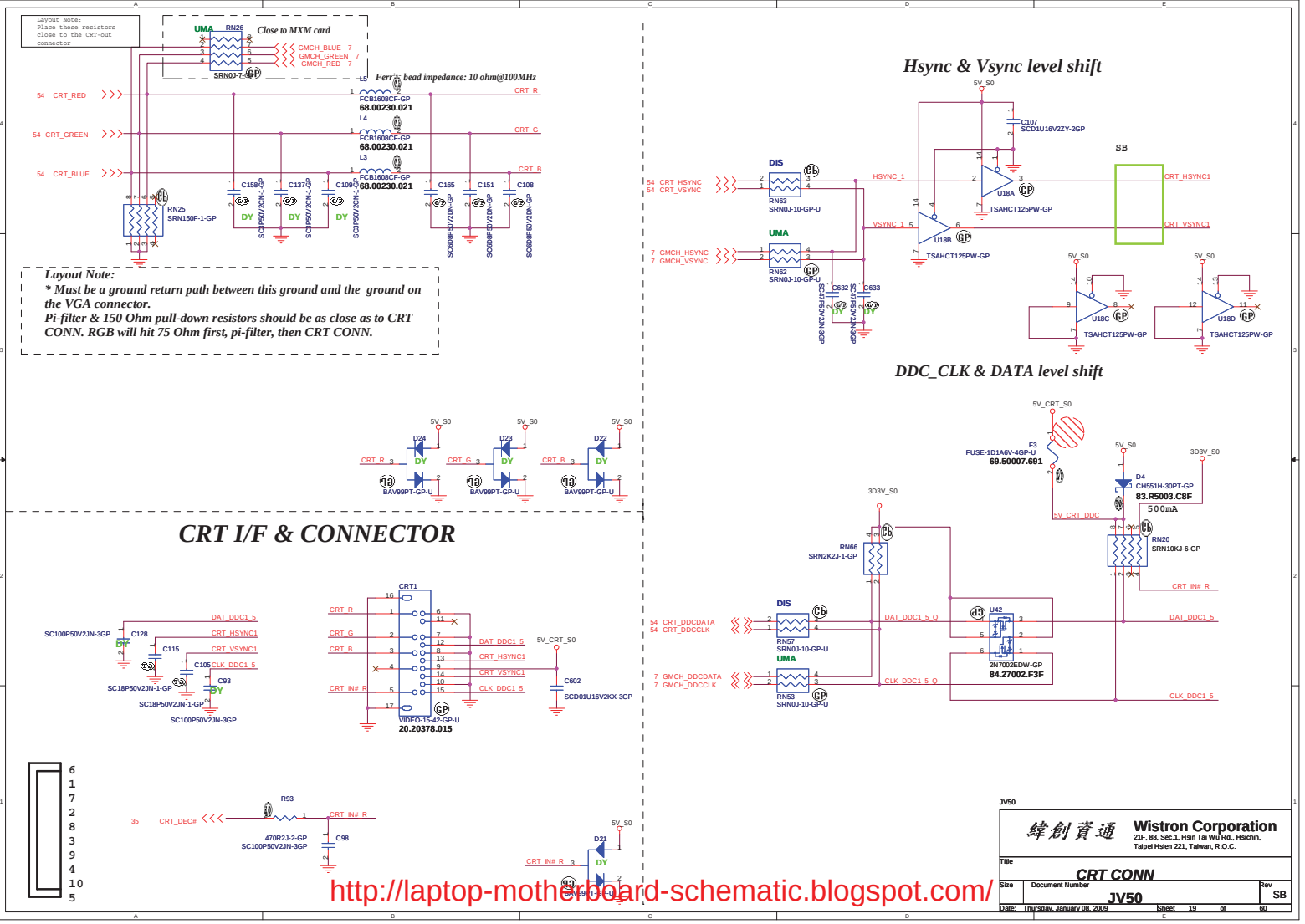

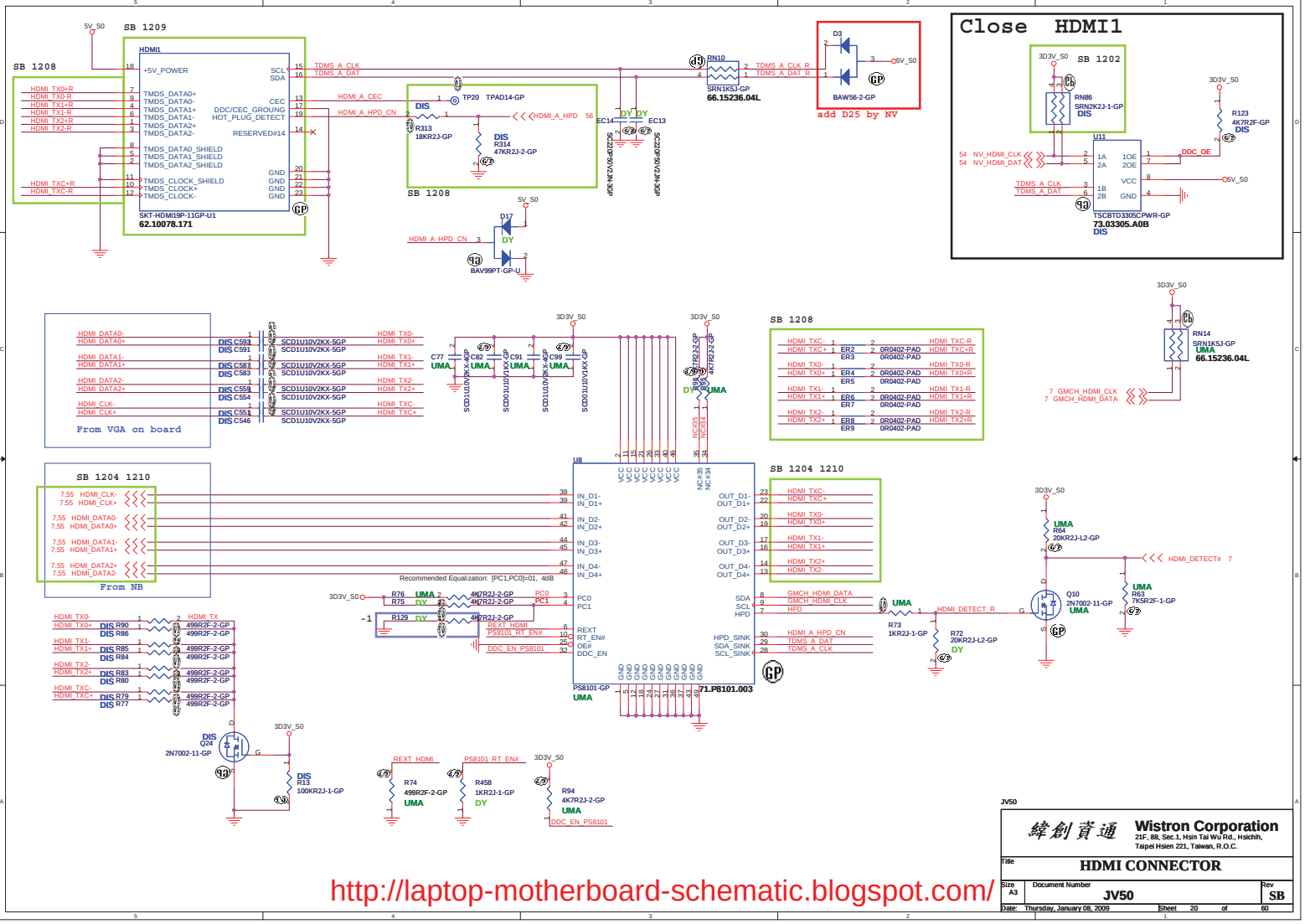

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Title: HDMI CONNECTOR

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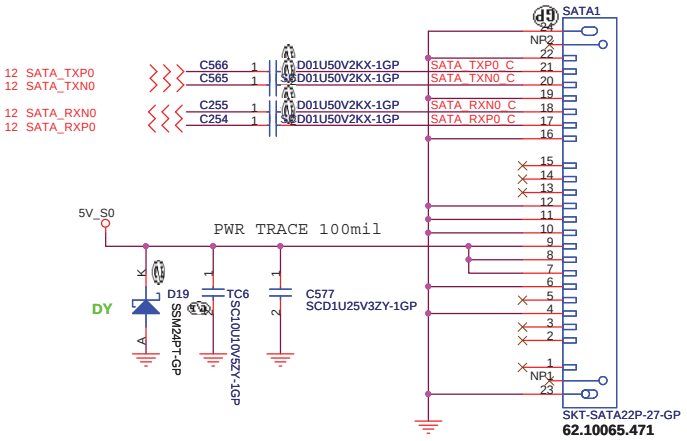
SATA Connector



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Title	***HDD CONN***
Size	Document Number: **JV50** — Rev: SB
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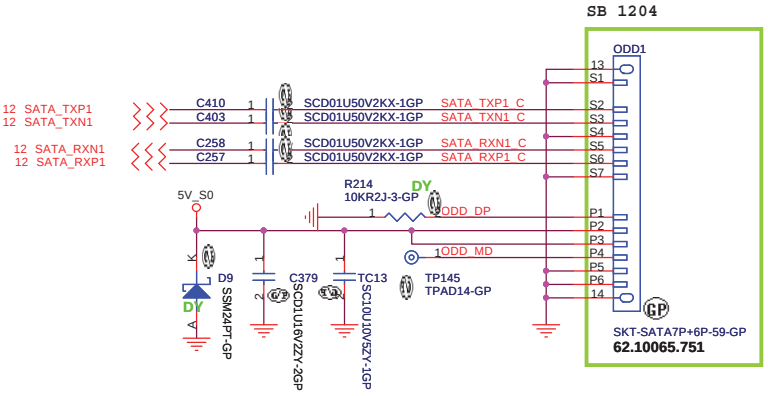
ODD Connector



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Title	***ODD***
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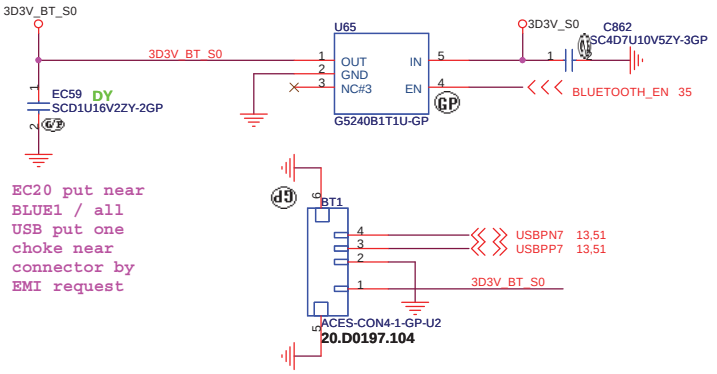
BLUETOOTH MODULE



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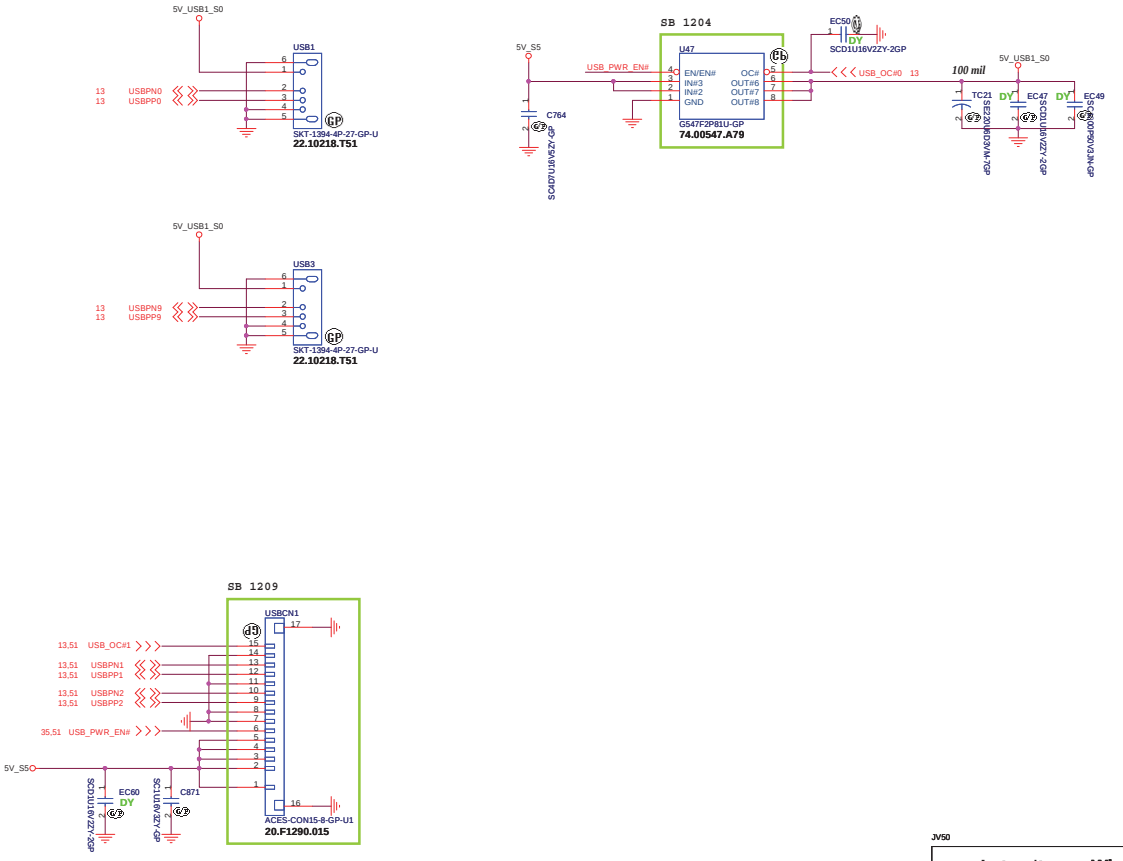

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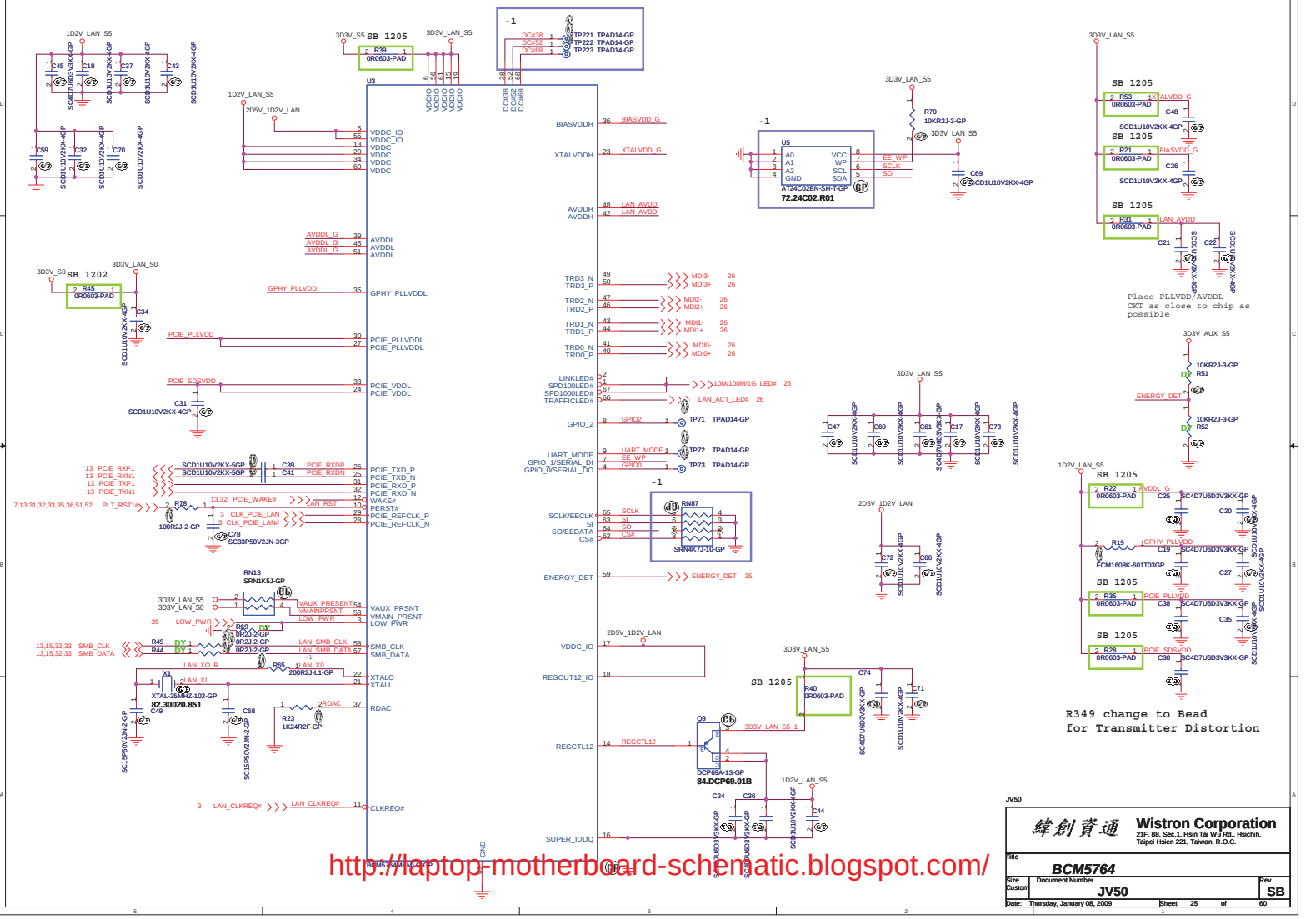
Taipei Hsien 221, Taiwan, R.O.C.

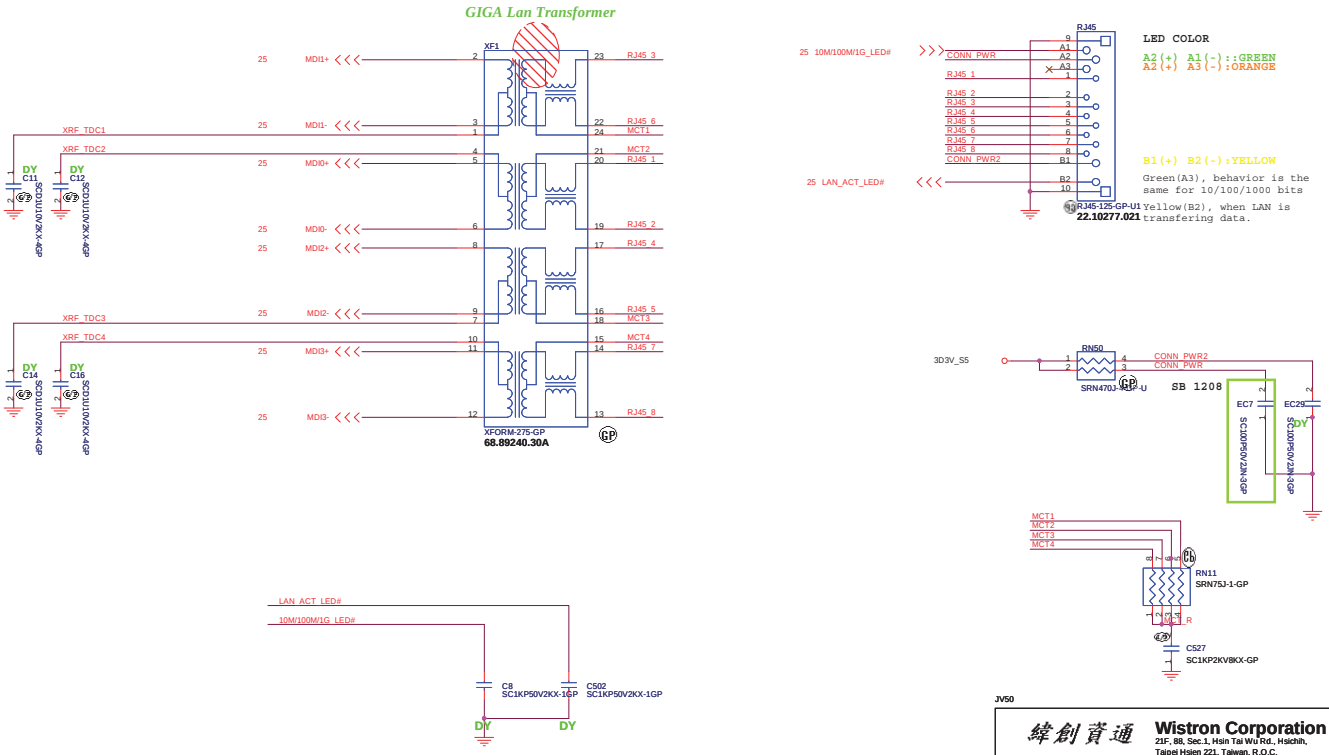
Title	USB CONN	
Size	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 24 of 60	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector



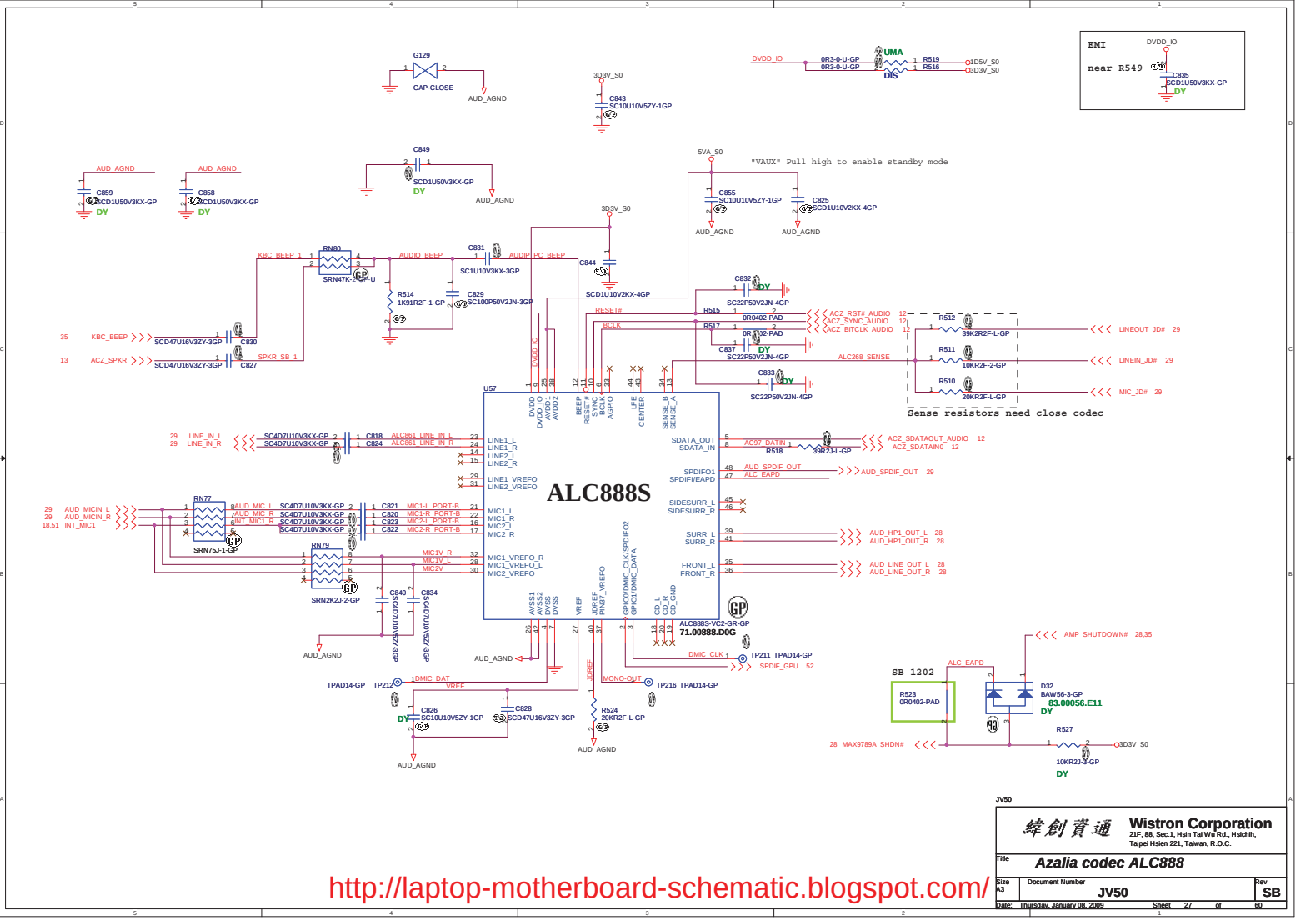
JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

Size	Document Number	Rev
A3	JV50	SB

Date: Thursday, January 08, 2009 Sheet 26 of 60



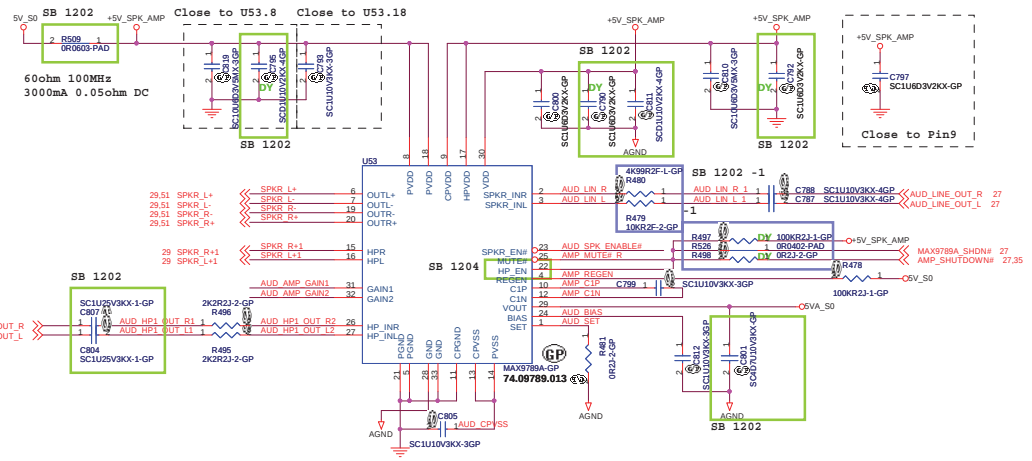
JV50

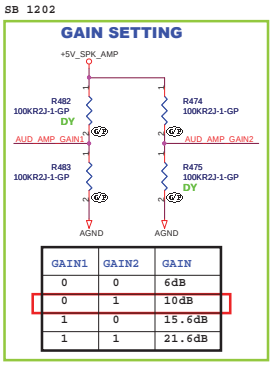
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC888***

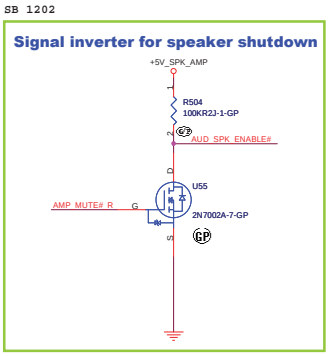
Size	Document Number	Rev
A3	JV50	SB

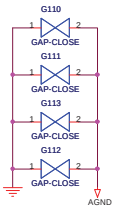
Date: Thursday, January 08, 2009 Sheet 27 of 60





GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





JV50

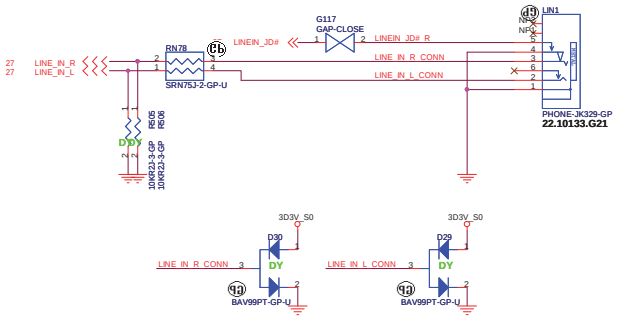
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP*

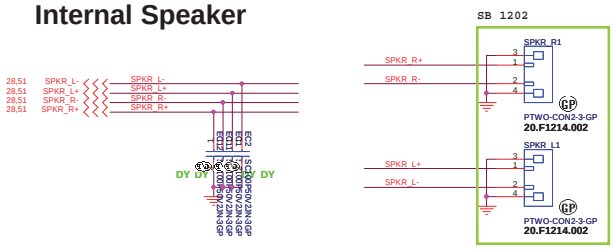
Size	Document Number	Rev
	JV50	SB

Date: Thursday, January 08, 2009 Sheet 28 of 60

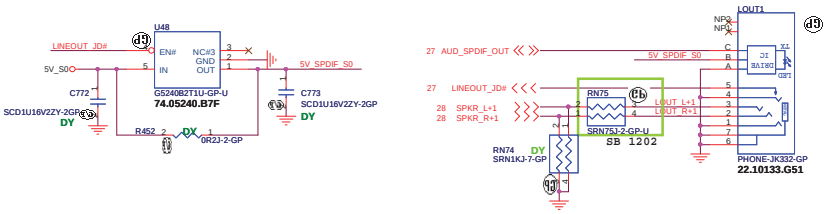
LINE IN



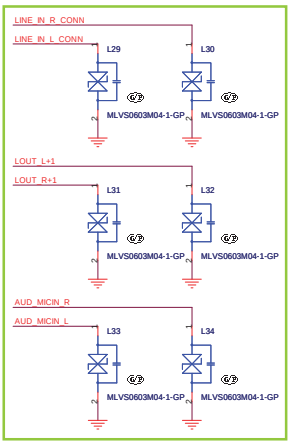
Internal Speaker



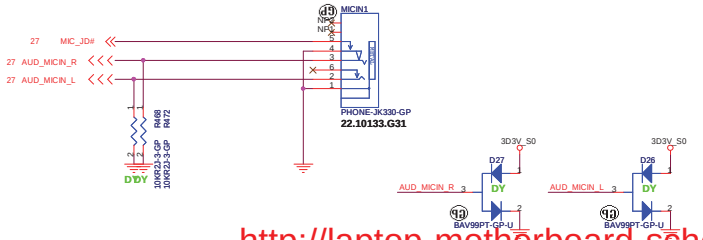
LINE OUT



SB 1202



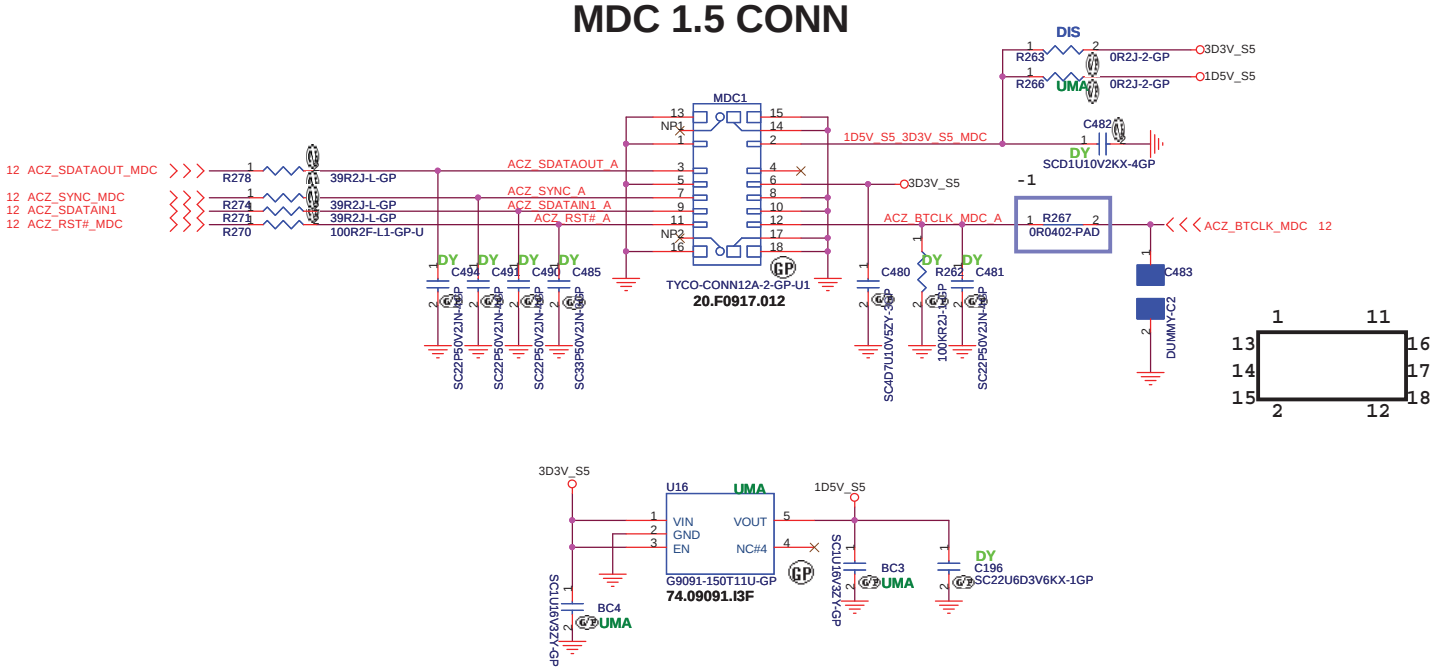
MIC IN



JV50

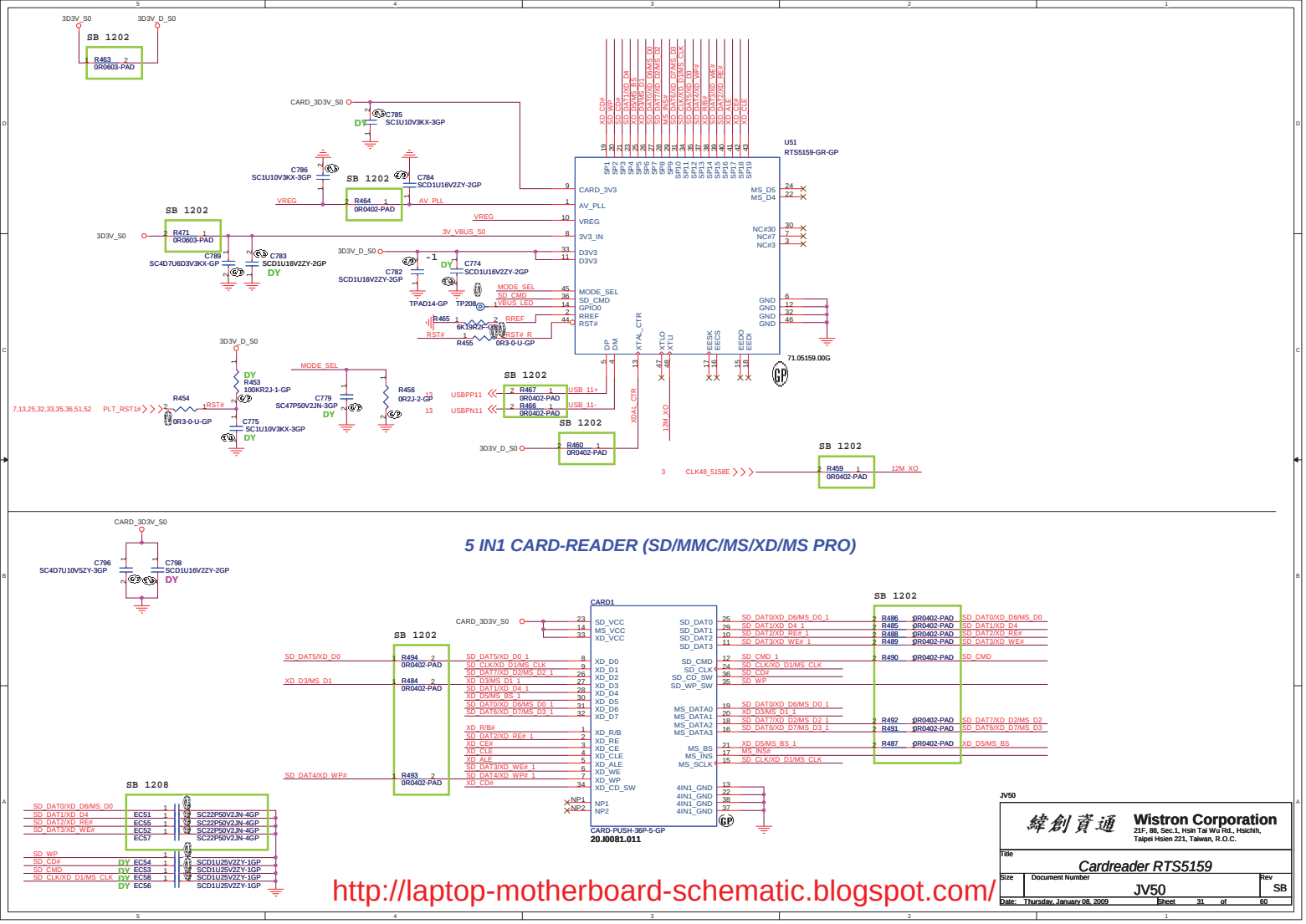
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO jack	
Size	Document Number: JV50	Rev: SB
Date: Thursday, January 08, 2009	Sheet 29 of 60	

MDC 1.5 CONN



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MDC***
Size / Document Number	JV50
Rev	SB
Date: Thursday, January 08, 2009	Sheet 30 of 60



5 IN1 CARD-READER (SD/MMC/MS/XD/MS PRO)

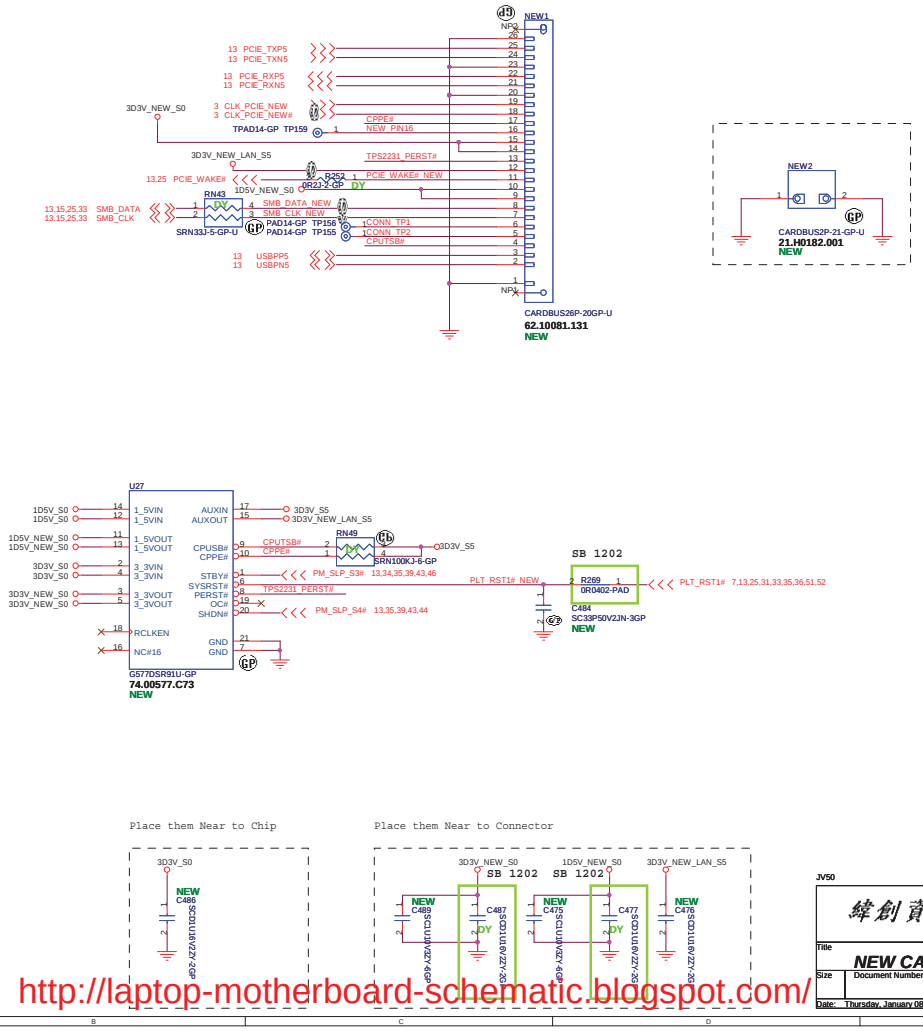
JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cardreader RTS5159

Size	Document Number	Rev
	JV50	SB

Date: Thursday, January 08, 2009 Sheet 31 of 60



Place them Near to Chip

Place them Near to Connector

JV50

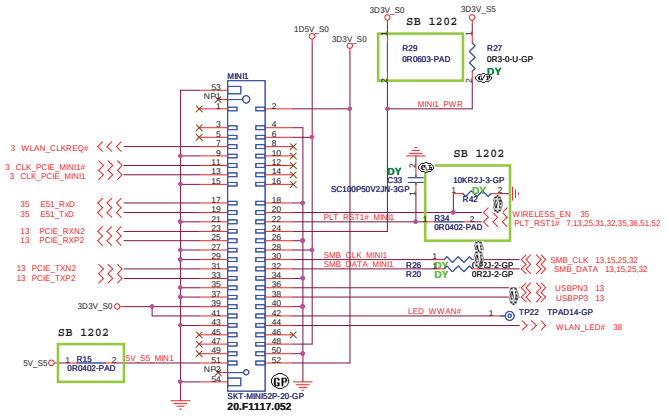
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

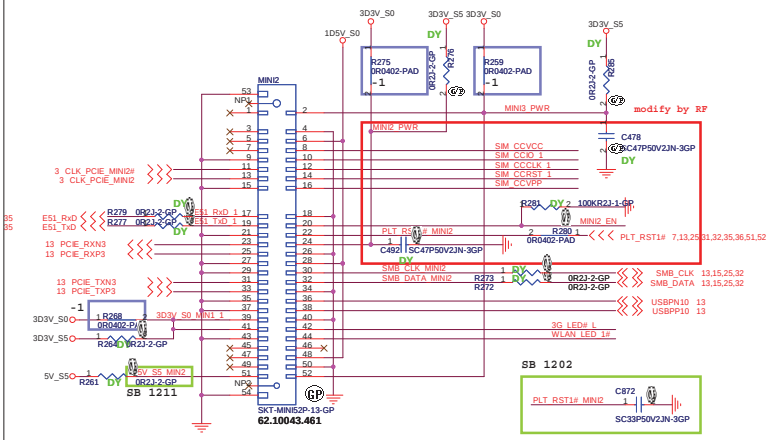
Size	Document Number	Rev
	JV50	SB

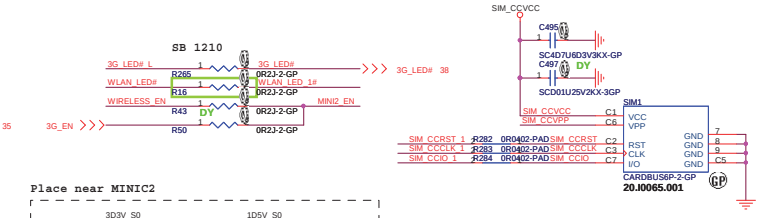
Date: Thursday, January 08, 2009 Sheet 32 of 60

Mini Card Connector(WLAN)
Support debug-card

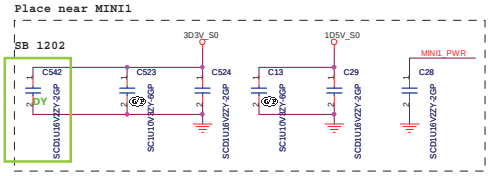


Mini Card Connector(Robson2 and 3G)

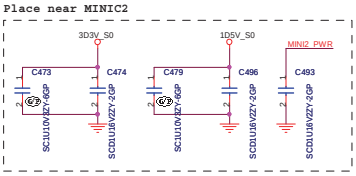




Place near MINI1

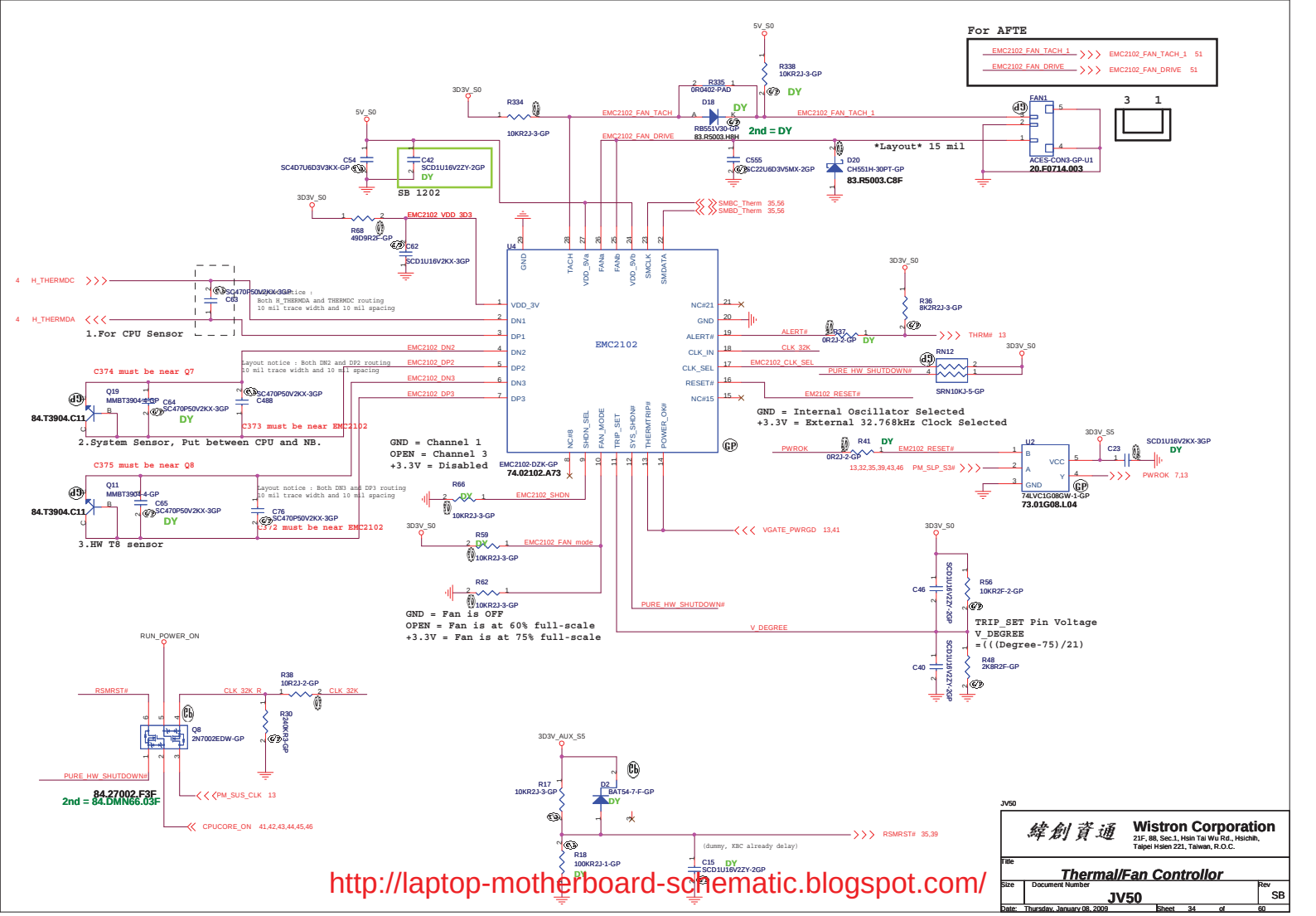


Place near MINIC2



JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 33 of 60	



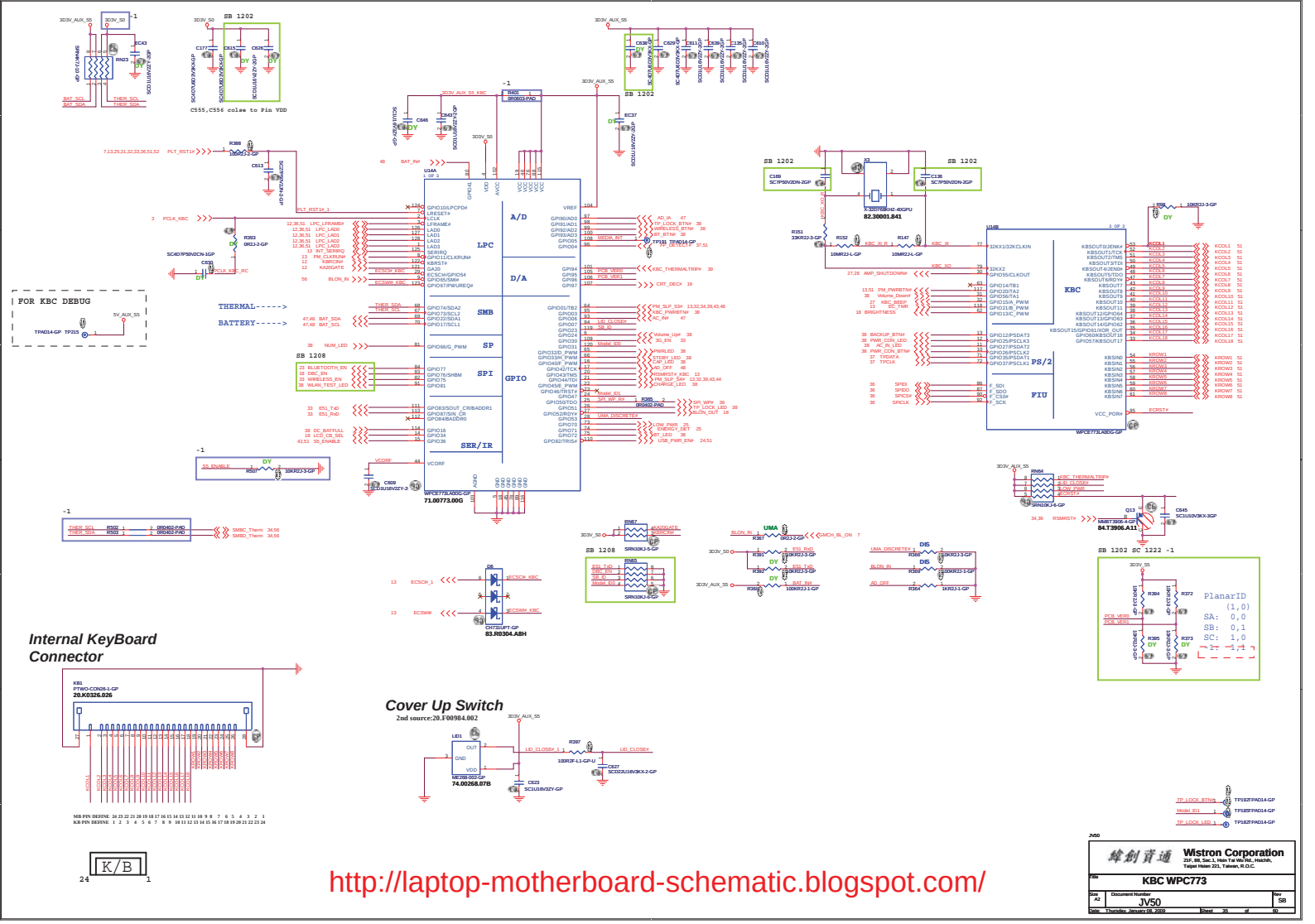
JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

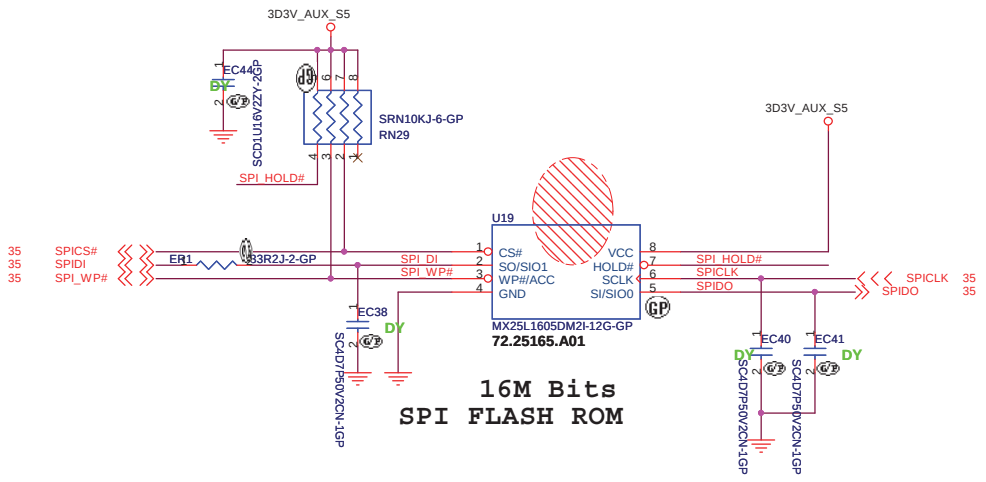
Size	Document Number	Rev
	JV50	SB

Date: Thursday, January 08, 2009 Sheet 34 of 60

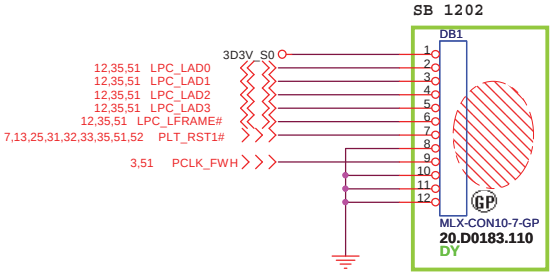


http://laptop-motherboard-schematic.blogspot.com/

鋒創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC WPC773
Size A2	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 35 of 40



GOLDEN FINGER FOR DEBUG BOARD



JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size	Document Number	Rev
	JV50	SB
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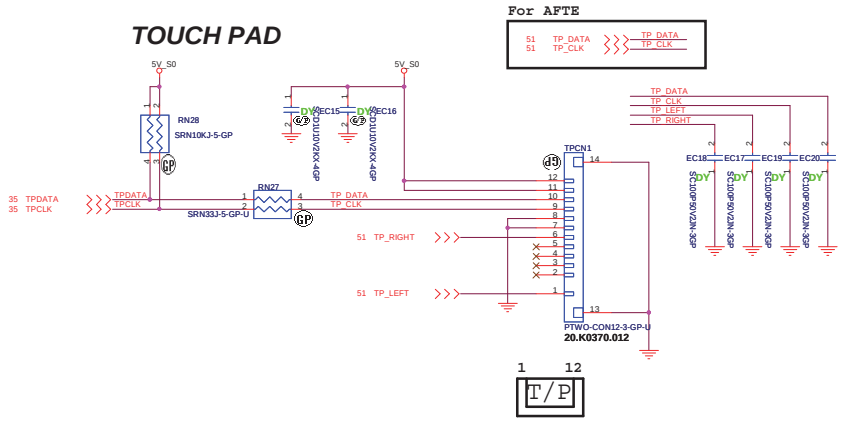
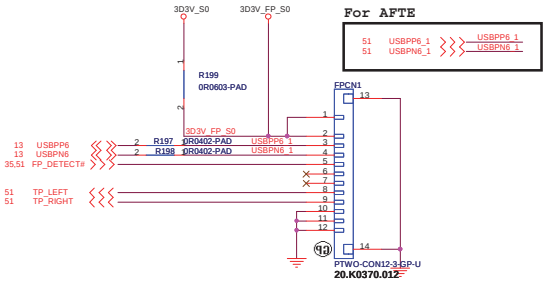
TOUCH PAD

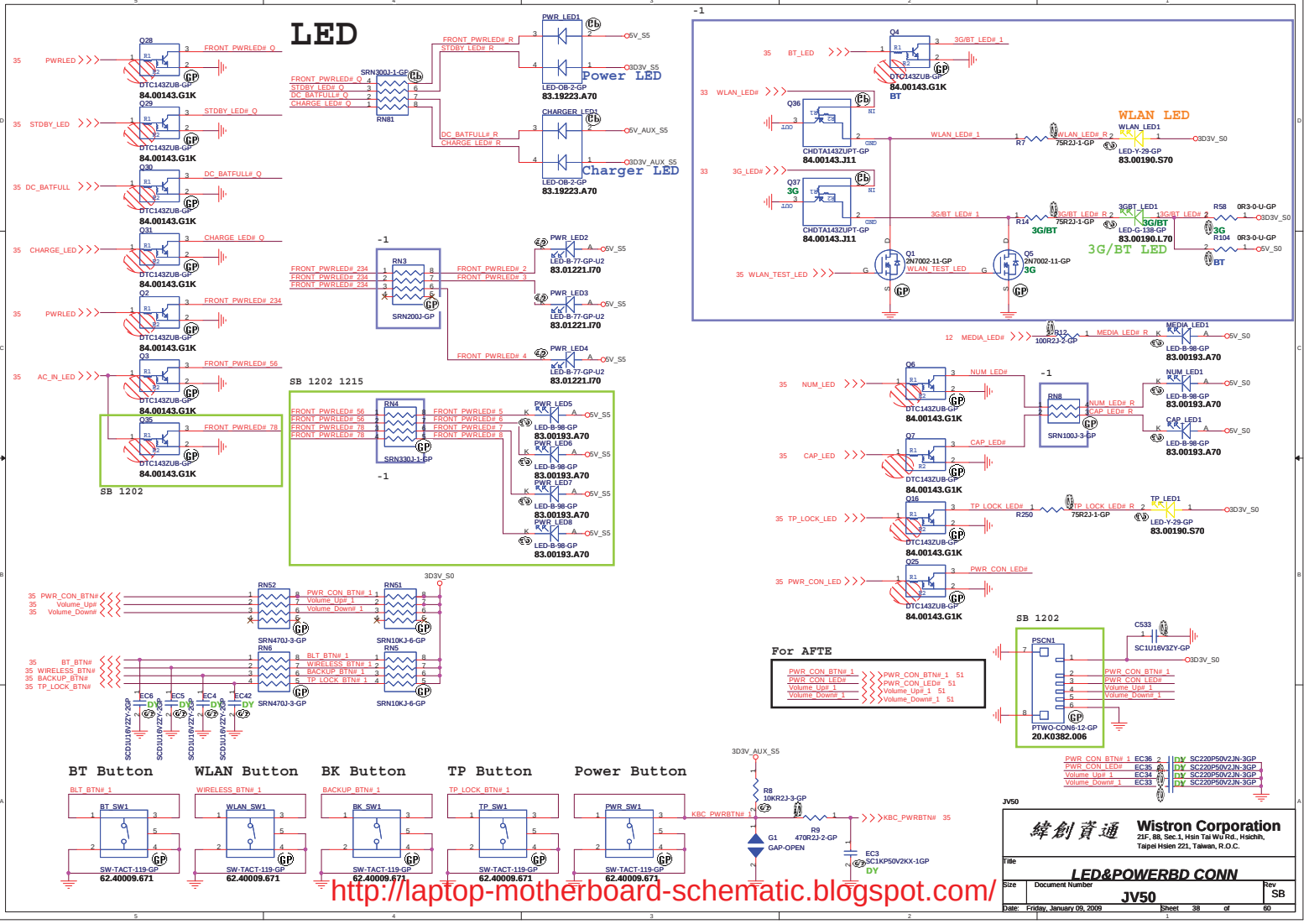


Finger printer



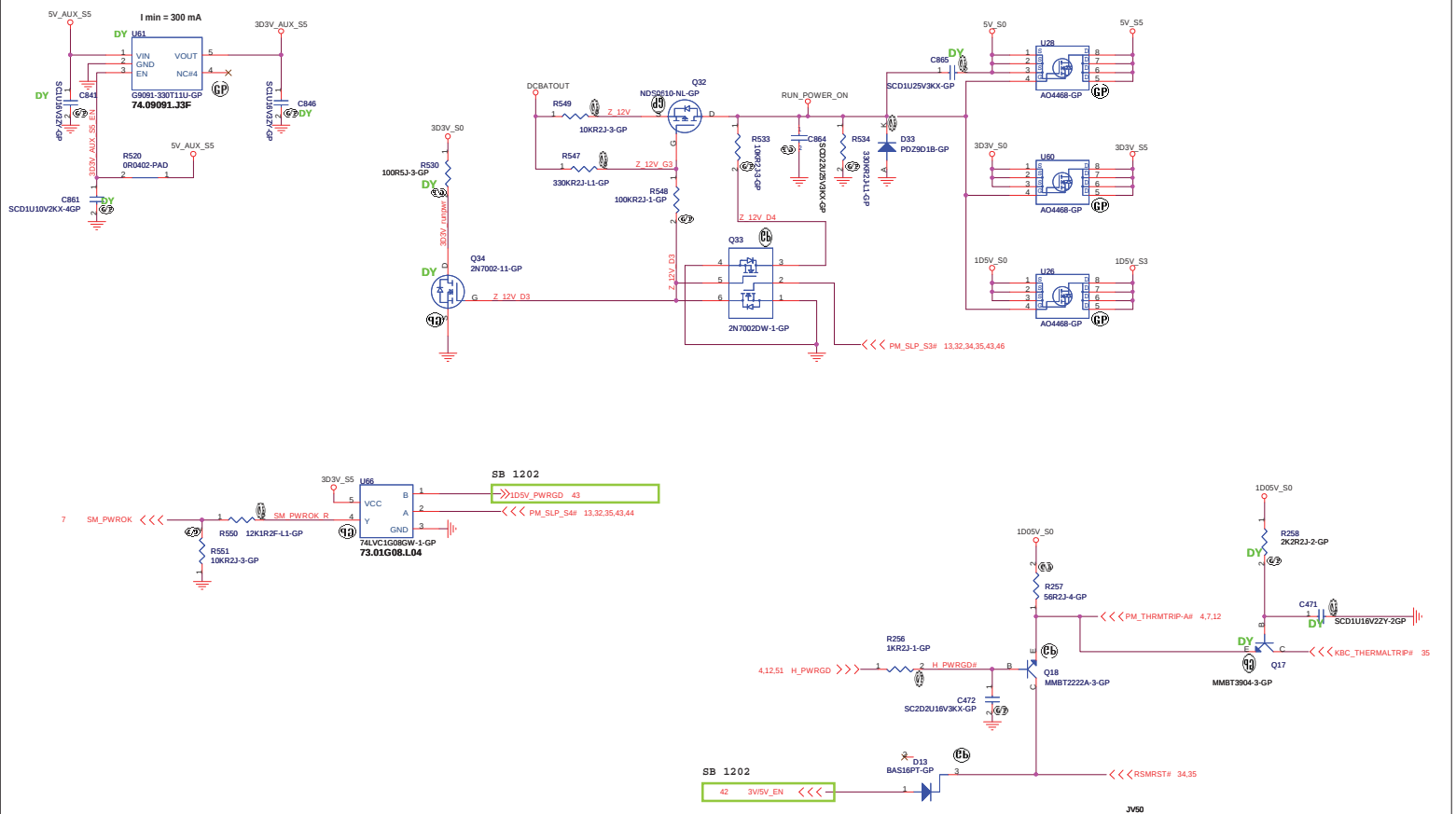
JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Touch PAD and FP
Size / Document Number	JV50
Rev	SB
Date: Thursday, January 08, 2009	Sheet 37 of 60



Aux Power 3D3V_AUX_S5

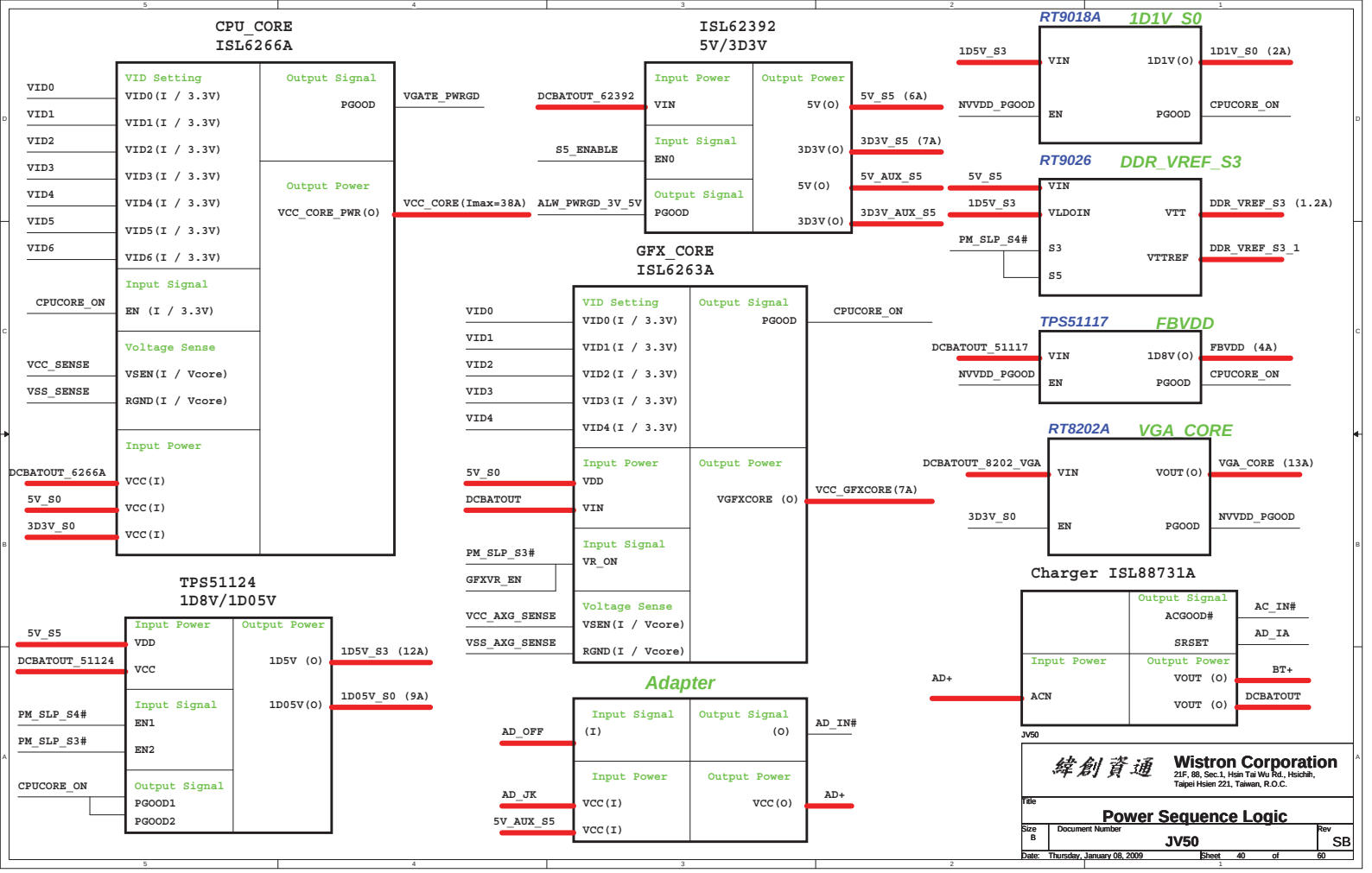
Run Power

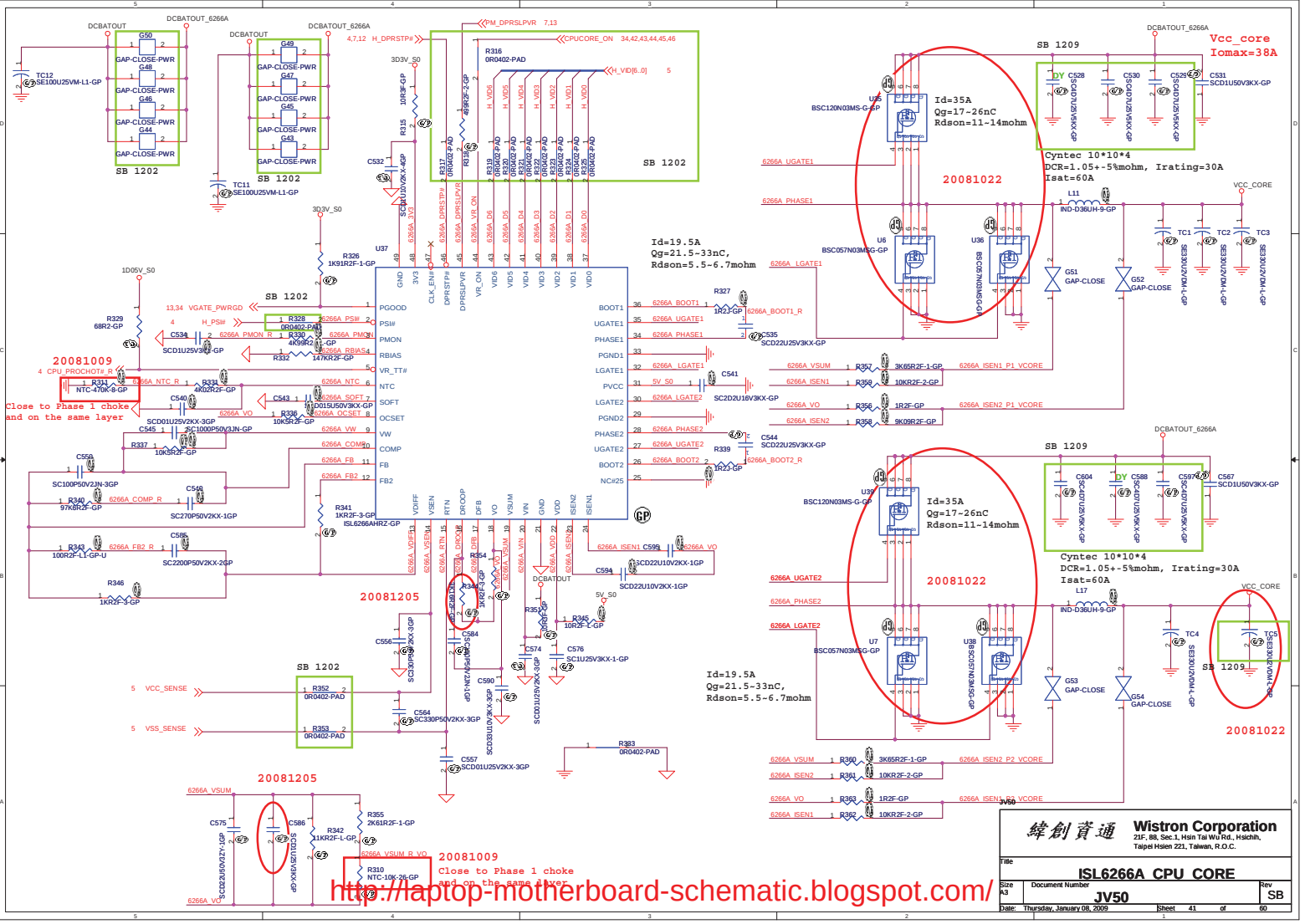


http://laptop-motherboard-schematic.blogspot.com/

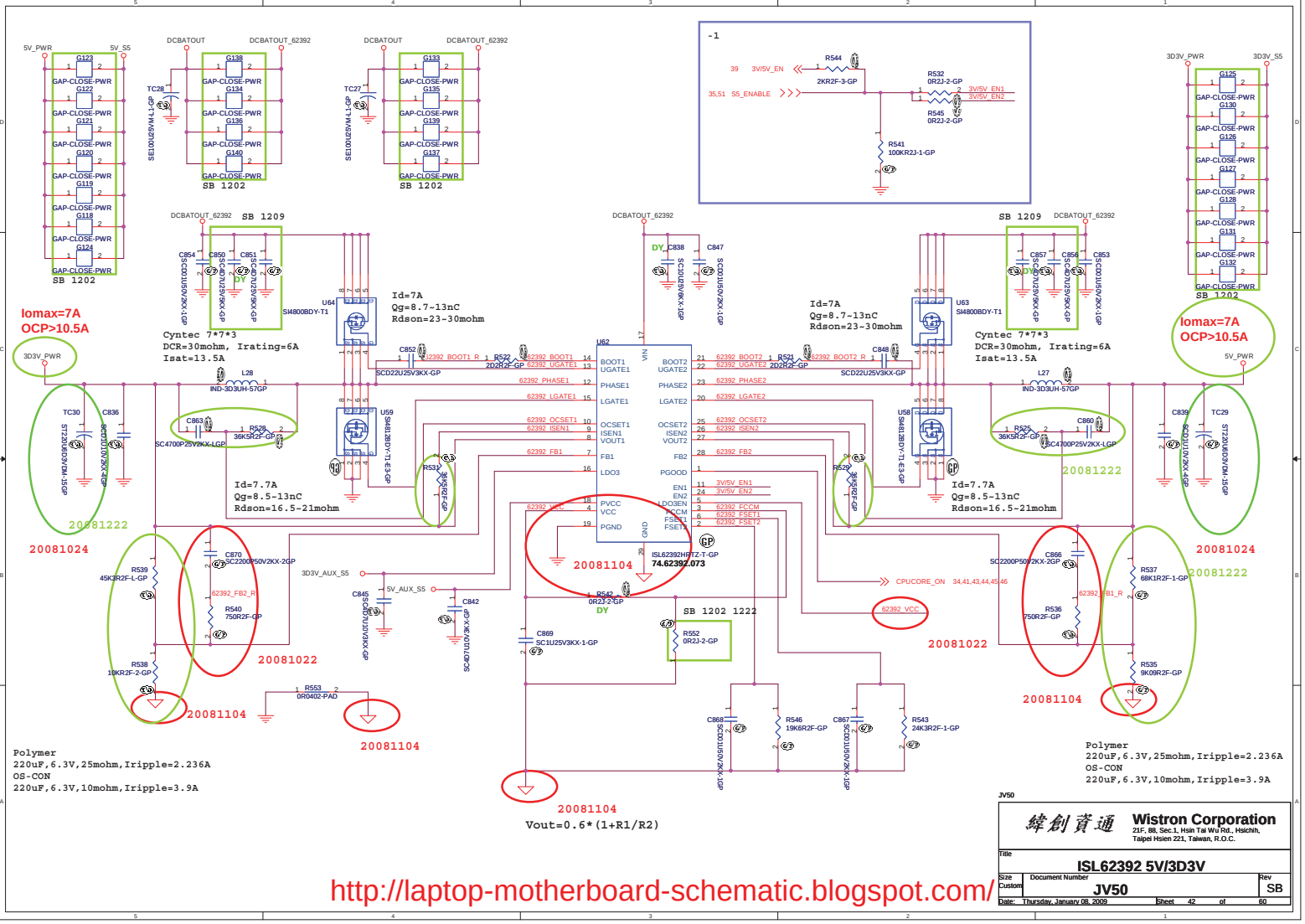
JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RUN POWER and 3D3V_AUX_S5
Size / Document Number	JV50
Rev	SB
Date: Thursday, January 08, 2009	Sheet 39 of 60





緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6266A CPU CORE
Size A3	Document Number JV50
Rev	SB
Date: Thursday, January 08, 2009	Sheet 41 of 60



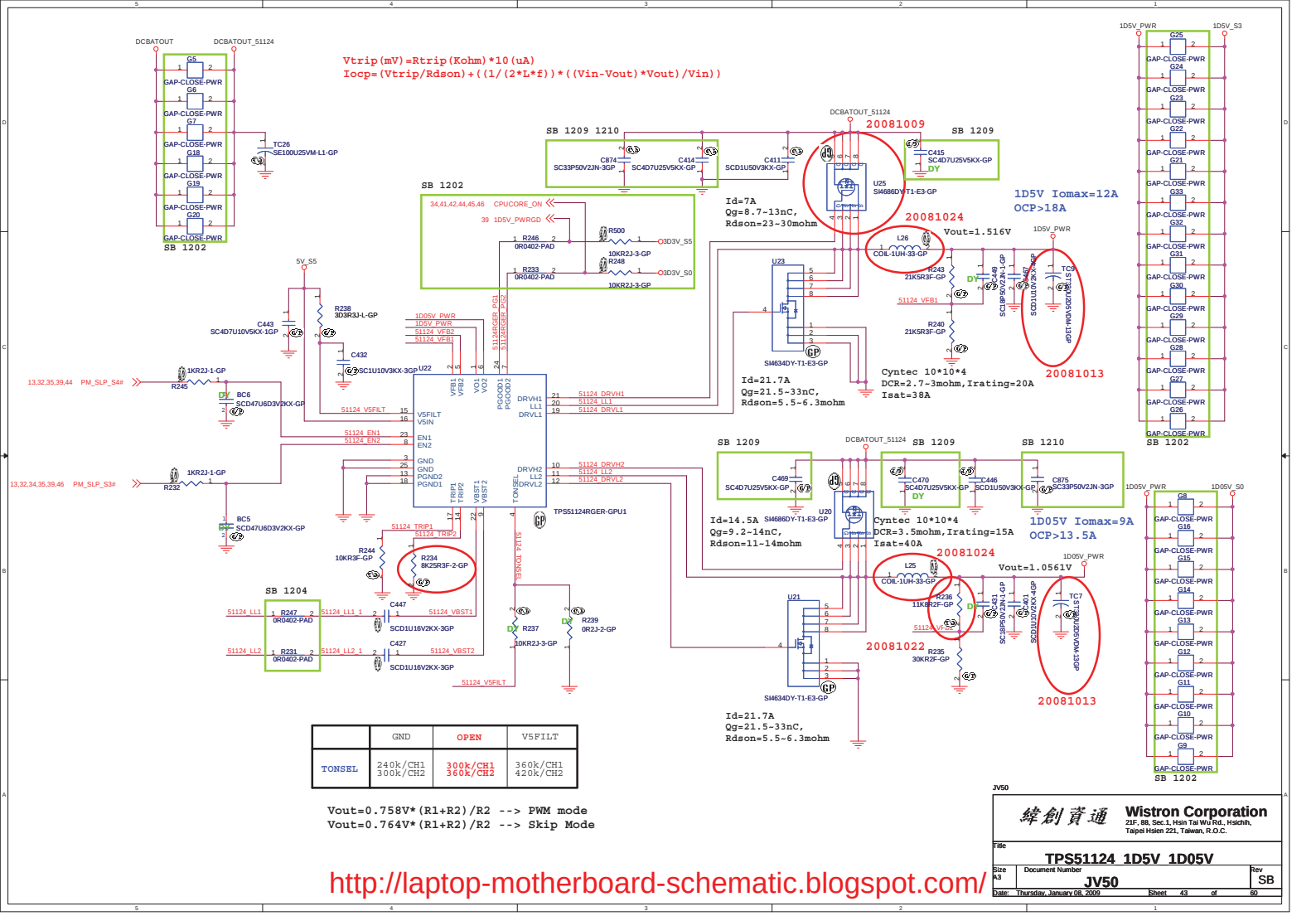
JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

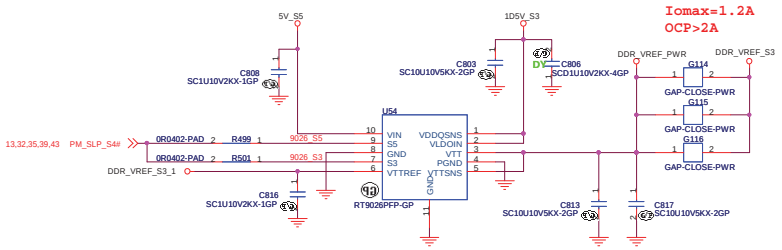
Title: ISL62392 5V/3D3V

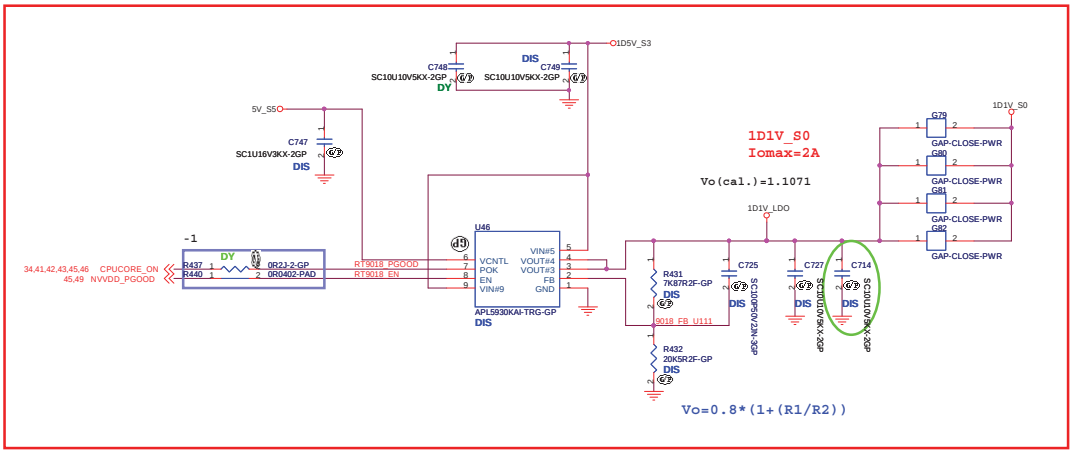
Size	Document Number	Rev
Custom	JV50	SB

Date: Thursday, January 08, 2009 Sheet 42 of 60



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

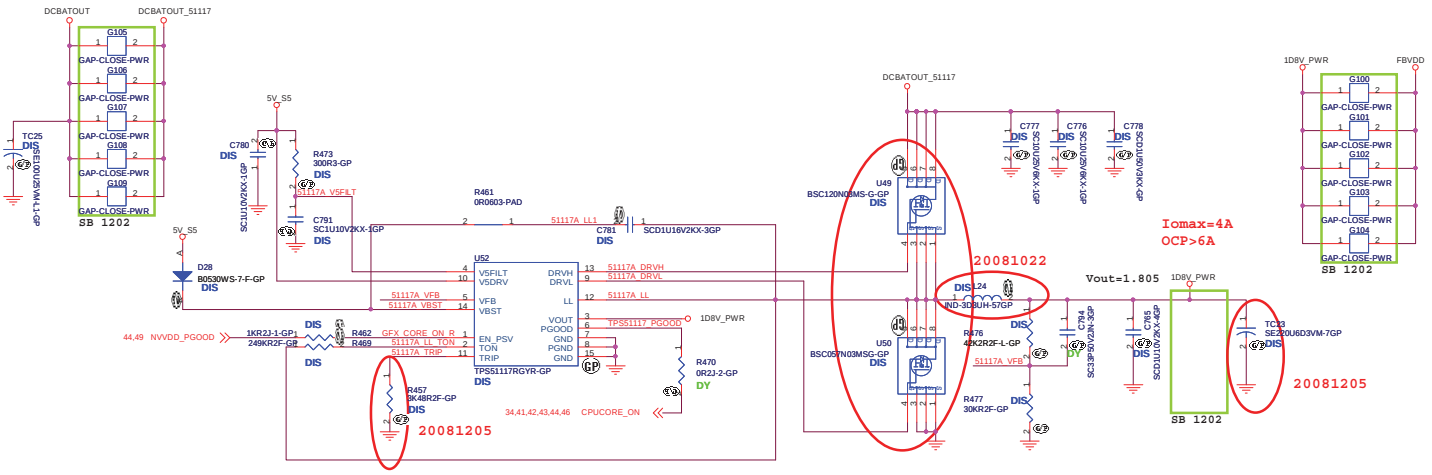




20090106

JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	0D75V/1D1V	
Size A3	Document Number JV50	Rev SB
Date: Thursday, January 08, 2009	Sheet 44 of 60	



Vout=0.75V*(R1+R2)/R2

JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117 1D8V

Size	Document Number	Rev
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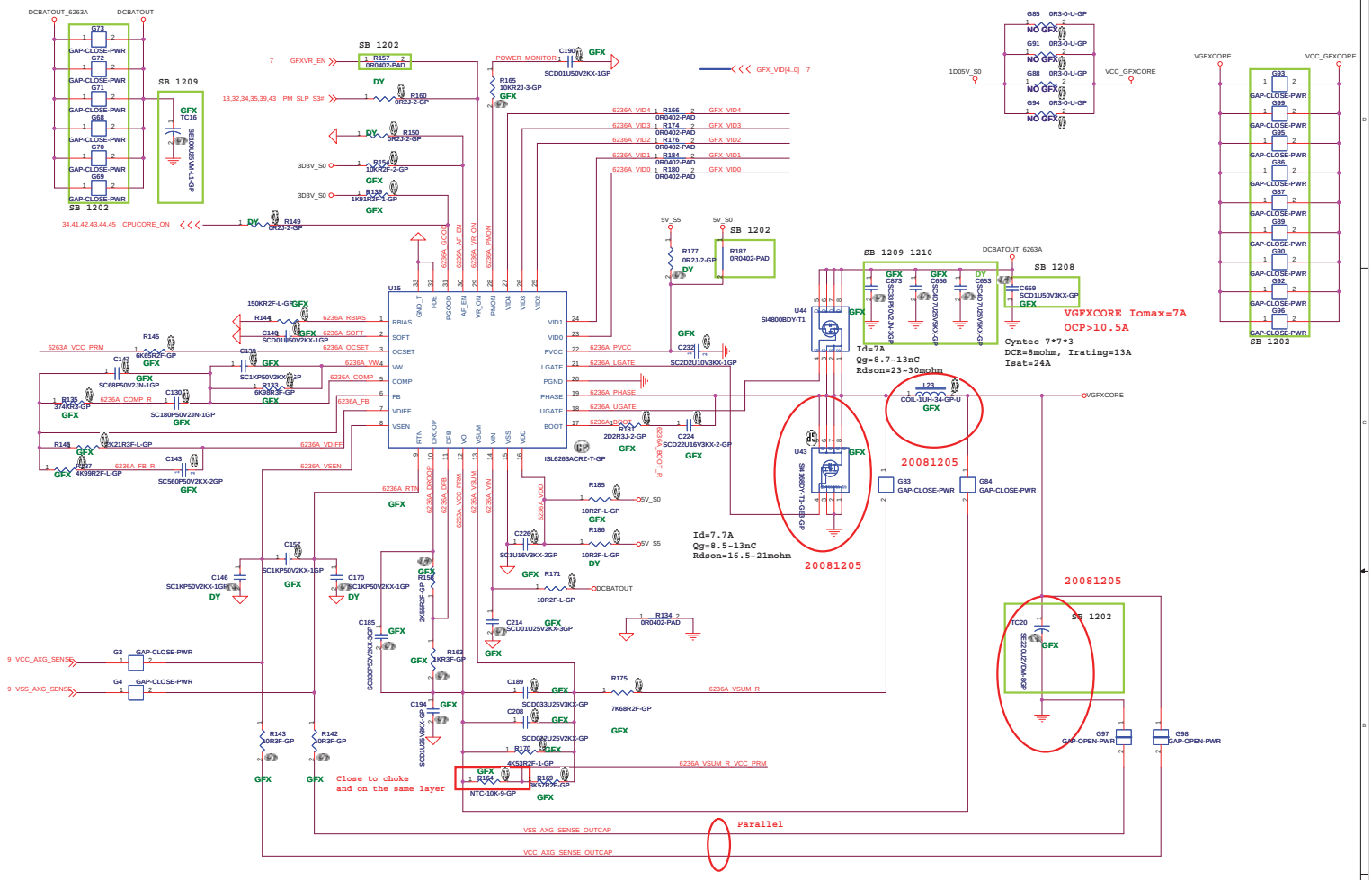
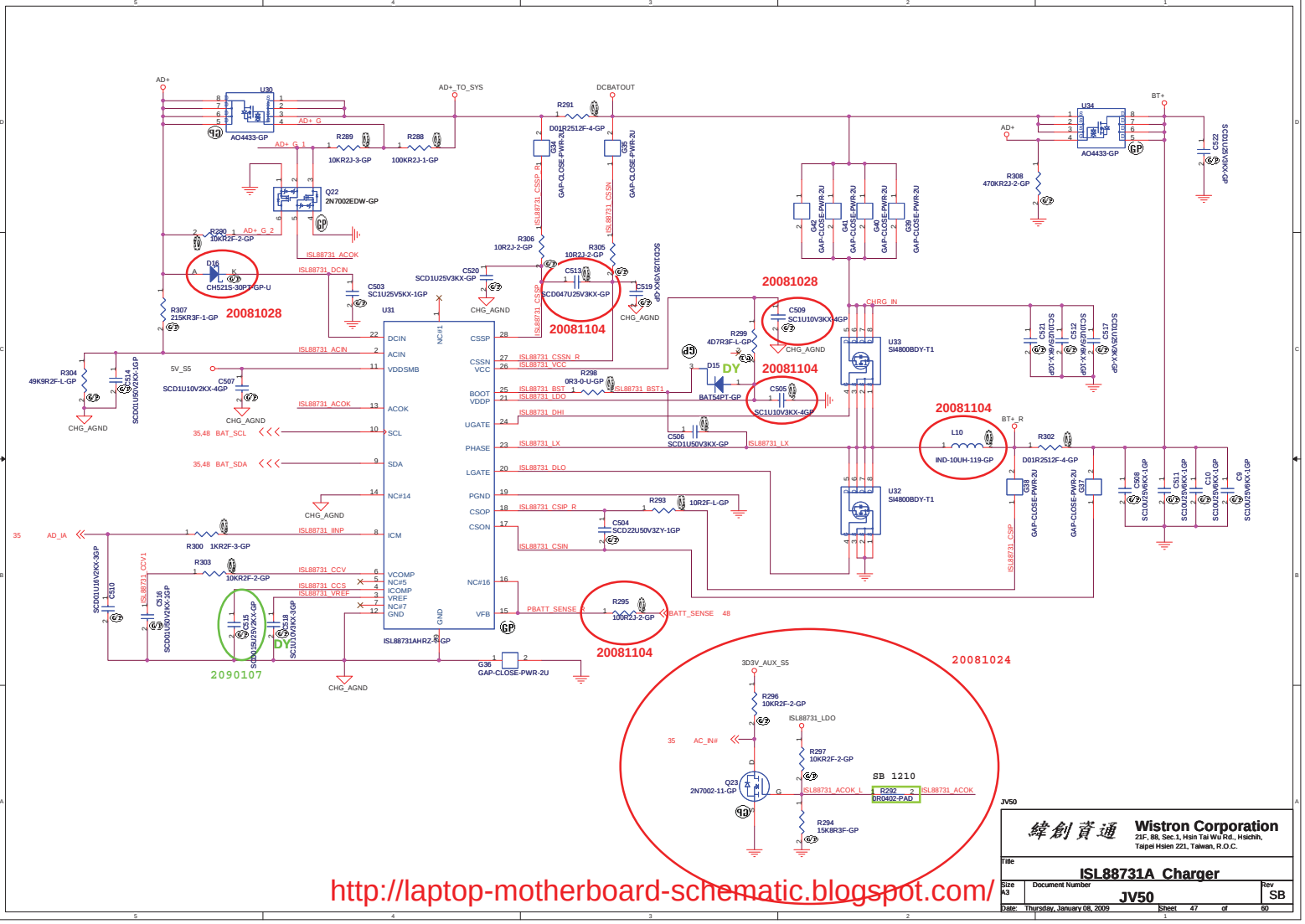
Date: Thursday, January 08, 2009 Sheet 45 of 60





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL88731A Charger

Size	Document Number	Rev
A3	JV50	SB

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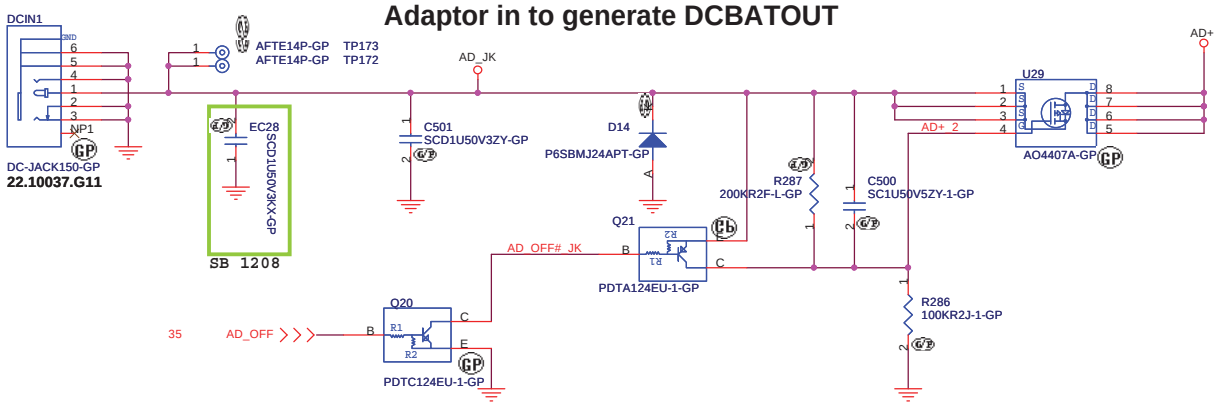
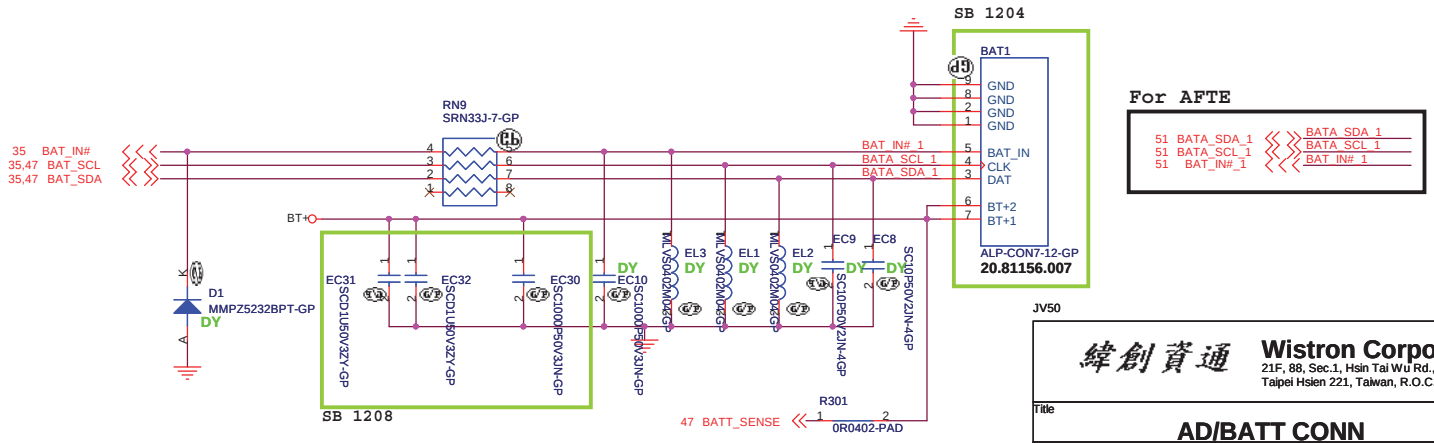
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JV50	SB

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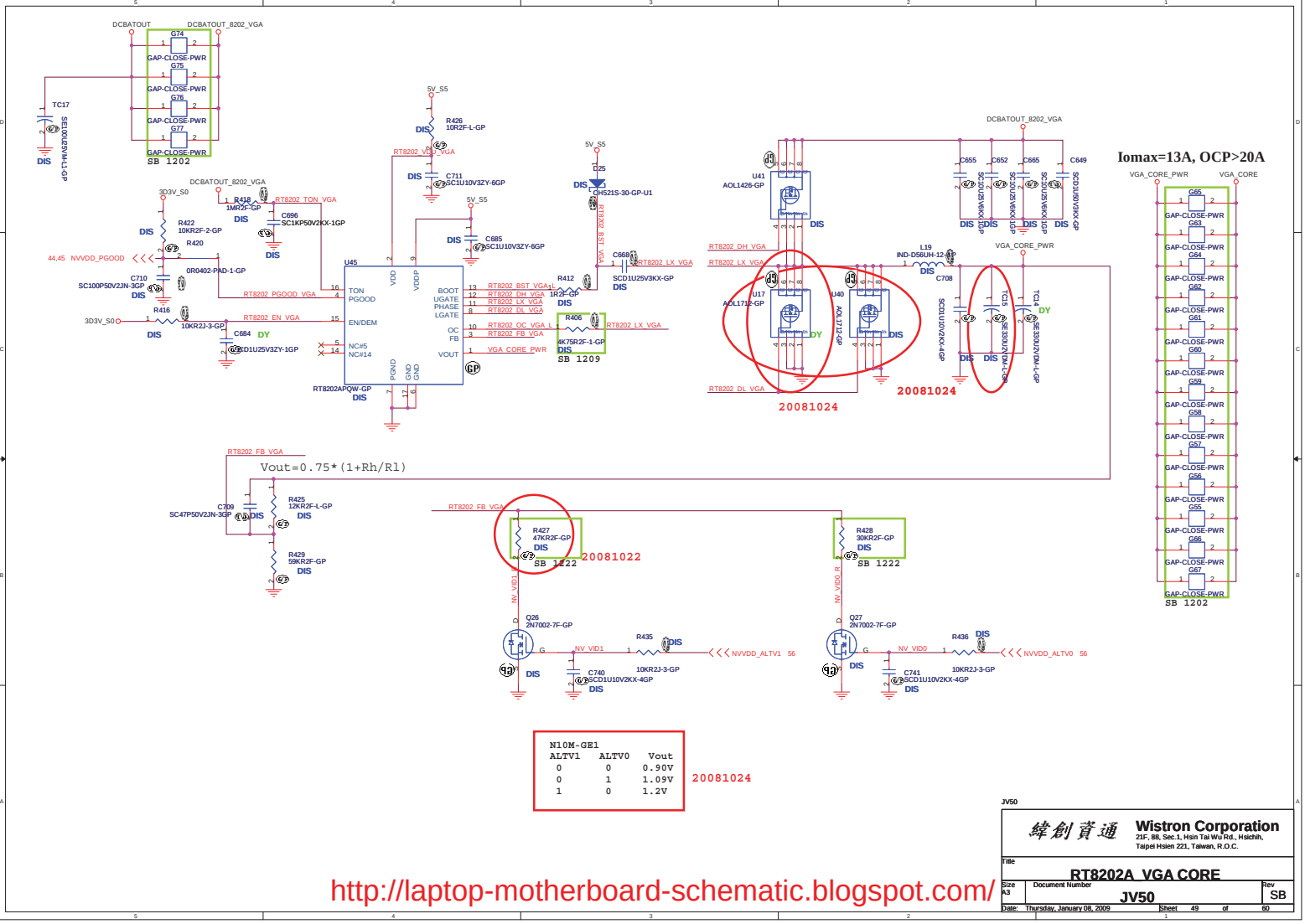


N10M-GE1		
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

20081024

JV50

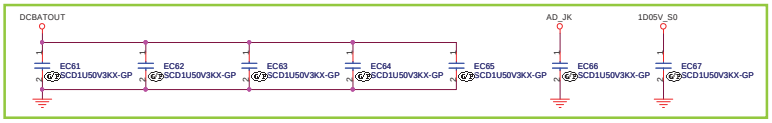
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202A VGA CORE

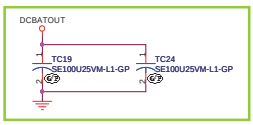
Size: A3 | Document Number: JV50 | Rev: SB

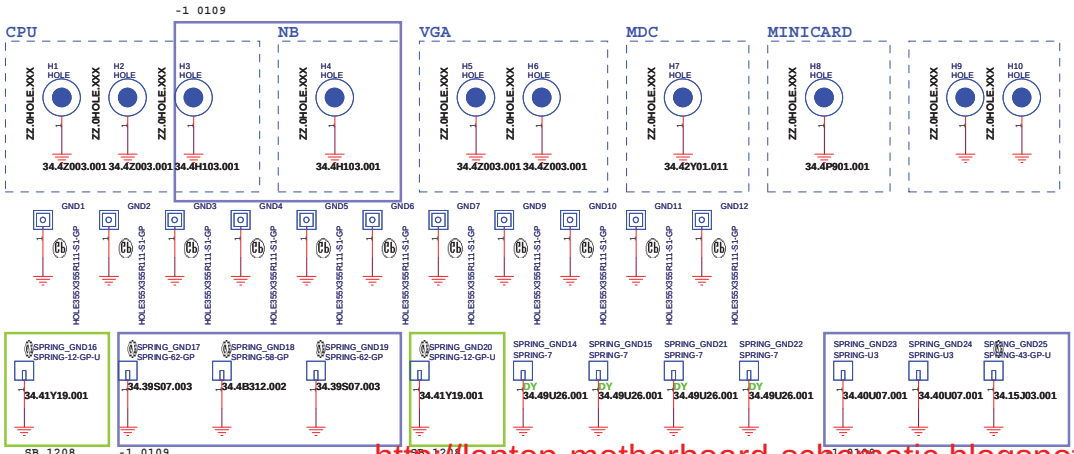
Date: Thursday, January 08, 2009 | Sheet 49 of 60

SB 1208



SB 1209





JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	EMI/Spring/Boss
Size / Document Number	JV50
Rev	SB
Date: Friday, January 09, 2009	Sheet 50 of 60

Check test point

	3D3V_S0	TP214 AFTE14P-GP
	3D3V_AUX_S5	TP213 AFTE14P-GP
	3D3V_S5	TP210 AFTE14P-GP
	5V_S5	TP209 AFTE14P-GP
13,35	PM_PWRBTN#	TP142 AFTE14P-GP
4,12,39	H_PWRGD	TP161 AFTE14P-GP
35,42	S5_ENABLE	TP160 AFTE14P-GP
4,6	H_CPURST#	TP112 AFTE14P-GP

Test Point放在Dimm Door打開可量測處

SPKR_L1 Conn. Test Point keep on conector side

28,29	SPKR_L+	TP7 AFTE14P-GP
28,29	SPKR_L-	TP8 AFTE14P-GP

FAN1 Conn. Test Point keep on conector side

34	EMC2102_FAN_TACH_1	TP175 AFTE14P-GP
34	EMC2102_FAN_DRIVE	TP176 AFTE14P-GP
		TP177 AFTE14P-GP

KB1 Conn. Test Point keep on connector side

35	KCOL1	TP48 AFTE14P-GP
35	KCOL2	TP64 AFTE14P-GP
35	KCOL3	TP47 AFTE14P-GP
35	KCOL4	TP55 AFTE14P-GP
35	KCOL5	TP38 AFTE14P-GP
35	KCOL6	TP65 AFTE14P-GP
35	KCOL7	TP42 AFTE14P-GP
35	KCOL8	TP61 AFTE14P-GP
35	KCOL9	TP45 AFTE14P-GP
35	KCOL10	TP56 AFTE14P-GP
35	KCOL11	TP39 AFTE14P-GP
35	KCOL12	TP62 AFTE14P-GP
35	KCOL13	TP46 AFTE14P-GP
35	KCOL14	TP59 AFTE14P-GP
35	KCOL15	TP43 AFTE14P-GP
35	KCOL16	TP60 AFTE14P-GP
35	KCOL17	TP44 AFTE14P-GP
35	KCOL18	TP57 AFTE14P-GP
35	KROW1	TP40 AFTE14P-GP
35	KROW2	TP52 AFTE14P-GP
35	KROW3	TP35 AFTE14P-GP
35	KROW4	TP53 AFTE14P-GP
35	KROW5	TP36 AFTE14P-GP
35	KROW6	TP37 AFTE14P-GP
35	KROW7	TP54 AFTE14P-GP
35	KROW8	TP51 AFTE14P-GP
		TP66 AFTE14P-GP

DB1 Conn. Test Point keep on conector side

	3D3V_S0	TP141 AFTE14P-GP
12,35,36	LPC_LAD0	TP140 AFTE14P-GP
12,35,36	LPC_LAD1	TP138 AFTE14P-GP
12,35,36	LPC_LAD2	TP137 AFTE14P-GP
12,35,36	LPC_LAD3	TP135 AFTE14P-GP
12,35,36	LPC_LFRAME#	TP133 AFTE14P-GP
7,13,25,31,32,33,35,36,52	PLT_RST1#	TP123 AFTE14P-GP
3,36	PCLK_FWH	TP117 AFTE14P-GP
		TP143 AFTE14P-GP

TPCN1 Conn. Test Point keep on conector side

	5V_S0	TP77 AFTE14P-GP
	5V_S0	TP93 AFTE14P-GP
37	TP_DATA	TP108 AFTE14P-GP
37	TP_CLK	TP106 AFTE14P-GP
		TP91 AFTE14P-GP
		TP90 AFTE14P-GP
37	TP_RIGHT	TP80 AFTE14P-GP
37	TP_LEFT	TP79 AFTE14P-GP

FPCN1 Conn. Test Point keep on connector side

	3D3V_FP_S0	TP126 AFTE14P-GP
	3D3V_FP_S0	TP125 AFTE14P-GP
37	USBPP6_1	TP128 AFTE14P-GP
37	USBPN6_1	TP127 AFTE14P-GP
35,37	FP_DETECT#	TP132 AFTE14P-GP
37	TP_LEFT	TP124 AFTE14P-GP
37	TP_RIGHT	TP131 AFTE14P-GP
		TP136 AFTE14P-GP
		TP134 AFTE14P-GP
		TP139 AFTE14P-GP

PSCN1 Conn. Test Point keep on connector side

	3D3V_S0	TP70 AFTE14P-GP
38	PWR_CON_BTN#_1	TP69 AFTE14P-GP
38	PWR_CON_LED#	TP67 AFTE14P-GP
38	Volume_Up#_1	TP58 AFTE14P-GP
38	Volume_Down#_1	TP63 AFTE14P-GP
		TP41 AFTE14P-GP

DCIN1 Conn. Test Point keep on connector side

	AD_JK	TP9 AFTE14P-GP
		TP10 AFTE14P-GP
		TP11 AFTE14P-GP
		TP12 AFTE14P-GP

TPCN1 Conn. Test Point keep on conector side

		TP13 AFTE14P-GP
		TP19 AFTE14P-GP
48	BATA_SDA_1	TP14 AFTE14P-GP
48	BATA_SCL_1	TP15 AFTE14P-GP
48	BAT_IN#_1	TP16 AFTE14P-GP
	BT+	TP17 AFTE14P-GP
	BT+	TP18 AFTE14P-GP

AMIC1 Conn. Test Point keep on connector side

18,27	INT_MIC1	TP6 AFTE14P-GP
		TP5 AFTE14P-GP

BT1 Conn. Test Point keep on connector side

13,23	USBPN7	TP217 AFTE14P-GP
13,23	USBPP7	TP218 AFTE14P-GP
		TP220 AFTE14P-GP
	3D3V_BT_S0	TP219 AFTE14P-GP

USBCN1 Conn. Test Point keep on connector side

		TP168 AFTE14P-GP
13,24	USB_OC#1	TP163 AFTE14P-GP
		TP162 AFTE14P-GP
13,24	USBPN1	TP164 AFTE14P-GP
13,24	USBPP1	TP166 AFTE14P-GP
13,24	USBPN2	TP165 AFTE14P-GP
13,24	USBPP2	TP167 AFTE14P-GP
24,35	USB_PWR_EN#	TP169 AFTE14P-GP
	5V_S5	TP170 AFTE14P-GP
	5V_S5	TP171 AFTE14P-GP

SPKR_R1 Conn. Test Point keep on conector side

28,29	SPKR_R+	TP24 AFTE14P-GP
28,29	SPKR_R-	TP21 AFTE14P-GP

JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AFTE_TP

Size	Document Number	Rev
A3	JV50	SB

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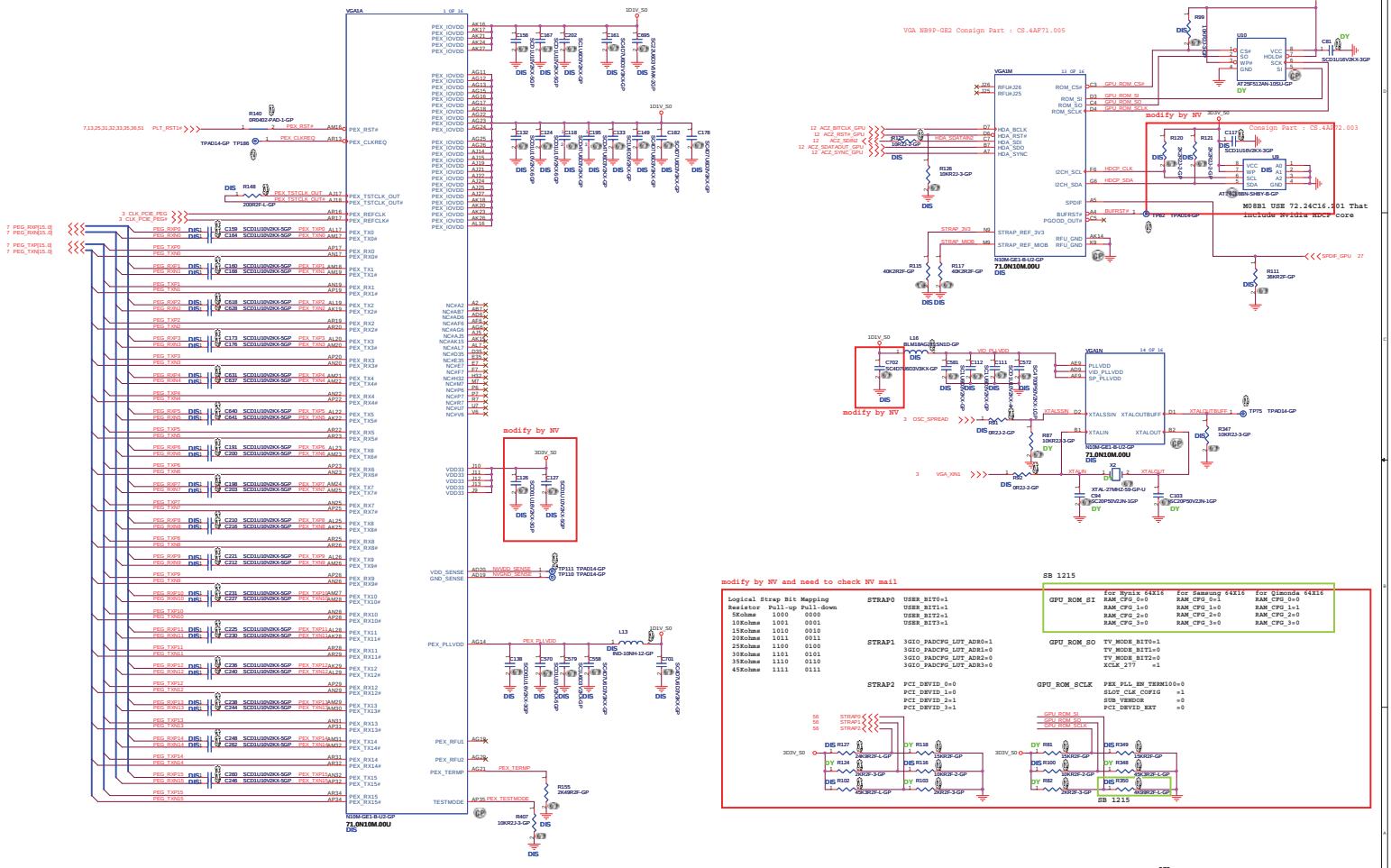
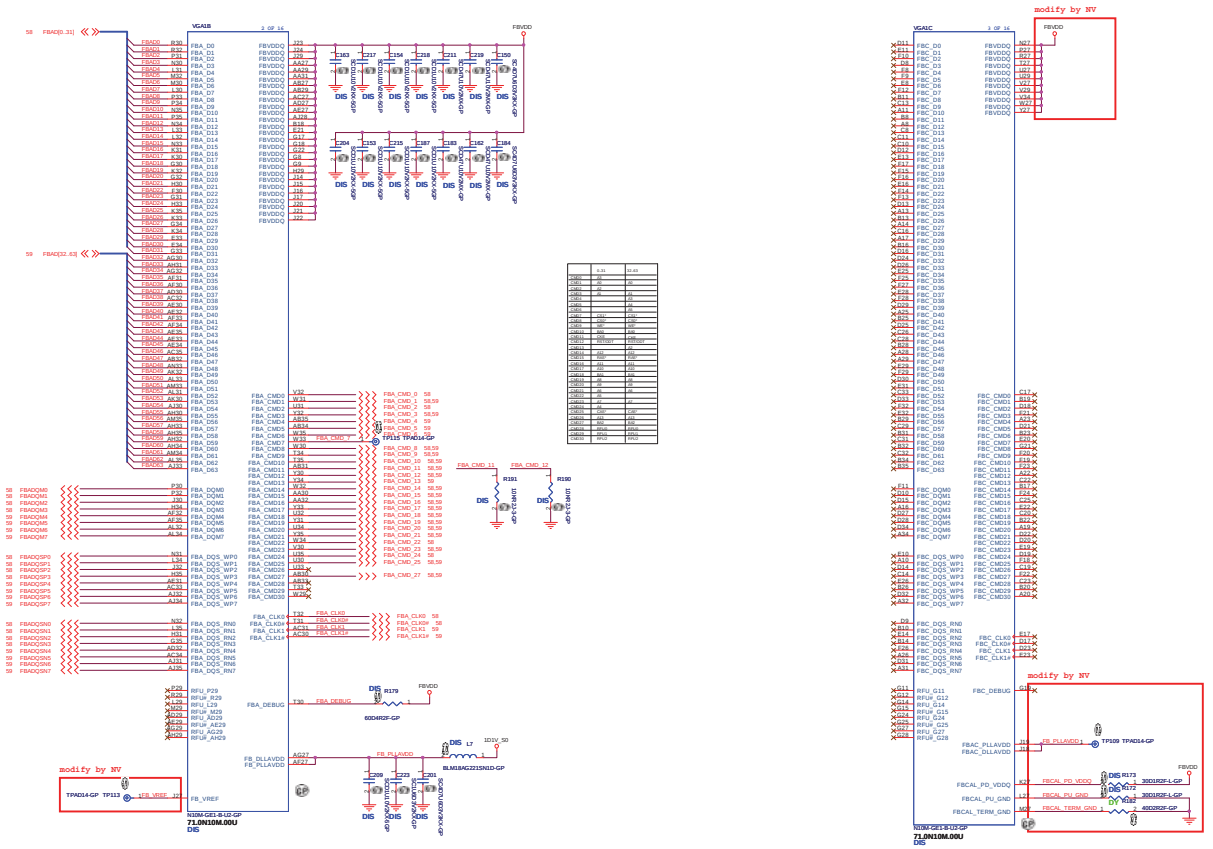

VGA NB9P-GE2 Consign Part : CS.4AF71.005
Consign Part : CS.4AP72.003
modify by NV
modify by NV and need to check NV mail
SB 1215
M08B1 USB 72.24C16.101 That include nvidia HDCP core
http://laptop-motherboard-schematic.blogspot.com/
Wistron Corporation
N10M(1/6)_PEG
JV50



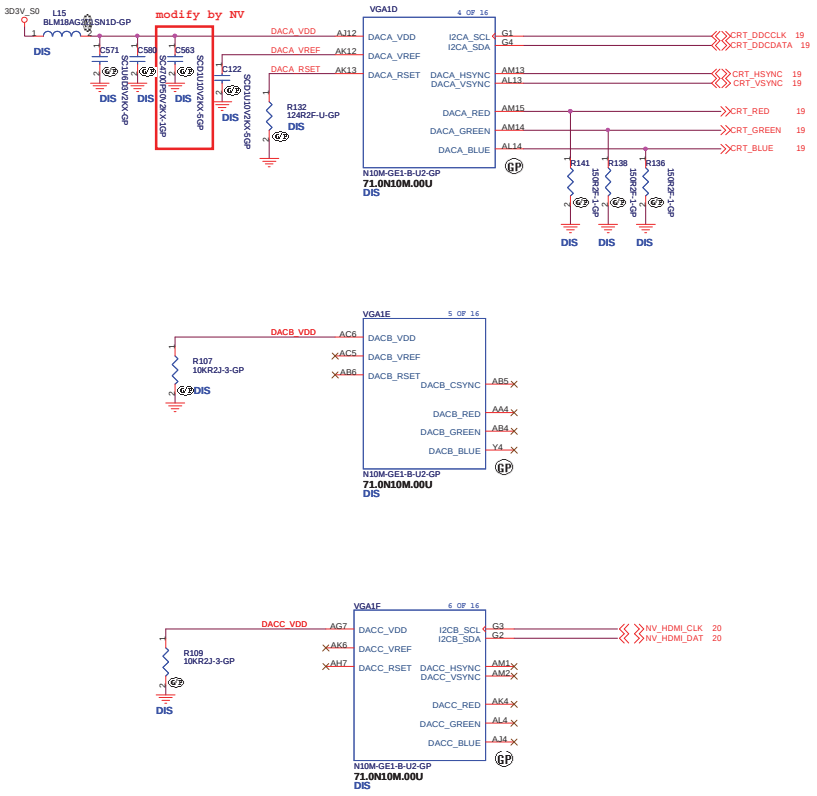
JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(2/6) MEMORY

Size: A2 | Document Number: JV50 | Rev: SB

Date: Thursday, January 08, 2009 | Sheet 53 of 60



JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *N10M(3/6) DAC*

Size: A3 | Document Number: JV50 | Rev: SB

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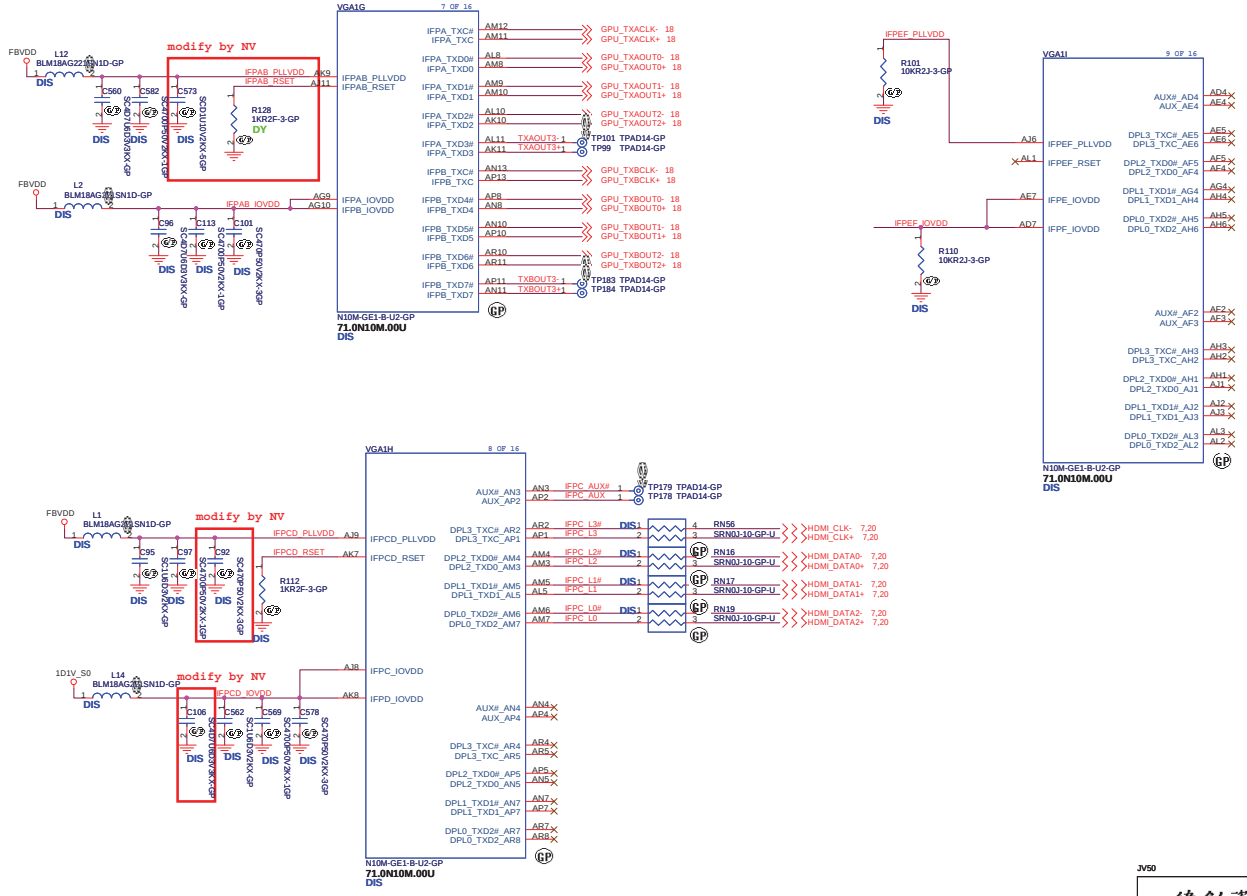

JV50

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Title	N10M(4/6)	
Size A3	Document Number JV50	Rev SB
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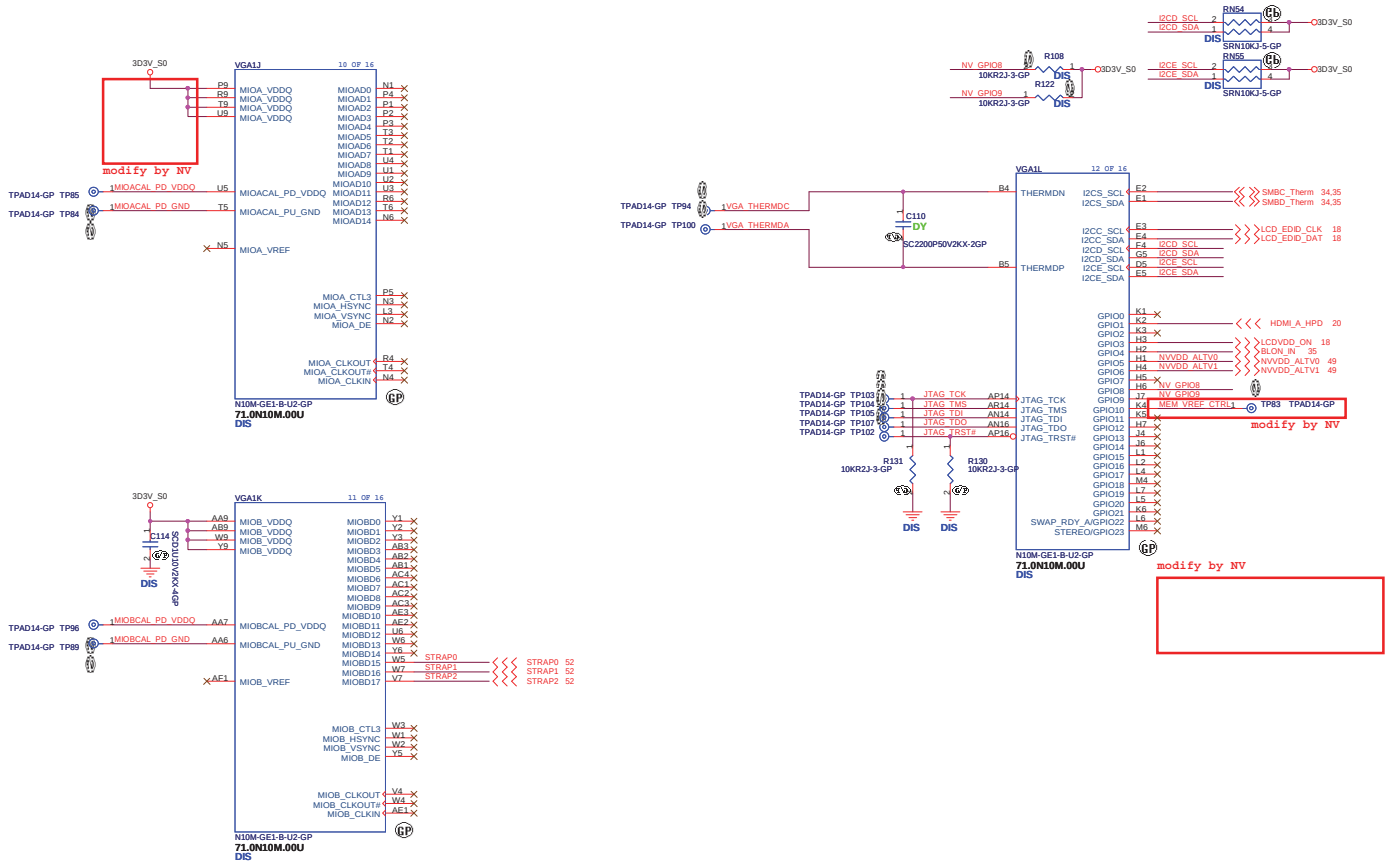
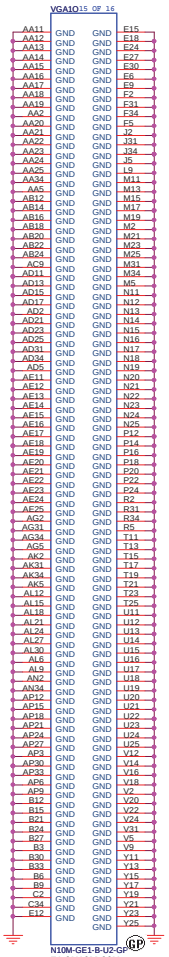
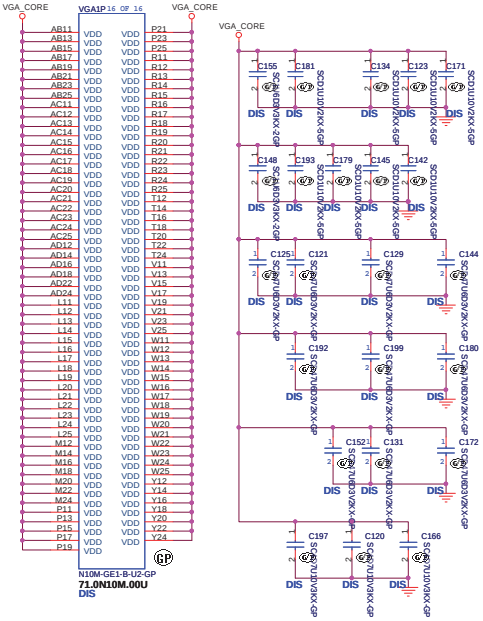


JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***N10M(5/6) MIO/ GPIO***
Size A3	Document Number **JV50** Rev **SB**
Date: Thursday, January 08, 2009	Sheet 56 of 60





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JV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(6/6) POWER***

Size	Document Number	Rev
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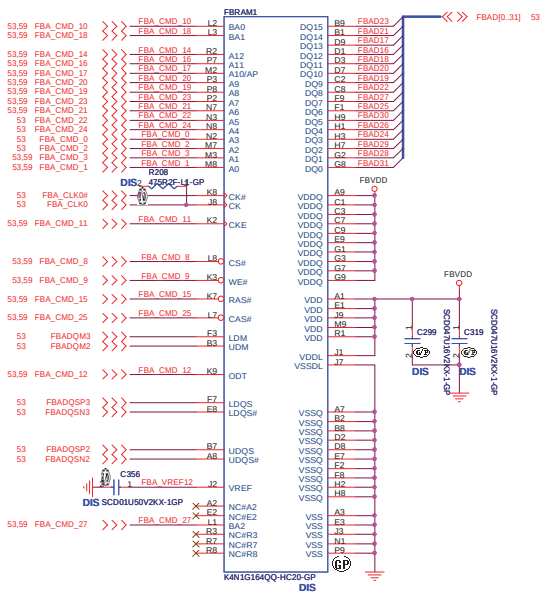
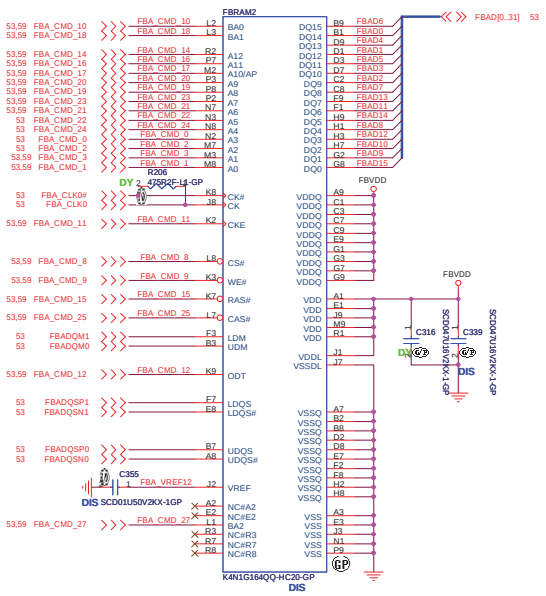
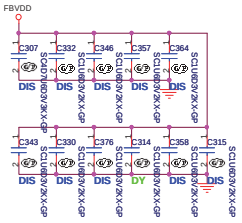
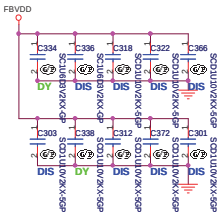
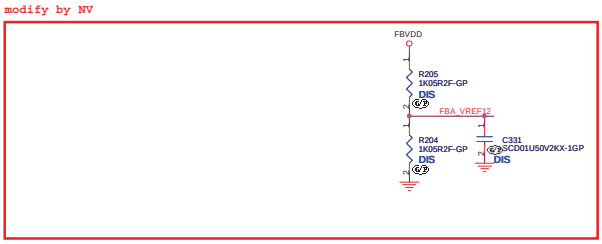








modify by NV



http://laptop-motherboard-schematic.blogspot.com/

JV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(1/2)**

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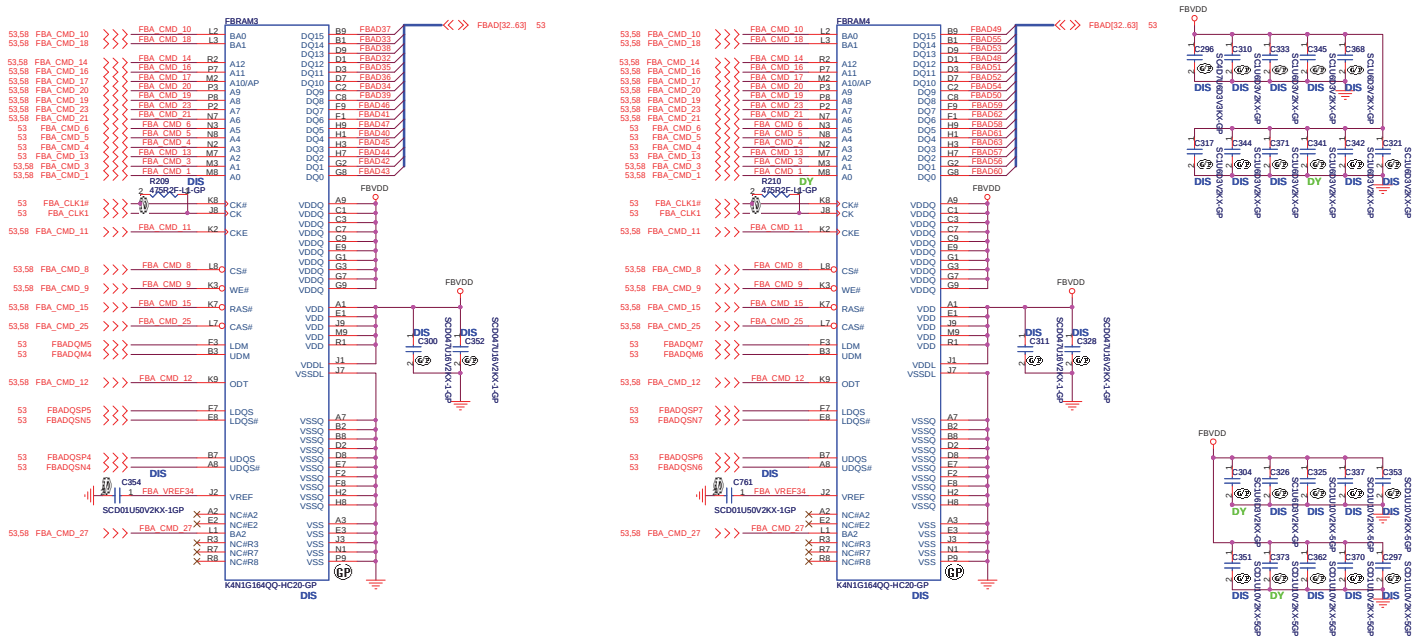
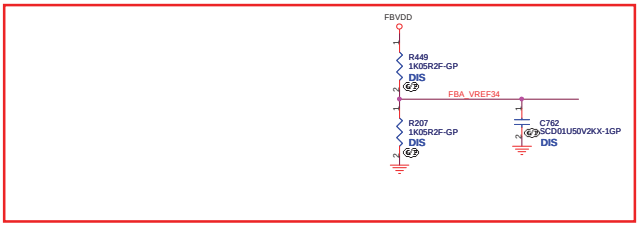


modify by NV



SB
All Component for NB9P-GE2

JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VRAM(2/2)
Size A3	Document Number JV50
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SB SB SC -1

12/02

Page3: change C452 C453 from 27P to 33P by vendor's request

Page33: add C872 33P for SIV

Page29: change SPKR_R1 SPKR_L1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page18: change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request

Page24: change USBCN1 from 20.F1290.015 to 20.F1035.015 by CE's request

Page38: change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request

Page18: change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page3: add R554 and change U24 pin16 from 3D3V_S0 to 3D3V_VDD48_S0

Page3: change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount

Page7: change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection

Page9: change C275 from UMA to DY and change C349 from mount to DY

Page10: change C243 C758 from mount to DY and change R167 R398 from DIS to DY

Page13: change R216 from 0ohm resistor to 0ohm pad

Page14: change C413 C252 C703 C392 C707 C734 from mount to DY

Page17: change C426 C429 from mount to DY

Page18: change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA

Page20: add RN86 for DIS HDMI SMbus

Page25: change R45 from 0ohm resistor to 0ohm pad

Page27: change R523 from 0ohm resistor to 0ohm pad

Page7: add R556 pull-low DY for A1 NB

Page28: change AGND & GND and change R509 from 0ohm resistor to 0ohm pad

Page28: change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2

Page28: combine C801 C802 two 1u to C801 4.7u

Page28: delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31

Page28: change R474 from DY to mount and change R475 from mount to DY for 10dB

Page29: add L29 L30 L31 L32 L33 L34 for ESD

Page31: change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad

Page32: change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad

Page12: change C385 C386 from 10p to 7p by vendor's request

Page35: change C136 C169 from 15p to 7p by vendor's request

Page33: change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY

Page34: change C42 from mount to DY

Page35: change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version

Page36: change DB1 from mount to DY

Page38: add Q35 PWR_LED7 PWR_LED8 and change RN4 from 4P2R to 8P4R and change PWR_LED5 PWR_LED6 from 83.01221.I70 to 83.00193.A70 for LED type

Page39: change U66 pin1 from CPUCORE_ON to 1D5V_PWRGD and change D13 pin1 from S5_ENABLE to 3V/5V_EN

Page40: update power sequence logic

Page41: change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad

Page42: change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap

Page43: change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap

Page43: change R246 pin2 from CPUCORE_ON to 1D5V_PWRGD and add R500 pull-high 10K 3D3V_S5

Page45: change G100-G109 from open gap to close gap

Page46: change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap

Page46: delete TC19 and change TC20 from DY to GFX

Page49: change G55-G67 G74-G77 from open gap to close gap

Page29: change RN75 from 47ohm to 75ohm

Page28: change C804 C807 from 4.7u to 1u 25V X5R

Page45: delete TC24

Page19: delete R104 R129

12/04

Page24: change U47 from 74.00545.A79 to 74.00547.A79

Page20: swap HDMI signals for routing

Page28: change U53 pin22 from AUD_HP1_EN to AMP_MUTE#_R

Page48: change BAT1 from 20.81094.007 to 20.81156.007

Page22: change ODD1 from 62.10065.541 to 62.10065.751

Page22: change R231 R247 from 0ohm resistor to 0ohm pad

12/05

Page25: change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad

Page46: change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request

Page41: change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request

Page41: change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request

Page45: change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request

12/08

Page26: change EC7 from DY to mount EMI's request

Page48: change EC28 EC30 EC31 EC32 from DY to mount EMI's request

Page31: change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request

Page5: change C79 C80 from DY to mount EMI's request

Page46: change C659 from DY to GFX EMI's request

Page50: change SPRING_GND16-SPRING_GND20 from DY to mount EMI's request

Page50: add EC61-EC67 0.1u by EMI's request

Page20: change R313 R314 from 10K 100K to 18K 47K by NV's request

Page35: change U14 pin83 RN65 pin2 from SHBM to DBC_EN by annie's request

Page18: change LCD1 pin35 from NC to DBC_EN by annie's request

Page20: add ER1-ER8 0ohm pad by EMI's request

Page10: change C636 from 1000p DY to 27p mount by RF's request

12/09

Page49: change R406 from 6K2 to 4K75 by power team's request

Page46: change TC16 from mount to GFX

Page50: add TC19 TC24 100u

Page41: change C528 C529 530 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY

Page46: change C656 C653 from 10u to 4.7u and change C653 from GFX to DY

Page42: change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY

Page41: change TC5 from DY to mount

Page5: change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount

Page17: change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount

Page16: change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount

Page20: change HDMI from 62.10078.161 to 62.10078.171 by CE's request

Page24: change USBCN1 from 20.F1035.015 to 20.F1290.015 by CE's request

12/10

Page46: add C873 33p GFX by RF's request

Page43: add C874 C875 33p by RF's request

Page20: swap U8 pin13 14 47 48

Page33: change R16 from DY to mount

Page47: change R292 from 0ohm resistor to 0ohm pad

12/11

Page33: change PWR1 pin1 from 5V_S5_MIN1 to 5V_S5_MIN2

12/15

Page52: change VRAM strap R350

JV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

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SB SB SC -1

12/22

Page49: change R427 from 30K 47K and R428 from 47K to 30K

SC

12/22

Page42: modify by power team's request

Page35: change R372 R395 from DY to mount and change R373 R394 from mount to DY

-1

01/06

Page17: change C400 from mount to DY and change C399 from DY to mount

Page30: change R267 from 39R to 0ohm pad

Page38: delete RN7 and add Q36 Q37

Page25: change U3 pin 38 52 from LAN_AVDD to TP and change U3 pin 68 from NC to TP

Page25: delete R58 and add RN87 and change U5 to 72.24C02.R01

Page3: change R255 from 22R to 33R and change RN42 from 0ohm to 33R

Page33: change R268 R275 R259 from 0ohm resistor to 0ohm pad

Page35: change R394 from DY to mount and change R395 from mount to DY

Page28: change R526 from 0ohm resistor to 0ohm pad

Page35: change R401 from 0ohm resistor to 0ohm pad

Page35: delete Q12 and add R502 R503

Page35: change RN23 pin 5 6 from 3D3V_AUX_S5 to 3D3V_S0

Page44: change U46 to APL5930 by power team's request

Page38: add 3G and BT option

Page28: change R479 from 8K2 to 10K and change R480 from 6K2 to 4K99 for audio speaker gain

Page28: merge CCD1 to LCD1

01/07

Page44: change R437 from 0ohm pad to 0ohm resistor

Page9: change TC18 from UMA to DY and change C276 from DY to mount

Page35: delete RN21 and add R507 10K DY

Page38: change RN4 to 330R and change RN8 to 100R and delete R10 and change RN3 to 8P4R 200R

Page47: change C515 to 78.15322.2FL by power team's request

Page3: mount 33p on EC23 EC24 EC25 EC39 EC48 for RF's request

Page3: add EC68 EC69 33p DY by RF's request

Page20: add R129 4K7 for diffierent vendor

01/08

Page42: change R541 from 200K to 100K and change R544 location

Page42: change R532 R545 from 0ohm pad to 0ohm resistor

01/09

Page38: change name from 3G/BT_LED1 to 3GBT_LED1

Page50: add SPRING_GND23 34.40U07.001, SPRING_GND24 34.40U07.001, SPRING_GND25 34.15J03.001

Page50: SPRING_GND17, SPRING_GND19 change from 34.41Y19.001 to 34.39S07.003

Page50: SPRING_GND18 change from 34.41Y19.001 to 34.4B312.002

JV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HISTORY
Size A2 / Document Number	JV50 / Rev SB
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