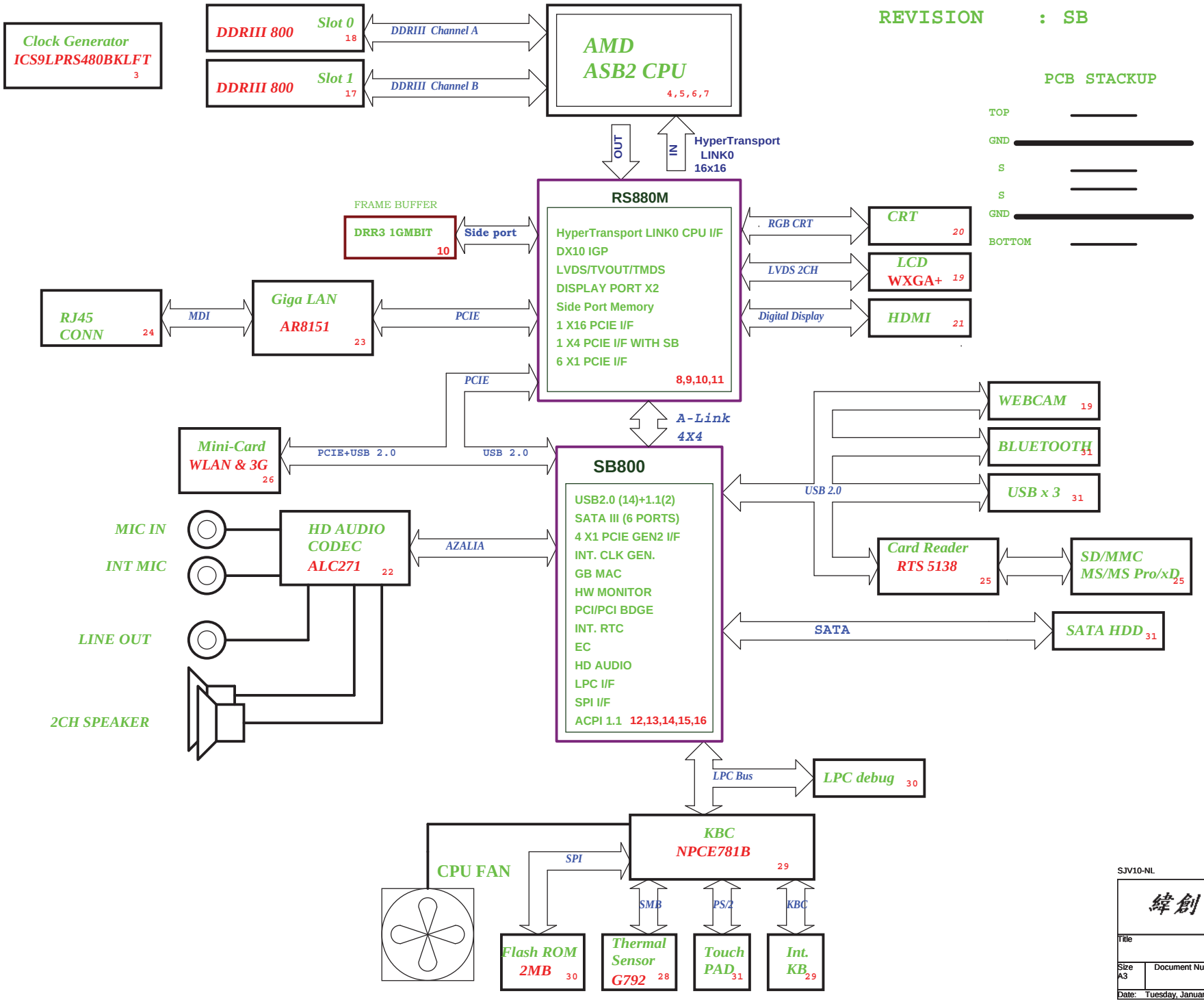
JV10-NL Block Diagram

Project code: 91.4HX01.001
PCB P/N : 48.4HX01.0SB
REVISION : SB



PCB STACKUP

TOP	
GND	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8223 34

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC RT8209E 35

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(7.5A)

SYSTEM DC/DC RT8209E 36

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(11A)

RT9026 35

5V_S5	DDR_VREF_S3

RT9025 37

3D3V_S5	1D1V_S5

RT9025 37

3D3V_S5	CPU_VDDR

CHARGER ISL88731A 38

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 33

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

SJV10-NL

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

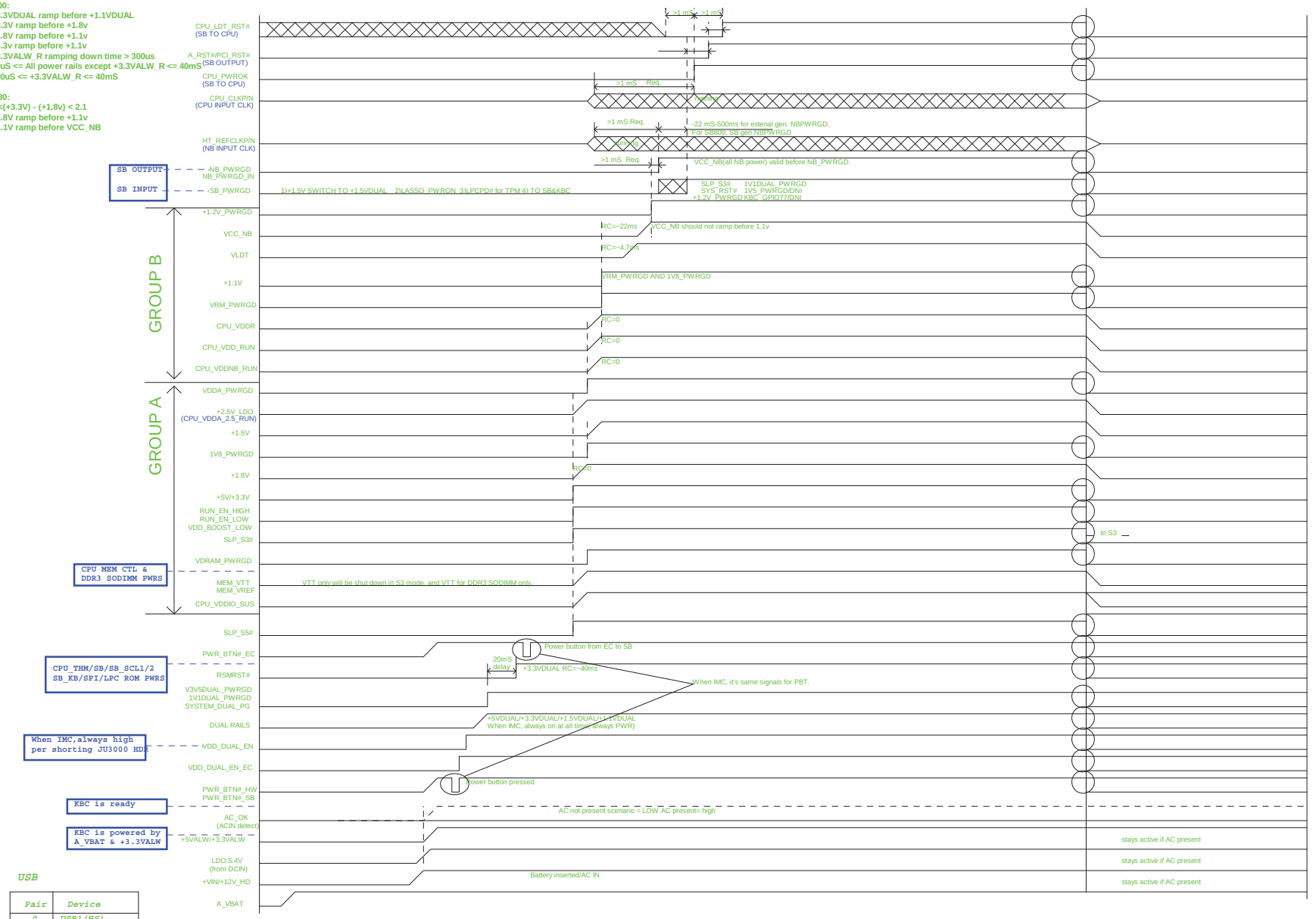
Size	Document Number	Rev
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Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



USB

Pair	Device
0	USB1(HS)
1	MINICARD1
2	NC
3	NC
4	Cardreader
5	USB2
6	USB3
7	Blue Tooth
8	NC
9	WECAM
10	NC
11	MINIC2(3G sim)
12	MINIC2(3G)
13	NC

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

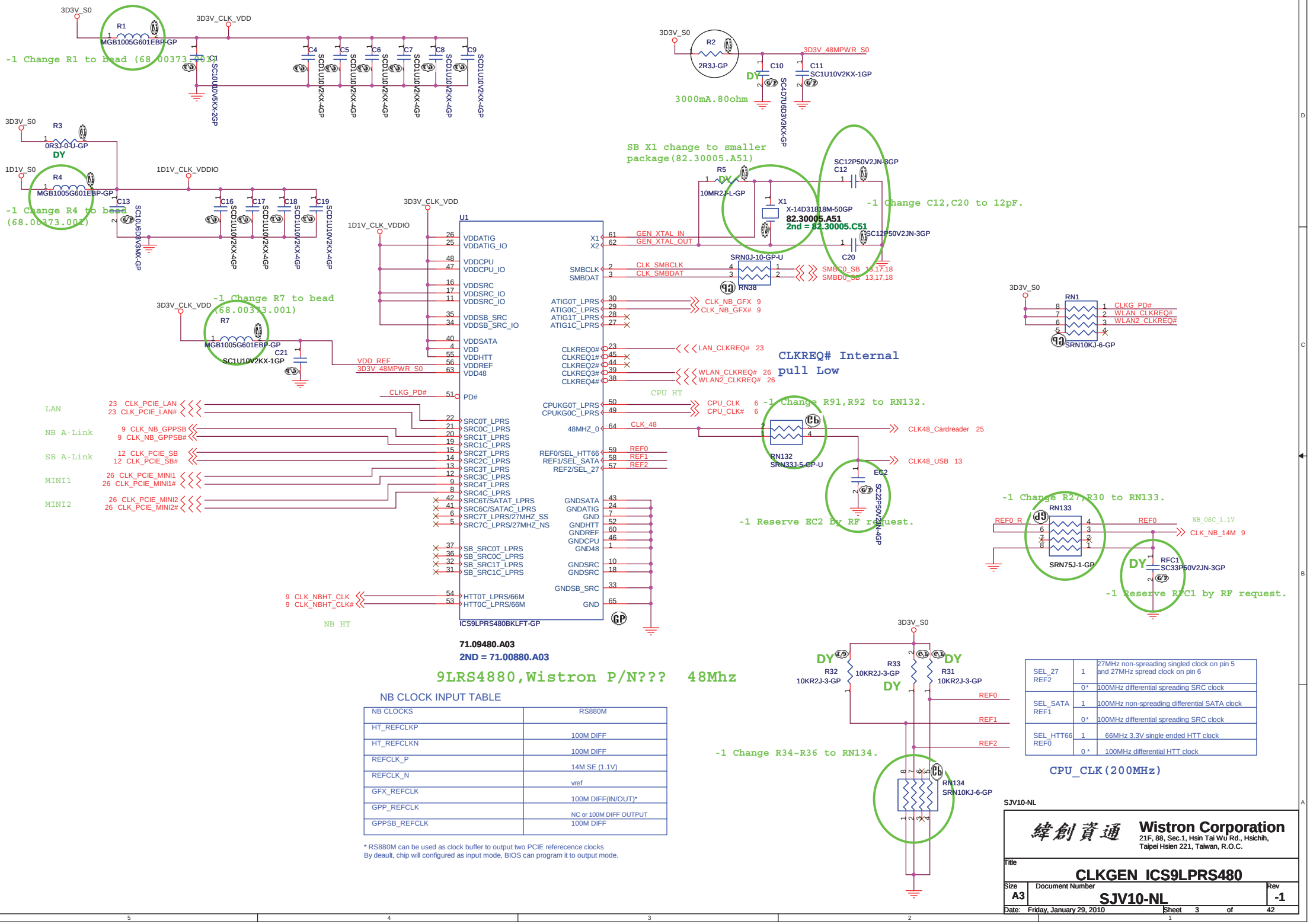
SJV10-NL

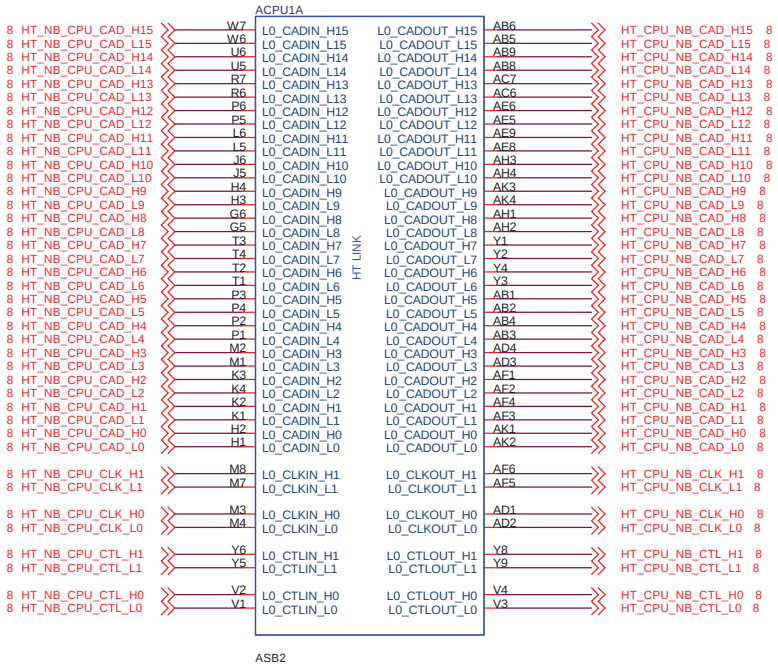
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Table of Content***

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-1 Change R1 to bead (68.00373.001)
-1 Change R4 to bead (68.00373.002)
-1 Change R7 to bead (68.00373.001)
SB X1 change to smaller package(82.30005.A51)
-1 Change C12,C20 to 12pF.
82.30005.A51
2nd = 82.30005.C51
CLKREQ# Internal pull Low
-1 Change R91,R92 to RN132.
-1 Reserve EC2 by RF request.
-1 Change R27,R30 to RN133.
-1 Reserve RFC1 by RF request.
-1 Change R34~R36 to RN134.
CPU_CLK(200MHz)
71.09480.A03
2ND = 71.00880.A03
9LRS4880,Wistron P/N??? 48Mhz
ICS9LPRS480BKLFT-GP
NB CLOCK INPUT TABLE
NB CLOCKS | RS880M
HT_REFCLKP | 100M DIFF
HT_REFCLKN | 100M DIFF
REFCLK_P | 14M SE (1.1V)
REFCLK_N | vref
GFX_REFCLK | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF
* RS880M can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
SEL_27 REFC2 | 1 | 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0* | 100MHz differential spreading SRC clock
SEL_SATA REF1 | 1 | 100MHz non-spreading differential SATA clock
0* | 100MHz differential spreading SRC clock
SEL_HTT66 REF0 | 1 | 66MHz 3.3V single ended HTT clock
0* | 100MHz differential HTT clock
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN ICS9LPRS480
Size A3
Document Number SJV10-NL
Rev -1
Date: Friday, January 29, 2010
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71.TURON.B0U

SJV10-NL

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU HT LINK I/F (1/4)

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17 M_A_DQ[63..0]
17 M_A_A[15..0]
17 M_A_DM[7..0]
17 M_A_DQS#[7..0]
17 M_A_DQS[7..0]

18 M_B_DQ[63..0]
18 M_B_A[15..0]
18 M_B_DM[7..0]
18 M_B_DQS#[7..0]
18 M_B_DQS[7..0]

ACPU1B

DDR III: CHANNEL A

M_A_A15	P30	MA_ADD15	MA_DATA63	AG11	M_A_DQ63
M_A_A14	M29	MA_ADD14	MA_DATA62	AH11	M_A_DQ62
M_A_A13	AG28	MA_ADD13	MA_DATA61	AJ12	M_A_DQ61
M_A_A12	P28	MA_ADD12	MA_DATA60	AJ14	M_A_DQ60
M_A_A11	T30	MA_ADD11	MA_DATA59	AF11	M_A_DQ59
M_A_A10	AC28	MA_ADD10	MA_DATA58	AF12	M_A_DQ58
M_A_A9	P27	MA_ADD9	MA_DATA57	AG12	M_A_DQ57
M_A_A8	R26	MA_ADD8	MA_DATA56	AH12	M_A_DQ56
M_A_A7	R27	MA_ADD7	MA_DATA55	AK14	M_A_DQ55
M_A_A6	U28	MA_ADD6	MA_DATA54	AF15	M_A_DQ54
M_A_A5	V30	MA_ADD5	MA_DATA53	AH19	M_A_DQ53
M_A_A4	U27	MA_ADD4	MA_DATA52	AK20	M_A_DQ52
M_A_A3	Y30	MA_ADD3	MA_DATA51	AF14	M_A_DQ51
M_A_A2	AB29	MA_ADD2	MA_DATA50	AG14	M_A_DQ50
M_A_A1	W29	MA_ADD1	MA_DATA49	AF17	M_A_DQ49
M_A_A0	AC26	MA_ADD0	MA_DATA48	AG19	M_A_DQ48
			MA_DATA47	AG20	M_A_DQ47
17 M_A_BS2	R29	MA_BANK2	MA_DATA46	AJ20	M_A_DQ46
17 M_A_BS1	AC29	MA_BANK1	MA_DATA45	AF22	M_A_DQ45
17 M_A_BS0	AE28	MA_BANK0	MA_DATA44	AK24	M_A_DQ44
			MA_DATA43	AF19	M_A_DQ43
	K30	MA_CHECK7	MA_DATA42	AF20	M_A_DQ42
	J29	MA_CHECK6	MA_DATA41	AJ23	M_A_DQ41
	G29	MA_CHECK5	MA_DATA40	AG23	M_A_DQ40
	F29	MA_CHECK4	MA_DATA39	AF23	M_A_DQ39
	L28	MA_CHECK3	MA_DATA38	AF25	M_A_DQ38
	L29	MA_CHECK2	MA_DATA37	AH27	M_A_DQ37
	H29	MA_CHECK1	MA_DATA36	AK30	M_A_DQ36
	H27	MA_CHECK0	MA_DATA35	AJ25	M_A_DQ35
			MA_DATA34	AG25	M_A_DQ34
	J27	MA_DQS_H8	MA_DATA33	AJ26	M_A_DQ33
	J26	MA_DQS_L8	MA_DATA32	AJ28	M_A_DQ32
M_A_DQS7	AJ11	MA_DQS_H7	MA_DATA31	D28	M_A_DQ31
M_A_DQS#7	AK12	MA_DQS_L7	MA_DATA30	G28	M_A_DQ30
M_A_DQS6	AG15	MA_DQS_H6	MA_DATA29	D26	M_A_DQ29
M_A_DQS#6	AH15	MA_DQS_L6	MA_DATA28	E26	M_A_DQ28
M_A_DQS5	AH22	MA_DQS_H5	MA_DATA27	F30	M_A_DQ27
M_A_DQS#5	AG22	MA_DQS_L5	MA_DATA26	E29	M_A_DQ26
M_A_DQS4	AG26	MA_DQS_H4	MA_DATA25	F27	M_A_DQ25
M_A_DQS#4	AH26	MA_DQS_L4	MA_DATA24	H26	M_A_DQ24
M_A_DQS3	E28	MA_DQS_H3	MA_DATA23	H25	M_A_DQ23
M_A_DQS#3	F28	MA_DQS_L3	MA_DATA22	D24	M_A_DQ22
M_A_DQS2	E25	MA_DQS_H2	MA_DATA21	H22	M_A_DQ21
M_A_DQS#2	F25	MA_DQS_L2	MA_DATA20	E22	M_A_DQ20
M_A_DQS1	G17	MA_DQS_H1	MA_DATA19	F26	M_A_DQ19
M_A_DQS#1	H17	MA_DQS_L1	MA_DATA18	G26	M_A_DQ18
M_A_DQS0	E12	MA_DQS_H0	MA_DATA17	D22	M_A_DQ17
M_A_DQS#0	F12	MA_DQS_L0	MA_DATA16	G23	M_A_DQ16
			MA_DATA15	G22	M_A_DQ15
	AK18	MA_CLK_H7	MA_DATA14	G20	M_A_DQ14
	AJ17	MA_CLK_L7	MA_DATA13	G15	M_A_DQ13
	AH17	MA_CLK_H6	MA_DATA12	F15	M_A_DQ12
	AG17	MA_CLK_L6	MA_DATA11	D20	M_A_DQ11
17 M_CLK_DDR0	Y28	MA_CLK_H5	MA_DATA10	F22	M_A_DQ10
17 M_CLK_DDR#0	Y27	MA_CLK_L5	MA_DATA9	D16	M_A_DQ9
17 M_CLK_DDR1	AB27	MA_CLK_H4	MA_DATA8	E17	M_A_DQ8
17 M_CLK_DDR#1	AB26	MA_CLK_L4	MA_DATA7	H15	M_A_DQ7
	W27	MA_CLK_H3	MA_DATA6	H14	M_A_DQ6
	W26	MA_CLK_L3	MA_DATA5	G12	M_A_DQ5
	P26	MA_CLK_H2	MA_DATA4	H12	M_A_DQ4
	M26	MA_CLK_L2	MA_DATA3	E15	M_A_DQ3
	D18	MA_CLK_H1	MA_DATA2	E14	M_A_DQ2
	F19	MA_CLK_L1	MA_DATA1	E11	M_A_DQ1
	E20	MA_CLK_H0	MA_DATA0	F11	M_A_DQ0
	E19	MA_CLK_L0			
				H30	
17 M_CKE1	M30	MA_CKE1	MA_DM8	AL12	M_A_DM7
17 M_CKE0	M28	MA_CKE0	MA_DM7	AK16	M_A_DM6
			MA_DM6	AK22	M_A_DM5
	AJ29	MA1_ODT1	MA_DM5	AJ27	M_A_DM4
	AF27	MA1_ODT0	MA_DM4	E27	M_A_DM3
17 M_ODT1	AJ30	MA0_ODT1	MA_DM3	E23	M_A_DM2
17 M_ODT0	AG29	MA0_ODT0	MA_DM2	H19	M_A_DM1
			MA_DM1	G14	M_A_DM0
	AH29	MA1_CS_L1	MA_DM0		
	AE29	MA1_CS_L0			
17 M_CS#1	AH30	MA0_CS_L1			
17 M_CS#0	AF29	MA0_CS_L0			
17 M_A_RAS#	AC27	MA_RAS_L			
17 M_A_CAS#	AF30	MA_CAS_L			
17 M_A_WE#	AE27	MA_WE_L			
17 DDR3_DRAMRST_A#	L27	MA_RESET_L			
17 PM_EXTTS#0	M32	FREE|MA_EVENT_L			

GENEVA-GP

ACPU1C

DDR III: CHANNEL B

M_B_A15	P33	MB_ADD15	MB_DATA63	AN13	M_B_DQ63
M_B_A14	P31	MB_ADD14	MB_DATA62	AL14	M_B_DQ62
M_B_A13	AJ33	MB_ADD13	MB_DATA61	AL16	M_B_DQ61
M_B_A12	T32	MB_ADD12	MB_DATA60	AN17	M_B_DQ60
M_B_A11	T31	MB_ADD11	MB_DATA59	AN12	M_B_DQ59
M_B_A10	AD32	MB_ADD10	MB_DATA58	AM12	M_B_DQ58
M_B_A9	T33	MB_ADD9	MB_DATA57	AM16	M_B_DQ57
M_B_A8	V32	MB_ADD8	MB_DATA56	AN16	M_B_DQ56
M_B_A7	U33	MB_ADD7	MB_DATA55	AL18	M_B_DQ55
M_B_A6	V33	MB_ADD6	MB_DATA54	AN19	M_B_DQ54
M_B_A5	V31	MB_ADD5	MB_DATA53	AM24	M_B_DQ53
M_B_A4	W33	MB_ADD4	MB_DATA52	AN24	M_B_DQ52
M_B_A3	Y31	MB_ADD3	MB_DATA51	AM18	M_B_DQ51
M_B_A2	Y33	MB_ADD2	MB_DATA50	AN18	M_B_DQ50
M_B_A1	Y32	MB_ADD1	MB_DATA49	AL22	M_B_DQ49
M_B_A0	AC33	MB_ADD0	MB_DATA48	AN23	M_B_DQ48
			MB_DATA47	AM25	M_B_DQ47
18 M_B_BS2	R33	MB_BANK2	MB_DATA46	AL26	M_B_DQ46
18 M_B_BS1	AD33	MB_BANK1	MB_DATA45	AN28	M_B_DQ45
18 M_B_BS0	AE33	MB_BANK0	MB_DATA44	AL28	M_B_DQ44
			MB_DATA43	AL24	M_B_DQ43
	K33	MB_CHECK7	MB_DATA42	AN25	M_B_DQ42
	K31	MB_CHECK6	MB_DATA41	AN27	M_B_DQ41
	G32	MB_CHECK5	MB_DATA40	AM28	M_B_DQ40
	F32	MB_CHECK4	MB_DATA39	AM29	M_B_DQ39
	L33	MB_CHECK3	MB_DATA38	AL30	M_B_DQ38
	K32	MB_CHECK2	MB_DATA37	AL32	M_B_DQ37
	H31	MB_CHECK1	MB_DATA36	AL33	M_B_DQ36
	G33	MB_CHECK0	MB_DATA35	AK28	M_B_DQ35
			MB_DATA34	AN29	M_B_DQ34
	J33	MB_DQS_H8	MB_DATA33	AM31	M_B_DQ33
	H32	MB_DQS_L8	MB_DATA32	AM32	M_B_DQ32
M_B_DQS7	AM14	MB_DQS_H7	MB_DATA31	E33	M_B_DQ31
M_B_DQS#7	AN14	MB_DQS_L7	MB_DATA30	D31	M_B_DQ30
M_B_DQS6	AL20	MB_DQS_H6	MB_DATA29	B31	M_B_DQ29
M_B_DQS#6	AM20	MB_DQS_L6	MB_DATA28	A31	M_B_DQ28
M_B_DQS5	AN26	MB_DQS_H5	MB_DATA27	E33	M_B_DQ27
M_B_DQS#5	AM26	MB_DQS_L5	MB_DATA26	F31	M_B_DQ26
M_B_DQS4	AN30	MB_DQS_H4	MB_DATA25	C32	M_B_DQ25
M_B_DQS#4	AM30	MB_DQS_L4	MB_DATA24	B32	M_B_DQ24
M_B_DQS3	D33	MB_DQS_H3	MB_DATA23	C30	M_B_DQ23
M_B_DQS#3	D32	MB_DQS_L3	MB_DATA22	A29	M_B_DQ22
M_B_DQS2	B28	MB_DQS_H2	MB_DATA21	B26	M_B_DQ21
M_B_DQS#2	A28	MB_DQS_L2	MB_DATA20	A26	M_B_DQ20
M_B_DQS1	A21	MB_DQS_H1	MB_DATA19	B30	M_B_DQ19
M_B_DQS#1	B20	MB_DQS_L1	MB_DATA18	A30	M_B_DQ18
M_B_DQS0	B16	MB_DQS_H0	MB_DATA17	A27	M_B_DQ17
M_B_DQS#0	A15	MB_DQS_L0	MB_DATA16	C26	M_B_DQ16
			MB_DATA15	A24	M_B_DQ15
	AN22	MB_CLK_H7	MB_DATA14	B24	M_B_DQ14
	AM22	MB_CLK_L7	MB_DATA13	C18	M_B_DQ13
	AN21	MB_CLK_H6	MB_DATA12	A18	M_B_DQ12
	AM21	MB_CLK_L6	MB_DATA11	A25	M_B_DQ11
	AA32	MB_CLK_H5	MB_DATA10	C24	M_B_DQ10
18 M_CLK_DDR2	AA33	MB_CLK_L5	MB_DATA9	C20	M_B_DQ9
18 M_CLK_DDR#2	AB33	MB_CLK_H4	MB_DATA8	A19	M_B_DQ8
18 M_CLK_DDR3	AB32	MB_CLK_L4	MB_DATA7	C16	M_B_DQ7
18 M_CLK_DDR#3	AB31	MB_CLK_H3	MB_DATA6	A16	M_B_DQ6
	AB30	MB_CLK_L3	MB_DATA5	B14	M_B_DQ5
	AD31	MB_CLK_H2	MB_DATA4	A13	M_B_DQ4
	AD30	MB_CLK_L2	MB_DATA3	B18	M_B_DQ3
	C22	MB_CLK_H1	MB_DATA2	A17	M_B_DQ2
	B22	MB_CLK_L1	MB_DATA1	C14	M_B_DQ1
	A22	MB_CLK_H0	MB_DATA0	A14	M_B_DQ0
	A23	MB_CLK_L0			
				H33	
18 M_CKE3	N33	MB_CKE1	MB_DM8	AN15	M_B_DM7
18 M_CKE2	P32	MB_CKE0	MB_DM7	AN20	M_B_DM6
			MB_DM6	AK26	M_B_DM5
	AK31	MB1_ODT1	MB_DM5	AN31	M_B_DM4
	AH31	MB1_ODT0	MB_DM4	C33	M_B_DM3
18 M_ODT3	AK32	MB0_ODT1	MB_DM3	C28	M_B_DM2
18 M_ODT2	AH33	MB0_ODT0	MB_DM2	A20	M_B_DM1
			MB_DM1	D14	M_B_DM0
	AK33	MB1_CS_L1	MB_DM0		
	AF33	MB1_CS_L0			
18 M_CS#3	AJ32	MB0_CS_L1			
18 M_CS#2	AF31	MB0_CS_L0			
18 M_B_RAS#	AF32	MB_RAS_L			
18 M_B_CAS#	AH32	MB_CAS_L			
18 M_B_WE#	AG33	MB_WE_L			
18 DDR3_DRAMRST_B#	L32	MB_RESET_L			
17,18 PM_EXTTS#1	M33	FREE|MB_EVENT_L			

GENEVA-GP

SJV10-NL

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

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2D5V
Iomax=0.2A

Place near to CPU
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

Route as 80ohm, diff
R value is TBD

CPU exceeds to 125℃

HDT Connectors

CPU_DBREQ#	TP109
CPU_DBRDY	TP102
CPU_TCK	TP104
CPU_TMS	TP105
CPU_TDI	TP106
CPU_TRST#	TP107
CPU_TDO	TP108

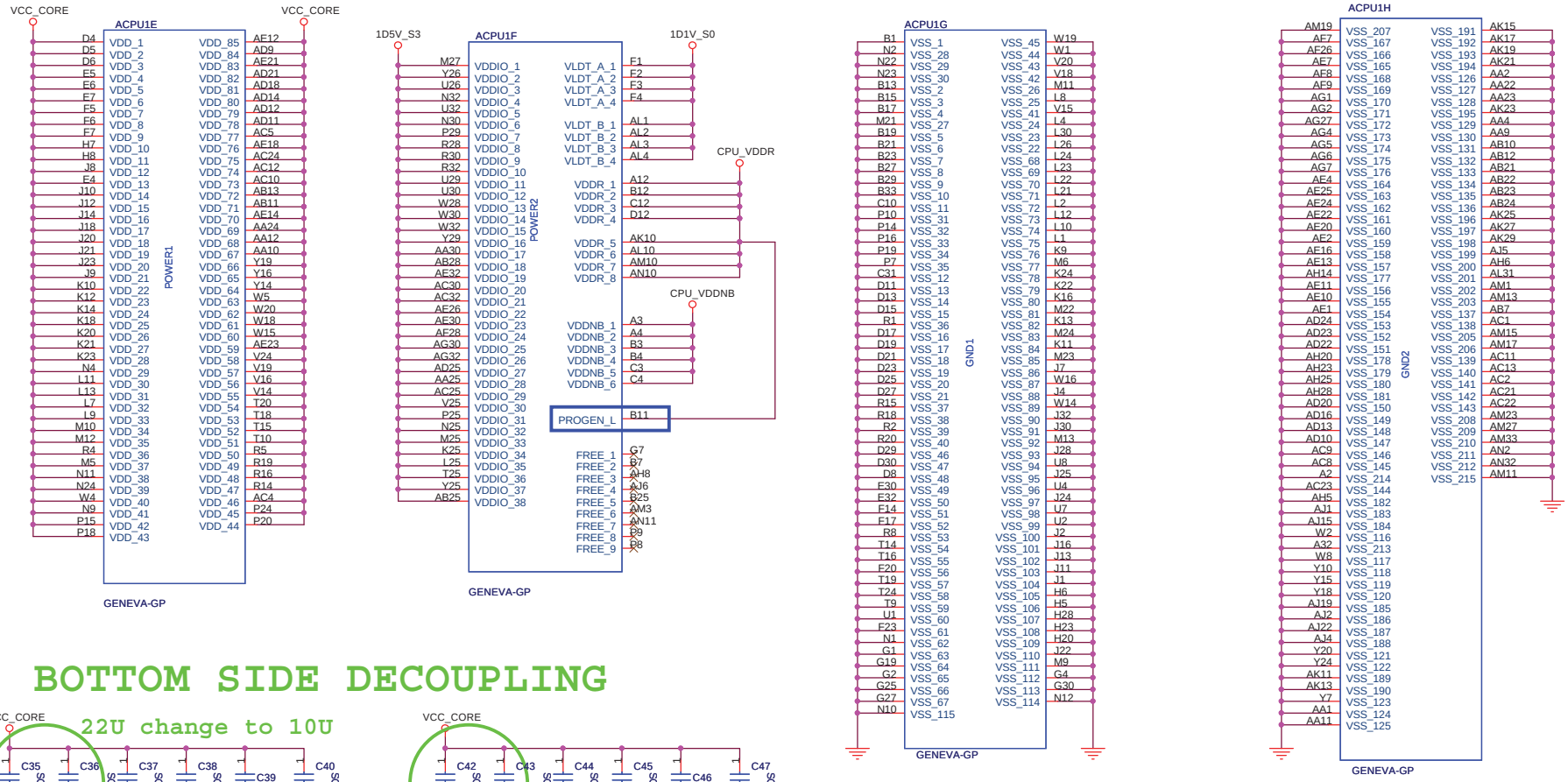
SJV10-NL

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Taipei Hsien 221, Taiwan, R.O.C.

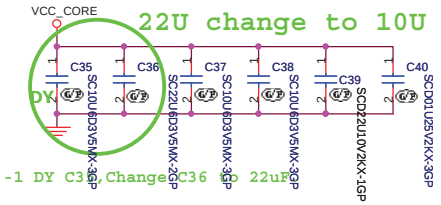
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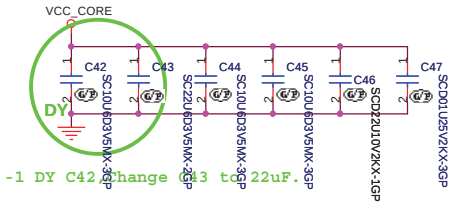
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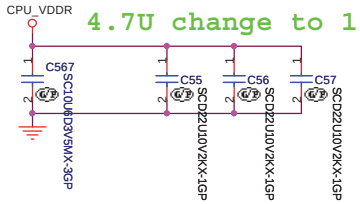
Date: Tuesday, January 26, 2010 | Sheet 6 of 42

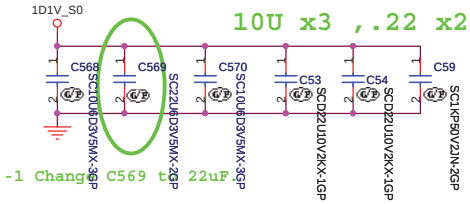


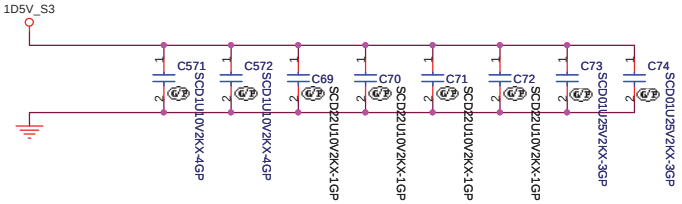
BOTTOM SIDE DECOUPLING



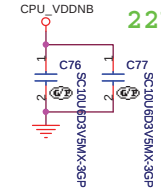


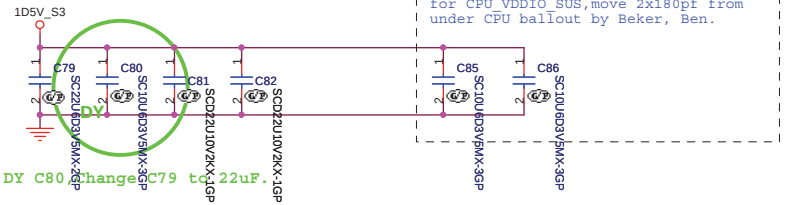






DECOUPLING betweem CPU and DIMMs
PLACE CLOSE TO CPU AS POSSIBLE

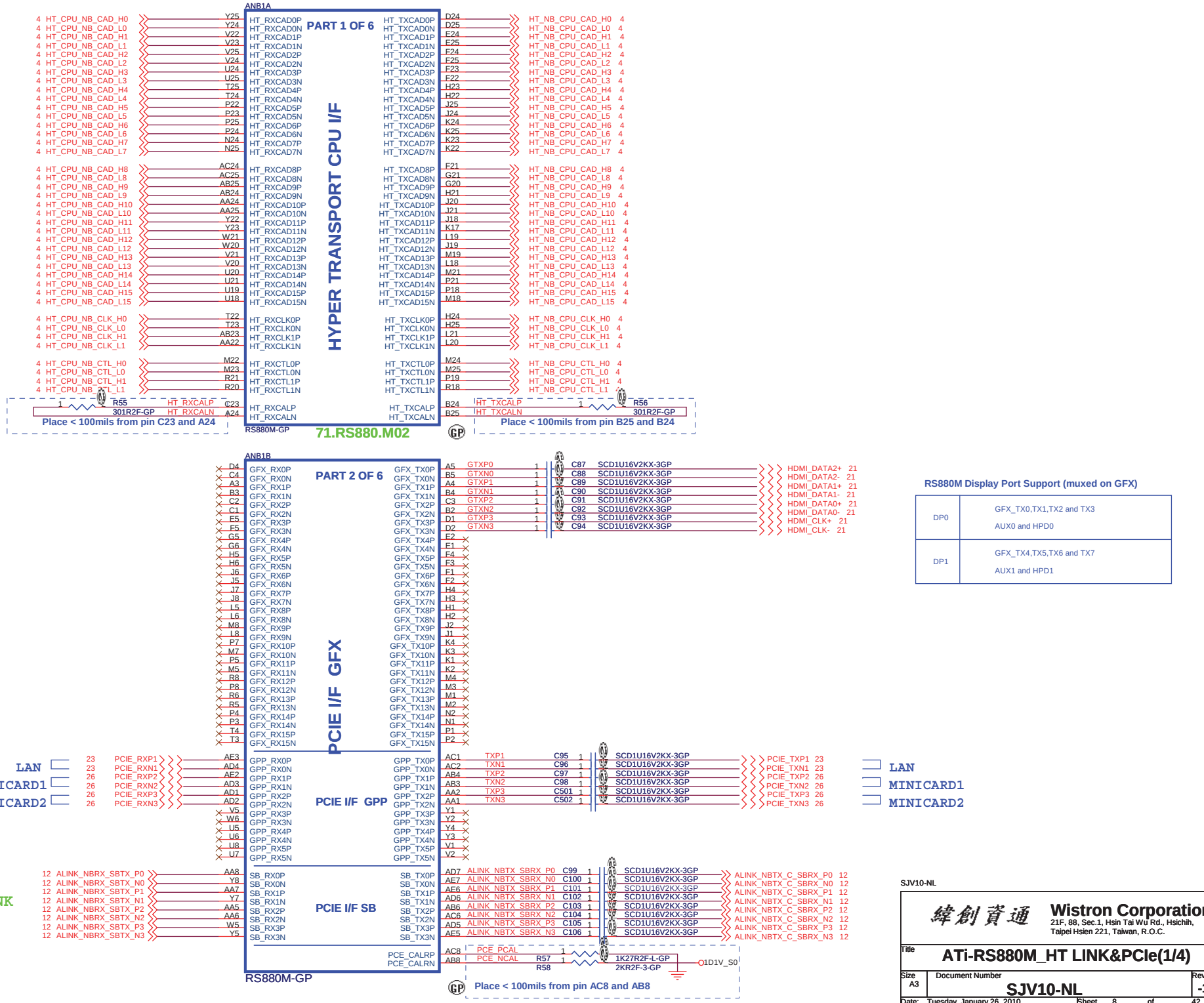


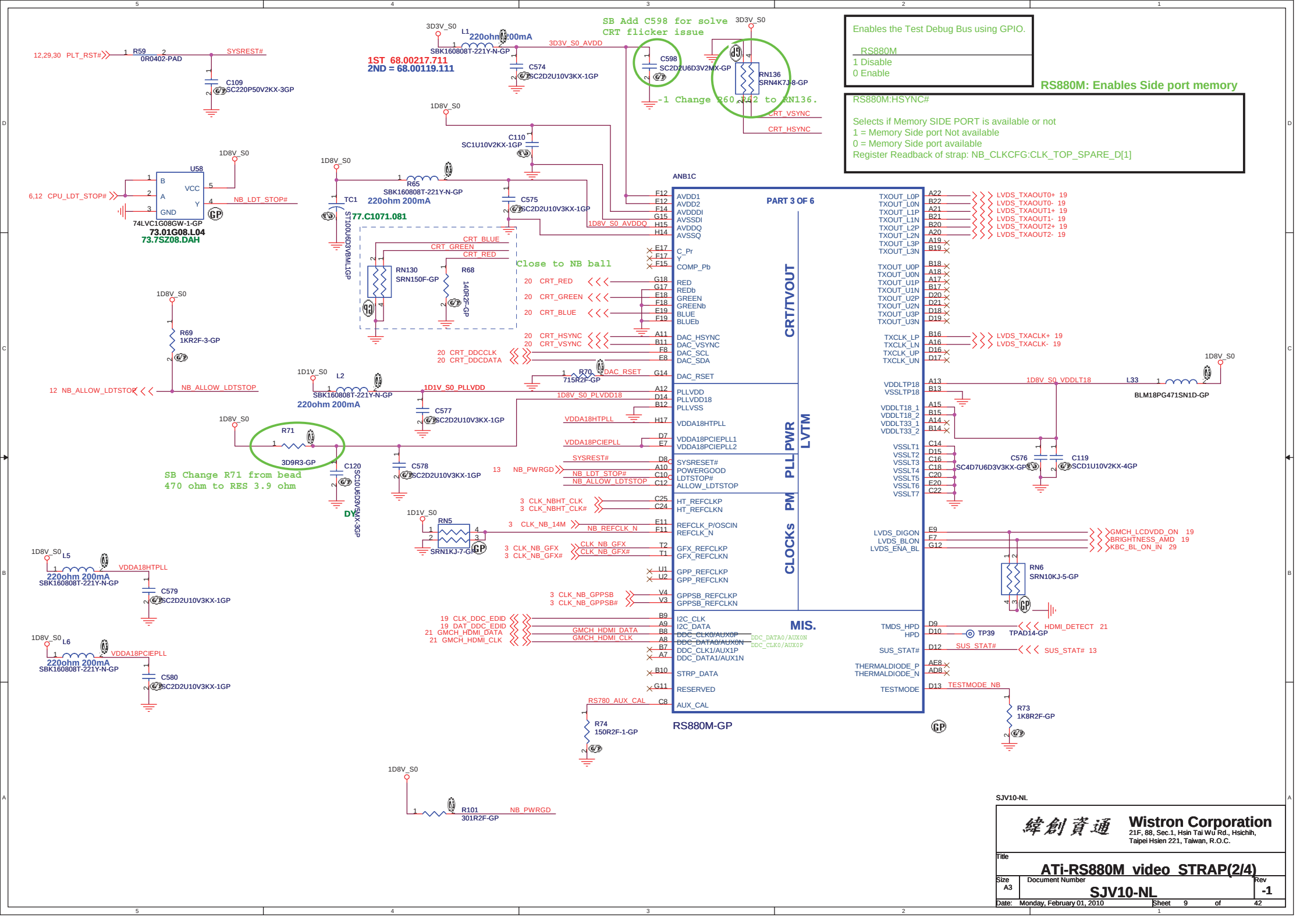


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Title	CPU_Power_(4/4)	
Size A3	Document Number SJV10-NL	Rev -1
Date: Thursday, January 14, 2010	Sheet 7 of 42	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS880M-GP
71.RS880.M02
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS880M-GP
Place < 100mils from pin AC8 and AB8
LAN
MINICARD1
MINICARD2
A-LINK
RS880M Display Port Support (muxed on GFX)
DP0
GFX_TX0,TX1,TX2 and TX3
AUX0 and HPD0
DP1
GFX_TX4,TX5,TX6 and TX7
AUX1 and HPD1
SJV10-NL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/4)
Size A3
Document Number
SJV10-NL
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Date: Tuesday, January 26, 2010
Sheet 8 of 42


SB Add C598 for solve CRT flicker issue
Enables the Test Debug Bus using GPIO.
RS880M
1 Disable
0 Enable
RS880M: Enables Side port memory
RS880M:HSYNC#
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
1ST 68.00217.711
2ND = 68.00119.111
-1 Change R60,R62 to RN136.
Close to NB ball
SB Change R71 from bead 470 ohm to RES 3.9 ohm
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL PWR LVTM
CLOCKs PM
MIS.
RS880M-GP
SJV10-NL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M video STRAP(2/4)
SJV10-NL
Rev -1
Date: Monday, February 01, 2010
Sheet 9 of 42

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

-1 Change R76,R78 to RN138. -1 Change R77,R79 to RN139.

CLOSE TO SDRAM

-1 Change R84,R85 to RN137.

CLOSE TO NB

-1 DY F139 Change C140 to 22uF.

VR.1GB0G.004

2nd = VR.1GB0B.006

3rd = VR.1GB0T.002

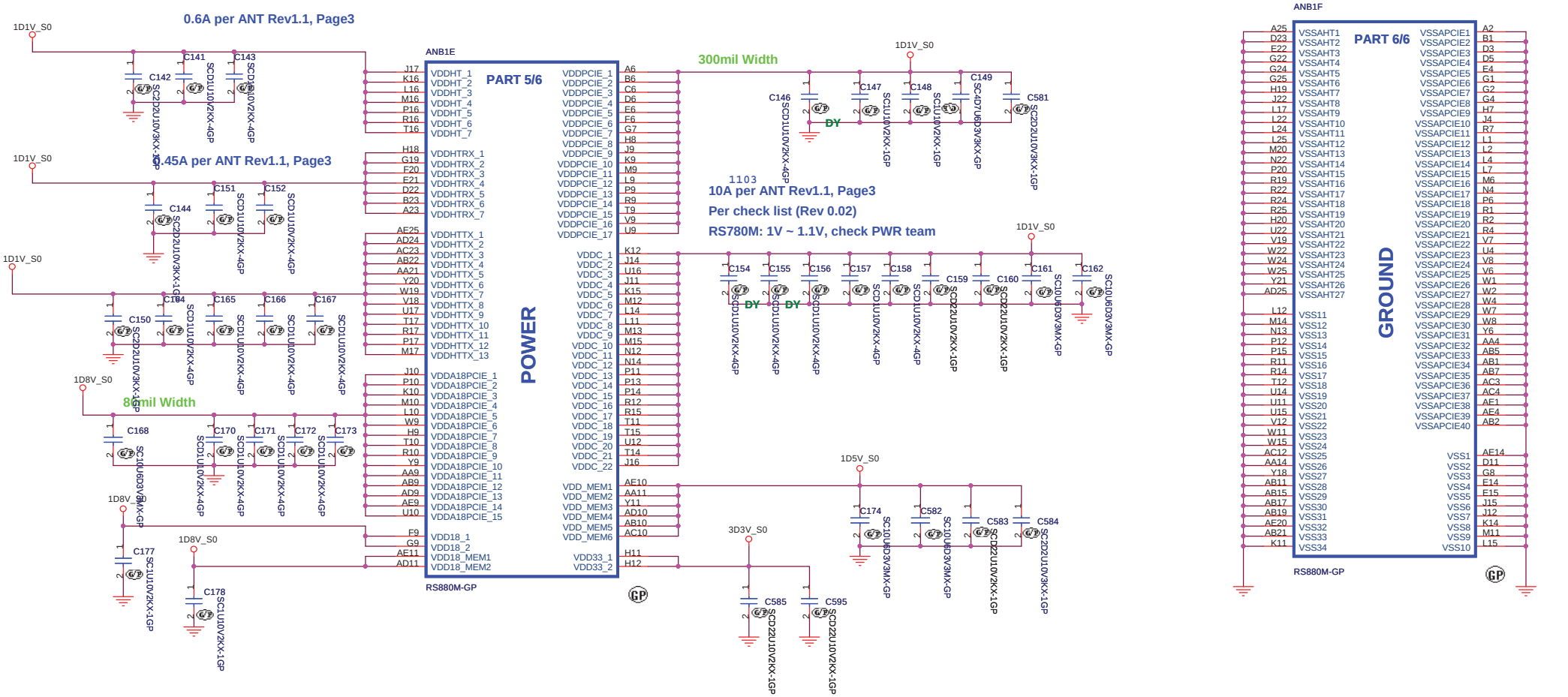
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Title: ATi-RS880M SIDE PORT(3/4)

Size: A3 | Document Number: SJV10-NL | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 10 of 42



SJV10-NL

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **ATi-RS880M PWR&GND(4/4)**		
Size: A3	Document Number: **SJV10-NL**	Rev: **-1**
Date: Tuesday, January 05, 2010	Sheet 11 of 42	

-1 Change R89,R88 to RN140.

SRN33J-5-GP-U
RN140

	HYNIX VR.1GB0G.004	SAMSUNG VR.1GB0B.006	ATI VR.1GB0T.002
VRAM_IDENT1	HIGH	LOW	HIGH
VRAM_IDENT2	LOW	HIGH	HIGH

DEFAULT

ASB1A
Part 1 of 5

PCI CLKS
PCI EXPRESS INTERFACES
LPC INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC

SB820 CSL 25-35:* Note: If PCI interface is not used, then these balls can be used for alternate GPIO/GPO function or left not connected.

-1 Add VRAM identify pins.

GPIO34,35 internal pull high

SB Add RTC charge circuit.

SB Change C189 to 22pF, C190 to 15pF.

-1 Change C189 to 15pF.

SB Change R43 from Dummy to 1M ohm.

-1 Change C193 to 12pF.

SB Add G122.

Place R <100mils form pins T25,T24

SB820M-GP

71.SB820.M03

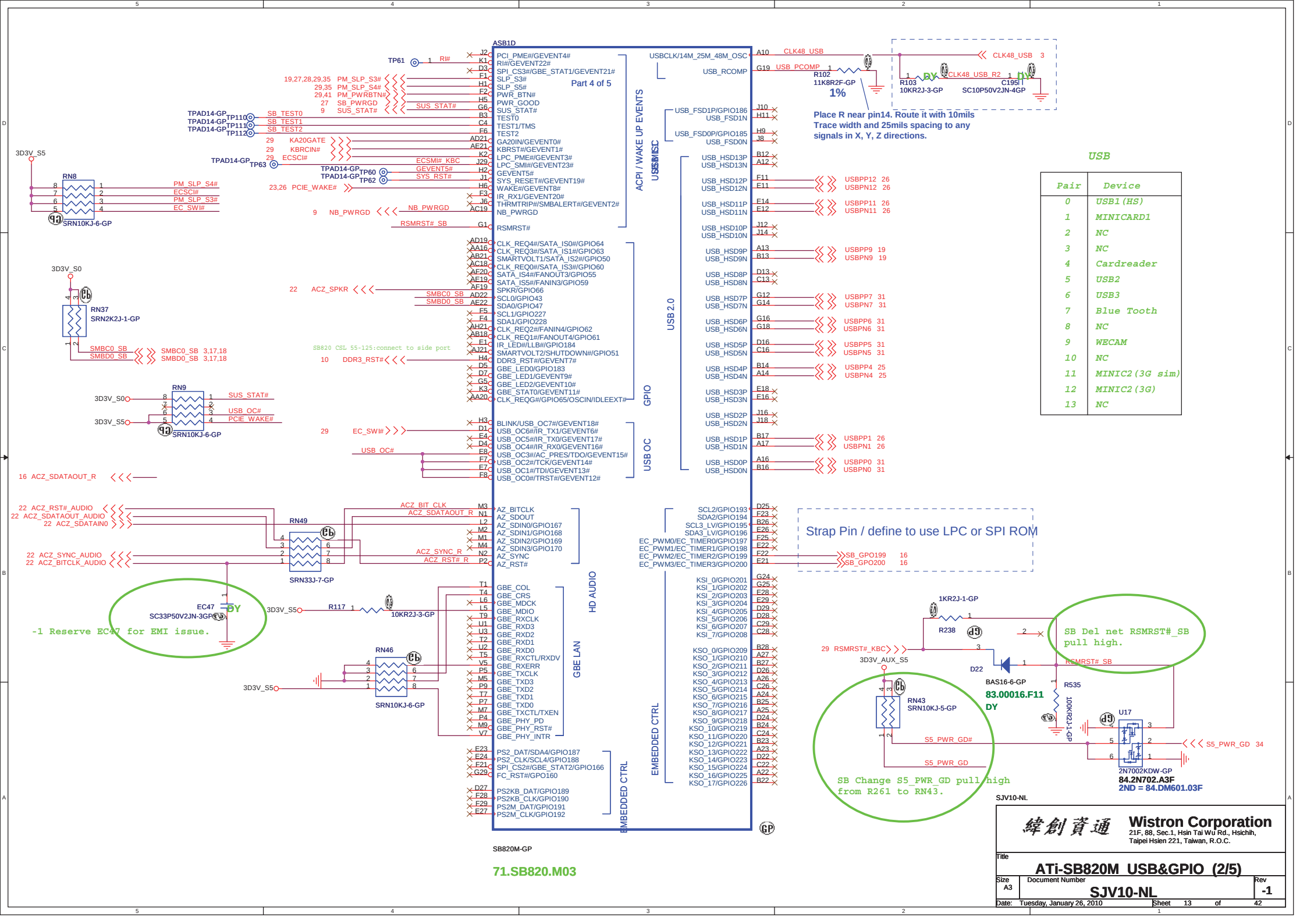
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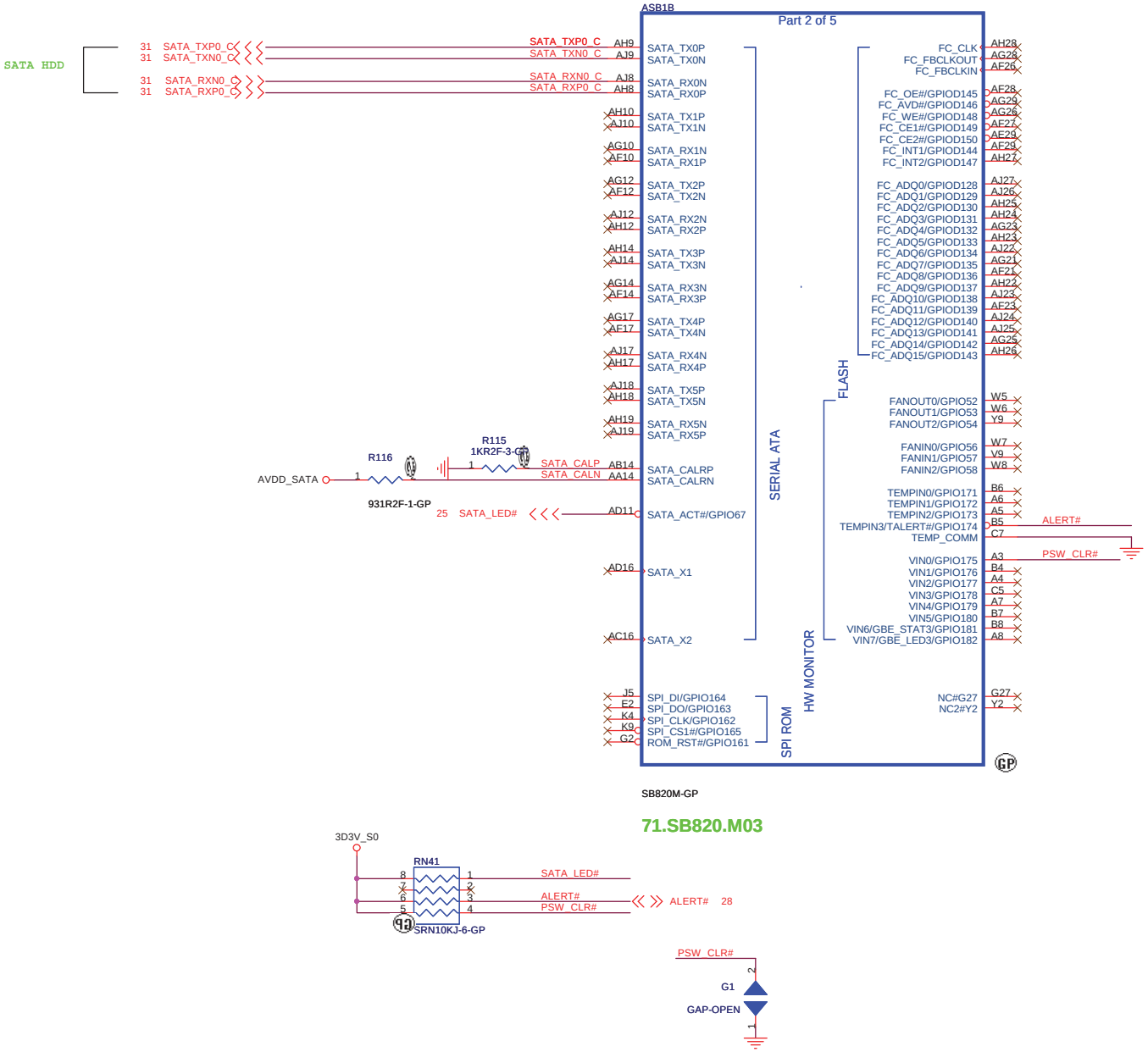
Title: ATi-SB820M PCIE&PCI (1/5)

Size: A3 | Document Number: SJV10-NL | Rev: -1

Date: Monday, February 01, 2010 | Sheet 12 of 42


ASB1D
Part 4 of 5
ACPI / WAKE UP EVENTS
USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
SB820M-GP
71.SB820.M03
TP61
TP110
TP111
TP112
TP63
TP60
TP62
RN8
SRN10KJ-6-GP
RN37
SRN2K2J-1-GP
RN9
SRN10KJ-6-GP
RN49
SRN33J-7-GP
RN46
SRN10KJ-6-GP
EC47
SC33P50V2JN-3GP
-1 Reserve EC47 for EMI issue.
R102
11K8R2F-GP
1%
R103
10KR2J-3-GP
C195
SC10P50V2JN-4GP
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
R117
10KR2J-3-GP
SB820 CSL 55-125:connect to side port
Strap Pin / define to use LPC or SPI ROM
SB_GPO199 16
SB_GPO200 16
1KR2J-1-GP
R238
D22
BAS16-6-GP
83.00016.F11
DY
R535
100KR2J-1-GP
RN43
SRN10KJ-5-GP
U17
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
SB Del net RSMRST#_SB
pull high.
SB Change S5_PWR_GD pull high
from R261 to RN43.
USB
Pair | Device
0 | USB1(HS)
1 | MINICARD1
2 | NC
3 | NC
4 | Cardreader
5 | USB2
6 | USB3
7 | Blue Tooth
8 | NC
9 | WECAM
10 | NC
11 | MINIC2(3G sim)
12 | MINIC2(3G)
13 | NC
SJV10-NL
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB820M USB&GPIO (2/5)
Size A3
Document Number SJV10-NL
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Sheet 13 of 42

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710



71.SB820.M03

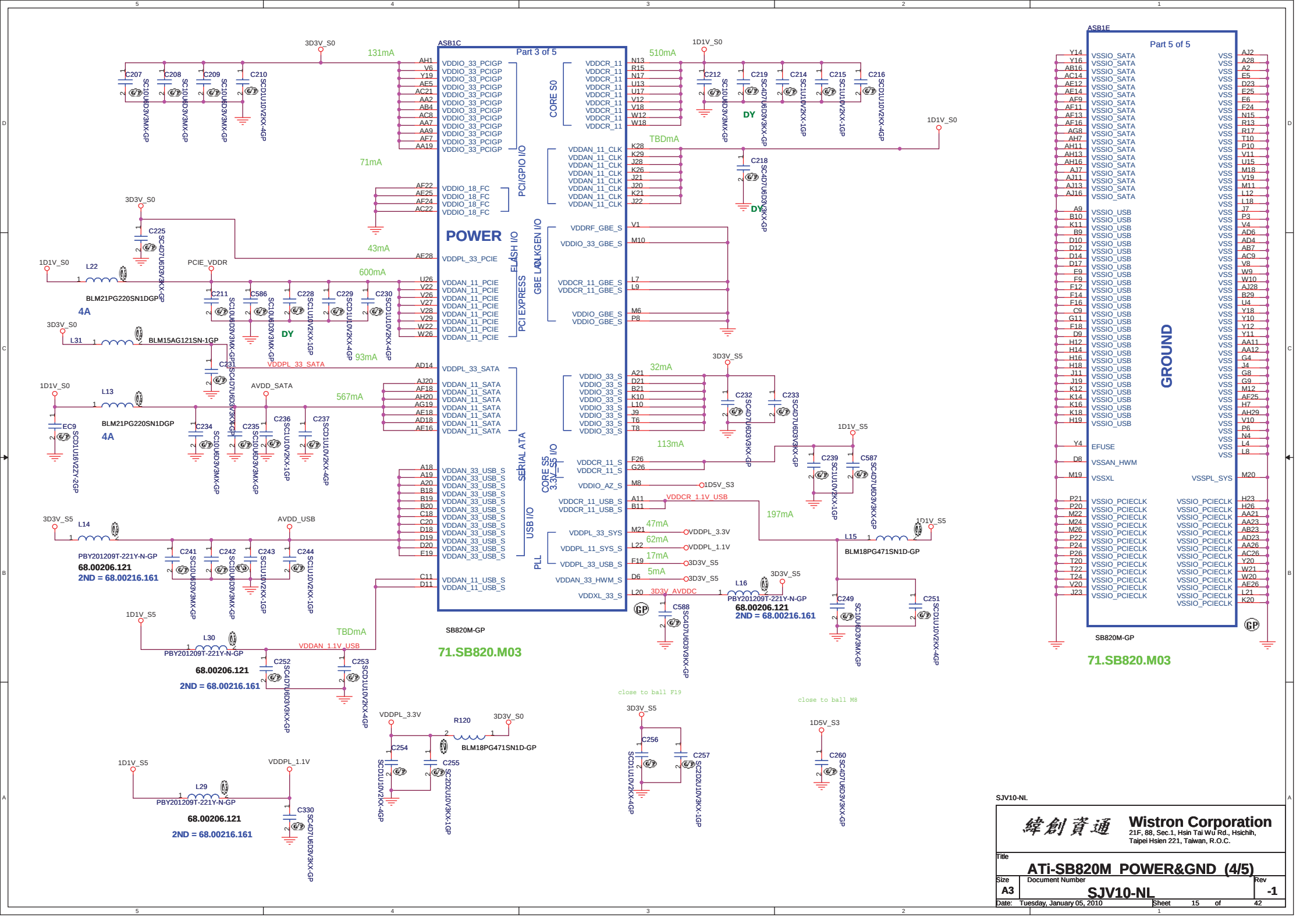
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Title: **ATi-SB820M SATA-FC (3/5)**

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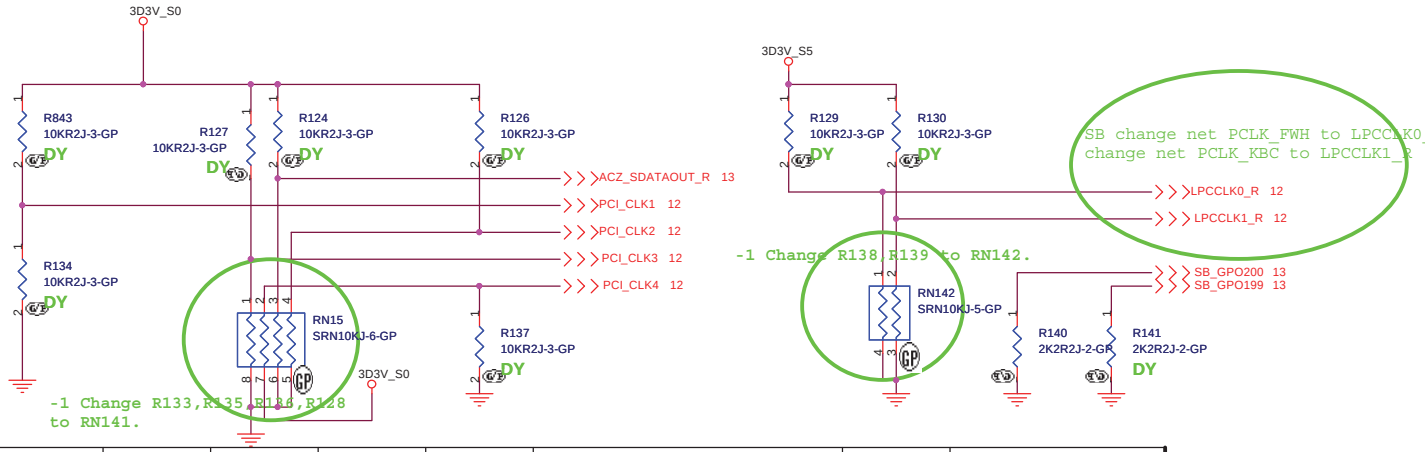
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Title: ATi-SB820M POWER&GND (4/5)

Size	Document Number	Rev
A3	SJV10-NL	-1

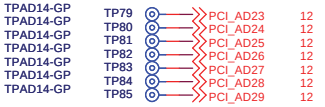
Date: Tuesday, January 05, 2010 Sheet 15 of 42



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

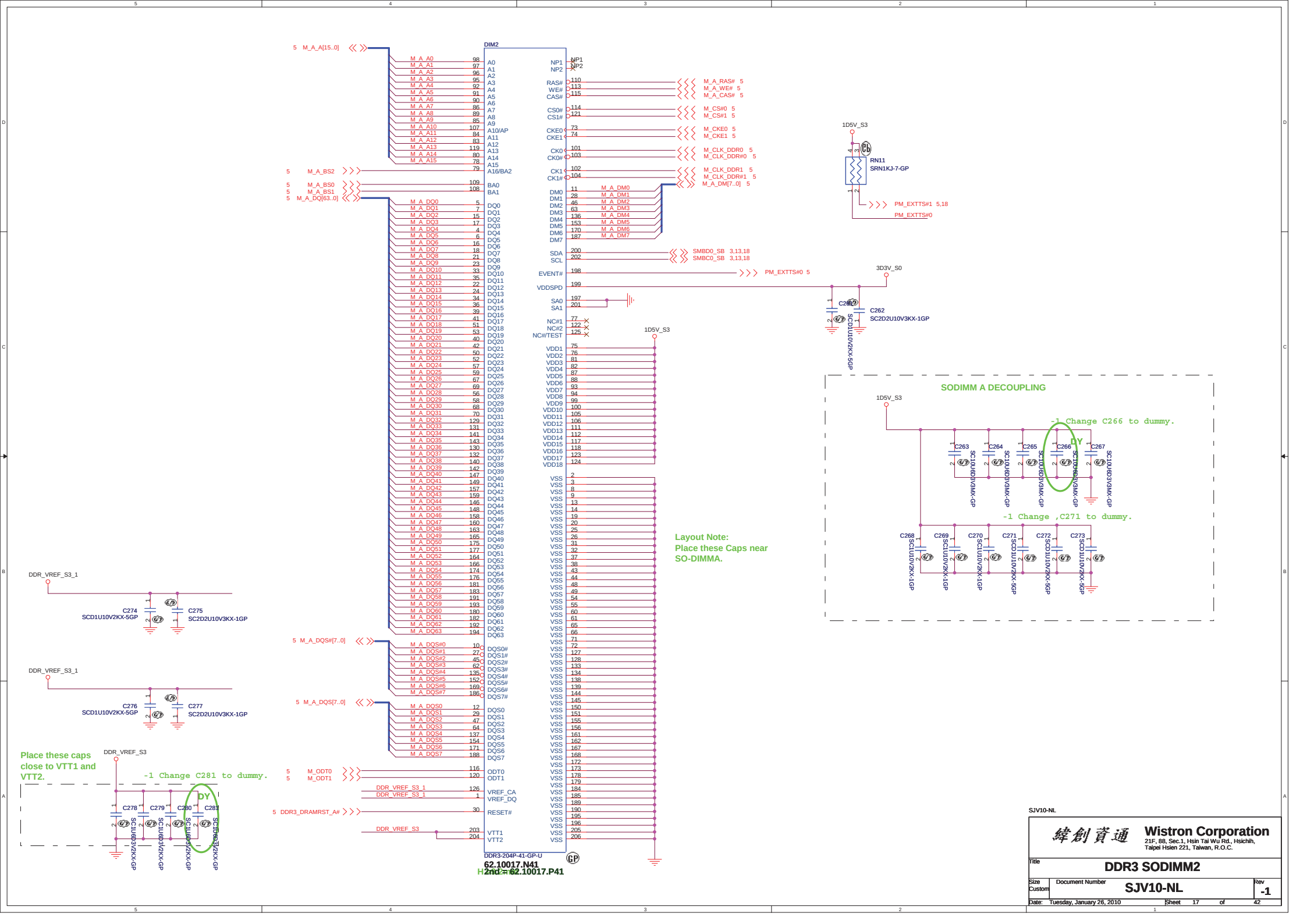
SJV10-NL

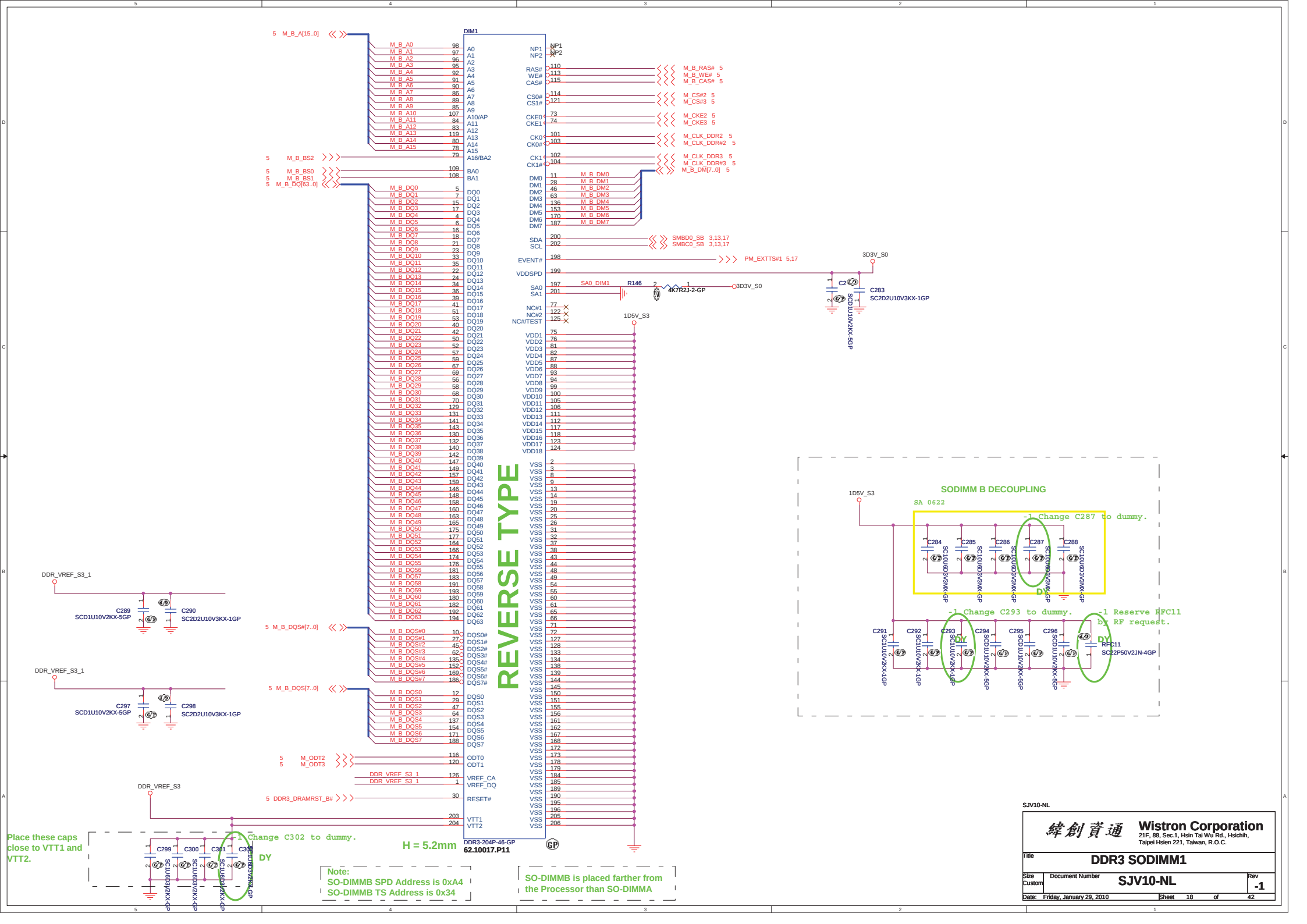
緯創資通 Wistron Corporation
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Title: ATi-SB820M STRAPPING (5/5)

Size: A3 | Document Number: SJV10-NL | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 16 of 42

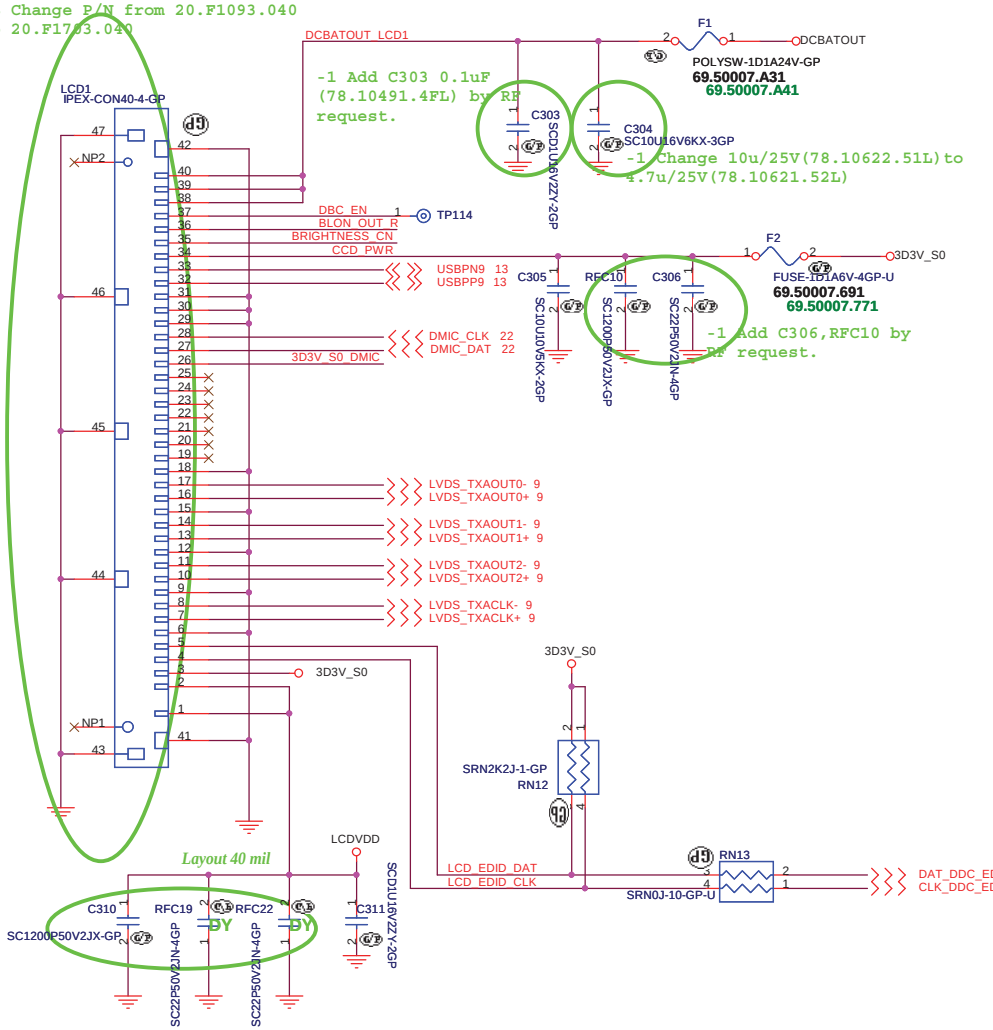

DIM2
DDR3-204P-41-GP-U
62.10017.N41
2nd = 62.10017.P41
SODIMM A DECOUPLING
-1 Change C266 to dummy.
-1 Change ,C271 to dummy.
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
-1 Change C281 to dummy.
RN11
SRN1KJ-7-GP
C262
SC2D2U10V3KX-1GP
C274
SCD1U10V2KX-5GP
C275
SC2D2U10V3KX-1GP
C276
SCD1U10V2KX-5GP
C277
SC2D2U10V3KX-1GP
1D5V_S3
3D3V_S0
DDR_VREF_S3_1
DDR_VREF_S3
PM_EXTTS#1 5,18
PM_EXTTS#0
SMBD0_SB 3,13,18
SMBC0_SB 3,13,18
M_A_RAS# 5
M_A_WE# 5
M_A_CAS# 5
M_CS#0 5
M_CS#1 5
M_CKE0 5
M_CKE1 5
M_CLK_DDR0 5
M_CLK_DDR#0 5
M_CLK_DDR1 5
M_CLK_DDR#1 5
M_A_DM[7..0] 5
M_ODT0
M_ODT1
DDR3_DRAMRST_A#
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR3 SODIMM2
SJV10-NL
-1
Tuesday, January 26, 2010
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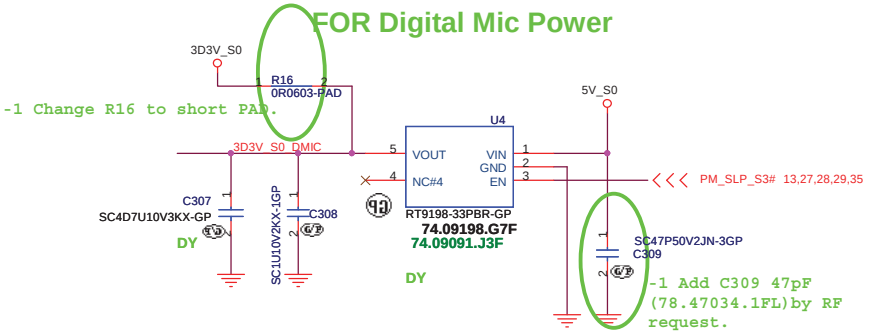

DIM1
REVERSE TYPE
DDR3-204P-46-GP
62.10017.P11
SODIMM B DECOUPLING
SA 0622
-1 Change C287 to dummy.
-1 Change C293 to dummy.
-1 Reserve RFC11 by RF request.
-1 Change C302 to dummy.
Place these caps close to VTT1 and VTT2.
H = 5.2mm
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR3 SODIMM1
SJV10-NL
-1
Friday, January 29, 2010
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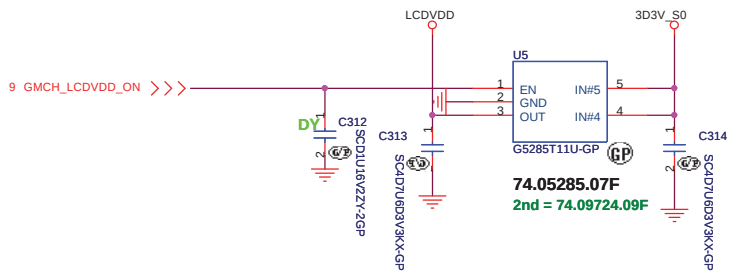
SB Change P/N from 20.F1093.040
to 20.F1703.040

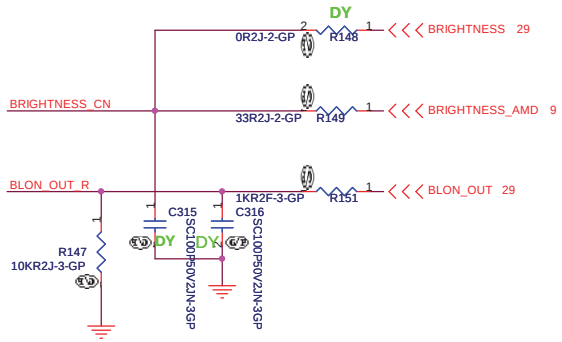
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	NC

D MIC Pin	
Pin	Symbol
1	DMIC_DAT
2	3D3V_S0_DMIC
3	DMIC_CLK
4	GND









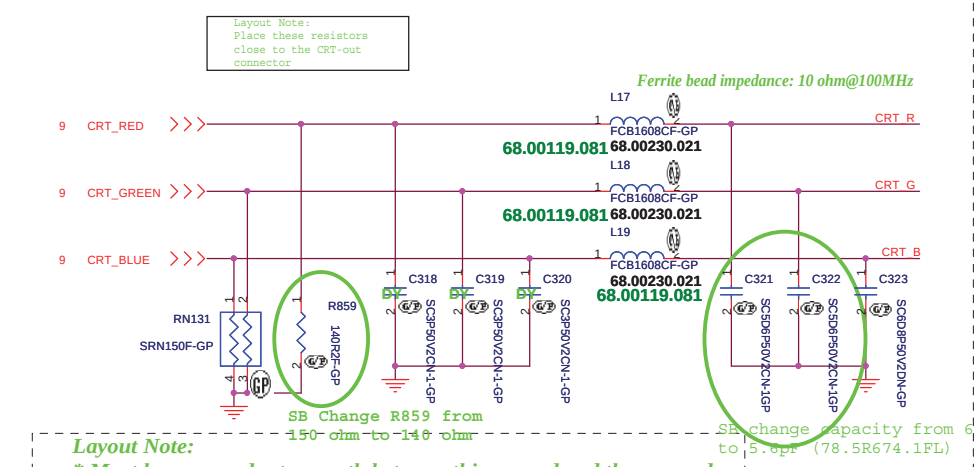
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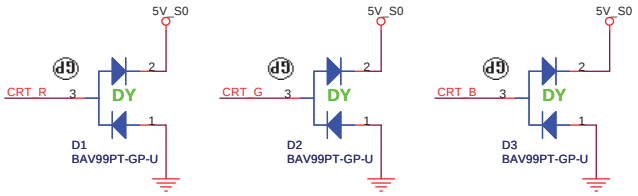
Title: **LCD Conn**

Size	Document Number	Rev
A3	SJV10-NL	-1

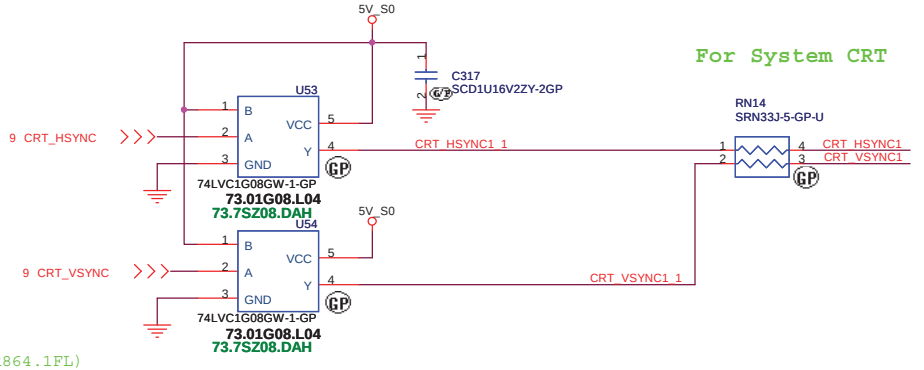
Date: Sunday, January 31, 2010 Sheet 19 of 42



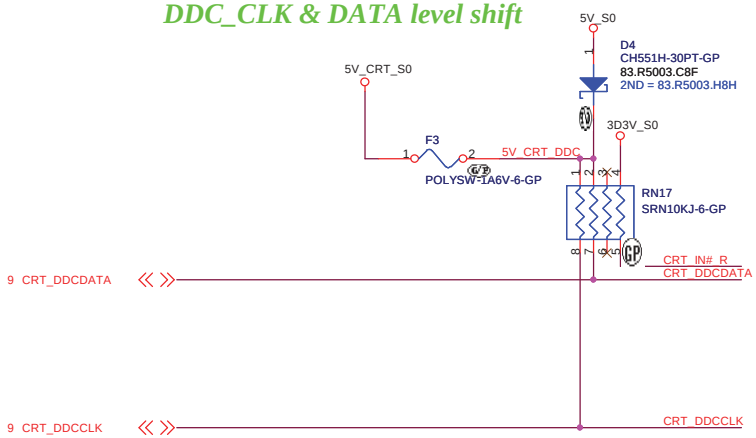
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



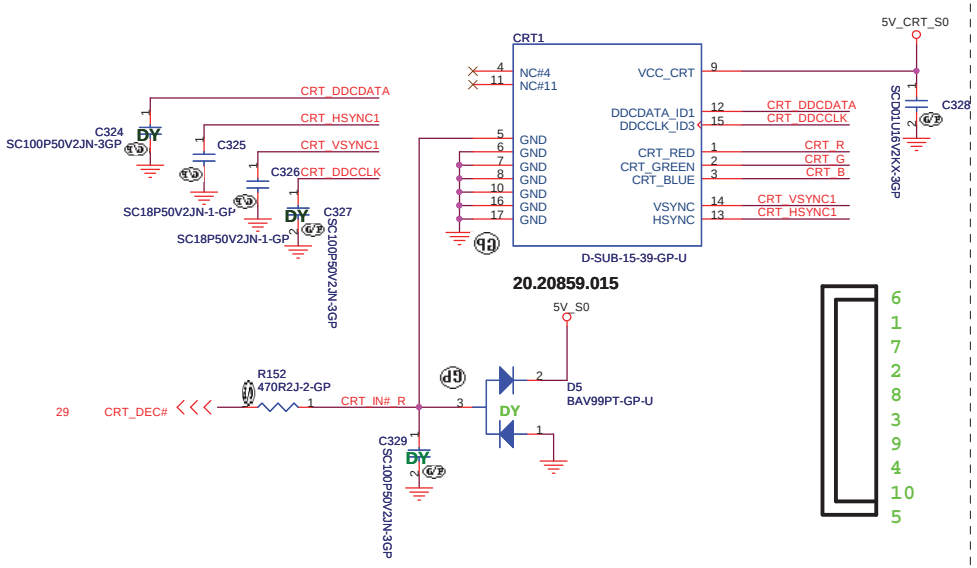
Hsync & Vsync level shift



DDC_CLK & DATA level shift



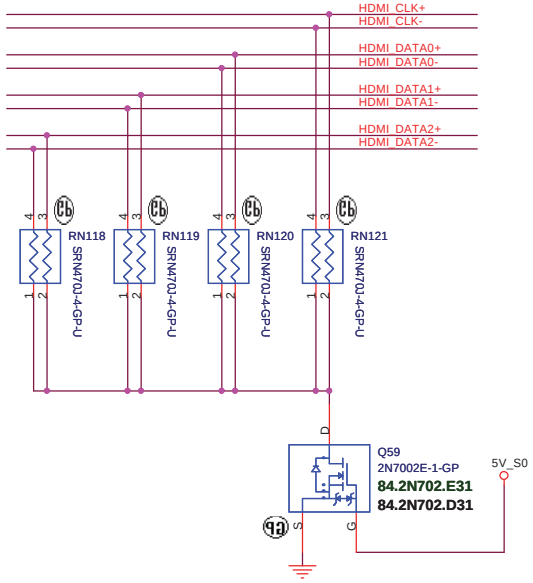
CRT I/F & CONNECTOR



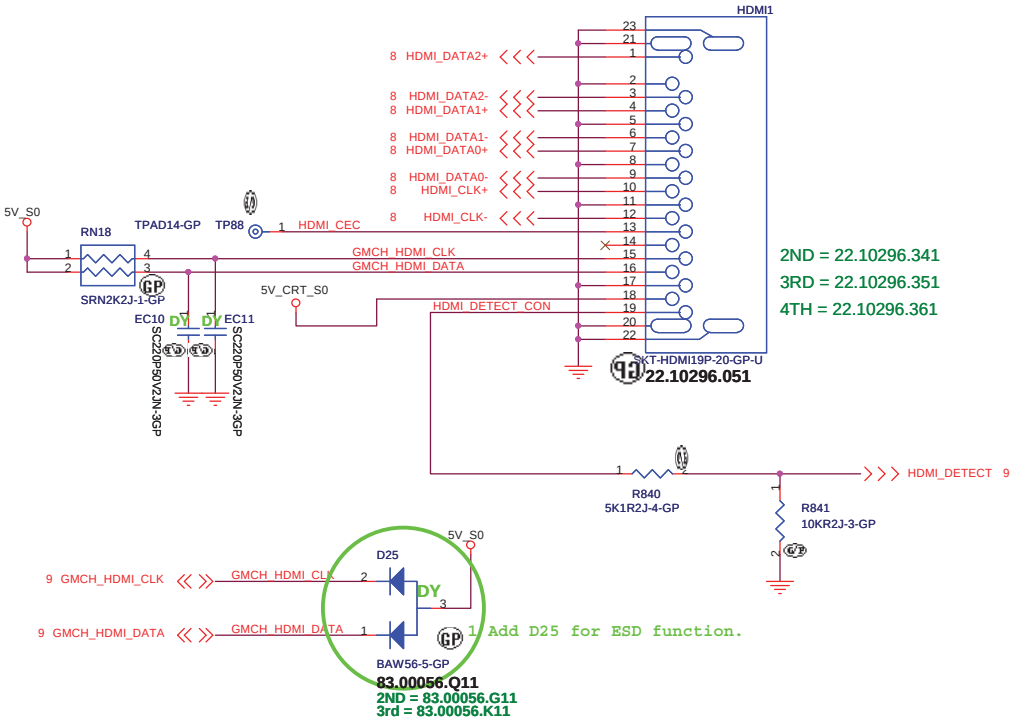
SJV10-NL

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT conn		
Size: A3	Document Number: SJV10-NL	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 20 of 42	



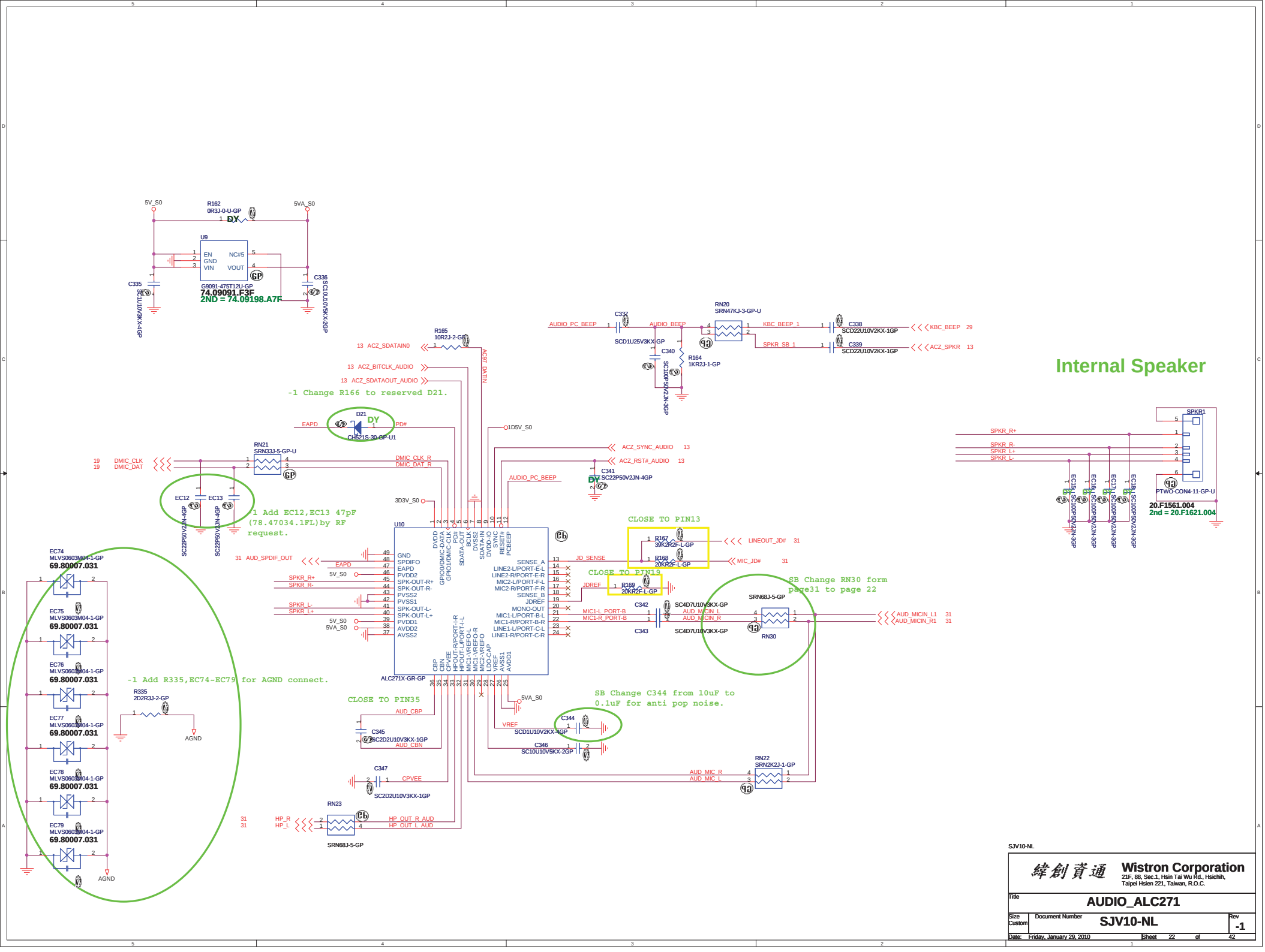
HDMI CONNECTOR



SJV10-NL

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI conn	
Size A3	Document Number SJV10-NL	Rev -1
Date: Tuesday, February 02, 2010	Sheet 21 of 42	



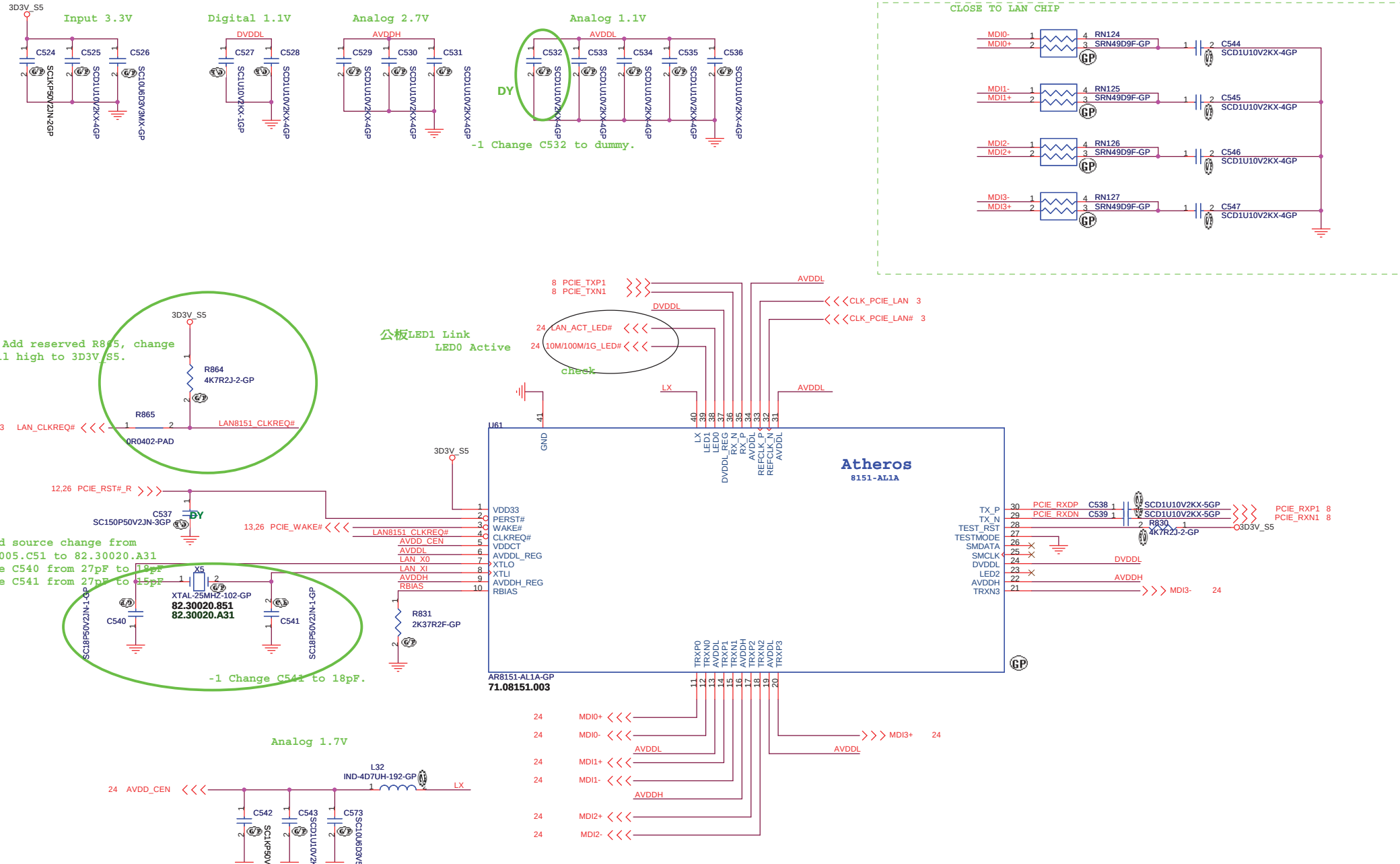
SJV10-NL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO_ALC271

Size: Custom | Document Number: SJV10-NL | Rev: -1

Date: Friday, January 29, 2010 | Sheet 22 of 42



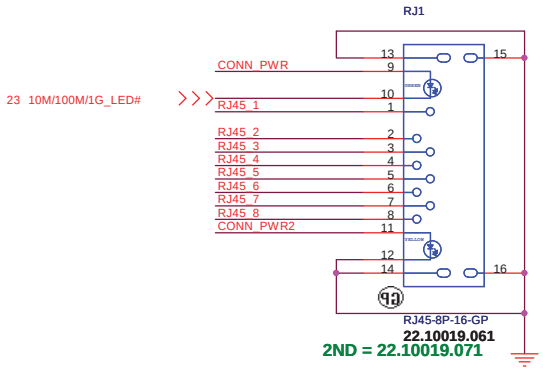
SJV10-NL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN AR8151	
Size A3	Document Number SJV10-NL	Rev -1
Date: Tuesday, January 26, 2010	Sheet 23 of 42	

LAN Connector

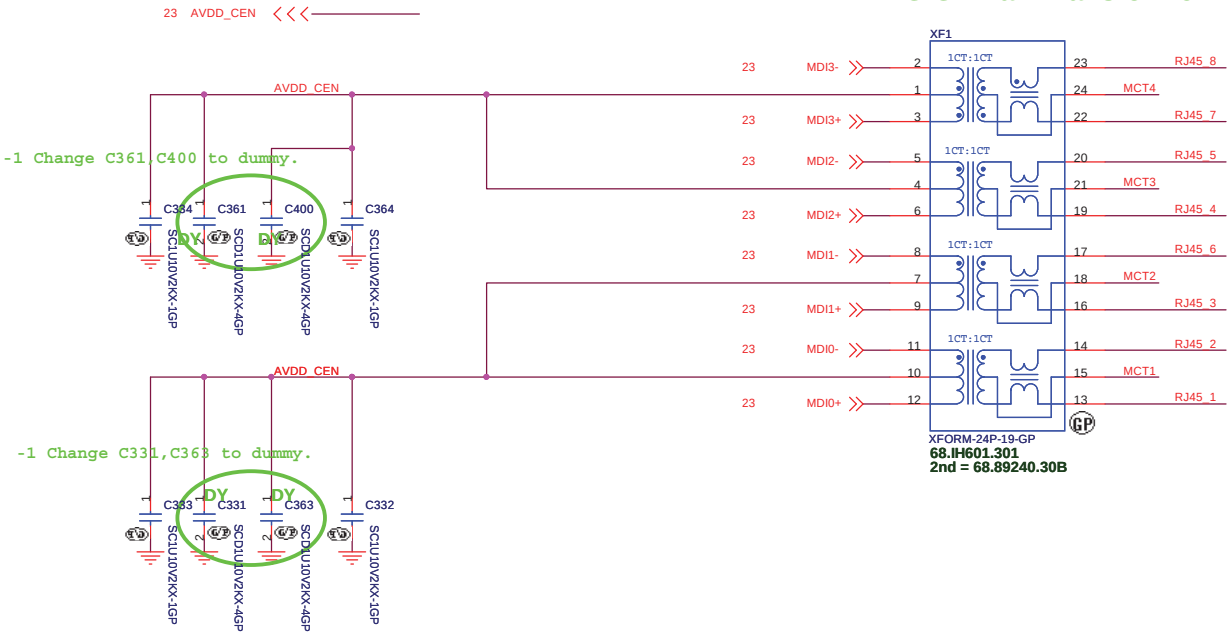
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

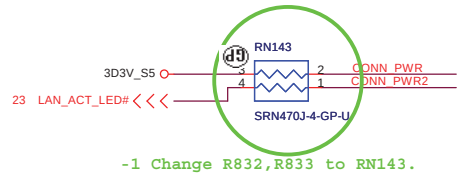


LED COLOR
B1(+) B2(-)::GREEN

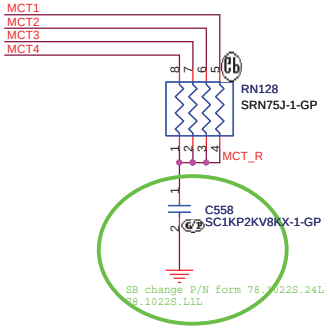
A1(+) A2(-):YELLOW
Green(A3), behavior is the same for 10/100/1000 bits
Yellow(B2), when LAN is transfering data.

Change 單顆
GIGA Lan Transformer

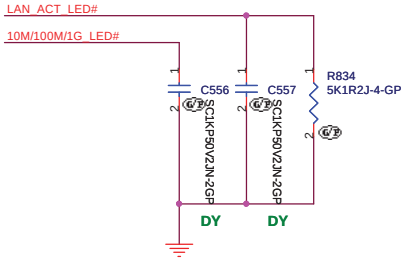




-1 Change R832,R833 to RN143.



SB change P/N form 78.1022S.24L to 78.1022S.L1L



SJV10-NL

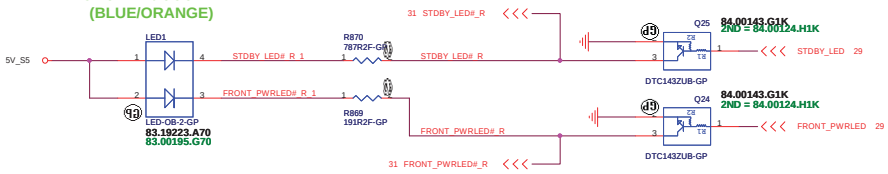
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
Size A3	Document Number SJV10-NL	Rev -1
Date: Tuesday, January 26, 2010	Sheet 24 of 42	

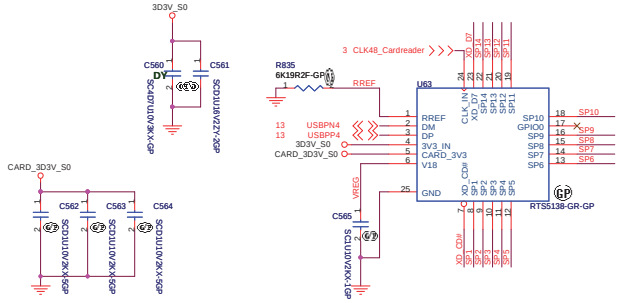
Conn<----------KBC

SYSTEM LED
(BLUE/ORANGE)

Power Button LED
(BLUE/ORANGE)



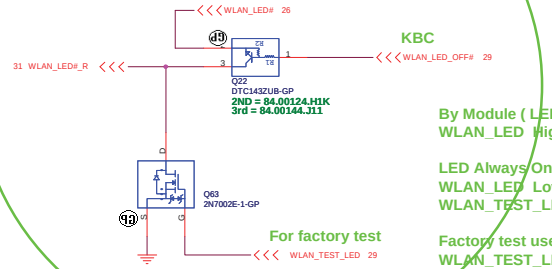
5 IN1 CARD-READER



C51,C52,C53 near CARD1 pin23, Pin14, Pin33

SB Change LED portion connection

from module

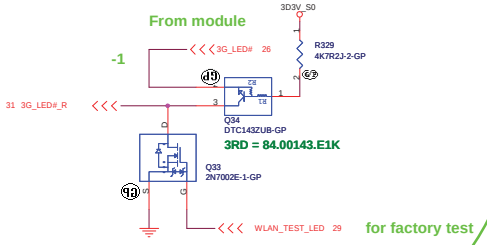


By Module (LED Flash)
WLAN_LED High

LED Always On
WLAN_LED Low
WLAN_TEST_LED High

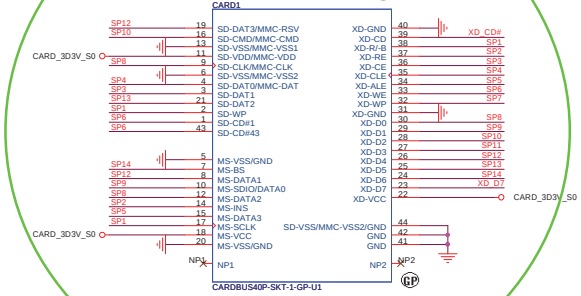
Factory test use
WLAN_TEST_LED High

-1 Change 3G LED portion circuit



SB change P/N to 20.I0087.011

-1 change Card1 P/N to 62.10024.B41

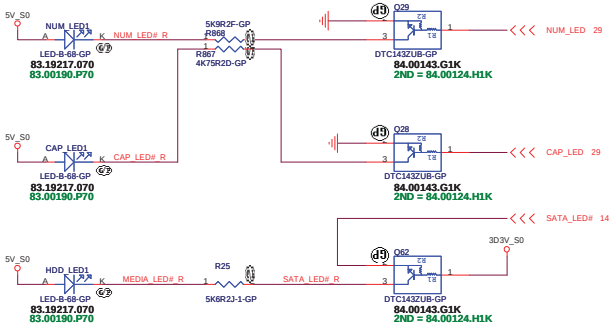


LED Function

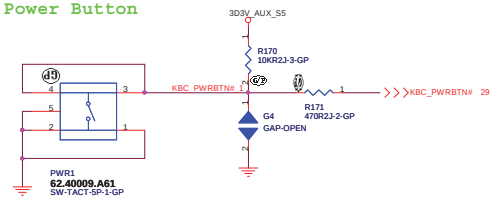
NUM LED
(BLUE)

CAP LED
(BLUE)

HDD LED
(BLUE)



Power Button

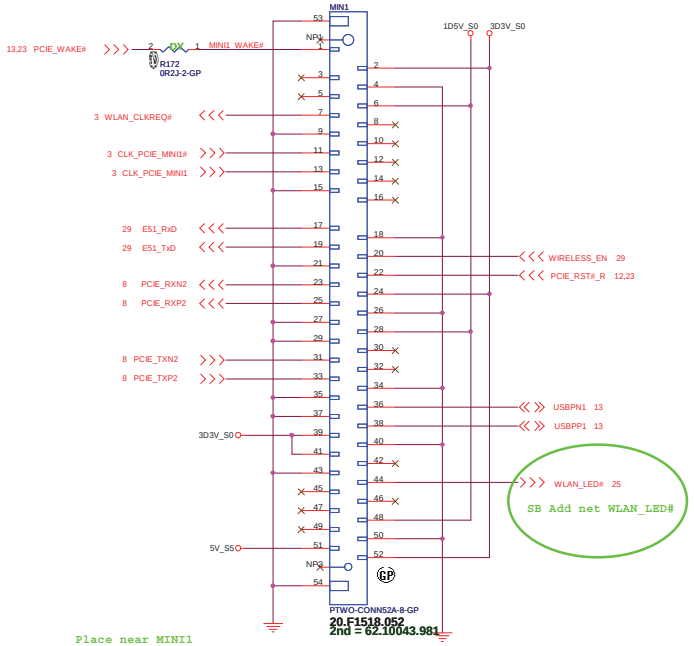


SJV10-NL

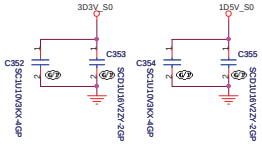
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED_CARD reader		
Size: A2	Document Number: SJV10-NL	Rev: -1
Date: Monday, February 01, 2010	Sheet 25 of 42	

Mini Card Connector(WLAN)

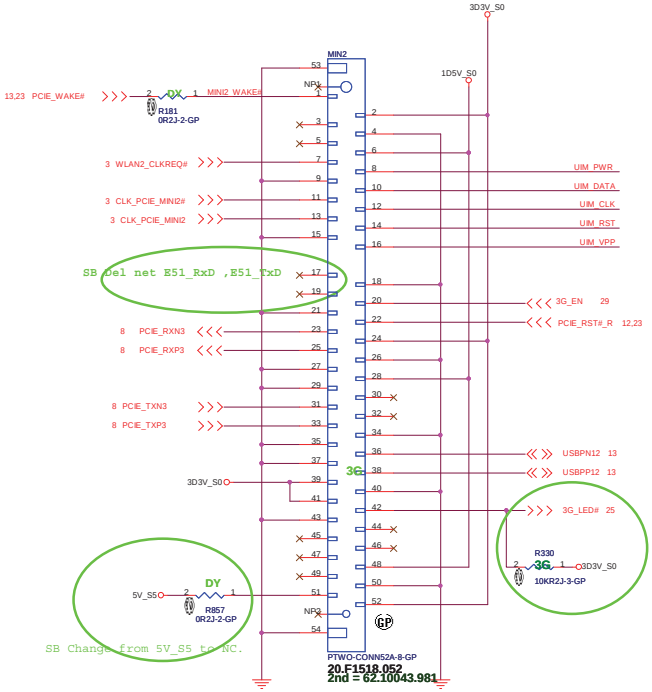
Support debug-card



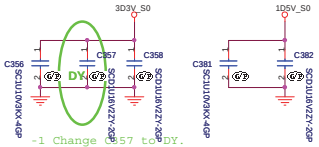
Place near MINI1



Mini Card Connector(3G)

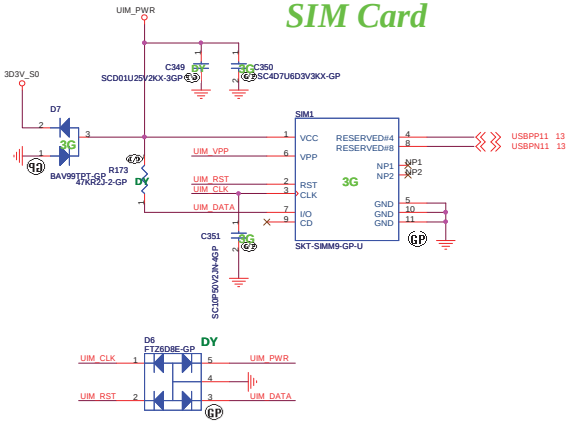


Place near MINIC2



-1 Change C357 to DY.

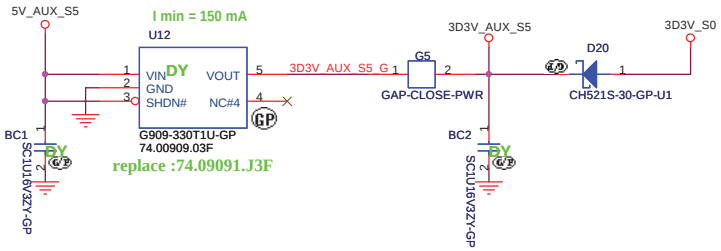
SIM Card



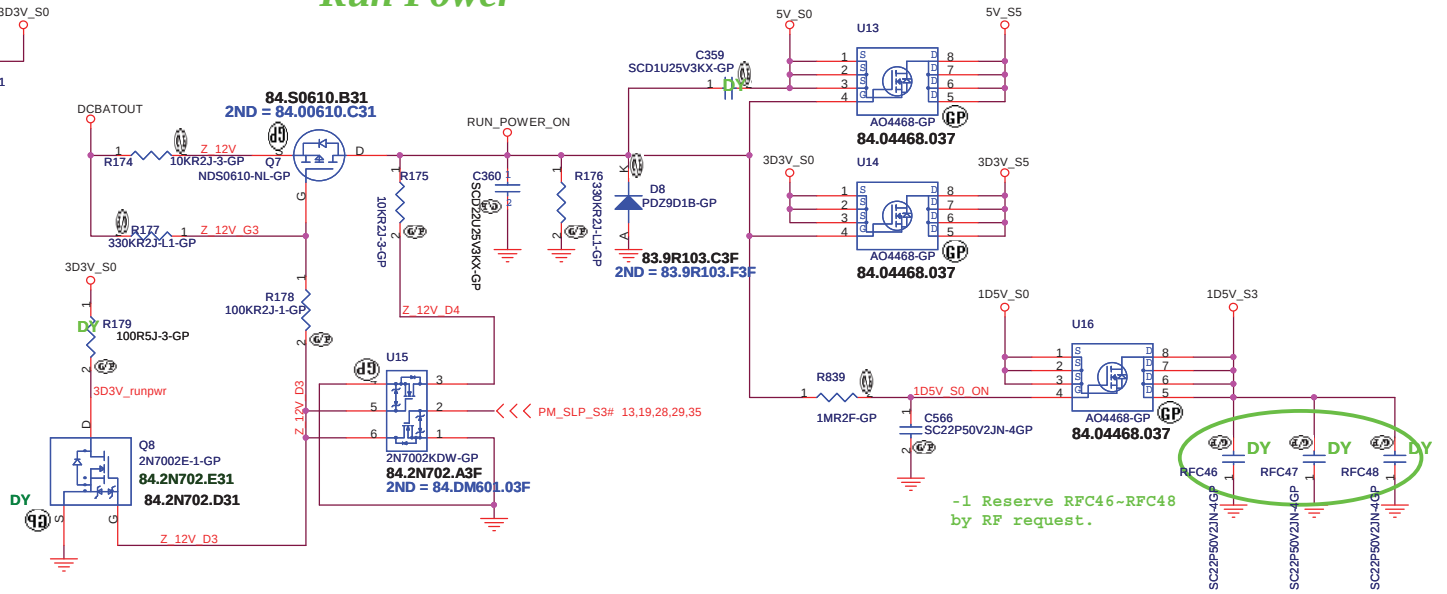
SJV10-NL

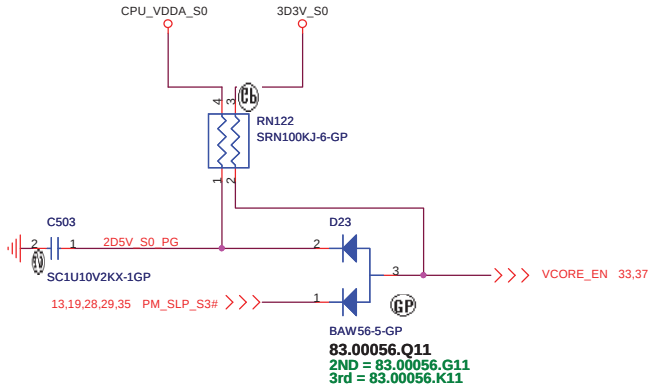
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI Conn		
Size: Custom	Document Number: SJV10-NL	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 26 of 42	

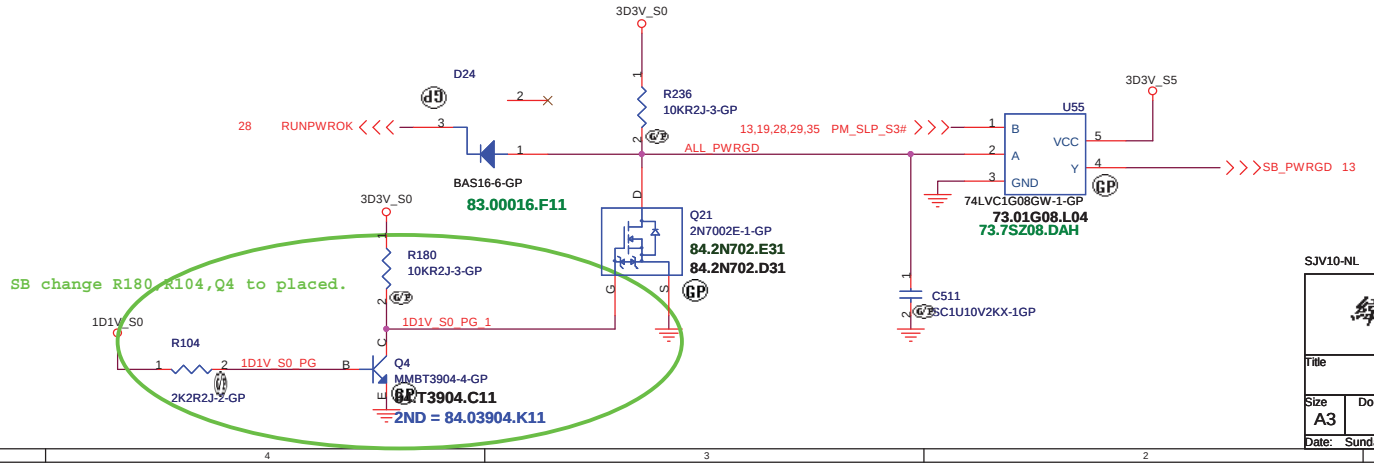
Aux Power 3D3V_AUX_S5



Run Power







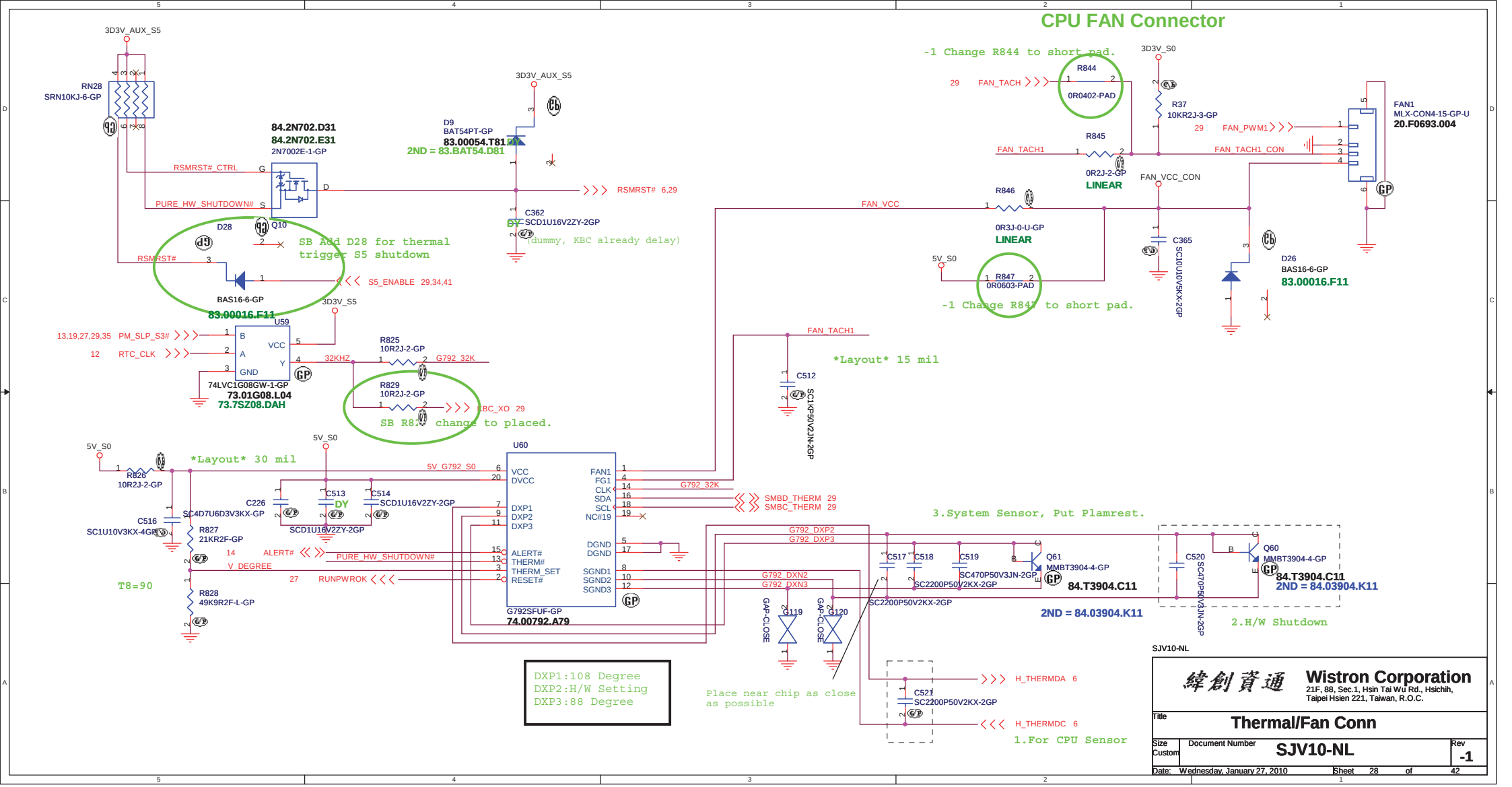
SJV10-NL

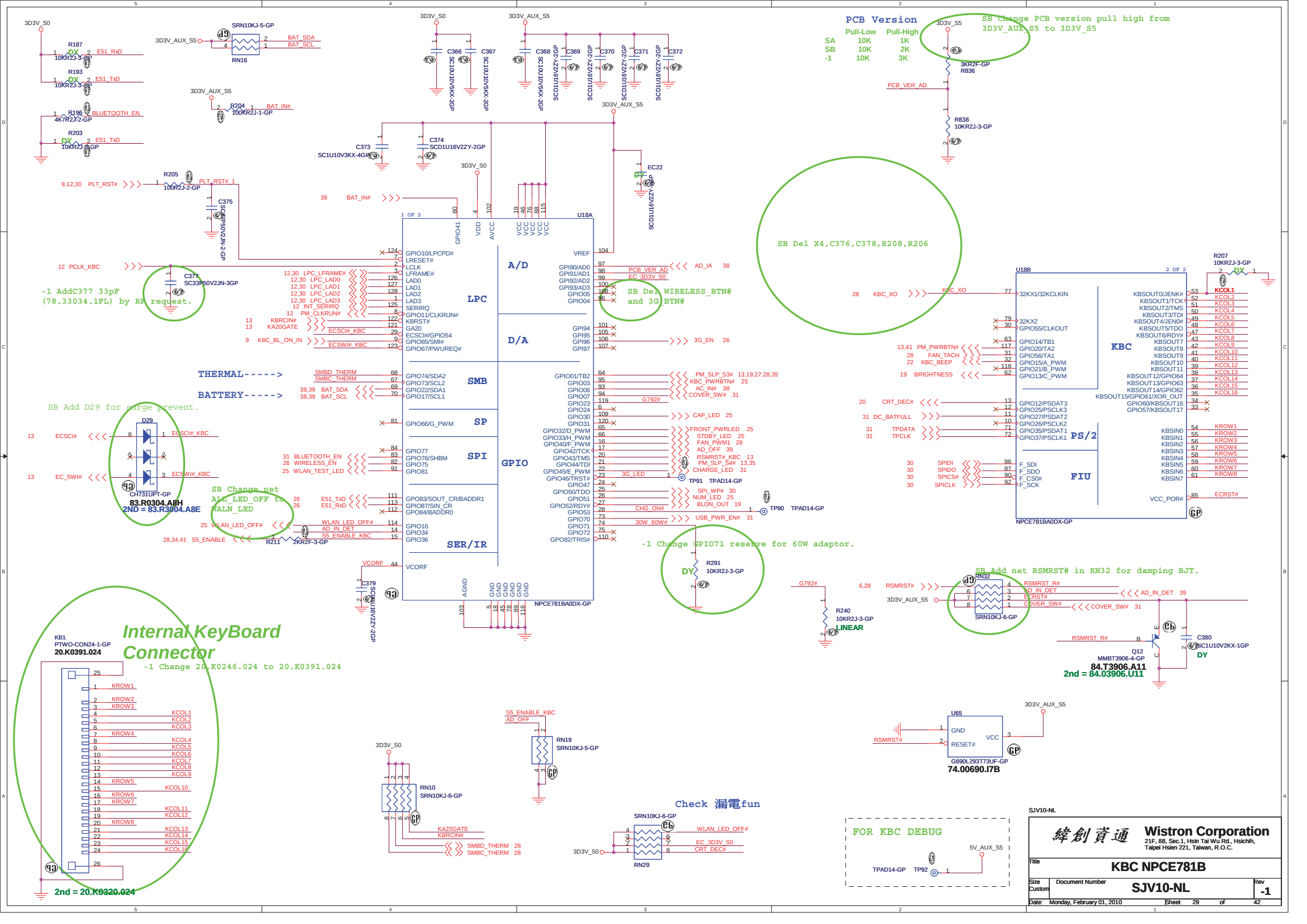
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

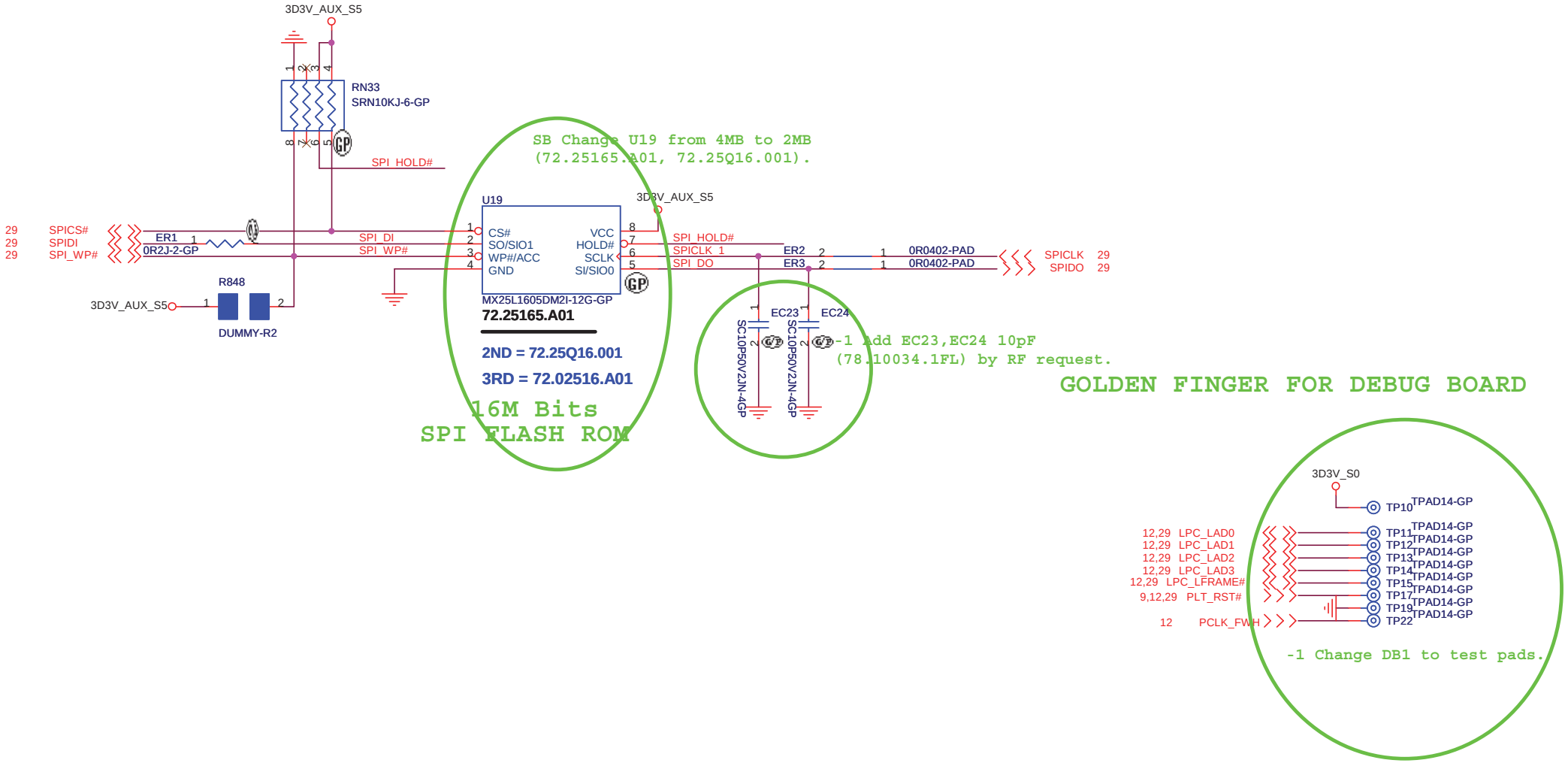
Title: RUN AND AUX POWER

Size	Document Number	Rev
A3	SJV10-NL	-1

Date: Sunday, January 31, 2010 Sheet 27 of 42


CPU FAN Connector
-1 Change R844 to short pad.
3D3V_AUX_S5
RN28
SRN10KJ-6-GP
84.2N702.D31
84.2N702.E31
2N7002E-1-GP
RSMRST#_CTRL
PURE_HW_SHUTDOWN#
D28
Q10
SB Add D28 for thermal trigger S5 shutdown
RSMRST#
BAS16-6-GP
83.00016.F11
S5_ENABLE 29,34,41
D9
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
RSMRST# 6,29
C362
SCD1U16V2ZY-2GP
(dummy, KBC already delay)
3D3V_S0
R844
0R0402-PAD
29 FAN_TACH
R37
10KR2J-3-GP
29 FAN_PWM1
FAN1
MLX-CON4-15-GP-U
20.F0693.004
R845
FAN_TACH1
0R2J-2-GP
LINEAR
FAN_TACH1_CON
FAN_VCC_CON
FAN_VCC
R846
0R3J-0-U-GP
LINEAR
C365
SC10U10V5KX-2GP
5V_S0
R847
0R0603-PAD
-1 Change R847 to short pad.
D26
BAS16-6-GP
83.00016.F11
U59
13,19,27,29,35 PM_SLP_S3#
12 RTC_CLK
74LVC1G08GW-1-GP
73.01G08.L04
73.7SZ08.DAH
R825
10R2J-2-GP
32KHZ
G792_32K
R829
10R2J-2-GP
KBC_XO 29
SB R829 change to placed.
FAN_TACH1
Layout 15 mil
C512
SC1KP50V2JN-2GP
Layout 30 mil
R826
10R2J-2-GP
5V_G792_S0
C226
SC4D7U6D3V3KX-GP
C513
DY
C514
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
C516
SC1U10V3KX-4GP
R827
21KR2F-GP
R828
49K9R2F-L-GP
T8=90
14 ALERT#
V_DEGREE
27 RUNPWROK
PURE_HW_SHUTDOWN#
U60
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
DGND
DGND
SGND1
SGND2
SGND3
FAN1
FG1
CLK
SDA
SCL
NC#19
G792SFUF-GP
74.00792.A79
G792_32K
SMBD_THERM 29
SMBC_THERM 29
3.System Sensor, Put Plamrest.
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
GAP-CLOSE
G119
GAP-CLOSE
G120
C517
C518
C519
SC2200P50V2KX-2GP
SC470P50V3JN-2GP
Q61
MMBT3904-4-GP
84.T3904.C11
SC2200P50V2KX-2GP
2ND = 84.03904.K11
C520
SC470P50V3JN-2GP
Q60
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.K11
2.H/W Shutdown
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C521
SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Conn
Size
Custom
Document Number
SJV10-NL
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-1
Date: Wednesday, January 27, 2010
Sheet 28 of 42


PCB Version
Pull-Low Pull-High
SA 10K 1K
SB 10K 2K
-1 10K 3K
SB Change PCB version pull high from 3D3V_AUX_S5 to 3D3V_S5
SB Del X4,C376,C378,R208,R206
SB Del WIRELESS_BTN# and 3G_BTN#
-1 AddC377 33pF (78.33034.1FL) by RF request.
SB Add D29 for surge prevent.
SB Change net ALL_LED_OFF to WALN_LED
-1 Change GPIO71 reserve for 60W adaptor.
SB Add net RSMRST# in RN32 for damping BJT.
Internal KeyBoard Connector
-1 Change 20.K0246.024 to 20.K0391.024
2nd = 20.K0320.024
Check 漏電fun
FOR KBC DEBUG
THERMAL------>
BATTERY------>
U18A
U18B
KBC
PS/2
FIU
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
NPCE781BA0DX-GP
Wistron Corporation
KBC NPCE781B
SJV10-NL



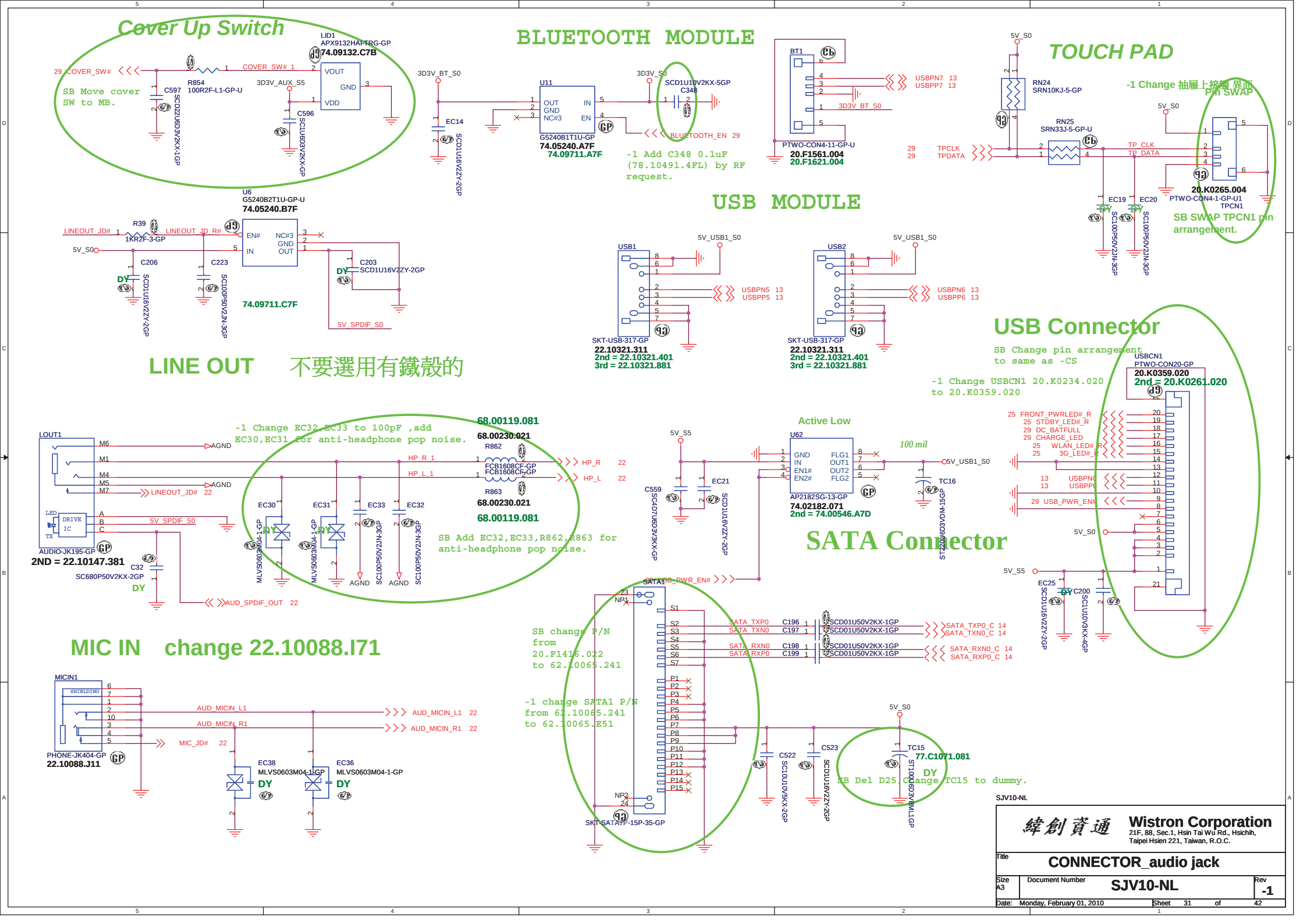
SJV10-NL

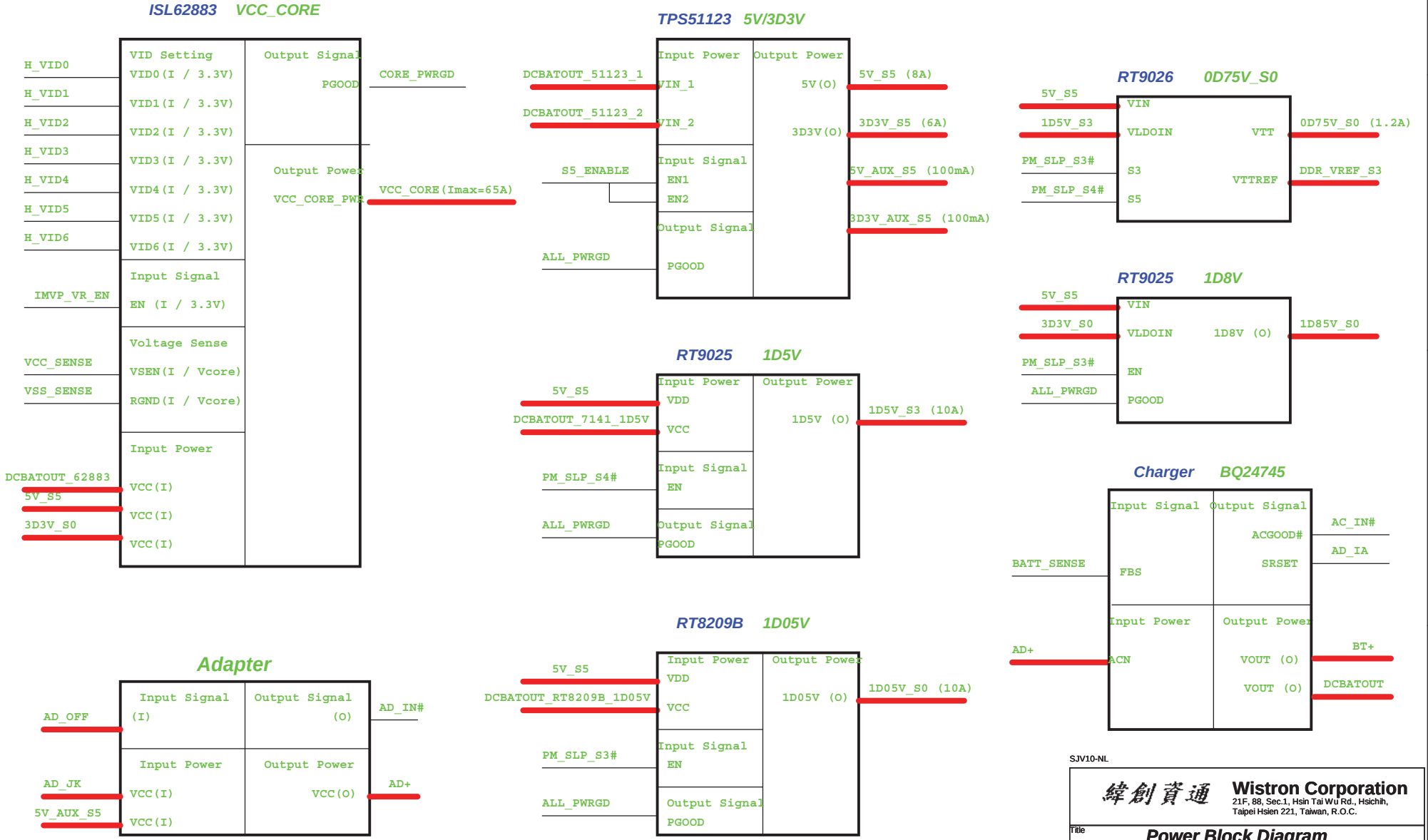
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

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Custom	**SJV10-NL**	**-1**

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Cover Up Switch
LID1
APX9132HAFTRG-GP
74.09132.C7B
29 COVER_SW#
COVER_SW# 1
R854
100R2F-L1-GP-U
3D3V_AUX_S5
C597
SC02U6D3V2KX-1GP
C596
SC1U6D3V2KX-GP
VOUT
GND
VDD
SB Move cover SW to MB.
BLUETOOTH MODULE
3D3V_BT_S0
EC14
SCD1U16V2ZY-2GP
U11
G5240B1T1U-GP
74.05240.A7F
74.09711.A7F
OUT
IN
GND
NC#3
EN
3D3V_S0
SCD1U10V2KX-5GP
C348
BLUETOOTH_EN 29
-1 Add C348 0.1uF (78.10491.4FL) by RF request.
BT1
PTWO-CON4-11-GP-U
20.F1561.004
20.F1621.004
USBPN7 13
USBPP7 13
3D3V_BT_S0
TOUCH PAD
5V_S0
RN24
SRN10KJ-5-GP
RN25
SRN33J-5-GP-U
TP_CLK
TP_DATA
29 TPCLK
29 TPDATA
-1 Change 抽屜上接觸 界面 Pin SWAP
20.K0265.004
PTWO-CON4-1-GP-U1
TPCN1
EC19
EC20
SC100P50V2JN-3GP
SB SWAP TPCN1 pin arrangement.
U6
G5240B2T1U-GP
74.05240.B7F
LINEOUT_JD#
LINEOUT_JD_R#
R39
1KR2F-3-GP
C206
C223
C203
SCD1U16V2ZY-2GP
SC100P50V2JN-3GP
74.09711.C7F
5V_SPDIF_S0
USB MODULE
USB1
USB2
5V_USB1_S0
USBPN5 13
USBPP5 13
USBPN6 13
USBPP6 13
SKT-USB-317-GP
22.10321.311
2nd = 22.10321.401
3rd = 22.10321.881
USB Connector
SB Change pin arrangement to same as -CS
-1 Change USBCN1 20.K0234.020 to 20.K0359.020
USBCN1
PTWO-CON20-GP
20.K0359.020
2nd = 20.K0261.020
25 FRONT_PWRLED#_R
25 STDBY_LED#_R
29 DC_BATFULL
29 CHARGE_LED
25 WLAN_LED#_R
25 3G_LED#_R
13 USBPN0
13 USBPP0
29 USB_PWR_EN#
LINE OUT 不要選用有鐵殼的
LOUT1
AUDIO-JK195-GP
2ND = 22.10147.381
AGND
LINEOUT_JD# 22
5V_SPDIF_S0
AUD_SPDIF_OUT 22
C32
SC680P50V2KX-2GP
-1 Change EC32,EC33 to 100pF ,add EC30,EC31 for anti-headphone pop noise.
EC30
EC31
EC33
EC32
MLVS0603M04-1-GP
SC100P50V2JN-3GP
68.00119.081
68.00230.021
R862
R863
FCB1608CF-GP
HP_R_1
HP_L_1
HP_R 22
HP_L 22
SB Add EC32,EC33,R862,R863 for anti-headphone pop noise.
Active Low
U62
AP2182SG-13-GP
74.02182.071
2nd = 74.00546.A7D
100 mil
5V_S5
EC21
SCD1U16V2ZY-2GP
SC4D7U6D3V3KX-GP
TC16
ST220U6D3VDM-15GP
5V_USB1_S0
SATA Connector
SATA1
SKT-SATA7P-15P-35-GP
SB change P/N from 20.F1416.022 to 62.10065.241
-1 change SATA1 P/N from 62.10065.241 to 62.10065.E51
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
C196
C197
C198
C199
SCD01U50V2KX-1GP
SATA_TXP0_C 14
SATA_TXN0_C 14
SATA_RXN0_C 14
SATA_RXP0_C 14
C522
C523
SC10U10V5KX-2GP
SCD1U16V2ZY-2GP
TC15
77.C1071.081
DY
SB Del D25,Change TC15 to dummy.
MIC IN change 22.10088.I71
MICIN1
PHONE-JK404-GP
22.10088.J11
AUD_MICIN_L1
AUD_MICIN_R1
MIC_JD# 22
EC38
EC36
MLVS0603M04-1-GP
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CONNECTOR_audio jack
Size A3
Document Number
SJV10-NL
Rev -1
Date: Monday, February 01, 2010
Sheet 31 of 42



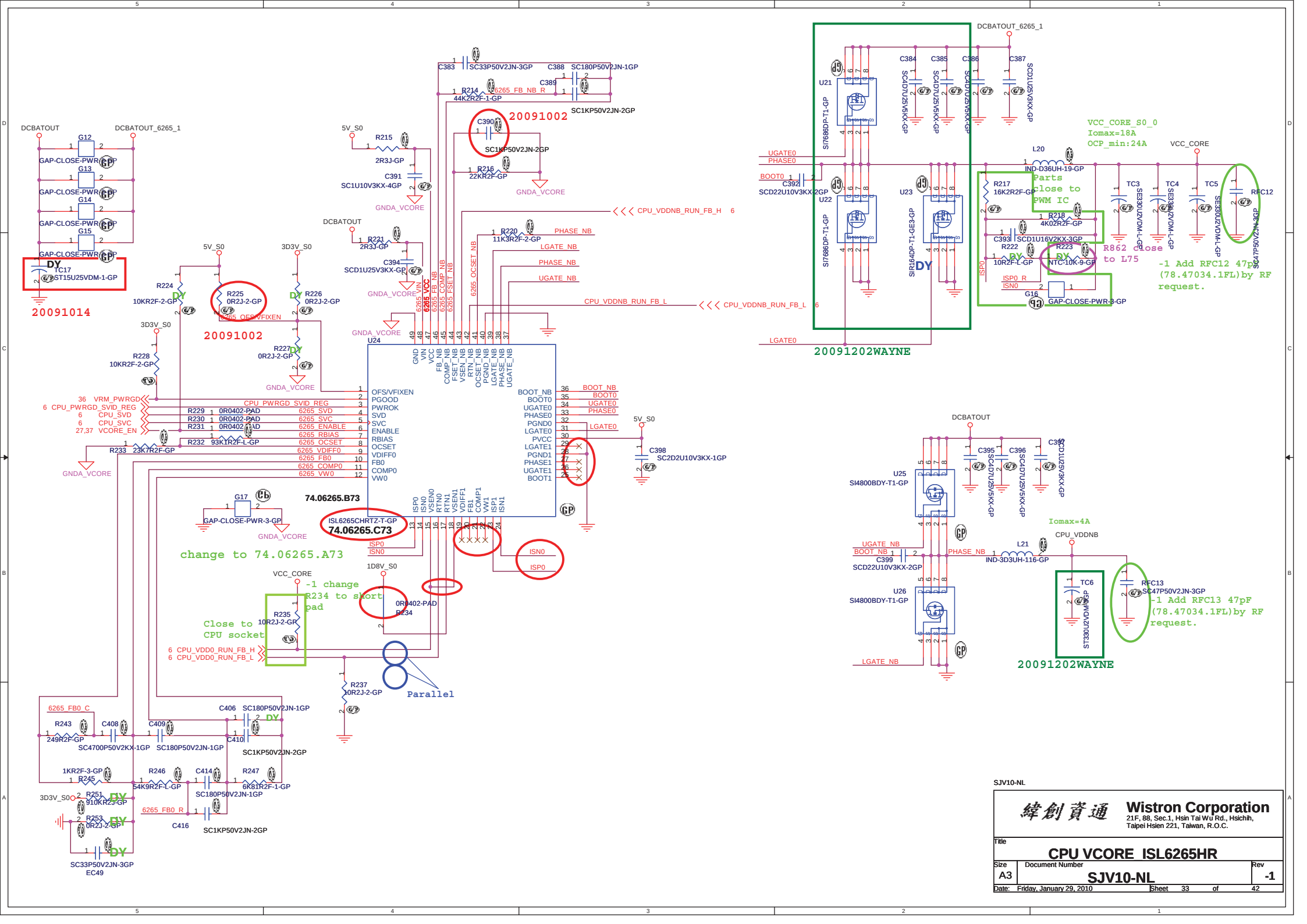
SJV10-NL

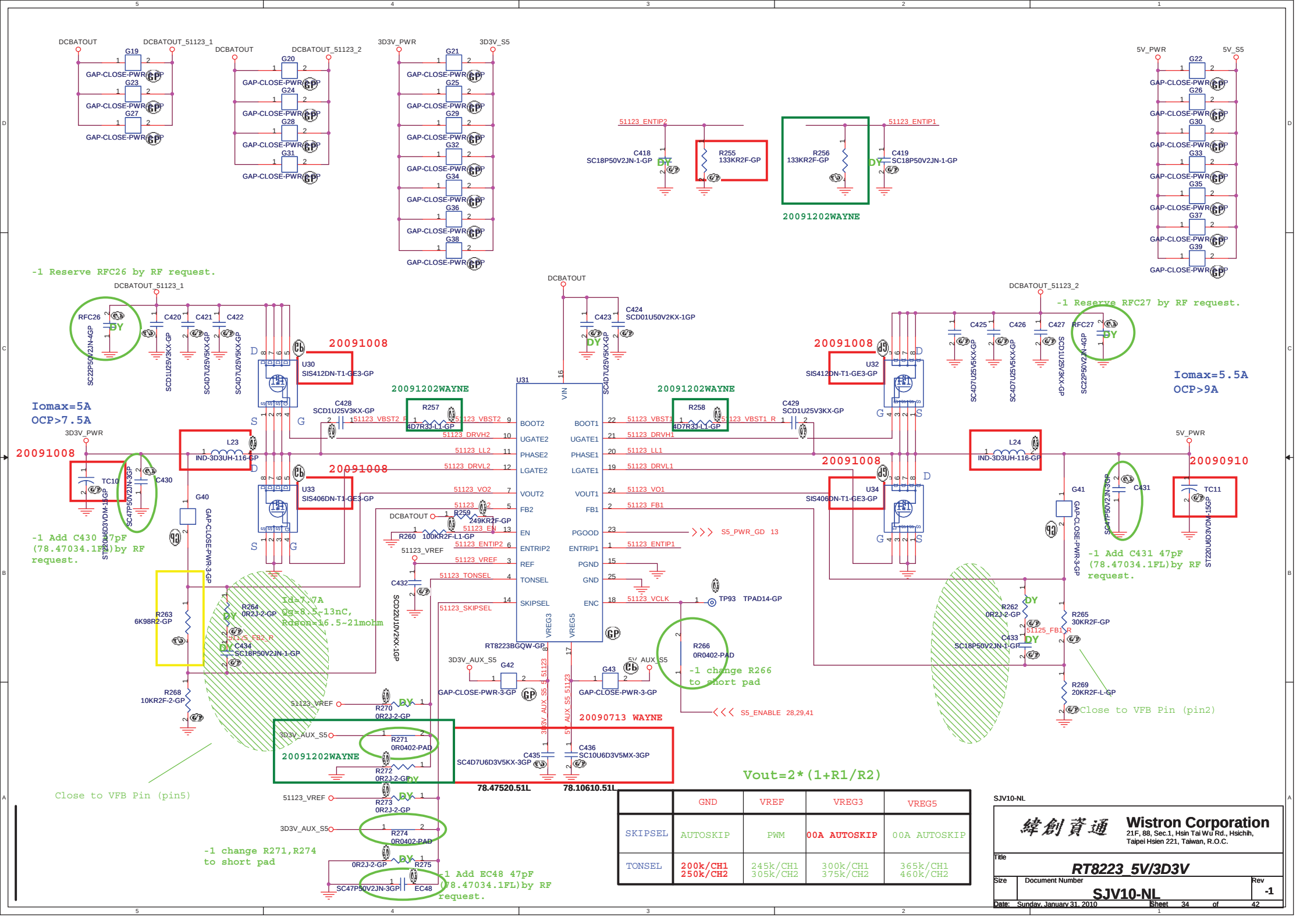
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

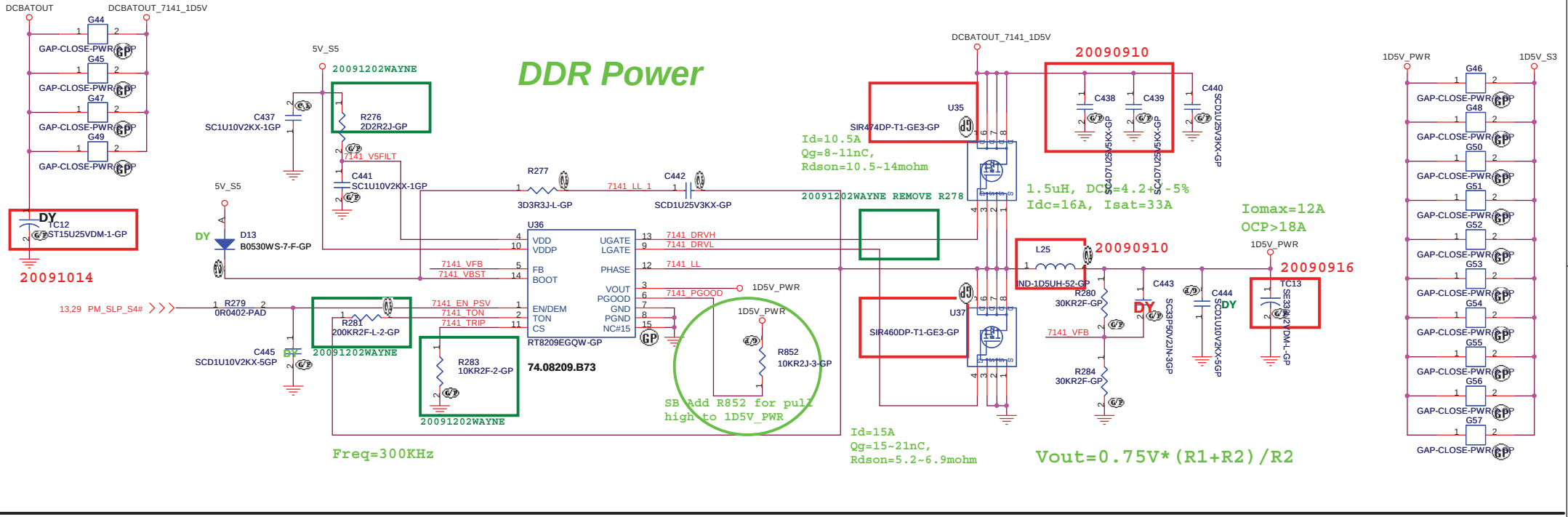
Size	Document Number	Rev
	SJV10-NL	-1

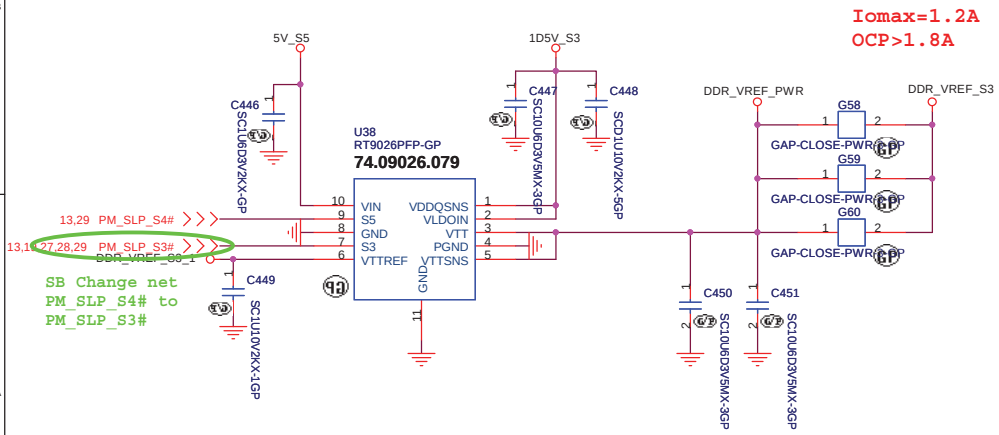
Date: Tuesday, January 05, 2010 Sheet 32 of 42


DCBATOUT
DCBATOUT_6265_1
GAP-CLOSE-PWR-GP
DY
TC17
ST15U25VDM-1-GP
20091014
5V_S0
3D3V_S0
R224
10KR2F-2-GP
R225
0R2J-2-GP
R226
0R2J-2-GP
R227
0R2J-2-GP
R228
10KR2F-2-GP
6265_OFS/VFIXEN
20091002
GNDA_VCORE
U24
OFS/VFIXEN
PGOOD
PWROK
SVD
SVC
ENABLE
RBIAS
OCSET
VDIFF0
FB0
COMP0
VW0
GND
VIN
VCC
FB_NB
COMP_NB
FSET_NB
VSEN_NB
RTN_NB
OCSET_NB
PGND_NB
LGATE_NB
PHASE_NB
UGATE_NB
BOOT_NB
BOOT0
UGATE0
PHASE0
PGND0
LGATE0
PVCC
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISL6265CHRTZ-T-GP
74.06265.C73
74.06265.B73
G17
GAP-CLOSE-PWR-3-GP
change to 74.06265.A73
VRM_PWRGD
CPU_PWRGD_SVID_REG
CPU_SVD
CPU_SVC
VCORE_EN
R229 0R0402-PAD 6265_SVD
R230 0R0402-PAD 6265_SVC
R231 0R0402-PAD 6265_ENABLE
R232 93K1R2F-L-GP 6265_RBIAS
R233 23K7R2F-GP
6265_OCSET
6265_VDIFF0
6265_FB0
6265_COMP0
6265_VW0
ISP0
ISN0
C398
SC2D2U10V3KX-1GP
1D8V_S0
VCC_CORE
-1 change R234 to short pad
0R0402-PAD
R234
R235
10R2J-2-GP
Close to CPU socket
6 CPU_VDD0_RUN_FB_H
6 CPU_VDD0_RUN_FB_L
R237
10R2J-2-GP
Parallel
C383
SC33P50V2JN-3GP
C388
SC180P50V2JN-1GP
C389
SC1KP50V2JN-2GP
R214
44K2R2F-1-GP
6265_FB_NB_R
C390
SC1KP50V2JN-2GP
R216
22KR2F-GP
R215
2R3J-GP
C391
SC1U10V3KX-4GP
R221
2R3J-GP
C394
SCD1U25V3KX-GP
6265_VIN
6265_VCC
6265_FB_NB
6265_COMP_NB
6265_FSET_NB
6265_OCSET_NB
R220
11K3R2F-2-GP
PHASE_NB
LGATE_NB
UGATE_NB
CPU_VDDNB_RUN_FB_H 6
CPU_VDDNB_RUN_FB_L 6
6265_FB0_C
R243
249R2F-GP
C408
SC4700P50V2KX-1GP
C409
SC180P50V2JN-1GP
C406
SC180P50V2JN-1GP
C410
SC1KP50V2JN-2GP
1KR2F-3-GP
R245
R246
54K9R2F-L-GP
C414
SC180P50V2JN-1GP
R247
6K81R2F-1-GP
R251
910KR2J-GP
R253
0R2J-2-GP
6265_FB0_R
C416
SC1KP50V2JN-2GP
SC33P50V2JN-3GP
EC49
DCBATOUT_6265_1
U21
SI7686DP-T1-GP
U22
SI7686DP-T1-GP
U23
SIR164DP-T1-GE3-GP
C384
C385
C386
C387
SCD1U25V3KX-GP
SC4D7U25V5KX-GP
UGATE0
PHASE0
BOOT0
C392
SCD22U10V3KX-2GP
LGATE0
20091202WAYNE
VCC_CORE_S0_0
Iomax=18A
OCP_min:24A
VCC_CORE
L20
IND-D36UH-19-GP
Parts close to PWM IC
R217
16K2R2F-GP
R218
4K02R2F-GP
C393
SCD1U16V2KX-3GP
R222
10R2F-L-GP
R223
NTC-10K-9-GP
R862 close to L75
ISP0_R
ISN0
G16
GAP-CLOSE-PWR-8-GP
TC3
TC4
TC5
SE330U2VDM-L-GP
RFC12
SC47P50V2JN-3GP
-1 Add RFC12 47pF (78.47034.1FL)by RF request.
DCBATOUT
U25
SI4800BDY-T1-GP
U26
SI4800BDY-T1-GP
C395
C396
C397
SC4D7U25V5KX-GP
SCD1U25V3KX-GP
Iomax=4A
CPU_VDDNB
UGATE_NB
BOOT_NB
C399
SCD22U10V3KX-2GP
PHASE_NB
L21
IND-3D3UH-116-GP
LGATE_NB
TC6
ST330U2VDM-GP
RFC13
SC47P50V2JN-3GP
-1 Add RFC13 47pF (78.47034.1FL)by RF request.
20091202WAYNE
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU VCORE ISL6265HR
Size
A3
Document Number
SJV10-NL
Rev
-1
Date: Friday, January 29, 2010
Sheet 33 of 42



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2



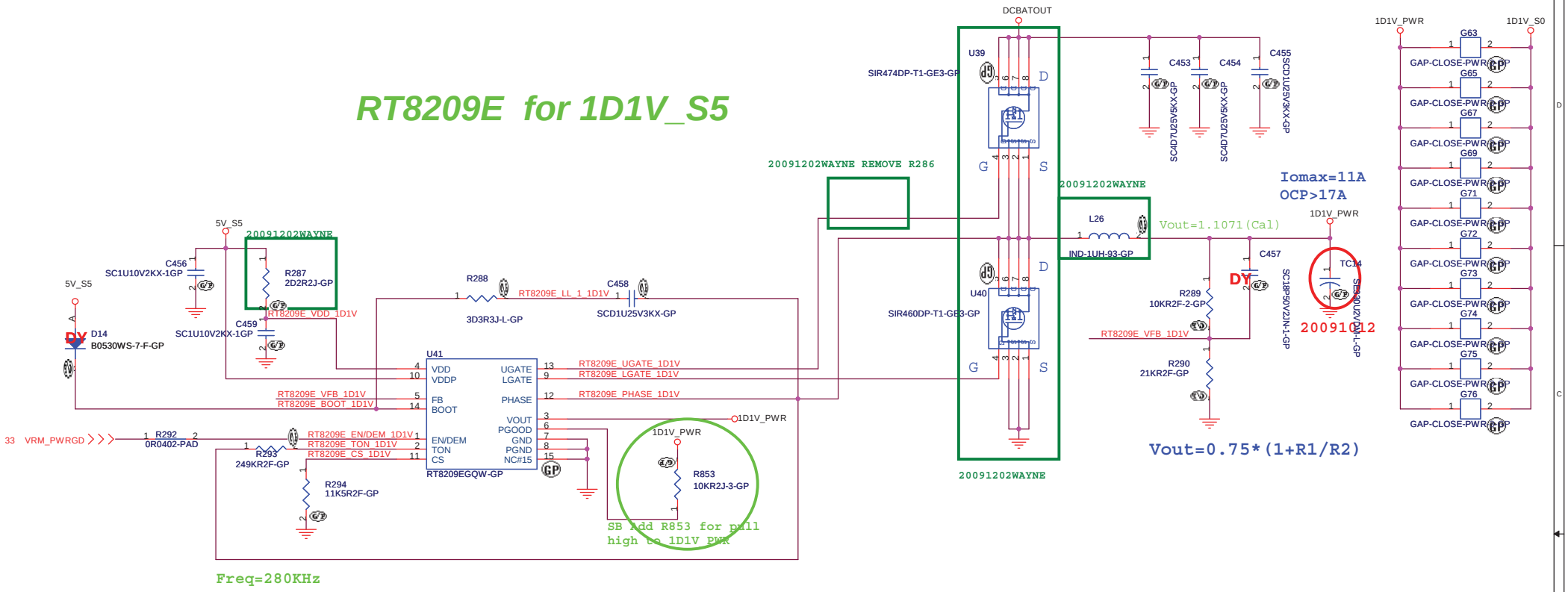


SJV10-NL

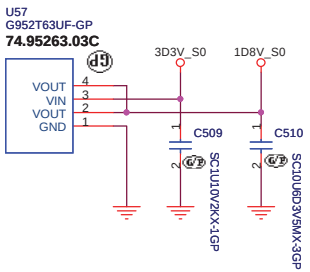
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209E_1D5V/RT9026_0D75V	
Size	Document Number: SJV10-NL	Rev: -1
Date: Sunday, January 31, 2010	Sheet 35 of 42	

RT8209E for 1D1V_S5



1.8V_S0 1.8V 1A Regulator



SJV10-NL

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RT8209E_1D1V/LDO 1D8V***
Size	Document Number: **SJV10-NL** — Rev: **-1**
Date: Tuesday, January 26, 2010	Sheet 36 of 42

RT9025 for 1D1V_S5

0921

Iomax=1.4A
OCP>2A

Iomax=1.4A
OCP>2A

3D3V_S5
5V_S5
C589 SC10U6D3V5MX-3GP DY
C590 SC10U6D3V5MX-3GP
C591 SC1U50V2KX-GP
U64
VDD VIN EN PGOOD GND NC#5 VOUT ADJ GND
RT9025-25PSP-GP
74.09025.03D
0925
TPAD14-GPTP113
1D1V_S5_PWRGD
Vo(cal.)=1.0518V
1D1V_S5
R849 6K2R2F
C592 SC100P50V2JN-3GP DY
C594 SC10U6D3V5MX-3GP
C593 SC10U6D3V5MX-3GP DY
9025_ADJ_1D1
R850 16K2R2F-GP
Vo=0.8*((R1+R2)/R2)
=0.8*((6.2K+16.2K)/16.2K)=1.106V

5V_S5
RFC39 RFC40 RFC41 RFC42 RFC43 RFC45 RFC37 RFC38 SC22P50V2JN-4GP DY
-1 Reserve RFC28~RFC30,RFC37~RFC42,RFC44,RFC45 by RF request.
RFC28 RFC29 RFC30 SC22P50V2JN-4GP DY
C504 SC1U10V3KX-4GP
1D5V_S3
U56
VDD VIN EN PGOOD GND NC#5 VOUT ADJ GND
RT9025-25PSP-GP
74.09025.03D
C508 SC1U10V5KX-2GP
27,33 VCORE_EN
3D3V_S0
R824 2K2R2J-2-GP
9025_POK
CPU_VDDR
R822 2K55R2F-GP
9025_FB
R823 20KR2F-L-GP
C505 SC100P50V2JN-3GP
C506 SC10U10V5KX-2GP
C507 SC10U10V5KX-2GP
Vo=0.8*(1+(R1/R2))

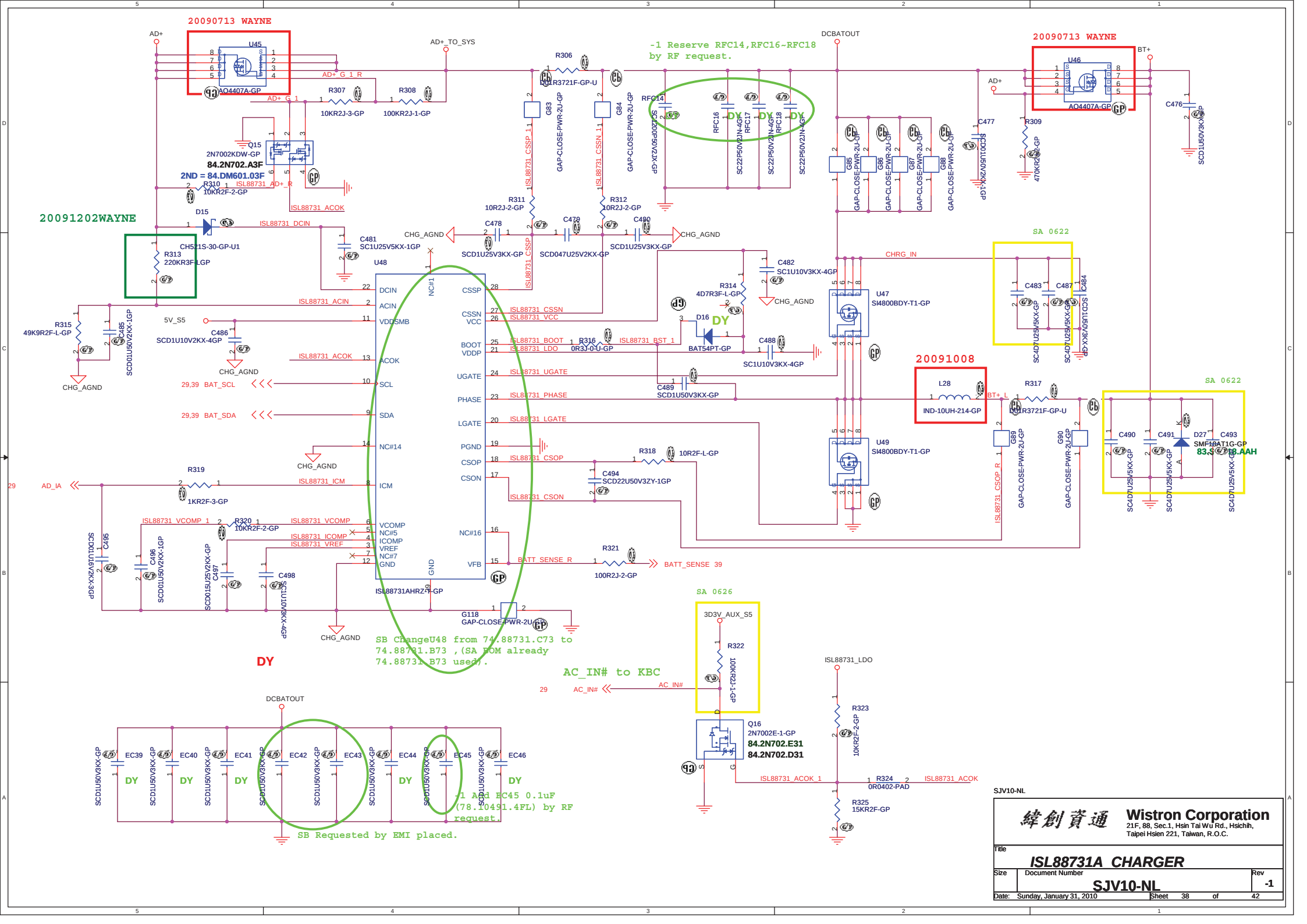
SJV10-NL

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

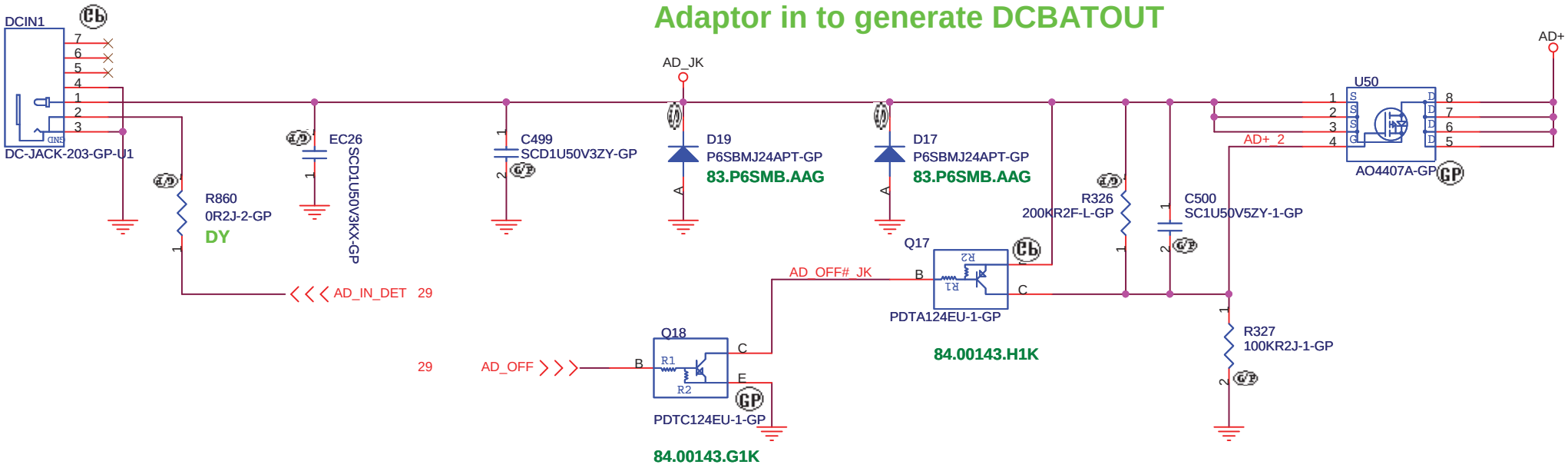
Title: LDO 1D5_S0 0D9_S0

Size	Document Number	Rev
A3	SJV10-NL	-1

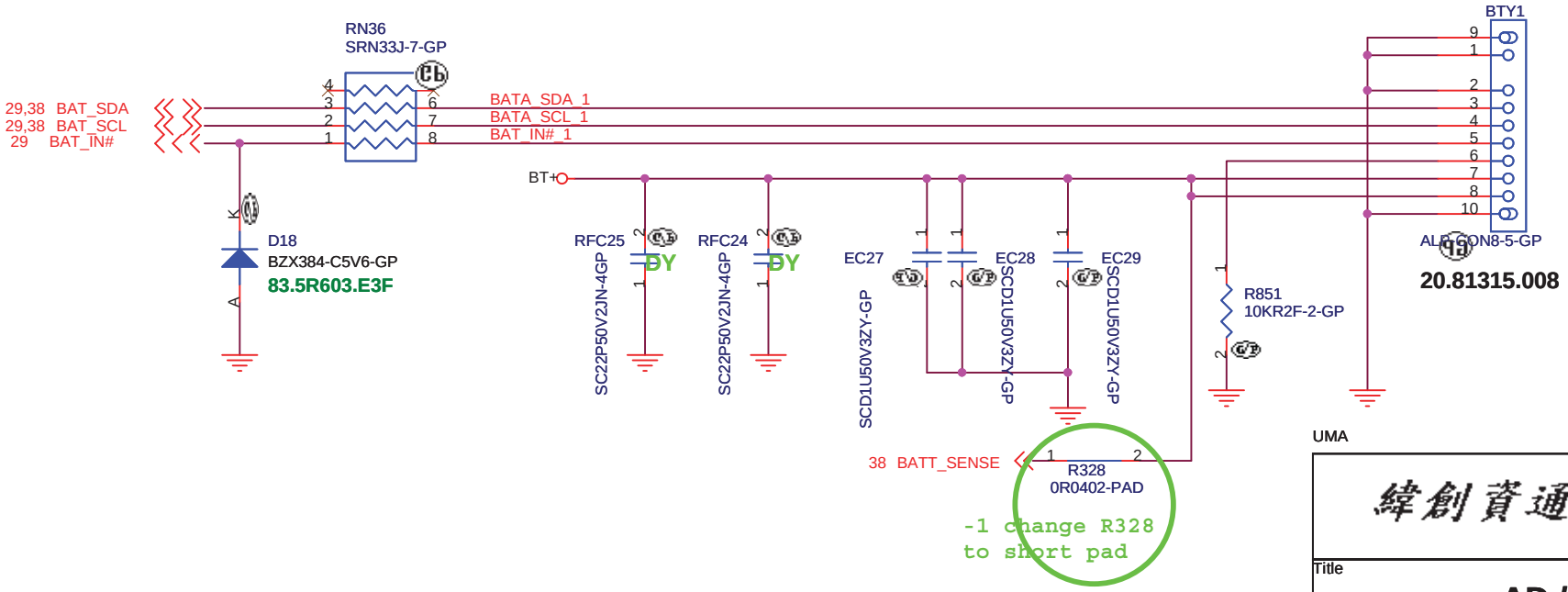
Date: Sunday, January 31, 2010 Sheet 37 of 42


20090713 WAYNE
AO4407A-GP
AD+
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R307
10KR2J-3-GP
R308
100KR2J-1-GP
R306
0R3R3721F-GP-U
-1 Reserve RFC14,RFC16~RFC18 by RF request.
DCBATOUT
20090713 WAYNE
AO4407A-GP
BT+
C476
SCD1U50V3KX-GP
R309
470KR2F-GP
C477
SCD001U50V2KX-1GP
Q15
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R310
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
20091202WAYNE
D15
ISL88731_DCIN
CH571S-30-GP-U1
R313
220KR3F-1-GP
C481
SC1U25V5KX-1GP
CHG_AGND
R311
10R2J-2-GP
R312
10R2J-2-GP
C478
SCD1U25V3KX-GP
C479
SCD047U25V2KX-GP
C480
SCD1U25V3KX-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
GAP-CLOSE-PWR-2U-GP
SC220P50V2JX-GP
RFC14
RFC16
RFC17
RFC18
SC22P50V2JN-4GP
SC22P50V2JN-1GP
DY
G83
G84
G85
G86
G87
G88
SA 0622
CHRG_IN
C482
SC1U10V3KX-4GP
R314
4D7R3F-L-GP
D16
BAT54PT-GP
C488
SC1U10V3KX-4GP
U47
SI4800BDY-T1-GP
U49
SI4800BDY-T1-GP
C483
C487
C484
SC4D7U25V5KX-GP
SCD01U50V2KX-1GP
U48
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_ACIN
ISL88731_ACOK
29,39 BAT_SCL
29,39 BAT_SDA
ISL88731_ICM
ISL88731_VCOMP_1
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_BST_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
R315
49K9R2F-L-GP
C485
SCD01U50V2KX-1GP
C486
SCD1U10V2KX-4GP
R316
0R3J-0-U-GP
C489
SCD1U50V3KX-GP
R317
0R3R3721F-GP-U
20091008
L28
IND-10UH-214-GP
BT+_L
SA 0622
C490
C491
D27
SMF18AT1G-GP
C493
SC4D7U25V5KX-GP
83.SMF18.AAH
R318
10R2F-L-GP
C494
SCD22U50V3ZY-1GP
R319
1KR2F-3-GP
AD_IA
R320
10KR2F-2-GP
C495
SCD01U16V2KX-3GP
C496
SCD01U50V2KX-1GP
C497
SCD015U25V2KX-GP
C498
SCD1U10V3KX-4GP
R321
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 39
G118
GAP-CLOSE-PWR-2U-GP
SA 0626
3D3V_AUX_S5
R322
100KR2J-1-GP
AC_IN#
AC_IN# to KBC
Q16
2N7002E-1-GP
84.2N702.E31
84.2N702.D31
R323
10KR2F-2-GP
R324
0R0402-PAD
R325
15KR2F-GP
ISL88731_ACOK_1
SB ChangeU48 from 74.88731.C73 to 74.88731.B73 ,(SA ROM already 74.88731.B73 used).
DY
EC39
EC40
EC41
EC42
EC43
EC44
EC45
EC46
SCD1U50V3KX-GP
Add EC45 0.1uF (78.10491.4FL) by RF request.
SB Requested by EMI placed.
SJV10-NL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A CHARGER
Size
Document Number
SJV10-NL
Rev
-1
Date: Sunday, January 31, 2010
Sheet 38 of 42

Adaptor in to generate DCBATOUT



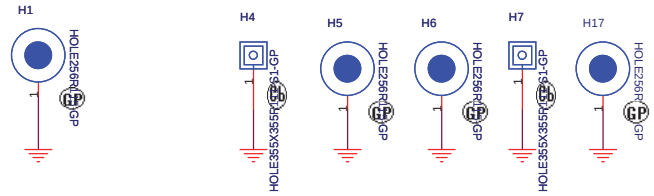
BATTERY CONNECTOR



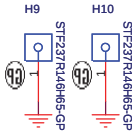
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD / BATT_CONN	
Size	Document Number: SJV10-NL	Rev: -1
Date: Saturday, January 30, 2010	Sheet 39 of 42	



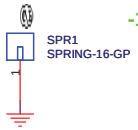
MB HOLE

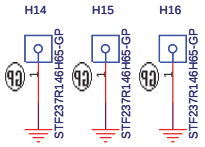


MINI CARD BOSS

SPRING

-1 Add SPR1 for RTC battery.

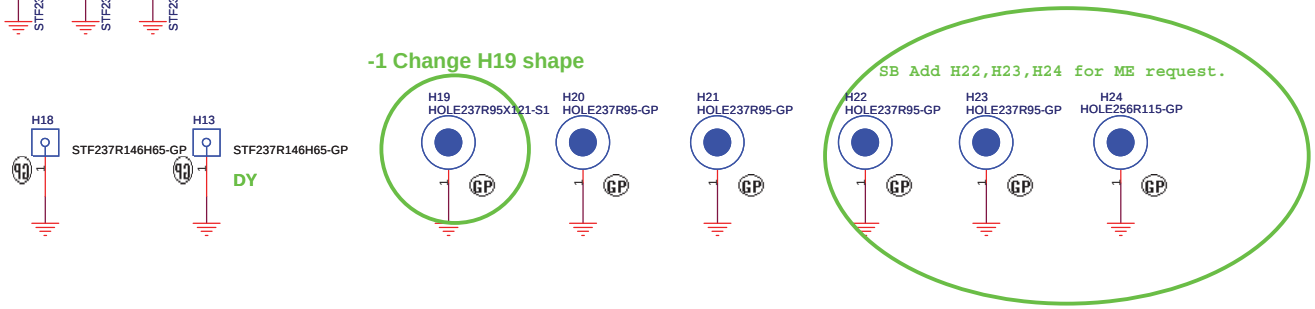




CPU NB BOSS

-1 Change H19 shape

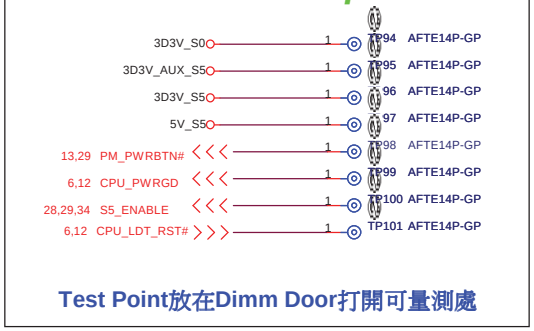
SB Add H22,H23,H24 for ME request.



SJV10-NL

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: EMI/Spring/Boss		
Size	Document Number: SJV10-NL	Rev: -1
Date: Wednesday, January 27, 2010	Sheet 40 of 42	

Check test point



Test Point放在Dimm Door打開可量測處

SJV10-NL

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AFTE_TP	
Size	Document Number: SJV10-NL	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 41 of 42	

SB Change notice:

1. Change C344 from 10uF to 0.1uF for anti pop noise.(Page 22)
2. ChangeU48 circuit from 74.88731.C73 to 74.88731.B73 ,(SA BOM already 74.88731.B73 used.).(Page 38)
3. SWAP TPCN1pin arrangement.(Page 31)
4. Change U19 to 2MB(72.25165.A01, 72.25016.A01).(Page 30)
5. X1 need to change to the same as JV10-CS (82.30005.A51).(Page 3)
6. Del X4,C376,C378,R208,R206 ,R829 change to placed.(Page 28,29)
7. Add G122 (Page 12).
8. Add net RSMRST# in RN32 for damping BJT.(Page 29)
9. X5 2nd source change from 82.30005.C51 to 82.30020.A31,Change C540 from 27pF to 18pF,Change C541 from 27pF to 15pF(Page 23)
10. R272 change to dummy.(Page 34)
11. Change R43 from Dummy to 1M ohm.(Page 12)
12. Del R285, Add R852,R853 for pull high to 1D1V_PWR and 1D5V_PWR.(Page 35,36)
13. Change RN30 form page31 to page 22.
14. Add D28 for thermal trigger S5 shutdown.(Page 28)
15. Del net RSMRST#_SB pull high , Change S5_PWR_GD pull high from R261 to RN43.(Page 13)
16. Change pin arrangement to same as -CS, move cover SW to MB,Del WIRELESS_BTN# and 3G_BTN#. (Page 29,31)
17. Change PCB version pull high from 3D3V_AUX_S5 to 3D3V_S5,R836 1K change to 2K (page29).
18. Change GPIO16 net name from ALL_LED_OFF to WLAN_LED .(page29)
19. Change C558 1000pF P/N form 78.1022S.24L to 78.1022S.L1L.(page24)
20. Change capacity from 6.8pF (78.6R864.1FL) to 5.6pF (78.5R674.1FL)(page20).
21. Change net PCLK_FWH to LPCCLK0_R change net PCLK_KBC to LPCCLK1_R(page16).
22. Change R180,R104,Q4 to placed(page27).
23. Change P/N from 20.F1416.022 to 62.10065.241(page31).
24. Add D29 for surge prevent.(page29).
25. Change Mini card 3G pin41 from 5V_S5 to NC.(page26).
26. Add C598 for solve CRT flicker issue (page9).
27. Change R859 from 150 ohm to 140 ohm (page20).
28. Add H22,H23,H24 for ME request. (page40).
29. Del net E51_RxD ,E51_TxD (page26).
30. Change R71 from bead 470 ohm to RES 3.9 ohm(page9).
31. Del D25.(page31).
32. Add RTC charge circuit.(page12).
33. EC42,EC43 requested by EMI placed.(page38).
34. Change LCD1 P/N from 20.F1093.040 to 20.F1703.040(page19).
35. Change net PM_SLP_S4# to PM_SLP_S3#.(page35).
36. Add EC32,EC33,R862,R863 for anti-headphone pop noise.(page31)
37. Change C189 to 22pF, C190 to 15pF.(page12)
38. Change TC15 to dummy.(page31)

-1 change notices:

1. Change R91,R92 to RN132,R27,R30 to RN133,R34~R36 to RN134.(Page 3)
2. DY C35,C42,C80,Change C36,C43,C569,C79 to 22uF.(Page 7)
3. Change R60,R62 to RN136.(Page 9)
4. Change R84,R85 to RN137,R76,R78 to RN138,R22,R79 to RN139.DY C139,Change C140 to 22uF.(Page 10)
5. Change R89,R88 to RN140.(Page 12)
6. Change R133,R135,R136,R128 to RN141,R138,R139 to RN142.(Page 16)
7. Change C266,C281 to dummy.(Page 17)
8. Change C287,C293,C302 to dummy.(Page 18)
9. Change R16 to short PAD.(Page 19)
10. Change C532 to dummy.(Page 23)
11. Change C331,C400,C361,C363 to dummy,change R832,R833 to RN143.(Page 24)
12. Change C357 to dummy.(Page 26)
13. Change R844,R847 to short pad.(Page 28)
14. Add reserved R865, change pull high to 3D3V_S5.(Page 23)
15. Change 10u/25V(78.10622.51L)to 4.7u/25V(78.47522.51L)(Page 19)
16. Change C483,C423,C487,C490,C491,C493. 10u/25V(78.10622.51L)to 4.7u/25V(78.47522.51L)(Page 34,38)
17. Change USBCN1 20.K0234.020 to 20.K0359.020 (Page 31)
18. Change KB1 20.K0246.024 to 20.K0391.024(Page 29)
19. Change R234 to short pad.(Page 33)
20. Change R266,R271,R274 to short pads.(Page 34)
21. Change R328 to short pad.(Page 39)
22. Change 3G LED portion circuit.(Page 26)
23. Change R166 to reserved D21.(Page 22)
24. Change 抽屜上接觸 異面.(Page 31)
25. Add SPR1 for RTC battery.(Page 40)
26. Add VRAM identify pins.(Page 12)
27. Change EC32,EC33 to 100pF,add EC30,EC31 for anti-headphone pop noise(Page 31)
28. Change GPIO71 reserve for 60W adaptor.(Page 29)
29. Reserve EC47 for EMI issue.(Page 13)
30. Change DB1 to test pads.(Page 30)
31. Change C12,C20,C193 to 12pF,C541 to 18pF.(Page 3,12,23)
32. Add R335,EC74~EC79 for AGND connect.(Page 22)
33. Change Card1 P/N to 62.10024.B41(Page 25)
34. Change 10u/25V(78.10622.51L)to 10u/16V(78.10621.52L)(Page 19)
35. Change SATA1 P/N from 62.10065.241 to 62.10065.E51.(Page 31)
36. Add F4,D25 for ESD function.(Page 21)
37. Reserve C310,RFC1,RFC11,RFC14,RFC16~RFC19,RFC22,RFC24~RFC30,RFC37~RFC42,RFC44~RFC48 by RF request.(Page 3,18,1

SJV10-NL

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