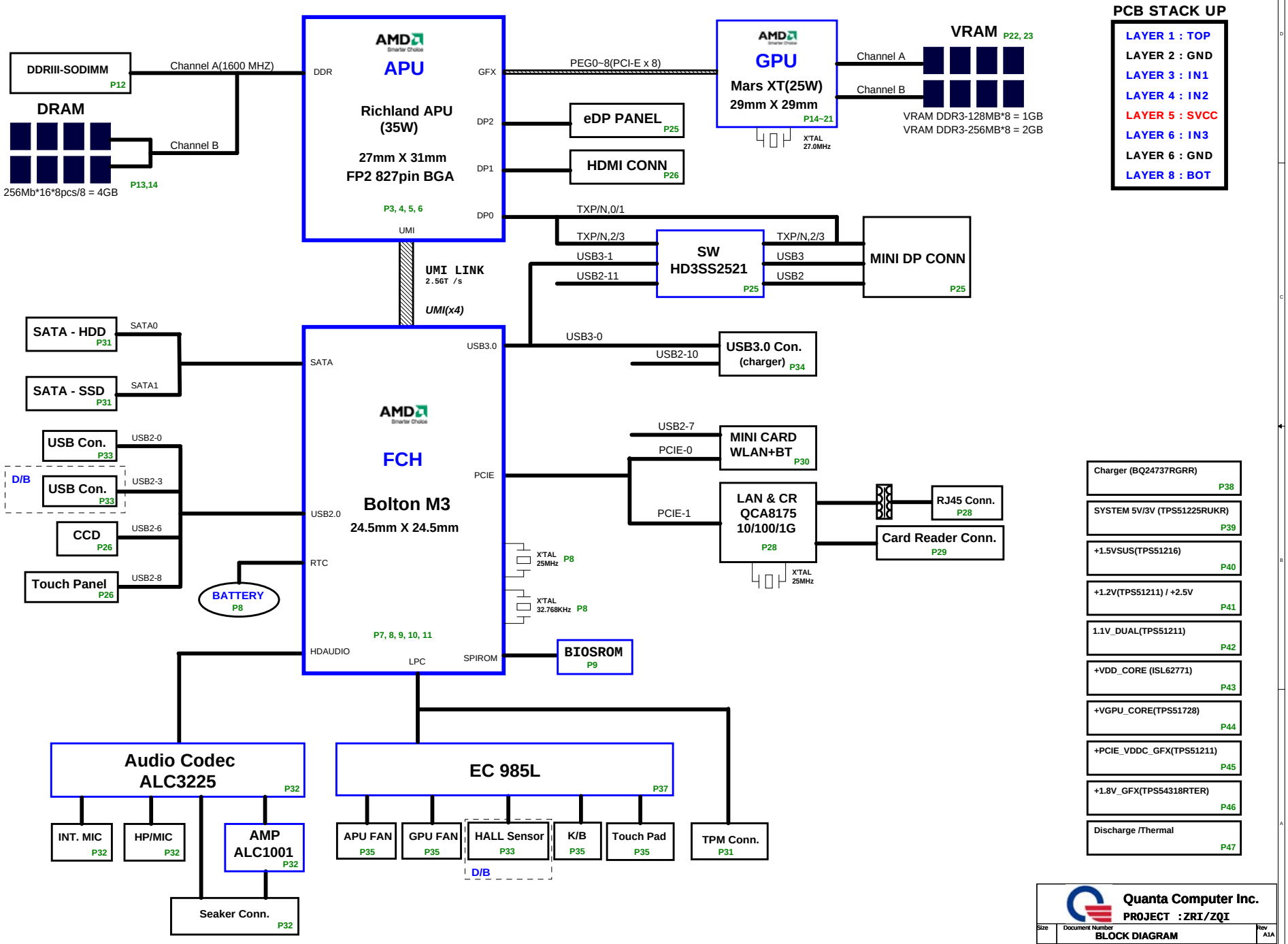
ZRI/ZQI Block Diagram



Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	BLOCK DIAGRAM	A1A

Date: Wednesday, April 24, 2013 Sheet 1 of 50

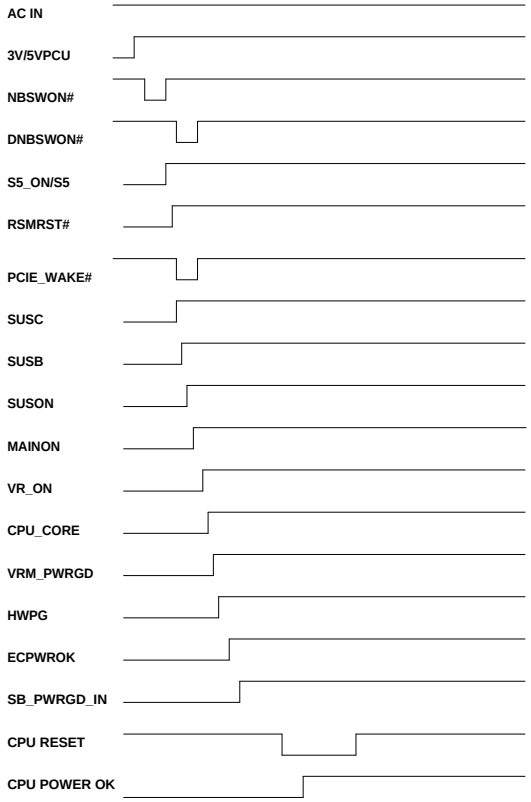
BOM Option

ITEM	DESCRIPTION	MARK
1	LVDS Panel Sku	LVDS@
2	eDP Panel Sku	eDP@
3	VGA Sku	EV@
4	VGA Thames Sku	EV_T@
5	VGA Mars Sku	EV_M@
6	VGA Sku for Thames and Mars stuff different value parts	EV_SP@
7	GPU 128bit Sku	EV_128@
8	GPU 128bit Sku of Special part value change	EV_128SP@
9	USB Charge Functions Sku	CH@
10	No USB Charge Functions Sku	NCH@
11	USB3.0 Re-Driver Sku	RD@
12	No USB3.0 Re-Driver Sku	NRD@
13	Always connect functions Sku	AC@
14	No Always connect functions Sku	NAC@
15	Special part value change or modify for different BOM sku	SP@
16	Key Board Back light Sku	KBL@
17	SSD Sku	SSD@
18	Touch panel Sku	TP@

Page 9 GPIO strap pin

ITEM	DESCRIPTION	MARK
1	Synaptics touch pad	SYNP@
2	ELAN touch pad	ELAN@
3	For UMA Sku	UMA@
4	ELPIDA on board DRAM	ELP@
5	HYNIX on board DRAM	HYN@

Power Sequence



Hudson M3 SMBUS

FCH SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AD25	DDR / WLAN
SCLK1 SDATA1 (+3V_S5)	T7 R7	Touch Pad
SMB_EC_CLK (SCLK2) SMB_EC_DAT (SDATA2) (+3V_S5)	H19 G19	EC
SCLK3 SDATA3 (+3VPCU)	G22 G21	Not used
SCL4 SDATA4 (+3V_S5)	J19 K19	Not used

EC SMBUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	70 69	Battery, FCH
APU_SIC_EC APU_SID_EC (+3V_S5)	67 68	APU
GPUT_CLK GPUT_DATA (+3V_GFX)	119 120	GPU
TPCLK TPDATA (+3V)	72 71	Touch Pad

EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

EC will Conflict with FCH.
Do not mount

Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	SYSTEM INFORMATION	A1A

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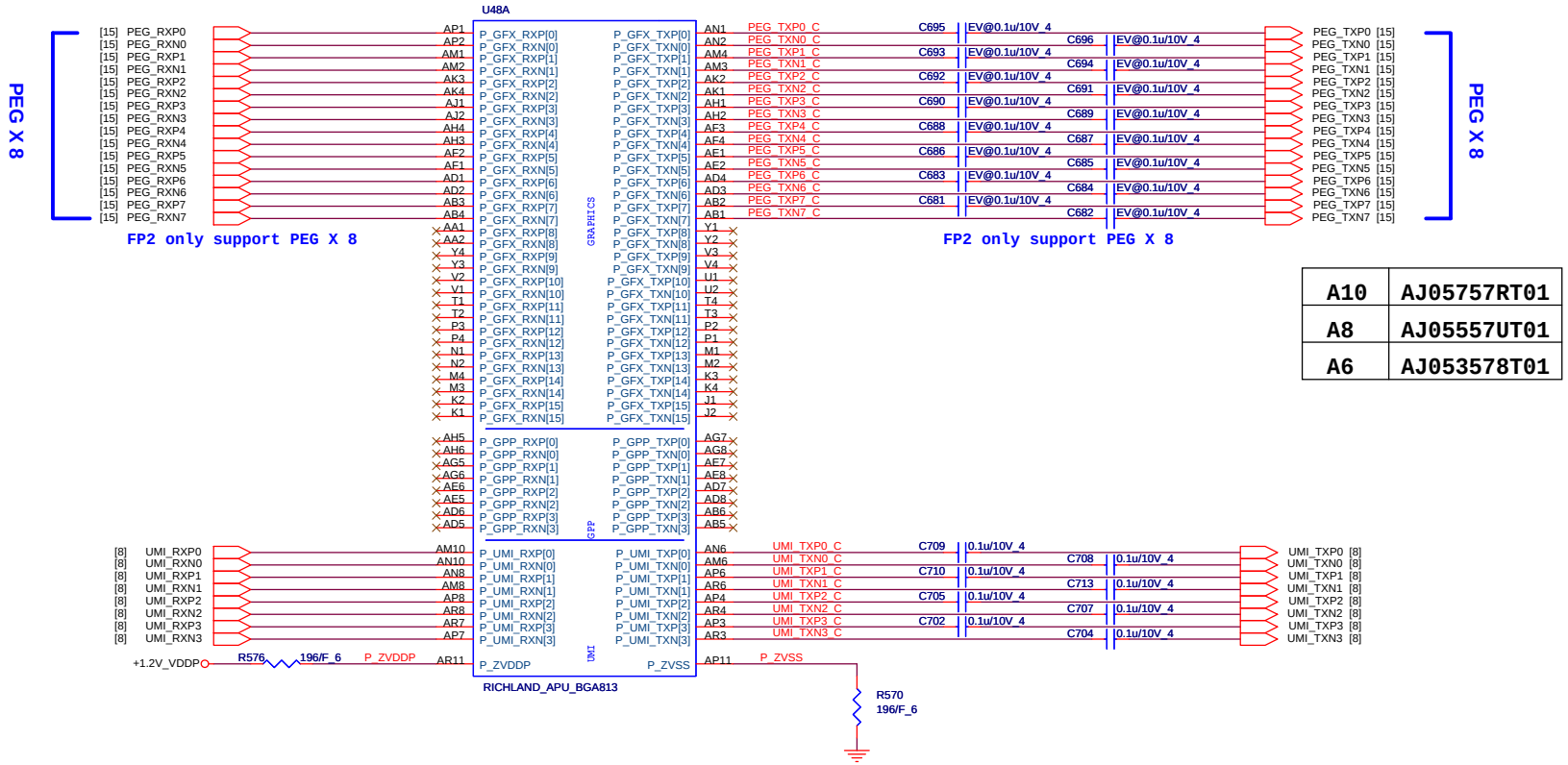
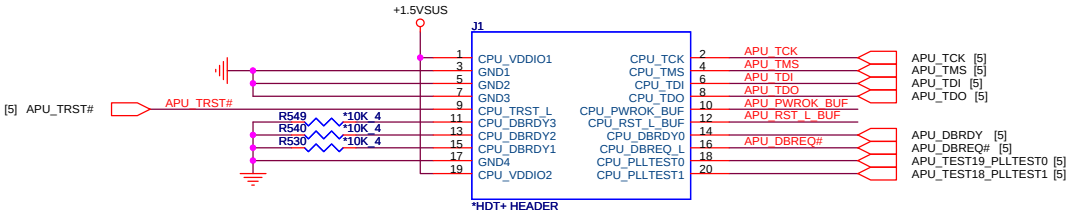
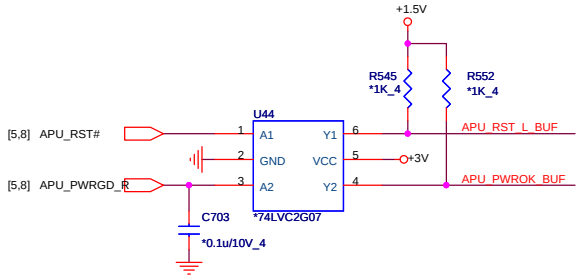


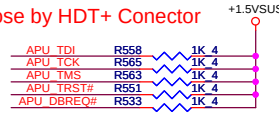
A10	AJ05757RT01
A8	AJ05557UT01
A6	AJ053578T01

HDT+ Connector for Debug only





Close by HDT+ Conector



Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
Size	Document Number: APU 1/4(PCIE/UMI/GPP/HDT)	Rev: A1A
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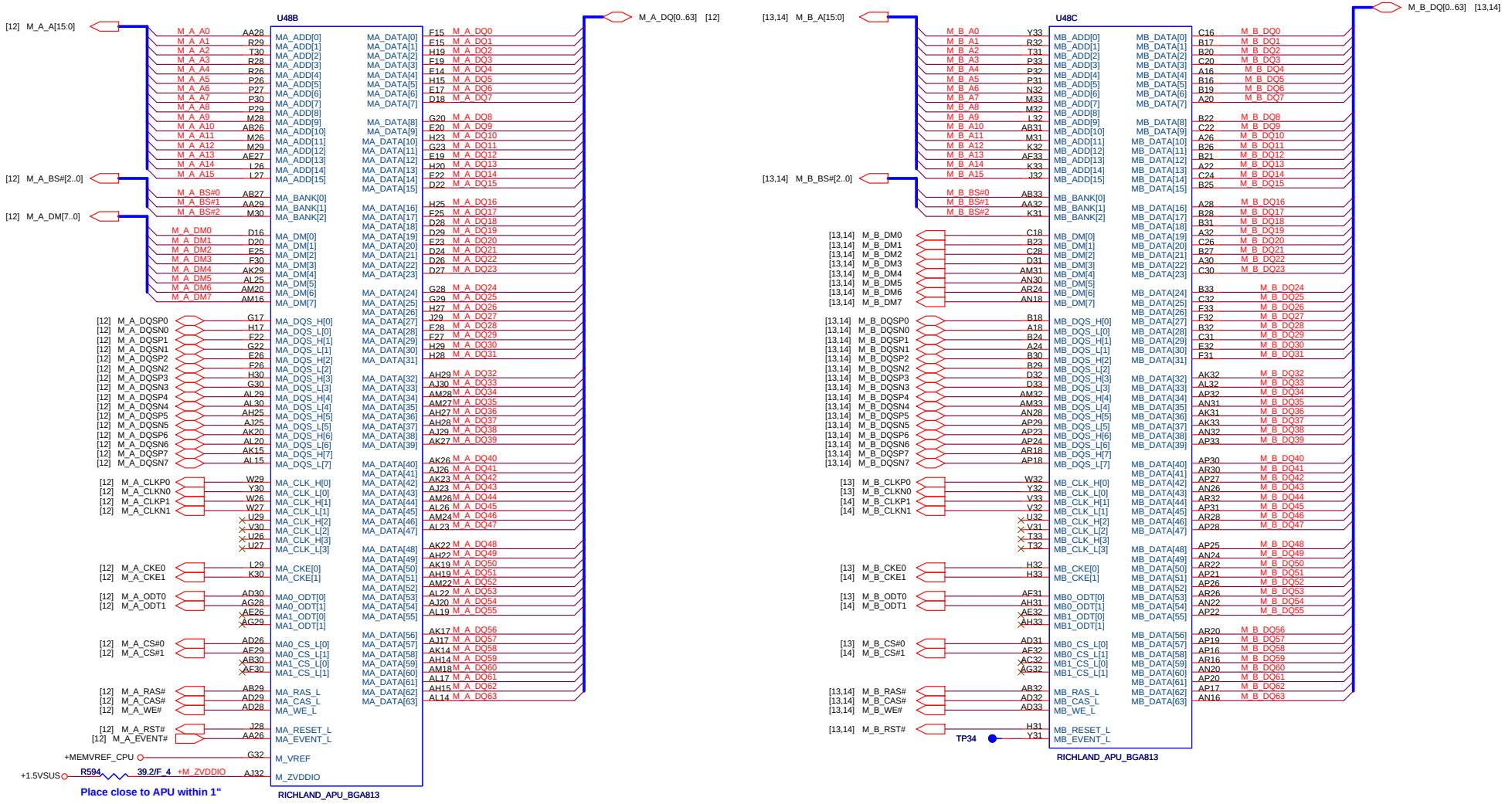
Soldermask openings for all bottom side vias/TPs under FS1



A10	AJ05757RT01
A8	AJ05557UT01
A6	AJ053578T01

Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	APU 2/4(DDR3 MEM I/F)	A1A

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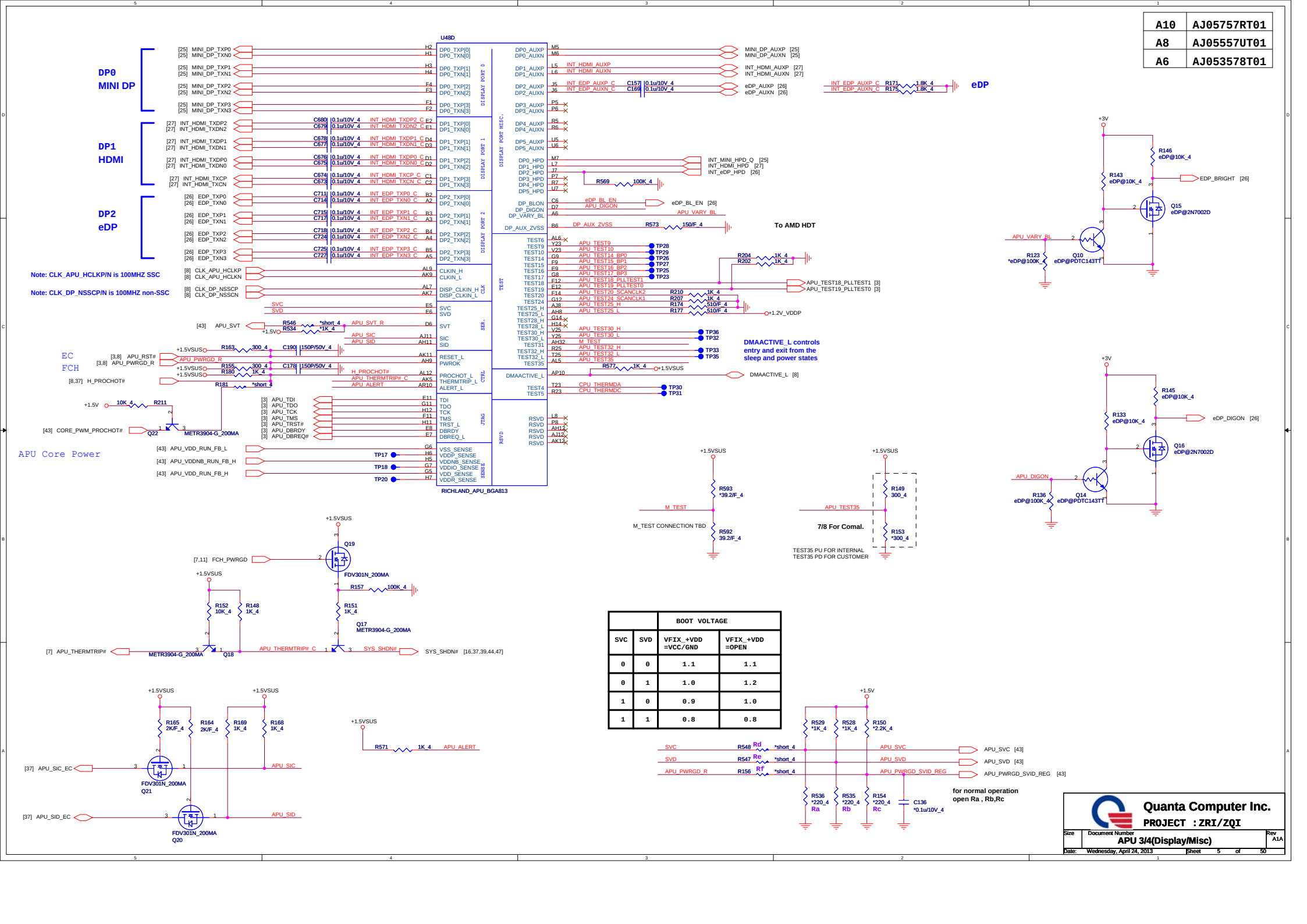
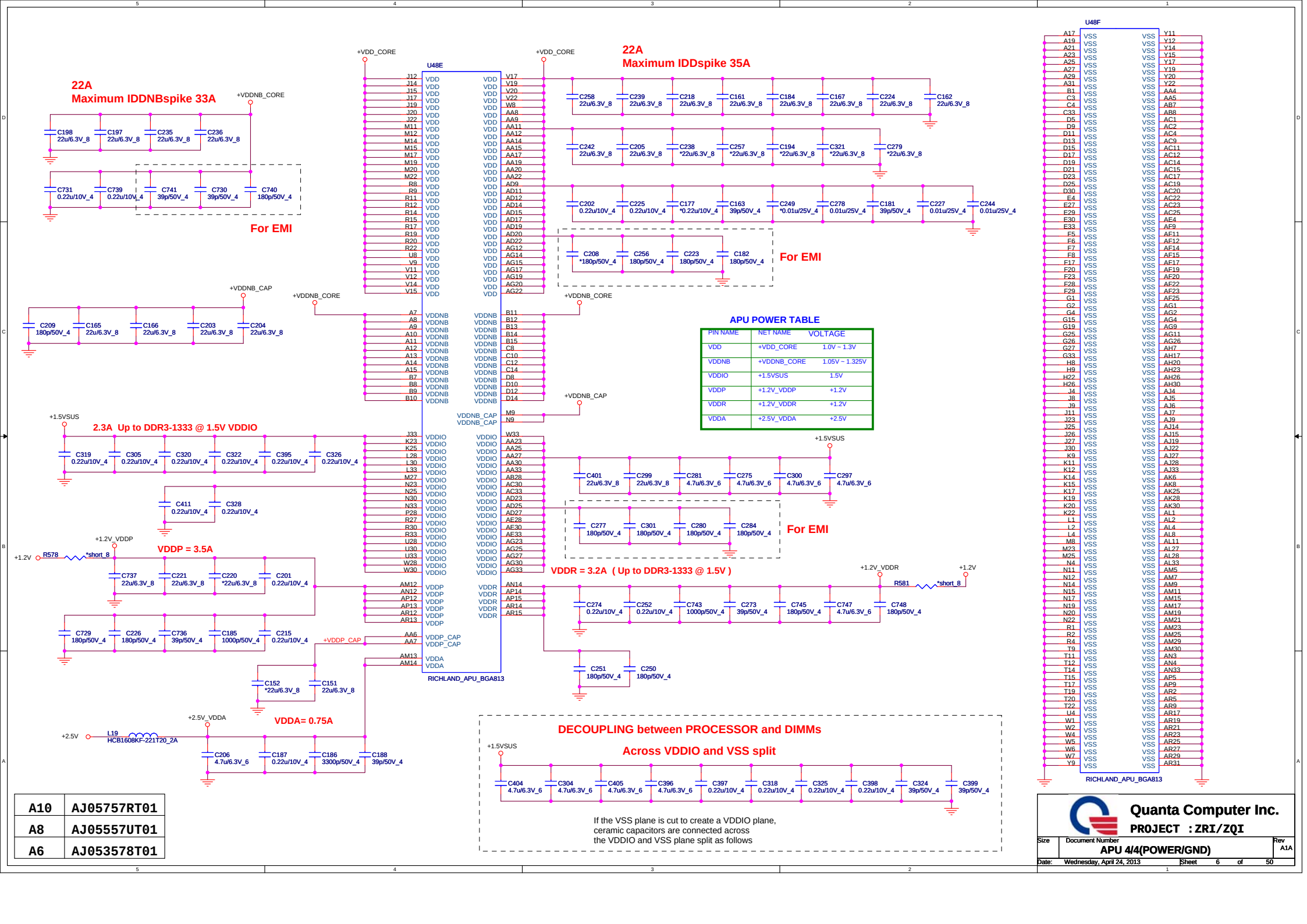
A10	AJ05757RT01
A8	AJ05557UT01
A6	AJ053578T01




22A
Maximum IDDNBspike 33A
+VDDNB_CORE
C198 22u/6.3V_8
C197 22u/6.3V_8
C235 22u/6.3V_8
C236 22u/6.3V_8
C731 0.22u/10V_4
C739 0.22u/10V_4
C741 39p/50V_4
C730 39p/50V_4
C740 180p/50V_4
For EMI
+VDDNB_CAP
C209 180p/50V_4
C165 22u/6.3V_8
C166 22u/6.3V_8
C203 22u/6.3V_8
C204 22u/6.3V_8
+VDD_CORE
U48E
+VDDNB_CORE
+VDDNB_CAP
+1.5VSUS
2.3A Up to DDR3-1333 @ 1.5V VDDIO
C319 0.22u/10V_4
C305 0.22u/10V_4
C320 0.22u/10V_4
C322 0.22u/10V_4
C395 0.22u/10V_4
C326 0.22u/10V_4
C411 0.22u/10V_4
C328 0.22u/10V_4
+1.2V_VDDP
+1.2V
R578 *short_8
VDDP = 3.5A
C737 22u/6.3V_8
C221 22u/6.3V_8
C220 *22u/6.3V_8
C201 0.22u/10V_4
C729 180p/50V_4
C226 180p/50V_4
C736 39p/50V_4
C185 1000p/50V_4
C215 0.22u/10V_4
+VDDP_CAP
C152 *22u/6.3V_8
C151 22u/6.3V_8
+2.5V_VDDA
+2.5V
L19 HCB1608KF-221T20_2A
VDDA= 0.75A
C206 4.7u/6.3V_6
C187 0.22u/10V_4
C186 3300p/50V_4
C188 39p/50V_4
RICHLAND_APU_BGA813
22A
Maximum IDDspike 35A
C258 22u/6.3V_8
C239 22u/6.3V_8
C218 22u/6.3V_8
C161 22u/6.3V_8
C184 22u/6.3V_8
C167 22u/6.3V_8
C224 22u/6.3V_8
C162 22u/6.3V_8
C242 22u/6.3V_8
C205 22u/6.3V_8
C238 *22u/6.3V_8
C257 *22u/6.3V_8
C194 *22u/6.3V_8
C321 *22u/6.3V_8
C279 *22u/6.3V_8
C202 0.22u/10V_4
C225 0.22u/10V_4
C177 *0.22u/10V_4
C163 39p/50V_4
C249 *0.01u/25V_4
C278 0.01u/25V_4
C181 39p/50V_4
C227 0.01u/25V_4
C244 0.01u/25V_4
C208 *180p/50V_4
C256 180p/50V_4
C223 180p/50V_4
C182 180p/50V_4
For EMI
APU POWER TABLE
PIN NAME | NET NAME | VOLTAGE
VDD | +VDD_CORE | 1.0V ~ 1.3V
VDDNB | +VDDNB_CORE | 1.05V ~ 1.325V
VDDIO | +1.5VSUS | 1.5V
VDDP | +1.2V_VDDP | +1.2V
VDDR | +1.2V_VDDR | +1.2V
VDDA | +2.5V_VDDA | +2.5V
C401 22u/6.3V_8
C299 22u/6.3V_8
C281 4.7u/6.3V_6
C275 4.7u/6.3V_6
C300 4.7u/6.3V_6
C297 4.7u/6.3V_6
C277 180p/50V_4
C301 180p/50V_4
C280 180p/50V_4
C284 180p/50V_4
For EMI
VDDR = 3.2A (Up to DDR3-1333 @ 1.5V)
+1.2V_VDDR
R581 *short_8
C274 0.22u/10V_4
C252 0.22u/10V_4
C743 1000p/50V_4
C273 39p/50V_4
C745 180p/50V_4
C747 4.7u/6.3V_6
C748 180p/50V_4
C251 180p/50V_4
C250 180p/50V_4
DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split
C404 4.7u/6.3V_6
C304 4.7u/6.3V_6
C405 4.7u/6.3V_6
C396 4.7u/6.3V_6
C397 0.22u/10V_4
C318 0.22u/10V_4
C325 0.22u/10V_4
C398 0.22u/10V_4
C324 39p/50V_4
C399 39p/50V_4
If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows
U48F
RICHLAND_APU_BGA813
A10 AJ05757RT01
A8 AJ05557UT01
A6 AJ053578T01
Quanta Computer Inc.
PROJECT : ZRI/ZQI
Size
Document Number
APU 4/4(POWER/GND)
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NC,no install by default

remove pull hi (chip internal have pull hi)

Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

GEVENT12# ~18# are +3V_S5

HDaudio interface are +3V_S5

GPIO193 ~196 are +3V_S5

To Azalia

HUDSON-M3
Part 4 of 5

BOLTON-M3

HUB3
MINI DP
USB2.0 co-lay USB3.0 port

HUB2
Touch Panel
WLAN
CCD on eDP

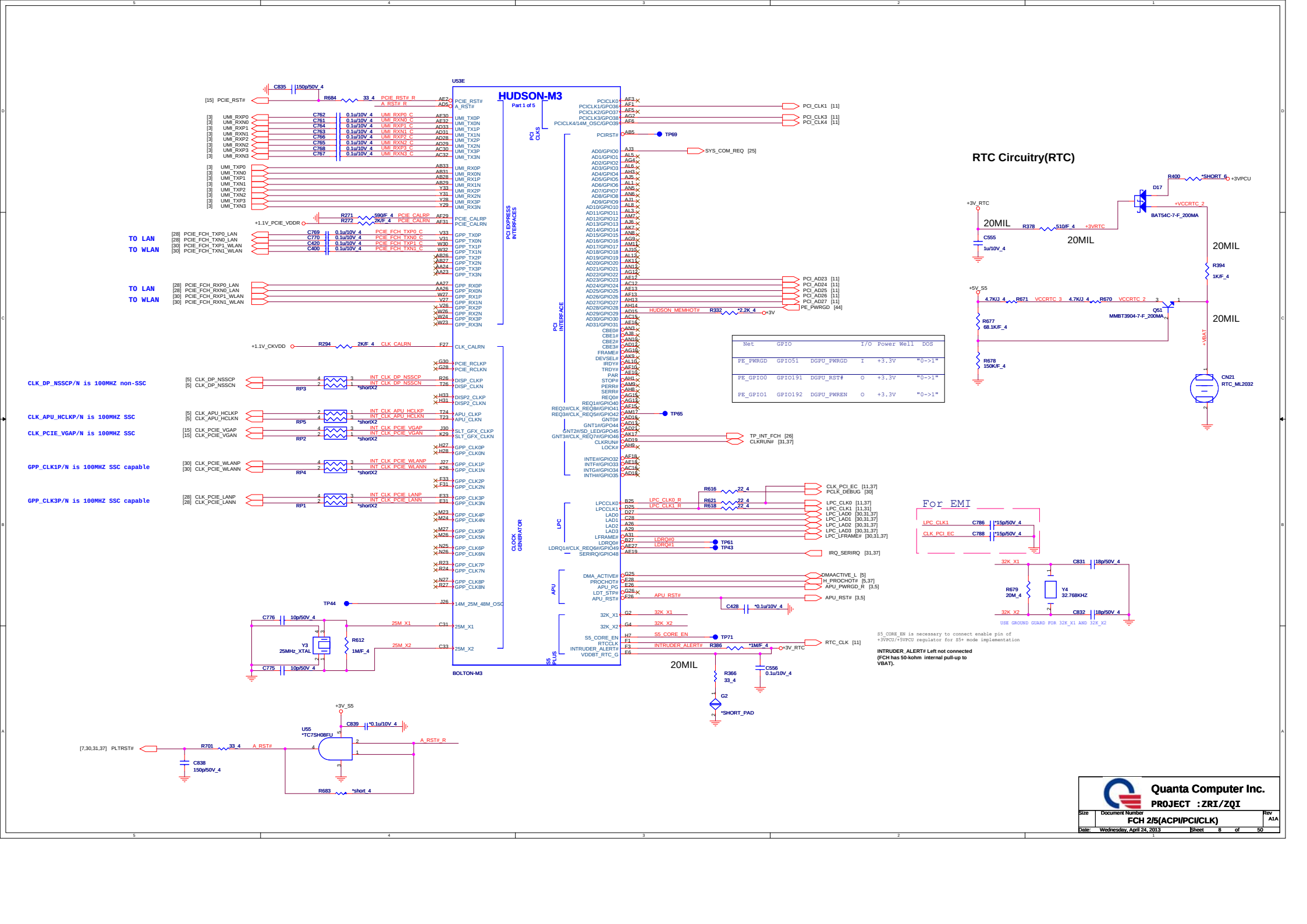
HUB1
USB2.0 D/B
USB2.0

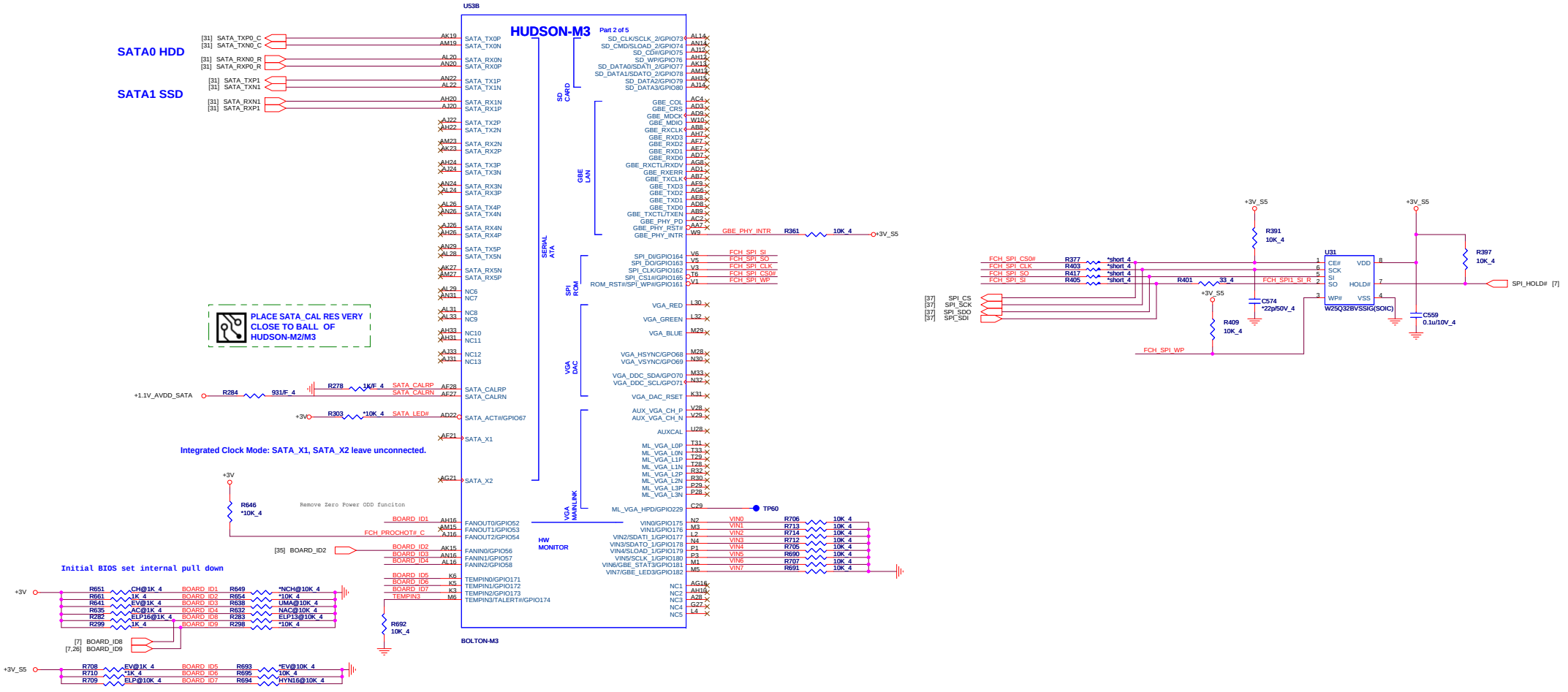
MINI DP
USB3.0

Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	FCH 1/5(GPIO/USB/AZ)	A1A

Date: Wednesday, April 24, 2013 Sheet 7 of 50


HUDSON-M3
Part 1 of 5
U53E
BOLTON-M3
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
S5 PLUS
PCI CLKS
TO LAN
TO WLAN
CLK_DP_NSSCP/N is 100MHZ non-SSC
CLK_APU_HCLKP/N is 100MHZ SSC
CLK_PCIE_VGAP/N is 100MHZ SSC
GPP_CLK1P/N is 100MHZ SSC capable
GPP_CLK3P/N is 100MHZ SSC capable
RTC Circuitry(RTC)
For EMI
Net GPIO I/O Power Well DOS
PE_PWRGD GPIO51 DGPU_PWRGD I +3.3V "0->1"
PE_GPIO0 GPIO191 DGPU_RST# O +3.3V "0->1"
PE_GPIO1 GPIO192 DGPU_PWREN O +3.3V "0->1"
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
Quanta Computer Inc.
PROJECT : ZRI/ZQI
FCH 2/5(ACPI/PCI/CLK)
Size Document Number Rev A1A
Date: Wednesday, April 24, 2013 Sheet 8 of 50



BOARD ID SETTING

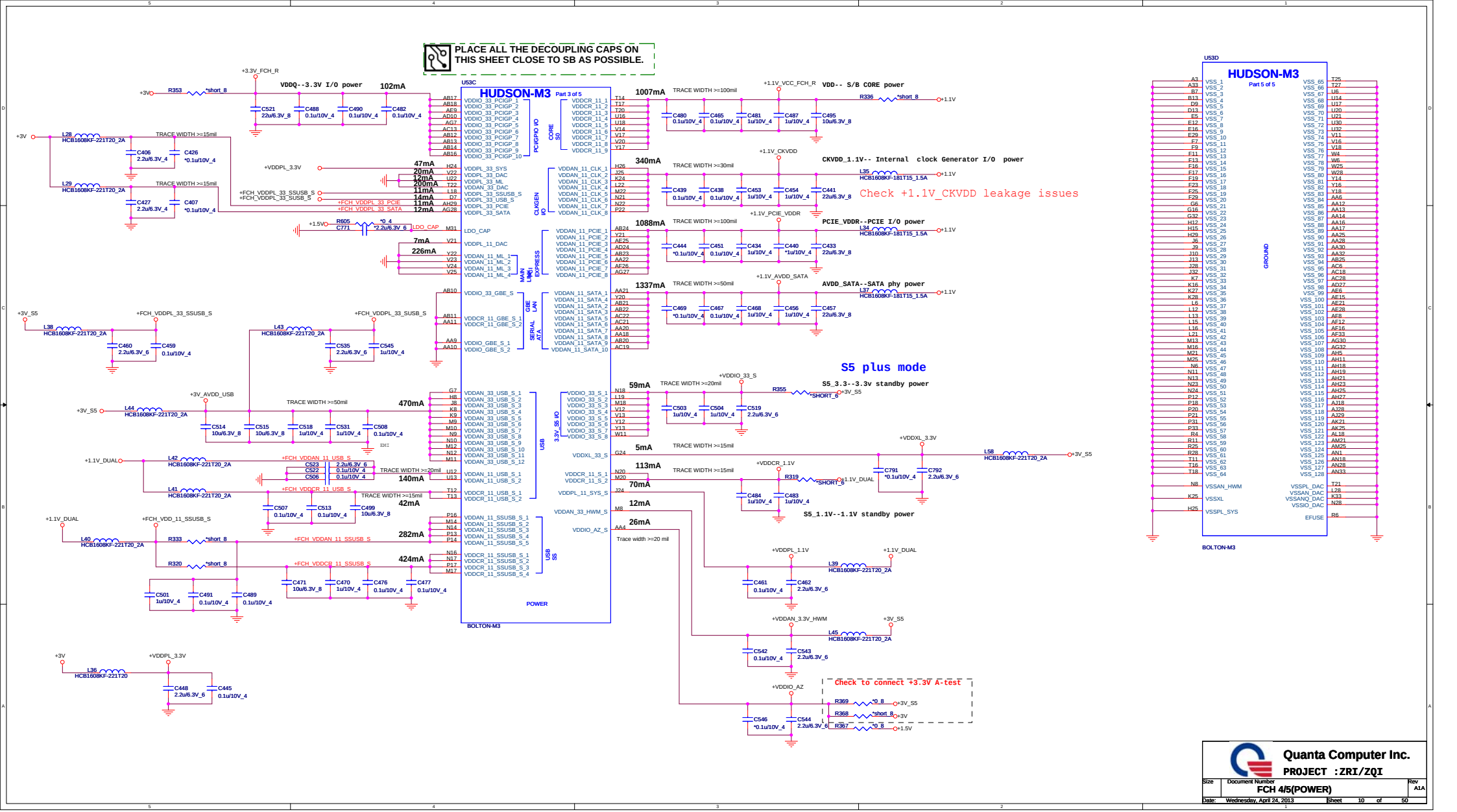
Board ID	ID1	ID2	ID3	ID4	ID5	ID9	
USB Charge No USB Charge	H L						
Reserved		H					
VGA SKU UMA SKU			H L				
AC No AC				H L			
VRAM 2G VRAM 4G					H L		
Non Touch Panel Touch Panel						H L	<= PD by cable

OnBorad RAM SETTING

ID6	ID7	ID8	
0	0	1	HYNIX DDR3L 1600 4GB H5TC4G63AFR-PBA
0	1	0	ELPIDA DDR3L 1333 4GB EDJ4216EBBG-DJ-F
0	1	1	ELPIDA DDR3L 1600 4GB EDJ4216EFBG-GNL-F
1	0	0	Disable OnBorad RAM

Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	FCH 3/5(SATA/VGA/GND/SPI)	A1A
Date: Wednesday, April 24, 2013	Sheet 9 of 50	


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
HUDSON-M3
Part 3 of 5
U53C
BOLTON-M3
POWER
VDDQ--3.3V I/O power
102mA
VDD-- S/B CORE power
1007mA
CKVDD_1.1V-- Internal clock Generator I/O power
340mA
Check +1.1V_CKVDD leakage issues
PCIE_VDDR--PCIE I/O power
1088mA
AVDD_SATA--SATA phy power
1337mA
S5 plus mode
S5_3.3--3.3v standby power
59mA
S5_1.1V--1.1V standby power
5mA
113mA
70mA
12mA
26mA
Check to connect +3.3V A-test
HUDSON-M3
Part 5 of 5
U53D
GROUND
BOLTON-M3
Quanta Computer Inc.
PROJECT :ZRI/ZQI
Size
Document Number
FCH 4/5(POWER)
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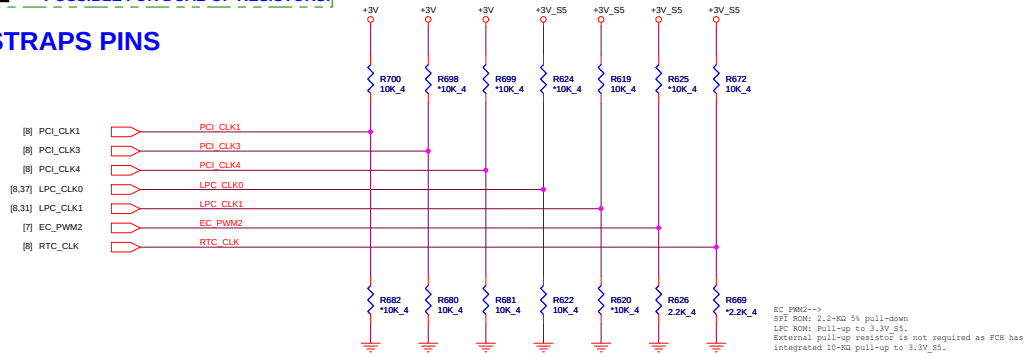
Date: Wednesday, April 24, 2013
Sheet 10 of 50

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

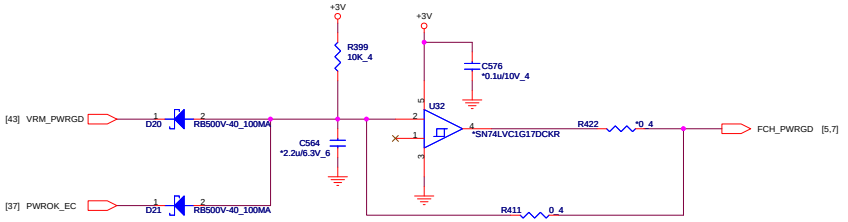


Remove PCI_CLK2 function

REQUIRED STRAPS

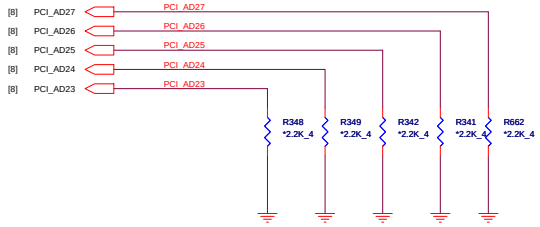
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

FCH PWRGD CKT



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	A1A
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DDR3 DIMM-A

+1.5VSUS [3,4,5,6,13,14,40,46]
+0.75V_DDR_VTT [13,14,40,47]
+3V [3,5,7,8,9,10,11,13,25,26,27,30,31,32,33,35,36,37,39,40,41,42,43,44,45,46,47]

CN11A

[4] M_A_A[15:0]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15

[4] M_A_BS#[2:0]
M_A_BS#0 M_A_BS#1 M_A_BS#2

[4] M_A_CS#0
[4] M_A_CS#1
[4] M_A_CLKP0
[4] M_A_CLKN0
[4] M_A_CLKP1
[4] M_A_CLKN1
[4] M_A_CKE0
[4] M_A_CKE1
[4] M_A_CAS#
[4] M_A_RAS#
[4] M_A_WE#
DIMM0_SA0
DIMM0_SA1
[7,13,25] PCLK_SMB
[7,13,25] PDAT_SMB

R238 10K_4
R241 10K_4

[4] M_A_ODT0
[4] M_A_ODT1
[4] M_A_DM[7:0]
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7

[4] M_A_DQSP[7:0]
M_A_DQSP0 M_A_DQSP1 M_A_DQSP2 M_A_DQSP3 M_A_DQSP4 M_A_DQSP5 M_A_DQSP6 M_A_DQSP7

[4] M_A_DQSN[7:0]
M_A_DQSN0 M_A_DQSN1 M_A_DQSN2 M_A_DQSN3 M_A_DQSN4 M_A_DQSN5 M_A_DQSN6 M_A_DQSN7

PC2100 DDR3 SDRAM SO-DIMM (204P)

M_A_DQ[63:0] [4]
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63

DDR3-DIMMA_H=5.2_STD

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

CN11B

+1.5VSUS
+3V R602 *short_8 +3V_JM9000
R268 1K_4
[4] M_A_EVENT#
[4] M_A_RST#
+DDR_VREF2
+DDR_VREF
C368 0.1u/10V_4
C364 1000p/50V_4
C387 0.1u/10V_4
C386 1000p/50V_4

PC2100 DDR3 SDRAM SO-DIMM (204P)

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VDDSPD
NC1 NC2 NCTEST
EVENT# RESET#
VREF_DQ VREF_CA
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15
VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52
VTT1 VTT2
GND GND

DDR3-DIMMA_H=5.2_STD

600mA
+0.75V_DDR_VTT_A
C388 4.7u/6.3V_6
C371 4.7u/6.3V_6
C367 0.1u/10V_4
R269 *short_8
+0.75V_DDR_VTT

Place these Caps near So-Dimm A

+1.5VSUS
C346 0.1u/10V_4
C376 0.1u/10V_4
C350 0.1u/10V_4
C349 0.1u/10V_4
C384 0.1u/10V_4

+1.5VSUS
C380 4.7u/6.3V_6
C345 4.7u/6.3V_6
C385 2.2u/6.3V_6
C351 2.2u/6.3V_6
C355 1u/6.3V_4
C377 1u/6.3V_4
C352 1u/6.3V_4

+1.5VSUS
C348 0.1u/10V_4
C381 0.1u/10V_4
C379 0.1u/10V_4
C383 0.1u/10V_4
C353 0.1u/10V_4

+1.5VSUS
C347 0.1u/10V_4
C378 180P/50V_4
C382 0.1u/10V_4
C354 0.1u/10V_4

+1.5VSUS
R266 1K/F_4
+SMDDR_VREF
R267 *0_6
3mA
+DDR_VREF
R265 1K/F_4

+1.5VSUS
R258 1K/F_4
R263 *0_6
3mA
+DDR_VREF2
R257 1K/F_4

Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	DDR3 SO-DIMM A	A1A
Date: Wednesday, April 24, 2013	Sheet 12 of 50	

<DDR>

BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63

[4,14] M_B_DQSP[7:0]
[4,14] M_B_DQSN[7:0]
[4,14] M_B_DQ[63:0]
[14] +SMDDR_VREF_DIMM
[14] SMDDR_VREF_DQ1

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

U24 U25 U26 U27 — 100-BALL SDRAM DDR3 — RAM_DDR3

Should be 243 Ohms +-1%

R357 243/F_4
R321 243/F_4
R273 243/F_4
R329 243/F_4

1333	AKD5JGST400
1600	AKD5JGST407

U54 — *M24C02-WMN6TP — address:A2

WP =1 : WRITE DISABLE

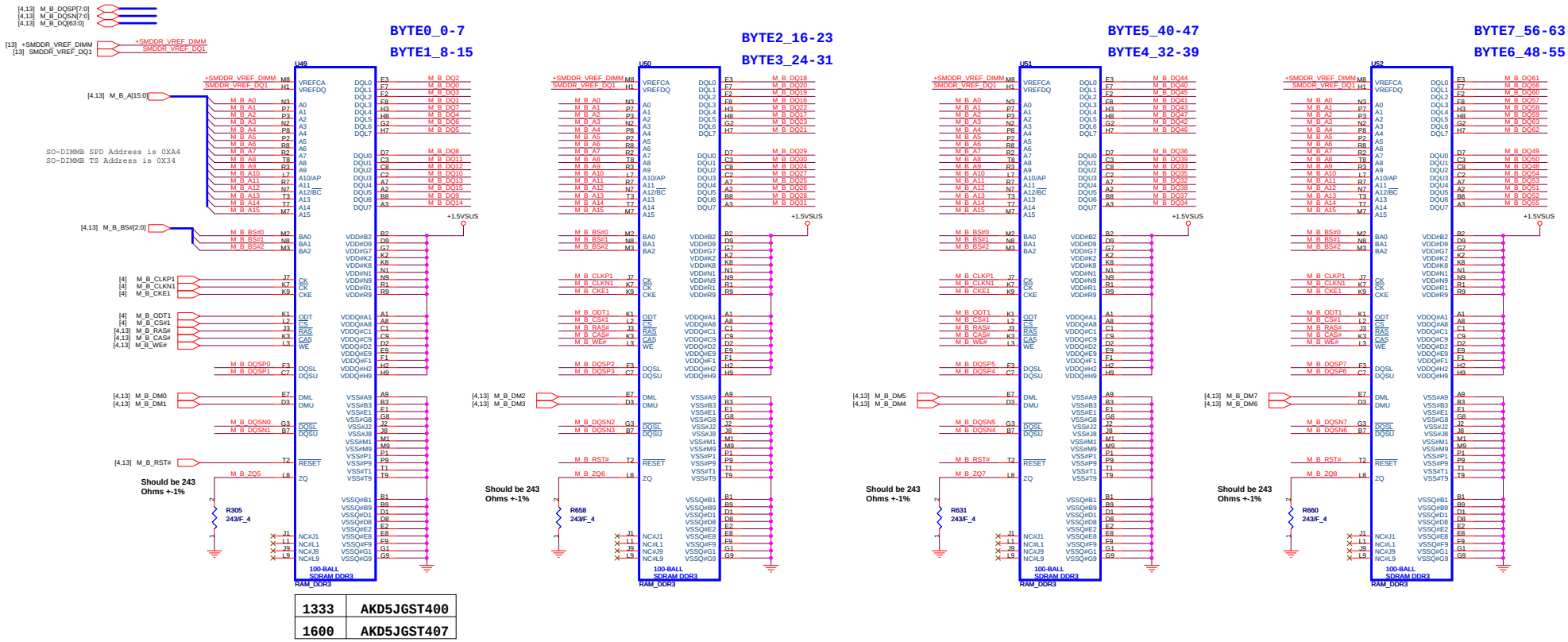
Place these Caps near Memory Down

C540 C541 C413 C412 C536 C410 0.22u/10V_4
C502 C512 C520 C524 C533 0.22u/10V_4
C529 C415 C414 C538 C409 C528 0.22u/10V_4
C547 C553 C548 C549 C550 0.22u/10V_4
C530 C526 C539 C417 C416 C525 0.22u/10V_4

R322 1K/F_4
R657 1K/F_4
R312 *0_6
C805 C794 C807 C479 0.1u/10V_4
R629 1K/F_4
R358 1K/F_4
R310 *0_6
C446 C464 C534 C450 0.1u/10V_4

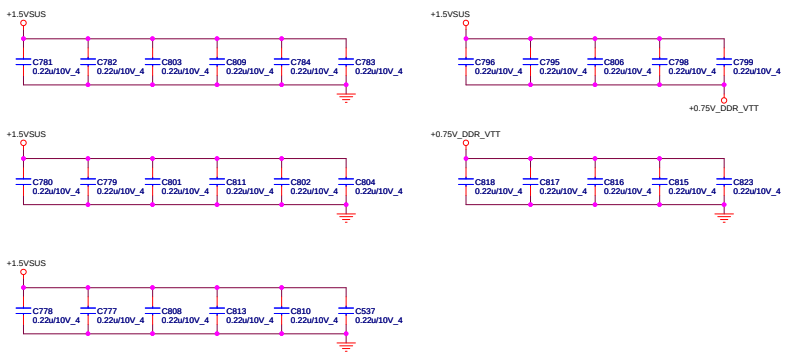
R309 R311 36/F_4
C455 0.1u/10V_4

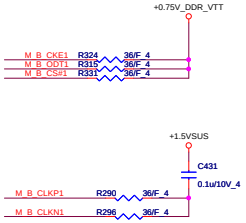
Quanta Computer Inc.
PROJECT : ZRI/ZQI
Size | Document Number: DDR3 MEMORY DOWNx16 B-1 | Rev: A1A
Date: Wednesday, April 24, 2013 | Sheet 13 of 50



1333	AKD5JGST400
1600	AKD5JGST407

Place these Caps near Memory Down

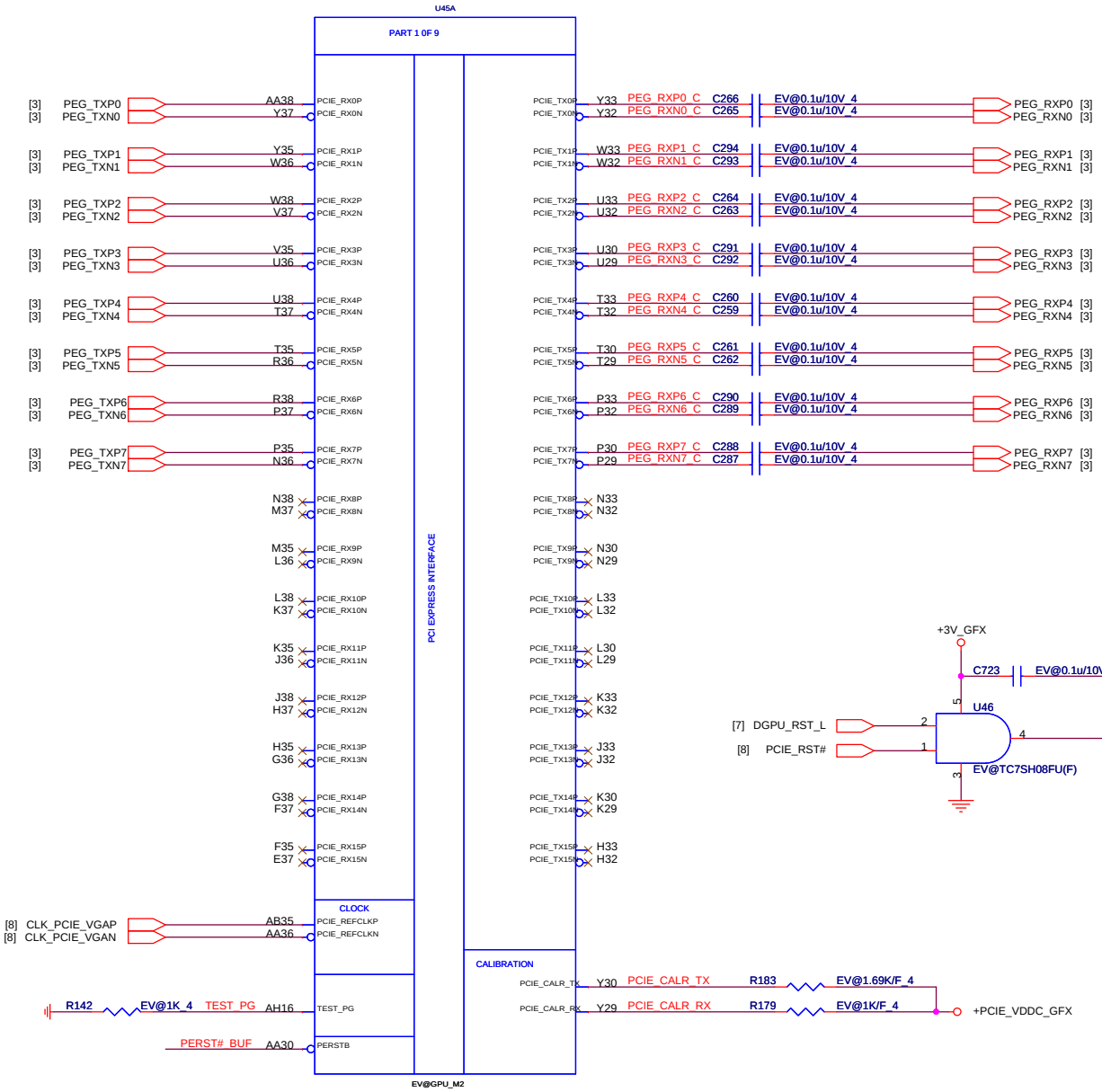




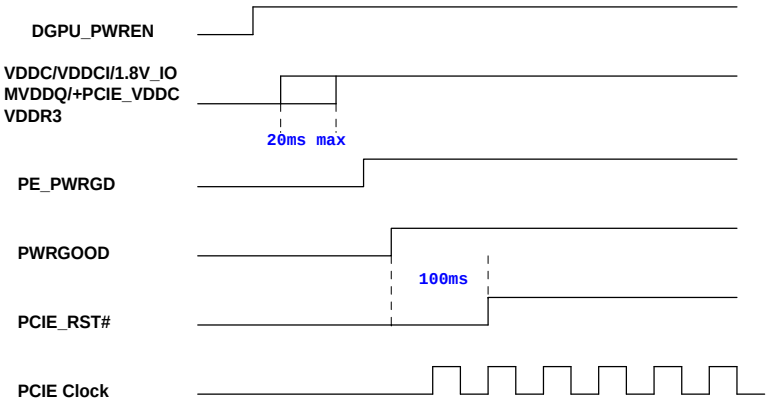
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	DDR3 MEMORY DOWNx16 B-2	A1A

Date: Wednesday, April 24, 2013 Sheet 14 of 50



Thames(Pro,XT) and Mars Power-on sequence PX5.0(no BACO)

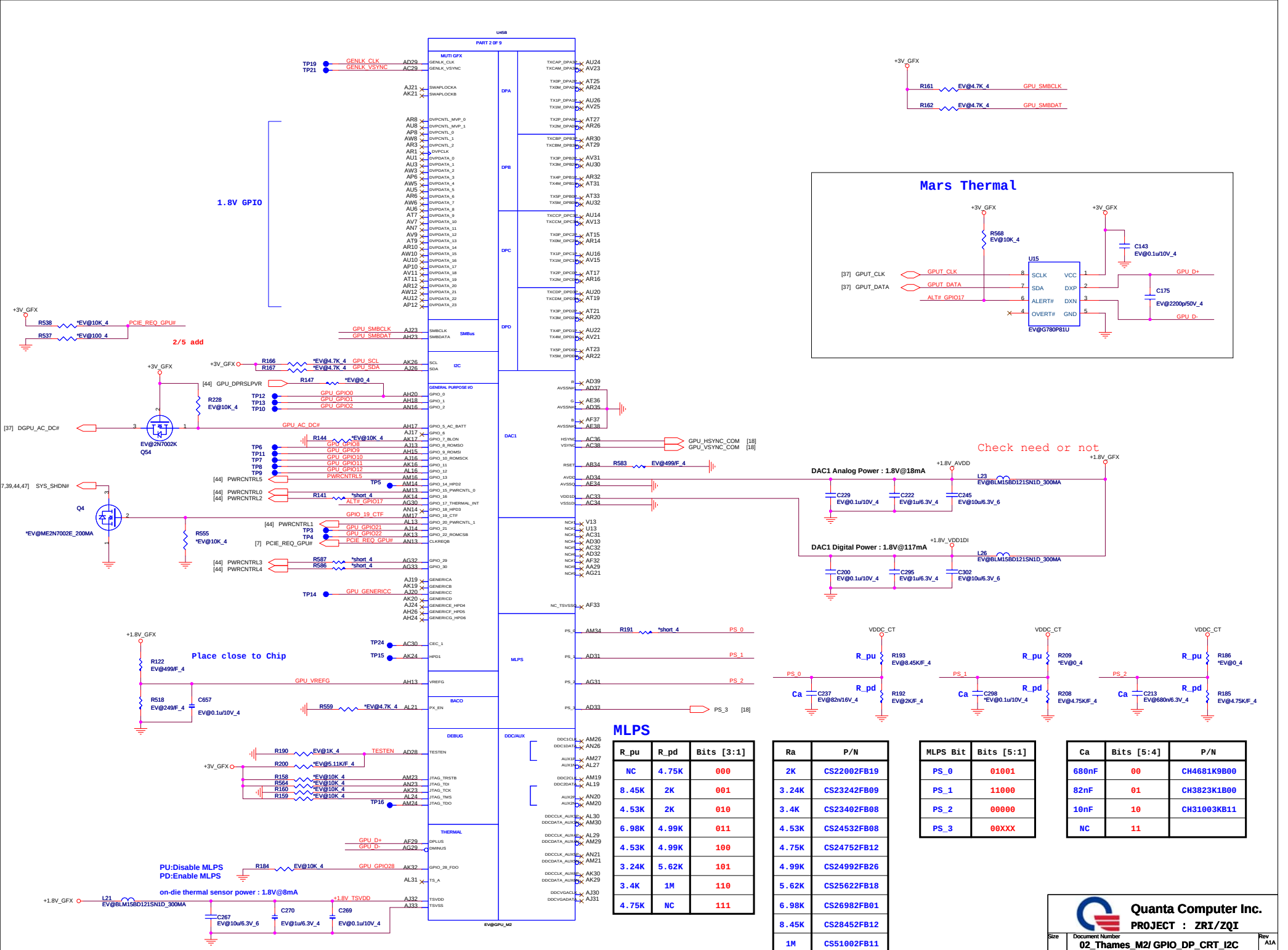


Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames_M2/ PEG*16	A1A

Date: Wednesday, April 24, 2013 Sheet 15 of 50



MLPS

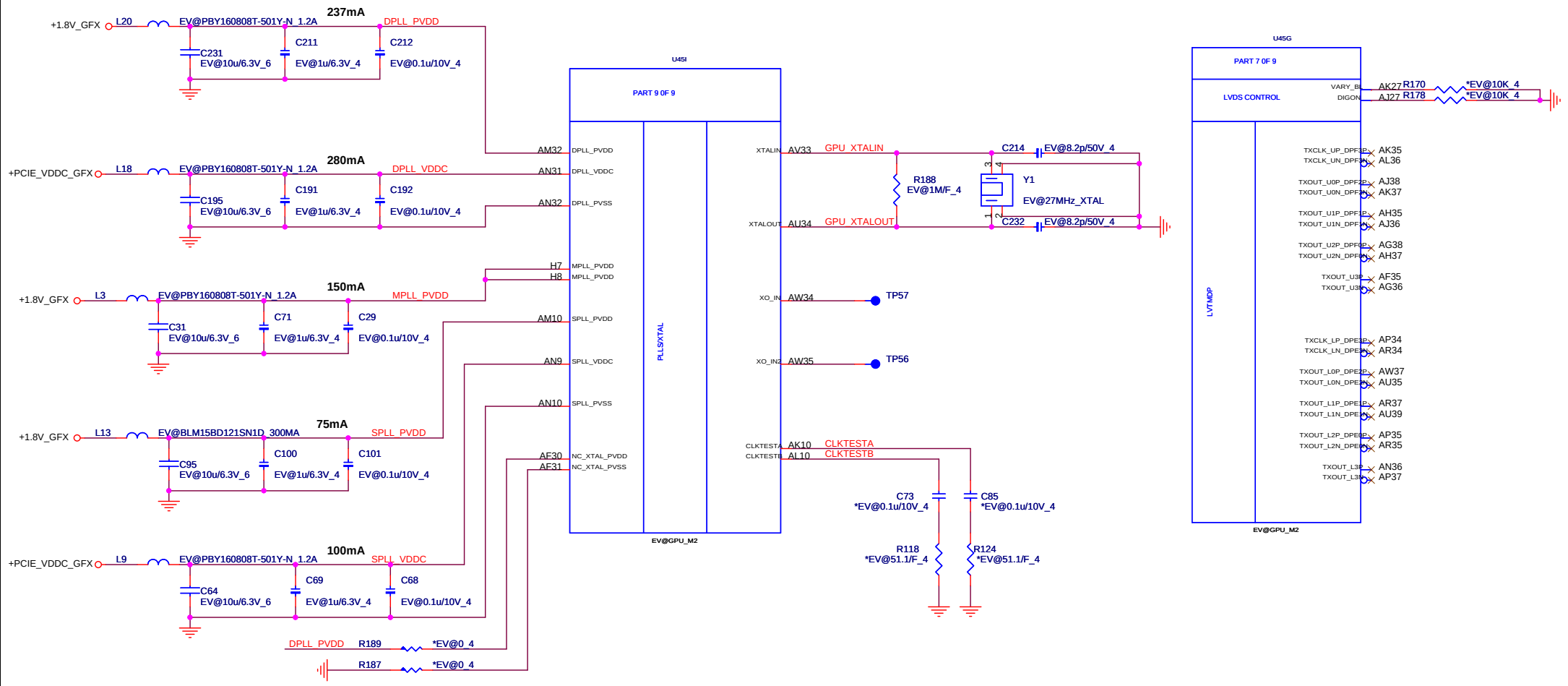
R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

MLPS Bit	Bits [5:1]
PS_0	01001
PS_1	11000
PS_2	00000
PS_3	00XXX

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

Quanta Computer Inc.
PROJECT : ZRI/ZQI
Size | Document Number: 02_Thames_M2/ GPIO_DP_CRT_I2C | Rev: A1A
Date: Wednesday, April 24, 2013 | Sheet 16 of 50



Quanta Computer Inc.

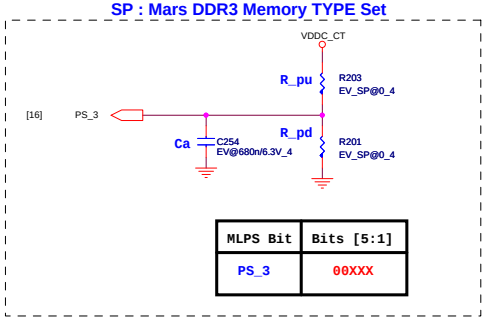
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames_M2/ XTAL_LVDS	A1A
Date: Wednesday, April 24, 2013	Sheet 17 of 50	

Vendor	Vendor P/N	STN B/S P/N	Size	Mars USE MLPS
Hynix	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW17 * 8	2GB	000
	H5TC2G63FFR-11C (128M*16)	AKD5MZDTW05 * 8	2GB	001
Micron	MT41K256M16HA-107G (256M*16)	AKD5PGSTL05 * 8	4GB	011

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

SP : Mars DDR3 Memory TYPE Set



MLPS Bit	Bits [5:1]
PS_3	00XXX

MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	D 000
8.45K	2K	F 001
4.53K	2K	B 010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

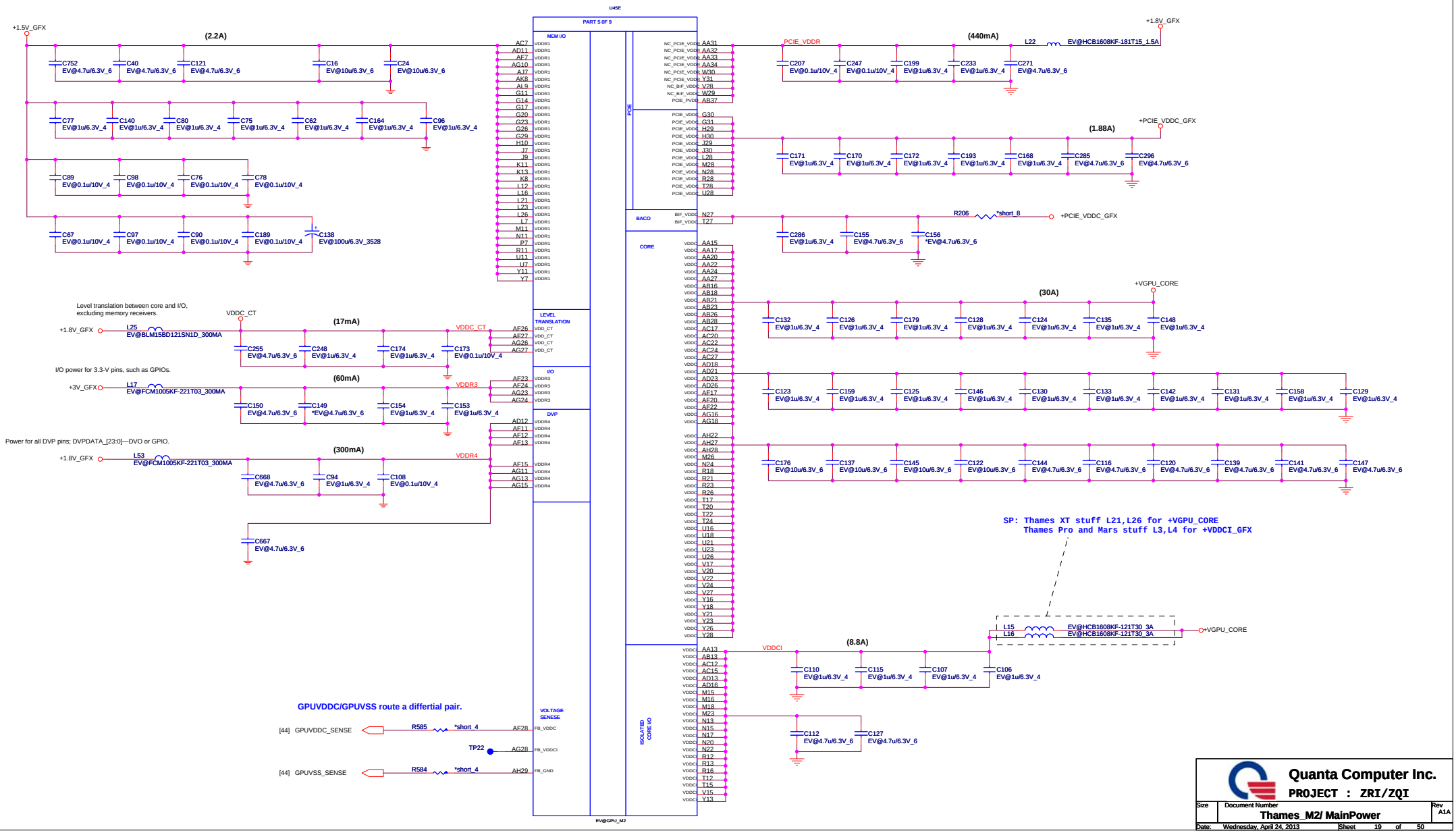
System Memory Aperture size

GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	32M	1	1	0

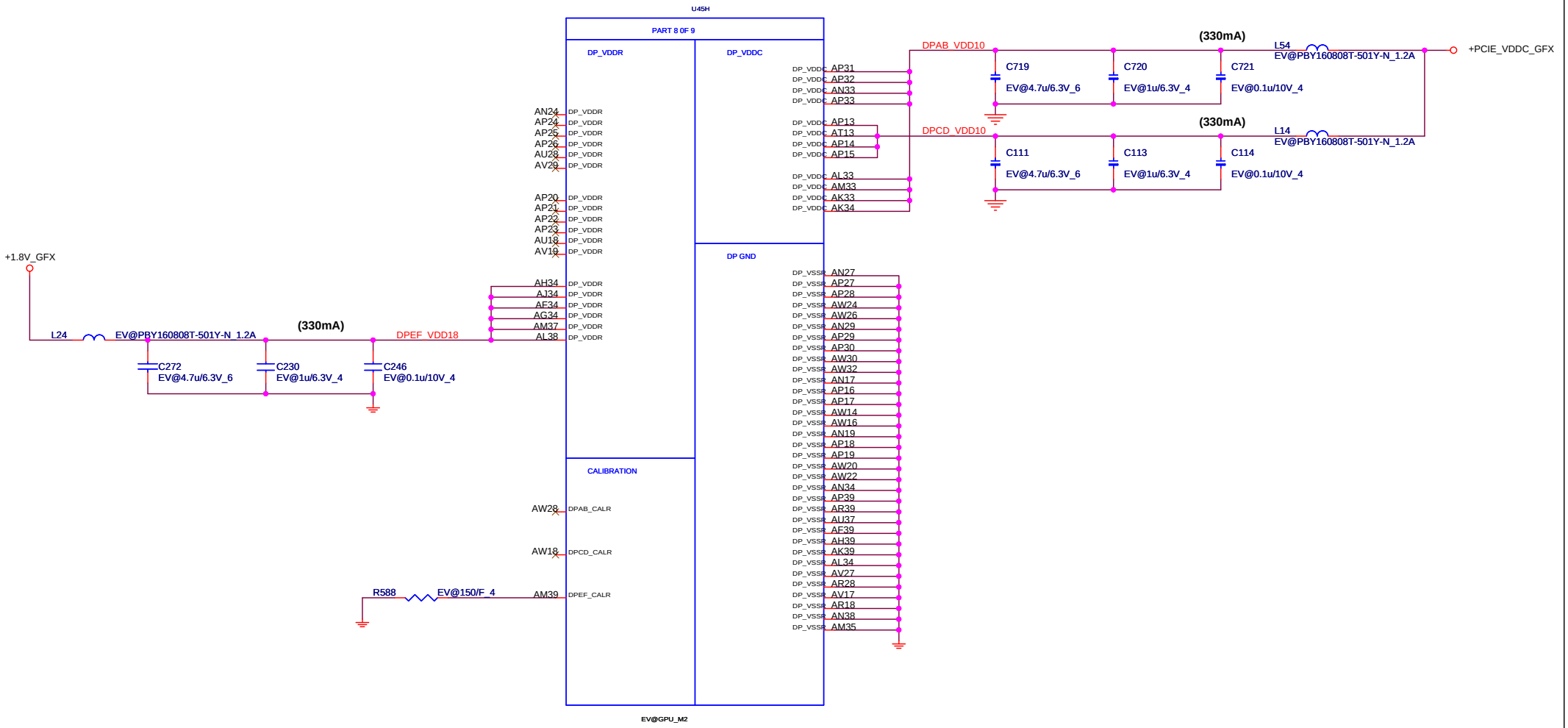


Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames_M2/ STRAPS_Thermal	A1A
Date: Wednesday, April 24, 2013	Sheet 18 of 50	

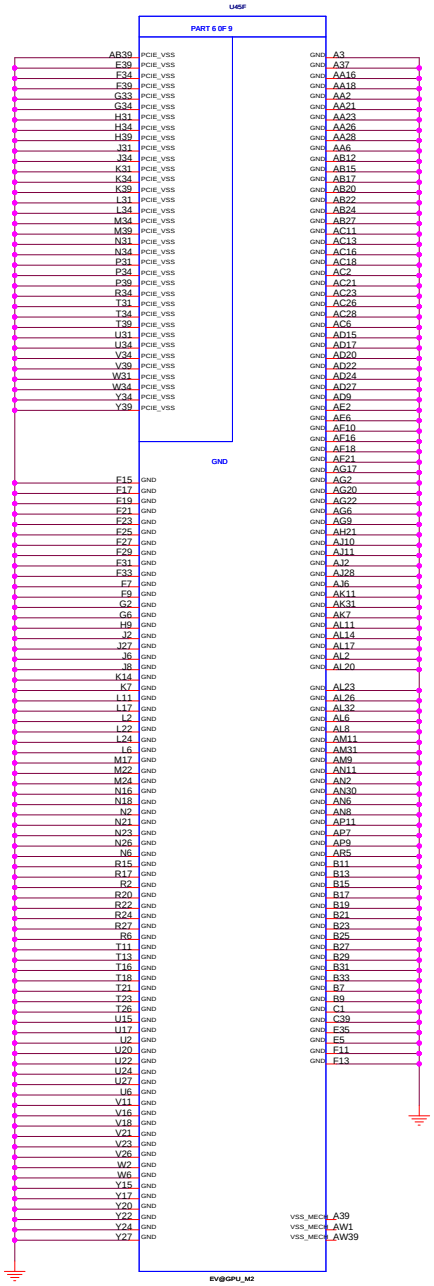


Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
Size	Document Number: Thames_M2/ MainPower	Rev: A1A
Date: Wednesday, April 24, 2013	Sheet 19 of 50	



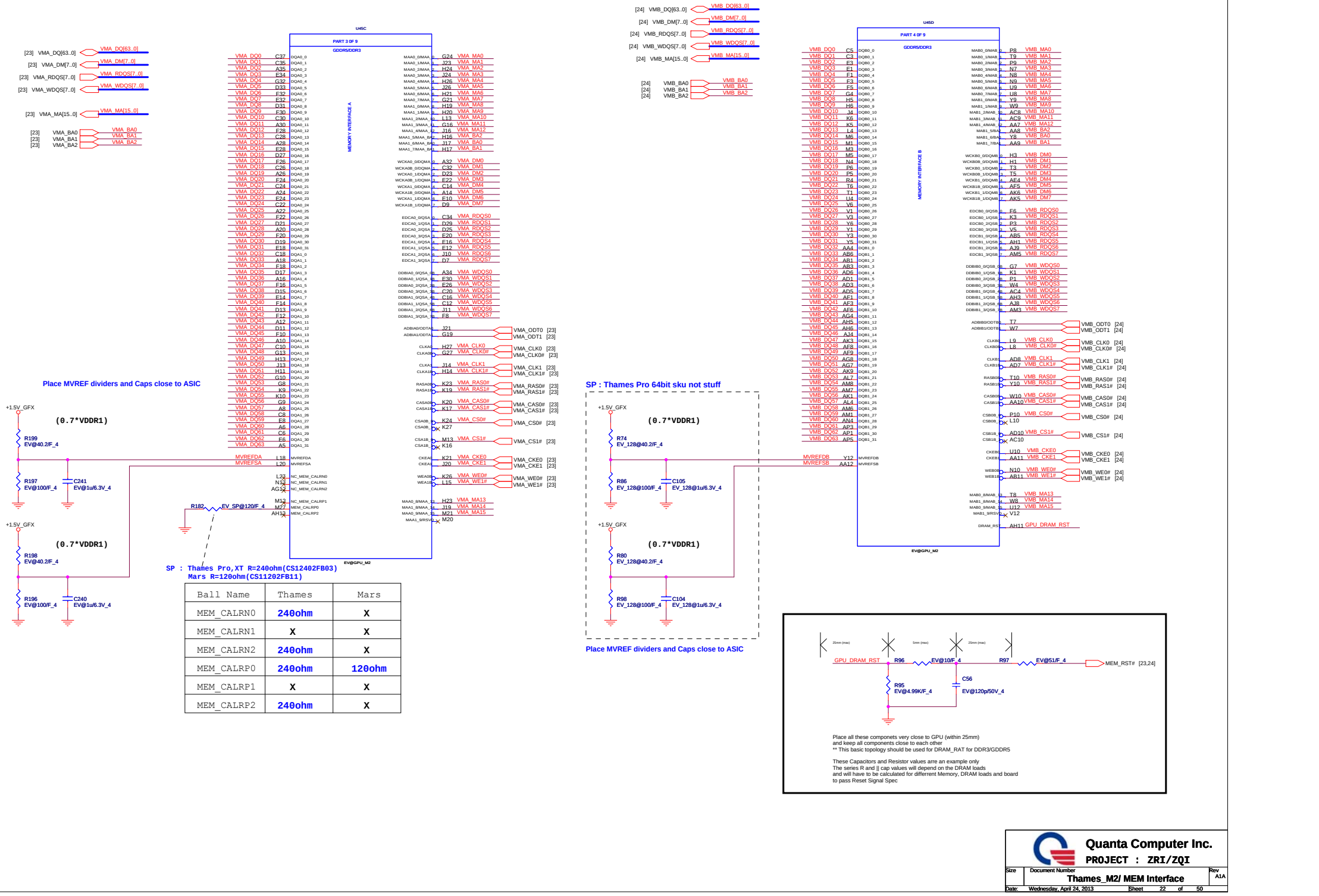
Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
Size	Document Number: Thames_M2/ DP_Powers	Rev: A1A
Date: Wednesday, April 24, 2013	Sheet 20 of 50	

<VGA>



Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
Size	Document Number: Thames_M2/ GND	Rev: A1A
Date: Wednesday, April 24, 2013	Sheet 21 of 50	

<VGA>

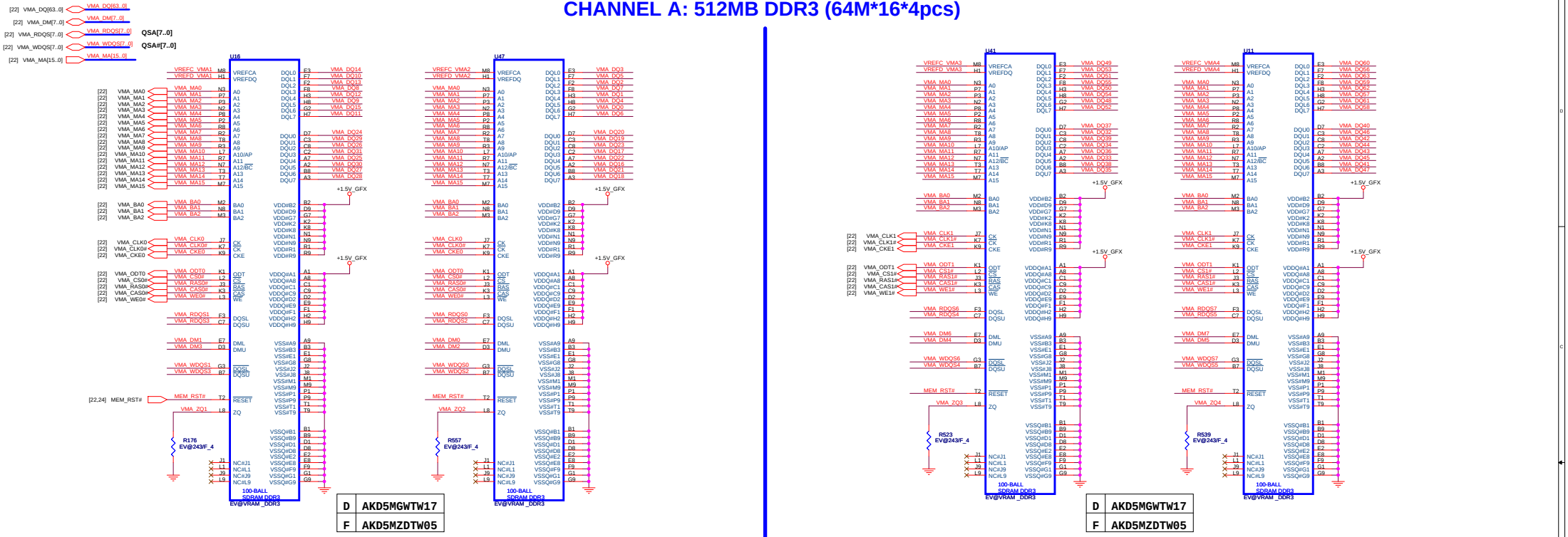


Ball Name	Thames	Mars
MEM_CALRN0	240ohm	X
MEM_CALRN1	X	X
MEM_CALRN2	240ohm	X
MEM_CALRP0	240ohm	120ohm
MEM_CALRP1	X	X
MEM_CALRP2	240ohm	X

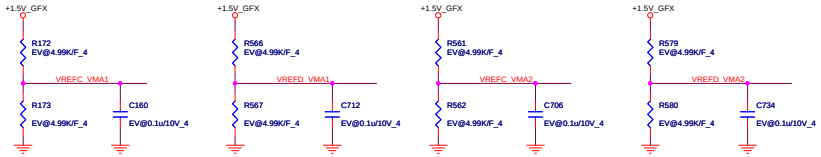
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames_M2/ MEM Interface	A1A
Date: Wednesday, April 24, 2013	Sheet 22 of 50	

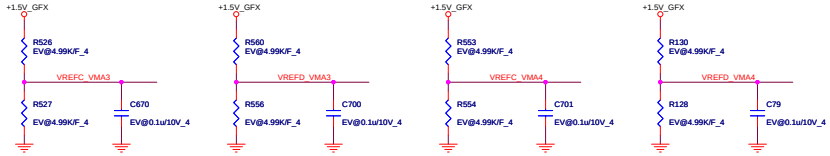
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



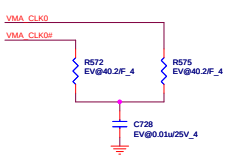
Group-A0 VREF



Group-A1 VREF

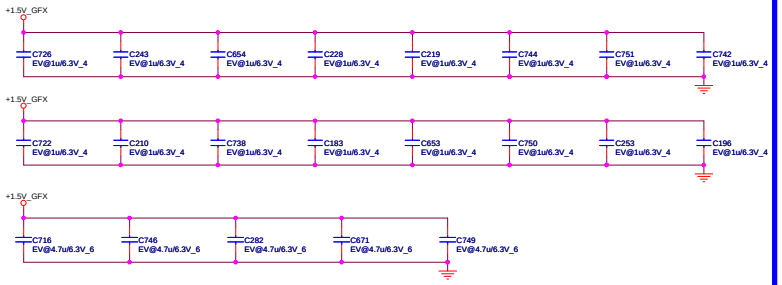


MEM_A0 CLK

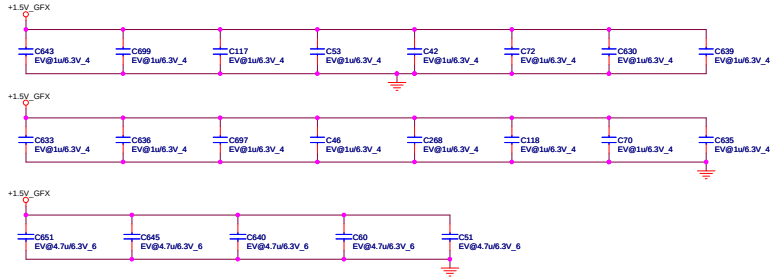


EV_SP@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

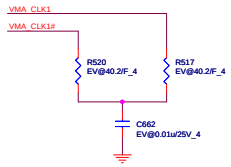
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



EV_SP@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

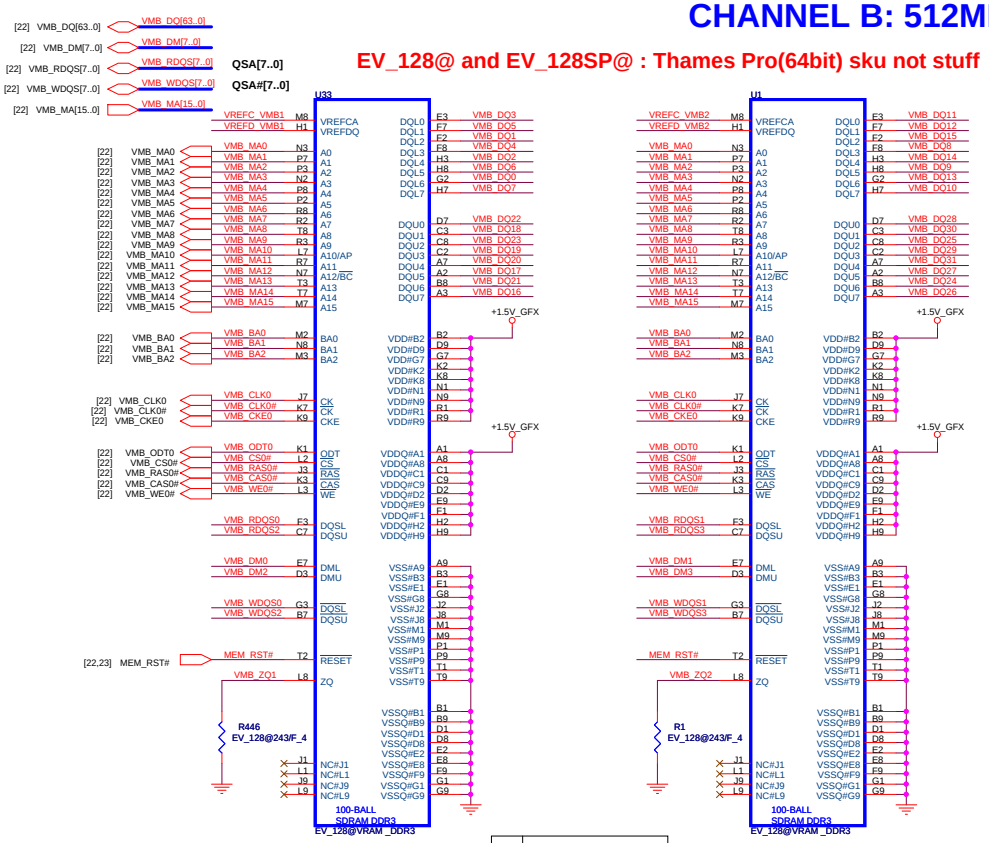
Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Thames_M2/VRAM_A	A1A

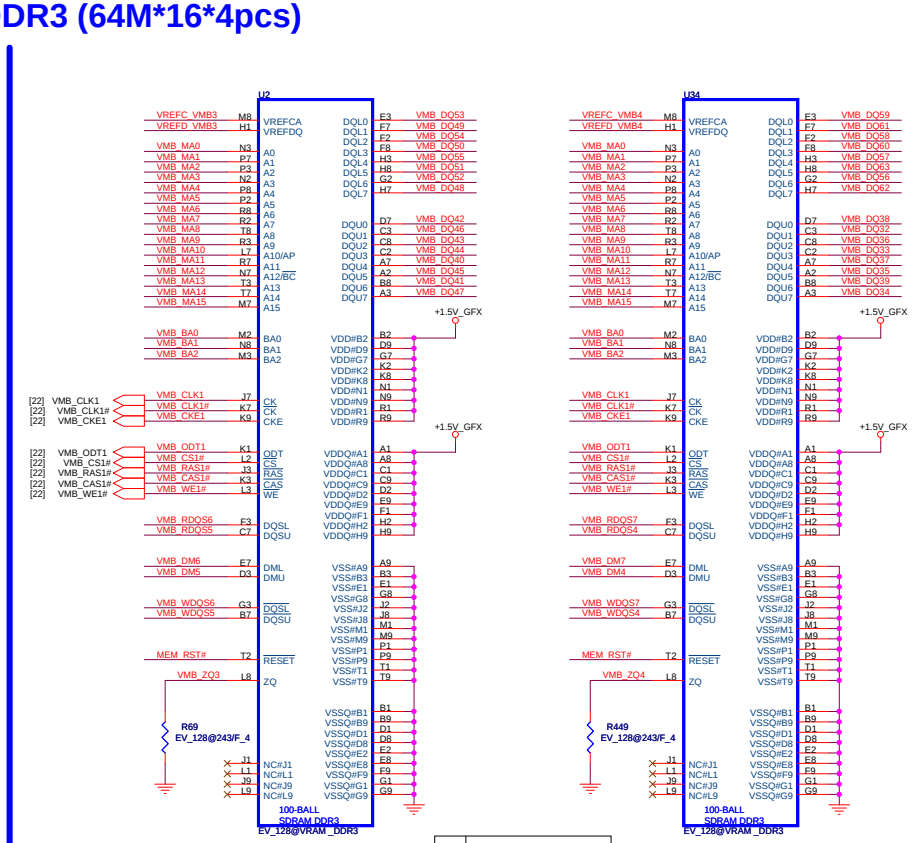
Date: Wednesday, April 24, 2013 Sheet 23 of 50

CHANNEL B: 512MB DDR3 (64M*16*4pcs)

EV_128@ and EV_128SP@ : Thames Pro(64bit) sku not stuff

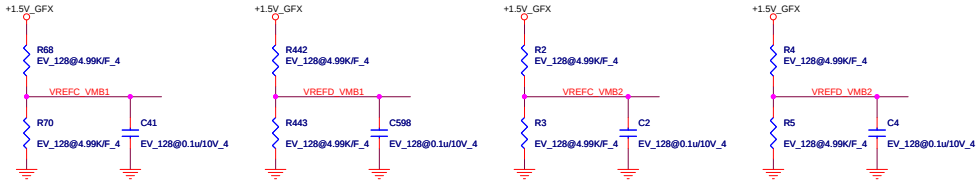


D	AKD5MGWTW17
F	AKD5MZDTW05

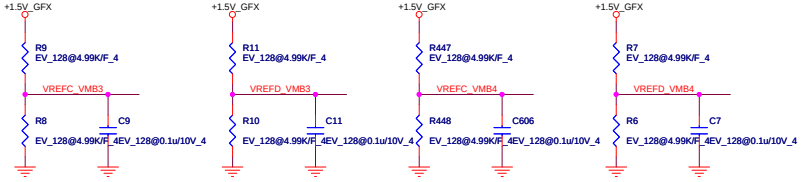


D	AKD5MGWTW17
F	AKD5MZDTW05

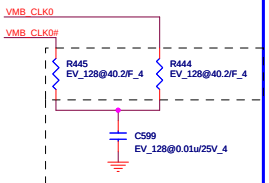
Group-B0 VREF



Group-B1 VREF

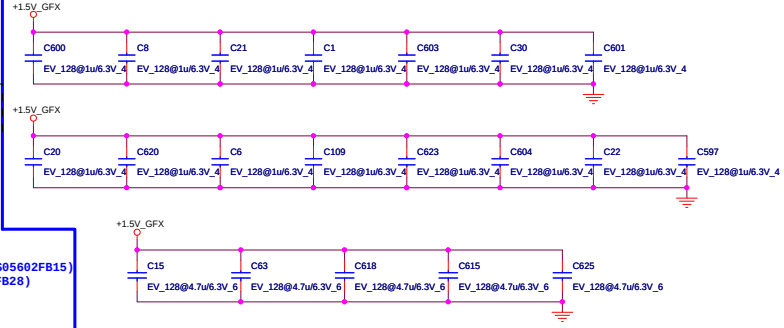


MEM_B0 CLK

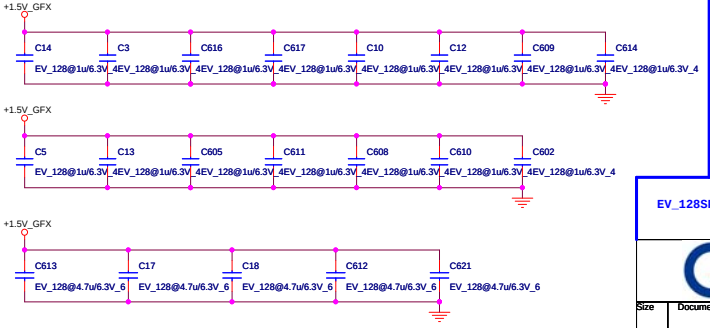


EV_128SP@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

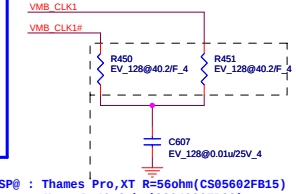
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK

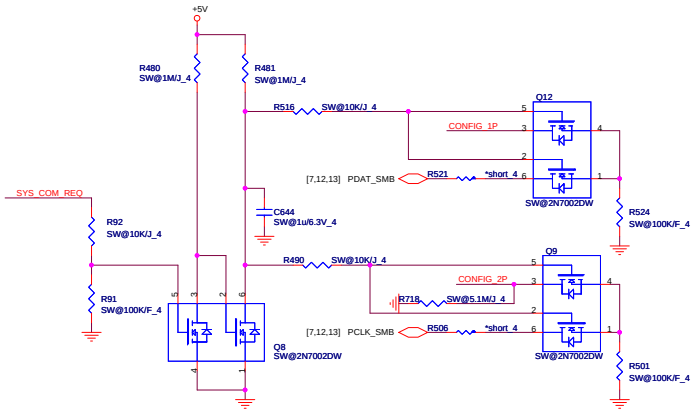


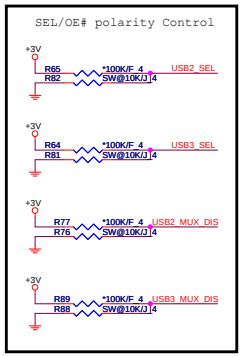
EV_128SP@ : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

Quanta Computer Inc.
PROJECT : ZRI/ZQI

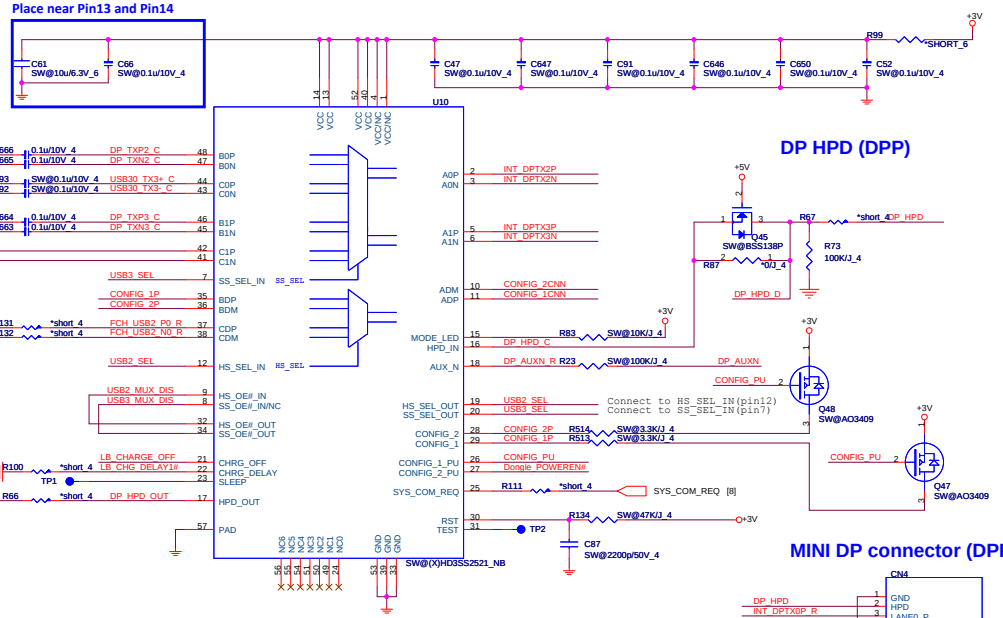
Size	Document Number	Rev
	Thames_M2/VRAM_B	A1A
Date: Wednesday, April 24, 2013	Sheet 24 of 50	

mini DP ML (DPP)



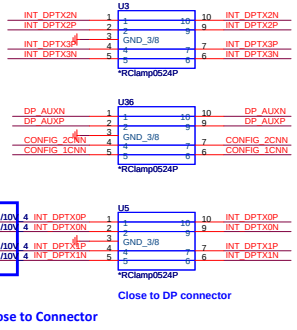


Layout Notes:
Place near Pin13 and Pin14



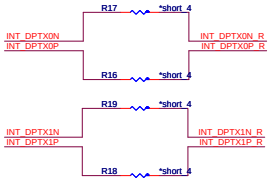
DP HPD (DPP)

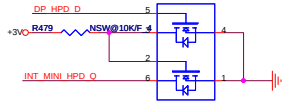
ESD Protect (EMC)

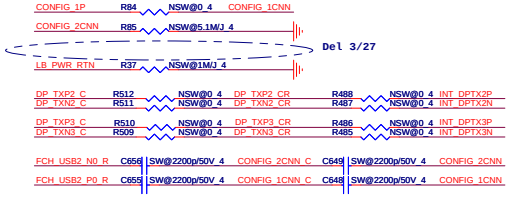


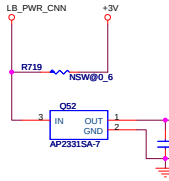
Layout Notes:
Place decoupling CAPs close to Connector

Close to DP connector

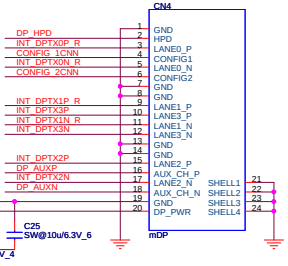




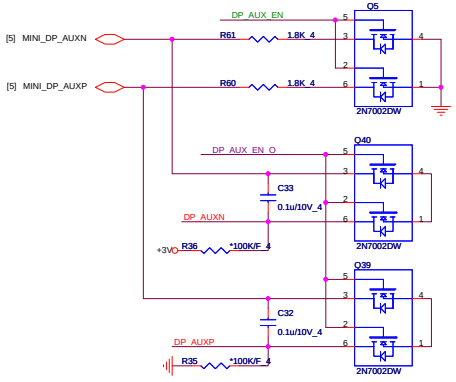


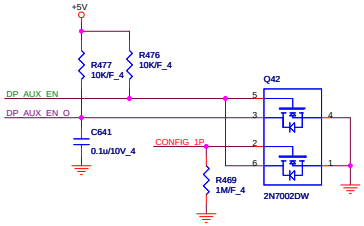


MINI DP connector (DPP)

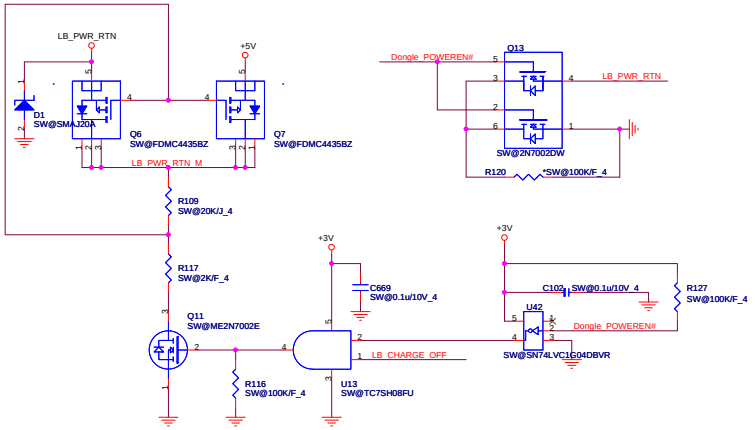


mDP AUX (DPP)





DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)



Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Mini DP	A1A
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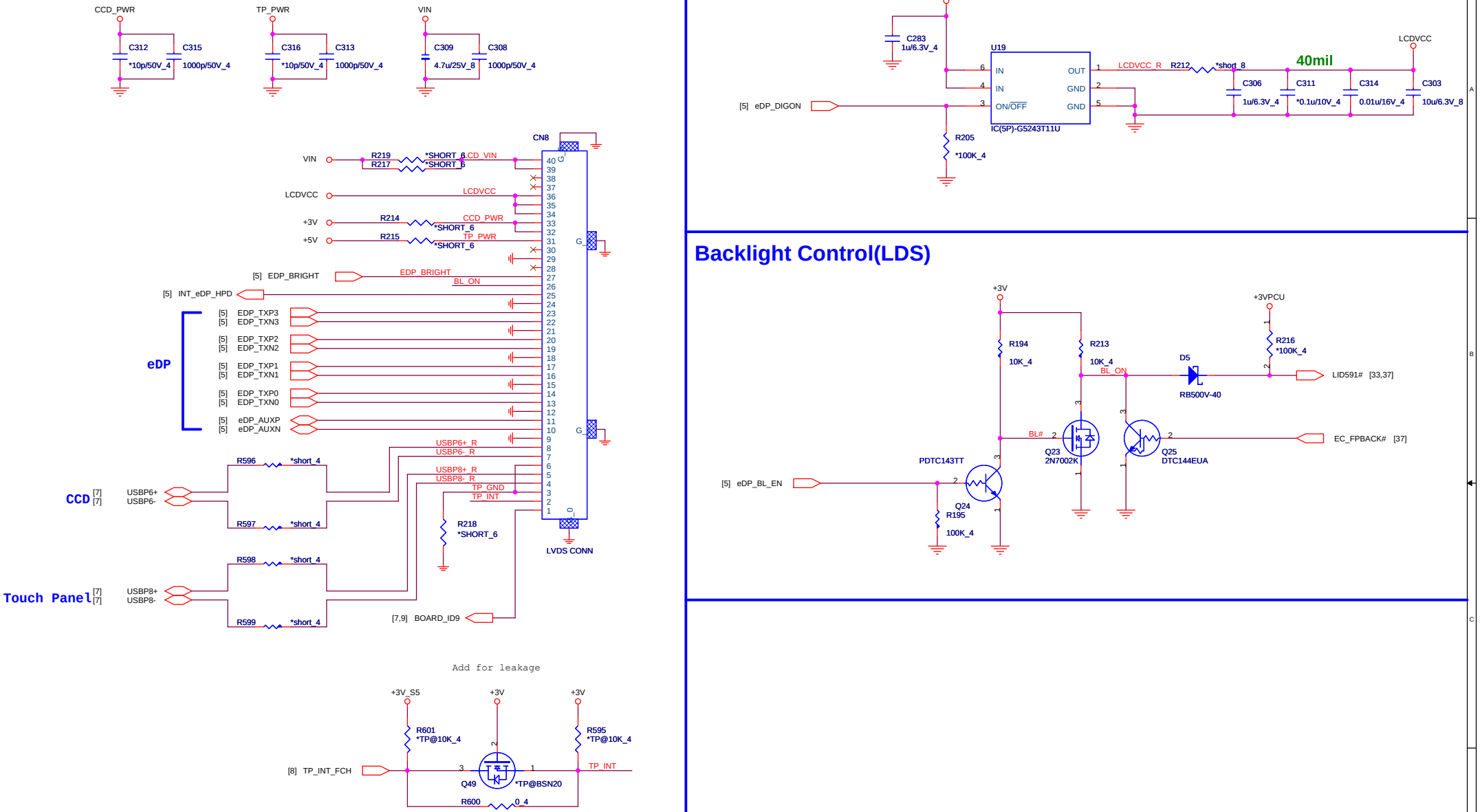
eDP(LDS)



LCD PW(LDS)

Backlight Control(LDS)

Quanta Computer Inc.

PROJECT : ZRI/ZQI

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	LVDS&CCD&CRT DB&LID	A1A
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HDMI

ESD

ESD1
[5] INT_HDMI_TXDP2
[5] INT_HDMI_TXDN2
[5] INT_HDMI_TXDP1
[5] INT_HDMI_TXDN1
GND_3/8
INT_HDMI_TXDP2
INT_HDMI_TXDN2
INT_HDMI_TXDP1
INT_HDMI_TXDN1
*HM@RClamp0524P

ESD2
[5] INT_HDMI_TXDP0
[5] INT_HDMI_TXDN0
[5] INT_HDMI_TXCP
[5] INT_HDMI_TXCN
GND_3/8
INT_HDMI_TXDP0
INT_HDMI_TXDN0
INT_HDMI_TXCP
INT_HDMI_TXCN
*HM@RClamp0524P

ESD3
HDMI_DDCCLK
HDMI_DDCDATA
HDMI_DET
+5V_HDMI
GND_3/8
HDMI_DDCCLK
HDMI_DDCDATA
HDMI_DET
+5V_HDMI
*HM@RClamp0524P

INT_HDMI_TXDP2 C365 1.6p/50V_4
INT_HDMI_TXDN2 C366 1.6p/50V_4
INT_HDMI_TXDP1 C437 1.6p/50V_4
INT_HDMI_TXDN1 C447 1.6p/50V_4
INT_HDMI_TXDP0 C452 1.6p/50V_4
INT_HDMI_TXDN0 C458 1.6p/50V_4
INT_HDMI_TXCP C466 1.6p/50V_4
INT_HDMI_TXCN C756 1.6p/50V_4

+5V
Q37
IN OUT GND
AP2331SA-7
C626 *220p/50V_4
D25 *EGA_4
RV1 *EGA_4
C19 *1000p/50V_4
C624 *1000p/50V_4

CN2
SHELL1 SHELL3
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHELL4 SHELL2
ABA-HDM-022-P05
INT_HDMI_TXDP2
INT_HDMI_TXDN2
INT_HDMI_TXDP1
INT_HDMI_TXDN1
INT_HDMI_TXDP0
INT_HDMI_TXDN0
INT_HDMI_TXCP
INT_HDMI_TXCN
HDMI_DDCCLK
HDMI_DDCDATA
+5V_HDMI
HDMI_DET

HDMI_PL_MOS
+5V
Q1
2N7002K
R20
100K_4
R38 604/F_4 INT_HDMI_TXDP2
R39 604/F_4 INT_HDMI_TXDN2
R40 604/F_4 INT_HDMI_TXDP1
R41 604/F_4 INT_HDMI_TXDN1
R42 604/F_4 INT_HDMI_TXDP0
R43 604/F_4 INT_HDMI_TXDN0
R44 604/F_4 INT_HDMI_TXCP
R45 604/F_4 INT_HDMI_TXCN

HDMI SDVO I2C Control

[5] INT_HDMI_AUXP
[5] INT_HDMI_AUXN
+5V
+3V
R454 2.2K_4
R460 2.2K_4
Q38 BSN20
Q41 BSN20
D26 RB501V-40
D29 RB501V-40
R456 2.2K_4
R459 2.2K_4
HDMI_DDCCLK
HDMI_DDCDATA

HDMI HPD SENSE

[5] INT_HDMI_HPD
+3V
R72 10K_4
R75 1K_4
Q3 2N7002K
Q2 2N7002K
R34 100K_4
HDMI_DET
HDMI_HPD_EC# [37]

EMI reserve for HDMI(EMC)

Close connector

INT_HDMI_TXDP2 R24 *100/F_4 INT_HDMI_TXDN2
INT_HDMI_TXDP1 R25 *100/F_4 INT_HDMI_TXDN1
INT_HDMI_TXDP0 R26 *100/F_4 INT_HDMI_TXDN0
INT_HDMI_TXCP R27 *100/F_4 INT_HDMI_TXCN

Quanta Computer Inc.
PROJECT : ZRI/ZQI

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	HDMI	A1A
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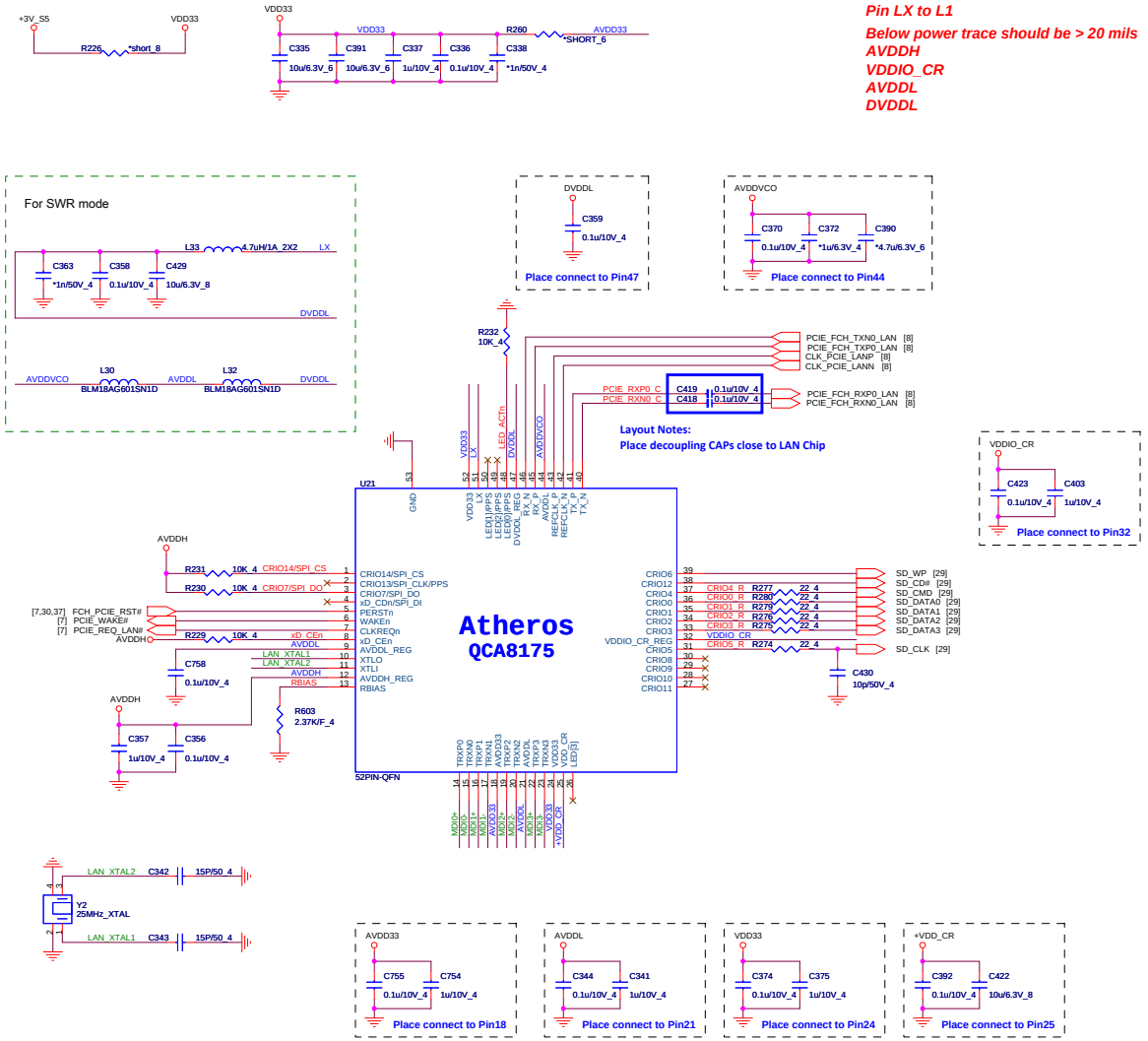
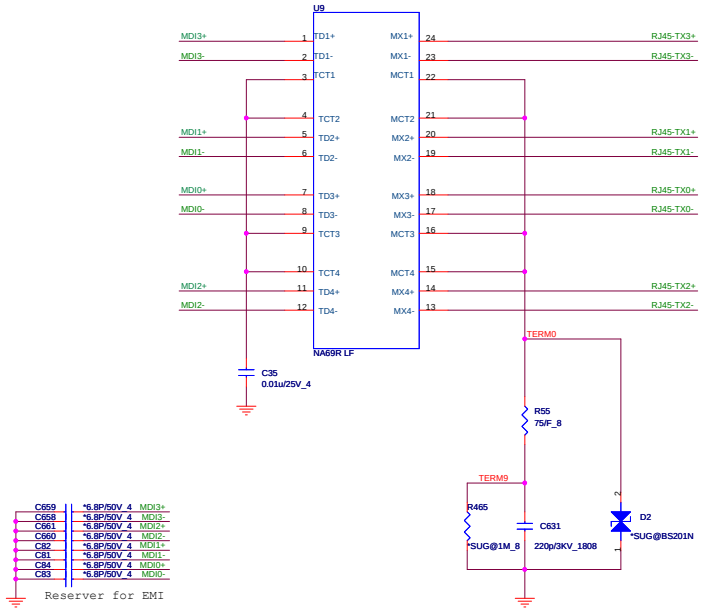
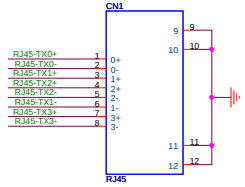
LAN/Card reader (LAN)



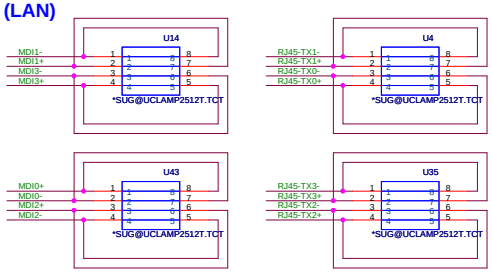
Transformer (LAN)



RJ45 CONNECTOR (LAN)



SURGE (LAN)



Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	LAN-RTL8411/CARD READER	A1A

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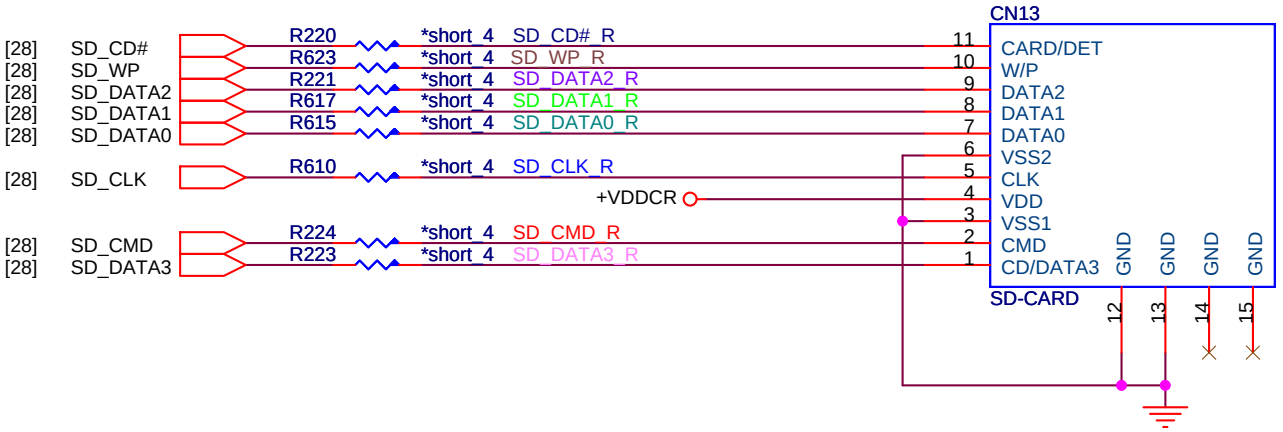
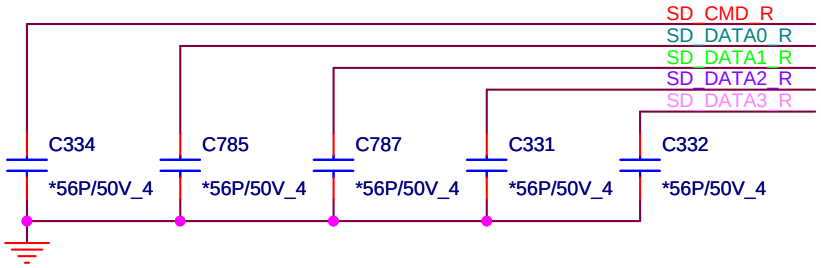
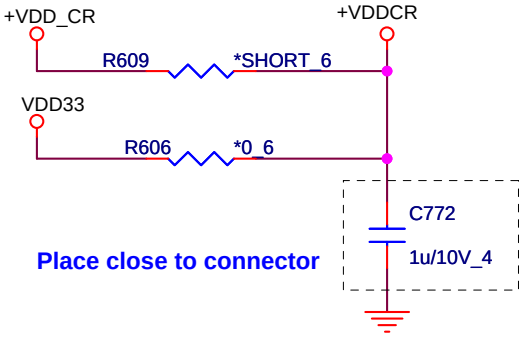
CARD READER CONNECTOR (MMC)

SD/MMC CARD READER (MMC)



EMI





Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
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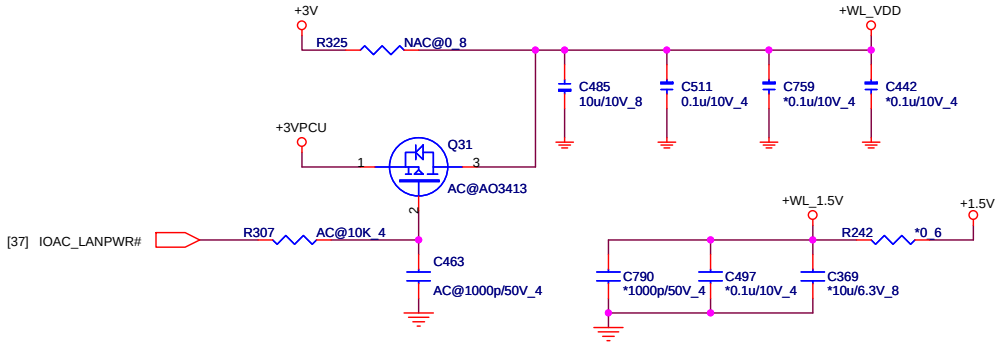
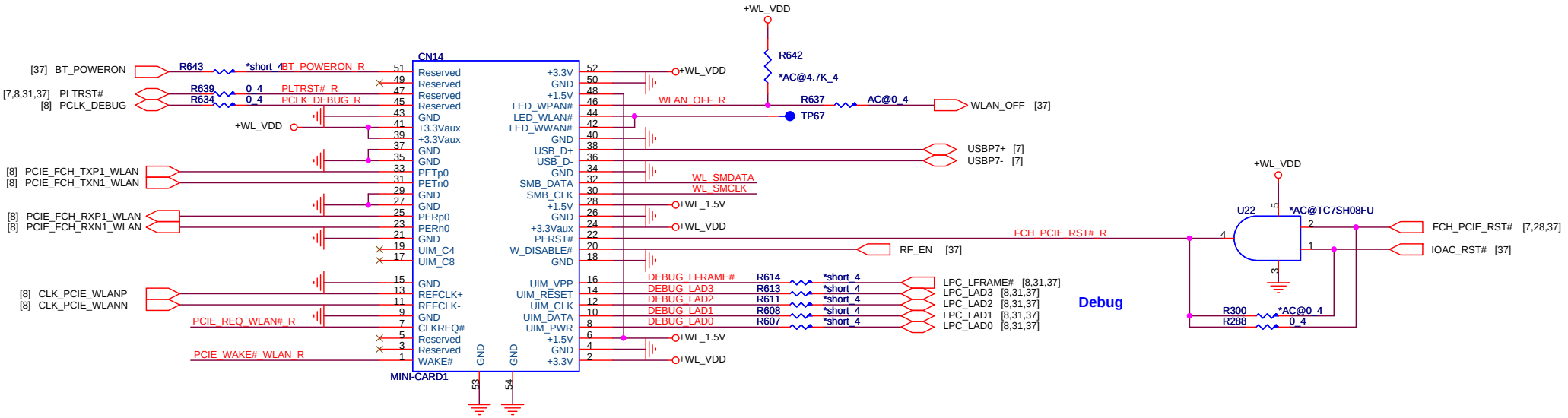
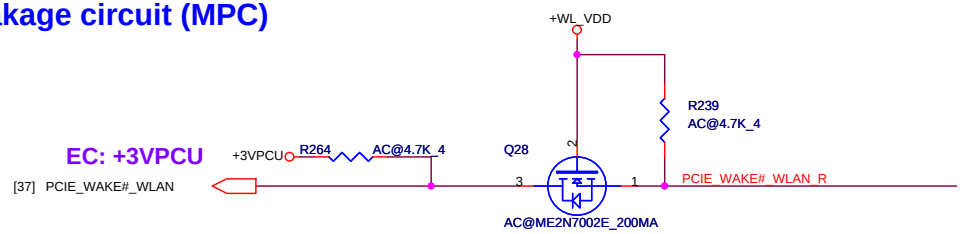
MINI-CARD WLAN&BT(MPC)

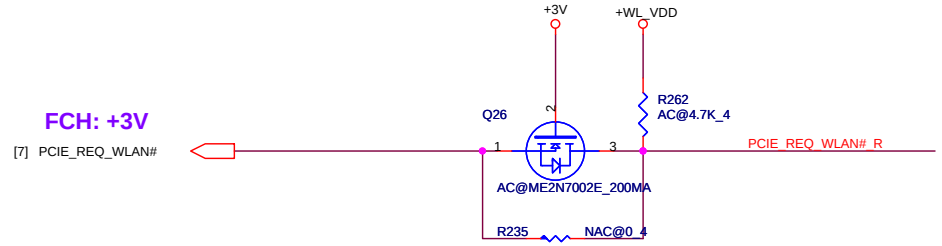
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

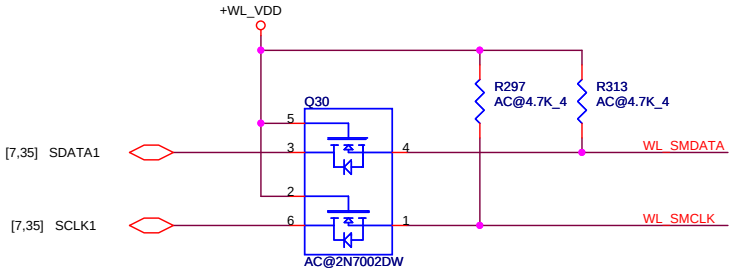




Leakage circuit (MPC)







Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
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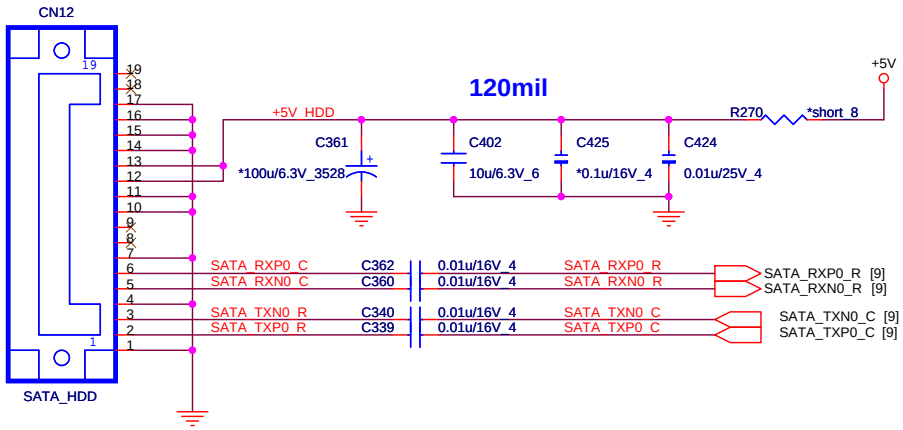
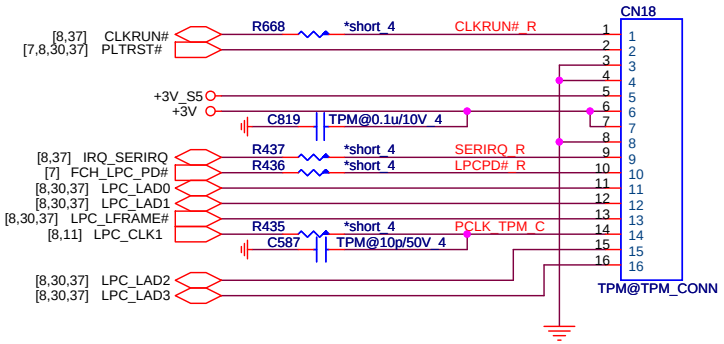
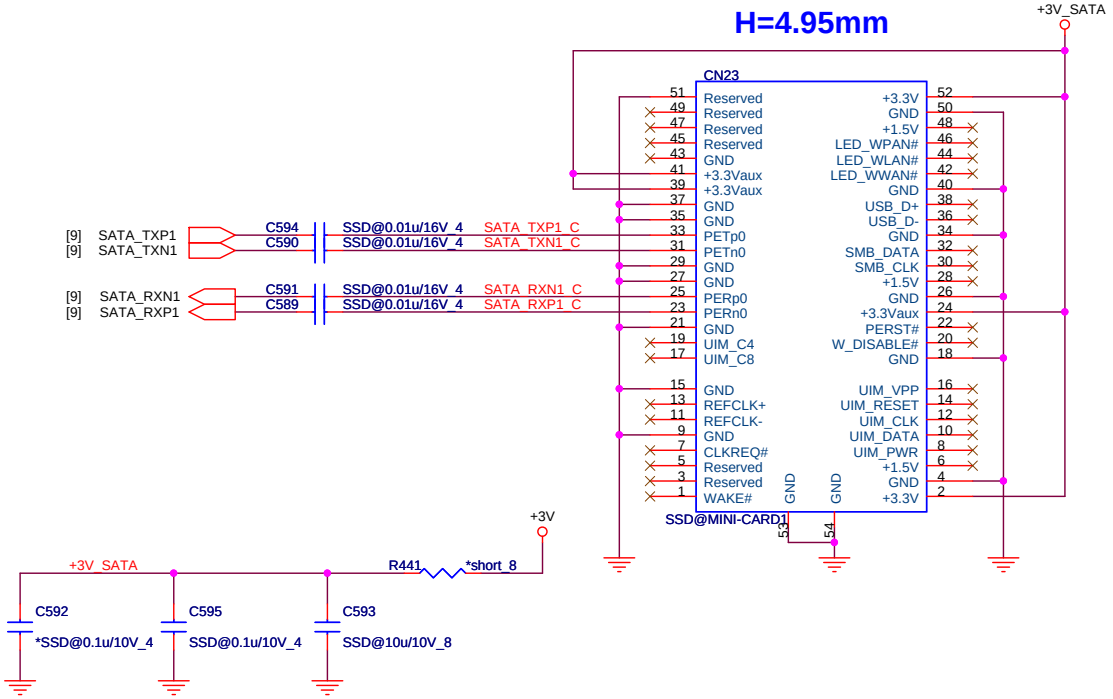
SATA HDD



TPM



MINI-CARD SSD



rating = 1000mA @ 128G

SATA Re-driver

Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	SATA(HDD/SSD/TPM)	A1A

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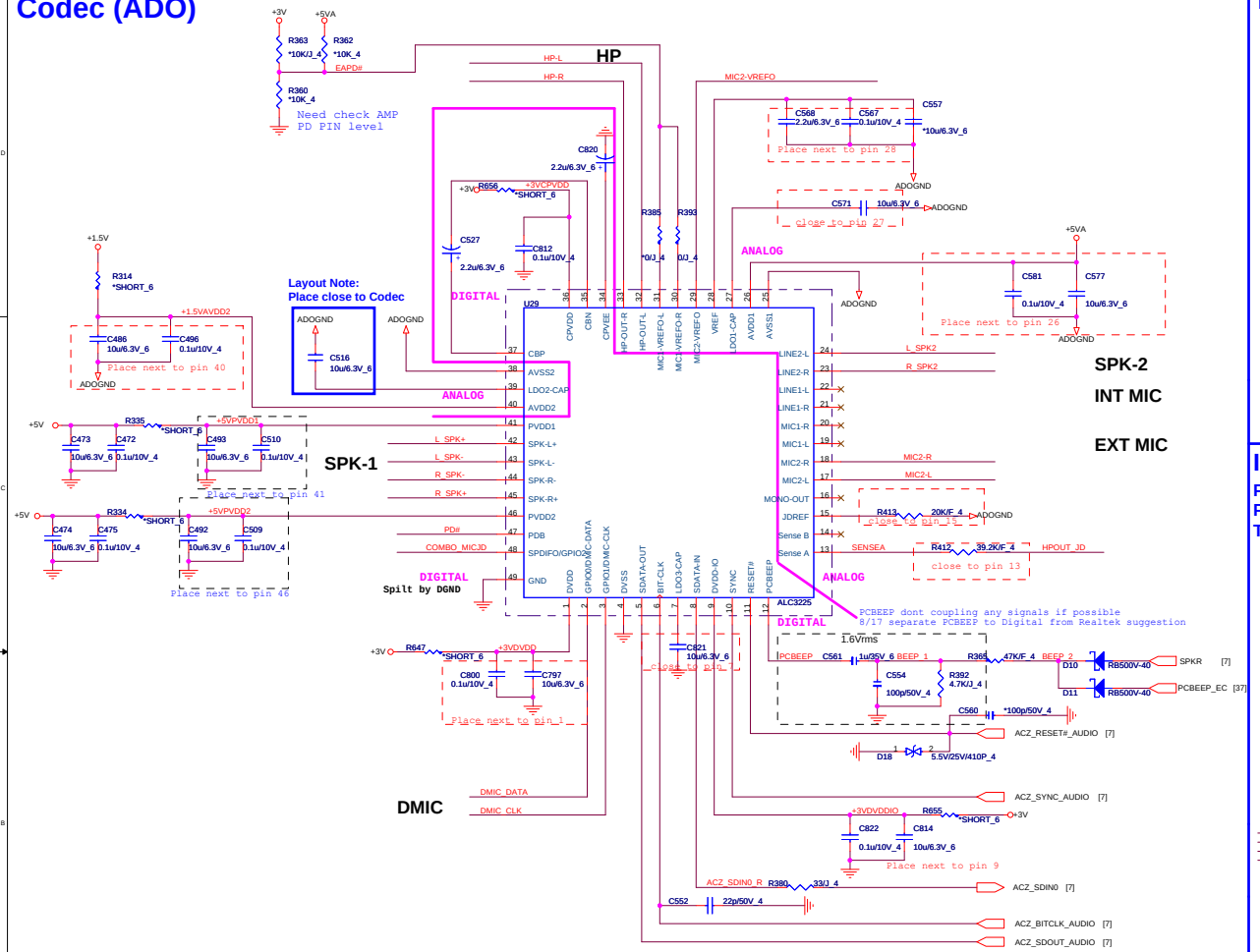
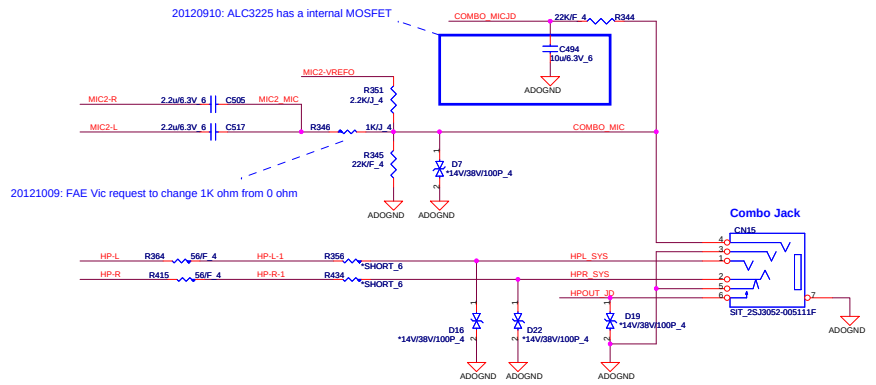
Codec (ADO)



HEADPHONE/Mic combo (AMP)

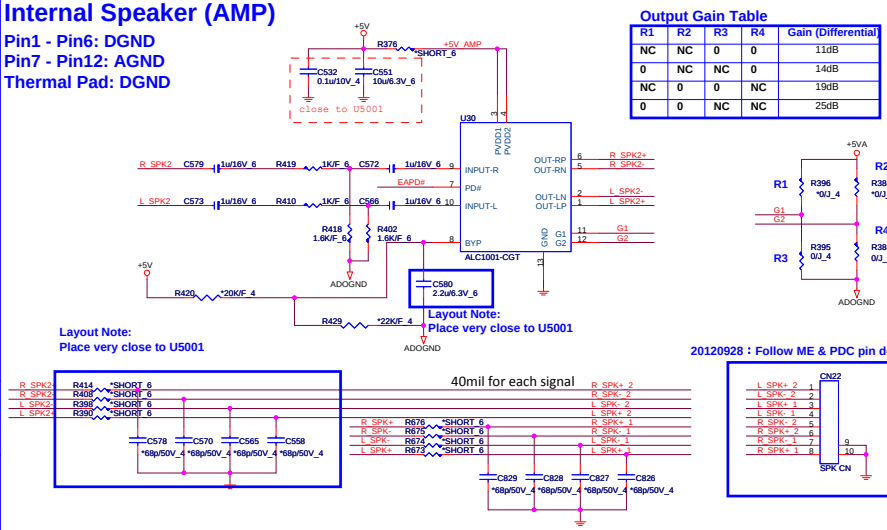


Internal Speaker (AMP)

Pin1 - Pin6: DGND
Pin7 - Pin12: AGND
Thermal Pad: DGND

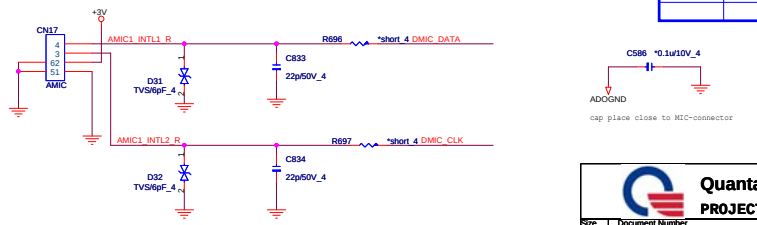
Output Gain Table

R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

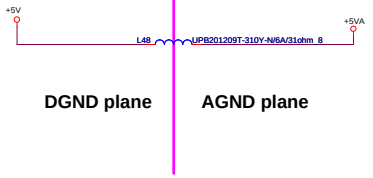


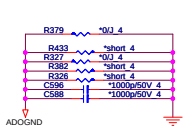
INT DIP AMIC(Reserve Stereo) (AMP)

	Mono MIC	Stereo MIC
CN1	N.C	stuff
R6	N.C	stuff
R5	stuff	N.C

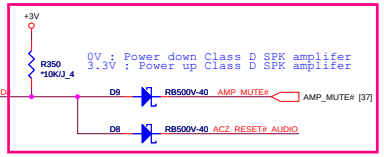


Power(ADO)





Mute(ADO)



Quanta Computer Inc.	
PROJECT : ZRI/ZQI	
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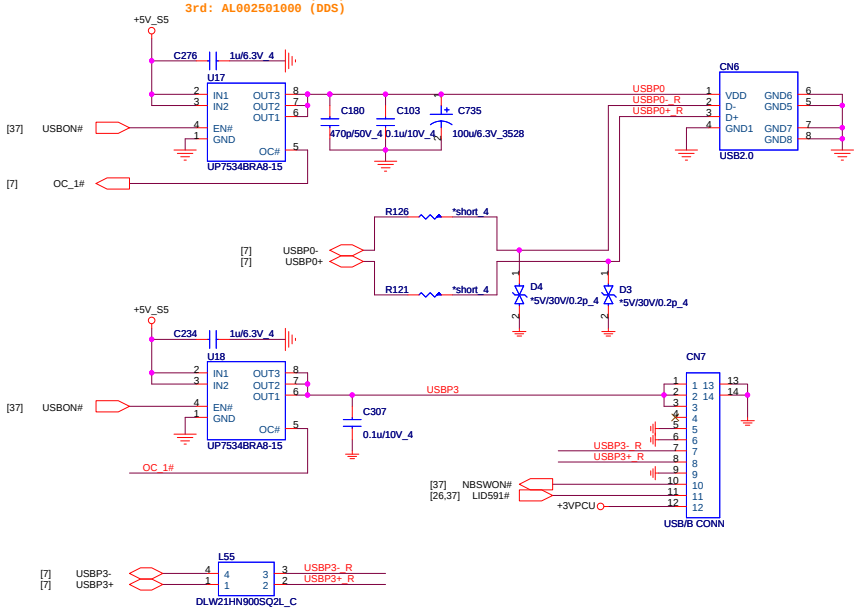
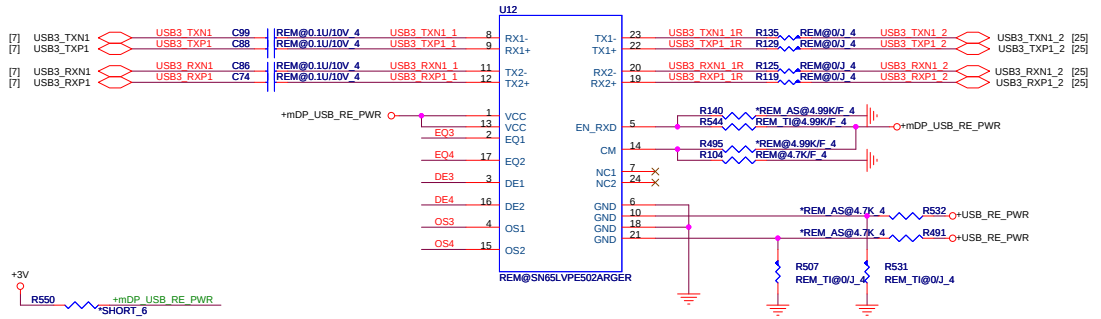
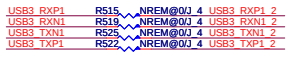
INT & EXT USB2.0

Active Low:
1st: AL007534000 (Promate)
2nd: AL000547005 (GMT)
3rd: AL002501000 (DDS)

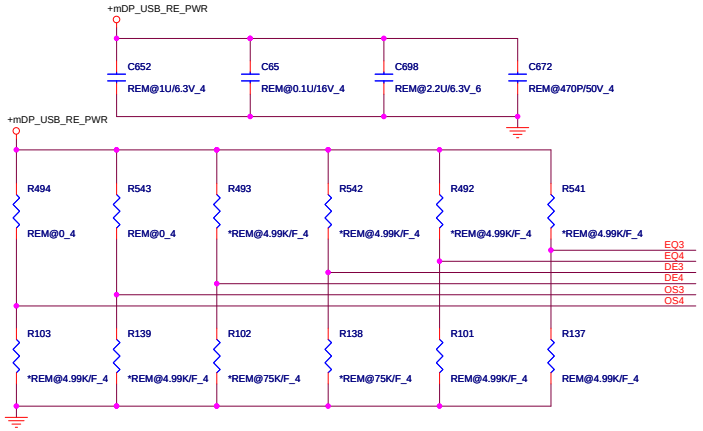


mDP USB3.0 re-driver IC





Control pins setting			
EN_RXD	Device function	CM	Device function
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode



Quanta Computer Inc.
PROJECT : ZRI/ZQI

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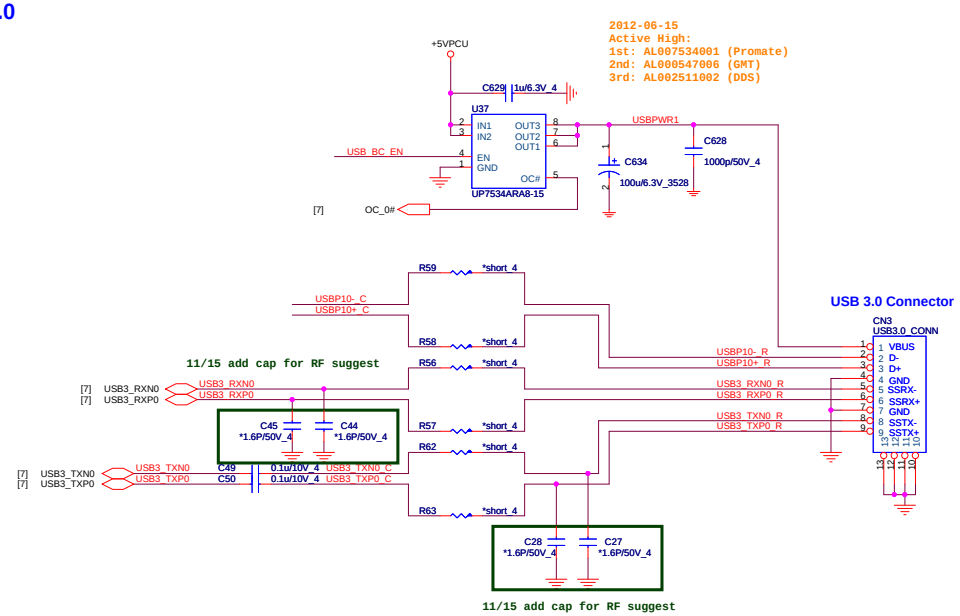
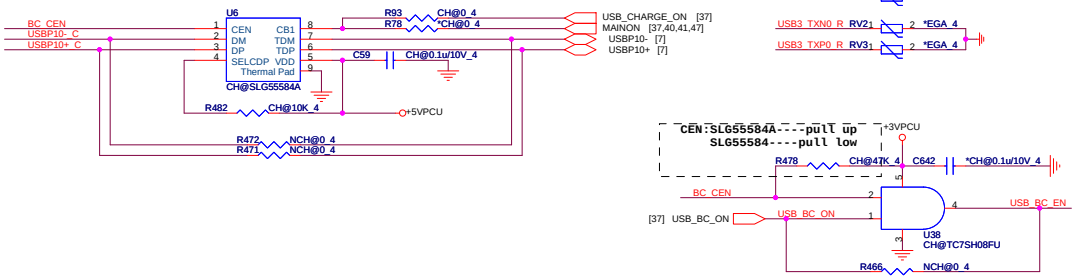
USB3.0/2.0



USB Charger to 3.0

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



USB3.0 re-driver IC

Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
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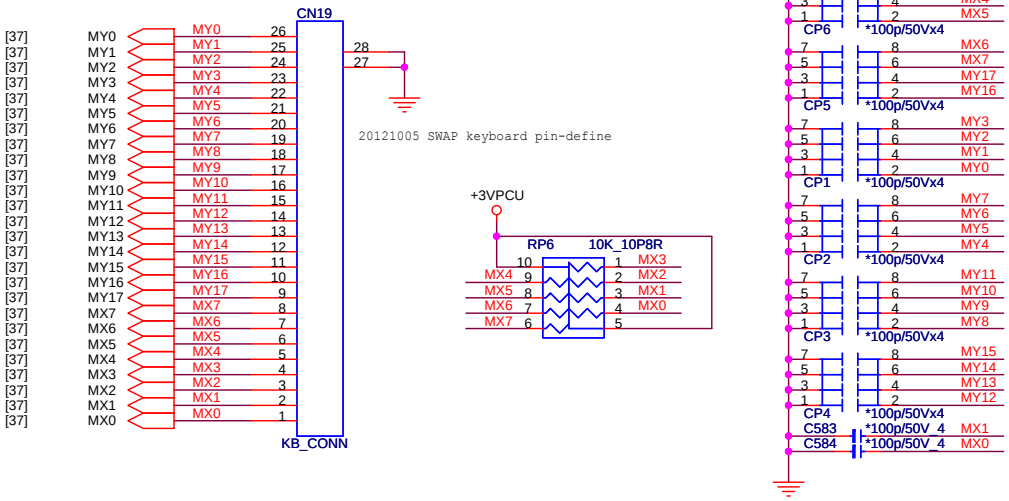
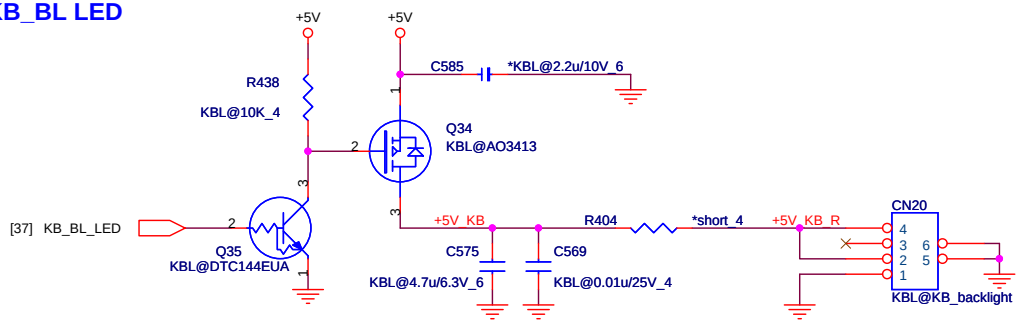
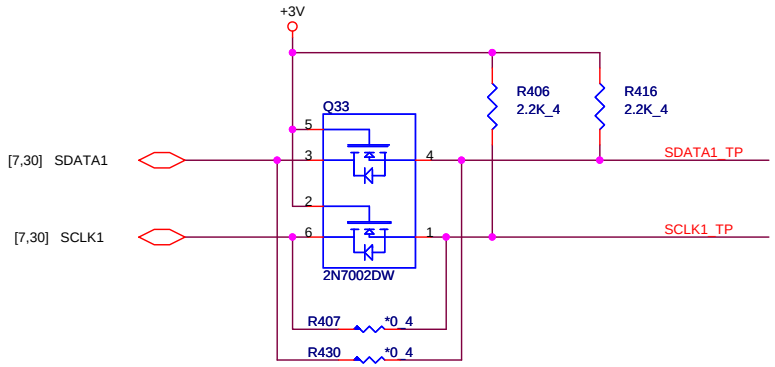
K/B(KBC)

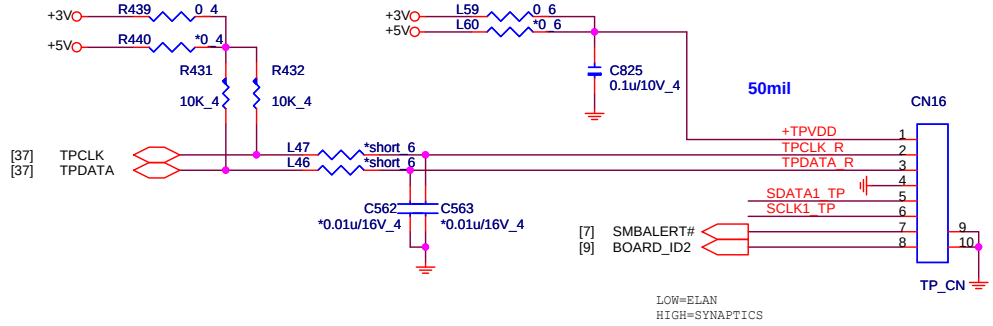


KB_BL LED



TOUCHPAD BOARD CONN(TPD)

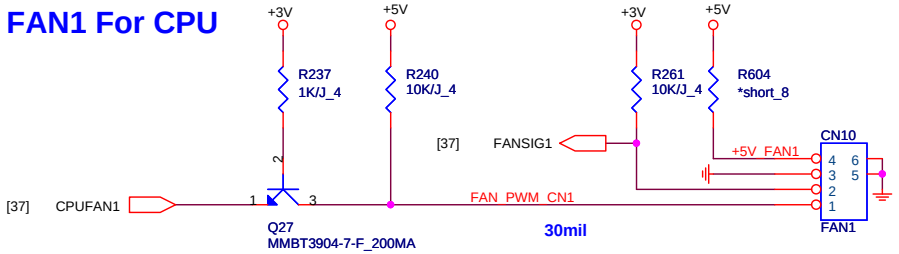




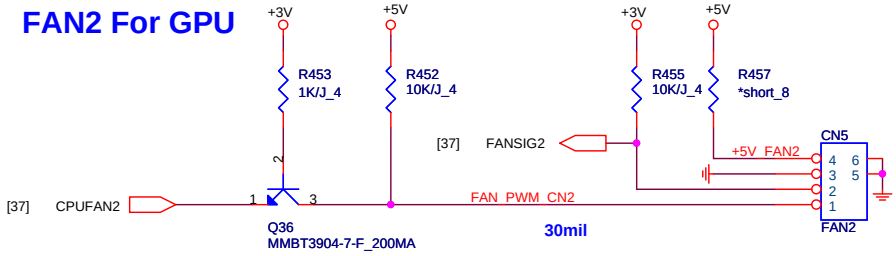
CPU FAN(THM)

If need to support XT(25) GPU, need check with thermal

FAN1 For CPU



FAN2 For GPU



Quanta Computer Inc.

PROJECT : ZRI/ZQI

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	KB/TP/FAN	A1A
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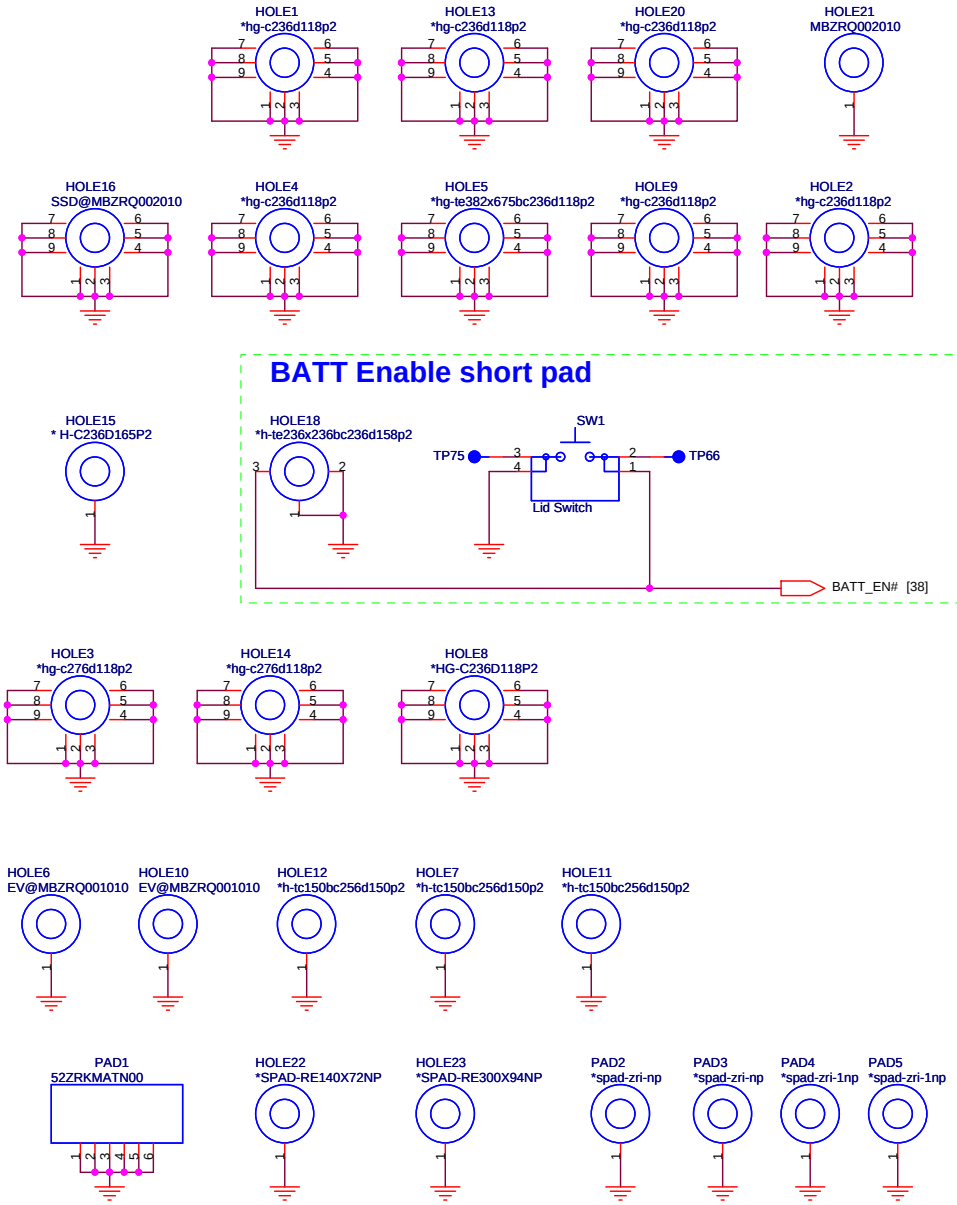
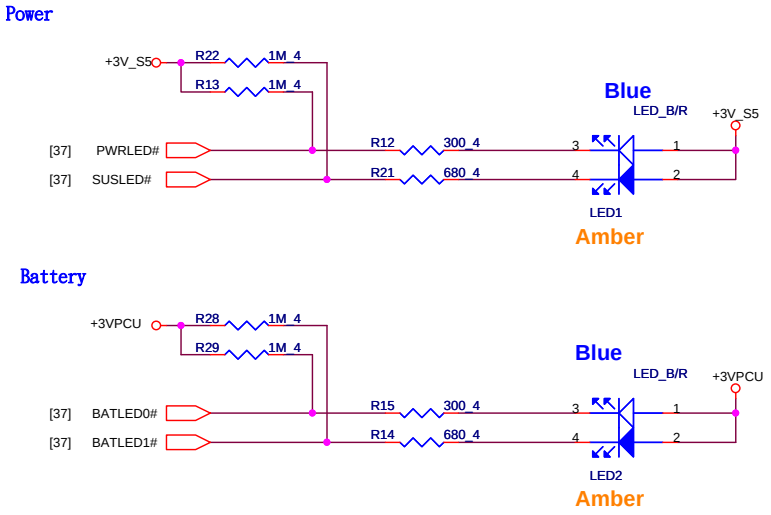
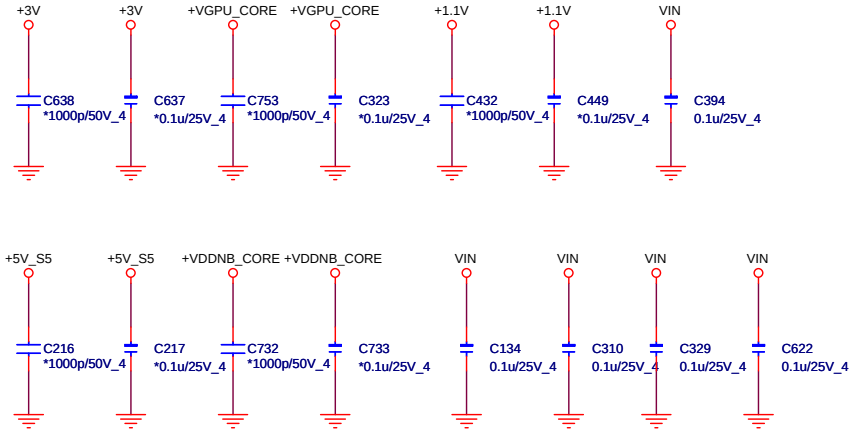
HOLE(OTH)



LED(UIF)



EE RETURN-PATH CAPACITORS(EMC)



Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	LAN DB/ LED/ EMI/ Hole	A1A
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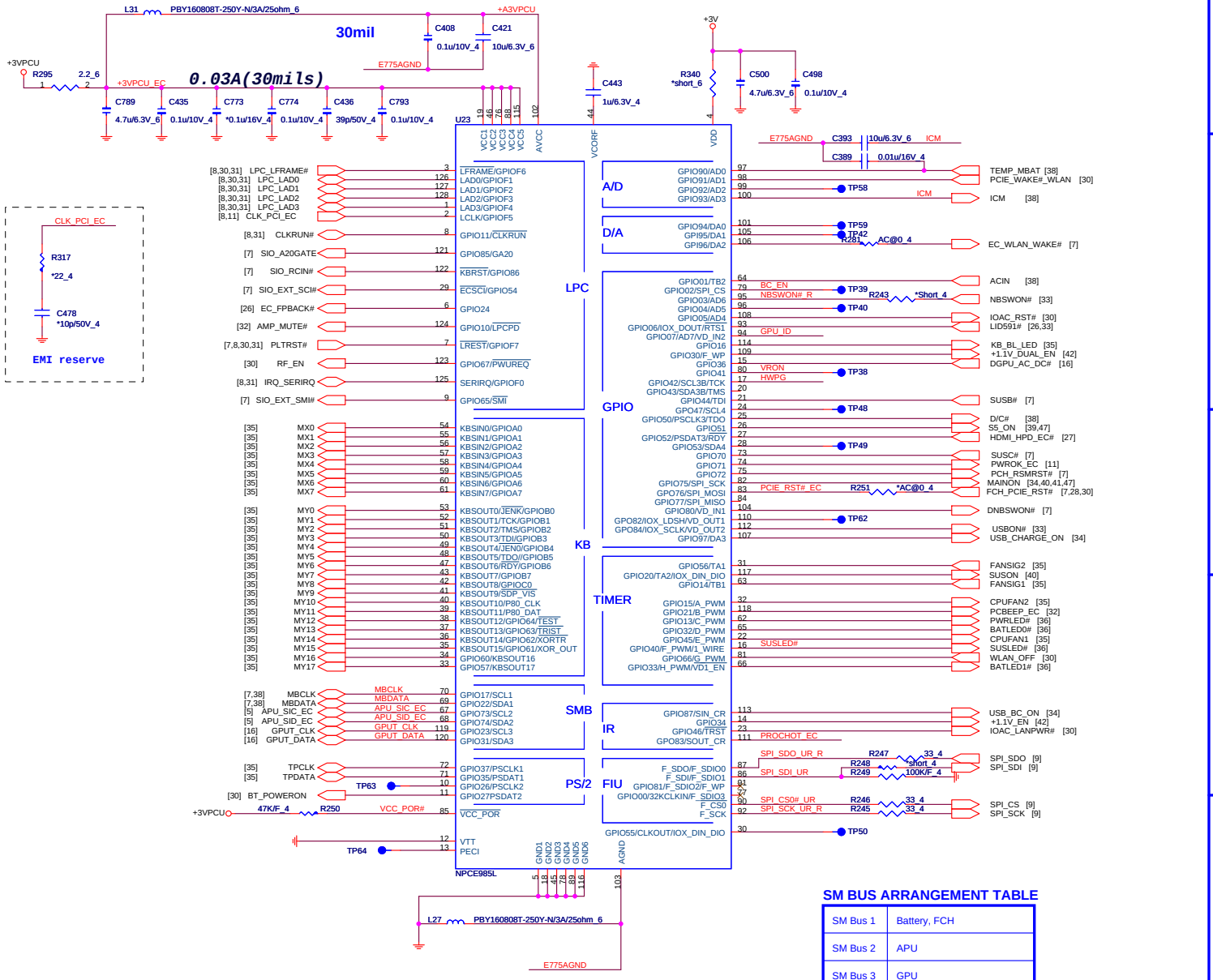
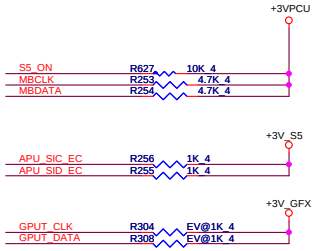
EC(KBC)

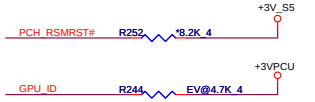


SM BUS ARRANGEMENT TABLE

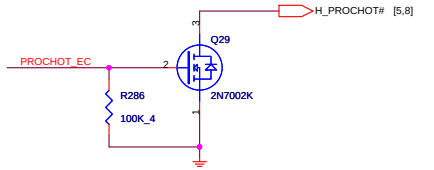
SM Bus 1	Battery, FCH
SM Bus 2	APU
SM Bus 3	GPU

SM BUS PU(KBC)

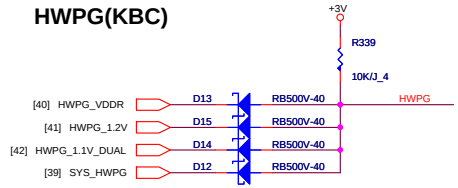




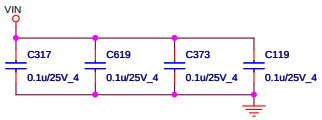
GPU_ID : H = Mars
L = Thames

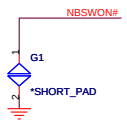


HWPG(KBC)

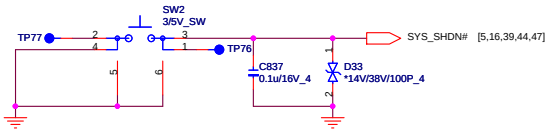


Placement for EC of VIN power plan





3/5VPCU reset switch (CLG)



Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	NPCE885/FLASH	A1A

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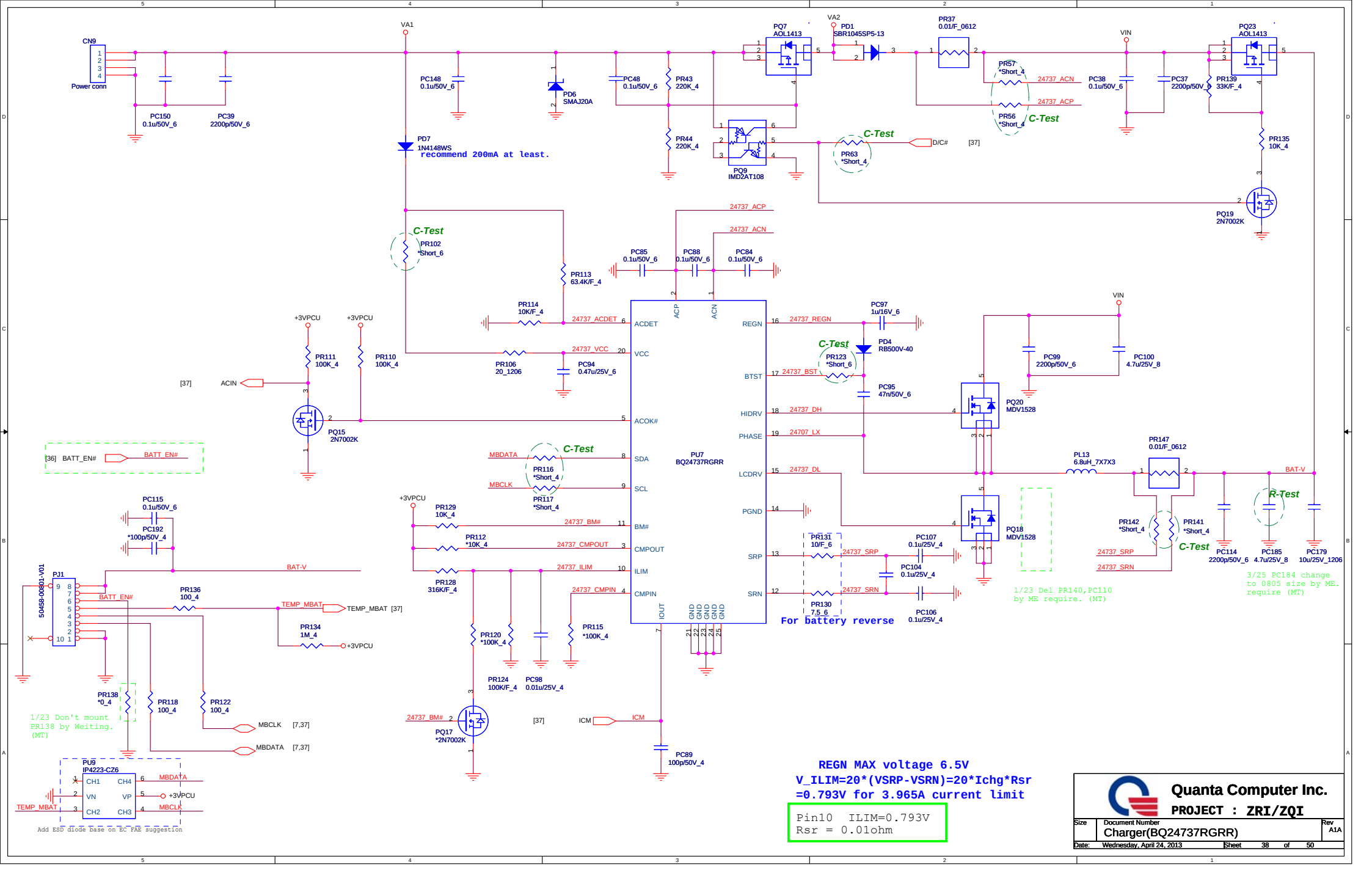
CN9
Power conn
PC150 0.1u/50V_6
PC39 2200p/50V_6
VA1
PC148 0.1u/50V_6
PD6 SMAJ20A
PC48 0.1u/50V_6
PR43 220K_4
PR44 220K_4
PQ7 AOL1413
VA2
PD1 SBR1045SP5-13
PR37 0.01/F_0612
PR57 *Short_4
PR56 *Short_4
24737_ACN
24737_ACP
C-Test
VIN
PC38 0.1u/50V_6
PC37 2200p/50V_6
PR139 33K/F_4
PQ23 AOL1413
PR135 10K_4
PQ19 2N7002K
PD7 1N4148WS
recommend 200mA at least.
PQ9 IMD2AT108
PR63 *Short_4
D/C#
[37]
PR102 *Short_6
PR113 63.4K/F_4
PC85 0.1u/50V_6
PC88 0.1u/50V_6
PC84 0.1u/50V_6
PR114 10K/F_4
24737_ACDET
24737_VCC
PR106 20_1206
PC94 0.47u/25V_6
+3VPCU
PR111 100K_4
PR110 100K_4
[37] ACIN
PQ15 2N7002K
[36] BATT_EN#
PU7 BQ24737RGRR
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
GND
PC97 1u/16V_6
24737_REGN
PD4 RB500V-40
PR123 *Short_6
24737_BST
PC95 47n/50V_6
24737_DH
24707_LX
24737_DL
PC99 2200p/50V_6
PC100 4.7u/25V_8
PQ20 MDV1528
PQ18 MDV1528
PL13 6.8uH_7X7X3
PR147 0.01/F_0612
BAT-V
R-Test
PR142 *Short_4
PR141 *Short_4
PC114 2200p/50V_6
PC185 4.7u/25V_8
PC179 10u/25V_1206
3/25 PC184 change to 0805 size by ME. require (MT)
MBDATA
MBCLK
PR116 *Short_4
PR117 *Short_4
PC115 0.1u/50V_6
PC192 *100p/50V_4
BAT-V
PJ1
50458-00801-V01
BATT_EN#
PR136 100_4
TEMP_MBAT
TEMP_MBAT [37]
PR134 1M_4
+3VPCU
PR129 10K_4
PR112 *10K_4
PR128 316K/F_4
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
PR120 *100K_4
PR124 100K/F_4
PC98 0.01u/25V_4
PR115 *100K_4
PQ17 *2N7002K
ICM
PC89 100p/50V_4
PR131 10/F_6
PR130 7.5_6
For battery reverse
PC107 0.1u/25V_4
PC104 0.1u/25V_4
PC106 0.1u/25V_4
24737_SRP
24737_SRN
1/23 Del PR140,PC110 by ME require. (MT)
PR138 *0_4
PR118 100_4
PR122 100_4
1/23 Don't mount PR138 by Weiting. (MT)
MBCLK [7,37]
MBDATA [7,37]
PU9
IP4223-CZ6
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : ZRI/ZQI
Size
Document Number
Charger(BQ24737RGRR)
Rev A1A
Date: Wednesday, April 24, 2013
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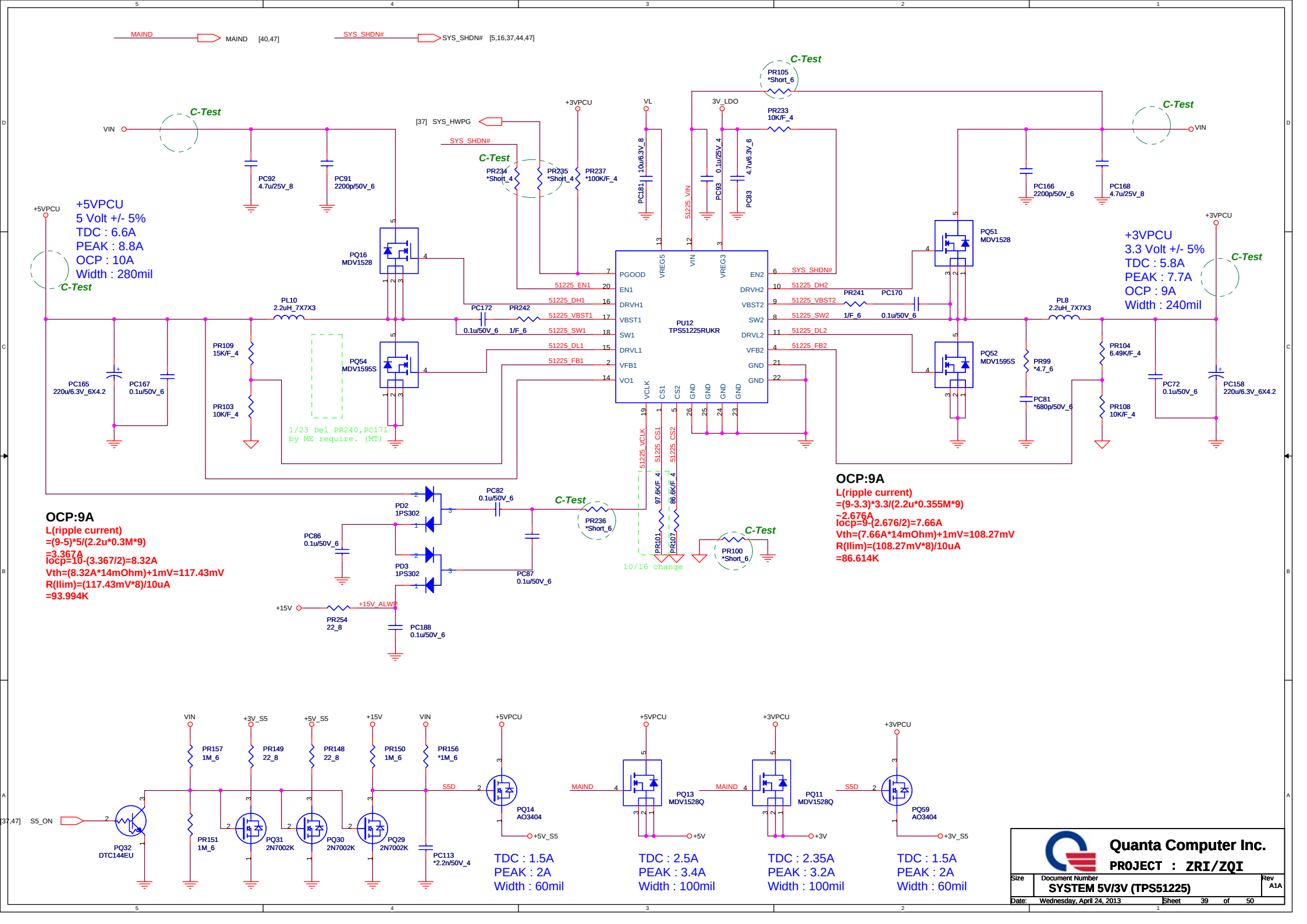
MAIND
MAIND [40,47]
SYS_SHDN#
SYS_SHDN# [5,16,37,44,47]
C-Test
VIN
PC92 4.7u/25V_8
PC91 2200p/50V_6
[37] SYS_HWPG
SYS_SHDN#
PR234 *Short_4
PR235 *Short_4
PR237 *100K/F_4
+3VPCU
VL
3V_LDO
PR105 *Short_6
PR233 10K/F_4
PC181 10u/6.3V_8
PC93 0.1u/25V_4
PC83 4.7u/6.3V_6
51225_VIN
PC166 2200p/50V_6
PC168 4.7u/25V_8
+5VPCU
+5VPCU
5 Volt +/- 5%
TDC : 6.6A
PEAK : 8.8A
OCP : 10A
Width : 280mil
PQ16 MDV1528
PL10 2.2uH_7X7X3
PC172 0.1u/50V_6
PR242 1/F_6
PU12 TPS51225RUKR
PGOOD
EN1
DRVH1
VBST1
SW1
DRVL1
VFB1
VO1
VREG5
VIN
VREG3
EN2
DRVH2
VBST2
SW2
DRVL2
VFB2
GND
VCLK
CS1
CS2
51225_EN1
51225_DH1
51225_VBST1
51225_SW1
51225_DL1
51225_FB1
51225_DH2
51225_VBST2
51225_SW2
51225_DL2
51225_FB2
PR241 1/F_6
PC170 0.1u/50V_6
PQ51 MDV1528
PQ52 MDV1595S
PR99 *4.7_6
PC81 *680p/50V_6
PL8 2.2uH_7X7X3
PR104 6.49K/F_4
PR108 10K/F_4
PC72 0.1u/50V_6
PC158 220u/6.3V_6X4.2
+3VPCU
+3VPCU
3.3 Volt +/- 5%
TDC : 5.8A
PEAK : 7.7A
OCP : 9A
Width : 240mil
PQ54 MDV1595S
PR109 15K/F_4
PR103 10K/F_4
PC165 220u/6.3V_6X4.2
PC167 0.1u/50V_6
1/23 Del PR240,PC171
by ME require. (MT)
OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=10-(3.367/2)=8.32A
Vth=(8.32A*14mOhm)+1mV=117.43mV
R(Ilim)=(117.43mV*8)/10uA
=93.994K
PD2 1PS302
PD3 1PS302
PC82 0.1u/50V_6
PC86 0.1u/50V_6
PC87 0.1u/50V_6
PR236 *Short_6
51225_VCLK
51225_CS1
51225_CS2
97.6K/F_4
86.6K/F_4
PR101
PR107
PR100 *Short_6
10/16 change
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=9-(2.676/2)=7.66A
Vth=(7.66A*14mOhm)+1mV=108.27mV
R(Ilim)=(108.27mV*8)/10uA
=86.614K
+15V
+15V_ALW
PR254 22_8
PC188 0.1u/50V_6
[37,47] S5_ON
PQ32 DTC144EU
PR157 1M_6
PR151 1M_6
+3V_S5
PR149 22_8
PQ31 2N7002K
+5V_S5
PR148 22_8
PQ30 2N7002K
+15V
PR150 1M_6
PQ29 2N7002K
VIN
PR156 *1M_6
PC113 *2.2n/50V_4
S5D
PQ14 AO3404
+5V_S5
TDC : 1.5A
PEAK : 2A
Width : 60mil
MAIND
PQ13 MDV1528Q
+5V
TDC : 2.5A
PEAK : 3.4A
Width : 100mil
PQ11 MDV1528Q
+3V
TDC : 2.35A
PEAK : 3.2A
Width : 100mil
PQ59 AO3404
+3V_S5
TDC : 1.5A
PEAK : 2A
Width : 60mil
Quanta Computer Inc.
PROJECT : ZRI/ZQI
Size
Document Number
SYSTEM 5V/3V (TPS51225)
Rev
A1A
Date: Wednesday, April 24, 2013
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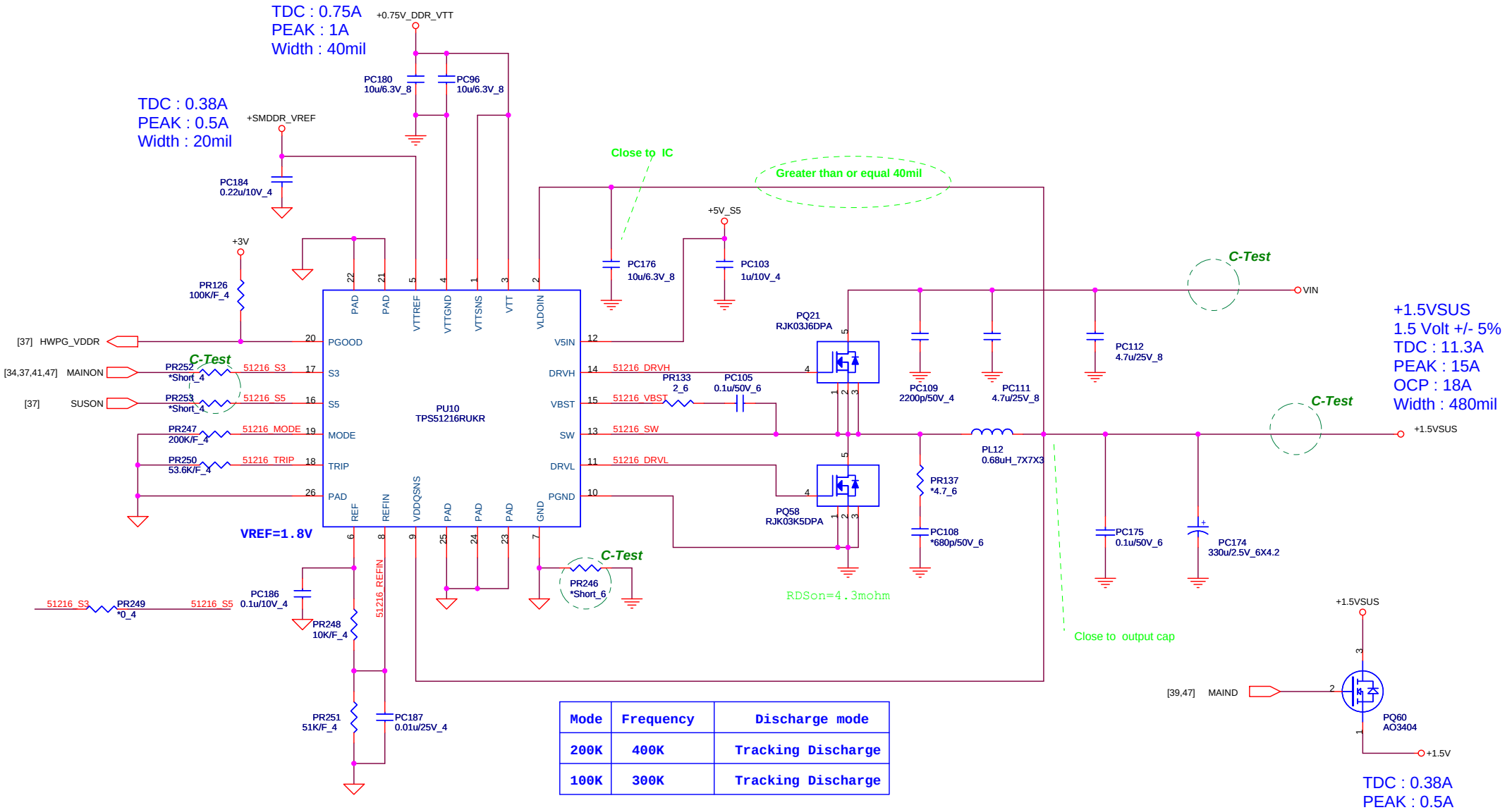


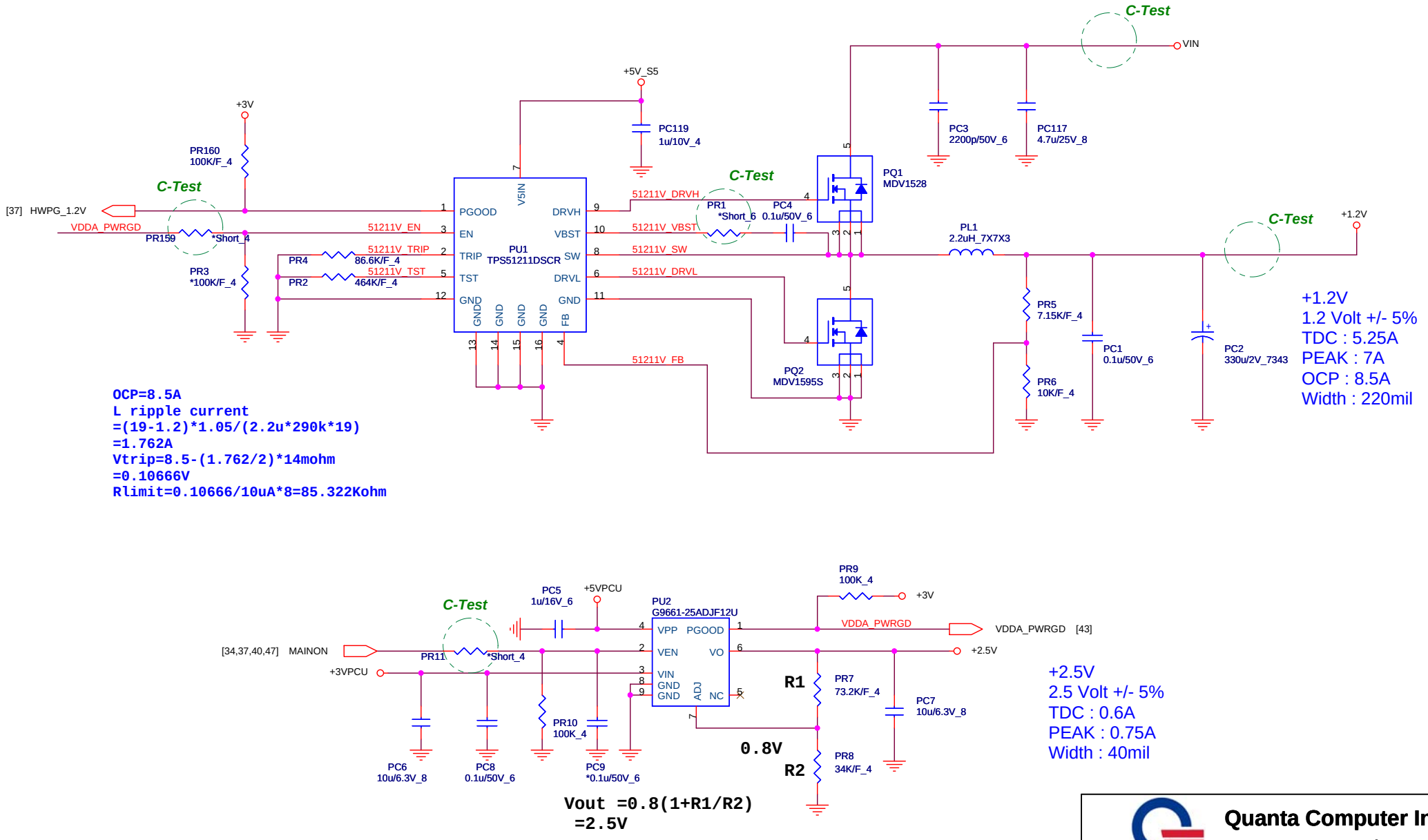
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

OCP=18A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=18-(5.079/2)*4.3mohm
=0.06647V
Rlimit=0.06647/10uA*8=53.183Kohm

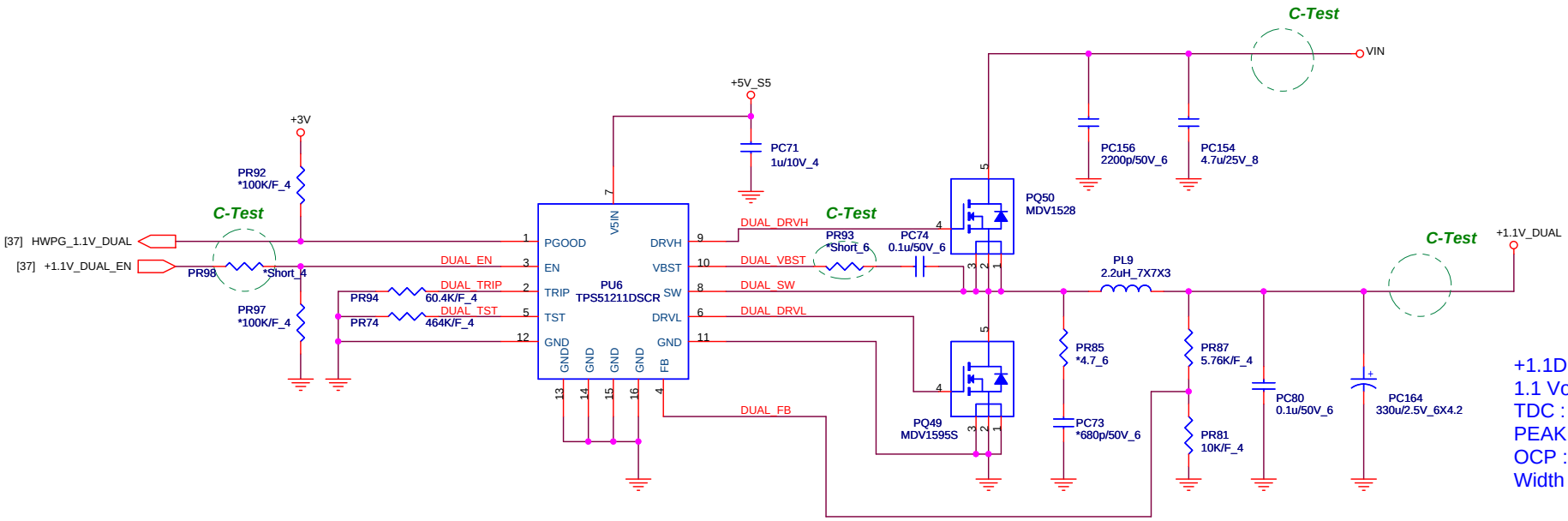
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZRI/ZQI

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	A1A
Date: Wednesday, April 24, 2013	Sheet 40 of 50	

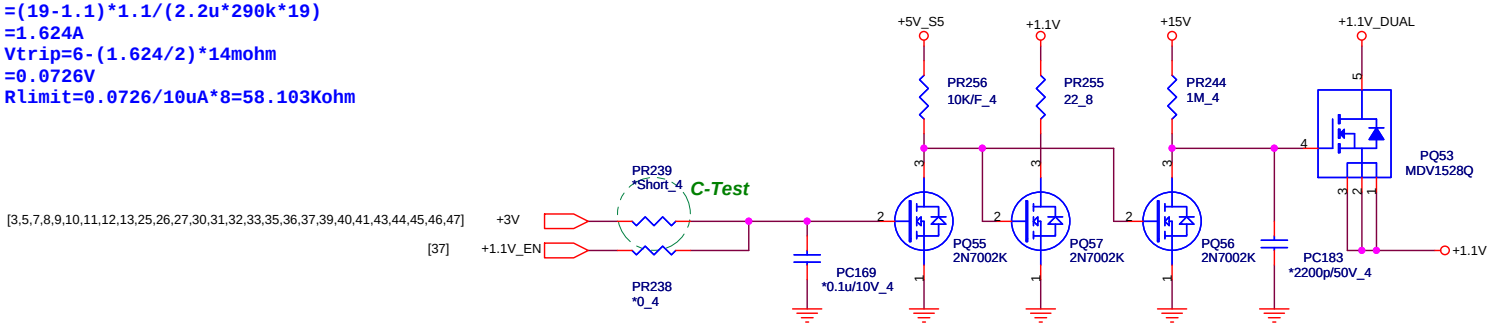


Quanta Computer Inc.		
PROJECT : ZRI/ZQI		
Size	Document Number: +1.2V(TPS51211)/+2.5V	Rev: A1A
Date: Wednesday, April 24, 2013	Sheet 41 of 50	



+1.1DUAL
1.1 Volt +/- 5%
TDC : 3.75A
PEAK : 5A
OCP : 6A
Width : 150mil

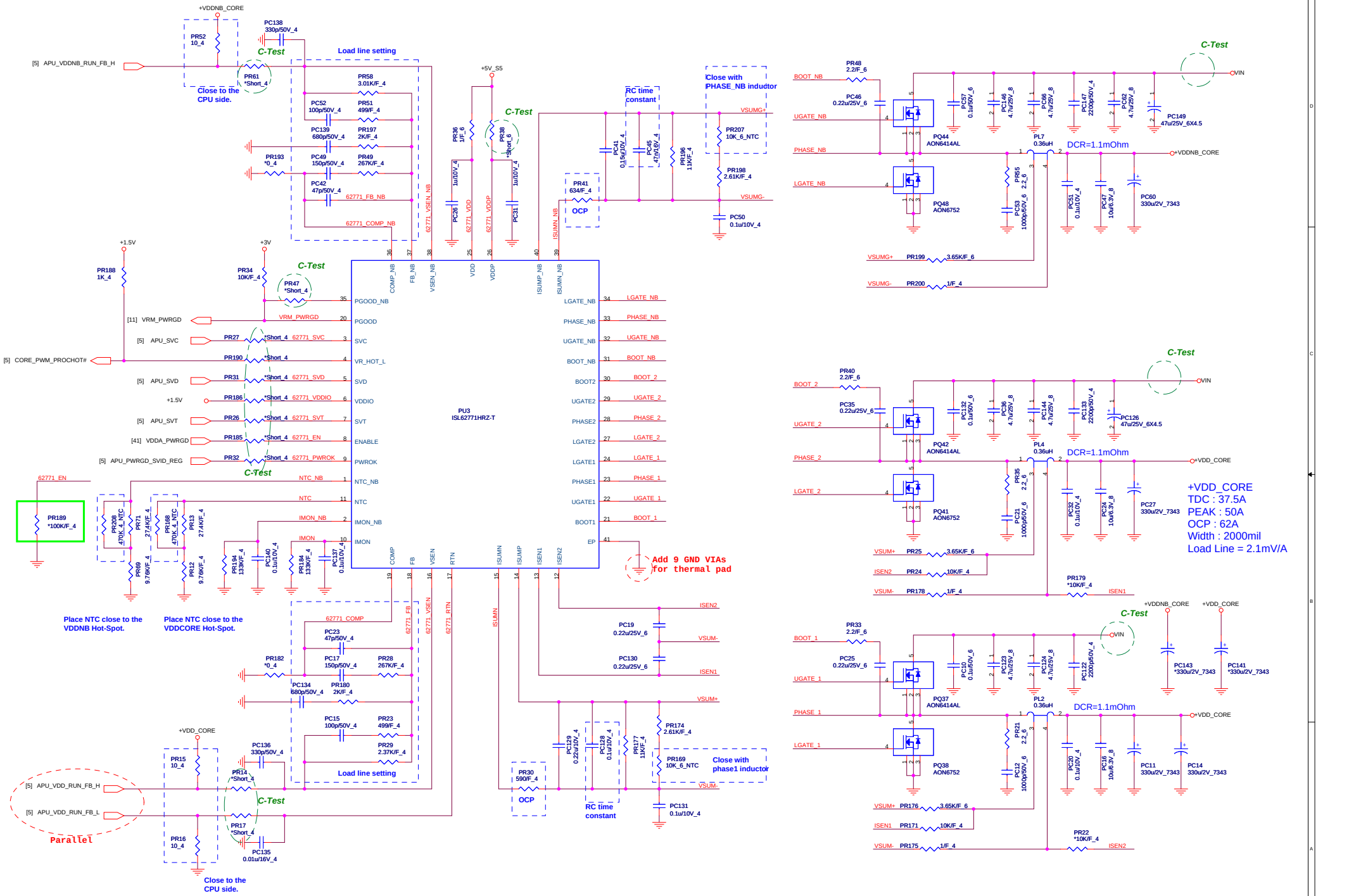
OCP=6A
L ripple current
=(19-1.1)*1.1/(2.2u*290k*19)
=1.624A
Vtrip=6-(1.624/2)*14mohm
=0.0726V
Rlimit=0.0726/10uA*8=58.103Kohm



+1.1V
TDC : 2.8A
PEAK : 3.8A
Width : 120mil

Quanta Computer Inc.
PROJECT : ZRI/ZQI

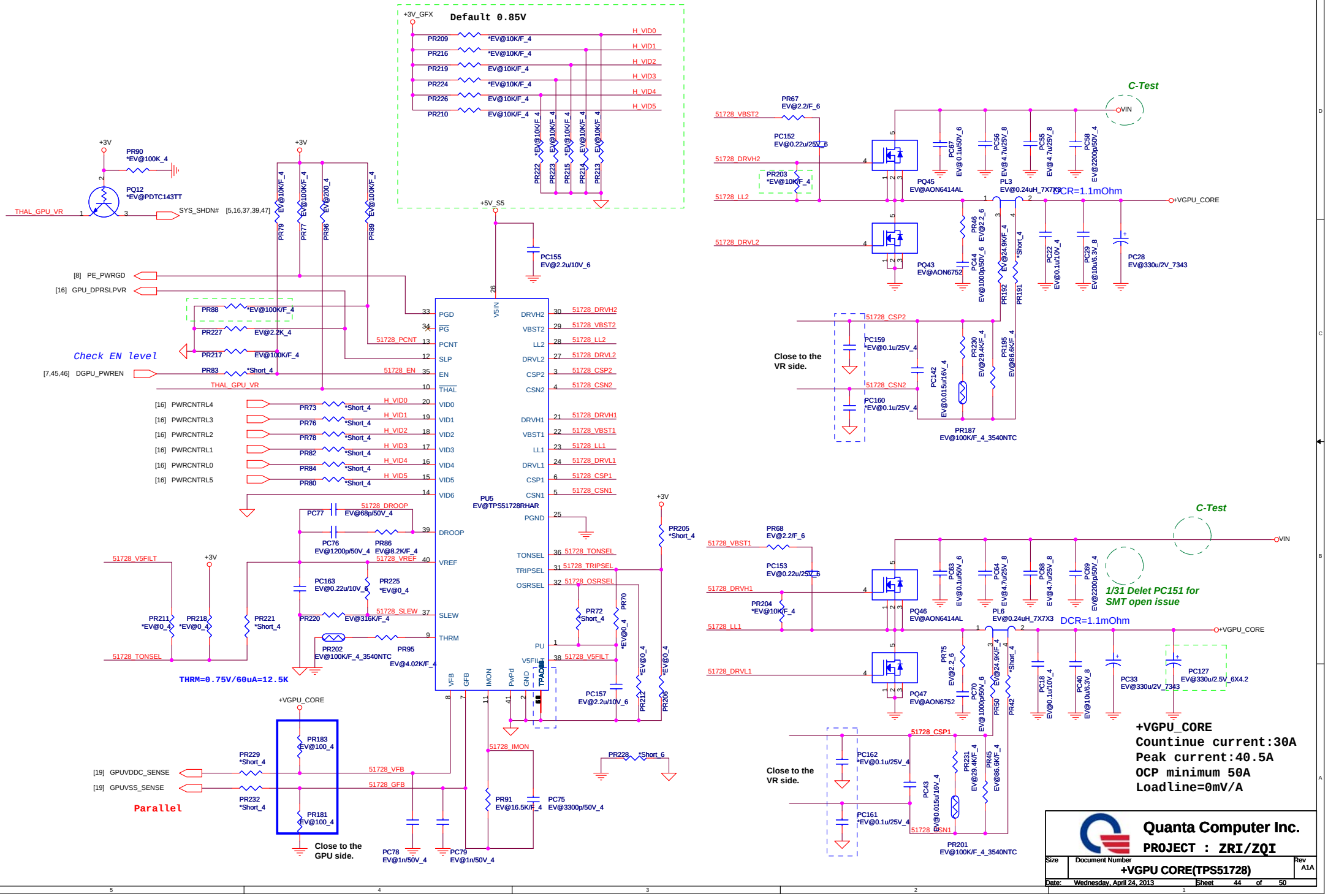
Size	Document Number	Rev
	+1.1V_DUAL(TPS51211)	A1A
Date: Wednesday, April 24, 2013	Sheet 42 of 50	



Quanta Computer Inc.

PROJECT : ZRI/ZQI

Size	Document Number	Rev
	VDD / VDDNB CORE (ISL62771)	A1A
Date: Wednesday, April 24, 2013	Sheet 43 of 50	


Default 0.85V
+3V_GFX
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
PR209 *EV@10K/F_4
PR216 *EV@10K/F_4
PR219 EV@10K/F_4
PR224 *EV@10K/F_4
PR226 EV@10K/F_4
PR210 EV@10K/F_4
PR222 *EV@10K/F_4
PR223 EV@10K/F_4
PR215 *EV@10K/F_4
PR214 EV@10K/F_4
PR213 EV@10K/F_4
+3V
PR90 *EV@100K_4
PQ12 *EV@PDTC143TT
THAL_GPU_VR
SYS_SHDN# [5,16,37,39,47]
PR79 EV@10K/F_4
PR77 EV@100K/F_4
PR96 EV@200_4
PR89 EV@100K/F_4
+5V_S5
PC155 EV@2.2u/10V_6
[8] PE_PWRGD
[16] GPU_DPRSLPVR
PR88 *EV@100K/F_4
PR227 EV@2.2K_4
PR217 EV@100K/F_4
Check EN level
[7,45,46] DGPU_PWREN
PR83 *Short_4
51728_EN
51728_PCNT
THAL_GPU_VR
[16] PWRCNTRL4
[16] PWRCNTRL3
[16] PWRCNTRL2
[16] PWRCNTRL1
[16] PWRCNTRL0
[16] PWRCNTRL5
PR73 *Short_4
PR76 *Short_4
PR78 *Short_4
PR82 *Short_4
PR84 *Short_4
PR80 *Short_4
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
PU5 EV@TPS51728RHAR
PGD
PG
PCNT
SLP
EN
THAL
VID0
VID1
VID2
VID3
VID4
VID5
VID6
V5IN
DRVH2
VBST2
LL2
DRVL2
CSP2
CSN2
DRVH1
VBST1
LL1
DRVL1
CSP1
CSN1
PGND
DROOP
VREF
SLEW
THRM
TONSEL
TRIPSEL
OSRSEL
PU
V5FILT
VFB
GFB
IMON
PWPd
GND
TPAD
51728_DRVH2
51728_VBST2
51728_LL2
51728_DRVL2
51728_CSP2
51728_CSN2
51728_DRVH1
51728_VBST1
51728_LL1
51728_DRVL1
51728_CSP1
51728_CSN1
51728_TONSEL
51728_TRIPSEL
51728_OSRSEL
51728_V5FILT
51728_DROOP
51728_VREF
51728_SLEW
51728_IMON
51728_VFB
51728_GFB
PC77 EV@68p/50V_4
PC76 EV@1200p/50V_4
PR86 EV@8.2K/F_4
PC163 EV@0.22u/10V_6
PR225 *EV@0_4
PR220 EV@316K/F_4
PR202 EV@100K/F_4_3540NTC
PR95 EV@4.02K/F_4
PR211 *EV@0_4
PR218 *EV@0_4
PR221 *Short_4
THRM=0.75V/60uA=12.5K
PR205 *Short_4
PR72 Short_4
PR70 *EV@0_4
PC157 EV@2.2u/10V_6
PR212 *EV@0_4
PR206 *EV@0_4
PR228 *Short_6
PR91 EV@16.5K/F_4
PC75 EV@3300p/50V_4
PC78 EV@1n/50V_4
PC79 EV@1n/50V_4
+VGPU_CORE
PR183 EV@100_4
PR181 EV@100_4
PR229 *Short_4
PR232 *Short_4
[19] GPUVDDC_SENSE
[19] GPUVSS_SENSE
Parallel
Close to the GPU side.
C-Test
VIN
PR67 EV@2.2/F_6
51728_VBST2
PC152 EV@0.22u/25V_6
51728_DRVH2
PR203 *EV@10K/F_4
51728_LL2
51728_DRVL2
PQ45 EV@AON6414AL
PQ43 EV@AON6752
PL3 EV@0.24uH_7X7X3
DCR=1.1mOhm
+VGPU_CORE
PC67 EV@0.1u/50V_6
PC56 EV@4.7u/25V_8
PC55 EV@4.7u/25V_8
PC58 EV@2200p/50V_4
PR46 EV@2.2_6
PC44 EV@1000p/50V_6
PR192 EV@24.9K/F_4
*Short_4
PR191
PC22 EV@0.1u/10V_4
PC29 EV@10u/6.3V_8
PC28 EV@330u/2V_7343
51728_CSP2
51728_CSN2
PC159 *EV@0.1u/25V_4
PC160 *EV@0.1u/25V_4
PC142 EV@0.015u/16V_4
PR230 EV@29.4K/F_4
PR195 EV@86.6K/F_4
PR187 EV@100K/F_4_3540NTC
Close to the VR side.
C-Test
VIN
PR68 EV@2.2/F_6
51728_VBST1
PC153 EV@0.22u/25V_6
51728_DRVH1
PR204 *EV@10K/F_4
51728_LL1
51728_DRVL1
PQ46 EV@AON6414AL
PQ47 EV@AON6752
PL6 EV@0.24uH_7X7X3
DCR=1.1mOhm
+VGPU_CORE
PC63 EV@0.1u/50V_6
PC64 EV@4.7u/25V_8
PC68 EV@4.7u/25V_8
PC69 EV@2200p/50V_4
1/31 Delet PC151 for SMT open issue
PR75 EV@2.2_6
PC70 EV@1000p/50V_6
PR50 EV@24.9K/F_4
*Short_4
PR42
PC18 EV@0.1u/10V_4
PC40 EV@10u/6.3V_8
PC33 EV@330u/2V_7343
PC127 EV@330u/2.5V_6X4.2
51728_CSP1
51728_CSN1
PC162 *EV@0.1u/25V_4
PC161 *EV@0.1u/25V_4
PC43 EV@0.015u/16V_4
PR231 EV@29.4K/F_4
PR45 EV@86.6K/F_4
PR201 EV@100K/F_4_3540NTC
Close to the VR side.
+VGPU_CORE
Countinue current:30A
Peak current:40.5A
OCP minimum 50A
Loadline=0mV/A
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PROJECT : ZRI/ZQI
Size
Document Number
+VGPU CORE(TPS51728)
Rev A1A
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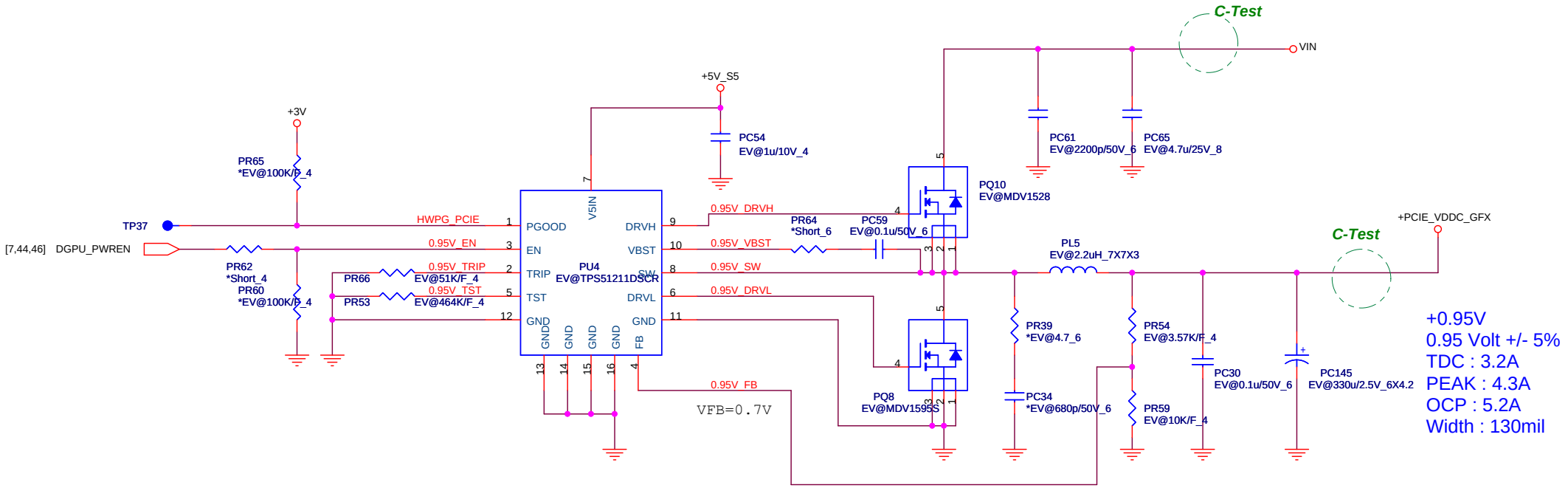

+0.95V
0.95 Volt +/- 5%
TDC : 3.2A
PEAK : 4.3A
OCP : 5.2A
Width : 130mil

OCP=5.2A
L ripple current
=(19-0.95)*0.95/(2.2u*290k*19)
=1.415A
Vtrip=5.2-(1.415/2)*14mohm
=0.06289V
Rlimit=0.06289/10uA*8=50.318Kohm

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PROJECT : ZRI/ZQI		
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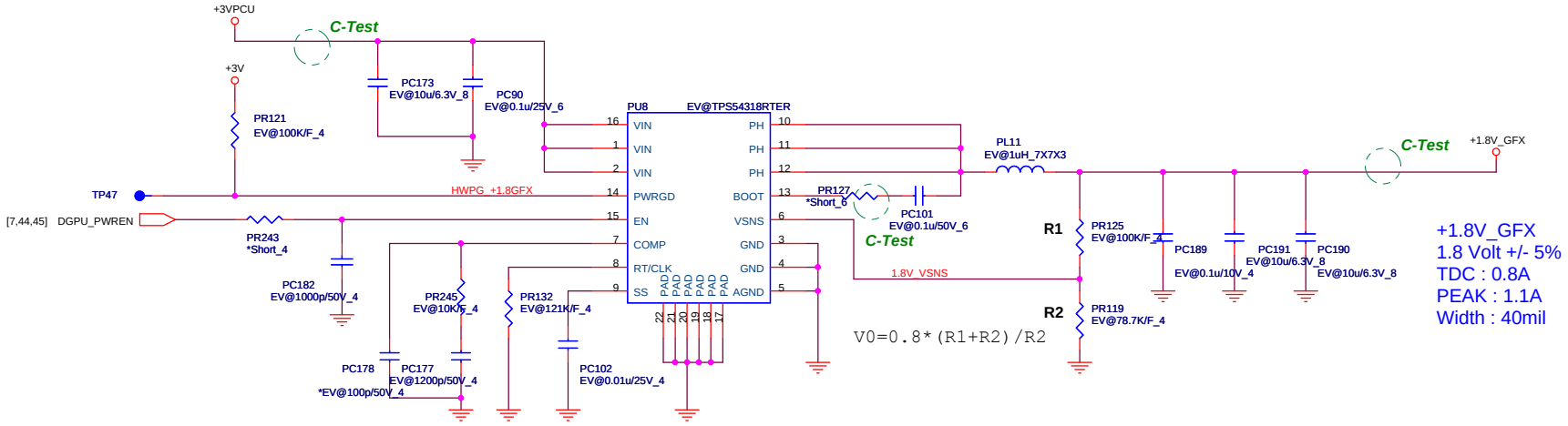

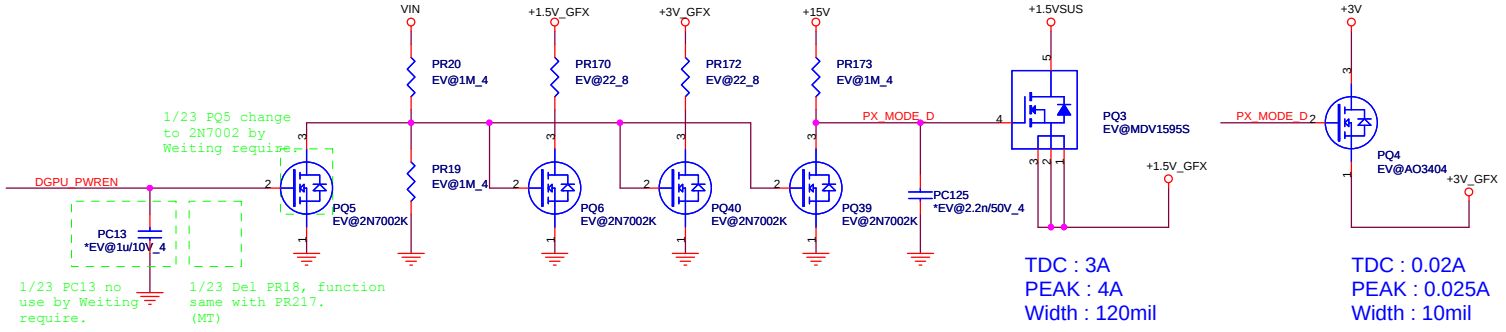

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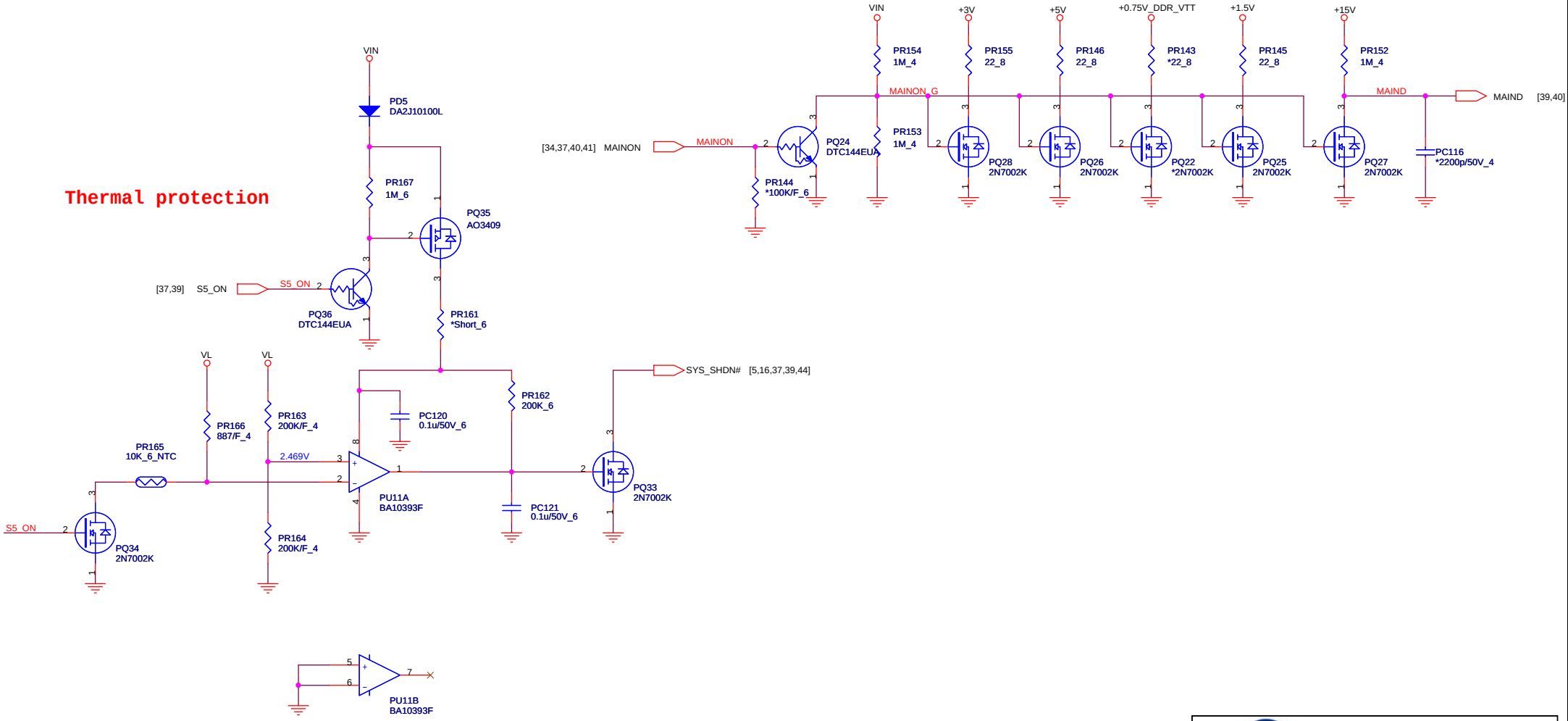
Size	Document Number: GPU_POWER/+1.8V_GPU	Rev: A1A
Date: Wednesday, April 24, 2013	Sheet 46 of 50	



For EC control thermal protection (output 3.3V)

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	Discharge/Thermal	A1A
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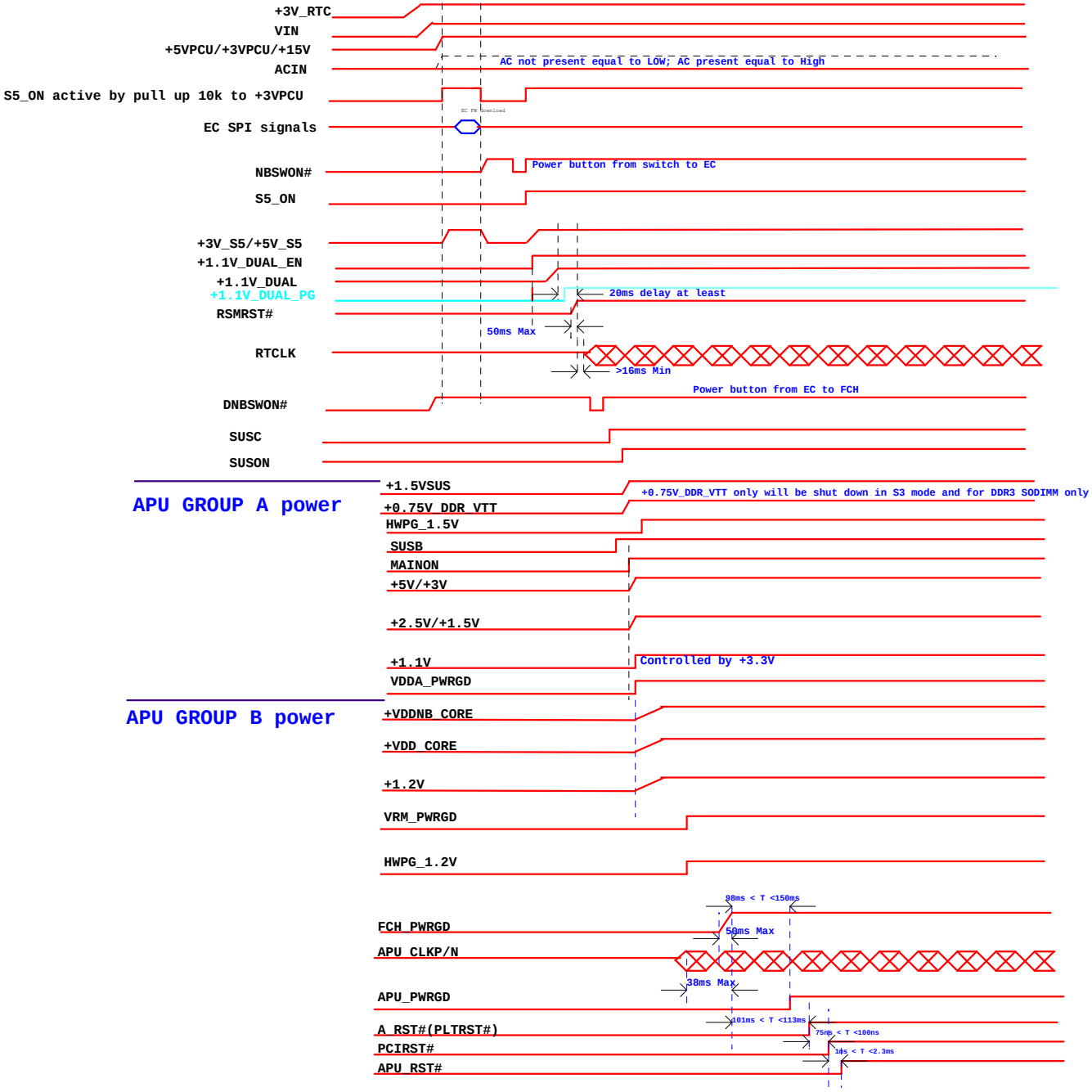
ZRP Power On Sequence: S5 > S0

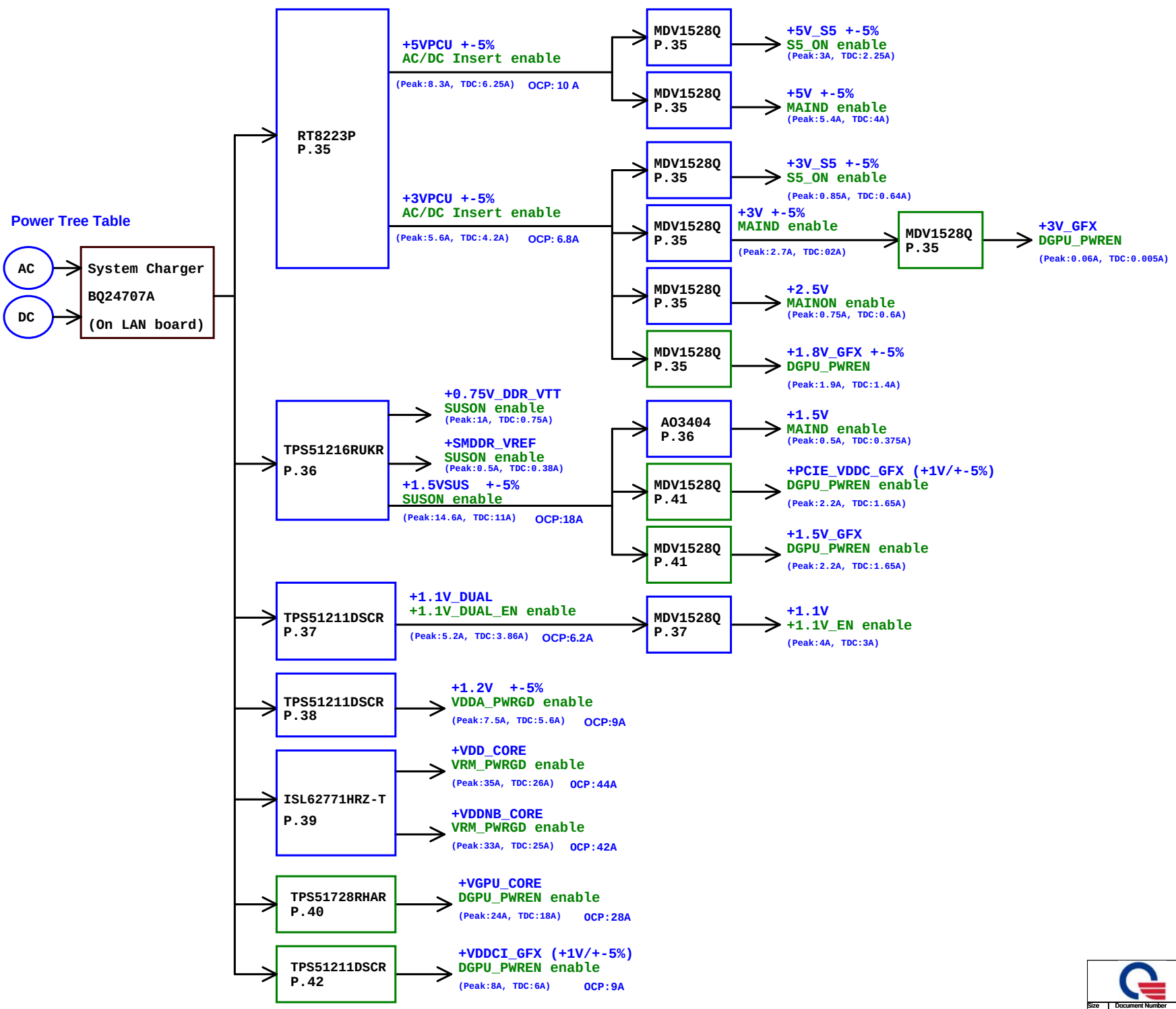


APU Power on sequence required:

Llano APU:
1.Group A (+1.5VSUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_S5,+3V ramping down time > 300us
4.100uS <= +3V_S5,+3V <= 40mS
5.100uS <= All power rails except +3V_S5,+3V <= 40mS

Power Tree Table



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PROJECT : ZRI/ZQI

Size	Document Number	Rev
	Power Tree	A1A

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