ZZZ1
LA5972P_LS5971P_LS5083P

ZZZ3
LA5972P
DAZ@

ZZZ4
LS5971P
DAZ@

ZZZ5
LS5083P
DAZ@

Compal Confidential

NAWA2 Schematics Document

AMD Tigris: Caspian Processor with RS880M/SB710/Park-S3 & M93-S3

2009-11-26

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Title: Cover Page

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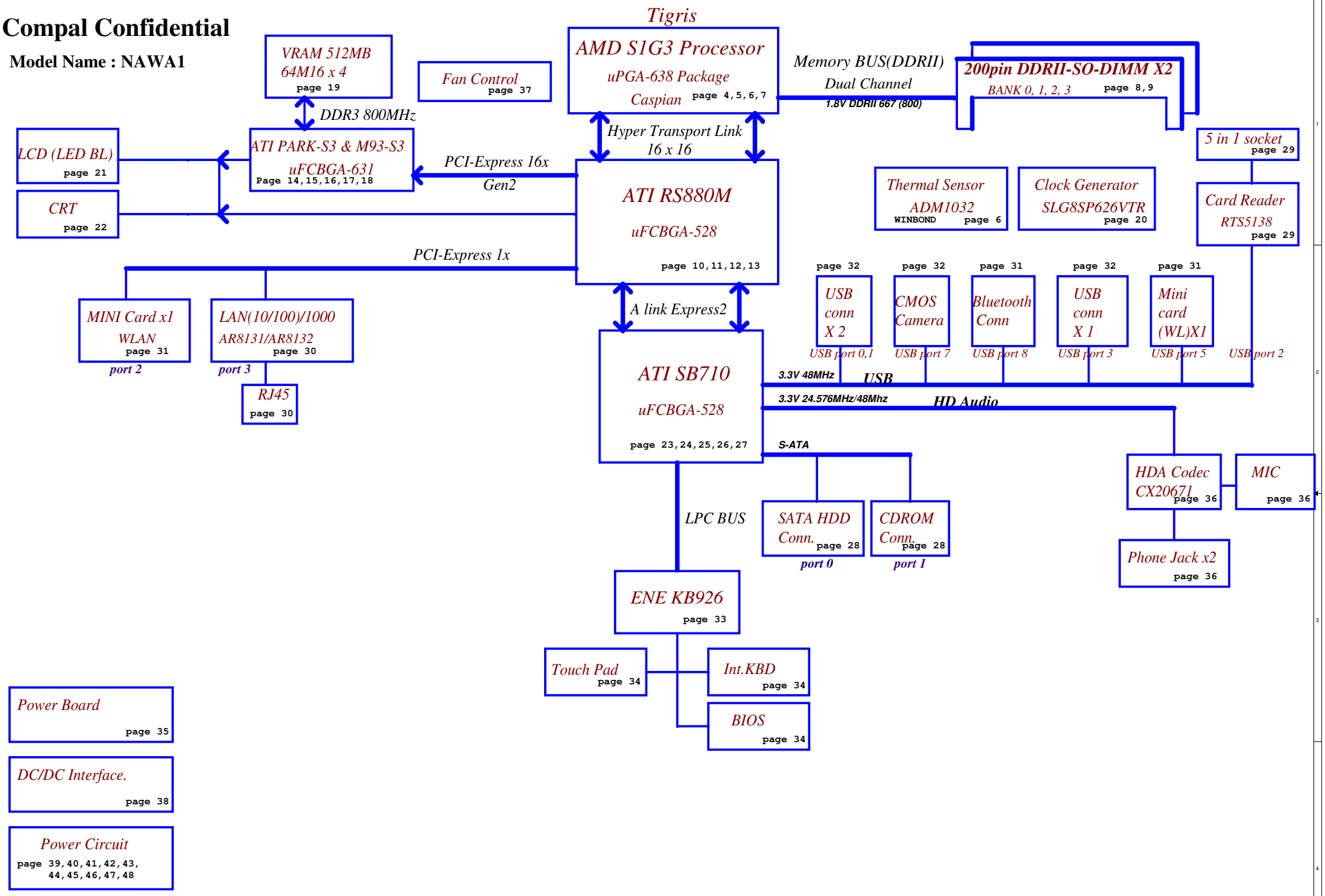
Compal Confidential

Model Name : NAWA1



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

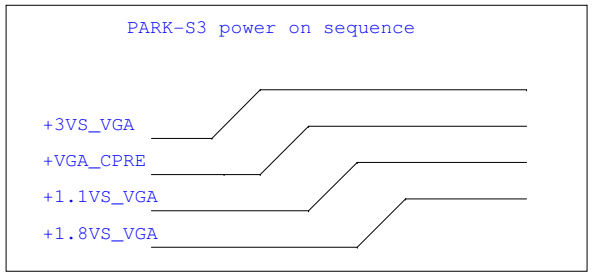
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

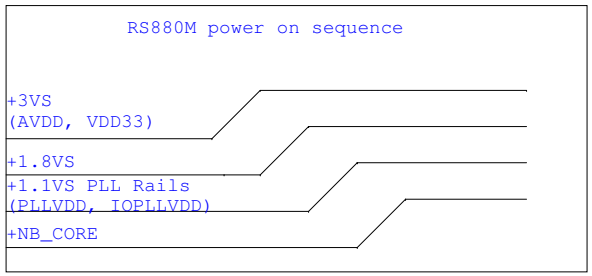
BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
PARK	PARK@
M93	M93@
HDT debug	HDT@
UMA	UMA@
Wireless LAN	WLAN@
Blue Tooth	BT@
Camera	CMOS@
New Card	New Card@
VRAM	X76@
UNPON	@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

NAWA1_UMA : UMA@/WLAN@/BT@/CMOS@/NEW CARD@
NAWA1_DIS : VGA@/M93@/WLAN@/BT@/NEW CARD@/CMOS@/X76@





External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
GMT G781-1 (GPU)	1001 101X b	9AH
SB-Temp Sensor		9CH

SB710 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB710 SM Bus 1 address

Device	Address
New card	

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Title: Notes List

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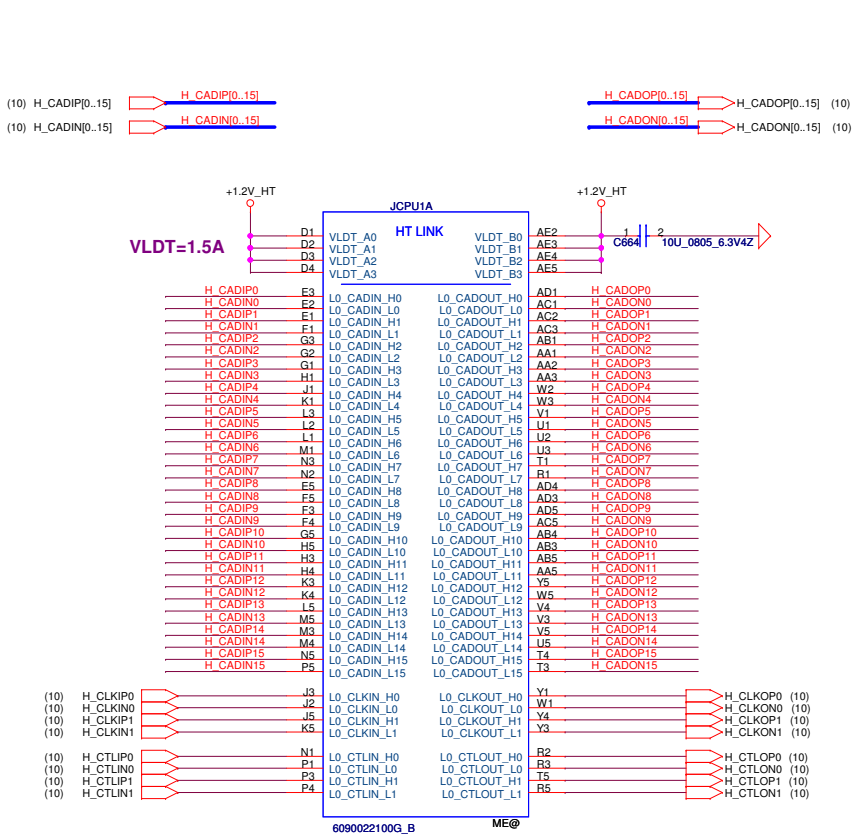

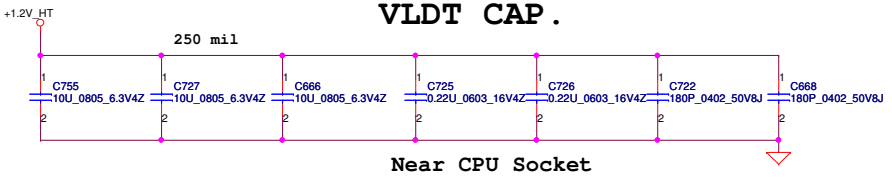

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Title: AMD CPU S1G3 HT I/F

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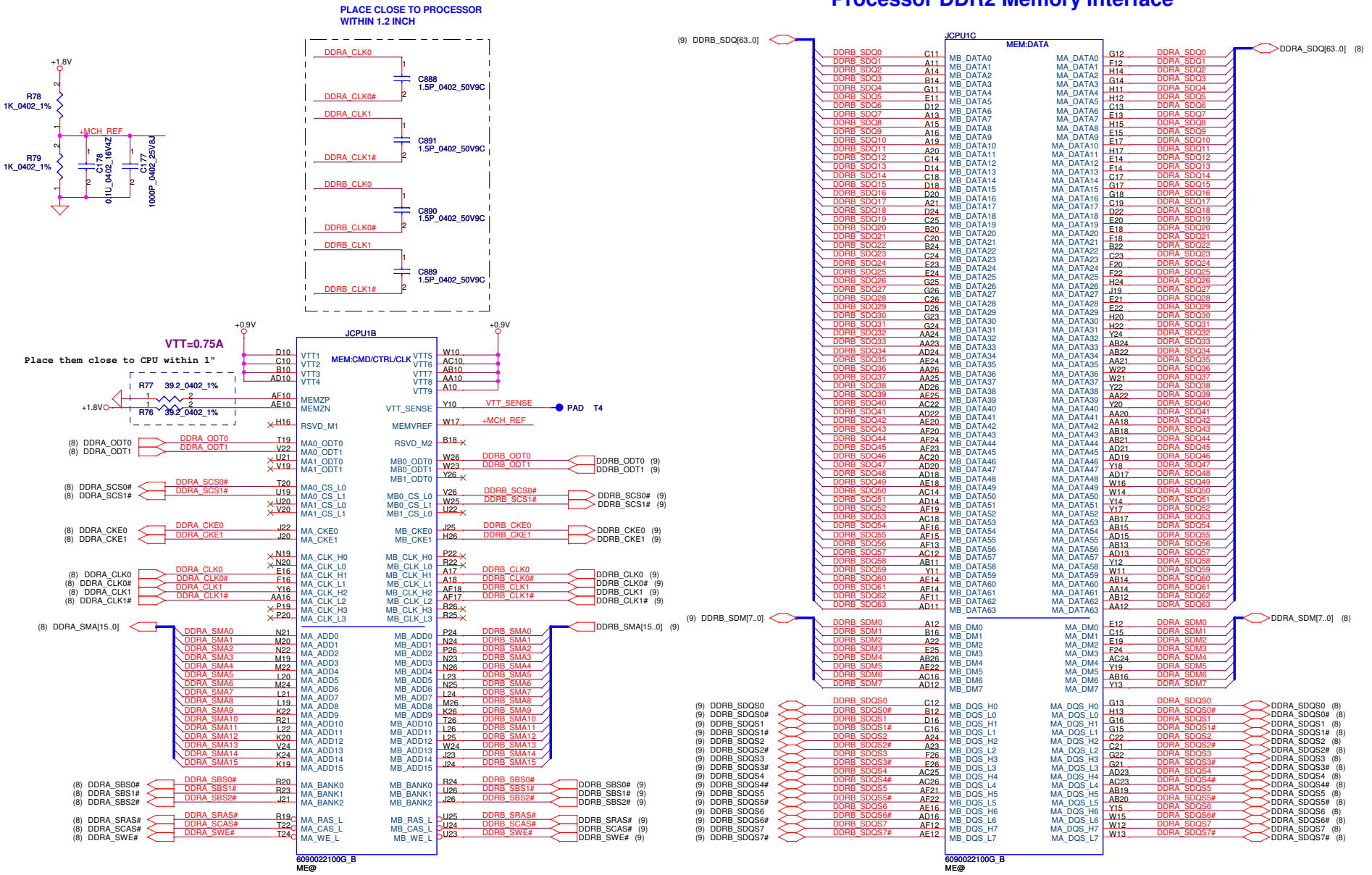
Processor DDR2 Memory Interface



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Compal Electronics, Inc.

Title: AMD CPU S1G3 DDRII I/F

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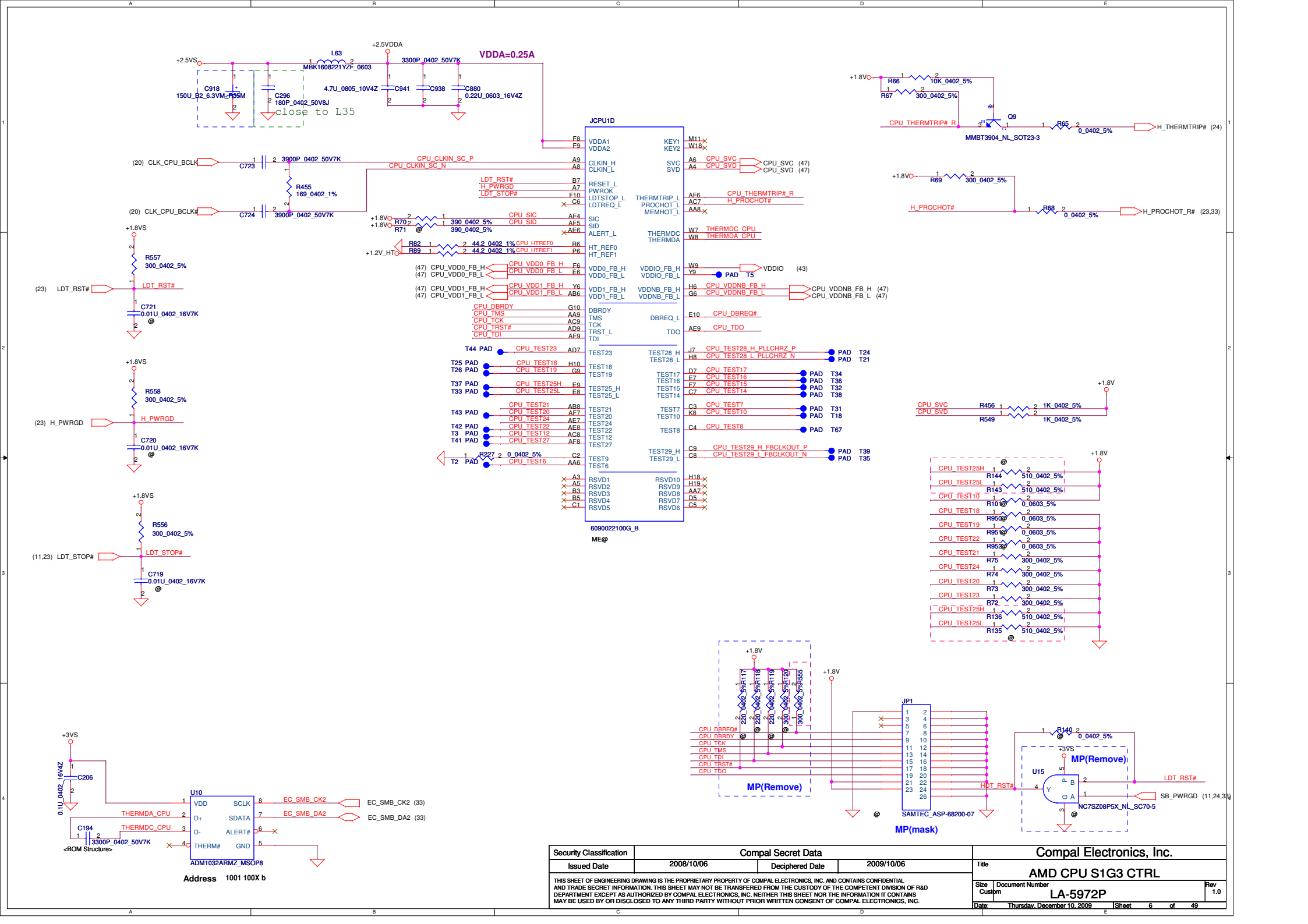

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Compal Electronics, Inc.

Title: AMD CPU S1G3 CTRL

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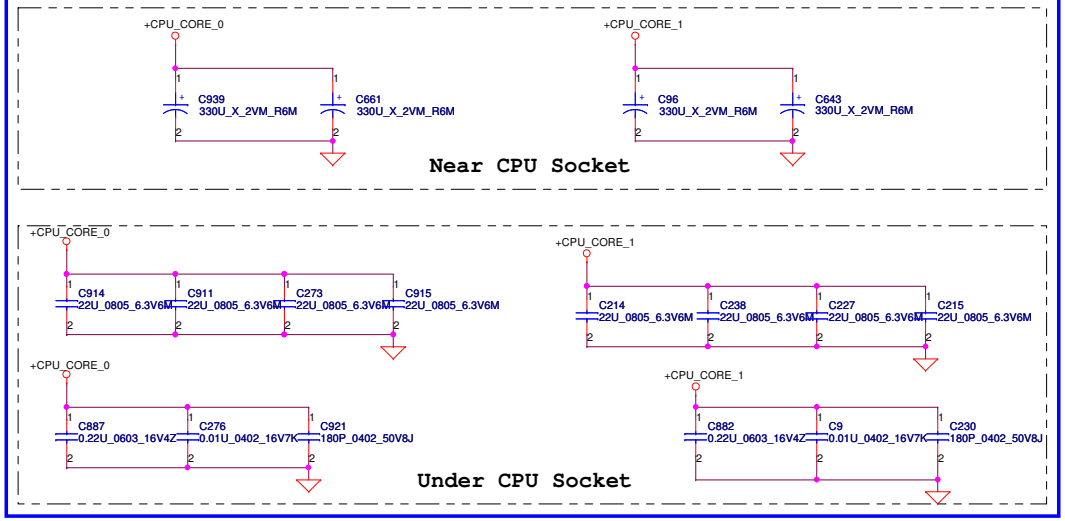
VDD (+CPU_CORE) decoupling.

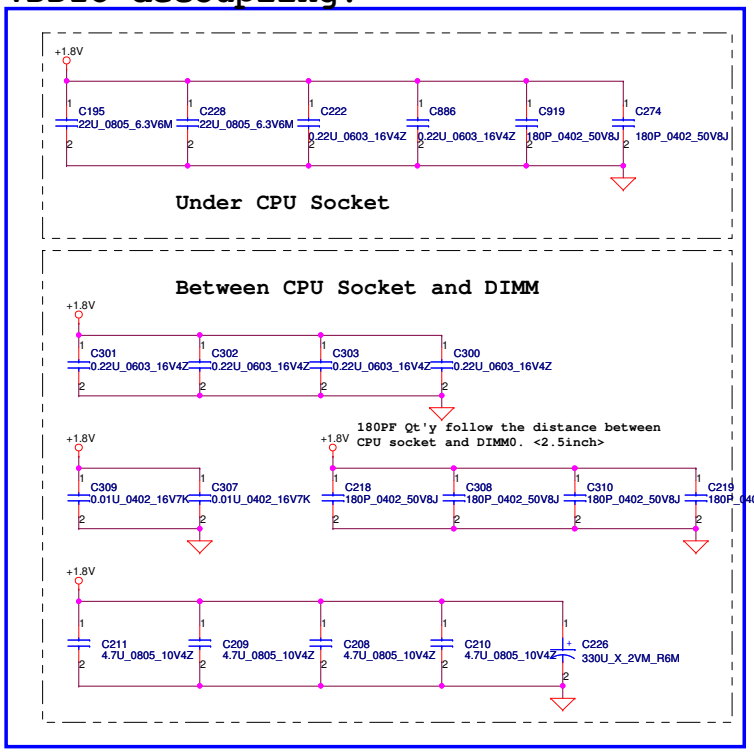


VDD0 = 18A

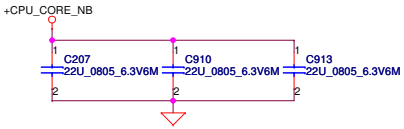
VDD1 =18A



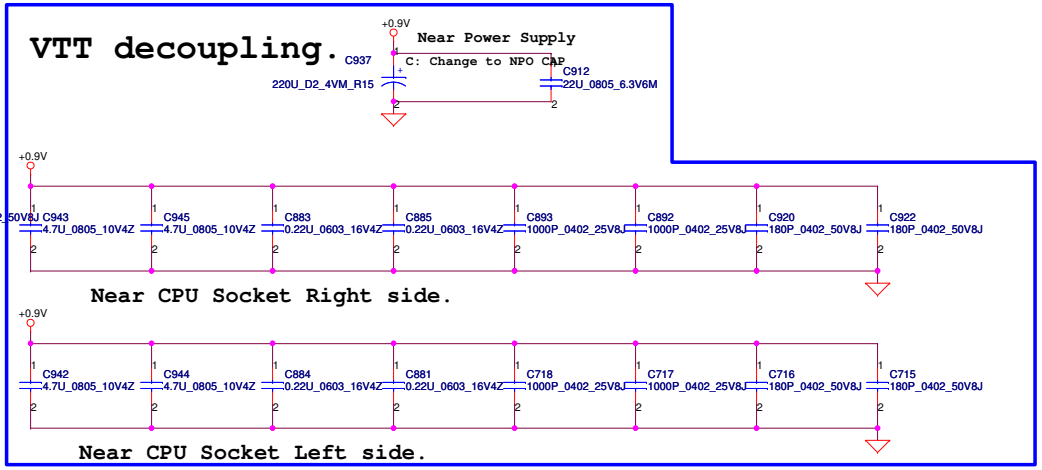
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



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Title: AMD CPU S1G3 PWR & GND

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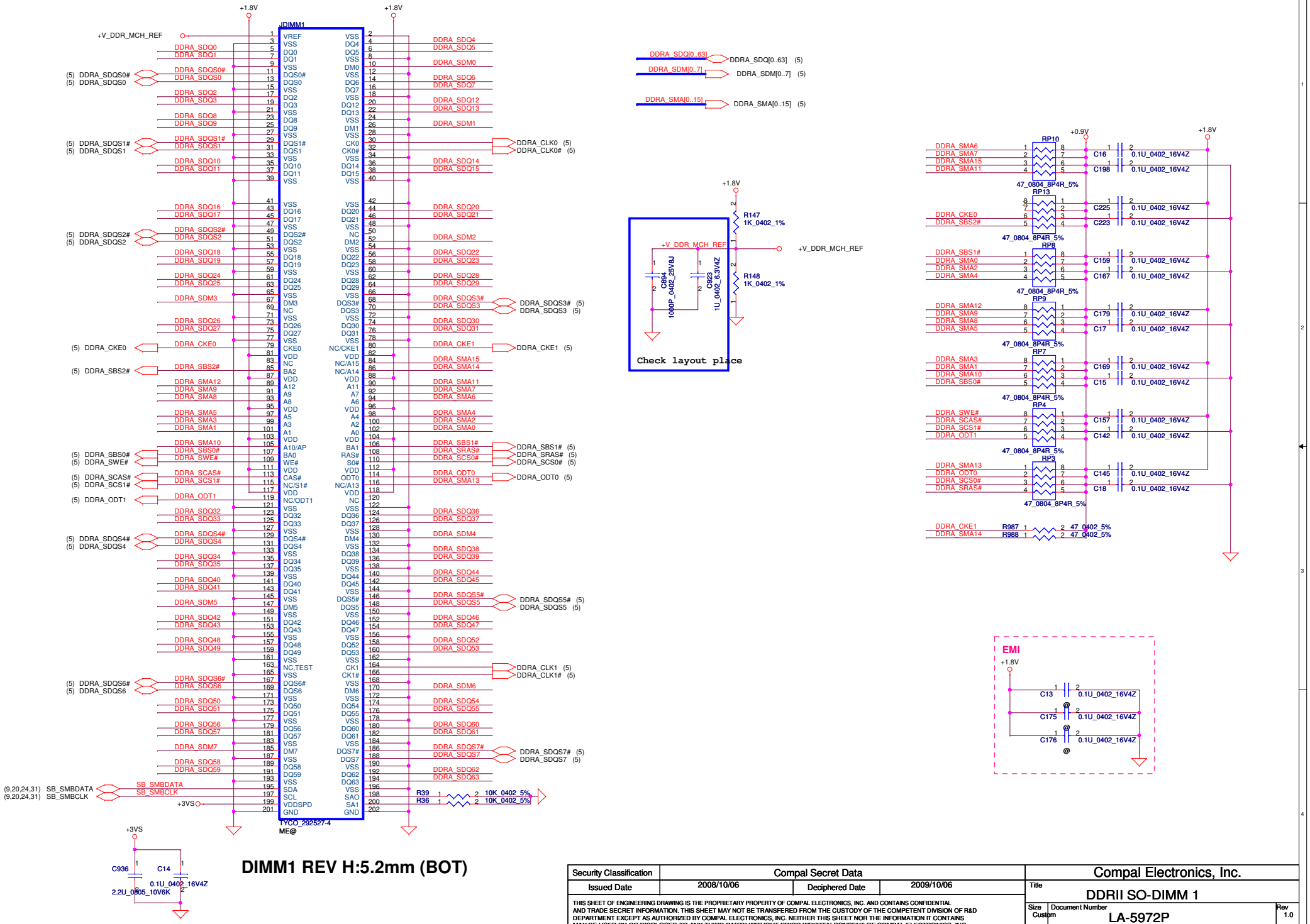

DIMM1 REV H:5.2mm (BOT)

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Title: DDRII SO-DIMM 1

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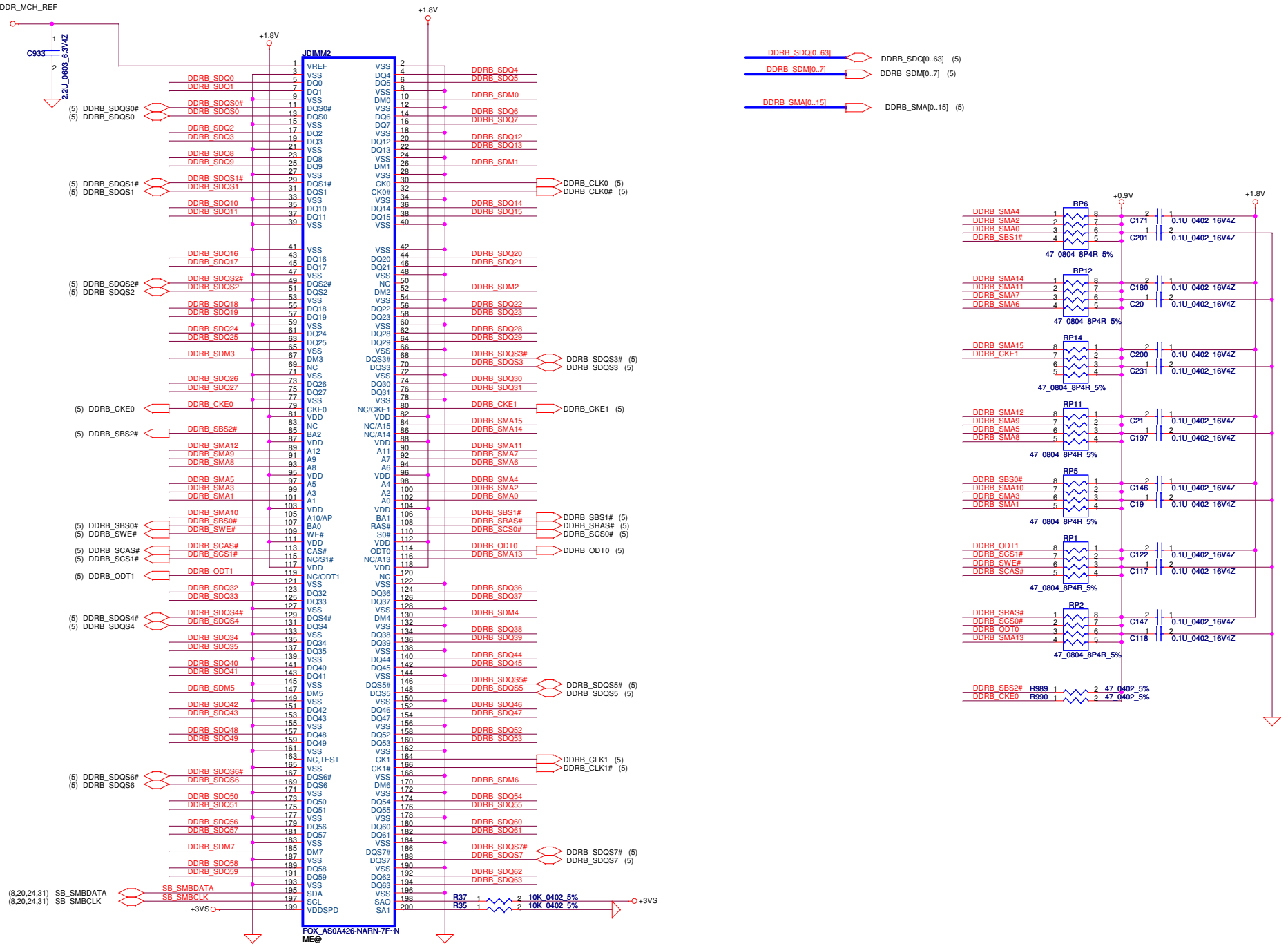

DIMM2 REV H:9.2mm (BOT)

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Title: DDRII SO-DIMM 2

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(14) PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]
(14) PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] (14)
PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] (14)

U20B

PART 2 OF 6

PCIE I/F GFX

PCIE_GTX_C_MRX_P0	D4	GFX_RX0P	GFX_TX0P	A5	PCIE_MTX_GRX_P0		C358 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P0
PCIE_GTX_C_MRX_N0	C4	GFX_RX0N	GFX_TX0N	B5	PCIE_MTX_GRX_N0	C646 1 2	VGA@ 0.1U 0402 10V7K	PCIE_MTX_C_GRX_N0
PCIE_GTX_C_MRX_P1	A3	GFX_RX1P	GFX_TX1P	A4	PCIE_MTX_GRX_P1		C649 1 2	VGA@ 0.1U 0402 10V7K PCIE_MTX_C_GRX_P1
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PCIE I/F GPP

	AE3	GPP_RX0P	GPP_TX0P	AC1			WLAN@
	AD4	GPP_RX0N	GPP_TX0N	AC2			WLAN@
(31) PCIE_PTX_C_IRX_P1	AE2	GPP_RX1P	GPP_TX1P	AB4	PCIE_ITX_PRX_P1	C614 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_P1 (31)
(31) PCIE_PTX_C_IRX_N1	AD3	GPP_RX1N	GPP_TX1N	AB3	PCIE_ITX_PRX_N1	C362 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_N1 (31)
(30) PCIE_PTX_C_IRX_P2	AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_ITX_PRX_P2	C357 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_P2 (30)
(30) PCIE_PTX_C_IRX_N2	AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_ITX_PRX_N2	C618 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_N2 (30)
	V5	GPP_RX3P	GPP_TX3P	Y1			
	W6	GPP_RX3N	GPP_TX3N	Y2			
(31) PCIE_PTX_C_IRX_P4	U5	GPP_RX4P	GPP_TX4P	Y4	PCIE_ITX_PRX_P4	C964 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_P4 (31)
(31) PCIE_PTX_C_IRX_N4	U6	GPP_RX4N	GPP_TX4N	Y3	PCIE_ITX_PRX_N4	C965 1 2	0.1U 0402 10V7K PCIE_ITX_C_PRX_N4 (31)
	U8	GPP_RX5P	GPP_TX5P	V1			NEWCARD@
	U7	GPP_RX5N	GPP_TX5N	V2			NEWCARD@

WLAN
LAN
New Card

(4) H_CADOP[0..15] → H_CADOP[0..15] → H_CADIP[0..15] → H_CADIP[0..15] (4)
(4) H_CADON[0..15] → H_CADON[0..15] → H_CADIN[0..15] → H_CADIN[0..15] (4)

PCIE I/F SB

(23) SB_RX0P	AA8	SB_RX0P	SB_TX0P	AD7	SB_TX0P_C	C352 1 2	0.1U 0402 10V7K SB_TX0P (23)
(23) SB_RX0N	Y8	SB_RX0N	SB_TX0N	AE7	SB_TX0N_C	C609 1 2	0.1U 0402 10V7K SB_TX0N (23)
(23) SB_RX1P	AA7	SB_RX1P	SB_TX1P	AE6	SB_TX1P_C	C38 1 2	0.1U 0402 10V7K SB_TX1P (23)
(23) SB_RX1N	Y7	SB_RX1N	SB_TX1N	AD6	SB_TX1N_C	C33 1 2	0.1U 0402 10V7K SB_TX1N (23)
(23) SB_RX2P	AA5	SB_RX2P	SB_TX2P	AB6	SB_TX2P_C	C37 1 2	0.1U 0402 10V7K SB_TX2P (23)
(23) SB_RX2N	AA6	SB_RX2N	SB_TX2N	AC6	SB_TX2N_C	C32 1 2	0.1U 0402 10V7K SB_TX2N (23)
(23) SB_RX3P	W5	SB_RX3P	SB_TX3P	AD5	SB_TX3P_C	C610 1 2	0.1U 0402 10V7K SB_TX3P (23)
(23) SB_RX3N	Y5	SB_RX3N	SB_TX3N	AE5	SB_TX3N_C	C616 1 2	0.1U 0402 10V7K SB_TX3N (23)

PCE_CALRP(PCE_BCALRP) AC8 R32 1 2 1.27K 0402 1%
PCE_CALRN(PCE_BCALRN) AB8 R267 1 2 2K 0402 1% → +1.1VS

RS880M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

U20A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

H_CADOP0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	H_CADIP0
H_CADON0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	H_CADIN0
H_CADOP1	Y22	HT_RXCAD1P	HT_TXCAD1P	E24	H_CADIP1
H_CADON1	Y23	HT_RXCAD1N	HT_TXCAD1N	E25	H_CADIN1
H_CADOP2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	H_CADIP2
H_CADON2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	H_CADIN2
H_CADOP3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	H_CADIP3
H_CADON3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	H_CADIN3
H_CADOP4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	H_CADIP4
H_CADON4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	H_CADIN4
H_CADOP5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	H_CADIP5
H_CADON5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	H_CADIN5
H_CADOP6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	H_CADIP6
H_CADON6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	H_CADIN6
H_CADOP7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	H_CADIP7
H_CADON7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	H_CADIN7
H_CADOP8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	H_CADIP8
H_CADON8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	H_CADIN8
H_CADOP9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	H_CADIP9
H_CADON9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	H_CADIN9
H_CADOP10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	H_CADIP10
H_CADON10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	H_CADIN10
H_CADOP11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	H_CADIP11
H_CADON11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	H_CADIN11
H_CADOP12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	H_CADIP12
H_CADON12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	H_CADIN12
H_CADOP13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	H_CADIP13
H_CADON13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	H_CADIN13
H_CADOP14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	H_CADIP14
H_CADON14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	H_CADIN14
H_CADOP15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	H_CADIP15
H_CADON15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	H_CADIN15
(4) H_CLKOP0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	H_CLKIP0 (4)
(4) H_CLKON0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	H_CLKIN0 (4)
(4) H_CLKOP1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	H_CLKIP1 (4)
(4) H_CLKON1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	H_CLKIN1 (4)
(4) H_CTLOP0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	H_CTLIP0 (4)
(4) H_CTLON0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	H_CTLIN0 (4)
(4) H_CTLOP1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	H_CTLIP1 (4)
(4) H_CTLON1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	H_CTLIN1 (4)
	C23	HT_RXCALP	HT_TXCALP	B24	
	A24	HT_RXCALN	HT_TXCALN	B25	

R56 1 2 301_0402_1%
0718 Place within 1" layout 1:2

R51 1 2 301_0402_1%
0718 Place within 1" layout 1:2

RS880M_FCBGA528

SA00002DR30 S IC 216-0674026 A13 RS780MN FCBGA 0FA
SA000032710 S IC 216-0752001 A11 RS880M FCBGA528 0FA

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: RS880-HT/PCIE

Size	Document Number	Rev
Custom	LA-5972P	1.0

Date: Thursday, December 10, 2009 Sheet 10 of 49

For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor

PLLVDD=65mA
AVDD=0.11A
AVDDDI=20mA
PLLVDD18=20mA
AVDDQ=4mA
VDDA18HTPLL=20mA
VDDA18PCIEPLL=0.12A
VDDLTP18=15mA
VDDLT18=0.3A

U20C — RS880M_FCBGA528

	POWER_SEL
HIGH	1.0V
LOW	1.1V

Strap pin

Strap pin

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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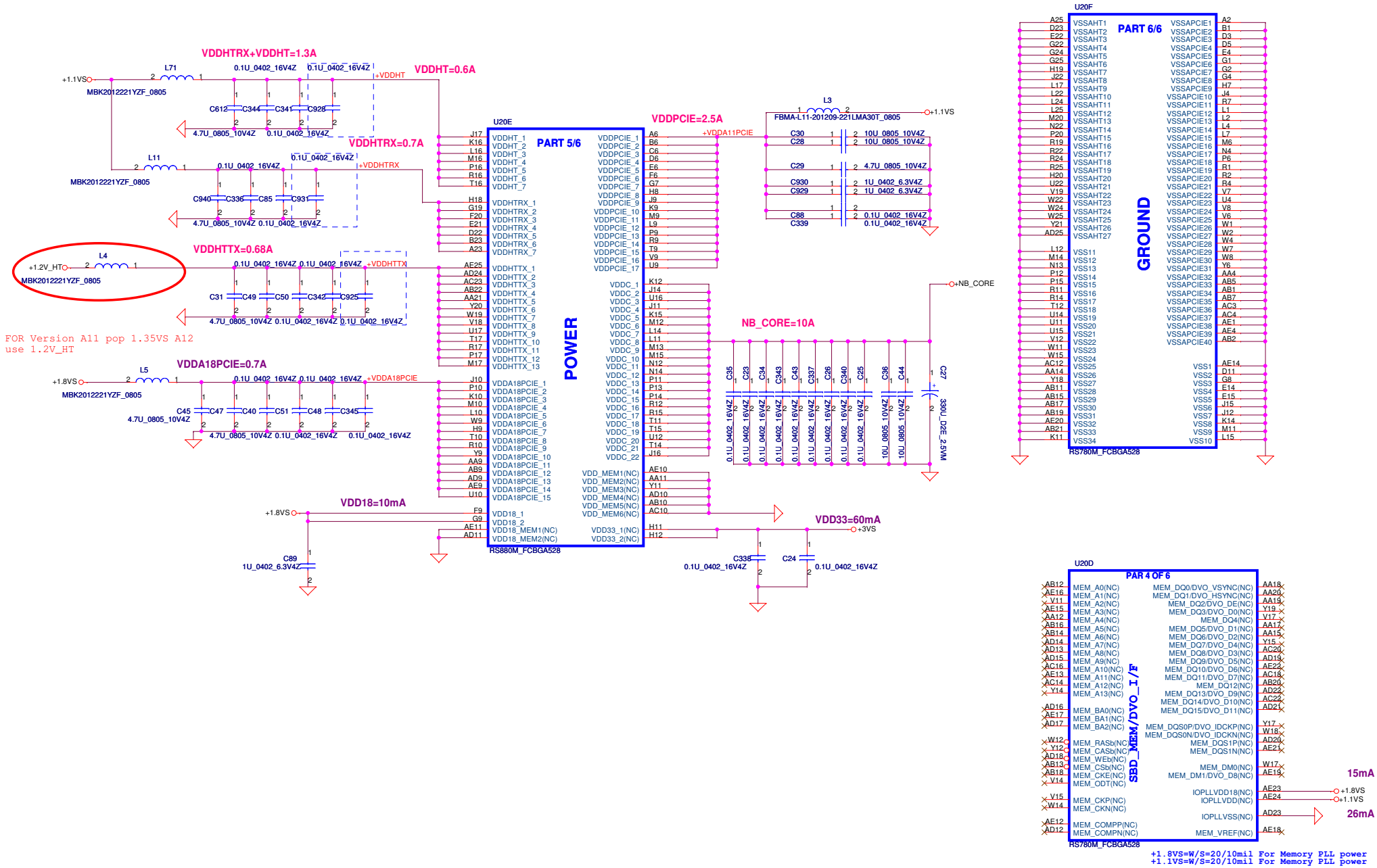
Compal Electronics, Inc.

Title: RS880 VEDIO/CLK GEN

Size: Custom | Document Number: LA-5972P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 11 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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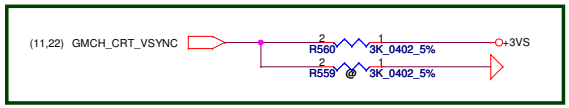
Compal Electronics, Inc.

Title: RS880 PWR/GND

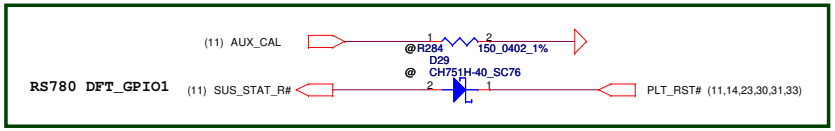
Size: Custom | Document Number: LA-5972P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 12 of 49



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

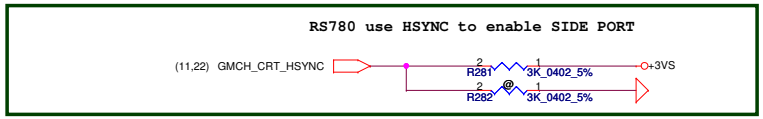
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS880m)
0 : Enable (RS880M)
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```

RS780 use HSYNC to enable SIDE PORT



RS780 use HSYNC to enable SIDE PORT

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.   Enable (RS880M)
1 :  Disable(RS880M)
```

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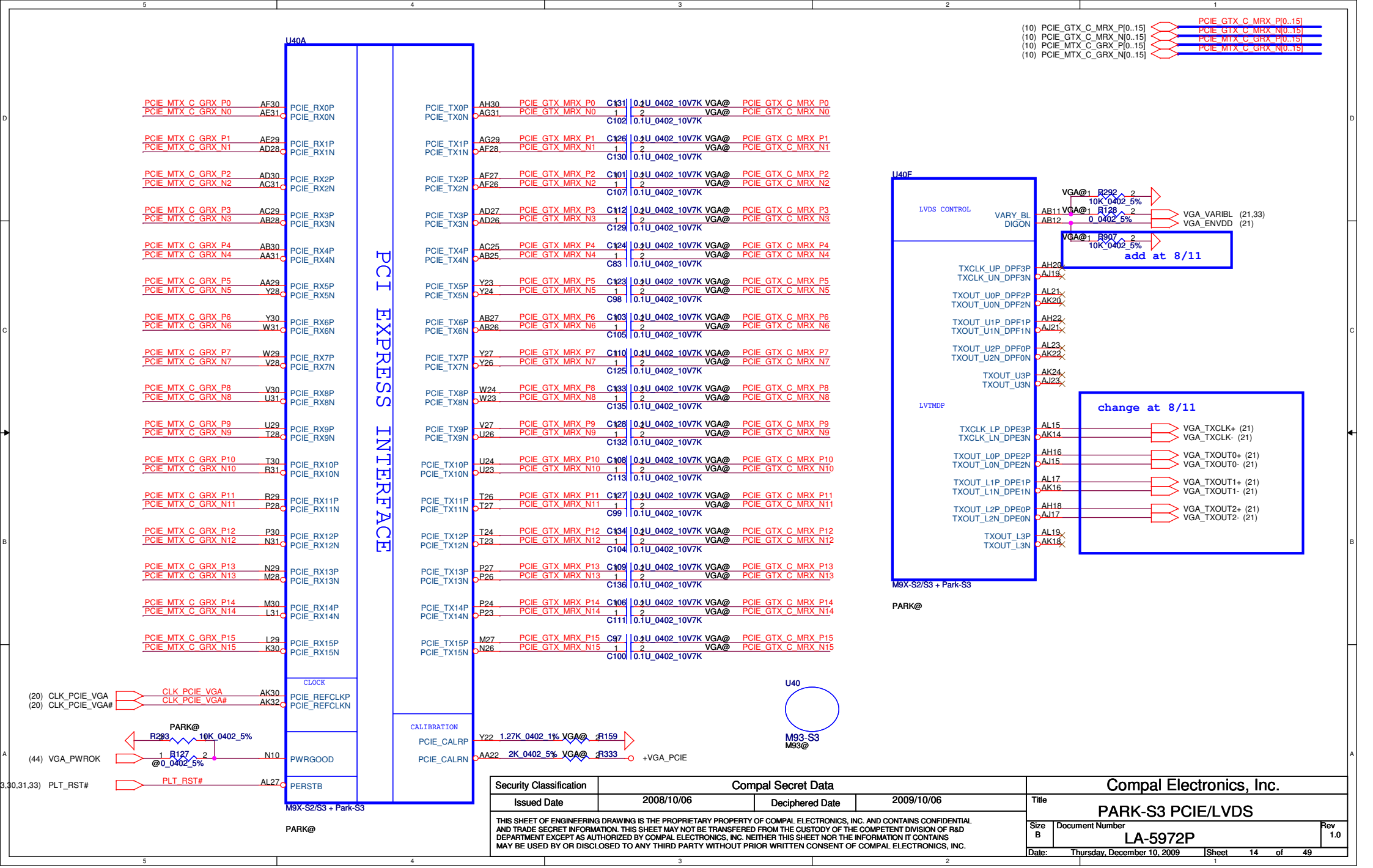
Compal Electronics, Inc.

Title: RS880 STRAPS

Size	Document Number	Rev
Custom	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 13 of 49



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Compal Electronics, Inc.

Title: PARK-S3 PCIE/LVDS

Size	Document Number	Rev
B	LA-5972P	1.0

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
	GPIO8		0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

STRAPS

GPU_GPIO0 R232 @ 10K_0402_5%
GPU_GPIO1 @R228 10K_0402_5%
GPU_GPIO2 @R215 10K_0402_5%
GPU_GPIO8 @R233 10K_0402_5%
GPU_GPIO9 @R231 10K_0402_5%
GPIO21_BBEN @R216 10K_0402_5%
GPU_GPIO11 R217 @ 10K_0402_5%
GPU_GPIO12 @R236 10K_0402_5%
GPU_GPIO13 @R234 10K_0402_5%
VGA_CRT_HSYNC @R229 10K_0402_5%
VGA_CRT_VSYNC @R230 10K_0402_5%
VGA_CRT_VSYNC2 @R295 10K_0402_5%
VGA_CRT_HSYNC2 @R108 10K_0402_5%
GPU_GPIO8 @R1018 10K_0402_5%

EMI request add at 8/17

add at 8/11

add at 8/11

08/11
Spread Spectrum For EMI

VGA Thermal Sensor G781-1P8F

Closed to GPU

Security Classification	Compal Secret Data
Issued Date	2008/10/06
Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: PARK-S3 Main Generic/MSIC

Size	Document Number	Rev
C	LA-5972P	1.0

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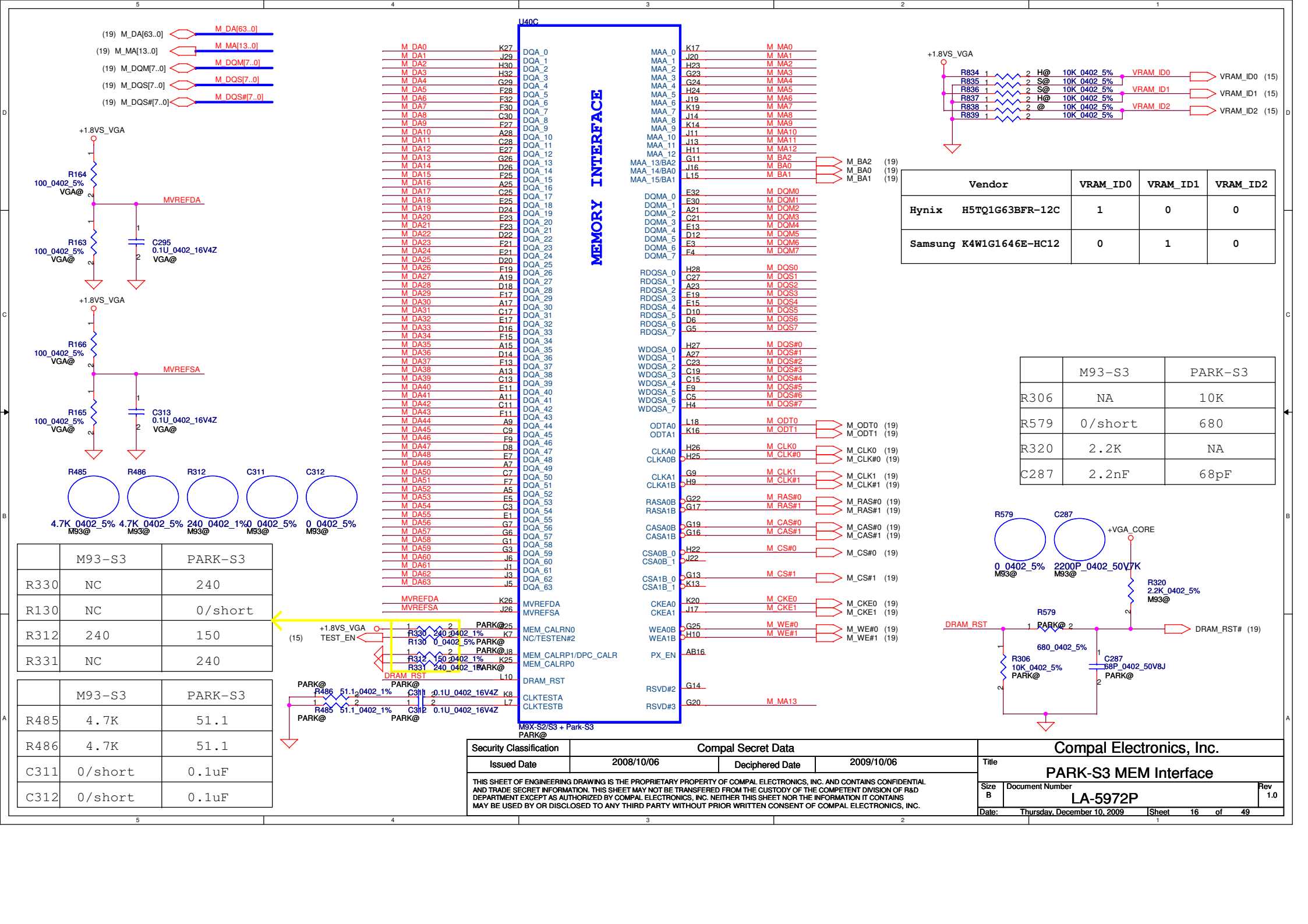

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix H5TQ1G63BFR-12C	1	0	0
Samsung K4W1G1646E-HC12	0	1	0

	M93-S3	PARK-S3
R306	NA	10K
R579	0/short	680
R320	2.2K	NA
C287	2.2nF	68pF

	M93-S3	PARK-S3
R330	NC	240
R130	NC	0/short
R312	240	150
R331	NC	240

	M93-S3	PARK-S3
R485	4.7K	51.1
R486	4.7K	51.1
C311	0/short	0.1uF
C312	0/short	0.1uF

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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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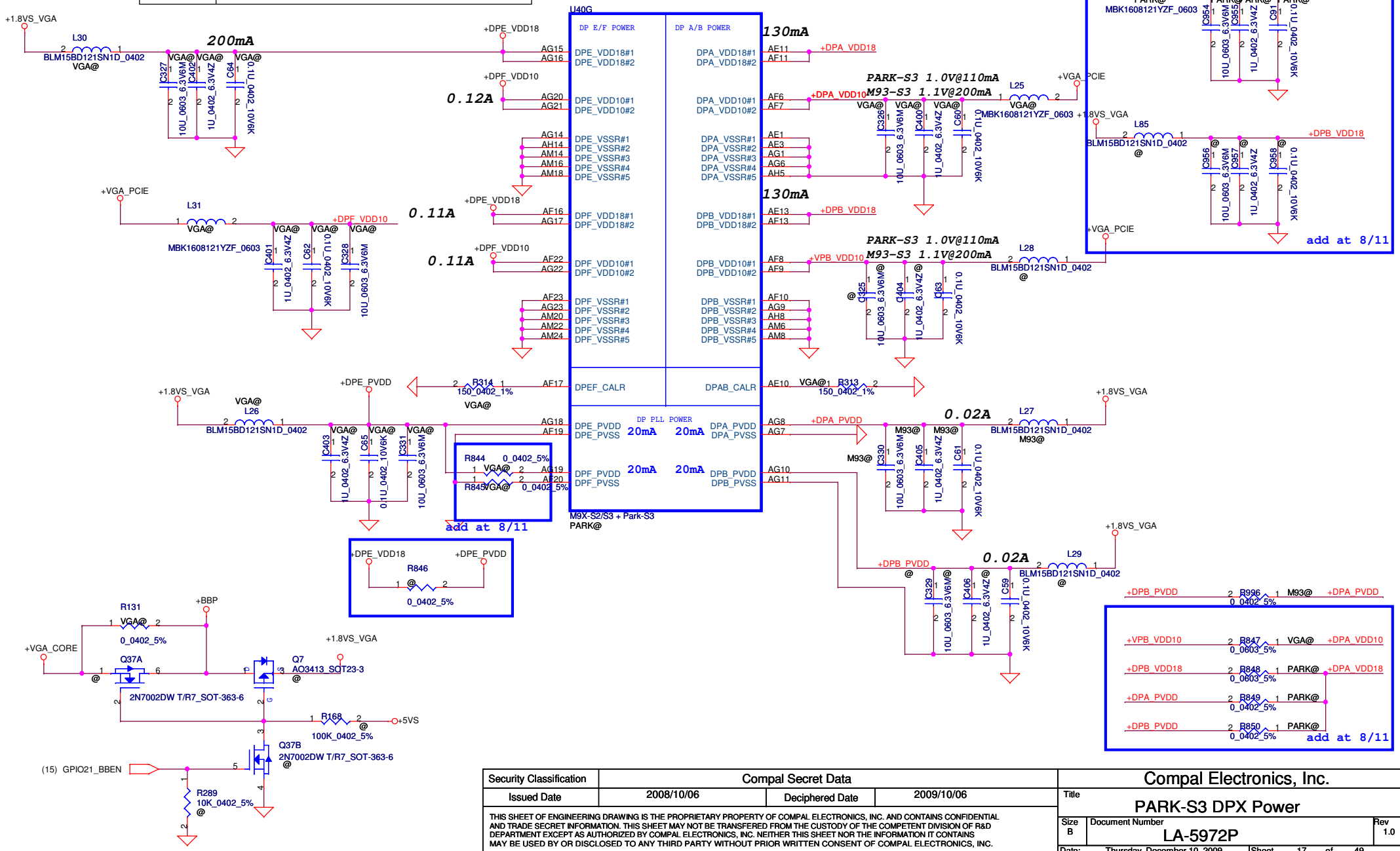
Compal Electronics, Inc.

Title: PARK-S3 MEM Interface

Size	Document Number	Rev
B	LA-5972P	1.0

Date: Thursday, December 10, 2009 Sheet 16 of 49

DPE_VDD10	Park-S3: TMDS/DP=110mA@1.0V : LVDS=120mA@1.0V
DPF_VDD10	M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V



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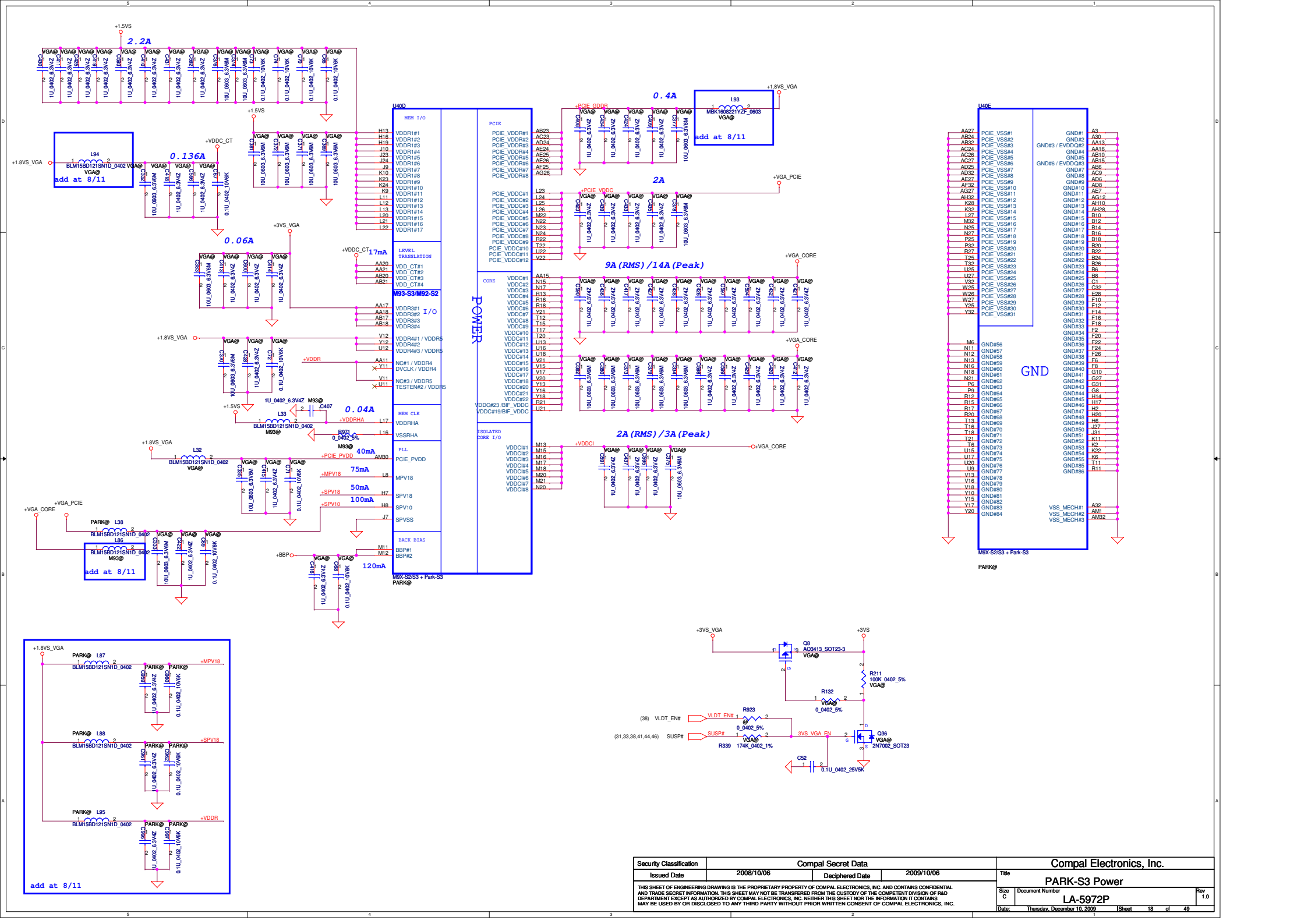
Compal Electronics, Inc.

Title: PARK-S3 DPX Power

Size	Document Number	Rev
B	LA-5972P	1.0

Date: Thursday, December 10, 2009 Sheet 17 of 49



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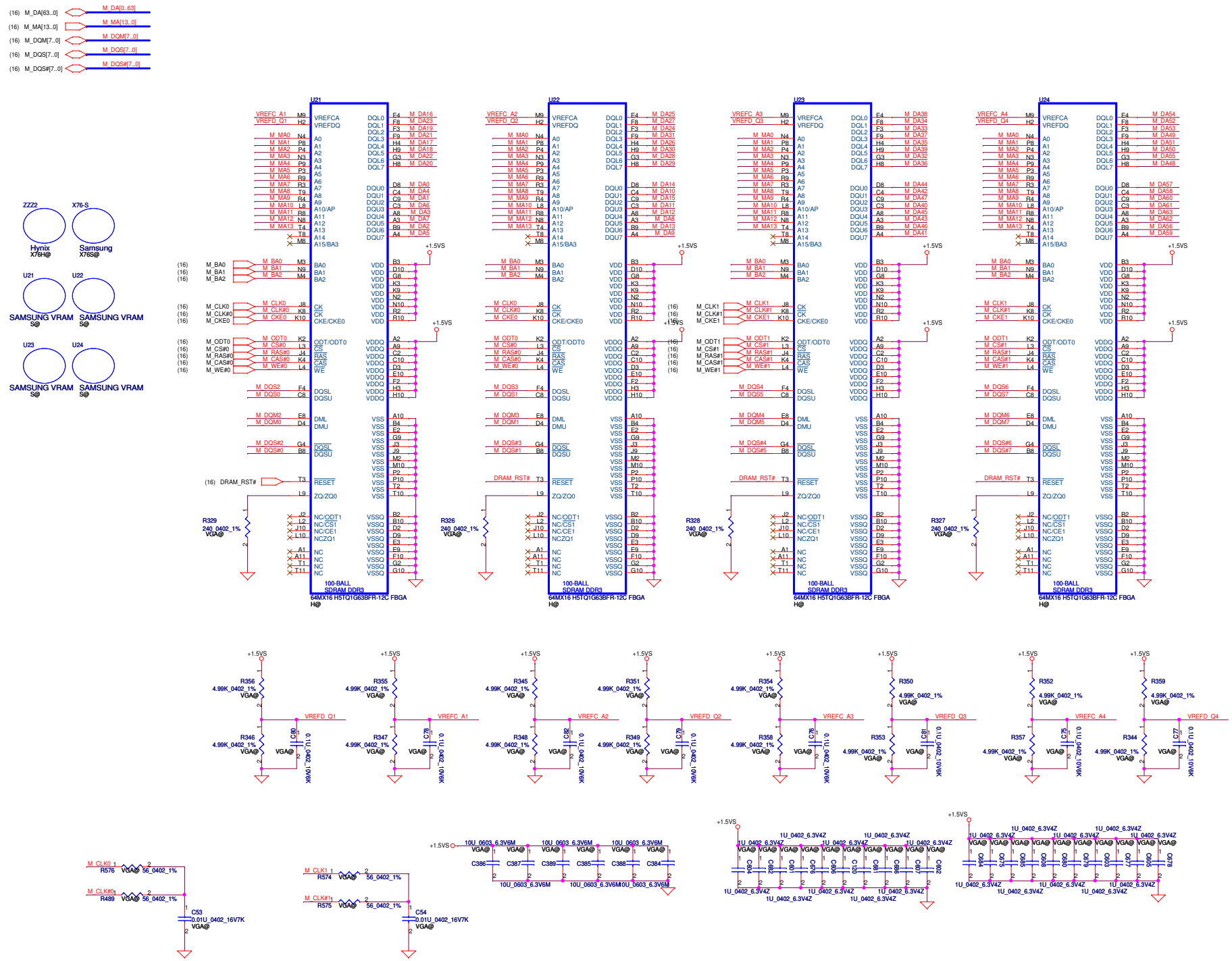
Compal Electronics, Inc.

Title: PARK-S3 Power

Size	Document Number	Rev
C	LA-5972P	1.0

Date: Thursday, December 10, 2009 Sheet 18 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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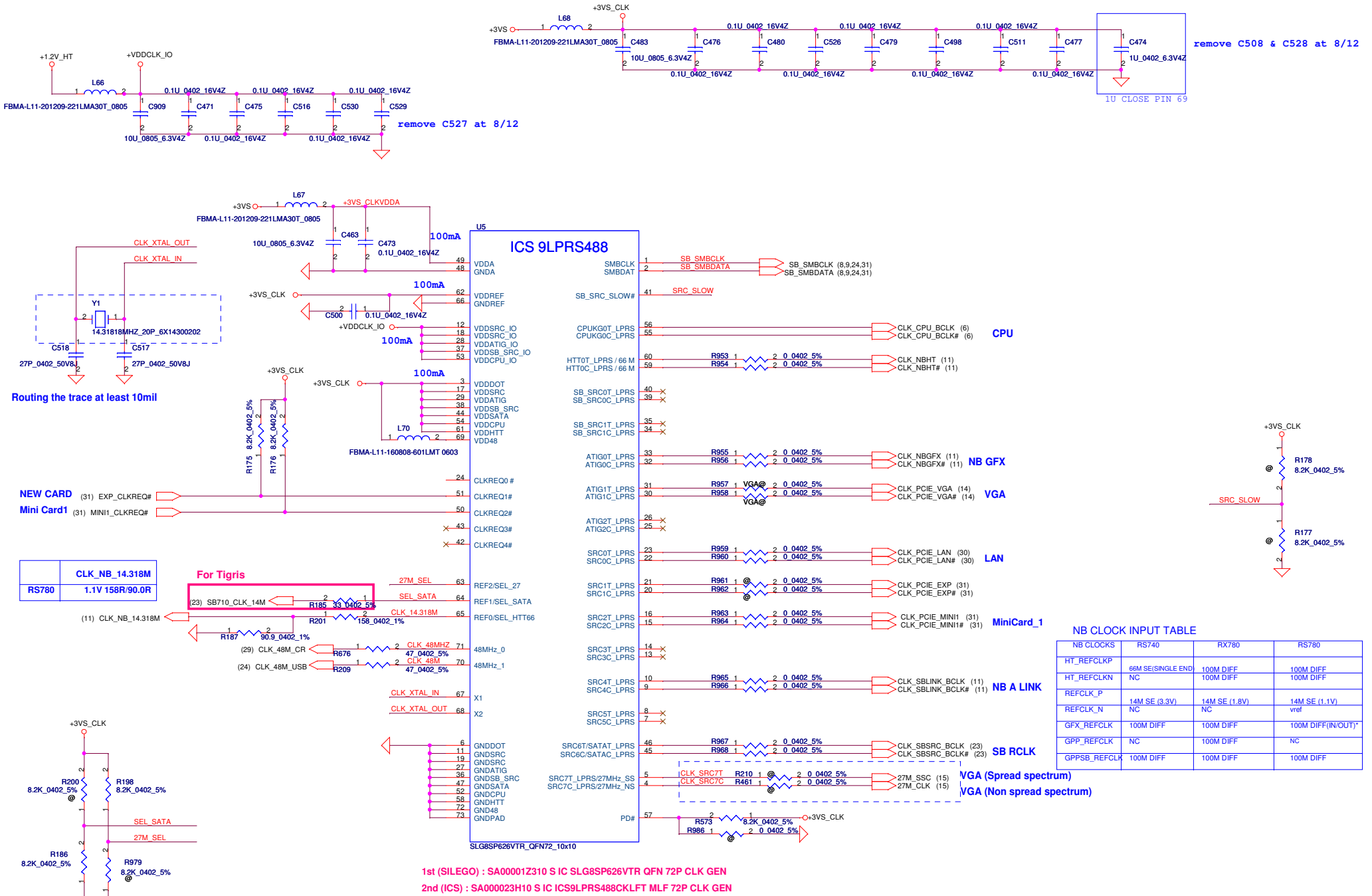
Compal Electronics, Inc.

Title: PARK-S3 DDR3 VRAM

Size: C | Document Number: LA-5972P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 19 of 49


+1.2V_HT
+VDDCLK_IO
L66
FBMA-L11-201209-221LMA30T_0805
C909
C471
C475
C516
C530
C529
10U_0805_6.3V4Z
0.1U_0402_16V4Z
remove C527 at 8/12
+3VS_CLK
L68
+3VS
FBMA-L11-201209-221LMA30T_0805
C483
C476
C480
C526
C479
C498
C511
C477
C474
1U_0402_6.3V4Z
remove C508 & C528 at 8/12
1U CLOSE PIN 69
L67
+3VS
+3VS_CLKVDDA
FBMA-L11-201209-221LMA30T_0805
C463
C473
100mA
U5
ICS 9LPRS488
VDDA
GNDA
VDDREF
GNDREF
VDDSRC_IO
VDDSRC_IO
VDDATIG_IO
VDDSB_SRC_IO
VDDCPU_IO
VDDDOT
VDDSRC
VDDATIG
VDDSB_SRC
VDDSATA
VDDCPU
VDDHTT
VDD48
SMBCLK
SMBDAT
SB_SMBCLK
SB_SMBDATA
SB_SMBCLK (8,9,24,31)
SB_SMBDATA (8,9,24,31)
SB_SRC_SLOW#
SRC_SLOW
CPUKG0T_LPRS
CPUKG0C_LPRS
CLK_CPU_BCLK (6)
CLK_CPU_BCLK# (6)
CPU
HTT0T_LPRS / 66 M
HTT0C_LPRS / 66 M
R953
R954
0_0402_5%
CLK_NBHT (11)
CLK_NBHT# (11)
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
ATIG0T_LPRS
ATIG0C_LPRS
R955
R956
CLK_NBGFX (11)
CLK_NBGFX# (11)
NB GFX
ATIG1T_LPRS
ATIG1C_LPRS
R957
R958
VGA@
CLK_PCIE_VGA (14)
CLK_PCIE_VGA# (14)
VGA
ATIG2T_LPRS
ATIG2C_LPRS
SRC0T_LPRS
SRC0C_LPRS
R959
R960
CLK_PCIE_LAN (30)
CLK_PCIE_LAN# (30)
LAN
SRC1T_LPRS
SRC1C_LPRS
R961
R962
CLK_PCIE_EXP (31)
CLK_PCIE_EXP# (31)
SRC2T_LPRS
SRC2C_LPRS
R963
R964
CLK_PCIE_MINI1 (31)
CLK_PCIE_MINI1# (31)
MiniCard_1
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
R965
R966
CLK_SBLINK_BCLK (11)
CLK_SBLINK_BCLK# (11)
NB A LINK
SRC5T_LPRS
SRC5C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
R967
R968
CLK_SBSRC_BCLK (23)
CLK_SBSRC_BCLK# (23)
SB RCLK
SRC7T_LPRS/27MHz_SS
SRC7C_LPRS/27MHz_NS
CLK_SRC7T
CLK_SRC7C
R210
R461
27M_SSC (15)
27M_CLK (15)
VGA (Spread spectrum)
VGA (Non spread spectrum)
PD#
R573
R986
8.2K_0402_5%
+3VS_CLK
CLKREQ0 #
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
REF2/SEL_27
REF1/SEL_SATA
REF0/SEL_HTT66
48MHz_0
48MHz_1
X1
X2
GNDDOT
GNDSRC
GNDSRC
GNDATIG
GNDSB_SRC
GNDSATA
GNDCPU
GNDHTT
GND48
GNDPAD
SLG8SP626VTR_QFN72_10x10
CLK_XTAL_OUT
CLK_XTAL_IN
Y1
14.31818MHZ_20P_6X14300202
C518
C517
27P_0402_50V8J
Routing the trace at least 10mil
+3VS_CLK
+3VS_CLK
L70
FBMA-L11-160808-601LMT 0603
100mA
R175
R176
8.2K_0402_5%
NEW CARD
(31) EXP_CLKREQ#
Mini Card1
(31) MINI1_CLKREQ#
CLK_NB_14.318M
RS780
1.1V 158R/90.0R
For Tigris
27M_SEL
SEL_SATA
CLK_14.318M
(23) SB710_CLK_14M
R185
33_0402_5%
(11) CLK_NB_14.318M
R201
158_0402_1%
R187
90.9_0402_1%
(29) CLK_48M_CR
R676
CLK_48MHZ
47_0402_5%
(24) CLK_48M_USB
R209
CLK_48M
47_0402_5%
+3VS_CLK
R200
R198
8.2K_0402_5%
SEL_SATA
27M_SEL
R186
R979
+3VS_CLK
R178
R177
SRC_SLOW
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN
SEL_HTT66
1 single-ended 66MHz HTT output
0* differential 100MHz HTT output
SEL_SATA
1 NON SPREAD 100M_SATA SRC6 output
0* SPREAD 100M_SATA SRC6 output
* default
27M_SEL
1 * NON SPREAD 27M and SPREAD 27M output
0 differential spread SRC_7 output
Security Classification
Compal Secret Data
Issued Date
2008/10/06
Deciphered Date
2009/10/06
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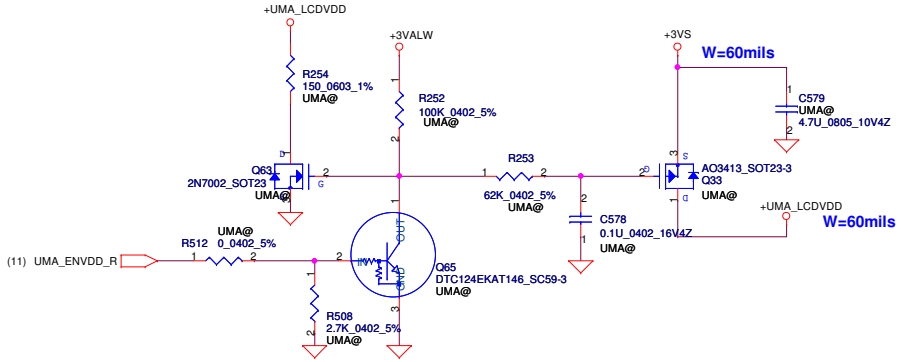
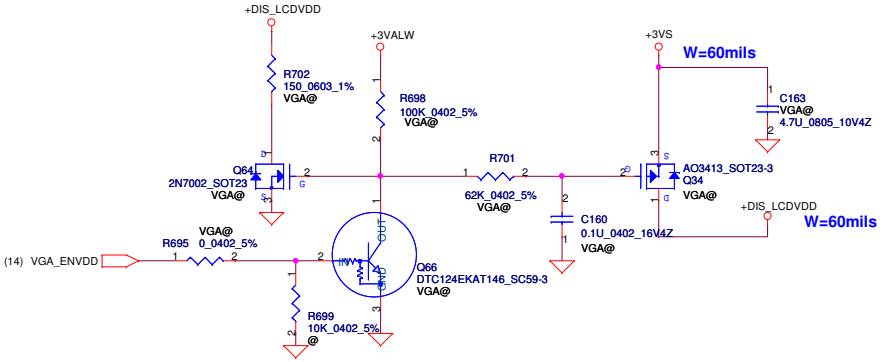
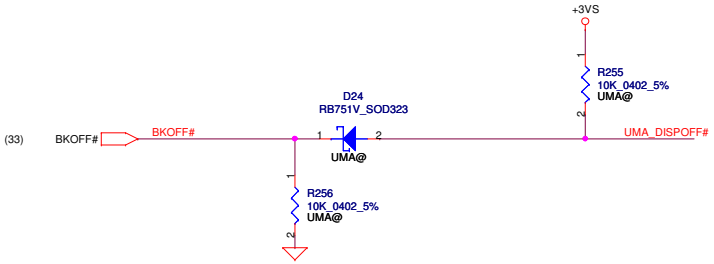
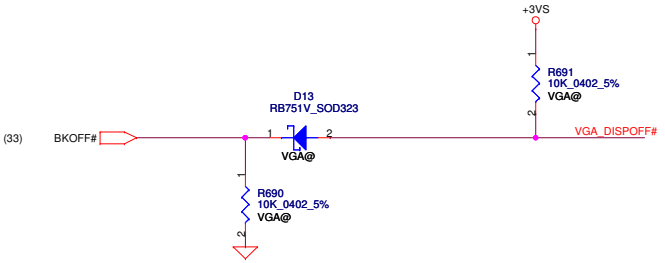
Compal Electronics, Inc.
Title
Clock generator
Size
Custom
Document Number
LA-5972P
Rev
1.0
Date: Thursday, December 10, 2009
Sheet 20 of 49

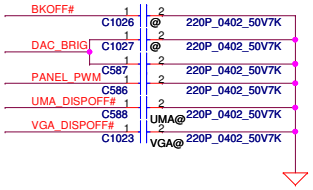
LCD POWER CIRCUIT

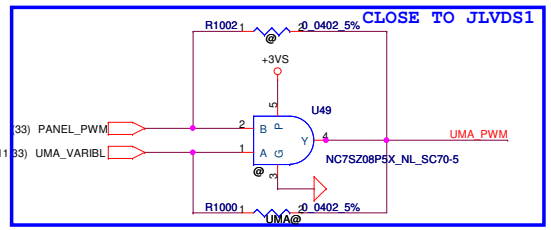


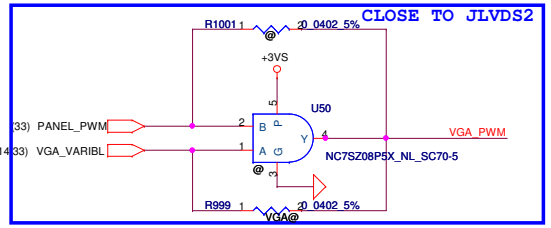




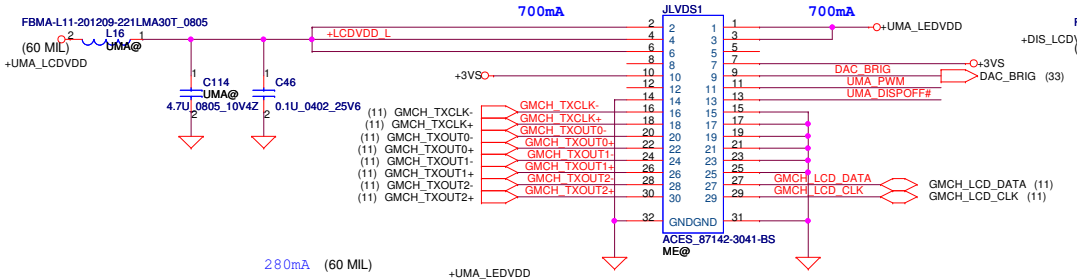


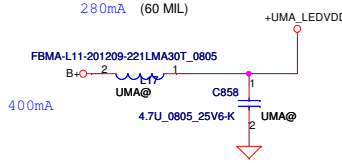


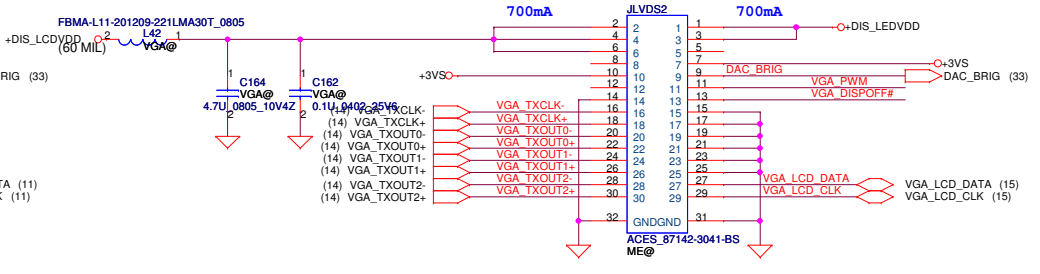


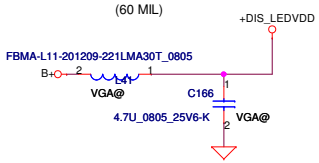


LCD/PANEL BD. Conn.









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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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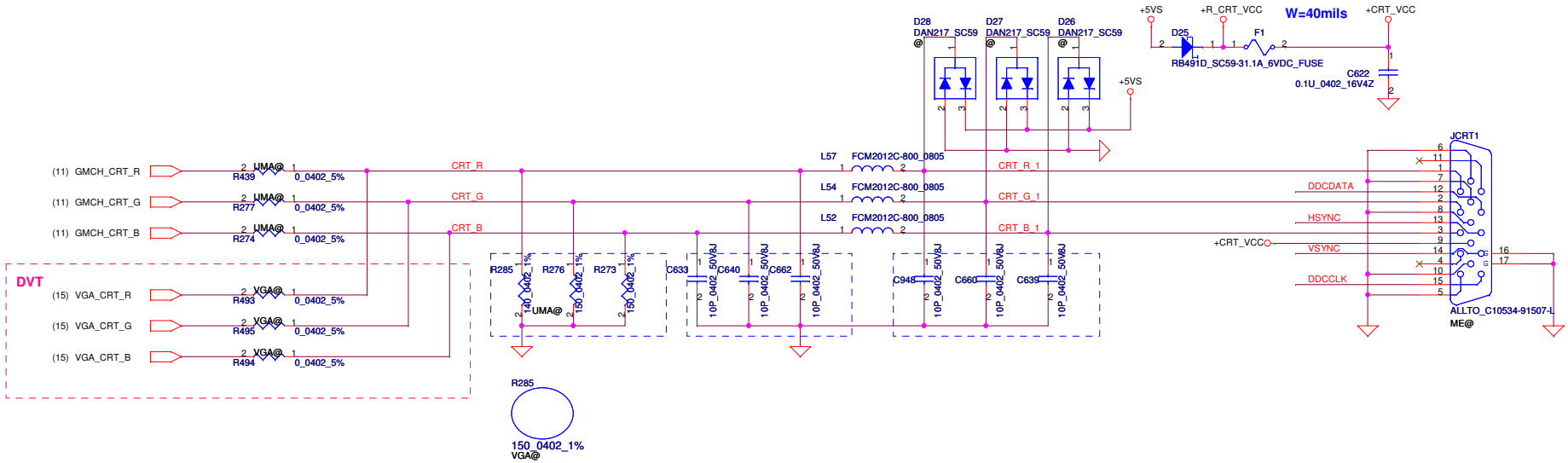
Compal Electronics, Inc.

Title: LVDS Connector

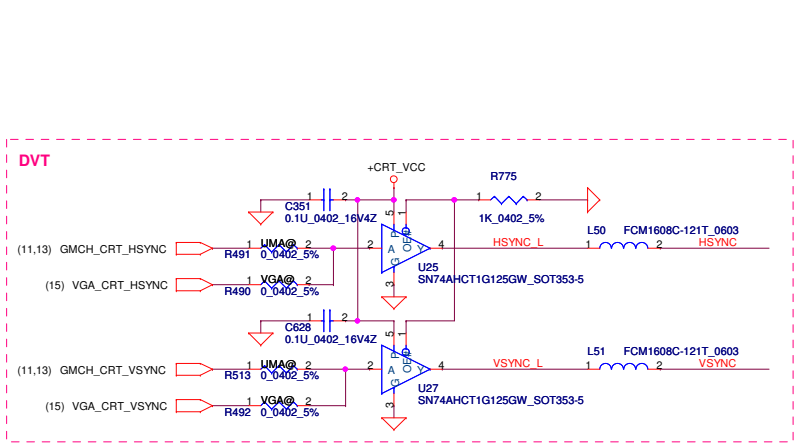
Size	Document Number	Rev
B	LA-5972P	1.0

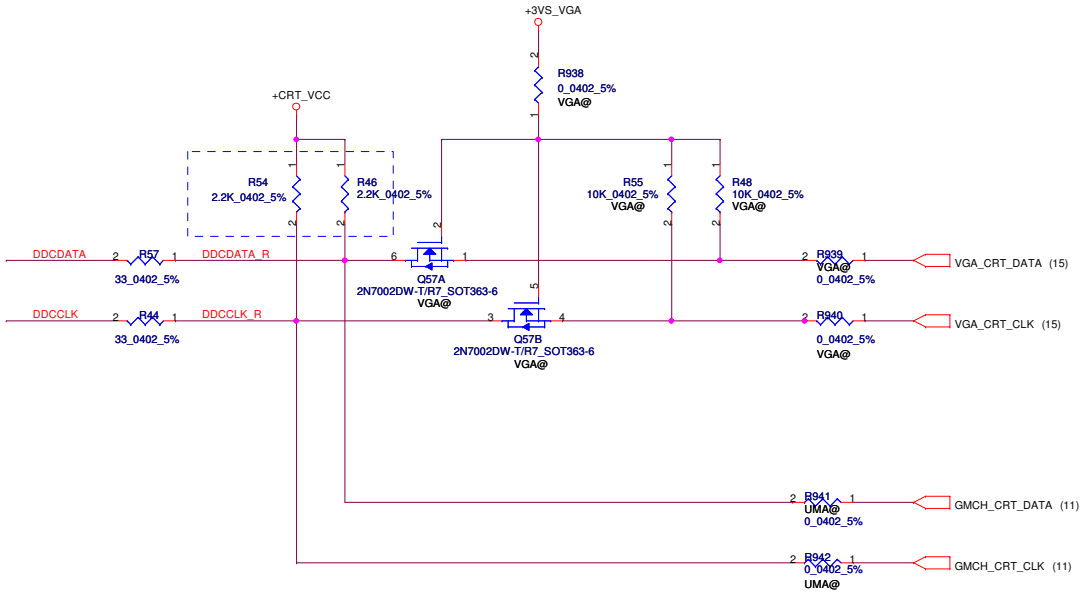
Date: Thursday, December 10, 2009 | Sheet 21 of 49

CRT CONNECTOR



Place closed to chipset





Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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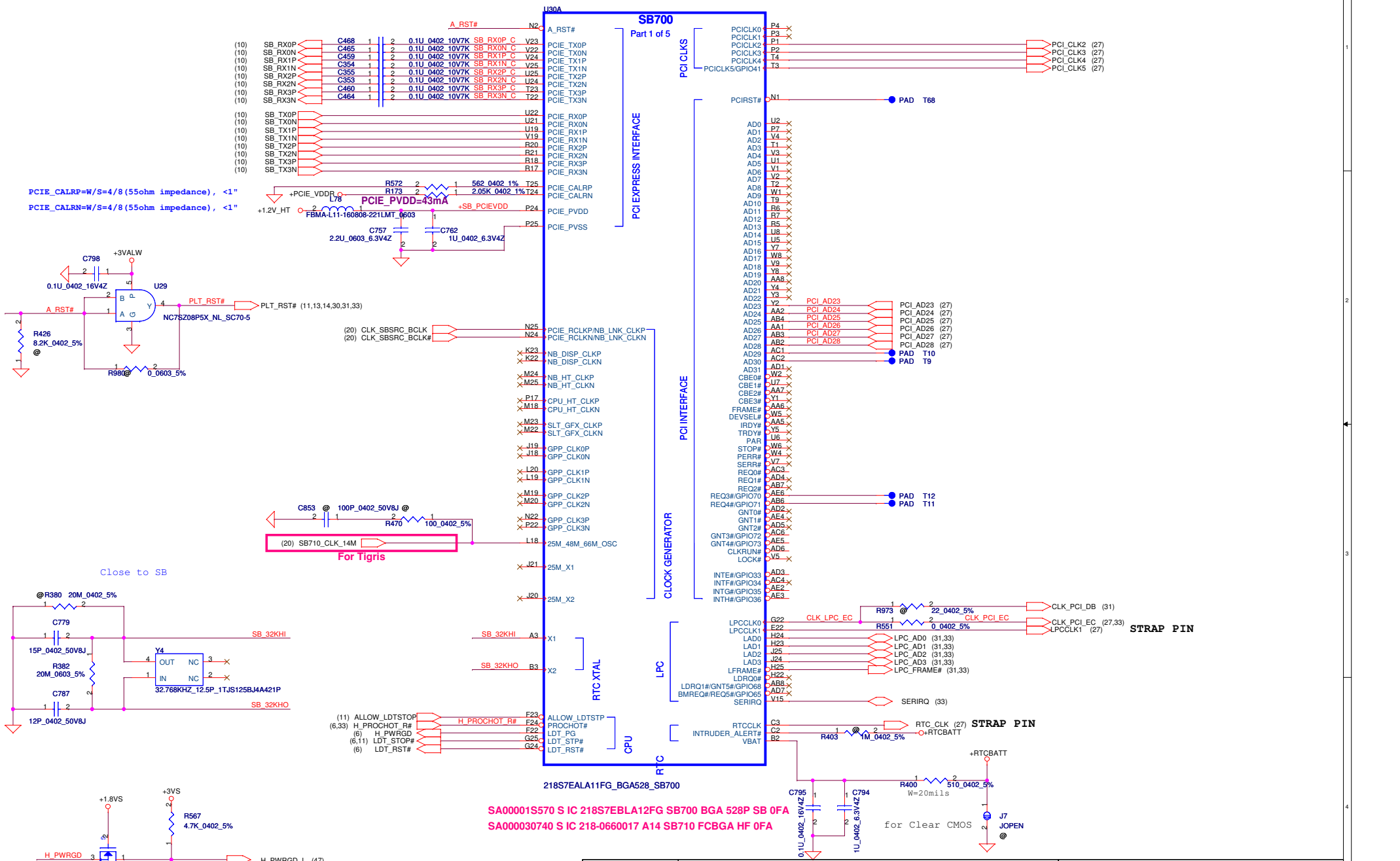
Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
B	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 22 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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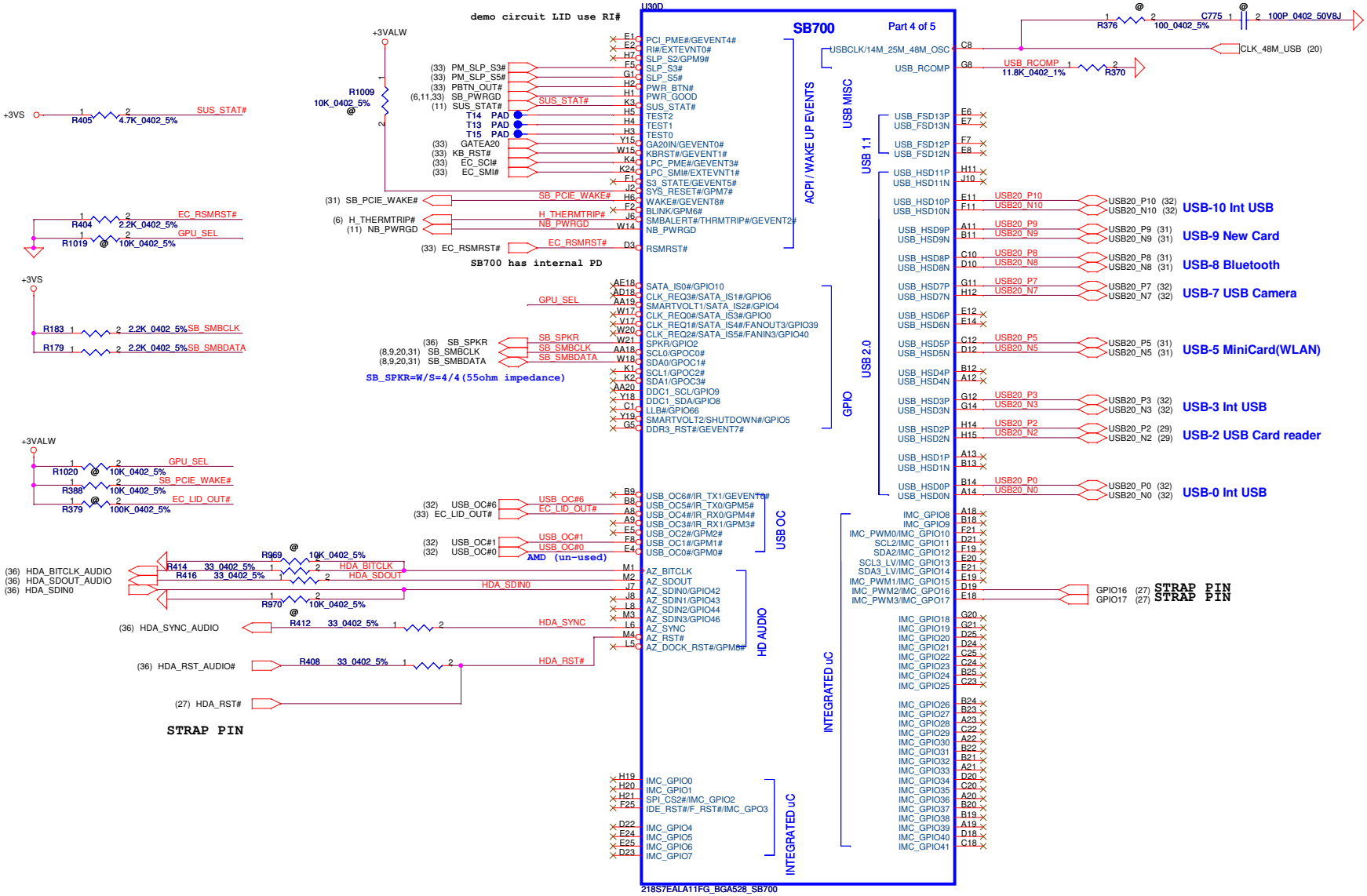
Compal Electronics, Inc.

Title: SB710-PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 23 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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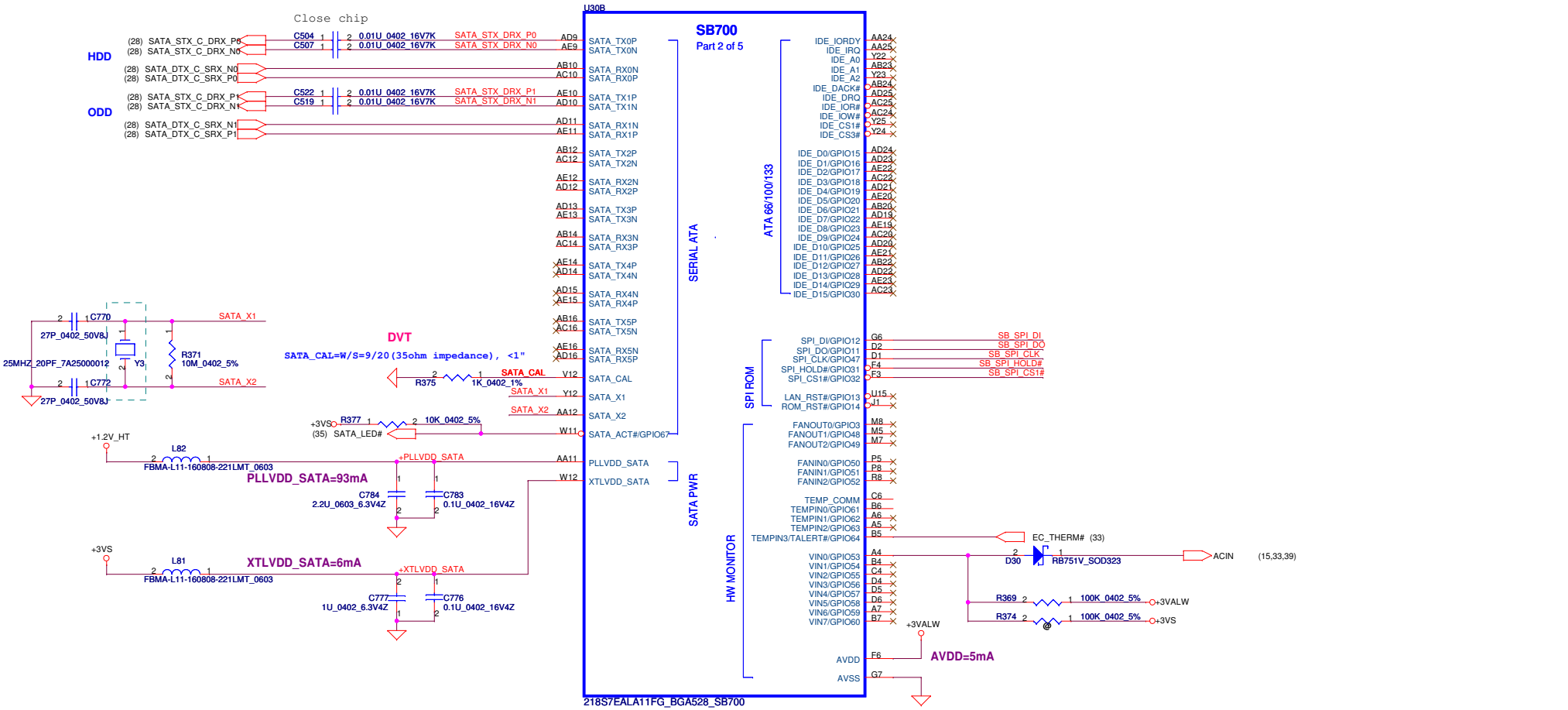
Compal Electronics, Inc.

Title: SB710 USB/HD audio

Size	Document Number	Rev
Custom	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 24 of 49



Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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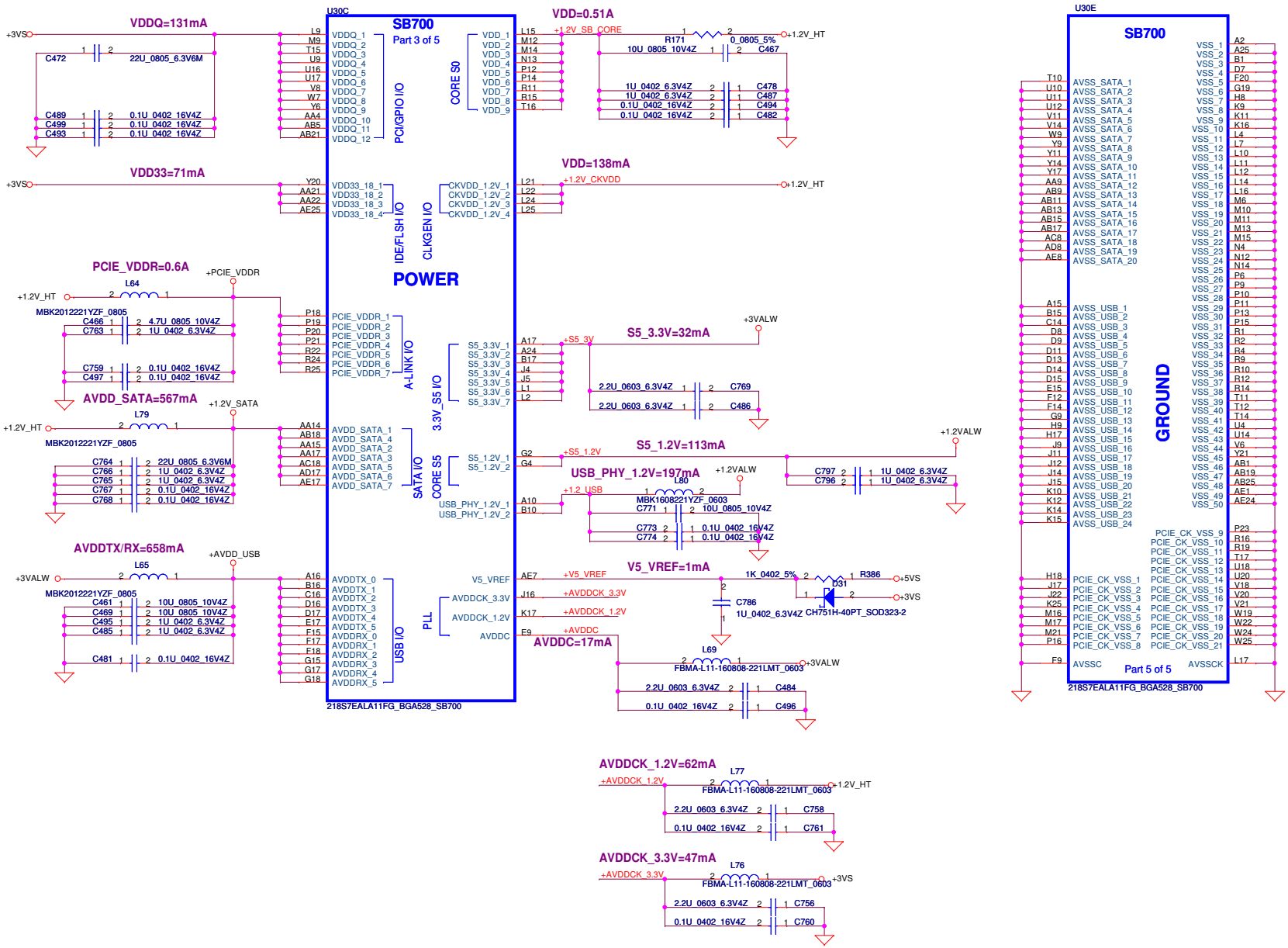
Compal Electronics, Inc.

Title: SB710 SATA/IDE/SPI

Size	Document Number	Rev
Custom	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 25 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: SB710 power/GND

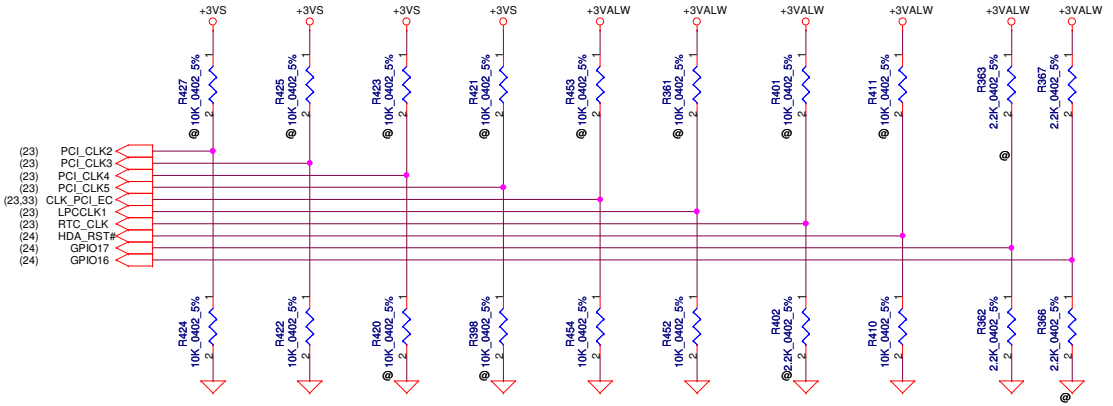
Size: Custom | Document Number: LA-5972P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 26 of 49

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

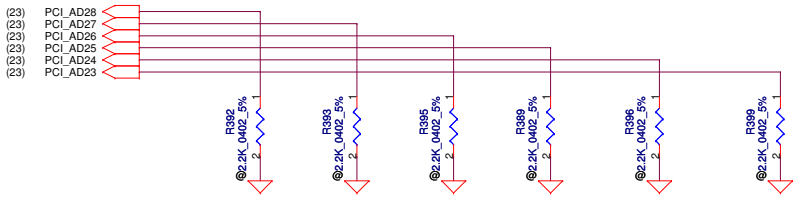
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	**INTERNAL RTC** **DEFAULT**	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	**BOOTFAIL TIMER DISABLED** **DEFAULT**	**IGNORE DEBUG STRAPS** **DEFAULT**			**DISABLE PCI MEM BOOT** **DEFAULT**	**CLKGEN DISABLED** **DEFAULT**	**EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK)	**EC DISABLED** **DEFAULT**	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	**USE LONG RESET** **DEFAULT**	**USE PCI PLL** **DEFAULT**	**USE ACPI BCLK** **DEFAULT**	**USE IDE PLL** **DEFAULT**	**USE DEFAULT PCIE STRAPS** **DEFAULT**	**RESERVED**
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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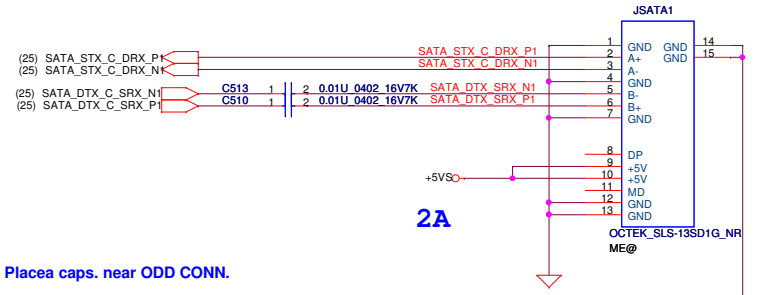
Compal Electronics, Inc.

Title: SB710 STRAPS

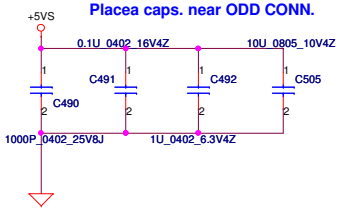
Size: Custom | Document Number: LA-5972P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 27 of 49

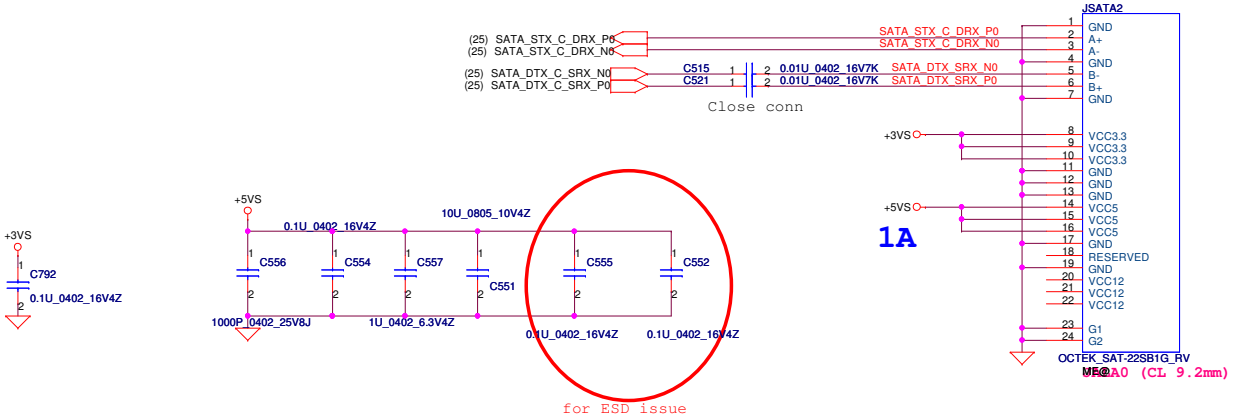
SATA ODD Conn.



Placea caps. near ODD CONN.



SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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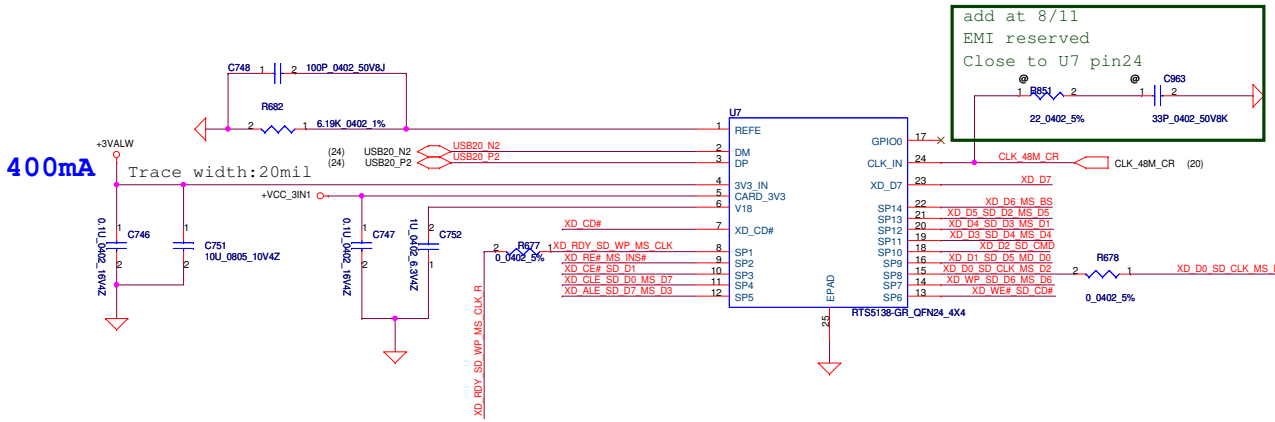
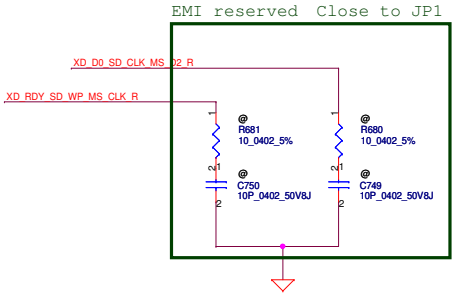
Compal Electronics, Inc.

Title: HDD & ODD Connector

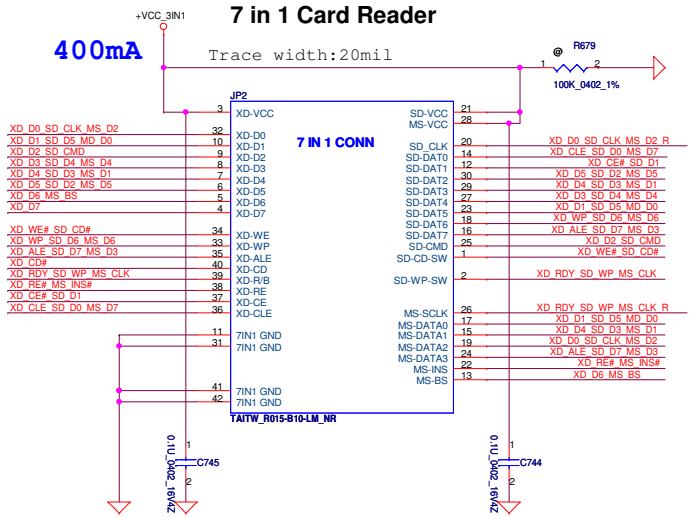
Size	Document Number	Rev
B	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 28 of 49





Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: RTS5138 Card Reader

Size	Document Number	Rev
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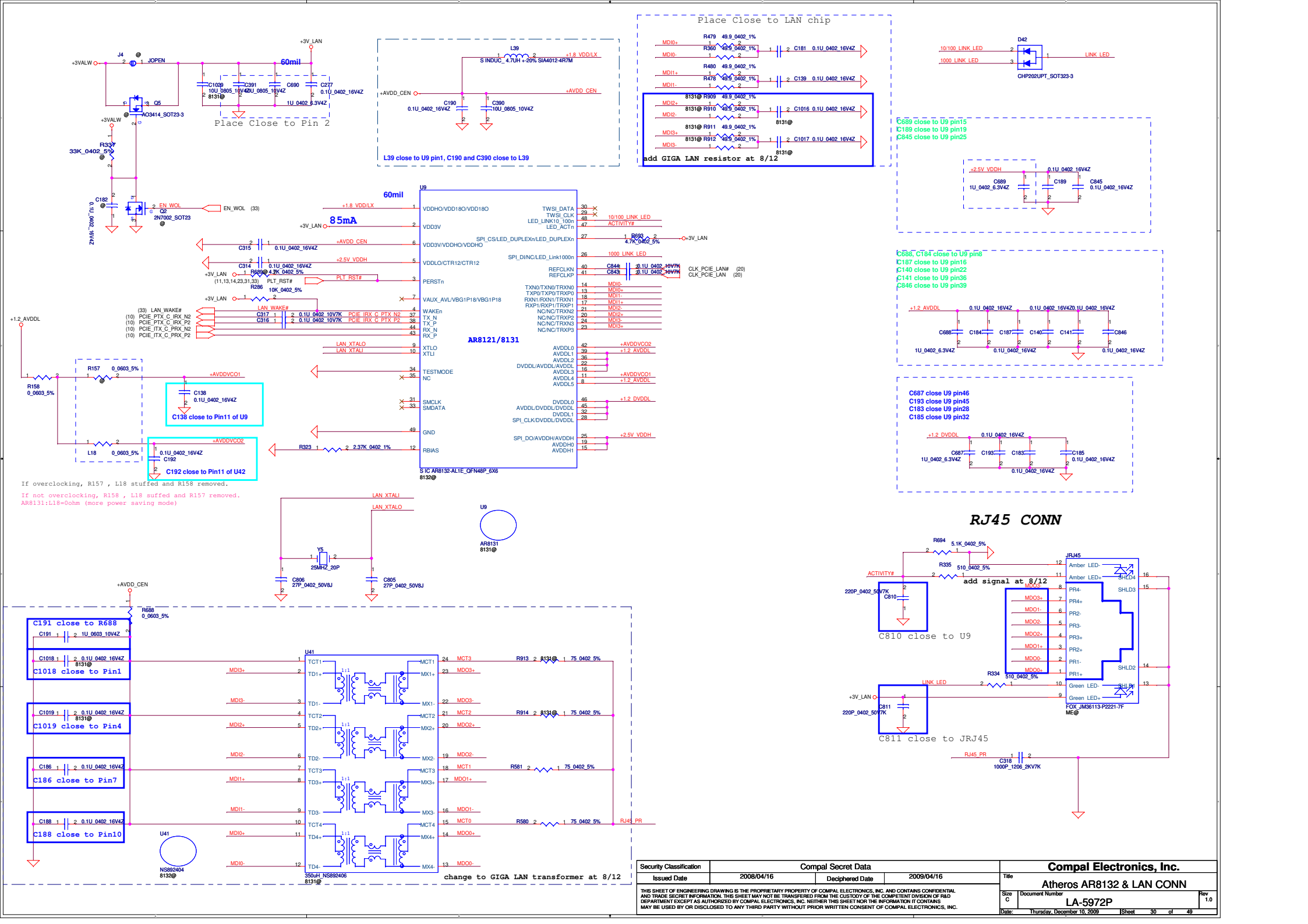
Date: Thursday, December 10, 2009 Sheet 29 of 49



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

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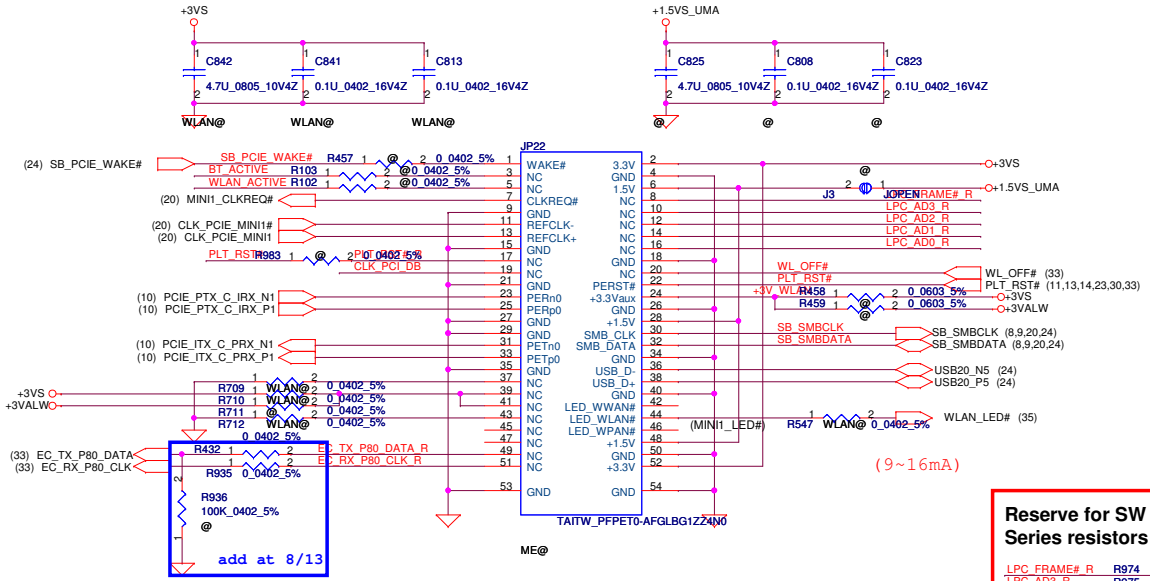
Compal Electronics, Inc.

Title: Atheros AR8132 & LAN CONN

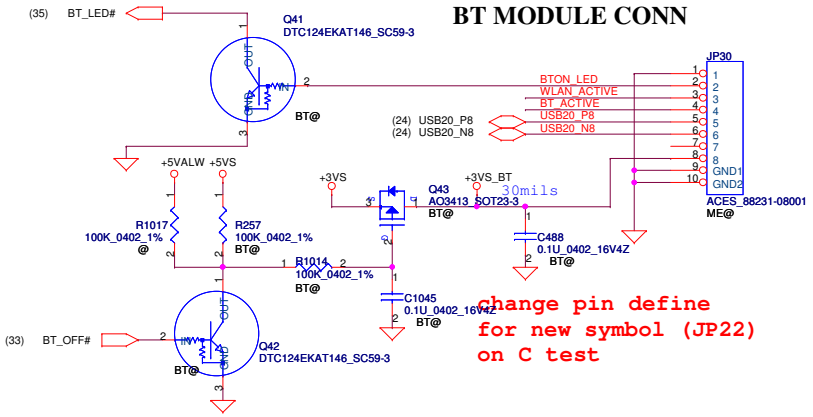
Size	Document Number	Rev
C	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 30 of 49

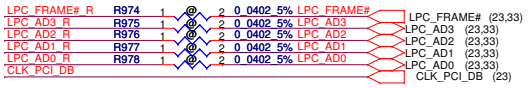
For Wireless LAN



BT MODULE CONN



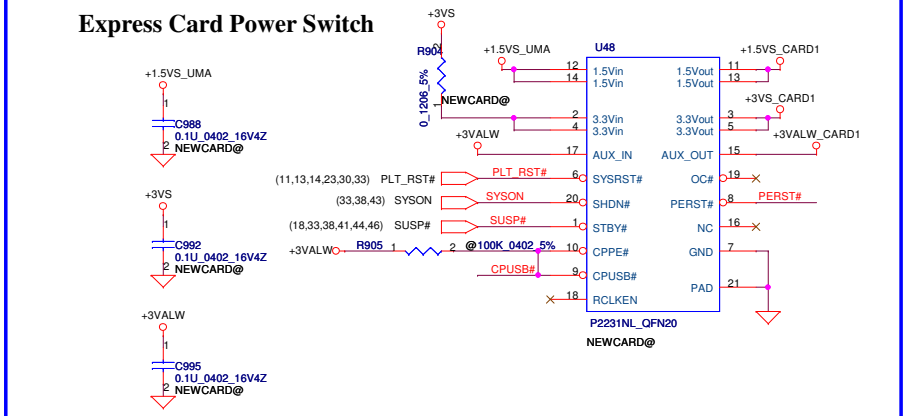
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



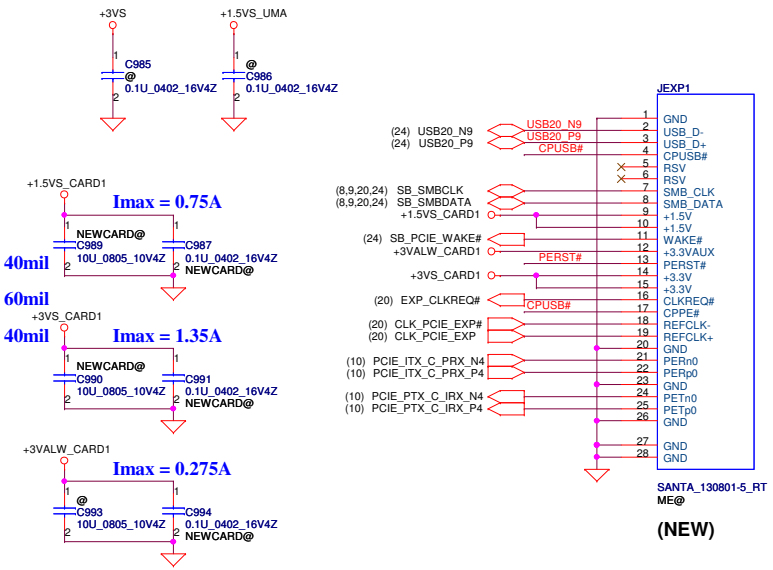
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

add at 8/11

Express Card Power Switch



add at 8/11



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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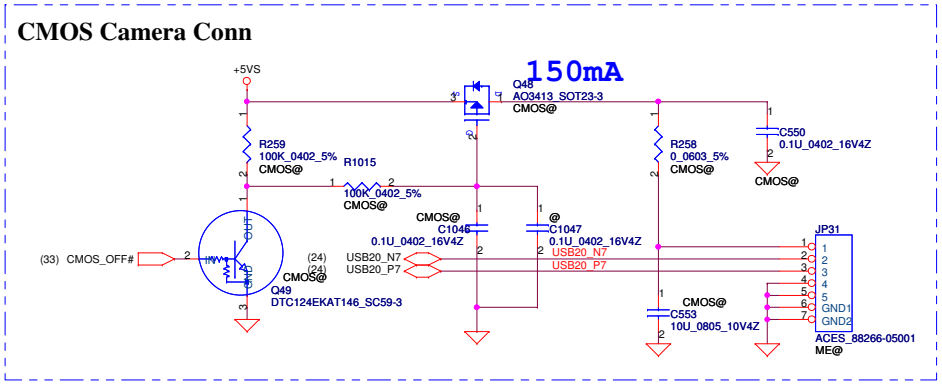
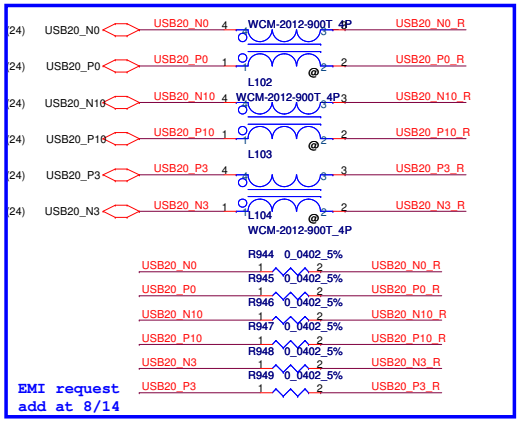
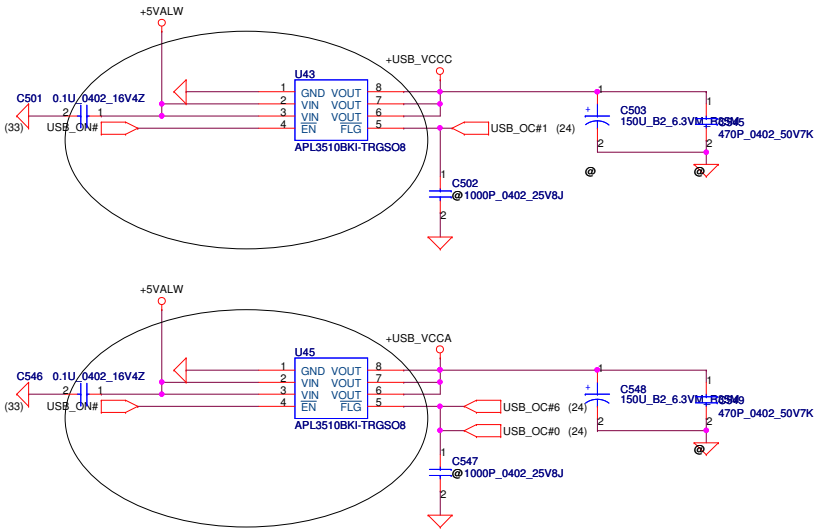
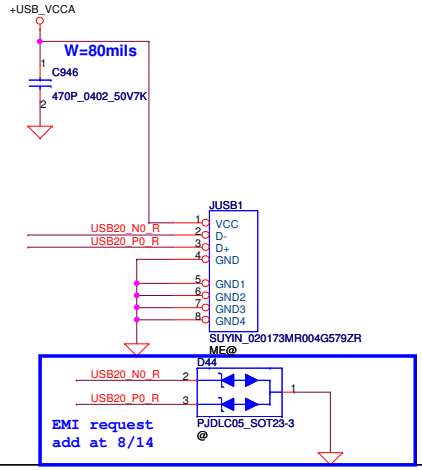
Compal Electronics, Inc.			
Title	MINI CARD/BT/ NEW CARD		
Size B	Document Number LA-5972P		Rev 1.0
Date: Thursday, December 10, 2009	Sheet 31 of 49		

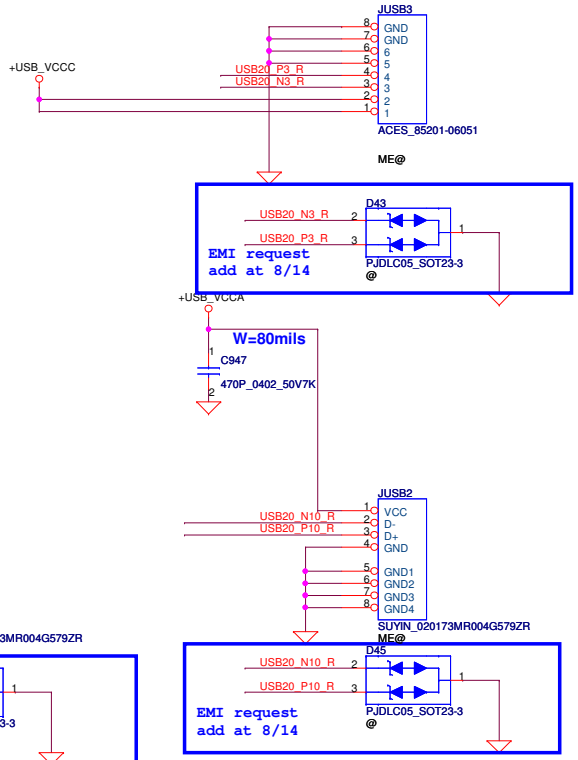
CMOS Camera Conn











Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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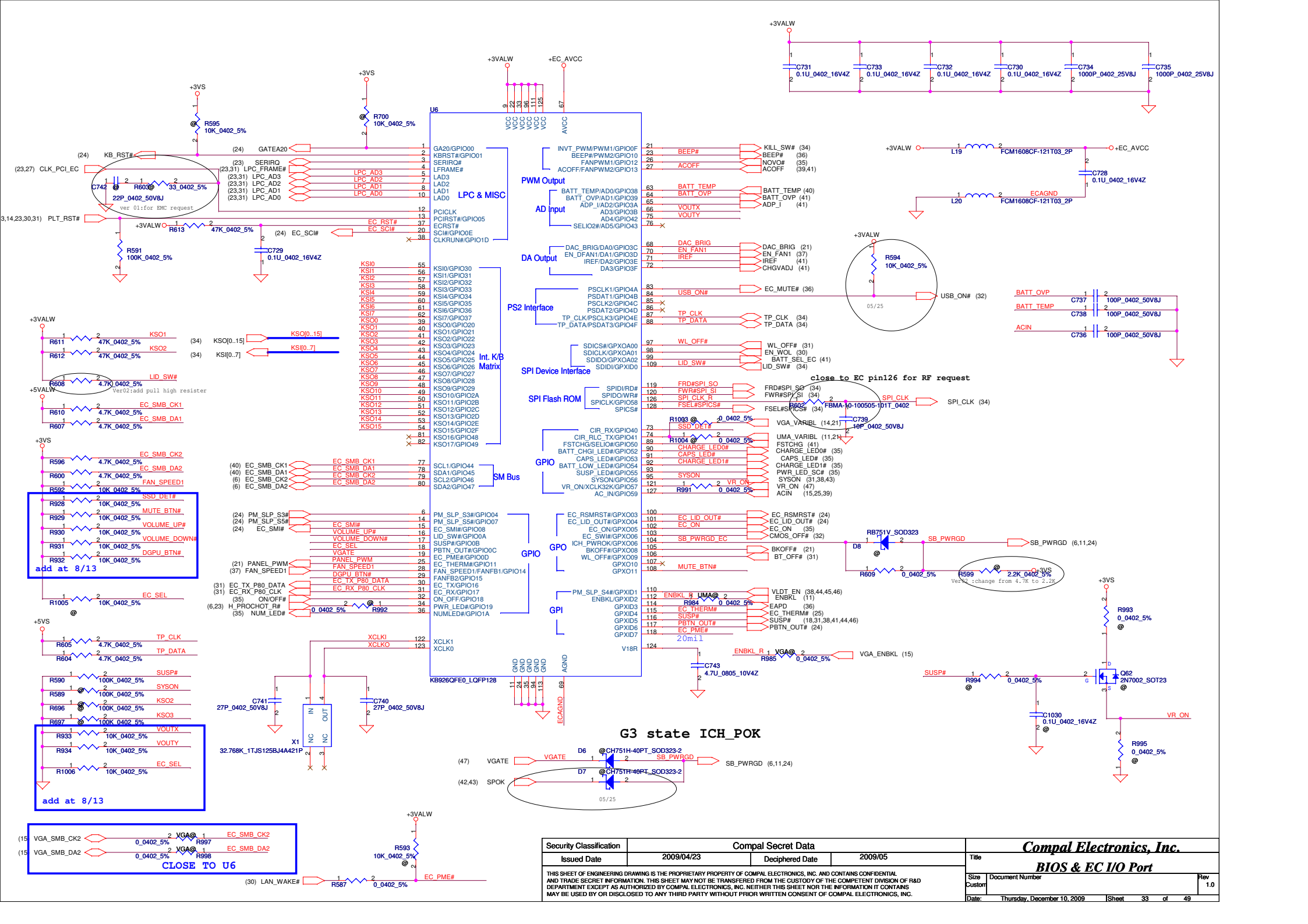
Compal Electronics, Inc.

Title: BlueTooth / Int USB x2 /eSATA

Size	Document Number	Rev
B	LA-5972P	1.0

Date: Thursday, December 10, 2009 | Sheet 32 of 49



Security Classification	Compal Secret Data		
Issued Date	2009/04/23	Deciphered Date	2009/05

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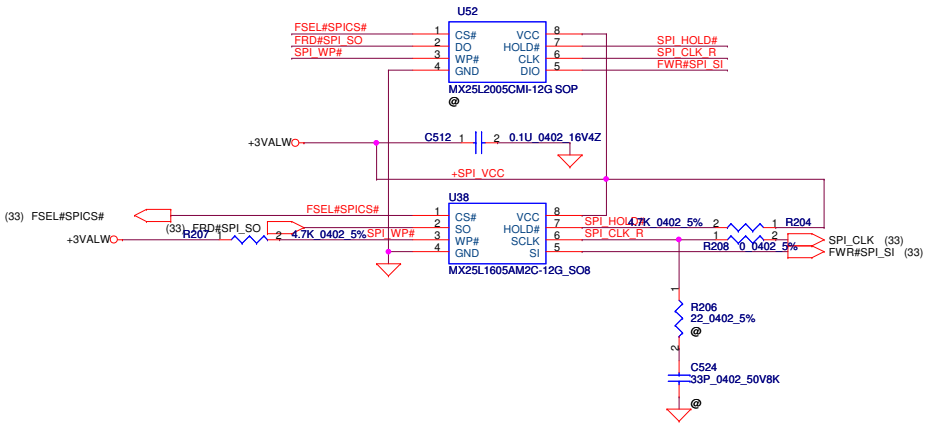
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

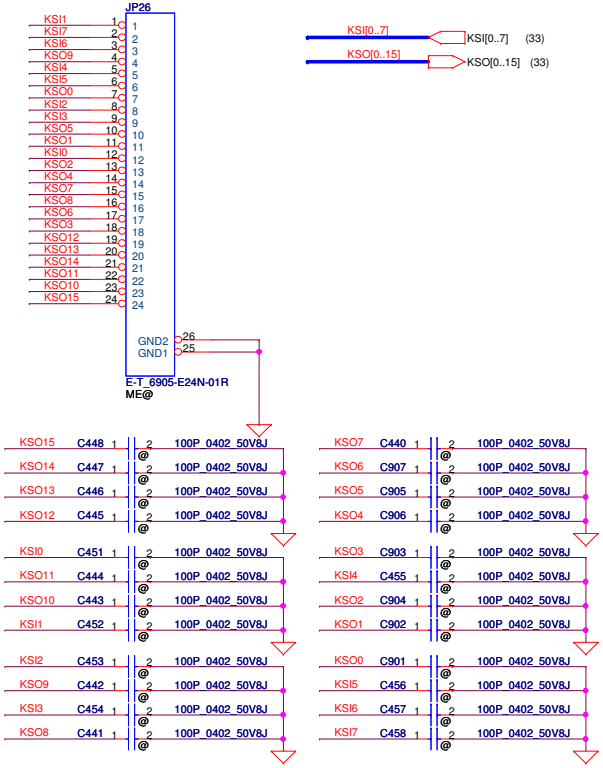
Size	Document Number	Rev
Custom		1.0

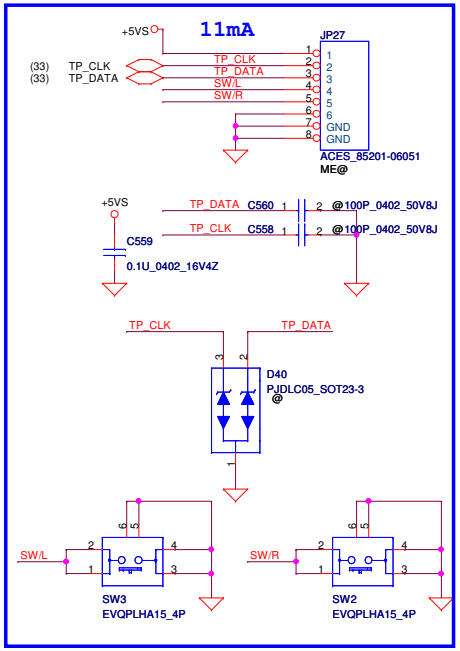
Date: Thursday, December 10, 2009 | Sheet 33 of 49

BIOS(SYS / EC / VGA)

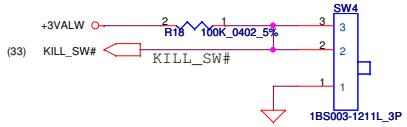


INT_KBD Conn.

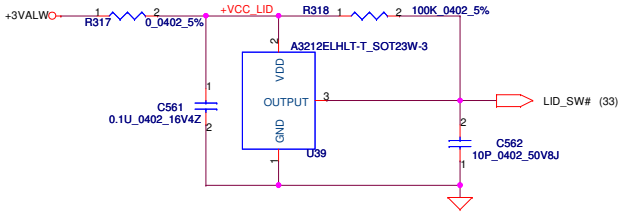




Kill Switch



Lid Switch



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

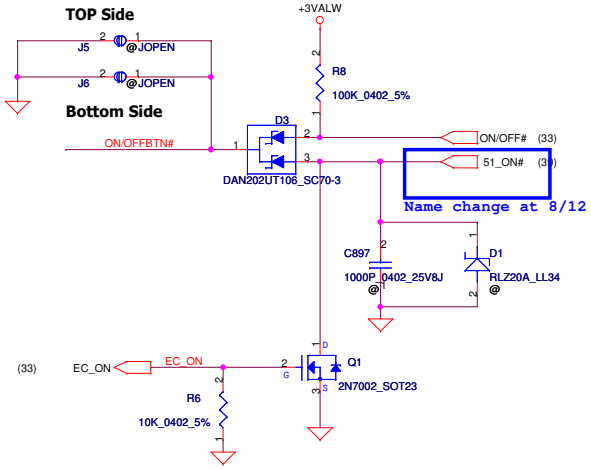
Title: BIOS, I/O Port & K/B Connector

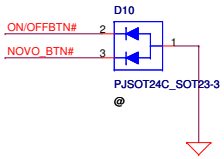
Size	Document Number	Rev
B	LA-5972P	1.0

Date: Thursday, December 10, 2009 Sheet 34 of 49

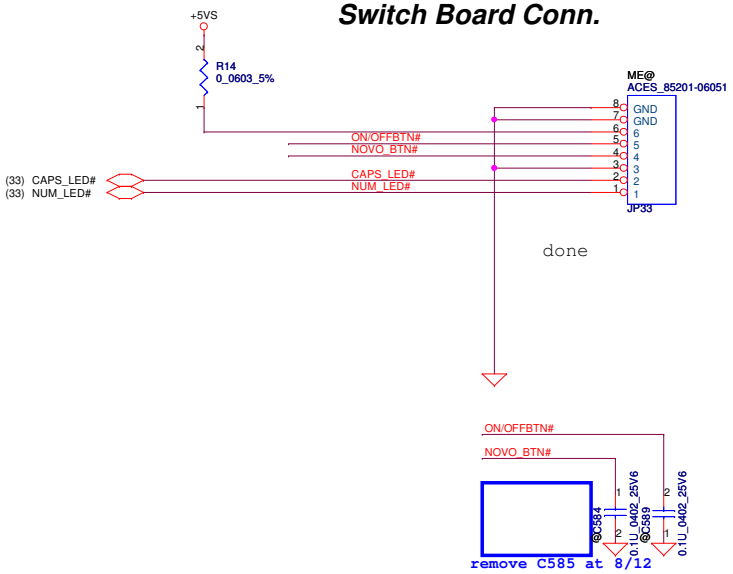
Power Button

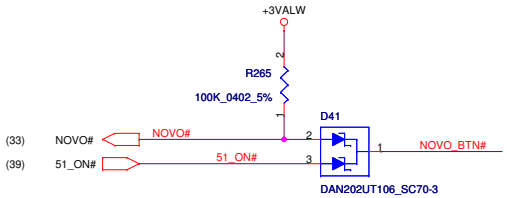
ON/OFF switch



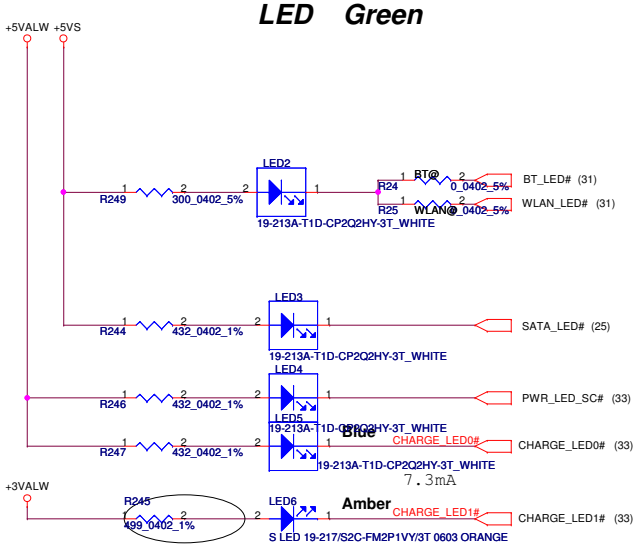


Switch Board Conn.





LED Green



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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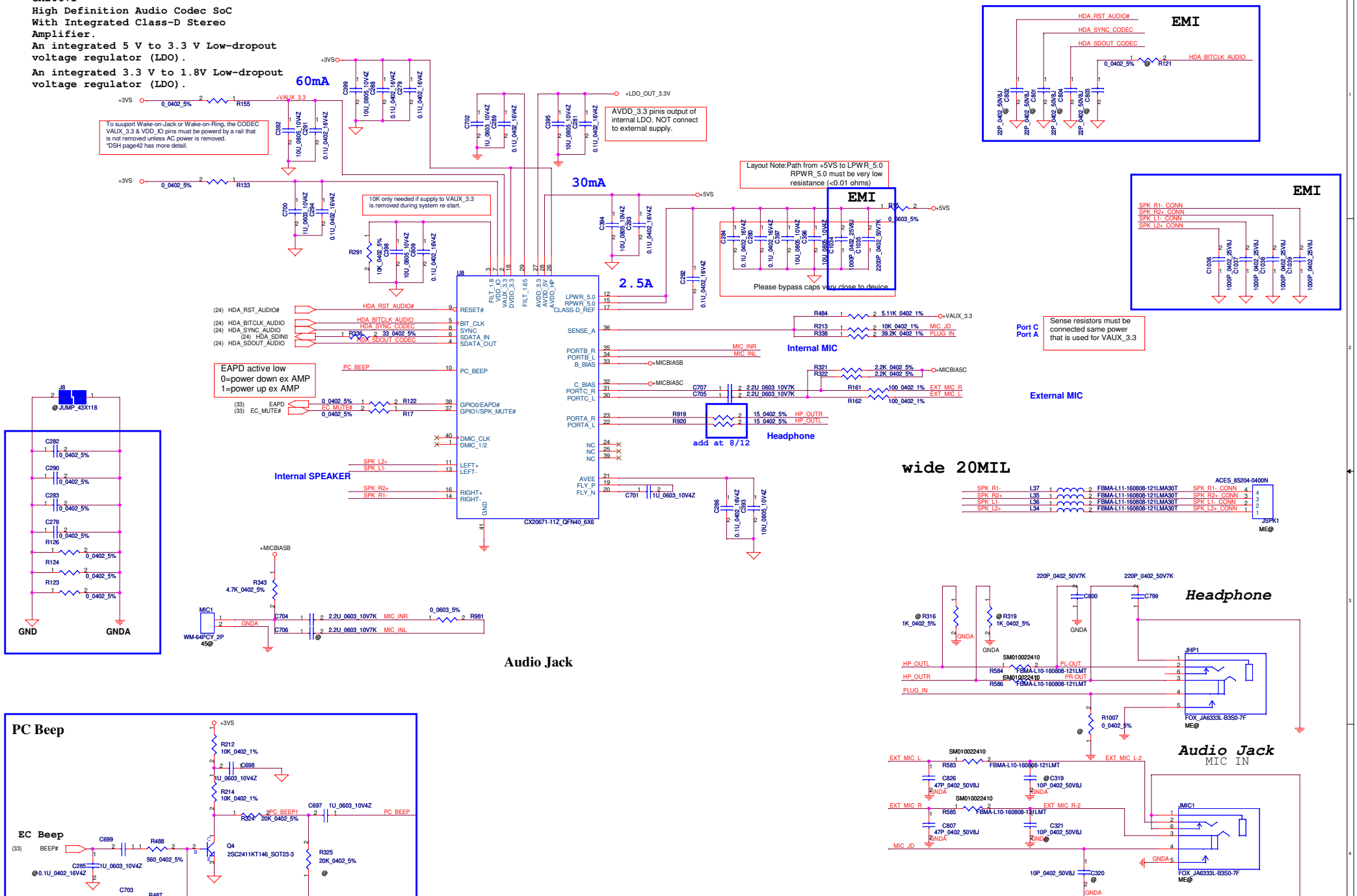
Compal Electronics, Inc.			
Title: Power BTN/LED			
Size: B	Document Number: LA-5972P		Rev: 1.0
Date: Thursday, December 10, 2009	Sheet 35 of 49		

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2009/10/06
Title	HD Audio Codec ALC888S-VC		
Size C	Document Number LA-5972P		Rev 1.0
Date: Thursday, December 10, 2009	Sheet 36 of 49		

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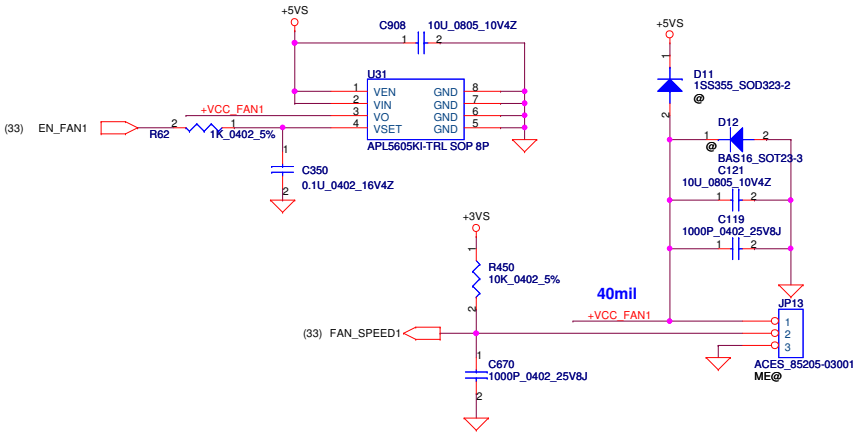
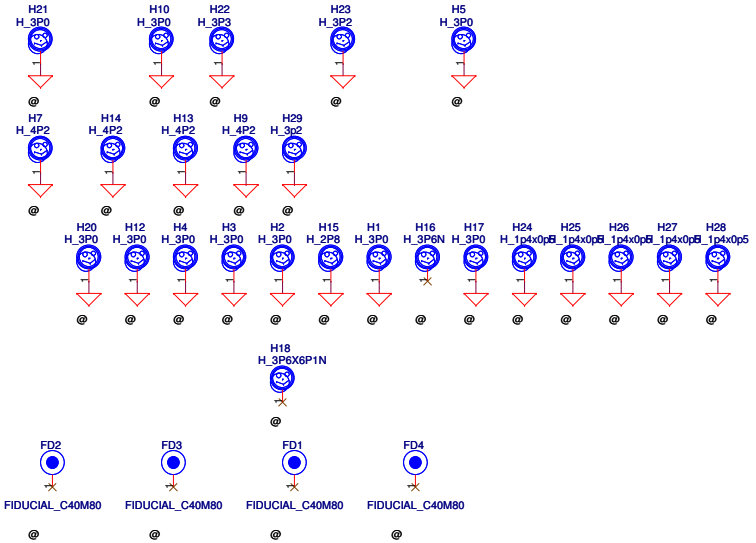
FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
B	LA-5972P	1.0

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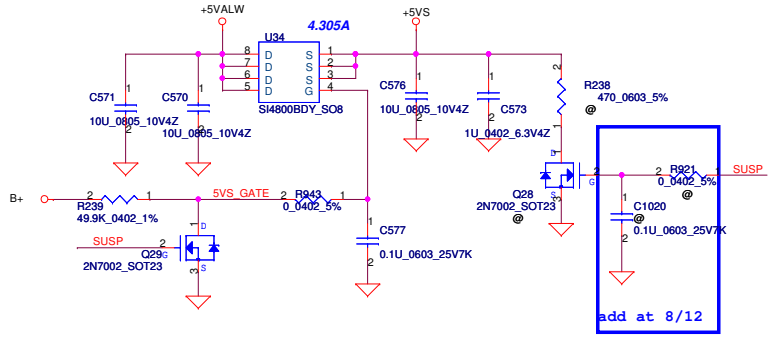
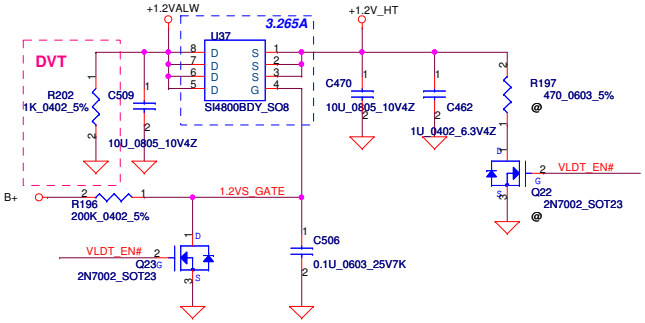
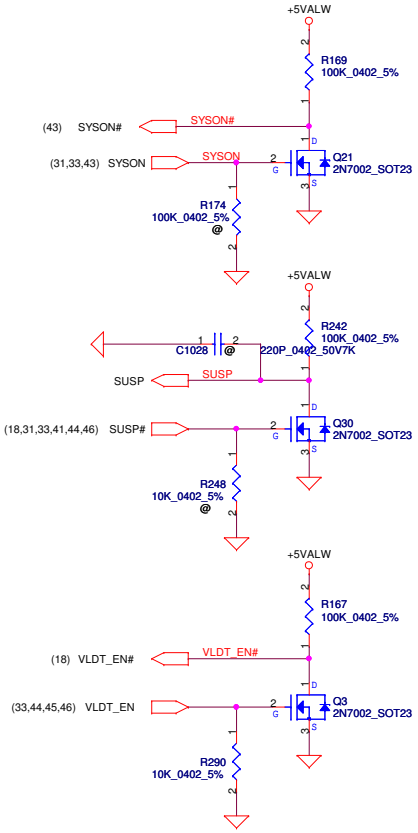
+5VALW TO +5VS

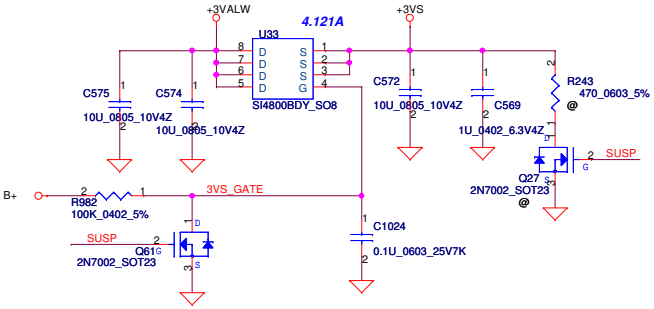


+1.2VALW TO +1.2V_HT

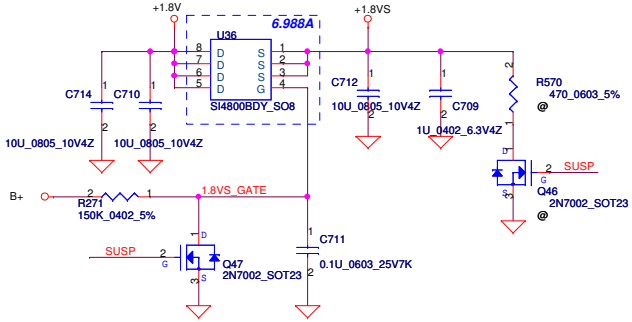


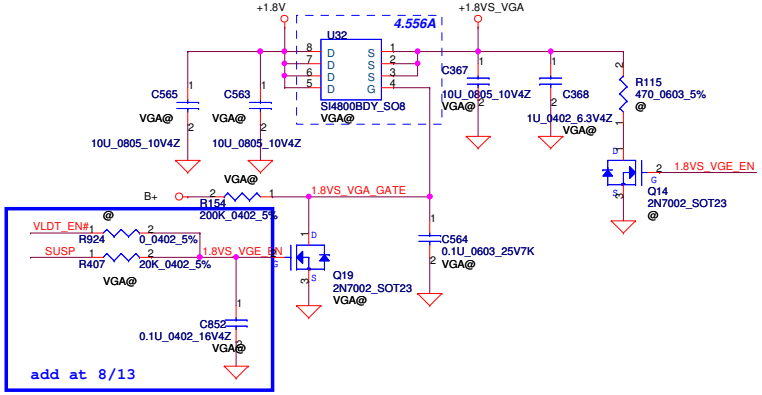


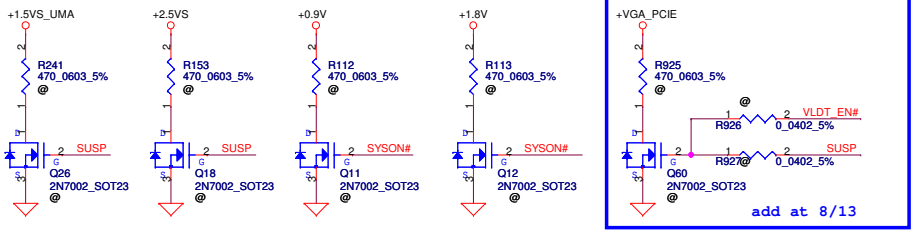
+3VALW TO +3VS



+1.8V to +1.8VS







Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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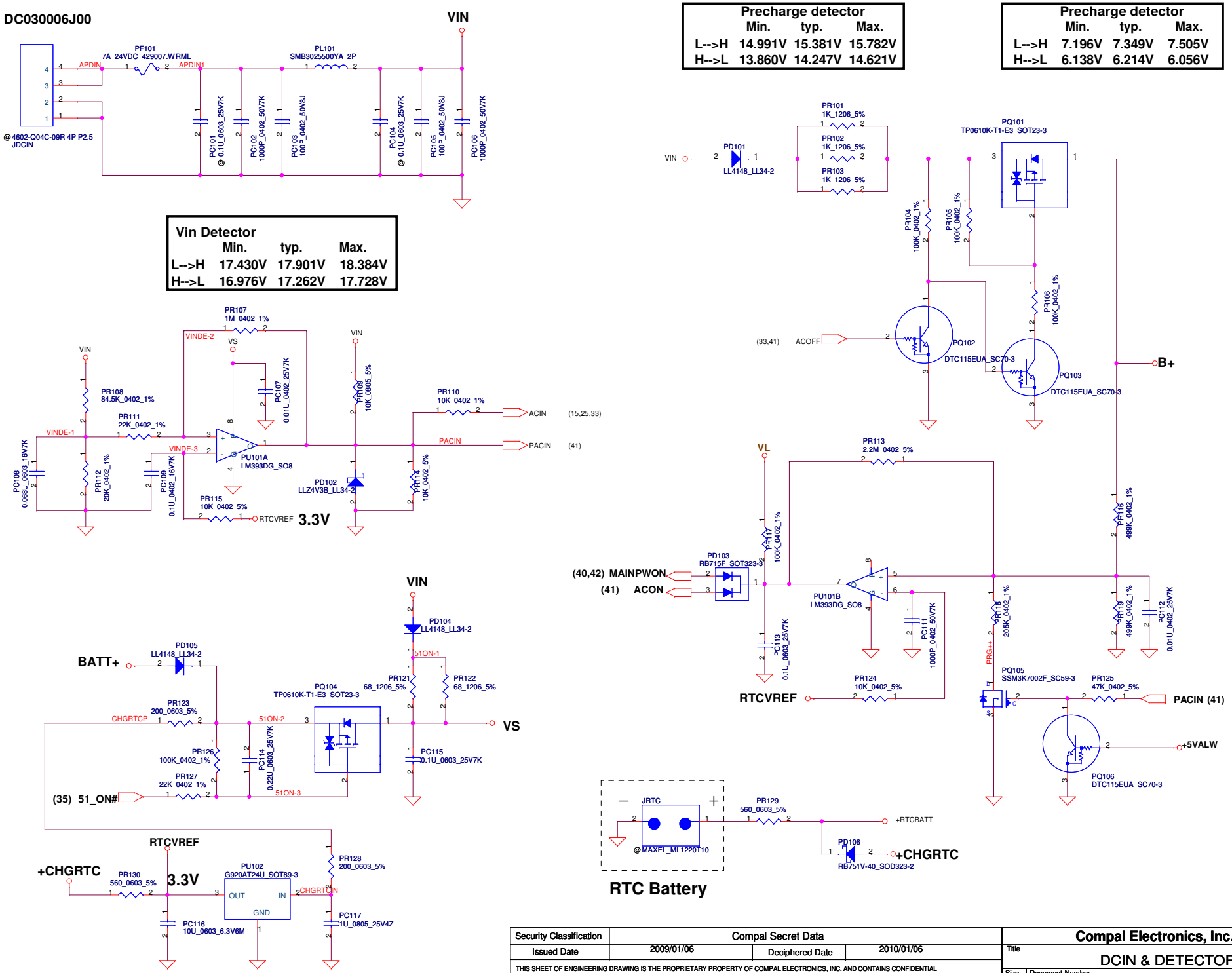
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: LA-5972P | Rev: 1.0

Date: Thursday, December 10, 2009 | Sheet 38 of 49



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: Custom | Document Number: | Rev: 1.0

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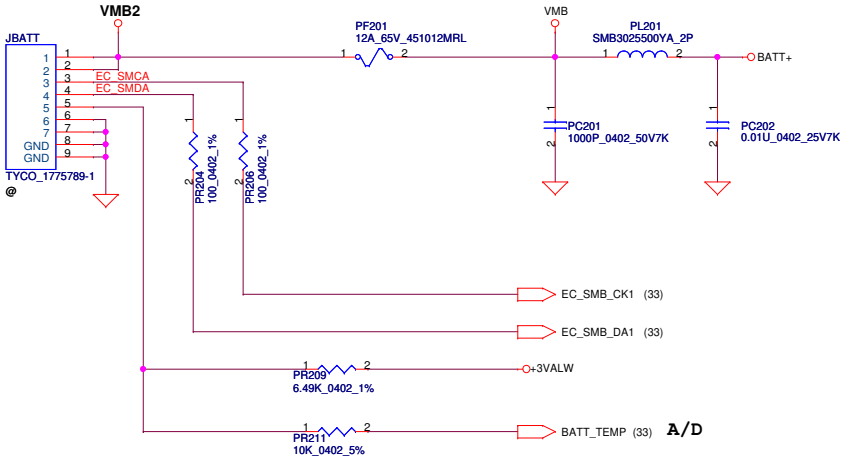
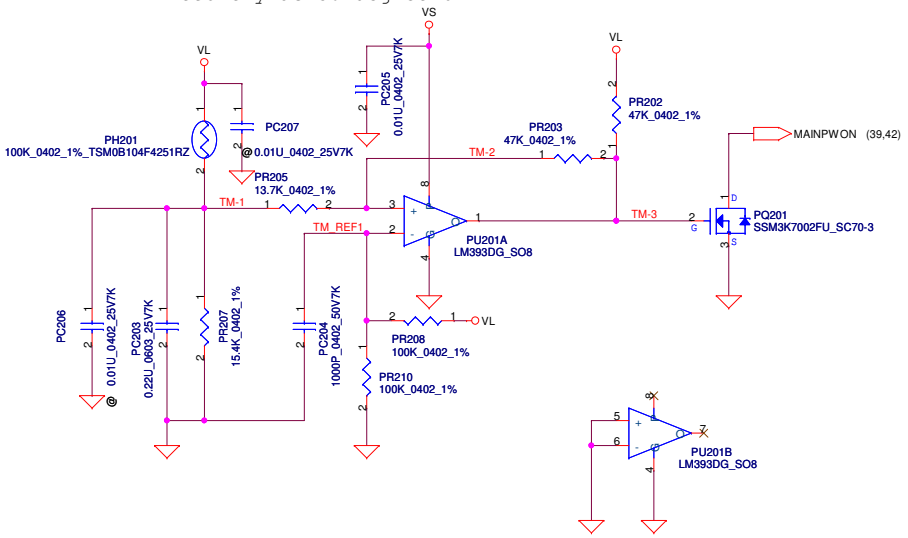
PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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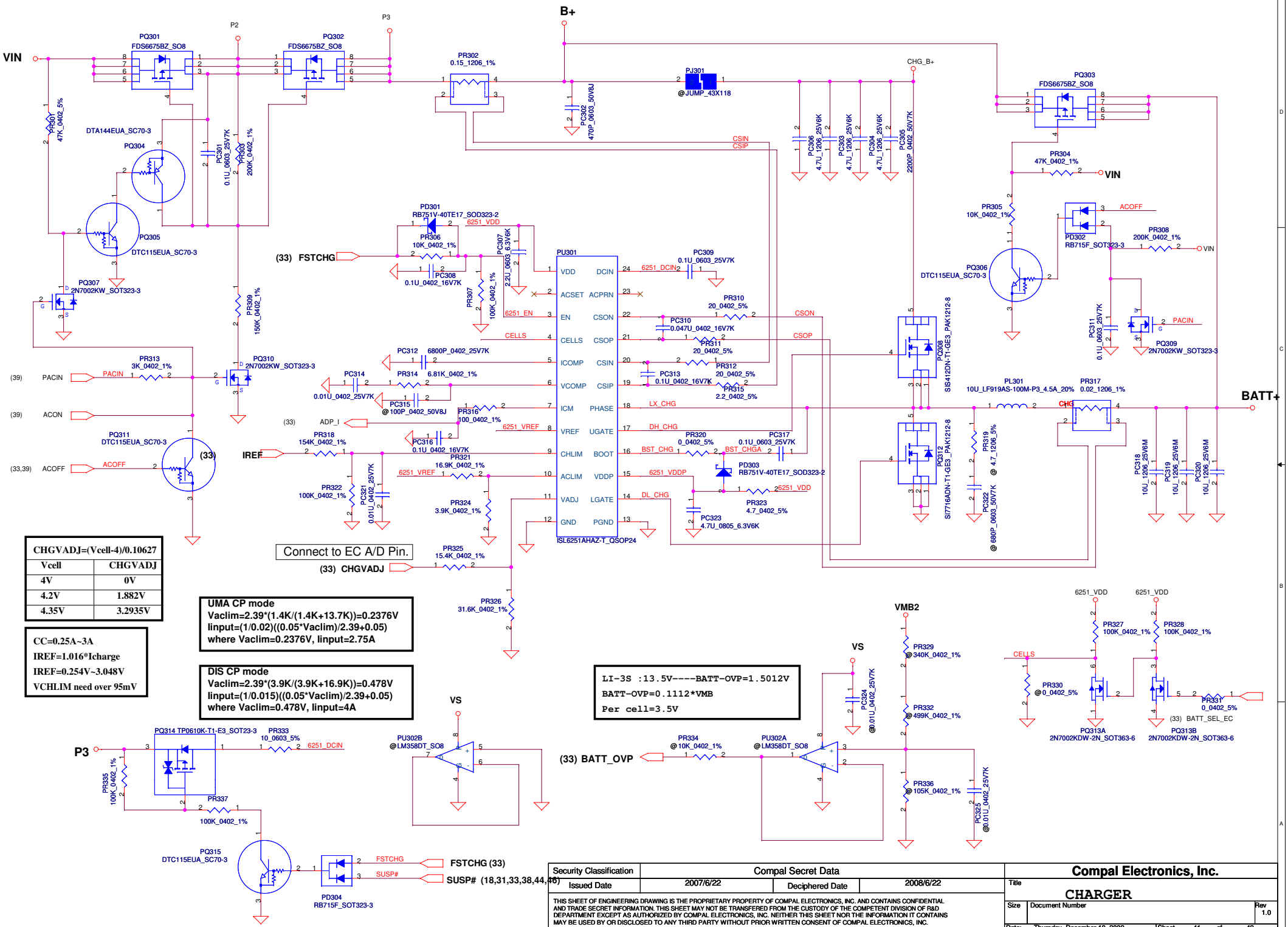
Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		1.0

Date: Thursday, December 10, 2009 | Sheet 40 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

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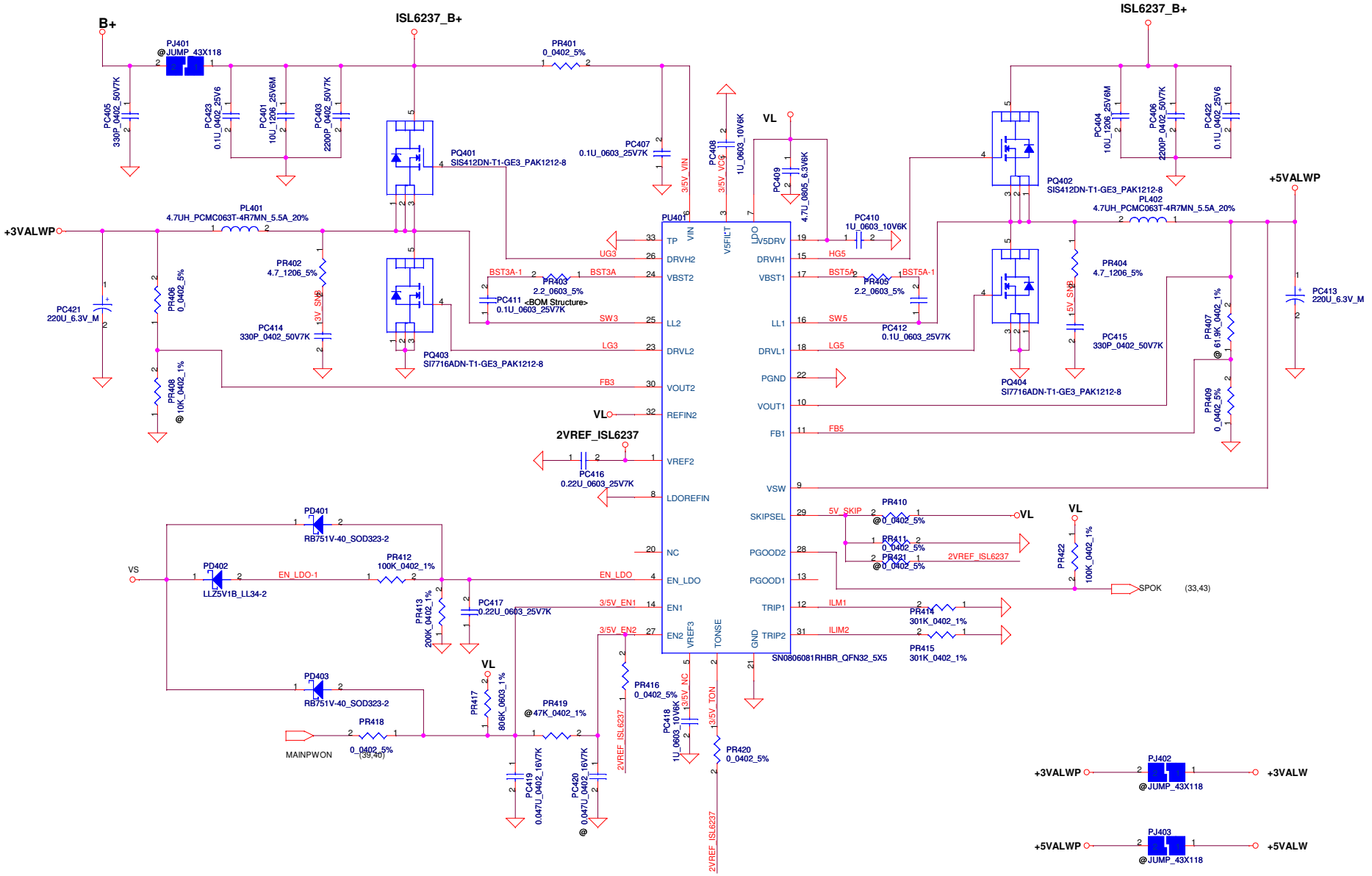
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 1.0

Date: Thursday, December 10, 2009 | Sheet 41 of 49



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		1.0

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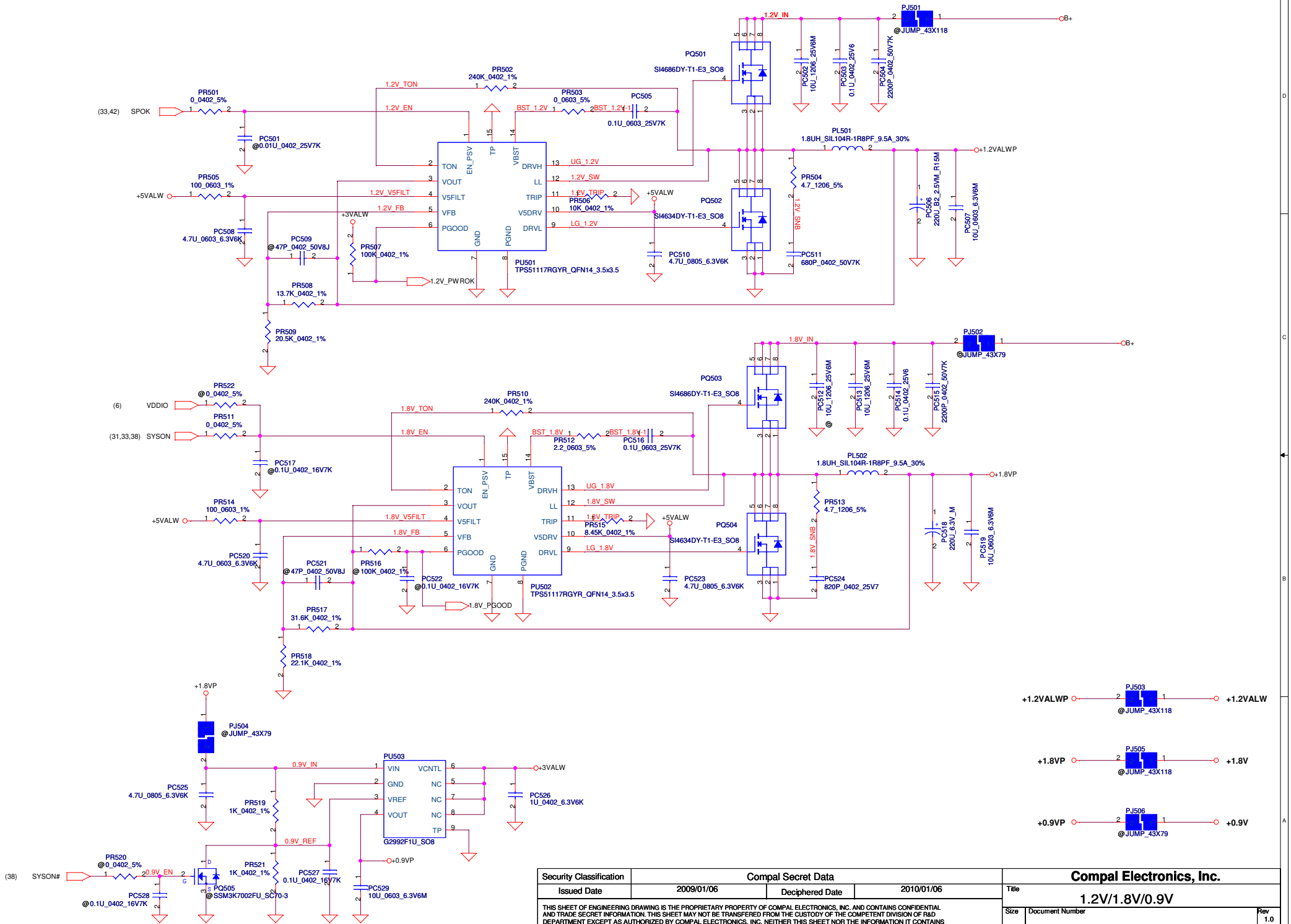

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Title: 1.2V/1.8V/0.9V

Size	Document Number	Rev
		1.0

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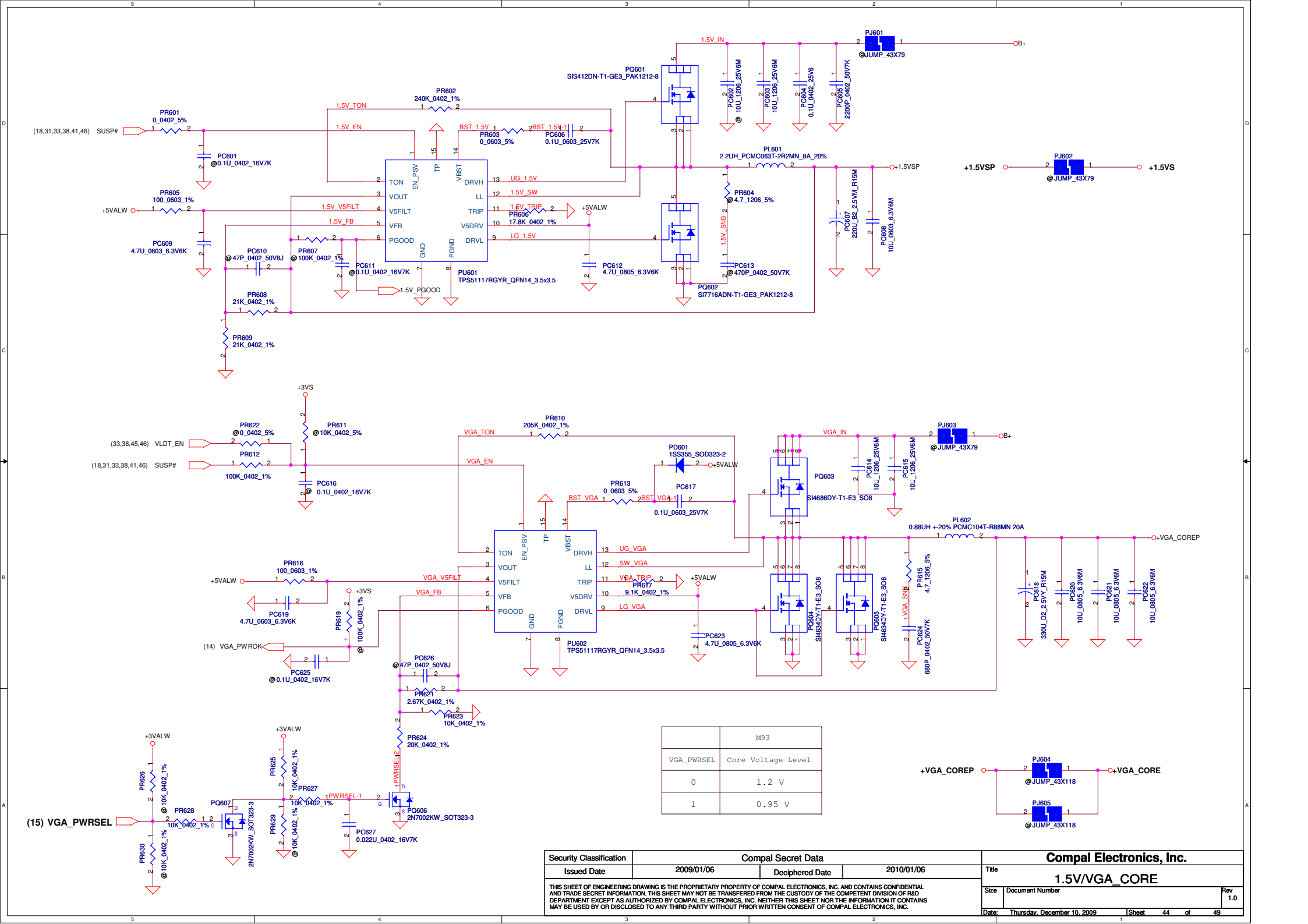

	M93
VGA_PWRSEL	Core Voltage Level
0	1.2 V
1	0.95 V

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Title: 1.5V/VGA_CORE

Size	Document Number	Rev
		1.0

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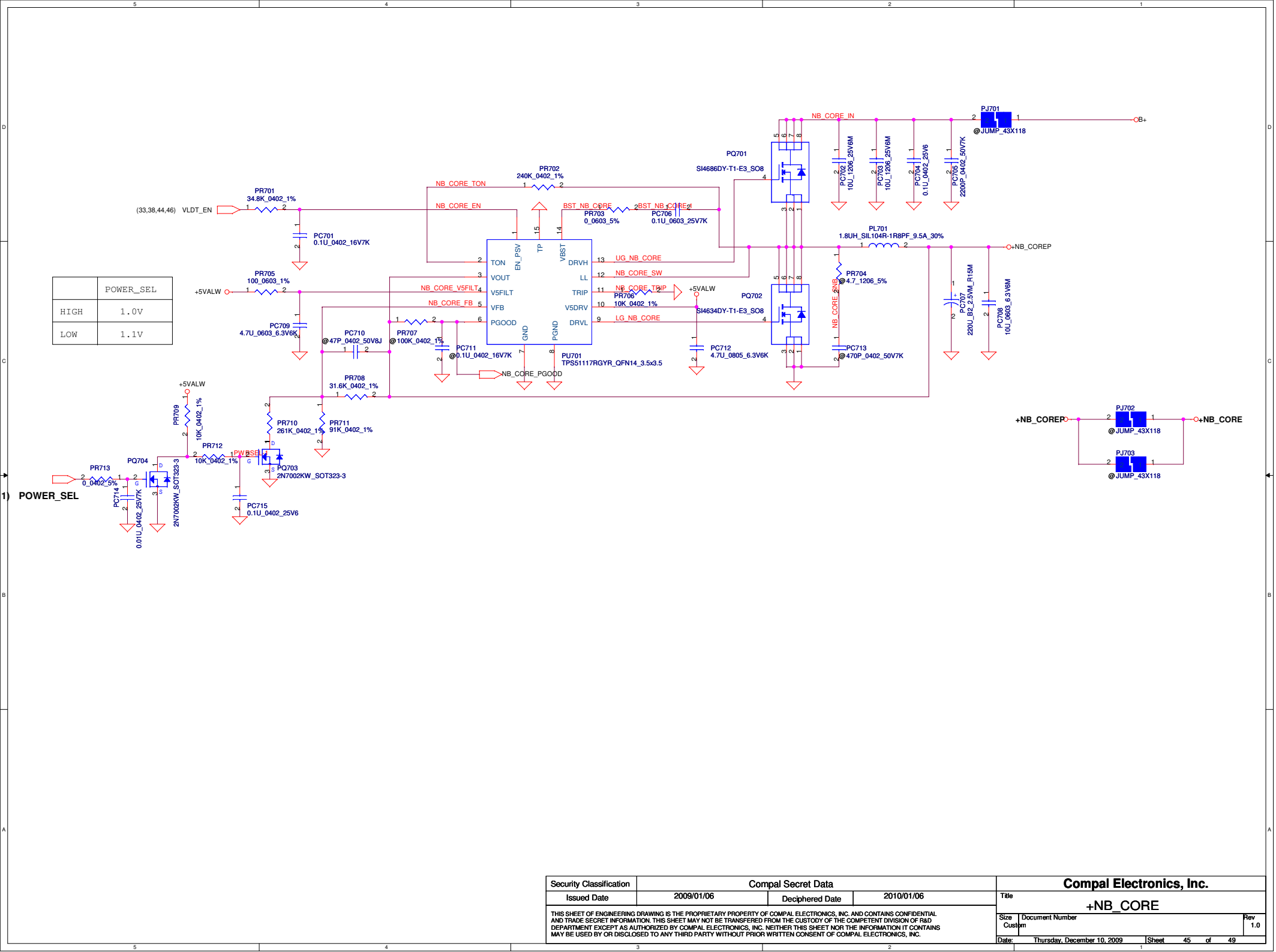

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Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Title: +NB_CORE

Size: Custom | Document Number | Rev: 1.0

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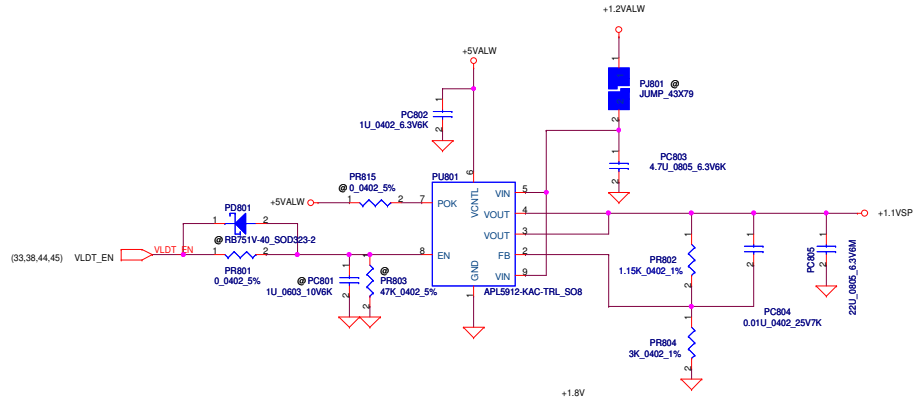

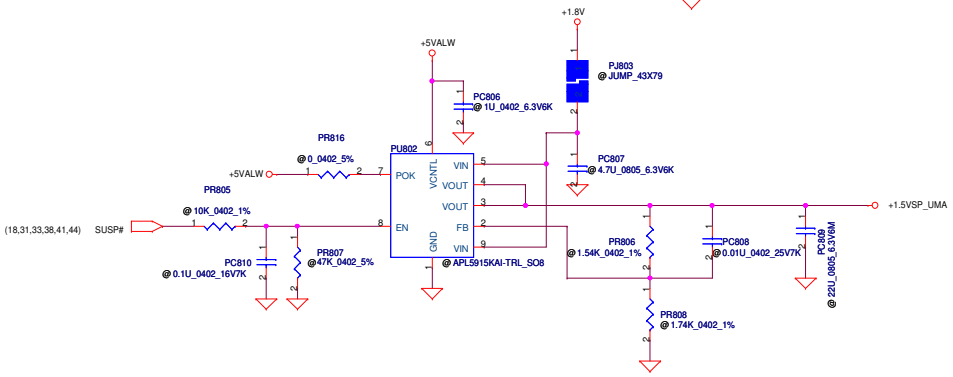

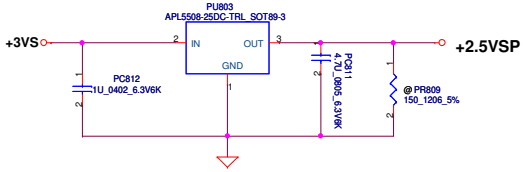

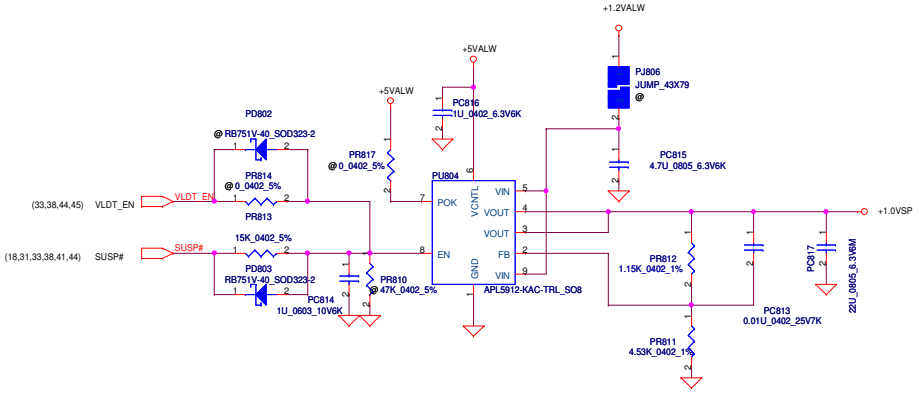

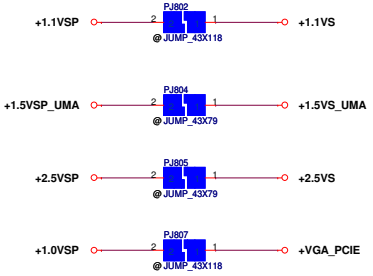

	Park	M93
VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K

Security Classification	Compal Secret Data		
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Title: 1.1V/1.5V/2.5V/1.0V

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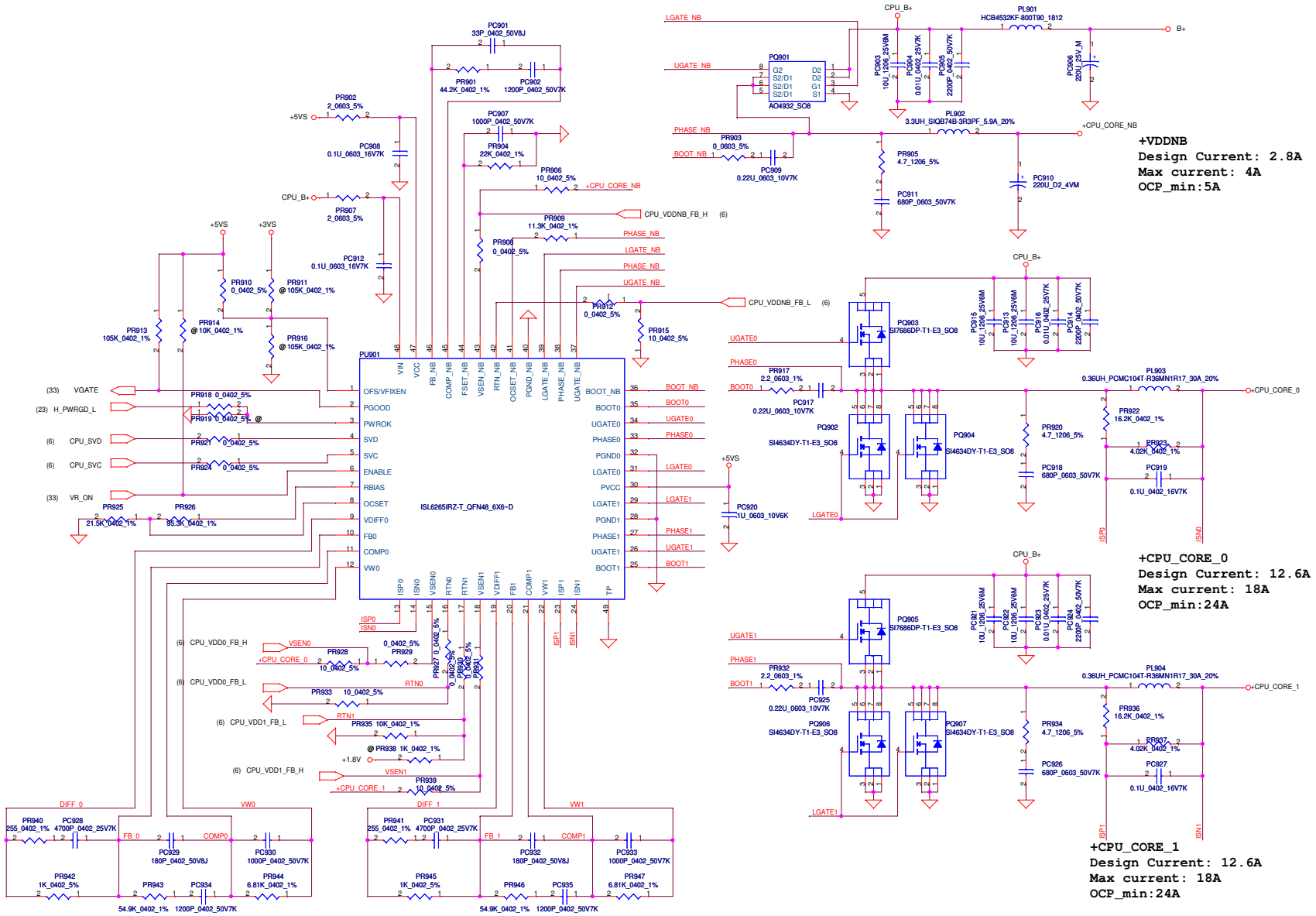

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Title: CPU_CORE			
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adjust power sequence for VGA_PCIE by HW request	P46	PR831=15K	2009.10.27	EVT
2	Change PC108 from 1000pF to 0.068uF for issue solution	P39	PC108=0.068uF	2009.11.17	PVT
3	Add snubber R & C and modify boost resistor for 1.8VP	P43	PR512=2.2 ohm;PR513=4.7 ohm;PC524=820pF	2009.11.17	PVT
4	Adjust power sequence	P45	PR701=34.8K,PC701=0.1uF Un-pop PR520,PQ505	2009.12.03	PVT
5					
6					
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14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2009/01/06

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1. change component AP2301GN to AO3413
2. remove R521, R517, R520 and R518, and reserve U49 , U50, R999, R1000, R1001 and R1002 for experiment Vari-bright function.
3. U6.18 add a pull up resistor R1005 and pull down resistor R1006 for check ENE KB926 version.
4. reserve R1003 and R1004 for Vari-bright test.
5. add J8, C1034, C1035, C1036, C1037, C1038 and C1039 for EMI request.
6. Change R583, R584, R585 and R586 Bead from SM010018110 to SM010022410.
7. reserve R1007 for EMI request.
8. Change C633, C640, C662, C948, C660 and C639 to 10pF for EMI rquest.

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

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Title: HW PIR

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B	LA-5972P	1.0

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